ALADDiN™-PRO II

M1621

North Bridge

Version 1.11

Please contact ALi applications deptment at 408-467-7456 to verify that all information is current before beginning a design using this datasheet.

M1621 : AGP, PCI and Memory Controller

Section 1.0 : Features

Processor Support

- Supports Pentium II™ processors. Host bus frequency can be either 66 or 100MHz
- 64 bit data bus and 32 bit addressing
- Optimum buffer design for CPU to memory write
- Optimum buffer design for CPU to memory read

Memory Support

- Supports FPM/EDO/Synchronized DRAMs
- Supports mixture of SDRAM, EDO and Fast Page Mode DRAMs
- Supports symmetrical and asymmetrical DRAM addressing
- Supports 4, 16, 64, 128, 256Mbit DRAMs
- Maximum memory size : 2GB
- Supports ECC, single bit error correct, and multiple bits error detection
- 64 bit data bus and additional 8 bit ECC protection
- Total of 8 RAS and 8 CAS lines available
- Supports 640K to 1MB address range shadowing
- x-1-1-1-1-1-1-1 back-to-back SDRAM page hit
- x-2-2-2-2-2-2-2 back-to-back EDO DRAM page hit
- CAS before RAS and self refresh for SDRAM
- CAS before RAS refresh for FPM and EDO DRAMs
- Pipelined DRAM cycle control with hidden pre-charge
- Supports optional SMI memory address remapping and protection
- Supports LVTTL signal level

Power Management

- Power plane design supports the following dark green power management function
  1. Power on Suspend
  2. Suspend to DRAM
  3. Suspend to Disk
  4. PCI bus CLKRUN
  5. Dynamic Clock Stop

AGP Support

- AGP specification 1.0 compliant
- 66 MHz PCI bus protocol support
- Supports up to 128 entries table look aside buffer for GART
- 1x/2x mode support
- 28 entries of request queue
- 32 QUAD words of read buffer
- 16 QUAD words of write buffer

PCI Bus Support

- Supports synchronous clock mode between processor bus and PCI bus
- 32-bit Address/Data PCI bus using PCI bus driver technology
- Supports up to 5 PCI masters excluding the M1621 and PCI-to-ISA bridge
- Parity protection on all PCI bus signals
- Fully supports PCI Configuration Space Enable (CSE) protocol
- Fully compliant with PCI Rev. 2.1
- Supports delayed transaction
- Dynamic memory prefetch algorithm and programmable post write flush algorithm
- Data Collection/Write assembly of line bursts
- Supports concurrent PCI bus burst transfer at zero wait-state
- More than 100 MBps data streaming for PCI bus to DRAM access with minimum latency

Packaging

- 476 pin BGA package

Others

- Supports NAND-TREE scan function

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1.1 Introduction

1.1.1 Aladdin Pro family

Aladdin Pro II is a new generation Pentium II system chip set which continuously supports cost effective PC solutions. Aladdin Pro II consists of two BGA packed chips, the M1621 and M1543C. However, the M1621 can also work with M1533, and M1543. The M1621 is an AGP, PCI and memory controller and a data path with multi-port buffers for data acceleration. Aladdin Pro II supports the Pentium II processor interface. The M1533, M1543 or M1543C is a PCI to ISA bus bridge, it provides full PCI and ISA compatible functions for different market applications.

1.1.2 PCI to ISA bridge

The M1533, M1543 and M1543C are all 328 pin BGA packaging design. The M1533 integrates power management unit, ACPI, deep green function, 2-channel dedicated Ultra-33 IDE master controller, 2-port USB controller, SMBus controller, and PS2 Keyboard/Mouse controller. The configuration of M1621/M1533 provides the user a high performance, efficient power management solution to meet notebook system requirements. Refer to the M1533 data sheet for detailed specifications.

The M1543 integrates ACPI, green function, 2-channel Ultra-33 IDE master controller, 2-port USB controller, SMBus controller, PS/2 keyboard/mouse controller and super I/O (floppy disk controller, 2 serial port/1 parallel port). In addition to the functions of the M1543 provided, the M1543C also integrates FIR functionality. The configuration of M1621/M1543 or M1621/M1543C provides the user a high performance, low cost solution for desktop systems. Refer to the M1543 or M1543C datasheet for detailed specifications.

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1.1.3 CPU interface

The M1621 supports the Intel Pentium II processor. The processor bus supports either 66 or 100 MHz.

1.1.4 Main memory size

The M1621 can support up to 2GB FPM, EDO, or SDRAM main memory. Refer to Memory Row Register to select DRAM type, row existence status, bank size, and timing information.

1.1.5 Throughput improvement

Aladdin Pro II employs various techniques to improve the memory and I/O throughput to match up with the advanced super-scalar, super-pipelined Pentium II processors. On the memory subsystem side, the processor data bus utilization is minimized. The pipelined memory cycle design helps hidden pre-charge latency and refresh cycles. Different configurations optimize the performance for a wide range of memory configurations. On the I/O subsystem side, deep data- in/out buffers shadow the latency for both PCI device initiated master reads and writes. Programmable data-in buffer management policy for post write cycles can be tuned to maximize the PCI to memory transfer rate for different memory configurations and PCI device characteristics.

1.1.6 ECC function over memory bus

Reliability and performance are the keys to a high quality PC design. They are also the major targets of the Aladdin Pro design for Pentium II processors. To reach this goal, 8 bit ECC protection over the 64 bit memory data bus is provided. The ECC can perform single bit error correction and multiple bit error detection.

1.1.7 PCI 2.1 Compliant

The M1621 is fully compliant to PCI 2.1 specification. With flexible PCI latency control, the M1621 can be adjusted to achieve the best system performance.

1.1.8 PCI arbiter

The M1621 integrates an enhanced PCI arbiter which executes a fair arbitration by using a PCI and CPU time slice mechanism. In addition to itself and the PCI to ISA bridge, the M1621 can support up to 5 PCI masters. According to the PCI specifications, it is possible to support more PCI masters depending on the layout arrangement, impedance load, and the quality of motherboard.

1.1.9 Power Management Design

To support the dark green power management function such as Power on Suspend, Suspend to DRAM, Suspend to Disk, PCI bus CLKRUN and Dynamic Clock Stop, three main power planes are implemented in the M1621. They are processor power plane, PCI and AGP power plane and main memory power plane. Each power plane has its own power source and is isolated from other power planes. To support the suspend mode, the main memory power plane is further divided into two sub-power planes. The power management design provides the desktop and notebook designs the most flexible green function available.

1.1.10 Accelerated Graphics Port

The M1621 supports the Accelerated Graphics Port (AGP or A.G.P.) 1.0 specifications. The AGP is a high performance, component level interconnect targeted at 3D graphical display applications. The AGP interface of the M1621 uses the 66MHz PCI specifications as an operational baseline and provides three significant performance enhancements to the PCI specifications. These enhancements are :

- Deeply pipelined memory read and write operations, fully hiding memory access latency.
- De-multiplexing of address and data on the bus, allowing almost 100% bus efficiency.
- AC timing for 133MHz data transfer rate, allowing almost 100% bus efficiency.

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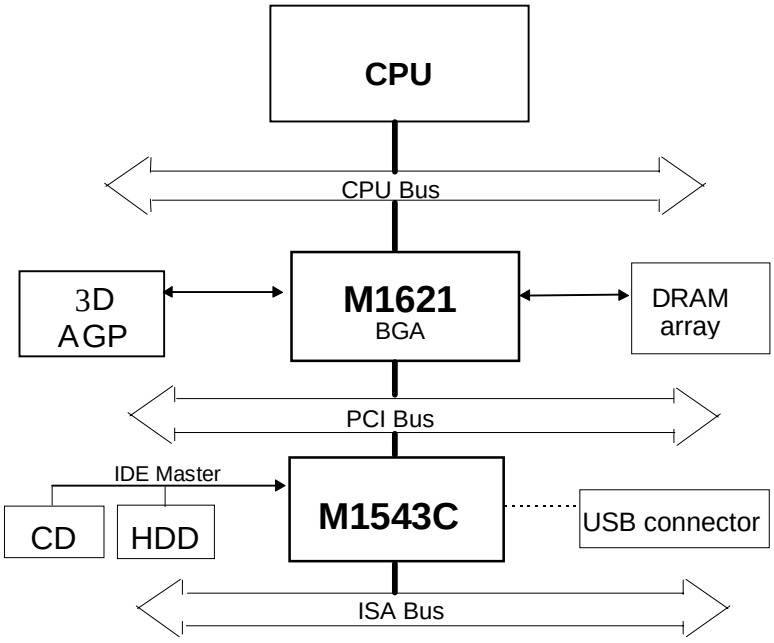
1.2 System Architecture



M1621/M1543C System Block Diagram

Section 2 : Pin Signal Description

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface. The "J" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level.

The following notations are used to describe the signal and type

I	Input pin
O	Output pin
O/tri	Output with tri-state pin
I/O	Bi-directional pin
PCI	PCI bus interface signals
AGP	AGP bus interface signals
LVTTL	Low voltage TTL compatible signals
GND	Ground

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2.1 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	AD 20	AD 21	AD 22	AD 24	AD 27	AD 31	PREQJ 1	PREQJ 3	HD 62	HD 58	HD 61	HD 60	HD 59	HD 51	HD 42	HD 36	HD 37	HD 28	HD 26	HD 24	HD 18	HD 13	HD 6	HD 4	GTL-REF 0	HD 1
B	AD 17	AD 18	AD 19	CBEJ 3	AD 26	AD 30	PGNTJ 0	PGNTJ 2	PGNTJ 4	HD 63	HD 55	GTL-REF 3	HD 48	HD 41	HD 44	HD 40	HD 38	HD 35	HD 30	HD 22	HD 21	HD 15	HD 9	HD 2	HD 0	HA 29
C	FRAM EJ	CBEJ 2	AD 16	AD 23	AD 25	AD 29	PREQJ 0	PREQJ 2	PREQJ 4	HCLK_SEL1	HD 56	HD 54	HD 46	GTL-REF 2	HD 45	HD 34	HD 32	HD 31	HD 25	HD 19	HD 20	HD 11	HD 8	HD 5	HD 3	HA 30
D	DEV SELJ	STOP J	PLOC KJ	PTRD YJ	IRDY J	AD 28	RES ETJ	PGNTJ 1	PGNTJ 3	Reserved	HD 50	HD 53	HD 52	HD 47	HD 39	HD 43	HD 33	HD 29	HD 27	HD 23	HD 17	HD 10	HD 14	CPU RSTJ	BREQJ0	HA 26
E	SERR J	PAR	CBEJ 1	AD 15	VCCP	VCCP	**GND**	**GND**	**GND**	**GND**	**GND**	HD 57	HD 49	VCCHP	VCCHP	**GND**	**GND**	**GND**	VCCHP	HD 16	**GND**	**GND**	HA 24	GTL-REF 1	HA 31	HA 28
F	AD 14	AD 13	AD 12	AD 11	AD 10	VCCP	VCCP	**GND**											VCCHP	**GND**	**GND**	**GND**	HD 7	HA 27	HA 22	HA 20
G	AD 9	AD 8	CBEJ 0	AD 7	**GND**	**GND**															**GND**	NC	HD 12	HA 21	HA 23	HA 25
H	AD 6	AD 5	AD 4	PHLD AJ	**GND**	**GND**															**GND**	HA 19	HA 15	HA 17	HA 18	HA 11
J	AD 3	AD 2	AD 1	PCI CLK	**GND**																	VCCHP	HA 16	HA 13	HA 12	HA 8
K	AD 0	GREQ J	GGNT J	PHLD J	RATI OJ																	**GND**	HA 14	HA 7	HA 10	BNRJ
L	ST 0	ST 1	ST 2	A REQJ	VCCP							GND	GND	GND	GND	GND	GND					H VDDA	HA 5	HA 3	HREQ J0	HREQ J1
M	RBF J	PIPE J	SBA 0	SBA 1	VCC5V							GND	GND	GND	GND	GND	GND					HA 6	HA 9	BPRI J	HA 4	HREQ J4
N	SBA 2	AGP-REF 2	SBA 3	SB-STB	SBA 4							GND	GND	GND	GND	GND	GND					TRDYJ	DEFE RJ	LOCKJ	DRDY J	HREQ J2
P	SBA 5	SBA 6	SBA 7	GAD 31	GAD 30							GND	GND	GND	GND	GND	GND					HGNDA	RSJ 0	HREQ J3	HITM J	HITJ
R	GAD 29	GAD 28	GAD 27	GAD 26	AVDDA							GND	GND	GND	GND	GND	GND					VCCP L3	RSJ 2	DBSY J	RSJ 1	ADSJ
T	GAD 25	GAD 24	AD-STB1	GCBE J3	AGNDA							GND	GND	GND	GND	GND	GND					HCLK	MD 1	TEST IN	MD 32	MD 0
U	GAD 23	GAD 22	GAD 21	GAD 20	VCC PL1																	**GND**	MD 3	MD 34	MD 2	MD 33
V	AGP-REF 1	GAD 19	GAD 18	GCLK O	**GND**																	VCCMP	MD 5	MD 36	MD 4	MD 35
W	GAD 17	GAD 16	GCBE J2	GCLK I	VDD PLL	**GND**															VCCMP	MD 39	MD 7	MD 38	MD 6	MD 37
Y	GFRA MEJ	GIRD YJ	GTRD YJ	GDEV SELJ	**GND**	VCCP															**GND**	MD 10	MD 41	MD 9	MD 40	MD 8
AA	GSTO PJ	GPAR	GCBE J1	GAD 15	VCCP	VCCP	**GND**	**GND**											VCCMP	VCCMP	**GND**	**GND**	MD 12	MD 43	MD 11	MD 42
AB	GAD 14	GAD 13	GAD 12	GAD 11	VCCP	**GND**	**GND**	**GND**	VCC_SP	VCC5V_SP	MD 50	MD 48	D VDDA	DGNDA	MA 6	DCLK I	VCCP L2	**GND**	SMI ACKJ	VCCMP	VCCMP	**GND**	MD 14	MD 45	MD 13	MD 44
AC	GAD 10	AGP-REF 0	GAD 9	GAD 8	MD 62	MD 60	MD 58	MD 56	MD 54	MD 52	MD 18	MD 16	CASJ 2	MA 11	MA 7	MA 2	CLK 32K	DCLK O	CKE	SUSPENDJ	REF ENV	CASJ 4	SCAS J2	MD 47	MD 15	MD 46
AD	AD-STB0	GAD 7	GAD 6	GCBE J0	MD 30	MD 28	MD 26	MD 24	MD 22	MD 20	MDP 7	MDP 2	CASJ 6	MA 12	MA 8	MA 3	MB 1	SRASJ 1	RASJ 0	RASJ 3	RASJ 6	CASJ 1	SCAS J1	MWE J1	MDP 5	MDP 0
AE	GAD 5	GAD4	GAD 3	MD 63	MD 61	MD 59	MD 57	MD 55	MD 53	MD 51	MD 49	MDP 6	CASJ 3	MA 13	MA 9	MA 4	MA 0	SRASJ 0	SRASJ 3	RASJ 2	RASJ 5	CASJ 5	SCAS J0	MWE J0	MWE J3	MDP 4
AF	GAD 2	GAD 1	GAD 0	MD 31	MD 29	MD 27	MD 25	MD 23	MD 21	MD 19	MD 17	MDP 3	CASJ 7	MA 14	MA 10	MA 5	MA 1	MB 0	SRASJ 2	RASJ 1	RASJ 4	RASJ 7	CASJ 0	SCAS J3	MWE J2	MDP 1
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**

M1621

Top View

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	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
AF	GAD 2	GAD 1	GAD 0	MD 31	MD 29	MD 27	MD 25	MD 23	MD 21	MD 19	MD 17	MDP 3	CASJ 7	MA 14	MA 10	MA 5	MA 1	MB 0	SRASJ 2	RASJ 1	RASJ 4	RASJ 7	CASJ 0	SCAS J3	MWE J2	MDP 1
AE	GAD 5	GAD4	GAD 3	MD 63	MD 61	MD 59	MD 57	MD 55	MD 53	MD 51	MD 49	MDP 6	CASJ 3	MA 13	MA 9	MA 4	MA 0	SRASJ 0	SRASJ 3	RASJ 2	RASJ 5	CASJ 5	SCAS J0	MWE J0	MWE J3	MDP 4
AD	AD-STB0	GAD 7	GAD 6	GCBE J0	MD 30	MD 28	MD 26	MD 24	MD 22	MD 20	MDP 7	MDP 2	CASJ 6	MA 12	MA 8	MA 3	MB 1	SRASJ 1	RASJ 0	RASJ 3	RASJ 6	CASJ 1	SCAS J1	MWE J1	MDP 5	MDP 0
AC	GAD 10	AGP-REF 0	GAD 9	GAD 8	MD 62	MD 60	MD 58	MD 56	MD 54	MD 52	MD 18	MD 16	CASJ 2	MA 11	MA 7	MA 2	CLK 32K	DCLK O	CKE	SUSPENDJ	REF ENV	CASJ 4	SCAS J2	MD 47	MD 15	MD 46
AB	GAD 14	GAD 13	GAD 12	GAD 11	VCCP	**GND**	**GND**	**GND**	VCC_SP	VCC5V_SP	MD 50	MD 48	D VDDA	DGNDA	MA 6	DCLK I	VCCP L2	**GND**	SMI ACKJ	VCCMP	VCCMP	**GND**	MD 14	MD 45	MD 13	MD 44
AA	GSTO PJ	GPAR	GCBE J1	GAD 15	VCCP	VCC P	**GND**	**GND**											VCCMP	VCCMP	**GND**	**GND**	MD 12	MD 43	MD 11	MD 42
Y	GFRA MEJ	GIRD YJ	GTRD YJ	GDEV SELJ	**GND**	VCC P							**M1621**								**GND**	MD 10	MD 41	MD 9	MD 40	MD 8
W	GAD 17	GAD 16	GCBE J2	GCLK I	VDD PLL	**GND**															VCCMP	MD 39	MD 7	MD 38	MD 6	MD 37
V	AGP-REF 1	GAD19	GAD18	GCLK O	**GND**																	VCCMP	MD 5	MD 36	MD 4	MD 35
U	GAD 23	GAD 22	GAD 21	GAD 20	VCC PL1																	**GND**	MD 3	MD 34	MD 2	MD 33
T	GAD 25	GAD 24	AD-STB1	GCBE J3	AGNDA						GND	GND	GND	GND	GND	GND						HCLK	MD 1	TEST IN	MD 32	MD 0
R	GAD 29	GAD 28	GAD 27	GAD 26	AVDDA						GND	GND	GND	GND	GND	GND						VCCP L3	RSJ 2	DBSY J	RSJ 1	ADSJ
P	SBA 5	SBA 6	SBA 7	GAD 31	GAD 30						GND	GND	GND	GND	GND	GND						HGNDA	RSJ 0	HREQ J3	HITM J	HITJ
N	SBA 2	AGP-REF 2	SBA 3	SB-STB	SBA 4						GND	GND	GND	GND	GND	GND						TRDYJ	DEFE RJ	LOCK J	DRDY J	HREQ J2
M	RBF J	PIPE J	SBA 0	SBA 1	VCC5V						GND	GND	GND	GND	GND	GND						HA 6	HA 9	BPRI J	HA 4	HREQ J4
L	ST 0	ST 1	ST 2	A REQJ	VCCP						GND	GND	GND	GND	GND	GND						H VDDA	HA 5	HA 3	HREQ J0	HREQ J1
K	AD 0	GREQ J	GGNT J	PHLD J	RATI OJ																	**GND**	HA 14	HA 7	HA 10	BNRJ
J	AD 3	AD 2	AD 1	PCI CLK	**GND**																	VCCHP	HA 16	HA 13	HA 12	HA 8
H	AD 6	AD 5	AD 4	PHLD AJ	**GND**	**GND**															**GND**	HA 19	HA 15	HA 17	HA 18	HA 11
G	AD 9	AD 8	CBEJ0	AD 7	**GND**	**GND**															**GND**	NC	HD 12	HA 21	HA 23	HA 25
F	AD 14	AD 13	AD 12	AD 11	AD 10	VCC P	VCCP	**GND**											VCCHP	**GND**	**GND**	**GND**	HD 7	HA 27	HA 22	HA 20
E	SERR J	PAR	CBEJ 1	AD 15	VCCP	VCCP	**GND**	**GND**	**GND**	**GND**	**GND**	HD 57	HD 49	VCCHP	VCCHP	**GND**	**GND**	**GND**	VCCHP	HD 16	**GND**	**GND**	HA 24	GTL-REF 1	HA 31	HA 28
D	DEV SELJ	STOP J	PLOC KJ	PTRD YJ	IRDY J	AD 28	RES ETJ	PGNTJ 1	PGNTJ 3	Reserved	HD 50	HD 53	HD 52	HD 47	HD 39	HD 43	HD 33	HD 29	HD 27	HD 23	HD 17	HD 10	HD 14	CPU RSTJ	BREQJ0	HA 26
C	FRAM EJ	CBEJ 2	AD 16	AD 23	AD 25	AD 29	PREQJ 0	PREQJ 2	PREQJ 4	HCLK_SEL1	HD 56	HD 54	HD 46	GTL-REF 2	HD 45	HD 34	HD 32	HD 31	HD 25	HD 19	HD 20	HD 11	HD 8	HD 5	HD 3	HA 30
B	AD 17	AD 18	AD 19	CBEJ 3	AD 26	AD 30	PGNTJ 0	PGNTJ 2	PGNTJ 4	HD 63	HD 55	GTL-REF 3	HD 48	HD 41	HD 44	HD 40	HD 38	HD 35	HD 30	HD 22	HD 21	HD 15	HD 9	HD 2	HD 0	HA 29
A	AD 20	AD 21	AD 22	AD 24	AD 27	AD 31	PREQJ 1	PREQJ 3	HD 62	HD 58	HD 61	HD 60	HD 59	HD 51	HD 42	HD 36	HD 37	HD 28	HD 26	HD 24	HD 18	HD 13	HD 6	HD 4	GTL-REF 0	HD 1
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**	**24**	**25**	**26**

Bottom View *(chip rotated top -bottom)*

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2.2 Pin Description Table :

Name	Type	Description
Host Interface :		
BPRIJ	I/O	**Priority Agent** bus request is issued by the high priority bus agent to acquire the request bus. The high priority agent will always be the next bus owner.
ADSJ	I/O	**Address Strobe**. The address strobe signal is asserted during the first cycle request phase and indicates that address and command signal are valid.
LOCKJ	I/O	**Lock**. The LOCKJ signal is asserted for indivisible sequence of transaction.
HA[31-3]	I/O	**Request Information**. HA[31-3] contain the transaction address on clock cycles with ADSJ asserted. Byte Enable, deferred ID, and additional transaction information are encoded on these lines during the cycle following ADSJ.
HREQJ[4-0]	I/O	**Request Type**. HREQJ[4-0] contain the command on the clock cycle with ADSJ asserted and data size/length information on the next cycle.
BREQJ[0]	I/O	**Bus Request 0**. Asserted at reset to set agent IDs on all processors.
BNRJ	I/O	**Block Next Request** is asserted by an agent to prevent the request bus owner from issuing further request.
HITJ	I/O	**Hit.** The bridge will assert HITJ and HITMJ together to extend the snoop window of a transaction targeting its PCI bus. HITJ indicates that a caching agent holds an unmodified version of the requested line.
HITMJ	I/O	**Hit Modified**. This signal indicates that a caching agent holds a modified version of the requested line and the agent assumes responsibility for providing the line. Also, driven in conjunction with HITMJ to extend the snoop window.
DEFERJ	I/O	**DEFERJ** is driven by addressed agent to indicate that the transaction cannot be guaranteed bus completion.
RSJ[2-0]	I/O	**RSJ[2-0]** encode the response to a request.
TRDYJ	I/O	**Target Ready** is driven by the target of the data to indicate that it is ready to receive data.
DRDYJ	I/O	**Data Ready** is driven by the data bus owner for each cycle that contains valid data. DRDYJ is asserted to indicate idle cycle during data phase.
DBSYJ	I/O	**DBSYJ** is asserted by the data bus owner to hold the data bus for the next cycle. DBSYJ is not asserted for single cycle transfer.
CPURSTJ	I/O	**CPU Bus Reset**. This signal is used to reset the CPU.
HD[63-0]	I/O	**Host Data**: These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.

Pin Description Table (continued) :

Name	Type	Description
DRAM Interface :		
MA[14-0]	I/O LVTTL	**Memory address**, multiplexed row and column memory address. These signals are connected to the address lines of all DRAMs. M1621 supports DRAM types from 256K to 256Mbits.
MB[1-0]	I/O LVTTL	**Memory address,** multiplexed row and column memory address for DRAM address bit 0,1. These two signals are the copy of MA[1-0].
RASJ[7-0]/ CSJ[7-0]	I/O LVTTL	**Row Address Strobe**. Indicates that address on MA[14-0] is the row address for EDO/FPM. There is one RASJ per memory row. When used with the SDRAM, the RASJ is used as chip select, CSJ, of SDRAM. There is one CSJ per memory row. When Index 82h bit4 is set to 1, RASJ[7:6] will become SDRAM CKE function.
CASJ[7-0]/ DQM[7-0]	I/O LVTTL	**Column Address Strobe**. Indicates that the address on MA[14-0] is the column address for EDO/FPM. There is one CASJ per memory row. When used with the SDRAM, this is the data mask, DQM, of SDRAM. There is one DQM per memory row.
SRASJ[3-0]	I/O LVTTL	**SDRAM, Row Address Strobe**. SRASJ[3-0] are of same function for sharing loading. They are used to connect SDRAM RASJ. There is one SRASJ per memory bank (two rows). When Index 82h bit4 is set to 1, SRASJ[3] will become SDRAM CKE function.
SCASJ[3-0]	I/O LVTTL	**SDRAM, Column Address Strobe**. SCASJ[3-0] are of same function for sharing loading. They are used to connect SDRAM CASJ. There is one SCASJ per memory bank (two rows). When Index 82h bit4 is set to 1, SCASJ[3] will become SDRAM CKE function.
REFENV	I/O LVTTL	**Refresh Envelope.** Indicates refresh period in 5V suspend mode. This signal will cover the whole period of refresh cycle.
MWEJ[3-0]	I/O LVTTL	**Write Enable**. Indicates that the current memory request is a write. MWEJ[3-0] are the same function to share loading. When Index 82h bit4 is set to 1, MWEJ[3] will become SDRAM CKE function.
MD[63-0]	I/O LVTTL	**Memory Data.** These signals are connected to the DRAM data bus. MD[63] is the most significant bit and MD[0] is the least significant bit.
MDP[7-0]	I/O LVTTL	**Memory ECC bits.** These signals are ECC bits of the DRAM data bus. MDP[7] is the most significant bit and MDP[0] is the least significant bit.

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Pin Description Table (continued) :

Name	Type	Description
AGP Addressing :		
PIPEJ	I	**Pipeline Request,** is asserted by master to indicate a full width request to be en-queued by the target. The master en-queues one request each rising edge of AGP clock while PIPEJ is asserted. When PIPEJ is de-asserted no new requests are en-queued across GAD bus.
SBA[7-0]	I/O	**Side band Address port,** provides an additional bus to pass address and command to the target from the master.
AGP Flow Control :		
RBFJ	I	**Read Buffer Full,** indicated if the master is ready to accept previously requested low priority read data or not. When RBFJ is asserted the arbiter is not allowed to initiate the return of low priority read data to the master.
ST[2-0]	I/O	**Status Bus,** provides information from the arbiter to a Master on what it may do. Refer to AGP spec. 1.0. for details.
AGP Clock List :		
AD_STB0	I/O	**AD Bus Strobe 0,** provides strobe timing for the 2x data transfer mode on the GAD[15-00]. The agent that is providing data drives this signal.
AD_STB1	I/O	**AD Bus Strobe 1,** provides strobe timing for the 2x data transfer mode on the GAD[31-16]. The agent that is providing data drives this signal.
SB_STB	I	**Side Band Strobe,** provides strobe timing for SBA[7:0] and is always driven by the AGP master.
AGP Semantics PCI Signals :		
GFRAMEJ	I/O	Not Used by AGP. It remains de-asserted by its own pull up resistor.
GIRDYJ	I/O	**GIRDYJ** indicates the AGP compliant master is ready to provide all write data for the current transaction. Once GIRDYJ is asserted for a write operation, the master is not allowed to insert wait states. The assertion of GIRDYJ for read, indicates that the master is ready to transfer a subsequent block of read data.
GTRDYJ	I/O	**GTRDYJ** indicates the AGP compliant target is ready to provide read data for the entire transaction or is ready to transfer a block of data, when the transfer requires more than four clocks to complete.
GSTOPJ	I/O	Not Used by AGP.
GDEVSELJ	I/O	Not Used by AGP.
GREQJ	I	**GREQJ** is used to request access to the bus to initiate a PCI or an AGP request.
GGNTJ	I/O	**GGNTJ** provides additional information on ST[2:0]. The additional information indicates that the master is the recipient of previously requested read data, it is to provide write data, for a previously en-queued write command or has been given permission to start a bus transaction.
GAD[31-0]	I/O	**GAD[31-0]** is the multiplexed address and data transfer bus. GAD[31] is the most significant bit and GAD[0] is the least significant bit.
GCBEJ[3-0]	I/O	**GCBEJ[3-0]** is the multiplexed command and byte enable bus. They also provide command information by the master when requests are being en-queued using PIPEJ. Provides valid byte information during AGP write transactions and is driven by the master.
GPAR	I/O	**GPAR** is parity bit on GAD[31:0] and GCBEJ[3:0].

Pin Description Table (continued) :

Name	Type	Description
PCI Interface :		
AD[31-0]	I/O	**PCI Address and Data.** These signals contain the address or data for PCI transaction, and connect to PCI bus.
CBEJ[3-0]	I/O	**PCI Bus Command and Byte Enables.** These signals contain command during address phase and byte enables during the data phase.
PTRDYJ	I/O	**PCI Target Ready.** This signal is asserted by the target to indicate that it is able to complete the current data transfer. A data transfer occurs if PTRDYJ and IRDYJ are asserted during the rising edge of PCICLK.
STOPJ	I/O	**STOPJ** is a request from the target to stop the current transaction.
PLOCKJ	I/O	**PCI Lock** is asserted by the agent requiring exclusive access to target.
DEVSELJ	I/O	**Device Select** is driven by the device that has decoded its address as the target of the current access.
PAR	I/O	**PCI Parity** is driven to even parity across AD[31-0] and CBEJ[3-0] by the master during address and write data phase. The target drives parity during read data phase.
IRDYJ	I/O	**PCI Initiator Ready** is asserted by the master to indicate that it is able to complete the current data transfer. A data transfer occurs if both PTRDYJ and IRDYJ are asserted during the rising edge of PCICLK.
FRAMEJ	I/O	**PCI Frame** is driven by a master to indicate the beginning and duration of a transaction.
SERRJ/ CLKRUNJ	I/O	**PCI System Error or PCI Clock Run.** When Index 5Ch bit0 is reset to 0, SERRJ function is selected. It is pulsed by the M1621 when the programmed error condition happened (like DRAM ECC checking). When Index 5Ch bit0 is set to 1, CLKRUNJ function is selected. CLKRUNJ is for stopping PCI clock during green function.
PCI Side band/Bridge Interface :		
PHLDJ	I	**PHLDJ: PCI Hold**, this signal comes from the standard bus bridge (South Bridge) to PCI arbiter to request the PCI bus.
PHLDAJ	I/O	**PHLDAJ: PCI Hold Acknowledge**: this signal is driven by the internal PCI arbiter to grant the PCI bus to the standard bus bridge (South Bridge).
PREQJ[4-0]	I	**Request**: PCI master requests for PCI slots or on board PCI device.
PGNTJ[4-0]	I/O	**Grant**: Permission is given to the PCI master to use PCI bus. These are inputs when the test mode is enabled. These pins are required to be external pull high.
HCLK_SEL1	I/O	**Hardware Setting.** Refer to hardware setup section 5.1.
AREQJ	I/O	**Any Request** represents bus request of any PCI bus masters. As output, this signal will be asserted by M1621 when any PREQJ[4:0] has been asserted. It is used to connect to south bridge to support ACPI function. As input, it is used to enable/disable host PLL. This signal wakes up system via south for the sake of ACPI circuitry there.

Pin Description Table (continued) :

Name	Type	Description
CLOCK :		
PCICLK	I LVTTL	**PCI Clock input**. The PCI state machine will be based on this clock. It comes from an external clock generator and must lag HCLK 1 ~ 4 ns.
HCLK	I LVTTL	**CPU Bus Clock**. This is the CPU bus clock input. When the Host PLL is disabled, the M1621 will use this clock for Host and DRAM state machines. When the Host PLL is enabled, this input clock will become the Host PLL reference clock.
DCLKO	I/O LVTTL	**DIMM Clock Output.** When DRAM PLL is enabled, M1621 will drive this clock out for Clock Buffer to generate DIMM clocks.
DCLKI	I/O LVTTL	**DRAM Side PLL's Reference Clock.** When DRAM PLL is enabled, this input signal must trace the DIMM clock to compensate the clock skew. Refer to the layout design guide.
GCLKO	I/O LVTTL	**AGP CLOCK Output.** When AGP PLL is enabled, the M1621 will drive this clock out for AGP slot. The M1621 will automatically determine if the Host bus frequency is 100 MHz or 66 MHz and generate the AGP clock. The M1621 AGP PLL will also generate an internal 133MHz frequency to enhance the 2X mode reliability.
GCLKI	I/O LVTTL	**AGP Side PLL's Reference Clock.** When AGP PLL is enabled, this clock input is for the PLL reference clock to compensate the layout delay. When AGP PLL is disabled, this clock input is for the AGP state machine clock. This input clock must delay Host clock for 1 ~ 4 ns due to drop specification.
CLK32K	I LVTTL	**32KHz Clock** for 5 volt suspend DRAM refresh. This signal must be pulled to a fixed value when the suspend feature is disabled.
SUSPENDJ	I/O LVTTL	**Suspend** request. This request is coming from a south bridge. When actively sampled, the M1621 will enter DRAM suspend refresh state. This signal must be pulled high when the suspend feature is disabled.
CKE	I/O LVTTL	**Clock enable** for SDRAM to perform a self refresh cycle. When Index 82h bit4 is set to 1, RASJ[7:6], SRASJ[3], SCASJ[3], and MWEJ[3] will become SDRAM CKE function also. This is the preferred configuration for a 3-DIMM layout.
Miscellaneous :		
AGP_REF[2-0]	I/O LVTTL	**AGP Bus Reference Voltage.** These inputs are used for the AGP pad reference input. System designer must provide a stable 0.4VCCP input for AGP pad to work reliably.
GTL_REF[3-0]	I/O LVTTL	**Host bus reference voltage.** GTL+ pad will use this voltage for the reference. System designer must provide a stable 1V input for GTL+ pad to work reliably.
SMIACKJ	I LVTTL	**Internal Test Mode.** This input is used to enable the internal NAND-tree scan function for Group 3, and 4. Refer to section 2.3 for more details. This pin must be pulled high for normal operation.
TESTIN	I LVTTL	**Internal Test Mode.** This input is used to enable the internal NAND-tree scan function for Group 1,2, 5, and 6. Refer to section 2.3 for more details. This pin must be pulled low for normal operation.
RESETJ	I LVTTL	**System Reset.** This reset is from the system. The M1621 will reset the whole state machine and generate CPURSTJ to the CPU.
RATIOJ	I/O LVTTL	**Ratio.** The M1621 will use this signal out to external circuitry to add the CPU configuration latch hold time. Refer to the reference circuit.

Pin Description Table (continued) :

Name	Type	Description
Power & Ground :		
VCC5V	P	Core power, 5V. No power is provided during suspend mode.
VCC5V_SP	P	Suspend core power, 5V. Provides necessary core power during suspend mode.
VCCP	P	PCI and AGP pad power, 3.3V.
VCCHP	P	Host pad power, 3.3V.
VCCMP	P	Memory pad power, 3.3V.
VCC_SP	P	Suspend pad power, 3.3V.
VCCPL1	P	AGP PLL pad power, 3.3V.
VCCPL2	P	Memory PLL pad power, 3.3V.
VCCPL3	P	Host PLL pad power, 3.3V.
VDDPLL	P	Digital pad power, 3.3V.
AVDDA	P	Analog power of AGP PLL, 3.3V.
DVDDA	P	Analog power of DRAM PLL, 3.3V.
HVDDA	P	Analog power of host PLL 3V.
AGNDA	G	Analog ground of AGP PLL.
DGNDA	G	Analog ground of memory PLL.
HGNDA	G	Analog ground of host PLL.
GND	G	Ground.

2.3 NAND-Tree Scan Functions:

Group 1 :

GCBEJ[0] ->	GAD[6] ->	GAD[11] ->	GAD[8] ->	GAD[0] ->	GAD[3] ->
GAD[1] ->	GAD[9] ->	GAD[15] ->	GAD[4] ->	GAD[2] ->	GAD[5] ->
GDEVSELJ ->	GAD[7] ->	AD_STB0 ->	GAD[10] ->	GAD[12] ->	GAD[13] ->
GAD[14] ->	GCBEJ[1] ->	GPAR ->	GCLKI ->	GCLKO ->	GSTOPJ ->
GTRDYJ ->	GIRDYJ ->	GFRAMEJ ->	GCBEJ[2] ->	GAD[16] ->	GAD[20] ->
GAD[17] ->	GAD[18] ->	GCBEJ[3] ->	GAD[19] ->	GAD[21] ->	GAD[22] ->
GAD[23] ->	AD_STB1->	GAD[26] ->	GAD[24] ->	GAD[25] ->	GAD[27] ->
GAD[31] ->	GAD[29] ->	GAD[28] ->	GAD[30] ->	SBA[7] ->	SBA[6] ->
SBA[5] ->	SBA[3] ->	SBA[2] ->	SBA[0] ->	PIPEJ ->	RBFJ ->
ST[2] ->	ST[1] ->	SBA[4] ->	ST[0] ->	SB_STB ->	GREQJ ->
SBA[1] ->	GGNTJ	----------	----------	----------	----------

Group 2 :

AD[0] ->	AD[2] ->	AD[1] ->	AD[3] ->	AD[6] ->	AD[5] ->
AREQJ ->	AD[9] ->	AD[4] ->	PHLDJ ->	AD[8] ->	RATIOJ ->
AD[7] ->	CBEJ[0] ->	AD[14] ->	AD[13] ->	AD[12] ->	AD[11] ->
PAR ->	SERRJ ->	PCICLK ->	CBEJ[1] ->	DEVSELJ ->	AD[15] ->
STOPJ ->	FRAMEJ ->	PLOCKJ ->	CBEJ[2] ->	AD[18] ->	AD[17] ->
AD[20] ->	PHLDAJ ->	AD[16] ->	AD[10] ->	PTRDYJ ->	AD[23] ->
AD[19] ->	AD[21] ->	AD[22] ->	IRDYJ ->	AD[25] ->	CBEJ[3] ->
AD[26] ->	AD[28] ->	AD[29] ->	AD[30] ->	AD[24] ->	AD[27] ->
RESETJ ->	PREQJ[0] ->	PGNTJ[0] ->	AD[31] ->	PGNTJ[1] ->	PREQJ[2] ->
PGNTJ[2] ->	PREQJ[1] ->	PREQJ[4] ->	PREQJ[3] ->	Reserved (D10) ->	HCLK_SEL1 ->
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Group 3 :

MD[63] ->	MD[62] ->	MD[31] ->	MD[60] ->	MD[30] ->	MD[61] ->
MD[28] ->	MD[29] ->	MD[58] ->	MD[59] ->	MD[27] ->	MD[26] ->
MD[57] ->	MD[56] ->	MD[16] ->	MD[25] ->	MD[24] ->	MD[50] ->
MD[55] ->	MD[23] ->	MD[54] ->	MD[53] ->	MD[22] ->	MD[21] ->
MD[52] ->	MD[19] ->	MD[51] ->	MD[20] ->	MD[18] ->	MD[17] ->
MD[49] ->	MD[48] ->	MDP[3] ->	MDP[7] ->	CASJ[2] ->	MDP[6] ->
MA[7] ->	MDP[2] ->	CASJ[3] ->	MA[14] ->	MA[13] ->	MA[11] ->
CASJ[6] ->	MA[10] ->	MA[2] ->	MA[9] ->	MA[6] ->	MA[5] ->
MA[4] ->	MA[1] ->	MB[0] ->	MA[12] ->	MA[0] ->	MA[8] ->
SRASJ[0] ->	SRASJ[2] ->	MA[3] ->	SRASJ[3] ->	RASJ[1] ->	RASJ[4] ->
CLK32K ->	CASJ[7] ->	----------	----------	----------	----------

Group 4 :

MD[32] ->	MD[0] ->	MD[3] ->	MD[34] ->	MD[1] ->	MD[2] ->
MD[33] ->	MD[36] ->	MD[4] ->	MD[5] ->	MD[35] ->	MD[38] ->
MD[6] ->	MD[37] ->	MD[7] ->	MD[9] ->	MD[40] ->	MD[8] ->
MD[41] ->	MD[42] ->	MD[39] ->	MD[43] ->	MD[11] ->	MD[12] ->
MD[10] ->	MD[14] ->	MD[45] ->	MD[44] ->	MD[13] ->	MD[47] ->
MD[46] ->	MD[15] ->	SMIACKJ ->	SCASJ[2] ->	MWEJ[1] ->	MDP[0] ->
MDP[5] ->	SCASJ[1] ->	CASJ[4] ->	MDP[4] ->	MWEJ[3] ->	MDP[1] ->
RASJ[6] ->	CASJ[1] ->	SUSPENDJ->	MWEJ[0] ->	CKE ->	MWEJ[2] ->
SCASJ[0] ->	RASJ[3] ->	SCASJ[3] ->	CASJ[5] ->	RASJ[0] ->	CASJ[0] ->
RASJ[5] ->	RASJ[7] ->	DCLKO ->	DCLKI ->	SRASJ[1] ->	SRASJ[2] ->
MB[1] ->	REFENV ->	----------	----------	----------	----------

Group 5 :

HCLK ->	ADSJ ->	RSJ[2] ->	RSJ[1] ->	DBSYJ ->	HITJ ->
HREQJ[2] ->	HITMJ ->	HREQJ[3] ->	RSJ[0] ->	HREQJ[4] ->	HREQJ[1] ->
DRDYJ ->	LOCKJ ->	DEFERJ ->	BNRJ ->	HA[4] ->	TRDYJ ->
BPRIJ ->	HA[8] ->	HA[9] ->	HREQJ[0] ->	HA[11] ->	HA[10] ->
HA[6] ->	HA[12] ->	HA[3] ->	HA[5] ->	HA[7] ->	HA[25] ->
HA[20] ->	HA[14] ->	HA[18] ->	HA[13] ->	HA[17] ->	HA[28] ->
HA[23] ->	HA[16] ->	HA[26] ->	HA[21] ->	HA[15] ->	HA[22] ->
HA[27] ->	HA[19] ->	HA[31] ->	HD[12] ->	HA[30] ->	HA[29] ->
HD[7] ->	HD[1] ->	HD[3] ->	HA[24] ->	BREQJ[0] ->	HD[0] ->
HD[5] ->	CPURSTJ ->	HD[2] ->	HD[4] ->	PGNTJ[4] ->	----------

Group 6 :

HD[8] ->	HD[6] ->	HD[14] ->	HD[10] ->	HD[9] ->	HD[11] ->
HD[17] ->	HD[13] ->	HD[15] ->	HD[20] ->	HD[23] ->	HD[16] ->
HD[21] ->	HD[19] ->	HD[27] ->	HD[18] ->	HD[22] ->	HD[25] ->
HD[24] ->	HD[29] ->	HD[30] ->	HD[31] ->	HD[26] ->	HD[33] ->
HD[35] ->	HD[28] ->	HD[32] ->	HD[37] ->	HD[38] ->	HD[43] ->
HD[34] ->	HD[36] ->	HD[40] ->	HD[39] ->	HD[45] ->	HD[42] ->
HD[44] ->	HD[47] ->	HD[51] ->	HD[41] ->	HD[59] ->	HD[46] ->
HD[48] ->	HD[49] ->	HD[60] ->	HD[52] ->	HD[54] ->	HD[61] ->
HD[57] ->	HD[53] ->	HD[58] ->	HD[55] ->	HD[56] ->	HD[50] ->
HD[62] ->	HD[63] ->	PGNTJ[3] ->	----------	----------	----------

2.4 Numerical Pin List :

Pin No.	Pin Name	Type
A1	AD20	I/O
A2	AD21	I/O
A3	AD22	I/O
A4	AD24	I/O
A5	AD27	I/O
A6	AD31	I/O
A7	PREQJ1	I
A8	PREQJ3	I
A9	HD62	I/O
A10	HD58	I/O
A11	HD61	I/O
A12	HD60	I/O
A13	HD59	I/O
A14	HD51	I/O
A15	HD42	I/O
A16	HD36	I/O
A17	HD37	I/O
A18	HD28	I/O
A19	HD26	I/O
A20	HD24	I/O
A21	HD18	I/O
A22	HD13	I/O
A23	HD6	I/O
A24	HD4	I/O
A25	GTL_REF0	I/O
A26	HD1	I/O
B1	AD17	I/O
B2	AD18	I/O
B3	AD19	I/O
B4	CBEJ3	I/O
B5	AD26	I/O
B6	AD30	I/O
B7	PGNTJ0	I/O
B8	PGNTJ2	I/O
B9	PGNTJ4	I/O
B10	HD63	I/O
B11	HD55	I/O
B12	GTL_REF3	I/O
B13	HD48	I/O
B14	HD41	I/O
B15	HD44	I/O
B16	HD40	I/O
B17	HD38	I/O
B18	HD35	I/O

Pin No.	Pin Name	Type
B19	HD30	I/O
B20	HD22	I/O
B21	HD21	I/O
B22	HD15	I/O
B23	HD9	I/O
B24	HD2	I/O
B25	HD0	I/O
B26	HA29	I/O
C1	FRAMEJ	I/O
C2	CBEJ2	I/O
C3	AD16	I/O
C4	AD23	I/O
C5	AD25	I/O
C6	AD29	I/O
C7	PREQJ0	I
C8	PREQJ2	I
C9	PREQJ4	I
C10	HCLK_SEL1	I/O
C11	HD56	I/O
C12	HD54	I/O
C13	HD46	I/O
C14	GTL_REF2	I/O
C15	HD45	I/O
C16	HD34	I/O
C17	HD32	I/O
C18	HD31	I/O
C19	HD25	I/O
C20	HD19	I/O
C21	HD20	I/O
C22	HD11	I/O
C23	HD8	I/O
C24	HD5	I/O
C25	HD3	I/O
C26	HA30	I/O
D1	DEVSELJ	I/O
D2	STOPJ	I/O
D3	PLOCKJ	I/O
D4	PTRDYJ	I/O
D5	IRDYJ	I/O
D6	AD28	I/O
D7	RESETJ	I/O
D8	PGNTJ1	I/O
D9	PGNTJ3	I/O
D10	RESERVED	

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Numerical Pin List : (continued)

Pin No.	Pin Name	Type
D11	HD50	I/O
D12	HD53	I/O
D13	HD52	I/O
D14	HD47	I/O
D15	HD39	I/O
D16	HD43	I/O
D17	HD33	I/O
D18	HD29	I/O
D19	HD27	I/O
D20	HD23	I/O
D21	HD17	I/O
D22	HD10	I/O
D23	HD14	I/O
D24	CPURSTJ	I/O
D25	BRJ0	I/O
D26	HA26	I/O
E1	SERRJ	I/O
E2	PAR	I/O
E3	CBEJ1	I/O
E4	AD15	I/O
E5	VCCP	P
E6	VCCP	P
E7	GND	P
E8	GND	P
E9	GND	P
E10	GND	P
E11	GND	P
E12	HD57	I/O
E13	HD49	I/O
E14	VCCHP	P
E15	VCCHP	P
E16	GND	P
E17	GND	P
E18	GND	P
E19	VCCHP	P
E20	HD16	I/O
E21	GND	P
E22	GND	P
E23	HA24	I/O
E24	GTL_REF1	I/O
E25	HA31	I/O
E26	HA28	I/O
F1	AD14	I/O
F2	AD13	I/O

Pin No.	Pin Name	Type
F3	AD12	I/O
F4	AD11	I/O
F5	AD10	I/O
F6	VCCP	P
F7	VCCP	P
F8	GND	P
F19	VCCHP	P
F20	GND	P
F21	GND	P
F22	GND	P
F23	HD7	I/O
F24	HA27	I/O
F25	HA22	I/O
F26	HA20	I/O
G1	AD9	I/O
G2	AD8	I/O
G3	CBEJ0	I/O
G4	AD7	I/O
G5	GND	P
G6	GND	P
G21	GND	P
G22	NC	
G23	HD12	I/O
G24	HA21	I/O
G25	HA23	I/O
G26	HA25	I/O
H1	AD6	I/O
H2	AD5	I/O
H3	AD4	I/O
H4	PHLDAJ	I/O
H5	GND	P
H6	GND	P
H21	GND	P
H22	HA19	I/O
H23	HA15	I/O
H24	HA17	I/O
H25	HA18	I/O
H26	HA11	I/O
J1	AD3	I/O
J2	AD2	I/O
J3	AD1	I/O
J4	PCICLK	I
J5	GND	P
J22	VCCHP	P

Numerical Pin List : (continued)

Pin No.	Pin Name	Type
J23	HA16	I/O
J24	HA13	I/O
J25	HA12	I/O
J26	HA8	I/O
K1	AD0	I/O
K2	GREQJ	I
K3	GGNTJ	I/O
K4	PHLDJ	I
K5	RATIOJ	I/O
K22	GND	P
K23	HA14	I/O
K24	HA7	I/O
K25	HA10	I/O
K26	BNRJ	I/O
L1	ST0	I/O
L2	ST1	I/O
L3	ST2	I/O
L4	AREQJ	I/O
L5	VCCP	P
L11	GND	P
L12	GND	P
L13	GND	P
L14	GND	P
L15	GND	P
L16	GND	P
L22	H VDDA	P
L23	HA5	I/O
L24	HA3	I/O
L25	HREQJ0	I/O
L26	HREQJ1	I/O
M1	RBFJ	I
M2	PIPEJ	I
M3	SBA0	I/O
M4	SBA1	I/O
M5	VCC5V	P
M11	GND	P
M12	GND	P
M13	GND	P
M14	GND	P
M15	GND	P
M16	GND	P
M22	HA6	I/O
M23	HA9	I/O
M24	BPRIJ	I/O
M25	HA4	I/O
M26	HREQJ4	I/O
N1	SBA2	I/O
N2	AGP_REF2	I/O
N3	SBA3	I/O
N4	SB_STB	I
N5	SBA4	I/O
N11	GND	P
N12	GND	P
N13	GND	P
N14	GND	P
N15	GND	P
N16	GND	P
N22	TRDYJ	I/O
N23	DEFERJ	I/O
N24	LOCKJ	I/O
N25	DRDYJ	I/O
N26	HREQJ2	I/O
P1	SBA5	I/O
P2	SBA6	I/O
P3	SBA7	I/O
P4	GAD31	I/O
P5	GAD30	I/O
P11	GND	P
P12	GND	P
P13	GND	P
P14	GND	P
P15	GND	P
P16	GND	P
P22	HGNDA	P
P23	RSJ0	I/O
P24	HREQJ3	I/O
P25	HITMJ	I/O
P26	HITJ	I/O
R1	GAD29	I/O
R2	GAD28	I/O
R3	GAD27	I/O
R4	GAD26	I/O
R5	AVDDA	P
R11	GND	P
R12	GND	P
R13	GND	P
R14	GND	P
R15	GND	P

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Numerical Pin List : (continued)

Pin No.	Pin Name	Type
R16	GND	P
R22	VCCPL3	P
R23	RSJ2	I/O
R24	DBSYJ	I/O
R25	RSJ1	I/O
R26	ADSJ	I/O
T1	GAD25	I/O
T2	GAD24	I/O
T3	AD_STB1	I/O
T4	GCBEJ3	I/O
T5	AGNDA	P
T11	GND	P
T12	GND	P
T13	GND	P
T14	GND	P
T15	GND	P
T16	GND	P
T22	HCLK	I/O
T23	MD1	I/O
T24	TESTIN	I
T25	MD32	I/O
T26	MD0	I/O
U1	GAD23	I/O
U2	GAD22	I/O
U3	GAD21	I/O
U4	GAD20	I/O
U5	VCCPL1	P
U22	GND	P
U23	MD3	I/O
U24	MD34	I/O
U25	MD2	I/O
U26	MD33	I/O
V1	AGP_REF1	I/O
V2	GAD19	I/O
V3	GAD18	I/O
V4	GCLKO	I/O
V5	GND	P
V22	VCCMP	P
V23	MD5	I/O
V24	MD36	I/O
V25	MD4	I/O
V26	MD35	I/O
W1	GAD17	I/O
W2	GAD16	I/O
W3	GCBEJ2	I/O
W4	GCLKI	I
W5	VDDPLL	P
W6	GND	P
W21	VCCMP	P
W22	MD39	I/O
W23	MD7	I/O
W24	MD38	I/O
W25	MD6	I/O
W26	MD37	I/O
Y1	GFRAMEJ	I/O
Y2	GIRDYJ	I
Y3	GTRDYJ	I/O
Y4	GDEVSELJ	I
Y5	GND	P
Y6	VCCP	P
Y21	GND	P
Y22	MD10	I/O
Y23	MD41	I/O
Y24	MD9	I/O
Y25	MD40	I/O
Y26	MD8	I/O
AA1	GSTOPJ	I/O
AA2	GPAR	I/O
AA3	GCBEJ1	I/O
AA4	GAD15	I/O
AA5	VCCP	P
AA6	VCCP	P
AA7	GND	P
AA8	GND	P
AA19	VCCMP	P
AA20	VCCMP	P
AA21	GND	P
AA22	GND	P
AA23	MD12	I/O
AA24	MD43	I/O
AA25	MD11	I/O
AA26	MD42	I/O
AB1	GAD14	I/O
AB2	GAD13	I/O
AB3	GAD12	I/O
AB4	GAD11	I/O
AB5	VCCP	P
AB6	GND	P

Numerical Pin List : (continued)

Pin No.	Pin Name	Type
AB7	GND	P
AB8	GND	P
AB9	VCC_SP	P
AB10	VCC5V_SP	P
AB11	MD50	I/O
AB12	MD48	I/O
AB13	DVDDA	P
AB14	DGNDA	P
AB15	MA6	I/O
AB16	DCLKI	I
AB17	VCCPL2	P
AB18	GND	P
AB19	SMIACKJ	I
AB20	VCCMP	P
AB21	VCCMP	P
AB22	GND	P
AB23	MD14	I/O
AB24	MD45	I/O
AB25	MD13	I/O
AB26	MD44	I/O
AC1	GAD10	I/O
AC2	AGP_REF0	I/O
AC3	GAD9	I/O
AC4	GAD8	I/O
AC5	MD62	I/O
AC6	MD60	I/O
AC7	MD58	I/O
AC8	MD56	I/O
AC9	MD54	I/O
AC10	MD52	I/O
AC11	MD18	I/O
AC12	MD16	I/O
AC13	CASJ2	I/O
AC14	MA11	I/O
AC15	MA7	I/O
AC16	MA2	I/O
AC17	CLK32K	I
AC18	DCLKO	I/O
AC19	CKE	I/O
AC20	SUSPENDJ	I
AC21	REFENV	I/O
AC22	CASJ4	I/O
AC23	SCASJ2	I/O
AC24	MD47	I/O

Pin No.	Pin Name	Type
AC25	MD15	I/O
AC26	MD46	I/O
AD1	AD_STB0	I/O
AD2	GAD7	I/O
AD3	GAD6	I/O
AD4	GCBEJ0	I/O
AD5	MD30	I/O
AD6	MD28	I/O
AD7	MD26	I/O
AD8	MD24	I/O
AD9	MD22	I/O
AD10	MD20	I/O
AD11	MPD7	I/O
AD12	MPD2	I/O
AD13	CASJ6	I/O
AD14	MA12	I/O
AD15	MA8	I/O
AD16	MA3	I/O
AD17	MB1	I/O
AD18	SRASJ1	I/O
AD19	RASJ0	I/O
AD20	RASJ3	I/O
AD21	RASJ6	I/O
AD22	CASJ1	I/O
AD23	SCASJ1	I/O
AD24	MWEJ1	I/O
AD25	MPD5	I/O
AD26	MPD0	I/O
AE1	GAD5	I/O
AE2	GAD4	I/O
AE3	GAD3	I/O
AE4	MD63	I/O
AE5	MD61	I/O
AE6	MD59	I/O
AE7	MD57	I/O
AE8	MD55	I/O
AE9	MD53	I/O
AE10	MD51	I/O
AE11	MD49	I/O
AE12	MPD6	I/O
AE13	CASJ3	I/O
AE14	MA13	I/O
AE15	MA9	I/O
AE16	MA4	I/O

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Numerical Pin List : (continued)

Pin No.	Pin Name	Type
AE17	MA0	I/O
AE18	SRASJ0	I/O
AE19	SRASJ3	I/O
AE20	RASJ2	I/O
AE21	RASJ5	I/O
AE22	CASJ5	I/O
AE23	SCASJ0	I/O
AE24	MWEJ0	I/O
AE25	MWEJ3	I/O
AE26	MPD4	I/O
AF1	GAD2	I/O
AF2	GAD1	I/O
AF3	GAD0	I/O
AF4	MD31	I/O
AF5	MD29	I/O
AF6	MD27	I/O
AF7	MD25	I/O
AF8	MD23	I/O
AF9	MD21	I/O
AF10	MD19	I/O
AF11	MD17	I/O
AF12	MPD3	I/O
AF13	CASJ7	I/O
AF14	MA14	I/O
AF15	MA10	I/O
AF16	MA5	I/O
AF17	MA1	I/O
AF18	MB0	I/O
AF19	SRASJ2	I/O
AF20	RASJ1	I/O
AF21	RASJ4	I/O
AF22	RASJ7	I/O
AF23	CASJ0	I/O
AF24	SCASJ3	I/O
AF25	MWEJ2	I/O
AF26	MPD1	I/O

2.5 Alphabetical Pin List :

Pin No.	Pin Name	Type
AD1	AD_STB0	I/O
T3	AD_STB1	I/O
K1	AD0	I/O
J3	AD1	I/O
F5	AD10	I/O
F4	AD11	I/O
F3	AD12	I/O
F2	AD13	I/O
F1	AD14	I/O
E4	AD15	I/O
C3	AD16	I/O
B1	AD17	I/O
B2	AD18	I/O
B3	AD19	I/O
J2	AD2	I/O
A1	AD20	I/O
A2	AD21	I/O
A3	AD22	I/O
C4	AD23	I/O
A4	AD24	I/O
C5	AD25	I/O
B5	AD26	I/O
A5	AD27	I/O
D6	AD28	I/O
C6	AD29	I/O
J1	AD3	I/O
B6	AD30	I/O
A6	AD31	I/O
H3	AD4	I/O
H2	AD5	I/O
H1	AD6	I/O
G4	AD7	I/O
G2	AD8	I/O
G1	AD9	I/O
R26	ADSJ	I/O
T5	AGNDA	P

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Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
AC2	AGP_REF0	I/O
V1	AGP_REF1	I/O
N2	AGP_REF2	I/O
L4	AREQJ	I/O
R5	AVDDA	P
K26	BNRJ	I/O
M24	BPRIJ	I/O
D25	BRJ0	I/O
AF23	CASJ0	I/O
AD22	CASJ1	I/O
AC13	CASJ2	I/O
AE13	CASJ3	I/O
AC22	CASJ4	I/O
AE22	CASJ5	I/O
AD13	CASJ6	I/O
AF13	CASJ7	I/O
G3	CBEJ0	I/O
E3	CBEJ1	I/O
C2	CBEJ2	I/O
B4	CBEJ3	I/O
AC19	CKE	I/O
AC17	CLK32K	I
D24	CPURSTJ	I/O
R24	DBSYJ	I/O
AB16	DCLKI	I
AC18	DCLKO	I/O
N23	DEFERJ	I/O
D1	DEVSELJ	I/O
AB14	DGNDA	P
N25	DRDYJ	I/O
AB13	DVDDA	P
C1	FRAMEJ	I/O
AF3	GAD0	I/O
AF2	GAD1	I/O
AC1	GAD10	I/O
AB4	GAD11	I/O
AB3	GAD12	I/O
AB2	GAD13	I/O
AB1	GAD14	I/O
AA4	GAD15	I/O
W2	GAD16	I/O
W1	GAD17	I/O
V3	GAD18	I/O
V2	GAD19	I/O
AF1	GAD2	I/O
U4	GAD20	I/O
U3	GAD21	I/O
U2	GAD22	I/O
U1	GAD23	I/O
T2	GAD24	I/O
T1	GAD25	I/O
R4	GAD26	I/O
R3	GAD27	I/O
R2	GAD28	I/O
R1	GAD29	I/O
AE3	GAD3	I/O
P5	GAD30	I/O
P4	GAD31	I/O
AE2	GAD4	I/O
AE1	GAD5	I/O
AD3	GAD6	I/O
AD2	GAD7	I/O
AC4	GAD8	I/O
AC3	GAD9	I/O
AD4	GCBEJ0	I/O
AA3	GCBEJ1	I/O
W3	GCBEJ2	I/O
T4	GCBEJ3	I/O
W4	GCLKI	I
V4	GCLKO	I/O
Y4	GDEVSELJ	I
Y1	GFRAMEJ	I/O
K3	GGNTJ	I/O
Y2	GIRDYJ	I

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Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
AA21	GND	P
AA22	GND	P
AA7	GND	P
AA8	GND	P
AB18	GND	P
AB22	GND	P
AB6	GND	P
AB7	GND	P
AB8	GND	P
E10	GND	P
E11	GND	P
E16	GND	P
E17	GND	P
E18	GND	P
E21	GND	P
E22	GND	P
E7	GND	P
E8	GND	P
E9	GND	P
F20	GND	P
F21	GND	P
F22	GND	P
F8	GND	P
G21	GND	P
G5	GND	P
G6	GND	P
H21	GND	P
H5	GND	P
H6	GND	P
J5	GND	P
K22	GND	P
L11	GND	P
L12	GND	P
L13	GND	P
L14	GND	P
L15	GND	P
L16	GND	P
M11	GND	P
M12	GND	P
M13	GND	P
M14	GND	P
M15	GND	P
M16	GND	P
N11	GND	P
N12	GND	P
N13	GND	P
N14	GND	P
N15	GND	P
N16	GND	P
P11	GND	P
P12	GND	P
P13	GND	P
P14	GND	P
P15	GND	P
P16	GND	P
R11	GND	P
R12	GND	P
R13	GND	P
R14	GND	P
R15	GND	P
R16	GND	P
T11	GND	P
T12	GND	P
T13	GND	P
T14	GND	P
T15	GND	P
T16	GND	P
U22	GND	P
V5	GND	P
W6	GND	P
Y21	GND	P
Y5	GND	P
AA2	GPAR	I/O
K2	GREQJ	I

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Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
AA1	GSTOPJ	I/O
A25	GTL_REF0	I/O
E24	GTL_REF1	I/O
C14	GTL_REF2	I/O
B12	GTL_REF3	I/O
Y3	GTRDYJ	I/O
K25	HA10	I/O
H26	HA11	I/O
J25	HA12	I/O
J24	HA13	I/O
K23	HA14	I/O
H23	HA15	I/O
J23	HA16	I/O
H24	HA17	I/O
H25	HA18	I/O
H22	HA19	I/O
F26	HA20	I/O
G24	HA21	I/O
F25	HA22	I/O
G25	HA23	I/O
E23	HA24	I/O
G26	HA25	I/O
D26	HA26	I/O
F24	HA27	I/O
E26	HA28	I/O
B26	HA29	I/O
L24	HA3	I/O
C26	HA30	I/O
E25	HA31	I/O
M25	HA4	I/O
L23	HA5	I/O
M22	HA6	I/O
K24	HA7	I/O
J26	HA8	I/O
M23	HA9	I/O
T22	HCLK	I/O
C10	HCLK_SEL1	I/O

Pin No.	Pin Name	Type
B25	HD0	I/O
A26	HD1	I/O
D22	HD10	I/O
C22	HD11	I/O
G23	HD12	I/O
A22	HD13	I/O
D23	HD14	I/O
B22	HD15	I/O
E20	HD16	I/O
D21	HD17	I/O
A21	HD18	I/O
C20	HD19	I/O
B24	HD2	I/O
C21	HD20	I/O
B21	HD21	I/O
B20	HD22	I/O
D20	HD23	I/O
A20	HD24	I/O
C19	HD25	I/O
A19	HD26	I/O
D19	HD27	I/O
A18	HD28	I/O
D18	HD29	I/O
C25	HD3	I/O
B19	HD30	I/O
C18	HD31	I/O
C17	HD32	I/O
D17	HD33	I/O
C16	HD34	I/O
B18	HD35	I/O
A16	HD36	I/O
A17	HD37	I/O
B17	HD38	I/O
D15	HD39	I/O
A24	HD4	I/O
B16	HD40	I/O
B14	HD41	I/O

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Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
A15	HD42	I/O
D16	HD43	I/O
B15	HD44	I/O
C15	HD45	I/O
C13	HD46	I/O
D14	HD47	I/O
B13	HD48	I/O
E13	HD49	I/O
C24	HD5	I/O
D11	HD50	I/O
A14	HD51	I/O
D13	HD52	I/O
D12	HD53	I/O
C12	HD54	I/O
B11	HD55	I/O
C11	HD56	I/O
E12	HD57	I/O
A10	HD58	I/O
A13	HD59	I/O
A23	HD6	I/O
A12	HD60	I/O
A11	HD61	I/O
A9	HD62	I/O
B10	HD63	I/O
F23	HD7	I/O
C23	HD8	I/O
B23	HD9	I/O
P22	HGNDA	P
P26	HITJ	I/O
P25	HITMJ	I/O
L25	HREQJ0	I/O
L26	HREQJ1	I/O
N26	HREQJ2	I/O
P24	HREQJ3	I/O
M26	HREQJ4	I/O
L22	HVDDA	P
D5	IRDYJ	I/O

Pin No.	Pin Name	Type
N24	LOCKJ	I/O
AE17	MA0	I/O
AF17	MA1	I/O
AF15	MA10	I/O
AC14	MA11	I/O
AD14	MA12	I/O
AE14	MA13	I/O
AF14	MA14	I/O
AC16	MA2	I/O
AD16	MA3	I/O
AE16	MA4	I/O
AF16	MA5	I/O
AB15	MA6	I/O
AC15	MA7	I/O
AD15	MA8	I/O
AE15	MA9	I/O
AF18	MB0	I/O
AD17	MB1	I/O
T26	MD0	I/O
T23	MD1	I/O
Y22	MD10	I/O
AA25	MD11	I/O
AA23	MD12	I/O
AB25	MD13	I/O
AB23	MD14	I/O
AC25	MD15	I/O
AC12	MD16	I/O
AF11	MD17	I/O
AC11	MD18	I/O
AF10	MD19	I/O
U25	MD2	I/O
AD10	MD20	I/O
AF9	MD21	I/O
AD9	MD22	I/O
AF8	MD23	I/O
AD8	MD24	I/O
AF7	MD25	I/O

Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
AD7	MD26	I/O
AF6	MD27	I/O
AD6	MD28	I/O
AF5	MD29	I/O
U23	MD3	I/O
AD5	MD30	I/O
AF4	MD31	I/O
T25	MD32	I/O
U26	MD33	I/O
U24	MD34	I/O
V26	MD35	I/O
V24	MD36	I/O
W26	MD37	I/O
W24	MD38	I/O
W22	MD39	I/O
V25	MD4	I/O
Y25	MD40	I/O
Y23	MD41	I/O
AA26	MD42	I/O
AA24	MD43	I/O
AB26	MD44	I/O
AB24	MD45	I/O
AC26	MD46	I/O
AC24	MD47	I/O
AB12	MD48	I/O
AE11	MD49	I/O
V23	MD5	I/O
AB11	MD50	I/O
AE10	MD51	I/O
AC10	MD52	I/O
AE9	MD53	I/O
AC9	MD54	I/O
AE8	MD55	I/O
AC8	MD56	I/O
AE7	MD57	I/O
AC7	MD58	I/O

Pin No.	Pin Name	Type
AE6	MD59	I/O
W25	MD6	I/O
AC6	MD60	I/O
AE5	MD61	I/O
AC5	MD62	I/O
AE4	MD63	I/O
W23	MD7	I/O
Y26	MD8	I/O
Y24	MD9	I/O
AD26	MPD0	I/O
AF26	MPD1	I/O
AD12	MPD2	I/O
AF12	MPD3	I/O
AE26	MPD4	I/O
AD25	MPD5	I/O
AE12	MPD6	I/O
AD11	MPD7	I/O
AE24	MWEJ0	I/O
AD24	MWEJ1	I/O
AF25	MWEJ2	I/O
AE25	MWEJ3	I/O
G22	NC	
E2	PAR	I/O
J4	PCICLK	I
B7	PGNTJ0	I/O
D8	PGNTJ1	I/O
B8	PGNTJ2	I/O
D9	PGNTJ3	I/O
B9	PGNTJ4	I/O
H4	PHLDAJ	I/O
K4	PHLDJ	I
M2	PIPEJ	I
D3	PLOCKJ	I/O
C7	PREQJ0	I
A7	PREQJ1	I
C8	PREQJ2	I

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Alphabetical Pin List (continued)

Pin No.	Pin Name	Type
A8	PREQJ3	I
C9	PREQJ4	I
D4	PTRDYJ	I/O
AD19	RASJ0	I/O
AF20	RASJ1	I/O
AE20	RASJ2	I/O
AD20	RASJ3	I/O
AF21	RASJ4	I/O
AE21	RASJ5	I/O
AD21	RASJ6	I/O
AF22	RASJ7	I/O
K5	RATIOJ	I/O
M1	RBFJ	I
AC21	REFENV	I/O
D10	Reserved	
D7	RESETJ	I/O
P23	RSJ0	I/O
R25	RSJ1	I/O
R23	RSJ2	I/O
N4	SB_STB	I
M3	SBA0	I/O
M4	SBA1	I/O
N1	SBA2	I/O
N3	SBA3	I/O
N5	SBA4	I/O
P1	SBA5	I/O
P2	SBA6	I/O
P3	SBA7	I/O
AE23	SCASJ0	I/O
AD23	SCASJ1	I/O
AC23	SCASJ2	I/O
AF24	SCASJ3	I/O
E1	SERRJ	I/O
AB19	SMIACKJ	I
AE18	SRASJ0	I/O
AD18	SRASJ1	I/O
AF19	SRASJ2	I/O
AE19	SRASJ3	I/O
L1	ST0	I/O
L2	ST1	I/O
L3	ST2	I/O
D2	STOPJ	I/O
AC20	SUSPENDJ	I
T24	TESTIN	I
N22	TRDYJ	I/O
AB9	VCC_SP	P
M5	VCC5V	P
AB10	VCC5V_SP	P
E14	VCCHP	P
E15	VCCHP	P
E19	VCCHP	I
F19	VCCHP	P
J22	VCCHP	P
AA19	VCCMP	P
AA20	VCCMP	P
AB20	VCCMP	P
AB21	VCCMP	P
V22	VCCMP	P
W21	VCCMP	P
AA5	VCCP	P
AA6	VCCP	P
AB5	VCCP	P
E5	VCCP	P
E6	VCCP	P
F6	VCCP	P
F7	VCCP	P
L5	VCCP	P
Y6	VCCP	P
U5	VCCPL1	P
AB17	VCCPL2	P
R22	VCCPL3	P
W5	VDDPLL	P

Section 3 : Function Description

3.1 SYSTEM MEMORY FEATURES DESCRIPTION AND CONFIGURATION

3.1.1 Memory Address Types supported

For the properly permuted MA mapping table, the M1621 can work with any available symmetric and asymmetric DRAM on the market. The DRAM sizing procedure of the M1621 is as follows. After determining if the DRAM is FPM, EDO or SDRAM, the BIOS detects its column address range with the proper algorithm. Then the BIOS can set the appropriate MA mapping. In other words, all DRAMs that have the same number of CAS address lines use the same MA mapping. After this, the BIOS then detects the row address range and calculates the DRAM size from the number of CAS address lines and the number of RAS address lines. Such arrangement of MA mapping also supports both 2-bank and 4-bank SDRAM configurations.

MA Mapping Table (64 bit DRAM)

	For FPM & EDO DRAMs									
	8-bit column address (0000)		9-bit column address (0001)		10-bit column address (0010)		11-bit column address (0011)		12-bit column address (0100)	
	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS
MA14	A25		A26		A27		A28		A29	
MA13	A24		A25		A26		A27		A28	
MA12	A23		A24		A25		A26		A27	
MA11	A22		A23		A24		A25		A25	A26
MA10	A21		A22		A23		A23	A13	A23	A13
MA9	A20		A21		A21	A12	A21	A12	A21	A12
MA8	A19		A19	A11	A19	A11	A19	A11	A19	A11
MA7	A11	A9	A20	A9	A20	A9	A20	A9	A20	A9
MA6	A12	A8	A12	A8	A22	A8	A22	A8	A22	A8
MA5	A13	A7	A13	A7	A13	A7	A24	A7	A24	A7
MA4	A14	A6	A14	A6	A14	A6	A14	A6	A14	A6
MA3	A15	A5	A15	A5	A15	A5	A15	A5	A15	A5
MA2	A18	A10	A18	A10	A18	A10	A18	A10	A18	A10
MA1	A17	A4	A17	A4	A17	A4	A17	A4	A17	A4
MA0	A16	A3	A16	A3	A16	A3	A16	A3	A16	A3

	For Synchronous DRAM									
	8-bit column address (0000)		9-bit column address (0001)		10-bit column address (0010)		11-bit column address (*1111*)			
	RAS	CAS	RAS	CAS	RAS	CAS	RAS	CAS		
MA14	A25	A25	A26	A26	A27	A27	A28	A28		
MA13	A24	A24	A25	A25	A26	A26	A27	A27		
MA12	A23	A23	A24	A24	A25	A25	A26	A26		
MA11	A22	A22	A23	A23	A24	A24	A25	A13		
MA10	A21	Pre	A22	Pre	A23	Pre	A23	Pre		
MA9	A20	A20	A21	A22	A21	A12	A21	A12		
MA8	A19	A20	A19	A11	A19	A11	A19	A11		
MA7	A11	A9	A20	A9	A20	A9	A20	A9		
MA6	A12	A8	A12	A8	A22	A8	A22	A8		
MA5	A13	A7	A13	A7	A13	A7	A24	A7		
MA4	A14	A6	A14	A6	A14	A6	A14	A6		
MA3	A15	A5	A15	A5	A15	A5	A15	A5		
MA2	A18	A10	A18	A10	A18	A10	A18	A10		
MA1	A17	A4	A17	A4	A17	A4	A17	A4		
MA0	A16	A3	A16	A3	A16	A3	A16	A3		

3.2 SDRAM Performance Summary

3.2.1 Outstanding DRAM Timing

Table 3.2.1 DRAM Timing Setting Summary

DRAM type	DRAM speed	timing parameter	66 MHz	75 MHz	83 MHz	100 MHz
FPM	60 ns	tASR	0	0	0	0
		tRAH	1	1	1	1
		tASC	1	1	1	1
		tCASW	2	2	2	2
		tCASR	2	2	2	2
		tCP	1	1	1	2
		tCSH	4	5	5	6
		tRAS	4	5	5	6
		tRP	3	3	4	5
	70 ns	tASR	0	0	0	x
		tRAH	1	1	1	x
		tASC	1	1	1	x
		tCASW	2	3	3	x
		tCASR	2	3	3	x
		tCP	1	1	1	x
		tCSH	5	6	6	x
		tRAS	5	6	6	x
		tRP	4	4	5	x
	80 ns	tASR	0	0	0	x
		tRAH	1	1	1	x
		tASC	1	1	1	x
		tCASW	3	3	4	x
		tCASR	3	3	4	x
		tCP	1	1	1	x
		tCSH	6	6	6	x
		tRAS	6	6	6	x
		tRP	4	5	5	x

x : not supported

Table 3.2.2 DRAM Timing Setting Summary

DRAM type	DRAM speed	timing parameter	66 MHz	75 MHz	83 MHz	100 MHz
EDO	50 ns	tASR	0	0	0	0
		tRAH	1	1	1	1
		tASC	1	1	1	1
		tCASW	1	1	1	1
		tCASR	1	1	1	1
		tCP	1	1	1	1
		tCSH	3	3	4	4
		tRAS	4	4	5	5
		tRP	2	3	3	3
	60 ns	tASR	0	0	0	0
		tRAH	1	1	1	1
		tASC	1	1	1	1
		tCASW	1	1	1	1
		tCASR	1	1	1	1
		tCP	1	1	1	1
		tCSH	3	3	4	4
		tRAS	4	5	5	6
		tRP	3	3	4	4
	70 ns	tASR	0	0	0	x
		tRAH	1	1	1	x
		tASC	1	1	1	x
		tCASW	1	1	1	x
		tCASR	1	1	1	x
		tCP	1	1	1	x
		tCSH	4	4	6	x
		tRAS	5	6	6	x
		tRP	4	4	5	x

x : not supported

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Table 3.2.3 SDRAM Performance Summary One

Read cycle (CL = 2, tRCD = 2, tRP = 2, Multi-Banking)							
	from idle	read-read page hit --> *Access to Same Bank or Different Opened Bank*	read-read page miss --> *Access to Same Opened Bank*	read-read page miss --> *Access to Different Unopened Bank*	write-read page hit --> *Access to Same Bank or Different Opened Bank*	write-read page miss --> *Access to Same Opened Bank*	write-read page miss --> *Access to Different Unopened Bank*
66 MHz	7-1-1-1	x-1-1-1 1-1-1-1	x-1-1-1 6-1-1-1	x-1-1-1 4-1-1-1	x-1-1-1 3-1-1-1	x-1-1-1 9-1-1-1	x-1-1-1 7-1-1-1
100 MHz	8-1-1-1	x-1-1-1 1-1-1-1	x-1-1-1 6-1-1-1	x-1-1-1 4-1-1-1	x-1-1-1 3-1-1-1	x-1-1-1 9-1-1-1	x-1-1-1 7-1-1-1

Table 3.2.4 SDRAM Performance Summary Two

Write cycle (tRCD = 2, tRP = 2, Multi-Banking)							
	from idle	write-write page hit --> *Access to Same Bank or Different Opened Bank*	write-write page miss --> *Access to Same Opened Bank*	write-write page miss --> *Access to Different Unopened Bank*	read-write page hit --> *Access to Same Bank or Different Opened Bank*	read-write page miss --> *Access to Same Opened Bank*	read-write page miss --> *Access to Different Unopened Bank*
66 MHz	6-1-1-1	x-1-1-1 1-1-1-1	x-1-1-1 7-1-1-1	x-1-1-1 5-1-1-1	x-1-1-1 2-1-1-1	x-1-1-1 4-1-1-1	x-1-1-1 2-1-1-1
100 MHz	7-1-1-1	x-1-1-1 1-1-1-1	x-1-1-1 7-1-1-1	x-1-1-1 5-1-1-1	x-1-1-1 2-1-1-1	x-1-1-1 4-1-1-1	x-1-1-1 2-1-1-1

Table 3.2.5 Performance Summary of FPM/EDO Read Cycle

DRAM type	Burst performance (in host CLK)			
	66 MHz	75 MHz	83 MHz	100 MHz
EDO-5	x-2-2-2	x-2-2-2	x-2-2-2	x-2-2-2
EDO-6	x-2-2-2	x-2-2-2	x-2-2-2	x-2-2-2
EDO-7	x-2-2-2	x-2-2-2	x-2-2-2	****
FPM-6	x-3-3-3	x-3-3-3	x-3-3-3	x-3-3-3
FPM-7	x-3-3-3	x-4-4-4	x-4-4-4	x-4-4-4
FPM-8	x-4-4-4	x-4-4-4	x-5-5-5	****

****** : not supported**

Table 3.2.6 Performance Summary of FPM/EDO Read Cycle

Relation to previous cycle	DRAM speed	The first data to previous last data (in host clocks)			
		66 MHz	75 MHz	83 MHz	100 MHz
from idle	EDO-5	4	4	4	4
	EDO-6	4	4	4	4
	EDO-7	4	4	4	x
	FPM-6	4	4	4	6
	FPM-7	4	5	5	x
	FPM-8	5	5	6	x
page hit	EDO-5	2	2	2	2
	EDO-6	2	2	2	2
	EDO-7	2	3	3	x
	FPM-6	3	3	3	3
	FPM-7	3	4	4	x
	FPM-8	4	4	5	x
page miss but same bank	EDO-5	6	7	7	7
	EDO-6	7	7	8	8
	EDO-7	8	9	10	x
	FPM-6	7	7	8	9
	FPM-7	8	9	10	x
	FPM-8	9	10	11	x
bank miss	EDO-5	5	5	5	5
	EDO-6	5	5	5	5
	EDO-7	5	6	6	x
	FPM-6	5	5	5	5
	FPM-7	5	6	6	x
	FPM-8	6	6	7	x

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3.2.3 DRAM Refresh Related Setting

Table 3.2.7 DRAM refresh rate setting (based on normal case, refresh once about every 15.625us)

	66 MHz	75 MHz	83 MHz	100 MHz
no. of host clock	1041=411H	1171=493H	1302=516H	1560=618H

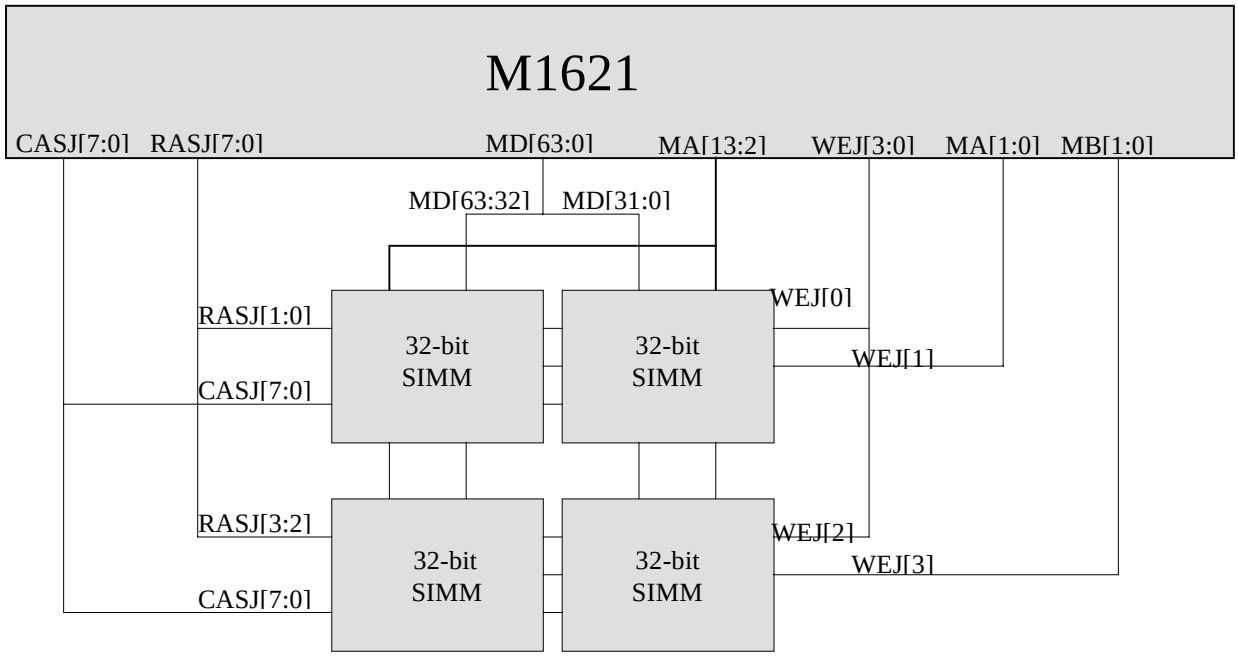
Table 3.2.8 DRAM refresh timing setting

DRAM speed	timing	66 MHz	75 MHz	83 MHz	100 MHz
EDO-5	tCSR	1	1	1	1
	tRAS	4	4	5	5
	tRP	2	3	3	3
FPM-6	tCSR	1	1	1	1
	tRAS	4	5	5	6
	tRP	3	3	4	5
EDO-6	tCSR	1	1	1	1
	tRAS	4	5	5	6
	tRP	3	3	4	4
FPM-7	tCSR	1	1	1	x
	tRAS	5	6	6	x
	tRP	4	4	5	x
EDO-7	tCSR	1	1	1	x
	tRAS	5	6	6	x
	tRP	4	4	5	x
FPM-8	tCSR	1	1	1	x
	tRAS	6	6	6	x
	tRP	4	5	5	x

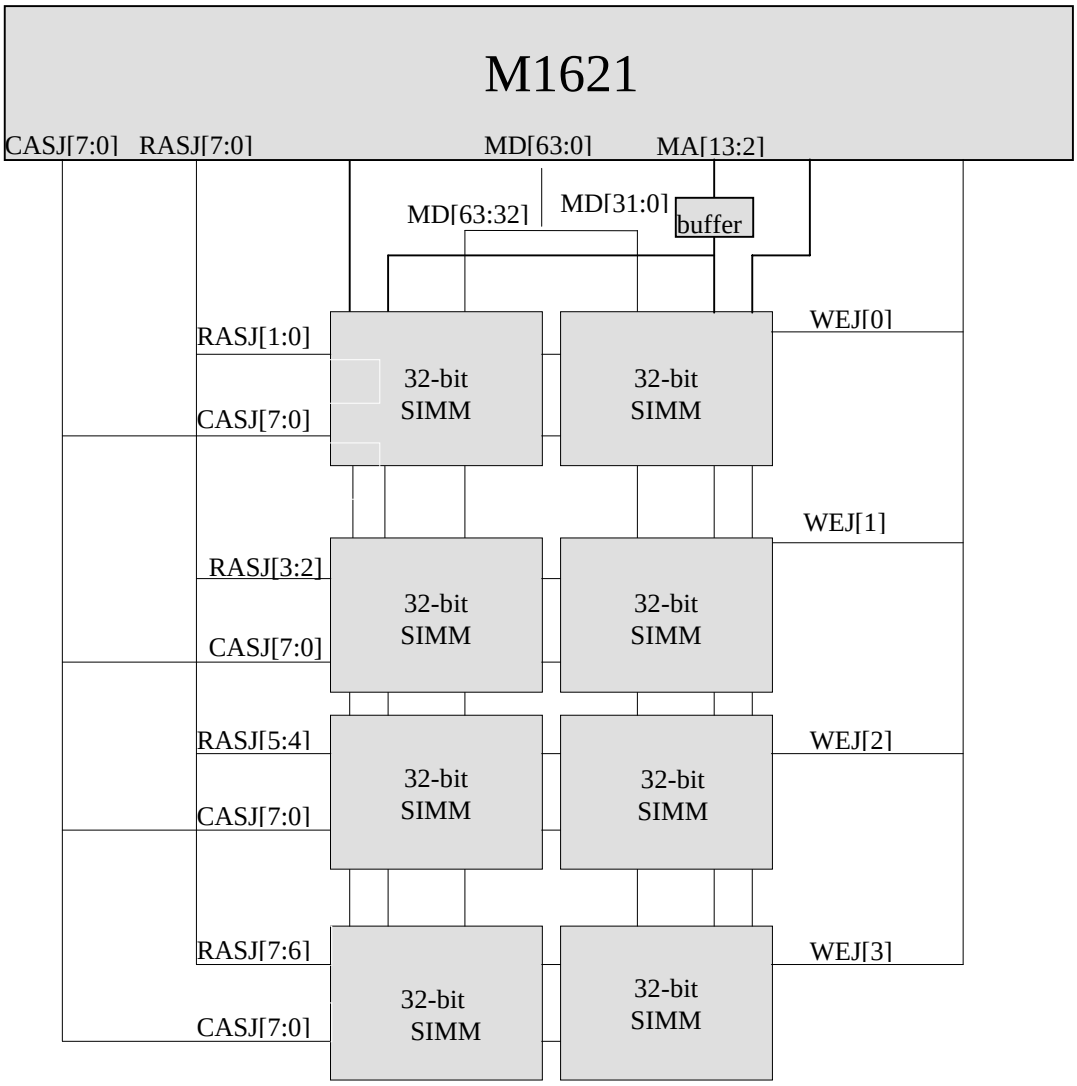
3.3 Connection between 72-pin Double-sided SIMM and the M1621

The following diagrams show some possible 72-pin double-sided SIMM applications with the M1621.

Application 1 : Without TTL buffer

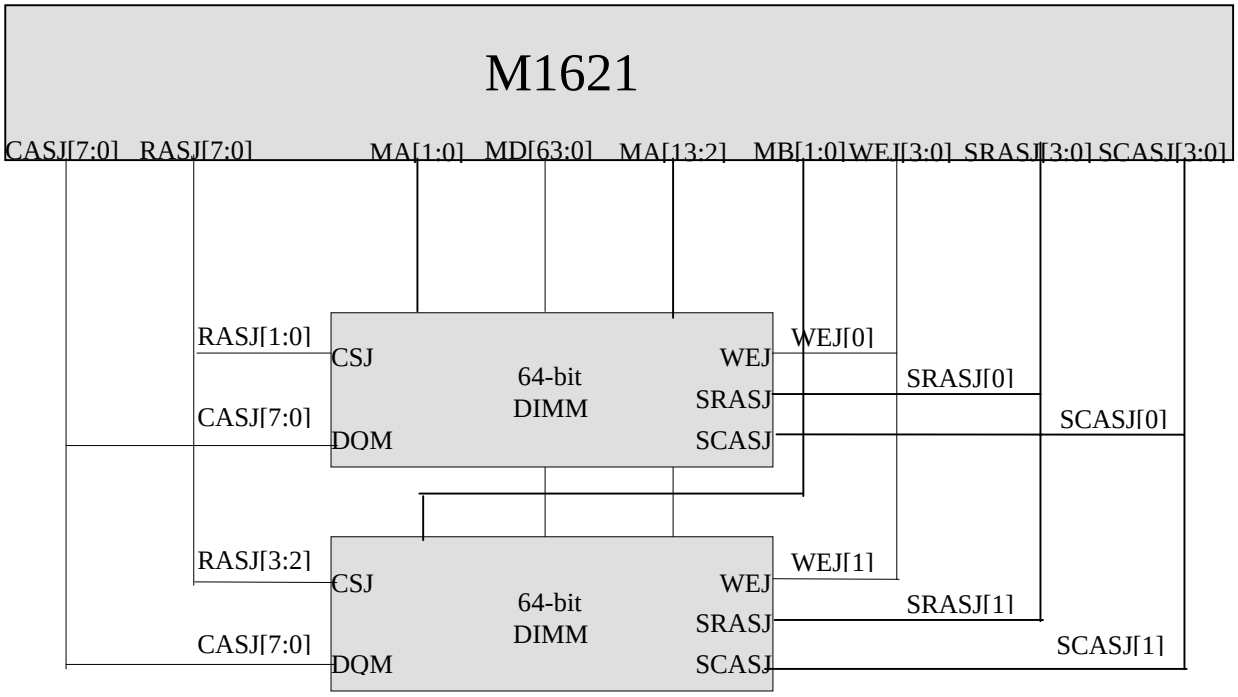


- Application 2: with TTL buffer



- Connection between 168-pins SDRAM DIMM and M1621

The following diagram shows possible 168-pin SDRAM DIMM applications with M1621.



Section 4 : Configuration Registers

I. M1621 PCI Mechanism #1 Configuration Cycle Ports

I/O Address **0CF8h**
Register Name : **CFGADR - Configuration Address Register**
Default Value 00000000h
Attribute Read/Write
Size This register must be 32-bit I/O access in PCI configuration access mechanism #1. An 8-bit or 16-bit access will pass through the Configuration Address Register onto the PCI bus.

Bit Number	Bit Function
31 (0)	PCI Configuration Space Access. 0 : Configuration Disable. 1 : Configuration Enable. When this bit is set to 1, accesses to PCI configuration space are enabled, otherwise, accesses to PCI configuration space are disabled.
30-24 (00h)	Reserved.
23-16 (00h)	Bus Number. When the bus number is programmed to 00H, the target of the configuration is directly connected to the M1621 and a type 0 configuration cycle is generated. If the bus number is non-zero, a type 1 configuration cycle is generated on the PCI bus.
15-11 (00h)	Device Number. Is used by the M1621 to drive the IDSEL lines that select a specific PCI device during initialization. The IDSEL lines are only driven when the Bus Number is 0h. As for the others, the M1621 will send the configuration to a PCI or PCI bridge device.
10-8 (0h)	Function Number. Is used to select a specific device function during initialization.
7-2 (00h)	Register Number. Is used to select a specific register during initialization.
1-0 (0h)	Reserved. Fixed at '00'.

I/O Address : **0CFCh**
Register Name : **CFGDAT - Configuration Data Register**
Default Value : 00000000h
Attribute : Read/Write
Size : This register may be 8-bit, 16-bit, or 32-bit I/O access in configuration access mechanism #1.
Description : This register contains the information which is sent or received during the PCI bus data phase of configuration write or read cycles. CPU accesses of 8, 16 or 32-bit wide to this register are supported.

Note : M1621 only supports PCI mechanism #1 access.

II. M1621 PCI Configuration Space Mapped Registers (IDSEL = AD11)

The M1621 will respond to CPU/PCI configuration access for which AD11 is high during the address phase.

The following table shows the register summary for device 0 (Host Bridge):

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default value
01h-00h	CR_VID	Vender Identification Register	R	10B9h
03h-02h	CR_DID	Device Identification Register	R	1621h
05h-04h	CR_CMD	Command Register	R/W	0006h
07h-06h	CR_STAS	Status Register	R/W Clear	0410h
08h	CR_RID	Revision Identification Register	R	01h
09h	CR_SRLP	Specific Register-level Programming Register	R	00h
0Ah	CR_SCC	Sub-Class Code Register	R	00h
0Bh	CR_BCC	Base-Class Code Identification Register	R	06h
0Fh-0Ch	Reserved	Reserved	R	00h
13h-10h	CR_BAR	Base Address Register	R/W	00000008h
33h-14h	Reserved	Reserved	R	00h
34h	CR_CPR	Capabilities Pointer Register	R	B0h
3Fh-35h	Reserved	Reserved	R	00h
40h	CR_FC3PCI	Flushing Counter for USWC Posted Write to 33PCI	R/W	0Ch
41h	CR_FC6PCI	Flushing Counter for USWC Posted Write to 66PCI	R/W	0Ch
43h-42h	CR_PIOW1	First I/O Address for Posted I/O Write	R/W	0000h
45h-44h	CR_PIOW2	Second I/O Address for Posted I/O Write	R/W	0000h
47h-46h	CR_PIOW3	Third I/O Address for Posted I/O Write	R/W	0000h
49h-48h	CR_PIOW4	Fourth I/O Address for Posted I/O Write	R/W	0000h
4Ah	CR_IOPWCNT	Control Register for I/O Posted Write Cycles	R/W	00h
4Bh	CR_CRSPCNF	Control Register for Special & Configuration Cycles	R/W	00h
4Ch	CR_CFDT3P	Counter for 33 PCI Delay Transaction	R/W	04h
4Dh	CR_CFDT6P	The Counter for 66 PCI Delay Transaction	R/W	04h
4Eh	CR_PPM1	Power Management for 33 PCI and 66 PCI Block	R/W	7Fh
4Fh	CR_PPM2	Power Management for Host Block	R/W	7Fh
50h	CR_HWGEN	Host to AGP Memory-Write Enhancement Register	R/W	0Ch
51h	CR_GPMFW	66 PCI Master Device Pre-Fetch & Post-Write Control Register	R/W	00h
52h	CR_GPCMD	66 PCI Bridge Command Register	R/W	00h
53h	CR_GPBRC	66 PCI Bridge Retry Counter Register (CR_GPBRC)	R/W	02h
55h-54h	CR_PBECR	66 PCI Bridge Error Command Register	R/W	0000h
56h	CR_PBECR	66 PCI Bridge Error Status Register	R/W	00h
57h	CR_GPBER	AGP Arbiter Control Register	R/W	00h

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default value
58h	CR_GPMDMT	66 PCI Master Device Multiple Transaction Timer	R/W	00h
59h	CR_GPBMT	66 PCI Bridge Multiple Transaction Timer	R/W	00h
5Ah	CR_P2PRCR	P2P Bridge Retry Counter Register	R/W	02h
5Bh	Reserved	Reserved	R	00h
5Ch	CR_PCLKRUN	PCI CLKRUN Control Register	R/W	00h
5Fh-5Dh	Reserved	Reserved	R	00h
60h	CR_HWEN	Host to PCI Memory-Write Enhancement Register	R/W	00h
61h	CR_PMFW	PCI Master Device Pre-Fetch & Post-Write Control Register	R/W	00h
2h	CR_PCMD	PCI Bridge Command Register	R/W	00h
63h	CR_PBRC	PCI Bridge Retry Counter Register	R/W	02h
65h-64h	CR_PBECR	PCI Bridge Error Command Register	R/W	0000h
66h	CR_PBECR	PCI Bridge Error Status Register	R/W Clear	00h
67h	CR_PBER	PCI Arbiter Control Register	R/W	00h
68h	CR_PMDMT	PCI Master Device Multiple Transaction Timer	R/W	00h
69h	CR_PBMT	PCI Bridge Multiple Transaction Timer	R/W	00h
6Bh-6Ah	Reserved	Reserved	R	00h
6Fh-6Ch	CR_MROW0	Memory Bank 0 Register	R/W	E600FFFFh
73h-70h	CR_MROW1	Memory Bank 1 Register	R/W	E000FFFFh
77h-74h	CR_MROW2	Memory Bank 2 Register	R/W	E000FFFFh
7Bh-78h	CR_MROW3	Memory Bank 3 Register	R/W	E000FFFFh
7Fh-7Ch	CR_MCMD	Memory Command Register	R/W	00C7C411h
81h-80h	CR_HCFG	Host Interface Configuration Register	R/W	0C01h
82h	CR_PDEC	PCI Decode Mode Register	R/W	00h
83h	CR_MSMM	A/B Page and SMM Range Register	R/W	08h
87h-84h	CR_MPAM	Memory Attribute Register	R/W	00000000h
8Bh-88h	CR_MRNG	Memory Gap Range Registers	R/W	00000000h
8Fh-8Ch	CR_USWC	USWC Gap Range Registers	R/W	00010000h
91h-90h	CR_ECCST	Memory ECC Error Status Register	R/W Clear	0000h
93h-92h	Reserved	Reserved	R	00h
97h-94h	CR_SPR1	Spare Register #1	R/W	00000000h
9Bh-98h	CR_SPR2	Spare Register #2	R/W	00000000h
9Fh-9Ch	CR_SPR3	Spare Register #3	R/W	00000000h
A3h-A0h	CR_PMC2	Power Management Control Block #2 - Starting Address	R/W	00000020h
AFh-A4h	Reserved	Reserved	R	00h
B3h-B0h	CR_AGPCI	AGP Capability Identifier Register	R/W	00800002h
B7h-B4h	CR_AGPSTA	AGP Status Register	R/W	20000203h
BBh-B8h	CR_AGPCMD	AGP Command Register	R/W	80000101h
BFh-BCh	CR_NLVMCTL	AGP NLVM Control Register	R/W	00000000h
C3h-C0h	CR_TGCLR	AGP TAG Clear Register	R/W	00000080h
C7h-C4h	CR_AGPCR1	AGP Control Register One	R/W	00000000h
CBh-C8h	CR_AGPCR2	AGP Control Register Two	R/W	00002400h
CFh-CCh	CR_AGPCR3	AGP Control Register Three	R/W	00000000h
D3h-D0h	CR_AGPCR4	AGP Control Register Four	R/W	00000000h
D7h-D4h	CR_AGPCR5	AGP Control Register Five	R/W	00000000h
EFh-D8h	Reserved	Reserved	R	00h

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default value
F3h-F0h	CR_RCA0	User-Defined Row/Column Address Mapping Registers 0	R/W	43214320h
F7h-F4h	CR_RCA1	User-Defined Row/Column Address Mapping Registers 1	R/W	43214320h
FBh-F8h	CR_RCA2	User-Defined Row/Column Address Mapping Registers 2	R/W	43214320h
FFh-FCh	CR_RCA3	User-Defined Row/Column Address Mapping Registers 3	R/W	43214320h

The following table shows the register summary for device 1 (P2P Bridge):

Byte Index	Mnemonic	Definition	Attribute (R/W)	Default value
01h-00h	CR_P2PVID	Vender Identification Register	R	10B9h
03h-02h	CR_P2PDID	Device Identification Register	R	5247h
05h-04h	CR_P2PCMD	Command Register	R/W	0007h
07h-06h	CR_P2PSTAS	Status Register	R/W	0000h
08h	CR_P2PRID	Revision Identification Register	R	01h
09h	CR_P2PSRLP	Specific Register-Level Programming Register	R	00h
0Ah	CR_P2PSCC	Sub-Class Code Register	R	04h
0Bh	CR_P2PBCC	Base-Class Code Identification Register	R	06h
0Dh-0Ch	Reserved	Reserved	R	00h
0Eh	CR_P2PHTR	Header Type Register	R	01h
17h-0Fh	Reserved	Reserved	R	00h
18h	CR_PBNR	Primary Bus Number Register	R	00h
19h	CR_SBNR	Secondary Bus Number Register	R/W	00h
1Ah	CR_SUBNR	Subordinate Bus Number Register	R/W	00h
1Bh	Reserved	Reserved	R	00h
1Ch	CR_IOBAR	IO Base Address Register	R/W	F0h
1Dh	CR_IOLAR	IO Limit Address Register	R/W	00h
1Fh-1Eh	CR_SPPSR	Secondary PCI-PCI Status Register	R/W	0020h
21h-20h	CR_MEMBAR	Memory Base Address Register	R/W	FFF0h
23h-22h	CR_MEMLAR	Memory Limit Address Register	R/W	0000h
25h-24h	CR_PMEMBAR	Pre-fetchable Memory Base Address Register	R/W	FFF0h
27h-26h	CR_PMEMLAR	Pre-fetchable Memory Limit Address Register	R/W	0000h
3Dh-28h	Reserved	Reserved	R	00h
3Fh-3Eh	CR_PPBCR	PCI-to- PCI Bridge Control Register	R/W	0000h
FFh-40h	Reserved	Reserved	R	00h

Vender Identification Register (CR_VID)
CSE Offset: 01 ~ 00h Read

Bits	Function	Default
[15:0]	This is a 16-bit value assigned to Acer Laboratories Inc. This register is combined with index 03h-02h to uniquely identify any PCI device. Writes to this register has no effect.	10B9h

Device Identification Register (CR_DID)
CSE Offset: 03 ~ 02h Read

Bits	Function	Default
[15:0]	This is a 16-bit value assigned to the M1621 from Acer Laboratories Inc.	1621h

Command Register (CR_CMD)
CSE Offset: 05 ~ 04h Read/Write

Bits	Function	Default
[15:9]	Reserved.	0000000b
[8]	SERRJ Enable : This bit is an enable bit for the SERRJ driver. A value of 0 disables SERRJ driver. A value of 1 enables the SERRJ driver. SERRJ uses an o/d (Open Drain) pad in the M1621. The motherboard design should use a pull-up resistor (2.7KΩ) to keep this pin logic high. When the DRAM ECC/Parity check or the PCI Parity check is enabled and an error is found, the M1621 will drive SERRJ low to the M1533/M1543/M1543C to generate NMI when this bit is enabled. Disabling the SERRJ output driver will always keep this output logic high. This bit is reset to 0 and should be set to 1 once memory has been scrubbed by the BIOS in systems that wish to report DRAM ECC/Parity error.	0b
[7:2]	Reserved.	01h
[1]	Memory Space Enable : Controls host bridge response to memory space accesses. A value of 0 disables the host bridge response. A value of 1 allows the device to respond to memory space accesses.	1b
[0]	Reserved.	0b

Status Register (CR_STAS)
CSE Offset: 07 ~ 06h Read/Write One to Clear

Bits	Function	Default
[15]	Detected Parity Error : The host bridge will set this bit whenever it detects a parity error, even if parity error handling is disabled.	0b
[14]	Signaled System Error : The host bridge will set this bit when it asserts SERRJ.	0b
[13]	Received Master Abort : The host bridge will set this bit when its transaction is terminated with Master-Abort.	0b
[12]	Received Target Abort : The host bridge will set this bit when its transaction is terminated with Target-Abort.	0b
[11]	Reserved	0b
[10:9]	DEVSEL timing : The host bridge is fixed to slow decode	10b
[8:5]	Reserved	0000b
[4]	AGP capability bit. This bit means the M1621 has implemented the function of Accelerated Graphics Port.	1b
[3:0]	Reserved	0h

Revision Identification Register (CR_RID)
CSE Offset: 08h Read

Bits	Function	Default
[7:0]	This is an 8-bit value that indicates the revision identification number for the M1621 from ALi.	01h

Specific Register-level Programming Register (CR_SRLP)
CSE Offset: 09h Read

Bits	Function	Default
[7:0]	This value in the M1621 is 00h.	00h

Sub-Class Code Register (CR_SCC)
CSE Offset: 0Ah Read

Bits	Function	Default
[7:0]	This value in the M1621 is 00h.	00h

Base-Class Code Identification Register (CR_BCC)
CSE Offset: 0Bh Read

Bits	Function	Default
[7:0]	This value in the M1621 is 06h. It means the M1621 is a Host Bridge device	06h

Reserved
CSE Offset: 0F ~ 0Ch Read
Default : 00h

Base Address Register (CR_BAR)
CSE Offset: 13 ~ 10h Read/Write

Bits	Function	Default
[31:0]	This is a memory base register in the M1621. The address type is 32 bit address space and the data is pre-fetchable. This memory space is located for Non-Local Video Memory of AGP function. The memory space is controlled by CR_NLVMCTL (Index BFh-BCh) register.	00000008h

Reserved
CSE Offset: 33 ~ 14h Read
Default : 00h

Capabilities Pointer Register (CR_CPR)
CSE Offset: 34h Read

Bits	Function	Default
[7:0]	This register contains a byte offset into the host bridge configuration space containing the first item in the capabilities list and is a read only register. The first capability of the M1621 is AGP and the byte offset is B0h.	B0h

Reserved
CSE Offset: 3F ~ 35h Read
Default : 00h

Flushing Counter for USWC (Un-cacheable Speculative Write Combining) Posted Write to 33PCI (CR_FC3PCI)
CSE Offset: 40h Read/Write

Bits	Function	Default
[7:0]	This register is used to program the host clock count to flush the USWC posted write buffer to the PCI bus. When the counter is decreasing count to zero, the 33 PCI bridge will flush the USWC posted write to the PCI bus. The default value for this counter is 0Ch. When the data stays in the posted write buffer with the programmed timer count before it flushes to the PCI bus, there is an opportunity to perform write combining with the incoming write data. The USWC posted write buffer is programmed in Index 8Bh-88h and 8Fh-8Ch. Bit18 is used to enable the memory Gap Range. Bit16 is used to enable the USWC mode. Bits[15:4] are used to program the starting address and bits[2:0] are used to program the gap size. When USWC mode is enabled, memory gap is enabled, and the starting address and size are set, the programmed range memory address will post to USWC buffer and perform write combining feature when Index 60h bit0 is set to 1. Also Index 60h bit1 is used to enable the PCI burst mode and write combining before it is flushed to the PCI bus when the bit is set to 1.	0Ch (0Ch Host Clock)

Flushing Counter for USWC (Un-cacheable Speculative Write Combining) Posted Write to 66PCI (CR_FC6PCI)
CSE Offset: 41h Read/Write

Bits	Function	Default
[7:0]	This register is used to program the host clock count to flush USWC posted write buffer to the AGP bus. When the counter is decreasing count to zero, the 66 PCI bridge will flush the USWC posted write to the AGP bus. The default value for this counter is 0Ch. When the data stays in the posted write buffer with the programmed timer count before it flushes to the AGP bus, there is an opportunity to perform write combining with the incoming write data. The USWC posted write buffer is programmed in the M1621 P2P bridge Index 27h-24h. When Index 27h-26h CR_PMEMLAR address is higher than Index 25h-24h CR_PMEMBAR, the programmed range memory address will post to the USWC buffer and perform write combining feature when Index 50h bit0 is set to 1. Also Index 50h bit1 is used to enable the AGP burst mode and write combining before it is flushed to the AGP bus when the bit is set to 1.	0Ch (0Ch Host Clock)

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First I/O Address for Posted I/O Write (CR_PIOW1)
CSE Offset: 43 ~ 42h Read/Write

Bits	Function	Default
[15:0]	The first I/O address for a Bridge slave to post an I/O write cycle. The programmed I/O address will post to the I/O write buffer when CR_IOPWCNT (Index 4Ah) register bit0 is enabled. CR_IOPWCNT bit1 is used to select the I/O address byte count. When CR_IOPWCNT bit1 is reset to 0, only the programmed address byte will post to the buffer. When CR_IOPWCNT bit1 is set to 1, the consecutive byte enable starting at the programmed I/O address byte will post to the buffer. For example, if this I/O address is set to 1F1h and CR_IOPWCNT register bit0 is enabled, only 1F1h will post to the buffer when CR_IOPWCNT bit1 is reset to 0. 1F0h, 1F2h, and 1F3h will not post to the write buffer. If the I/O address is set to 1F1h and CR_IOPWCNT register bit0 is enabled, 1F3h-1F1h will post to the buffer when CR_IOPWCNT bit1 is set to 1. 1F0h still can not post to the buffer.	0000h (Address : 0000h)

Second I/O Address for Posted I/O Write (CR_PIOW2)
CSE Offset: 45 ~ 44h Read/Write

Bits	Function	Default
[15:0]	The second I/O address for a Bridge slave to post an I/O write cycle. The programmed I/O address will post to the I/O write buffer when CR_IOPWCNT (Index 4Ah) register bit2 is enabled. CR_IOPWCNT bit3 is used to select the I/O address byte count. When CR_IOPWCNT bit3 is reset to 0, only the programmed address byte will post to the buffer. When CR_IOPWCNT bit3 is set to 1, the consecutive byte enable starting at the programmed I/O address byte will post to the buffer. For example, if this I/O address is set to 1F1h and CR_IOPWCNT register bit2 is enabled, only 1F1h will post to the buffer when CR_IOPWCNT bit3 is reset to 0. 1F0h, 1F2h, and 1F3h will not post to the write buffer. If the I/O address is set to 1F1h and CR_IOPWCNT register bit2 is enabled, 1F3h-1F1h will post to the buffer when CR_IOPWCNT bit3 is set to 1. 1F0h still can not post to the buffer.	0000h (Address : 0000h)

Third I/O Address for Posted I/O Write (CR_PIOW3)
CSE Offset: 47 ~ 46h Read/Write

Bits	Function	Default
[15:0]	The third I/O address for a Bridge slave to post an I/O write cycle. The programmed I/O address will post to the I/O write buffer when CR_IOPWCNT (Index 4Ah) register bit4 is enabled. CR_IOPWCNT bit5 is used to select the I/O address byte count. When CR_IOPWCNT bit5 is reset to 0, only the programmed address byte will post to the buffer. When CR_IOPWCNT bit5 is set to 1, the consecutive byte enable starting at the programmed I/O address byte will post to the buffer. For example, if this I/O address is set to 1F1h and CR_IOPWCNT register bit4 is enabled, only 1F1h will post to the buffer when CR_IOPWCNT bit5 is reset to 0. 1F0h, 1F2h, and 1F3h will not post to the write buffer. If the I/O address is set to 1F1h and CR_IOPWCNT register bit4 is enabled, 1F3h-1F1h will post to the buffer when CR_IOPWCNT bit5 is set to 1. 1F0h still can not post to the buffer.	0000h (Address : 0000h)

Fourth I/O Address for Posted I/O Write (CR_PIOW4)
CSE Offset: 49 ~ 48h Read/Write

Bits	Function	Default
[15:0]	The fourth I/O address for a Bridge slave to post an I/O write cycle. The programmed I/O address will post to the I/O write buffer when CR_IOPWCNT (Index 4Ah) register bit6 is enabled. CR_IOPWCNT bit7 is used to select the I/O address byte count. When CR_IOPWCNT bit7 is reset to 0, only the programmed address byte will post to the buffer. When CR_IOPWCNT bit7 is set to 1, the consecutive byte enable starting at the programmed I/O address byte will post to the buffer. For example, if this I/O address is set to 1F1h and CR_IOPWCNT register bit6 is enabled, only 1F1h will post to the buffer when CR_IOPWCNT bit7 is reset to 0. 1F0h, 1F2h, and 1F3h will not post to the write buffer. If the I/O address is set to 1F1h and CR_IOPWCNT register bit6 is enabled, 1F3h-1F1h will post to the buffer when CR_IOPWCNT bit7 is set to 1. 1F0h still cannot post to the buffer.	0000h (Address : 0000h)

Control Register for I/O Posted Write Cycles (CR_IOPWCNT)
CSE Offset: 4Ah Read/Write

Bits	Function	Default
[7]	Mode of the ***Fourth*** I/O Address : 0 : Exactly that byte. 1 : Starting at that byte. This bit is used to select the byte count for the fourth I/O address. Refer to Index 49h-48h for more details.	0b (Exactly that byte)
[6]	Enable bit for the posted I/O write cycle of the ***Fourth*** I/O address : 0 : Disable. 1 : Enable. When this bit is set to 1 , the programmed fourth I/O address defined in Index 49h-48h will post to the I/O write buffer. If index 62h bit 0 is reset to 0, this bit must reset to 0 due to chip limitation.	0b (Disable)
[5]	Mode of the ***Third*** I/O Address : 0 : Exactly that byte. 1 : Starting at that byte. This bit is used to select the byte count for the third I/O address. Refer to Index 49h-48h for more details.	0b (Exactly that byte)
[4]	Enable bit for the posted I/O write cycle of the ***Third*** I/O address : 0 : Disable. 1 : Enable. When this bit is set to 1 , the programmed third I/O address defined in Index 47h-46h will post to the I/O write buffer. If index 62h bit 0 is reset to 0, this bit must reset to 0 due to chip limitation.	0b (Disable)
[3]	Mode of the ***Second*** I/O Address : 0 : Exactly that byte. 1 : Starting at that byte. This bit is used to select the byte count for the second I/O address. Refer to Index 49h-48h for more details.	0b (Exactly that byte)
[2]	Enable bit for the posted I/O write cycle of the ***Second*** I/O address : 0 : Disable. 1 : Enable. When this bit is set to 1 , the programmed second I/O address defined in Index 45h-44h will post to the I/O write buffer. If index 62h bit 0 is reset to 0, this bit must reset to 0 due to chip limitation.	0b (Disable)
[1]	Mode of the ***First*** I/O Address : 0 : Exactly that byte. 1 : Starting at that byte. This bit is used to select the byte count for the first I/O address. Refer to Index 49h-48h for more detail programming information.	0b (Exactly that byte)
[0]	Enable bit for the posted I/O write cycle of the ***First*** I/O address : 0 : Disable. 1 : Enable. When this bit is set to 1 , the programmed first I/O address defined in Index 43h-42h will post to the I/O write buffer. If index 62h bit 0 is reset to 0, this bit must reset to 0 due to chip limitation.	0b (Disable)

Control Register for Special & Configuration Cycles (CR_CRSPCNF)
CSE Offset: 4Bh Read/Write

Bits	Function	Default
[7:4]	Reserved.	0h
[3]	This control bit is used to guarantee the data in MWB (Memory Write Buffer) will flush to the correct DRAM location before the configuration cycle is issued to the PCI bus. When this bit is set, the PCI master state machine will flush and wait until the MWB is empty, then issues a ***configuration*** cycle. If this bit is disabled, the PCI master state machine will issue the configuration cycle no matter what the MWB status is. 0 : Disable. 1 : Enable .	0b (Disable)
[2]	This control bit is used to guarantee the data in MWB (Memory Write Buffer) will flush to the correct DRAM location before the stop clock grant cycle is issued to the PCI bus. When this bit is set, the PCI master state machine will flush and wait until the MWB is empty, then issues the ***stop clock grant*** special cycle. If this bit is disabled, the PCI master state machine will issue the stop clock grant cycle no matter what the MWB status is. 0 : Disable. 1 : Enable.	0b (Disable)
[1]	This control bit is used to guarantee the data in MWB (Memory Write Buffer) will flush to the correct DRAM location before the halt cycle is issued to the PCI bus. When this bit is set, the PCI master state machine will flush and wait until the MWB is empty, then issues the ***halt*** special cycle. If this bit is disabled, the PCI master state machine will issue the halt cycle no matter what the MWB status is. 0 : Disable. 1 : Enable.	0b (Disable)
[0]	This control bit is used to guarantee the data in MWB (Memory Write Buffer) will flush to the correct DRAM location before the shutdown cycle is issued to the PCI bus. When this bit is set, the PCI master state machine will flush and wait until the MWB is empty, then issues the ***shutdown*** special cycle. If this bit is disabled, the PCI master state machine will issue the shutdown cycle no matter what the MWB status is. 0 : Disable. 1 : Enable.	0b (Disable)

Counter for 33 PCI Delay Transaction (CR_CFDT3P)
CSE Offset: 4Ch Read/Write

Bits	Function	Default
[7:0]	This byte counter is for the aborting mechanism of 33 PCI delay transaction. Delay transaction is a feature to control the PCI bus latency. When a PCI master issues a cycle to the M1621 and it will take more than 8 PCI clocks to complete, the PCI cycle will be retried and the M1621 will start this cycle internally. When the internal cycle is finished and the PCI master retried cycle comes back, the cycle can be terminated normally. If the same PCI master device issues a different line boundary cycle, when the previous issued read cycle is served as a delay transaction, the M1621 will add the internal count and retry the PCI master. If the number of different cycles are equal to this counter value, the M1621 will abort the current delay transaction and start the new PCI request cycle to avoid dead lock conditions.	04h (4 times)

Counter for 66 PCI Delay Transaction (CR_CFDT6P)
CSE Offset: 4Dh Read/Write

Bits	Function	Default
[7:0]	This byte counter is for the aborting mechanism of 66 PCI delay transactions. Delay transaction is a feature to control the AGP bus latency. When a master issues a cycle to the M1621 and it will take more than 8 AGP clocks to complete, the AGP cycle will be retried and the M1621 will start this cycle internally. When the internal cycle is finished and the AGP master retried cycle comes back, the cycle can be terminated normally. If the same AGP master device issues the different line boundary cycle when the previous issued read cycle is served as a delay transaction, the M1621 will add the internal count and retry the AGP master. If the number of different cycles are equal to this counter value, the M1621 will abort the current delay transaction and start the new AGP request cycle to avoid dead lock conditions.	04h (4 times)

Power Management for 33 PCI and 66 PCI Block (CR_PPM1)
CSE Offset: 4Eh Read/Write

Bits	Function	Default
[7]	Power Management for 33 PCI/66 PCI Enable Bit : 0 : Disable. 1 : Enable. This bit is used to enable the power management feature for dark green use. When this bit is enabled, 33 PCI and 66 PCI to DRAM master state machine clock will be gated off when the programming idle clock count defined in bits[6:0] is up.	0b (Disable)
[6:4]	Base Unit of Idle Clock : 111 : 255 clocks. 110 : 127 clocks. 101 : 63 clocks. 100 : 31 clocks. 011 : 15 clocks. 010 : 7 clocks. 001 : 3 clocks. 000 : 1 clock.	111b (255 PCI Clocks for 33 PCI, 255 AGP Clocks for 66PCI)
[3:0]	Number of Idle Units Before Stop Clock.	1111b (Fh)

Power Management for Host Block (CR_PPM2)
CSE Offset: 4Fh Read/Write

Bits	Function	Default
[7]	Power Management for Host Block Enable Bit : 0 : Disable. 1 : Enable . This bit is used to enable the power management feature for dark green use. When this bit is enabled, host to 33 PCI and 66 PCI slave state machine clock will be gated off when the programming idle clock count defined in bits[6:0] is up.	0b (Disable)
[6:4]	Base unit of idle clock : 111 : 255 clocks 110 : 127 clocks 101 : 63 clocks 100 : 31 clocks 011 : 15 clocks 010 : 7 clocks 001 : 3 clocks 000 : 1 clock	111b (255 PCI Clocks for 33 PCI, 255 AGP Clocks for 66PCI)
[3:0]	Number of idle units before stop clock.	1111b (Fh)

Host to AGP Memory-Write Enhancement Register (CR_HWGEN)
CSE Offset: 50h Read/Write

Bits	Function	Default
[7]	A.G.P. Frame Cycle to Memory Write Cannot Allocate Buffer : 0 : Busy wait for buffer. 1 : Retry PCI Master cycle. When AGP master issues a cycle to memory and the MWB is full, the AGP master cycle will keep waiting until the buffer has the space to serve this cycle if this bit is reset to 0. Otherwise, the M1621 will retry this AGP master cycle.	0b (Busy wait)
[6]	A.G.P. Frame Write Cycle Data Flow Rate : 0 : 1-1-1-1. 1 : 2-2-2-2. This bit is used to control the data flow rate for AGP master write cycles.	0b (1-1-1-1)
[5]	Posted All Memory Write Cycles of Host to 66 PCI : 0 : Disable. 1 : Enable. This bit combines with Index 52h bit0 = 1 to enhance the defer mode performance. When this bit is enabled and defer mode is selected, all host memory cycle will post to 66 PCI write buffer. This bit must be disabled when Index 52h bit0 is reset to 0.	0b (Disable)
[4]	Reserved.	0b
[3]	66 PCI DEVSEL# Response Timing : 0 : Medium. 1 : Slow. This bit is used to select the response timing for the AGP bus. When this bit is reset to 0, medium timing is selected. Otherwise, slow timing is selected.	1b (Slow)
[2]	A.G.P. Master Access DRAM : 0 : Disable. 1 : Enable. When this bit is set, the AGP master can issue PCI frame cycle to access memory. When this bit is cleared, the AGP PCI slave state machine will ignore any access cycle of memory. This bit is for test mode only.	1b (Enable)
[1]	Host Memory Write Line or QW-Combining Enable/Disable : 0 : Disable. 1 : Enable. When this bit is enabled, 66 PCI master state machine will perform burst and QWORD combining before the posted cycle is written to AGP bus.	0b (Disabled)
[0]	Partial Write - QW Combining Enable on USWC Region : 0 : Disable. 1 : Enable. When this bit is enabled, USWC post write buffer will perform QWORD combining.	0b (Disabled)

66 PCI Master Device Pre-Fetch & Post-Write Control Register (CR_GPMFW)
CSE Offset: 51h Read/Write

Bits	Function	Default
[7]	PCI Spec. 2.1 Cache Line Wrap Mode Enable / Disable on 66 PCI Side : 0 : Disable. 1 : Enable. When this bit is set to 1 and the AGP master issues a cache line wrap mode burst access (GAD[1:0]=10b during Memory access), the M1621 will disconnect this AGP master burst access to become single access.	0b (Disable)
[6]	Partial Write Byte Combining Enable / Disable on 66 PCI side : 0 : Disable. 1 : Enable. When this bit is enabled, the partial data will be posted until the address on 66 PCI side location is not continuous. Otherwise, the partial data will be flushed when the transaction is completed.	0b (Disable)
[5]	66 PCI Single Read Hit Enable / Disable : 0 : Disable. 1 : Enable. When the AGP issues a single DW, the M1621 will pre-fetch a line. When this bit is disabled, the single DW reads will be treated individually. Which means the next single read will cause the M1621 to pre-fetch a line again. When this bit is enabled, the single DW reads will be treated as line_unit_group. This means the next single read will return data from the previous pre-fetch line if the address read-hits the line.	0b (Disable)
[4]	Delayed Transaction Function Enable / Disable on 66 PCI Side : 0 : Disable. 1 : Enable. When this bit is disabled, the M1621 will keep the AGP master waiting if the target initial latency (8 AGP Clocks) of the first data does not obey the PCI 2.1 spec. When this bit is enabled, the M1621 will retry the AGP master if the target initial latency (8 AGP Clocks) of the first data meets the PCI 2.1 spec.	0b (Disable)
[3]	66 PCI Master Guarantee Mode (Retry Priority Queue) Enable / Disable : 0 : Disable. 1 : Enable . When this mode is enabled, the M1621 will memorize the retry the PCI master and put this master as the top priority when the PCI request comes back.	0b (Disable)
[2:0]	Pre-fetch Prediction for 66 PCI Read Line/Multiple Command : 000 : One Line mode. 001 : Dual line mode. 010 : Three line mode. 011 : Four line mode. 100 : Adaptive Mode, started from one line. 101 : Adaptive Mode, started from two lines. 110 : Adaptive Mode, started from three lines. 111 : Adaptive Mode, started from four lines. These three bits are used to select the pre-fetch line mode for the AGP master read Line/Multiple command. One (000b), dual (001b), three (010b), and four (011b) line mode mean the pre-fetch line count for the AGP master read Line/Multiple command. Adaptive mode means the M1621 will fetch increasing line count if the AGP master keep reading hit the pre-fetch buffer data.	000b (One line mode)

66 PCI Bridge Command Register (CR_GPCMD)
CSE Offset: 52h Read/Write

Bits	Function	Default
[7]	PCI 2.1 Latency Compliant mode on 66 PCI side : 0 : Disable. 1 : Enable. This bit combines with the Index 51h bit4 to control the delay transaction feature. This bit is used to control the latency of second, third, and the next data. Note: This bit can only be enabled if Index 51h bit4 is enabled. Otherwise it will cause a system failure.	0b (Disable)
[6:5]	Reserved.	00b
[4]	Enable/Disable the M1621 to Issue PCI Lock Access on 66 PCI Side : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 will pass Host side lock cycle to 66 PCI (AGP) side. Otherwise, the M1621 will ignore Host side lock signal.	0b (Disable)
[3]	Enable/Disable the M1621 to Transfer 66 PCI Lock Access to CPU Bus : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 will pass 66 PCI (AGP) side lock cycle to Host side. Otherwise, the M1621 will ignore 66 PCI side lock signal.	0b (Disable)
[2]	PALETTE SNOOP : 0 : Disable. 1 : Enable. When this bit is set to 1, the P2P bridge will monitor 3C6h, 3C8h, 3C9h, I/O write cycle and issue it to another PCI bus. Otherwise, the P2P bridge will not monitor 3C6h, 3C8h, 3C9h, I/O write cycle and issue it to another PCI bus.	0b (Disable)
[1]	Criterion of Defer Retry When the Entry on Top of I.O.Q. : 0 : When the GO.B.Q. is full. 1 : When both of GO.B.Q. and GI.B.Q. are full. When this bit is reset to 0, the cycle at the top of I.O.Q. will be defer retried if the GO.B.Q is full. GO.B.Q is the out bound queue to the AGP bus. When this bit is set to 1, the cycle at the top of I.O.Q. will only be defer retried if the GO.B.Q and GI.B.Q are full. GI.B.Q is the input bound queue from the AGP bus.	0b
[0]	66 PCI Bridge Side Enhancement Mode : 0 - Synchronous Mode. 1 - Deferred Mode. When synchronous mode is selected, the M1621 will stall the CPU to 66 PCI cycle in the Snoop phase until the cycle is passed to 66 PCI (AGP) bus. If synchronous mode is selected, disable PCI66 memory posted write buffer (Index 50h bit 5 must be reset as 0) due to chip limitation. Otherwise, the M1621 will defer this cycle and use defer reply when this cycle is passed to 66 PCI (AGP) bus.	0b (Synchronous Mode)

66 PCI Bridge Retry Counter Register (CR_GPBRC)
CSE Offset: 53h Read/Write

Bits	Function	Default
[7:0]	66 PCI Retry Counter : the PCI master functional block will re-issue the O.B.Q. command entry on the PCI bus following this number. When the counter expires, the PCI master functional block will abort the O.B.Q. command entry and terminate the Host cycle. A value of 0Fh is recommended for normal operation. 02h - Default (retry twice).	02h (Retry twice)

66 PCI Bridge Error Command Register (CR_PBECR)
CSE Offset: 55 ~ 54h Read/Write

Bits	Function	Default
[15:9]	Reserved.	Undefined
[8]	Issues SERRJ when the M1621 Issues Host Cycle to 66 PCI Bus and That Cycle Is Master Aborted : 0 : Does not assert SERRJ. 1 : Assert SERRJ. This bit is used to control the condition when the Host issues a cycle to 66 PCI bus and this cycle is master aborted. When this bit is reset to 0, the M1621 will ignore this condition and terminate the Host cycle with the reply defined in bit7 (Normal reply or Hard Failure). When this bit is set to 1 and bit7 is set to 1, the status bit defined in P2P bridge Index 07h-06h bit14 and Index 1Fh-1Eh bit13 will be set to 1. If P2P bridge Index 05h-04h bit8 is enabled, the M1621 will drive the PCI SERRJ signal to notify the south bridge to issue NMI to the CPU.	0b (Report Hard Failure)
[7]	Report Normal or Hard Failure When the 66 PCI Host Cycle is Master Aborted : 0 : Normal. 1 : Hard Failure. When bit8 is reset to 0, the Host issues a cycle to 66 PCI bus and this cycle is master aborted, the M1621 will terminate the Host cycle with Normal reply if this bit is reset to 0. Otherwise, Hard Failure is replied to the Host bus.	0b (Normal)
[6]	Reserved.	0b
[5]	Issue SERRJ on Received Data Parity Error : 0 : Disable. 1 : Enable. When the M1621 detects the parity error occurring when the external master writes data to DRAM or the M1621 reads data from the AGP device and this bit is enabled, the status bit defined in Index 56h bit5 will be set to 1 and the M1621 will drive the PCI SERRJ signal to notify the south bridge to issue NMI to the CPU if P2P bridge Index 05h-04h bit8 is enabled.	0b (Disable)
[4]	Issue SERRJ on Address Parity Error detecting : 0 : Disable. 1 : Enable. When the M1621 detects the AGP bus address parity error, the status bit defined in Index 56h bit4 will be set to 1 and the M1621 will drive the PCI SERRJ signal to notify the south bridge to issue NMI to the CPU if P2P bridge Index 05h-04h bit8 is enabled.	0b (Disable)
[3]	Reserved.	0b
[2]	When the 66 PCI Host Cycle Target Aborted Will Report SERRJ : 0 : Disable. 1 : Enable. This bit is used to control the condition when the Host issues a cycle to 66 PCI bus and this cycle is target aborted. When this bit is reset to 0, the M1621 will ignore this condition and terminate the Host cycle with Normal reply. When this bit is set to 1, the status bit defined in P2P bridge Index 07h-06h bit14 and Index 1Fh-1Eh bit12 will be set to 1. If P2P bridge Index 05h-04h bit8 is enabled, the M1621 will drive PCI SERRJ signal to notify the south bridge to issue NMI to the CPU.	0b (Disable)
[1:0]	Reserved.	00b

66 PCI Bridge Error Status Register (CR_PBECR)
CSE Offset: 56h Read & Write One to Clear

Bits	Function	Default
[7:6]	Reserved.	Undefined
[5]	This bit will be set if the M1621 66 PCI Data Parity Error is detected when the external master writes data to DRAM or the M1621 reads data from the PCI device and Index 55h-54h bit5 is enabled.	0b
[4]	This bit will be set if 66 PCI Address Parity Error is detected and Index 55h-54h bit4 is enabled.	0b
[3:0]	Reserved.	0h

AGP Arbiter Control Register (CR_GPBER)
CSE Offset: 57h Read/Write

Bits	Function	Default
[7:4]	Reserved	Undefined
[3]	Bus Parking Function Mode Enable / Disable bit : 0 : Disable. 1 : Enable. When this bit is enabled, the AGP bus will park on the M1621. This bit must set to 1 for normal operation.	0b (Disable)
[2:0]	Reserved.	000b

66 PCI Master Device Multiple Transaction Timer (CR_GPMDMT)
CSE Offset: 58h Read/Write

Bits	Function	Default
[7:0]	Time Slice Timer for AGP Master Device to issue Multiple Transactions : 00h : Default. This register is used to control the AGP clock count which the AGP master can occupy AGP bus to issue multiple transactions. When the count is up and the final issued cycle is finished, the AGP arbiter will allow the M1621 an AGP bus access. A value of 1Fh is recommended for normal operation.	00h (Indefinite)

66 PCI Bridge Multiple Transaction Timer (CR_GPBMT)
CSE Offset: 59h Read/Write

Bits	Function	Default
[7:0]	Time Slice Timer for M1621 to Issue Multiple Transactions : 00h : Default. This register is used to control the AGP clock count which the M1621 can occupy AGP bus to issue multiple transaction. When the count is up and the final issued cycle is finished, the AGP arbiter will allow the AGP master a DRAM bus access. A value of 1Fh is recommended for normal operation.	00h (Indefinite)

P2P Bridge Retry Counter Register(CR_P2PRCR)
CSE Offset: 5Ah Read/Write

Bits	Function	Default
[7:0]	P2P Retry Counter : The P2P master functional block will reissue the P2P slave posted write cycle on another PCI bus following this number. When the counter expires, the P2P master functional block will abort this current posted cycle. A value of 0Fh is recommended for normal operation. 02h - Default (retry twice).	02h (Retry twice)

Reserved
CSE Offset: 5Bh Read
Default : 00h

PCI CLKRUN Control Register (CR_PCLKRUN)
CSE Offset: 5Ch Read/Write

Bits	Function	Default
[7:1]	Reserved.	00h
[0]	SERRJ/CLKRUNJ Pin Function Select : 0 : SERRJ. 1 : CLKRUNJ. If this bit is enabled, SERRJ/CLKRUNJ pin on the PCI bus will be used as CLKRUNJ function and compliant to CLKRUNJ protocol in PCI Mobile Design Guide. Otherwise, the SERRJ function is selected.	0b

Reserved
CSE Offset: 5F ~ 5Dh Read
Default : 00h

Host to PCI Memory-Write Enhancement Register (CR_HWEN)
CSE Offset: 60h Read/Write

Bits	Function	Default
[7]	PCI to Memory Write Cannot Allocate Buffer : 0 : Busy wait for buffer. 1 : Retry PCI Master cycle. When the PCI master issues a write cycle to memory and the MWB is full, the PCI master cycle will keep waiting until the buffer has the space to serve this cycle if this bit is reset to 0. Otherwise, the M1621 will retry this PCI master cycle.	0b (Busy wait)
[6]	PCI Write Cycle Data Flow Rate. 0 : 1-1-1-1. 1 : 2-2-2-2. This bit is used to control the data flow rate for the PCI master write cycle.	0b (1-1-1-1)
[5]	Write Control Bit for P2P Device ID. 0 : Disabled. 1 : Enabled. When this bit is set, the P2P bridge device ID (Index 03h-02h) can be written to any value. Otherwise, the P2P bridge device ID is read-only. The Default value is 0x5247h.	0b (Disabled)
[4]	PCI Slave Lock Acceptance Enable : 0 : Disabled. 1 : Enabled. When this bit is disabled, the M1621 will ignore the PCI bus lock signal. Otherwise, it will monitor the lock signal.	0b (Disabled)
[3]	PCI DEVSEL# Response Timing : 0 : Medium. 1 : Slow. This bit is used to select the response timing for the PCI bus. When this bit is reset to 0, medium timing is selected. Otherwise, slow timing is selected.	0b (Medium)
[2]	Posted All Memory Write Cycles of CPU to 33pci : 0 : Disable. 1 : Enable. This bit combines with Index 62h bit0 = 1 to enhance the defer mode performance. When this bit is enabled and defer mode is selected, all host memory cycle will post to the 33 PCI write buffer. This bit must be disabled when Index 62h bit0 is reset to 0.	0b
[1]	Host Memory Write Line or QW-Combining Enable/Disable : 0 : Disable. 1 : Enable. When this bit is enabled, the 33 PCI master state machine will perform burst and QWORD combining before the posted cycle is written to the PCI bus.	0b (Disabled)
[0]	Partial Write - QW Combining Enable on USWC Region : 0 : Disable. 1 : Enable. When this bit is enabled, the USWC post write buffer will perform QWORD combination.	0b (Disabled)

PCI Master Device Pre-Fetch & Post-Write Control Register (CR_PMFW)
CSE Offset: 61h Read/Write

Bits	Function	Default
[7]	PCI Spec. 2.1 Cache Line Wrap Mode Enable / Disable. 0 : Disable. 1 : Enable. When this bit is set to 1 and the PCI master issues a cache line wrap mode burst access (AD[1:0]=10b during Memory access), the M1621 will disconnect this PCI master burst access to become single access.	0b (Disable)
[6]	Partial Write Byte Combining Enable / Disable : 1 : Enabled. 0 : Disable. When this bit is enabled, the partial data will be posted until the address on 33 PCI side location is not continuous. Otherwise, the partial data will be flushed when the transaction is completed.	0b (Disable)
[5]	PCI Single Read Hit Enable / Disable : 0 : Disable. 1 : Enable. When the PCI issues a single DW, the M1621 will pre-fetch a line. When this bit is disabled, the single DW reads will be treated individually. Which means the next single read will cause the M1621 to pre-fetch a line again. When this bit is enabled, the single DW reads will be treated as line_unit_group. Which means the next single read will return data from the previous pre-fetch line if the address is read-hitting the line.	0b (Disable)
[4]	PCI Delayed Transaction Function Enable / Disable : 0 : Disable. 1 : Enable. When this bit is disabled, the M1621 will keep the PCI master waiting if the target initial latency (8 PCI Clocks) of the first data does not obey the PCI 2.1 spec. When this bit is enabled, the M1621 will retry the PCI master if the target initial latency (8 PCI Clocks) of the first data meets the PCI 2.1 spec.	0b (Disable)
[3]	PCI Master Guarantee Mode (Retry Priority Queue) Enable / Disable 0 : Disable. 1 : Enable. When this mode is enabled, the M1621 will memorize the retry PCI master and put this master as the top priority when the PCI request comes back.	0b (Disable)
[2:0]	Pre-fetch Prediction for PCI Read Line/Multiple Command : 000 : One Line mode, 001 : Dual line mode, 010 : Three line mode, 011 : Four mode, 100 : Adaptive Mode, started from one line, 101 : Adaptive Mode, started from two lines, 110 : Adaptive Mode, started from three lines, 111 : Adaptive Mode, started from four lines. These three bits are used to select the pre-fetch line mode for the PCI master read Line/Multiple command. One (000b), dual (001b), three (010b), and four (011b) line mode mean the pre-fetch line count for the PCI master read Line/Multiple command. Adaptive mode means the M1621 will fetch increasing line count if the PCI master keeps reading hit the pre-fetch buffer data.	000b (One line mode)

PCI Bridge Command Register (CR_PCMD)
CSE Offset: 62h Read/Write

Bits	Function	Default
[7]	PCI 2.1 Latency Compliant Mode for PCI Bus. 0: Disable. 1: Enable. This bit combines with the Index 61h bit4 to control the delay transaction feature. This bit is used to control the latency of second, third, and the next data. Note: This bit can only be enabled if Index 61h bit4 is enabled, Otherwise, it will cause a system fail.	0b (Disable)
[6]	Issue DEFERJ When Bridge Slave Report Hard Failure in Defer-Reply Cycle : 0 : Disable. 1 : Enable. This bit is used to control the DEFERJ assertion during the snoop phase when defer mode is selected and a Hard Failure response is going to reply to the CPU. When this bit is enabled, the DEFERJ signal will be asserted during the snoop phase. Otherwise, the DEFERJ signal will not be asserted during the snoop phase.	0b (Disable)
[5]	Issue DEFERJ When Bridge Slave Reports Hard Failure in Synchronous Mode : 0 : Disable. 1 : Enable. This bit is used to control the DEFERJ assertion during the snoop phase when synchronous mode is selected and a Hard Failure response is going to the CPU. When this bit is enabled, the DEFERJ signal will be asserted during the snoop phase. Otherwise, the DEFERJ signal will not be asserted during the snoop phase.	0b (Disable)
[4]	Enable/Disable the M1621 to Issue PCI Lock Access : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 will pass a Host side lock cycle to the PCI bus. Otherwise, the M1621 will ignore the Host side lock signal.	0b (Disable)
[3]	Enable/Disable the M1621 to Transfer Lock Access to P6 Bus : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 will pass a PCI bus lock cycle to the Host side. Otherwise, the M1621 will ignore the PCI bus lock signal.	0b (Disable)
[2]	Transfer The Shutdown Special Cycle to I/O Port 92 Write Cycle : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 will transfer a Host shutdown special cycle to I/O port 92 write cycle. Otherwise, a PCI special cycle will be issued.	0b

PCI Bridge Command Register (CR_PCMD) continued
CSE Offset: 62h Read/Write

Bits	Function	Default
[1]	Criterion of Defer Retry the Entry on Top of I.O.Q. : 0 : When the O.B.Q. is full. 1 : When Both of O.B.Q. and I.B.Q. are full. When this bit is reset to 0, the cycle at the top of I.O.Q. will be defer retried if the O.B.Q is full. O.B.Q is the out bound queue to the PCI bus. When this bit is set to 1, the cycle at the top of I.O.Q. will only be defer retried if the O.B.Q and I.B.Q are full. I.B.Q is the input bound queue from the PCI bus.	0b
[0]	PCI Bridge Side Enhancement Mode : 0 : Synchronous Mode. 1 : Deferred Mode. When synchronous mode is selected, the M1621 will stall the CPU to PCI cycle during the Snoop phase until the cycle is passed to the PCI bus. If synchronous mode is selected, disable the I/O posted write buffer (Index 4Ah bit 0, bit2, bit4, and bit 6 must be reset to 0) and PCI-33 memory post write buffer (index 60h bit 2 must be reset to 0) due to chip limitation. Otherwise, the M1621 will defer this cycle and use defer reply when this cycle is passed to the PCI bus.	0b (Synchronous Mode)

PCI Bridge Retry Counter Register (CR_PBRC)
CSE Offset: 63h Read/Write

Bits	Function	Default
[7:0]	PCI Retry Counter : the PCI master functional block will reissue the O.B.Q. command entry on the PCI bus following this number. When the counter expires, the PCI master functional block will abort the O.B.Q. command entry and terminate the Host cycle. A value of 0Fh is recommended for normal operation. 02h - Default (retry twice).	02h (Retry twice)

PCI Bridge Error Command Register (CR_PBECR)
CSE Offset: 65 ~ 64h Read/Write

Bits	Function	Default
[15:9]	Reserved	Undefined
[8]	Issue SERRJ When the M1621 Issues Host Cycle to the PCI Bus And That Cycle Is Master Aborted : 0 : Does not assert SERRJ. 1 : Assert SERRJ. This bit is used to control the condition when the Host issues a cycle to 66 PCI bus and this cycle is master aborted. When this bit is reset to 0, the M1621 will ignore this condition and terminate the Host cycle with the reply defined in bit7 (Normal reply or Hard Failure). When this bit is set to 1, the status bit defined in Index 07h-06h bit14 and Index 07h-06h bit13 will be set to 1. If P2P bridge Index 05h-04h bit8 is enabled, the M1621 will drive the PCI SERRJ signal to notify the south bridge to issue NMI to the CPU.	0b (Report Hard Failure)
[7]	Report Normal or Hard Failure When The PCI Host Cycle Is Master Aborted : 0 : Normal. 1 : Hard Failure. When bit8 is reset to 0, the Host issues a cycle to the PCI bus and this cycle is master aborted, the M1621 will terminate the Host cycle with Normal reply if this bit is reset to 0. Otherwise, a Hard Failure is replied to the Host bus.	0b (Normal)
[6]	Reserved.	0b
[5]	Issue SERRJ on Received Data Parity Error : 0 : Disable. 1 : Enable. When the M1621 detects the parity error occurring when the external master writes data to DRAM or the M1621 reads data from the PCI device and this bit is enabled, the status bit defined in Index 66h bit5 and Index 07h-06h bit15 will be set to 1 and the M1621 will drive the PCI SERRJ signal to notify the south bridge to issue NMI to the CPU if Index 05h-04h bit8 is enabled.	0b (Disable)
[4]	Issue SERRJ on Address Parity Error detecting : 0 : Disable. 1 : Enable. When the M1621 detects the PCI bus address parity error, the status bit defined in Index 66h bit4 and Index 07h-06h bit15 will be set to 1 and the M1621 will drive PCI SERRJ signal to notify the south bridge to issue NMI to CPU if Index 05h-04h bit8 is enabled.	0b (Disable)
[3]	Reserved.	0b
[2]	When the PCI Host Cycle Be Target Aborted Will Report SERRJ : 0 : Disable. 1 : Enable. This bit is used to control the condition when the Host issues a cycle to the PCI bus and this cycle is target aborted. When this bit is reset to 0, the M1621 will ignore this condition and terminate the Host cycle with Normal reply. When this bit is set to 1, the status bit defined in Index 07h-06h bit14 and Index 07h-06h bit12 will be set to 1. If Index 05h-04h bit8 is enabled, the M1621 will drive PCI SERRJ signal to notify the south bridge to issue NMI to the CPU.	0b (Disable)

PCI Bridge Error Command Register (CR_PBECR) Continued

CSE Offset: 65 ~ 64h Read/Write

Bits	Function	Default
[1]	ECC Single-Bit Error issues SERRJ Enable / Disable : 0 : Disable. 1 : Enable. When an ECC single bit error has occurred and this bit is enabled, Index 07h-06h bit14 and Index 66h bit1 will be set to 1 and issue SERRJ if Index 05-04h 08h is enabled.	0b (Disable)
[0]	ECC Multiple-Bits Error issues SERRJ Enable / Disable : 0 : Disable. 1 : Enable. When an ECC multiple-bit error has occurred and this bit is enabled, Index 07h-06h bit14 and Index 66h bit0 will be set to 1 and issue SERRJ if Index 05-04h 08h is enabled.	0b (Disable)

PCI Bridge Error Status Register (CR_PBECR)

CSE Offset: 66h Read Only & Write One to Clear

Bits	Function	Default
[7:6]	Reserved.	Undefined
[5]	This bit will be set if the M1621 PCI Data Parity Error is detected when the external master writes data to DRAM or the M1621 reads data from the PCI device and Index 65h-64h bit5 is enabled.	0b
[4]	This bit will be set if a PCI Address Parity Error is detected and Index 65h-64h bit4 is enabled.	0b
[3:2]	Reserved.	Undefined
[1]	Memory Data ECC Single-Bit Error : This bit will be set to 1 when a memory data ECC single bit error is detected and Index 66h-65h bit1 is enabled.	0b
[0]	Memory Data ECC Multiple-Bits Error : This bit will be set to 1 when a memory data ECC multiple bit error is detected and Index 66h-65h bit1 is enabled.	0b

PCI Arbiter Control Register (CR_PBER)

CSE Offset: 67h Read/Write

Bits	Function	Default
[7]	Guarantee Mode for All PCI Masters : 0 : Disable. 1 : Enable. When this bit is enabled, cycles pending in IOQ/OBQ will be flushed before grant to requesting masters.	0b (Disable)
[6]	Guarantee Mode for PCI Master 2 : 0 : Disable. 1 : Enable. When this bit is enabled, cycles pending in IOQ/OBQ will be flushed before grant to PCI Master 2.	0b (Disable)
[5]	PHOLDJ/PHLDAJ Timing : 0 : PHLDAJ is de-asserted when PHOLDJ is de-asserted for 2 clocks. 1 : PHLDAJ is de-asserted once PHOLDJ is de-asserted. When this bit is reset to 0, the M1621 will de-assert PHLDAJ only when PHOLDJ is de-asserted for more than 2 PCI clocks. The M1621 will not de-assert PHLDAJ if PHOLDJ is not de-asserted or just de-asserted for 1 PCI clock. When this bit is set to 1, the M1621 will de-assert PHLDAJ once PHOLDJ is de-asserted.	0b (Disable)
[4]	Release Delay Transaction when PHLDAJ occurs : 0 : Disable. 1 : Enable. When this bit is enabled and the PCI delay transaction feature is enabled, the pre-fetch line for the delay transaction PCI master will be invalidated when PHLDAJ is asserted. This bit must be set to 1 for normal operation when the PCI delay transaction feature is enabled.	0b (Disable)
[3]	Bus Parking Function Mode Enable / Disable Bit : 0 : Disable. 1 : Enable. When this bit is enabled, the PCI bus will park on the M1621. This bit must set to 1 for normal operation.	0b (Disable)
[2]	ISA Guarantee Mode Enable / Disable Bit : 0 : Disable. 1 : Enable. When this bit is enabled, cycles pending in IOQ/OBQ will be flushed before grant to south bridge.	0b (Disable)
[1]	Passive Release Enable / Disable Bit : 0 : Disable. 1 : Enable. When this bit is enabled and arbiter grants to a south bridge by asserting PHLDAJ, the M1621 will grant to Host bus if the south bridge de-asserts PHOLDJ for one PCI clock to notify the M1621 it can access the PCI bus.	0b (Normal)
[0]	Complete Bus Lock Function Enable / Disable Bit : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 PCI arbiter will monitor PCI lock signal and will not grant to another master to guarantee the lock access. Otherwise, it will ignore PCI lock signal.	0b (Disable)

PCI Master Device Multiple Transaction Timer (CR_PMDMT)
CSE Offset: 68h Read/Write

Bits	Function	Default
7:0]	Time Slice Timer for PCI Master Device to issue Multiple Transactions : 00h : Default. This register is used to control the PCI clock count which the PCI master can occupy PCI bus to issue multiple transactions. When the count is up and the final issued cycle is finished, PCI arbiter will grant the M1621 access to PCI bus A value of 1Fh is recommended for normal operation.	00h (Indefinite)

PCI Bridge Multiple Transaction Timer (CR_PBMT)
CSE Offset: 69h Read/Write

Bits	Function	Default
[7:0]	Time Slice Timer for the M1621 to issue Multiple Transactions : 00h : Default. This register is used to control the PCI clock count which the M1621 can occupy PCI bus to issue multiple transactions. When the count is up and the final issued cycle is finished, the PCI arbiter will grant the PCI master access to the DRAM bus. A value of 1Fh is recommended for normal operation.	00h (Indefinite)

Reserved
CSE Offset: 6B ~ 6Ah Read
Default : 00h

Memory Bank Register (CR_MROW0 ~ 3)
CSE Offset: 6F ~ 6Ch, 73 ~ 70h, 77 ~ 74h, 7B ~ 78h Read/Write

Bits	Function	Default
[31]	MA Assertion in Deactivate (Pre-charge) Command (for SDRAM only) : 0 : Normal. 1 : 1 Host Clock before De-activate command. When this bit is reset to 0, 2 Host Clocks MA setup time for deactivate command is selected. When this bit is enabled, one more Host Clock wait delay to add MA setup time for deactivate command will be added.	1b (1 Host Clock)
[30]	Page Hit Insert Wait State (tPHITW) (not for SDRAM) : 0 : Zero wait. 1 : One wait (1 Host Clock). Only used when the DRAM is FPM or EDO When this bit is set to 1, CASJ will be delayed one more Host clock to add MA setup time for a Page Hit cycle. Otherwise, no delay will be added.	1b (One wait)
[29]	Self-Refresh Support for ***EDO/FPM*** in Power-Off Mode : 0 : Self-refresh not supported. 1 : Self-refresh Supported. When the DRAM is FPM or EDO, this bit is used to select the DRAM refresh protocol. If this bit is reset to 0, the M1621 will support the DRAM self-refresh protocol. Otherwise, CAS-before-RAS protocol will be used for refresh. Or ***SDRAM*** CAS Latency (CL) : 0 : 2 Host Clocks. 1 : 3 Host Clocks. When theDRAM SDRAM, this bit is used to select CAS Latency.	1b (Self refresh not supported for EDO/FPM) (CL = 3 for SDRAM)
[28:27]	DRAM Type : 00 : Fast Page Mode DRAM. 01 : EDO Page Mode DRAM. 10 : Synchronous DRAM. 11 : Reserved. These two bits are used to program the DRAM type for this bank. A bank has two rows.	00b (Fast Page Mode)
[26:25]	1st Row Existence Status : 00 : Not present. 01 : Reserved. 10 : Reserved. 11 : 64 or 72 bits present. These two bits are used to present the first row status: Not present or 64 or 72 bits present.	6C:11b others : 00b (Not present)
[24:23]	2nd Row Existence Status : 00 : Not present. 01 : Reserved. 10 : Reserved. 11 : 64 or 72 bits presented. These two bits are used to present the second row status: Not present or 64 or 72 bits present.	00b (Not presented)

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Memory Bank Register (CR_MROW0 ~ 3) continued
CSE Offset: 6F ~ 6Ch, 73 ~ 70h, 77 ~ 74h, 7B ~ 78h Read/Write

Bits	Function	Default
[22:20]	DRAM Row size : 000 : 4 MB. 001 : 8 MB. 010 : 16 MB. 011 : 32 MB. 100 : 64 MB. 101 : 128 MB. 110 : 256 MB. 111 : Reserved. The BIOS needs to write the correct Row size to these three bits. The M1621 will use this row size to calculate the bank size. Total memory size is the sum of the four banks.	000b (4 MB)
[19:16]	DRAM Column Address Type : 0000 : 8 bits column address. 0001 : 9 bits column address. 0010 : 10 bits column address. 0011 : 11 bits column address. (EDO / FPM only) 0100 : 12 bits column address. (EDO / FPM only) 0101 ~ 1110 : Reserved. 1111 : User-Defined Type, and set CSE with offset FFh ~ F0h, (SDRAM only). These three bits are used to program the column address type. Refer to the MA mapping table listed in section 3.1.1. When these four bits are programmed as 1111b, the user can define the SDRAM type through Index FFh-F0h programming.	0000b (8 bit column address)
[15]	Row Address Setup Time (tASR) : for ***EDO/FPM*** 0 : Normal. 1 : Longer. When this bit is set to 1, one more MA address setup time for RASJ will be added for EDO/FPM. Activation of Control Signals Qualified by Chip Select : for ***SDRAM*** only : 0 : Active one clock before Chip Select active. 1 : Active at the same clock as Chip Select active. When this bit is reset to 0, activation of the control signal will be asserted one clock ahead of CSJ assertion. Otherwise, they will assert on the same clock edge.	1b (Longer for EDO/FPM) (Same Clock for SDRAM)
[14:13]	Row Address Hold Time (tRAH) for ***FPM/EDO*** : 00 : 1 Host Clock. 01 : 2 Host Clocks. 10 : 3 Host Clocks. 11 : 4 Host Clocks. These two bits are used to program the MA address hold for RASJ assertion. or Bank Select Signals Detection Results for ***SDRAM*** *:* [14] 0 : MA14 is not bank select signal. [14] 1 : MA14 is bank select signal. [13] 0 : MA13 is not bank select signal. [13] 1 : MA13 is bank select signal. When Index 84h bit0 SDRAM bank detection is enabled, the M1621 will automatically detect SDRAM bank select signals and write to bits[14:11] respectively. The BIOS can read the content and write to bits[3:0]. The M1621 will take the appropriate action based on the content of bits[3:0].	11b (4 Host Clocks)

Memory Bank Register (CR_MROW0 ~ 3) continued
CSE Offset: 6F ~ 6Ch, 73 ~ 70h, 77 ~ 74h, 7B ~ 78h Read/Write

Bits	Function	Default
[12:11]	CAS Address Setup Time (tASC) for ***FPM/EDO*** *:* 00 : 1 Host Clock. 01 : 2 Host Clocks. 10 : 3 Host Clocks. 11 : 4 Host Clocks. These two bits are used to program the MA address setup time for CASJ assertion. or Bank Select Signals Detection Results for ***SDRAM*** *:* [12] 0 : MA12 is not bank select signal. [12] 1 : MA12 is bank select signal. [11] 0 : MA11 is not bank select signal. [11] 1 : MA11 is bank select signal. When Index 84h bit0 SDRAM bank detection is enabled, the M1621 will automatically detect SDRAM bank selection signals and write to bits[14:11] respectively. The BIOS can read the content and write to bits[3:0]. The M1621 will take the appropriate action based on the content of bits[3:0].	11b (4 Host Clocks)
[10:9]	Write CASJ Timing (tCAS) for ***FPM/EDO*** : 00 - 1 Clock. 01 - 2 Clocks. 10 - 3 Clocks. 11 - 4 Clocks. These two bits are used to program the active write CASJ low pulse width.	11b (4 Clocks)
[8:7]	Read CASJ Timing (tCAS) for ***FPM/EDO*** : 00 - 1 Clock. 01 - 2 Clocks. 10 - 3 Clocks. 11 - 4 Clocks. These two bits are used to program the active read CASJ low pulse width.	11b (4 Clocks)
[6]	CASJ Pre-charge Timing (tCP) for ***FPM/EDO*** *:* 0 : 1 Clock. 1 : 2 Clocks. This bit is used to program the CASJ pre-charge time. Or ***SDRAM*** type : 0 - Registered. 1 - Normal. When this bit is programmed as registered the M1621 will delay the data strobe point for one clock to meet the behavior of register SDRAM.	1b (2 Clocks for FPM/EDO) or (Normal for SDRAM)

Memory Bank Register (CR_MROW0 ~ 3) Continued
CSE Offset: 6F ~ 6Ch, 73 ~ 70h, 77 ~ 74h, 7B ~ 78h Read/Write

Bits	Function	Default
[5:4]	CASJ Hold Timing (tCSH,) for ***FPM/EDO*** : 00 : 3 Clocks. 01 : 4 Clocks. 10 : 5 Clocks. 11 : 6 Clocks. These two bits are used to program the CASJ de-assertion to RASJ de-assertion clock. or for ***SDRAM*** : [5] : Activate to Command Delay (tRCD) [4] : RAS Pre-charge Time (tRP) tRCD, tRP 00 : 2 Clocks, 2 Clocks. 01 : 2 Clocks, 3 Clocks. 10 : 3 Clocks, 2 Clocks. 11 : 3 Clocks, 3 Clocks. These two bits are used to program SDRAM tRCD and tRP.	11b (6 Clocks) or (3/3 Clocks)
[3:2]	RASJ Pulse Duration (tRAS,), for ***FPM/EDO*** : (must be >= tCSH) 00 : 3 Clocks. 01 : 4 Clocks. 10 : 5 Clocks. 11 : 6 Clocks. These two bits are used to select the minimum RASJ pulse duration. It must be larger or equal to tCSH. or Bank Selecting Signals for ***SDRAM*** to Open Multi-Banks : 00 : Reserved. 01 : Reserved. 10 : See [1:0] further. 11 : See [1:0] further.	11b (6 Clocks) or (see [1:0])

[1:0]	RASJ Pre-charge Timing (tRP,) for ***FPM/EDO*** only :
	00 : 2 Clocks.
	01 : 3 Clocks.
	10 : 4 Clocks.
	11 : 5 Clocks.
	These two bits are used to program the RASJ pre-charge time.
	or Bank Selecting Signals for ***SDRAM*** to Open Multi-Banks :
	if [3:2] = 10 then
	00 : MA11.
	01 : MA12.
	10 : MA13.
	11 : MA14.
	Else if [3:2] = 11 then
	00 - MA11, MA12.
	01 - MA12, MA13.
	10 - MA13, MA14.
	11 - No Multi-Banking.
	Else
	Reserved.
	End if.
	The BIOS must read the bits[14:11] value to program bits[3:0]. For example, bits[3:0] are set to 1110b if bits[14:11] = 1100b. Which means MA13, and MA14 are bank selection signals for SDRAM.
		11b
		(5 Clocks) or
		(No Multi-Banking)

Memory Command Register (CR_MCMD)
CSE Offset: 7F ~ 7Ch Read/Write

Bits	Function	Default
[31:30]	Memory Data Protection Mode : 0x : No memory protection. 10 : ECC protected memory. 11 : Error Check Only. When these two bits are set as 10b, ECC protected memory algorithm will be used. Which means single bit error will be corrected and multiple bits error will be reported. When these two bits are set as 11b, only error checking is selected and reported. The M1621 will not correct any single bit error.	00b (Disable)
[29:28]	Memory Write Buffer (MWB) Allocation Policy : 0x : Depth set to 2. 10 : Depth set to 8, dynamically allocated for PCI and Host access. 11 : Depth set to 8, fixed allocated for PCI. 8 Lines (1 Line = 4 QWORDs) Memory Write Buffer is implemented in the M1621 and they are shared by the PCI master and the Host DRAM access. When these two bits are programmed as 0xb, only 2 lines are used: one line is dedicated for the PCI master access, and the other one is dedicated for the Host DRAM access. When these two bits are programmed as 10b, all 8 lines will be used and dynamically allocated for both PCI and Host access. When these two bits are programmed as 11b, 4 lines are dedicated for the PCI master access, and the other four lines are dedicated for the Host DRAM access.	00b (Depth set to 2)
[27]	Refresh Queue Depth (REFHQ) : 0 : 0 entry. 1 : 4 entries. 4 entries DRAM refresh queues are implemented in the M1621. When 0 entry is selected, the M1621 will do the DRAM refresh immediately when the programmed time in bits[13:0] is up. Otherwise, it will push to the refresh queue first, wait for the idle clock defined in bits[26:24], and then do the DRAM refresh.	0b (0 entry)
[26:24]	Refresh Starting Control (enabled only when REFHQ = 4 entries) : 000 : 5 extra idle clocks. 001 : 10 extra idle clocks. 010 : 15 extra idle clocks. 011 : 20 extra idle clocks. 100 : 25 extra idle clocks. 101 : 30 extra idle clocks. 110 : 35 extra idle clocks. 111 : 40 extra idle clocks. Refer to bit[27].	000b (5 Clocks)
[23:22]	Auto-Flush Starting Control (AFIDLE) : 00 : 4 clocks of memory slave idle cycles. 01 : 8 clocks of memory slave idle cycles. 10 : 12 clocks of memory slave idle cycles. 11 : 16 clocks of memory slave idle cycles. These two bits are used to select the DRAM bus idle clock to start flushing the MWB. When the programmed clocks are up, the M1621 memory controller will start to flush the MWB.	11b (16 Clocks)

Memory Command Register (CR_MCMD) Continued
CSE Offset: 7F ~ 7Ch Read/Write

Bits	Function	Default
[21]	DRAM Refresh Envelope Pin (RFHENV) Function : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 will drive the RFHENV pin high to notify DRAM refresh is proceeding. Otherwise, the RFHENV pin will remain low.	0b (Disable)
[20]	EDO Detect Mode : 0 : Disable. 1 : Enable. When this bit is set to 1, EDO detect mode is enabled. Refer to section 5.2 software programming guide for more information.	0b (Disable)
[19]	DRAM Refresh Enable : 0 : Disable. 1 : Enable. This bit is used for the DRAM type interrogation as defined in section 5.2. Note: Remember to enable after the DRAM type is determined, otherwise, DRAM refresh will be disabled and the content will be lost.	0b (Disable)
[18]	DRAM Refresh Cycle, CASJ Low to RASJ Low Timing : 0 : 1 Clock. 1 : 2 Clocks. This bit is used to program the CASJ low to RASJ low timing during DRAM refresh cycle.	1b (2 Clocks)
[17:16]	DRAM Refresh Cycle, RASJ Pulse Duration Timing (tRAS) : 00 : 3 Clocks. 01 : 4 Clocks. 10 : 5 Clocks. 11 : 6 Clocks. These two bits are used to program the RASJ pulse duration (low clock) timing during DRAM refresh cycle.	11b (6 Clocks)
[15:14]	DRAM Refresh cycle, RASJ Pre-charge Timing (tRP) : 00 : 2 Clocks. 01 : 3 Clocks. 10 : 4 Clocks. 11 : 5 Clocks. These two bits are used to program the RASJ pre-charge timing during DRAM refresh cycle.	11b (5 Clocks)
[13:0]	DRAM Refresh Cycle : This is determined by the host bus clock rate. It shall be set to 15.620µsec for 50MHz, or 781 clocks; 15.616µsec for 60MHz, or 937 clocks; 15.615µsec for 66.66MHz, or 1041 clocks; 15.615µsec for 100MHz, or 1560(618h) clocks.	1041d (or 411h)

Host Interface Configuration Register (CR_HCFG)
CSE Offset: 81 ~ 80h Read/Write

Bits	Function	Default
[15]	CASJ Layout : 0 : One-to-one. 1 : Cross-bar. When one-to-one mode is selected, the layout should connect the M1621 CASJ[0] to all CASJ[7:0] of row 0, CASJ[1] to all CASJ[7:0] of row 1, .., CASJ[7] to all CASJ[7:0] of row 7. When cross-bar is selected, the layout should connect the M1621 CASJ[7:0] to CASJ[7:0] of all rows. The BIOS should write the correct system layout to this bit, as it will affect the DRAM timing.	0b (One-to-One)
[14]	Command Decoding : 0 : Normal (default). 1 : Fast. When normal decoding is selected, T4 is the command decoding point. Otherwise, T3 is the point for command decoding.	0b (Normal)
[13]	Reserved.	0b
[12]	Global In-Order-Queue Depth (Read Only) : 0 : Depth 8 queue, 1 : Depth 1 queue. This is the latch value of the In-Order-Queue.	Capture from A[7] during RESET.
[11:10]	Local In-Order-Queue Depth : 00 : Depth 1 queue. 01 : Depth 2 queue. 10 : Depth 4 queue. 11 : Depth 8 queue. The M1621 can change the internal In-Order-Queue Depth through these two bits. This number must be equal to or less than the Global In-Order-Queue Depth.	11b (depth 8 queue)
[9:8]	APIC Cluster ID : A[12:11] driving value during RESET (Read Only) These two bits are the Latch value of APIC Cluster ID.	00b
[7]	A[10] Driving Value for Next RESET (BINITJ Observation Policy, Read Only) : 0 : Disable. 1 : Enable. This bit is the latch value of BINITJ Observation Policy.	0b (Disable)
[6]	A[9] driving value for next RESET (BERRJ observation policy, Read Only) : 0 : Disable. 1 : Enable. This bit is the latch value of BERRJ observation policy.	0b (Disable)
[5]	A[8] Driving Value for Next RESET (AERRJ observation policy, Read Only) : 0 : Disable. 1 : Enable. This bit is the latch value of AERRJ observation policy.	0b (Disable)
[4]	A[6] Driving Value for Next RESET (Power-on Reset Vector, Read Only) : 0 : 0FFFF_FFF0h. 1 : 0FFFF0h. This bit is the latch value of Power-on Reset Vector.	0b (0FFFF_FFF0h)

Host Interface Configuration Register (CR_HCFG) Continued
CSE Offset: 81 ~ 80h Read/Write

Bits	Function	Default
[3]	A[5] Driving Value for Next RESET (FRC Mode Enable, Read Only) : 0 : FRC disable. 1 : FRC enable. This bit is the latch value of FRC Mode Enable.	Captured from configuration pins during RESET.
[2:1]	Memory Read Buffer Depth : 00 : 1 Cache Line. 01 : 2 Cache Lines. 10 : 4 Cache Lines. 11 : Reserved. The M1621 has implemented 4 cache lines for Host memory read. These two bits can change the available lines for the host memory read.	00b (1 Cache Line)
[0]	Internal Data Buffer Write Cycle Slow Down. 0 : Disable. 1 : Enable. When internal data buffer write cycle slow down function is enabled, internal write to data buffer will slow down one clock. Otherwise, the fastest timing is chosen.	1b (Enable)

PCI Decode Mode Register (CR_PDEC)

CSE Offset: 82h Read/Write

Bits	Function	Default
[7]	Pad Driving Capability Selection for RASJ/CASJ (RCASJ_PR) : 0 : Full driving. 1 : Half driving. This bit is used to control the DRAM command pad driving. Half driving has only one half driving capability of full driving.	0b
[6]	Pad Driving Capability Selection for MA (MA_PR) : 0 : Full driving. 1 : Half driving. This bit is used to control the DRAM MA pad driving. Half driving has only one half driving capability of full driving.	0b
[5]	Pad Driving Capability Selection for MD (MD_PR) : 0 : Full driving. 1 : Half driving. This bit is used to control the DRAM data pad driving. Half driving has only one half driving capability of full driving.	0b
[4]	Number of DIMMs (For CKEs Multiplexing) : 0 : 4 DIMMs. 1 : Not 4 DIMMs. When not 4 DIMMs mode is selected, SRASJ[3], SCASJ[3], MWEJ[3], RASJ[7:6] will become CKEs function for SDRAM self refresh. This is the preferred layout for a 3-DIMM motherboard implementation. Otherwise, only one CKE is available and need to be buffered to drive the four DIMM CKEs inputs.	0b (4 DIMMs)
[3]	Reserved.	0b
[2]	Monochrome Device Adapters Presence : 0 : Disable (MDA is not present). 1 : Enable (MDA presence). If this bit is 1, the following standard MDA resources will be directed to 33MHz PCI Bus. Memory : 0B0000h - 0B7FFFh. I/O : 3B4h,3B5h,3B8h,3B9h,3BAh,3BFh. Otherwise, the cycle will pass to AGP bus.	0b (Disable)
[1]	High I/O Address Mask Enable : 0 : Disabled, passed on as received. 1 : Enabled, outbound I/O request address [31:16] will be fixed to zero. When this bit is enabled, the M1621 will mask I/O request address [31:16] before it issues this cycle. Otherwise, no masking will be done by the M1621.	0b (Disable)
[0]	ISA I/O Address Aliasing : 0 : Disable, passed on as received. 1 : if I/O request address A[9:8] are not both 0, A[15:10] will be alias to 0. When this bit is set to 1, the M1621 will alias A[15:10] to become 00h if I/O request address A[9:8] are not both 0. Otherwise, the M1621 will pass the address as received.	0b (Disable)

A/B Page and SMM Range Register (CR_MSMM)
CSE Offset: 83h Read/Write

Bits	Function	Default
[7]	A0000 ~ BFFFFh Read Enable **(SMREN)** : 0 : Disable. 1 : Enable. When this bit is disabled, memory address A0000 ~ BFFFFh read requests will be forwarded to the PCI Bridge. Otherwise, memory address A0000 ~ BFFFFh read requests are handled based on SMRAM and SMMENJ bit of the corresponding requests.	0b (Disable)
[6]	A0000 ~ BFFFFh, Write Enable **(SMWEN)** : 0 : Disabled. 1 : Enabled. When this bit is disabled, memory address A0000 ~ BFFFFh write requests will be forwarded to the PCI Bridge. Otherwise, memory address A0000 ~ BFFFFh write requests are handled based on SMRAM and SMMENJ bit of the corresponding requests.	0b (Disable)
[5:4]	SMM Memory Range Access Mode **(SMRAM[1:0])** : 00 : Close. 01 : Open. 10 : Lock. 11 : Protected. The request handling is based on its SMM bit and code or data references and illustrated in the following table.	00b (Close)
[3]	SMM Default Range Re-mapping : 0 : Disable. 1 : Enable. When this bit is enabled, requests with SMM bit set and target at 38000h ~ 3FFFFh address range will be re-mapped to A8000h ~ AFFFFh. Otherwise, no re-mapping will be done.	1b (Enable)
[2]	A0000 ~ BFFFFh USWC Mode Enable : 0 : Disable. 1 : Enable. This bit is used to enable USWC mode for memory address range A0000 ~ BFFFFh.	0b (Disable)
[1:0]	Reserved.	Undefined

The following table shows the response of requests targeting at SMM space (0A_0000h ~ 0B_FFFFh.)

SMREN/SMWEN	SMM	Mode	Code	Data
Disabled	X	X	PCI	PCI
Enabled	No	Close, Lock, Protect	PCI	PCI
Enabled	No	Open	DRAM	DRAM
Enabled	Yes	Open, Protect	DRAM	DRAM
Enabled	Yes	Close, Lock	DRAM	PCI

Memory Attribute Register (CR_MPAM)
CSE Offset: 87 ~ 84h Read/Write

Bits	Function	Default
[31:30]	Reserved.	Undefined
[29:28]	0F0000h - 0FFFFFh, System BIOS Region **(MPAM_F0[1:0])** : [29] 1 : Write Enable, 0 : Write Disable. [28] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0F0000h - 0FFFFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[27:26]	0EC000h - 0EFFFFh, Extended BIOS Region **(MPAM_EC[1:0])** : [27] 1 : Write Enable, 0 : Write Disable. [26] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0EC000h - 0EFFFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[25:24]	0E8000h - 0EBFFFh, Extended BIOS Region **(MPAM_E8[1:0])** : [25] 1 : Write Enable, 0 : Write Disable. [24] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0E8000h - 0EBFFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[23:22]	0E4000h - 0E7FFFh, Extended BIOS Region **(MPAM_E4[1:0])** : [23] 1 : Write Enable, 0 : Write Disable. [22] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0E4000h - 0E7FFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[21:20]	0E0000h - 0E3FFFh, Extended BIOS Region **(MPAM_E0[1:0])** : [21] 1 : Write Enable, 0 : Write Disable. [20] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0E0000h - 0E3FFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[19:18]	0DC000h - 0DFFFFh, ISA Expansion Region **(MPAM_DC[1:0])** : [19] 1 : Write Enable, 0 : Write Disable. [18] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0DC000h - 0DFFFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[17:16]	0D8000h - 0DBFFFh, ISA Expansion Region **(MPAM_D8[1:0])** : [17] 1 : Write Enable, 0 : Write Disable. [16] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0D8000h - 0DBFFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[15:14]	0D4000h - 0D7FFFh, ISA Expansion Region **(MPAM_D4[1:0])** : [15] 1 : Write Enable, 0 : Write Disable. [14] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0D4000h - 0D7FFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)

Memory Attribute Register (CR_MPAM) ***(continued)***

Bits	Function	Default
[13:12]	0D0000h - 0D3FFFh, ISA Expansion Region **(MPAM_D0[1:0])** : [13] 1 : Write Enable, 0 : Write Disable. [12] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0D0000h - 0D3FFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[11:10]	0CC000h - 0CFFFFh, ISA Expansion Region **(MPAM_CC[1:0])** : [11] 1 : Write Enable, 0 : Write Disable. [10] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0CC000h - 0CFFFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[9:8]	0C8000h - 0CBFFFh, ISA Expansion Region **(MPAM_C8[1:0])** : [9] 1 : Write Enable, 0 : Write Disable. [8] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0C8000h - 0CBFFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[7:6]	0C4000h - 0C7FFFh, ISA Expansion Region **(MPAM_C4[1:0])** : [7] 1 : Write Enable, 0 : Write Disable. [6] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0C4000h - 0C7FFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[5:4]	0C0000h - 0C3FFFh, ISA Expansion Region **(MPAM_C0[1:0])** : [5] 1 : Write Enable, 0 : Write Disable. [4] 1 : Read Enable, 0 : Read Disable. When the write/read bit is enabled, the write/read 0C0000h - 0C3FFFh cycle will forward to DRAM. Otherwise, it will forward to the PCI bus.	00b (Write & Read Disable)
[3:1]	Counter for SDRAM Enhanced Pre-charge Mode : 000 : Enhanced Mode Off. 001 : 4 extra idle clocks. 010 : 8 extra idle clocks. 011 : 12 extra idle clocks. 100 : 16 extra idle clocks. 101 : 20 extra idle clocks. 110 : 24 extra idle clocks. 111 : 28 extra idle clocks. These three bits are used to control the idle clocks for SDRAM multiple bank operation. When these three bits are programmed as 000, the M1621 will issue pre-charge all commands to close all the SDRAM pages when DRAM refresh time is up. Otherwise, the M1621 will wait extra idle clocks to issue pre-charge all commands to close DRAM open page.	000b (Off)
[0]	Bank Select Signals Detection for SDRAM : 0 : Disable. 1 : Enable. This bit is used to enabled the SDRAM bank detection algorithm. Write 0 first, then write 1 will enable this function. When this function is enabled, the BIOS should be programmed to wait for 50 us. The M1621 will automatically write the detect data to Index 6Fh - 6C, 73h - 70h, 77h - 74h, and 7Bh - 78h bits[14:11]. The BIOS needs to read the respective bits data and write the result to bits[3:0]. The M1621 internal state machine will be based on bits[3:0] to do multiple-bank operation to enhance SDRAM performance.	0b (Disable)

Memory Gap Range Registers (CR_MRNG)
CSE Offset: 8B ~ 88h Read/Write

Bits	Function	Default
[31]	Host Clock Frequency : 0 : 66 MHz. 1 : 100 MHz. The M1621 will automatically detect host clock frequency and set this bit.	Read Only
[30]	Reserved.	0b
[29:28]	Delay Line Units for Power-Off Mode : 00 : One 20-ns unit. 01 : Two 20-ns units. 10 : Three 20-ns units. 11 : Four 20-ns units. When system is running suspend refresh, the M1621 will use delay line to generate refresh command. These two bits are used to control the delay line time unit.	00b (20 ns)
[27:24]	Extra Idle Clocks to Stop Clocks : [27] : Enable bit : 0 : Disable clock stopping function. 1 : Enable clock stopping function. [26:24] : Extra idle clocks : 000 : 2 host clocks. 001 : 4 host clocks. 010 : 6 host clocks. 011 : 8 host clocks. 100 : 10 host clocks. 101 : 20 host clocks. 110 : 40 host clocks. 111 : 60 host clocks. These four bits are used to enable the clock stop function when the programmed number of clock is up. The M1621 will gate off the Host and DRAM state machines to save power consumption if the bus is idle.	0000b (Disable)
[23:22]	COR_GCLKSEL[1:0] : 00 : Pass through. 01 : Delay one stage. 10 : Delay two stages. 11 : Delay three stages. These two bits can be used to delay the AGP clock input (used by AGP state machine). One stage is about 0.4 ns.	00b
[21:19]	Reserved.	Undefined
[18]	Memory Gap Range Enable : 0 : Disable. 1 : Enable. This bit is used to enable the first memory gap.	0b (Disabled)
[17]	Reserved.	Undefined.
[16]	USWC Mode Enable : 0 : Disable. 1 : Enable. This bit is used to enable the USWC mode for the first memory gap.	0b (Disable)
[15:4]	Starting Address bits [31:20] : Starting address and the size defines the first memory gap range.	000h

Memory Gap Range Registers (CR_MRNG) continued
CSE Offset: 8B ~ 88h Read/Write

Bits	Function	Default
[3]	M_START is clocked out for SDRAM : 0 : Disable. 1 : Enable. When this bit is enabled, the DRAM state machine will delay one clock to issue DRAM command to gain command setup time for one more clock. When the M1621 is running at 100 MHz, this bit will help to get more reliability.	0b (Disable)
[2:0]	Memory Gap Size : 000 : 1MB. 001 : 2MB. 010 : 4MB. 011 : 8MB. 100 : 16MB. 101, 110, 111 : Reserved. These three bits are used to select the second memory gap size. It combines with bits[15:4] to define second memory gap.	000b (1 MB)

*** USWC Mode - Uncacheable, Speculative Write Combining Mode.**

USWC Gap Range Registers (CR_USWC)
CSE Offset: 8F ~ 8Ch Read/Write

Bits	Function	Default
[31]	Register of GTLP_DL : When REFENV is pulled high, this bit will be set to 1 and GTL+ input will delay 3 ns before it gets into internal core. Otherwise, there is no input delay and this bit will be 0.	Captured REFENV during Reset
[30]	Register of HCLKPLL_EN : When AREQJ is pulled high, this bit will be set to 1 and the Host PLL will be enabled. System designer can use this PLL to delay or lead the Host clock for internal Host and DRAM state machines. Otherwise, Host PLL will be disabled, this bit will be 0, and the Host and DRAM state machines will run based on HCLK input.	Captured AREQJ during Reset
[29]	Register of HADV_LAGJ : When PGNTJ4 is pulled high, this bit will be set to 1 and the Host clock for internal Host and DRAM state machines will lead external HCLK input. The lead time will be programmed through HCLK_SEL[2:0]. When PGNTJ4 is pulled low, this bit will be reset to 0 and Host clock for internal Host and DRAM state machines will lag external HCLK input. The lag time will be programmed through HCLK_SEL[1:0].	Captured PGNTJ[4] during Reset
[28:27]	Index D7-D4h bit[15]+Index 8F-8Ch bits[28:27] : Register of HCLK_SEL[2:0] : 111 : Pass through. 110 : Delay one stage. 101 : Delay two stages. 100 : Delay three stages. 011 : Delay four stages 010 : Delay five stages 001 : Delay six stages 000 : Delay seven stages One stage is about 0.4 ns.	Captured PGNTJ[0] HCLK_SEL[1], PHLDAJ during Reset

USWC Gap Range Registers (CR_USWC) (continued)
CSE Offset: 8F ~ 8Ch Read/Write

Bits	Function	Default
[26:25]	Register of DMRCLK_SEL[1:0] : 00 : Pass through. 01 : Delay one stage. 10 : Delay two stages. 11 : Delay three stages. These two bits can be used to delay the clock for the SDRAM read data input latch. One stage is about 0.4 ns.	00b (Pass through)
[24]	Register of DCLKPLL_EN : This bit is used to enable SDRAM PLL. When this bit is enabled, DCLKO will output for clock buffer to generate DIMM clocks. DCLKI is used to compensate the clock delay. Notice that the SDRAM state machine is running based on the same clock as the host, and the SDRAM PLL is used for DIMM clocks.	0b (Disable)
[23]	Register of DADV_LAGJ : When this bit is set to 1, the SDRAM clock out DCLKO will lead the internal Host clock. The lead time will be programmed through DCLK_SEL[1:0]. When this bit is reset to 0, the SDRAM clock out DCLKO will lag the internal Host clock. The lag time will be programmed through DCLK_SEL[2:0].	0b (Lag)
[22:21]	Index D7-D4h bit[13]+Index 8F-8Ch bits[22:21] : Register of DCLK_SEL[2:0] : 000 : Pass through. 001 : Delay one stage. 010 : Delay two stages. 011 : Delay three stages. 100 : Delay four stages 101 : Delay five stages 110 : Delay six stages 111 : Delay seven stages One stage is about 0.4 ns.	00b (Pass through)
[20:19]	Index D7-D4h bit[7]+Index 8F-8Ch bits[20:19] : Register of GCLK_SEL[2:0] : 000 : Pass through. 001 : Delay one stage. 010 : Delay two stages. 011 : Delay three stages. 100 : Delay four stages 101 : Delay five stages 110 : Delay six stages 111 : Delay seven stages One stage is about 0.4 ns.	00b (Pass through)
[18]	Memory Gap Range Enable : 0 : Disabled. 1 : Enabled. This bit is used to enable the memory gap.	0b (Disable)
[17]	GCLKPLL_EN : When PNTJ[3] is pulled high, this bit will be set to 1 and the AGP PLL will be enabled. System designer can use this PLL to delay or lead the GCLKO. Otherwise, the AGP PLL will be disabled, this bit will be 0, and the AGP state machine will run based on GCLKI.	Captured PGNTJ[3] during Reset
[16]	USWC Mode Enable : 0 : Disable. 1 : Enable. This bit is used to enable USWC mode for the second memory gap.	1b (Enable)
[15:4]	Starting Address Bits [31:20]. Starting address and the size define the second memory gap range.	000h
[3]	GADV_LAGJ : When this bit is set to 1, the AGP clock out GCLKO will lead the internal AGP clock. The lead time will be programmed through GCLK_SEL[2:0]. When this bit is reset to 0, the AGP clock out GCLKO will lag the internal Host clock. The lag time will be programmed through GCLK_SEL[1:0].	0b (Lag)

USWC Gap Range Registers (CR_USWC) Continued
CSE Offset: 8F ~ 8Ch Read/Write

Bits	Function	Default
[2:0]	Memory Gap Size : 000 : 1MB. 001 : 2MB. 010 : 4MB. 011 : 8MB. 100 : 16MB. 101, 110, 111 : Reserved. These three bits are used to select the first memory gap size. They combine with bits[15:4] to define the first memory gap.	000b (1 MB)

Memory ECC Error Status Register (CR_ECCST)
CSE Offset: 91 ~ 90h Read Only/Write Once to Clear

Bits	Function	Default
[15:11]	Reserved.	Undefined.
[10:8]	DRAM Row Number when ECC Error occurs (Read Only) : When the M1621 detects an ECC error, it will write the error row number to these three bits.	Undefined.
[7:0]	ECC Syndrome Bits (Read Only) : When the M1621 detects an ECC error, it will write the error syndrome bits to these eight bits.	Undefined.

Reserved
CSE Offset: 93 ~ 92h Read
Default : 00h

Spare Register #1 (CR_SPR1)
CSE Offset: 97 ~ 94h Read / Write

Bits	Function	Default
[31:0]	Stored Data: These registers can be used by the BIOS to store temporary data.	00000000h

Spare Register #2 (CR_SPR2)
CSE Offset: 9B ~ 98h Read / Write

Bits	Function	Default
[31:0]	Stored Data: These registers can be used by the BIOS to store temporary data.	00000000h

Spare Register #3 (CR_SPR3)
CSE Offset: 9F ~ 9Ch Read / Write

Bits	Function	Default
[31:0]	Stored Data: These registers can be used by the BIOS to store temporary data.	00000000h

Power Management Control Block #2 - Starting Address (CR_PMC2)
CSE Offset: A3 ~ A0h Read/Write

Bits	Function	Default
[31-16]	Reserved.	Undefined.
[15-2]	PM2BLK Starting Address : This register is programmed as the I/O base address of the ACPI PM2_CNTL port.	0008h
[1:0]	Reserved.	00b

Reserved
CSE Offset: AF ~ A4h Read
Default : 00h

A.G.P. Capability Identifier Register (CR_AGPCI)
CSE Offset: B3 ~ B0h Read

Bits	Function	Default
[31:24]	Reserved.	00h
[23:20]	Major AGP Revision Number : The M1621 supports the Accelerated Graphics Port Interface Specification revision 1.0. So, this byte contains 1h.	1h
[19:16]	Minor AGP Revision Number : The M1621 supports the Accelerated Graphics Port Interface Specification revision 1.0. So, this byte contains 0h.	0h
[15:8]	Next Capability Pointer Number : The A.G.P. is the only capability of the M1621. So this byte contains 00h to indicate the final item in the list.	00h
[7:0]	AGP Capability ID : The value of 02h in this field identifies the list item as pertaining to A.G.P. registers.	02h

AGP Status Register (CR_AGPSTA)
CSE Offset: B7 ~ B4h Read

Bits	Function	Default
[31:24]	RQ : The M1621 supports the maximum number of AGP command request which is 20h.	20h
[23:10]	Reserved.	00000000000000b
[9]	SBA : The M1621 supports the side band addressing . So the value of this bit is 1b.	1b
[8:2]	Reserved.	0000000b
[1:0]	Data Rate : The M1621 supports the 1x and 2x transfer rates, so the value of these bits is 11b.	11b

A.G.P. Command Register (CR_AGPCMD)

CSE Offset: BB ~ B8h Read/Write

Bits	Function	Default
[31:24]	RQ_DEPTH : The default number of A.G.P. command request is 10h. The request queue depth can be changed by programming these bits.	10h
[23:10]	Reserved.	00000000000000b
[9]	SBA_ENABLE : When set, the side band address mechanism is enabled in the the M1621.	0b
[8]	AGP_ENABLE : When this bit is set to 1, the M1621 allows the master to initiate A.G.P. operations. When it is cleared, the master cannot initiate A.G.P. operation. The default value of this bit is 1b.	1b
[7:2]	Reserved.	000000b
[1:0]	Data Rate : 01 : 1X mode. 10 : 2X mode. The default transfer rate of the M1621 is 1x mode.	01b

AGP NLVM Control Register (CR_NLVMCTL)

CSE Offset: BF ~ BCh Read/Write

Bits	Function	Default
[31:12]	The starting address of Graphic Address Re-mapping Table (GART) is specified by these 20 bits. This is 4K boundary alignment.	00000h
[11:4]	Reserved.	00000000b
[3:0]	NLVM Size : 0000 : 0 MB. 0001 : 1 MB. 0010 : 2 MB. 0011 : 4 MB. 0100 : 8 MB. 0101 : Reserved. 0110 : 16 MB. 0111 : 32 MB. 1000 : 64 MB. 1001 : 128 MB. 1010 : 256 MB. 1011 ~ 1111 Reserved. These 4 bits specify the size of Non-Local Video Memory (NLVM). The base address of NLVM is defined in Index 13h-10h.	0000b (0 MB)

A.G.P. TAG Clear Register (CR_TGCLR)
CSE Offset: C3 ~ C0h Read/Write

Bits	Function	Default
[31:8]	Reserved.	Undefined
[7]	TLB_EN : 0 : Enable. 1 : Disable. Control bit is for graphic address translation function. When this bit is set , the M1621 will execute the address translation function. Otherwise, the M1621 will pass the address to the DRAM controller.	1b (Disable)
[6]	Reserved.	Undefined
[5:4]	TLBSIZ : 00 : 32 entries, 4 sectors. 01 : 64 entries, 8 sectors. 1X : 128 entries, 16 sectors. These two bits specify the size of the internal buffer used for caching the tag data.	00b (32 entries, 4 sectors)
[3:1]	Reserved.	Undefined
[0]	TLB_2L : 0 : One level. 1 : Two levels. The selection bit controls the one level or two level address translation mechanism used by the M1621. This bit is used by AGP driver only. Do not program it in the BIOS.	0b

AGP Control Register One(CR_AGPCR1)
CSE Offset: C7 ~ C4h Read/Write

Bits	Function	Default
[31:0]	Reserved for internal tag buffer invalidation. It is used by AGP driver only. The BIOS should not program this register.	00000000h

AGP Control Register Two (CR_AGPCR2)

CSE Offset: CB ~ C8h Read/Write

Bits	Function	Default
[31]	PCI_SHADOW_RW_EN. Enable PCI Master Access Shadow Region (for Legacy USB function) : 0 : Disable. 1 : Enable. This bit must be set just before system boot up to enable the C.E4 errata fix circuit. Refer to the chip history and errata. It will take effect after M1621-A0E version.	0b
[30: 27]	Reserved	Undefined
[26]	Enable Synchronous Mode Fix Circuit : 0 : Disable. 1 : Enable. This bit must be set to enable the synchronous mode fix circuit. Refer to the chip history and errata. It will take effect after M1621-A0C version and must be set to 1.	0b
[25]	POI_HITM_EN : 0 : Disable. 1 : Enable. This bit is used to enable the A.E1 errata fix circuit. Refer to the chip history and errata. It will take effect after M1621 A0B version and must be set to 1.	0b
[24]	RG_MD_PH : 0 : Normal condition. 1 : MD bus pull high and MDP bus park at low when the ECC/EC is off. When this bit is set to 1, MDP will remain low when the ECC/EC feature is off.	0b
[23]	Reserved.	0b
[22]	RG_WAIT_CYCRDY : This bit is used with Index D7h-D4h bit 8 to add delay for the GART address translation : RG_GHITDEC RG_WAIT_CYCRDY Delay Clocks 0 x 1 clock 1 0 2 clocks 1 1 3 clocks	0b
[21]	Enhanced PCI,AGP to Host Interface Timing Circuit : 0 : Disable. 1 : Enable. When this bit is enabled, the M1621 will enhance the timing between PCI, AGP and Host Interface. It is recommended to be enabled during normal operation.	0b
[20]	RG_CA_HT : 0 : Normal condition. 1 : Column Address hold time having 2 clocks long as CAS Rd/Wt longer than 1 clock. When this bit is set to 1, column address hold time will be 2 clocks long if CASJ read/write active low pulse is larger than 1 clock.	0b
[19]	Enhanced PCI to Host Interface Skew Control Circuit : 0 : Disable 1 : Enable When this bit is enabled, the M1621 will allow more internal PCI to Host interface skew to enhance reliability for 100 MHz operation. It is recommended to be enabled during normal operation.	0b
[18]	DEVSEL_EN : 0 : Disable. 1 : Enable. When this bit is set to 1, the M1621 will latch PCI DEVSELJ once it is detected active low until the PCI cycle is finished. It is recommended to be enabled during normal operation.	0b

AGP Control Register Two (CR_AGPCR2) Continued
CSE Offset: CB ~ C8h Read/Write

Bits	Function	Default
[17]	PARK_DRIVE_PCI_EN : 0 : Disable. 1 : Enable. When this bit is enabled and PCI bus is parked on PCI bus, the M1621 will keep driving the PCI bus signal to avoid PCI bus floating. This bit must be set to 1 during normal operation.	0b
[16]	PARK_DRIVE_GPCI_EN : 0 : Disable. 1 : Enable. When this bit is enabled and AGP bus is parked on AGP bus, M1621 will keep driving AGP bus to avoid AGP bus floating. This bit must be set to 1 during normal operation.	0b
[15:14]	IndexD7-D4h bit[6]+IndexCB-C8h bits[15:14] : RG_STB_DLYSEL[2:0]: 000 : 2 stages delay line. 001 : 1 stage delay line. 010 : 3 stages delay line. 100 : 4 stages delay line. 101 : 5 stages delay line 110 : 6 stages delay line x11 : Reserved These three bits are used to control the AGP data output delay and adjust the skew with strobe signal. One stage is about 0.4 ns delay.	00b (2 Stages)
[13]	RG_FLHW_ENJ : 0 : Enable. 1 : Disable. This bit controls the flushing of high priority write cycle when the flush command is searched behind the high priority write cycle. This means the AGP FLUSH command will flush the high priority write cycle which occurred before the flush command.	1b (Disable)
[12]	STATUS_WE : 0 : Disable (AGP STATUS register is read only). 1 : Enable (AGP STATUS register is read/write). This bit controls the write mechanism of AGP STATUS register (Index B7h-B4h).	0b (Disable)
[11]	RG_DLY_LW_QINJ : 0 : Enable (Delay the low priority write cycle). 1 : Disable. This bit is the control bit for delaying queue in low priority write cycle to AGP to DRAM write state machine when the fence command is searched. After the fence command is de-queued , the low priority write cycle will continuously be served. Otherwise, the low priority write cycle will keep waiting.	1b (Disable)
[10:8]	RG_XOBRQ_DPTH[2:0] : 000 : Throttle length. 001 : 4 QW. 010 : 8 QW. 011 : 12 QW. 100 : 16 QW. 101 : 20 QW. 110 : 24 QW. 111 : 28 QW. These three bits are used to control the throttle data depth of the AGP read data buffer before it starts to return data to AGP bus. Note : the throttle level is 4QW when 2x transfer is selected, else 2QW when 1x transfer is selected.	000b (Throttle length)
[7]	DXO32 : 0 : 16QW. 1 : 32QW. The internal buffer depth of the AGP read data buffer is specified by this bit.	0b
[6:4]	Reserved.	Undefined

AGP Control Register Two (CR_AGPCR2) Continued

CSE Offset: CB ~ C8h Read/Write

Bits	Function	Default
[3:2]	ARBMODE : When these two bits are reset to 00b, the AGP command priority will be High Priority Read -> Low Priority Read -> Flush -> High Priority Write -> Low Priority Write, no matter what the AGP buffer status is. Which means, the AGP high priority request will always keep top priority and wait until the buffer is available for this command. When these two bits are programmed to 01b, the arbiter will watch the buffer status. If the buffer is full, it will move to serve the next high priority request. When these two bits are programmed to 10b, the arbiter will enable a counter to count for 256 clocks for low priority read request. If the time has expired, the low priority request will become the top priority. When these two bits are programmed to 11b, the arbiter will change a write request to top priority if the write command buffer is full.	00b
[1:0]	Reserved.	Undefined

AGP Control Register Three (CR_AGPCR3)

CSE Offset: CF ~ CCh Read/Write

Bits	Function	Default
[31:0]	Reserved for internal tag buffer debugging. It is used by AGP driver only. The BIOS should not program this register.	00000000h

AGP Control Register Four (CR_AGPCR4)

CSE Offset: D3~D0h Read/Write

Bits	Function	Default
[31]	Enable I740 AGP Card Reliability Fix Circuit : 0 : Disable. 1 : Enable. This bit must be enabled to fix I740 AGP card reliability issue. Refer to the chip history and errata C.E1. It will take effect after the M1621-A0E version and must be set to 1b.	0b
[30:23]	Reserved.	Undefined
29	Enable the Arbiter fix circuit with M1543C 0 : disable 1 : enable This bit must be enabled to fix the deadlock situation with M1543C when M1543C is running two masters concurrently. This issue will not happen with M1533&M1543. This bit will take effect after M1621 A1G version.	
28	Enable In-order Queue = 8 Fix Circuit 0 : disable 1 : enable This bit must be set to 1 when index 81h to 80h bits 11 to 10 are set to 11h. The fix circuit will take effect after M1621 A1J version.	
[22]	Enable Passive Release Issue Fix Circuit : 0 : Disable. 1 : Enable. This bit must be enabled to fix the passive release feature enable issue. Refer to the chip history and errata C.E5. It will take effect after the M1621-A0E version and must be set to 1b.	0b
[21:8]	Reserved.	Undefined
[7]	Enable Power On Suspend Fix Circuit when internal PLL is off : 0 : Disable. 1 : Enable. This bit must be enabled to fix the power on suspend issue when the internal PLL is off. Refer to chip history and errata C.E3. It will take effect after the M1621 A0E version and must be set to 1b.	0b
[6:0]	Reserved.	Undefined

AGP Control Register Five (CR_AGPCR5)
CSE Offset: D7~D4h Read/Write

Bits	Function	Default
[31:24]	RG_HSTCNT : The number of Host commands that were executed in a time period (historical information). Used with bits[3:0] flow control mode. Refer to bits[3:0] for explanation.	00000000b
[23:16]	RG_EXPCNT : The number of AGP commands that were executed in a time period (historical information). Used with bits[3:0] flow control mode. Refer to bits[3:0] for explanation.	00000000b
[15]	Index D7-D4h bit[15] : HCLK_SEL[2] This bit combines with Index 8F-8Ch bits[28:27] as HCLK_SEL[2:0]. Refer to register Index 8F-8Ch for details.	Captured by PGNTJ[0]
[14]	Index D7-D4h bit[14] : Feedback of AGP PLL is external or internal 0 : Internal PLL 1 : External PLL This bit is used to select the AGP block state machine clock. When this bit is 1, the clock comes from the internal PLL. Otherwise, it will come from the GCLKI input. This bit function only takes effect when the AGP PLL is enabled and 1 is recommended for normal operation. When the AGP PLL is disabled, the AGP block state machine clock always comes from the GCLKI input. Refer to the Board Guidelines for Aladdin Pro II for more detailed information.	Captured by PGNTJ[2]
[13]	Index D7-D4h bit[13] : DCLK_SEL[2]. This bit combines with Index 8F-8Ch bits[22:21] as DCLK_SEL[2:0]. Refer to Index 8F-8Ch for details.	0b
[12]	Reserved.	Undefined
[11]	RG_DXO_STRDY : 0 : Not optimized with SDRAM. 1 : Optimized for SDRAM. When this bit is set to 1, the internal state machine will optimize AGP master read performance when SDRAM is used . It is recommended to set this bit to 1b in SDRAM configurations.	0b (Not optimized)
[10]	RG_PAD_SEL : 0 : TTL input. 1 : Differential pair. This bit is used to program the AGP data input pad circuit. When this bit is reset to 0, TTL input levels are used to decide the input status. Otherwise, the input pad will behave like a differential pair based on the AGP input reference voltage.	0b (TTL input)
[9]	RG_AVOID_DL : 0 : Disable. 1 : Enable. There is a deadlock situation which will occur when MCC is serving the AGP data read cycle: If the 66 PCI/AGP bus is occupied by a PCI master read cycle and the function of delay transaction is off, the AGP read data agent cannot return data to the AGP bus and the read data buffer will keep pre-fetching until it becomes full. The data path will halt the current MCC memory read cycle and the AGP master memory read cycle will stall at IOQ waiting for MCC. The 66 PCI master will occupy the AGP AD bus to wait for the read data forever. This RG_AVOID_DL bit controls the AGP command queue to issue AGP data read cycle to memory access control. If this bit is set, the command decomposer will count the QW number that data is still staying in the AGP data read FIFO. When the FIFO is full, the decomposer will stop to issue an AGP read cycle to MCC. This can prevent the deadlock situation. This bit must be enabled when the delay transaction feature is disable.	0b (Disable)
[8]	RG_GHITDEC : 0 : One Host Clock. 1 : Two Host Clocks. This bit is used to program the time period of GTLB looking for the hit or miss TLB tag in the current NLVM access.	1b (Two Host Clocks)
[7]	GCLK_SEL[2] : This bit combines with Index 8F-8Ch bits[20:19] as GCLK_SEL[2:0]. Refer to register index 8F-8Ch for details.	0b
[6]	RG_STB_DLYSEL[2] : This bit combines with Index CB-C8h bits[15:14] as RG_STB_DLYSEL[2:0]. Refer to register index CB-C8h for details.	00b
[5]	FMISS : 0 : Disable. 1 : Enable. When this bit is set , the TLB action always fetches translation data from DRAM.	0b (Disable)

AGP Control Register Five (CR_AGPCR5) Continued
CSE Offset: D7~D4h Read/Write

Bits	Function	Default
[4]	NLVM_EN : 0 : Disable (ignore the NLVM region cycle in PCI bus). 1 : Enable (response to NLVM region cycle in PCI bus). This bit determins if the Host, 33 PCI, and 66 PCI slave state machines will respond to the NLVM region cycle or not. When it is enabled, the M1621 will translate the NLVM address before the cycle is issued to destination.	1b (Enable)
[3]	MRGEN : 0 : Disable merging function. 1 : Enable merging function. This bit controls the function for merging AGP master write data.	0b (Disable)
[2:0]	MACMODE : The mechanism for flow control of AGP & Host cycle. [2]= 0 : Disable. [2]= 1 : Enable flow control mode or test mode. [1]= 0 : Flow control mode. [1]= 1 : Test mode. ***flow control mode:*** macmode[0]=0 : Use lower half counter (8 bits). macmode[0]=1 : Use full counter (16 bits). ***test mode :*** macmode[0]=0 : Use lower half counter (8 bits). macmode[0]=1 : Use higher half counter (8 bits). Flow control mode will use the counter to count RG_HSTCNT host command number (bits[31:24]) and RG_EXPCNT (bits[23:16]). If macmode[0]=0 (8 bits counter is used), the M1621 will change AGP master and Host priority when the cycle number has more than 8-cycle differences. If macmode[0]=1 (16 bits counter is used), the M1621 will change AGP master and Host priority when the cycle number has more than 32-cycle differences. Notice: Test mode is for test only and should not be enabled in normal operation.	00b

Reserved
CSE Offset: EF ~ D8h Read
Default : 00h

User-Defined Row/Column Address Mapping Registers : (CR_RCA0 ~ CR_RCA3)
CSE Offset: F3 ~ F0h, F7 ~ F4h, FB ~ F8h, FF ~ FCh Read/Write

Bits	Function	Default
[31:28]	Rx_RA14[3:0] : Host-Bus Address Bit mapped onto Memory Row Address Bit 14 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0100b (A28)
[27:24]	Rx_RA13[3:0] : Host-Bus Address Bit mapped onto Memory Row Address Bit 13 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0011b (A27)
[23:20]	Rx_RA12[3:0] : Host-Bus Address Bit mapped onto Memory Row Address Bit 12 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0010b (A26)
[19:16]	Rx_RA11[3:0] : Host-Bus Address Bit mapped onto Memory Row Address Bit 11 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0001b (A25)

User-Defined Row/Column Address Mapping Registers : (CR_RCA0 ~ CR_RCA3) Continued
CSE Offset: F3 ~ F0h, F7 ~ F4h, FB ~ F8h, FF ~ FCh Read/Write

Bits	Function	Default
[15:12]	Rx_C14[3:0] : Host-Bus Address Bit mapped onto Memory Column Address Bit 14 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0100b (A28)
[11:8]	Rx_CA13[3:0] : Host-Bus Address Bit mapped onto Memory Column Address Bit 13 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0011b (A27)
[7:4]	Rx_CA12[3:0] : Host-Bus Address Bit mapped onto Memory Column Address Bit 12 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0010b (A26)
[3:0]	Rx_CA11[3:0] : Host-Bus Address mapped onto Memory Column Address 11 0000 : Host-Bus Address Bit 13. 0001 : Host-Bus Address Bit 25. 0010 : Host-Bus Address Bit 26. 0011 : Host-Bus Address Bit 27. 0100 : Host-Bus Address Bit 28. 0101 : Host-Bus Address Bit 29. 0110 ~ 1111 : Reserved. Refer to the MA mapping table for SDRAM listed in section 3.1.1. (11-bit column address)	0000b (A13)

PCI-to-PCI BRIDGE (Bus 0 , Device 1)

Vender Identification Register (CR_P2PVID)

CSE Offset: 01 ~ 00h Read

Bits	Function	Default
[15:0]	This is a 16-bit value assigned to Acer Laboratories Inc. This register is combined with index 03h-02h to uniquely identify any PCI device. Writes to this register has no effect.	10B9h

Device Identification Register (CR_P2PDID)

CSE Offset: 03 ~ 02h Read

Bits	Function	Default
[15:0]	This is a 16-bit value assigned to the M1621 PCI-to-PCI Bridge from Acer Laboratories Inc.	5247h

Command Register (CR_P2PCMD)

CSE Offset: 05 ~ 04h Read/Write

Bits	Function	Default
[15:9]	Reserved.	0000000b
[8]	SERRJ Enable : This bit is an enable bit for the SERRJ driver. A value of 0 disables the SERRJ driver. A value of 1 enables the SERRJ driver. SERRJ uses an o/d (Open Drain) pad in the M1621. The motherboard design should use a pull-up resistor (2.7KΩ) to keep this pin at logic high. When the AGP bus error checking is enabled and an error is found, the M1621 will drive SERRJ low to the M1533/M1543/M1543C to generate NMI when this bit is enabled. Disabling the SERRJ output will always keep this output at logic high.	0b
[7]	Reserved.	0b
[6]	Parity Error Response : When this bit is set, the M1621 will take its normal action when a parity error is detected. When the bit is 0, the M1621 will ignore any parity error that it detects and continue normal operation.	0b
[5:2]	Reserved.	01h
[1]	Memory Space Enable : Control P2P bridge response to memory space accesses. A value of 0 disables the P2P bridge response. A value of 1 allows the device to respond to memory space access.	1b
[0]	I/O Space Enable : Control P2P bridge response to I/O space accesses on primary bus. A value of 0 disables the P2P response. A value of 1 allows the device to respond to I/O space access.	1b

Status Register (CR_STAS)
CSE Offset: 07 ~ 06h Read/Write One to Clear

Bits	Function	Default
[15]	Reserved.	0b
[14]	Signaled System Error : When the M1621 P2P bridge asserts the SERRJ due to error conditions on the A.G.P. bus, this bit will be set to 1.	0b
[13:0]	Reserved.	0000h

Revision Identification Register (CR_P2PRID)
CSE Offset: 08h Read

Bits	Function	Default
[7:0]	This is an 8-bit value that indicates the revision identification number for the P2P bridge in the M1621 .	01h

Specific Register-Level Programming Register (CR_P2PSRLP)
CSE Offset: 09h Read

Bits	Function	Default
[7:0]	This value for the P2P bridge in the M1621 is 00h.	00h

Sub-Class Code Register (CR_P2PSCC)
CSE Offset: 0Ah Read

Bits	Function	Default
[7:0]	This value for the P2P bridge in the M1621 is 04h.	04h

Base-Class Code Identification Register (CR_P2PBCC)
CSE Offset: 0Bh Read

Bits	Function	Default
[7:0]	This value for the P2P bridge in the M1621 is 06h.	06h

Header Type Register (CR_P2PHTR)
CSE Offset: 0Eh Read

Bits	Function	Default
[7:0]	This Header Type value for the P2P bridge in the M1621 is 01h.	01h

Reserved
CSE Offset: 17 ~ 0Fh Read
Default : 00h

Primary Bus Number Register (CR_PBNR)
CSE Offset: 18h Read

Bits	Function	Default
[7:0]	The primary bus number of the host bridge is 00h.	00h

Secondary Bus Number Register (CR_SBNR)
CSE Offset: 19h Read/Write

Bits	Function	Default
[7:0]	This register identifies the bus number assigned to the second bus (A.G.P. bus) for the P2P bridge in the M1621.	00h

Subordinate Bus Number Register (CR_SUBNR)
CSE Offset: 1Ah Read/Write

Bits	Function	Default
[7:0]	This register identifies the subordinate bus number assigned to the second bus (A.G.P. bus) for the P2P bridge in the M1621.	00h

IO Base Address Register (CR_IOBAR)
CSE Offset: 1Ch Read/Write

Bits	Function	Default
[7:4]	These four bits correspond to A[15:12] of the I/O address.	Fh
[3:0]	Reserved.	0h

IO Limit Address Register (CR_IOLAR)
CSE Offset: 1Dh Read/Write

Bits	Function	Default
[7:4]	These four bits correspond to A[15:12] of the I/O address.	0h
[3:0]	Reserved.	0h

Secondary PCI-to-PCI Status Register (CR_SPPSR)
CSE Offset: 1F ~ 1Eh Read/Write

Bits	Function	Default
[15]	Detected Parity Error on A.G.P. Bus : The M1621 will set this bit whenever it detects a parity error, even if parity error handling is disabled.	0b
[14]	Reserved.	0b
[13]	Received Master Abort on A.G.P. Bus : The M1621 will set this bit when its 66 PCI transaction is terminated with Master-Abort.	0b
[12]	Received Target Abort on A.G.P. Bus : The M1621 will set this bit when its 66 PCI transaction is terminated with Target-Abort.	0b
[11:9]	Reserved.	000b
[8]	Data Parity Error Detected on A.G.P. Bus Side : This bit will be set to 1, when the below conditions are met: 1) The M1621 asserted GPERRJ or sampled GPERRJ asserted. 2) The M1621 is the initiator for the operation in which the parity error occurs. 3) The bit 0 is 1 in the CR_PPBCR (bridge control register).	0b
[7:0]	Reserved.	20h

Memory Base Address Register (CR_MEMBAR)
CSE Offset: 21 ~ 20h Read/Write

Bits	Function	Default
[15:4]	These twelve bits correspond to A[31:20] of the Memory address.	FFFh
[3:0]	Reserved.	0h

Memory Limit Address Register (CR_MEMLAR)
CSE Offset: 23 ~ 22h Read/Write

Bits	Function	Default
[15:4]	These twelve bits correspond to A[31:20] of the Memory address.	000h
[3:0]	Reserved.	0h

Pre-fetchable Memory Base Address Register (CR_PMEMBAR)
CSE Offset: 25 ~ 24h Read/Write

Bits	Function	Default
[15:4]	These twelve bits correspond to A[31:20] of the Memory address.	FFFh
[3:0]	Reserved.	0h

Pre-fetchable Memory Limit Address Register (CR_PMEMLAR)
CSE Offset: 27 ~ 26h Read/Write

Bits	Function	Default
[15:4]	These twelve bits correspond to A[31:20] of the Memory address.	000h
[3:0]	Reserved.	0h

Reserved
CSE Offset: 3D ~ 28h Read
Default : 00h

PCI-to-PCI Bridge Control Register (CR_PPBCR)
CSE Offset: 3F ~ 3Eh Read/Write

Bits	Function	Default
[15:4]	Reserved.	000h
[3]	VGA Enable : When this bit is set, the M1621 will positively decode and forward the following accesses to A.G.P. bus. Memory accesses in the range 0A0000h to 0BFFFFh I/O accesses where AD[9:0] are in the ranges 3B0-3B9h, 3C0h-3DFh.	0b
[2]	ISA Enable : When this bit is set, the M1621 will block any forwarding to A.G.P. bus of I/O transactions addressing the last 768 bytes in each 1k byte block. The M1621 will transfer these I/O transactions to the primary PCI bus.	0b
[1]	System Error Enable : When this bit is set and the GSERRJ enable bit in the command register is set. The M1621 will forward GSERRJ assertions to the primary bus (SERRJ) .	0b
[0]	Parity Error Response Enable : When this bit is 0, the M1621 will ignore data parity error on the A.G.P. bus. Otherwise, the M1621 will assert GPERRJ when it detects data parity errors on the A.G.P. bus.	0b

Reserved
CSE Offset: FF ~ 40h Read
Default : 00h

Section 5 : Hardware Setup and Software Programming Guide

5.1 Hardware Setup Table :

The M1621 will strobe the hardware setting in the respective registers when RESET goes inactive.

Pin Name	Description	Pull up	Pull down	Register	Note
REFENV	GTL pad delay line	Enable	Disable	Index 8Fh bit 7	(1)
AREQJ	Host PLL enable	Enable	Disable	Index 8Fh bit 6	(2)
PGNTJ[4]	Host Clock Timing	Lead	Lag	Index 8Fh bit 5	(3)
HCLK_SEL[1]	Host Clock SEL(1)	------	------	Index 8Fh bit 4	(4)
PHLDAJ	Host Clock SEL(0)	------	------	Index 8Fh bit 3	(4)
PGNTJ[3]	AGP PLL Enable	Enable	Disable	Index 8Eh bit 1	(5)
PGNTJ[1]	Short Reset for Tester	------	------	------	(6)
PGNTJ[0]	Host Clock SEL(2)			Index D5h bit 7	(4)
PGNTJ[2]	Feedback of AGP's PLL is external or internal			Index D5h bit 6	(7)

Note :

1. When GTL pad delay line is enabled, 3-stage (2.1ns) delay will be added for GTL+ input and Index 8Fh bit7 will be set to 1. Otherwise, there is no delay and Index 8Fh bit7 will be reset to 0.

2. When AREQJ is pulled high, Host PLL will be enabled and Index 8Fh bit6 will be set to 1. Otherwise, Host PLL will be disabled and Index 8Fh bit6 will be reset to 0.

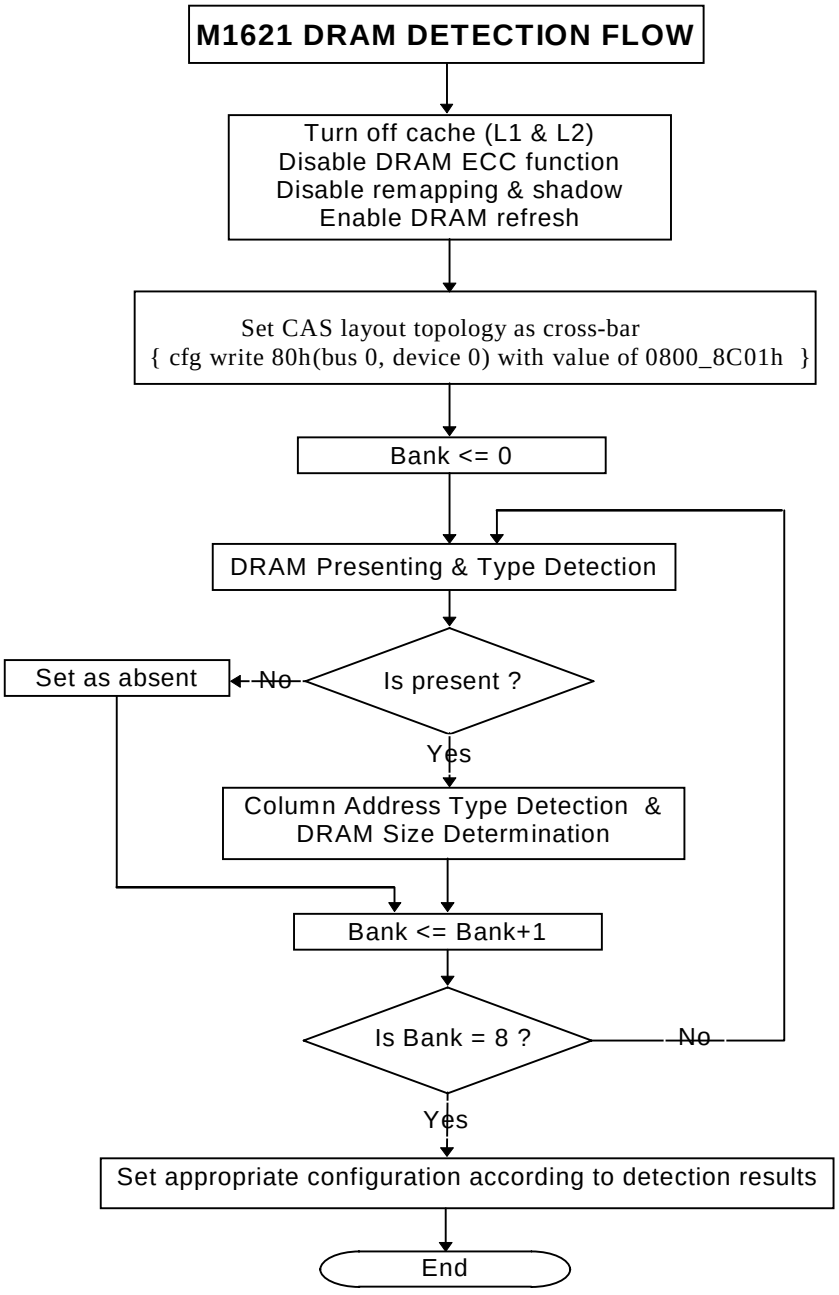
3. When PGNTJ[4] is pulled high, internal Host clock will lead external Host clock and Index 8Fh bit5 will be set to 1. Otherwise, internal Host clock will lag external Host clock and Index 8Fh bit5 will be reset to 0. The lead or lag timing is selected by HCLK_SEL[1:0].

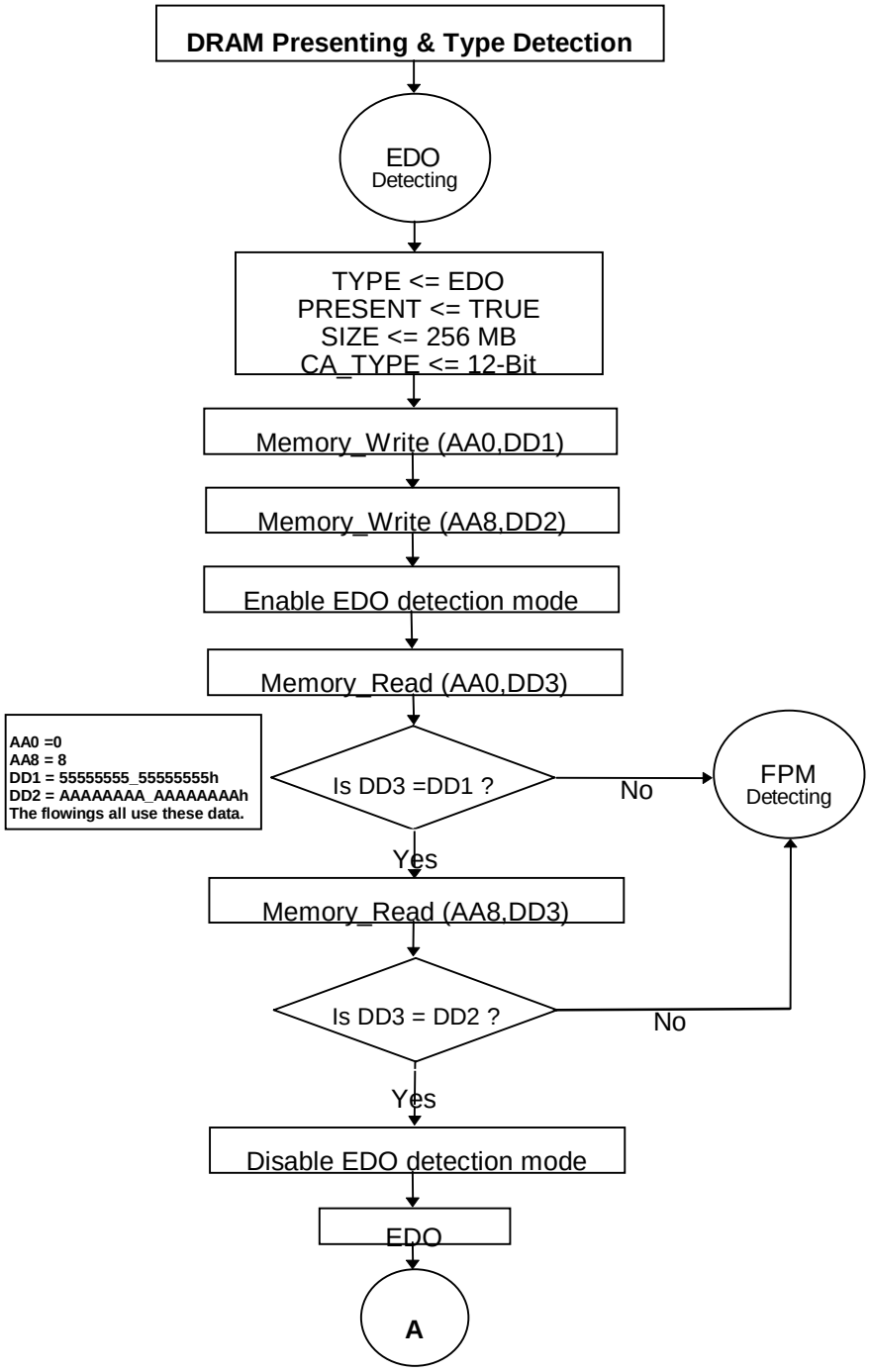
4. Determine the amount of host clock lead or lag

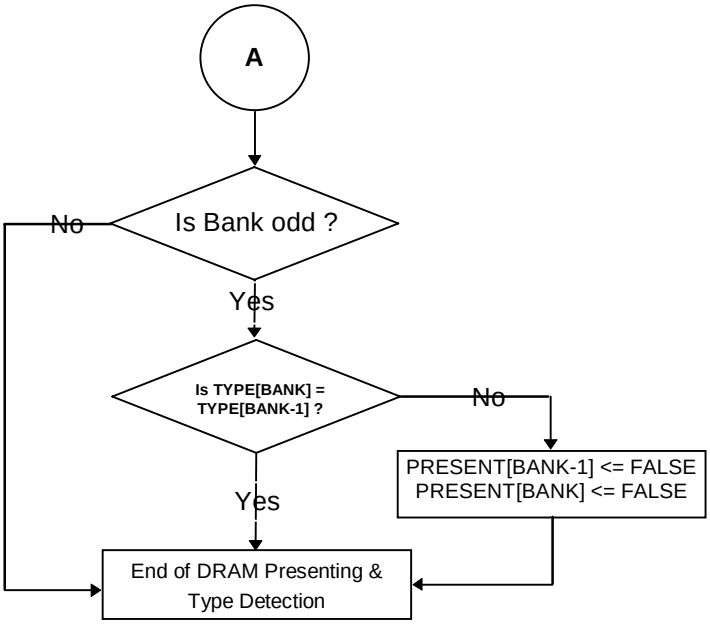
HCLK_SEL[2]	HCLK_SEL[1]	HCLK_SEL[0]	Approximate time
1	1	1	0 ns
1	1	0	0.4 ns
1	0	1	0.8 ns
1	0	0	1.2 ns
0	1	1	1.6 ns
0	1	0	2.0 ns
0	0	1	2.4 ns
0	0	0	2.8 ns

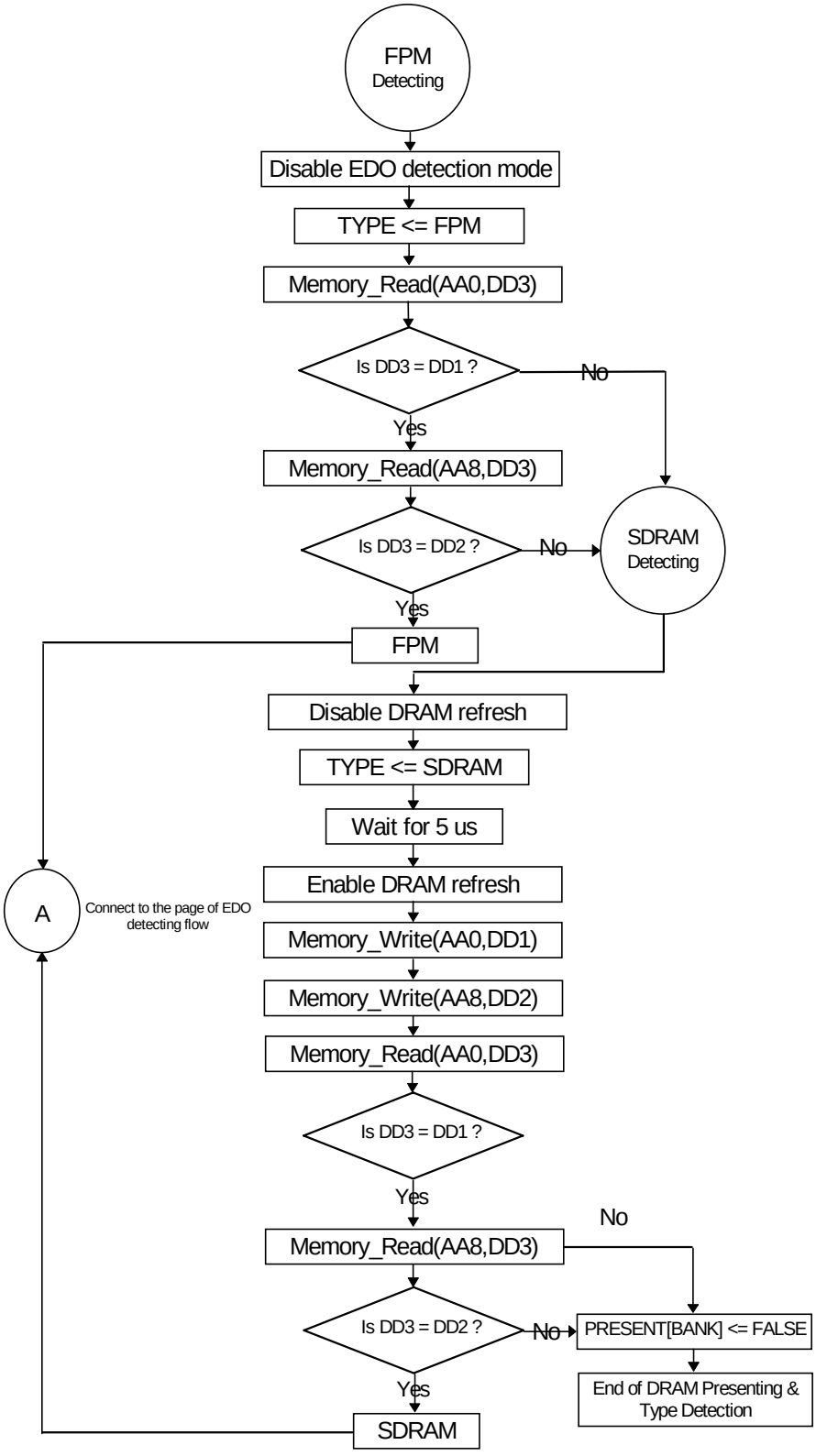
5. When PGNTJ[3] is enabled, the AGP PLL will be enabled and Index 8Eh bit1 will be set to 1. Otherwise, the AGP PLL will be disabled and Index 8Eh bit1 will be reset to 0.
6. If this value is set to '0', the CPU RESET driven by the M1621 will be a short reset for test use. Normal setting for this value is 1..
7. When PGNTJ[2] is pulled low, the AGP block state machine clock will come from GCLKI pad and Index D5h bit 6 is reset to 0. When PGNTJ[2] is pulled high, the AGP block state machine clock will come from the internal PLL and Index D5h bit6 is set to 1. This selection only takes effect when the AGP PLL is enabled. Otherwise, the AGP block state machine clock will come from the GCLKI pad only.

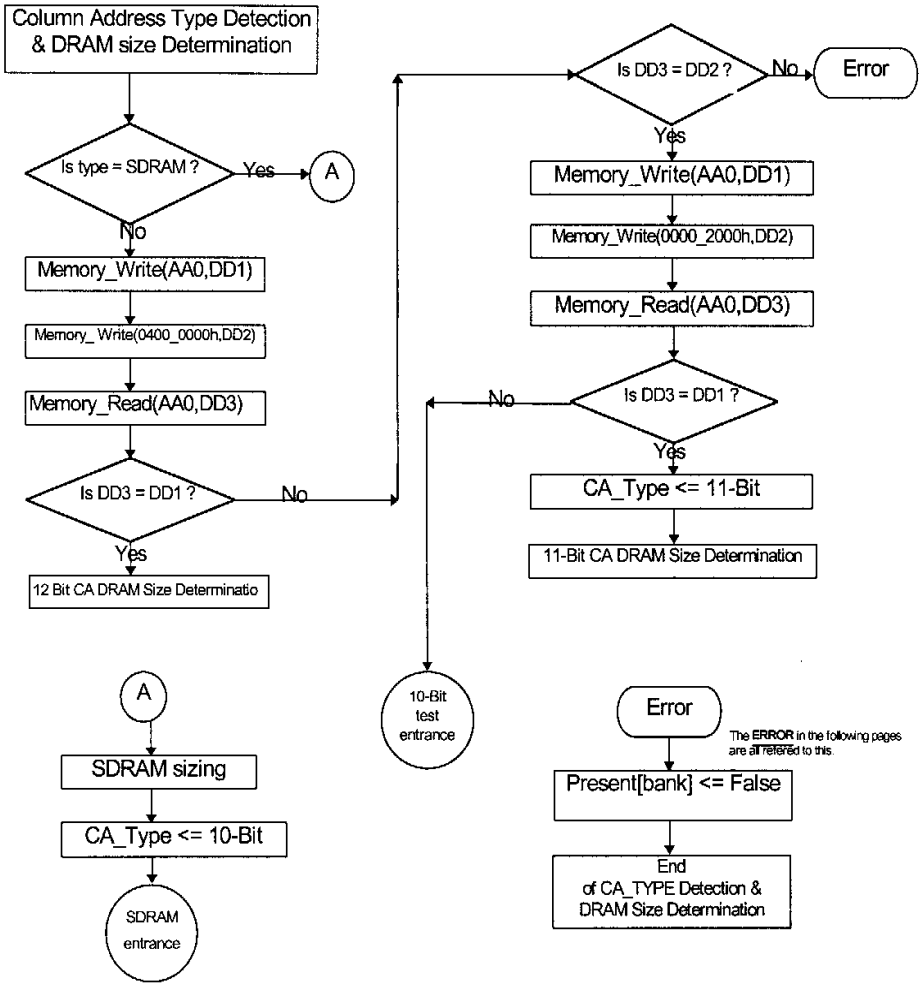
5.2 Software Programming Guide

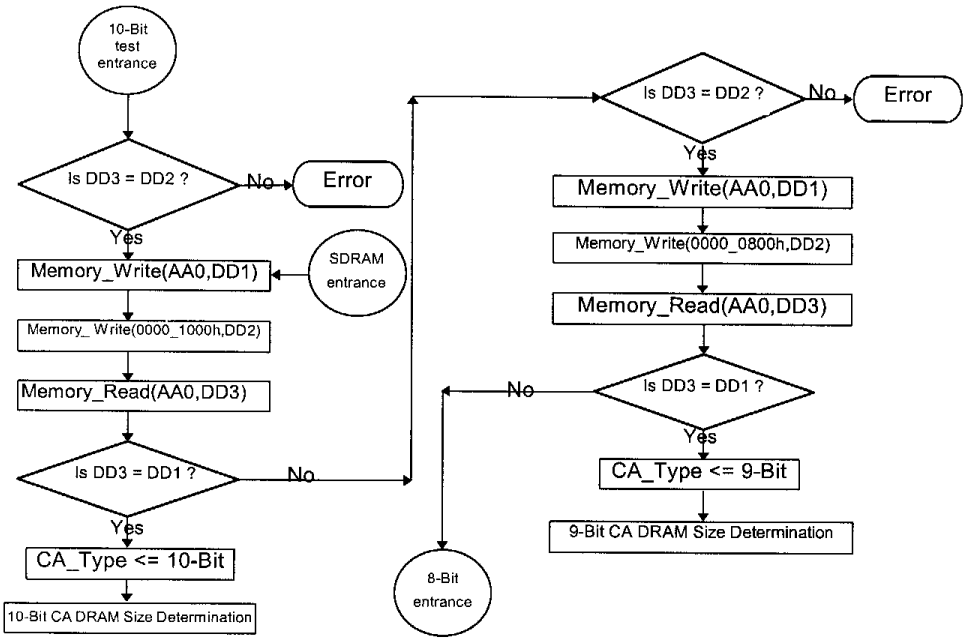


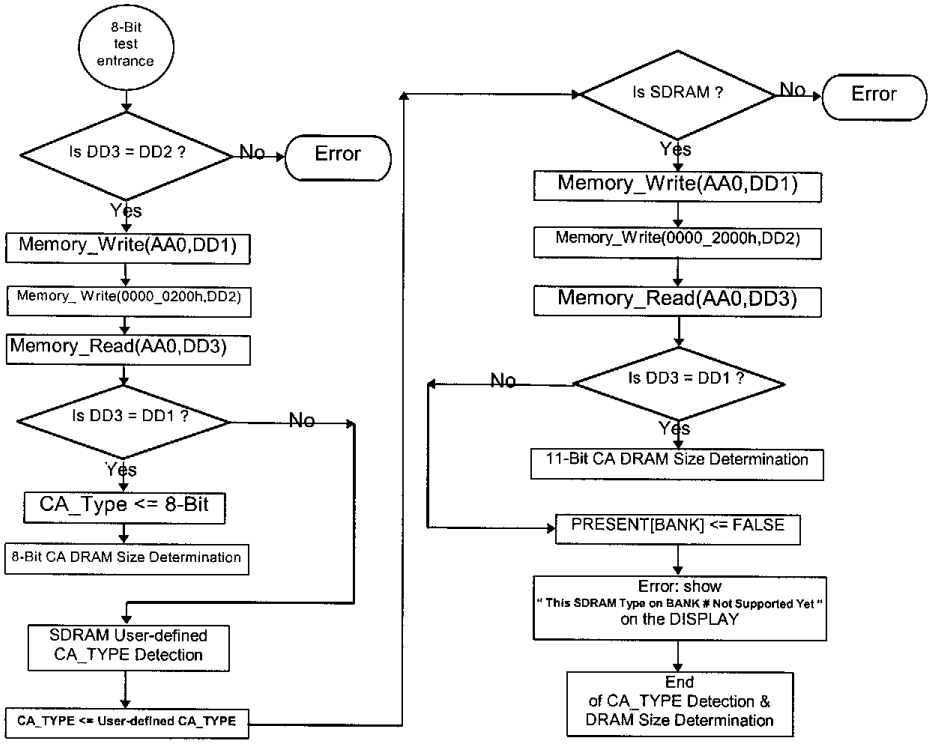

DRAM Presenting & Type Detection
EDO
Detecting
TYPE <= EDO
PRESENT <= TRUE
SIZE <= 256 MB
CA_TYPE <= 12-Bit
Memory_Write (AA0,DD1)
Memory_Write (AA8,DD2)
Enable EDO detection mode
Memory_Read (AA0,DD3)
AA0 =0
AA8 = 8
DD1 = 55555555_55555555h
DD2 = AAAAAAAA_AAAAAAAAh
The flowings all use these data.
Is DD3 =DD1 ?
No
FPM
Detecting
Yes
Memory_Read (AA8,DD3)
Is DD3 = DD2 ?
No
Yes
Disable EDO detection mode
EDO
A

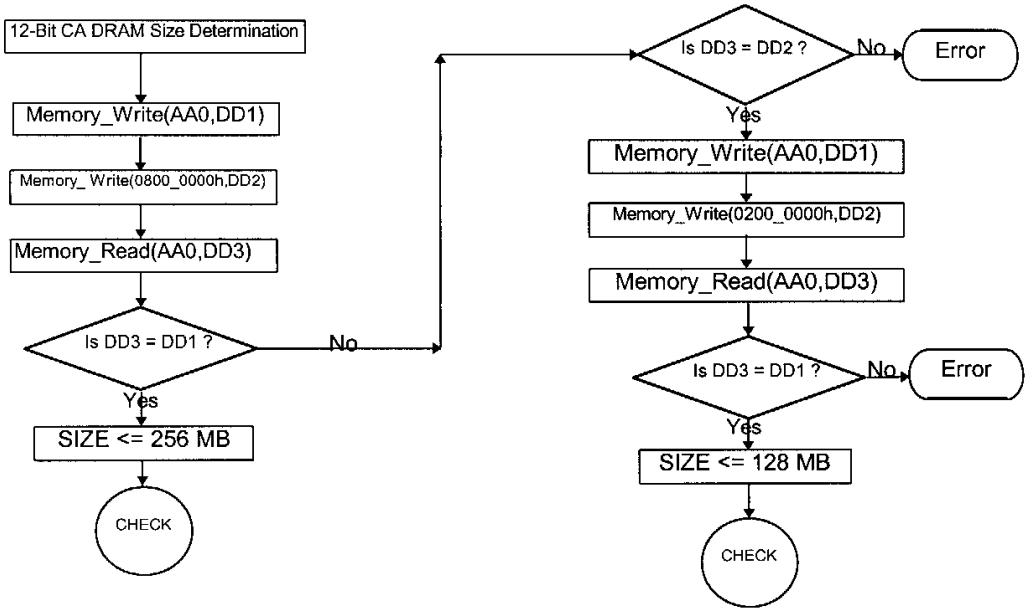

A
Is Bank odd ?
No
Yes
Is TYPE[BANK] = TYPE[BANK-1] ?
No
Yes
PRESENT[BANK-1] <= FALSE
PRESENT[BANK] <= FALSE
End of DRAM Presenting & Type Detection

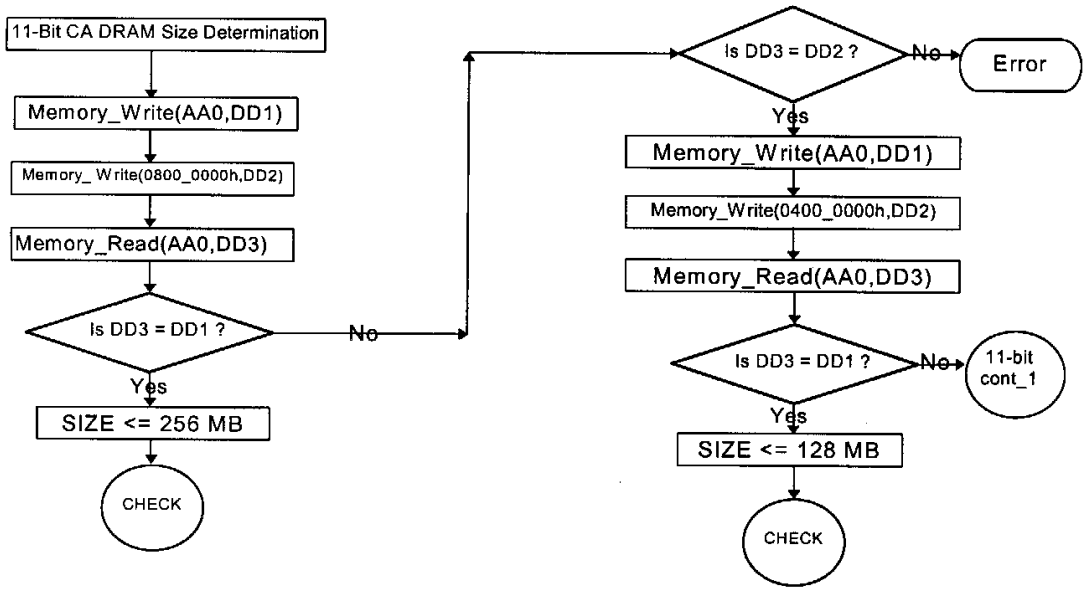

FPM
Detecting
Disable EDO detection mode
TYPE <= FPM
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
Memory_Read(AA8,DD3)
Is DD3 = DD2 ?
No
SDRAM
Detecting
Yes
FPM
Disable DRAM refresh
TYPE <= SDRAM
Wait for 5 us
Enable DRAM refresh
A
Connect to the page of EDO detecting flow
Memory_Write(AA0,DD1)
Memory_Write(AA8,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
Yes
No
Memory_Read(AA8,DD3)
Is DD3 = DD2 ?
No
PRESENT[BANK] <= FALSE
End of DRAM Presenting & Type Detection
Yes
SDRAM

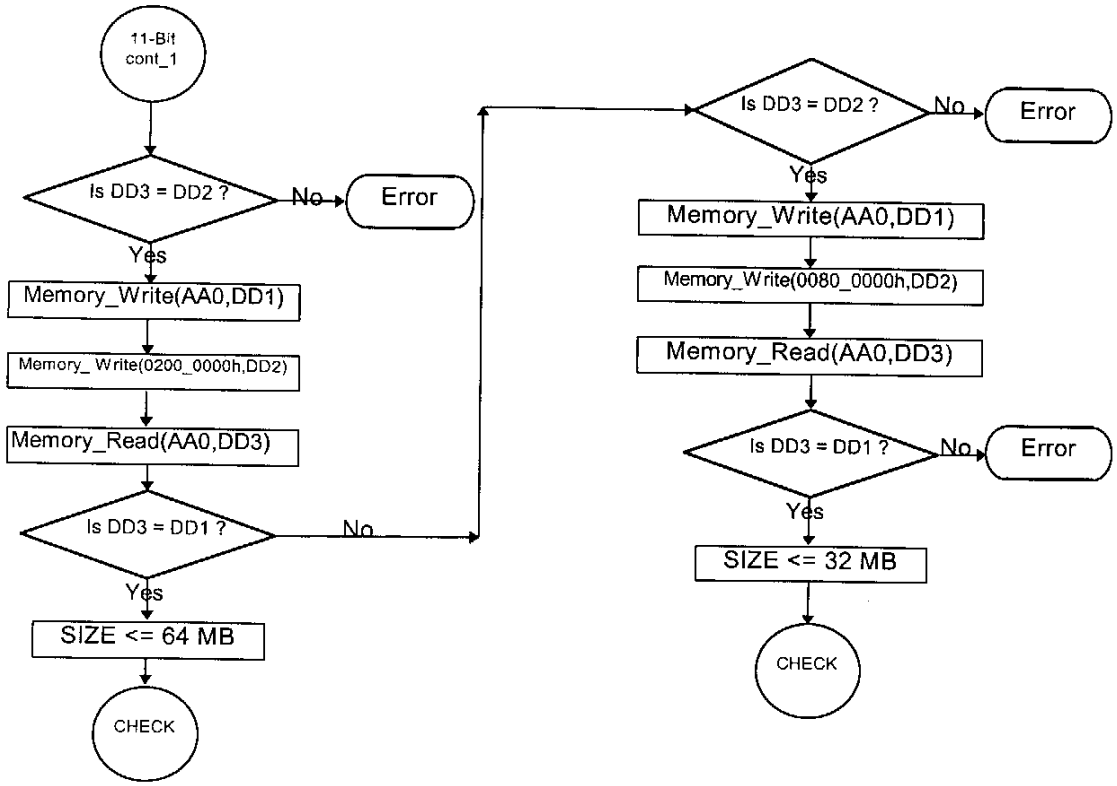

Column Address Type Detection & DRAM size Determination
Is type = SDRAM ?
Yes
A
No
Memory_Write(AA0,DD1)
Memory_ Write(0400_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
12 Bit CA DRAM Size Determinatio
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0000_2000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
CA_Type <= 11-Bit
11-Bit CA DRAM Size Determination
A
SDRAM sizing
CA_Type <= 10-Bit
SDRAM entrance
10-Bit test entrance
Error
The ERROR in the following pages are all refered to this.
Present[bank] <= False
End of CA_TYPE Detection & DRAM Size Determination

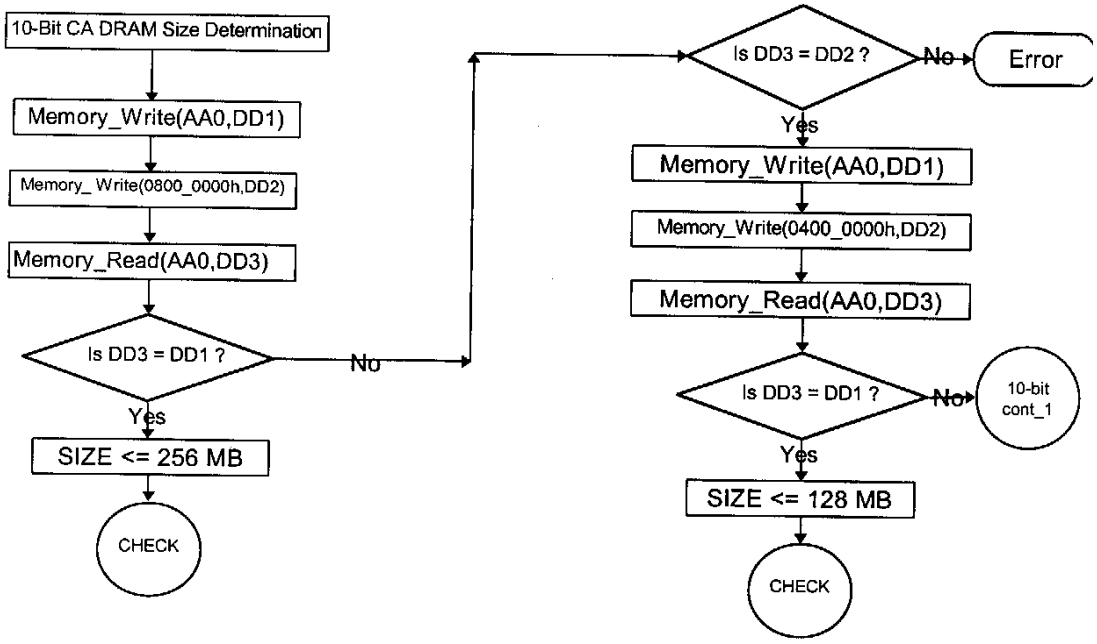

10-Bit test entrance
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
SDRAM entrance
Memory_ Write(0000_1000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
CA_Type <= 10-Bit
10-Bit CA DRAM Size Determination
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0000_0800h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
CA_Type <= 9-Bit
9-Bit CA DRAM Size Determination
8-Bit entrance

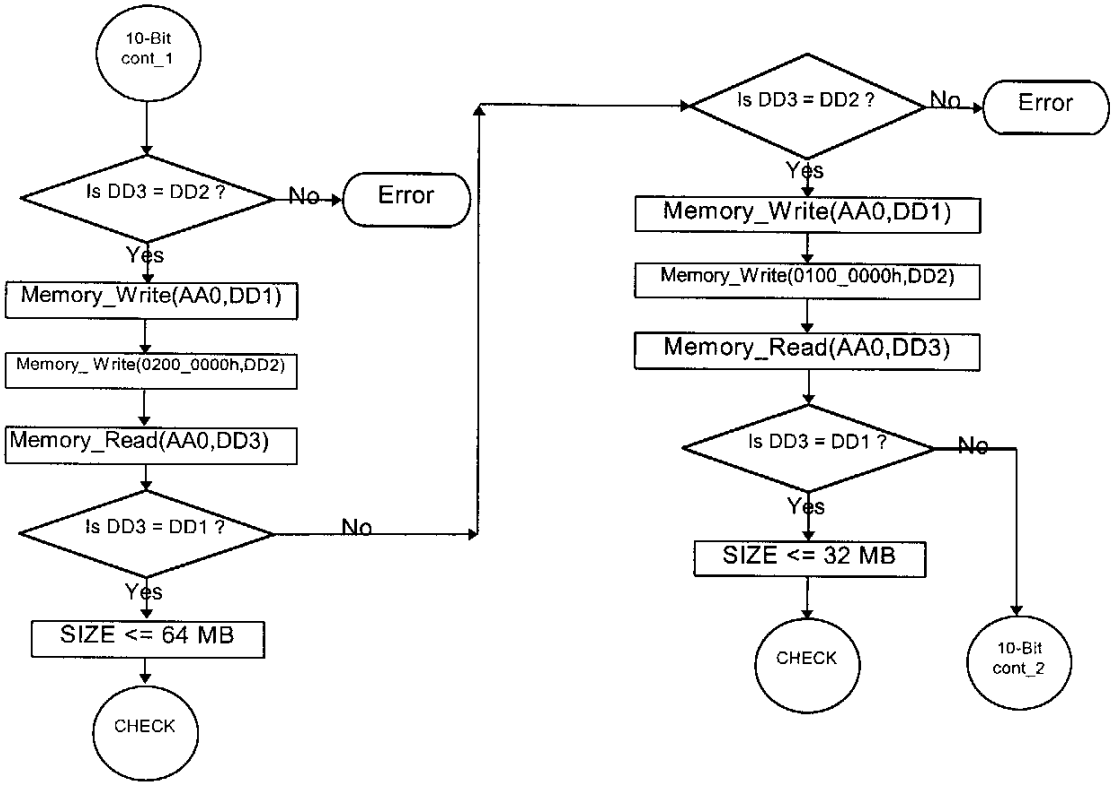

8-Bit test entrance
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0000_0200h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
CA_Type <= 8-Bit
8-Bit CA DRAM Size Determination
SDRAM User-defined CA_TYPE Detection
CA_TYPE <= User-defined CA_TYPE
Is SDRAM ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0000_2000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
11-Bit CA DRAM Size Determination
PRESENT[BANK] <= FALSE
Error: show
" This SDRAM Type on BANK # Not Supported Yet "
on the DISPLAY
End
of CA_TYPE Detection &
DRAM Size Determination

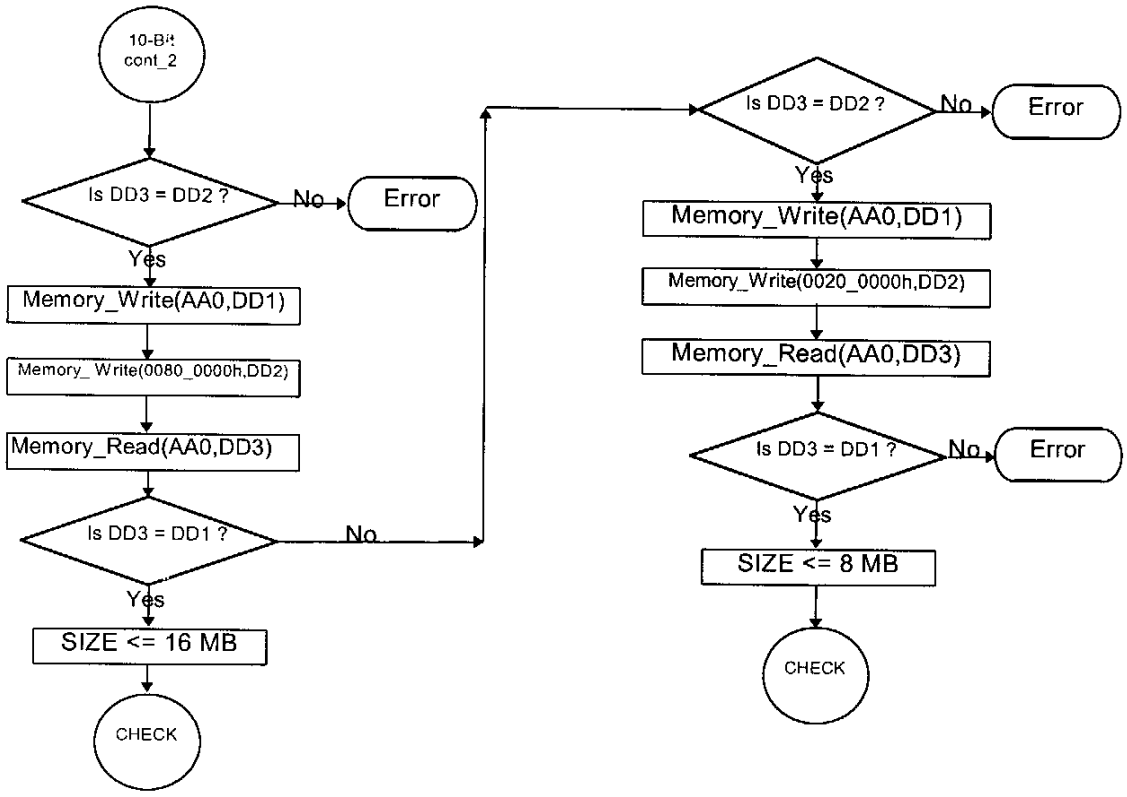

12-Bit CA DRAM Size Determination
Memory_Write(AA0,DD1)
Memory_ Write(0800_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 256 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0200_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Error
Yes
SIZE <= 128 MB
CHECK

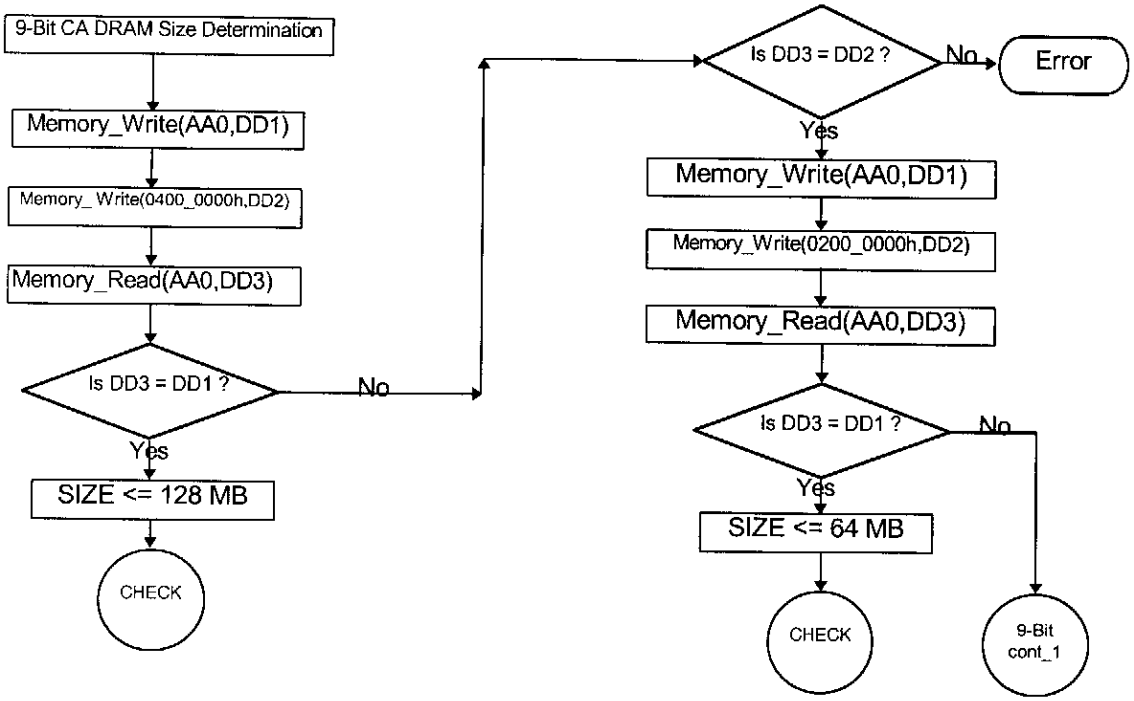

11-Bit CA DRAM Size Determination
Memory_Write(AA0,DD1)
Memory_ Write(0800_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 256 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0400_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
11-bit cont_1
Yes
SIZE <= 128 MB
CHECK

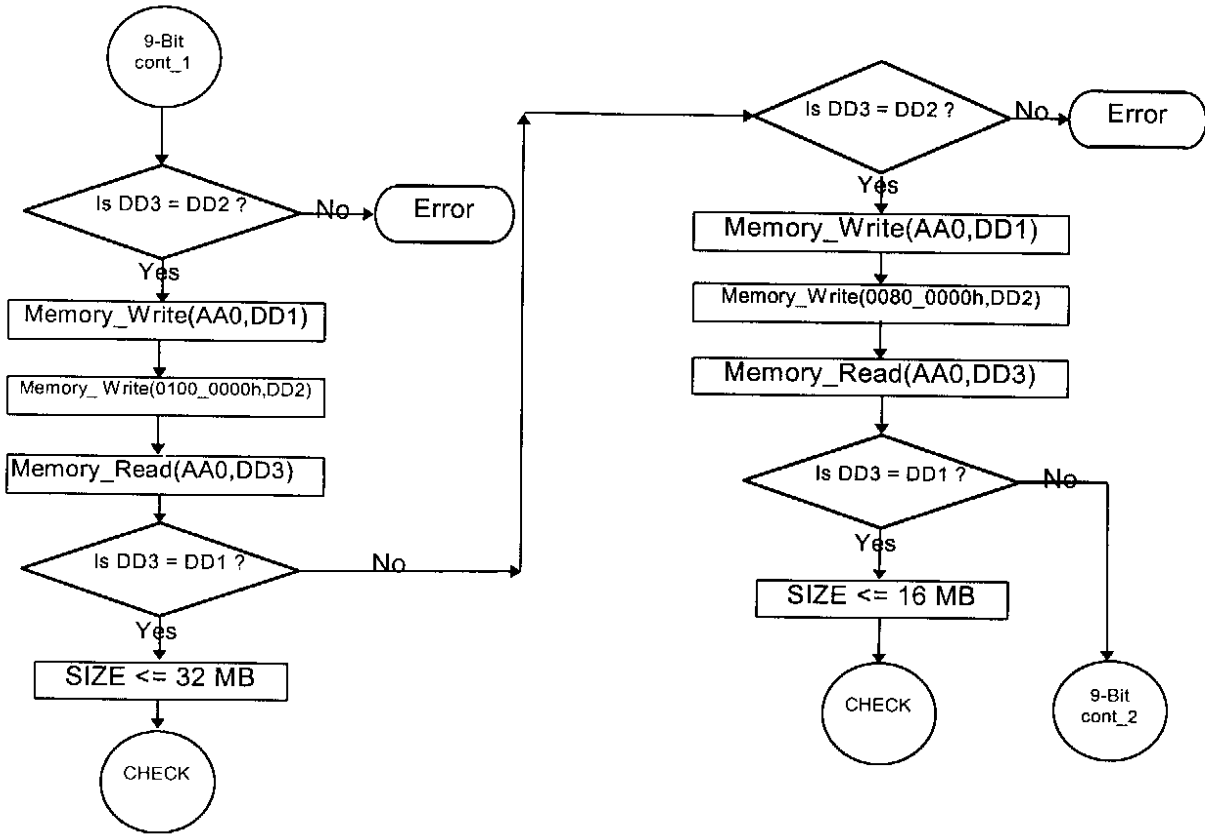

11-Bit cont_1
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0200_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 64 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0080_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Error
Yes
SIZE <= 32 MB
CHECK

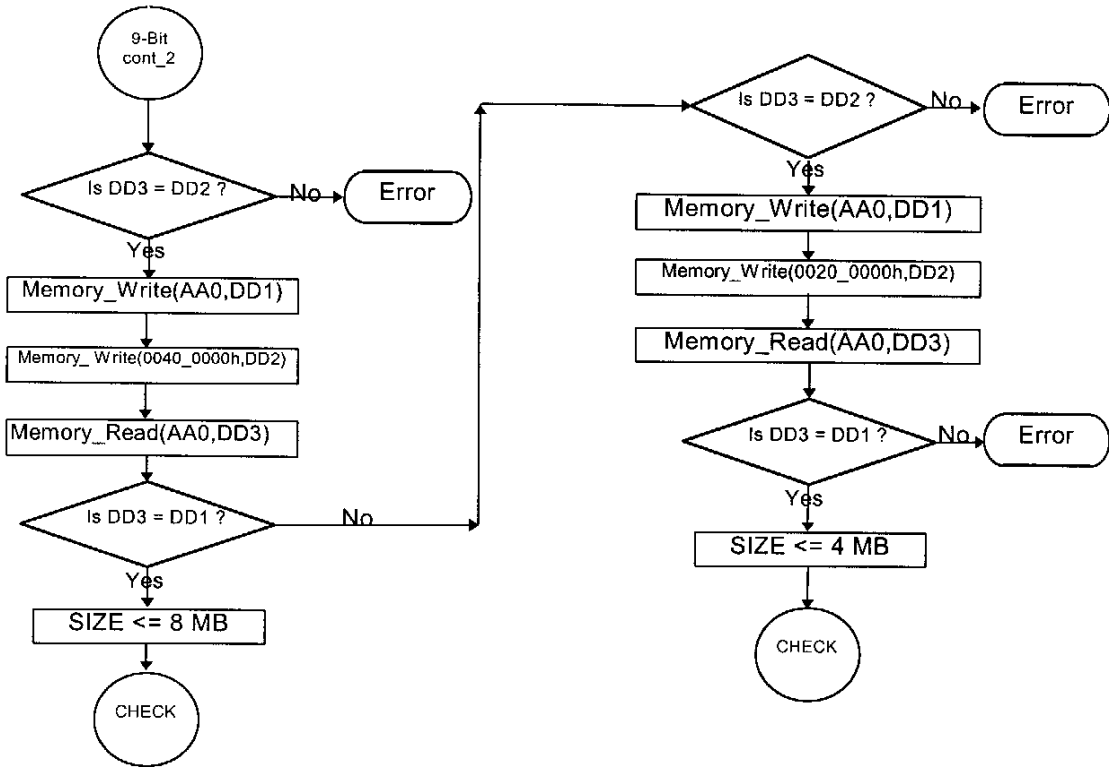

10-Bit CA DRAM Size Determination
Memory_Write(AA0,DD1)
Memory_ Write(0800_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 256 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0400_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
10-bit cont_1
Yes
SIZE <= 128 MB
CHECK

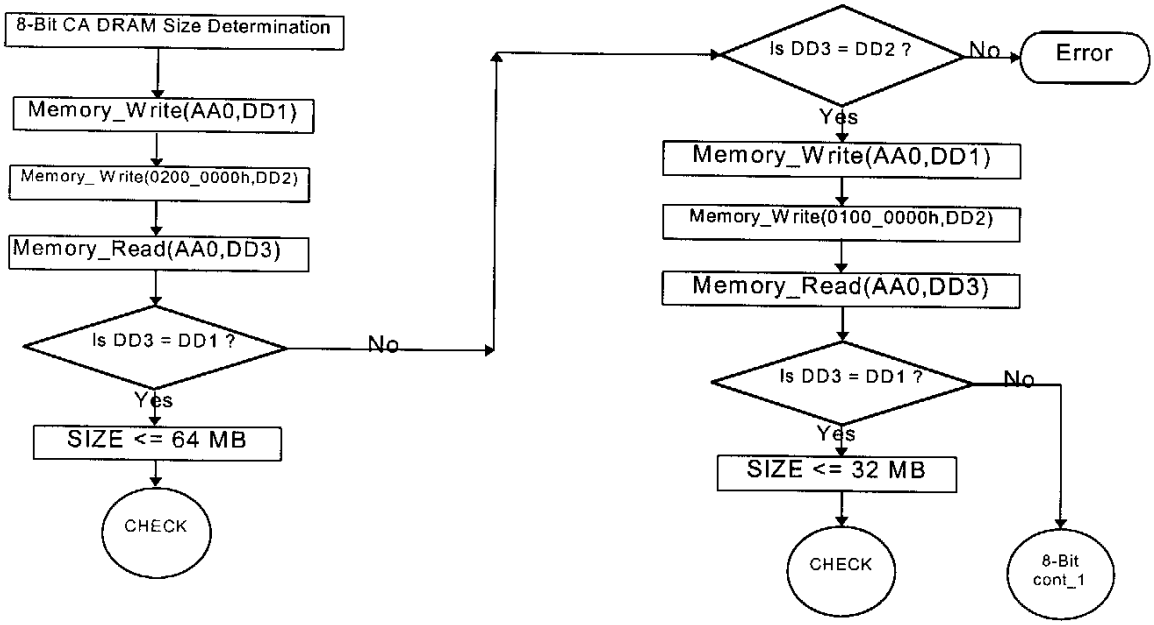

10-Bit cont_1
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0200_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 64 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0100_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 32 MB
CHECK
10-Bit cont_2

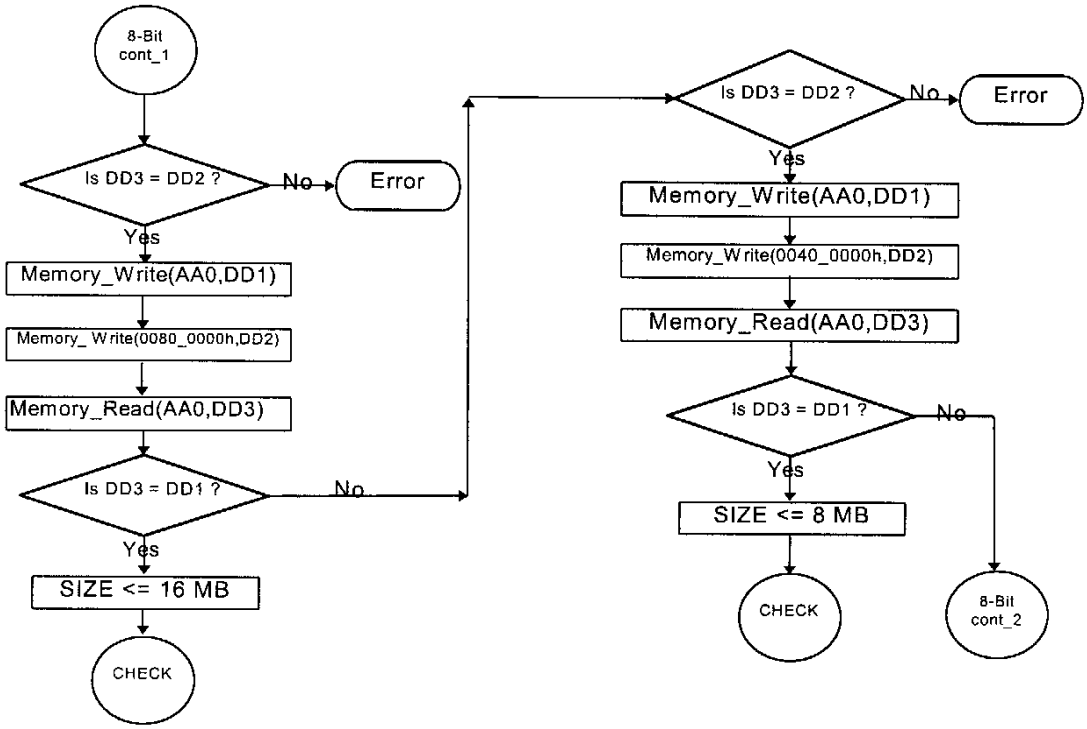

10-Bit
cont_2
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0080_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 16 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0020_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Error
Yes
SIZE <= 8 MB
CHECK

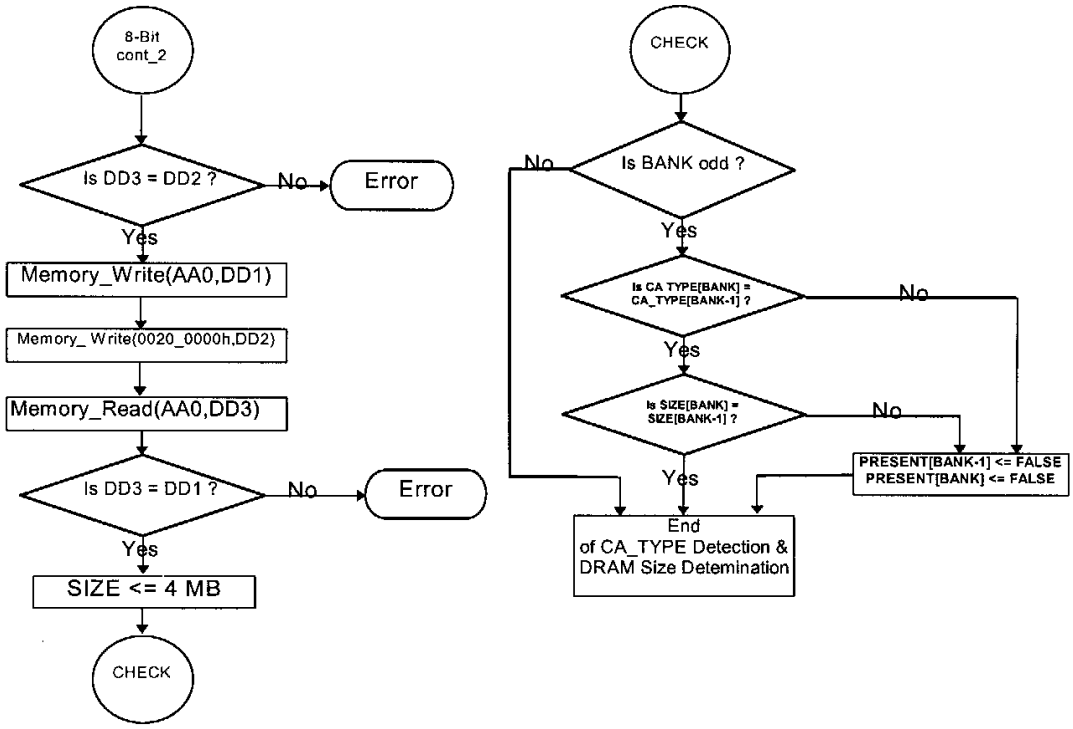

9-Bit CA DRAM Size Determination
Memory_Write(AA0,DD1)
Memory_ Write(0400_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 128 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0200_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 64 MB
CHECK
9-Bit
cont_1


9-Bit cont_1
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0100_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 32 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0080_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 16 MB
CHECK
9-Bit cont_2

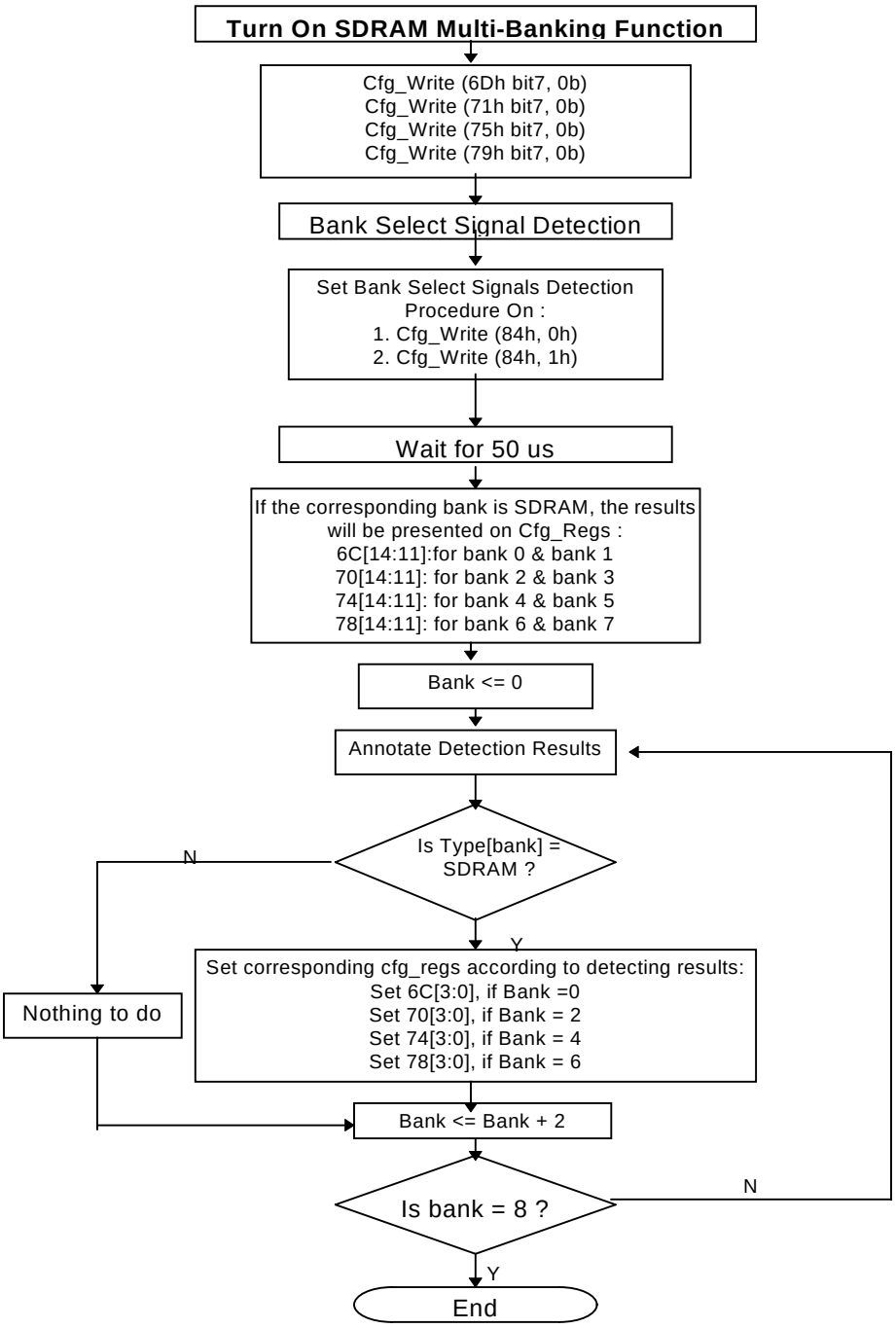

9-Bit
cont_2
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0040_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 8 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0020_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Error
Yes
SIZE <= 4 MB
CHECK


8-Bit CA DRAM Size Determination
Memory_Write(AA0,DD1)
Memory_ Write(0200_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 64 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0100_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 32 MB
CHECK
8-Bit cont_1


8-Bit cont_1
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0080_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 16 MB
CHECK
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_Write(0040_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Yes
SIZE <= 8 MB
CHECK
8-Bit cont_2

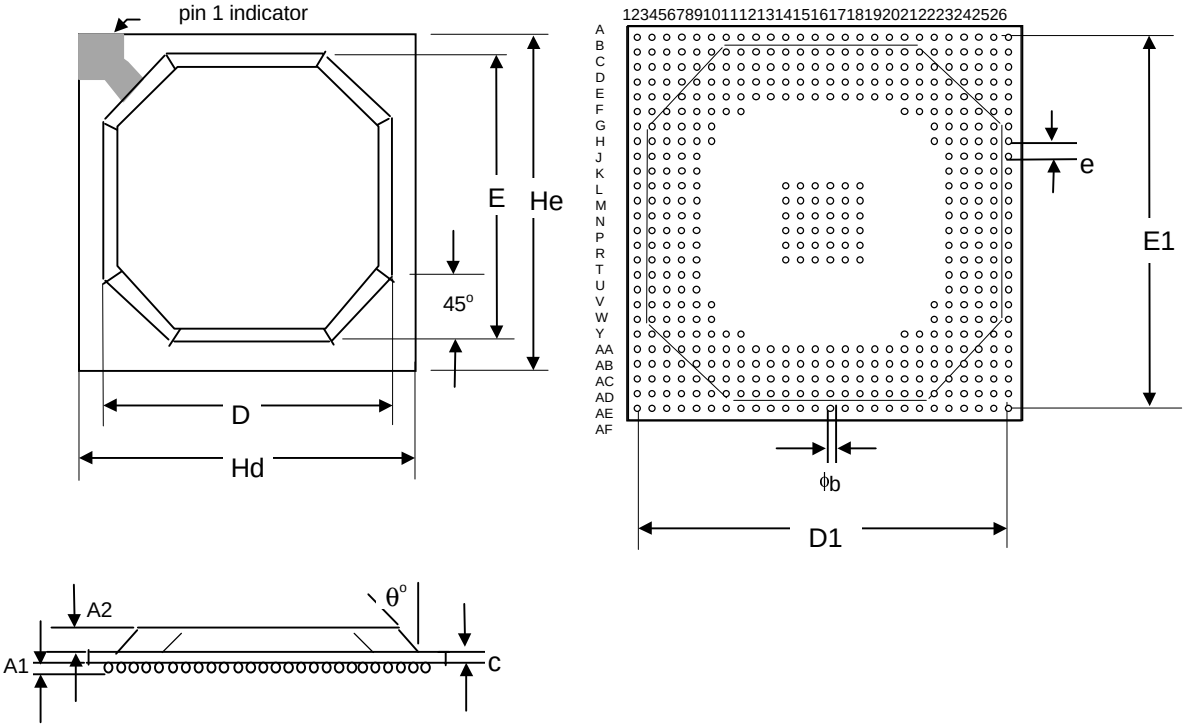

8-Bit cont_2
Is DD3 = DD2 ?
No
Error
Yes
Memory_Write(AA0,DD1)
Memory_ Write(0020_0000h,DD2)
Memory_Read(AA0,DD3)
Is DD3 = DD1 ?
No
Error
Yes
SIZE <= 4 MB
CHECK
CHECK
No
Is BANK odd ?
Yes
Is CA TYPE[BANK] = CA_TYPE[BANK-1] ?
No
Yes
Is SIZE[BANK] = SIZE[BANK-1] ?
No
Yes
PRESENT[BANK-1] <= FALSE
PRESENT[BANK] <= FALSE
End of CA_TYPE Detection & DRAM Size Detemination

In M1621, we support SDRAM Bank Select Signals auto-detection using hardware method, and after bank select detection, you can turn multi-bank on. The procedure is as follows :



Section 6 : Packaging Information

BGA -4 Dimension Specification (35 x 35 mm)
476 BGA



Symbol	Min.	Nom.	Max.
A1	0.55	0.60	0.65
A2	1.12	1.17	1.22
ϕb	0.60	0.75	0.90
c	0.51	0.56	0.61
D	29.80	30.00	30.20
D1	31.55	31.75	31.95
E	29.80	30.00	30.20
E1	31.55	31.75	31.95
e		1.27	
Hd	34.80	35.00	35.20
He	34.80	35.00	35.20
θ°	23°	30°	37°
Y(radius of ball)			0.25

Section 7 : Revision History

i.v.	12/97		
p. all	03/98		
p.53,68,88,102,109,111	04/20/98		
p.81,82,83,88,89,91,100	05/15/98		
p.15,40,49,55,56,58,59,63,67,78,81,83,88,90,91,100	07/13/98	v1.0	CCH
p.1,13,14,46,55	07/22/98	1.01	RK,CCH
p.88,89,90	12/02/98	v1.11	CCH

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