Am29114

Real-Time Interrupt Controller

PRELIMINARY

DISTINCTIVE CHARACTERISTICS

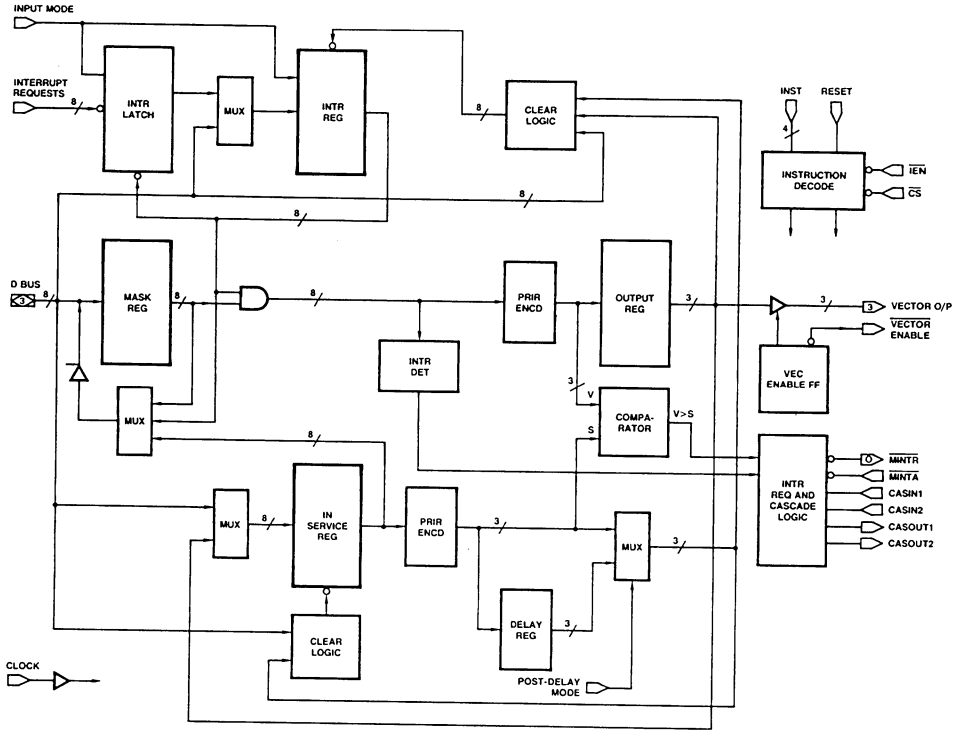
- **Real-Time Interrupt Servicing**
  Supports interrupts at microinstruction boundaries, making interrupt responses virtually instantaneous
- **Expandable**
  Cascadable to accept any number of interrupt inputs
- **Accepts Eight Interrupt Inputs**
  Interrupt request signals may be levels or pulses
- **Vector Outputs**
  Output is binary code for the highest priority un-masked interrupt request
- **On-Chip Prioritization**
  Only interrupts having higher priority than the highest interrupt in service are allowed
- **8-Bit Mask Register**
  Allows particular interrupt inputs to be temporarily disabled

GENERAL DESCRIPTION

The Am29114 is a high-performance 8-bit vectored priority interrupt controller intended for use in very high-speed microprogrammed machines. Its architecture and instruction set are optimized to take full advantage of the real-time interrupt capabilities of state-of-the-art sequencers such as the Am29C111.

The Am29114 features 16 microinstructions which allow designers to read from and write to key registers for maximum control flexibility.

BLOCK DIAGRAM



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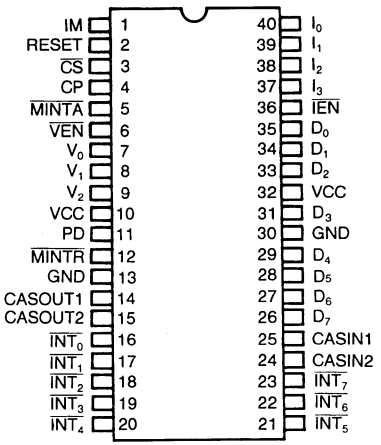
RELATED AMD PRODUCTS

Part No.	Description
Am2904	Status and Shift Control Unit
Am29C111	CMOS 16-Bit Microprocessor Sequencer
Am29116	High-Performance Bipolar 16-Bit Microprocessor
Am29C116	High-Performance CMOS 16-Bit Microprocessor
Am29118	8-Bit Bidirectional I/O Port/Accumulator
Am29PL141	Field-Programmable Controller
Am2925	System Clock Generator and Driver
Am29C323	CMOS 32-Bit Parallel Mulitplier
Am29325	32-Bit Floating Point Processor
Am29C325	CMOS 32-Bit Floating Point Processor
Am29331	16-Bit Microprogram Sequencer
Am29C331	CMOS 16-Bit Microprogram Sequencer
Am29332	32-Bit Extended Function ALU
Am29C332	CMOS 32-Bit Extended Function ALU
Am29334	64 x 18 Four-Port Dual-Access Register File
Am29C334	CMOS 64 x 18 Four-Port Dual-Access Register File
Am29337	16-Bit Bounds Checker
Am29338	Byte Queue
Am2940	DMA Address Generator
Am2942	Programmable Timer/Counter/DMA
Am2950A/ 51A/52A/53A	8-Bit Bidirectional I/O Port

CONNECTION DIAGRAM
Top View



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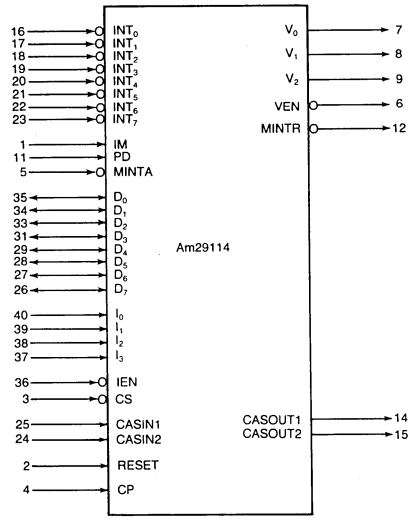
Note: Pin 1 is marked for orientation.

LOGIC SYMBOL

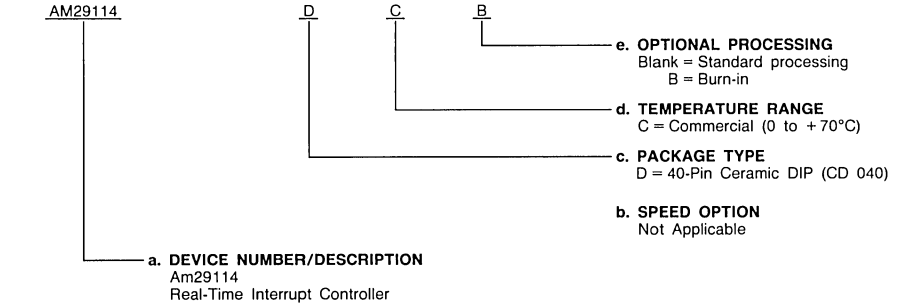


LS001880

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Package Type
d. Temperature Range
e. Optional Processing



Valid Combinations	
AM29114	DC, DCB

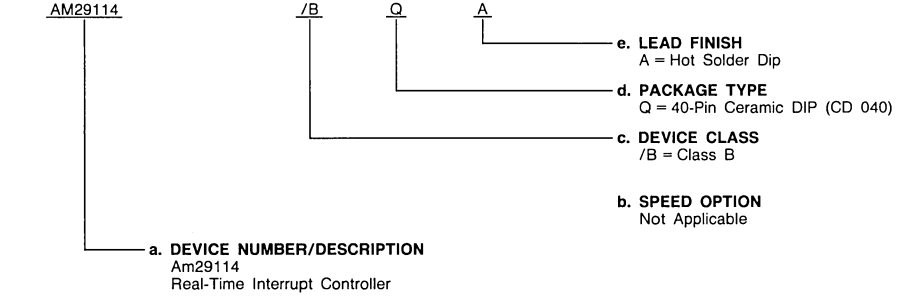
Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

MILITARY ORDERING INFORMATION

APL Products

AMD products for Aerospace and Defense applications are available in several packages and operating ranges. APL (Approved Products List) products are fully compliant with MIL-STD-883C requirements. The order number (Valid Combination) for APL products is formed by a combination of: **a. Device Number**
b. Speed Option (if applicable)
c. Device Class
d. Package Type
e. Lead Finish



Valid Combinations	
AM29114	/BQA

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations or to check for newly released valid combinations.

Group A Tests

Group A Tests consist of Subgroups
1, 2, 3, 7, 8, 9, 10, 11.

PIN DESCRIPTION

CASIN1 Cascade-In 1 (Input)
HIGH level forces $\overline{\text{MINTR}}$ HIGH and causes the CHSR and CCIR instructions to have no effect.

CASIN2 Cascade-In 2 (Input)
HIGH level forces $\overline{\text{MINTR}}$ HIGH and clears the vector-enable flip-flop on the next active clock edge.

CASOUT1 Cascade-Out 1 (Output)
Forced HIGH if any bit in the in-service register is set or if CASIN1 is HIGH.

CASOUT2 Cascade-Out 2 (Output)
Forced HIGH if there is an unmasked interrupt request in the interrupt register, or if CASIN2 is HIGH.

CP Clock Pulse (Input)
All state changes occur on the LOW-to-HIGH transition of the clock.

$\overline{\text{CS}}$ Chip Select (Input; Active LOW)
Instructions 4 – 15 (those that use the D-bus) are ignored if $\overline{\text{CS}}$ is HIGH.

$D_0 - D_7$ Data Lines (Input/Output)
Used to transfer information between the system data bus and the mask, interrupt, and in-service registers of the Am29114.

$I_0 - I_3$ Instruction (Inputs)

$\overline{\text{IEN}}$ Instruction Enable (Input; Active LOW)
The instruction on $I_0 - I_3$ is ignored if $\overline{\text{IEN}}$ is HIGH.

$\overline{\text{INT}_0} - \overline{\text{INT}_7}$ Interrupt (Inputs; Active LOW)
Accepts requests as active-LOW levels or pulses, depending on the level at the IM pin.

IM Input Mode Select (Input)
When IM is LOW, $\overline{\text{INT}_0} - \overline{\text{INT}_7}$ detect asynchronous pulse inputs. When IM is HIGH, $\overline{\text{INT}_0} - \overline{\text{INT}_7}$ detect level inputs.

$\overline{\text{MINTA}}$ Maskable Interrupt Acknowledge (Input; Active LOW)
Active-LOW signal causes the interrupting request vector in the vector output register to be enabled onto the vector output pins ($V_0 - V_2$). It also causes the bit corresponding to the interrupting request to be cleared in the interrupt register and set in the in-service register. Note: to permit cascading, these operations occur if the $\overline{\text{VEN}}$ output is LOW (i.e., vector-enable flip-flop is set).

$\overline{\text{MINTR}}$ Maskable Interrupt (Output; Active LOW)
LOW level indicates that an unmasked interrupt request that has a priority higher than the request currently being serviced is in the interrupt register waiting for service. $\overline{\text{MINTR}}$ is forced HIGH when either $\overline{\text{MINTA}}$ is LOW, or CASIN1 or CASIN2 are HIGH. $\overline{\text{MINTR}}$ is an open-collector output.

PD Post-Delay Mode (Input)
Hard-wire HIGH when operating with the Am29112 in post-delay mode. HIGH level causes the CASIN1 input and prioritized output of the in-service register to be delayed by one clock cycle.

RESET Master Reset (Input)
HIGH level causes the interrupt latches, interrupt register, in-service register, and mask register to be cleared on the next active clock edge.

$V_0 - V_2$ Interrupt Vector (Output; Three State)
Three-state $V_0 - V_2$ lines are output enabled with the interrupting vector when the $\overline{\text{MINTA}}$ input is LOW and the $\overline{\text{VEN}}$ output is LOW (i.e., vector-enable flip-flop is set).

$\overline{\text{VEN}}$ Vector Enable (Output; Active LOW)
Output of vector-enable flip-flop. The vector-enable flip-flop is cleared ($\overline{\text{VEN}}$ HIGH) on the next active clock edge when CASIN2 is HIGH. When CASIN2 is LOW, the vector-enable flip-flop is set ($\overline{\text{VEN}}$ LOW) on each active clock edge if an unmasked interrupt is waiting in the interrupt register; otherwise it is cleared.

FUNCTIONAL DESCRIPTION

The Am29114 receives interrupt requests on eight interrupt input lines ($\text{INT}_0 - \text{INT}_7$). A LOW level is a request. An internal latch may be used to catch pulses on these lines, or the latch may be bypassed so the request lines drive the edge-triggered interrupt register directly. An 8-bit mask register is used to mask individual interrupts. Requests in the interrupt register are ANDed with the corresponding bits in the mask register and the result is sent to a priority encoder, which produces a 3-bit encoded vector representing the highest numbered input which is not masked. This encoded vector will be held in the vector output register.

An 8-bit in-service register holds a bit for each interrupt request that is currently being serviced. If a new interrupt has a higher priority than the one in process, an interrupt request output will occur and this signal will be sent to the sequencer. Subsequently, an acknowledge signal from the sequencer is used to enable the vector outputs and to set the corresponding bit in the in-service register to prevent the interrupt routine from being interrupted by a lower priority interrupt. When the service routine is complete, an instruction clearing the in-service register bit allows system operation to continue as before.

The Am29114 is controlled by a 4-bit instruction field which allows the three above-mentioned registers to be read or modified under microprogram control.

Architecture Of The Am29114

The Am29114 is a high-performance priority interrupt controller. As shown in the Block Diagram, the device contains four registers: the Interrupt Register, the Mask Register, the In-Service Register, and the Vector Output Register.

Interrupt Latch/Register

The 8-bit Interrupt Register stores pending interrupt requests in clocked D flip-flops. A bit in the register is automatically cleared when the corresponding interrupt request is acknowledged by the system sequencer. Interrupt requests can be accepted via eight S-R latches in either of two modes depending on the level of the IM input.

Asynchronous Pulse Mode: LOW-going pulses on the $\overline{\text{INT}}$ inputs set the latches. The outputs of the latches cause the respective flip-flops to be set on the next active clock edge. The outputs of the flip-flops are then used to clear the latches. Requests remain stored in the register until their interrupts are acknowledged.

Level Mode: The latches become transparent, and the Interrupt Register contains the interrupt requests only as long as the corresponding $\overline{\text{INT}}$ lines are held LOW. Therefore, in order to be recognized, an interrupt signal must be held LOW until it is acknowledged.

Bits may also be set in the Interrupt Register under microprogram control, thus permitting software-generated interrupts.

Mask Register

The 8-bit Mask Register allows selected interrupt inputs to be disabled. When a bit is set, the corresponding output of the Interrupt Latch Register is disabled without affecting the Interrupt Register itself.

In-Service Register

The 8-bit In-Service Register keeps track of which interrupt requests have been accepted by the system sequencer for servicing. When a bit corresponding to a particular interrupt is set, all equal and lower priority interrupts are masked. Once a bit in the In-Service Register is set, a micro-instruction must be issued to clear it.

Vector Output Register

The 3-bit Vector Output Register is loaded on each active clock edge with the priority code of the highest-priority unmasked interrupt currently in the Interrupt Register.

Interrupt Detector/Priority Encoder

The Interrupt Detector detects the presence of an unmasked interrupt waiting for service. The Priority Encoder determines the highest-priority unmasked interrupt waiting for service and forms a binary-coded interrupt vector.

Comparator

The 3-bit Comparator determines whether or not the priority of the highest unmasked interrupt waiting for service is higher than the priority of the interrupt currently being serviced.

Clear Control Logic

The Clear Control Logic generates clear signals for individual bits of the Interrupt and In-Service Registers. The Clear Control Logic takes inputs from the D-Bus and from the Vector Output Register (after an interrupt acknowledge is received).

Interface Logic

The Interface Logic circuitry generates the interrupt, vector enable, and cascade signals.

Instruction Set

The Am29114 is controlled by the 4-bit instruction inputs $I_0 - I_3$. The instruction input is ignored if $\overline{IEN}$ is HIGH, allowing the four I bits in the instruction word to be shared with other functions. Instructions that access the D-Bus (instructions 4 – 15) are ignored if $\overline{CS}$ is HIGH, allowing the D-Buses of several Am29114s in a cascaded system to be tied together (see Table 1).

TABLE 1. INSTRUCTION SET

I_3	I_2	I_1	I_0	Mnemonic	Description
0	0	0	0	MCLR	Master Clear
0	0	0	1	CHSR	Clear highest priority bit in In-Service Register (Note 1)
0	0	1	0	CCIR	Clear current interrupt bit in Interrupt Register (Note 2)
0	0	1	1	NOOP	No Operation
0	1	0	0	BSMK	Bit set Mask Register from D-Bus (Note 3)
0	1	0	1	BCMK	Bit clear Mask Register from D-Bus (Note 4)
0	1	1	0	LDMK	Load Mask Register from D-Bus
0	1	1	1	RDMK	Read Mask Register from D-Bus
1	0	0	0	BSSR	Bit set In-Service Register from D-Bus (Notes 3 & 5)
1	0	0	1	BCSR	Bit clear In-Service Register from D-Bus (Notes 4 & 5)
1	0	1	0	LDSR	Load In-Service Register from D-Bus (Note 5)
1	0	1	1	RDSR	Read In-Service Register from D-Bus (Note 5)
1	1	0	0	BSIR	Bit set Interrupt Register from D-Bus (Notes 3 & 6)
1	1	0	1	BCIR	Bit clear Interrupt Register from D-Bus (Notes 4 & 6)
1	1	1	0	LDIR	Load Interrupt Register from D-Bus (Note 6)
1	1	1	1	RDIR	Read Interrupt Register from D-Bus (Note 6)

NOTES:

1. CHSR may be used at the end of an interrupt service routine to restore the previous priority level. In post-delay mode, CHSR clears the bit that had the highest priority one clock cycle before the instruction arrived at the instruction inputs.
2. CCIR clears the Interrupt Register bit corresponding to the highest bit set in the In-Service Register. In post-delay mode, CCIR clears the bit in the Interrupt Register corresponding to the bit that had the highest priority in the In-Service Register one clock cycle before the instruction arrived at the instruction inputs.
3. Sets those register bits that have corresponding D-Bus bits equal to one. Other register bits are not affected.
4. Clears those register bits that have corresponding D-Bus bits equal to one. Other register bits are not affected.
5. Overrides the effect of an interrupt request or an interrupt acknowledge on bits being modified if received during the same clock cycle.
6. An interrupt acknowledge received during the same clock cycle will override this instruction where they affect the same bit.

APPLICATIONS

System Implementation

Connection to Am29C111

The Am29114 is connected to the Am29C111 as shown in Figure 1. The three-state vector outputs are connected to three bits of the Y-bus of the Am29C111. The other 13 bits of the Y-bus are taken from the outputs of a three-state buffer. The inputs of the buffer may be hardwired to define the other 13 bits of the interrupt jump address. The $\overline{INTA}$ output of the Am29C111 is used to enable the vector output onto the Y-bus. The instruction inputs to the Am29114 are taken from the microinstruction pipeline register, and the D-Bus is connected to the data highway of the system. In a system employing only a single Am29114, the CASIN1 and CASIN2 are hardwired LOW.

Cascading Am29114s

Am29114s are cascaded by connecting the CASOUT1 and CASOUT2 signals of one chip to the CASIN1 and CASIN2 of the next most significant chip (see Figures 2 and 3). CASIN1 and CASIN2 of the most significant chip are usually tied LOW, but open-collector CASIN2 may be forced HIGH in order to disable all interrupts. The $\overline{\text{MINTR}}$ outputs are tied together to form one common interrupt line. Also common to all chips are the instruction enable, instruction, acknowledge, reset, and clock lines. The D-Bus pins of each chip may either be tied together or left separate if the width of the system bus allows. If tied together, the chip-select inputs may be used to select a particular chip for D-Bus operations.

The vector outputs of each chip are tied together to form the least significant three bits of the interrupt vector. There are two ways of forming the most significant bits of the interrupt vector. In Method 1 (Figure 2), a priority encoder with tri-state outputs is used to priority encode the vector-enable outputs. In Method 2 (Figure 3), the priority encode of the CASOUT2 outputs is clocked into a register with tri-state outputs. Method 2 may be useful where it is necessary to remove the priority encoder from a critical timing path that includes the microprogram memory. If only two Am29114s are cascaded, the vector-enable output of the least significant chip may be used directly as the fourth bit of the interrupt vector (Figure 4).

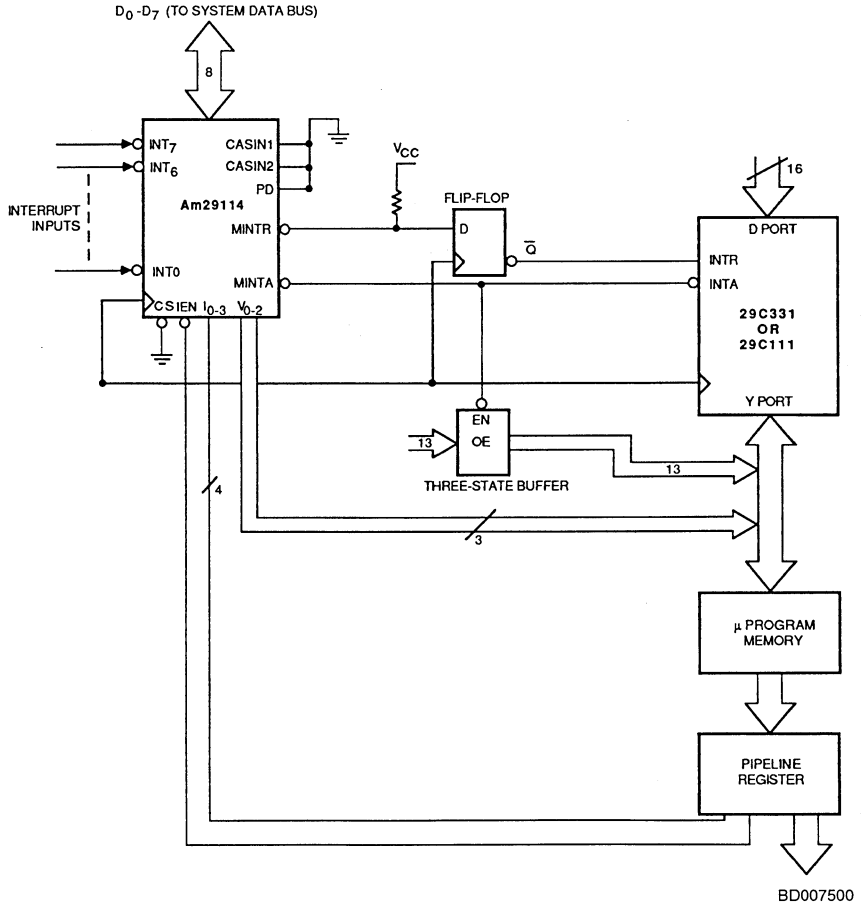


Figure 1. Connection of Am29114 to Am29C111

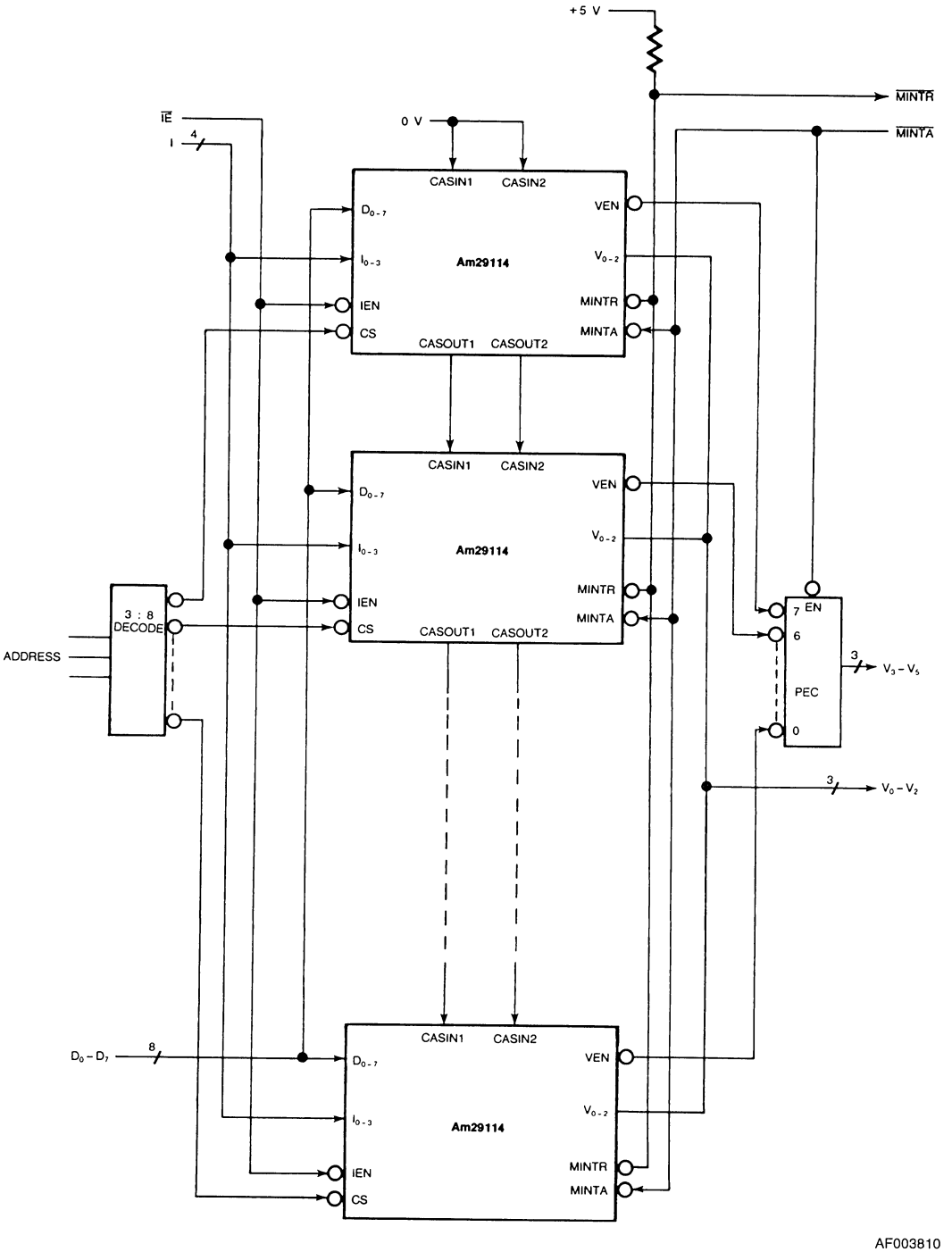


Figure 2. Cascading the Am29114 – Method 1

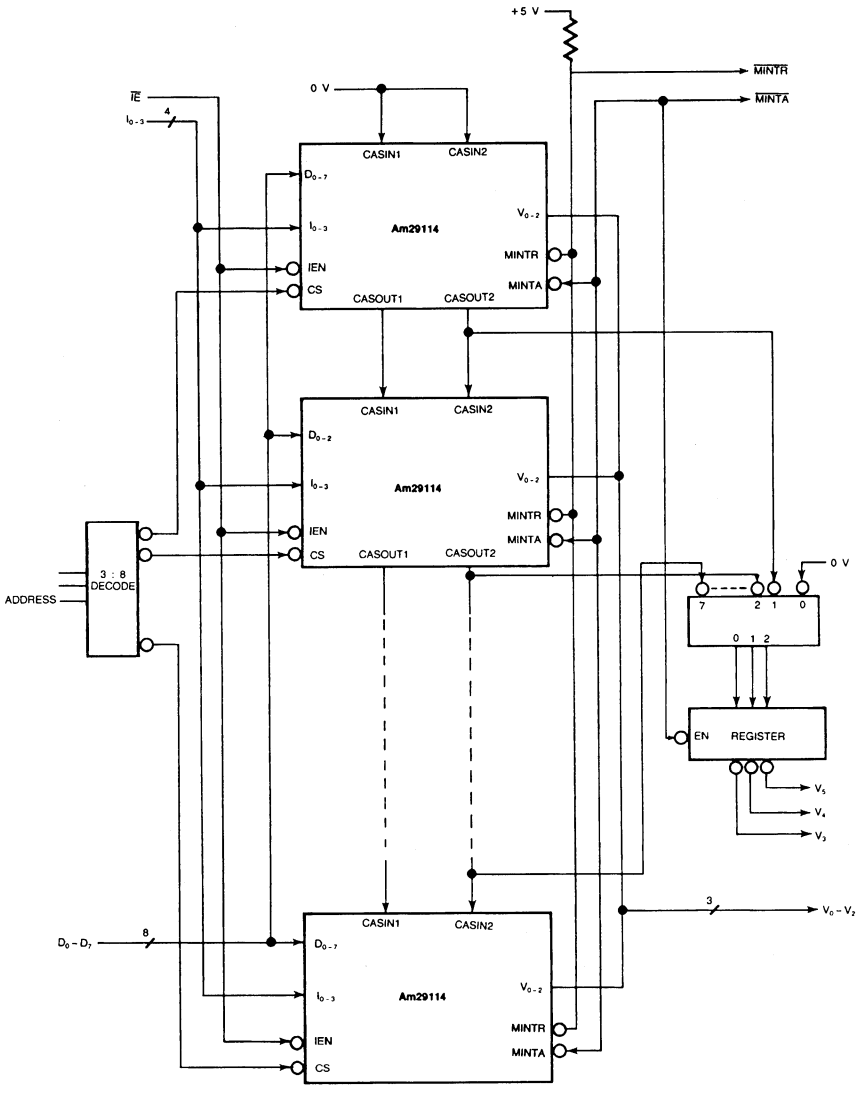


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Figure 3. Cascading the Am29114 – Method 2

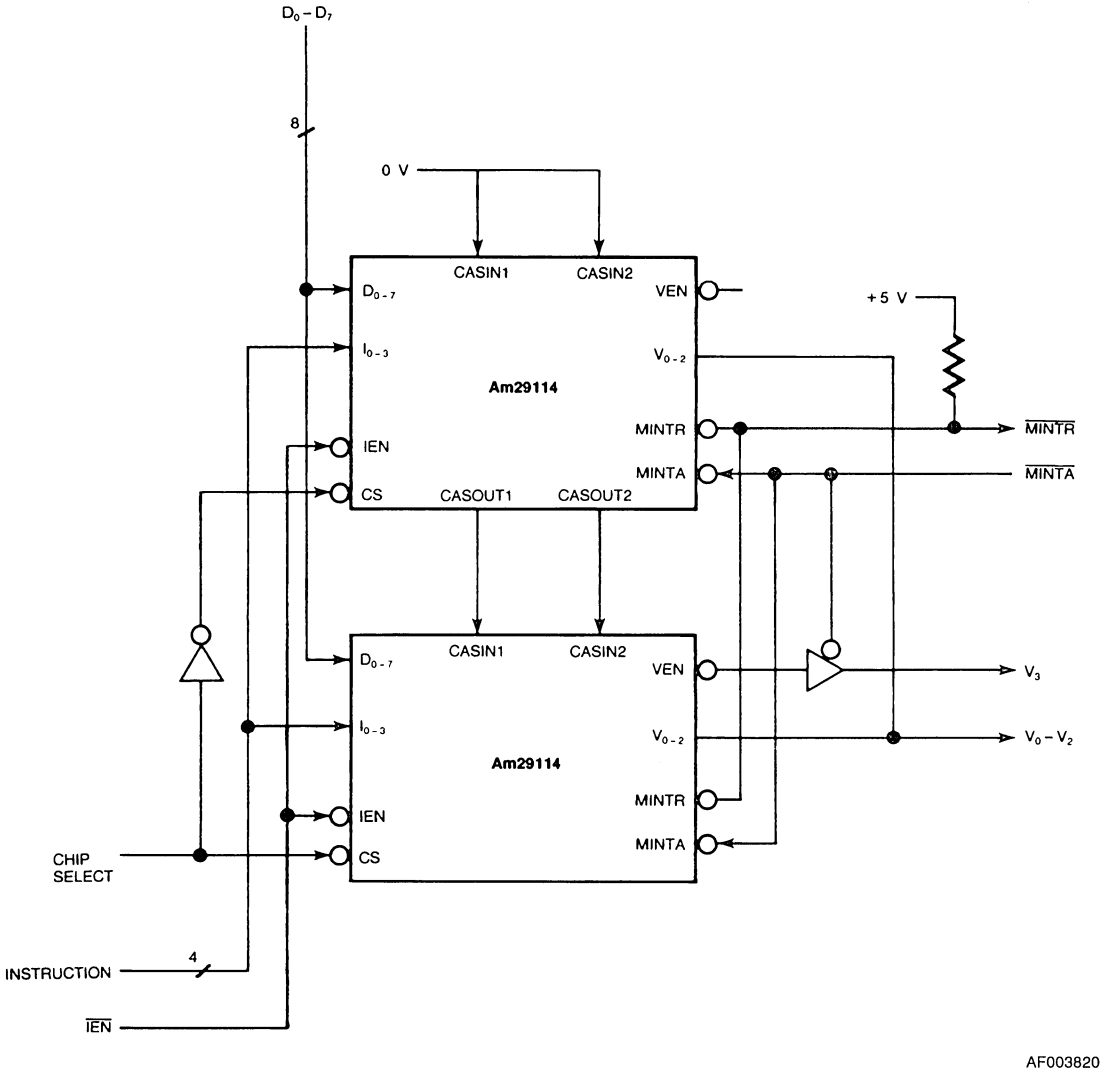


Figure 4. Cascading the Am290114 – 16-Bit Configuration

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65 to +150°C
Case Temperature Under Bias ..... −55 to +125°C
Supply Voltage to Ground Potential ..... −0.5 to +7.0 V
DC Voltage Applied to Outputs for HIGH Output State ..... −0.5 to +V_{CC} Max.
DC Input Voltage ..... −0.5 to +5.5 V
DC Output Current, Into Outputs ..... 30 mA
DC Input Current ..... −30 to +5.0 mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Ambient Temperature (T_A) ..... 0 to +70°C
Supply Voltage (V_{CC}) ..... +4.75 to +5.25 V

Military* (M) Devices
Case Temperature (T_C) ..... −55 to +125°C
Supply Voltage (V_{CC}) ..... +4.5 to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

*Military product 100% tested at T_C = +25°C, +125°C, and −55°C.

DC CHARACTERISTICS over operating range unless otherwise specified (for APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted)

Parameter Symbol	Parameter Description	Test Conditions (Note 1)			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	All Outputs Except MINTR	I_{OH} = −1.6 mA (COM'L)	2.4		V
				I_{OH} = −1.2 mA (MIL)			
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	All Outputs			0.5	V
V_{IH}	Guaranteed Input Logical HIGH Voltage (Note 5)		All Inputs		2.0		V
V_{IL}	Guaranteed Input Logical LOW Voltage (Note 5)		All Inputs			0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min.	All Inputs	I_{IN} = −18 mA		−1.5	V
I_{IL}	Input LOW Current	V_{CC} = Max., V_{IN} = 0.5 V (Note 3)	All Inputs			−1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = Max., V_{IN} = 2.4 V (Note 3)	All Inputs			100	μA
I_I	Input HIGH Current	V_{CC} = Max., V_{IN} = 5.5 V	All Inputs			1.0	mA
I_{OZH}	Off-State (High Impedance) Output Current	V_{CC} = Max., V_O = 2.4 V (Note 3)	D_{0-7}, V_{0-2}			100	μA
I_{OZL}	Off-State (High Impedance) Output Current	V_{CC} = Max., V_O = 0.5 V (Note 3)	D_{0-7}, V_{0-2}			−1000	μA
I_{OS}	Output Short-Circuit Current	V_{CC} = Max. + 0.5 V V_O = 0.5 V (Note 3)	All Outputs Except $\overline{MINTR}$		−30	−100	mA
I_{CEX}	Output Leakage Current for $\overline{MINTR}$ = 0 Output	V_{CC} = Min., V_O = 5.5 V (Note 7) V_{IN} = V_{IH} or V_{IL}	$\overline{MINTR}$			250	μA
I_{CC}	Power Supply Current (Note 4)	V_{CC} = Max.	COM'L	T_A = 0 to +70°C (Note 6)		360	mA
				T_A = +70°C		340	
			MIL	T_C = −55 to +125°C (Note 6)			mA
				T_C = +125°C			

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Operating Ranges for the applicable device type.
2. Not more than one output should be shorted at a time. Duration of the short-circuit test should not exceed one second.
3. Y_{0-15}, T_{1-4} are three-state outputs internally connected to TTL inputs. Input characteristics are measured under conditions such that the outputs are in the OFF state.
4. Worst-case I_{CC} is a minimum temperature.
5. These input levels provide zero noise immunity and should be tested only in a static, noise-free environment.
6. Cold start.
7. $\overline{MINTR}$ is an open-collector output.

A. Delay Times

No.	Parameter Symbol	Parameter Description	COM'L		MIL		Unit
			Min.	Max.	Min.	Max.	
1	t_{PC1MR}	Delay from CASIN1 to $\overline{MINTR}$		19			ns
2	t_{PC2MR}	Delay from CASIN2 to $\overline{MINTR}$		20			ns
3	t_{PCPMR}	Delay from CP to $\overline{MINTR}$		25			ns
4	t_{PMAMR}	Delay from $\overline{MINTA}$ to $\overline{MINTR}$		18			ns
5	t_{PCPVN}	Delay from CP to $\overline{VEN}$		19			ns
6	t_{PC1C1}	Delay from CASIN1 to CASOUT1		15			ns
7	t_{PCPC1}	Delay from CP to CASOUT1		23			ns
8	t_{PC2C2}	Delay from CASIN2 to CASOUT2		16			ns
9	t_{PCPC2}	Delay from CP to CASOUT2		24			ns
10	t_{PCPD}	Delay from CP to D_{0-7}		19			ns

B. Setup and Hold Times

No.	Parameter Symbol	Parameter Description	COM'L		MIL		Unit
			Min.	Max.	Min.	Max.	
11	t_{SINT}	$\overline{INT}_{0-7}$ Setup Time	5				ns
12	t_{HINT}	$\overline{INT}_{0-7}$ Hold Time	4				ns
13	t_{SCAS1}	CASIN1 Setup Time	5				ns
14	t_{HCAS1}	CASIN1 Hold Time	5				ns
15	t_{SCAS2}	CASIN2 Setup Time	4				ns
16	t_{HCAS2}	CASIN2 Hold Time	4				ns
17	t_{SMA}	$\overline{MINTA}$ Setup Time	4				ns
18	t_{HMA}	$\overline{MINTA}$ Hold Time	2				ns
19	t_{SCS}	$\overline{CS}$ Setup Time	7				ns
20	t_{HCS}	$\overline{CS}$ Hold Time	3				ns
21	t_{SIEN}	$\overline{IEN}$ Setup Time	5				ns
22	t_{HIEN}	$\overline{IEN}$ Hold Time	4				ns
23	t_{SI}	I_{0-3} Setup Time	21*		*		ns
24	t_{HI}	I_{0-3} Hold Time	5*		*		ns
25	t_{SD}	D_{0-7} Setup Time	7				ns
26	t_{HD}	D_{0-7} Hold Time	4				ns
27	t_{SRST}	RESET Setup Time	7				ns
28	t_{HRST}	RESET Hold Time	3				ns
29	t_{SIM}	IM Setup Time	3				ns
30	t_{HIM}	IM Hold Time	2				ns
31	t_{SPD}	PD Setup Time	7				ns
32	t_{HPD}	PD Hold Time	2				ns

*These specifications are derived but are not tested.

C. Enable/Disable Times

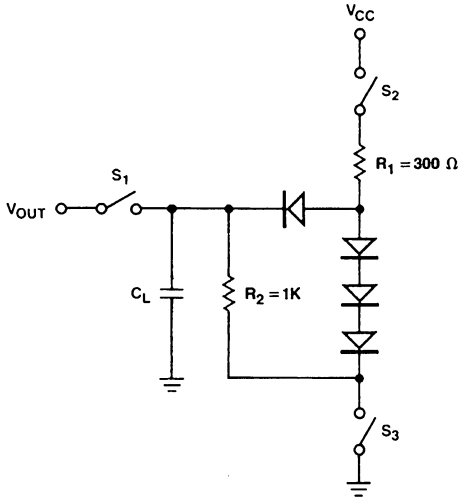
No.	Parameter Symbol	Parameter Description	COM'L		MIL		Unit
			Min.	Max.	Min.	Max.	
33	t_{EMAV}	$\overline{MINTA}$ Enable V_{0-2}	21				ns
34	t_{DMAV}	$\overline{MINTA}$ Disable V_{0-2}	24				ns
35	t_{ECPV}	CP Enable V_{0-2}	27				ns
36	t_{DCPV}	CP Disable V_{0-2}	28				ns
37	t_{ECSD}	$\overline{CS}$ Enable D_{0-7}	26				ns
38	t_{DCSD}	$\overline{CS}$ Disable D_{0-7}	27				ns
39	t_{EIND}	$\overline{IEN}$ Enable D_{0-7}	26				ns
40	t_{DIND}	$\overline{IEN}$ Disable D_{0-7}	27				ns
41	t_{EID}	I_{0-3} Enable D_{0-7}	26				ns
42	t_{DID}	I_{0-3} Disable D_{0-7}	27				ns
43	t_{ERSD}	RESET Enable D_{0-7}	26				ns
44	t_{DRST}	RESET Disable D_{0-7}	27				ns

D. Clock Times

No.	Parameter Symbol	Parameter Description	COM'L		MIL		Unit
			Min.	Max.	Min.	Max.	
45	t_{CPH}	Clock HIGH Time	15				ns
46	t_{CPL}	Clock LOW Time	15				ns
47	t_{CP}	Clock Period	40				ns
48	t_{INTL}	Interrupt LOW Time for Guaranteed Acceptance*	15				ns
49	t_{INT1}	Required Interrupt LOW Time to Guarantee Automatic Clearing of Interrupt Reg.*		$2T_{CP}$		$2T_{CP}$	ns

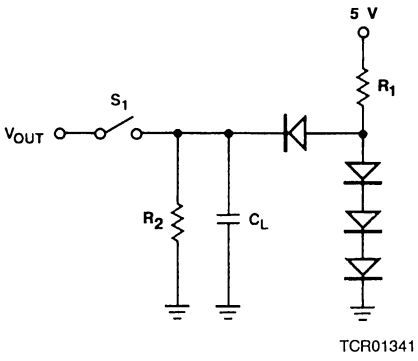
*Asynchronous Pulse Mode
T_{CP} = Clock Period

SWITCHING TEST CIRCUITS



TCR01331

A. Three-State Outputs
$R_1 = 300\ \Omega$



TCR01341

B. Normal Outputs
$R_1 = 300\ \Omega$
$R_2 = 3.0\ k\Omega$

Notes: 1. $C_L = 50$ pf includes scope probe, wiring, and stray capacitances without device in test fixture.
2. S_1, S_2, S_3 are closed during function tests and all AC tests except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{PZH} test.
S_1 and S_2 are closed while S_3 is open for t_{PZL} test.
4. $C_L = 5.0$ pF for output disable tests.

Test Philosophy and Methods

The following points give the general philosophy that we apply to tests that must be properly engineered if they are to be implemented in an automatic environment. The specifics of what philosophies applied to which test are shown.

1. Ensure the part is adequately decoupled at the test head. Large changes in V_{CC} current as the device switches may cause erroneous function failures due to V_{CC} changes.
2. Do not leave inputs floating during any tests, as they may oscillate at high frequency.
3. Do not attempt to perform threshold tests at high speed. Following an input transition, ground current may change by as much as 400 mA in 5 – 8 ns. Inductance in the ground cable may allow the ground pin at the device to rise by hundreds of millivolts momentarily. Current level may vary from product to product.
4. Use extreme care in defining input levels for AC tests. Many inputs may be changed at once, so there will be significant noise at the device pins which may not actually reach V_{IL} or V_{IH} until the noise has settled. AMD recommends using $V_{IL} \leqslant 0$ V and $V_{IH} \geqslant 3.0$ V for AC tests.
5. To simplify failure analysis, programs should be designed to perform DC, Function, and AC tests as three distinct groups of tests.
6. Capacitive Loading for AC Testing

   Automatic testers and their associated hardware have stray capacitance that varies from one type of tester to another but is generally around 50 pF. This makes it impossible to make direct measurements of parameters that call for a smaller capacitive load than the associated stray capacitance. Typical examples of this are the so-called "float delays," which measure the propagation delays into and out of the high-impedance state and are usually specified at a load capacitance of 5.0 pF. In these cases, the test is performed at the higher load capacitance (typically 50 pF), and engineering correlations based on data taken with a bench setup are used to predict the result at the lower capacitance.

   Similarly, a product may be specified at more than one capacitive load. Since the typical automatic tester is not capable of switching loads in mid-test, it is impossible to make measurements at <u>both</u> capacitances even though they may both be greater than the stray capacitance. In these cases, a measurement is made at one of the two capacitances. The result at the other capacitance is predicted from engineering correlations based on data taken with a bench setup and the knowledge that certain DC measurements (I_{OH}, I_{OL}, for example) have already been taken and are within spec. In some cases, special DC tests are performed in order to facilitate this correlation.
7. Threshold Testing

   The noise associated with automatic testing, (due to the long inductive cables) and the high gain of the tested device when in the vicinity of the actual device threshold frequently give rise to oscillations when testing high-speed circuits. These oscillations are not indicative of a reject device, but instead, of an overtaxed test system. To minimize this problem, thresholds are tested at least once for <u>each</u> input pin. Thereafter, "hard" high and low levels are used for other tests. Generally this means that function and AC testing are performed at "hard" input levels rather than at V_{IL} Max. and V_{IH} Min.
8. AC Testing

   Occasionally parameters are specified that cannot be measured directly on automatic testers because of tester limitations. Data input hold times often fall into this category. In these cases, the parameter in question is guaranteed by correlating these tests with other AC tests that have been performed. These correlations are arrived at by the cognizant engineer using data from precise bench measurements in conjunction with the knowledge that certain DC parameters have already been measured and are within spec.

   In some cases, certain AC tests are redundant since they can be shown to be predicted by other tests that have already been performed. In these cases, the redundant tests are not performed.
9. Output Short-Circuit Testing

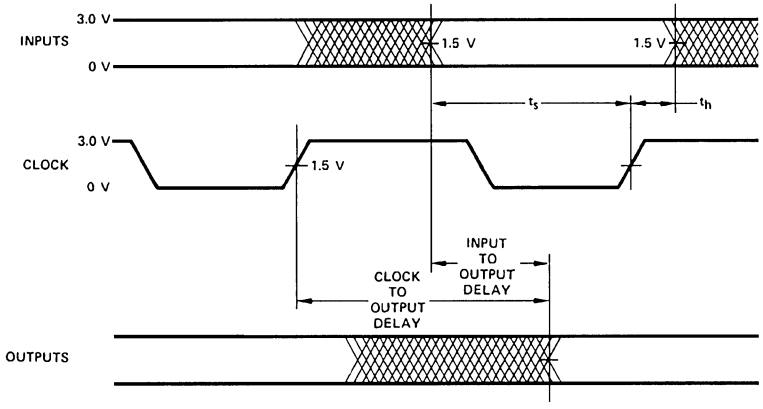
   When performing I_{OS} tests on devices containing RAM or registers, great care must be taken that undershoot caused by grounding the high-state output does not trigger parasitic elements which in turn cause the device to change state. In order to avoid this effect, it is common to make the measurement at a voltage (V_{output}) that is slightly above ground. The V_{CC} is raised by the same amount so that the result (as confirmed by Ohm's law and precise bench testing) is identical to the $V_{OUT} = 0$, V_{CC} = Max. case.

SWITCHING WAVEFORMS

KEY TO SWITCHING WAVEFORMS

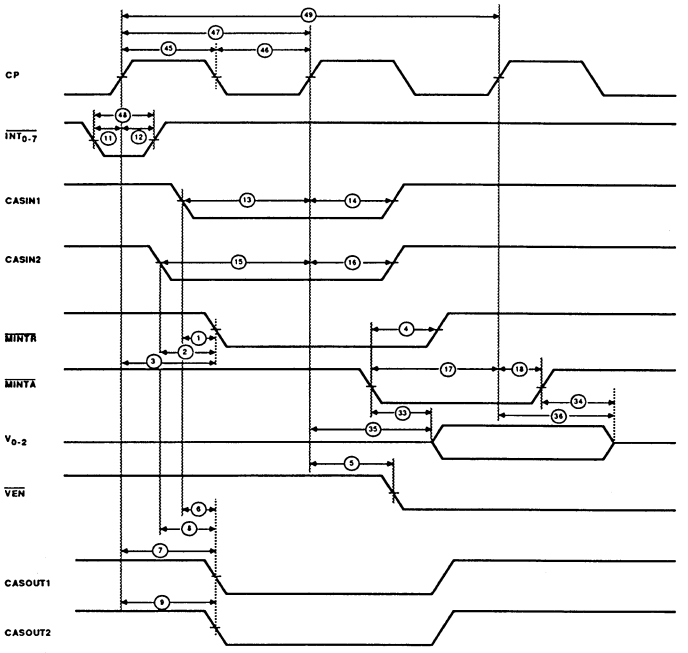
WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
⟍⟍⟍	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
⟋⟋⟋	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
⟋⟍⟋⟍	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
⟋⟍ ⟍⟋	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010



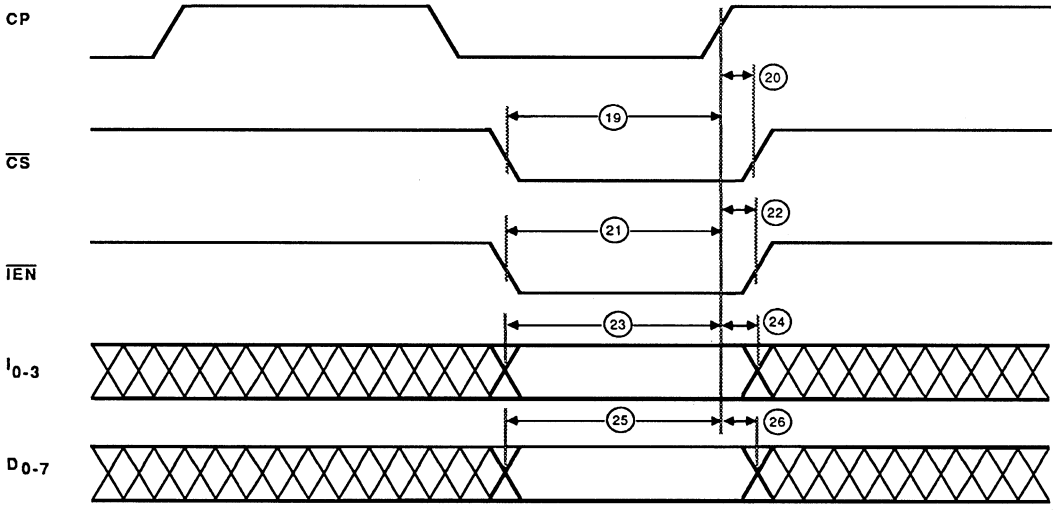
WFR02990

SWITCHING WAVEFORMS (Cont'd.)



WF025240

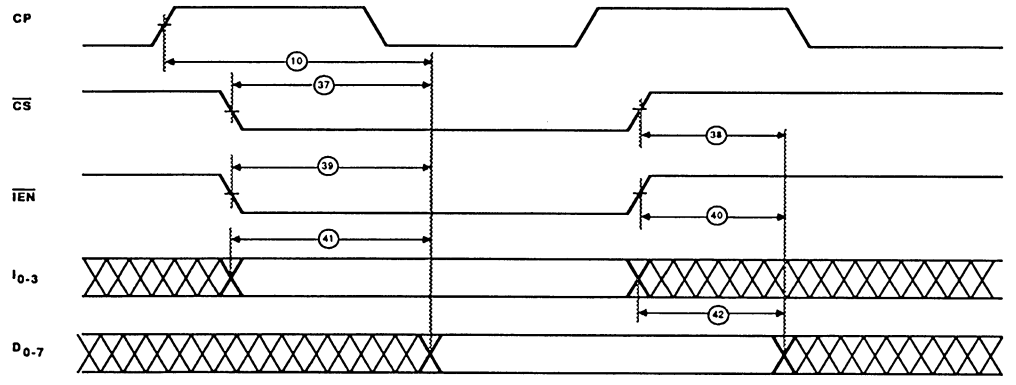
Interrupt Request Timing



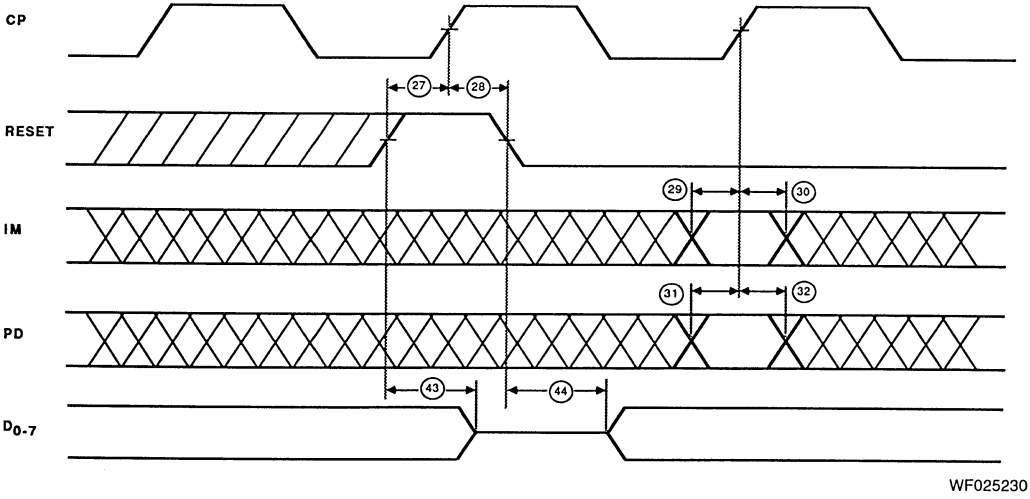
WF025211

Write Internal Register

SWITCHING WAVEFORMS (Cont'd.)



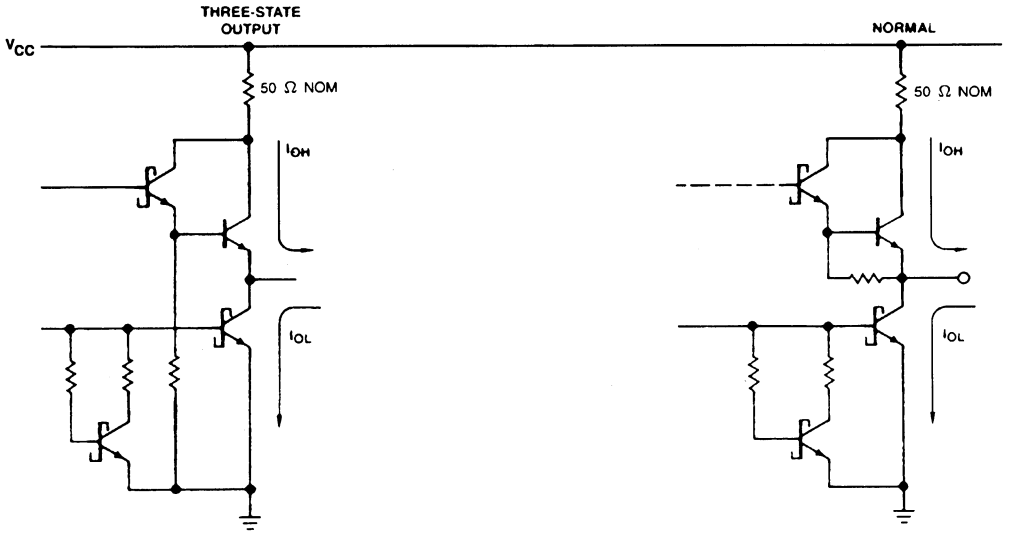
Read Internal Register



Reset Timing

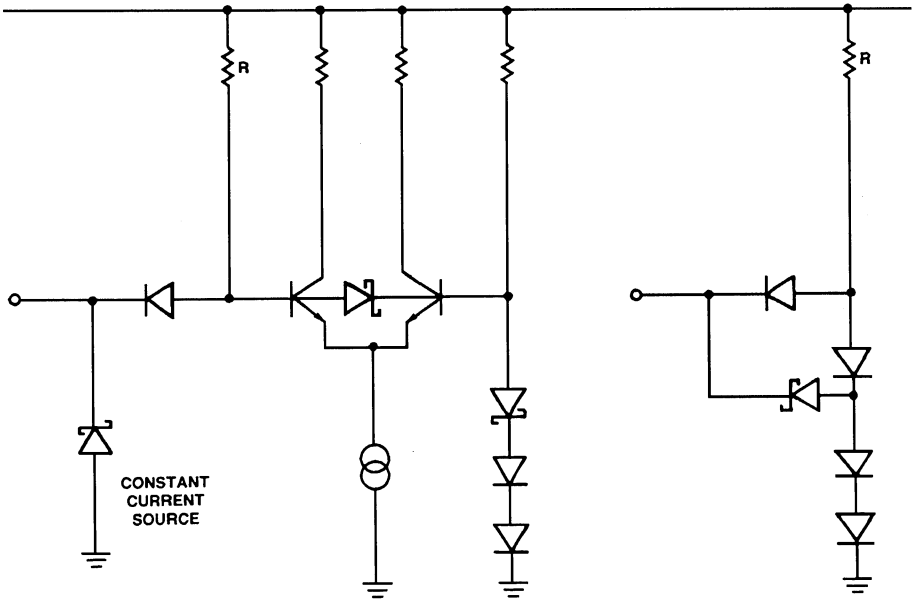
INPUT/OUTPUT CIRCUIT DIAGRAM

TTL



ICR00525

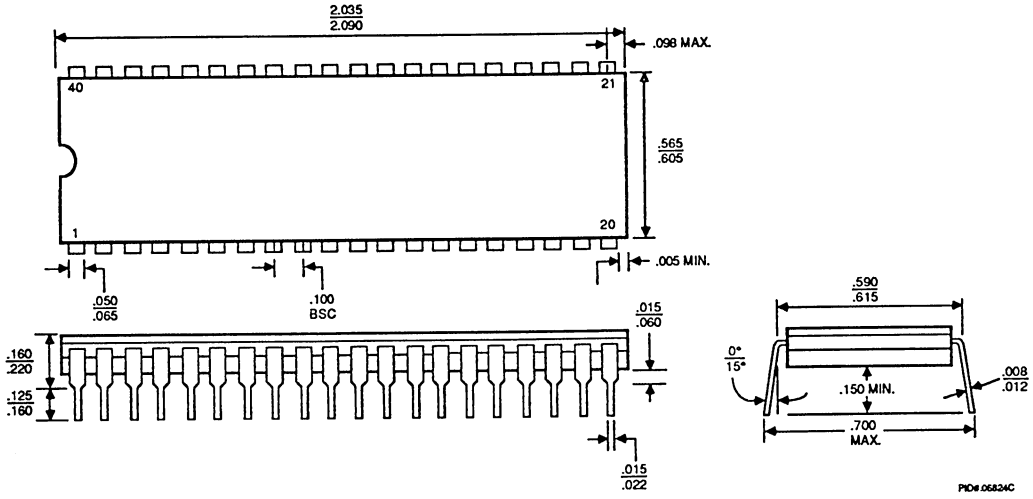
$C_O \cong 5.0$ pF, all outputs



ICR00534

PHYSICAL DIMENSIONS*

CD 040



*For reference only.

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