CL-GD62XX

Preliminary Data Book

FEATURES

- **IBM®–VGA hardware-compatible**
- **Integrated RAMDAC™**
- **Integrated programmable frequency synthesizer**
  - — 65 MHz at 5.0V; 40 MHz at 3.3V
- **Supports single 256K x 16 DRAM configuration**
  - — Symmetric or asymmetric RAS/CAS-address DRAM
- **Color STN panel support *(CL-GD6225/'6235 only)***
  - — Dual-scan color STN panel support (CL-GD6235 only)
  - — 8- and 16-bit interfaces (no extra components required)
  - — Up to 256 simultaneous colors from a palette of 256K
- **Integrates color TFT panel support**
  - — Supports 9-, 12-, 15-, and 18-bit TFT panels
  - — Up to 256 simultaneous colors from a palette of 256K
- **Connects directly to local bus, ISA bus (PC AT) or PI bus** *(CL-GD6205 connects to ISA bus only)*
- **Windows performance-improvement features**
  - — True packed-pixel addressing
  - — Improved data latches for block moves
  - — Color expansion for 8 bits-per-pixel graphics
  - — 32 x 32 hardware cursor (2 bits-per-pixel)
- **Supports 3.3V and 5.0V mixed-voltage operation**
- **Standby and Suspend modes save power**
  - — Internal timers for backlight control and Standby mode
  - — Dedicated Hardware-suspend Mode pin
  - — 32-kHz DRAM refresh clock in Suspend mode
- **Frame-Accelerator for low-active power**
  - — No additional DRAMs required
  - — Supports self-refresh DRAMs
- **Simultaneous CRT and LCD (SimulSCAN™) operation**

(cont.)

Single DRAM LCD/VGA Controllers for Monochrome/ Color Notebook Computers

OVERVIEW

The CL-GD62XX (CL-GD6205/'6215/'6225/'6235) family of advanced single-chip flat panel VGA controllers are designed for use in portable systems with stringent power consumption and form-factor requirements. Product family pin compatibility provides easy upgrade capability to color or higher-performance systems.

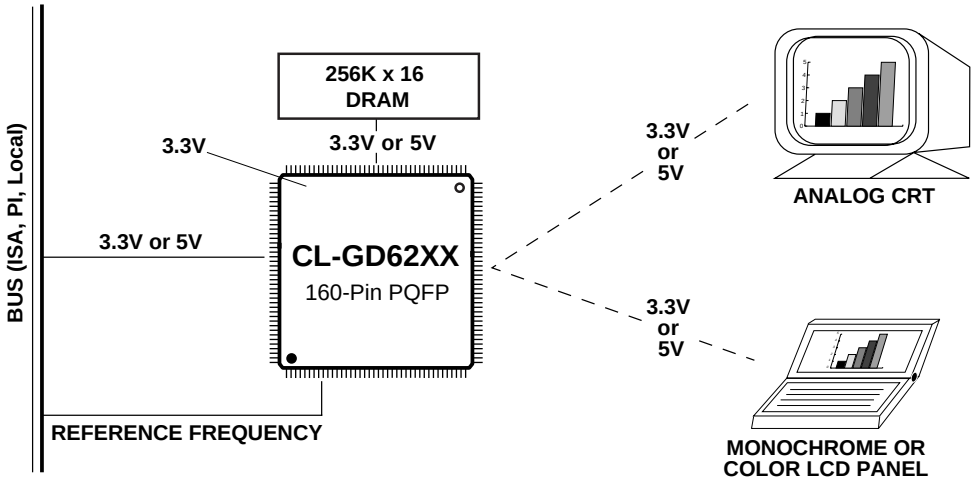
Integration of the frequency synthesizer, RAMDAC, monochrome and color STN/TFT panel interfaces minimizes the form-factor requirement for color and monochrome graphics subsystems. All necessary panel-power sequencing logic has been integrated into the CL-GD62XX family, and a complete graphics subsystem can be built using only two active components (in less than three square inches).

The CL-GD62XX family uses a single 256K x 16 DRAM (or four 256K x 4 DRAMs) for video memory. For added flexibility, dual-CAS*-DRAM and dual-WE*-DRAM configurations are supported.

With integrated Frame-Accelerator technology, the CL-GD62XX controllers feature low-power LCD operation, yet support high LCD panel vertical-refresh rates. No additional DRAMs are required for frame

(cont.)

Functional Block Diagram



October 1993

FEATURES (cont.)

- **64-shade grayscale at 640 x 480 resolution on monochrome STN LCD**
- **CRT Resolution up to 1024 x 768 with 16 colors**
- **CRT Resolution up to 800 x 600 with 256 colors**
- **132-column text modes on CRTs**
- **Automatic vertical expansion or centering option for LCD panels**
- **160-pin (EIAJ standard) PQFP package**

OVERVIEW (cont.)

acceleration because the CL-GD62XX family efficiently uses the unused portions of video memory.

Since the CL-GD62XX can use a 3.3V or 5.0V power supply, mixed-voltage operation is optimized for quick implementation of a notebook computer with reduced power consumption. The video memory, host bus interface, panel interface, and CRT interface each may be implemented with either 3.3V or 5.0V used in any combination.

The CL-GD62XX family also offers flexibility in host-interface connections. In addition to an ISA-bus connection, the CL-GD6215/'25/'35 can be connected directly to a PI- or local-bus to provide additional graphics performance. The 16-bit local-bus interface can be used directly with '386SX microprocessors. Connections to 32-bit buses, such as '386DX or '486 microprocessors, can be made by using the 16-bit modes or with a minimum of extra components. The CL-GD62XX controllers also use the '486 Burst mode for multiple-cycle accesses.

The CL-GD62XX family offers true packed-pixel addressing, color expansion for 8-bit-per-pixel graphics, and hardware cursor, thus improving Windows performance. Other incorporated features, such as memory write buffers and internal asynchronous display data FIFOs, also boost performance.

Standby and Suspend power-management modes reduce power consumption when the system is not in active use. The internal Standby Counter initiates Standby mode without software intervention. During this reduced-power mode, the LCD panel is turned off while the video memory can be accessed and modified. In Suspend mode, all I/O pins, except a dedicated Suspend Mode pin, are deactivated to further reduce power consumption. In this mode, the video memory data is preserved, but cannot be accessed; this is useful in situations when a system remains inactive for a relatively long period of time.

The CL-GD62XX family also features SimulSCAN™, a technique introduced by Cirrus Logic for achieving simultaneous CRT and LCD operation. SimulSCAN allows portable computers to become a key part of presentation environments for sales-force automation, field service, and educational organizations. SimulSCAN is supported in both single- and dual-scan, color and monochrome, LCD panels, and fixed- and multi-frequency analog CRTs.

Proprietary algorithms in the CL-GD62XX family expand the available palette depth for color flat panels. High clock rates provide extended-resolution capability in CRT mode. At 1024 x 768 resolution, 16 simultaneous colors can be displayed; at 640 x 480 resolution, up to 256 simultaneous colors are available.

The CL-GD62XX family offers highly integrated, pin-compatible LCD VGA controllers that provide unmatched performance while featuring design flexibility in CPU, video-memory interface, and power management. The CL-GD62XX family can also drive a wide variety of color and monochrome LCD flat-panel displays.

Controller Selection Guide

CL-GD62XX Device	Buses Supported			Panels Supported			
	ISA	PI	Local	Mono. STN	Color TFT	Color STN	Dual-Scan Color STN
CL-GD6205	✔			✔	✔		
CL-GD6215	✔	✔	✔	✔	✔		
CL-GD6225	✔	✔	✔	✔	✔	✔	
CL-GD6235	✔	✔	✔	✔	✔	✔	✔

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List of Tables

Revision History

Major changes between the previous version, dated September 1992, and this version are listed below.

General

The major addition to this data book is information specific to the CL-GD6235 device.These additions are labeled as CL-GD6235 only', if they do not apply to other devices in the family. Also, the LCD Timing (Shadow) registers (Rxx), that were listed with the CR1D[7] register description, have been broken out into individual register descriptions at the end of Section 6.0.

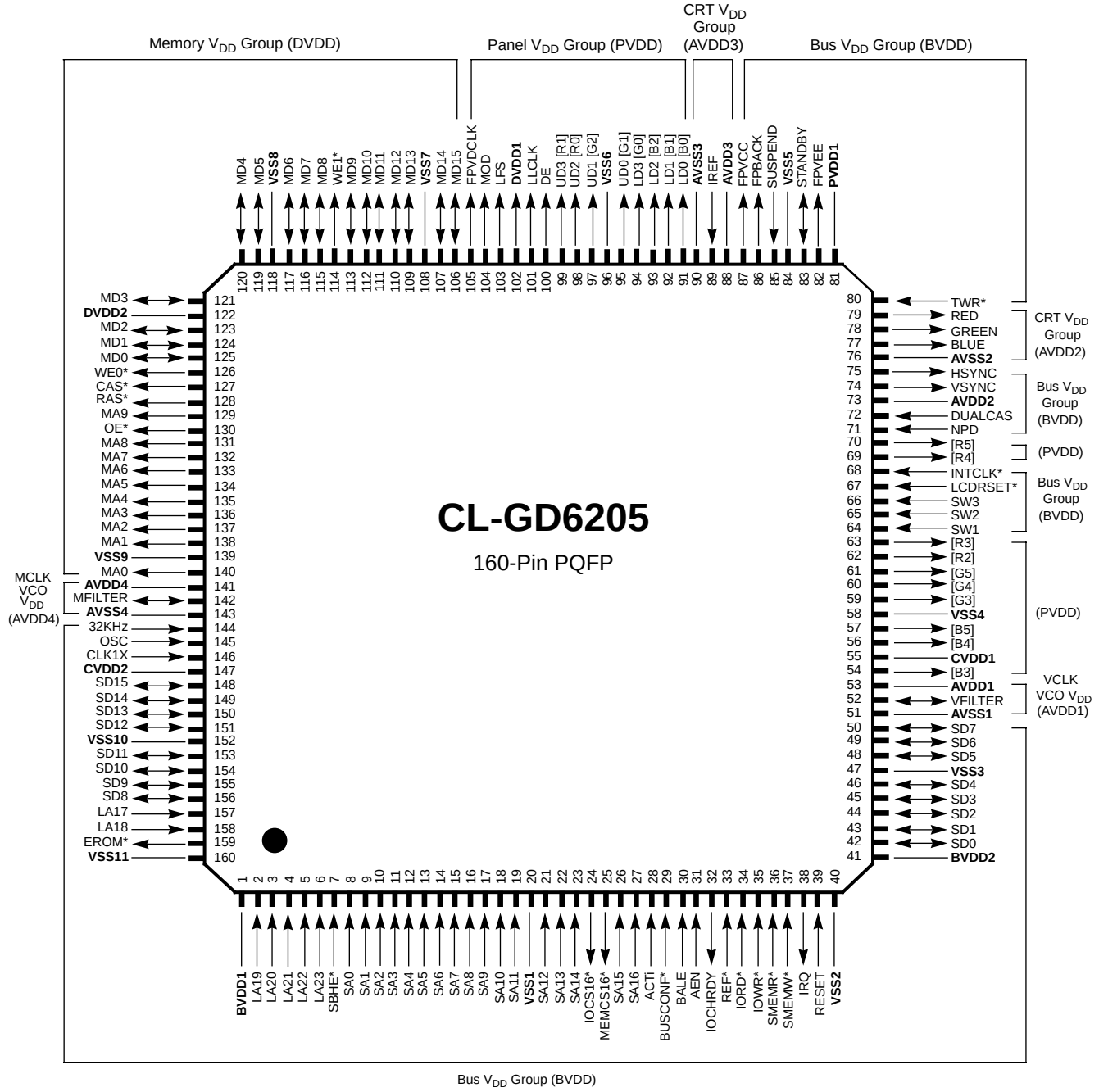
Specific

Section	Revision
1.0	The CL-GD6235 is added to the CL-GD6225 pin diagram. One of the filter capacitors in the AVDD filter circuit has been changed from '.1't9'1.0' CLF. The Pin Summary Tables for the Host Interfaces has been consolidated into one table. The Output Loading Parameters have been moved from the Pin Summary tables to the Electrical Test section.
2.0	The detailed pin descriptions have been modified for consistency and to add the pin numbers to the individual pins. Information has been added to many of the descriptions.
2.4	The recommended filter circuit components have been changed.
2.5	The IREF circuit for 3.3V operation has been added.
3.0	The functional description has been modified to add CL-GD6235-specific information.
3.8	Standby and Suspend mode descriptions have been modified for clarity. Also, the power sequencing parameters have been changed.
4.3	The Host Interface Signals table has been included in Section 1.9, *Pin Summary*.
6.0	The register information has been expanded to include CL-GD6235–specific register data. Register descriptions have been added for: CR29 — Configuration register ROX through REX — LCD Timing registers (these3hadow' registers were described under the CR1D[7] register description).
7.2	DC Specifications — the CMOS input-threshold and output-limit specifications have been corrected. An Output Loading table has been added.
7.6	AC Specifications — many of the tables and waveforms have consolidated to reflect operating relationships, and some new parameters have been added to the Memory Read and Write tables. Most of the limits are equal to or tighter than the original data. The STN and TFT panel interface timing specifications have been modified to reflect more current LCD-industry limits.
8.0	Package dimensions have been modified slightly to reflect the latest plastic package.

1. PIN INFORMATION

The CL-GD62XX family of VGA controllers is available in a 160-pin plastic quad flat pack device configuration, shown below.

1.1 Pin Diagram for the CL-GD6205

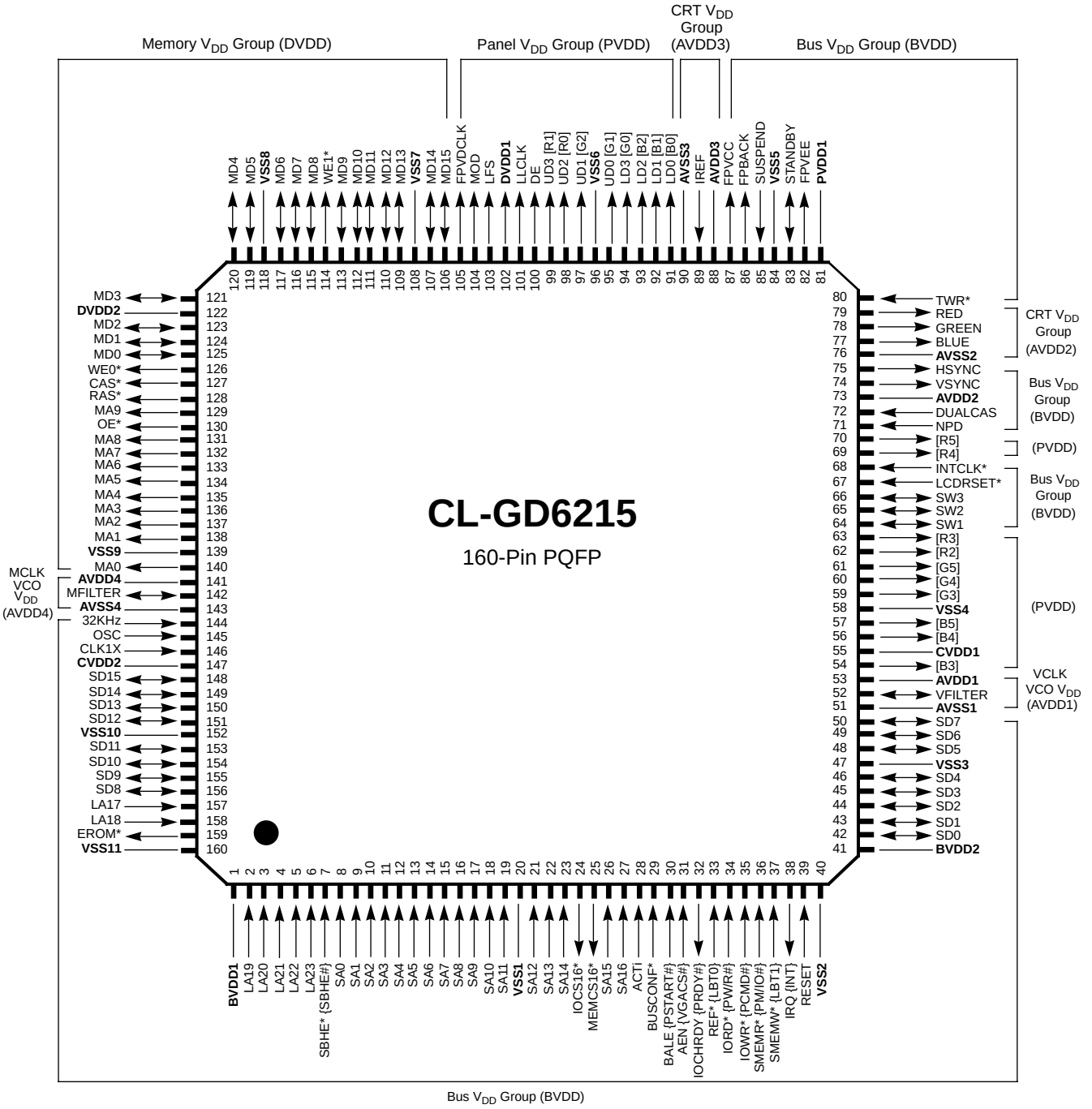


NOTES:

1) All pins in '[ ]' are color TFT data interface pins.

2) Power pin signal names are in bold type.

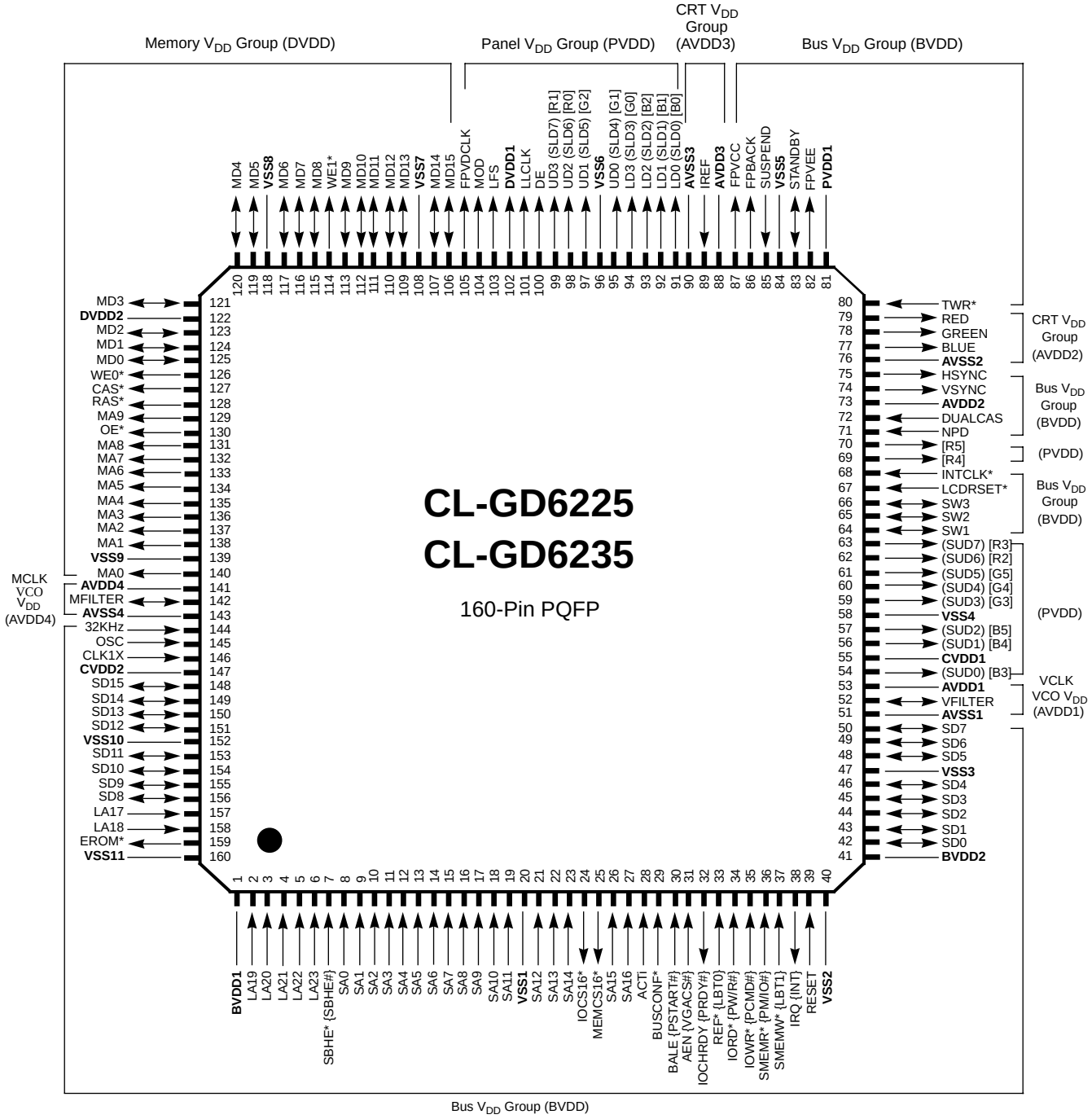
1.2 Pin Diagram for the CL-GD6215



NOTES:

1) All pins in '[ ]' are color TFT data interface pins.
2) All pins in '{ }' are PI bus interface pins.
3) Power pin signal names are in bold type.

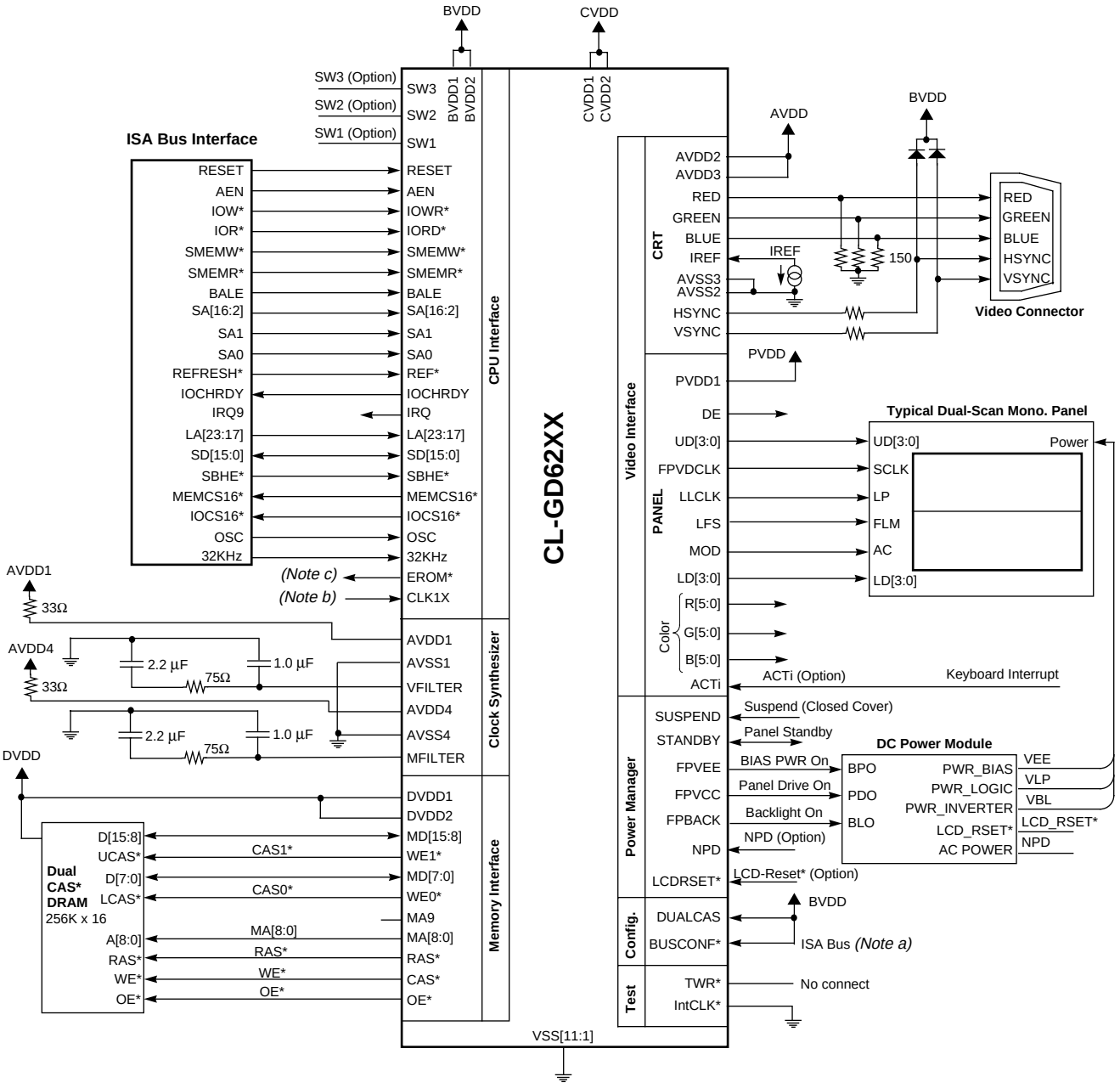
1.3 Pin Diagram for the CL-GD6225 and CL-GD6235.



NOTES:

1) All pins in '( )' are color STN data interface pins.
2) All pins in '[ ]' are color TFT data interface pins.
3) All pins in '{ }' are PI bus interface pins.
4) Power pin signal names are in bold type.

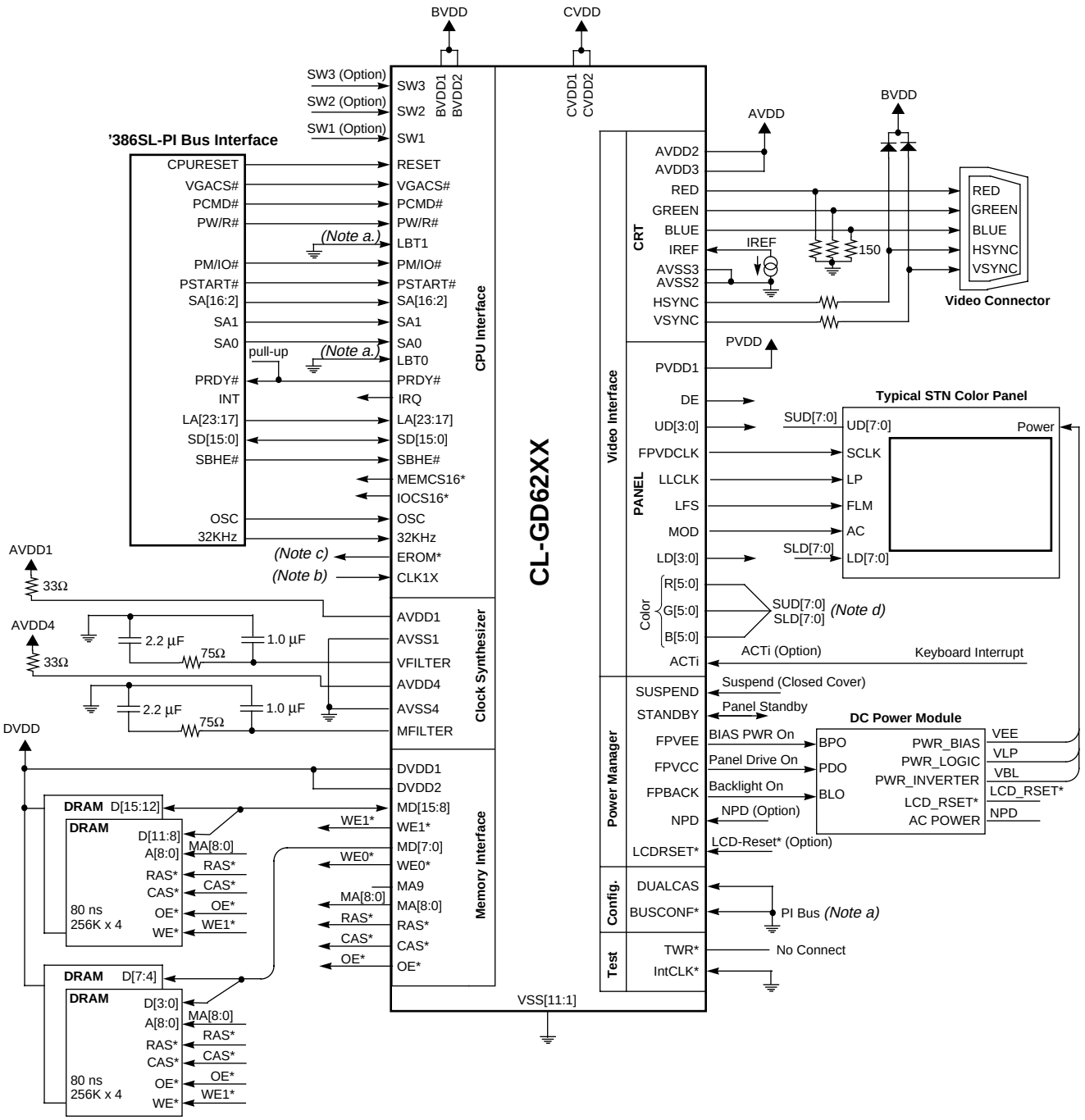
1.4 Typical Dual Monochrome Panel Connections — ISA Bus Using 256K x 16 DRAM with Dual CAS*



NOTES:

a. Refer to Table 2-1 for bus configuration.
b. Ground these input signals when not used.
c. EROM controls the Chip Enable of the 'optional' BIOS EPROMs.

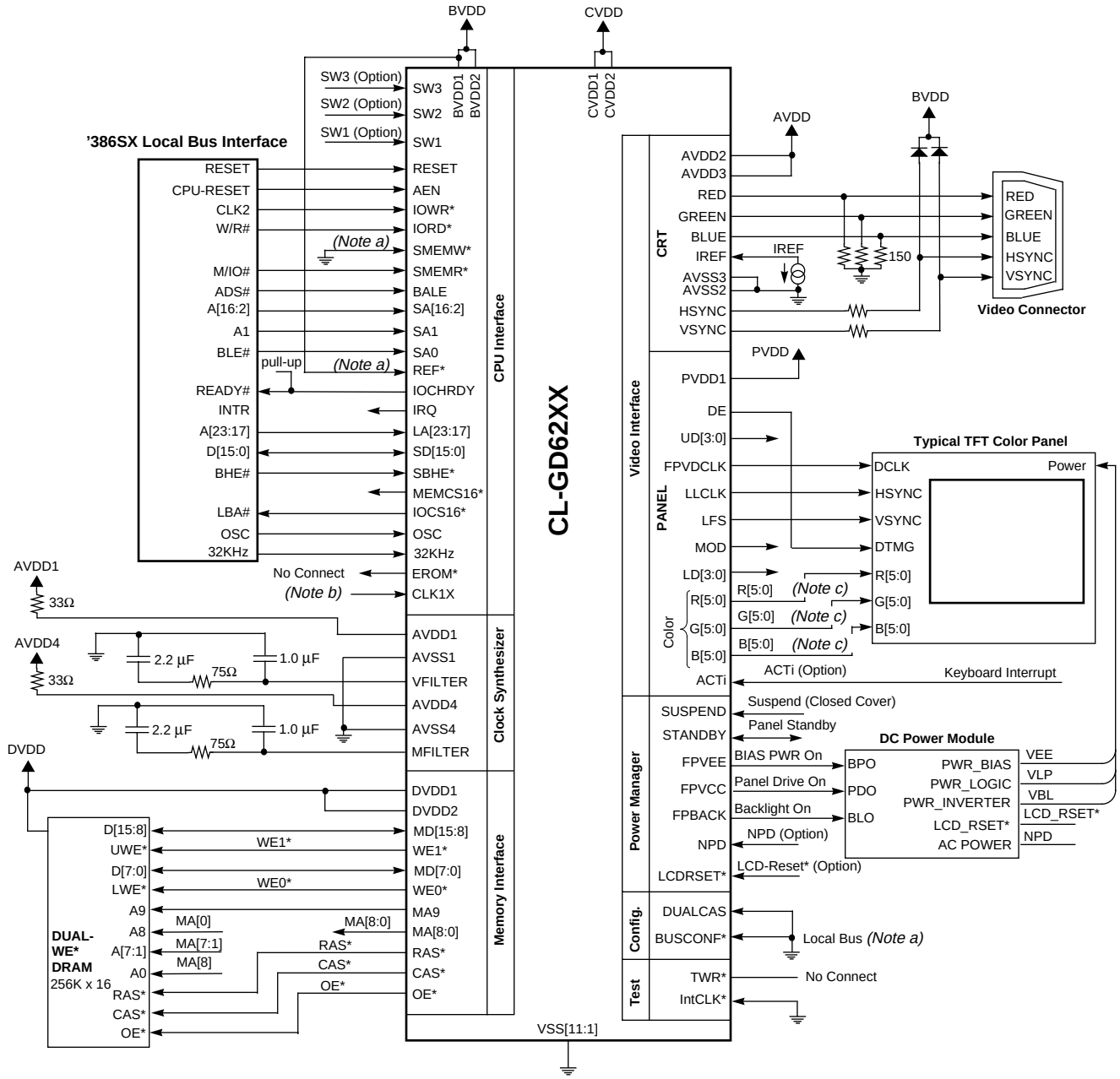
1.5 STN Color Panel Connections — ’386SL/’486SL PI Bus Using 256K x 4 DRAMs



NOTES:

a. Refer to Table 2-1 for bus configuration.
b. Ground these input signals when not used.
c. EROM controls the Chip Enable of the ‘optional’ BIOS EPROMs.
d. See Panel Interface Connection Tables for specific pin connections.

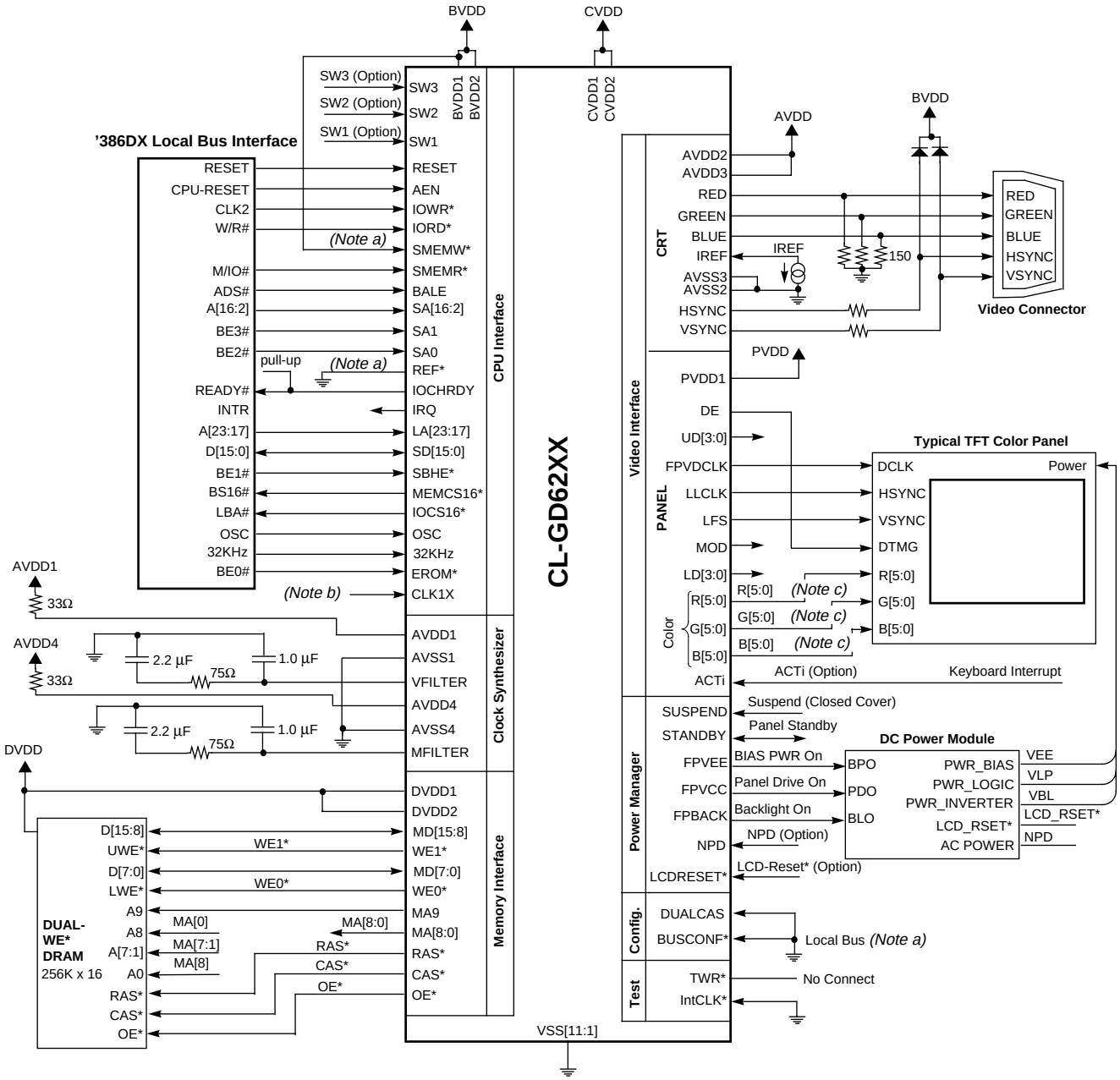
1.6 TFT Color Panel Connections — ’386SX Local Bus Using 256K x 16 DRAM with Dual WE*



NOTES:

a. Refer to Table 2-1 for bus configuration.
b. Ground these input signals when not used.
c. See Panel Interface Connection Tables for specific pin connections.

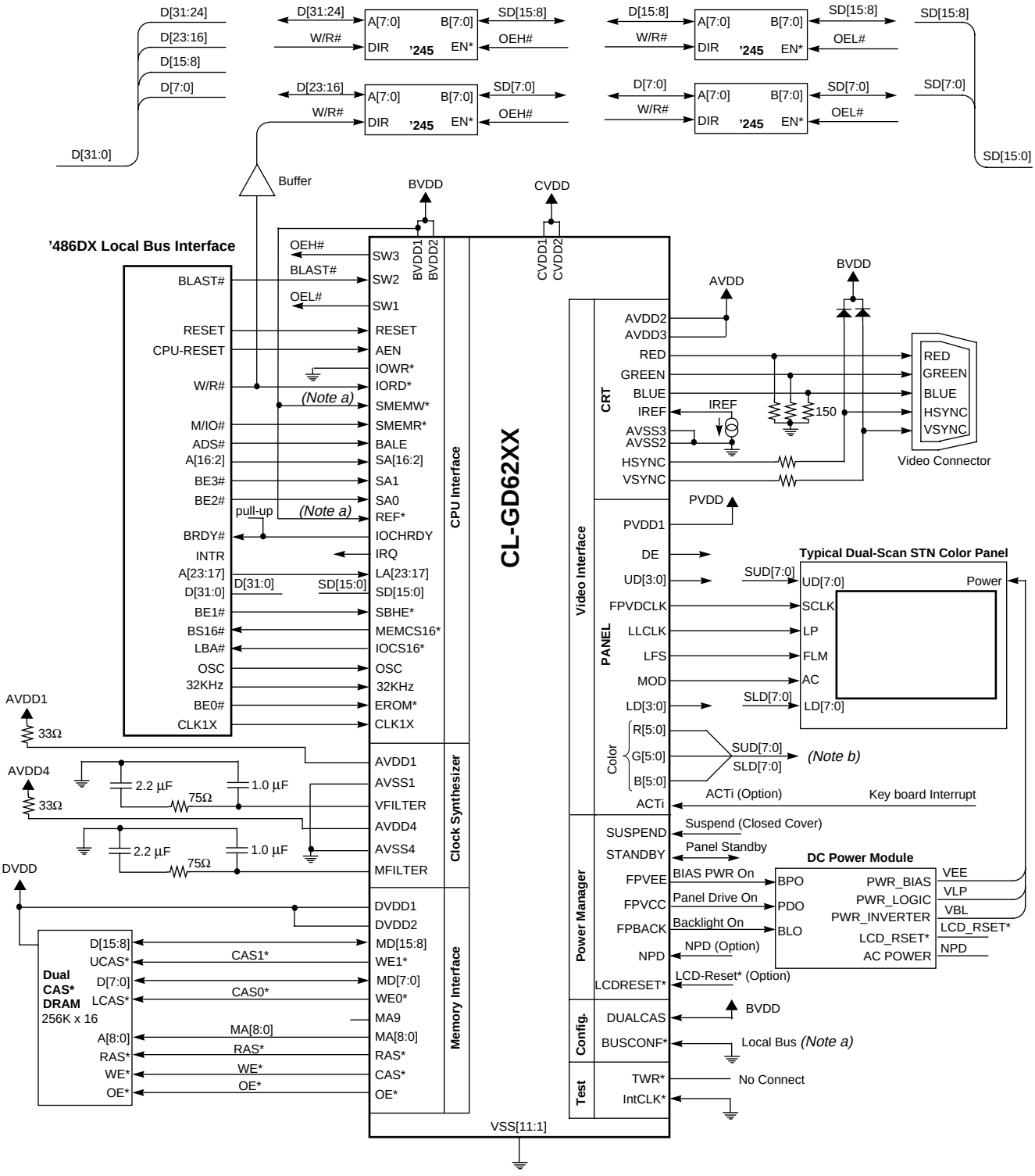
1.7 TFT Color Panel Connections — ’386DX Local Bus Using 256K x 16 DRAMs with Dual WE*



NOTES:

a. Refer to Table 2-1 for bus configuration.
b. Ground these input signals when not used.
c. See Panel Interface Connection Tables for specific pin connections.

1.8 Dual-Scan STN Color Panel — ’486DX Local Bus/256K x 16 DRAM with Dual CAS*



NOTES:

a. Refer to Table 2-1 for bus configuration.
b. See Panel Interface Connection Tables for specific pin connections.

1.9 Pin Summary *(See Section 2 for definition of abbreviations used in these tables)*

Table 1–1. Host Interface

CL-GD62XX Pins			ISA Bus (6205/15/25/35)	'386SL (PI) Bus (6215/25/35)	'386SX Local Bus (6215/25/35)	'386DX Local Bus (6215/25/35)	'486 Local Bus (6215/25/35)
Pin Number	Pin Name	Pin Type					
6:2	LA[23:19]	In	LA[23:19]	LA[23:19]	A[23:19]	A[23:19]	A[23:19]
158:157	LA[18:17]	In	LA[18:17]	LA[18:17]	A[18:17]	A[18:17]	A[18:17]
27:26	SA[16:15]	In	SA[16:15]	SA[16:15]	A[16:15]	A[16:15]	A[16:15]
23:21	SA[14:12]	In	SA[14:12]	SA[14:12]	A[14:12]	A[14:12]	A[14:12]
19:10	SA[11:2]	In	SA[11:2]	SA[11:2]	A[11:2]	A[11:2]	A[11:2]
9	SA[1]	In	SA[1]	SA[1]	A[1]	BE3#	BE3#
8	SA[0]	In	SA[0]	SA[0]	BLE#	BE2#	BE2#
148:151	SD[15:12]	I/O	SD[15:12]	SD[15:12]	D[15:12]	D[15:12]	D[15:12]
153:156	SD[11:8]	I/O	SD[11:8]	SD[11:8]	D[11:8]	D[11:8]	D[11:8]
50:48	SD[7:5]	I/O	SD[7:5]	SD[7:5]	D[7:5]	D[7:5]	D[7:5]
46:42	SD[4:0]	I/O	SD[4:0]	SD[4:0]	D[4:0]	D[4:0]	D[4:0]
7	SBHE*	In	SBHE*	SBHE#	BHE#	BE1#	BE1#
24	IOCS16*	OC	IOCS16*	*No connect*	LBA#	LBA#	LBA#
25	MEMCS16*	OC	MEMCS16*	*No connect*	*No connect*	BS16#	BS16#
29	BUSCONF*	In	'high'	'low'	'low'	'low'	'low'
30	BALE	In	BALE	PSTART#	ADS#	ADS#	ADS#
31	AEN	In	AEN	VGACS#	CPU-RESET	CPU-RESET	CPU-RESET
32	IOCHRDY	3-S	IOCHRDY	PRDY#	READY#	READY#	BRDY#
33	REF*	In	REFRESH*	LBT0	Tie to BVDD1	Tie to Ground	Tie to BVDD1
34	IORD*	In	IORD*	PW/R#	W/R#	W/R#	W/R#
35	IOWR*	In	IOWR*	PCMD#	CLK2	CLK2	Tie to Ground
36	SMEMR*	In	SMEMR*	PM/IO#	M/IO#	M/IO#	M/IO#
37	SMEMW*	In	SMEMW*	LBT1	Tie to Ground	Tie to BVDD1	Tie to BVDD1
38	IRQ	Out	IRQ9	INT	*No connect*	*No connect*	*No connect*
39	RESET	In	RESET	RESET	RESET	RESET	RESET
64	SW1	I/O	*No connect*	*No connect*	SW1	SW1	OEL#
65	SW2	In	*No connect*	*No connect*	SW2	SW2	BLAST#
66	SW3	I/O	*No connect*	*No connect*	SW3	SW3	OEH#
68	INTCLK	In	Tie to Ground	Tie to Ground	Tie to Ground	Tie to Ground	Tie to Ground
72	DUALCAS	In	Sets Dual-CAS or Dual-WE Memory Interface — See Table 1–4				
80	TWR*	In	No connect	No connect	No connect	No connect	No connect
144	32KHz	In	32KHz	32KHz	32KHz	32KHz	32KHz
145	OSC	In	OSC	OSC	OSC	OSC	OSC
146	CLK1X	In	No connect	No connect	No connect	No connect	CLK1X
159	EROM*	I/O	(Note [a])	(Note a)	Tie to Ground	BE0#	BE0#

[a] If an EPROM is used to load the BIOS, the EROM* pin is an active-'low' output used to control the EPROM Chip Enable.

Table 1–2. CRT Interface

CL-GD62XX Pins			Description
Pin Number	**Pin Name**	**Pin Type**	
74	VSYNC	Three-State Out	Vertical synchronization pulse for monitor
75	HSYNC	Three-State Out	Horizontal synchronization pulse for monitor
79	RED	Analog Out	Analog current representing Red value of pixel
78	GREEN	Analog Out	Analog current representing Green value of pixel
77	BLUE	Analog Out	Analog current representing Blue value of pixel
89	IREF	Analog In	DAC current reference — sets full scale DAC output

Table 1–3. LCD Flat Panel Interface

CL-GD62XX Pins			Monochrome Panel Pins	STN[a,b] Color Panel Pins	TFT[b] Color Panel Pins
Pin Number	**Pin Name**	**Pin Type**			
105	FPVDCLK	Out	FPVDCLK	FPVDCLK	FPVDCLK
104	MOD	Out	MOD	MOD	MOD
103	LFS	Three-State	LFS	LFS	LFS
101	LLCLK	Three-State	LLCLK	LLCLK	LLCLK
100	DE	Out	DE	N/C	DE
99	UD3	Out	UD3	SLD7	R1
98	UD2	Out	UD2	SLD6	R0
97	UD1	Out	UD1	SLD5	G2
95	UD0	Out	UD0	SLD4	G1
94	LD3	Out	LD3	SLD3	G0
93	LD2	Out	LD2	SLD2	B2
92	LD1	Out	LD1	SLD1	B1
91	LD0	Out	LD0	SLD0	B0
63	SUD7	Out	N/C	SUD7	R3
62	SUD6	Out	N/C	SUD6	R2
61	SUD5	Out	N/C	SUD5	G5
60	SUD4	Out	N/C	SUD4	G4
59	SUD3	Out	N/C	SUD3	G3
57	SUD2	Out	N/C	SUD2	B5
56	SUD1	Out	N/C	SUD1	B4
54	SUD0	Out	N/C	SUD0	B3
70	R5	Out	N/C	N/C	R5
69	R4	Out	N/C	N/C	R4

a. All ‘(SLD[7:0])’ and ‘(SUD[7:0])’ Signals are present only in the CL-GD6225 and CL-GD6235.

b. For exact pin connections, check the Panel Interface Connection Tables located in the *Panel Interface Guide* section of the *CL-GD62XX Family Applications Book*.

Table 1–4. Display Memory Interface

CL-GD62XX Pins			Dual-WE DRAM (DUALCAS = 'low')	Dual-CAS DRAM (DUALCAS = 'high')
Pin Number	Pin Name	Pin Type		
129	MA9	Out	MA9[a]	MA9[a]
131	MA8	Out	MA8	MA8
132	MA7	Out	MA7	MA7
133	MA6	Out	MA6	MA6
134	MA5	Out	MA5	MA5
135	MA4	Out	MA4	MA4
136	MA3	Out	MA3	MA3
137	MA2	Out	MA2	MA2
138	MA1	Out	MA1	MA1
140	MA0	Out	MA0[a]	MA0[a]
106	MD15	I/O	MD15	MD15
107	MD14	I/O	MD14	MD14
109	MD13	I/O	MD13	MD13
110	MD12	I/O	MD12	MD12
111	MD11	I/O	MD11	MD11
112	MD10	I/O	MD10	MD10
113	MD9	I/O	MD9	MD9
115	MD8	I/O	MD8	MD8
116	MD7	I/O	MD7	MD7
117	MD6	I/O	MD6	MD6
119	MD5	I/O	MD5	MD5
120	MD4	I/O	MD4	MD4
121	MD3	I/O	MD3	MD3
123	MD2	I/O	MD2	MD2
124	MD1	I/O	MD1	MD1
125	MD0	I/O	MD0	MD0
114	WE1*	Out	WE1*	CAS1*
126	WE0*	Out	WE0*	CAS0*
127	CAS*	Out	CAS*	WE*
128	RAS*	Out	RAS*	RAS*
130	OE*	Out	OE*	OE*

a. MA9 and MA0 are not used to drive column addresses on asymmetrical DRAMs. For a detailed explanation, see Section 5.4 of Application Note AN-GD30, *A Single DRAM LCD Motherboard Solution for Monochrome/Color Notebook Computers.*

Table 1–5. Power Management Pins

CL-GD62XX Pins			Description
Pin Number	Pin Name	Pin Type	
87	FPVCC	Out	Panel power-on enable
86	FPBACK	Out	Backlight power-on enable
82	FPVEE	Out	BIAS power-on enable
83	STANDBY	I/O	Standby mode control/standby status
85	SUSPEND	In	Suspend mode control (close-cover power sequence)
71	NPD	In	No power-down (disable power-down timers)
28	ACTi	In	Activity indicator (reset power-down timers)
67	LCDRSET*	In	LCD reset (initiates power-down sequence)

Table 1–6. Synchronizer/Clock Interface

CL-GD62XX Pins			Description
Pin Number	Pin Name	Pin Type	
145	OSC	In	Oscillator input for dual-frequency synthesizer
144	32KHz	In	Optional 32-KHz clock input for video RAM refresh during Suspend mode
142	MFILTER	Analog out	Memory clock filter connection
52	VFILTER	Analog out	Video clock filter connection

Table 1–7. Miscellaneous Pins

CL-GD62XX Pins			Description
Pin Number	Pin Name	Pin Type	
29	BUSCONF*	In	Bus configuration select (use with REF* and SMEMW*)
64	SW1	I/O	Programmable input (OEL# for ’486 local bus)
65	SW2	In	Programmable input (BLAST# for ’486 local bus)
66	SW3	I/O	Programmable input (OEH# for ’486 local bus)
68	INTCLK*	In	Internal clock enable
72	DUALCAS	In	Dual-CAS or Dual-WE DRAM select
80	TWR*	In	Test Write Enable (used for testing only)

Table 1–8. Power and Ground

CL-GD62XX Pins		Connect to Rail	Bypass Capacitor	Video Controller Section Serviced by Power Pins
Pin Number	PIN Name			
53	AVDD1	VDD(VCC) thru 33 ohms	10 µF to AVSS1	Analog voltage for video clock synthesizer
73	AVDD2	VDD(VCC)	0.1 µF	Analog voltage for palette DAC
88	AVDD3	VDD(VCC)	0.1 µF	
141	AVDD4	VDD(VCC) thru 33 ohms	10 µF to AVSS4	Analog voltage for memory clock synthesizer
1	BVDD1	VDD(VCC)	0.1 µF	Digital voltage for bus interface section
41	BVDD2	VDD(VCC)	0.1 µF	
55	CVDD1	VDD(VCC)	0.1 µF	Digital voltage for core logic of controller
147	CVDD2	VDD(VCC)	0.1 µF	
102	DVDD1	VDD(VCC)	0.1 µF	Digital voltage for memory interface section
122	DVDD2	VDD(VCC)	0.1 µF	
81	PVDD1	VDD(VCC)	0.1 µF	Digital voltage for LCD panel interface section
51	AVSS1	Analog ground		The analog ground plane should be isolated from the VSS (Digital) ground plane to prevent noise and crosstalk.
76	AVSS2	Analog ground		
90	AVSS3	Analog ground		
143	AVSS4	Analog ground		
20	VSS1	Digital ground		
40	VSS2	Digital ground		
47	VSS3	Digital ground		
58	VSS4	Digital ground		
84	VSS5	Digital ground		
96	VSS6	Digital ground		
108	VSS7	Digital ground		
118	VSS8	Digital ground		
139	VSS9	Digital ground		
152	VSS10	Digital ground		
160	VSS11	Digital ground		

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2. DETAILED PIN DESCRIPTIONS

These abbreviations are used for pin types in the following sections:

- (I) indicates Input
- (O) indicates Output
- (I/O) indicates either an Input or Output function, depending on the mode.
- (OC) indicates Open-Collector output
- (3-S) indicates three-state output
- (*) and (#) indicate active-'low' function
- Programmable levels '1' and '0' are equivalent to logic levels 'high' and 'low', respectively.

2.1 Host Interface — ISA Bus Mode

Pin Name	Pin No.	Type	Description
AEN	31	I	**ADDRESS ENABLE:** When this input is 'high', it indicates that the current cycle is a DMA cycle. In this case, the CL-GD62XX will not respond to I/O cycles. There is no effect on the memory interface which still performs refresh cycles.
BALE	30	I	**BUS ADDRESS LATCH ENABLE:** Data on the LA[23:17] pins is loaded into the internal address latch while BALE is 'high'. The data on the LA[23:17] pins during the logic 'high'-to-'low' transition of BALE is stored in the address latch.
BUSCONF*	29	I	**BUS CONFIGURATION*:** This active-'low' pin is used with REF*(LBT0) and SMEMW*(LBT1) pins to choose the CL-GD62XX host-bus type. Table 2-1 below shows the available host-bus configurations.

Table 2–1. Host-Bus Configuration

Bus Type	BUSCONF*	REF* (LBT0)	SMEMW* (LBT1)
ISA bus	'high'[a]	Tie to ISA bus REFRESH*	Tie to ISA bus SMEMW*
'386SL (PI bus)	'low'	'low'	'low'
'386SX	'low'	'high'	'low'
'386DX	'low'	'low'	'high'
'486SX/DX	'low'	'high'	'high'

[a] For the CL-GD6205, tie BUSCONF* to BVDD.

2.1 Host Interface — ISA Bus Mode *(cont.)*

Pin Name	Pin No.	Type	Description
IOCHRDY	32	3-S	**I/O CHANNEL READY:** This output is 'high' during I/O and BIOS read cycles. During a **display memory read cycle**, this output is always driven 'low' as soon as SMEMR* goes 'low'. When the data bits are ready to be placed on the System Data bus, this output goes 'high'. It remains 'high' until SMEMR* goes 'high'; it then goes high impedance. During a **display memory write cycle**, if there is space in the Write Buffer, this output is driven 'high' when SMEMW* goes 'low'. If the Write Buffer is full when SMEMW* goes 'low', IOCHRDY is driven 'low' and remains 'low' until there is space in the buffer. This output, when 'low', indicates that additional wait states must be inserted into the current display memory read or write cycle. Once there is space in the Write Buffer, IOCHRDY goes 'high', and remains 'high', until SMEMW* goes 'high'; it then goes high impedance.
IOCS16*	24	OC	**I/O CHIP SELECT 16*:** This open-collector output is driven 'low' to indicate the CL-GD62XX can execute a 16-bit I/O operation at the address currently on the bus. This output is generated from a decode of A[15:0] and AEN. Table 2–2 gives the range of addresses for which IOCS16* will go 'low'. In an 8-bit environment, this pin is not connected.
IORD*	34	I	**I/O READ*:** This active-'low' input is forced 'low' by the host to request an I/O data transfer. When the address on SA[15:0] is within the range of the CL-GD62XX, the CL-GD62XX will respond by placing the contents of the appropriate register on the System Data bus.

Table 2–2. IOCS16* Addresses

Address	Function
3C4, 3C5	Sequencer
3CE, 3CF	Graphics controller
3B4/3D4, 3B5/3D5	CRT controller
3BA/3DA	Input Status register 1

2.1 Host Interface — ISA Bus Mode *(cont.)*

Pin Name	Pin No.	Type	Description
IOWR*	35	I	**I/O WRITE*:** This active-'low' input is forced 'low' by the host to initiate an I/O data write to the CL-GD62XX. When the address on SA[15:0] is within the range of the CL-GD62XX, the contents of the System Data bus is written into the addressed register during the logic 'low'-to-'high' transition of IOWR*. A list of I/O addresses that the CL-GD62XX responds to appears in Table 2–2. When a 16-bit I/O write is performed, the specified address is typically the Index register for one of the VGA groups. In this case, the index should appear on SD[7:0], and the data should appear on SD[15:8].
IRQ	38	3-S	**INTERRUPT REQUEST:** This output is typically unused in an ISA-bus design, but it may be connected to IRQ2(IRQ9) if necessary. Register CR11 controls the interrupt function.
LA[23:17]	6:2 158:157	I	**LA ADDRESS [23:17]:** These address inputs extend the system address to 24 bits. They are used, along with SA[16:0], to select the resource to be accessed during memory and I/O operations. Data on the LA[23:17] pins is loaded into the internal address latch while BALE is 'high', and is stored in the latch during the logic 'high'-to-'low' transition of BALE.
MEMCS16*	25	OC	**MEMORY CHIP SELECT 16*:** This open-collector output is driven 'low' to indicate that the CL-GD62XX can execute a 16-bit memory operation at the address currently on the bus. Table 2–1 summarizes the conditions under which MEMCS16* goes 'low'. In an 8-bit environment, this pin is not connected.
REF*	33	I	**REFRESH*:** This active-'low' input is driven 'low' by the host to initiate a DRAM refresh cycle. System memory read operations, occurring when REFRESH* is 'low', are ignored.
RESET	39	I	**RESET:** This input is used to initialize the CL-GD62XX. When 'high', it forces all outputs to a high-impedance state, and initializes all registers to their reset state. When RESET goes 'low' normal operation is enabled.

Table 2–3. MEMSC16* Addresses

Resource	Address Bits	Address Range	Qualifier
Display Memory	A[23:17]	A000:0-BFFF:F	SR8[6] = 'high' (No other VGA card)

2.1 Host Interface — ISA Bus Mode *(cont.)*

Pin Name	Pin No.	Type	Description
SA[16:0]	27:26 23:21 19:8	I	**SYSTEM ADDRESS [16:0]:** These address inputs are used, along with LA[23:17], to select the resource to be accessed during memory and I/O operations. These address bits are not latched by the CL-GD62XX, and therefore, ***must*** remain stable *throughout* the cycle.
SBHE*	7	I	**SYSTEM BYTE HIGH ENABLE*:** This active-'low' input is used in conjunction with SA[0] to determine the width and alignment of a data transfer. SBHE* and SA[0] are decoded as shown in Table 2–4. In an 8-bit environment, tie SBHE* 'high'.
SD[7:0]	50:48 46:42	I/O	**SYSTEM DATA [7:0]:** These bi-directional pins are used to transfer data during memory or I/O operations. These pins may be connected directly to the corresponding ISA bus pins.
SD[15:8]	148:151 153:156	I/O	**SYSTEM DATA [15:8]:** These bi-directional pins are used to transfer data during 16-bit memory or I/O operations. These pins may be connected directly to the corresponding ISA bus pins. The SD[15:8] pins have internal pull-up resistors to guarantee a valid input level when not connected.
SMEMR*	36	I	**SYSTEM MEMORY READ*:** This active-'low' input is forced 'low' by the host to initiate a data transfer (read) from the CL-GD62XX to system memory. When a BIOS read is occurring, which is determined by decoding A[23:15], the EROM* output goes 'low' when SMEMR* is 'low'.
SMEMW*	37	I	**SYSTEM MEMORY WRITE*:** This active-'low' input is forced 'low' by the host to initiate a data transfer (write) from system memory to the CL-GD62XX. The data bits are stored in the write latch on the logic 'low'-to-'high' transition of this signal and transferred to display memory later.

Table 2–4. SBHE/SA[0] Decoding

SBHE*	SA[0]	Function
'low'	'low'	16-bit transfer
'low'	'high'	Upper-byte transfer
'high'	'low'	Lower-byte transfer

2.2 Host Interface — ’386SL/’486SL (PI Bus Mode) *(CL-GD6215/’25/’35 only)*

Pin Name	Pin No.	Type	Description
BUSCONF*	29	I	**BUS CONFIGURATION*:** This active-‘low’ pin is used with the REF*(LBT0) and SMEMW*(LBT1) pins to choose the CL-GD62XX host-bus type. The following table shows how to use this pin for the ’386SL/’486SL (PI) bus, which is only supported by the CL-GD6215/’25/’35.
IRQ	38	3-S	**INTERRUPT REQUEST:** This output is typically unused in a PI-bus design, but it may be connected to the INT input if necessary. Register CR11 controls the interrupt function.
LA[23:17]	6:2 158:157	I	**LOCAL ADDRESS [23:17]:** The PI bus shares these local address inputs with the ISA bus. These inputs provide a path between the ’386SL/’486SL CPU and the VGA subsystem.
PCMD#	35	I	**PI-BUS COMMAND#:** The host drives this input ‘low’ to indicate that a valid PI-bus cycle is in progress.
PM/IO#	36	I	**PI-BUS MEMORY–I/O SELECT#:** This input, along with PW/R#, indicates the type of access currently being executed. A ‘high’ on PM/IO# indicates a memory cycle, while a ‘low’ on PM/IO# indicates an I/O cycle. PM/IO# is sampled during the ‘low’-to-‘high’ transition of PSTART# for PI-bus transfers.
PRDY#	32	3-S	**PI-BUS READY#:** This active-‘low’ output terminates a bus cycle. The PI bus is normally not ready, and a bus cycle will continue until PRDY# goes ‘low’. To guarantee cycle termination, PRDY# ***must*** remain ‘low’ until the logic ‘low’-to-‘high’ transition of PCMD#.
PSTART#	30	I	**PI-BUS START#:** This active-‘low’ input indicates to the CL-GD62XX the start of the PI-bus cycle. Address and status inputs are latched during the logic ‘high’-to-’low’ transition.

Table 2–5. Bus Type Configuration

Bus Type	BUSCONF*	LBT0 (REF*)	LBT1 (SMEMW*)
PI bus	‘low’	‘low’	‘low’

2.2 Host Interface — ’386SL/’486SL (PI Bus Mode) *(CL-GD6215/’25/’35 only)* *(cont.)*

Pin Name	Pin No.	Type	Description
PW/R#	34	I	**PI BUS WRITE/READ#:** This input, along with PM/IO#, indicates the type of access currently being executed. A ‘high’ on PW/R# indicates a write access, while a ‘low’ on PW/R# indicates a read access. PW/R# is sampled during the logic ‘low’-to-‘high’ transition of PSTART# for PI-bus transfers.
RESET	39	I	**RESET:** This input is used to initialize the CL-GD62XX. When ‘high’, it forces all outputs to a high-impedance state and initializes all registers to their reset state. When RESET goes ‘low’, normal operation is enabled.
SA[16:0]	27:26 23:21 19:8	I	**SYSTEM ADDRESS [16:0]:** The PI bus shares these address inputs with the ISA bus. These inputs provide normal addressing on the PI bus, and are connected to ’386SL/’486SL CPU outputs during PI-bus cycles.
SBHE#	7	I	**SYSTEM BYTE HIGH ENABLE#:** This active-‘low’ input is used in conjunction with SA[0] to determine the width and alignment of a data transfer. SBHE* and SA[0] are decoded as shown in Table 2–6. This input is latched when PCMD# is ‘low’.
SD[15:0]	156:153 151:148 50:48, 46:42	I/O	**SYSTEM DATA [15:0]:** These bi-directional pins are used to transfer 16-bit data during a memory or I/O operation.
VGACS#	31	I	**VGA CHIP SELECT#:** This active-‘low’ input is driven ‘low’ by the host when an access occurs to a user-defined VGA-memory address space. VGACS# is driven ‘low’ whether memory space has been defined for the ISA bus or the PI bus. This input is driven ‘high’ during VGA I/O accesses.

Table 2–6. SBHE#/SA[0] Decoding

SBHE#	SA[0]	Function
‘low’	‘low’	16-bit transfer
‘low’	‘high’	Upper-byte transfer
‘high’	‘low’	Lower-byte transfer

2.3 Host Interface — Local Bus *(CL-GD6215/'25/'35 only)*

Several bus interface pins are redefined according to the local bus type that the CL-GD6215/'25/'35 is connected. Both the '386SX and '386DX/'486 local bus pin names and descriptions are shown. For the equivalent CL-GD62XX pin names, refer to Table 1–1.

Pin Name	Pin No.	Type	Local Bus Name/Description
A[1]	9	I	**ADDRESS [1]:** For the **'386SX** this active-'low' signal is connected directly to the corresponding '386SX byte enable output.
BE3#			**BYTE ENABLE 3#:** For the **'386DX** and the **'486** this active-'low' input is connected directly to the corresponding CPU byte enable output.
A[16:2]	27:26 23:21 19:10	I	**ADDRESS [16:2]:** These inputs are used to select the resource to be accessed during memory or I/O operations.
A[23:17]	6:2 158:157	I	**ADDRESS [23:17]:** These inputs are used to select the resource to be accessed during memory or I/O operations.
ADS#	30	I	**ADDRESS STROBE#:** This active-'low' input indicates that a new cycle has begun. It ***must*** be connected directly to the ADS# pin on the CPU.
BE0#	159	I	**BYTE ENABLE 0#:** For the **'386DX** and the **'486**, this active-'low' input is connected directly to the '386DX/'486 BE0# pin. For the **'386SX** this pin is unused and ***must*** be tied to ground.
BHE#	7	I	**BYTE HIGH ENABLE#:** For the **'386SX**, this active-'low' input is connected directly to the corresponding '386SX high-byte enable output.
BE1#			**BYTE ENABLE 1#:** For the **'386DX** and the **'486**, this active-'low' input is connected directly to the corresponding CPU byte enable output.
BLE#	8	I	**BYTE LOW ENABLE:** For the **'386SX**, this active-'low' signal is connected directly to the corresponding '386SX low-byte enable output.
BE2#			**BYTE ENABLE 2#:** For the **'386DX** and the **'486**, this active-'low' input is connected directly to the corresponding CPU byte enable output.

2.3 Host Interface — Local Bus *(CL-GD6215/'25/'35 only)* *(cont.)*

Pin Name	Pin No.	Type	Local Bus Name/Description
BS16#	25	OC	**BUS SIZE 16#:** This active-'low' output is used by the **'386DX/'486** local bus. It is driven by the CL-GD6215/'25/'35 to indicate that the current cycle addresses a 16-bit resource. The '386DX/'486 will convert the cycle to an appropriate number of 16-bit transfers. This output is not used in a **'386SX** system.
BUSCONF*	29	I	**BUS CONFIGURATION*:** This input is used with the REF*(LBT0) and SMEMW*(LBT1) pins to choose the CL-GD62XX host-bus type. Table 2–7 shows the available host-bus configurations.
CLK2	35	I	**CLOCK 2X:** When connected to the **'386SX** or **'386DX** local bus, this input is the timing reference for the device. In a **'486** system, this pin ***must*** be tied to ground (see CLK1X).
CLK1X	146	I	**CLOCK 1X:** This is the timing reference for the device when it is connected to a **'486** local bus. This pin ***must*** be connected directly to the CLK1X pin of the '486. If no CLK1X is available from the **'486**, the CLK2X can be divided by two and tied to the device CLK1X pin, but the clock skew must be less than 2 ns. In a **'386** system, this pin is unused and ***must*** be grounded.
CPU-RESET	31	I	**CPU-RESET:** A 'high' on this input is used to synchronize the CL-GD6215/'25/'35 to the CPU. In a **'386** system, this pin ***must*** be connected to the '386 CPU-RESET output to synchronize the CL-GD6215/'25/'35 to CLK2.
D[15:0]	156:153 151:148 50:48 46:42	I/O	**DATA [15:0]:** These bi-directional pins are used to transfer data during any memory or I/O operation. In a **'386SX** or **'386DX** local bus system, these pins are connected directly to D[15:0]. For the **'486** 32-bit local data bus, these pins are connected via bi-directional data transceivers. The transceivers are controlled with SW3 (OEH#), SW1 (OEL#), and IORD (W/R#) — (See Section 1.8 for schematic).

Table 2–7. Host Bus Configurations

Bus Type	BUSCONF*	REF* (LBT0)	SMEMW* (LBT1)
'386SX	'low'	'high'	'low'
'386DX	'low'	'low'	'high'
'486SX/DX	'low'	'high'	'high'

2.3 Host Interface — Local Bus *(CL-GD6215/'25/'35 only) (cont.)*

Pin Name	Pin No.	Type	Local Bus Name/Description
IRQ	38	3-S	**INTERRUPT REQUEST:** This output is typically unused in a local-bus design, but it may be connected to the INTR input if necessary. Register CR11 controls the interrupt function.
LBA#	24	OC	**LOCAL BUS ACKNOWLEDGE#:** This open-collector output is driven 'low' to indicate that the CL-GD6215/'25/'35 will respond to the current cycle. This signal is generated from a decode of the CPU output signals, A[23:2] and M/IO#. This output will be 'low' before the middle of the first timing (T2) cycle after ADS# goes 'low'.
M/IO#	36	I	**MEMORY / IO:** This input indicates whether a memory or I/O operation is to occur. It ***must*** be connected directly to the M/IO# pin on the CPU. When M/IO# is 'high', a memory operation will occur. When M/IO# is 'low', an I/O operation will occur.
READY#	32	I/O	**READY#:** For the **'386** this signal is defined as READY#. It ***must*** be connected directly to the READY# pin of the '386. This active-'low' **input** is used to track bus activity for pipelined cycles. It is used as an **output** to terminate a CL-GD6215/'25/'35 cycle. The pin ***must*** be connected to a pull-up resistor.
BRDY#		O	**BURST READY#:** For the **'486**, this signal is redefined as BRDY#. It ***must*** be connected directly to the BRDY# pin of the '486. On the '486, this active-'low' **output** is used to terminate a CL-GD6215/'25/'35 cycle. The pin ***must*** be connected to a pull-up resistor.
RESET	39	I	**RESET:** This input is used to initialize the CL-GD62XX. When 'high', it forces all outputs to a high-impedance state and initializes all registers to their reset state. When RESET goes 'low', normal operation is enabled.
SW1#	64	I/O	**SWITCH 1:** On any bus, except the **'**486 local bus, this active-'low' **input** can be used as an optional input that can be read under register control.
OEL#			**OUTPUT ENABLE LOW#:** On the **'486** local bus, this active-'low' **output** controls the output enables for the data transceivers that connect the CL-GD6215/'25/'35 SD[15:0] pins to the '486 D[15:0] pins.

SW2#	65	I	**SWITCH 2:** On any bus, except the **'**486 local bus, this active-'low' **input** can be used as an optional input that can be read under register control.
BLAST#			**BURST LAST#:** On the **'486** local bus, this pin is used to determine when the end of a burst cycle occurs. It ***must*** be connected to the BLAST# pin of the CPU.
SW3#	66	I/O	**SWITCH 3:** On any bus, except the **'**486 local bus, this active-'low' **input** can be used as an optional input that can be read under register control.
OEH#			**OUTPUT ENABLE HIGH#:** On the **'486** local bus, this active-'low' **output** controls the output enables for the data transceivers that connect the CL-GD6215/'25/'35 SD[15:0] pins to the '486 D[31:16] pins.
W/R#	34	I	**WRITE/READ#:** This input indicates whether a write or read operation is selected by the CPU. It ***must*** be connected directly to the W/R# pin on the CPU. When W/R# is 'high', a **write** will occur; when WR# is 'low', a **read** will occur.

2.4 Dual-Frequency Synthesizer Interface

Pin Name	Pin No.	Type	Description
32KHz	144	I	**32KHz:** This input may be connected to an externally supplied 32-KHz clock signal to be used for memory refresh during Suspend mode. If not used, this pin should be tied to ground.
MFILTER	142	O	**MEMORY CLOCK FILTER:** This pin ***must*** be connected to a π-RC filter, which is returned to AVSS4. The filter components, especially the input capacitor and the resistor, ***must*** be placed as close as possible to the MFILTER pin.
OSC	145	I	**OSCILLATOR INPUT:** This TTL input pin supplies the reference frequency for the dual-frequency synthesizer. It requires an input frequency of 14.31818 MHz ± 0.01% with a duty cycle of 50% ± 10%. This input can be supplied from the appropriate pin on the ISA bus, or from an oscillator.
VFILTER	52	O	**VIDEO CLOCK FILTER:** This pin ***must*** be connected to a π-RC filter, which is returned to AVSS1. The filter components, especially the input capacitor and the resistor, ***must*** be placed as close as possible to the VFILTER pin.

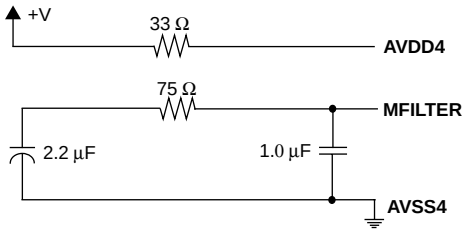


Figure 2–1. Typical Memory Clock Filter

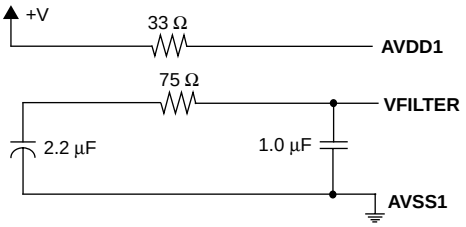


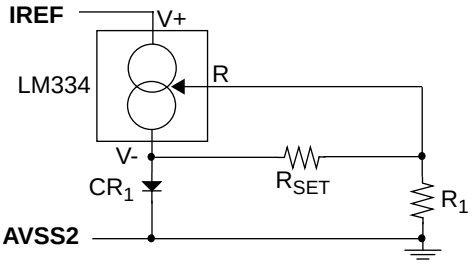
Figure 2–2. Typical Video Clock Filter

2.5 CRT Interface

Pin Name	Pin No.	Type	Description
BLUE	77	O	**BLUE VIDEO:** This analog output supplies current corresponding to the blue value of the pixel being displayed. Each of the three DACs consists of 255 summed current sources. For each pixel, the 6-bit value from the Look-up table is applied to each DAC input to determine the number of current sources to be summed. Full-scale current on the RED, GREEN, and BLUE outputs is related to IREF as follows: I_{full} = (63/31) x IREF To maintain IBM VGA-compatibility, each DAC output is typically terminated to monitor ground with a 150-Ω, 2% resistor. This resistor, in parallel with the 75-Ω resistor in the monitor, will yield a 50-Ω impedance to ground. For a full-scale voltage of 700 mV, the full-scale current output should be 14 mA.
GREEN	78	O	**GREEN VIDEO:** This analog output supplies current corresponding to the green value of the pixel being displayed. See the description above of BLUE VIDEO for information regarding the termination of this pin.
HSYNC	75	3-S	**HORIZONTAL SYNC:** This output supplies the horizontal synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the monitor connector.
IREF	89	I	**DAC CURRENT REFERENCE:** The current drawn from AVDD2/AVDD3 through this pin determines the full-scale output of each DAC. This pin should be connected to a constant-current source (typically 6.9 mA). See Application Alert AA-GD3, *IREF Current Source for the CL-GD62XX.*

Example:

V_{CC}/V_{DD}	R_{SET} ± 1%	R_1 ± 1%	Diode CR_1
5.0 Volts	22.1 Ω	200 Ω	1N4148 or equivalent
3.3 Volts	15 Ω	121 Ω	Schottky Diode (V_F < 0.4V)



RED	79	O	**RED VIDEO:** This analog output supplies current corresponding to the red value of the pixel being displayed. See the description above of BLUE VIDEO for information regarding the termination of this pin.

2.5 CRT Interface *(cont.)*

Pin Name	Pin No.	Type	Description
VSYNC	74	3-S	**VERTICAL SYNC:** This output supplies the vertical synchronization pulse to the monitor. The polarity of this output is programmable. This pin may be connected directly to the corresponding pin on the monitor connector.

2.6 Display Memory Interface

Pin Name	Pin No.	Type	Description
CAS*	127	O	**COLUMN ADDRESS STROBE*:** This active-'low' output is used to latch the column address from MA[9:0] into the DRAMs. When DUALCAS [pin 72] is 'low' (dual-WE DRAMs), this pin is defined as CAS*, and must be connected to the CAS* inputs of the DRAMs. When DUALCAS = 'high', this pin is defined as WE*, and is connected to the WE* inputs of the DRAMs.
DUALCAS	72	I	**DUALCAS:** This input is used to select between a dual-CAS-type DRAM and a dual-WE-type DRAM. When DUALCAS = 'low' (dual-WE DRAMs), pin 114 is defined as WE1*. pin 126 is defined as WE0*, and pin 127 is defined as CAS*. When DUALCAS = 'high' (dual-CAS DRAMs), pin 114 is defined as CAS1*, pin 126 is defined as CAS0*, and pin 127 is defined as WE*.
MA[9:0]	129 131:138 140	O	**MEMORY ADDRESS [9:0]:** These outputs drive the address inputs of the DRAMs, and must be connected to their corresponding address pins. MA[0] and MA[8] are often swapped to make the interface to symmetric and asymmetric DRAMs consistent. On asymmetrical DRAMs, MA[0] and MA[9] are only used to drive row addresses (not column addresses). For a detailed explanation, see Section 5.4 of Application Note AN-GD30, *A Single DRAM LCD Motherboard Solution for Monochrome/Color Notebook Computers.*
MD[15:0]	106:107, 109:113, 115:117 119:121, 123:125	I/O	**MEMORY DATA [15:0]:** These pins are used to transfer data between the CL-GD62XX and the display memory. These pins must be connected to the data pins of the DRAMs.
OE*	130	O	**OUTPUT ENABLE*:** This active-'low' output is used to control the DRAM Output Enables. For 256K x 4 DRAMs and 256K x 16 DRAMs with Dual-write Enables, this pin must be connected to the OE* pins of all the DRAMs in the display memory array.
RAS*	128	O	**ROW ADDRESS STROBE*:** This active-'low' output is used to latch the row address from MA[9:0] into the DRAMs. This pin must be connected to the RAS* pins of all the DRAMs in the display memory array.

2.6 Display Memory Interface *(cont.)*

Pin Name	Pin No.	Type	Description
WE[1:0]*	114, 126	O	**WRITE ENABLE [1:0]*:** These active-'low' outputs are used to control the WE* or CAS* inputs of the DRAMs, depending on the state of the DUALCAS input. When DUALCAS [pin 72] = 'low' (dual-WE DRAMs), these pins are defined as WE[1:0]*, and are connected to the WE1* and WE0* inputs of the display memory array. When DUALCAS = 'high' (dual-CAS DRAMs), these pins are defined as CAS[1:0]*, and are connected to the CAS1* and CAS0* inputs of the display memory array.

2.7 Miscellaneous Pins

Pin Name	Pin No.	Type	Description
EROM*	159	O	**ENABLE ROM*:** This is a multi-use pin that is configured differently for each host bus. When the ISA or PI bus is selected, EROM* is an active-'low' **output** gated with SMEMR* to control the Output Enable pins of up to two 8-bit bus drivers. These drivers are used to connect the data pins of the 'optional' BIOS EPROMs to the system data bus. This output goes active only for memory read cycles to the Address Range C000:0 through C7FF:F.
BE0#		I	**BYTE ENABLE 0#:** When the local bus for the '386DX or '486 is selected, this pin is defined as the active-'low' BE0# **input**, which is connected to the BE0# output of the CPU. This pin is not used with the '386SX local bus. The EROM* output is forced to high-impedance when RESET is 'high'.
INTCLK*	68	I	**INTERNAL CLOCK*:** This input may be set 'high' at Reset, so that externally supplied clocks can be used for testing. This pin should normally be connected to ground for internal voltage-controlled oscillator operations.
SW1#	64	I/O	**SWITCH 1:** On any bus, except the **'**486 local bus, this active-'low' **input** can be used as an optional input readable under register control.
OEL#			**OUTPUT ENABLE LOW#:** On the **'486** local bus, this active-'low' **output** controls the output enables for the data transceivers that connect the CL-GD6215/'25/'35 SD[15:0] pins to the '486 D[15:0] pins.
SW2#	65	I	**SWITCH 2:** On any bus, except the **'**486 local bus, this active-'low' **input** can be used as an optional input that can be read under register control
BLAST#			**BURST LAST#:** On the **'486** local bus, this input is used to determine when the end of a burst cycle occurs. It ***must*** be connected to the BLAST# pin of the CPU.
SW3#	66	I/O	**SWITCH 3:** On any bus, except the **'**486 local bus, this active-'low' **input** can be used as an optional input that can be read under register control.
OEH#			**OUTPUT ENABLE HIGH#:** On the **'486** local bus, this active-'low' **output** controls the output enables for the data transceivers that connect the CL-GD6215/'25/'35 SD[15:0] pins to the '486 D[31:16] pins.

2.7 Miscellaneous Pins *(cont.)*

Pin Name	Pin No.	Type	Description
TWR*	80	I	**TEST WRITE*:** This active-'low' input is for factory testing and ***must not be connected*** to the system for normal operation. It has internal pull-up resistors.

2.8 Power Management Pins

Pin Name	Pin No.	Type	Description
ACTi	28	I	**ACTIVITY:** This pin is an optional activity-sense input. Any logic 'low'-to-'high' transition on this input may be used, with register masking, to reset the internal power-down timers. When not used, connect ACTi to ground.
FPBACK	86	O	**FLAT PANEL BACKLIGHT:** This output is part of the panel power sequencing. It should be connected to the panel backlight enable.
FPVCC	87	O	**FLAT PANEL VCC:** This output is part of the panel power sequencing. It should be connected to the panel logic power enable.
FPVEE	82	O	**FLAT PANEL VEE:** This output is part of the panel power sequencing. It should be connected to the panel power enable.
LCDRSET*	67	I	**LCD RESET*:** This active-'low' signal is an optional LCD-display reset input. Any logic 'high'-to-'low' transition on this input will clear both the LCD and CRT Enable bits in the Power Management register (CR20[6:5]). This will initiate the LCD-panel power-down sequence, and stop video memory refresh. The logic 'low'-to-'high' transition on this pin does ***not*** restore the CRT or LCD Enable bits. These bits must be restored by writing to the appropriate registers. This input has an internal pull-up resistor. When LCDRSET* is not used, it should not be connected.
NPD	71	I	**NO POWER DOWN:** This input can be used to indicate the presence of AC power. When NPD is 'high', the internal power-down timers will be stopped and prevented from initiating a panel power-down sequence. When this input goes 'low', the timers will resume. This pin has an internal pull-down resistor, and may be left disconnected if not used.
STANDBY	83	I/O	**STANDBY:** This pin can be programmed to be an input or an output with register CR20[7]. When programmed as an **input**, CR20[7] = '0', it is the hardware control for the Standby mode. When STANDBY goes 'high', the power-down sequence that starts the Standby mode is initiated. When programmed as an **output**, CR20[7] = '1', it indicates the Standby mode status; when 'high', the CL-GD62XX is in Standby mode.

2.8 Power Management Pins *(cont.)*

Pin Name	Pin No.	Type	Description
SUSPEND	85	I	**SUSPEND:** This input is programmable in polarity, SR8[3], and is monitored by an internal timer, CR21[3:0], for debounce. It can be used to initiate hardware-Suspend mode or turn off the flat-panel display. The hardware-Suspend mode is the most efficient power-saving mode for the system. The default polarity is active-'high'.

2.9 LCD Flat Panel Interface

The LCD flat-panel interface is panel and CL-GD62XX controller dependent.

NOTE: Refer to the *Cirrus Logic Flat Panel Interface Connection Table* in the *CL-GD62XX Applications Book* for specific panel-connection information. Also, see Table 1–3 for panel-vs.-pin cross references.

Pin Name	Pin No.	Type	Description
B[5:0]	57:56 54 93:91	O	**BLUE BITS [5:0]:** These bits contain BLUE color data for TFT color flat panels. Refer to **NOTE** above.
DE	100	O	**DISPLAY ENABLE:** For those flat panels that require an external display enable, this pin is used to provide a data enable. For the CL-GD6225/'35 it is the second Shift Clock output for STN single-scan dual-clock color panels.
FPVDCLK	105	O	**FLAT PANEL VIDEO CLOCK:** This signal is used to drive the flat panel shift clock which is designated as CP2 by some panel manufacturers.
G[5:0]	61:59 97 95:94	O	**GREEN BITS [5:0]:** These bits contain GREEN color data for TFT color flat panels. Refer to **NOTE** above.
LD[3:0]	94:91	O	**LOWER DATA [3:0]:** The Lower Data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4-bit parallel data for the lower portion of the panel.
LFS	103	O	**LCD FRAME START:** This output provides a pulse to start a new frame on flat panels.
LLCLK	101	O	**LCD LINE CLOCK:** This output is used to drive the LCD-panel line clock. This signal is also designated as LP or CP1 by some panel manufacturers.
MOD	104	O	**MODULATION:** This output provides AC inversion. It should be connected to the MOD, FR or DF inputs of the panel, as is appropriate. Some panel manufacturers provide this function in the panel circuitry.
R[5:0]	70:69 63:62 99:98	O	**RED BITS [5:0]:** These bits contain RED color data for TFT color flat panels. Refer to **NOTE** above.
SLD[7:0]	99:97 95:91	O	**STN LOWER DATA [7:0]:** The Lower Data bits [7:0] are for use with color STN LCD panels and are available only on the CL-GD6225/'35.

2.9 LCD Flat Panel Interface *(cont.)*

Pin Name	Pin No.	Type	Description
SUD[7:0]	63:59 57:56 54	O	**STN UPPER DATA [7:0]:** The Upper Data bits [7:0] are for use with color STN LCD panels, and are available only on the CL-GD6225/'35.
UD[3:0]	99:97 95	O	**UPPER DATA [3:0]:** The Upper Data bits [3:0] are typically used with monochrome dual-scan flat panels to provide 4-bit parallel data for the upper portion of the panel.

2.10 Power And Ground Pins

Pin Name	Pin No.	Type	Description
AVDD1	53	Power	**ANALOG VDD (VCLK):** This pin is used to supply +3.3V or +5.0V to the video clock synthesizer of the CL-GD62XX. The same voltage as CVDD ***must*** be used. This pin ***must*** be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS1 with 0.1-µF and 10-µF capacitors.
AVDD2 AVDD3	73 88	Power	**ANALOG VDD (DAC):** These two pins are used to supply +3.3V or +5.0V to the palette DAC of the CL-GD62XX. Both pins ***must*** be connected to the same voltage as CVDD. Each pin ***must*** be connected directly to the VCC rail and bypassed with 0.1-µF and 10-µF capacitors, with proper high-frequency characteristics, placed as close to the pin as possible. When a multi-layer board is used, connect each AVDD pin to the power plane.
AVDD4	141	Power	**ANALOG VDD (MCLK):** This pin is used to supply +3.3V or +5.0V to the memory clock synthesizer of the CL-GD62XX. The same voltage as CVDD ***must*** be used. This pin ***must*** be connected to the VCC rail via a 33-Ω resistor and bypassed to AVSS4 with 0.1-µF and 10-µF capacitors.
AVSS1	51	Ground	**ANALOG VSS (VCLK):** This pin is used to supply ground reference to the video clock synthesizer of the CL-GD62XX. This pin ***must*** be connected to the analog ground rail, which should be isolated from VSS (digital) ground.
AVSS2 AVSS3	76 90	Ground	**ANALOG VSS (DAC):** These two pins are used to supply ground reference to the palette DAC of the CL-GD62XX. Each pin ***must*** be connected to the analog ground rail, which should be isolated from VSS (digital) ground.
AVSS4	143	Ground	**ANALOG VSS (MCLK):** This pin is used to supply ground reference to the memory clock synthesizer of the CL-GD62XX. This pin ***must*** be connected to the analog ground rail, which should be isolated from VSS (digital) ground.

2.10 Power And Ground Pins *(cont.)*

Name	Pin No.	Type	Description
BVDD1 BVDD2	1 41	Power	**BUS VDD:** These two pins are used to supply +3.3V or +5.0V to the bus interface pin group of the CL-GD62XX. Both pins ***must*** be connected to the same voltage. Each pin ***must*** be connected directly to the VCC rail. Each pin ***must*** be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect each VDD pin to the power plane.
CVDD1 CVDD2	55 147	Power	**CORE VDD:** These two pins are used to supply +3.3V or +5.0V to the internal core logic of the CL-GD62XX. Each pin ***must*** be connected directly to the VCC rail. Each pin ***must*** be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect each VDD pin to the power plane.
DVDD1 DVDD2	102 122	Power	**DRAM VDD:** These two pins are used to supply +3.3V or +5.0V to the internal DRAM interface pin group of the CL-GD62XX. Each pin ***must*** be connected directly to the VCC rail. Each pin ***must*** be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect each VDD pin to the power plane.
PVDD1	81	Power	**PANEL VDD:** This pin is used to supply +3.3V or +5.0V to the LCD flat panel interface pin group of the CL-GD62XX. This pin ***must*** be connected directly to the VCC rail. This pin ***must*** be bypassed with a 0.1-µF capacitor with proper high-frequency characteristics, as close to the pin as possible. When a multi-layer board is used, connect this VDD pin to the power plane.
VSS1-VSS11	20, 40, 47, 58, 84, 96, 108, 118, 139, 152, 160	Ground	**VSS (Digital) Ground:** These 11 pins are used to supply ground reference for the core logic and pin groups of the CL-GD62XX. Each pin ***must*** be connected directly to the ground rail. When a multi-layer board is used, each VSS pin ***must*** be connected to the ground plane.

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3. FUNCTIONAL DESCRIPTION

This section provides functional information and design guidelines on chip resources and interfaces to the CL-GD62XX VGA controllers.

3.1 General

The CL-GD62XX family of VGA controllers offers a complete solution for LCD VGA subsystems. All of the hardware necessary for CPU updates to memory, screen refresh, and DRAM refresh is included in the CL-GD62XX. With any family member, a VGA motherboard solution can be implemented with only one 256K x 16 DRAM.

3.2 Functional Blocks

The following functional blocks have been integrated into the CL-GD62XX:

3.2.1 CPU Interface

The CL-GD62XX connects directly to the ISA bus, ’386/’486SL PI bus, or ’386 and ’486 local bus (CL-GD6215/25 only). No glue logic is required. The CL-GD62XX internally decodes a 16- or 24-bit address and responds to the applicable control lines. It executes both I/O accesses and memory accesses as either an 8- or 16-bit device.

3.2.2 CPU Write Buffer

The CPU Write Buffer contains a queue of CPU write accesses to display memory that have not been executed because of memory arbitration. Maintaining a queue allows the CL-GD62XX to release the CPU as soon as it has recorded the address and data, and to execute the operation when display memory is available, increasing CPU performance.

3.2.3 Graphics Controller

The graphics controller is located between the CPU interface and the memory sequencer. It performs text manipulation, data rotation, color mapping, and other miscellaneous operations.

3.2.4 Memory Arbitrator

The memory arbitrator allocates bandwidth to the three functions that compete for the limited bandwidth of display memory. These are CPU access, screen refresh, and DRAM refresh. DRAM refresh is handled transparently by allocating a selectable number of CAS*-before-RAS* refresh cycles at the beginning of each scanline. Screen refresh and CPU access are allocated cycles according to the FIFO-control parameters, with priority given to screen refresh.

3.2.5 Memory Sequencer

The memory sequencer generates timing for display memory. This includes RAS*, CAS* and multiplexed-address timing, as well as WE* and OE* timing. The memory sequencer generates CAS*-before-RAS* refresh cycles, Random-Read and Random-Early-Write cycles, and Fast Page-mode Read and Early-Write cycles. The memory sequencer generates multiple CAS* or WE* signals according to the memory type used.

3.2.6 CRT Controller

The CRT controller generates the HSYNC and VSYNC signals required for the monitor, as well as BLANK* signals required by the palette DAC.

3.2.7 LCD Flat-Panel Controller

The LCD flat-panel controller drives single-scan and dual-scan color SDN and active-matrix color TFT panels. It also drives monochrome panels with multiple gray-shading options. Additionally, it provides all the power sequencing controls needed by the panels.

3.2.8 Video FIFO

The Video FIFO allows the memory sequencer to execute the display memory accesses needed for screen refresh at maximum memory speed rather than at the screen refresh rate. This makes it possible to collect the accesses for screen refresh near the beginning of the scanline, and to execute them in Fast-page mode rather than Random-Read mode.

3.2.9 Attribute Controller

The attribute controller formats the display for the screen. Display color selection, text blinking, and underlining are performed by the attribute controller.

3.2.10 Palette DAC

The palette DAC contains the color palette and three 6-bit digital-to-analog converters. The color palette, with 256 18-bit entries, converts a color code that specifies the color of a pixel into three 6-bit values — one each for red, green, and blue.

3.2.11 Dual-Frequency Synthesizer

The dual-frequency synthesizer generates the memory sequencer clock and the video display clock from a single-reference frequency. The frequency of each clock is programmable. The reference frequency can be generated with an internal crystal-controlled oscillator. Alternatively, it can be supplied from an external TTL source.

3.3 Functional Operation

The four major operations handled in the CL-GD62XX are discussed below.

3.3.1 CPU Access to Registers

The host can be any processor controlling an ISA, ’386/’486SL PI, or ’386/’486 local bus. It accesses CL-GD62XX registers by setting up a 16- or 24-bit address and forcing IORD* or IOWR* ‘low’. The CL-GD62XX responds either as an 8- or 16-bit peripheral, depending on the system configuration, and the host bus interface.

CPU register access does not affect DRAM or screen refresh, which can occur concurrently with CPU access, unless the host is changing display parameters or has suppressed refresh.

3.3.2 CPU Access to Display Memory

All host accesses to display memory are handled by the CL-GD62XX. The host first sets up parameters, such as color and write masks, then generates a memory access in the programmed response range of the CL-GD62XX.

3.3.3 Display Memory Refresh

The CL-GD62XX automatically generates a selectable number of CAS*-before-RAS* refresh cycles during each horizontal timing period.

3.3.4 Screen Refresh

The CRT monitor requires near-constant rewriting (refresh), since the only memory is the phosphor persistence of the screen. Phosphor persistence is typically only a few milliseconds. The CL-GD62XX fetches information from the display memory for each scanline as quickly as possible, using Fast-Page-mode cycles to fill the video FIFO. This allows the maximum possible time for the host to access the display memory.

3.4 Performance

The CL-GD62XX offers the following performance-enhancing features:

- 16-bit CPU interface to I/O registers for faster host access
- 16-bit CPU interface to display memory for faster host access in all modes, including Planar
- DRAM Fast-Page-mode operations for faster access to display memory
- CPU Write Buffer to accelerate CPU access for display writes
- Video FIFO minimizes memory contention
- 32 x 32 hardware cursor to improve Microsoft™ Windows performance
- Increased throughput with ’386 and ’486 local-bus interface (CL-GD6215/’25/’35)

3.5 Compatibility

The CL-GD62XX includes all registers and data paths required for VGA controllers.

The CL-GD62XX supports extensions to VGA, including 1024 x 768 x 16 non-interlaced modes. Additionally, various 132-column text modes are supported.

The CL-GD62XX has programmable input threshold levels that support TTL or CMOS logic inputs (see register SR16{1:0]).

3.6 Data Bus Interface for 32-Bit Processors

The CL-GD62XX has a 16-bit data bus that must transfer data to/from the 32-bit ’386DX/’486 data bus.

The ’386DX and ’486 assists such transfers, during multiple-word requests, by producing an additional read or write cycle. The CL-GD62XX drives BS16# output ‘low’ to signal 32-bit accesses to video memory or related I/O registers.

During the additional cycle, the ’386DX processor provides internal byte steering, that routes the high-order word to the low-order word pins, but the ’486 does not. The ’486 requires external transceivers to route its 32-bit CPU data to the 16-bit CL-GD62XX data pins.

To accommodate 32-bit aligned word transfers, the CL-GD62XX provides two outputs (OEH# and OEL#) to select between two 16-bit words. These two control lines enable the high-word and low-word bi-directional data transceivers (74F245), respectively (see Section 1.8 for schematic). Data direction is determined by the CPU status line W/R# attached to the DIR pin of the transceivers. During the first cycle of a 32-bit aligned read from the CL-GD62XX, BS16# and OEL# are driven ‘low’, and OEH# is driven ‘high’. The processor reads the lower-order word from the low-word bus transceivers that route the contents of the CL-GD62XX SD[15:0] to the CPU D[15:0] pins. At the beginning of the second cycle, the CL-GD62XX drives BS16# and OEH# ‘low’, and OEL# ‘high’, causing the high-word transceivers to drive the contents of SD[15:0] onto the D[31:16] CPU pins. Status line W/R# must be held stable throughout both cycles, ensuring that the bus transceivers are driving in the correct direction. Also, since the load on the W/R# output can be four or more, a buffer should be used on W/R# to drive the transceivers.

3.6.1 ’486 Burst Mode Support

The CL-GD62XX can request and respond to burst cycles for accesses that require more than a single cycle. By supporting ’486 burst transfers, the CL-GD62XX delivers higher performance. During a CPU 32-bit write when BS16# is ‘low’, a non-burstable CL-GD62XX would normally require two cycles to complete the transfer. The second cycle of a multiple transfer following the first cycle requires an additional clock to produce ADS# (T1 timing). In contrast, burst cycles eliminate the need for this additional clock. As a result of Burst-mode support for 32-bit writes, one CPU clock is saved.

3.6.2 CL-GD62XX Address Decode and Latching

The CL-GD62XX responds to cycles after decoding addresses A[23:2] and status line M/IO#. The CL-GD62XX indicates to the rest of the system that it owns the cycle by asserting LBA# (LDEV# by VL-Bus naming convention). Other devices should not respond when LBA# goes ‘low’ before the middle of the first T2 timing cycle. For the 32-bit address bus of the ’386DX and ’486 processors, the address lines A31:23 must be externally decoded and a ‘low’-true signal (for a valid CL-GD62XX cycle) should be supplied to the A23 (upper address) input of the CL-GD62XX. This decode must be performed in the minimum possible time; less than 10 ns is recommended.

Since the CL-GD62XX does not decode status line D/C#, it does not respond to special and interrupt acknowledge cycles. The address produced by the CPU during these cycles lies outside the memory and I/O range of the CL-GD62XX. The CL-GD62XX will not respond to I/O locations 0002H-0005H, since responding would cause an inappropriate reaction to certain special cycles.

Because AHOLD of the ’486 may go ‘high’ in the middle of a cycle, the CL-GD62XX will latch the address at the end of the T1 timing cycle. The address latch allows the local bus address to change during an address-hold response without any effect on the CL-GD62XX address decode for the current cycle.

3.6.3 Bus Cycle Restart

The CL-GD62XX does not support ’486 bus restart cycles. Since the CL-GD62XX does not receive BOFF#, it does not sense bus cycle restarts and cannot respond appropriately.

3.6.4 Other Considerations

For ’386SX:

CPU-RESET is used with CLK2X to generate an internal synchronous 1X system clock. The CPU NA# output (for pipelined cycles) is not an input to the CL-GD62XX, but the controller automatically detects and responds to system-initiated-pipelined cycles.

For ’386DX:

CPU-RESET is used with CLK2X to generate an internal synchronous 1X system clock. BS16# is always set ‘low’ for CL-GD62XX bus cycles. Pipelined cycles are not supported for ’386DX.

For ’486:

BS16# is always set ‘low’ for CL-GD6215/’25/’35 bus cycles.

For ’386SL/’486SL (PI):

PCMD#, when ‘low’, enables the data bus buffers for the current cycle. The ‘high’-to-’low’ transition of PSTART# latches the address on LA[23:17] and SA[16:0].

The READY# line for local bus support is normally ‘off’ (high-impedance), and a system pull-up resistor is needed. When the CL-GD62XX decodes a valid address, the READY# line remains ‘off’ until it can be driven active-‘low’ for one clock period to end the bus cycle. READY# is then driven ‘high’ for about 5 ns before returning to ‘off’. For memory-read cycles, the READY# output does not go ‘low’ until the read data is valid. Memory-write cycles are performed in the minimum time possible, as long as the system Write Buffer is not full. I/O read and write cycles (except DAC) have a READY# delay of four CPU clock periods for data cycle requirements. All I/O to the internal video DAC have a READY# delay of four VCLK periods to meet the DAC minimum cycle-time requirements.

The local bus is always 16-bit. All registers are compatible with 16-bit bus cycles; they use SD[7:0] for even-byte addresses, and SD[15:8] for odd-byte addresses. READY# goes ‘low’ for any I/O read or write to any decoded address in the CL-GD62XX I/O address range (even the unused addresses). The unused locations at decoded CL-GD62XX I/O addresses will always be read as ‘00H’ and will ignore any write data.

3.7 LCD Flat Panel Interface

The CL-GD62XX directly drives a variety of LCD flat panels, including dual-scan/dual-data/passive-matrix monochrome, color active-matrix TFT, color passive-matrix STN (CL-GD6225), and dual-scan color STN (CL-GD6235) panels. Proprietary techniques minimize flicker, noise, and pattern motion while enhancing contrast within the grayscales being used.

Grayscale mapping is accomplished by modulating the on-to-off time of individual pixels in the panel and allowing the eye to integrate the superimposed pixels to perceptible grayscales. There are four grayscale mapping options available through register control:

- NTSC weighted
- DAC Look-up table ‘green’ output
- 4- or 6-bit video data direct
- Attribute Controller 64-shade color data

Color TFT, on all CL-GD62XX devices, and color STN, on the CL-GD6225/’35 are directly supported without additional circuitry. Both 8- and 16-bit interfaces to STN panels are supported on the CL-GD6225/’35. All CL-GD62XX family members support 9-bit (3x RGB), 12-bit (4x RGB), 15- and 18-bit TFT color LCD panels. Up to 256 colors from a palette of 256,000 are supported for graphics modes on TFT panels, as well as 16 colors from a palette of 64 colors for text modes.

The CL-GD62XX allows a full spectrum of PC applications written for analog monitors and various video modes to run on standard 640 x 480 LCD flat panels. This is accomplished through color emulation, attribute remapping, and resolution mapping.

In addition, summing circuitry allows rapid generation of IBM-compatible grayscale equivalents of color images. Up to 64 grayscale levels are available by using this proprietary logic. This technique permits all applications that generate monochrome, 4-, 16-, or 256-color images to be run on a monochrome flat panel display.

Cirrus Logic AutoMap™ logic maps 256 colors into a monochrome image; the colors then appear either in 16 shades of gray with grayscale enhancement, or 64 shades of gray in 256-color modes. The hardware-based algorithm tracks the particular palette map being used by the internal RAMDAC™. RAMDAC data may be stored, as desired by the application, in orderly or random sequences. Realistic renditions of color images are not affected.

Video resolutions can be automatically centered or expanded. Expansion serves to fill the screen regard-

less of the number of lines generated by the video mode. If expansion is not selected, then automatic centering can be selected.

3.8 Intelligent Power Management and Sequencing

Notebook and laptop computers have stringent power limitations due to battery operation and heat dissipation. To support these needs, the CL-GD62XX family of VGA controllers use power-saving design techniques for the devices themselves, and efficient power management of the display system. The devices are manufactured with low-power CMOS technology and provide the following power-saving capabilities:

- 3.3- and 5.0-volt operation
- Low-power video DAC operation
- Stop or slow on-chip oscillators and related circitry to reduce power
- Slow down video-memory refresh
- Turn off I/O circuitry to reduce power

In addition, the CL-GD62XX provides efficient power management of the display system by turning-off, or shutting-down the LCD flat panel and CRT when not being used. The controllers offer both hardware methods (using device pins) and software methods (using programmable timers and on-chip registers) to control the LCD flat panel and CRT.

3.8.1 Normal Mode

In the Normal mode, the LCD flat panel and/or the CRT are being used. During the Normal mode, the following occur:

- Display(s) are active and receive power
- Full-screen refresh occurs
- CPU can access:
  - — Video memory
  - — RAMDAC™
  - — I/O registers
- Refresh is provided to video memory
- VDD = 3.3V, when performance permits

Since the power consumption is proportional to the square of the supply voltage, the use of 3.3-volt supplies, whenever possible, saves a vast amount of power. Since power consumption is directly proportional to the frequency where the controller is run, the CL-GD62XX uses a proprietary on-chip Frame-Accelerator. The Frame-Accelerator is used only with dual-scan LCD panels to maintain the maximum screen refresh rate, while the clock to the CL-GD62XX functions at 25 MHz or less.

3.8.2 Hardware Power-Management Modes

Several dedicated pins have been assigned to facilitate power management while in LCD-only or CRT-only modes.

- The FPVCC, FPVEE, and FPBACK pins are used to control or enable external voltage generation circuitry during power sequencing.
- The LCDRSET, STANDBY, and SUSPEND pins can be connected to external sources to force the system into power-down modes.
- The NPD pin, when 'high', stops the power-down counters from decrementing. This pin is used to inhibit automatic power-down, when the system is supplied from an AC power source.

3.8.3 Standby Mode

Standby mode stops power to the LCD panel (and/or CRT) when the panel is not being used. As a result, since there is no screen refresh, normal clock rates may be stopped or slowed to further reduce power consumption. During Standby mode, the following occurs:

- LCD panel power-down sequence occurs automatically when this mode is entered
- VCLK oscillator is shut off
- MCLK frquency is divided by six
- No clock is provided to the CRT controller
- Video DAC is in low-power mode
- Video display memory refresh is maintained
- The CPU can access and modify the video display memory and DAC palette
- When Standby mode is terminated, the previous state is restored

3.8.3.1 Initiating/Entering Standby Mode

The CL-GD62XX provides three methods for entering Standby mode — two are software-based and the other is hardware-based. All methods offer the features itemized above. One or more of these methods can be used simultaneously to start and/or maintain Standby mode. All active methods must be removed to terminate Standby mode and start the power-up sequence.

- The Standby Mode Timer, CR21[3:0], can be programmed (in increments of one minute) up to 16 minutes. If the timer is allowed to count down to zero, the Standby mode power-down sequence is started.
- Standby mode is initiated, using software, by setting CR20[4] to '1', starting the Standby mode power-down sequence.
- To enter Standby mode through hardware, connect the STANDBY input (pin 83) to an external source. When the STANDBY pin is driven 'high', the Standby mode power-down sequence starts.

3.8.3.2 Terminating/Exiting Standby Mode

The LCD panel power-up sequence occurs automatically when the Standby mode is terminated, which occurs when all of the methods that initiated the mode are removed.

- Reset the Standby Mode Timer in one of the following ways:
  - — Use activity on the ACTi input (pin 28), that is enabled by setting CR1D[6] to '1'.
  - — Use any VGA access (memory or I/O), that is enabled by setting CR1D[5] to '1'.
  - — Use any keyboard access (except in PI-bus mode) that is enabled by setting SR8[5] to '1'.
- Terminate software Standby mode by setting CR20[4] to '0'.
- Terminate hardware Standby mode by driving the STANDBY input (pin 83) 'low'.

If a power-up or power-down sequence is in progress when there is a request to terminate or initiate Standby mode, the power-up/down sequence is allowed to complete before the new request is executed.

3.8.4 Suspend Mode

The CL-GD62XX Suspend mode is used to save power when the system is not being actively used for a long period of time. The Suspend mode not only turns off the screen(s), but also suspends operation of application programs, and, in the case of hardware-Suspend mode , prohibits the CPU from accessing video memory, I/O registers or the RAMDAC. In hardware-Suspend mode, even though application programs cease to run in either foreground or background, all the register states are saved. When the Suspend mode is terminated, the environment continues from where it stopped.

3.8.4.1 Hardware-Suspend Mode

Hardware-Suspend mode provides the most efficient means of power saving with the CL-GD62XX devices. hardware-Suspend mode is initiated using the SUSPEND input (pin 85). This pin has programmable polarity using register SR8[3], and it uses a debounce timer CR23[7:4] to minimize accidental attempts to initiate Suspend mode. In this mode, the input pads are shut off and the bus interface does not receive power. All I/O pins, except the dedicated Suspend-mode input, are de-activated to further reduce power consumption. Additional power savings occurs because CPU host access to video memory is denied, and a slower 32-kHz clock refreshes the video memory by performing CAS*-before-RAS* refresh. This slow clock input comes from one of two sources:

- By setting CR1D[4] to '1', a 32-kHz clock output results by dividing the 14.318-MHz clock by 432.
- By setting CR1D[4] to '0', an external 32-kHz clock input can be provided via the 32-kHz input (pin 144). A further power reduction is now possible by disabling the 14.318-MHz clock by setting SR16[2] to '1'.

When the system is in hardware-Suspend mode, the following occurs:

- The LCD panel power-up/down sequence occurs automatically when Suspend mode is entered or exited.
- The VCLK and MCLK oscillators are shut off, if CR1C[2] = '1'.

- No CPU access is allowed to the following:
  - — Video memory
  - — RAMDAC™
  - — I/O registers
- Although video display memory cannot be accessed by the CPU during Suspend mode, the contents are preserved. (This action is useful when a system remains inactive for a relatively long time.)
- Register data contents are retained.
- The CL-GD62XX refresh clock for video memory is set to 32 kHz , unless DRAMs are self-refresh.

▼ WARNING: In local-bus systems, CPU attempts to access the CL-GD62XX can cause a system-hang condition.

3.8.4.2 Software-Suspend Mode

This mode is initiated by setting CR20[3] to '1'. In contrast to the hardware-Suspend mode, software-Suspend mode allows the CPU to access video RAM, the I/O bus, and the RAMDAC.

3.8.4.3 Initiating/Entering Suspend Mode

The following methods are used to initiate Suspend mode. To minimize power consumption, the hardware-Suspend mode is recommended.

- To enter hardware-Suspend mode, connect the dedicated SUSPEND input (pin 85) to an external source. The SUSPEND input is programmable in polarity, and the CL-GD62XX internal Debounce Timer (register CR23[7:4]) monitors the input for accidental activation.
- The SUSPEND input pin can also be used to indicate a 'cover-closed' condition by programming CR1C[2] to '0', this prohibits power-down of the MCLK and VCLK. Since CPU access is not disabled in this mode, more power is required.
- The software-Suspend mode is entered by setting CR20[3] to '1'. In this mode, CPU access is still active and the SUSPEND pin is disabled. This mode is not recommended, because it requires more power than hardware-Suspend mode.

3.8.4.4 Terminating/Exiting Suspend Mode

Suspend mode must be terminated/exited in the same manner that it was entered. When the SUSPEND input is driven 'inactive' ('high' or 'low' depending on programmed polarity), Suspend mode is terminated. In software, Suspend mode is terminated by setting CR20[3] to '0'. When Suspend mode is terminated, the system returns to the same operational state it was in before Suspend mode was entered.

3.8.5 Power Sequencing

The CL-GD62XX internal logic controls the sequencing the LCD contrast voltage, logic power, data inputs, and control inputs. To minimize the possibility of damaging the LCD panel, the CL-GD62XX provides the recommended power-up/down sequences shown below. These sequences meet most panel manufacturer specifications.

3.8.5.1 LCD Panel Power-Down Sequence

1) Shut off FPVEE and FPBACK

2) Wait 96-to-128 ms

3) Force all CL-GD62XX panel control signals 'low'

4) Wait 32 ms

5) Shut off FPVCC

6) Shut off internal VCLK

3.8.5.2 LCD Panel Power-Up Sequence

1) Turn on VCLK, increase MCLK frequency

2) Wait 32 ms

3) Enable FPVCC

4) Wait 32 ms

5) Enable CL-GD62XX panel control signals

6) Wait 32 ms

7) Enable FPVEE and FPBACK

3.8.6 Additional Power Management Features

3.8.6.1 LCD-only Operation (CRT Disable)

During LCD-only operation, the CRT is disabled. In this mode, DAC analog power is off, and the HSYNC and VSYNC drive is off.

NOTE: When the CRT is disabled and Text mode is selected (CR1E[7] = '1'), power is removed from the video DAC and LUT. CPU access to the LUT is available by using the I/O read/write to 3C6-3C9. Graphics modes can use the LUT for shading.

3.8.6.2 CRT-only Operation (LCD Panel Disable)

During CRT-only operation, the LCD panel is disabled. In this mode, panel-drive signals are all inactive, and automatic power-down sequencing occurs.

3.8.6.3 Backlight Timer

An additional internal timer allows the LCD panel backlight to be controlled without entering a power-down mode. Extension register CR21[7:4] can be programmed from 0-15 minutes to activate the timer. When the register counts down to zero, the FPBACK output will be 'low' and can be used to turn off the panel backlight. Programming this register to a zero disables the Backlight Timer. This timer can be reset to extend the time-out by activity on the ACTi input, or by a VGA access. Extension register CR1D controls these choices.

3.8.6.4 ACTi Function

This input pin can be used to reset both the Standby and Backlight Internal Timers. For example, this pin can be connected to the keyboard interrupt from the system logic. Extension register CR1D[6,3] controls which timers are reset by activity on this pin.

3.9 Internal RAMDAC™

The CL-GD62XX includes an on-chip, high-speed memory digital-to-analog converter known as a RAMDAC (see Figure 3–1). The RAMDAC circuitry helps the CL-GD62XX process color-video signals and timing information to the display.

The RAMDAC includes:

- a 256-entry by 18-bit word color Look-up table
- three 6-bit digital-to-analog converters (DACs)
- a Pixel Mask register
- a Border Color register.

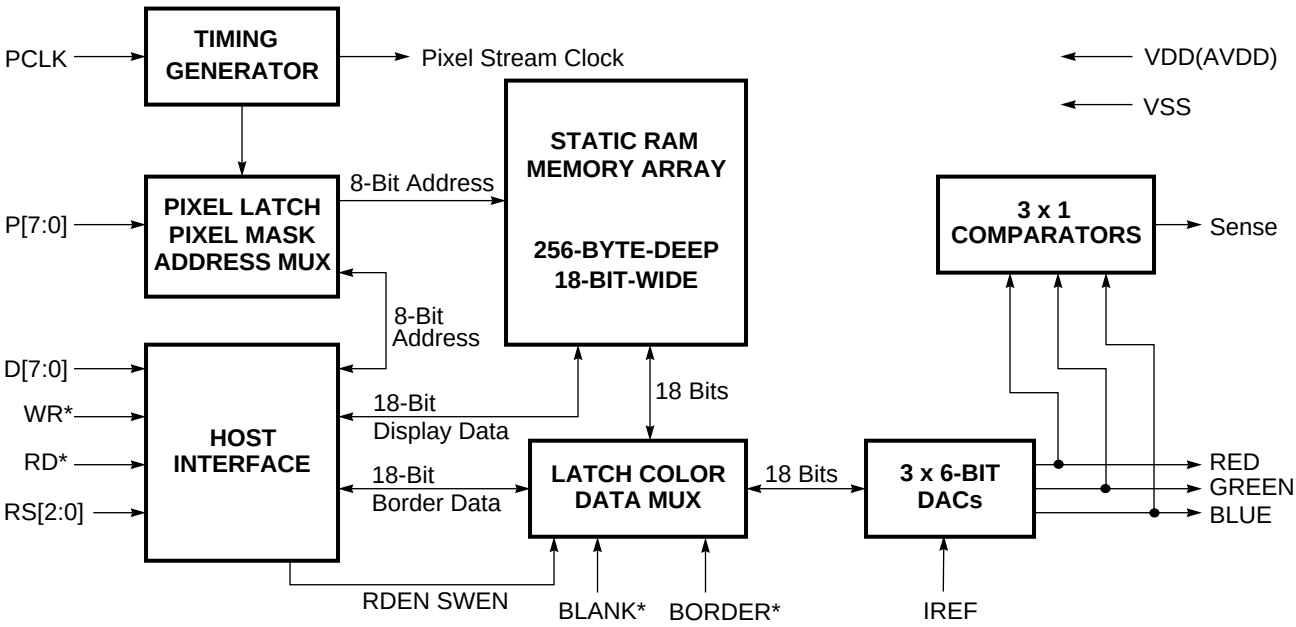

Figure 3–1. RAMDAC™ Block Diagram

An 8-bit address on the pixel address inputs defines the memory location for reading an 18-bit color data word from the Color Look-up table. This data is partitioned as three fields of six bits each (the three fields are Red, Green, and Blue) that drive the individual DAC inputs.

A pixel word mask is included so the incoming pixel address can be altered. This permits immediate changes to the Color Look-up table allowing creation of special display operations such as flashing objects and overlays.

The Color-Look-up table contents are accessed via its 8-bit host interface. An internal synchronizing circuit allows the color-value access to be completely asynchronous to the pixel video operation.

3.9.1 RAMDAC™ Video Operation

In video operation, the pixel addresses (P0-P7), and the Blank and Border inputs to the DAC are synchronized to the internal pixel clock (PCLK). Their effect appears at the DAC outputs after three further rising edges of PCLK.

The Blank and Border input signals to the DAC are internally generated by the CL-GD62XX. When the Blank input to the DAC is asserted, a binary '0' is applied to the DAC inputs, producing a zero-volt DAC output. When the Border input is asserted, the color data from the Border Color register is applied to the DAC inputs.

The DACOFF input to the DAC is both a display disable control and a DAC power-down control. When DACOFF is asserted, the DACs in the RAMDAC are totally inoperative, that results in the power dissipation being reduced to standby minimum. During this time, the three DAC outputs are at a zero-volt level. When DACOFF is removed, several PCLK cycles are required before the DACs in the RAMDAC will function properly.

3.9.2 Analog Outputs

The DAC outputs produce a 0.7-volt peak white amplitude when supplied with a reference constant current (I_{REF}). The I_{REF} current is supplied with the circuit shown in the IREF pin description in Section 2.5. For all values of I_{REF} and output loading:

$$V_{blacklevel} = \text{zero volts}$$

$$V_{Max\ White} = 0.7 \text{ volts}$$

3.9.3 Writing to the Color Look-up Table

To write a color definition to the Look-up table, a value specifying an address location in the Look-up table is first written to the Write Mode Address register. The color values for the red, green, and blue intensities are then written in succession to the Color Value register. After the blue data is latched, this new color data is then written into the Look-up table at the defined address and the Address register is incremented automatically.

Since the Address register increments after each transfer of data to the Look-up table, it is best to write a set of consecutive locations at once. The start address of the set of locations is first written to the Write Address Mode register. The color data for each address location is then sequentially written to the Color Value register. The RAMDAC automatically writes data to the Look-up table, and increments the Address register after each host transfer of three bytes of color data.

3.9.4 Reading from the Color Look-up Table

To read color data from the Look-up table, a value specifying the address location of the data is written to the Read Mode Address register. After the address is latched, the data from this location is automatically read out to the Color Value register and the Address register automatically increments.

The color intensity values are then read from the Color Value register by the sequence of three read (RD*) commands. After the blue value is transferred out, new data is read from the Look-up table at the current address to the Color Value register and the Address register automatically increments again.

If the Address register is loaded with a new starting address while an unfinished sequence is in progress, the system resets and starts a new sequence. This occurs for both read and write operations.

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4. CL-GD62XX VIDEO MODE TABLES

This section lists tables for configuring the CL-GD62XX for various CRT and flat panel video modes. For detailed information on specific LCD panels that the CL-GD62XX devices can drive, refer to the *Panel Interface Guides* section of the *CL-GD62XX Applications Book*.

4.1 CRT Video Modes

Table 4–1. IBM® Standard VGA Video Modes

Mode No. (Hex)	No. of Colors	Characters x Rows	Char. Cell (pixels)	Screen Format (pixels)	Display Mode	Dot Clock (MHz)	Horizontal Frequency (kHz)	Vertical Frequency (Hz)
0, 1	16/256K	40 x 25	9 x 16	360 x 400	Text	28	31.5	70
2, 3	16/256K	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
4, 5	4/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70
6	2/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70
7	Monochrome	80 x 25	9 x 16	720 x 400	Text	28	31.5	70
D	16/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70
E	16/256K	80 x 25	8 x 8	640 x 200	Graphics	25	31.5	70
F	Monochrome	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
10	16/256K	80 x 25	8 x 14	640 x 350	Graphics	25	31.5	70
11	2/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
12	16/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
12[a]	16/256K	80 x 30	8 x 16	640 x 480	Graphics	31.5	37.9	72
13	256/256K	40 x 25	8 x 8	320 x 200	Graphics	25	31.5	70

[a] Modes denoted by (a) are IBM® Standard VGA modes that have been enhanced by Cirrus Logic for a higher vertical frequency.

Table 4–2. Cirrus Logic Extended CRT Video Modes[a]

Mode[a] No. (Hex)	VESA No. (Hex)	No. of Colors	Characters x Rows	Character Cell (pixels)	Screen Format (pixels)	Display Mode	Dot Clock (MHz)	Horiz. Freq. (kHz)	Vert. Freq. (Hz)
14	–	16/256K	132 x 25	8 x 16	1056 x 400	Text	41.5	31.5	70
54	10A	16/256K	132 x 43	8 x 8	1056 x 350	Text	41.5	31.5	70
55	109	16/256K	132 x 25	8 x 14	1056 x 350	Text	41.5	31.5	70
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.8	60
58, 6A	102	16/256K	100 x 37	8 x 16	800 x 600	Graphics	50	48.1	72
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	36	35.2	56
5C	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	40	37.9	60
5C[b]	103	256/256K	100 x 37	8 x 16	800 x 600	Graphics	50[b]	48.1	72
5D	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	65	48.3	60
5D[c]	104	16/256K	128 x 48	8 x 16	1024 x 768	Graphics	44.9	35.5	87[c]
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	60
5F	101	256/256K	80 x 30	8 x 16	640 x 480	Graphics	25	31.5	72

[a] These extended CRT video modes are supported by the Cirrus Logic BIOS. Modes may differ if using another BIOS.

[b] Mode 5C with 72-Hz vertical frequency is only available when high-performance memory has been enabled with function 9Eh, and the dot clock is at least 50 MHz. If high-performance memory is disabled, a refresh rate of 60 Hz will be substituted.

[c] Mode 5D with Vertical Frequency = 87 Hz is an Interlaced mode.

[d] Some modes are not supported by all monitors. The best-quality vertical refresh rate for the monitor type selected will be automatically used.

4.2 LCD Flat Panel Video Modes

Table 4–3. IBM Standard VGA Video Modes

Mode No.	Mono. STN Number of Shades	Color STN Number of Colors	Color TFT Number of Colors	Characters x Rows	Character Cell (pixels)	CRT Screen Format (pixels)	Display Mode	Expanded Size (pixels)
0, 1	16/16	16/256K	16/256K	40 x 25	8 x 16	360 x 400	Text	640 x 475
2, 3	16/16	16/256K	16/256K	80 x 25	8 x 16	720 x 400	Text	640 x 475
4, 5	4/64	4/256K	4/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475
6	2/16	2/256K	2/256K	80 x 25	8 x 8	640 x 200	Graphics	640 x 475
7	2/16	Mono.	Mono.	80 x 25	8 x 16	720 x 400	Text	640 x 475
D	16/64	16/256K	16/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 475
E	16/16	16/256K	16/256K	80 x 25	8 x 8	640 x 200	Graphics	640 x 475
F	2/16	Mono.	Mono.	80 x 25	8 x 14	640 x 350	Graphics	640 x 475
10	16/16	16/256K	16/256K	80 x 25	8 x 14	640 x 350	Graphics	640 x 475
11	2/16	2/256K	2/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
12	16/16	16/256K	16/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480
13	64/256K	256/256K	256/256K	40 x 25	8 x 8	320 x 200	Graphics	640 x 480

Table 4–4. Cirrus Logic Extended LCD Video Mode[a]

Mode No.	Mono. STN Number of Shades	Color STN Number of Colors	Color TFT Number of Colors	Characters x Rows	Character Cell (pixels)	CRT Screen Format (pixels)	Display Mode	Expanded Size (pixels)
5F	64/256K	256/256K	256/256K	80 x 30	8 x 16	640 x 480	Graphics	640 x 480

a. This extended CRT video mode reflects the Cirrus Logic BIOS. Modes may differ if another BIOS is used.

5. VGA REGISTER PORT MAP

Table 5–1. VGA Register Port Map

Address	Port	Port Type
3?4[a]	CRT controller index	Read/Write
3?5[a]	CRT controller data	Read/Write
3BA	Feature control — monochrome	Write
	Input Status register 1 — monochrome	Read
3C0	Attribute controller index/data	Write
3C1	Attribute controller index/data	Read
3C2	Miscellaneous output	Write
	Input Status register 0	Read
3C3	VGA enable	Read/Write
3C4	Sequencer index	Read/Write
3C5	Sequencer data	Read/Write
3C6	Video DAC pixel mask	Read/Write
3C7	Pixel Address Read mode	Write
	DAC state	Read
3C8	Pixel Mask Write mode	Read/Write
3C9	Pixel data	Read/Write
3CA	Feature control readback	Read
3CC	Miscellaneous output readback	Read
3CE	Graphics controller index	Read/Write
3CF	Graphics controller data	Read/Write
3DA	Feature control — color	Write
	Input Status register 1 — color	Read

[a] The '?' in an address is 'B' for monochrome and 'D' for color.

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6. REGISTER INFORMATION

The following tables list the VGA Registers and CL-GD62XX Extension Registers that are contained in these devices. The CL-GD62XX Extension Registers are fully explained in this document. The standard VGA registers are explained in detail in various documents published by IBM and others, but they are not explained here.

External/General Registers

Abbreviation	Register Name	Index	Port	Page
MISC	Miscellaneous Output	–	3C2 (W)	
MISC	Miscellaneous Input	–	3CC(R)	
FC	Feature Control	–	3?A (W)	
FC	Feature Control	–	3CA (R)	
FEAT	Input Status Register 0	–	3C2	
STAT	Input Status Register 1	–	3?A	72
3C6	Pixel Mask	–	3C6	
3C7	Pixel Address Read Mode	–	3C7(W)	
3C7	DAC State	–	3C7(R)	
3C8	Pixel Address Write Mode	–	3C8	
3C9	Pixel Data	–	3C9	

The “?” in the Port Address is “B” for Monochrome mode and “D” for Color mode.

VGA Sequencer Registers

Abbreviation	Register Name	Index	Port
SRX	Sequencer Index	–	3C4
SR0	Reset	0	3C5
SR1	Clocking Mode	1	3C5
SR2	Plane Mask	2	3C5
SR3	Character Map Select	3	3C5
SR4	Memory Mode	4	3C5

CRT Controller Registers

Abbreviation	Register Name	Index	Port
CRX	CRTC Index	–	3?4
CR0	Horizontal Total	0	3?5
CR1	Horizontal Display End	1	3?5
CR2	Horizontal Blanking Start	2	3?5
CR3	Horizontal Blanking End	3	3?5
CR4	Horizontal Sync Start	4	3?5
CR5	Horizontal Sync End	5	3?5
CR6	Vertical Total	6	3?5
CR7	Overflow	7	3?5
CR8	Screen A Preset Row Scan	8	3?5
CR9	Character Cell Height	9	3?5

6. REGISTER INFORMATION *(cont.)*

CRT Controller Registers

Abbreviation	Register Name	Index	Port	Page
CRA	Text Cursor Start	A	3?5	
CRB	Text Cursor End	B	3?5	
CRC	Screen Start Address High	C	3?5	
CRD	Screen Start Address Low	D	3?5	
CRE	Text Cursor Location High	E	3?5	
CRF	Text Cursor Location Low	F	3?5	
CR10	Vertical Sync Start	10	3?5	
CR11	Vertical Sync End	11	3?5	
CR12	Vertical Display End	12	3?5	
CR13	Offset	13	3?5	
CR14	Underline Row Scan	14	3?5	
CR15	Vertical Blanking Start	15	3?5	
CR16	Vertical Blanking End	16	3?5	
CR17	CRTC Mode Control	17	3?5	
CR18	Line Compare	18	3?5	
CR22	Graphics Data Latches Readback	22	3?5	
CR24	Attribute Controller Toggle Readback	24	3?5	
CR26	Attribute Controller Index Readback	26	3?5	
CR28, CR2A—CR3FReserved				

The “?” in the Port Address is “B” for Monochrome mode and “D” for Color mode.

VGA Graphics Controller Registers

Abbreviation	Register Name	Index	Port	Page
GRX	Graphics Controller Index	–	3CE	
GR0	Set/Reset	0	3CF	73
GR1	Set/Reset Enable	1	3CF	74
GR2	Color Compare	2	3CF	
GR3	Data Rotate	3	3CF	
GR4	Read Map Select	4	3CF	
GR5	Mode	5	3CF	75
GR6	Miscellaneous	6	3CF	
GR7	Color Don’t Care	7	3CF	
GR8	Bit Mask	8	3CF	

6. REGISTER INFORMATION *(cont.)*

VGA Attribute Controller Registers

Abbreviation	Register Name	Index	Port	Page
ARX	Attribute Controller Index	–	3C0/3C1	
AR0-ARF	Attribute Controller Palette	0:F	3C0/3C1	
AR10	Attribute Controller Mode Control	10	3C0/3C1	
AR11	Overscan (Border) Color	11	3C0/3C1	
AR12	Color Plane Enable	12	3C0/3C1	
AR13	Pixel Panning	13	3C0/3C1	
AR14	Color Select	14	3C0/3C1	

NOTES:

1) VGA Attribute Controller data registers (AR0—ARF and AR10—AR14) are read from port 3C1 and written to port 3C0.

2) After initialization, I/O writes to 3C0 toggle between the Attribute Controller Index Register (ARX) and the VGA Attribute Controller data registers.

CL-GD62XX Extension Registers

Abbreviation	Register Name	Index	Port	Page
SR6	Unlock ALL Extensions	6	3C5	56
SR7	Extended Sequencer Mode	7	3C5	57
SR8	Miscellaneous Control	8	3C5	58
SR9	Scratch-Pad 0	9	3C5	60
SRA	Scratch-Pad 1	A	3C5	60
SRB	VCLK0 Numerator	B	3C5	61
SRC	VCLK1 Numerator	C	3C5	61
SRD	VCLK2 Numerator	D	3C5	61
SRE	VCLK3 Numerator	E	3C5	61
SRF	DRAM Control	F	3C5	62
SR10	Graphics Cursor X Position	10	3C5	64
SR11	Graphics Cursor Y Position	11	3C5	65
SR12	Graphics Cursor Attributes	12	3C5	66
SR13	Graphics Cursor Pattern Address Offset	13	3C5	67
SR14	Scratch-Pad 2	14	3C5	60
SR15	Scratch-Pad 3	15	3C5	60
SR16	Miscellaneous Control 2	16	3C5	68
SR19	Scratch-Pad 4	19	3C5	60
SR1A	Miscellaneous Control 3	1A	3C5	69
SR1B	VCLK0 Denominator and Post-Scalar Value	1B	3C5	70
SR1C	VCLK1 Denominator and Post-Scalar Value	1C	3C5	70
SR1D	VCLK2 Denominator and Post-Scalar Value	1D	3C5	70
SR1E	VCLK3 Denominator and Post-Scalar Value	1E	3C5	70
SR1F	Memory Clock Frequency Programming	1F	3C5	71

6. REGISTER INFORMATION *(cont.)*

Abbreviation	Register Name	Index	Port	Page
GR9	Offset Register 0	9	3CF	76
GRA	Offset Register 1	A	3CF	77
GRB	Graphics Controller Mode Extensions	B	3CF	78
CR19	Interlace End	19	3?5	79
CR1A	Interlace Control	1A	3?5	80
CR1B	Extended Display Controls	1B	3?5	82
CR1C	Flat-Panel Interface	1C	3?5	83
CR1D	Flat-Panel Expansion, Centering Locks	1D	3?5	85
CR1E	Flat-Panel Shading	1E	3?5	87
CR1F	Modulation Control	1F	3?5	89
CR20	Power Management	20	3?5	90
CR21	Power-down Timers	21	3?5	92
CR23	FPVCC, FPBACK, SUSPEND Control	23	3?5	93
CR25	Part Status Register	25	3?5	94
CR27	ID Register	27	3?5	95
CR29	Configuration Register	29	3?5	96

The “?” in the Port Address is “B” for Monochrome mode and “D” for Color mode.

LCD Timing Registers

Abbreviation	Register Name	Index	Port	Page
R0X	Horizontal Total for 80-Column Display	1D	3?5	97
R1X	Horizontal Total for 40-Column Display	1D	3?5	98
R2X	LFS Vertical Counter Value Compare (not centered)	1D	3?5	99
R3X	LFS Vertical Counter Value Compare (centered)	1D	3?5	100
R4X	LFS Vertical Counter Value Compare (centered)	1D	3?5	101
R5X	LFS Vertical Counter Value Compare (centered)	1D	3?5	102
R6X	Overflow Bits for LFS Signal Compare	1D	3?5	103
R7X	Panel Signal Control for TFT	1D	3?5	104
R8X	STN Color Panel Data Format	1D	3?5	105
R9X	TFT Panel Data Format	1D	3?5	106
RAX	TFT Panel HSYNC Position Control	1D	3?5	107
RBX	Special Controls for CL-GD6235	1D	3?5	108

6.1 CL-GD62XX Extended-Register Details

NOTE: "Reserved" and "Unused" bits are initialized to '0' at Reset, unless otherwise specified.

6.1.1 SR6: Unlock All CL-GD62XX Register Extensions

I/O Port Address: 3C5

Index: 6

Bit	Description	Access	Reset State
7(MSB)	Unused		
6	Unused		
5	Unused		
4	Lock Bit 4	R/W	'0'
3	Lock Bit 3	R/W	'0'
2	Lock Bit 2	R/W	'0'
1	Lock Bit 1	R/W	'0'
0(LSB)	Lock Bit 0	R/W	'0'

This register is used to enable or disable access to all the Extension Registers.

Bit	Description
7:5	Reserved
4:0	**Extension Register Access Value:** If this field is loaded with 'xxx1x010', it will be read as '00010010' (12h), and the Extension Registers will be enabled for read and write access. If this field is loaded with any other value, it will be read as '00001111' (0Fh), and the Extension Registers will be disabled for read and write access.

6.1.2 SR7: Extended Sequencer Modes

I/O Port Address: 3C5

Index: 7

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Select LCD Panel/CRT Sense	R	MD14
5	Select LCD Panel/CRT Sense	R	MD13
4	Select LCD Panel/CRT Sense	R	MD12
3	Reserved		
2	Reserved		
1	Reserved		
0(LSB)	High-Resolution Color/Packed Pixel	R/W	'0'

Bit	Description
7	Reserved
6:4	**Select LCD Panel/CRT Sense Method:** The state of memory data lines MD[14:12] is latched at system reset and stored in bits [6:4]. The Cirrus-Logic BIOS uses these bits to select an LCD panel class, or these bits may be used for digitally sensing the type of CRT monitor that is attached at boot-up.
3:1	Reserved
0	**Select 256-color Mode and Packed-pixel Addressing:** If this bit is programmed to a '1', the Video Shift Registers are configured so that one character clock is equal to eight pixels. At the same time, true packed-pixel memory addressing is enabled. If this bit is programmed to '0', this mode is "don't care". **NOTE:**With true packed-pixel addressing, consecutive pixels are stored at consecutive addresses. In contrast, with Chain-4 Addressing, consecutive pixels are stored at every fourth address in Display Memory.

6.1.3 SR8: Miscellaneous Control

I/O Port Address: 3C5

Index: 8

Bit	Description	Access	Reset State
7(MSB)	Symmetrical DRAM Addressing	R/W	=DUALCAS*
6	Disable MCS16* for Display Memory	R/W	'0'
5	Reset Standby Timer	R/W	'0'
4	Reset Backlight Timer	R/W	'0'
3	SUSPEND Active Polarity	R/W	'0'
2	SW3 Read	R	=SW3
1	SW2 Read	R	=SW2
0(LSB)	SW1 Read	R	=SW1

Bit	Description
7	**Symmetrical DRAM Addressing:** This bit is used to select symmetrical DRAM addressing for Page mode text on a CRT. This bit must be set to '1' only if using the CL-GD62XX with Dual-WE* DRAMs having 9-bit addressing (symmetrical DRAM), and the CL-GD62XX is to be set for a 132-column text mode on the CRT. The RESET state of this bit is determined by the DUALCAS* Input Select (pin 72). If Dual-CAS* DRAM is selected (that is, pin 72 is connected to VDD), then bit 7 is automatically programmed to '1', and symmetrical addressing is automatically set. To enable asymmetrical Dual-CAS* DRAM, bit 7 must be programmed manually to '0'. If Dual-WE* DRAM is selected (that is, pin 72 is connected to VSS), then bit 7 is automatically programmed to '0', and asymmetrical addressing is automatically set. To enable symmetrical Dual-WE* DRAM, bit 7 must be programmed manually to '1'. For a 256K x 4 DRAM environment, (that is, pin 72 is connected to VSS), then bit 7 is automatically programmed to '0', and asymmetrical addressing is automatically set. However, because all 256K x 4 DRAMs are symmetrical, bit 7 must be programmed manually to '1'.
6	**Disable MEMCS16* for Display Memory:** If this bit is programmed to '1', accesses to Display Memory will not cause MEMCS16* to become active. This prevents interference when two video subsystems are installed (i.e., a portable computer mounted in a docking station). This bit is meaningful only when the CL-GD62XX is installed on an ISA-bus adapter. For all other configurations, it must be programmed to '0'.

6.1.3 SR8: Miscellaneous Control *(cont.)*

Bit	Description
5	**Reset Standby Timer:** This bit is used to reset the internal Standby mode timer, when there is an I/O read to the keyboard controller (port 60h).
4	**Reset Backlight Timer:** This bit is used to reset the internal Backlight timer when there is an I/O read to the keyboard controller (port 60h).
3	**SUSPEND Active Polarity:** This bit is used to select the polarity of the SUSPEND input pin for Suspend mode activation. This bit must be set to match the input state of the SUSPEND input before activating the MCLK & VCLK power-down operation with register CR1C[2]. If this bit is set to a '0', then SUSPEND is active-'high' (reset state). If this bit is set to a '1', then SUSPEND is active-'low'.
2:0	**SW3 - SW1 Read:** These read-only bits reflect the active state of Switch Inputs SW3 - SW1 respectively. These bits are for BIOS use. In a '486 Local-bus system, the SW3 - SW1 pins are redefined as outputs OEH#, BLAST#, and OEL# respectively. Therefore, these bits are not used.

6.1.4 SR9, SRA, SR14, SR15, SR19: Scratch-pad Registers 0-4

I/O Port Address: 3C5

Index: 9, A, 14, 15, 19

Bit	Description	Access	Reset State
7(MSB)	R/W Data [7]	R/W	'0'
6	R/W Data [6]	R/W	'0'
5	R/W Data [5]	R/W	'0'
4	R/W Data [4]	R/W	'0'
3	R/W Data [3]	R/W	'0'
2	R/W Data [2]	R/W	'0'
1	R/W Data [1]	R/W	'0'
0(LSB)	R/W Data [0]	R/W	'0'

These registers are reserved exclusively for the CL-GD62XX BIOS and must never be written by an application program. They are listed here only for completeness.

Bit	Description
7:0	These bits are reserved for the Cirrus Logic Video BIOS.

6.1.5 SRB, SRC, SRD, SRE: VCLK0, 1, 2, 3 Numerator Value

I/O Port Address: 3C5

Index: B, C, D, E

Bit	Description	Access	Reset State
7(MSB)	Reserved		—
6	VCLK Numerator [6]	R/W	Refer to table below
5	VCLK Numerator [5]	R/W	Refer to table below
4	VCLK Numerator [4]	R/W	Refer to table below
3	VCLK Numerator [3]	R/W	Refer to table below
2	VCLK Numerator [2]	R/W	Refer to table below
1	VCLK Numerator [1]	R/W	Refer to table below
0(LSB)	VCLK Numerator [0]	R/W	Refer to table below

These registers, in conjunction with SR1B-SR1E, are used to determine the frequency of video clocks, and are selected by register MISC[2:3].

Bit	Description
7	Reserved
6:0	**VCLK Numerator [6:0]:** The following table shows the frequency loaded in these registers at Reset:

Clock	Freq. (MHz)	N	D	P	Numerator (SRi)		Denominator/Prescalar	
VCLK0	25.180	102	29	1	SRB	66h	SR1B	3Bh
VCLK1	28.325	91	23	1	SRC	5Bh	SR1C	2Fh
VCLK2	41.165	69	24	0	SRD	45h	SR1D	30h
VCLK3	36.082	126	25	1	SRE	7Eh	SR1E	33h

For each Video Clock (VCLK), the frequency is determined with the following expression:

$$\text{VCLKn (MHz)} = \frac{\text{OSC} \times \text{N}}{\text{D} \times [\text{P} + 1]}$$

Where:

OSC = Input Clock, 14.31818 MHz
Numerator = Register Data bits SRi[6:0], i = B, C, D, E
Denominator = Register Data bits SR1i[5:1]
Post-Scalar = Register Data bits SR1i[0]

6.1.6 SRF: DRAM Control

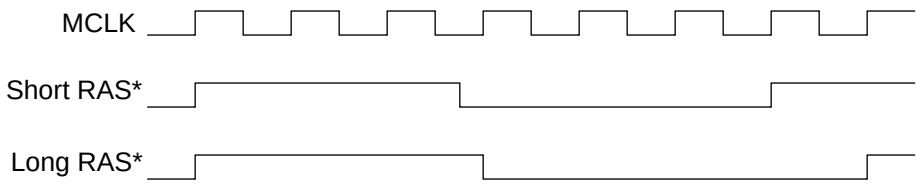
I/O Port Address: 3C5

Index: F

Bit	Description	Access	Reset State
7(MSB)	Extended Frame-Accelerator Enable	R/W	'0'
6	Reserved		
5	CPU Write Buffer Depth Control	R/W	'0'
4	Reserved		
3	Reserved		
2	RAS* Timing Select	R/W	'1'
1	MCLK Frequency Select [1]	R/W	'1'
0(LSB)	MCLK Frequency Select [0]	R/W	'1'

Bit	Description
7	**Extended Frame-Accelerator Enable:** When this bit is '1', the internal refresh mechanism provides only half of the normal refresh cycles; thereby, reducing power in the dual-scan monochrome LCD-only mode.
6	Reserved
5	**CPU Write Buffer Depth Control:** When this bit is programmed to a '0', the CPU Write Buffer depth will be set to one level (16 bits/level), and this is the default. Typically, this setting will be used for standard Video Modes and Extended 16-Color Modes. When this bit is programmed to a '1', the CPU Write Buffer depth will be set to four levels (16 bits/level). This setting should never be used for any Text mode. This bit will typically be used for any Extended 8-bit Pixel Modes. In **Local-bus mode**, this bit has no effect. Depth is always set to one level.
4:3	Reserved
2	**RAS* Timing Select**: When this bit is programmed to '1' (the default), RAS* timing for **short-RAS* DRAMs** is selected. In this mode, the RAS* output (pin 128) is 'high' for 2.5+ MCLK cycles, and 'low' for 3.0+ MCLK cycles, for a total period of six MCLK cycles. When this bit is programmed to '0', RAS* timing for **long-RAS* DRAMs** is selected. In this mode, the RAS* output is 'high' for 3 MCLK cycles, and 'low' for 4 MCLK cycles.

NOTE: The Long-RAS* timing option allows the use of faster MCLKs with DRAMs that have a better CAS* cycle time without violating the RAS* access-time requirements.



6.1.6 SRF: DRAM Control *(cont.)*

Bit	Description
1:0	**MCLK Frequency Select:** These bits select the active memory clock frequency according to the table below. To adjust the frequency, refer to SR1F[5:0].

SRF[1]	SRF[0]	MCLK Frequency
'0'	'0'	50.11 MHz
'0'	'1'	44.74 MHz
'1'	'0'	25.00 MHz
'1'	'1'	37.58 MHz (default at reset)

▼ **CAUTION**: Do not select an MCLK frequency that is slower than the VCLK frequency.

6.1.7 SR10, 30, 50, 70, 90, B0, D0, F0: Graphics Cursor X Position

I/O Port Address: 3C5

Index: 10, 30, 50, 70, 90, B0, D0, F0

Bit	Description	Access	Reset State
7(MSB)	Cursor X [10]	R/W	'0'
6	Cursor X [9]	R/W	'0'
5	Cursor X [8]	R/W	'0'
4	Cursor X [7]	R/W	'0'
3	Cursor X [6]	R/W	'0'
2	Cursor X [5]	R/W	'0'
1	Cursor X [4]	R/W	'0'
0(LSB)	Cursor X [3]	R/W	'0'

This register, and bits [7:5] of the index used to access it, are used to define the horizontal (X) pixel offset of the graphics cursor.

The data forms the upper-eight bits of the 11-bit position; bits [7:5] of the index form the lower-three bits of the 11-bit position. This allows the entire 11-bit cursor offset to be written in a single 16-bit I/O write. The offset must be placed in AX[15:5]; AX[4:0] must be '10000', and DX must be 03C4. If 10, 30, 50...F0 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the ***previously*** stored three bits of the cursor position.

Bit	Description
7:0	**Cursor X [10:3]:** This 8-bit field forms the upper-eight bits of the 11-bit horizontal offset of the graphics cursor. The index used to access this register forms the low-order three bits of the 11-bit offset.

6.1.8 SR11, 31, 51, 71, 91, B1, D1, F1: Graphics Cursor Y Position

I/O Port Address: 3C5

Index: 11, 31, 51, 71, 91, B1, D1, F1

Bit	Description	Access	Reset State
7(MSB)	Cursor Y [10]	R/W	'0'
6	Cursor Y [9]	R/W	'0'
5	Cursor Y [8]	R/W	'0'
4	Cursor Y [7]	R/W	'0'
3	Cursor Y [6]	R/W	'0'
2	Cursor Y [5]	R/W	'0'
1	Cursor Y [4]	R/W	'0'
0(LSB)	Cursor Y [3]	R/W	'0'

This register, and bits [7:5] of the index used to access it, are used to define the vertical (Y) pixel offset of the graphics cursor.

The data forms the upper-eight bits of the 11-bit position; bits [7:5] of the index form the lower-three bits of the 11-bit position. This allows the entire 11-bit cursor offset to be written in a single 16-bit I/O write. The offset must be placed in AX[15-5]; AX[4:0] must be '10000', and DX must be 03C4. If 11, 31, 51...F1 is written to 3C4 without writing to 3C5 (a byte write), then a read of 3C4 will return the ***previously*** stored three bits of the cursor position.

Bit	Description
7:0	**Cursor Y [10:3]:** This 8-bit field forms the upper-eight bits of the 11-bit vertical offset of the graphics cursor. The index used to access this register forms the low-order three bits of the 11-bit offset.

6.1.9 SR12: Graphics Cursor Attributes

I/O Port Address: 3C5

Index: 12

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Allow Access to DAC Extended Colors	R/W	'0'
0(LSB)	Graphics Hardware Cursor Enable	R/W	'0'

Bit — **Description**

7:2 — Reserved

1 — **Allow Access To Dac Extended Colors:** The table below shows the result of programming this bit to either a '0' or a '1':

SR12[1]	Result		
	DAC Lookup Table (LUT) Entry	How Table Entry Is Used	How Accessible
'0'	Entire LUT	Entire LUT is VGA-compatible.	—
'1'	256[a]	Used as hardware cursor background.	Accessible as Location x0h.
	257[a]	Used as hardware cursor foreground.	Accessible as Location xFh.
	258	Provides selected overscan color.	Accessible as Location x2h.

a. Entry 256 & 257, when SR12[1] = '1', provides a cursor that is completely independent of the display data colors

0 — **Graphics Hardware Cursor Enable:** If this bit is set to '1', the graphics hardware cursor will be enabled and will appear on the screen. If this bit is programmed to '0' (the default), the graphics hardware cursor will be disabled and will not appear on the screen.
See SR13[1:0] for cursor pattern select options.

6.1.10 SR13: Graphics Cursor Pattern Address Offset

I/O Port Address: 3C5

Index: 13

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Cursor Pattern Select [1]	R/W	'0'
0(LSB)	Cursor Pattern Select [0]	R/W	'0'

Bit	Description
7:2	Reserved
1:0	**Cursor Pattern Select [1:0]:** When SR12[0] = '1' ', this 2-bit field is used to select one of four possible 32 x 32-bit cursor patterns stored at the top (highest-addressed 8K bytes) of the display memory.

6.1.11 SR16: Miscellaneous Control 2

I/O Port Address: 3C5

Index: 16

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Select Minimum-Delayed READY#	R/W	'0'
4	Timing Adjust for '486 COMMAND	R/W	'0'
3	Reserved		
2	OSC Input Disable in Suspend	W	'0'
1	DRAM Interface-input Threshold Select	W	'0'
0(LSB)	CPU-bus Interface-input Threshold Select	W	'0'

This register is reserved exclusively for the CL-GD62XX BIOS and must never be written by an application program. It is listed here only for completeness.

Bit	Description
7:6	Reserved
5	**Select Minimum-Delayed READY#:** When this bit is set to '0', a minimum READY# (pin32) signal delay for memory cycles is selected. This is the normal setting for this bit. When this bit is set to '1', the READY# output pin is delayed by three wait states. This is for **test mode only** and should not be used in normal operation.
4	**Timing Adjust for '486 COMMAND pin:** This bit should be set to '0' for normal operation. When this bit is set to '1', an additional 1/2 CPU clock delay is selected for the '486 COMMAND pin. This is for **test mode only** and should not be used in normal operation.
3	Reserved
2	**OSC Input Disable During Suspend Mode:** When this bit is '1', the oscillator input pad is disabled during hardware-Suspend mode shutting off internal clocks and their associated power dissipation. This bit should be set to '1' only when an external 32 kHz source (CR1D[4] = '0') is supplied for memory refresh during Suspend mode. When this bit is '0', the oscillator input pad is always enabled.
1	**DRAM Interface-input Threshold Select:** When this bit is '0', the DRAM interface-input thresholds are set for TTL levels. When this bit is '1', the DRAM interface-input thresholds are set for CMOS levels.
0	**CPU-bus Interface-input Threshold Select:** When this bit is '0', the CPU-bus interface-input thresholds are set for TTL levels. When this bit is '1', the CPU-bus interface-input thresholds are set for CMOS levels

6.1.12 SR1A: Dual-Scan Color Control (CL-GD6235 only)

I/O Port Address: 3C5

Index: 1A

Bit	Description	Access	Reset State
7(MSB)	Refresh Select	R/W	'0'
6	Dual-Scan Color STN Select	R/W	'0'
5	Video Mem/CPU Bandwidth	R/W	'0'
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0(LSB)	Reserved		

The SR1A[7:5] bits of this register are user programmable for the CL-GD6235 only. For the CL-GD6205/'15/'25, this register is reserved exclusively for the BIOS, and must never be written by an application program.

Bit	Description
7	**Refresh Per Line Select:** When this bit is set to '1', one refresh cycle per scanline is selected (for CL-GD6235 only). When this bit is set to '0' (default), register CR11[5] selects three or five refresh cycles per scanline.
6	**Dual-Scan Color STN Select**: When this bit is set to '1', Dual-scan Color STN mode is selected (for CL-GD6235 only). Also, register CR1C[7:6] must be programmed to '10' to select Color STN panels. This register is "Reserved" on CL-GD6205/'15/'25 devices.
5	**Video Memory/CPU Bandwidth Allocation**: When this bit is set to '1', the CPU has more access to the memory bus by reducing the FIFO latency (for CL-GD6235 only). When set to '0', the CPU access uses normal FIFO latency.
4:0	Reserved.

6.1.13 SR1B, SR1C, SR1D, SR1E: VCLK0, 1, 2, 3 Denominator and Post Scalar Value

I/O Port Address: 3C5

Index: 1B, 1C, 1D, 1E

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	VCLK Denominator [4]	R/W	'0'
4	VCLK Denominator [3]	R/W	'0'
3	VCLK Denominator [2]	R/W	'0'
2	VCLK Denominator [1]	R/W	'0'
1	VCLK Denominator [0]	R/W	'0'
0(LSB)	VCLK Post Scalar	R/W	'0'

This register, in conjunction with SRB, is used to determine the frequency of Video Clock 0 (VCLK0). The reset values for these four registers are shown in the VCLK Numerator Table in Section 6.1.5.

Bit	Description
7:6	Reserved
5:1	**VCLK Denominator [4:0]** The following table shows an example of the frequency loaded into these registers at Reset:

Clock	Freq. (MHz)	N	D	P	Numerator		Denominator/ Prescalar	
VCLK0	25.180	102	29	1	SRB	66h	SR1B	3Bh
VCLK1	28.325	91	23	1	SRC	5Bh	SR1C	2Fh
VCLK2	41.165	69	24	0	SRD	45h	SR1D	30h
VCLK3	36.082	126	25	1	SRE	7Eh	SR1E	33h

0	**VCLK Post Scalar:** Defines a divide-by-one or divide-by-two operator in the denominator.

The 7-bit numerator (N), 5-bit denominator (D), and 1-bit post scalar (P) for each video clock (VCLK) determines its frequency according to the following expression:

$$\textbf{VCLKn (MHz)} = \frac{\textbf{OSC x N}}{\textbf{D x [P + 1]}}$$

Where:

OSC = Input Clock, 14.31818 MHz
N = Register Data bits SRi(6:0), i = B, C, D, E
D = Register Data bits SR1i(5:1)
P = Register Data bits SR1i(0)

6.1.14 SR1F: Memory Clock Frequency Programming

I/O Port Address: 3C5

Index: 1F

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	MCLK Frequency [5]	R/W	(See MCLK Table below)
4	MCLK Frequency [4]	R/W	(See MCLK Table below)
3	MCLK Frequency [3]	R/W	(See MCLK Table below)
2	MCLK Frequency [2]	R/W	(See MCLK Table below)
1	MCLK Frequency [1]	R/W	(See MCLK Table below)
0(LSB)	MCLK Frequency [0]	R/W	(See MCLK Table below)

Bit	Description
7:6	Reserved
5:0	**MCLK Frequency [5:0]:** As indicated in the following equation, this field directly programs an adjustment to the MCLK frequency that was selected with register SRF. **MCLK = (Reference Frequency ÷ 8) x SR1F[5:0]** This field may be programmed with any value from 21 to 28 (decimal) or 15 to 1C (hex).

The MCLK table below provides examples with a reference frequency of 14.31818 MHz.

SR1F[5:0] (Decimal)	SR1F[5:0] (Hex)	MCLK Frequency (MHz)
21	15	37.585
23	17	41.165
25	19	44.744
26	1A	46.534
28	1C	50.114

6.1.15 STAT: Input Status Register 1

I/O Port Address: 3?A

Index: 1

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved/Interlaced Field Status	R	'0'
5	Diagnostic 0	R	'0'
4	Diagnostic 1	R	'0'
3	Vertical Retrace	R	'0'
2	Reserved		
1	Reserved		
0(LSB)	Display Enable	R	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7	Reserved
6	**Reserved** in VGA-compatible mode. **Interlaced Field Status:** If Interlaced mode is programmed by setting the CRTC register, CR1A[0] = '1', then this bit reflects the interlaced-frame field number.
5:4	**Diagnostic [1:0]:** These bits follow two of eight outputs of the Attribute Controller. The selection is made according to the Attribute register AR12[5:4] (Color Plane Enable register), as indicated in the following table:

AR12[5]	AR12[4]	STAT[5]	STAT[4]
'0'	'0'	P[2] Red	P[0] Blue
'0'	'1'	P[3] Secondary Blue	P[1] Green
'1'	'0'	P[5] Secondary Red	P[4] Secondary Green
'1'	'1'	P[7]	P[6]

3	**Vertical Retrace:** A '1' indicates that vertical retrace is in progress.
2:1	Reserved
0	**Display Enable:** If this bit is read as a '0', video is being serialized and displayed. If this bit is read as a '1', vertical or horizontal blanking is active.

6.1.16 GR0: Set/Reset Register (CL-GD62XX Extensions)

Bit	*VGA Write Modes 0 or 3*	*CL-GD62XX Extended Write Mode 5*	*Reset State*
7	Set/Reset Map 7	Write Mode 5 — Background Color Bit 7	'0'
6	Set/Reset Map 6	Write Mode 5 — Background Color Bit 6	'0'
5	Set/Reset Map 5	Write Mode 5 — Background Color Bit 5	'0'
4	Set/Reset Map 4	Write Mode 5 — Background Color Bit 4	'0'
3	Set/Reset Map 3	Write Mode 5 — Background Color Bit 3	'0'
2	Set/Reset Map 2	Write Mode 5 — Background Color Bit 2	'0'
1	Set/Reset Map 1	Write Mode 5 — Background Color Bit 1	'0'
0	Set/Reset Map 0	Write Mode 5 — Background Color Bit 0	'0'

The function of these bits is changed from the normal VGA Set/Reset definition. These bits define the **background** color, if the CL-GD62XX Extended Write mode 5 is selected as described in the GR5 and GRB register descriptions

Bit	Description
7:0	**Set/Reset Map for Background Color:** If GRB[2] = '1', then bits [7:4] of this register are read/write. In addition, if GRB[2] = '1', Write modes 0 or 3 use only bits [3:0] of this register, although bits [7:4] are read/write. If GRB[2] = '0', then GR0[7:4] are read only, and set to '0'.

6.1.17 GR1: Enable Set/Reset Register *(CL-GD62XX* Extensions)

Bit	*VGA Write Mode 0*	*CL-GD62XX Extended Write Modes 4 or 5*	*Reset State*
7	Enable Set/Reset Map 7	Write Modes 4/5 — Foreground Color Bit 7	'0'
6	Enable Set/Reset Map 6	Write Modes 4/5 — Foreground Color Bit 6	'0'
5	Enable Set/Reset Map 5	Write Modes 4/5 — Foreground Color Bit 5	'0'
4	Enable Set/Reset Map 4	Write Modes 4/5 — Foreground Color Bit 4	'0'
3	Enable Set/Reset Map 3	Write Modes 4/5 — Foreground Color Bit 3	'0'
2	Enable Set/Reset Map 2	Write Modes 4/5 — Foreground Color Bit 2	'0'
1	Enable Set/Reset Map 1	Write Modes 4/5 — Foreground Color Bit 1	'0'
0	Enable Set/Reset Map 0	Write Modes 4/5 — Foreground Color Bit 0	'0'

The function of these bits is changed from the normal VGA Enable Set/Reset definition. These bits define the **foreground** color, if the CL-GD62XX Extended Write modes 4 or 5 are selected as described in the GR5 and GRB register descriptions.

Bit	Description
7:0	**Set/Reset Map Enable for Foreground Color:** If GRB[2] = '1', then bits [7:4] of this register are read/write. In addition, if GRB[2] = '1', Write mode 0 uses only bits [3:0] of this register, although bits [7:4] are read/write. If GRB[2] = '0', then GR1[7:4] are read only, and set to '0'.

6.1.18 GR5: Mode Register (*CL-GD62XX* Extensions)

I/O Port Address: 3CF

Index: 5

Bit	Description	Mode	Reset State
7(MSB)	Reserved		
6	256-Color Mode (used in all 256-color Modes)	VGA	NA
5	Shift Register Mode	VGA	NA
4	Odd/Even	VGA	NA
3	Read Type	VGA	NA
2	Extended Write Mode Bit [2]	CL-GD62XX	NA
1	Write Mode Bit [1]	VGA	NA
0(LSB)	Write Mode Bit [0]	VGA	NA

Bit	Description
7	Reserved
6:3	These are normal VGA functions and are not explained here.
2	**Extended Write Mode Select Bit [2:** When GRB[2] = '1', then this is a third Write mode Select Bit, in conjunction with Write mode bits[1] and [0], GR5[1:0]. Clearing GRB[2] to '0' directly clears GR5[2] to '0', and makes it read only.
1:0	**Write Mode Select Bits[1:0]:** When GRB[2] = '0' and GR5[2] = '0', these bits select standard VGA Write Modes 3 through 0. When GRB[2] = '1' and GR5[2] = '1', these two bits select Extended Write Modes 4 and 5 (explained below). Extended Write Modes 6 and 7 are not implemented.

The CL-GD62XX ***Extended Write Modes*** operate on eight pixels at a time in 256-color Graphics Modes, with packed-pixel addressing. They can be used for text write, line draw, or pattern fills. Both Modes 4 and 5 should be used with x8 Addressing selected, GRB[1] = '1'.

Extended Write Mode 4: 256-Color Text Write Mode — Preserve Background

If the CPU Data Bit is '1', then the Graphics Controller Enable Set/Reset register (GR1) 8-bit value is the foreground color selected. If the CPU Data Bit is a '0', then that pixel is not changed by the write.

The Enable Set/Reset register GR1 is normally four bits; to extend it to eight bits, set GRB[2] to '1'.

The Sequencer Map Mask register (SR2) is also normally four bits. To extended it to eight bits, set GRB[2] to '1'. However, in 8-bit mode, it inhibits writes.

Extended Write Mode 5: 256-Color Text Write Mode — Foreground/Background

Write mode 5 is similar to Write mode 4, except that the Graphics Controller Set/Reset register (GR0) 8-bit value is used as the background color to be written to the pixels selected when CPU Data = 0.

The Set/Reset register GR0 is normally four bits; to extend it to eight bits, set GRB[2] to '1'.

The Sequencer Map Mask register (SMMR) is also normally four bits. To extend it to eight bits, set GRB[2] to '1'. When SMMR is extended to eight bits, it is used to inhibit writes to selected pixels.

6.1.19 GR9: Offset Register 0

I/O Port Address: 3CF

Index: 9

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Offset 0 [6]	R/W	'0'
5	Offset 0 [5]	R/W	'0'
4	Offset 0 [4]	R/W	'0'
3	Offset 0 [3]	R/W	'0'
2	Offset 0 [2]	R/W	'0'
1	Offset 0 [1]	R/W	'0'
0(LSB)	Offset 0 [0]	R/W	'0'

This register provides access for up to 512K bytes of Display Memory with 4K-byte granularity. The contents of this register are added to SA[18:12] when GRB[0] = '0', or when GRB[0] = '1' and address bit SA15 = '0'.

Bit	Description
7	Reserved
6:0	**Offset Register 0 [6:0]:** This value is added to SA[18:12] to provide the address into Display Memory. This Offset register is selected when GRB[0] = '0', or when GRB[0] = '1', and SA15 = '0'.

The Display Memory Address, prior to being modified by address wrap controls, is called XMA. It is the sum of XA and an Offset register. XA is the address on the bus with bits 16 and 15 possibly forced to a '0', as indicated in the following table:

Configuration	XA[16]	XA[15]	XA[14:0]
128K Memory: GR6[3:2] = '00'	SA[16]	SA[15]	SA[14:0]
64K Memory: GR6[3:2] = '01' ***and*** Offset 1 Disabled: GRB[0] = '0'	'0'	SA[15]	SA[14:0]
64K Memory: GR6[3:2] = '01' ***or*** Offset 1 Enabled: GRB[0] = '1'	'0'	'0'	SA[14:0]

The XA address is summed with the contents of an Offset register with one relative alignment according to the configuration. This is indicated in the mapping that follows:

Table 6-1: 512K-byte Memory with 4K-byte Granularity and VGA Mapping

'0'	'0'	XA[16]	XA[15]	SA[14]	SA[13]	SA[12]
OFF[6]	OFF[5]	OFF[4]	OFF[3]	OFF[2]	OFF[1]	OFF[0]

XMA[18]	XMA[17]	XMA[16]	XMA[15]	XMA[14]	XMA[13]	XMA[12]

6.1.20 GRA: Offset Register 1

I/O Port Address: 3CF

Index: A

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Offset 1 [6]	R/W	'0'
5	Offset 1 [5]	R/W	'0'
4	Offset 1 [4]	R/W	'0'
3	Offset 1 [3]	R/W	'0'
2	Offset 1 [2]	R/W	'0'
1	Offset 1 [1]	R/W	'0'
0(LSB)	Offset 1 [0]	R/W	'0'

This register is used to provide access to up to 512K bytes of Display Memory with 4K-byte granularity. The contents of this register are added to A[18:12] when Extension register GRB[0] = '1' and SA[15] = '1'.

Bit	Description
7	Reserved
6:0	**Offset Register 1:** This value is added to A[18:12] to provide the address into Display Memory. This Offset register is selected when GRB[0] = '1', and SA[15] = '1'. If GRB[0] = '0', this register is unused.

6.1.21 GRB: Graphics Controller Mode Extensions

I/O Port Address: 3CF

Index: B

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Enable Eight-Byte Data Latches	R/W	'0'
2	Enable Extended Write Modes	R/W	'0'
1	Enable x8 Addressing	R/W	'0'
0(LSB)	Enable Offset Register 1	R/W	'0'

Bit	Description
7:4	Reserved
3	**Enable Eight-byte Data Latches:** If this bit is '1', the display memory latches are eight bytes wide, rather than the normal four. Write mode 1 is selected by writing '01' to the Graphics mode register 5, GR5[1:0]. If this bit is '0' and x8 Addressing is not selected (GRB[1] = '0'), then Write mode 1 moves four latched pixels from Display Memory, as in the normal VGA operation.
2	**Enable Extended Write Modes:** If this bit is '1', the CL-GD62XX will execute Extended mode write. In particular: • **8-Byte Transfer Enabled:** Up to eight bytes (eight pixels) can be written into display memory for each CPU byte transferred. • **GR5[2] Enabled:** Extended Write modes 4 and 5 can be enabled • **GR0 Extended:** Register GR0 is extended from four bits to eight bits • **GR1 Extended:** Register GR1 is extended from four bits to eight bits • **SR2 Extended:** Register SR2 is extended from four bits to eight bits
1	**Enable X8 Addressing:** When this bit is '1', the system address is shifted by three relative to true packed-pixel addressing, so that each system-byte address points to a different 8-pixel (8-byte) block in display memory. When this bit is '0', normal addressing is used.
0	**Enable Offset Register 1:** When this bit is '1', then SA[15] will be used to choose between Offset register 0 (GR9) and Offset register 1 (GRA). When this bit is '0', then Offset register 0 (GR9) will always be chosen, regardless of the value of SA[15]. This bit must be set to '0' for 1-Mbyte linear addressing.

6.1.22 CR19: Interlace End

I/O Port Address: 3?5

Index: 19

Bit	Description	Access	Reset State
7(MSB)	Interlace End [7]	R/W	'0'
6	Interlace End [6]	R/W	'0'
5	Interlace End [5]	R/W	'0'
4	Interlace End [4]	R/W	'0'
3	Interlace End [3]	R/W	'0'
2	Interlace End [2]	R/W	'0'
1	Interlace End [1]	R/W	'0'
0(LSB)	Interlace End [0]	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This register specifies the ending horizontal character count for the Odd Field VSYNC.

Bit	Description
7:0	**Interlace End [7:0]:** This value is the number of characters in the last scanline of the odd field in interlaced timing. This can be adjusted to center the scanlines in the odd field halfway between scanlines in the even field. This register is typically programmed to approximately half the horizontal total**.**

6.1.23 CR1A: Interlace Control

I/O Port Address: 3?5

Index: 1A

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Enable Double-Buffered Display Start Address	R/W	'0'
0(LSB)	Enable Interlaced	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7:2	Reserved
1	**Enable Double-Buffered Display Start Address:** If this bit is programmed to a '1', the Display Start address will be updated on the VSYNC following a write to Start Address Low. This provides control of display-frame switching without the need to explicitly monitor VSYNC.
0	**Enable Interlaced**: If this bit is programmed to a '1', interlaced timing is enabled (i.e., interlaced sync in Text mode, and interlaced sync and video data in Graphics mode). In addition, IRQ requests are generated only at the end of odd fields, i.e., at the end of a frame. For interlaced sync and data in Graphics mode, the CRTC Scan Double (CR9[7]) must be set to '0'. Graphics modes 4 and 6 must always be non-interlaced.

6.1.24 CR1B: Extended Display Controls

I/O Port Address: 3?5

Index: 1B

Bit	Description	Access	Reset State
7(MSB)	Disable Text Cursor Blink	R/W	'0'
6	Enable Text Mode Fast-Page	R/W	'0'
5	Blanking Control	R/W	'0'
4	Reserved		
3	Reserved		
2	Reserved		
1	Enable Extended Address Wrap	R/W	'0'
0(LSB)	Extended Display Start Address Bit 16	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7	**Disable Text Cursor Blink:** Setting this bit to '1' disables the text cursor blink.
6	**Enable Text Mode Fast-Page**: If this bit is set to '0', all font-fetch cycles occur as random-read cycles. This bit must be set to '0' for standard VGA dual-font operation. If this bit is set to '1', Fast-page mode cycles will be used to fetch font data. This allows for text modes with a VCLK greater than 30 MHz, as is required for 132-column modes. (See Section 6.1.48 at the end of this chapter for more details).
5	**Blanking Control:** If this bit is set to '0', the DAC blanking will be controlled by the blanking signal generated by the CRTC. In this case, the border can be used (register AR11). If this bit is set to '1', the DAC blanking will be controlled by Display Enable. The DAC will be blanked during the time when the border is normally displayed.
4:2	Reserved

Continued on next page.

6.1.24 R1B: Extended Display Controls *(cont.)*

Bit	Description
1	**Enable Extended Address Wrap:** If this bit is set to '0', the display memory address wraps at 64K maps (256K total memory). This provides VGA compatibility. Also, the CRT Controller Character Address Counter is 16 bits wide; this also assures compatibility. Even with 512K memory installed, the counter does not access the second 256K bytes. If this bit is set to a '1', the counter is 17 bits. Also, the display memory address wraps at the total available memory size. In particular, this bit provides the following functions: a If this bit is '1' and Chain-4 Addressing is selected, SR4[3] = '1', then DRAM addresses A[0] and A[1], normally supplied by CPU addresses XMA[14] and XMA[15], are supplied by addresses XMA[16] and XMA[17]. The XMA[18:12] addresses are the sum of XA(16:12) and an Offset register. Refer to the description of register bit GRB[0] for definitions of XMA[18:12] and XA[16:12]. b If this bit is set to a '1' and CRT Controller Double Word Addressing is selected, R14[6] = '1', then DRAM Addresses A[0] and A[1] — normally supplied by CRTC Character Counter Addresses CA[12] and CA[13] — are supplied by addresses CA[14] and CA[15]. This provides four displayable pages in mode 13h. With four DRAMs installed, Character Counter address CA[16] is added, allowing an 128K-byte displayable page.
0	**Extended Display Start Address Bit 16:** This is Bit 16 of the Extended-display Start address.

6.1.25 CR1C: Flat-Panel Interface

I/O Port Address: 3?5

Index: 1C

Bit	Description	Access	Reset State
7(MSB)	LCD Flat Panel Class Select [1]	R/W	'0'
6	LCD Flat Panel Class Select [0]	R/W	'0'
5	Enable Extra LLCLK	R/W	'0'
4	Reserved	–	
3	Protect CRTC Registers for LCD	R/W	'0'
2	MCLK Suspend Mode Power-Down	R/W	'0'
1	Invert LLCLK Control	R/W	'0'
0(LSB)	Invert LFS Control	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit **Description**

7:6 **LCD Flat Panel Class Select [1:0]:** These two bits select the class of LCD flat panel to be connected. The following table lists available choices:

Bit [7]	Bit [6]	Panel Class Selected
'0'	'0'	Single or Dual-Scan/Dual-Data monochrome panels. R8x = '0' for Dual Scan R8x = '1' for Single Scan UD[3:0] and LD[3:0] = two sets of four shaded pixels with frame modulation
'0'	'1'	Grayscale plasma and electro-luminescent panels. LD[3:0] = 4-bit unshaded video data
'1'	'0'	STN color panels[a]. (CL-GD6225 and CL-GD6235 only)
'1'	'1'	TFT-color panels.

a. See SR1A[6] for CL-GD6235 Dual-Scan enable for STN color panels.

5 **Enable Extra LLCLK:** This bit enables one extra LLCLK for LCD monochrome panels that require 242 line clocks for the upper panel.

4 Reserved

Continued on next page.

6.1.25 CR1C: Flat-Panel Interface *(cont.)*

Bit	Description
3	**Protect CRTC Registers for LCD:** If this bit is set to '1', certain CRTC Registers are protected for LCD panel timing. For LCD operation, some of the CRTC Registers need to be write-protected, that is, the last data bits written are used for CRTC timing control, and a Read/Write 'Shadow' register is enabled for any subsequent I/O. **CRTC Registers that are protected are as follows:** CR6: [7:0], Vertical Total (protected value is used) CR7: [7, 5, 2, 0], Vertical Overflow bits for total and sync start CR10: [7:0], Vertical Retrace Start (protected value used for CRT Vsync) CR11: [7:0], Vertical Retrace End (protected value used for CRT Vsync) CR15: [7:0], Vertical Blanking Start CR16: [7:0], Vertical Blanking End
2	**MCLK Suspend Mode Power Down:** If this bit = '0', the MCLK and VCLK voltage-controlled oscillators (VCOs) will **not** power down in Suspend mode. If this bit = '1', the MCLK and VCLK VCOs will power down in hardware-Suspend mode, but not in software-Suspend mode. If this bit is '0', then the SUSPEND input will force LCD and Backlight power-down sequencing, but CPU access is still allowed, and the CRT outputs remain active. This mode is actually a 'cover-closed' condition that turns off only the LCD display. If this bit = '1', and CR20[3] = '0', then hardware-Suspend mode, using the SUSPEND input pin, will power down both the MCLK and VCLK VCOs, and access by the CPU will not be allowed. Software-Suspend mode (CR20[3] = '1') will force LCD and Backlight power-down sequencing, but CPU access is still allowed.
1	**Invert LLCLK Control:** Setting this bit to '1' inverts the LLCLK signal.
0	**Invert LFS Control:** Setting this bit to '1' inverts the LFS signal.

6.1.26 CR1D: Flat-Panel Display Controls

I/O Port Address: 3?5

Index: 1D

Bit	Description	Access	Reset State
7(MSB)	Enable LCD Timing Registers	R/W	'0'
6	Enable ACTi to Reset Standby	R/W	'0'
5	Enable VGA Access to Reset Standby	R/W	'0'
4	Suspend Mode Clock Source	R/W	'0'
3	Enable ACTi to Reset Backlight	R/W	'0'
2	Enable VGA Access to Reset Backlight	R/W	'0'
1	Enable Auto-expand	R/W	'0'
0(LSB)	Enable Auto-center	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7	**Enable LCD Timing Registers:** This bit acts as an extra CRTC Index bit. When this bit is '1', it enables read/write of the hidden LCD Timing Registers, R0X through RBX, which are mapped at the standard CRTC locations. These special registers are used to control LLCLK, LFS, and other LCD panel control signals.
6	**Enable ACTi to Reset Standby Timer:** When this bit is set to '1', activity on the ACTi input will reset the internal Standby timer.
5	**Enable VGA Access to Reset Standby Timer:** When this bit is set to '1', any valid VGA memory access will reset the internal Standby timer.
4	**Suspend Mode Clock Source**: This bit selects the source for the clock used during Suspend mode. If this bit is set to '0', a 32-kHz clock is expected on the 32kHz pin. If this bit is set to '1', the 14-MHz clock, required on the Input OSC, will be divided by 432 to derive the 32-kHz clock.
3	**Enable ACTi to Reset Backlight Timer:** When this bit is set to '1', activity on the ACTi input will reset the Backlight control timer for the LCD.
2	**Enable VGA Access to Reset Backlight Timer:** When this bit is set to '1', any valid VGA memory access will reset the Backlight control timer for the LCD.

Continued on next page

6.1.26 CR1D: Flat-Panel Display Controls *(cont.)*

Bit	Description
1	**Enable Auto-Expand:** The automatic vertical expansion feature is controlled by the programming of the two sync polarity bits in Port 3C2[7:6] '00' = Reserved (defaults to 480 lines, no vertical expansion) '01' = 400-line/200-line modes (400-line mode is for text only. 200-line mode is for double-scanned graphics only.) '10' = 350-line modes (text or graphics) '11' = 480-line mode (graphics only, no vertical expansion) ***Expansion Method for Graphics Modes:*** **200 lines:** a pattern of 2,2,3,2,2,3,2,3 (double-scan and triple-scan) expands 200 lines to 475 lines by expanding every 8 lines to 19. **350 lines:** a pattern of 1,1,2,1,1,2,1,2,1,1,2,1,1,2 (single-scan and double-scan) expands 350 lines to 475 lines by expanding every 14 lines to 19. ***Expansion Method for Text Modes:*** **200 line, 8 x 8 font**: normal double-scan is applied, and an extra top line and two extra bottom lines are added to each character row (only if Max Row Scan is set for 7). **350 line, 8 x 14 font**: an extra two top lines and three extra bottom lines are added to each character row (only if Max Row Scan is set for 14 lines). **400 line, 8 x 16 font:** an extra top line and two extra bottom lines are added to each character row (only if Max Row Scan is set for 16 lines).
0	**Enable Auto-Center:** Setting this bit to '1' shifts LCD centering, if the auto-expand bit CR1D[1] = '0' (based on sync polarities). This uses the alternate LFS (Line-Frame Store) timing as programmed in LCD Timing registers R2X, R3X, R4X, R5X and R6X.

6.1.27 CR1E: Flat-Panel Shading

I/O Port Address: 3?5

Index: 1E

Bit	Description	Access	Reset State
7(MSB)	Shade Mapping [1]	R/W	'0'
6	Shade Mapping [0]	R/W	'0'
5	Reverse Video for Text Modes	R/W	'0'
4	Reverse Video for Graphics Modes	R/W	'0'
3	Maximum-generated Grayshades [1]	R/W	'0'
2	Maximum-generated Grayshades [0]	R/W	'0'
1	Contrast Enhancement	R/W	'0'
0(LSB)	Enable Planer Graphics Mode Dithering	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit **Description**

7:6 **Shade Mapping [1:0]:** These two bits are used to program monochrome gray-scale mapping (shading) according to the following table:

Bit[7]	Bit[6]	Shade Map
'0'	'0'	18-bit output of LUT converted to 64 shades, with NTSC weighting
'0'	'1'	Green output of LUT only; 6-bit output converted to 64 shades
'1'	'0'	Direct display pixel data (4 bit planer, or lower 6-of-8 bits packed) to 16 or 64 shades
'1'	'1'	6-bit output of Attribute Controller converted to 64 shades

5 **Reverse Video for Text Modes:** If this bit is set to '1', all Text Modes are displayed in reverse video.

4 **Reverse Videofor Graphics Modes:** If this bit is set to '1', all Graphics Modes are displayed in reverse video.

3:2 **Maximum-Generated Grayshades [1:0]:** With these two bits, grayshades are generated according to the following tables:

CR1C[7:6] = '00' — Monochrome Grayshades			
CR1E[3]	**CR1E[2]**	**Number of Shades for Monochrome**	
'0'	'0'	16	16 frame with no dithering
'0'	'1'	64	4 frame x 16 dithering[a]
'1'	'0'	64	8 frame x 8 dithering[a]
'1'	'1'	64	16 frame x 4 dithering

a. Must set CR1E[1] = '1' and R8X[7] = '1'.

6.1.27 CR1E: Flat-Panel Shading *(cont.)*

Bit **Description**

3:2*(cont.)* **Maximum Generated Grayshades:**

CR1C[7:6] = '10' — STN Color			
CR1E[3]	**CR1E[2]**	**Number of Colors per Gun**	
'0'	'0'	16	16 frame modulation only (4096 colors)
'0'	'1'	64	4 frame x 16 dithering (64-text, 256K-graphics)
'1'	'0'	64	8 frame x 8 dithering (512-text, 256K-graphics)
'1'	'1'	64	16 frame x 4 dithering (4096-text, 256K-graphics)

1 **Contrast Enhancement:** This bit is used along with R8X[4] to enable text-mode contrast enhancement.

CR1E[1]	R8X[4]	Enhancement Characteristics
'0'	'0'	No enhancement
'0'	'1'	Foreground only enhancement If BG > FG then BGC = BG; FGC = '0' If BG < FG then BGC = BG; FGC = '1'
'1'	'0'	Contrast enhancement If BG > FG then BGC = BG; FGC = '0' If BG< FG then BGC = '0'; FGC = FG

BG = Background, FG = Foreground, xxC = Color

0 **Enable Planar Graphics Mode Dithering**: This bit is set to '0' to disable dithering in non-packed pixel graphics mode.

6.1.28 CR1F: Flat Panel Modulation Control

I/O Port Address: 3?5

Index: 1F

Bit	Description	Access	Reset State
7(MSB)	Internal / External Modulation Control	R/W	'0'
6	MOD or Retrace LLCLK Control [6]	R/W	'0'
5	MOD or Retrace LLCLK Control [5]	R/W	'0'
4	MOD or Retrace LLCLK Control [4]	R/W	'0'
3	MOD or Retrace LLCLK Control [3]	R/W	'0'
2	MOD or Retrace LLCLK Control [2]	R/W	'0'
1	MOD or Retrace LLCLK Control [1]	R/W	'0'
0(LSB)	MOD or Retrace LLCLK Control [0]	R/W	'0'

NOTES: 1) The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.
2) A value ***must*** be programmed into this register.

This register is used to control the characteristics of the Modulation (MOD) signal for the flat panel. This function is useful for those dual-scan flat panels that generate the MOD signal based on the number of LLCLKs that appear during retrace on the lower half of the panel. When using single-scan panels, using these bits will increase the line clock count for the entire panel.

Bit	Description
7	**Internal or External Modulation Control:** This bit controls the source of the Modulation Signal (MOD) for the flat panel. If this bit = '0', the External Modulation signal is selected for the flat panel. In this case, bits [6:0] can select up to 128 scanlines before the MOD signal changes polarity. If this bit = '1', internal modulation signal is provided through the MOD pin to the flat panel. In this case, the total number of LLCLKs is determined by this register (see bits [6:0] below).
6:0	**MOD or Retrace Line Clock (LLCLK) Control**: If bit 7 = '0', then bits [6:0] can select up to 128 scanlines before the MOD signal changes polarity. If bit 7 = '1', the total number of LLCLKs is determined by adding the content of bits [6:0] of this register to 180h (or 384 decimal). LLCLK = 180h + value(bits[6:0])h

6.1.29 CR20: Power Management Register

I/O Port Address: 3?5

Index: 20

Bit	Description	Access	Reset State
7(MSB)	Enable STANDBY	R/W	'0'
6	CRT Enable	R/W	'0'
5	LCD Enable	R/W	'0'
4	Activate Standby Mode	R/W	'0'
3	Activate Suspend Mode	R/W	'0'
2	Refresh Select [1]	R/W	'0'
1	Refresh Select [0]	R/W	'0'
0(LSB)	Text Mode Shading Control	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7	**Enable STANDBY:** When this bit is set to '1', the STANDBY I/O pin becomes an **output** used to indicate the status of Standby mode. STANDBY is 'high', when the CL-GD62XX is in Standby mode. When this bit is '0', the STANDBY pin is an input that, when 'high', initiates the Standby mode.
6	**CRT Enable**: Setting this bit to '1' enables the analog output from the video DAC.
5	**LCD ENABLE:** This bit must be set to '1', to enable the LCD Interface. Unlike the Standby mode, when the LCD is disabled, VCLK is still running and normal high-power operation is in effect. Transitions of this bit will cause the panel power-up ('low'-to-'high') and power-down ('high'-to-'low') sequence to occur starting from VCLK or up to the point of VCLK shutdown. That is, the panel BIAS, backlight, logic supply, and drive signals will be enabled or disabled. When this bit = '1', the Line Frame Signal (LFS) and LCD Line Clock (LLCLK) LCD Timing signals for monochrome panels are generated. These bits are generated from the LCD Timing registers, R0X through RBX. For TFT-color panels, the CRTC-programmed sync timing is used. Also, VSYNC and HSYNC signals are sent to the CRT outputs and to the LFS and LLCLK outputs. In addition, when LCD operation is enabled, the Display Enable signal controls the display data. Therefore, border is **not** supported.

6.1.29 CR20: Power Management Register *(cont.)*

Bit	Description
5(cont.)	***When this bit = '1', some of the VGA Register bits are redefined for LCDs as follows:***
	SR1,2,3 VCLK/2: The LCD always gets a shift clock at 1/4 the VCLK rate. This bit selects the horizontally-locked timing for 40- or 80-column Modes (except for mode 13h).
	SR1[0] 8/9-dot characters, 'locked' and set for 8-dots/character.
	AR13: Pixel panning, if SR1[0] ='0', then the effect of AR13[4] is masked, and a value of either '8h' or '0h' is equal to "no shift".
	MISC Output (3C2): CRT Sync polarity will always be negative/negative; sync polarity bits control Vertical Expansion/Vertical Centering.
	NOTE: Clock Selct bits do not need to be locked. The clock programming registers should all be set to produce the same frequency (as required by the LCD).
4	**Activate Standby Mode:** Setting this bit to '1' overrides the current internal Standby timer setting and immediately places the device into Standby mode.
3	**Activate Suspend Mode:** Setting this bit to '1' initiates software Suspend mode. In this mode, the power-down sequence is started to blank the panel; however, the CPU can still access video memory, RAMDAC, and I/O registers. Also, the hardware-Suspend mode, using the SUSPEND input pin, is disabled as long as this bit is '1'. **NOTE**: Hardware-Suspend mode also requires CR1C[2] = '1'.
2:1	**Refresh Select:** The programming of these two bits control the type of refresh applied to the video DRAMs during Suspend mode as follows.

Bit [2]	Bit [1]	Refresh Type
'0'	'0'	8-ms refresh cycle, CAS-before-RAS refresh.
'0'	'1'	64-ms refresh cycle, CAS-before-RAS refresh.
'1'	'0'	Self-refresh.
'1'	'1'	No refresh. All clocks inputs are disabled, and RAS/CAS outputs are 'high'.

0	**Text Mode Shading Control**: If this bit is set to '0', text shades are derived directly from foreground/background data. If this bit is set to '1', text shades are derived in the same way as graphics, that is, by using CR1E[7:6].

6.1.30 CR21: Power-Down Timer Control

I/O Port Address: 3?5

Index: 21

Bit	Description	Access	Reset State
7(MSB)	Timer for Backlight Control (FPBACK) [3]	R/W	'0'
6	Timer for Backlight Control (FPBACK) [2]	R/W	'0'
5	Timer for Backlight Control (FPBACK) [1]	R/W	'0'
4	Timer for Backlight Control (FPBACK) [0]	R/W	'0'
3	Timer for Standby Mode Control [3]	R/W	'0'
2	Timer for Standby Mode Control [2]	R/W	'0'
1	Timer for Standby Mode Control [1]	R/W	'0'
0(LSB)	Timer for Standby Mode Control [0]	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Timers are set in increments of 1-to-15 minutes. A value of '0' disables the timer. For the CL-GD62XX, the timers actually count 64 seconds per minute, minus 32 seconds from the total [i.e., (count * 64sec) - 32sec]. Therefore, a setting of 15 minutes (Fh) will result in an actual time of 15.5 minutes. See table below for typical power-down timer settings.

Bit	Description
7:4	**Timer For Backlight Control (FPBACK) [3:0]:** This is the programmed value for the internal Backlight timer. Seconds = (value • 64) - 32
3:0	**Timer For Standby Mode Control [3:0]:** This is the programmed value for the internal Standby mode timer. Seconds = (value • 64) - 32

Table 6-2: Typical Power-Down Timer Settings

Backlight Control Bits				Hex Code	Actual Seconds Programmed (Seconds)	Approximate Delay Time (Minutes)
[7]	[6]	[5]	[4]			
Standby Control Bits						
[3]	[2]	[1]	[0]			
'0'	'0'	'0'	'0'	0h	disabled	disabled
'0'	'0'	'0'	'1'	1h	32	0.5
'0'	'1'	'0'	'1'	5h	288	4.8
'0'	'1'	'1'	'1'	7h	416	6.9
'1'	'0'	'1'	'0'	Ah	608	10.1
'1'	'1'	'1'	'1'	Fh	928	15.5

6.1.31 CR23: Suspend Mode Input Switch Debounce Timer

I/O Port Address: 3?5

Index: 23

Bit	Description	Access	Reset State
7(MSB)	SUSPEND Input Debounce Timer [3]	R/W	'0'
6	SUSPEND Input Debounce Timer [2]	R/W	'0'
5	SUSPEND Input Debounce Timer [1]	R/W	'0'
4	SUSPEND Input Debounce Timer [0]	R/W	'0'
3	FPBACK Control Override	R/W	'0'
2	FPBACK Output State	R/W	'0'
1	FPVCC Control Override	R/W	'0'
0(LSB)	FPVCC Output State	R/W	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7:4	**SUSPEND Input Debounce Timer [3:0]:** These bits define the number of seconds the SUSPEND input must remain active (either 'high' or 'low' as defined by SR8[3]), and stable, before the device enters Suspend mode. Set for 1.0 to 15 seconds. A '0000' setting disables the debounce function.
3	**FPBACK Control Override**: Setting this bit to '1' overrides the FPBACK Standby mode, and enables CR23[2] to control the output state of FPBACK.
2	**FPBACK Output State:** If CR23[3] = '1', then this bit defines the '1' or '0' output state of FPBACK.
1	**FPVCC Control Override**: Setting this bit to '1' overrides the FPVCC Standby mode, and enables CR23[0] to control the output state of FPVCC.
0	**FPVCC Output State:** If CR23[1] = '1', then this bit defines the '1' or '0' output state of FPVCC."

6.1.32 CR25: CL-GD62XX Part Status Register

I/O Port Address: 3?5

Index: 25

Bit	Description	Access	Reset State
7(MSB)	PSR [7]	R	'0'
6	PSR [6]	R	'0'
5	PSR [5]	R	'0'
4	PSR [4]	R	'0'
3	PSR [3]	R	'0'
2	PSR [2]	R	'0'
1	PSR [1]	R	'0'
0(LSB)	PSR [0]	R	'0'

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This read-only register is used for factory testing and internal tracking. Application programs should not depend on contents read from this register.

Bit	Description
7:0	**Part Status Values:** These bits are used only for factory testing and internal tracking.

6.1.33 CR27: CL-GD62XX Part ID Register

I/O Port Address: 3?5

Index: 27

Bit	Description	Access	Reset State
7(MSB)	Chip ID [3]	R	Refer to table below
6	Chip ID [2]	R	Refer to table below
5	Chip ID [1]	R	Refer to table below
4	Chip ID [0]	R	Refer to table below
3	Static bit	R	'1'
2	Chip Revision Level [2]	R	Revision dependant
1	Chip Revision Level [1]	R	Revision dependant
0(LSB)	Chip Revision Level [0]	R	Revision dependant

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This read-only register will return a value that uniquely identifies the chip.

Bit	Description
7:4	**Chip ID [1:0]:** This 4-bit field contains a value that identifies the chip according to the following table:

Identification Value Bits[7:4]	Chip
'0000'	CL-GD6205
'1000'	CL-GD6215
'1100'	CL-GD6225
'0001'	CL-GD6235

3	Always '1'
2:0	**Chip Revision Level [2:0]:** This 3-bit field contains a value that identifies the revision level of the chip.

6.1.34 CR29: CL-GD62XX Configuration Register

I/O Port Address: 3?5

Index: 27

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Power Up/down Cycling Activity	R	‘0’
4	NPD Input Status	R	‘0’
3	DRAM Type Selected	R	‘0’
2	Local Bus Type 1 Status	R	‘0’
1	Local Bus Type 0 Status	R	‘0’
0	ISA/Local Bus Status	R	‘0’

NOTE: The ‘?’ in the above register address is ‘B’ in Monochrome mode and ‘D’ in Color mode.

This read-only register identifies the configuration of the memory and bus interface selected for the chip.

Bit	Description
7:6	Reserved
5	**Power Up/Down Cycling Activity:** This bit is ‘1’ while the device is going through a power-up or power-down sequence. It can be read in all modes except hardware-Suspend which locks out access to all registers.
4	**NPD Input Status**: This bit is ‘1’ when the NPD pin is ’high’, indicating that the internal Standby and Backlight Power-down timers are disabled.
3	**DRAM Type Selected**: When this bit = ‘0’, the Dual-Write-Enable type DRAMs are selected, when ‘1’, the Dual-CAS type DRAMs are selected.
2	**Local Bus Type 1 (LBT1/SMEMW*) Status**: Defines CPU bus type. See table below.
1	**Local Bus Type 0 (LBT0/REF*) Status**: Defines CPU bus type. See table below.
0	**ISA/Local Bus (BUSCONF*) Status**: Defines CPU bus type. See table below.

Bus Type	BUSCONF* CR29[0]	LBT0/REF* CR29[1]	LBT1/SMEMW* CR29[2]
ISA bus	‘1’	Don’t care	Don’t care
PI bus	‘0’	‘0’	‘0’
‘386SXL	‘0’	‘1’	‘0’
‘386DXL	‘0’	‘0’	‘1’
‘486SX/DX	‘0’	‘1’	‘1’

6.1.35 R0X: LCD Timing Register — Horizontal Total for 80-Column and Mode 13h

I/O Port Address: 3?5

Index: 0 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
6	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
5	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
4	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
3	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
2	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
1	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
0(LSB)	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7:0	**Horizontal Total for 80-Column Display:** When R1X[7] = '1', this register defines the upper eight bits of the horizontal total of an 80-column display. When R1X[7] = '0', this register may be used as a scratch-pad register. This register controls horizontal LCD timing when (SR1[3] = '0' or GR5[6] = '1').

6.1.36 R1X: LCD Timing Register — Horizontal Total Enable and 40-Column Horizontal Total

I/O Port Address: 3?5

Index: 1 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Horizontal Total Enable	R/W	NA—Must be set by BIOS
6	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
5	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
4	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
3	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
2	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
1	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS
0(LSB)	Horizontal Total/Scratch Pad	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7	**Horizontal Total Enable**: When this bit is '1', register R0X[7:0] defines the horizontal total for an 80-column display, and R1X[6:0] defines the horizontal total for a 40-column display. When this bit is '0', registers R0X[7:0] AND R1X[6:0] are scratch-pad registers.
6:0	**Horizontal Total for 40-Column Display:** When R1X[7] = '1', these seven bits define the Horizontal Total of an 40-column display. When R1X[7] = '0', these seven bits may be used as a scratch-pad register. This register controls horizontal LCD timing when SR1[3] = '1' and GR5[6] = '0'.

6.1.37 R2X: LCD Timing — LFS Vertical Counter Value Compare (3C2[7:6] = '11')

I/O Port Address: 3?5

Index: 2 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
6	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
5	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
4	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
3	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
2	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
1	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
0(LSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This register defines the number of lines that data is delayed from the frame start. This is the least-significant eight bits of a 10-bit value. The most-significant two bits are stored in register R6X[7:6].

Bit	Description
7:0	**LFS Vertical Counter Value Compare**: This register is used when 3C2[7:6] = '11', if Automatic Centering is ***not*** selected, CR1D[0] = '1', and Automatic Expand is disabled, CR1D[1] = '0'.

6.1.38 R3X: LCD Timing — LFS Vertical Counter Value Compare (3C2[7:6] = '10')

I/O Port Address: 3?5

Index: 3 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
6	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
5	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
4	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
3	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
2	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
1	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
0(LSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This register defines the number of lines that data is delayed from the frame start. This is the least-significant eight bits of a 10-bit value. The most-significant two bits are stored in register R6X[5:4].

Bit	Description
7:0	**LFS Vertical Counter Value Compare**: This register is used when 3C2[7:6] = '10', if Automatic Centering is selected, CR1D[0] = '1', and Automatic Expand is disabled, CR1D[1] = '0'.

6.1.39 R4X: LCD Timing — LFS Vertical Counter Value Compare (3C2[7:6] = '01')

I/O Port Address: 3?5

Index: 4 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
6	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
5	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
4	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
3	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
2	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
1	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
0(LSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This register defines the number of lines that data is delayed from the frame start. This is the least-significant eight bits of a 10-bit value. The most-significant two bits are stored in register R6X[3:2].

Bit	Description
7:0	**LFS Vertical Counter Value Compare**: This register is used when 3C2[7:6] = '01', if Automatic Centering is selected, CR1D[0] = '1', and Automatic Expand is disabled, CR1D[1] = '0'.

6.1.40 R5X: LCD Timing — LFS Vertical Counter Value Compare (3C2[7:6] = '00')

I/O Port Address: 3?5

Index: 5 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
6	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
5	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
4	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
3	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
2	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
1	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS
0(LSB)	LFS Vert. Counter Value	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This register defines the number of lines that data is delayed from the frame start. This is the least-significant eight bits of a 10-bit value. The most-significant two bits are stored in register R6X[1:0].

Bit	Description
7:0	**LFS Vertical Counter Value Compare**: This is used when 3C2[7:6] = '00', if Automatic Centering is selected, CR1D[0] = '1'; and Automatic Expand is disabled, CR1D[1] = '0'.

6.1.41 R6X: LCD Timing — Overflow (Most-Significant) Bits for LFS Signal Compare

I/O Port Address: 3?5

Index: 6 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	LFS Compare Bit	R/W	NA—Must be set by BIOS
6	LFS Compare Bit	R/W	NA—Must be set by BIOS
5	LFS Compare Bit	R/W	NA—Must be set by BIOS
4	LFS Compare Bit	R/W	NA—Must be set by BIOS
3	LFS Compare Bit	R/W	NA—Must be set by BIOS
2	LFS Compare Bit	R/W	NA—Must be set by BIOS
1	LFS Compare Bit	R/W	NA—Must be set by BIOS
0(LSB)	LFS Compare Bit	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

This register defines the most-significant two bits for the LFS Vertical Counter Value Compare registers.

Bit	Description
7:6	**LFS Compare Data Bits[9:8]**: When 3C2[7:6] = '11', these bits are appended as the most-significant two bits of register R2X creating a 10-bit value.
5:4	**LFS Compare Data Bits[9:8]**: When 3C2[7:6] = '10', these bits are appended as the most-significant two bits of register R3X creating a 10-bit value.
3:2	**LFS Compare Data Bits[9:8]**: When 3C2[7:6] = '01', these bits are appended as the most-significant two bits of register R4X creating a 10-bit value.
1:0	**LFS Compare Data Bits[9:8]**: When 3C2[7:6] = '00', these bits are appended as the most-significant two bits of register R5X creating a 10-bit value.

6.1.42 R7X: LCD Timing — Panel Signal Control for Color TFT Panels

I/O Port Address: 3?5

Index: 7 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	CRT-only in Standby/Suspend	R/W	NA—Must be set by BIOS
6	Reserved		
5	Reserved		
4	Reserved		
3	LFS Output	R/W	NA—Must be set by BIOS
2	LLCLK Output	R/W	NA—Must be set by BIOS
1	FPVDCLK Inversion	R/W	NA—Must be set by BIOS
0(LSB)	FPVDCLK Enable	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7	**CRT-Only Enable for Standby and Suspend Modes:** When this bit is '1', Standby and Suspend modes are only available in CRT-only mode. When this bit is '0', Standby and Suspend modes are only available in LCD-only mode
6:4	Reserved
3	**LFS Output:** When this bit is '0', the LFS output pin drives STN and DE-type TFT panels. When this bit is '1', the LFS output pin drives the VSYNC input for non-DE type TFT panels.
2	**LLCLK Output:** When this bit is '0', the LLCLK output pin drives STN and DE-type TFT panels. When this bit is '1', the LLCLK output pin drives the HSYNC input for non-DE type TFT panels.
1	**FPVDCLK Inversion:** When this bit is '1', the FPVDCLK is inverted, allowing panel data to be latched on the 'low'-to-'high' transition of FPVDCLK. When this bit is '0', panel data is latched on the 'high'-to-'low' transition of FPVDCLK.
0	**FPVDCLK Enable:** When this bit is '0', the FPVDCLK is gated by display enable, and remains active only during display time. When this bit is '1', FPVDCLK is always active (free-running).

6.1.43 R8X: LCD Timing — STN Color Panel Data Format

I/O Port Address: 3?5

Index: 8 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Alternate Gray Shade Mode Select	R/W	NA—Must be set by BIOS
6	Reserved		
5	Dual-Scan/Single-Scan Mono. Select	R/W	NA—Must be set by BIOS
4	Foreground Text Enhancement	R/W	NA—Must be set by BIOS
3	Line-Pulse Width Select	R/W	NA—Must be set by BIOS
2	Reserved		
1	Shift-Clock Select for STN Panels	R/W	NA—Must be set by BIOS
0(LSB)	8-Bit/16-Bit Data Interface Select	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit **Description**

7 **Alternate Gray Scale Mode Select:** When this bit is '1', the "alternate" gray shade mode for monochrome panels is selected. This bit is '0', for normal operation.

6 Reserved

5 **Dual-Scan/Single-Scan Monochrome Panel Select:** When this bit is '0', dual-scan monochrome panels are selected. When this bit is '1', single-scan monochrome panels are selected.

4 **Foreground Text Enhancement:** When this bit is '1', the foreground text enhancement is enabled (see CR1E[1] for details). When this bit is '0', normal text is displayed.

3 **Line-Pulse Width Selection:** When this bit is '1', and R7X[2] = '0', a shortened line-pulse width is selected. When this bit is '0', line-pulse width is controlled by other registers.

R7X[2]	R8X[3]	Line-Pulse Width Option
'0'	'0'	LP width controlled by CR4 and CR5; typical = 3.8 µs
'0'	'1'	300 ns fixed pulse width (color STN panels only)
'1'	'0'	1.2 µs fixed pulse width

2 Reserved

1 **Shift-Clock Select for STN Panels:** When this bit is '0', a single-shift clock is supplied to STN panels, FPVDCLK pin. When this bit is '1', dual-shift clocks are supplied to STN panels, FPVDCLK and DE pins.

0 **Data Interface Select:** When this bit is '0', 16-bit data interface is selected. When this bit is '1', 8-bit data interface is selected, R9X: LCD Timing — TFT Panel Data Format.

6.1.44 R9X: LCD Timing — TFT Panel Data Format

I/O Port Address: 3?5

Index: 9 — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Shift-clock Delay	R/W	NA—Must be set by BIOS
5	Shift-clock Delay	R/W	NA—Must be set by BIOS
4	Shift-clock Delay	R/W	NA—Must be set by BIOS
3	Reserved		
2	Reserved		
1	Data Format	R/W	NA—Must be set by BIOS
0(LSB)	Data Format	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7	Reserved
6:4	**Shift-Clock Delay:** These bits select a 0-to-7 shift(pixel)-clock delay from the internal character clock counter (8 VCLK per Character Clock) to TFT HSYNC (LLCLK) signal. Bit[6] is the MSB. Increasing the value in this register moves the image on the LCD to the left.
3:2	Reserved
1:0	**TFT-Panel Data Format**: These two bits select the data format for the TFT panels as shown in the table below. See the "Panel Interface Tables" section in the CL-GD62XX *Applications Book* for specific panel types and detail connection information.

R9X[1:0]	TFT Panel Data Format
'00'	9-bit (333)
'10'	12-bit (444)
'x1'	18-bit Direct

6.1.45 RAX: LCD Timing — TFT Panel HSYNC Position Control

I/O Port Address: 3?5

Index: A — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS
6	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS
5	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS
4	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS
3	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS
2	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS
1	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS
0(LSB)	TFT Panel HSYNC Counter	R/W	NA—Must be set by BIOS

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7:0	**TFT-Panel HSYNC Position-Control Counter:** This register contains the 8-bit horizontal-counter value for generating the HSYNC output. This register is set in multiples of eight VCLKs (80-column character clocks). Increasing the value in this register moves the image on the LCD to the left.

6.1.46 RBX: LCD Timing — Special Functions for CL-GD6235 Only

I/O Port Address: 3?5

Index: B — This register is only accessible when CR1D[7] = '1'.

Bit	Description	Access	Reset State
7(MSB)	Reserved		
6	Reserved		
5	Reserved		
4	Reserved		
3	Reserved		
2	Reserved		
1	Reserved		
0	Reserved		

NOTE: The '?' in the above register address is 'B' in Monochrome mode and 'D' in Color mode.

Bit	Description
7:0	Reserved

6.2 132-Column Alphanumeric Mode

This Extended Video mode is for the CRT display only. It is selected by setting CR1B[6] to '1'. For a 31.5-kHz HSYNC rate, the Video Dot Clock (VCLK) should be set to 41.164 MHz (registers SRB/C/D/E). The Sequencer is programmed for 8-dot character intervals with a non-divided Dot Clock.

The Character Map(s), SR3[5:0], should be loaded while this mode is selected, because the memory organization of the Character Maps differs from the normal VGA case. Loading the Character Maps requires no special address translation, because the CL-GD62XX re-maps Video Memory automatically, when this mode is selected.

The Character Maps should be loaded by unchained (sequential) addressing, with the CL-GD62XX mapped into System Address Segment A0000 for 64-Kbyte locations, and with the Sequencer Map Mask register, programmed to enable writing to Plane 2. Subsequently, the Sequencer should be programmed for Chain-2 Addressing with Planes 0 and 1 enabled, as is normally the case in an alphanumeric mode.

The 132-column alphanumeric mode does not support the simultaneous display of two different character maps, as determined by character attribute Bit 3 in the normal VGA operation. However, by programming the Sequencer Character Map Select register 3C5, Index 03, bits[2:0] with a Character Map number, one of eight Character Maps can be selected for the entire screen display. The Character Map number represents one 8-Kbyte segment of the total available 64 Kbytes of Character Maps in this mode. Each Character Map number corresponds to an 8-Kbyte offset from the initial System Address segment where the Maps are loaded initially (Map 0 is loaded into A0000-A1FFF, Map 1 into A2000-A3FFF, etc.). Note the functional change of the Character Map Select register bits[2:0] when this mode is selected; the remaining bits[5:3] are not used.

In the 132-column alphanumeric mode, the CL-GD62XX uses both Plane 2 and Plane 3 physical DRAM pages for Character Map storage. However, the Character Maps appear to be loaded into Plane 2 only. The character-generator dot patterns of all lower-128-character codes are re-mapped into Plane 2, and all upper-128-character codes are re-mapped into Plane 3. Only half of each 64-Kbyte physical plane is used, providing a total of eight 8-Kbyte Character Maps.

While using the 132-column alphanumeric mode, the following CRT Controller parameters are recommended:

Data	***Register***
9Fh	Horizontal Total (Index 0)
83h	Horizontal Display Enable End (Index 1)
84h	Start Horizontal Blanking (Index 2)
82h	End Horizontal Blanking (Index 3)
8Ah	Start Horizontal Retrace (Index 4)
9Eh	End Horizontal Retrace (Index 5)
42h	Offset (Index 13H)

6.2.1 Write Buffer and Display FIFO

Video memory data FIFO depth is four 32-bit levels for all text and eight levels for all Graphics Modes. The write buffer may be selected to be either one or four levels deep by 16-bit by SRF Bit D6.

If the Color Don't Care register (GR7) is set to 00h, and Read mode 1 is selected (GR5(3) = 1), then a CPU memory read cycle will still load the internal data latches, but will not have wait states added. This is useful for both 16- and 256-color block moves where the CPU is using Write mode 1 to move data with the data latches and never actually reads any screen data.

6.3 Hardware Cursor

The hardware cursor is used in 16-color Planar and 256-color Packed-pixel modes to provide a pointer for graphical user interfaces. A hardware cursor (mouse pointer) will improve performance, because the screen data will not have to be rewritten when the cursor is moved. Also, it will improve the appearance of the screen by providing a smoothly moving cursor. The cursor is a 32 x 32-pixel array of two planes:

Cursor Plane 0 = Invert plane

Cursor Plane 1 = Opaque plane

Each pixel of the cursor 'floats' over a corresponding pixel of the screen. The Opaque Cursor Plane,

when set to '1', selects the VGA video data or cursor pixel. The cursor is one of two colors; for the internal video DAC the cursor color is supplied by two extra palette locations for foreground and background colors (See Table 6-3, on page 111 and register SR12: Graphics Cursor Attributes on page 66 for explanation).

The Invert Cursor Plane controls the selected video data. When the Invert Bit is a '1' and the Opaque Bit is a '0', the VGA video data D[7:0] is the inversion of the internal video DAC data. The video data is inverted after the effect of any other VGA registers. The Invert Bit controls the Cursor Color ('0' or '1'), when the Opaque Bit is a '1'. The cursor therefore has four possible states for each pixel:

'00' = Transparent

'01' = Inverted VGA video data

'10' = Cursor Color 0

'11' = Cursor Color 1

The cursor position is defined relative to the upper-left corner of the active display screen (border is not included), and sets the upper-left corner of the cursor. The cursor location X is in pixels and Y is in scanlines. The cursor position on the screen is changed only on the VSYNC, following a write to the Y Location register (SEQ Index 11h). The location '00' is the first pixel of the top-active video scanline.

The cursor data is located in the upper 16K of Display Memory at all times (upper 4K in each memory map). There are four possible cursor patterns that are selected by the Cursor Pattern Offset register (SEQ Index 13h). Each cursor pattern is 256 bytes; 64 bytes in each logical memory map. The first 32 bytes of each memory map are Cursor Plane 0, the last 32 bytes are Cursor Plane 1. One byte from each memory map forms the Cursor Plane for each scanline. Map 0 data is displayed first, with bit D[7] being the first pixel. The CPU can write cursor data either in Unchained mode or in Chain-4 mode with true packed-pixel addressing.

In packed-pixel addressing, with Chain-4 addressing selected, the cursor-data write sequence is all of Cursor Plane 0, followed by Cursor Plane 1. For example, if SR13h = 00 (cursor pattern address offset), then the first byte of the first scanline of the Cursor Plane 0 is located at address 1F000h in Map 0 (for 512K).

The Cursor CRT-Controller data-read replaces the DRAM refresh on the active-cursor display lines. The cursor data read is two CAS* Page Reads; one for Cursor Plane 0 and one for Cursor Plane 1. All four Display Memory maps are read. The 17-bit (for 512K of memory) CRT-Controller address is generated as follows:

HCR[17:14] = all '1's

HCR[13:8] = Cursor Pattern Offset Register SR13(5:0)

HCR[7] = Cursor Plane Read Select

6.4 Graphics Hardware Cursor

Table 6-3 provides information for programming the CL-GD62XX extension registers for the graphics hardware cursor.

Table 6-3. Programming the Graphics Hardware Cursor

To:	Program:			
	Index or Extension Register	**I/O Port Address**	**Register Bits**	**Bit Value**
Disable graphics hardware cursor (the default)	SR12	3C5h	[0]	'0'
Enable the graphics hardware cursor	SR12	3C5h	[0]	'1'
Allow access to a graphics palette video DAC color look-up table that is VGA-compatible	SR12	3C5h	[1]	'0'
Allow for a cursor that is completely independent of the display data colors[a]	SR12	3C5h	[1]	'1'
Position the graphics hardware cursor[b] on the screen's horizontal X axis[c]	Indexes: 10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:5]	2047...0
	Corresponding Extension Registers: SR10, 30, 50, 70, 90, B0, D0, F0	3C4h/3C5h	[7:0]	2047...0
Position the graphics hardware cursor[b] on the screen's vertical Y axis[c]	Indexes: 11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:5]	2047...0
	Corresponding Extension Registers: SR11, 31, 51, 71, 91, B1, D1, F1	3C4h/3C5h	[7:0]	2047...0
Select the graphics hardware cursor pattern offset. (Four patterns available.)	SR13	3C5h	[1:0]	'00','01' '10','11'

a. DAC LUT entries 256, 257, and 258 will be accessible as locations x0h, xFh, and x2h respectively.
Entry 256 will be used as the cursor background.
Entry 257 will be used as the cursor foreground.
Entry 258 will be used to provide a selected overscan color.

b. The cursor position is defined relative to the upper-left corner of the active display screen (border is not included), and sets the upper-left corner of the 32 x 32-bit (or 64 x 64-bit in CL-GD6235 only) cursor.

c. The cursor location X is in pixel. The cursor location Y is in scanlines.

7. ELECTRICAL SPECIFICATIONS

7.1 Absolute Maximum Ratings

Ambient temperature under bias ..... 0° to 70° C

Storage temperature.....-65° to 150° C

Voltage on any pin ..... V_{SS} -0.5V to $V_{CC/DD}$ + 0.5V

Operating power dissipation ..... 1.5 Watts

Power supply voltage.....7.0 Volts

Injection current (latch-up testing) .....100 mA

NOTES:

1) System components should be run below the stress ratings shown in the absolute maximum ratings list. If system components are run at ratings at or above these stress ratings, the system components may be permanently damaged.
2) Functional operation at or above any of the conditions indicated in the absolute maximum ratings is not implied.
3) Exposure to absolute maximum rating conditions for extended periods may affect system reliability.

7.2 DC Specifications (Digital)

(VCC = VDD = 5.0V ± 0.25V (or VDD = 3.3V ± 0.3V) TA = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions	Note
V_{DD}	Power Supply Voltage	4.75	5.25	Volts	Normal Operation	
V_{DD}(3.3V)	Power Supply Voltage	3.0	3.6	Volts	Normal Operation	
V_{IL}	Input LOW Voltage (TTL)	0	0.8	Volts	3.0V < V_{DD} < 5.25V	
V_{IH}	Input HIGH Voltage (TTL)	2.0	V_{DD} + 0.5	Volts	3.0V < V_{DD} < 5.25V	
V_{IHC}	Input HIGH Voltage (CMOS)	0.7V_{DD}	V_{DD} + 0.5	Volts	3.0V < V_{DD} < 5.25V	
V_{ILC}	Input LOW Voltage (CMOS)	-0.5	0.3V_{DD}	Volts	3.0V < V_{DD} < 5.25V	
V_{OHC}	Output HIGH Voltage (CMOS)	0.9V_{DD}		Volts	I_{OHC} = -200 µA	
V_{OLC}	Output LOW Voltage (CMOS)		0.1V_{DD}	Volts	I_{OLC} = 3.2 mA	
V_{OL}	Output LOW Voltage		0.4	Volts	I_{OL} = (See Table 7– 0)	1
V_{OH}	Output HIGH Voltage	2.4		Volts	I_{OH} = (See Table 7– 0)	2
I_{CC1}	Power Supply Current		140	mA	CRT only Operation	3
I_{CC2}	Power Supply Current		50	mA	LCD only Operation	3
I_{CC3}	Power Supply Current		1.0	mA	Hdwr. Suspend mode	3
I_{IL}	Input LOW Current		-10	µA	V_{IN} = 0.0V	
I_{IH}	Input HIGH Current		10	µA	V_{IN} = V_{DD}	
I_{OZ}	Output Leakage Current	-10	10	µA	0 < V_{OUT} < V_{DD}	4
C_{IN}	Input Capacitance		10	pF		5
C_{OUT}	Output Capacitance		10	pF		5

NOTES:

1) Data outputs (SD[15:0]) rated at I_{OL} = 12 mA at V_{OL} = 0.4V, will sink I_{OL} = 24 mA at V_{OL} = 0.5V.
2) Data outputs (SD[15:0]) rated at I_{OH} = -3.0 mA at V_{OH} = 2.4V, will source I_{OH} = -15 mA at V_{OH} = 2.0V.
3) V_{CC} = 3.3V; FPVDCLK = 28 MHz; MCLK = 33 MHz.
4) This is a measure of Three-state output leakage current when in High-impedance (High-Z) mode.
5) This is not 100% tested, but is periodically sample tested.

Table 7–0. Output Loading Values

Output Pins	I_{OH} (mA)	I_{OL} (mA)	LOAD (pF)
SD[15:0]	-3.0	8.0	100
IOCHRDY	-3.0	8.0	100
IOCS16*	—	8.0	100
MEMCS16*	—	8.0	100
IRQ	-3.0	8.0	100
SW1, SW3	-3.0	8.0	50
HSYNC	-12	12	50
VSYNC	-12	12	50
SUD[7:0]	-12	12	50
R5, R4	-12	12	50
LD[3:0]	-12	12	50
UD[3:0]	-12	12	50
DE	-12	12	50
FPVDCLK	-12	12	250

Table 7–0. Output Loading Values *(cont.)*

Output Pins	I_{OH} (mA)	I_{OL} (mA)	LOAD (pF)
LLCLK	-12	12	50
LFS	-12	12	50
MOD	-3.0	3.0	20
MA[9:0]	-6.0	6.0	35
MD[15:0]	-6.0	6.0	35
CAS*	-6.0	6.0	35
RAS*	-6.0	6.0	35
OE*	-6.0	6.0	35
WE[1:0]	-6.0	6.0	35
FPVCC	-12	12	35
FPVEE	-12	12	35
FPBACK	-12	12	35
STANDBY	-6.0	6.0	35
EROM*	-6.0	6.0	35

7.3 DC Specifications (Palette DAC)

(V_{CC} = 3.3V ± 0.3V, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
$AV_{DD2,3}$	DAC Supply Voltage	3.00	3.60	Volts	Normal Operation
$I_{DD2,3}$	Analog Supply Current		90	mA	$AV_{DD2,3}$ = 3.6V
I_{REF}[1]	DAC Reference Current	-3	-10	mA	Note 1

NOTE:

1) See the detailed pin description in Section 2.5 for information regarding nominal I_{REF} .

7.4 DC Specifications (Frequency Synthesizer)

(V_{CC} = 3.3V ± 0.3V, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions	Note
$AV_{DD1,4}$	Synthesizer Supply Voltage	3.00	3.60	Volts		
I_{DD1}	Analog Supply Current		tbd[8]	mA	$AV_{DD1,4}$ = 3.6V	

7.5 DAC Characteristics

(V_{CC} = 3.3V ± 0.3V, T_A = 0° to 70° C, unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions	Note
R	Resolution		6	Bits		
I_O	Output Current		30	mA	VO < 1V	
t_D	Analog Output Delay		tbd[8]	ns		1, 2, 3
t_r, t_f	Analog Output Rise/Fall Time		8	ns		2, 3, 4
t_S	Analog Output Settling Time		15	ns		2, 3, 5
t_{SK}	Analog Output Skew		tbd	ns		2, 3, 6
FT	Clock and Data Feed-through		tbd	db		2, 3, 6
DT	DAC-to-DAC Correlation		tbd	%		6, 7
GI	Glitch Impulse		tbd	pV/sec.		2, 3, 6
CT	DAC-to-DAC Crosstalk		tbd	db		2, 3, 4

NOTES:

1) t_D is measured from the 50% point of VCLK to 50% point of full-scale transition.
2) Load is 50 ohms and 30 pF per analog output.
3) I_{REF} = -6.9 mA.
4) t_r and t_f are measured from 10% to 90% full-scale.
5) t_S is measured from 50% of full-scale transition to output remaining within 2% of final value.
6) Outputs loaded identically.
7) About the mid-point of the distribution of the three DACs measured at full-scale output.
8) *tbd* = to be determined.

7.6 AC Specifications

7.6.1 List of Waveforms

Table/Figure **Title** **Page**

Table 7–1. Bus Signal Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_{1a} t_{1b}	MEMCS16* 'low' delay from LA[23:17] valid MEMCS16* 'low' delay from SA[16:15] valid	– –	20 14	ns ns
t_2	IOCS16* 'low' delay from Address	–	25	ns
t_3[b, c]	Address, SBHE* setup time to any command active	5.0	–	ns
t_4	Any command active to IOCHRDY 'low' delay	–	28	ns
t_5	MEMCS16* 'high' delay from address invalid	–	25	ns
t_6	IOWR* pulse width IORD* pulse width SMEMW* pulse width SMEMR* pulse width	40 60 3 3	– – – [d]	ns ns t[e] t[e]
t_7	IOWR* 'high' setup time to any command active SMEMW* 'high' setup time to next SMEMW* 'low'	80 3	– –	ns t[e]
t_8	Address, SBHE* hold time from any command inactive	0	–	ns
t_9	Data valid delay from SMEMW* 'low' Data valid delay from IOWR* 'low'	– –	3 130	t[e] ns
t_{10}	Data hold time from SMEMW* 'high' Data hold time from IOWR* 'high'	10 0	– –	ns ns
t_{11}	Data setup time to IOWR* 'high'	5.0	–	ns
t_{12}	Data delay from IORD*,SMEMR* 'low'	0	60	ns
t_{13}	Data delay from IOCHRDY 'high'	–	15	ns
t_{14}	Data hold time from IORD*, SMEMR* 'high' Data to high-impedance delay from IORD*, SMEMR* 'high'	0 –	– 20	ns ns
t_{15}	AEN 'high' (hold time) from IORD* or IOWR* 'high'	5.0	–	ns
t_{16}	REFRESH* setup time to SMEMR* 'low'	20	–	ns
t_{17}	REFRESH* 'high' (hold time) from SMEMR* 'low'	0	–	ns
t_{18}	IOCHRDY 'low' pulse width	10	–	ns

a. The ISA-bus interface specifications are valid from 0° to 70° C at operating voltages of 3.3 volts ± 0.3 volts and 5 volts ± 0.25 volts.

b. AEN must be 'low' for t_2, t_3, t_6.

c. Command is defined as IORD*, IOWR*, SMEMR*, or SMEMW*.

d. SMEMR* active-pulse width is determined by IOCHRDY.

e. t = MCLK period.

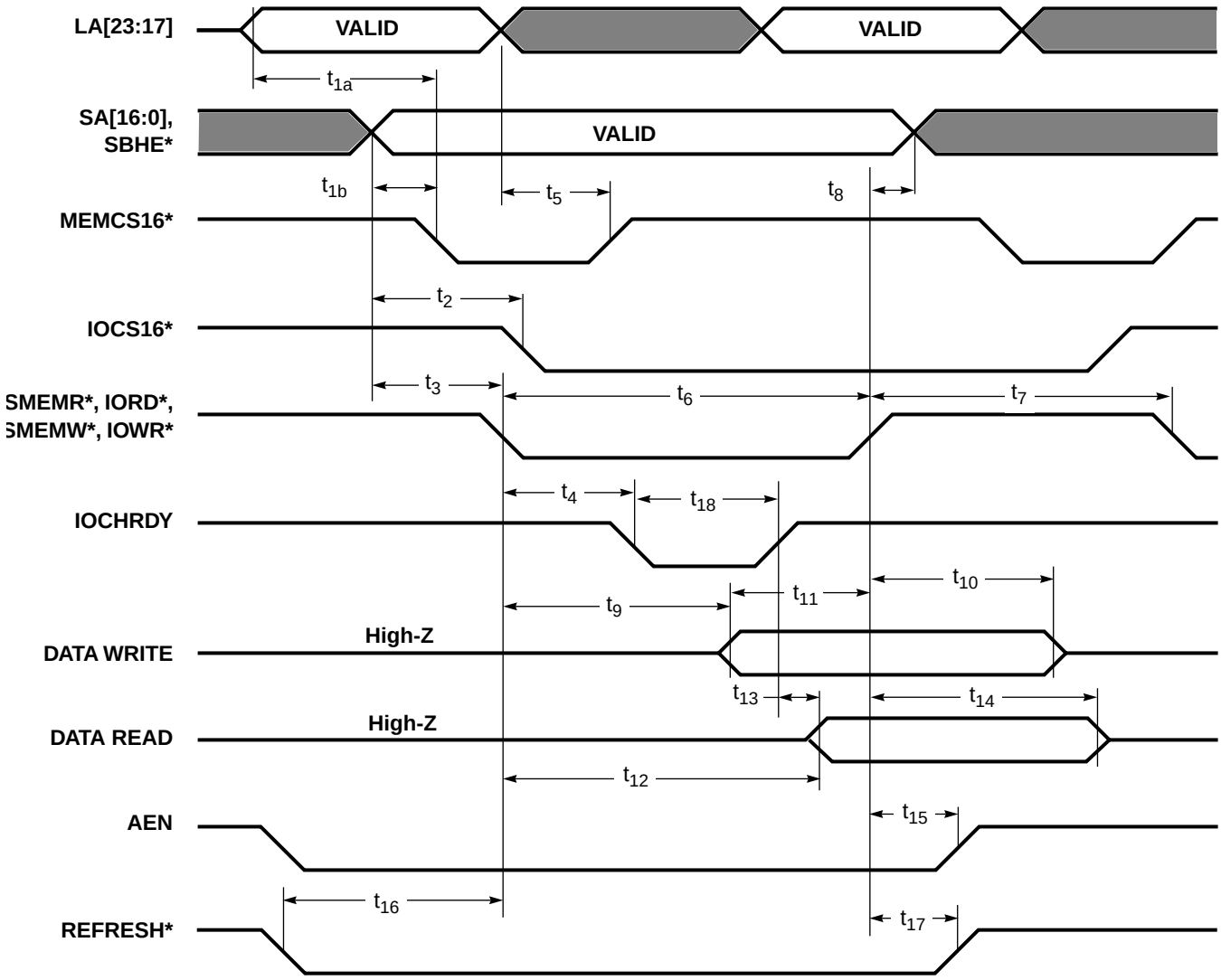


Figure 7–1. Bus Signal Timing (ISA Bus)

Table 7–2. BALE Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	LA23:17 setup time to BALE negative transition	20	–	ns
t_2	SBHE* setup time to BALE negative transition	20	–	ns
t_3	LA23:17 hold time from BALE negative transition	20	–	ns
t_4	SBHE* hold time from BALE negative transition	20	–	ns
t_5	BALE 'high' Pulse Width	20		ns

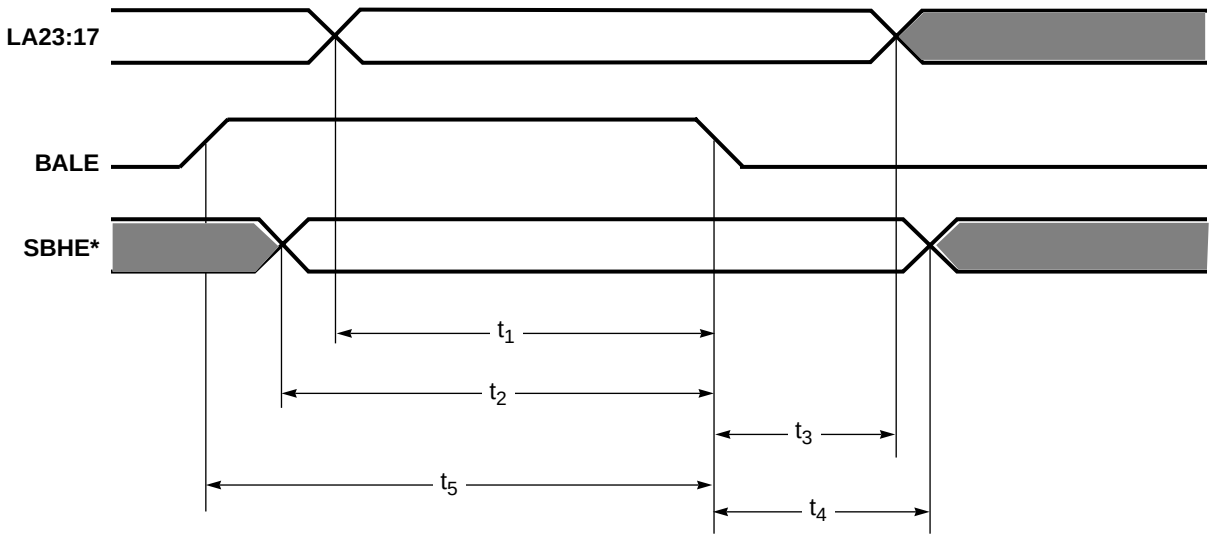


Figure 7–2. BALE Timing (ISA Bus)

Table 7–3. EROM* Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	EROM* 'low' delay from SMEMR* 'low'	–	30	ns
t_2	EROM* 'high' delay from SMEMR* 'high'	–	20	ns

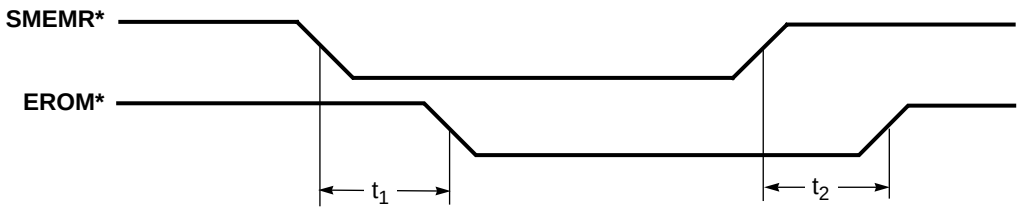


Figure 7–3. EROM* Timing (ISA Bus)

Table 7–4. AEN Timing (ISA Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	AEN setup time to IORD* or IOWR* 'low'	5.0	–	ns
t_2	AEN hold time from IORD* or IOWR* 'high'	5.0	–	ns

a. AEN 'high', as shown below, will cause the CL-GD62XX to ***disregard*** the I/O Cycle.

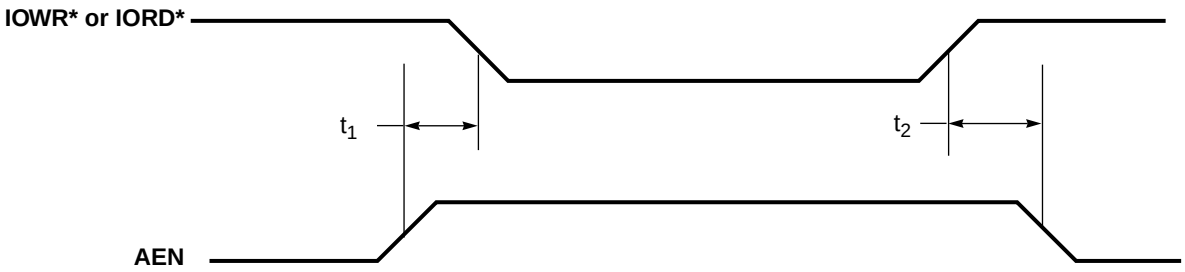


Figure 7–4. AEN Timing (ISA Bus)

Table 7–5. PI Bus-Interface Timing[a]

Symbol	Parameter	MIN	MAX	Units
t_1	Address setup time to PSTART# 'low'	10	–	ns
t_2	Command setup time to PSTART# 'low'	20	–	ns
t_3	Command hold time from PSTART# 'low'	38	–	ns
t_4	Address hold time from PSTART# 'low'	40	–	ns
t_5	PSTART# 'low' pulse width	35	–	ns
t_6	PCMD# 'low' setup time from PSTART# 'low'	20	–	ns
t_7	Write data valid delay from PSTART# 'low'	–	52	ns
t_8	Write data valid delay from PCMD# 'low'	–	20	ns
t_9	PRDY# 'low' delay from PCMD# 'low'	80	5000	ns
t_{10}	PCMD# 'high' hold time from PRDY# 'low'	26	–	ns
t_{11}	PSTART# 'low' setup time from PCMD# 'high'	0	–	ns
t_{12}	PDRY# 'high' delay from PCMD# 'high'	0	10	ns
t_{13}	Read data setup time to PCMD# 'high'	48	–	ns
t_{14}	Read data hold time from PCMD# 'high'	12	–	ns
t_{15}	Write data hold time from PCMD# 'high'	20	–	ns
t_{16}	PRDY# 'low' delay from PCMD# 'low'	0	30	ns
t_{17}	PRDY# 'high' to PRDY# high-impedance delay	5.0	30	ns

a. The PI-bus interface specifications are valid from 0° to 70° C at operating voltages of 3.3 volts ± 0.3 volts and 5 volts ± 0.25 volts.

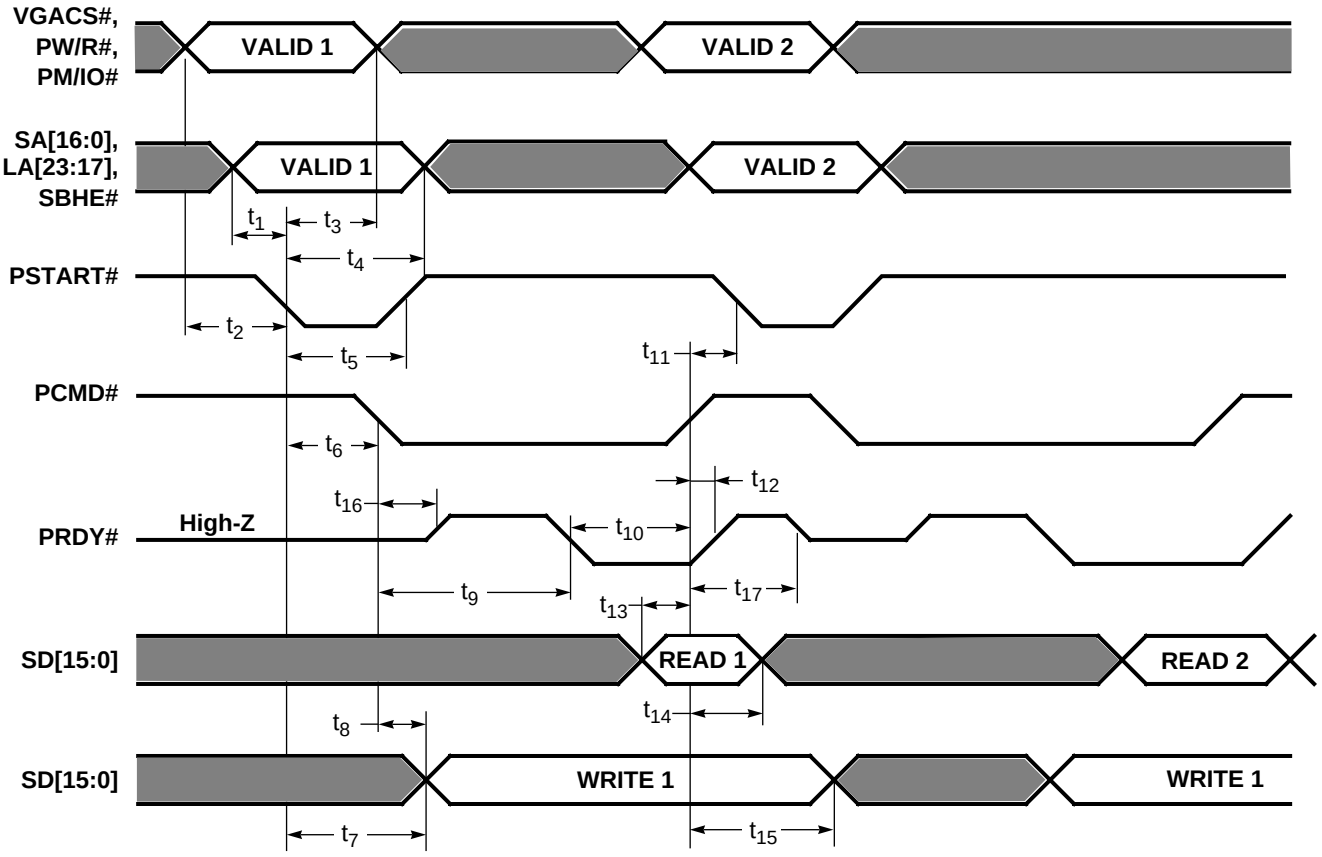


Figure 7–5. PI Bus Interface Timing

Table 7–6. CLK1X, CLK2X Timing (Local Bus)

Symbol	Parameter	CLK2X		CLK1X		Units
		MIN	MAX	MIN	MAX	
t_1	Rise time	–	4.0	–	4.0	ns
t_2	Fall time	–	4.0	–	4.0	ns
t_3	Positive ‘high’ pulse width	40	60	40	60	% t_5
t_4	Negative ‘low’ pulse width	40	60	40	60	% t_5
t_5	Period	12.5	–	20	–	ns

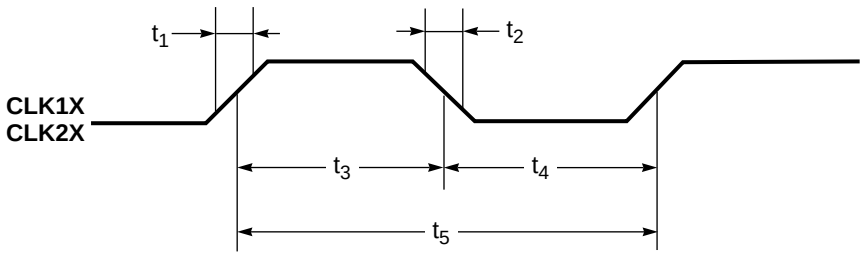


Figure 7–6. CLK1X, CLK2X Timing (Local Bus)

Table 7–7. Reset Timing (Local Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	CPU-RESET hold time from CLK2X	4.0	–	ns
t_2	CPU-RESET setup time to CLK2X	2.0	–	ns

a. Applies to ’386 only. For ’486, CPU-RESET may be tied to RESET.

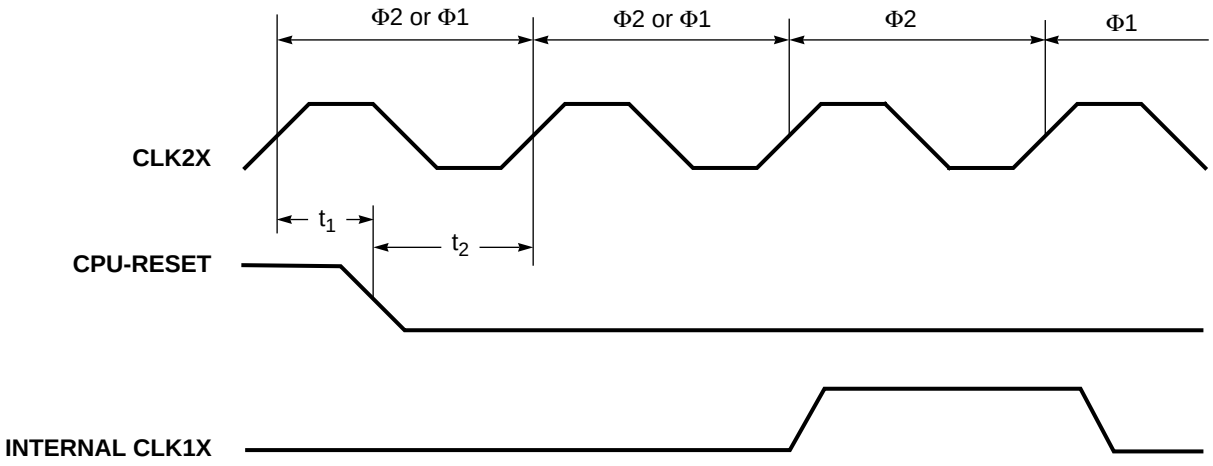


Figure 7–7. Reset Timing (Local Bus)

Table 7–8. ADS#, LBA# Timing (Local Bus) (Not Pipelined)

Symbol	Parameter	MIN	MAX	Units
t_1	Address, status, ADS# setup time to CLK1X	5.0	–	ns
t_2	LBA# 'low' delay from address, Status (20-pF loading)	–	15	ns
t_3	BS16# 'low' delay from address, status	–	15	ns
t_4	LBA# 'high' delay from address, status	–	18	ns

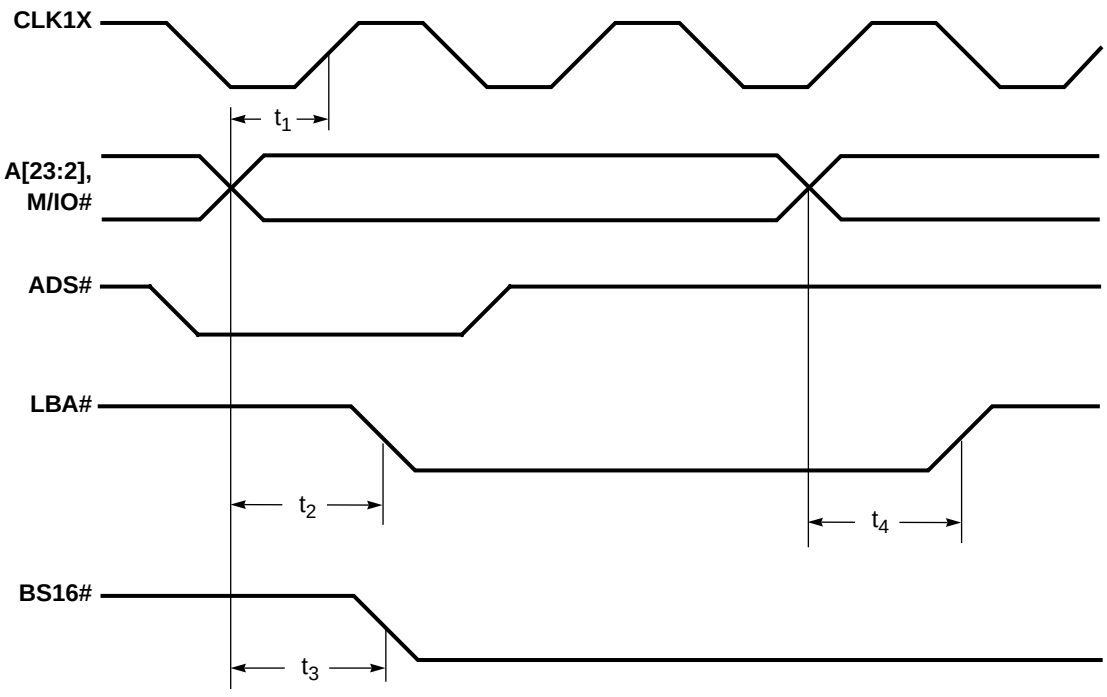


Figure 7–8. ADS#, LBA# Timing (Local Bus) (Not Pipelined)

Table 7–9. LBA#, BS16# Timing (Local Bus) (Pipelined)

Symbol	Parameter	MIN	MAX	Units
t_1	LBA# delay from address	–	25	ns
t_2	BS16# delay from address	–	25	ns

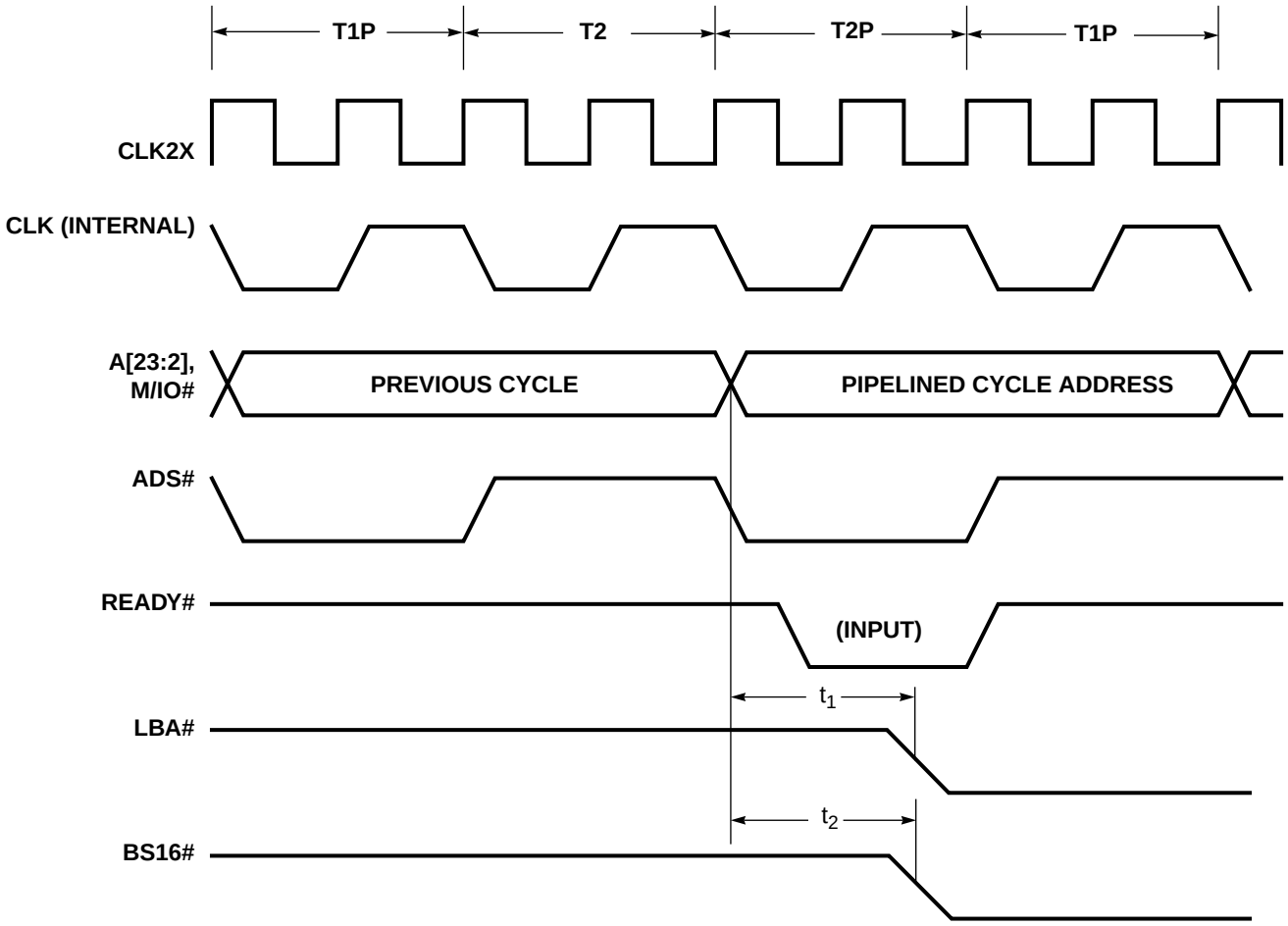


Figure 7–9. LBA#, BS16# Timing (Local Bus) (Pipelined)

Table 7–10. BRDY# Delay (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	BRDY# active delay from CLK1X	–	12	ns
t_2	BRDY# 'high' delay from CLK1X	–	12	ns
t_3	BRDY# 'high' before high-impedance	–	1/2	CCLK1X

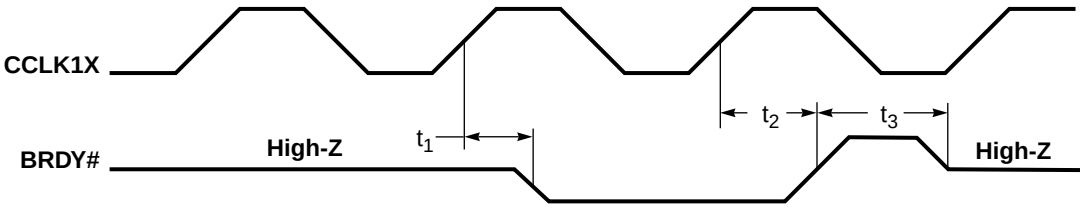


Figure 7–10. BRDY# Delay (Local Bus)

Table 7–11. Read Data Timing (Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Read data setup time to READY#, BRDY# 'low'	15	–	ns
t_2	Read data hold time from READY#, BRDY# 'high'	12	–	ns

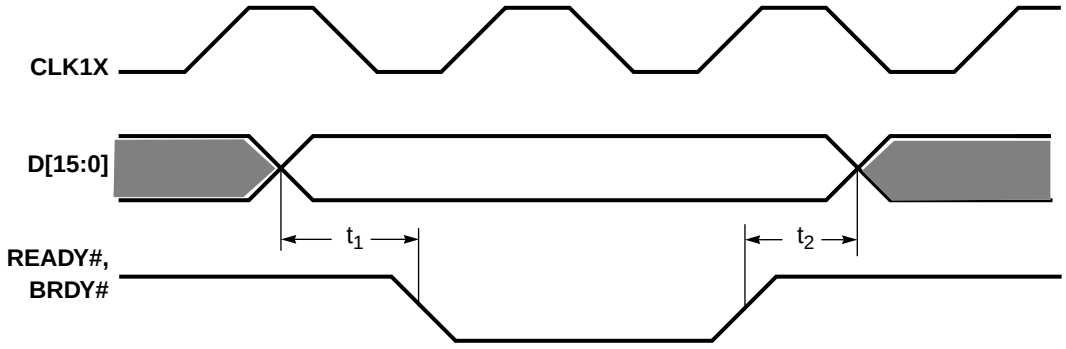


Figure 7–11. Read Data Timing (Local Bus)

Table 7–12. Buffer Control Timing: 16-Bit Cycle ('486 Local Bus)

Symbol	Parameter	MIN	MAX	Units
t_1	Clock to OEL#, OEH# delay	0	14	ns

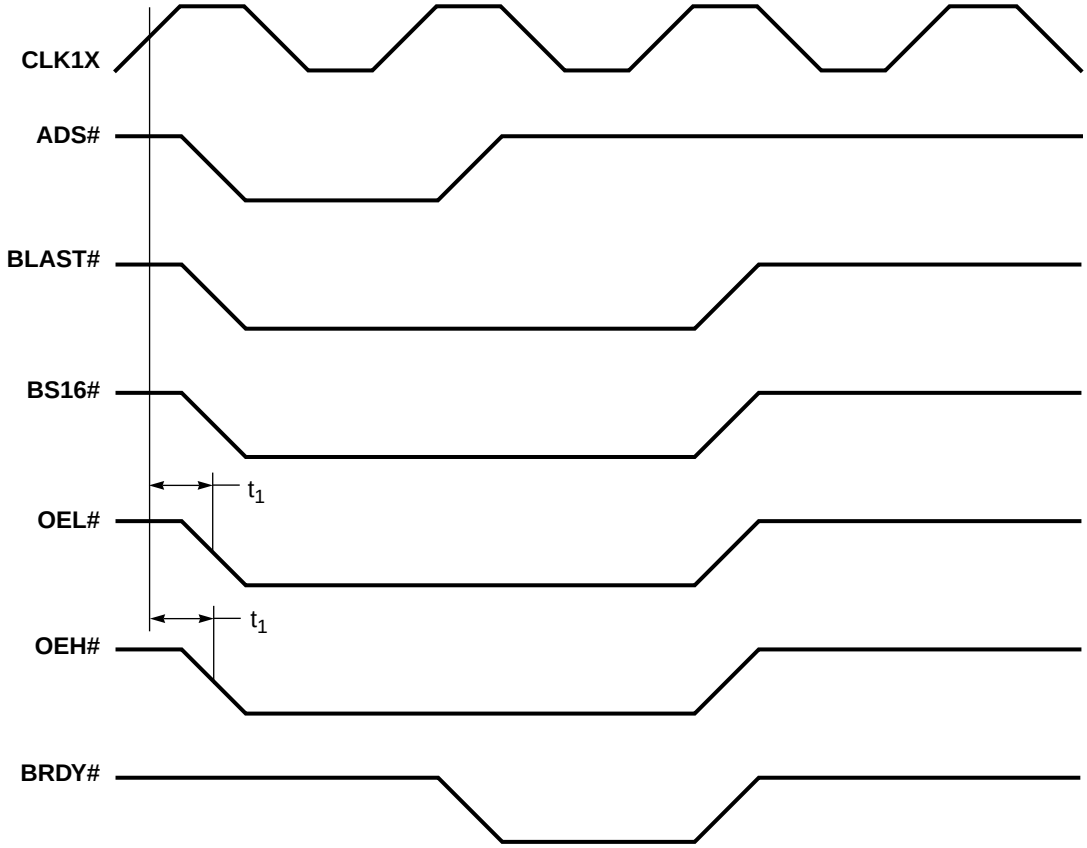


Figure 7–12. Buffer Control Timing: 16-Bit Cycle ('486 Local Bus)

Table 7–13. Display-Memory Bus Read Timing (t^b = MCLK)[a]

Symbol	Parameter	MIN	MAX	UNITS
t_1	Row address setup time to RAS* 'low'	5.0	–	ns
t_2	Column address setup time to CAS* 'low'	5.0	–	ns
t_3	RAS* 'low' to CAS* 'low' delay	2.5	–	t^b
t_4	Row address hold time from RAS* 'low'	1.0	–	t^b
t_5	Column address hold time from CAS* 'low'	1.0	–	t^b
t_6	Data valid delay from RAS* 'low'	–	4.0	t^b
t_7	Data valid delay from CAS* 'low'	–	1.5	t^b
t_8	Data valid delay from column address valid	–	2.0	t^b
t_9	RAS* precharge (RAS* Pulse Width 'high')	3.0	–	t^b
t_{10}	Read cycle time	7.0	–	t^b
t_{11}	Read command hold time from CAS* 'high'	0.5	–	t^b
t_{12}	CAS* precharge (CAS* pulse width 'high')	0.5	–	t^b
t_{13}	RAS* pulse width 'low' RAS* pulse width 'low' (Page mode)	4.0 –	– 32	t^b µs
t_{14}	CAS* pulse width 'low'	1.5 –	– 32	t^b µs
t_{15}	Read data hold time from CAS* 'high'	10	–	ns
t_{16}	Read command setup time	5.0	–	ns
t_{17}	Data valid delay from OE* 'low'	–	1.5	t^b
t_{18}	Read command hold time from RAS* 'high'	1.0	–	t^b
t_{19}	RAS* hold time from OE* 'low'	1.5	–	t^b
t_{20}	CAS* 'high' setup time to RAS* 'low' (precharge time)	0.5	–	t^b
t_{21}	RAS* 'low' to CAS* 'high'	4.0	–	t^b
t_{22}	CAS* cycle time	2.0	–	t^b
t_{23}	Read data hold time from OE* 'high'	10	–	ns

a. The memory interface specifications are valid from 0° to 70° C at operating voltages of 3.3 volts ± 0.3 volts and 5 volts ± 0.25 volts.
b. 't' is the MCLK period, an internal clock.

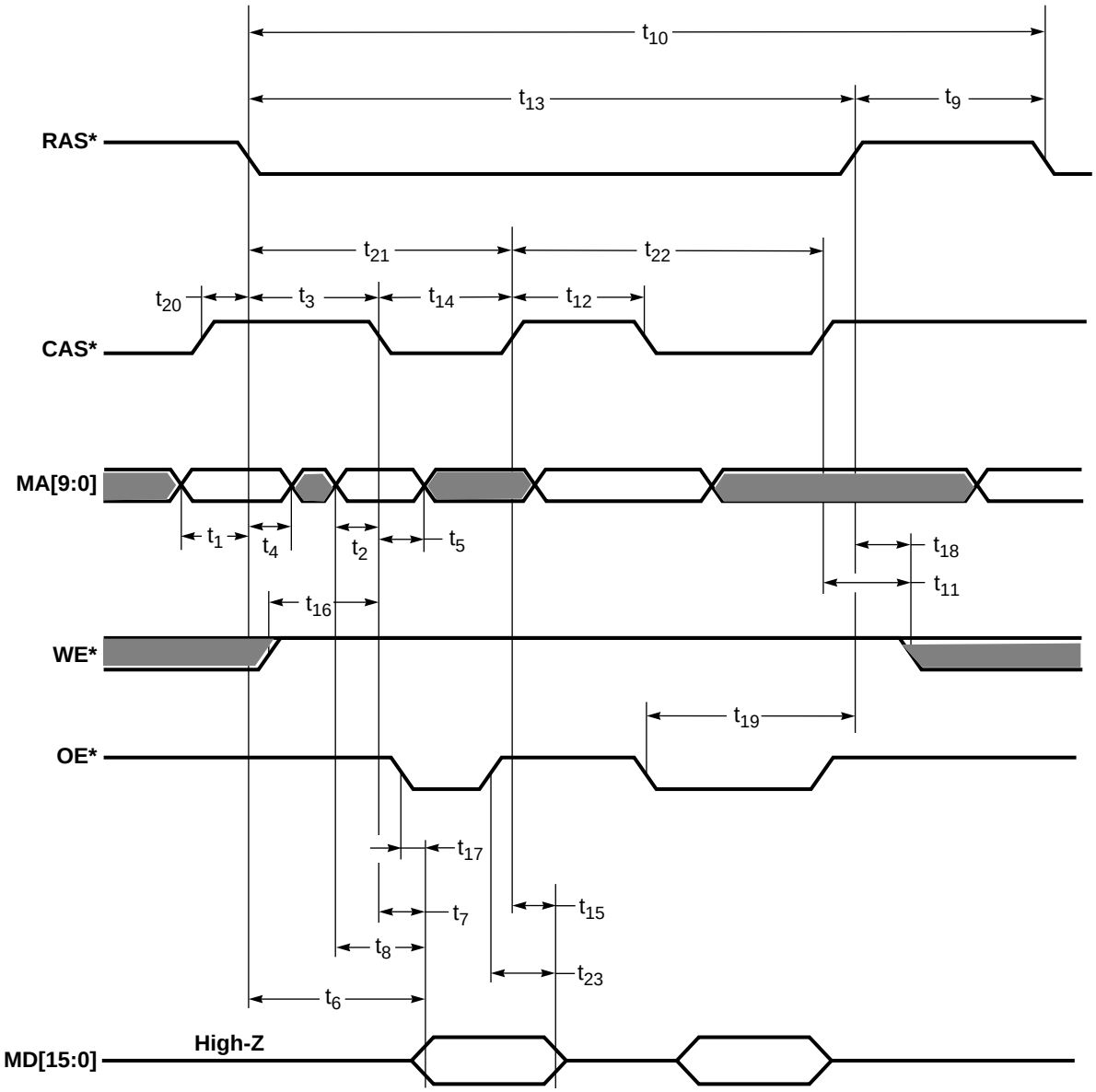


Figure 7–13. Display-Memory Bus Read Timing (t = MCLK)

Table 7–14. Display-Memory Bus Write Timing (t^b = MCLK)[a]

Symbol	Parameter	MIN	MAX	UNITS
t_1	Address setup time to RAS* 'low'	5.0	–	ns
t_2	Address setup time to CAS* 'low'	5.0	–	ns
t_3	RAS* 'low' to CAS* 'low' delay	2.5	–	t^b
t_4	Row address hold time from RAS* 'low'	1.0	–	t^b
t_5	Column address hold time from CAS* 'low'	1.0	–	t^b
t_6	RAS* precharge (RAS* pulse width 'high')	3.0	–	t^b
t_7	Write cycle time	7.0	–	t^b
t_8	CAS* precharge (CAS* pulse width 'high')	0.5	–	t^b
t_9	CAS* 'high' setup time to RAS* 'low' (precharge time)	0.5	–	t^b
t_{10}	RAS* 'low' to CAS* 'high'	4.0	–	t^b
t_{11}	CAS* cycle time	2.0	–	t^b
t_{12}	CAS* pulse width 'low'	1.5 –	– 32	t^b µs
t_{13}	RAS* pulse width 'low' RAS* pulse width 'low' (Page mode)	4.0 –	– 32	t^b µs
t_{14}	WE* 'low' setup time to CAS* 'low'	0.5	–	t^b
t_{15}	WE* 'low' hold time to CAS* 'low'	0.5	–	t^b
t_{16}	WE* 'low' pulse width	1.0	–	t^b
t_{17}	Write data setup time to CAS* 'low'	5.0	–	ns
t_{18}	Write data hold time from CAS* 'low'	1.0	–	t^b
t_{19}	WE* 'low' to CAS* 'high' delay time	1.0	–	t^b

a. The memory interface specifications are valid from 0° to 70° C at operating voltages of 3.3 volts ± 0.3 volts and 5 volts ± 0.25 volts.
b. 't' is the MCLK period, an internal clock.

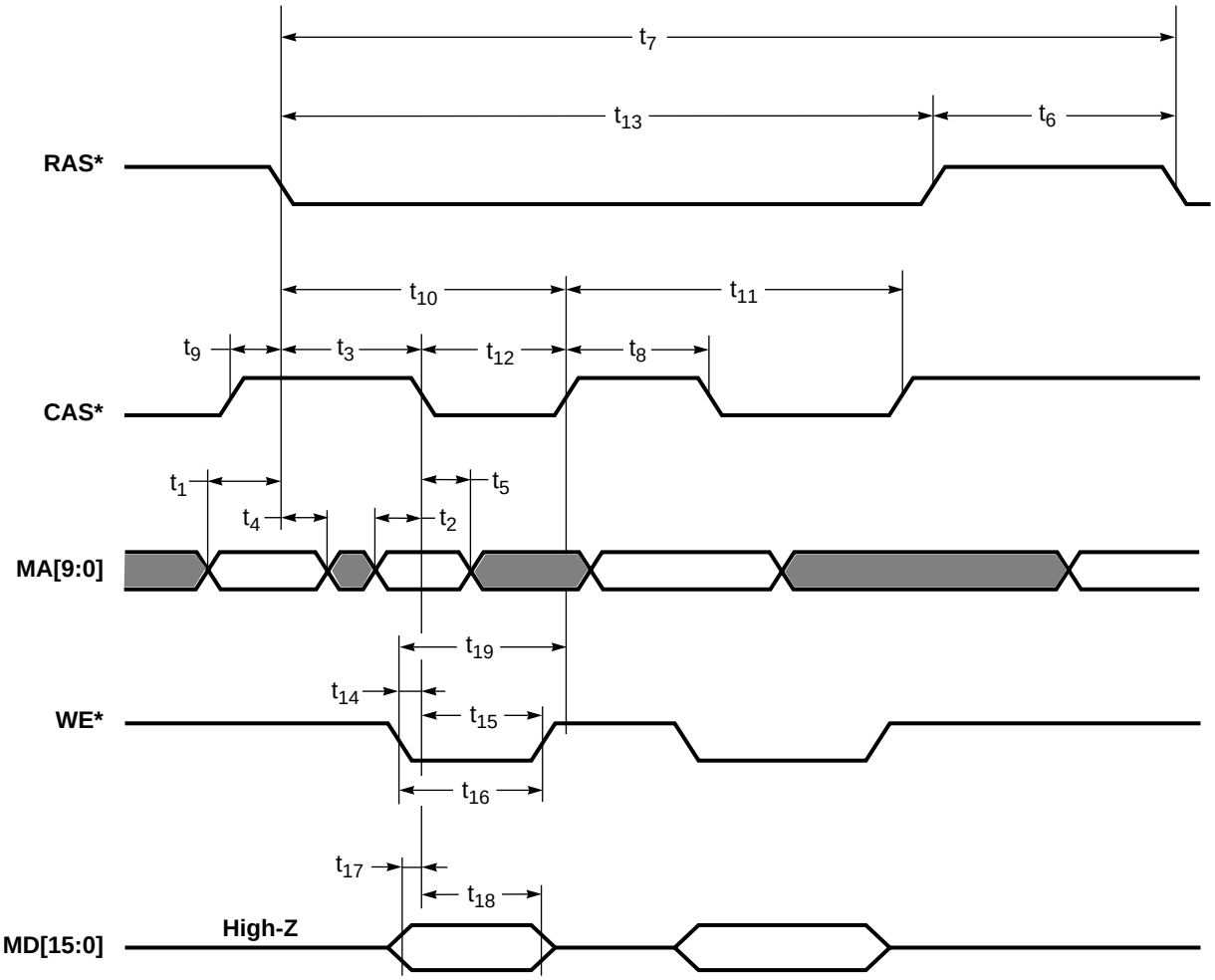


Figure 7–14. Display-Memory Bus Write Timing

Table 7–15. CAS*-Before-RAS* Refresh Timing (Display Memory Bus)[a]

Symbol	Parameter	MIN	MAX	Units
t_1	CAS* 'low' setup time to RAS* 'low'	1.0	–	t[b]
t_2	RAS* 'low' pulse width	4.0	–	t[b]
t_3	RAS* 'high' pulse width	3.0	–	t[b]
t_4	CAS* hold time for refresh	1.5	–	t[b]
t_5	Refresh cycle period	7.0	–	t[b]
t_6	CAS* pulse width 'high' (precharge time)	2.0	–	t[b]
t_7	RAS* 'high' to CAS* 'low' (precharge time)	1.0	–	t[b]

a. There will be either three or four RAS* pulses while CAS* remains 'low'.
b. 't' is the SQCLK period, an internal clock.

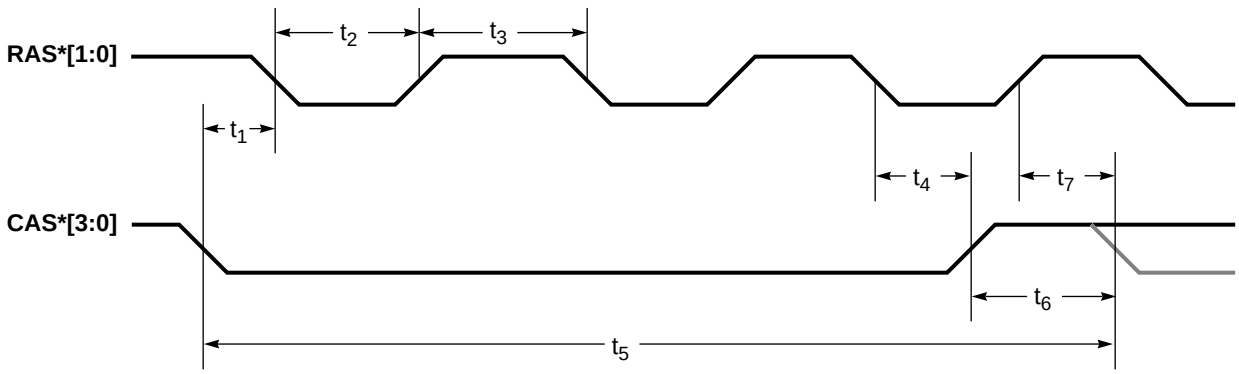


Figure 7–15. CAS*-Before-RAS* Refresh Timing (Display Memory Bus)

Table 7–16. Reset Timing

Symbol	Parameter	MIN	MAX	Units
t_1	RESET pulse width 'high'	12	–	t[a]
t_2	MD[15:0] setup to RESET negative edge	2.0	–	ns
t_3	MD[15:0] hold from RESET negative edge	5.0	–	ns
t_4	RESET 'low' to first IOWR*	12	–	t[a]

a. t = MCLK period

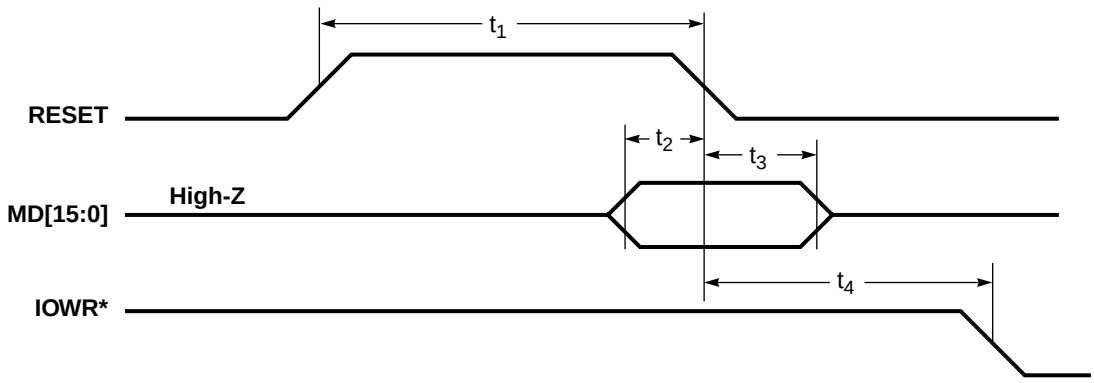


Figure 7–16. Reset Timing

Table 7–17. STN Monochrome and Color-Passive LCD Interface Timing[a]

Symbol	Parameter	M2DD-8	M2SS-4	C8DD-8	C8DD-16	C8SS-16	C8SSI-d-8
		Mono.	Mono.	Color	Color	Color	Color
t_1	FPVDCLK period	160 ns	225 ns	82 ns	175 ns	200 ns	210 ns
t_2	FPVDCLK ‘high’ time	145 ns	70 ns	30 ns	60 ns	50 ns	30 ns
t_3	FPVDCLK ‘low’ time	145 ns	70 ns	30 ns	60 ns	50 ns	30 ns
t_4	FPVDCLK rise and fall time	150 ns MAX	20 ns MAX	13 ns MAX	30 ns MAX	30 ns MAX	30 ns MAX
t_5	Data setup time	80 ns	50 ns	30 ns	30 ns	40 ns	30 ns
t_6	Data hold time	80 ns	100 ns	20 ns	30 ns	50 ns	30 ns
t_7	FPVDCLK ‘low’ to LLCLK ‘low’	150 ns	100 ns	100 ns	70 ns	250 ns	270 ns
t_8	FPVDCLK ‘low’ from LLCLK ‘low’	150 ns	100 ns	200 ns	20 ns	250 ns	260 ns
t_9	LLCLK ‘high’ time	125 ns	63 ns	70 ns	60 ns	150 ns	70 ns
t_{10}	LFS ‘high’ setup to LLCLK ‘low’	100 ns	100 ns	150 ns	10 ns	150 ns	100 ns
t_{11}	LFS ‘high’ hold time to LLCLK ‘low’	100 ns	100 ns	150 ns	40 ns	50 ns	40 ns
t_{12}	MOD delay from FPVDCLK ‘high’	300 ns MAX	300 ns MAX	300 ns MAX	300 ns MAX	300 ns MAX	300 ns MAX
t_{13}	LFS ‘low’ setup to FPVDCLK	NA	NA	NA	NA	NA	100 ns
t_{14}	LFS ‘low’ hold from FPVDCLK	NA	NA	NA	NA	NA	40 ns

a. Values are MIN unless specified otherwise.

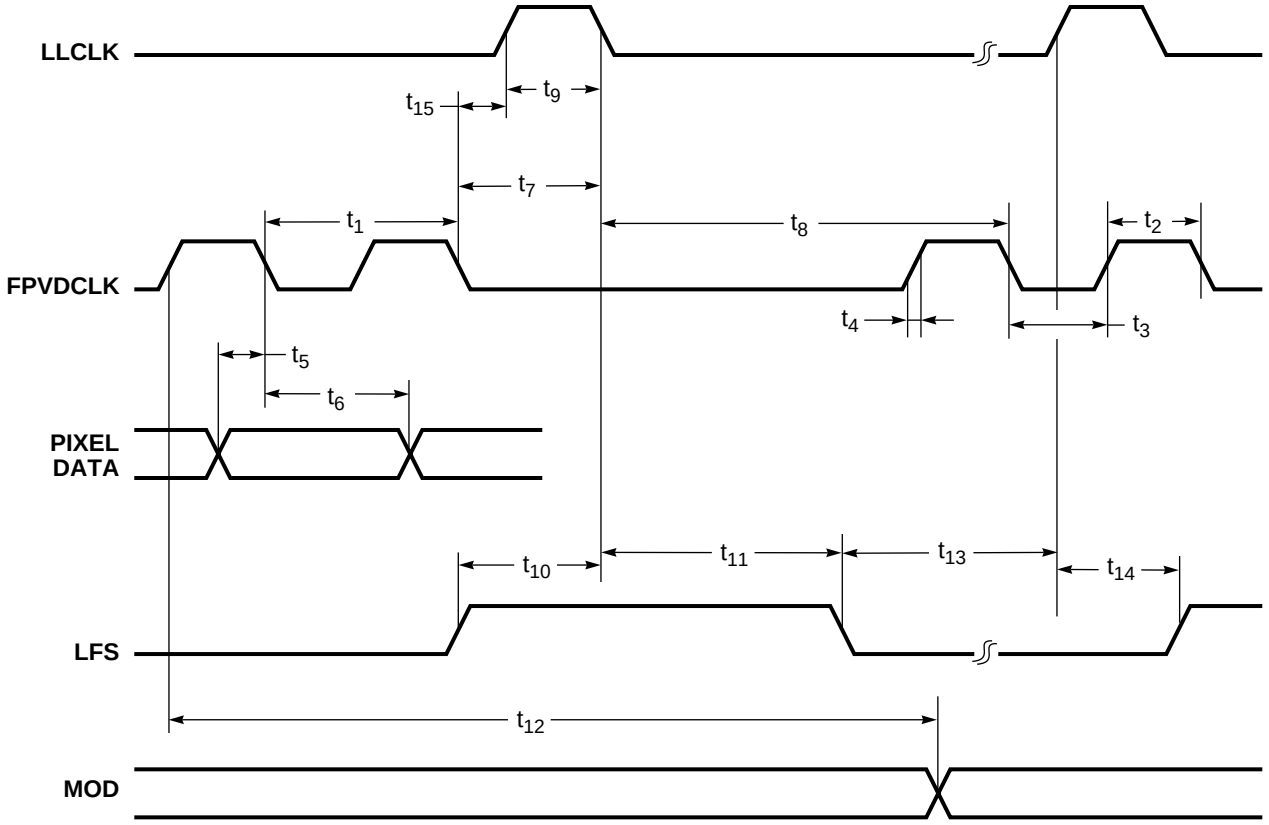


Figure 7–17. STN Monochrome and Color-Passive LCD Interface Timing

Table 7–18. TFT Color Single-Scan LCD Interface Timing[a, b]

Symbol	Parameter	MIN	MAX	UNITS
t_1	FPVDCLK period	40	–	ns
t_2	FPVDCLK 'high' time	10	–	ns
t_3	FPVDCLK 'low' time	10	–	ns
t_4	FPVDCLK rise and fall time	–	10	ns
t_5	Data setup time	10	–	ns
t_6	Data hold time	12	–	ns
t_7	HSYNC setup to FPVDCLK	13	–	ns
t_8	HSYNC hold to FPVDCLK	13	–	ns
t_9	VSYNC setup to HSYNC	1.5	–	t_1
t_{10}	VSYNC hold to HSYNC	1.0	–	t_1
t_{11}	DE setup to FPVDCLK	10	–	ns
t_{12}	DE hold to FPVDCLK	10	–	ns
t_{13}	Vertical front porch	0	30	lines
t_{14}	Vertical back porch	1.0	31	lines
t_{15}	Horizontal front porch	0	96	t_1
t_{16}	Horizontal back porch	32	128	t_1
t_{17}	HSYNC width	32	128	t_1
t_{18}	VSYNC width	1.0	2.0	lines
t_{19}	Horizontal cycle time		*tbd*	
t_{20}	Vertical cycle time		*tbd*	

a. HYSYNC pulse width is programmable with a choice of 32, 64, 96, and 128 FPVDCLKs. Refer to the explanation of ERF4. VSYNC pulse width is programmable with a choice of one line period or two line periods. Refer to the explanation of ERF4.

b. *tbd* = to be determined.

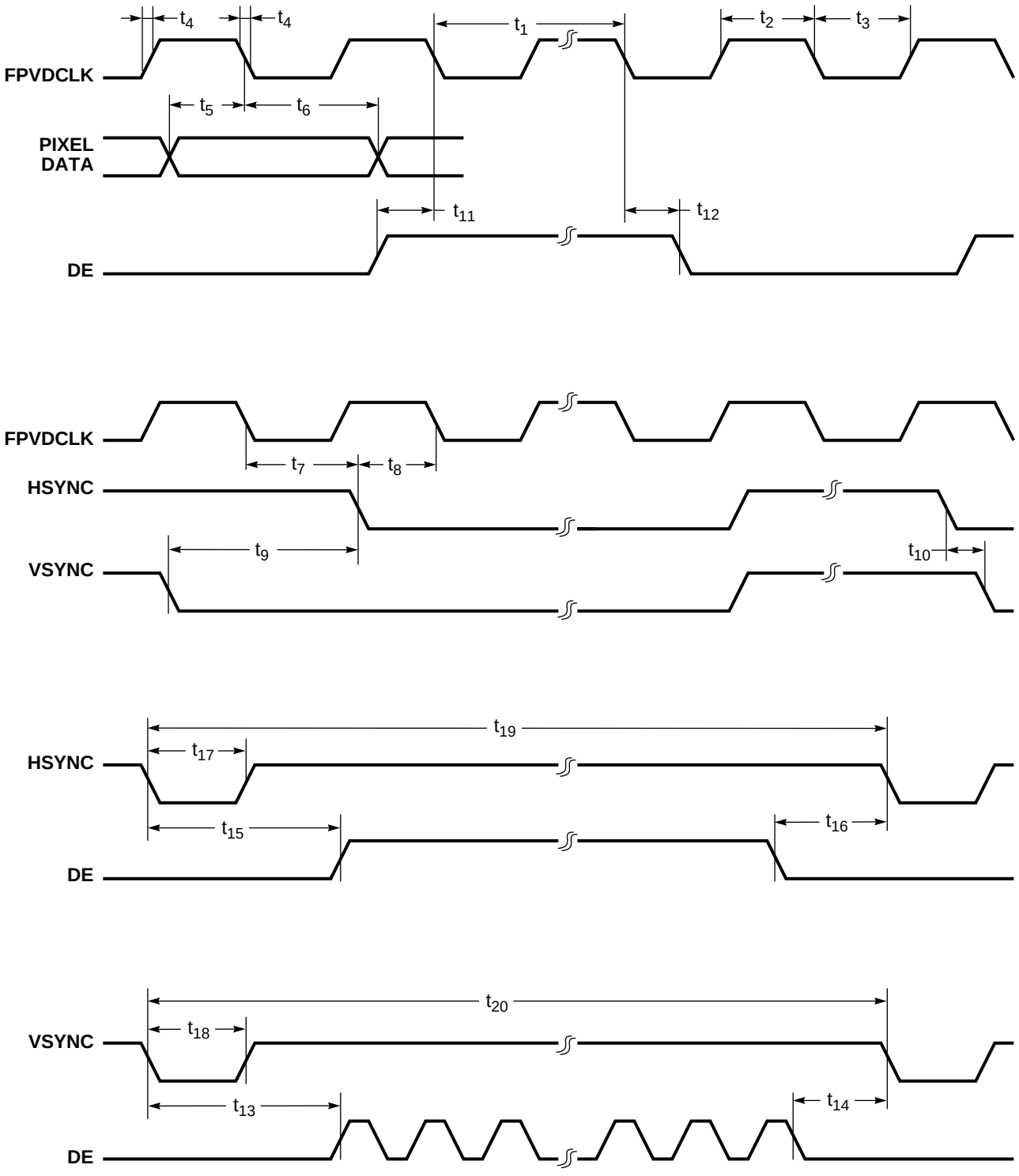


Figure 7–18. TFT, EL, Plasma Color, and Monochrome Single-Scan LCD Interface Timing

Table 7–19. Frequency Synthesizer Input Clock Specification

Symbol	Parameter	V_{DD} = 3.3V ± 0.3V		V_{DD} = 5.0V ± 0.25V	
		MIN	MAX	MIN	MAX
t_1	Input clock rise time	1.0 ns	7.0 ns	1.0 ns	7.0 ns
t_2	Input clock fall time	1.0 ns	7.0 ns	1.0 ns	7.0 ns
t_3	Input clock 'low' period	t_{CLKP}/2 - 10% t_5	t_{CLKP} + 10% t_5	t_{CLKP} - 10% t_5	t_{CLKP} + 10 % t_5
t_4	Input clock 'high' period	t_{CLKP}/2 - 10% t_5	t_{CLKP} + 10% t_5	t_{CLKP} - 10% t_5	t_{CLKP} + 10 % t_5
t_5	Input clock frequency/ period	69.84 ns - 0.1 %	69.84 ns + 0.1 %	69.84 ns - 0.1 %	69.84 ns + 0.1 %
V_{IH}	Input 'high' voltage	2.0 volts	V_{DD}	2.0 volts	V_{DD}
V_{IL}	Input 'low' voltage	GND	0.5 volts	GND	0.8 volts

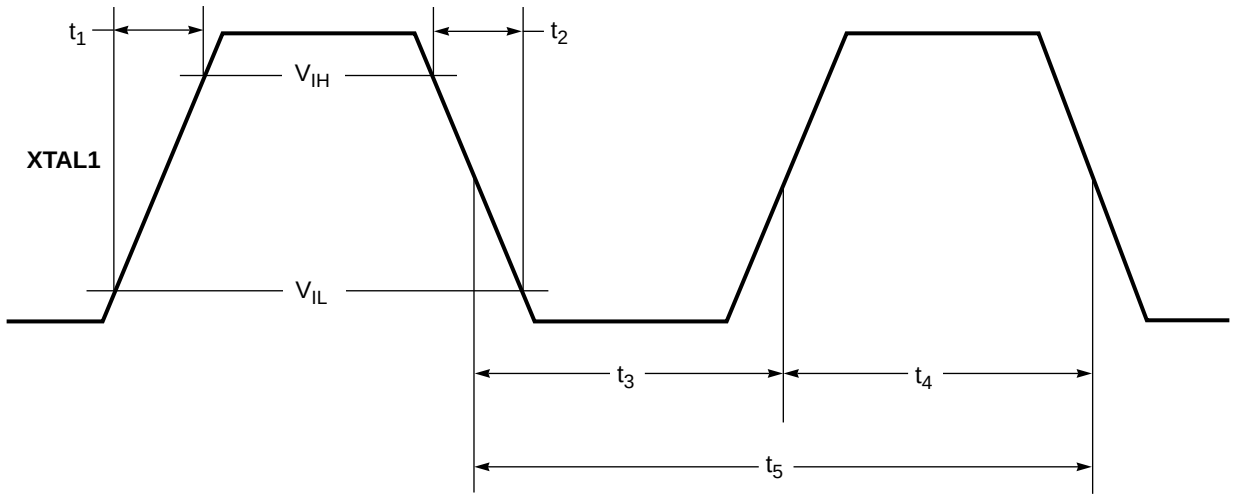
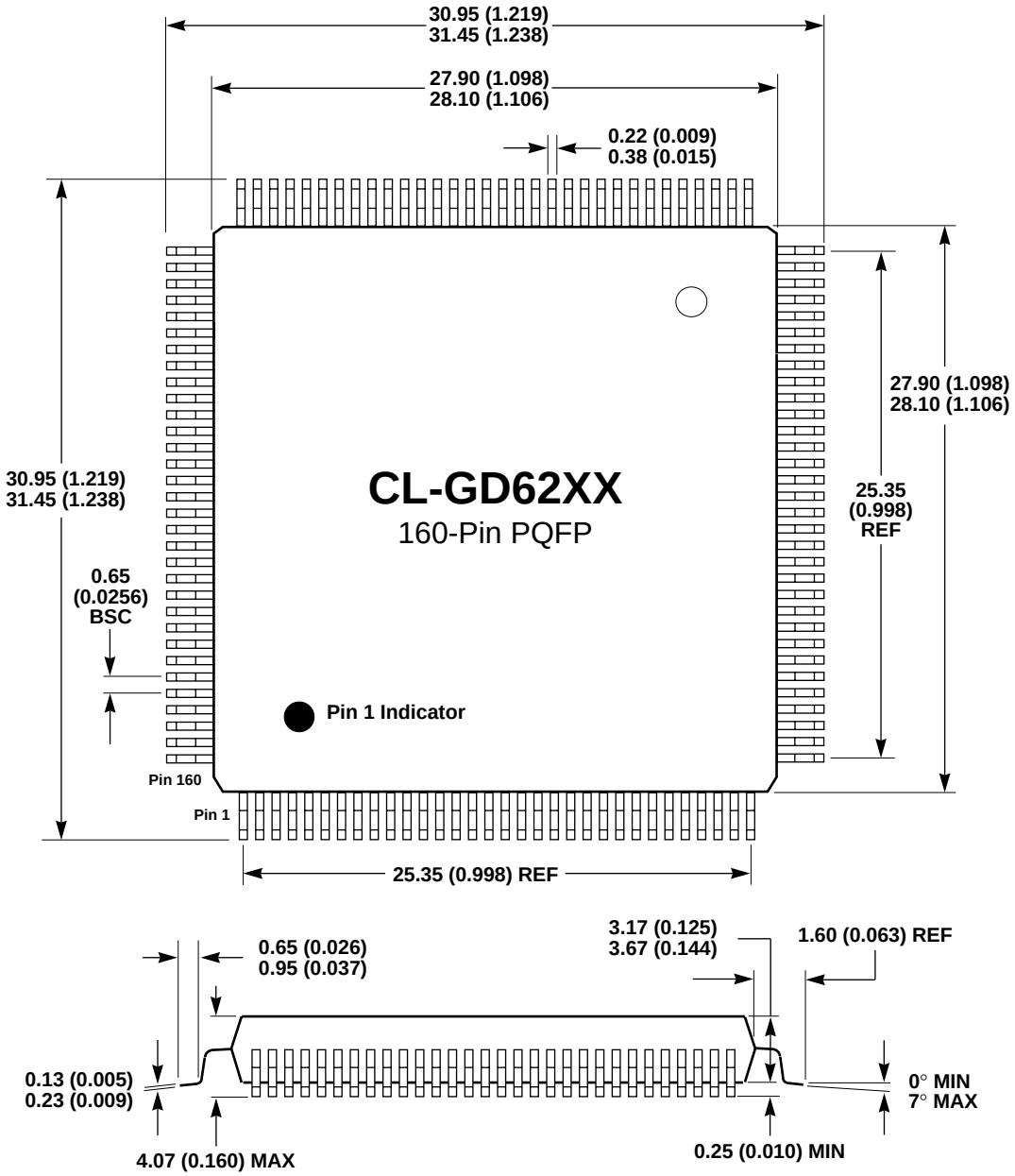


Figure 7–19. Frequency Synthesizer Input Clock Waveform

8. PACKAGE DIMENSIONS — CONTACT CIRRUS LOGIC

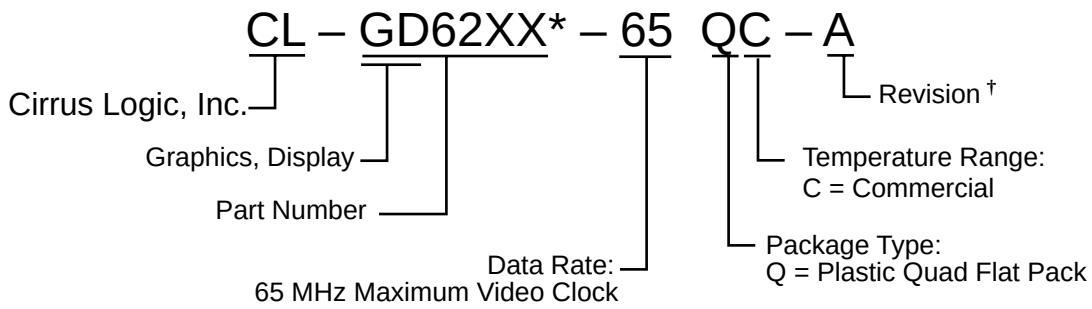


NOTES:

1) Dimensions are in millimeters (inches).
2) Drawing above does not reflect exact package pin count.
3) Before beginning any new design with this device, please contact Cirrus Logic for the latest information.

9. ORDERING INFORMATION

9.1 Package Marking Numbering Guide



* 'GD62XX' represents CL-GD6205, CL-GD6215, CL-GD6225, or CL-GD6235, respectively.
† Contact Cirrus Logic, Inc. for up-to-date information on revisions.

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