FUJITSU

ATM FACT SHEET

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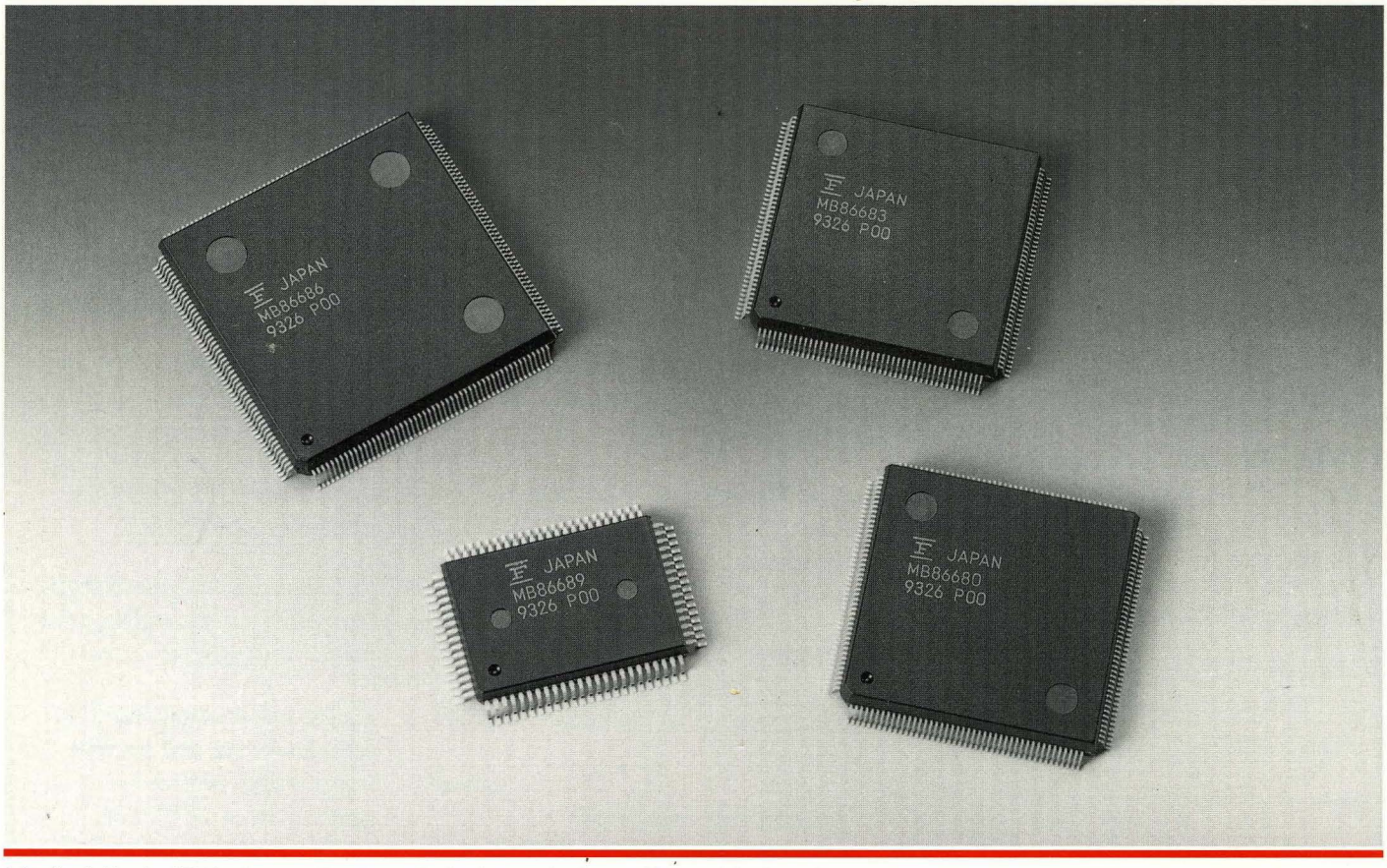

A family of chips for ATM implemented in advanced sub-micron technology and low-cost plastic packages.

A family of chips for ATM

Fujitsu has developed 4 devices which support the most comprehensive set of functions currently available:

MB86680 ATM Switch Routing Element (SRE)

MB86686 Adaptation Layer Controller (ALC)

MB86683 Network Termination Controller (NTC)

MB86689 Address Translation Controller (ATC)

Typical applications

The Fujitsu family of chips for ATM has been designed to be suitable for both adapter card and Hub applications. Examples of the architecture of a Hub port and an Adapter card using the chipset are shown on pages 3 and 4.

Key features

SRE

Switch Routing Element

- 4 x 4 Self-routing ATM Cell switch. Routing based on a Tag appended by ATC.
- Non-blocking output buffered architecture.
- Selectable high and low priority output queues.
- Selectable cell discard based on CLP bit and programmable output buffer thresholds.
- Supports Multicast mode.
- Active matrix expansion ports for row and column interconnect.

ALC

Adaptation Layer Controller

- Autonomous termination of Broadband ISDN Adaptation Layer standards Type 3/4 and Type 5.
- Single-chip segmentation and reassembly on up to 1024 Virtual Circuits.
- Leaky-bucket traffic shaping on each active virtual circuit. Separate peak and average rates for each VC.
- Transparent mode for constant bit rate support.
- Selectable 32-/64-bit high speed DMA Controller for 155Mbps performance.

NTC

Network Termination Controller

- ATM Cell framing to SONET, DS3, E3 and Cell-based frame formats.
- Maintains statistics for all active virtual circuits, including cell and error counts.
- Supports framed and Cell-based physical layer OAM functions for F1, F2 and F3 flows.
- On-chip DMA controller for high speed transfer of link statistics to system memory.
- Connects to MB86689 Address Translation Controller for real-time address translation in both directions.

ATC

Address Translation Controller

- 1024 entry Content Addressable Memory for address field translation and Routing Tag addition.
- 28 bit-comparison for each entry supporting UNI and NNI cell header formats.
- Selectable VPI and VCI mask for each entry.
- Supports CLP and congestion indication setting and removal for each entry.
- Translation completed in less than one cell period supporting real-time operation at 155Mbps.

HUB Port Architecture

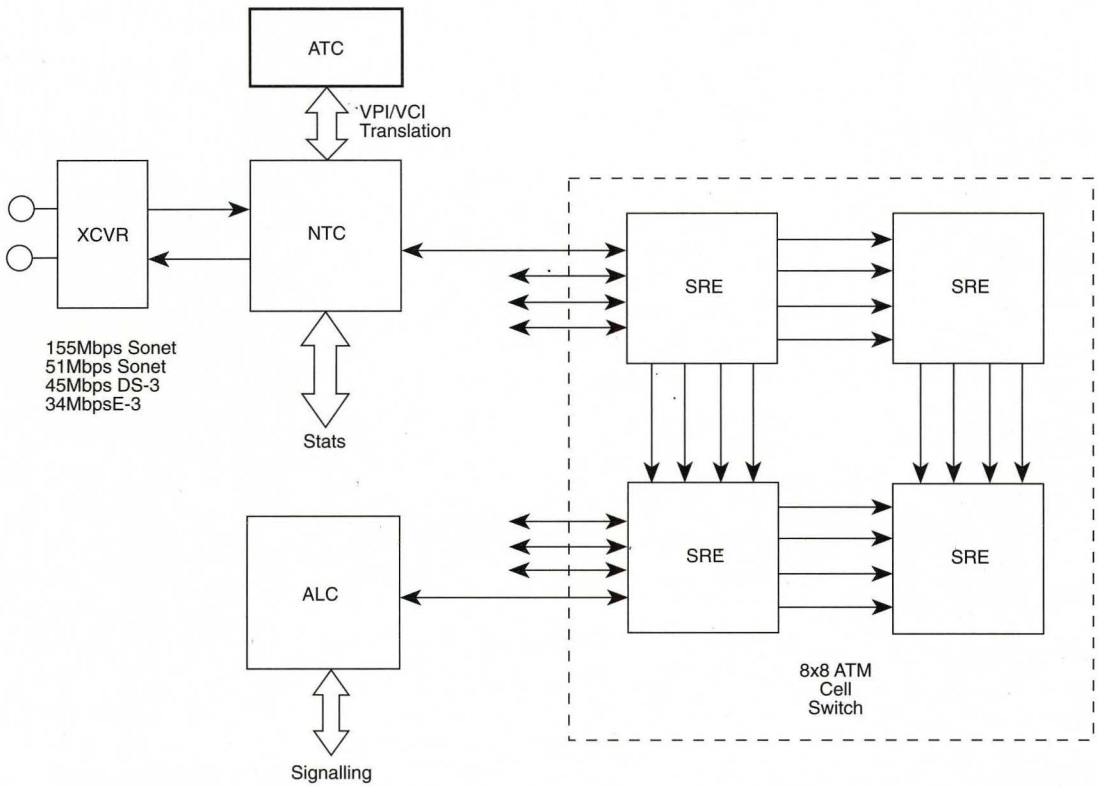

Figure 1

Basic Operation

The NTC fully terminates Sonet STS-3 and STS-1, DS-3 and E-3 received frames. All Sonet overhead bytes are made available to the system processor through on-chip registers. The NTC also maintains statistics on link quality and Cell and error counts for all active virtual circuits. These statistics are passed to the system via an on-chip DMA Controller.

The Address Translation Controller (ATC) is a Content Addressable Memory (CAM) structure used for translation of the received VPI/VCI, if appropriate, and for the addition of a 3 octet Tag which specifies the route through the switching fabric. The NTC passes the address field to the ATC for translation across a private interface. Translation is completed in less than one cell period. The ATC can also be used to set the Cell Loss Priority and Congestion Indication bits.

The SRE is a 4 x 4 output buffered ATM Cell switch. It supports many switch architectures through its flexibility in interpreting the 3 octet Tag appended by the ATC. The matrix architecture shown above is well suited to Multicast applications where a cell can be copied into multiple output buffers simultaneously. Up to 32 ports are supported in a single matrix.

In the application shown in figure 1 the ALC is handling all signalling and OAM traffic in the switch. It is also possible for an NTC and an ALC to share a switch port.

Adapter Card Architecture

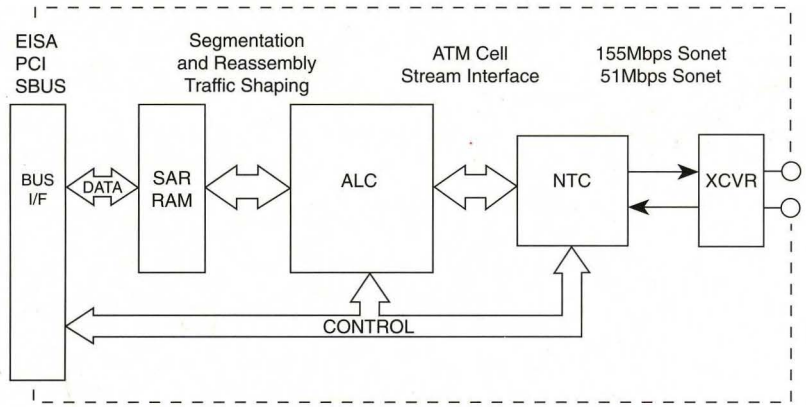

Figure 2

Basic Operation

In the transmit direction, user data packets are passed across the Host Bus interface to SAR RAM. The Adaptation Layer Controller (ALC) performs segmentation on up to 1024 simultaneaus Virtual Circuits (VCs) conforming to ATM Adaptation Layers 3/4 or 5. A transparent mode is also supported. In addition the ALC autonomously shapes the transmit traffic using leaky-bucket averaging to smooth the average cell rate. Separate peak and average rate parameters are supported for each VC. During data transfer the interaction between the ALC and the host system is on a per packet basis.

The ALC connects to the Network Termination Controller (NTC) via an 8-bit parallel cell stream interface. The NTC maps the raw cell stream into a SONET frame at 155 or 51Mbps conforming to the ATM Forum UNI specification. All Sonet overhead bytes are controlled by the NTC from microprocessor accessible registers.

In the receive direction, the Incoming Sonet frame is fully terminated by the NTC. ATM Cells are recovered from the Sonet payload and passed to the ALC for reassembly. The ALC reassembles user data packets according to the appropriate Adaptation Layer and checks for protocol errors before passing the reassembled frame to the host system.

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