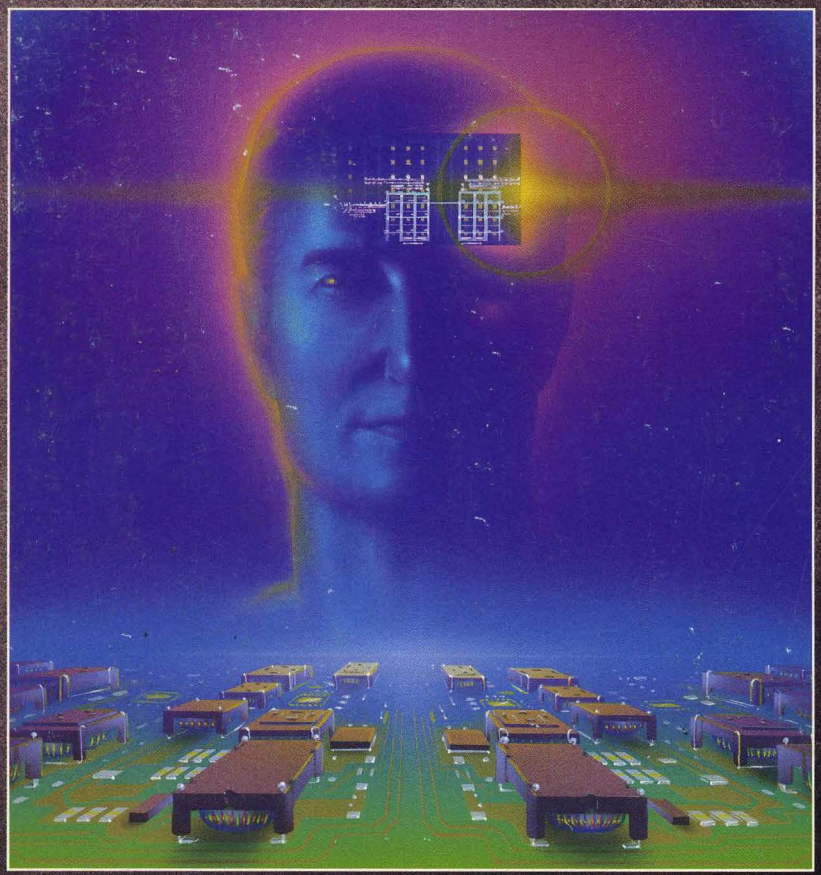

Intelligent Power ICs

FOR COMMERCIAL, INDUSTRIAL AND AUTOMOTIVE APPLICATIONS

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FOR COMMERCIAL, INDUSTRIAL & AUTOMOTIVE APPLICATIONS

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INTELLIGENT POWER ICs

1

GENERAL INFORMATION

ALPHA NUMERIC PRODUCT INDEX

ALPHA NUMERIC PRODUCT INDEX (Continued)

PRODUCT INDEX BY FAMILY

PRODUCT INDEX BY FAMILY (Continued)

INTELLIGENT POWER ICs 2

LOW SIDE SWITCHES

Low Side Switches Selection Guide

	TYPE NUMBER							
	CA3242 (QUAD)	CA3262 (QUAD)	CA3262A (QUAD)	CA3272 (QUAD)	CA3292 (QUAD)	HIP0080 (QUAD)	HIP0081 (QUAD)	CA3282 (OCTAL)
	INVERTING	INVERTING	INVERTING	INVERTING	INVERTING	INVERTING	INVERTING	LOGIC SELECT
Output Current Rating	0.6A	0.7A	0.7A	0.4A	0.4A	0.5A	1.0A	0.5A
V_{SAT} @ Current Rating	0.8V	0.6V	0.6V	0.4V	0.4V	-	-	0.5V
R_{ON} Output Resistance	-	-	-	-	-	1.0Ω	0.5Ω	-
Voltage Rating $(V_{CC})_{SUS}$	$35V_{DC}$	$35V_{DC}$	$40V_{DC}$	$40V_{DC}$	$32V_{DC}$ (Clamp)	35 (Clamp)	79 (Clamp)	$32V_{DC}$ (Clamp)
Load Dump Voltage (V_{PEAK})	$80V_{PK}$	$80V_{PK}$	$80V_{PK}$	$80V_{PK}$	$80V_{PK}$	$80V_{PK}$	$80V_{PK}$	TBD
Output Current Limiting	No	1.4A	1.3A	1.2A	1.2A	1.5A	3A	1.5A
Short-Circuit Protection	Yes Latches OFF	No	No	No	No	Yes Latches OFF	Yes Latches OFF	Yes Latches OFF
Thermal-Limiting Temperature, T_J	No	Yes +155°C	Yes +155°C	No	No	No	No	No
Thermal Shutdown Temperature, T_J	No	No	No	Yes +165°C	Yes +165°C	Yes +150°C	Yes +150°C	Yes +170°C
Fault Indicator Flag	No	No	No	Yes	Yes	Yes	Yes	Yes
Diagnostic Feedback	No	No	No	No	No	Yes	Yes	Yes
TEMPERATURE RANGE								
-40°C to +85°C	X	X						
-40°C to +125°C			X	X	X	X	X	X
PACKAGE OPTIONS								
16 DIP (Std)	X	X	X					
15 SIP							X	X
28 PLCC			X	X	X	X		

HARRIS SEMICONDUCTOR

CA3242

Quad-Gated Inverting Power Driver For Interfacing Low-Level Logic to High Current Load

May 1992

Features

- Driven Outputs Capable of Switching 600mA Load Currents Without Spurious Changes in Output State
- Inputs Compatible with TTL or 5 Volt CMOS Logic
- Suitable for Resistive or Inductive Loads
- Output Overload Protection
- Power-Frame Construction for Good Heat Dissipation

Applications

- Relays
- Solenoids
- AC and DC Motors
- Heaters
- Incandescent Displays
- Vacuum Fluorescent Displays

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3242E	-40°C to +105°C	16 Lead Plastic DIP

Description

The CA3242 quad-gated inverting power driver contains four gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

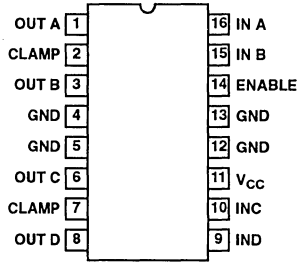
Output overload protection is provided when the load current (approximately 1.2A) causes the output V_{CE}(sat) to rise above 1.3V. A built-in time delay, nominally 25µs, is provided during output turn-on as output drops from V_{DD} to V_{SAT}. That output will be shut down by its protection network without affecting the other outputs. The corresponding Input or Enable must be toggled to reset the output protection circuit.

Steering diodes in the outputs in conjunction with external zener diodes protect the IC against voltage transients due to switching inductive loads.

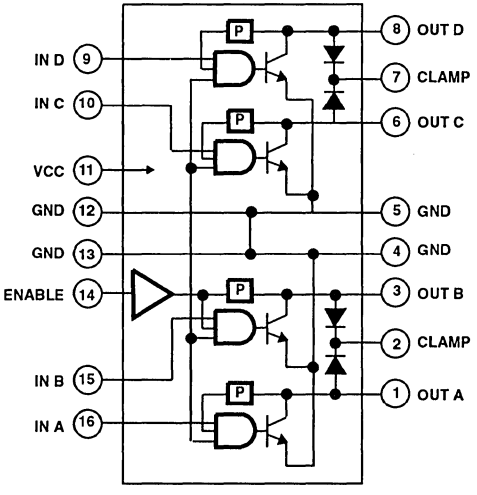
To allow for maximum heat transfer from the chip, the two center leads are directly connected to the die mounting pad. In free air, junction-to-air thermal resistance ($R_{\theta JA}$) is 50°C/W (typical), This coefficient can be lowered to 40°C/W (typical) by suitable design of the PC board to which the CA3242 is soldered.

Pinout

16 LEAD DUAL-IN-LINE
PLASTIC PACKAGE (E SUFFIX)
TOP VIEW



Block Diagram



TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1561.1**

Absolute Information (T_A = +25°C) Unless Otherwise Specified

Logic Supply Voltage, V_{CC} 7V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} . . . . . $50V_{DC}$
Output Sustaining Voltage, V_{CESUS} . . . . . $35V_{DC}$
Output Current, I_O . . . . . $1A_{DC}$
Power Dissipation, P_D
Up to 60°C 1.5W
Above 60°C . . . . . Derate Linearly at 16.6mW/°C
Up to 90°C w/heat sink (PC Board) 1.5W
Above 90°C w/heat sink (PC board) . . Derate Linearly at 25mW/°C

Ambient Temperature Range
Operating . . . . . -40°C to +105°C
Storage . . . . . -55°C to +150°C
Maximum Junction Temperature, T_J . . . . . +150°C
Maximum Thermal Resistance
Junction-to-Air, θ_{JA} . . . . . 60°C/W
Junction-to-Case, θ_{JC} to pins 4, 5, 12, 13 at seat . . . . . 12°C/W
Lead Temperature (During Soldering)
At distance 1/16" ± 1/32" (1.59 ± 0.79mm) from
case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = -40°C to +105°C, V_{CC} = 5V Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS		UNITS
			MIN	MAX	
Output Leakage Current	I_{CEX}	V_{CE} = 50V, V_{IN} = 0.8V	-	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 100mA, V_{IN} = 0.8V	30	-	V
Collector Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 100mA, V_{IN} = 2.4V	-	0.25	V
		I_C = 400mA, V_{IN} = 2.4V	-	0.6	V
		I_C = 600mA, V_{IN} = 2.4V	-	0.8	V
Input Low Voltage	V_{IL}		-	0.8	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	±10	µA
Input High Voltage	V_{IH}	I_C = 600mA	2	-	V
Input High Current	I_{IH}	I_C = 700mA, V_{IN} = 4.5V	-	10	µA
Supply Current ON	$I_{CC(ON)}$	I_C = 700mA, V_{CC} = V_{IH} = 5.5V	-	80	mA
Supply Current OFF	$I_{CC(OFF)}$		-	5	mA
Clamp Diode Leakage Current	I_R	V_R = 50V	-	100	µA
Clamp Diode Forward Voltage	V_F	I_F = 1A	-	1.8	V
		I_F = 1.5A	-	2.5	V
Turn-On Delay	t_{PHL}		-	20	µs
Turn-Off Delay	t_{PLH}		-	30	µs

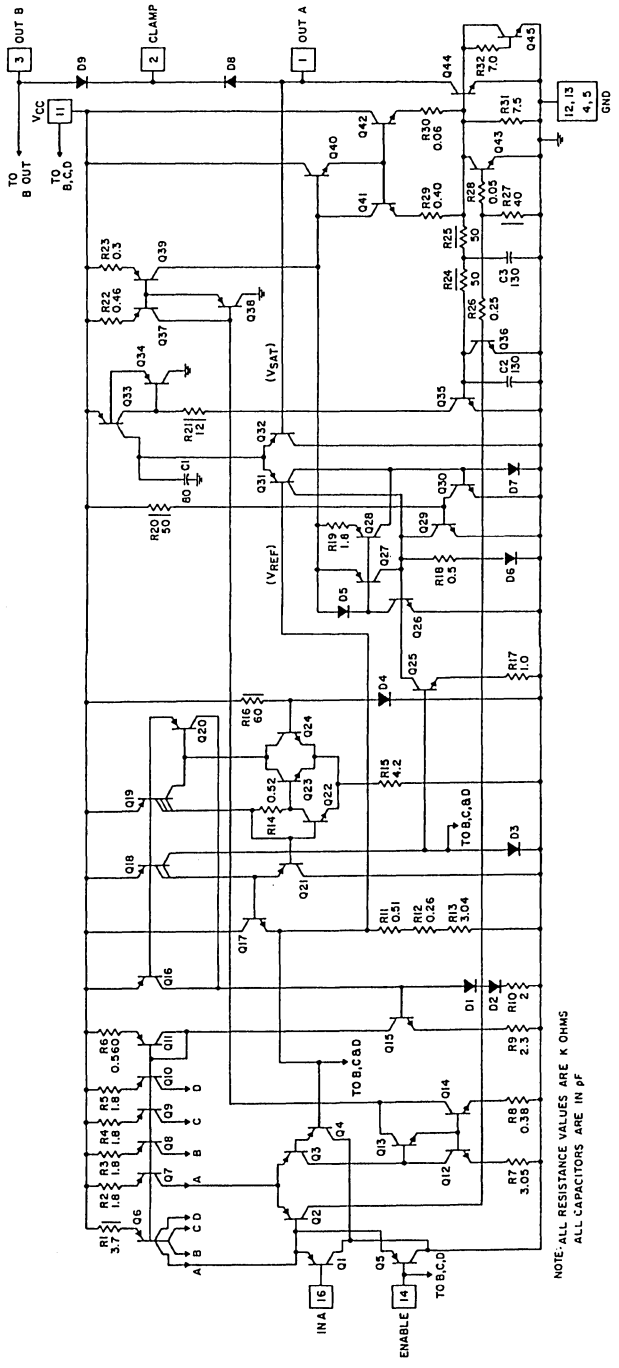


FIGURE 1. SCHEMATIC DIAGRAM OF THE CA3242 (SWITCH SECTION A)

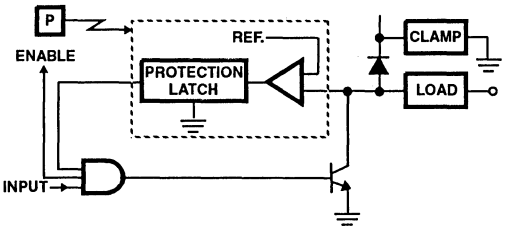


FIGURE 2. LOGIC DIAGRAM FOR EACH OUTPUT

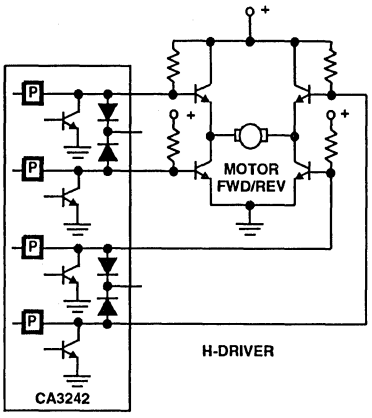


FIGURE 3. TYPICAL APPLICATIONS FOR THE CA3242 QUAD

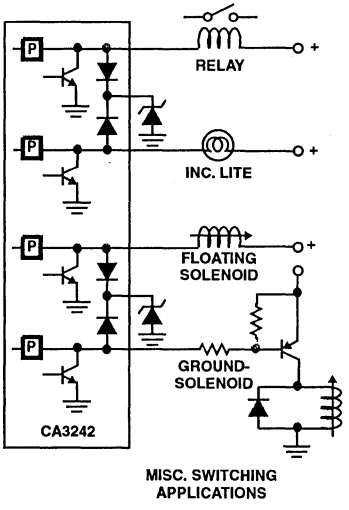


FIGURE 4. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER

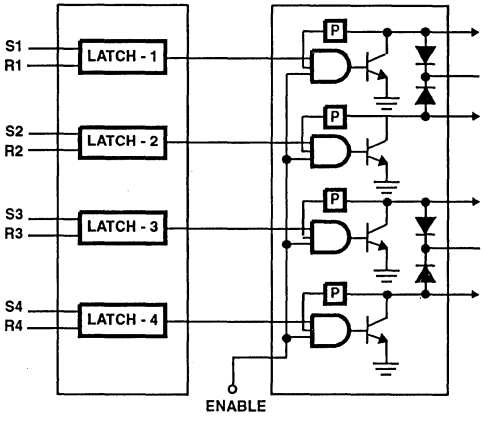


FIGURE 5. TYPICAL APPLICATIONS FOR THE CA3242 QUAD DRIVER

HARRIS SEMICONDUCTOR

CA3262

PRELIMINARY

May 1992

Quad-Gated Inverting Power Driver

Features

- Independent Over-Current Limiting On Each Output
- Independent Over-Temperature Limiting On Each Output
- Output Drivers Capable of Switching 700mA Load
- Inputs Compatible With TTL or 5V CMOS Logic
- Suitable For Resistive, Lamp or Inductive Loads
- Power-Frame Construction For Good Heat Dissipation
- Operational Temperature Ranges
  - CA3262A ..... -40°C to +125°C
  - CA3262 ..... -40°C to +85°C

Applications

- Solenoid
- Relay
- Light
- Steppers
- Motors
- Displays

System Applications

- Automotive
- Appliance
- Industrial Control
- Robotics

Description

The CA3262 is used to interface Low-Level Logic to High Current Loads. Each Power Driver has four inverting switches consisting of a non-inverting logic input stage and an inverting low-side driver output stage. All input stages have a common enable input. Each output device has independent current limiting (I_{LIM}) and thermal limiting (T_{LIM}) for protection from over-load conditions. Steering diodes in the outputs are used in conjunction with external zener diodes to protect the IC against over-voltage transients due switching of inductive loads. To allow for maximum heat transfer from the chip, all ground pins on the DIP and PLCC package are directly connected to the mounting pad of the chip.

The CA3262 can drive four incandescent lamp loads without modulating their brilliance when the "cold" lamps are energized.

Outputs can be paralleled to drive large loads. The maximum output current is determined by the minimum limit for over-current limiting which is typically 1.2 Amps but may be as low as 0.7 Amps.

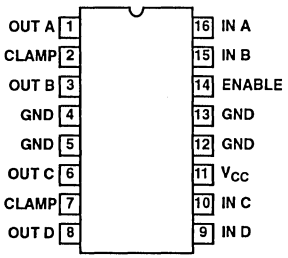
The best choice for over-voltage protection is to provide zener clamping diodes connected to the CLAMP pins with inductive loads. A typical zener diode voltage value for the CA3262 is 30 Volts or a value sufficient to guarantee that the CA3262 output does not exceed the sustaining voltage limit of 40 Volts when the zener diode is conducting. (Continued on 2-8)

Ordering Information

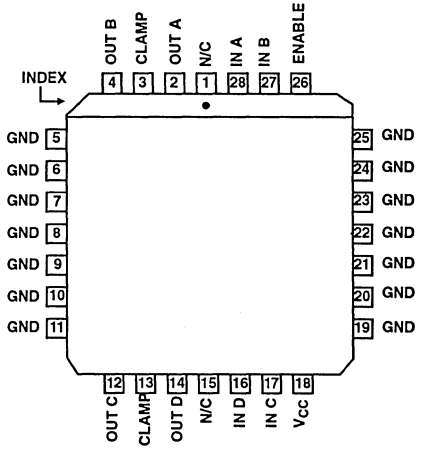
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3262E	-40°C to +85°C	16 Pin DIP
CA3262AE	-40°C to +125°C	16 Pin DIP
CA3262AQ	-40°C to +125°C	28 Pin PLCC

Pinouts

16 LEAD (DIP (E SUFFIX)
TOP VIEW



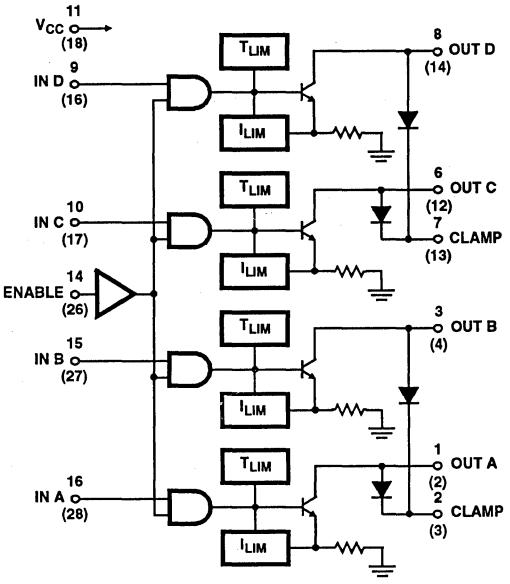
28 LEAD PLCC (Q SUFFIX)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1836.1**

Functional Block Diagram



NOTES:

1. Pins 4, 5, 12, 13 ground (Package E)
2. Pins 5-11, 19-25 ground (Package Q)
3. Pin numbers in parentheses apply to the Plastic 28 Leaded Chip Carrier (PLCC)

TRUTH TABLE

ENABLE	IN	OUT
H	5H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

Description (Continued)

Over-voltage protection may or may-not be satisfied by connecting the CLAMP pin to a positive voltage equal or greater than the output load power supply. In many applications transient variations and non-tracking conditions may allow forward conduction through the steering diodes, further up-setting an unstable condition.

Current-limiting is provided as protection for shorted or over-loaded output conditions. Voltage is sampled across a small metal resistor in the emitter of each output stage. When the voltage exceeds a preset comparator level, drive is reduced to the output. Current limiting is sustained unless thermal conditions exceed the preset thermal shutdown temperature of 155°C.

If an output is shorted, the remaining three outputs will continue to function normally unless the continued heat spreading is sufficient to raise the junction temperature at any other output to a level greater than 155°C. High ambient temperature conditions may allow this to happen. The degree of interaction is minimized by separation of the output devices, each to a separate corner of the chip. The output stage does not oscillate when in the current limiting or thermal limiting mode.

As noted, the thermal resistance of both the DIP and PLCC packages are improved by direct connection of the leads to the chip mounting pad. In free air, the junction-to-air thermal resistance, θ_{JA} is 50°C/W (typical) for the DIP package and 40°C/W (typical) for the PLCC package. This coefficient can be lowered to 40°C/W and 30°C/W respectively by suitable design of the PC board to which the CA3262 is soldered.

Absolute Maximum Ratings

Logic Supply Voltage, V_{CC} 7.0V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} 60V
Output Sustaining Voltage, $V_{CE(SUS)}$ 40V
Output Current, I_O 1A
Storage Temperature Range ..... -65°C to +150°C
Operating Temperature Range:
CA3262AE, CA3262AQ ..... -40°C to +125°C
CA3262E ..... -40°C to +85°C
Thermal Resistance, θ_{ja}:
CA3262AQ ..... 43°C/W
CA3262E, CA3262AE ..... 60°C/W
Maximum Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

Power Dissipation, P_D:
CA3262E, CA3262AE:
Up to +60°C (Free Air) 1.5W
Above +60°C: ..... Derate Linearly at 16.6mW/°C
Up to +90°C w/heat sink (PC Board): 1.5W
Above +90°C;
w/heat sink (PC Board): ..... Derate Linearly at 25mW/°C
CA3262AQ:
Up to +85°C (Free Air): 1.5W
Above +85°C: ..... Derate Linearly at 23mW/°C
Up to +105°C with heat sink (PC Board): 1.5W
Above +105°C;
with heat sink (PC Board): ..... Derate Linearly at 33mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

At V_{CC} = 5.5V, T_A = -40°C to +125°C, CA3262A; T_A = -40°C to +85°C for CA3262

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3262			CA3262A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Output Leakage Current	I_{CEX}	V_{CE} = 60V, V_{ENABLE} = 0.8V	-	-	100	-	-	50	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 40mA	40	-	-	40	-	-	V
Collector Emitter Saturation Voltage (See Figure 5)	$V_{CE(SAT)}$	V_{IN} = 2V, V_{CC} = 4.75V I_C = 100mA	-	-	0.25	-	-	0.15	V
		I_C = 200mA	-	-	-	-	-	0.2	V
		I_C = 300mA	-	-	-	-	-	0.25	V
		I_C = 400mA	-	-	0.4	-	-	0.3	V
		I_C = 500mA	-	-	-	-	-	0.4	V
		I_C = 600mA	-	-	0.6	-	-	0.5	V
		I_C = 700mA, T_A = -40°C	-	-	0.6	-	-	0.5	V
Input Low Voltage	V_{IL}		-	-	0.8	-	-	0.8	V
Input High Voltage	V_{IH}		2	-	-	2	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	-	-	10	-	-	10	µA
Input High Current	I_{IH}	V_{IN} = V_{ENABLE} = 5.5V, I_C = 600mA	-	-	10	-	-	10	µA
Supply Current All Outputs ON (See Figure 4)	$I_{CC(ON)}$	V_{IN} = 2V, V_{ENABLE} = 5.5V, I_{OUTA} = I_{OUTB} = I_{OUTC} = I_{OUTD} = 250mA	-	-	70	-	-	55	mA
Supply Current All Outputs OFF (See Figure 4)	$I_{CC(OFF)}$	V_{IN} = 0V	-	-	10	-	-	10	mA
Clamp Diode Leakage Current	I_R	V_R = 50V	-	-	100	-	-	50	µA
Clamp Diode Forward Voltage (See Figure 7)	V_F	I_F = 1A, V_{IN} = 0V	-	-	1.7	-	-	1.7	V
		I_F = 1.5A, V_{IN} = 0V	-	-	2.1	-	-	2.1	V
Turn-On Delay (See Figure 6)	t_{PHL}, t_{PLH}	I_{OUT} = 500mA	-	-	10	-	-	10	µs
Over Current Limiting (Note 1)	I_{LIM}	V_{OUT} = 4.5V to 24.5V	0.7	-	1.8	0.7	-	1.8	A
DESIGN PARAMETER									
Over Temperature Limiting (Junction Temperature)	T_{LIM}		-	155	-	-	155	-	°C

NOTE:

1. With voltage on the collector of the output transistor as indicated (V_{OUT} = 4.5V to 24.5V) and with that output transistor turned on, the current will increase to a limiting value which will be a value of 0.7 A, minimum. That output will shortly thereafter (approx. 5ms) go into over-temperature limiting. (Excessive dissipation during thermal limiting may damage the chip.)

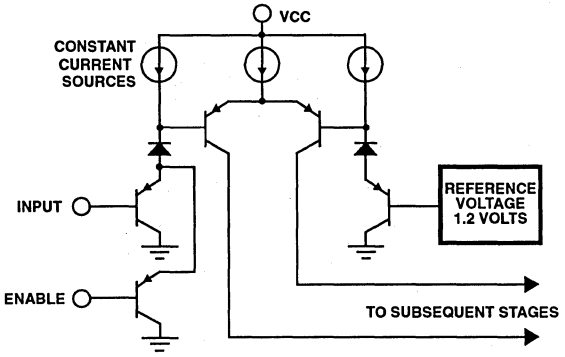


FIGURE 1. CA3262 EQUIVALENT SCHEMATIC OF ONE INPUT STAGE

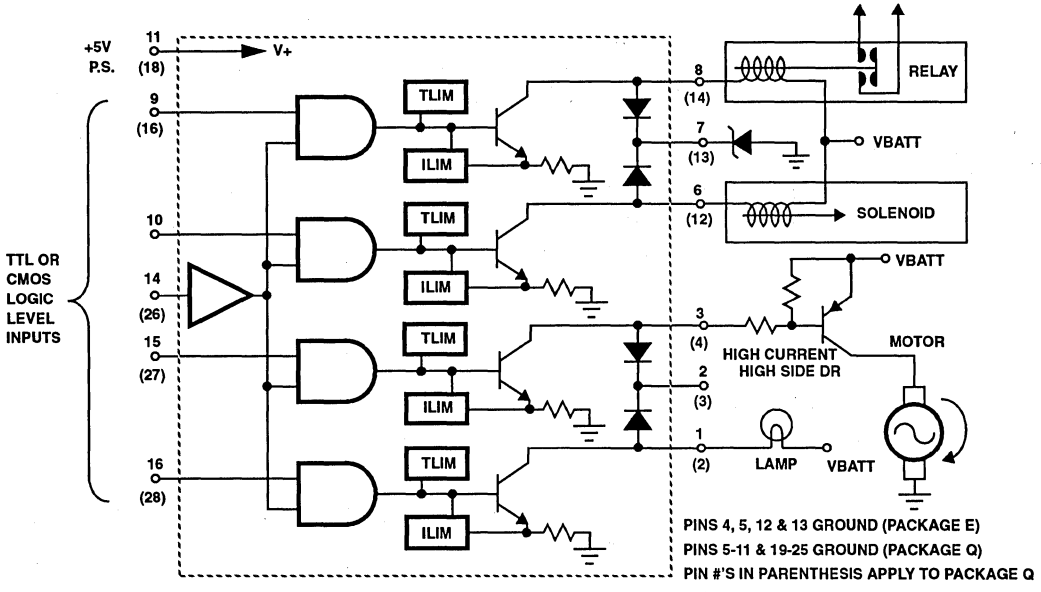
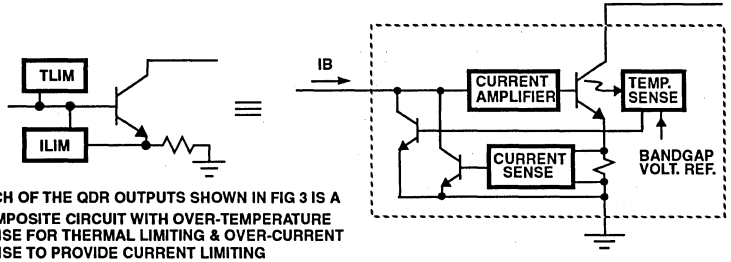


FIGURE 2. QUAD-GATED INVERTING POWER DRIVER (QDR) SCHEMATIC WITH TYPICAL LOAD-DRIVE APPLICATIONS SHOWN. (SEE FIGURE 3)



EACH OF THE QDR OUTPUTS SHOWN IN FIG 3 IS A COMPOSITE CIRCUIT WITH OVER-TEMPERATURE SENSE FOR THERMAL LIMITING & OVER-CURRENT SENSE TO PROVIDE CURRENT LIMITING

FIGURE 3. QUAD-GATED INVERTING POWER DRIVER (QDR) OUTPUT EQUIVALENT CIRCUIT

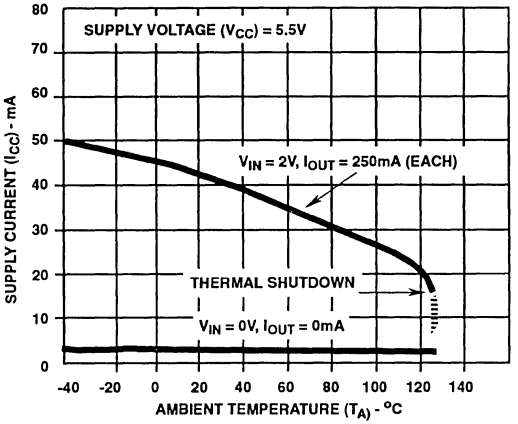


FIGURE 4. TYPICAL SUPPLY CURRENT (PIN 11) CHARACTERISTICS

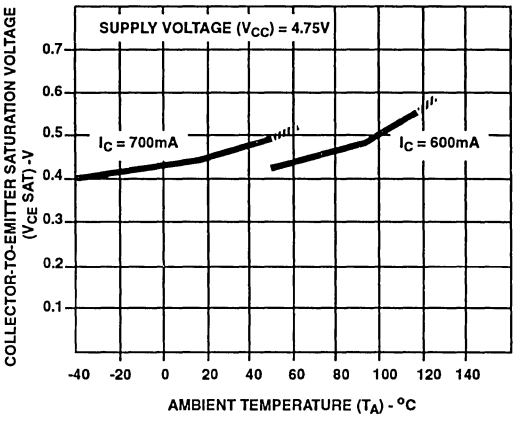


FIGURE 5. TYPICAL COLLECTOR-TO-EMITTER SATURATION VOLTAGE CHARACTERISTICS IN QUAD-GATED INVERTING POWER DRIVER OUTPUT

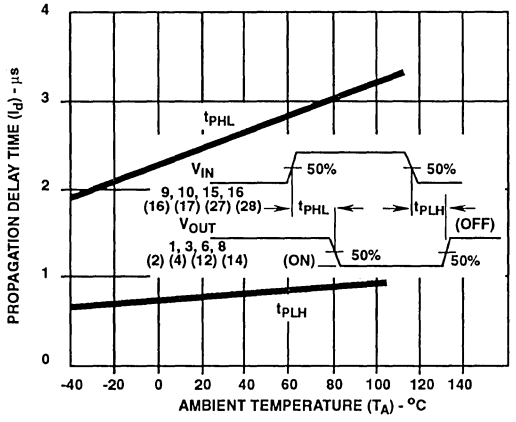


FIGURE 6. TYPICAL PROPAGATION DELAY TIME CHARACTERISTICS

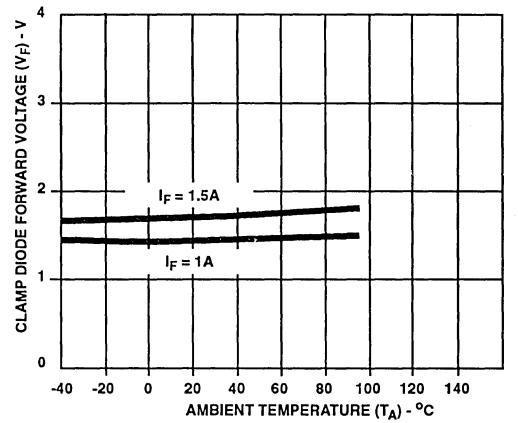


FIGURE 7. TYPICAL CLAMP-DIODE FORWARD VOLTAGE CHARACTERISTICS

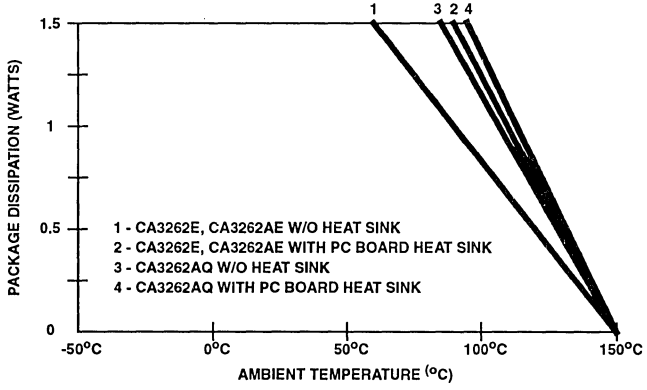


FIGURE 8. PACKAGE DISSIPATION RATING CHART

HARRIS SEMICONDUCTOR

CA3272

Quad-Gated Inverting Power Driver With Fault Mode Diagnostic Flag Output

May 1992

Features

- Independent Over-Current Limiting on Each Output
- Independent Over-Temperature Shutdown With Hysteresis on Each Output
- Capable of Switching 600mA Load Currents
- Inputs Compatible With TTL or 5 Volt CMOS Logic
- Suitable For Resistive or Inductive Loads
- Power-Frame Construction for Good Heat Dissipation
- Fault Mode Output Flag
- Operating Temperature Range . . . . . -40°C to +125°C

Applications

- Solenoid
- Relay
- Light
- Steppers
- Motors
- Displays

System Applications

- Automotive
- Appliance
- Industrial Control
- Robotics

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3272	-40°C to +125°C	28 Lead PLCC

Description

The CA3272 quad-power NAND driver contains four NAND-gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters, incandescent displays, and vacuum fluorescent displays.

To allow for maximum heat transfer from the chip, all ground leads are directly connected to the die substrate and to the ground bond pads. In free air, junction-to-air thermal resistance ($R_{\theta JA}$) is 40°C/W (typical).

This coefficient can be lowered to 30°C/W (typical) by suitable design of the PC board to which the CA3272 is soldered.

The individual outputs are protected with over-current limiting (I_{LIM}) and over-temperature (T_{LIM}) shutdown. Any one output that faults (see Fault Logic Table) will switch Pin 1 to a constant current pulldown.

If an output load is shorted, the remaining three outputs function normally unless the junction temperature (typically +165°C) of those outputs is exceeded. The output stage does not change state (oscillate) when in the current limit mode.

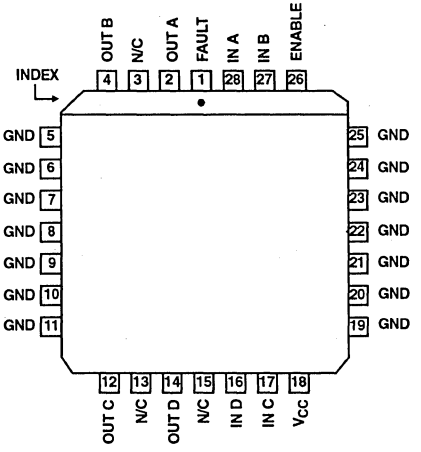
All inputs and enable have internal pulldowns to turn "off" the outputs when inputs are floating.

The CA3272 can drive four incandescent lamp loads without modulating their brilliance when "cold" lamps are energized. Outputs can be "ganged" to drive large loads.

The CA3272 is supplied in a plastic 28 leaded chip carrier, PLCC (Q suffix).

Pinout

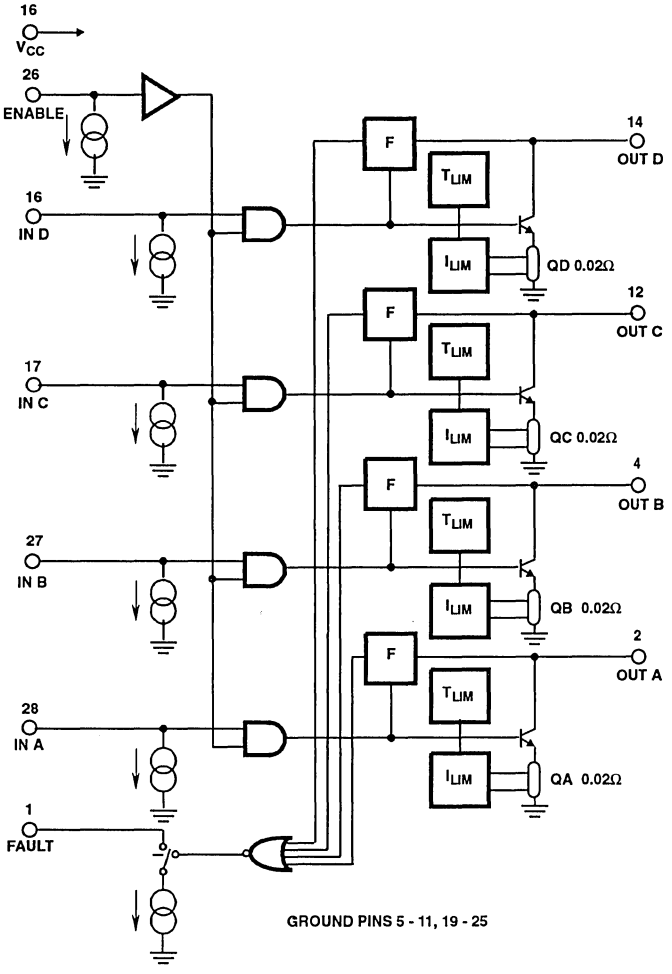
PLASTIC 28 LEADED CHIP CARRIER (PLCC)
(Q SUFFIX)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2223.1**

Block Diagram



TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	X	H

H = High, L = Low, X = Don't Care

FAULT LOGIC TABLE

IN	OUT	FAULT	MODE
H	L	H	Normal
H	H	L	Over Current, Over Temperature or Short to Power Supply
L	L	L	
L	H	H	Normal

Absolute Maximum Ratings (T_A = +25°C) Unless Otherwise Specified

Logic Supply Voltage, V_{CC} 7V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CEX} . . . . . -12, +50V_{DC}
Output Sustaining Voltage, $V_{CE(SUS)}$ . . . . . 40V_{DC}
Output Current, I_O . . . . . 1.6A_{DC}
Power Dissipation, P_D
Up to 85°C 1.5W
Above 85°C . . . . . Derate Linearly at 23mW/°C
Up to 105°C w/Heat Sink (PC Board) 1.5W
Above 105°C w/Heat Sink (PC Board) . . . Derate Linearly at 33mW/°C

Ambient Temperature Range
Operating . . . . . -40°C to +125°C
Storage . . . . . -55°C to +150°C
Maximum Junction Temperature, T_J . . . . . +150°C
Maximum Thermal Resistance
Junction-to-Air, θ_{JA} . . . . . 43°C/W
Lead Temperature (During Soldering)
At distance $^1/_{16} \pm {}^1/_{32}$" (1.59 ± 0.79mm) from
case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = -40°C to +125°C, V_{CC} = 5V Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Output Leakage Current	I_{CEX}	V_{CE} = 50V, V_{ENABLE} = 0.8V	-	100	µA
Output Sustaining Voltage	$V_{CE(SUS)}$	I_C = 40mA	40	-	V
Collector Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 400mA, V_{IN} = 2V, V_{CC} = 4.75V, T_A = +125°C	-	0.4	V
		I_C = 500mA, V_{IN} = 2V, V_{CC} = 4.75V, T_A = +25°C	-	0.5	V
		I_C = 600mA, V_{IN} = 2V, V_{CC} = 4.75V, T_A = -40°C	-	0.6	V
Input Low Voltage	V_{IL}		-	0.8	V
Input Low Current	I_{IL}	V_{IN} = 0.8V	10	60	µA
Input High Voltage	V_{IH}		2	-	V
Input High Current	I_{IH}	V_{IN} = 5.5V, V_{ENABLE} = 5.5V	10	60	µA
Supply Current ON (All Outputs ON)	$I_{CC(ON)}$	I_{OUT}(A, B, C, D) = 250mA, V_{IN} = 2V V_{ENABLE} = 5.5V	-	60	mA
Supply Current OFF (All Outputs OFF)	$I_{CC(OFF)}$	V_{IN} = 0V	-	10	mA
Turn-On Delay	t_{PHL}, t_{PLH}		-	10	µs
Over Current Limiting* (For Each Output)		V_{OUT} = 4.5V to 24.5V, R_L(Min) = 4Ω	0.7	1.6	A
Fault Output	I_{OL}	I_{LOAD} = 30µA	40	80	µA
	I_{OH}		-	2	µA
	V_{OL}		-	0.4	V
Output Sense Thresholds	V_{HT}	Input = 2V Min	3	5.5	V
	V_{LT}	Input = 0.8V Max	3	5.5	V
DESIGN PARAMETER					
Over Temperature Limiting (Junction Temperature)			165 (Typical)		°C

* With voltage on the collector of the output transistor as indicated (V_{OUT} = 4.5V to 24.5V) and with that output transistor turned on, the current will increase to a limiting value which will be a value of 0.7A minimum. That output will shortly (≈5ms) thereafter go into over temperature shutdown. (Excessive dissipation during thermal shutdown may damage the chip.)

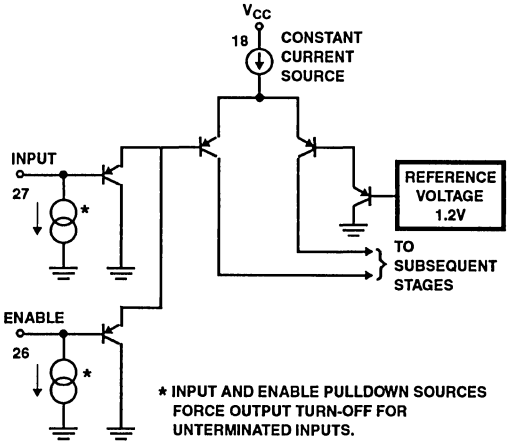


FIGURE 1. SCHEMATIC OF ONE INPUT SECTION

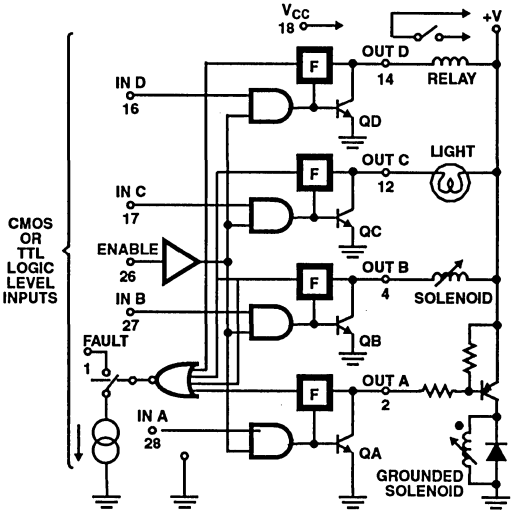


FIGURE 2. QUAD-GATED INVERTING POWER DRIVER (QDR) SCHEMATIC WITH TYPICAL LOAD-DRIVE APPLICATIONS SHOWN (SEE FIGURE 3)

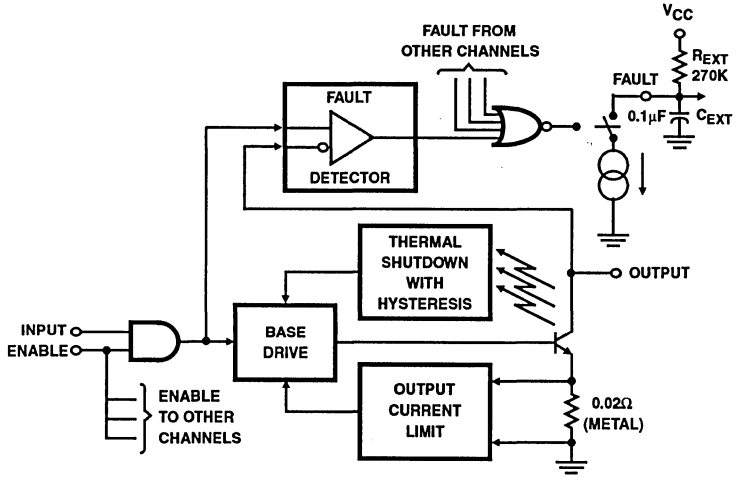


FIGURE 3. QUAD-GATED INVERTING POWER DRIVER (QDR) OUTPUT EQUIVALENT CIRCUIT. THE FAULT OUTPUT REQUIRES A PULL-UP LOAD SUCH AS AN EXTERNAL RESISTOR (R_{EXT}). A CAPACITOR, C_{EXT} SHOULD BE USED TO SUPPRESS SWITCHING SPIKES

HARRIS SEMICONDUCTOR

CA3282

PRELIMINARY

May 1992

CMOS Octal Serial Solenoid Driver

Features

- Eight Open Collector Drivers
- Capable of 1A Per Output
- Capable of 0.5A All Outputs "ON"
- Transient Protection
- Current Limiting
- Individual Output Latch
- Individual Fault Unlatch & Feedback
- Common Reset Line
- Operating Temperature Range . . . . . -40°C to +125°C
- High Voltage Power BiMOS

Applications

- Logic & µP Controlled Drivers
- Solenoids, Relays & Lamp Drivers
- Automotive & Industrial Systems
- Robotic Controls

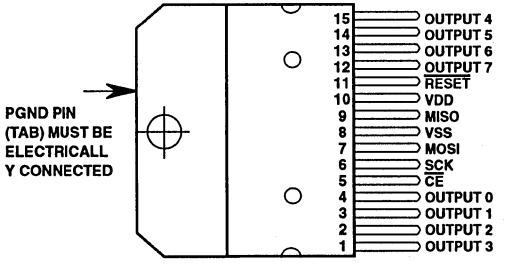
Description

The CA3282 is a logic controlled, eight channel octal serial solenoid driver. The serial peripheral interface (SPI) utilized by the CA3282 is a serial synchronous bus compatible with Harris CDP68HC05, or equivalent, microcomputers. The functional diagram for the CA3282 is shown in Figure 1. Each of the open collector output drivers has individual protection for over voltage and over current; each output channel has separate output latch control. Under normal ON conditions, each output driver is in a low, saturation state. Comparators in the diagnostic circuitry monitor the output drivers to determine if an out of saturation condition exists. If a comparator senses a fault, the respective output driver is unlatched. In addition, over current protection is provided with current limiting in each output, independent of the diagnostic feedback loop.

The CA3282 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving lamps, relays, and solenoids in applications where low operating power, high breakdown voltage, and high output current at high temperatures is required.

The CA3282 is supplied in 15 lead Power SIP package with lead forms for either vertical or surface mount.

Pinout



15 LEAD POWER SIP (TOP VIEW)

Block Diagram

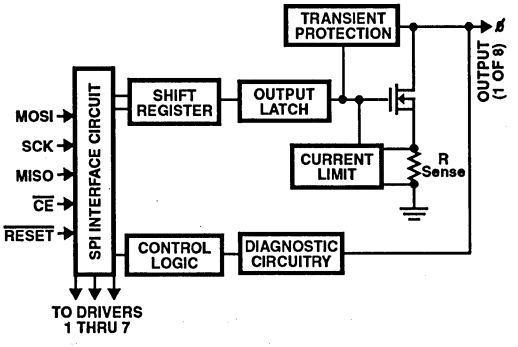


FIGURE 1. BLOCK DIAGRAM OF THE CA3282 OCTAL DRIVER WITH SPI (SERIAL PERIPHERAL INTERFACE) BUS

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
CA3282AS1	-40°C to +125°C	15 Pin Plastic SIP Staggered Vertical
CA3282AS2	-40°C to +125°C	15 Pin Plastic SIP Surface Mount

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2767.2**

Absolute Maximum Ratings

DC Logic Supply, V_{DD} ..... -0.7V to +7.0V
Output Voltage, V_O ..... -0.7V to 40V
Output Current, I_{LOAD} ..... 1A Max
Input Voltage, V_{IN} ..... 7V Max
Operating Temperature Range ..... -40°C to +150°C
Storage Temperature Range (T_{stg}) ..... -55°C to +150°C

Thermal Characteristics

Thermal Resistance Junction-Case, θ_{JC} ..... +3°C/W Max
Thermal Resistance Junction-Ambient, θ_{JA} ..... +35°C/W Max
Lead Temperature (During Soldering):
At distance $^1/_{16} \pm ^1/_{32}$ In. (1.59 ± 0.79mm)
from case for 10s max ..... +265°C

Electrical Specifications V_{DD} = -5V ± 5%, T_j = -40°C to +125°C; Unless Otherwise Specified.

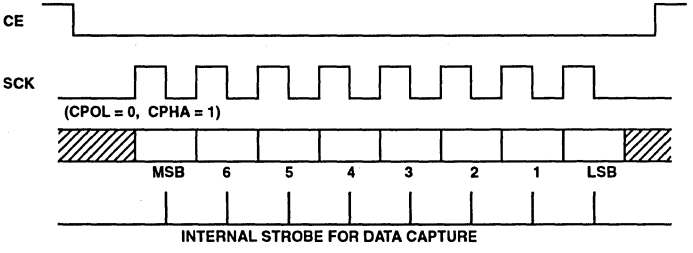
PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Quiescent Supply Current	I_{DD}	All Outputs ON, 0.5A Load Per Output		5	10	mA
Output Clamping Voltage	V_{OC}	I_{LOAD} = 0.5A, Output Programmed OFF	30	32	40	V
Output Clamping Energy	E_{OC}	I_{LOAD} = 0.5A, Output ON	20			mJ
Output Leakage Current	$I_{O\ LEAK}$	Output Programmed OFF				
		V_O = 24V		150	1000	µA
		V_O = 14V		150	500	µA
		V_O = 5V		150	200	µA
Output Saturation Voltage	V_{SAT}	Output Programmed ON				
		I_{LOAD} = 0.5A		0.3	0.5	V
		I_{LOAD} = 0.75A		0.4	1.25	V
		I_{LOAD} = 1.0A		0.6	2.0	V
Output Current Limit	$I_{O\ LIMIT}$	Output Programmed ON, V_{OUT} > 3V	1.05	1.5		A
Turn-On Delay	t_{PHL}	I_O = 500 mA, No Reactive Load		1	10	µs
Turn-Off Delay	t_{PLH}	I_O = 500 mA, No Reactive Load		2	10	µs
Fault Reference Voltage	$V_{O\ REF}$	Output Programmed ON, Fault Detected If $V_O > V_{O\ REF}$	1.6	1.8	2.0	V
Fault Reset Delay (After $\overline{CE}$ Low to High Transition)	t_{UD}	See Figure 2	TBD	65	250	µs
Output OFF Voltage	V_{OFF}	Output Programmed OFF, Output Pin Floating		0	1	V
LOGIC INPUTS (MOSI, $\overline{CE}$, SCK and $\overline{RESET}$)						
Threshold Voltage at Falling Edge	V_{T-}	V_{DD} = 5V ±10%	$0.2V_{DD}$	$0.3V_{DD}$		V
Threshold Voltage at Rising Edge	V_{T+}	V_{DD} = 5V ±10%		$0.6V_{DD}$	$0.7V_{DD}$	V
Hysteresis Voltage	V_H	$V_{T+} - V_{T-}$	0.85	1.4	2.25	V
Input Current	I_I	V_{DD} = 5.5V, 0 < V_I < V_{DD}	-10		+10	µA
Input Capacitance	C_I	0 < V_I < V_{DD}			20	pF
LOGIC OUTPUT (MISO)						
Output LOW Voltage	V_{OL}	I_{OL} = 1.6 mA		0.2	0.4	V
Output HIGH Voltage	V_{OH}	I_{OL} = 0.8 mA	V_{DD} -1.3V	V_{DD} -0.2V		V
Output Tristate Leakage Current	I_{OL}	V_{DD} = 5.25V, 0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High	-10		+10	µA
Output Capacitance	C_{OUT}	0 < V_O < V_{DD}, $\overline{CE}$ Pin Held High			20	pF

Serial Peripheral Interface Timing (See Figure 2)

PARAMETERS	SYMBOL		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Frequency		f_{OPER}		D.C.	Note 1	1.0	MHz
Cycle Time	(1)	t_{CYC}		1.0	0.1		µs
Enable Lead Time	(2)	t_{LEAD}			<100	1000	ns
Enable Lag Time	(3)	t_{LAG}			<100	1000	ns
Clock HIGH Time	(4)	t_{WSCKH}		410	50		ns
Clock LOW Time	(5)	t_{WSCKL}		410	50		ns
Data Setup Time	(6)	t_{SU}		150	20		ns
Data Hold Time	(7)	t_H		150	20		ns
Enable Time	(8)	t_{EN}			50	1000	ns
Disable Time	(9)	t_{DIS}			150	1000	ns
Data Valid Time	(10)	t_V			75	360	ns
Output Data Hold Time	(11)	t_{HO}		0	50		ns
Rise Time (MISO Output)	(12)	t_{rSO}	V_{DD} = 20% to 70%, C_L = 200pF		35	150	ns
Rise Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(12)	t_{rSI}	V_{DD} = 20% to 70%, C_L = 200pF			90	ns
Fall Time (MISO Output)	(13)	t_{fSO}	V_{DD} = 20% to 70%, C_L = 200pF		45	150	ns
Fall Time SPI Inputs (SCK, MOSI, $\overline{CE}$)	(13)	t_{fSI}	V_{DD} = 20% to 70%, C_L = 200pF			90	ns

NOTE:

1. Operating Frequency is typically greater than 10MHz but it is application limited primarily by external SPI input rise/fall times and MISO output loading.



DATA AND CLOCK TIMING

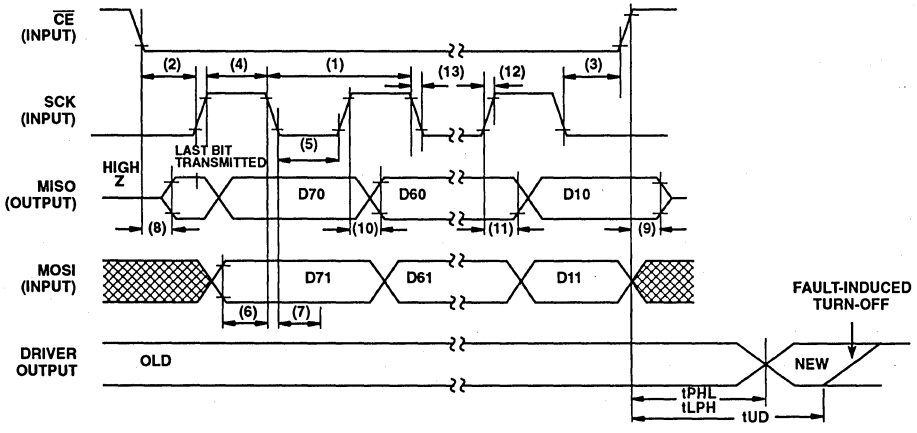


FIGURE 2. SPI TIMING

Signal Descriptions

Output 0 - Output 7 - Power Output Drivers. The input and output bits corresponding to Output 0 thru Output 7 are transmitted and received most significant bit (MSB) first via the SPI bus. The outputs are provided with current limiting and voltage sense functions for fault indication and protection. The nominal load current for these outputs is 500mA, with current limiting set to a minimum of 1.05A. An on chip clamp circuit capable of handling 500mA is provided at each output for clamping inductive loads.

$\overline{\text{RESET}}$ - Active low reset input. When this input line is low, the shift register and output latches are configured to turn off all output drivers. A power on clear function may be implemented by connecting this pin to V_{DD} with an external resistor, and to V_{SS} with an external capacitor. In any case, this pin must not be left floating.

$\overline{\text{CE}}$ - Active low chip enable. Data is transferred from the shift register to the outputs on the rising edge of this signal. The falling edge of $\overline{\text{CE}}$ loads the shift register with the output voltage sense bits coming from the output stages. The output driver for the MISO pin is enabled when this pin is low. $\overline{\text{CE}}$ must be a logic low prior to the first serial clock (SCK) and must remain low until after the last (eighth) serial clock cycle. A low level on $\overline{\text{CE}}$ also activates an internal disable circuit used for unlatching output states that are in a fault mode as sensed by an out of saturation condition. A high on $\overline{\text{CE}}$ forces MISO to a high impedance state. Also, when $\overline{\text{CE}}$ is high, the octal driver ignores the SCK and MOSI signals.

SCK, MISO, MOSI - See Serial Peripheral Interface (SPI) section in this data sheet.

V_{DD} and V_{SS} - Positive and negative power supply lines.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) utilized by the CA3282 is a serial synchronous bus for control and data transfers. The clock (SCK), which is generated by the microcomputer, is active only during data transfers. In systems using CDP68HC05 family microcomputers, the inactive clock polarity is determined by the CPOL bit in the microcomputer's control register. The CPOL bit is used in conjunction with the clock phase bit, CPHA to produce the desired clock data relationship between the microcomputer and octal driver. The CPHA bit in general selects the clock edge which captures data and allows it to change states. For the CA3282, the CPOL bit must be set to a logic zero and the CPHA bit to a logic one. Configured in this manner, MISO (output) data will appear with every rising edge of SCK, and MOSI (input) data will be latched into the shift register with every falling edge of SCK. Also, the steady state value of the inactive serial clock, SCK, will be at a low level. Timing diagrams for the serial peripheral interface are shown in Figure 2.

SPI Signal Descriptions

MOSI (Master Out/Slave In) - Serial data input. Data bytes are shifted in at this pin, most significant bit (MSB) first. The data is passed directly to the shift register which in turn controls the latches and output drivers. A logic "0" on this pin will program the corresponding output to be ON, and a logic "1" will turn it OFF.

MISO (Master In/ Slave Out) - Serial data output. Data bytes are shifted out at this pin, most significant bit (MSB) first. This pin is the serial output from the shift register and is tri stated when CE is high. A high for a data bit on this pin indicates that the corresponding output is high. A low on this pin for a data bit indicates that the output is low. Comparing the serial output bits with the previous input bits, the microcomputer implements the diagnostic data supplied by the CA3282.

SCK - Serial clock input. This signal clocks the shift register. New MISO (output) data will appear on every rising edge of SCK and new MOSI (input) data will be latched into the shift register on every falling edge of SCK. The SCK phase bit, CPHA, and polarity bit, CPOL, must be set to 1 and 0, respectively in the microcomputer's control register.

Functional Description

The CA3282 is a low operating power, high voltage, high current, octal, serial solenoid driver featuring eight channels of open collector drivers. The drivers have low saturation voltage and output short circuit protection, suitable for driving resistive or inductive loads such as lamps, relays and solenoids. Data is transmitted to the device serially using the Serial Peripheral Interface (SPI) protocol. Each channel is independently controlled by an output latch and a common $\overline{\text{RESET}}$ line that disables all eight outputs. Byte timing with asynchronous reset is shown in Figure 3. The circuit receives 8 bit serial data by means of the serial input (MOSI), and stores this data in an internal register to control the output drivers. The serial output (MISO) provides 8 bit diagnostic data representing the voltage level at the driver output. This allows the microcomputer to diagnose the condition at the output drivers. The device is selected when the chip enable ($\overline{\text{CE}}$) line is low. When $\overline{\text{CE}}$ is high, the device is deselected and the serial output (MISO) is placed in a tri state mode. The device shifts serial data on the rising edge of the serial clock (SCK), and latches data on the falling edge. On the rising edge of chip enable ($\overline{\text{CE}}$), new input data from the shift register is latched in the output drivers. The falling edge of chip enable ($\overline{\text{CE}}$) transfers the output driver fault information back to the shift register. The output drivers have low ON voltage at rated current, and are monitored by a comparator for an out of saturation condition, in which case the output driver with the fault becomes unlatched and diagnostic data is sent to the microcomputer via the MISO line. A typical microcomputer interface circuit is shown in Figure 4. This circuit is also cascadable with another octal driver.

Shift Register

The shift register has both serial and parallel inputs and outputs. Serial output and input data are simultaneously transferred to and from the SPI bus. The parallel outputs are latched into the output latch in the CA3282 at the end of a data transfer. The parallel inputs jam diagnostic data into the shift register at the beginning of a data transfer cycle.

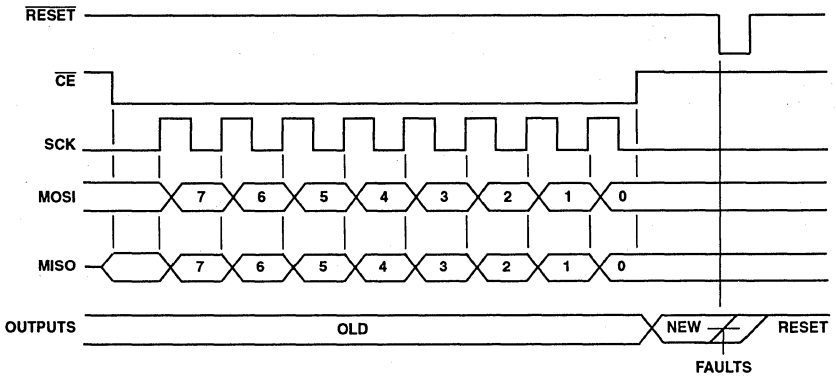


FIGURE 3. BYTE TIMING WITH ASYNCHRONOUS RESET

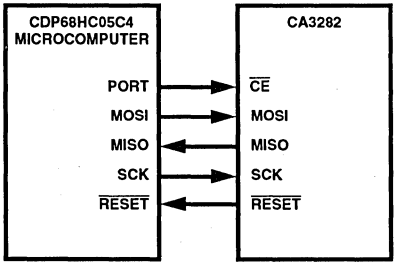


FIGURE 4. TYPICAL MICROCOMPUTER INTERFACE WITH THE CA3282

Output Latch

The output latch holds input data from the shift register which is used to activate the outputs. The latch circuit may be cleared by a fault condition (to protect the overloaded outputs), or by the $\overline{\text{RESET}}$ signal.

Output Drivers

The output drivers provide an active low output of 500mA nominal with current limiting set to 1.05A to allow for high inrush currents. In addition, each output is provided with a voltage clamp circuit to limit inductive transients. Each output driver is also monitored by a comparator for an out of saturation condition. If the output voltage of an ON output pin exceeds the saturation voltage limit, a fault condition is assumed and the latch driving this output is reset, turning the output off. The output comparators, which also provide diagnostic feedback data to the shift register, contain an internal pulldown current which will cause the cell to indicate a low output voltage if the output is programmed OFF and the output pin is open circuited.

$\overline{\text{CE}}$ High to Low Transition

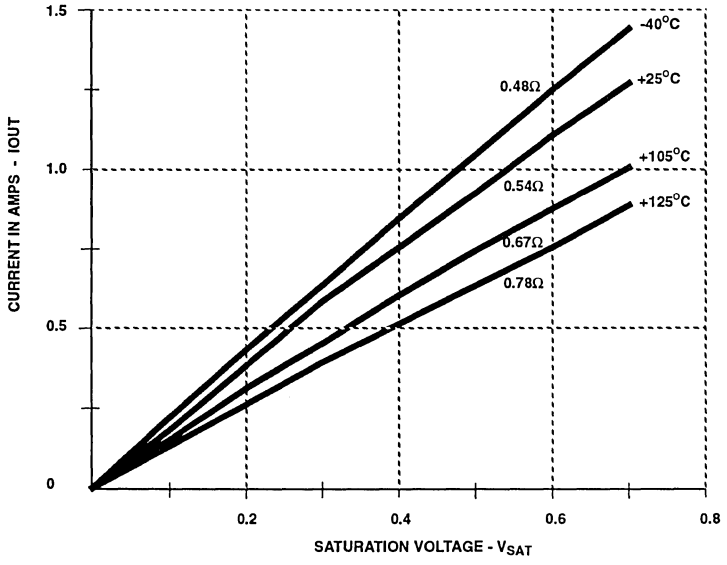
When $\overline{\text{CE}}$ is low, the tri-state MISO pin is enabled. On the falling edge of $\overline{\text{CE}}$, diagnostic data from the output voltage comparators will be latched into the shift register. If an output is high, a logic one will be loaded into that bit in the shift register. If the output is low, a logic zero will be loaded. During the time that $\overline{\text{CE}}$ is low, data bytes controlling the output drivers are shifted in at the MOSI pin most significant bit (MSB) first. A logic zero on this pin will program the corresponding output to be ON, and a logic one will turn it OFF

$\overline{\text{CE}}$ Low to High Transition

When the last data bit has been shifted into the CA3282, the $\overline{\text{CE}}$ pin should be pulled high. At the rising edge of $\overline{\text{CE}}$, shift register data is latched into the output latch and the outputs are activated with the new data. An internal 150msec delay timer will start at this rising edge to compensate for high inrush currents in lamps and inductive loads. During this period, the outputs will be protected only by the analog current limiting circuits since resetting of the output latches by fault conditions will be inhibited during this time. This allows the device to handle inrush currents immediately after turn on. When the 150msec delay has elapsed, the out-put voltages are sensed by the comparators and any out of saturation outputs are latched off. The serial clock input pin (SCK) should be low during $\overline{\text{CE}}$ transitions to avoid false clocking of the shift register. The SCK input is gated by $\overline{\text{CE}}$ so that the SCK input is ignored when $\overline{\text{CE}}$ is high.

Detecting Fault Conditions

Fault conditions may be checked as follows. Clock in a new control byte and wait approximately 150msec to allow the outputs to settle. Clock in the same control byte and note the diagnostic data output at the MISO pin. The diagnostic bits should be identical to the data clocked in. Any differences will indicate a fault at the corresponding outputs. For example, if an output was programmed ON by clocking in a zero, and the corresponding diagnostic bit for that output is a one, indicating the driver output is still high, then a short circuit or overload condition may have caused the output to unlatch. Alternatively, if the output was programmed OFF by clocking in one, and the diagnostic bit for that output shows a zero, then the probable cause is an open circuit resulting in a floating output.



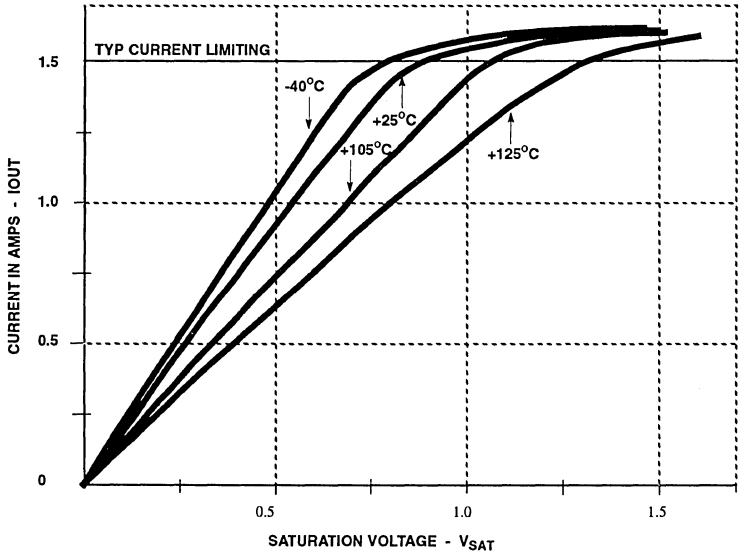


FIGURE 5. CA3282 TYPICAL OUTPUT DRIVER vs V_{SAT}

HARRIS SEMICONDUCTOR

CA3292

ADVANCED INFORMATION

May 1992

Quad-Gated Inverting Power Driver With Fault Mode Diagnostic Flag Output

Features

- Load Current Switch 600mA
- Suitable for Resistive or Inductive Loads
- Fault Mode Diagnostic Flag Output
- Over-Voltage Zener Clamp
- Independent Over-Current Limiting
- Independent Over-Temperature Shutdown
- Temperature Shutdown Hysteresis
- Operating Temperature ..... -40°C to +125°C
- High Dissipation Power-Frame Package
- 5 Volt CMOS or TTL Input Logic

Applications

- Drivers For:
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use:
  - Automobiles
  - Appliances
  - Industrial
  - Robotics

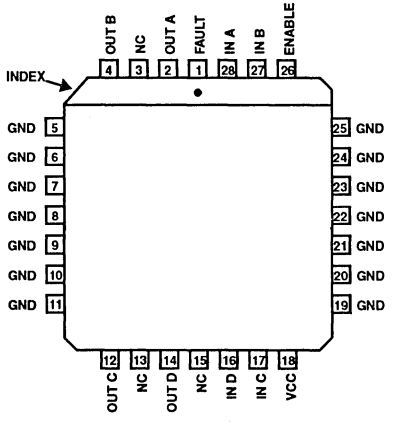
Description

The CA3292 quad-power NAND driver contains four NAND-gate switches for interfacing low-level logic to inductive and resistive loads such as: relays, solenoids, AC and DC motors, heaters and incandescent displays. The CA3292 is similar to the CA3272, except for zener diode over-voltage clamp protection on each output. Each output is protected for current limiting, over-temperature shutdown and has diagnostic feedback to indicate fault conditions.

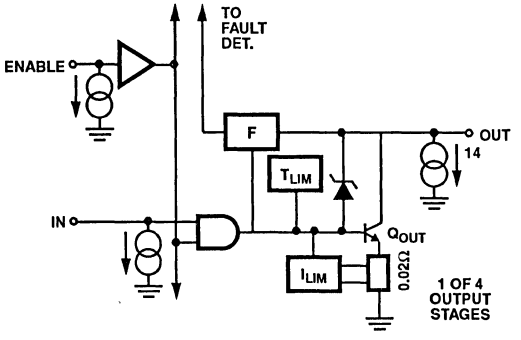
The FAULT DETECTOR block diagram of the CA3292 is shown in Figure 1 in an equivalent logic form while the function block diagram with all four switches is shown in Figure 2. Channel A is one of the 4 power switching functions displayed in the FAULT DETECTOR diagram. Transistor Q_A is the protected power transistor switch that drives the "OUT A" terminal. The dotted block outlines the logic block associated with the FAULT DETECTOR. The ENABLE input is common to each of the 4 power switches and, when low, disables the FAULT output. From the "IN A" input to the "OUT A" output, the switch condition is inverting (NAND). When IN is high, OUT is low and the switch is conducting. The FAULT DETECTOR senses the IN and OUT states and switches Q_F "ON" if a fault is detected. When a fault is detected, transistor Q_F activates a sink current source to pull-down the FAULT pin to a 0 (low) state. Both shorted and open load conditions are detected.

Pinout

PLASTIC 28-LEADED PLASTIC LEADED CHIP CARRIER
(JEDEC MO-047AB)
(Q SUFFIX)



Block Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3292Q	-40°C +125°C	28 Lead PLCC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2946**

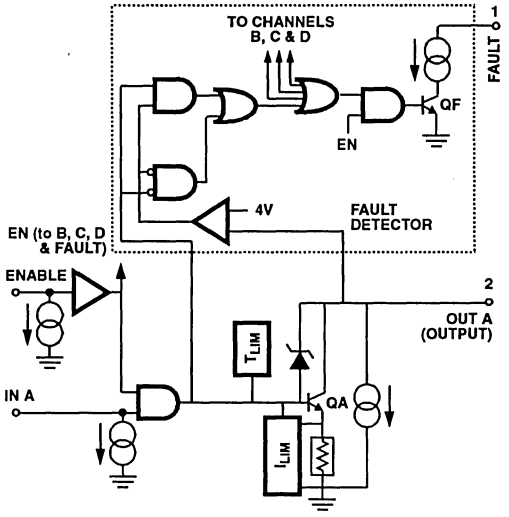
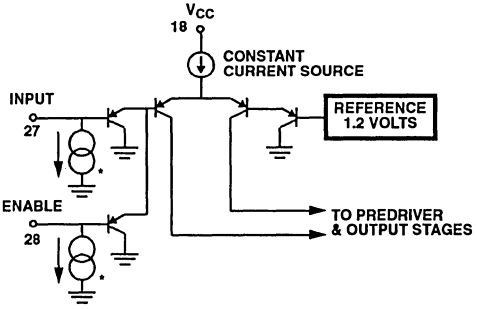


FIGURE 1. FUNCTIONAL BLOCK DIAGRAM OF THE CA3292 FAULT DETECTOR



*INPUT AND ENABLE PULLDOWN SOURCES FORCE OUTPUT TURN-OFF FOR ALL UNDETERMINATED INPUTS

FIGURE 3. SCHEMATIC OF ONE INPUT STAGE

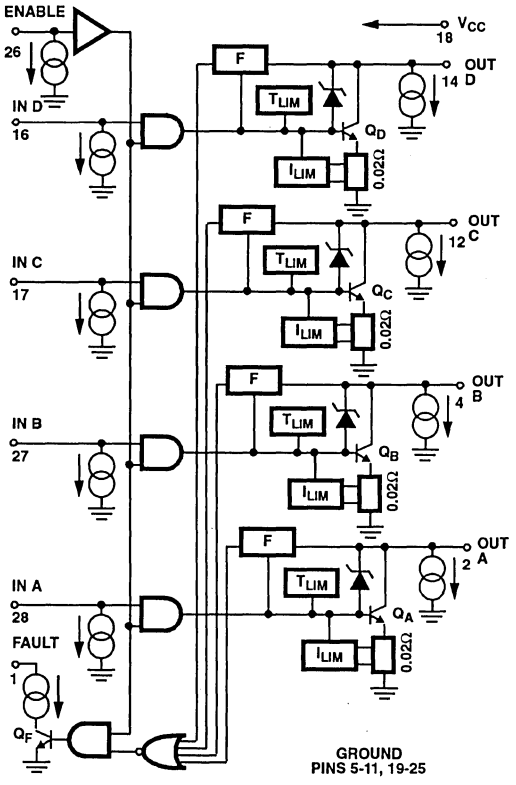


FIGURE 2. CA3292 FUNCTIONAL BLOCK DIAGRAM SHOWING ALL OUTPUTS

TRUTH TABLE

ENABLE	IN	OUT
H	H	L
H	L	H
L	DON'T CARE	H

FAULT LOGIC TABLE

IN	OUT	FAULT	MODE
H	L	H	NORMAL
H L	H L	L L	Over current or over temperature or output short to power supple
L	H	H	Normal

Absolute Maximum Ratings

Logic Input Supply Voltage, V_{CC} ..... +7.0V
Logic Input Voltage, V_{IN} 15V
Output Voltage, V_{CLAMP} ..... (Note1)
Output Sustaining Voltage, $V_{CE(SUS)}$ ..... (Note1)
Output Current, I_O 1.6A
Power Dissipation:
Up to 85°C 1.5W
Above 85°C ..... Derate Linearly at 23mW/°C
Above 105°C w/heat sink (PC Board) . Derate Linearly at 33mW/°C
Up to 125°C w/heat sink (PC Board) 1.0W
Above 125°C w/ heat sink (PC Board) . Derate Linearly at 33mW/°C

Ambient Temperature Range:
Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +150°C
Maximum Junction Temperature, T_j ..... +150°C
Maximum Thermal Resistance:
Junction-to-Air, $R_{\theta JA}$ ..... 43°C/W
Lead Temperature (During Soldering):
At distance $^1/_{16} \pm {}^1/_{32}$ in. (1.59 ± 0.79 mm) from
case for 10s max. ..... 265 °C

NOTE:

1. The output voltage level is limited by the clamping action of the internal zener diode. See the clamp voltage limits specified in the electrical characteristics table.

Electrical Specifications At T_A = -40°C to +125°C, V_{CC} = 5.5V Except as Noted.

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Leakage Current	I_{CEX}	V_{CE} 24V, V_{ENABLE} = 0.8V			100	µA
Output Clamp Voltage	V_{CLAMP}	I_{CE} = 300µA	28		40	
COLLECTOR EMITTER SATURATION VOLTAGE:	$V_{CE(SAT)}$	I_C = 400mA, V_{IN} 2V, V_{CC} = 4.75V, T_A = +125°C			0.4	V
		I_C = 500mA, V_{IN} 2V, V_{CC} = 4.75V, T_A = +25°C			0.5	V
		I_C = 600mA, V_{IN} 2V, V_{CC} = 4.75V, T_A = -40°C			0.6	V
LOGIC INPUT THRESHOLDS:						
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN} = 0.8V	10		60	µA
Input High Current	I_{IH}	V_{IN} = 5.5V, V_{ENABLE} = 5.5V	10		60	µA
SUPPLY CURRENT:						
All Outputs ON	$I_{CC(ON)}$	I_{OUT}(A,B,C,D) = 250mA, V_{IN} = 2V, V_{ENABLE} = 5.5V			60	mA
All Outputs OFF	$I_{CC(OFF)}$				10	mA
Turn-On Delay	t_{PHL}, t_{PLH}				10	µS
Over-Current Limiting for each Output (Note 1)		V_{OUT} = 4.5V to 24.5V, R_L = (Min.) = 4Ω	0.7		1.6	A
FAULT OUTPUT, I_{LOAD} = 30µA:						
Output Low Current	I_{OL}		40		80	µA
Output High Current	I_{OH}				2	µA
Output Low Voltage	V_{OL}	I_{OL} = 30µA			0.4	V
Output Sense Thresholds:						
Output High Threshold	V_{HT}	V_{IN} = 2.0V (Min.)	3		5.5	V
Output Low Threshold	V_{LT}	V_{IN} = 0.8V (Max.)	3		5.5	V
OVER-TEMPERATURE SHUTDOWN (DESIGN PARAMETER):						
Typical Junction Temperature at Thermal Shutdown				165		°C

NOTE:

1. With voltage on the collector of the output transistor as indicated (V_{OUT} = 4.5V to 24.5V) and with that output transistor switched "ON", the current will increase to a limiting value which will be a value of 0.7A, minimum. That output will shortly thereafter (~5 ms) go into Over-Temperature shutdown. (Excessive dissipation during thermal shutdown may damage the chip.)

HARRIS SEMICONDUCTOR

HIP0080
HIP0081

ADVANCE INFORMATION

May 1992

Quad Inverting Power Driver With Diagnostic Interface

Features

- Low Side Power MOSFET Output Drivers
- Output Driver Protection:
  - Over-Current Shutdown
  - Over-Temperature Shutdown
  - Over-Voltage Internal Clamp
- Load Currents Switching Capability with All Outputs ON:
  - HIP0081 . . . . . 1 Amp Each
  - HIP0080 . . . . . 0.5 Amp Each
- Regulated 5V Logic Interface
- 5 Volt CMOS Inputs logic
- Fault Mode Output for Shorts, Opens & Over-Temperature
- 16 Bit Serial Diagnostic Register
- SPI Bus Compatible Data Readout
- 3°C/W - 15 Lead Power SIP Package
- -40°C to +125°C Operating Temperature

Applications

- Drivers For:
  - Solenoids
  - Relays
  - Power Output
  - Lamps
  - Injectors
  - Steppers
  - Motors
  - Displays
- System Use:
  - Automotive
  - Appliances
  - Industrial
  - Robotics

Description

The HIP0080/0081 Quad Power Drivers contain four individually protected NDMOS power output transistor switches to drive inductive and resistive loads such as: relays, solenoids, injection drivers, AC and DC motors, heaters and incandescent displays. The 4 Power Drivers are low-side switches driven by CMOS logic input control stages. The output drivers are protected against over-current, over-temperature and over-voltage. An internal drain-to-gate zener diode provides the clamping protection for over-voltage. Diagnostic circuits provide ground short, supply short, open load and thermal overload detection for each of the 4 output stages. Each of the 4 input drivers and their respective diagnostic filters are controlled by one ENABLE input.

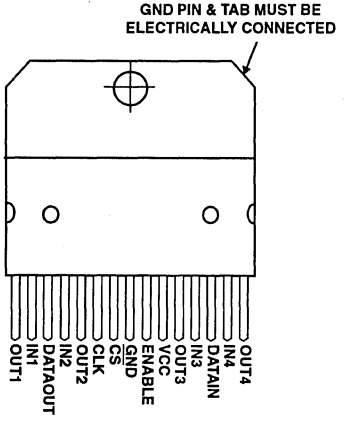
The inputs are CMOS logic compatible and individually control the output drivers with an active high state for turn-on. All other control inputs are active high with the exception of the Chip Select ($\overline{CS}$) which is active low. The DATAIN and DATAOUT are positive logic and the Clock (CLK) input for the Serial Interface is active on the rising edge of the CLK pulse. All inputs include a nominal level of hysteresis. IN1, IN2, IN3, IN4 and ENABLE have pull-down resistors of approximately 100kΩ. This switches off any channel that has an unterminated input.

Ordering Information

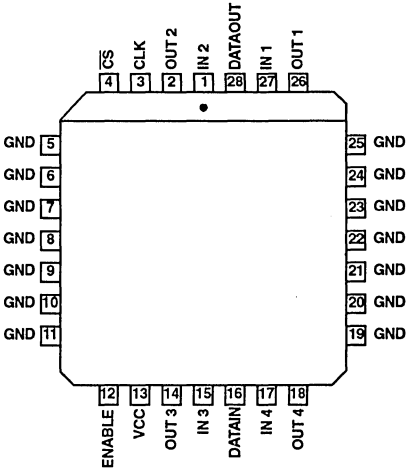
PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
HIP0081AS1	-40°C to +125°C	15 Pin Plastic SIP Staggered Vert.
HIP0081AS2	-40°C to +125°C	15 Pin Plastic SIP Surface Mount
HIP0080AM	-40°C to +125°C	28 Pin PLCC

Pinouts

15 LEAD PLASTIC SIP
TOP VIEW



28 LEAD PLCC
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3018**

Absolute Maximum Ratings

Supply Voltage, V_{CC} . . . . . -16V to 45V
Output Voltage V_O . . . . . -0.5 to V_{CLAMP}
Input Voltage, V_{IN} . . . . . -0.5V to 7V
Output Current, I_{OUT} . . . . . -2A to +3A
Operating Temperature Range . . . . . -40°C to +125°C
Operating Junction Temperature Range . . . . . -40°C to +150°C
Storage Temperature Range, T_{STG} . . . . . -55°C to +150°C

Thermal Resistance	θ_{ja}	θ_{jc}
HIP0080, HIP0081	35°C/W	3°C/W

Lead Temperature (During Soldering)
At distance $^1/_{16} \pm {}^1/_{32}$" (1.59 ± 0.79mm) from case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V_{CC} = 5.5 to 25V ± 5%, T_A = -40°C to +125°C; Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS						UNITS
			HIP0080			HIP0081			
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER OUTPUTS:									
Output ON Resistance	R_{ON}	V_{CC} 10 to 25V, I_{OUT} = 1A V_{CC} 5.5 to 10V, I_{OUT} = 0.7A	-	-	1.0 2.0	-	-	0.5 1.0	Ω Ω
Output Over-Voltage Clamp Range	V_{CLAMP}	Output Programmed OFF	27	-	43	73	-	85	V
Output Short Prot. Current Range	I_{SC}		1.5	-	2.1	3	-	4.1	A
Output Short Circuit Det. Delay	t_{SCDLY}		-	6	-	-	6	-	µs
Output ON-OFF Voltage Ramp Rate		(Resistive load)	-	10	-	-	10	-	V/µs
Turn-On Delay	t_{PHL}	V_{CC} = 14V, R_{LOAD} =14Ω	-	-	8	-	-	8	µs
Turn-Off Delay	t_{PLH}	V_{CC} = 14V, R_{LOAD} =14Ω	-	-	8	-	-	8	µs
SUPPLY:									
Power Supply Current	I_{CC}		-	20	-	-	20	-	mA
Power Supply Reset Active	V_{CC_RST}		3	-	4	3	-	4	V
Shut-Down Current Mode	I_{SHTDN}	Enable LOW	-	20	-	-	N/A	-	µA
INPUTS:									
Low-Level Input Voltage	V_{IL}		-	-	1	-	-	1	V
High-Level Input Voltage	V_{IH}		3.5	-	-	3.5	-	-	V
Input Hysteresis Threshold	V_{IN_HYS}		0.85	-	2.25	0.85	-	2.25	V
Input Pull-Down Resistance	R_{pd}		-	100k	-	-	100k	-	Ω
DATAOUT:									
Tristate Leakage Current	I_{DO_LEAK}		-10	-	10	-10	-	10	µA
Logic High Output Voltage	V_{OH}	I_{OH} = 1.6 mA	3.7	-	-	3.7	-	-	V
Unloaded Max. DATAOUT	V_{HIGH}	No Load	-	-	5	-	-	5	V
Logic Low Output Voltage	V_{OL}	I_{OH} = -1.6 mA	-	-	0.4	-	-	0.4	V
Oscillator Frequency	f_{OSC}		-	500	-	-	500	-	kHz
Serial Interface Clock Freq.	f_{CLK}		-	-	2	-	-	2	MHz
DIAGNOSTIC & PROTECTION:									
Over-Temperature Shutdown Threshold			150	-	-	150	-	-	°C
Shutdown Temp. Hysteresis			-	15	-	-	15	-	°C
Output Short-to-Gnd Thd			-	.24xV_{CC}	-	-	.24xV_{CC}	-	V
Short-to-Gnd Hysteresis			-	.02xV_{CC}	-	-	.02xV_{CC}	-	V
Open-Load Resistance for No-Load Warning			10	-	20	10	-	20	kΩ
Filter Delay Time for O.L. or Short-to-Gnd			-	12	-	-	12	-	µs

Overview

As shown in the Functional Block Diagram, each output stage has voltage and temperature sensors with comparators and delay filters. Four bits of diagnostic information is provided as feedback from each of the four stages. The diagnostic data for all outputs is converted to a serial sequence of 16 bits which is output to a diagnostic register. The data may be read when the Chip Select, $\overline{CS}$ is low and the Clock, CLK transitions positive. With $\overline{CS}$ low, the CLK clock input synchronously shifts the register data while new data is shifted in from the DATAIN input. After 16 clocks, the DATAIN information is shifted to the DATAOUT output. The diagnostic register is cleared after the falling edge of $\overline{CS}$ to allow new diagnostic data to be stored while the existing serial data is read. Figure 2 shows a complete functional signal flow diagram. In each switching channel, the diagnostic sense circuits set 1 bit in the diagnostic register for each of the 4 diagnostics fault conditions as follows:

Bit 1 - indicates a thermal overload when the sensed junction temperature of the output is greater than 150°C. When over-temperature is sensed, the sensor output directly gates-off the drive to the power output and the respective fault bit is set in the diagnostic register. When the chip is sufficiently cooled, the output is gated-on if the input remains ON.

Bit 2 - indicates the fault condition for an output-to-supply short (shorted load). A small value of resistance (~0.01Ω) in the source-to-ground line of the output stage is used to sense the output short. A comparator senses the voltage level and filters the output to provide an input to the control stage and to the diagnostic register. The control state directly shuts down the output when an over-current condition is sensed. Under this condition of fault, the input driver is latched off. To restore the output drive, the short must be removed and the input toggled OFF and then ON.

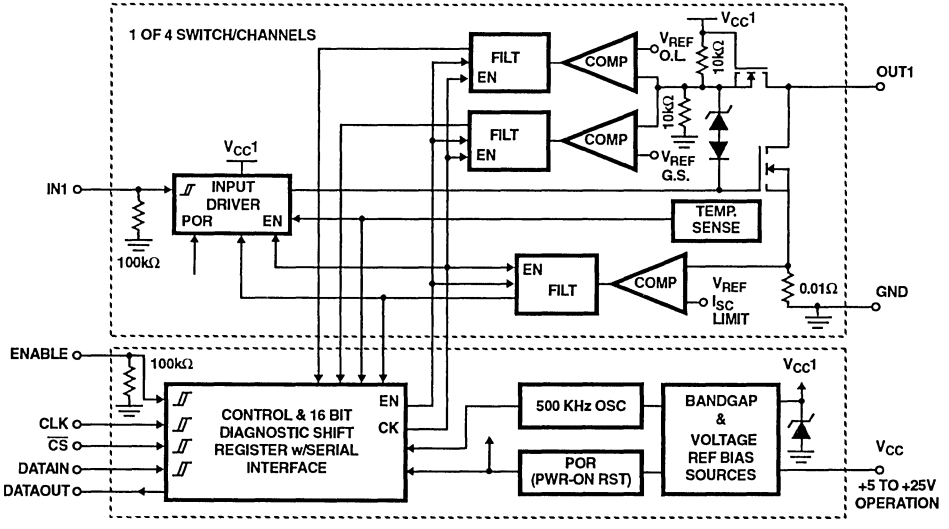
Bit 3 - indicates the condition of an output to ground short. Each output stage has drain-to-supply ($V_{CC}1$) and drain-to-ground pull-up and pull-down resistors of approximately 10kΩ to sense this condition. When the output is off and the sense level is low, an output-to-ground short is detected by the comparator.

Bit 4 - indicates the condition of an open load on the output. The same divider noted above is used to set the output level. If the sense level is at or near the mid-range of the voltage supply, $V_{CC}1$ when the output is in the off condition, a no-load condition is detected.

For normal operating conditions, a Reset turns off all outputs when the V_{CC} level drops below 3.5 volts. The internal bandgap and bias supply function includes a 5V regulated supply for the low voltage signal and logic circuits.

Filters are used on the outputs of the fault sensing comparators to avoid the detection of short duration transient spikes. The on chip oscillator is used to clock an internal shift register in each filter. If the fault condition is longer than a preset number of clock cycles, the fault condition is recognized and the respective bit is set in the diagnostic register. No filter is used in the thermal-overload feedback circuit and the bit is set when thermal shutdown occurs.

Functional Block Diagram



Serial Data Timing Information:

The order or sequence of bits for the diagnostic register is as follows:

Switching Channel 1:

1	Over-temperature	OT1
2	Short to Supply	SB1
3	Short to Ground	SG1
4	Open Load	OI1

Switching Channel 2:

5	Over-temperature	OT2
6	Short to Supply	SB2
7	Short to Ground	SG2
8	Open Load	OI2

Switching Channel 3:

9	Over-temperature	OT3
10	Short to Supply	SB3
11	Short to Ground	SG3
12	Open Load	OI3

Switching Channel 4:

13	Over-temperature	OT4
14	Short to Supply	SB4
15	Short to Ground	SG4
16	Open Load	OI4

Referring to figure 1, the error bits are jammed from DI (DATAIN) to DO (DATAOUT) when enabled by $\overline{CS}$ going low (active). The GATE is an internal control signal that goes high when $\overline{CS}$ goes low. The CLK signal starts when activated to read the first diagnostic data bit (OT1). The first DO bit following the $\overline{CS}$ low and GATE high is a fault error flag which goes high if any one of the 16 fault bits have been set HIGH. This Fault Flag data bit precedes the 16 fault bits and is ORed with the fault bits. In cascaded operation (See Fig 3), the DI input for the first of the selected chips should be tied to ground. When cascaded, the error flags are also cascaded. A fault condition is immediately evident without reading all bits. However, all bits must be read to determine on which chip the diagnostic bit has been set.

The diagnostic interfaces to the HIP0080 and HIP0081 are SPI compatible. The microcontroller is programmed to control the read and respond action based on the diagnostic readout. The Error Flag bit requires a separate input back to the microcontroller. When the CLK signal starts, the serial sequence starting with the first diagnostic bit (OT1) is input to the microcontroller.

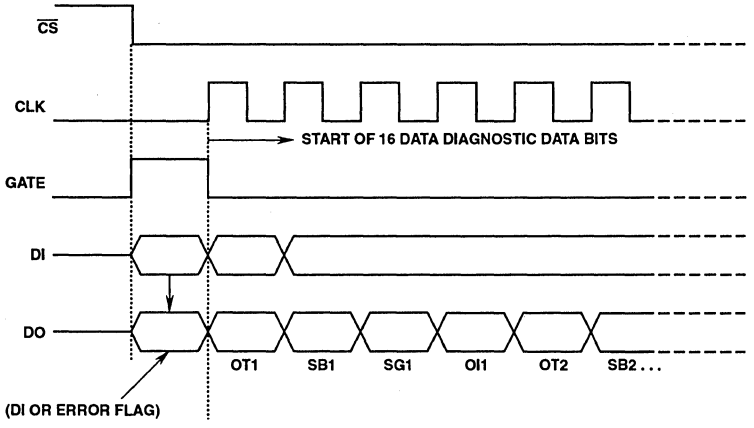


FIGURE 1. DATA AND CLOCK TIMING

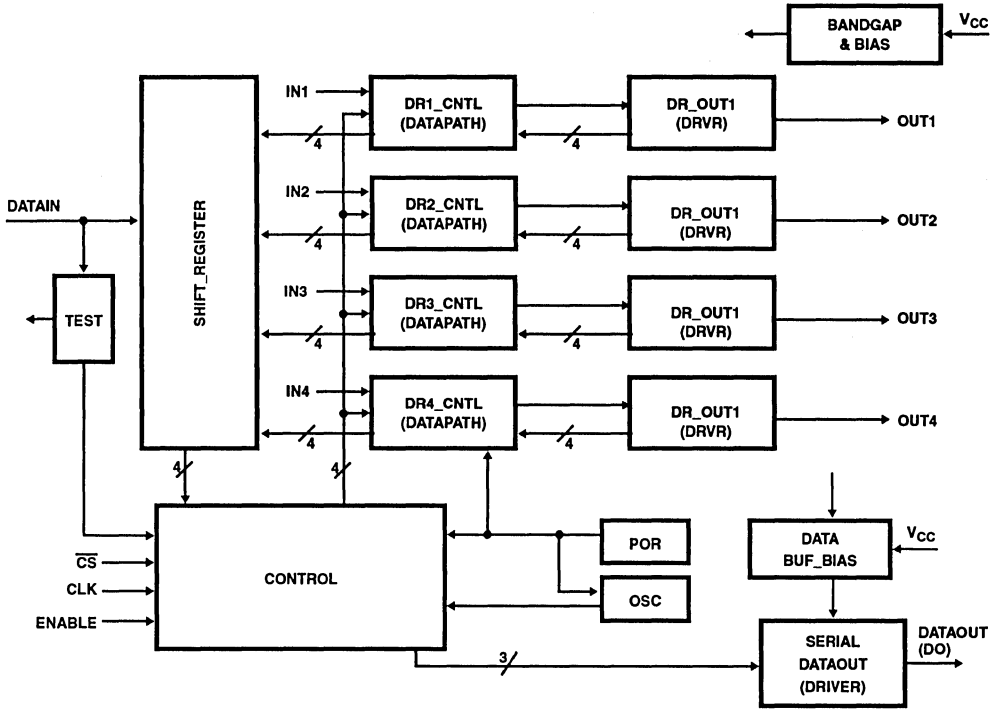


FIGURE 2. FUNCTIONAL SIGNAL FLOW DIAGRAM

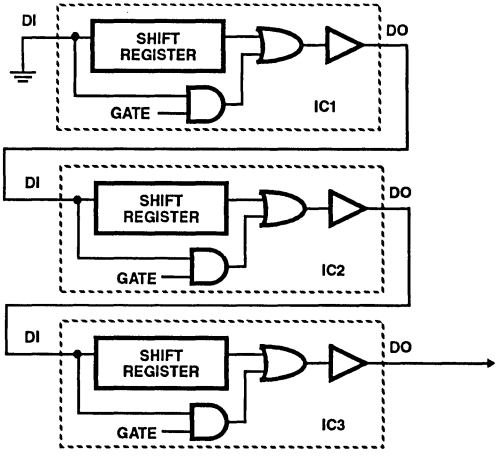


FIGURE 3. CASCADED CHIP OPERATION TO READ DIAGNOSTIC DATA

INTELLIGENT POWER ICs

3

HIGH SIDE SWITCHES

High Side Selection Guide

MOSFET Driver Circuits

TYPE	FUNCTION	MAX. SUPPLY	RECOMMENDED SUPPLY VOLT	MAX. CURRENT	MAX. FREQ.	CURRENT LIMIT	PACKAGE	RECOMMENDED APPLICATION
CA3273	400mA High Side Driver	25V	$4V_{DC}$ to $24V_{DC}$	400mA	-	1.2A	TO-202 Modified	Solenoid or Lamp Drive
HIP1030	1 Amp High Side Driver	25V	$4.5V_{DC}$ to $25V_{DC}$	1 Amp	-	1.4A	5 Pin SIP	Motor Control Solenoid or Lamp
HV400	Single High Speed	30V	$15V_{DC}$ to $40V_{DC}$	6 Amps (Pulsed Gate)	300kHz	No	8 PDIP & SOIC	SMPS
ICL7667	Dual Power	18V	$1.5V_{DC}$ to $15V_{DC}$	1.5 Amps (Pulsed Gate)	100kHz	No	8 P/CDIP, Can & SOIC	SMPS

CA3273

May 1992

High-Side Driver

Features

- Equivalent High Pass p-n-p Transistor
- Current Limiting.....0.6A to 1.2A
- Over-Voltage Shutdown ..... +25V to -40V
- Junction Temperature Thermal Limit.....+150°C
- Equivalent beta of 25.....400mA/0.5V
- Internal Bandgap Voltage and Current Reference

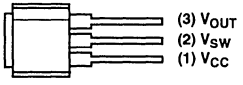
Applications

- Fuel Pump Driver
- Relay Driver
- Solenoid Driver
- Stepper Motor Driver
- Remote Power Switch
- Logic Control Switch

Description

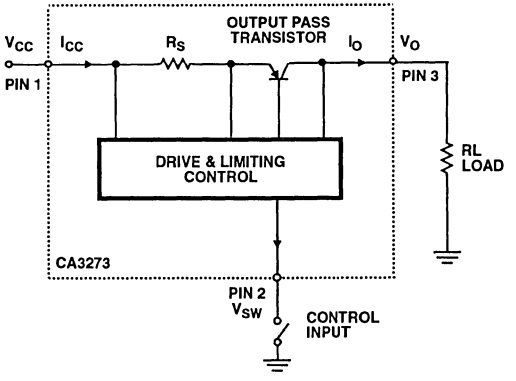
The CA3273 is a power IC equivalent of a p-n-p pass transistor operated as a high-side-driver current switch in either the saturated (ON) or cutoff (OFF) modes. The CA3273 incorporates circuitry to protect the pass currents, excessive input voltage, and thermal overstress. The high-side driver is intended for general purpose, automotive and potentially high-stress applications. If high-stress conditions exist, the use of an external zener diode of 35 volts or less between supply and load terminals may be required to prevent damage due to severe conditions (such as load dump, reverse battery and positive or negative transients). The CA3273 is designed to withstand a nominal reverse-battery (VBAT = 13V) condition without permanent damage to the IC. The CA3273 is supplied in a modified 3-lead TO-202 plastic power package.

Package



MODIFIED TO-202

Block Diagram



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
CA3273	-40°C to +85°C	TO-202 MODIFIED

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2113.2**

Absolute Maximum Ratings

Fault Max, V_{CC} (Limited I_{CC}, -40 to +85°C) ..... 25V to 40V
Operating V_{CC} (R_L = 40Ω, -40 to +85°C) 16V
Operating V_{CC} (R_L = 40Ω, -40 to +25°C) 24V
V_O (Output) Inductive Pulse Rating (-40 to +85°C),
V_{SW} Open..... V_{CC} + 12V
Operating I_{CC} (-40 to +85°C) 1.2A
I_O (-40 to +85°C)..... 400mA
I_O (-40 to +25°C)..... 600mA
Dissipation, P_D at +25°C Ambient (Note1)..... 1.8W
Derate Above +25°C (No Heat Sink) ..... 14.3mW/°C

Thermal Resistance, Junction to Ambient..... +70°C/W
Junction Temperature (Note 2) ..... +150°C
Ambient Temperature Range:
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -40°C to +150°C
Lead Temperature (During Soldering):
At distance 1/16± 1/32 in. (1.59 ± 0.79 mm)
from case for 12s max. ..... +260 °C

NOTES:

1. $P_D = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{SW}$, $T_J = T_A + P_D \times (\theta_{ja})$
2. Thermal limiting (shutdown) occurs at +150°C on the chip.

Electrical Specifications at T_A = -40°C to +85°C,(See Block Diagram For Test Pin Reference)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Operating Voltage Range	V_{CC}	V_{CC} Reference to V_{SW}	4	-	24	V
Sat. Voltage(V_{CC} - V_O):	V_{SAT}	I_O = -400 mA, V_{SW} = 0V V_{CC} = 16V	-	-	0.5	V
Operating Load	R_L	V_{CC} = 16V to 24V	40	-	-	W
Overvolt, T_{HD} (Increase V_{CC})	$V_{CC(THD)}$	V_{SW} = 0V, R_L = 1kΩ (V_O goes Low)	25	-	40	V
Current Limiting	$I_O(I_{IM})$	V_{CC} = 16V, V_{SW} = 1V	-	-	1.2	Amp
Control Current, Switch ON:		V_{CC} = 16V,V_{SW} =0V				
I_{SW} (no load)		I_O = 0mA	-	-15	-	mA
I_{SW} (max. load$_1$)		I_O = -400mA	-	-22	-	mA
Control Current, Switch ON:		V_{CC} = 24V, I_O = -600mA	-	-33	-	mA
I_{SW} (max. load$_2$)		V_{SW} = 0V				
Max. Control Current:		R_L = 40Ω, V_{SW} = 1V				
High V_{CC}:	$I_{SW\ (HI\ VCC)}$	V_{CC} = 24V	-50	-	-	mA
Low V_{CC}:	$I_{SW\ (LO\ VCC)}$	V_{CC} = 7V	-50	-	-	mA
Output Current Cutoff:		V_O = 0V, V_{CC} = 16V				
$I_{O\ (SWOFF1)}$		V_{SW} = 16V	-10	-	+100	µA
$I_{O\ (SWOFF2)}$		V_{SW} = 15V	-100	-	+100	µA
Control Current, Switch OFF:		V_O = Open				
No Load:	$I_{SW\ (HI\ VCC)}$	V_{CC} = 24V, V_{SW} = 23V	-200	-	+50	µA
	$I_{SW\ (LO\ VCC)}$	V_{CC} = 7V, V_{SW} = 6V	-200	-	+50	µA

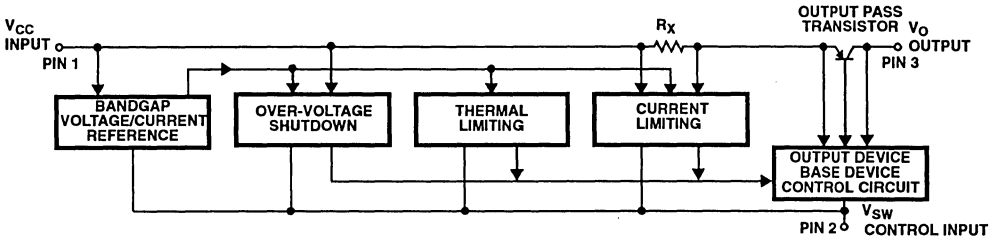


FIGURE 1. FUNCTION BLOCK DIAGRAM OF CA3273

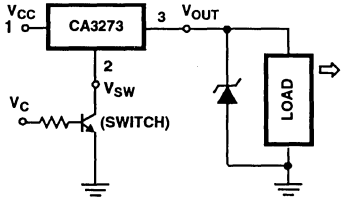


FIGURE 2. TYPICAL APPLICATION WITH ZENER DIODE ($\leq V_{CC}$ +12V) FOR INDUCTIVE SWITCHING PULSE OVER-VOLTAGE PROTECTION

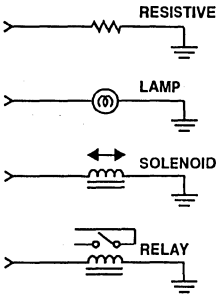


FIGURE 3. TYPICAL LOADS

HARRIS SEMICONDUCTOR

HIP1030

ADVANCE INFORMATION

May 1992

1A High Side Driver With Over-Load Protection

Features

- Over Operating Range: -40°C to +125°C
  - 1V Max at 1A Saturation Voltage
  - 1A Current Switching Capability
  - 4.5V to 25V Power Supply Range
- Over-Voltage Shutdown Protected
- Over-Current Limiting
- Thermal Limiting Protection
- 80Vpk Load Dump
- Reverse Battery Protection

Applications

- Motor Driver/Control
- Driver forSolenoids, Relays and Lamps
- MOSFET and IGBT Driver
- Driver for Temperature Controller

Description

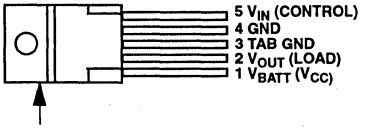
The HIP1030 is a Power Integrated Circuit designed as a High Side Driver to switch power to the output load. The functional block diagram for the HIP1030 is shown in Figure 1. It is the equivalent of a PNP pass transistor operated as a high side current switch in either the saturated ON mode or switched OFF. The HIP1030 is designed with internal circuitry to protect the pass transistor from being damaged by over stress conditions of current, voltage or temperature. It is particularly well suited for driving lamps, relays, and solenoids in automotive and industrial control applications where voltage and current over-load protection at high temperatures is required. The HIP1030 is supplied in a 5 lead TO-220 Power SIP package.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE AND LEAD FORM
HIP1030AS	-40°C to +125°C	5 Pin Plastic SIP (5 Lead TO-220)

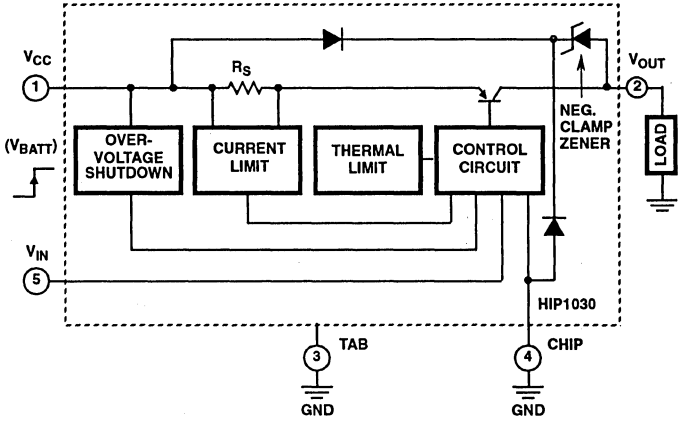
Pinout

TO-220 5 LEAD
TOP VIEW



TAB (GND) INTERNALLY CONNECTED TO PIN 3

Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2788.3**

Absolute Maximum Ratings

Continuous Supply Voltage 25V
Input Voltage, V_{IN} ..... -1V to +7V
Load Current, I_{OUT} ..... Internally Limiting 1.4A
Load Dump (Survival) ..... ±80Vpk

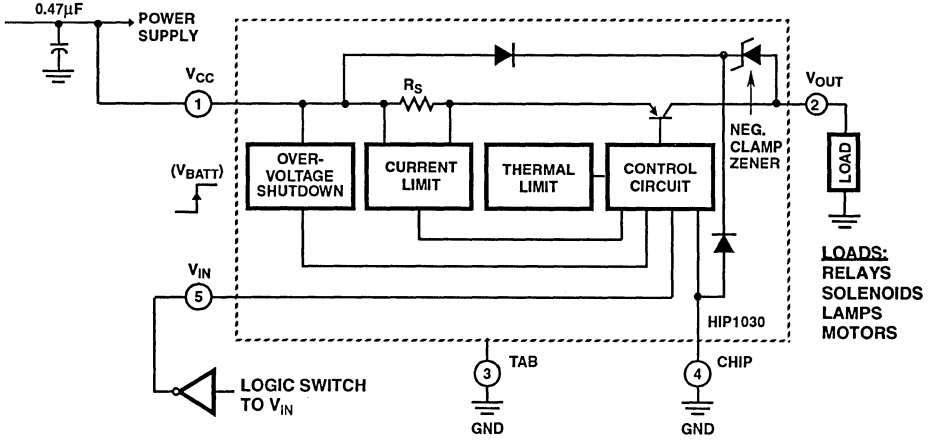
Thermal Resistance (θ_{jc}) ..... 4°C/W
Junction Temperature ..... 150°C
Ambient Operating Temperature ..... -40°C to +125°C
Storage Temperature ..... -40°C to +150°C
Lead Temperature (Soldering 10s max) ..... 265°C

NOTE: $Pd = (V_{CC} - V_{OUT})(I_{OUT}) + (V_{CC})(I_{GND})$
$T_j = T_A + (Pd)(\text{Thermal Resistance})$

Electrical Specifications T_A = -40°C to +125°C, V_{IN} = 2V; I_{OUT} = 0.5A, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Operating Voltage Range	V_{CC}		4.5	-	24	V
Over-Voltage Shutdown	V_{OVSD}		26	-	36	V
Over-Temperature Limiting	T_{LIMIT}		-	150	-	°C
Negative Pulse Output Clamp Voltage	V_{CLAMP}		V_{CC}	-	V_{CC} - 28	V
Input Bias Current	I_{IN}	V_{IN} = 0.8V	-	-	30	µA
Input Control OFF	V_{IL}		-	-	0.8	V
Input Control ON	V_{IH}		2.0	-	-	V
Short Circuit Current Limiting	I_{SC}		-1.4	-	-3.0	A
Supply Current - Full Load	I_{CCMax}	I_{OUT} = 1A	-	-	1.1	A
Supply Current - No Load	$I_{QUIENSCENT}$	V_{IN} = 0V; I_{OUT} = 0A; V_{CC} = 12V	-	-	100	µA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 1A	-	-	100	µA
Output Leakage	I_{OFF}	V_{IN} = 0.8V	-50	-	-	µA

Typical Application



HARRIS SEMICONDUCTOR

HV400

May 1992

High Current MOSFET Driver

Features

- **Fast Fall Times.....16ns at 10,000pF**
- **No Supply Current in Quiescent State**
- **Peak Source Current 6A**
- **Peak Sink Current 30A**
- **High Frequency Operation 300kHz**

Applications

- **Switch Mode Power Supplies**
- **DC/DC Converters**
- **Motor Controllers**
- **Uninterruptible Power Supplies**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HV400CP	0°C to +75°C	8 Pin Plastic Mini-DIP
HV400CB	0°C to +75°C	8 Pin Plastic SOIC
HV400IP	-40°C to +85°C	8 Pin Plastic Mini-DIP
HV400IB	-40°C to +85°C	8 Pin Plastic SOIC
HV400MJ/883*	-55°C to +125°C	8 Pin CerDIP
HV400Y	+25°C	DICE

* Contact Harris for availability date.

Description

The HV400 is a single monolithic, non-inverting high current driver designed to drive large capacitive loads at high slew rates. The device is optimized for driving single or parallel connected N-channel power MOSFETs with total gate charge from 5nC to >1000nC. It features two output stages pinned out separately allowing independent control of the MOSFET gate rise and fall times. The current sourcing output stage is an NPN capable of 6A. An SCR provides over 30A of current sinking. The HV400 achieves rise and fall times of 54ns and 16ns respectively driving a 10,000pF load.

Special features are included in this part to provide a simple, high speed gate drive circuit for power MOSFETs. The HV400 requires no quiescent supply current, however, the input current is approximately 15mA while in the high state. With the internal current steering diodes (pin 7) and an external capacitor, both the timing and MOSFET gate power come from the same pulse transformer; no special external supply is required for high side switches. No high voltage diode is required to charge the bootstrap capacitor.

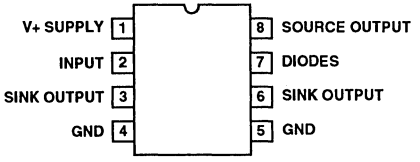
The HV400 in combination with the MOSFET and pulse transformer makes an isolated power switch building block for applications such as high side switches, secondary side regulation and synchronous rectification. The HV400 is also suitable for driving IGBTs, MCTs, BJTs and small GTOs.

The HV400 is a type of buffer; it does not have input logic level switching threshold voltages. This single stage design achieves propagation delays of 20ns. The output NPN begins to source current when the voltage on pin 2 is approximately 2V more positive than the voltage at pin 8.

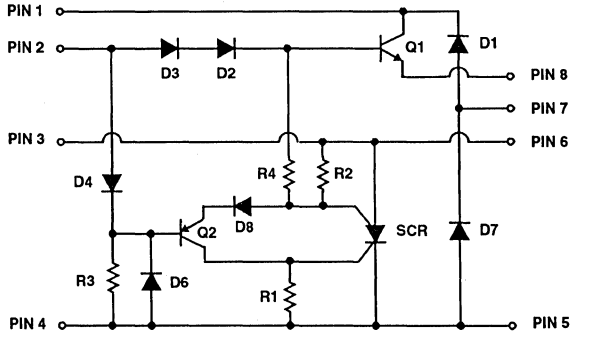
The output SCR switches on when the input pin 2 voltage is 1V more negative than the voltage at pins 3/6. Due to the use of the SCR for current sinking, once the output switches low, the input must not go high again until all the internal SCR charge has dissipated, 0.5µs - 1.5µs later.

Pinout

HV400 (PLASTIC MINI-DIP AND SOIC)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2850**

Absolute Maximum Ratings

Voltage Between Pin1 and Pin 4/5 ..... 35V
Input Voltage Pin 7 (Max) ..... Pin 1 + 1.5V
Input Voltage Pin 7 (Min) ..... Pin 4/5 -1.5V
Input Voltage Pin 2 to Pin 4/5 ..... +/- 35V
Input Voltage Pin 2 to Pin 6 ..... -35V
Maximum Clamp Current (Pin 7) ..... ±300mA
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... $-65°C < T_A < +150°C$

Thermal Resistance ..... θ_{ja} θ_{jc}
PDIP ..... 93.8°C/W 31.5°C/W
SOIC ..... 157.1°C/W 42.8°C/W
Power Dissipation at T_A = +25°C ..... 1.33W Mini-DIP
Power Dissipation at T_A = +25°C ..... 0.8W SOIC
Operating Temperature Range
HV400CP/CB ..... $0°C < T_A < +70°C$
HV400IP/IB ..... $-40°C < T_A < +85°C$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications V_{SUPPLY} = 15V

PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INPUT (PIN 2)							
Input High Differential Voltage (Pin 2 - Pin 8)	V_{IH}	V_{OUT} = 0V, I_{OUT} HI = 10mA	+25°C	0.6	1.7	2.8	V
			Full	0.5	-	3.5	V
Input Low Differential Voltage (Pin 2 - Pin 3/6)	V_{IL}	V_{OUT} = 12V, I_{OUT} LO = -3mA	+25°C	-1.1	-0.9	-0.8	V
			Full	-1.26	-	-0.65	V
Input High Current	I_{IH}	$V_{PIN\ 1,2}$ = 30V, I_{SOURCE} = 0	+25°C	15	18	20	mA
			Full	15		22	mA
Input High Current Peak	I_{IHP}	I_{SOURCE} = 6A, 1µs pulse, V_{IN} = 9V, V_{OUT} = 0V	+25°C		700		mA
Input Low Current	I_{IL}	$V_{PIN\ 2}$ = -30V	+25°C	-80	-50		µA
			Full	-120			µA
SOURCE OUTPUT (PIN 8)							
High Output Voltage	V_{OH}	V_{IN} = +V, I_{OUT} = 150mA	+25°C	12.1	12.8	13.4	V
			Full	12.0		13.5	V
Peak Output Current	I_{OP8}	V_{IN} = 9V, 1µs Pulse, V_{OUT} = 0V	+25°C		6		A
Output Low Leakage	I_{OL}	V_{OUT} = 0V, V_{IN} = 0V	+25°C	0	10	50	µA
			Full			55	µA
SINK OUTPUT (PIN 3/6)							
Low Output Voltage	V_{OL}	V_{IN} = 0V, I_{OUT} = -150mA	+25°C	0.8	0.89	1.0	V
			Full	0.8		1.05	V
Peak Output Current	I_{OP6}	V_{IN} = 0V, 5µs Pulse, V_{OUT} = 4V	+25°C		30		A
Output High Leakage	I_{OH}	V_{IN} = 15V	+25°C	0	0.3	2	µA
			Full	0		13.5	µA
DIODES D1 AND D7 (PIN 7)							
Forward Voltage	V_F	I_D = 100mA	+25°C	0.9	1.03	1.1	V
			Full	0.8		1.4	V
Reverse Leakage Current	I_R	V_R = 30V	+25°C	0	0.1	1	µA
			Full	0		1	µA
Diode (Pin 7) Stored Charge	Q_{RR}	I_D = 100mA	+25°C		6.5		nC

NOTE: Limits are 100% tested at +25°C; limits over the full temperature range are guaranteed but not tested.

Pin Descriptions

SYMBOL	DESCRIPTION
DC INPUT PARAMETERS	
V_{IH}	The differential voltage between the input (Pin 2) to the output (Pin 8) required to source 10mA
V_{IL}	The differential voltage between the input (Pin 2) to the output (Pins 3, 6) required to sink 3mA
I_{IH}	The current required to maintain the input (Pin 2) high with I_{OUT} = 0A
I_{IHP}	The input (Pin 2) current for a given pulsed output current
I_{IL}	The current require to maintain the input (Pin 2) low
DC OUTPUT PARAMETERS	
V_{OH}	The output (Pin 8) voltage with input (Pin 2) = V+
I_{OP8}	The pulsed peak source current form output (Pin 8)
I_{OL}	The output (Pin 8) leakage current with the input (Pin 2) = Ground
V_{OL}	The output (Pins 3, 6) voltage with the input (Pin 2) = Ground
I_{OP6}	The pulsed peak sink current into output (Pins 3, 6)
I_{OH}	The output (Pins 3, 6) leakage current with the input (Pin 2) = V+
V_F	The forward voltage of diode D1 or D7
I_R	The reverse leakage current of diode D1 or D7
Q_{RR}	The time integral of the reverse current at turn off
AC PARAMETERS (See Switching Time Specifications)	
T_R	The low to high transition of the output
T_F	The high to low transition of the output
T_{DR}	The output propagation delay from the input (Pin 2) rising edge
T_{DF}	The output propagation delay from the input (Pin 2) falling edge
T_{OR}	The minimum time required after an output high to low transition before the next input low to high transition

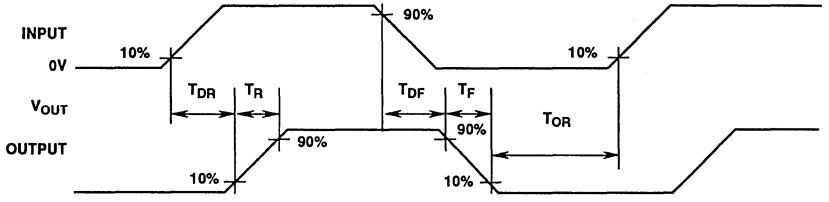
Switching Time Specifications V_{SUPPLY} = 15V

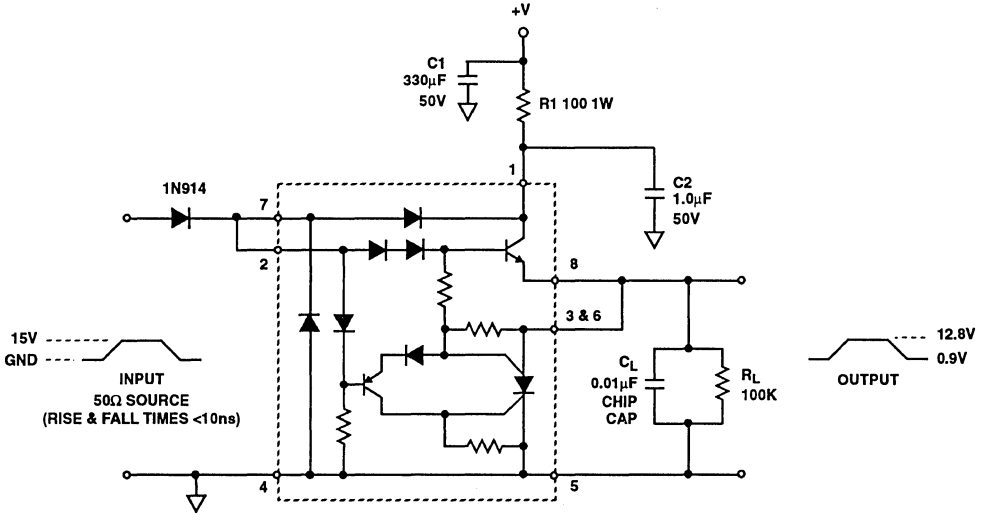
PARAMETERS	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS			UNITS
				MIN	TYP	MAX	
Rise Time	T_R	See Switching Test Circuit	Full		50	66	ns
Fall Time	T_F	See Switching Test Circuit	Full		15	24	ns
Delay Time (Lo to Hi)	T_{DR}	See Switching Test Circuit	Full		20	25	ns
Delay Time (Hi to Lo)	T_{DF}	See Switching Test Circuit	Full		17	28	ns
Minimum Off Time	T_{OR}	See Switching Test Circuit	Full		900	1500	ns

NOTES:

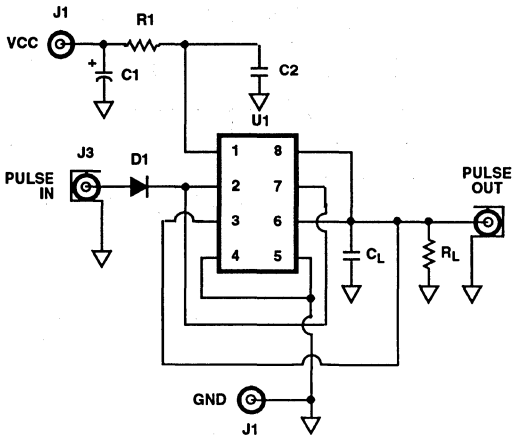
1. Switching times are guaranteed but not tested
2. Typical values are for +25°C

Switching Diagram and Test Circuit



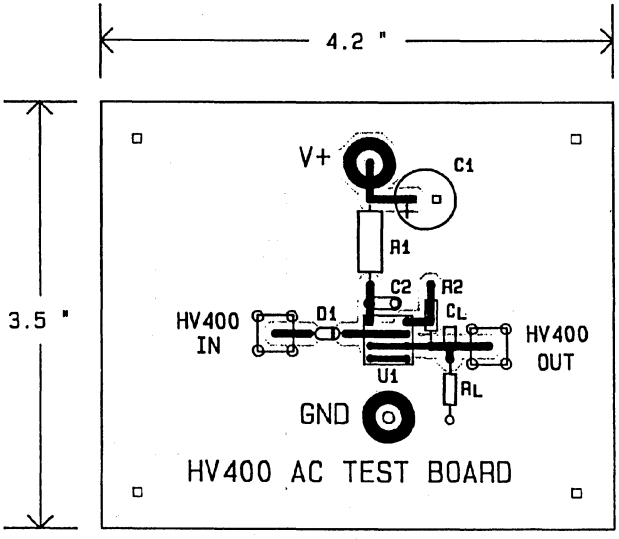


HV400 Switching Test Circuit



Parts List

R1 100Ω, 1W Carbon Resistor
R2 Wire
R_L 100KΩ, 1/8W Carbon Resistor
C1 330µF, 50V Capacitor
C2 1µF, 50V Capacitor
C_L 0.01µF, 50V Chip Capacitor
D1 1N914 Diode
J1, J2 PC Mount Banana Jack Johnson 108-0740-001
J3, J4 PC Mount SMA Connector Johnson EFJ142
U1 Harris HV400 I.C.



Application Information

Circuit Operation

The HV400's operation is easily explained by referring to the schematic. The control signal is applied to pin 2. If the control signal is about 2V above pin 8, the output NPN Q1 turns on charging the MOSFET gate from a capacitor connected to pin 1. Resistor R4 helps keep the SCR off by applying a reverse bias to the SCR anode gate.

When the control input drops about 1V below pin 3/6, PNP Q2 turns on which triggers the SCR by driving both the anode and cathode gates. The SCR discharges the MOSFET gate and when its current becomes less than 10mA, it turns off. Transistor Q2 conducts any gate leakage currents, through resistors R1 and R2, once the SCR turns off. Figure 7 shows the output characteristics before the SCR turns on and after it turns off. When the SCR turns on, resistor R4 provides a path to remove Q1 base charge. Resistor R3 provides the base current for Q2 to reduce the turn off delay time. Resistors R1 and R2 reduce the SCR recovery time.

The two diodes connected to the diode input pin 7 provide some operation flexibility. With pins 2 and 7 connected together, diode D1 provides a path to recharge the storage capacitor once the MOSFET gate is pulled high and, along with diodes D2 and D3, keeps Q1 from going into hard saturation which would increase delay times. Diode D7 would clamp the input near ground and provide a current path if an input DC blocking capacitor is used.

Alternatively, pin 7 can be connected to pin 6 so that the SCR and NPN Q1 don't have to pass reverse current if the output "rings" above the supply or below ground. When high performance diodes are required, pin 7 can be left disconnected and external diodes substituted.

The diodes in series with pin 2 decouple the input from the output during negative going transitions. The absence of input current turns off Q1 and allows Q2 to trigger the SCR. Diode D8 turns off Q2 once the SCR turns on pulling the output low, otherwise Q2 would saturate and slow down circuit operation. In addition, the diodes D2, D3 and D8 improve noise immunity by adding about 2.5V of input hysteresis.

The HV400 is capable of large output currents but only for brief durations due to power dissipation.

Circuit Board Layout

PC board layout is very important. Pins 3 and 6 should be connected together as should pins 4 and 5. Otherwise the internal interconnect impedance is doubled and only half of the bond wires are used which would degrade the reliability.

The bootstrap capacitor should hold at least 10x the charge of the MOSFET and should be connected between pins 1 and 4/5 with minimum lead lengths and spacings. Likewise, the HV400 should be as close to the MOSFET as possible. Any long PC traces (parasitic inductances) between the MOSFET gate and pins 8 or 3/6 or between the source and pins 4/5 should be avoided. Inductance between the HV400 and the MOSFET limit the MOSFET switching time. If they are too large, the HV400 may operate erratically as discussed below.

Cross Conduction Faults

It is possible to have both Q1 and the SCR on at the same time resulting in very large cross conduction currents. The SCR has larger current capacity so the output goes low and the storage capacitor is discharged. The conditions that cause cross conduction and precautions are discussed below.

Minimum Off Time

The SCR requires a recovery time before voltage can be reapplied without it switching back on. Figure 13 shows how this SCR recovery time, called "minimum off time" (T_{OR}), is a function of the load capacitance. If the input voltage goes high before this recovery time is complete, the SCR will switch back on.

Note that reverse current flowing through the SCR, for example due to load inductance ringing, extends the minimum off time. Since the minimum off time is really dependent upon how much stored charge remains in the SCR when the anode (pin 3/6) is taken positive, it may vary for different applications. Figure 13 indirectly shows that the minimum off time increases with larger currents. It also increases at elevated temperatures as shown in Figure 14. Excessive ringing increases the minimum off time since the stored charge doesn't begin to dissipate until the current drops below 10mA for the last time. Rising anode voltage acts on the internal SCR capacitance to generate its own triggering current. The excess stored charge increases this capacitance. Faster rise times and/or higher voltages also increase the amount of internal trigger current from the internal capacitance so applications with larger dV/dt require longer minimum off times.

The minimum off time must be considered for all occurrences of SCR current. For example, in a half bridge switch mode power supply, there are two MOSFET's connected to the transformer primary. Assume that the high side MOSFET switch is off. When the low side MOSFET switch is turned on, the HV400 driving the high side MOSFET will have to sink gate current from C_{gd} and will have to source gate current when the low side MOSFET switches back off. Both of these current pulses will try to flow through pin 3/6 since the pin 8 output is turned off. Sourcing current from pins 3/6 through the SCR is possible, the pin 3/6 voltage becoming negative with respect to pins 4/5 (See Figure 8). But a better practice would be to connect a Schottky diode between pins 4/5 (anode) and 3/6 (cathode) so reverse current does not flow through the SCR.

False SCR Triggering

The SCR may be triggered inadvertently. The output may overshoot the input due to inductive loading or over driving the output NPN (allowing it to saturate). Whenever pin 6 is more positive than pin 2 by 1V, the SCR is triggered on. Also,

if the output rises too rapidly, greater than 0.5V/nS, the SCR may self trigger. Both issues are resolved by minimizing the load inductance and inserting sufficient resistance, usually 0.1 to 10 ohms, between pin 8 and the load.

A very fast negative going input voltage can result in minimum off times of about 2.5µs. If the output can not keep up with the falling input, the stored charge of diode D4 is transferred into the base of Q2. This excess charge in Q2 must have time to dissipate. Otherwise, when pin 3/6 goes positive, Q2 will turn on and trigger the SCR. An external diode in series with pin 2, as shown in Figure 1, will prevent D4 from discharging into the base of Q2 but that will also reduce the output voltage by the forward voltage of that diode.

Internal Diodes

The internal diodes connected to pin 7 are provided for convenience but may not be suitable for large currents. Since they are part of the integrated circuit, they are physically small, operate at high current densities, and have long recovery times. Figure 15 shows that their forward characteristics degrade above 100mA. In addition, Figure 16 shows their reverse recovery charge as a function of forward current. The product of this charge, the applied reverse voltage and the frequency is the additional power dissipation due to the diodes. For stored charge calculations, use the peak forward current within 100ns of the application of reverse bias. In addition to the extra power dissipation, the capacitance of these diodes may extend the switching delay times.

Power Dissipation Calculations

The power required to drive the MOSFET is the product of its total gate charge times the gate supply voltage (maximum voltage on HV400 pin 1, 2 or 7) times the frequency. Assuming that the MOSFET gate resistance is negligible, this power is dissipated within the HV400. If resistors are placed between the HV400 and the MOSFET, then some of the power is dissipated in the resistors, the percentage depending upon the ratio of resistors to HV400 output impedance.

There are two other sources of power dissipation to consider. First there is the power in R3 which is the product of the input pin 2 current and voltage (with no output current) times the duty cycle. Second is the product of the pin 7 diode stored charge, which is dependent upon the forward current, times the applied diode reverse voltage times the frequency. This information is available from figures 3 and 16 in this data sheet.

Applications Circuits

The HV400 was designed to interface a pulse transformer to a power MOSFET. There must be some means to balance the transformer volt-second product over a cycle. The unipolar drive shown in Figure 1 lets the core magnetization inductance reverse the primary and secondary voltages. The zener diode on the primary side limits this voltage and must be capable of dissipating the energy stored in the transformer. The load may be connected to either the power MOSFET drain or source.

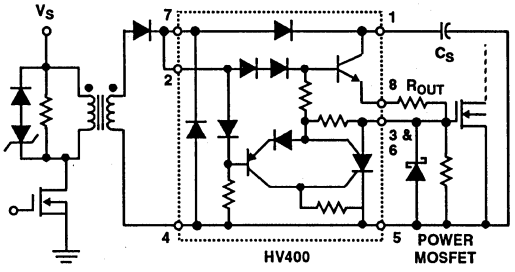


FIGURE 1. UNIPOLAR DRIVE

A diode is added in series with pins 2 and 7 to allow the transformer secondary to go negative. The charge storage of the pin 7 diode may cause the turn off delay time to be too long. Alternatively, pin 7 could be left disconnected and a second external diode connected between the transformer (anode) and pin 1 (cathode). In some applications the diode in series with pin 2 may be unnecessary but the -35V input to output or ground maximum rating should be observed.

Sometimes the volt-second balance is achieved by a push-pull drive on the pulse transformer primary. This is especially useful if there are two secondary windings driving two HV400's out of phase such as in a half-bridge configuration

Other times it is more convenient to achieve volt-second balance by using capacitors to block DC in the primary and secondary windings as shown in Figure 2. The pin 7 diodes provide a path for discharging the secondary side DC blocking capacitor. Both capacitors, C_{IN} and C_S, should be at least 10 times the equivalent MOSFET gate capacitance.

The HV400 can be used as a current booster for low side switches by connecting directly to the PWM output. The circuit would be similar to the switching time test circuit.

It is worth restating that some consideration (and experimentation) should be given to the choice of external components, i.e. resistors, capacitors and diodes, to optimize performance in a given application.

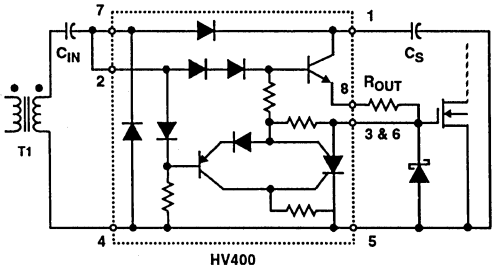


FIGURE 2. BIPOLAR DRIVE WITH DC BLOCKING CAPACITOR

Typical Performance Curves T_A = +25°C Unless Otherwise Specified

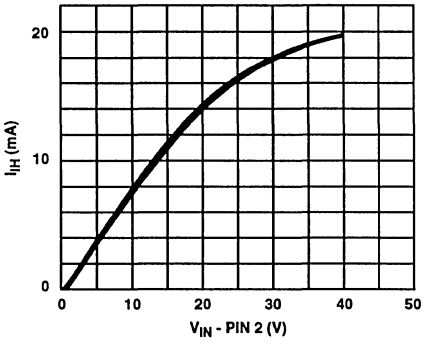


FIGURE 3. PIN 2 INPUT CURRENT vs INPUT VOLTAGE WITH ZERO OUTPUT CURRENT

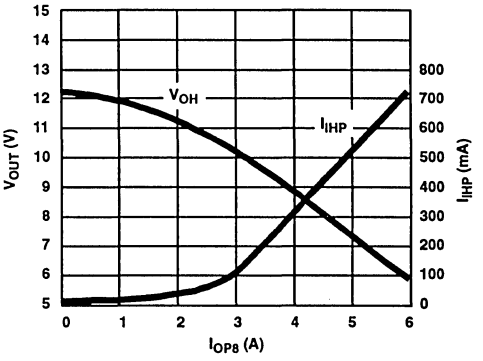


FIGURE 4. PIN 2 I_{IHP} & V_{OH} vs OUTPUT SOURCE CURRENT

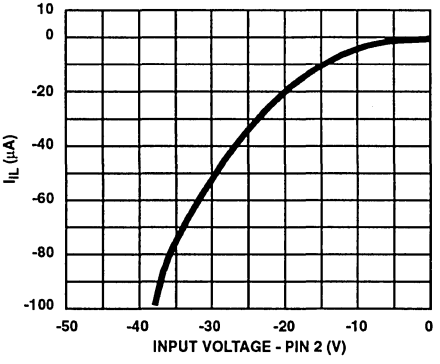


FIGURE 5. PIN 2 I_{IL} vs INPUT VOLTAGE

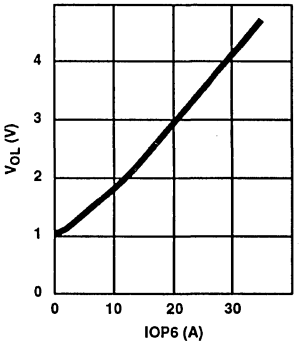


FIGURE 6. V_{OL} vs I_{OP6} (5µs PULSES)

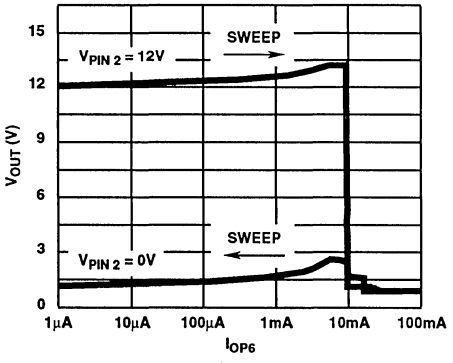


FIGURE 7. PIN 3/6 ILLUSTRATING OUTPUT VOLTAGE vs SCR OUTPUT SINK LATCHING AND HOLDING CURRENT

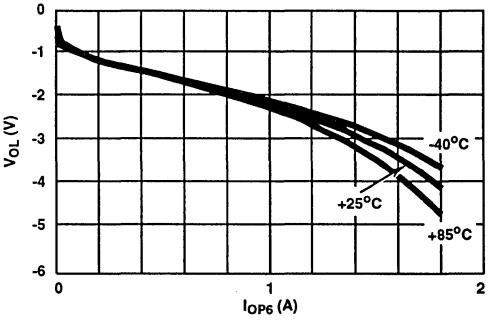


FIGURE 8. PIN 3/6 VOLTAGE vs REVERSE CURRENT 300µs PULSES

Typical Performance Curves T_A = +25°C Unless Otherwise Specified (Continued)

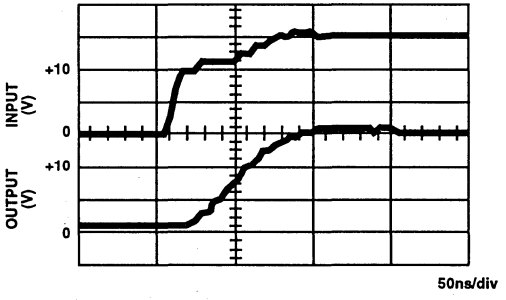


FIGURE 9. LOW TO HIGH TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

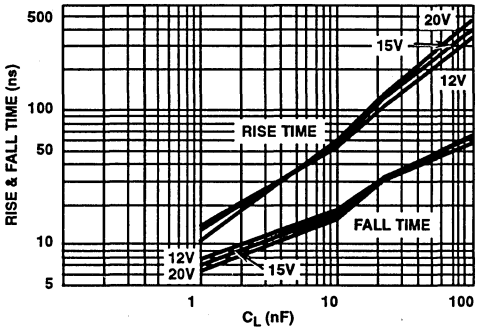


FIGURE 10. RISE & FALL TIMES vs C_L(V+ = 12V, 15V, 20V)

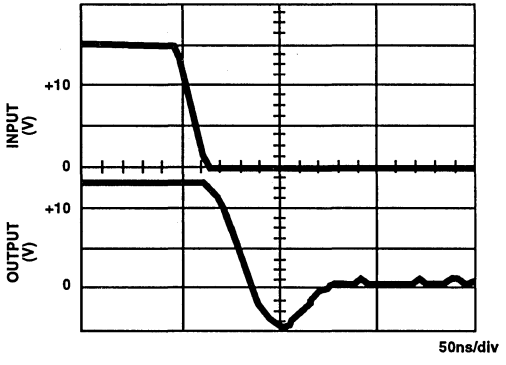


FIGURE 11. HIGH TO LOW TRANSIENT RESPONSE WAVEFORMS (C_L = 10nF)

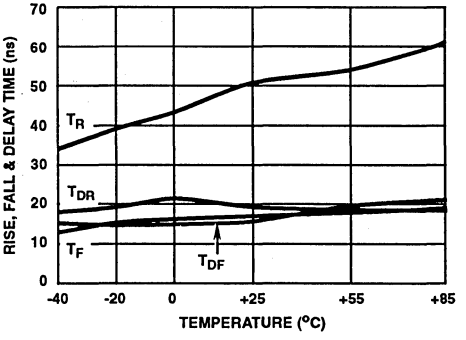


FIGURE 12. RISE, FALL & DELAY TIMES vs TEMPERATURE

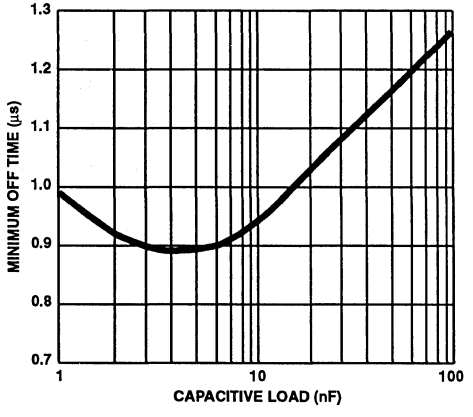


FIGURE 13. MINIMUM OFF TIME (T_{OR}) vs C_L AT +25°C

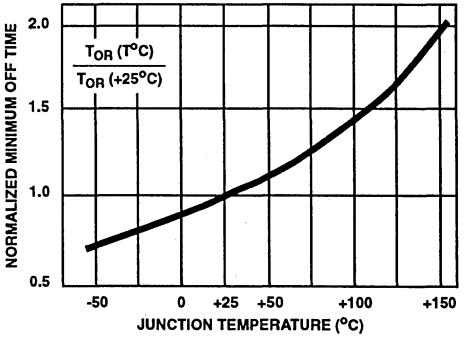


FIGURE 14. NORMALIZED MINIMUM OFF TIME (T_{OR}) vs TEMPERATURE (C_L = 10nF)

Typical Performance Curves T_A = +25°C Unless Otherwise Specified (Continued)

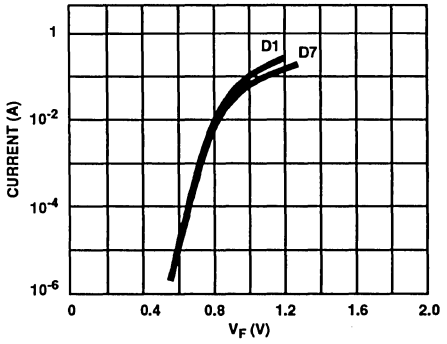


FIGURE 15. DIODE D1 & D7 CURRENT vs V_F

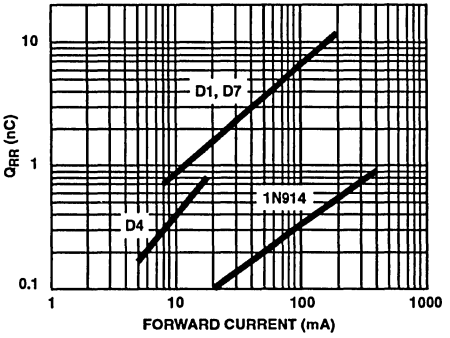
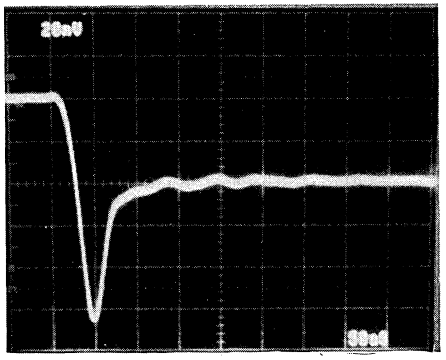


FIGURE 16. DIODE Q_{RR} vs FORWARD CURRENT



Vertical 100mA/div
Horizontal 50ns/div

FIGURE 17. DIODE D1 REVERSE RECOVERY WAVEFORM
I_F = 200mA, 20V REVERSE BIAS

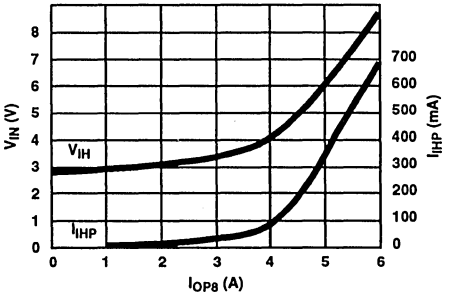


FIGURE 18. V_{IH} & I_{IHP} vs I_{OP8} [V_{OUT} (PIN 8) = 0, V+ = 15V, 1µs PULSE]

Metallization Topology

DIE DIMENSIONS:
66.9 x 71.65 x 19 mils
(1700 x 1820 x 483µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

SUBSTRATE POTENTIAL (POWERED UP):
Unbiased

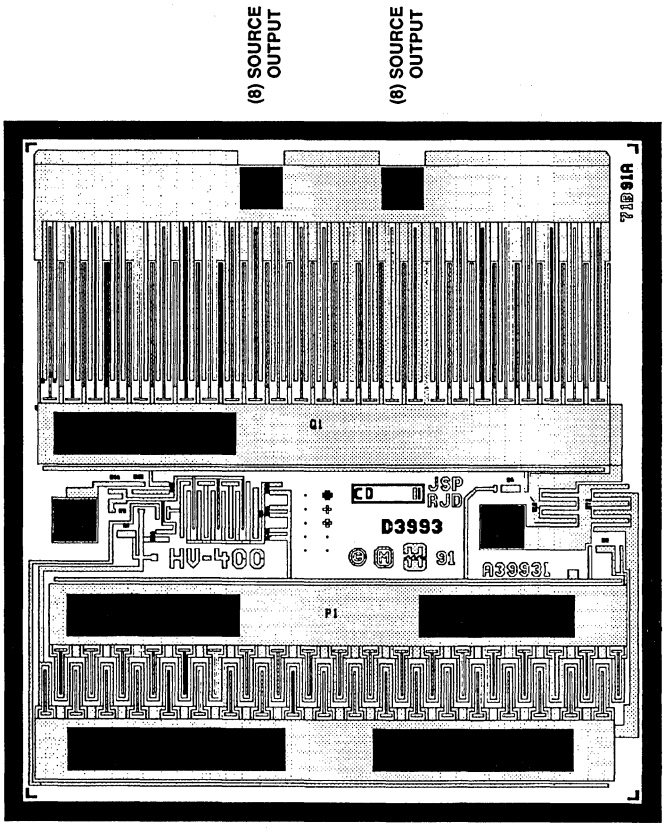
GLASSIVATION:
Type: Silox
Thickness: 12kÅ ± 2kÅ
Type: Nitride
Thickness: 3.5kÅ ± 2.5kÅ

TRANSISTOR COUNT: 3

PROCESS: HFSB Linear Dielectric Isolation

Metallization Mask Layout

HV400Y



NOTE: Pin Numbers Correspond to Mini-DIP and SOIC Packages Only.

HARRIS SEMICONDUCTOR

ICL7667

May 1992

Dual Power MOSFET Driver

Features

- Fast Rise and Fall Times
  - 30ns with 1000pF Load
- Wide Supply Voltage Range
  - V_{CC} = 4.5 to 15V
- Low Power Consumption
  - 4mW with Inputs Low
  - 20mW with Inputs High
- TTL/CMOS Input Compatible Power Driver
  - R_{OUT} = 7Ω Typ
- Direct Interface with Common PWM Control ICs
- Pin Equivalent to DS0026/DS0056; TSC426

Typical Applications

- Switching Power Supplies
- DC/DC Converters
- Motor Controllers

Description

The ICL7667 is a dual monolithic high-speed driver designed to convert TTL level signals into high current outputs at voltages up to 15V. Its high speed and current output enable it to drive large capacitive loads with high slew rates and low propagation delays. With an output voltage swing only millivolts less than the supply voltage and a maximum supply voltage of 15V, the ICL7667 is well suited for driving power MOSFETs in high frequency switched-mode power converters. The ICL7667's high current outputs minimize power losses in the power MOSFETs by rapidly charging and discharging the gate capacitance. The ICL7667's input are TTL compatible and can be directly driven by common pulse-width modulation control ICs.

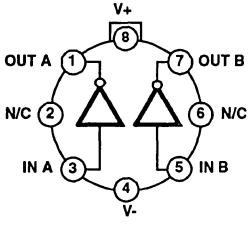
Order Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7667CBA	0°C to +70°C	8 Pin SOIC
ICL7667CPA	0°C to +70°C	8 Pin Plastic
ICL7667CJA	0°C to +70°C	8 Pin Ceramic DIP
ICL7667CTV	0°C to +70°C	TO-99 Can
ICL7667MTV*	-55°C to +125°C	TO-99 Can
ICL7667MJA*	-55°C to +125°C	8 Pin Ceramic DIP

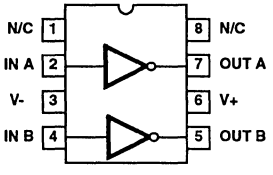
* Add /883B to Part Number for 883B Processing

Pinouts

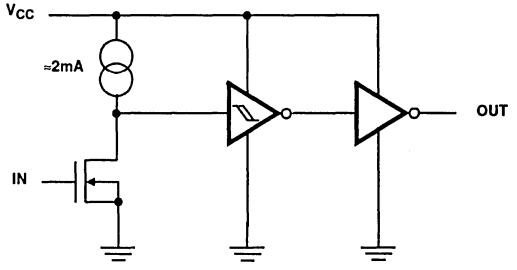
TO-99 CAN (TV)
TOP VIEW



8 LEAD DUAL-IN-LINE PACKAGE (PA, JA, BA)
TOP VIEW



Functional Diagram



3 HIGH SIDE SWITCHES

File Number **2853.1**

Absolute Maximum Ratings

Supply Voltage V+ to V- 15V
Input Voltage ..... V- -0.3V to V+ +0.3V
Package Dissipation, T_A +25°C 500mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Linear Derating Factors
TO-99 ..... 6.7mW/°C above 50°C
Plastic DIP Package ..... 5.6mW/°C above 36°C
Ceramic DIP Package ..... 6.7mW/°C above 50°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Temperature Range

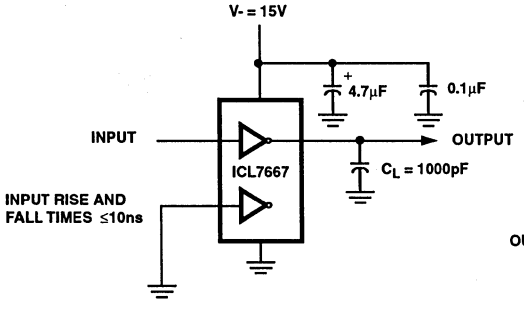
ICL7667C ..... 0°C to +70°C
ICL7667M ..... -55°C to +125°C

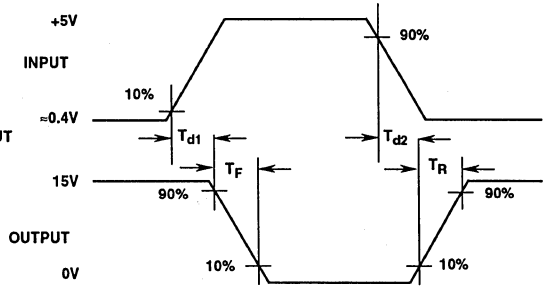
Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	ICL7667C, M T_A = +25°C			ICL7667M -55°C ≤ T_A ≤ +125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DC SPECIFICATIONS									
Logic 1 Input Voltage	V_{IH}	V_{CC} = 4.5V	2.0	-	-	2.0	-	-	V
Logic 1 Input Voltage	V_{IH}	V_{CC} = 15V	2.0	-	-	2.0	-	-	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 4.5V	-	-	0.8	-	-	0.5	V
Logic 0 Input Voltage	V_{IL}	V_{CC} = 15V	-	-	0.8	-	-	0.5	V
Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V and 15V	-0.1	-	0.1	-0.1	-	0.1	µA
Output Voltage High	V_{OH}	V_{CC} = 4.5V and 15V	V_{CC} -0.05	V_{CC}	-	V_{CC} -0.1	-	-	V
Output Voltage Low	V_{OL}	V_{CC} = 4.5V and 15V	-	0	0.05	-	-	0.1	V
Output Resistance	R_{OUT}	V_{IN} = V_{IL}, I_{OUT} = -10mA, V_{CC} = 15V	-	7	10	-	-	12	Ω
Output Resistance	R_{OUT}	V_{IN} = V_{IH}, I_{OUT} = 10mA, V_{CC} = 15V	-	8	12	-	-	13	Ω
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 3V both inputs	-	5	7	-	-	8	mA
Power Supply Current	I_{CC}	V_{CC} = 15V, V_{IN} = 0V both inputs	-	150	400	-	-	400	µA
SWITCHING SPECIFICATIONS									
Delay Time	T_{D2}	Figure 3	-	35	50	-	-	60	ns
Rise Time	T_R	Figure 3	-	20	30	-	-	40	ns
Fall Time	T_F	Figure 3	-	20	30	-	-	40	ns
Delay Time	T_{D1}	Figure 3	-	20	30	-	-	40	ns

* NOTE: All typical values have been characterized but are not tested.

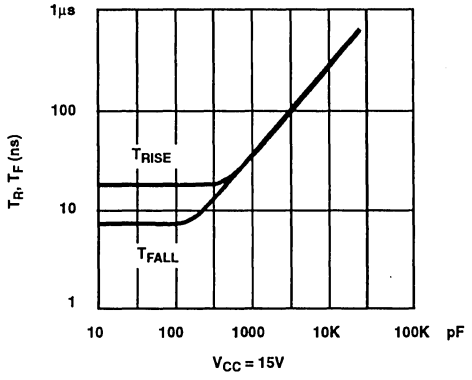
Test Circuits



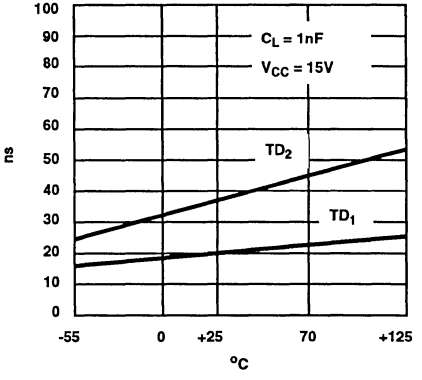


Typical Performance Characteristics

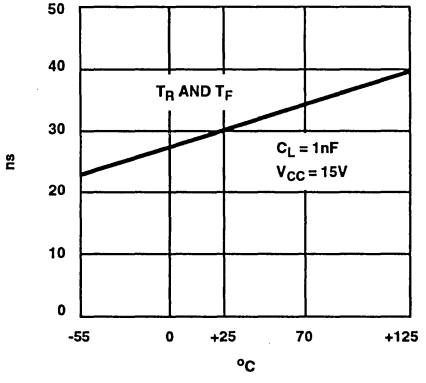
RISE AND FALL TIMES vs. C_L



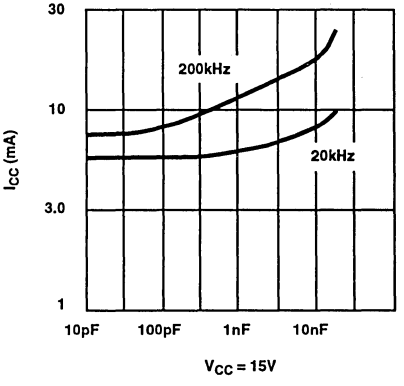
T_{D1}, T_{D2} vs. TEMPERATURE



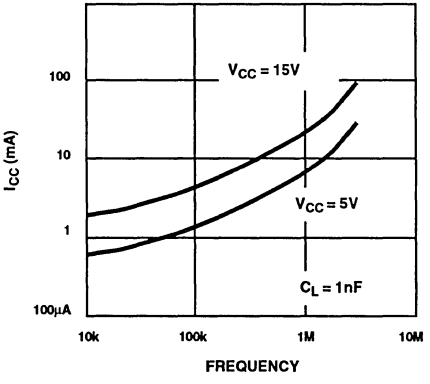
T_R, T_F vs. TEMPERATURE



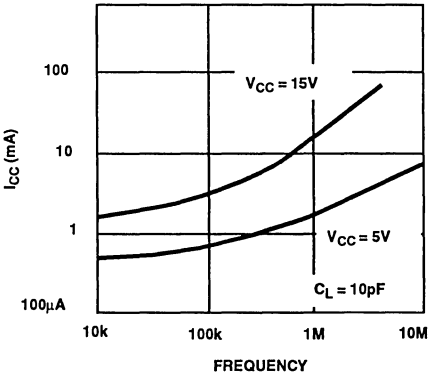
I_{CC} vs. C_L



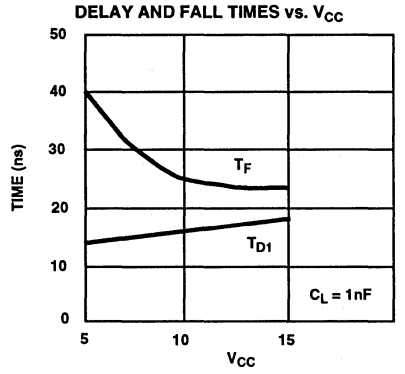
I_{CC} vs. FREQUENCY

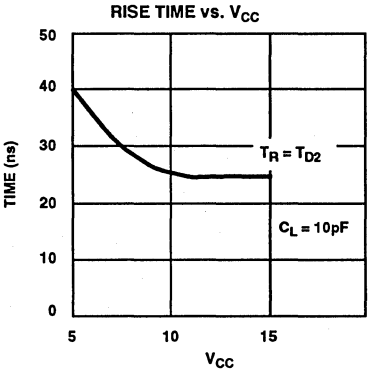


NO LOAD I_{CC} vs. FREQUENCY



Typical Performance Characteristics (Continued)





Detailed Description

The ICL7667 is a dual high-power CMOS inverter whose inputs respond to TTL levels while the outputs can swing as high as 15V. Its high output current enables it to rapidly charge and discharge the gate capacitance of power MOSFETs, minimizing the switching losses in switchmode power supplies. Since the output stage is CMOS, the output will swing to within millivolts of both ground and V_{CC} without any external parts or extra power supplies as required by the DS0026/56 family. Although most specifications are at V_{CC} = 15V, the propagation delays and specifications are almost independent of V_{CC}.

In addition to power MOS drivers, the ICL7667 is well suited for other applications such as bus, control signal, and clock drivers on large memory of microprocessor boards, where the load capacitance is large and low propagation delays are required. Other potential applications include peripheral power drivers and charge-pump voltage inverters.

Input Stage

The input stage is a large N-channel FET with a P-channel constant-current source. This circuit has a threshold of about 1.5V, relatively independent of the V_{CC} voltage. This means that the inputs will be directly compatible with TTL over the entire 4.5V - 15V V_{CC} range. Being CMOS, the inputs draw less than 1µA of current over the entire input voltage range of ground to V_{CC}. The quiescent current or no load supply current of the ICL7667 is affected by the input voltage, going to nearly zero when the inputs are at the 0 logic level and rising to 7mA maximum when both inputs are at the 1 logic level. A small amount of hysteresis, about 50mV to 100mV at the input, is generated by positive feedback around the second stage.

Output Stage

The ICL7667 output is a high-power CMOS inverter, swinging between ground and V_{CC}. At V_{CC} = 15V, the output impedance of the inverter is typically 7Ω. The high peak current capability of the ICL7667 enables it to drive a 1000pF load with a rise time of only 40ns. Because the output stage impedance is very low, up to 300mA will flow through the series N- and P-channel output devices (from V_{CC} to ground) during output transitions. This crossover current is responsible for a significant portion of the internal power dissipation of the ICL7667 at high frequencies. It can be minimized by keeping the rise and fall times of the input to the ICL7667 below 1µs.

Application Notes

Although the ICL7667 is simply a dual level-shifting inverter, there are several areas to which careful attention must be paid.

Grounding

Since the input and the high current output current paths both include the ground pin, it is very important to minimize and common impedance in the ground return. Since the ICL7667 is an inverter, any common impedance will generate negative feedback, and will degrade the delay, rise and fall times. Use a ground plane if possible, or use separate ground returns for the input and output circuits. To minimize any common inductance in the ground return, separate the input and output circuit ground returns as close to the ICL7667 as is possible.

Bypassing

The rapid charging and discharging of the load capacitance requires very high current spikes from the power supplies. A parallel combination of capacitors that has a low impedance over a wide frequency range should be used. A 4.7µF tantalum capacitor in parallel with a low inductance 0.1µF capacitor is usually sufficient bypassing.

Output Damping

Ringing is a common problem in any circuit with very fast rise or fall times. Such ringing will be aggravated by long inductive lines with capacitive loads. Techniques to reduce ringing include:

1. Reduce inductance by making printed circuit board traces as short as possible.
2. Reduce inductance by using a ground plane or by closely coupling the output lines to their return paths.
3. Use a 10Ω to 30Ω resistor in series with the output of the ICL7667. Although this reduces ringing, it will also slightly increase the rise and fall times.

4. Use good bypassing techniques to prevent supply voltage ringing.

Power Dissipation

The power dissipation of the ICL7667 has three main components:

1. Input inverter current loss
2. Output stage crossover current loss
3. Output stage I^2R power loss

The sum of the above must stay within the specified limits for reliable operation.

As noted above, the input inverter current is input voltage dependent, with an I_{CC} of 0.1mA maximum with a logic 0 input and 6mA maximum with a logic 1 input.

The output stage crowbar current is the current that flows through the series N- and P-channel devices that form the output. This current, about 300mA, occurs only during output transitions. **Caution:** The inputs should never be allowed to remain between V_{IL} and V_{IH} since this could leave the output stage in a high current mode, rapidly leading to destruction of the device. If only one of the drivers is being used, be sure to tie the unused input to a ground. **NEVER** leave an input floating. The average supply current drawn by the output stage is frequency dependent, as can be seen in I_{CC} vs. Frequency graph in the Typical Characteristics Graphs.

The output stage I^2R power dissipation is nothing more than the product of the output current times the voltage drop across the output device. In addition to the current drawn by any resistive load, there will be an output current due to the charging and discharging of the load capacitance. In most high frequency circuits the current used to charge and discharge capacitance dominates, and the power dissipation is approximately

$$P_{AC} = CV_{CC}^2f$$

where C = Load Capacitance, f = Frequency

In cases where the load is a power MOSFET and the gate drive requirement are described in terms of gate charge, the ICL7667 power dissipation will be

$$P_{AC} = Q_GV_{CC}f$$

where Q_G = Charge required to switch the gate, in Coulombs,
f = Frequency.

Power MOS Driver Circuits

Power MOS Driver Requirements

Because it has a very high peak current output, the ICL7667 the at driving the gate of power MOS devices. The high current output is important since it minimizes the time the power MOS device is in the linear region. Figure 4 is a typical curve of charge vs. gate voltage for a power MOSFET. The flat region is caused by the Miller capacitance, where the drain-to-gate capacitance is multiplied by the voltage gain of the FET. This increase in capacitance occurs while the power MOSFET is in the linear region and is dissipating significant amounts of power. The very high current output of the ICL7667 is able to rapidly overcome this high capacitance and quickly turns the MOSFET fully on or off.

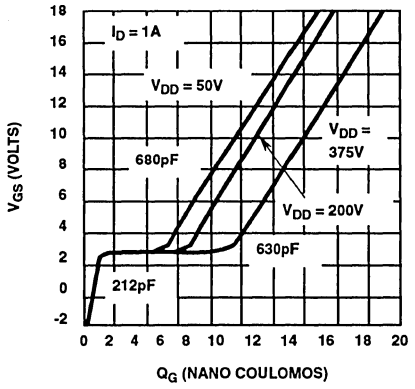


FIGURE 4: MOSFET GATE DYNAMIC CHARACTERISTICS

Direct Drive of MOSFETs

Figure 6 shows interfaces between the ICL7667 and typical switching regulator ICs. Note that unlike the DS0026, the ICL7667 does not need a dropping resistor and speedup capacitor between it and the regulator IC. The ICL7667, with its high slew rate and high voltage drive can directly drive the gate of the MOSFET. The 1527 IC is the same as the 1525 IC, except that the outputs are inverted. This inversion is needed since ICL7667 is an inverting buffer.

Transformer Coupled Drive of MOSFETs

Transformers are often used for isolation between the logic and control section and the power section of a switching regulator. The high output drive capability of the ICL7667 enables it to directly drive such transformers. Figure 6 shows a typical transformer coupled drive circuit. PWM ICs with either active high or active low output can be used in this circuit, since any inversion required can be obtained by reversing the windings on the secondaries.

Buffered Drivers for Multiple MOSFETs

In very high power applications which use a group of MOSFETs in parallel, the input capacitance may be very large and it can be difficult to charge and discharge quickly. Figure 8 shows a circuit which works very well with very large capacitance loads. When the input of the driver is zero, Q1 is held in conduction by the lower half of the ICL7667 and Q2 is clamped off by Q1. When the input goes positive, Q1 is turned off and a current pulse is applied to the gate of Q2 by the upper half of the ICL7667 through the transformer, T1. After about 20ns, T1 saturates and Q2 is held on by its own C_{gs} and the bootstrap circuit of C1, D1 and R1. This bootstrap circuit may not be needed at frequencies greater than 10kHz since the input capacitance of Q2 discharges slowly.

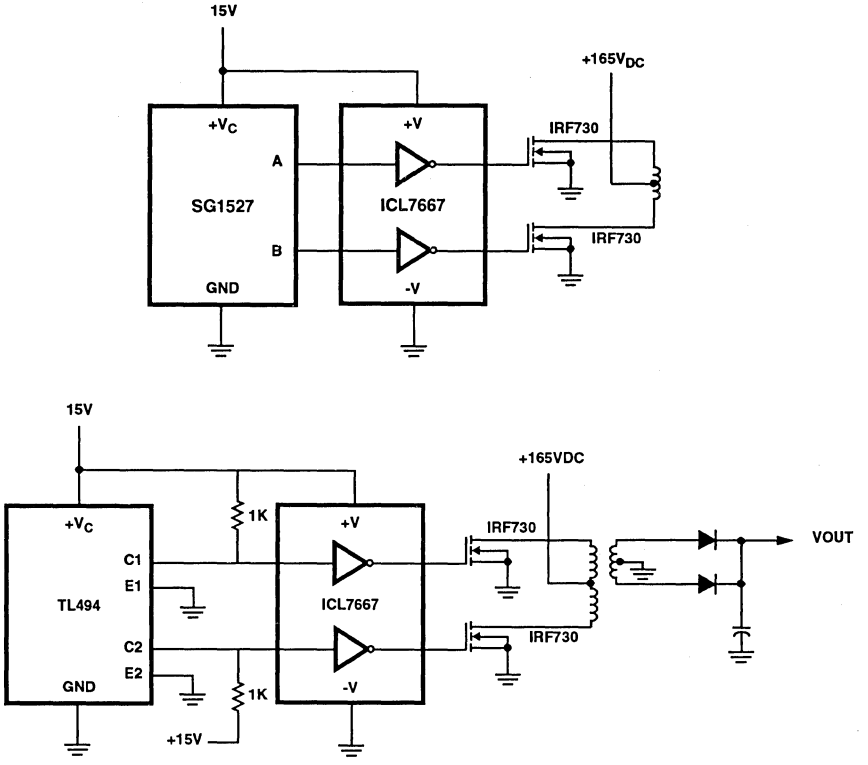


FIGURE 5. DIRECT DRIVE OF MOSFET GATES

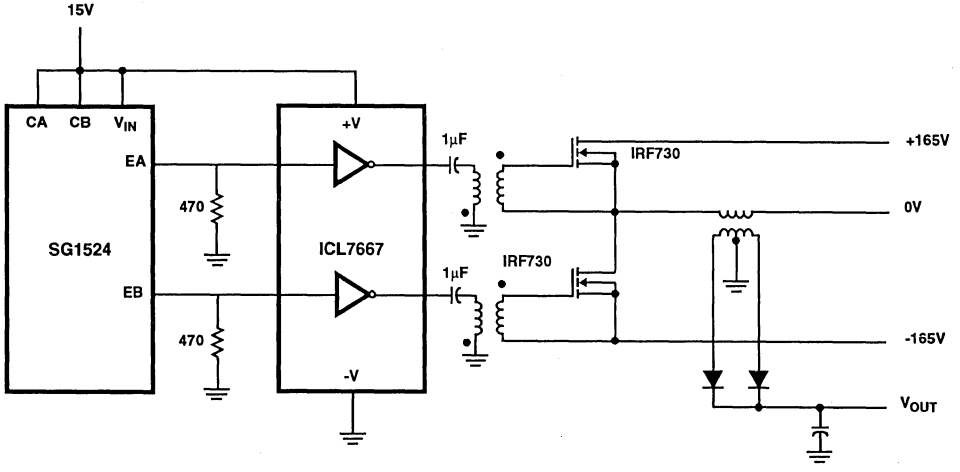


FIGURE 6. TRANSFORMER COUPLED DRIVE CIRCUIT

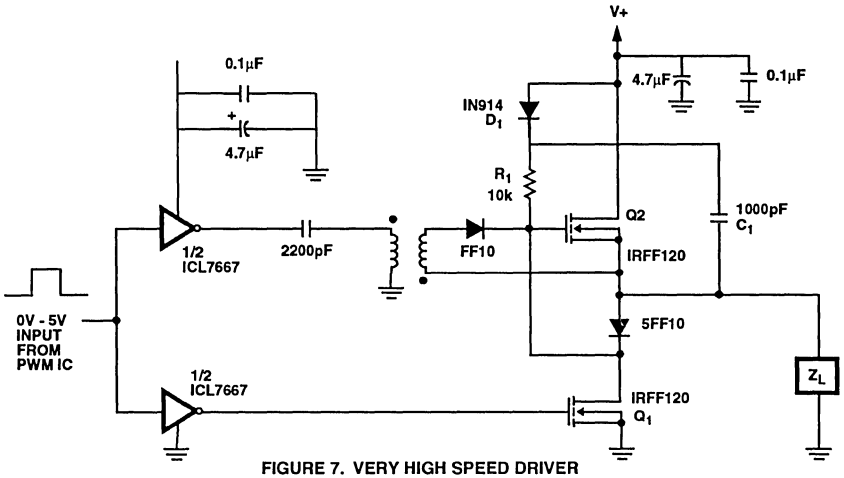
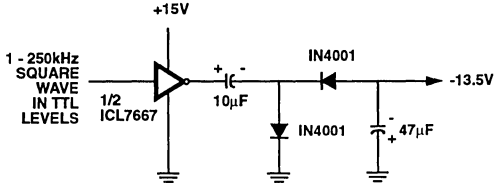


FIGURE 7. VERY HIGH SPEED DRIVER



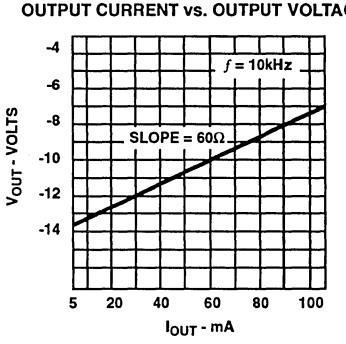


FIGURE 8. VOLTAGE INVERTER

Other Applications

Relay and Lamp Drivers

The ICL7667 is suitable for converting low power TTL or CMOS signals into high current, high voltage outputs for relays, lamps and other loads. Unlike many other level translator/driver ICs, the ICL7667 will both source and sink current. The continuous output current is limited to 200mA by the I^2R power dissipation in the output FETs.

Charge Pump or Voltage Inverters and Doublers

The low output impedance and wide V_{CC} range of the ICL7667 make it well suited for charge pump circuits. Figure 8 shows a typical charge pump voltage inverter circuit and a typical performance curve. A common use of this circuit is to provide a low current negative supply for analog circuitry or RS232 drivers. With an input voltage of +15V, this circuit will deliver 20mA at -12.6V. By increasing the size of the capacitors, the current capability can be increased and the voltage loss decreased. The practical range of the input frequency is 500Hz to 250kHz. As the frequency goes up, the charge pump capacitors can be made smaller, but the internal losses in the ICL7667 will rise, reducing the circuit efficiency.

Figure 9, a voltage doubler, is very similar in both circuitry and performance. A potential use of Figure 8 would be to supply the higher voltage needed for EEPROM or EPROM programming.

Clock Driver

Some microprocessors (such as the 68XX and 65XX families) use a clock signal to control the various LSI peripherals of the family. The ICL7667's combination of low propagation delay, high current drive capability and wide voltage swing make it attractive for this application. Although the ICL7667 is primarily intended for driving power MOSFET gates at 15V, the ICL7667 also works well as a 5V high-speed buffer. Unlike standard 4000 series CMOS, the ICL7667 uses short channel length FETs and the ICL7667 is only slightly slower at 5V than at 15V.

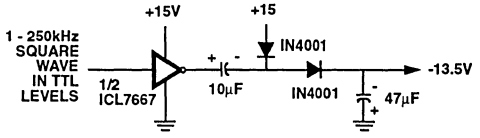


FIGURE 9. VOLTAGE DOUBLER

INTELLIGENT POWER ICs

4

HALF BRIDGES

Half Bridge Selection Guide

MOSFET Driver Circuits

TYPE	FUNCTION	MAX. BUS VOLT	RECOMMENDED SUPPLY VOLT	MAX. PULSED GATE CURRENT	MAX. PWM FREQ.	SHOOTTHRU PROTECTION	PKG.	RECOMMENDED APPLICATION
CA3169	$^1/_2$ H Driver	N/A	10.5V to 18V	N/A	40kHz	Yes	5 Lead TO-220	Motor Control
HIP2500	N-Channel Half Bridge	$500V_{DC}$	10 to $15V_{DC}$	2 Amps	100kHz	No	14 PDIP	Motor Control SMPS
HIP2501	N-Channel 3 Phase	$500V_{DC}$	10 to $15V_{DC}$	0.5 Amp	100kHz	No	18 PDIP	Motor Control SMPS
SP600	N-Channel Half Bridge	$500V_{DC}$	14.5 to $16.5V_{DC}$	0.5 Amp	20kHz	Yes	22 PDIP	Motor Control
SP601	N-Channel Half Bridge	$500V_{DC}$	14.5 to $16.5V_{DC}$	0.5 Amp	20kHz	Yes	22 PDIP	Motor Control
HIGH SIDE DRIVERS THAT CAN BE USED IN HALF BRIDGE CONFIGURATION								
HV400	N-Channel Power Driver	$30V_{DC}$	15 to $30V_{DC}$	6A (ON) Source 30A(OFF) Sink	20KHz(MC) 200KHz (SMDS)	N/A	8PDIP 8 SOIC	Motor Control SMPS
ICL7667	N, P-Channel Half Bridge Driver	$15V_{DC}$	4.5 to $15V_{DC}$	0.3 Amp	1MHz	No	TO-99 8 PDIP	Motor Control SMPS

HARRIS SEMICONDUCTOR

CA3169

Solenoid and Motor Driver (1/2 H Driver)

April 1992

Features

- Chip Encapsulated in a 5-Lead Plastic TO-220 Style Package (VERSA-VI)
- Output Short Circuit Protection
- Thermal Overload Protection
- Solenoid Inductive "Kick" Protection with Internal-Clamp Diodes
- Output Sink and Source Capacity of 600mA Minimum Overtemperature
- Horizontal and Vertical Mounting Packages Available
- Separate Sink Circuit and Source Circuit, Each Individually Controlled

Applications

- Latching Solenoid Driver (Single and Multiple)
- Non-Latching Solenoid Driver
- Relay Driver
- Lamp Controller
- Lamp Driver
- Motor Controller (Forward and Reverse)
- Stepper Motor Controller
- On-Off Logic Controllers (TTL Logic)
- Intermediate Power Driver
- Triac, SCR, and Transistor Drivers

Description

The CA3169 ia a monolithic integrated circuit capable of driving lamps and other devices that can be changed between two states (on or off). Transistors, SCR's, and triacs are some of the solid state devices that can be controlled by the CA3169. This device can also control relays, solenoids (latching or nonlatching), motors (DC - forward and reverse) and DC stepping motors.

The CA3169 contains a separate source driver circuit with internal current limiting protection and a separate sink driver circuit. The sink driver contains an energy absorbing diode to protect the device against any inductive "kick" during state changes. The CA3169 is protected against overvoltage conditions on the output drivers and overtemperature conditions (thermal-shutdown protection).

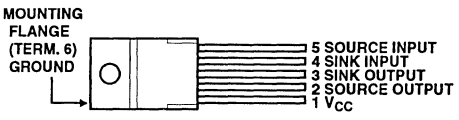
The input operating levels are TTL compatible. The source and sink outputs are in their off condition (non-conducting) when their respective inputs are in a HI state, or open-circuited. The outputs are in their on state (conducting) when their respective inputs are LO. The VERSA-VI package is available with two lead configurations. The CA3169 has a vertical-mount lead form, and the CA3169M has a horizontal-mount lead form.

Ordering Information

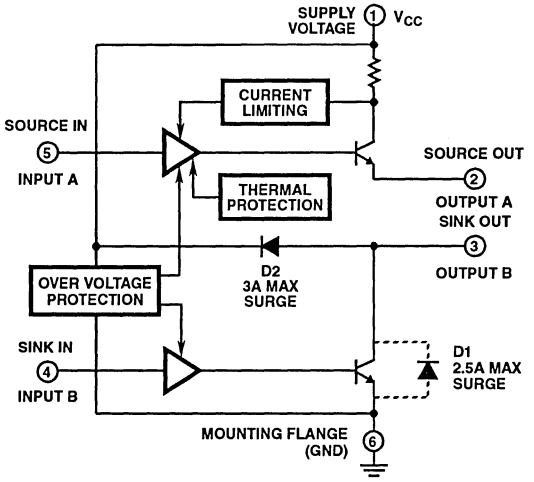
PART NUMBER	TEMPERATURE	PACKAGE
CA33169	-40°C to +85°C	5 Lead Plastic SIP Staggered Vertical
CA33169M	-40°C to +85°C	5 Lead Plastic SIP Surface Mount

Pinout

5 PIN PLASTIC TO-220 SIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1277.2

Absolute Maximum Ratings

Supply Voltage (Pin 1 to GND)
- Positive ..... 41V DC
- Negative ..... 1.4V DC
- Sink Current 1.9A
- Source Current ..... Controlled by Internal Current Limiting

Input Voltage:
- Sink Input (Pin 4 to GND) 17V
- Source Input (Pin 5 to GND) 17V

Maximum Forward Current - Diode D1 ..... 2.5A
Maximum Forward Current - Diode D2 ..... 3A
Power Dissipation, P_D at T_A = 90°C 15W
Thermal Resistance, Junction to Case: ..... 4°C/W
- Junction Temperature ..... +150°C
- Operating Temperature ..... -40°C to +85°C
- Storage Temperature ..... -55°C to +150°C

Lead Temperature (During Soldering):
At Distance 1/16 ± 1/32 in. (1.59 ± 0.79mm)
- from case for 10s max. ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications at T_A = +25°C, V_{CC} = 10.5V to 18V Unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current, Pin 2 See Figure5		Inputs Open V_{CC} = 4V to 18V Source and Sink Loads = 20Ω	-110	±0.5	110	µA
Output Leakage Current, Pin 3 See Figure 5		Inputs Open V_{CC} = 4V to 18V Source and Sink Loads = 20Ω	-110	±0.5	110	
Thermal Resistance	θ_{JC}		-	3	4	°C/W
Quiescent Current, Pin 1 See Figure 4		Device "ON" Input Terminals Shorted, V_{CC} = 14V	-	70	100	mA
Quiescent Current, Pin 1 See Figure 3		Device "OFF" Input Terminals Open, V_{CC} = 14V	-	17	40	
Thermal Shutdown Temperature		R_L = Short Circuit	128	140	162	°C
Overvoltage Shutdown -Circuit Upper Trip Point, Pin 1 Voltage See Figure7		R_L = 20Ω	20	25	27	V
Overvoltage Shutdown - Circuit Lower Trip Point, Pin 1 Voltage See Figure 7		R_L = 20Ω	18	21.4	23	
Input Logic Levels; Source Input - Pin 5, Sink Input - Pin 4						
Input Low Threshold Sink or Source	V_{IL}	V_{CC} = 14V (See Note 1)	-	0.4	0.8	V
Input High Threshold Sink or Source	V_{IH}	V_{CC} = 14V (See Note 2)	1.9	2.4	-	
Input Low Current Sink or Source	I_{LL}	$V_{IN} \leq 0.4V$	-0.9	-0.3	-	mA
Input High Current Sink or Source	I_{IH}	$V_{IN} \leq 5.5V$	-110	-23	110	µA
Output Voltage, Pin 2 See Figure 6	V_{OS}	Referenced to V_{CC} with I_{SOURCE} = 600mA, See Note 3	-	1	1.6	V
Short-Circuit Current Limit, Pin 2 to Ground			0.65	1.11	2.6	A
Turn-On Delay to Output-On, Pin 2		C_L = 100pF, RL = 33Ω	-	0.45	5.6	µs
Turn-Off Delay to Output-Off, Pin 2		C_L = 100pF, RL = 33Ω	-	5	55	µs
Sink Outputs						
Output Saturation Voltage See Figure 9	V_3	I_{SINK} = 600mA VIN ≤ 0.4V See Note 3	-	0.3	0.85	V
Output Saturation Voltage See Figure 9	V_3	I_{SINK} = 1000mA VIN ≤ 0.4V See Note 3	-	0.8	1.65	

Electrical Specifications at T_A = +25°C, V_{CC} = 10.5V to 18V Unless otherwise specified. **(Continued)**

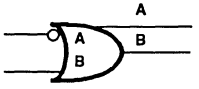
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Turn-On Delay to Output-On Pin 3	T_{ON}	CL = 100pF, RL = 33Ω to V_{CC}	-	0.45	5.6	µs
Turn-Off Delay to Output-Off Pin 3	T_{OFF}	CL = 100pF, RL = 33Ω to V_{CC}	-	0.95	25	

NOTES:

1. I_{SOURCE} or $I_{SINK} \leq 600mA$, $V_{OS} \leq 1.5V$, $V_{SINK} \leq 0.75V$.
2. I_{SOURCE} or $I_{SINK} \leq 100\mu A$, V_{SOURCE} = GND, for V_{SINK} 20Ω to V_{CC}.
3. Measured over temperature range of -40°C to +85°C.

TRUTH TABLE FOR SOLENOID DRIVER
TTL Logic Conditions: 0 ≤ VL ≤ 0.8, 1.9 ≤ VH ≤ 5.5

INPUT A SOURCE IN	INPUT B SINK IN	OUTPUT A SOURCE OUT	OUTPUT B SINK OUT
V_L	V_L	HIGH (ON)	LOW (ON)
V_L	V_H	HIGH (ON)	(OFF)
V_H	V_L	(OFF)	LOW (ON)
V_H	V_H	(OFF)	(OFF)



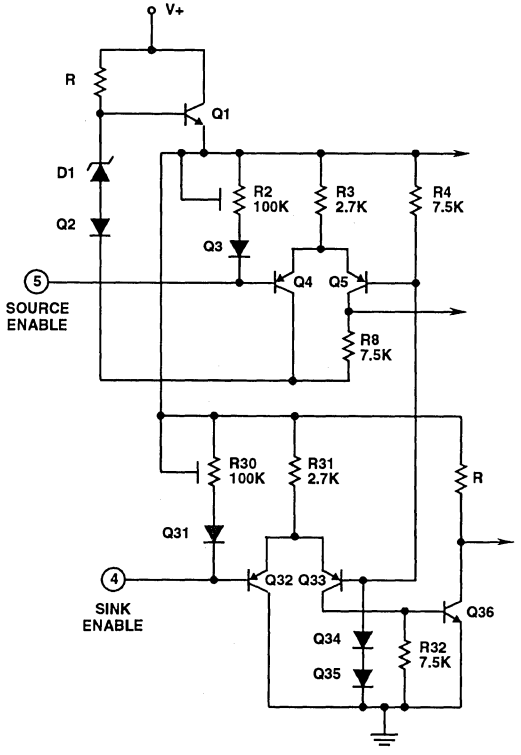


FIGURE 1. DETAILED SCHEMATIC OF THE INPUT CIRCUIT FOR CA3169.

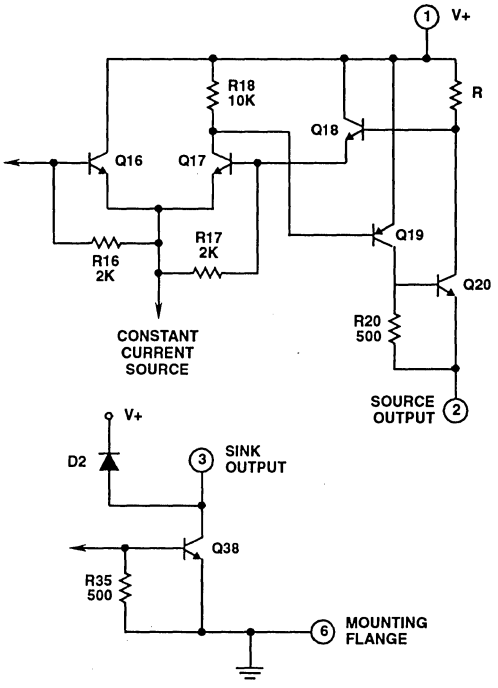


FIGURE 2. DETAILED SCHEMATIC OF THE OUTPUT CIRCUIT FOR CA3169.

Test Circuits

(VCC = VIN = PIN 1 VOLTAGE)

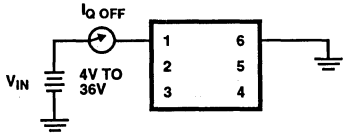


FIGURE 3. QUIESCENT CURRENT DEVICE "OFF".

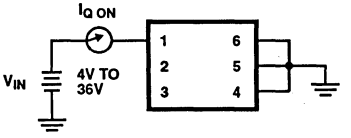


FIGURE 4. QUIESCENT CURRENT DEVICE "ON".

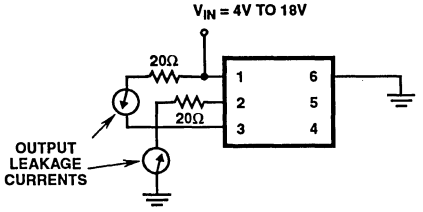


FIGURE 5. OUTPUT LEAKAGE CURRENTS.

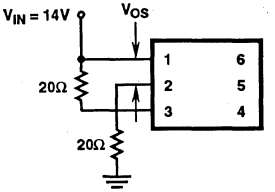
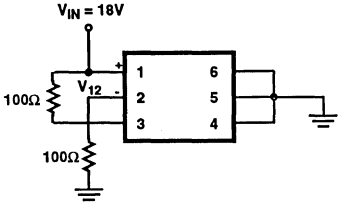
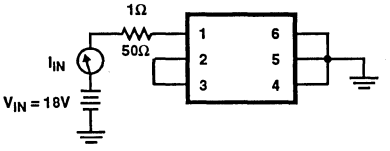


FIGURE 6. OUTPUT SOURCE VOLTAGE (REFERENCED TO VCC).





PROCEDURE

1. Measure V12.
2. Increase V_{CC} until V12 ≥ 2V.
3. Measure V_{CC}; this voltage is the high trip point. Pin 2 should be off; i.e., pin 3 should be high.
4. Observe and measure the voltage at pin 3.
5. Decrease V_{CC} until pin 3 switches, i.e., ≤ 18V. The supply voltage will be the low trip point voltage.

FIGURE 7. OVERVOLTAGE PROTECTION.

When V_{CC} is turned on, IIN should be equal to or greater than 1A. Thermal shutdown will operate properly if the input current drops below 0.5A (0.3A typ.) in 10 to 15 seconds. Cover the unit during this test in the event that the thermal shutdown is not operating properly.

FIGURE 8. THERMAL SHUTDOWN.

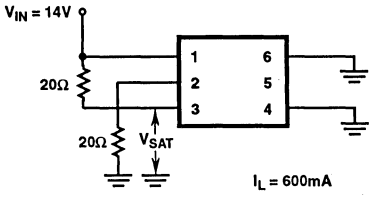
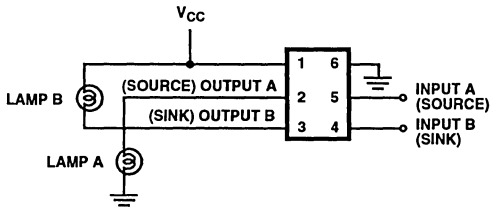


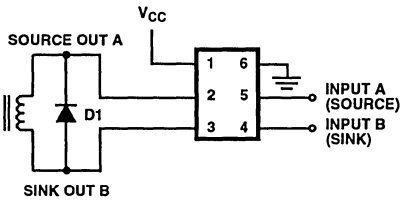
FIGURE 9. OUTPUT SATURATION VOLTAGE.

Typical Applications



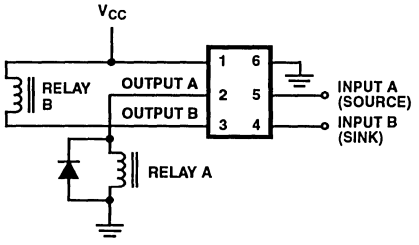
When input A goes low, lamp A will light.
When input B goes low, lamp B will light.

FIGURE 10. LAMP DRIVER.



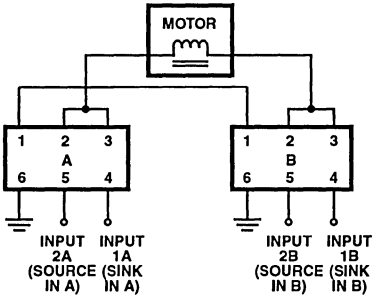
Input A and input B must both be low for the solenoid to switch.

FIGURE 11. NON-LATCHING SOLENOID.



Relay A will close when in input A goes low. Relay B will close when input B goes low. Both relays will close when both inputs go low.

FIGURE 12. RELAY DRIVER.



When opposing inputs go low, the motor will switch direction; if source input A and sink input B both go low, current will flow from A to B. If source input B and sink input A both go low, current will flow from B to A.

FIGURE 13. MOTOR DRIVER OR LATCHING SOLENOID DRIVER.

HARRIS SEMICONDUCTOR

HIP2500

PRELIMINARY

May 1992

Half-Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive N-Channel Power Devices
- Floating Bootstrap Power Supply for Upper Rail Drive
- CMOS S4chmitt-Triggered Inputs with Hysteresis and Pull-Down
- 100kHz Operation
- Single Low Current Bias Supply Operation .... 7mA Typ
- Latch-up Immune CMOS Logic
- Peak Drive .....Up to 2.0A
- Gate Drive Switching Time ..... < 150ns Typ

Applications

- High Frequency Switch-Mode Power Supply
- Induction Heating and Welding
- Switch Mode Amplifiers
- AC and DC Motor Drives
- Electronic Lamp Ballasts
- Battery Chargers
- UPS Inverters

Description

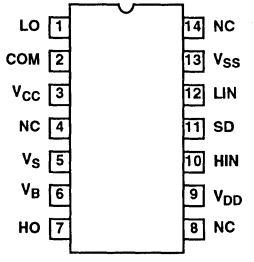
The HIP2500 is a high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control for PWM motor drive, power supply, and UPS applications.

Ordering Information

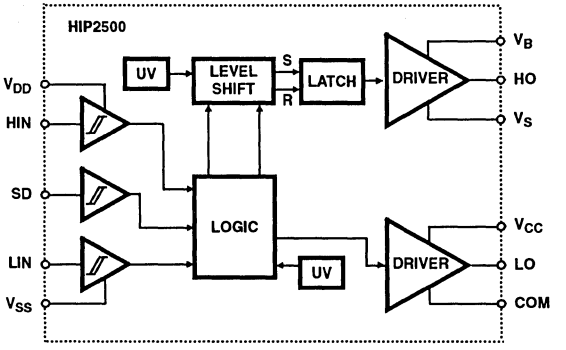
PART	TEMPERATURE	PACKAGE
HIP2500IP	-40°C to +85°C	14 Lead Plastic DIP

Pinout

14 PIN PLASTIC DIP
TOP VIEW



Functional Block Diagram



File Number **2801.1**

Absolute Maximum Ratings

Full Temperature Range Unless Otherwise Noted, All Voltages Referenced to V_{SS} Unless Otherwise Noted.

Floating Supply Voltage, V_B . . . . . V_S-0.5V to V_S+16.5V (Positive Terminal)
Floating Supply Voltage, V_S . . . . . 500V (Common Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . -0.5V to V_B+0.5V
Fixed Supply Voltage, V_{CC} . . . . . -0.5V to 16.5V
Low Side Channel Output Voltage, V_{LO} . . . . . -0.5V to V_{CC}+0.5V
Logic Supply Voltage, V_{DD} . . . . . -0.5V to 16.5V
Logic Input Voltage, V_{IN} . . . . . -0.5V to V_{DD}+0.5V [HIN, LIN & SD (Shutdown)]

Thermal Characteristics

Thermal Resistance, Junction-to-Ambient θ_{ja}
Plastic DIP Package . . . . . 75°C/W
Maximum Package Power Dissipation at +85°C
Plastic DIP Package 500mW
Maximum Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range, T_S . . . . . -40°C to +150°C
Operating Ambient Temperature Range, T_A . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended DC Operating Conditions

Floating Supply Voltage, V_B . . . . . V_S+10V to V_S+15V (Floating Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . 10V to V_B (With Respect to V_S)
Fixed Supply Voltage, V_{CC} . . . . . 10V to 15V
Low Side Channel Output Voltage, VLO . . . . . 0V to V_{CC}
Logic Supply Voltage, V_{DD} . . . . . 4V to V_{CC}
Floating Supply Voltage, V_S . . . . . -4.0V to 500V (Common Terminal)

Electrical Specifications

V_{CC} = (V_B-V_S) = V_{DD} = 15V, C_{OM} = V_{SS} = 0 and T_A = +25°C, Unless Otherwise Noted

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS					
Quiescent V_{CC} Current	I_{QCC}	-	1.4	1.7	mA
Quiescent V_{BS} Current	I_{QBS}	-	280	400	µA
Quiescent V_{DD} Current	I_{QDD}	-	0.1	1	µA
Logic Input Bias Current, V_{IN} = V_{DD} (HIN, LIN, SD)	IN+	-	12	20	µA
Logic Input Leakage Current, V_{IN} = V_{SS} (HIN, LIN, SD)	IN-	-	0	1	µA
Logic Input Positive Going Threshold	V_{TH}+	7.5	8.0	8.5	V
Logic Input Negative Going Threshold	V_{TH}-	5.5	5.9	6.3	V
Undervoltage Positive Going Threshold	UV+	6.8	8.3	9.85	V
Undervoltage Negative Going Threshold	UV-	6.3	8.2	9.5	V
Output High Open Circuit Voltage (HO, LO)	V_{OUT}+	-	-	15	V
Output Low Open Circuit Voltage (HO, LO)	V_{OUT}-	-	-	0.1	V
Output High Short Circuit Current (Sourcing)	I_{OUT}+	1.9	2.3	-	A
Output Low Short Circuit Current (Sinking)	I_{OUT}-	2	2.5	-	A

Switching Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
HIGH SIDE CHANNEL WITH 500V OFFSET, CL = 1000pF					
High Side Turn-On Propagation Delay	t_{ON}	350	420	500	ns
High Side Turn-Off Propagation Delay	t_{OFF}	300	365	450	ns
High Side Turn-On Rise Time	t_R	20	28	35	ns
High Side Turn-Off Fall Time	t_F	20	28	35	ns
LOW SIDE CHANNEL, CL = 1000pF					
Low Side Turn-on Propagation Delay	t_{ON}	275	350	425	ns
Low Side Turn-off Propagation Delay	t_{OFF}	225	275	330	ns
Low Side Turn-on Rise Time	t_R	20	27	35	ns
Low Side Turn-off Fall Time	t_F	20	27	35	ns
Shutdown Propagation Delay High Side Shutdown	t_{SDHO}	300	385	450	ns
Low Side Shutdown	t_{SDLO}	240	300	360	ns
HIGH SIDE CHANNEL WITH 500V OFFSET, CL = 1000pF					
Propagation Delay Matching (Between HO and LO)	M_t	0	-	75	ns
Minimum On Output Pulse Width (HO, LO)	$PW_{OUT(MIN)}$	-	35	50	ns
Minimum Input Pulse Width (ON)	$PW_{ON(MIN)}$	-	200	250	ns
Minimum Input Pulse Width (OFF)	$PW_{OFF(MIN)}$	-	245	350	ns
Deadtime LO Turn-off to HO Turn-on	DHt_{ON}	125	145	170	ns
Deadtime HO Turn-off to LO Turn-on	DLt_{ON}	15	25	120	ns
MAXIMUM TRANSIENT CONDITIONS					
Offset Supply Operating Transient	dV_S/dt	-	-	50	V/ns

Logic Truth Table

HIN	LIN	UV_H	UV_L	SD	HO	LO	COMMENTS
0	0	0	0	0	0	0	Normal Off
0	1	0	0	0	0	1	Lower On
1	0	0	0	0	1	0	Upper On
1	1	0	0	0	1	1	Both On
X	X	X	X	1	0	0	Chip Disabled
X	X	1	1	X	0	0	V_{CC} UV Lockout and V_{BS} Lockout
X	1	1	0	0	0	1	V_{BS} UV Lockout
1	X	0	1	0	1	0	V_{CC} UV Lockout

HARRIS SEMICONDUCTOR

SP600

May 1992

Half-Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive Standard and Current Sensing n-Channel Power MOSFET/IGBT Devices
- Creation and Management of a Floating Power Supply for Upper Rail Drive
- Simultaneous Conduction Lockout
- Overcurrent Protection
- Single Low Current Bias Supply Operation
- Latch Immune CMOS Logic
- Peak Drive in Excess of 0.5 Amp

Description

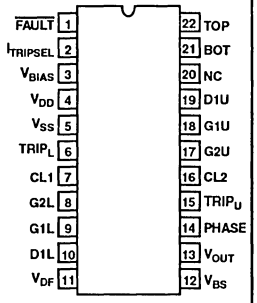
The SP600 is a smart power high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control and management for PWM motor drive, power supply, and UPS applications.

Ordering Information

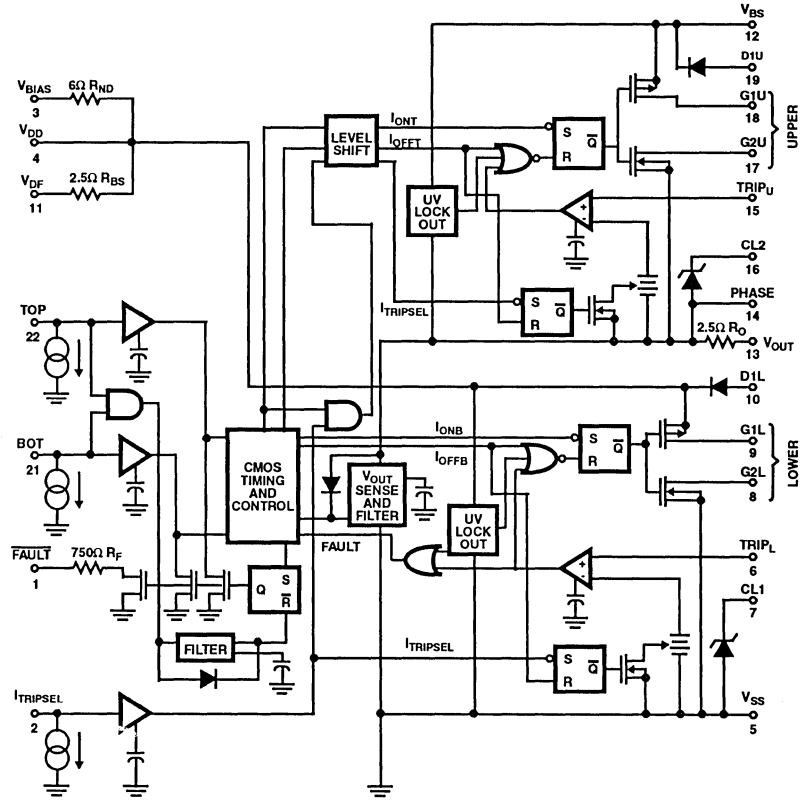
PART	TEMPERATURE	PACKAGE
SP600	-40°C to +85°C	22 Pin Plastic DIP

Pinout

22 PIN DIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2428.2**

Absolute Maximum Ratings

Full Temperature Range, All Voltage Referenced to V_{SS} Unless Otherwise Noted. Notes 1, 2.

Low Voltage Power Supply, V_{BIAS} (Note 1) ..... $18V_{DC}$
Floating Low Voltage Boot Strap ..... $18V_{DC}$
Power Supply to Phase, V_{BS}
Low Voltage Signal Pins
Fault, $I_{TRIP\ SEL}$, V_{DD}, $TRIP_L$, CL1, G2L .....-0.5V_{DC} to V_{DD} +0.5
G1L, D1L, V_{DF}, TOP, BOT
CL2, $TRIP_U$, G1U, G2U, D1U to Phase ..... -0.5V_{DC} to V_{BS}+0.5
High Voltage Pins
Phase, V_{PHASE} ..... $500V_{DC}$
(V_{BS}, V_{OUT}, $TRIP_U$, CL2, G2U & D1U: 0V-18V Higher Than Phase)
Dynamic High Voltage Rating Phase,..... 10,000V/µs
$DV_{PHASE/dt}$

Power Dissipation and Thermal Characteristics

Thermal Resistance, Junction-to-Ambient θ_{ja}
Plastic DIP Package 75°C/W
Maximum Package Power Dissipation at T_A = +85°C, P_O
Plastic DIP Package 500mW
Operating Ambient Temperature Range, T_A .....-25°C to +85°C
Storage Temperature Range, T_S.....-40°C to +150°C

NOTES:
1. Care must be taken in the application of V_{BIAS} as not to impose high peak dissipation demands on a relatively small metallized noise dropping resistor (R_{ND}). Prolonged high peak currents may result if +15V_{DC} is applied abruptly and/or if the local bypass capacitor C_{DD} is large. It is suggested that C_{DD} be ≤ 10MFD. If it is desirable to switch the 15V_{DC} source or if a C_{DD} is larger, additional series impedance may be required.
2. Consult factory for additional package offerings.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Current (5V < V_{TOP}, V_{BOT}, $V_{TRIP_{SEL}}$ < 15V)	I_{IN}	+25°C	-	20	30	µA
		-40°C to +85°C	-	30	33	µA
I_{BIAS} Quiescent Current (All Inputs Low)	I_{BIAS_L}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BIAS} Quiescent Current ($V_{OUT} \geq V_{BIAS}$, and All Inputs Low)	I_{BIAS_H}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BS} Quiescent Current Bootstrap Supply	I_{BS}	+25°C	-	875	1000	µA
		-40°C to +85°C	-	900	1060	µA
TOP Threshold Level	V_{TOP}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
BOTTOM Threshold Level	V_{BOT}	+25°C	7	8	9	V
		-40°C to +85°C	6.9	8	9.1	V
Current Trip Select Threshold Level	$V_{TRIP_{SEL}}$	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Trip Lower and Upper Comparator Threshold Level - Normal ($I_{TRIP_{SEL}}$ = V_{SS})	$V_{TRIP\ L/U_N}$	+25°C	90	105	125	mV
		-40°C to +85°C	90	105	127	mV
Trip Lower and Upper Comparator Threshold Level - Boost ($I_{TRIP_{SEL}}$ = V_{DD}) % of Measured $V_{TRIP\ L/U_N}$	$V_{TRIP\ L/U_B}$	+25°C	110	130	150	%
		-40°C to +85°C	109	130	152	%
Under Voltage Lockout Thresholds (V_{DD} & V_{BS})	V_{LOCK}	+25°C	9	10	11.5	V
		-40°C to +85°C	9.7	10.5	11.8	V
Phase Out of Status Voltage Threshold (PHASE)	V_{OSVT}	+25°C	5	7	9	V
		-40°C to +85°C	4.7	7	9.6	V
Faultbar Impedance at I_{FBAR} = 1mA	RF	+25°C	500	760	1000	Ω
		-40°C to +85°C	450	760	1100	Ω

Electrical Specifications (V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Upper/Lower Source Impedances (I_{Source} = 10mA)	$R_{SO\ L/U}$	+25°C	12	17	23	Ω
		-40°C to +85°C	7	17	29	Ω
Upper/Lower Sink Impedances (I_{SINK} = 10mA)	$R_{SI\ L/U}$	+25°C	8	12	16	Ω
		-40°C to +85°C	5	12	20	Ω
Bootstrap Supply Current Limiting Impedance	R_{BS}	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω
Noise Dropping Resistor Impedance	R_{ND}	+25°C	6	10	14	Ω
		-40°C to +85°C	5.4	10	14.6	Ω
High Voltage Leakage (500V V_{BS}, V_{OUT}, PHASE, $TRIP_U$, CL2, G1U, G2U, & D1U to V_{SS}. All other Pins at V_{SS})	I_{LK}	+25°C	-	1	3	µA
		-40°C to +85°C	-	1	3	µA
Miller Clamp Diodes; D1U and D1L (I_D = 10mA)	$V_{D1U/L}$	+25°C	1.05	1.4	1.7	V
		-40°C to +85°C	1.05	1.4	1.7	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 10mA)	$V_{CL2/1\text{-}Low}$	+25°C	6.35	6.61	6.85	V
		-40°C to +85°C	6.15	6.61	7.15	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 50mA)	$V_{CL2/1\text{-}High}$	+25°C	7.7	8.1	8.7	V
V_{OUT} Limiting Resistance	R_O	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω

NOTE: Maximum Steady State + $15V_{DC}$ Supply Current = I_{BIAS_L} + I_{BS}

Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_u$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Refresh One Shot Timer	t_{REF}	+25°C	200	350	500	µs
		-40°C to +85°C	180	350	540	µs
Delay Time of Trip I/u Voltage (I_{TRIP} sel. low) to G2U/G2L Low (50% Overdrive	$t_{OFF_{TN}}$	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Trip I Voltage (I_{TRIP} sel. low) to Faultbar Low	t_{FN}	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Phase Out of Status to Faultbar Low (TOP High)	t_{OSVF}	+25°C	500	700	900	ns
		-40°C to +85°C	400	700	1050	ns
Minimum Logic Input Pulse Width: TOP & BOTTOM	t_{MINIW}	+25°C	300	430	600	ns
		-40°C to +85°C	275	430	660	ns
Minimum G1U/G1L On Time	t_{ON}	+25°C	1.6	2.3	3.1	µs
		-40°C to +85°C	1.5	2.4	3.4	µs
Minimum Pulsed Off Time, G2U/G2L	t_{OFF}	+25°C	1.3	2.0	3.4	µs
		-40°C to +85°C	1.05	2.1	3.9	µs
Turn On Delay Time of G1U (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs
Turn On Delay Time of G1L (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs

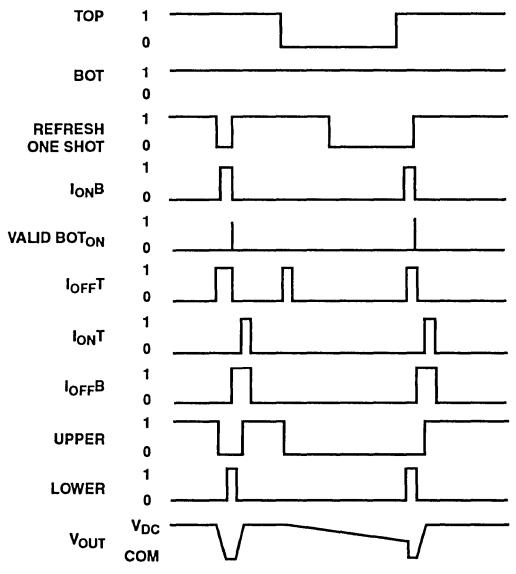
Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_u$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE) **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Turn On Delay Time of G1U (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn On Delay Time of G1L (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn Off Delay Time of G2U and G2L	t_{OFF_D}	+25°C	0.75	1.0	1.45	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Minimum Dead Time: G1U off to G1L on, or G1L off to G1U on (BISTATE MODE)	$t_{D.T.}$	+25°C	1.5	2.5	3.5	µs
		-40°C to +85°C	1.2	2.6	4	µs
Fault Reset Delay to Clear Faultbar	$t_{R.T.}$	+25°C	3.4	4.5	6.6	µs
		-40°C to +85°C	3.15	4.8	7.4	µs
Rise Time of Upper & Lower Driver (Load = 2000pF)	$t_{R\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns
Fall Time of Upper & Lower Driver (Load = 2000pF)	$t_{F\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns

Recommended Operating Conditions and Functional Pin Description (All Voltages Referenced to V_{SS}, Unless Otherwise Noted. See Figure 1)

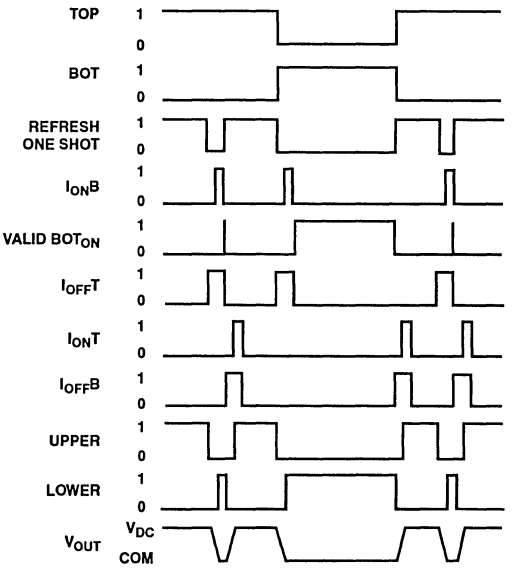
PARAMETER	CONDITION
Faultbar	Open Drain Fault Indicator Output
$I_{TRIP\ SELECT}$	Digital Input Command to Increase TRIP L and U Threshold by 30%
V_{BIAS}	14.5V to 16.5V with 15V nominal, ≅ 1.5mA DC BIAS Current
V_{DD}	C_{DD} to V_{SS}
V_{SS}	COMMON
Trip I	100mV Signal to Shut Off LOWER Drive and Trigger a Fault Output
CL1	Lower Noise Clamp Zener
G2L & G1L	Low Impedance Driver Designed to Drive Power MOS Transistors (LOWER)
V_{DF}	Current Limiting Charging Resistor for Bootstrap Capacitor Power Supply
V_{BS}	Bootstrap Supply, Normally a Diode Drop Below V_{DD} Voltage with Respect to the Floating PHASE Reference
V_{OUT}	Load Connection Node
Phase	Floating Reference Point for High Side Control Circuitry: V_{BS}, $TRIP_U$, CL2, G1U, G2U & D1U
$Trip_U$	100mV Signal, Referenced to PHASE, to Shut Off UPPER Drive
CL2	Upper Noise Clamp Zener
G2U & G1U	Low Impedance Driver Designed to Drive Power MOS Transistors (UPPER)
Top	Digital Input to Command the UPPER On
Bot	Digital Input to Command the LOWER On
D1U	Miller Clamp UPPER to V_{BS}
D1L	Miller Clamp LOWER to V_{DD}

Timing Diagram



TRISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER

NOTE: BOT switching not relevant.



BISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER

Typical Circuit Configuration

TRUTH TABLE

Applicable to Typical Circuit Configuration (Figure 1)

INPUTS						OUTPUTS		
TOP	BOT	$TRIP_L$	$TRIP_U$	PHASE	V_{BIAS}	UPPER	LOWER	FAULT BAR
0	0	0	X	X	1	0	0	1
1	1	0	0	1	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	0	X	0	1	0	0	0
X	X	1	X	X	1	0	0	0
0	1	0	X	X	1	0	1	1
1	0	0	X	X	1	0	0	1
X	X	X	X	X	0	0	0	0

NOTE: 0 = False, 1 = True, X = Don't Care

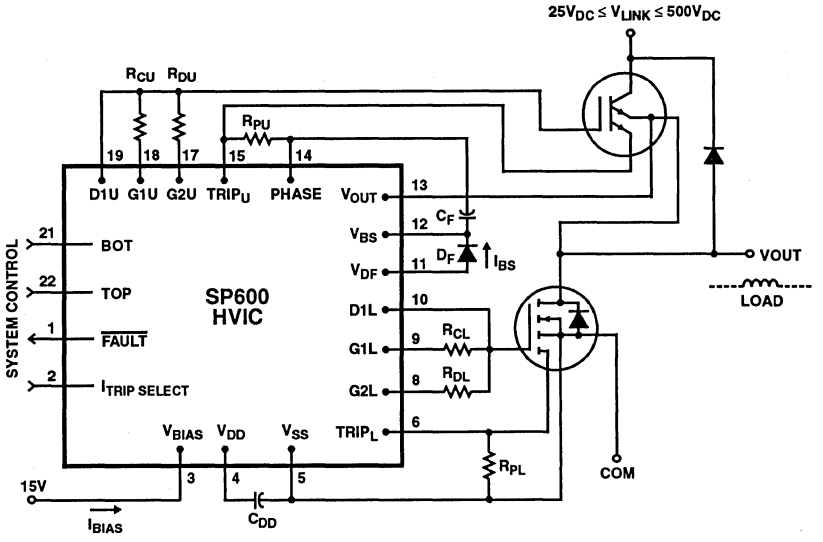


FIGURE 1. TYPICAL CIRCUIT CONFIGURATION

LEGEND		
Application Specific	R_{CU}	Upper Gate Charging Resistor
Application Specific	R_{DU}	Upper Gate Discharge Resistor
Application Specific	R_{PU}	Upper Current Pilot Resistor
Application Specific	R_{CL}	Lower Gate Charging Resistor
Application Specific	R_{DL}	Lower Gate Discharging Resistor
Application Specific	R_{PL}	Lower Current Pilot Resistor
3µF @ ≥ 15DC	C_{DD}	Local LV Filter Capacitor
0.22µF Ceramic X7R @ ≥ $15V_{DC}$	C_F	Flying Capacitor for Bootstrap Supply
Harris P/N A114M or Equiv PRV ≥ V_{LINK}	D_F	Flying Diode for Bootstrap Supply

Refer to 'Additional Product Offerings' for information concerning power output devices.

Functional Description

The SP600 provides a flexible, digitally controlled power function which is intended to be used as PWM drivers of n-channel MOSFETs and/or IGBTs for up to 240VAC line rectified totem-pole applications. The CMOS driveable inputs are filtered and captured by the control logic to determine the output state. The logic includes fixed timing to prohibit simultaneous conduction of the external power switches and, thru the V_{OUT} sense detector, verifies the output voltage state is in agreement with the controlled inputs. The > 11VDC floating power supply required to drive the upper rail external power device is created and managed by the HVIC through Cf and Df. This capacitor is refreshed from the V_{DD} supply each time V_{OUT} goes low. If the upper channel is commanded on for a long period of time, the bootstrap capacitor Cf is automatically refreshed by bringing V_{OUT} low. This is accomplished by turning off the upper rail MOSFET/IGBT, momentarily turning on the lower rail output device, followed by returning control back to the upper switch. Otherwise, Cf would gradually deplete its charge allowing the upper switch to come out of saturation. The upper and lower gate drivers allow for controlled charge and discharge rates as well as facilitate the use of nearly lossless current sensing power MOS devices. The over current trip level can be boosted 30% on a pulse by pulse basis by logic level '1' applied to $I_{TRIP\ SELECT}$. A $\overline{FAULT}$ output signal is generated when any of the following occurs:

V bias is low
Over current is detected
V phase doesn't agree with the input signal

Reset of $\overline{FAULT}$ is provided by externally removing power or by holding both TOP and BOT inputs low for the required reset time (trt_{MAX}).

Each application can be individually optimized by the selection of external components tailored to ensure proper overall system operation including:

Determining the ratings and sizing of MOSFETs and IGBTs, mixed or matched, as well as flyback diodes (FBD).

The selection of separate gate charge (R_C) & discharge (R_D) impedance chosen per the load capacitance, frequency of operation, and D_I/D_T dependent recovery characteristics of the associated FBDs. R_D should also be sized to prevent simultaneous bridge conduction by ensuring gate discharge in the allotted turn off pulse width ($t_{OFF\ MIN}$).

The selection of over current detection resistors (R_P), compatible with current sense MOSFETs/IGBTs or shunt(s) may be used.

For the floating bootstrap supply D_F & C_F must be determined. D_F must support the worse case system bus voltage and handle the charging currents of C_F. Proper selection should take into consideration T_{RR} and T_{FR} per the desired operating frequency. Proper selection of C_F is a trade off between the minimum t_{ON} time of the lower rail to charge up the capacitor, the amount of charge transfer required by the load, and cost. Due to automatic refresh the capacitor is replenished every 350µs TYP (or even sooner if input commands the TOP to switch at a faster repetition rate).

The local filter capacitor (C_{DD}) should be sized sufficiently large enough to transfer the charge to C_F without causing a significant droop in V_{DD}. As a rule of thumb it should be at least 10 times larger than C_F and be located adjacent to the V_{DD} and V_{SS} pins to minimize series resistance and inductance.

Refer to Application Note AN-8829 for more details about module operation and selection of external components.

HARRIS SEMICONDUCTOR

SP601

May 1992

Half-Bridge 500V_{DC} Driver

Features

- Maximum Rating 500V
- Ability to Interface and Drive Standard and Current Sensing N-Channel Power MOSFET/IGBT Devices
- Creation and Management of a Floating Power Supply for Upper Rail Drive
- Simultaneous Conduction Lockout
- Overcurrent Protection
- Single Low Current Bias Supply Operation
- Latch Immune CMOS Logic
- Peak Drive in Excess of 0.5 Amp

Description

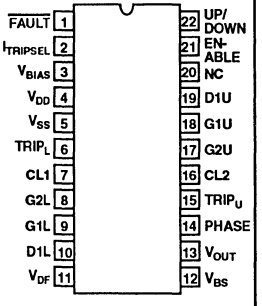
The SP601 is a smart power high voltage integrated circuit (HVIC) optimized to drive MOS gated power devices in half-bridge topologies. It provides the necessary control and management for PWM motor drive, power supply, and UPS applications.

Ordering Information

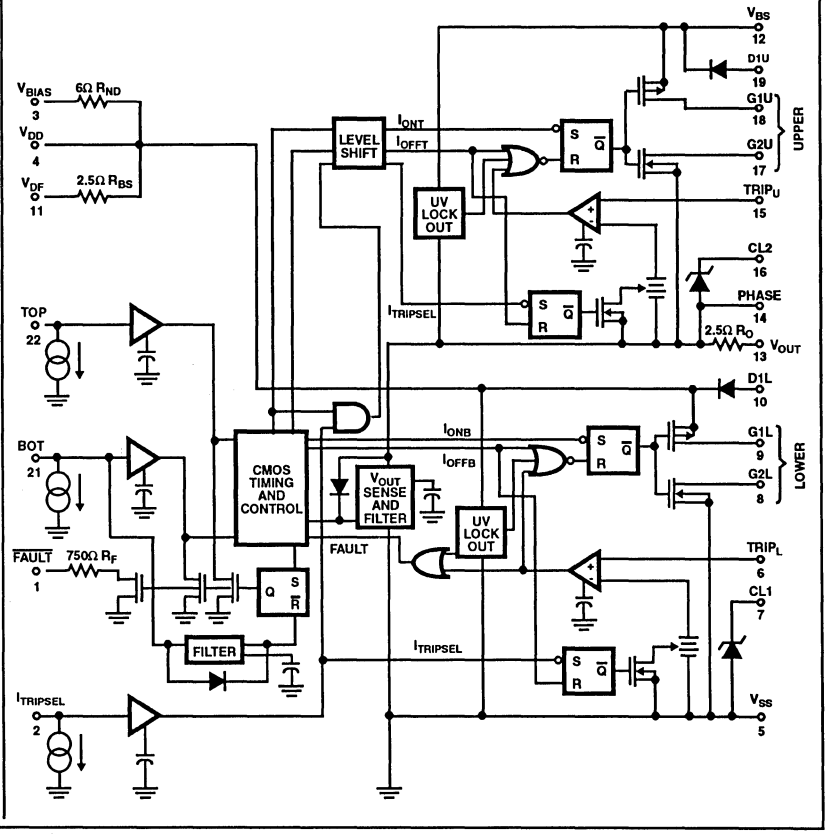
PART	TEMPERATURE	PACKAGE
SP601	-40°C to +85°C	22 Pin Plastic DIP

Pinout

22 PIN DIP
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2429.2**

Absolute Maximum Ratings

Full Temperature Range, All Voltage Referenced to V_{SS} Unless Otherwise Noted. Notes 1, 2.

Low Voltage Power Supply, V_{BIAS} (Note 1) ..... $18V_{DC}$
Floating Low Voltage Boot Strap ..... $18V_{DC}$
Power Supply to Phase, V_{BS}
Low Voltage Signal Pins
Fault, $I_{TRIP\ SEL}$, V_{DD}, $TRIP_L$, CL1, G2L .....$-0.5V_{DC}$ to V_{DD} +0.5
G1L, D1L, V_{DF}, TOP, BOT
CL2, $TRIP_U$, G1U, G2U, D1U to Phase ..... -0.5_{VDC} to V_{BS}+0.5
High Voltage Pins
Phase, V_{PHASE} ..... $500V_{DC}$
(V_{BS}, V_{OUT}, $TRIP_U$, CL2, G2U & D1U: 0V-18V Higher Than Phase)
Dynamic High Voltage Rating Phase,..... 10,000V/µs
$DV_{PHASE/dt}$

Power Dissipation and Thermal Characteristics

Thermal Resistance, Junction-to-Ambient θ_{ja}
Plastic DIP Package 75°C/W
Maximum Package Power Dissipation at T_A = +85°C, P_O
Plastic DIP Package 500mW
Operating Ambient Temperature Range, T_A .....-25°C to +85°C
Storage Temperature Range, T_S.....-40°C to +150°C

NOTES:
1. Care must be taken in the application of V_{BIAS} as not to impose high peak dissipation demands on a relatively small metallized noise dropping resistor (R_{ND}). Prolonged high peak currents may result if $+15V_{DC}$ is applied abruptly and/or if the local bypass capacitor C_{DD} is large. It is suggested that C_{DD} be ≤ 10MFD. If it is desirable to switch the $15V_{DC}$ source or if a C_{DD} is larger, additional series impedance may be required.
2. Consult factory for additional package offerings.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

. (V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Current (5V < V_{TOP}, V_{BOT}, $V_{TRIPSEL}$ < 15V)	I_{IN}	+25°C	-	20	30	µA
		-40°C to +85°C	-	30	33	µA
I_{BIAS} Quiescent Current (All Inputs Low)	I_{BIAS_L}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BIAS} Quiescent Current ($V_{OUT} \geq V_{BIAS}$, and All Inputs Low)	I_{BIAS_H}	+25°C	-	1.7	2.05	mA
		-40°C to +85°C	-	1.7	2.1	mA
I_{BS} Quiescent Current Bootstrap Supply	I_{BS}	+25°C	-	875	1000	µA
		-40°C to +85°C	-	900	1060	µA
ENABLE Threshold Level	V_{TOP}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
UP/DN Threshold Level	V_{BOT}	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Current Trip Select Threshold Level	$V_{TRIPSEL}$	+25°C	7	8	9	V
		-40°C to +85°C	6.95	8	9.1	V
Trip Lower and Upper Comparator Threshold Level - Normal ($I_{TRIPSEL}$ = V_{SS})	$V_{TRIP\ L/U_N}$	+25°C	90	105	125	mV
		-40°C to +85°C	90	105	127	mV
Trip Lower and Upper Comparator Threshold Level - Boost ($I_{TRIPSEL}$ = V_{DD}) % of Measured $V_{TRIP\ L/U_N}$	$V_{TRIP\ L/U_B}$	+25°C	110	130	150	%
		-40°C to +85°C	109	130	152	%
Under Voltage Lockout Thresholds (V_{DD} & V_{BS})	V_{LOCK}	+25°C	9	10	11.5	V
		-40°C to +85°C	9.7	10.5	11.8	V
Phase Out of Status Voltage Threshold (PHASE)	V_{OSVT}	+25°C	5	7	9	V
		-40°C to +85°C	4.7	7	9.6	V
Faultbar Impedance at I_{FBAR} = 1mA	RF	+25°C	500	760	1000	Ω
		-40°C to +85°C	450	760	1100	Ω

Electrical Specifications .(V_{BIAS} = 15V, Pulsed <300ms), Unless Otherwise Noted, All Parameters Referenced to V_{SS} Except $TRIP_U$, CL2, G1U, D1U, & V_{BS} Referenced to PHASE. DF: V_{DF} to V_{BS}, CF: V_{BS} to PHASE **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Upper/Lower Source Impedances (I_{Source} = 10mA)	$R_{SO\ L/U}$	+25°C	12	17	23	Ω
		-40°C to +85°C	7	17	29	Ω
Upper/Lower Sink Impedances (I_{SINK} = 10mA)	$R_{SI\ L/U}$	+25°C	8	12	16	Ω
		-40°C to +85°C	5	12	20	Ω
Bootstrap Supply Current Limiting Impedance	R_{BS}	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω
Noise Dropping Resistor Impedance	R_{ND}	+25°C	6	10	14	Ω
		-40°C to +85°C	5.4	10	14.6	Ω
High Voltage Leakage (500V V_{BS}, V_{OUT}, PHASE, $TRIP_U$, CL2, G1U, G2U, & D1U to V_{SS}. All other Pins at V_{SS})	I_{LK}	+25°C	-	1	3	µA
		-40°C to +85°C	-	1	3	µA
Miller Clamp Diodes; D1U and D1L (I_D = 10mA)	$V_{D1U/L}$	+25°C	1.05	1.4	1.7	V
		-40°C to +85°C	1.05	1.4	1.7	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 10mA)	$V_{CL2/1\text{-}Low}$	+25°C	6.35	6.61	6.85	V
		-40°C to +85°C	6.15	6.61	7.15	V
Noise Clamping Zeners; CL2 and CL1 (I_Z = 50mA)	$V_{CL2/1\text{-}High}$	+25°C	7.7	8.1	8.7	V
V_{OUT} Limiting Resistance	R_O	+25°C	2	3.5	5	Ω
		-40°C to +85°C	1.4	3.5	5.6	Ω

NOTE: Maximum Steady State ÷ $15V_{DC}$ Supply Current = I_{BIAS_L} + I_{BS}

Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_u$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Refresh One Shot Timer	t_{REF}	+25°C	200	350	500	µs
		-40°C to +85°C	180	350	540	µs
Delay Time of Trip I/u Voltage (I_{TRIP} sel. low) to G2U/G2L Low (50% Overdrive	$t_{OFF_{TN}}$	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Trip I Voltage (I_{TRIP} sel. low) to Faultbar Low	t_{FN}	+25°C	2	3	4	µs
		-40°C to +85°C	1.85	3	4.35	µs
Delay Time of Phase Out of Status to Faultbar Low (TOP High)	t_{OSVF}	+25°C	500	700	900	ns
		-40°C to +85°C	400	700	1050	ns
Minimum Logic Input Pulse Width: TOP & BOTTOM	t_{MINIW}	+25°C	300	430	600	ns
		-40°C to +85°C	275	430	660	ns
Minimum G1U/G1L On Time	t_{ON}	+25°C	1.6	2.3	3.1	µs
		-40°C to +85°C	1.5	2.4	3.4	µs
Minimum Pulsed Off Time, G2U/G2L	t_{OFF}	+25°C	1.3	2.0	3.4	µs
		-40°C to +85°C	1.05	2.1	3.9	µs
Turn On Delay Time of G1U (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs
Turn On Delay Time of G1L (BISTATE MODE)	t_{ON_D}	+25°C	2.5	3.2	4.5	µs
		-40°C to +85°C	2.1	3.3	5.2	µs

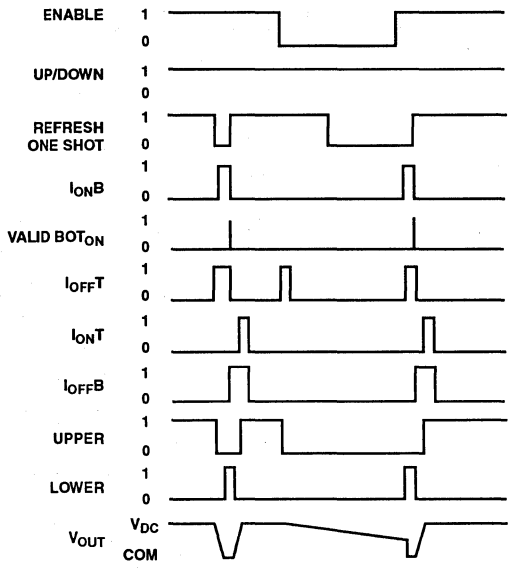
Switching Characteristics (All Referenced to V_{ss}, Except: $Trip_u$, Cl2, G1u, G2u, And D1u Referenced to PHASE. D_F: V_{DF} to V_{BS}, C_F: V_{BS} to PHASE) **(Continued)**

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
Turn On Delay Time of G1U (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn On Delay Time of G1L (TRISTATE MODE)	t_{ON_D}	+25°C	0.75	1.0	1.5	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Turn Off Delay Time of G2U and G2L	t_{OFF_D}	+25°C	0.75	1.0	1.45	µs
		-40°C to +85°C	0.60	1.1	1.75	µs
Minimum Dead Time: G1U off to G1L on, or G1L off to G1U on (BISTATE MODE)	$t_{D.T.}$	+25°C	1.5	2.5	3.5	µs
		-40°C to +85°C	1.2	2.6	4	µs
Fault Reset Delay to Clear Faultbar	$t_{R.T.}$	+25°C	3.4	4.5	6.6	µs
		-40°C to +85°C	3.15	4.8	7.4	µs
Rise Time of Upper & Lower Driver (Load = 2000pF)	$t_{R\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns
Fall Time of Upper & Lower Driver (Load = 2000pF)	$t_{F\ U/L}$	+25°C	25	50	100	ns
		-40°C to +85°C	15	50	115	ns

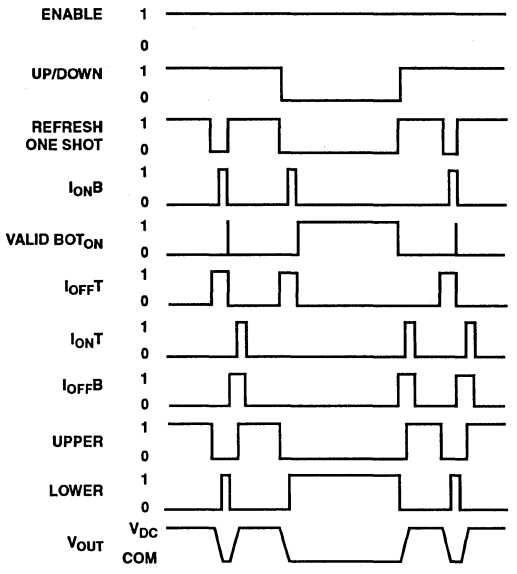
Recommended Operating Conditions and Functional Pin Description (All Voltages Referenced to V_{SS}, Unless Otherwise Noted. See Figure 1)

PARAMETER	CONDITION
Faultbar	Open Drain Fault Indicator Output
$I_{TRIP\ SELECT}$	Digital Input Command to Increase TRIP L and U Threshold by 30%
V_{BIAS}	14.5V to 16.5V with 15V nominal, ≅ 1.5mA DC BIAS Current
V_{DD}	C_{DD} to V_{SS}
V_{SS}	COMMON
Trip I	100mV Signal to Shut Off LOWER Drive and Trigger a Fault Output
CL1	Lower Noise Clamp Zener
G2L & G1L	Low Impedance Driver Designed to Drive Power MOS Transistors (LOWER)
V_{DF}	Current Limiting Charging Resistor for Bootstrap Capacitor Power Supply
V_{BS}	Bootstrap Supply, Normally a Diode Drop Below V_{DD} Voltage with Respect to the Floating PHASE Reference
V_{OUT}	Load Connection Node
Phase	Floating Reference Point for High Side Control Circuitry: V_{BS}, $TRIP_U$, CL2, G1U, G2U & D1U
$Trip_U$	100mV Signal, Referenced to PHASE, to Shut Off UPPER Drive
CL2	Upper Noise Clamp Zener
G2U & G1U	Low Impedance Driver Designed to Drive Power MOS Transistors (UPPER)
ENABLE	Digital Input to ENABLE the UP/DN Command to Turn on Top/Bottom Devices
UP/DN	Digital Input to Top/Bottom Device (If ENABLE is High)
D1U	Miller Clamp UPPER to V_{BS}
D1L	Miller Clamp LOWER to V_{DD}

Timing Diagram



TRISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER
NOTE: BOT switching not relevant.



BISTATE MODE SLOWER THAN REFRESH ONE SHOT TIMER

Typical Circuit Configuration

TRUTH TABLE
Applicable to Typical Circuit Configuration (Figure 1)

INPUTS						OUTPUTS		
UP/DN	ENABLE	$TRIP_L$	$TRIP_U$	PHASE	V_{BIAS}	UPPER	LOWER	FAULT BAR
0	0	0	X	X	1	0	0	1
1	1	0	0	1	1	1	0	1
1	1	0	1	1	1	0	0	0
1	1	0	X	0	1	0	0	0
X	X	1	X	X	1	0	0	0
0	1	0	X	X	1	0	1	1
1	0	0	X	X	1	0	0	1
X	X	X	X	X	0	0	0	0

NOTE: 0 = False, 1 = True, X = Don't Care

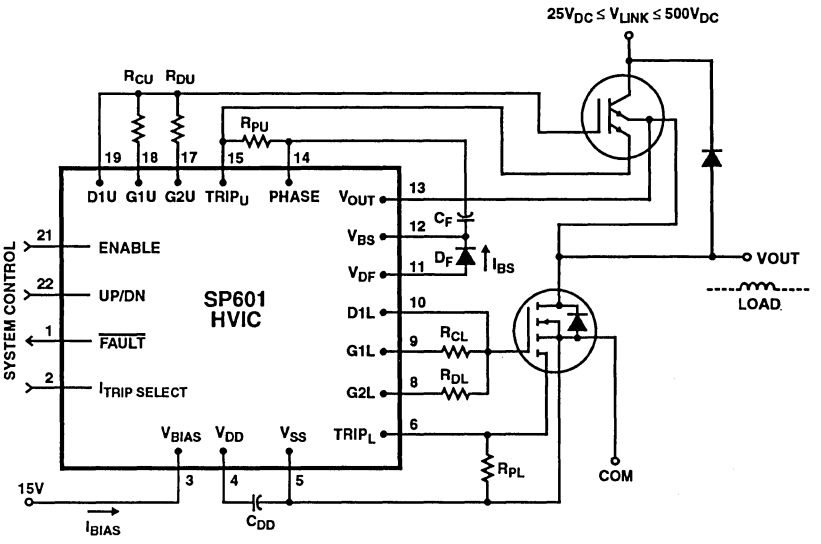


FIGURE 1. TYPICAL CIRCUIT CONFIGURATION

LEGEND		
Application Specific	R_{CU}	Upper Gate Charging Resistor
Application Specific	R_{DU}	Upper Gate Discharge Resistor
Application Specific	R_{PU}	Upper Current Pilot Resistor
Application Specific	R_{CL}	Lower Gate Charging Resistor
Application Specific	R_{DL}	Lower Gate Discharging Resistor
Application Specific	R_{PL}	Lower Current Pilot Resistor
3µF @ ≥ 15DC	C_{DD}	Local LV Filter Capacitor
0.22µF Ceramic X7R @ ≥ $15V_{DC}$	C_F	Flying Capacitor for Bootstrap Supply
Harris P/N A114M or Equiv PRV ≥ V_{LINK}	D_F	Flying Diode for Bootstrap Supply

Refer to 'Additional Product Offerings' for information concerning power output devices.

Functional Description

The SP601 provides a flexible, digitally controlled power function which is intended to be used as PWM drivers of n-channel MOSFETs and/or IGBTs for up to 240VAC line rectified totem-pole applications. The CMOS driveable inputs are filtered and captured by the control logic to determine the output state. The logic includes fixed timing to prohibit simultaneous conduction of the external power switches and, thru the V_{OUT} sense detector, verifies the output voltage state is in agreement with the controlled inputs. The > 11VDC floating power supply required to drive the upper rail external power device is created and managed by the HVIC through Cf and Df. This capacitor is refreshed from the V_{DD} supply each time V_{OUT} goes low. If the upper channel is commanded on for a long period of time, the bootstrap capacitor Cf is automatically refreshed by bringing V_{OUT} low. This is accomplished by turning off the upper rail MOSFET/IGBT, momentarily turning on the lower rail output device, followed by returning control back to the upper switch. Otherwise, Cf would gradually deplete its charge allowing the upper switch to come out of saturation. The upper and lower gate drivers allow for controlled charge and discharge rates as well as facilitate the use of nearly lossless current sensing power MOS devices. The over current trip level can be boosted 30% on a pulse by pulse basis by logic level '1' applied to $I_{TRIP\ SELECT}$. A $\overline{FAULT}$ output signal is generated when any of the following occurs:

V bias is low
Over current is detected
V phase doesn't agree with the input signal

Reset of $\overline{FAULT}$ is provided by externally removing power or by holding the ENABLE input low for the required reset time (trt_{MAX}).

Each application can be individually optimized by the selection of external components tailored to ensure proper overall system operation including:

Determining the ratings and sizing of MOSFETs and IGBTs, mixed or matched, as well as flyback diodes (FBD).

The selection of separate gate charge (R_C) & discharge (R_D) impedance chosen per the load capacitance, frequency of operation, and D_I/D_T dependent recovery characteristics of the associated FBDs. R_D should also be sized to prevent simultaneous bridge conduction by ensuring gate discharge in the allotted turn off pulse width ($t_{OFF\ MIN}$).

The selection of over current detection resistors (R_P), compatible with current sense MOSFETs/IGBTs or shunt(s) may be used.

For the floating bootstrap supply D_F & C_F must be determined. D_F must support the worse case system bus voltage and handle the charging currents of C_F. Proper selection should take into consideration T_{RR} and T_{FR} per the desired operating frequency. Proper selection of C_F is a trade off between the minimum t_{ON} time of the lower rail to charge up the capacitor, the amount of charge transfer required by the load, and cost. Due to automatic refresh the capacitor is replenished every 350µs TYP (or even sooner if the UP/DN input switches at a faster repetition rate).

The local filter capacitor (C_{DD}) should be sized sufficiently large enough to transfer the charge to C_F without causing a significant droop in V_{DD}. As a rule of thumb it should be at least 10 times larger than C_F and be located adjacent to the V_{DD} and V_{SS} pins to minimize series resistance and inductance.

Refer to Application Note AN-8829 for more details about module operation and selection of external components.

INTELLIGENT POWER ICs

5

AC TO DC CONVERTERS

AC to DC Converter Selection Guide

DEVICE	DESCRIPTION	AC INPUT VOLTAGE AT 50-60Hz & 400Hz (VAC)	MAX DC SUPPLY VOLTS (V)	MAX INPUT CURRENT (mA)	SENSOR RANGE (RX) (KΩ)	CONTROL CURRENT TO THYRISTOR GATE (mA)
CA3059	Zero Voltage Switch	24V 120V 208/230V 277V	14	1	2 to 100	Up to 124 with Internal Supply; Up to 240 with One External Supply
CA3079			10	2	2 to 50	

NOTE:

1. Electrical Characteristics at T_A = +25°C, 14 Lead Dual-In-Line (E) Package Operating Temperature Range (T_A): -55°C to +125°C.

HARRIS SEMICONDUCTOR

CA3059
CA3079

Zero-Voltage Switches for 50-60Hz and 400Hz Thyristor Control Applications

May 1992

Features

- Relay Control
- Valve Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator with Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control
- Heater Control
- Lamp Control

Type Features

	CA3059	CA3079
• 24V, 120V, 208/230V, 277V at 50/60 .... or 400Hz Operation	X	X
• Differential Input	X	X
• Low Balance Input Current (Max) - μA...	1	2
• Built-In Protection Circuit for ..... Opened or Shorted Sensor (Term 14)	X	X
• Sensor Range (Rx) - kΩ.....	2 - 100	2 - 50
• DC Mode (Term 12)	X	
• External Trigger (Term 6).....	X	
• External Inhibit (Term 1)	X	
• DC Supply Volts (Max)	14	10
• Operating Temperature Range (°C) ...	-55 to +125	

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3059	-55°C to +125°C	14 Lead Plastic DIP
CA3079	-55°C to +125°C	14 Lead Plastic DIP
CA3059H	+25°C	Dice
CA3079H	+25°C	Dice

Description

The CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V, and 277V at 50-60Hz and 400Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see the Functional Block Diagram) as follows:

1. Limiter-Power Supply - Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit - Provides high-current pulses to the gate of the power controlling thyristor.

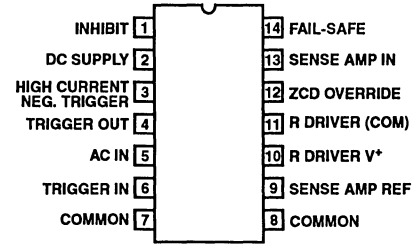
In addition, the CA3059 provides the following important auxiliary functions (see the Functional Block Diagram).

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

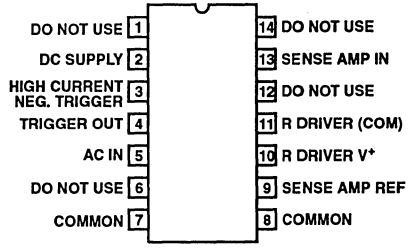
The CA3059 and CA3079 are supplied in 14 lead dual-in-line plastic packages. They are also available in chip form (H suffix).

Pinouts

CA3059
TOP VIEW



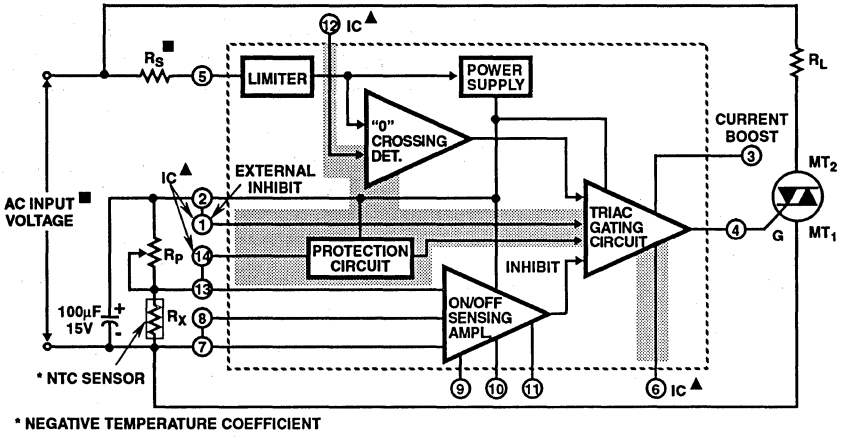
CA3079
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **490.2**

Functional Block Diagram



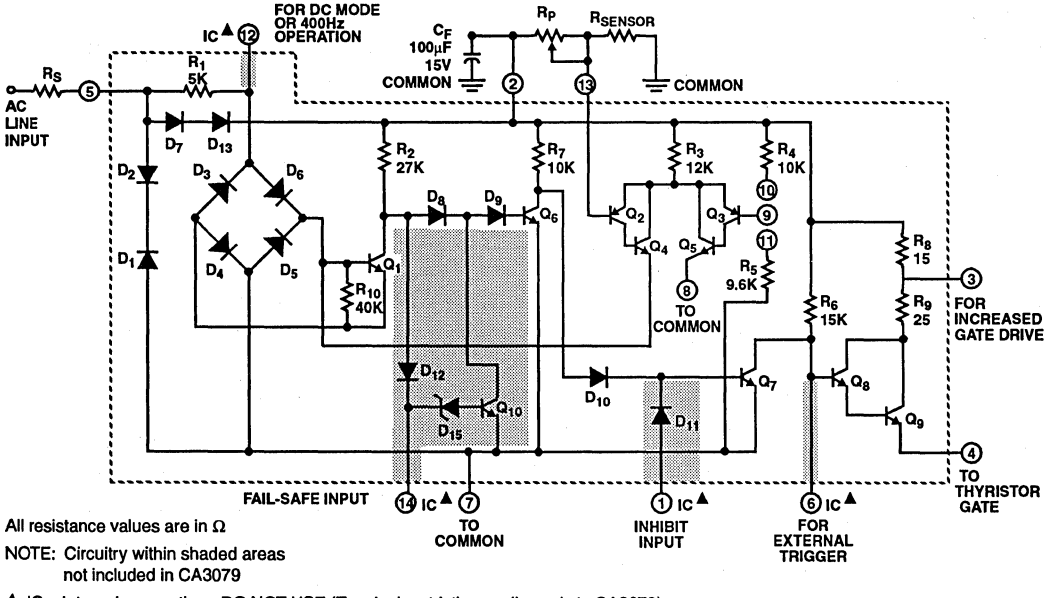
* NEGATIVE TEMPERATURE COEFFICIENT

AC INPUT VOLTAGE (50/60 OR 400Hz) V AC	INPUT SERIES RESISTOR (R_S) kΩ	DISSIPATION RATING FOR R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE: Circuitry within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)



All resistance values are in Ω

NOTE: Circuitry within shaded areas not included in CA3079

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)

FIGURE 1. SCHEMATIC DIAGRAM OF CA3059 AND CA3079

Absolute Maximum Ratings T_A = +25°C

DC Supply Voltage (Between Terminals 2 & 7)
- CA3059 ..... 14V
- CA3079 ..... 10V

DC Supply Voltage (Between Terminals 2 & 8)
- CA3059 ..... 14V
- CA3079 ..... 10V

Peak Supply Current (Terminals 5 & 7) ..... ±50mA
Output Pulse Current (Terminal 4) 150mA

Power Dissipations
- Up to T_A = +55°C CA3059, CA3079 ..... 700mW
- Above T_A = +55°C CA3059, CA3079 ..... Derate Linearly 6.67mW/°C

Ambient Temperature
- Operating ..... -55°C to +125°C
- Storage ..... -65°C to +150°C

Lead Temperature (During Soldering)
- At distance $^1/_{16}$" ± $^1/_{32}$" (1.59 ± 0.79) from case for 10 seconds max ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at 120V_{RMS}, 50-60Hz (AC Line Voltage) (Note 1)

PARAMETERS		SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DC SUPPLY VOLTAGE (Figure 2a, 2b, 2c)							
Inhibit Mode	At 50/60Hz	V_S	R_S = 8kΩ, I_L = 0	6.1	6.5	7	V
	At 400Hz		R_S = 10kΩ, I_L = 0	-	6.8	-	V
	At 50/60Hz		R_S = 5kΩ, I_L = 0	-	6.4	-	V
Pulse Mode	At 50/60Hz	V_S	R_S = 8kΩ, I_L = 0	6	6.4	7	V
	At 400Hz		R_S = 10kΩ, I_L = 0	-	6.7	-	V
	At 50/60Hz		R_S = 5kΩ, I_L = 0	-	6.3	-	V
GATE TRIGGER CURRENT (Figures 3, 4(a))		I_{GT}(4)	Terminals 3 and 2 connected, V_{GT} = 1V	-	105	-	mA
PEAK OUTPUT CURRENT (PULSED) (Figures 4, 5)							
With Internal Power Supply Figure 4a, 4b		I_{OM}(4)	Terminal 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	-	mA
			Terminals 3 and 2 connected, Gate Trigger Voltage (V_{GT}) = 0	90	124	-	mA
With External Power Supply Figure 5a, 5b, 5c		I_{OM}(4)	Terminal 3 open, V+ = 12V, V_{GT} = 0	-	170	-	mA
			Terminals 3 and 2 connected, V+ = 12V, V_{GT} = 0		240	-	mA
INHIBIT INPUT RATIO (Figure 6)		V_9/V_2	Voltage Ratio of Terminals 9 to 2	0.465	0.485	0.520	-
TOTAL GATE PULSE DURATION (Note 2) (Figure 7a, 7b, 7c, 7d)							
For Positive dv/dt	50-60Hz	t_P	C_{EXT} = 0	70	100	140	µs
	400Hz		C_{EXT} = 0, R_{EXT} = ∞	-	12	-	µs
For Negative dv/dt	50-60Hz	t_N	C_{EXT} = 0	70	100	140	µs
	400Hz		C_{EXT} = 0, R_{EXT} = ∞	-	10	-	µs
PULSE DURATION AFTER ZERO CROSSING (50-60Hz) (Figure 7a)							
For Positive dv/dt		t_{P1}	C_{EXT} = 0, R_{EXT} = ∞	-	50	-	µs
For Negative dv/dt		t_{N1}		-	60	-	µs
OUTPUT LEAKAGE CURRENT (Figure 8)							
Inhibit Mode		I_4		-	0.001	10	µA
INPUT BIAS CURRENT (Figure 9)							
CA3059		I_I		-	220	1000	nA
CA3079				-	220	2000	nA
COMMON-MODE INPUT VOLTAGE RANGE		V_{CMR}	Terminals 9 and 13 connected	-	1.5 to 5	-	V

Electrical Specifications T_A = +25°C, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at $120V_{RMS}$, 50-60Hz (AC Line Voltage) (Note 1) **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
SENSITIVITY (Note 3) (Figures 4(a), 11)						
Pulse Mode	ΔV_{13}	Terminal 12 open	-	6	-	mV

NOTES:

1. The values given in the Electrical Characteristics Chart at 120V also apply for operation at input voltages of 208/230V, and 277V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in the Functional Block Diagram, for the specified input voltage.
2. Pulse Duration in 50Hz applications is approximately 15% longer than shown in Figure 7(b).
3. Required voltage change at Terminal 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

Maximum Voltage Ratings T_A = +25°C

	MAXIMUM VOLTAGE RATINGS T_A = +25°C														MAXIMUM CURRENT RATINGS	
TERM. NO.	NOTE 3 1	2	3	4	NOTE 1 5	NOTE 3 6	7	8	9	10	11	NOTE 3 12	13	NOTES 2,3 14	I_{IN} mA	I_{OUT} mA
1 Note 3		*	*	*	*	15 0	10 -2	*	*	*	*	*	*	*	10	0.1
2			0 -15	0 -15	2 -14	0 -14	0** -14	0** -14	0 -14	0 -14	0 -14	*	0 -14	0 -14	150	10
3				0 -15	*	*	*	*	*	*	*	*	*	*	*	*
4					*	2 -10	*	*	*	*	*	*	*	*	0.1	150
5 Note 1						*	7 -7	*	*	*	*	*	*	*	50	10
6 Note 3							14 0	*	*	*	*	*	*	*	*	*
7								*	14 0	*	20 0	2.5 -2.5	14 0	6 -6	*	*
8									10 0	*	*	*	*	*	0.1	2
9										*	*	*	*	*	*	*
10											*	*	*	*	*	*
11												*	*	*	*	*
12 Note 3													*	*	50	50
13														*	*	*
14 Note 3															2	2

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to -10 volts.

NOTES:

1. Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50mA.
2. Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2mA.
3. For the CA3079 indicated terminal is internally connected and, therefore, should not be used.

* Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.

** For CA3079 (0V to -10V).

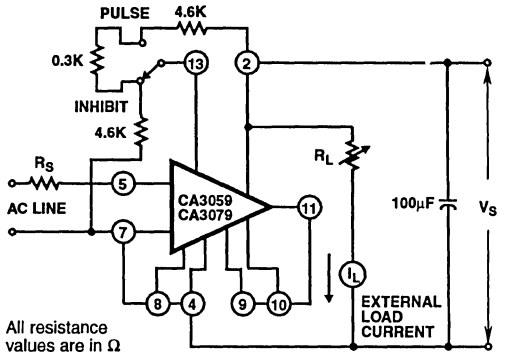


FIGURE 2(a). DC SUPPLY VOLTAGE TEST CIRCUIT FOR CA3059 AND CA3079

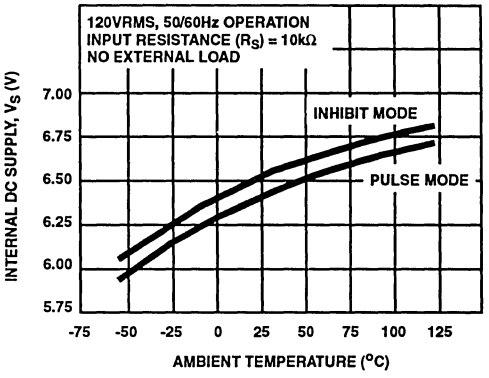


FIGURE 2(b). DC SUPPLY VOLTAGE vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

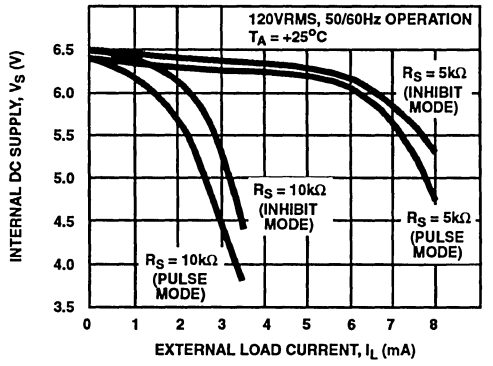


FIGURE 2(c). DC SUPPLY VOLTAGE vs. EXTERNAL LOAD CURRENT FOR CA3059 AND CA3079

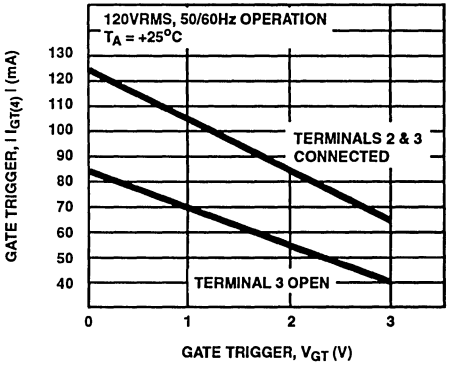


FIGURE 3. GATE TRIGGER CURRENT vs. GATE TRIGGER VOLTAGE FOR CA3059 AND CA3079

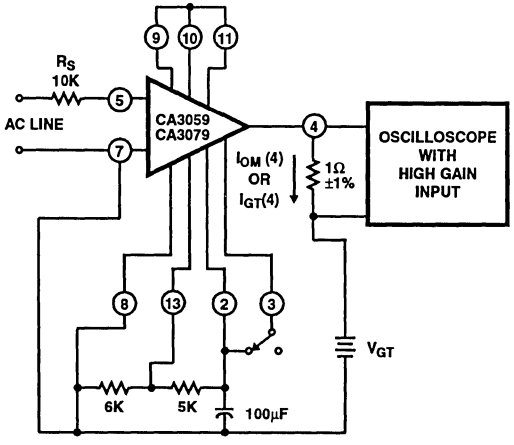


FIGURE 4(a). PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059 AND CA3079

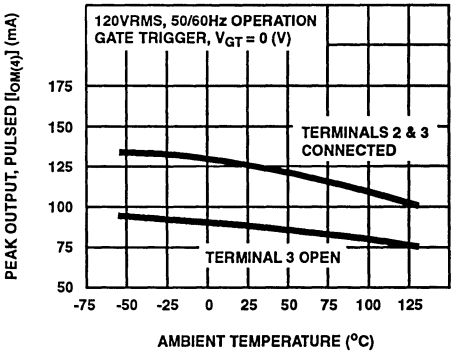


FIGURE 4(b). PEAK OUTPUT CURRENT (PULSED) vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

FIGURE

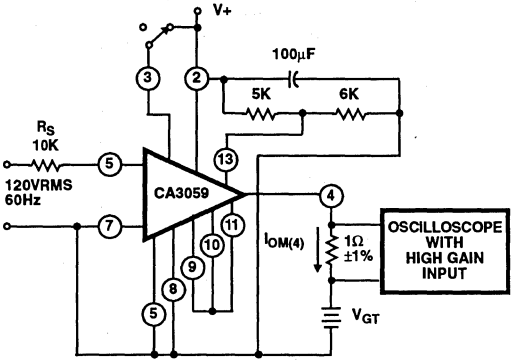


FIGURE 5(a). PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059

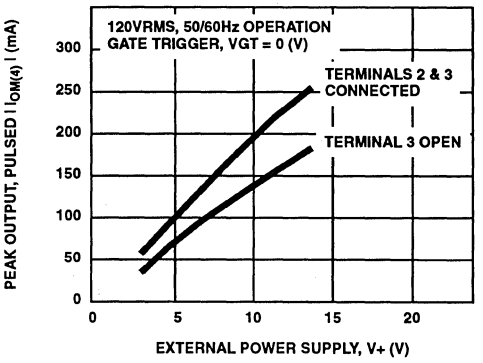


FIGURE 5(b). PEAK OUTPUT CURRENT (PULSED vs. EXTERNAL POWER SUPPLY VOLTAGE FOR CA3059

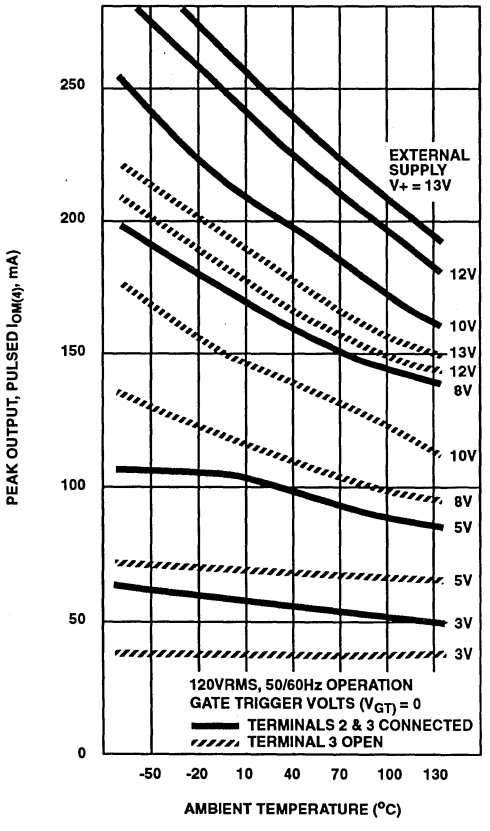


FIGURE 5(c). PEAK OUTPUT CURRENT (PULSED) vs. AMBIENT TEMPERATURE FOR CA3059

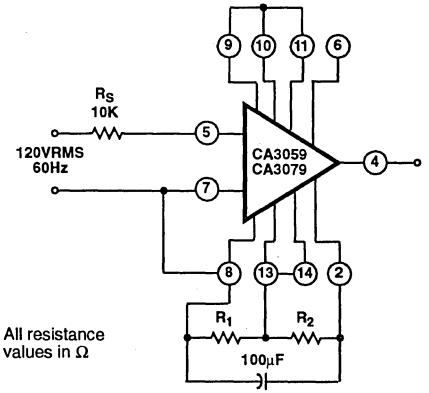


FIGURE 6(a). INPUT INHIBIT VOLTAGE RATIO TEST CIRCUIT FOR CA3059 AND CA3079

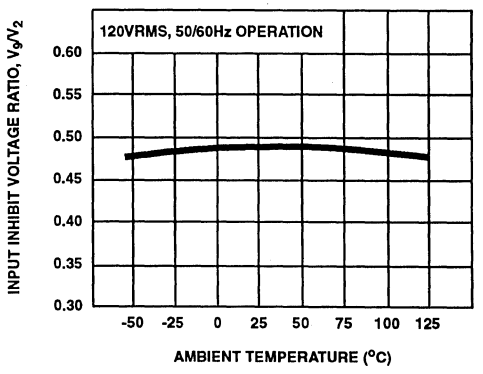
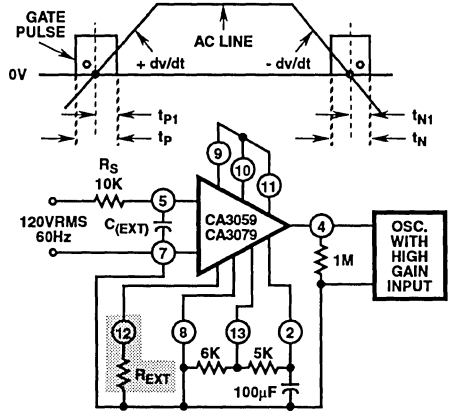


FIGURE 6(b). INPUT INHIBIT VOLTAGE RATIO vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079



NOTE: Circuitry within shaded area not included in CA3079. All resistance values are in Ω

FIGURE 7(a). GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM FOR CA3059 AND CA3079

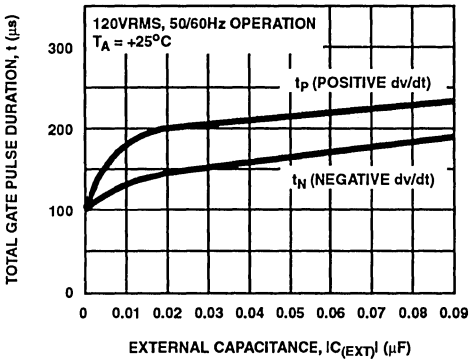


FIGURE 7(b). TOTAL GATE PULSE DURATION vs. EXTERNAL CAPACITANCE FOR CA3059 AND CA3079

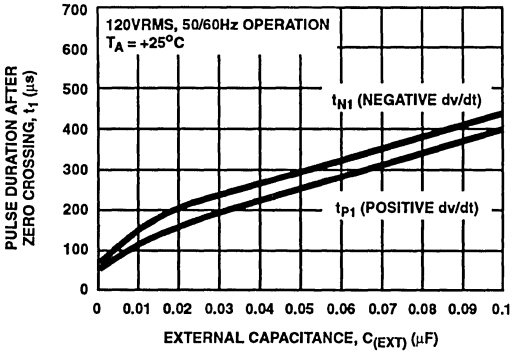


FIGURE 7(c). PULSE DURATION AFTER ZERO CROSSING vs. EXTERNAL CAPACITANCE FOR CA3059 AND CA3079

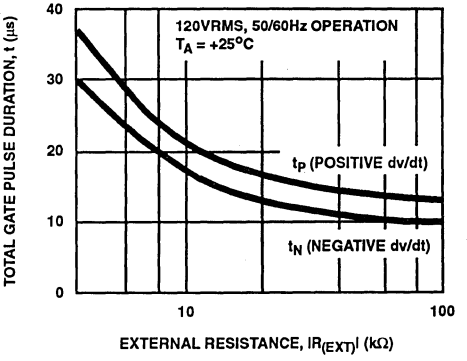


FIGURE 7(d). TOTAL GATE PULSE DURATION vs. EXTERNAL RESISTANCE FOR CA3059

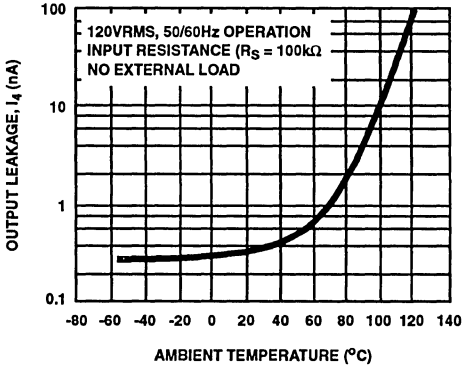


FIGURE 8. OUTPUT LEAKAGE CURRENT (INHIBIT MODE) vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

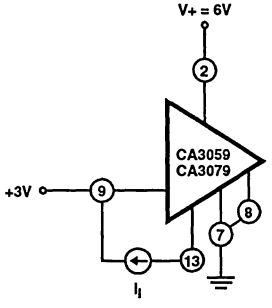


FIGURE 9. INPUT BIAS CURRENT TEST CIRCUIT FOR CA3059 AND CA3079

5 AC TO DC CONVERTERS

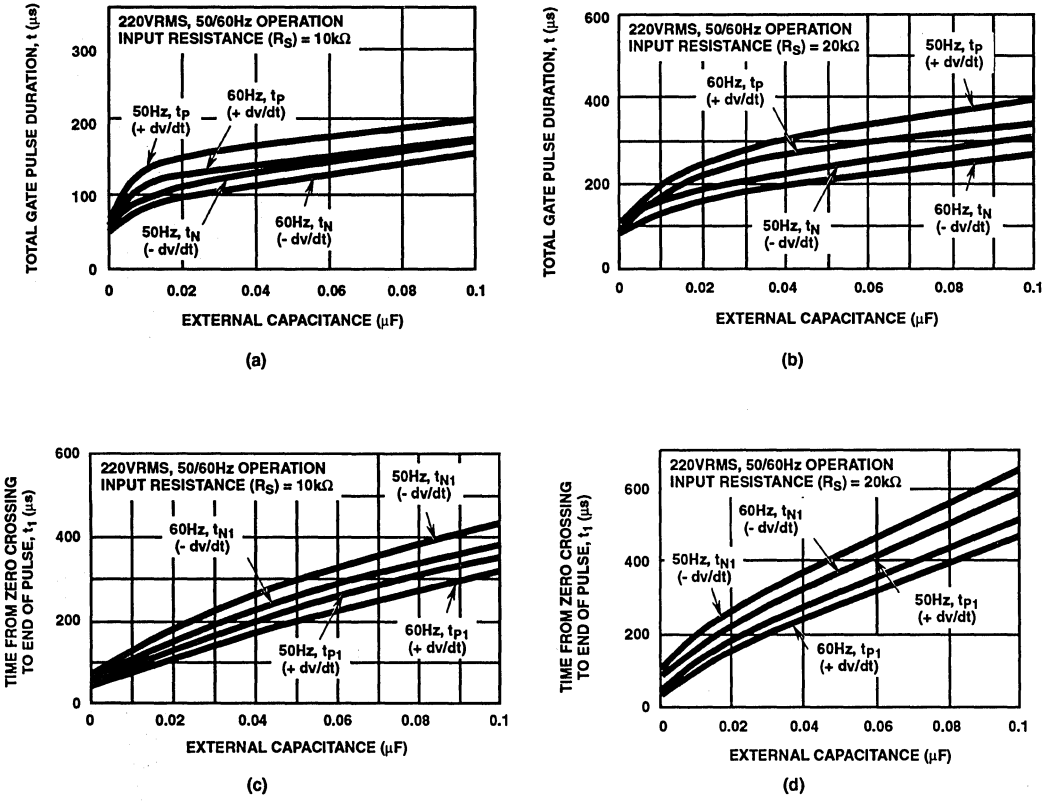


FIGURE 10. RELATIVE PULSE WIDTH AND LOCATION OF ZERO CROSSING FOR 220 VOLT OPERATION FOR CA3059 AND CA3079

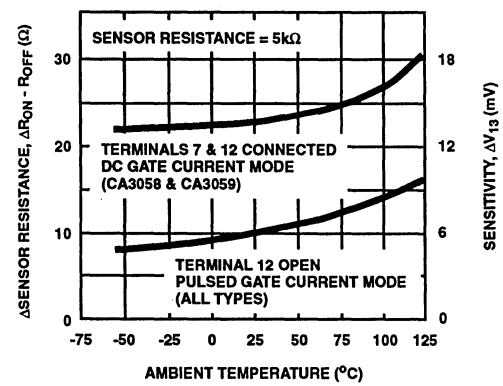


FIGURE 11. SENSITIVITY vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

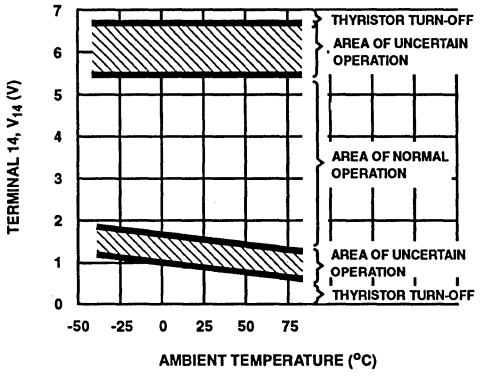
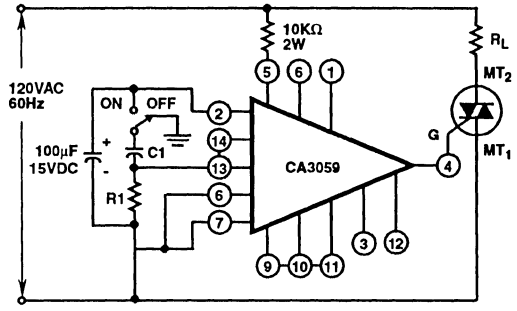


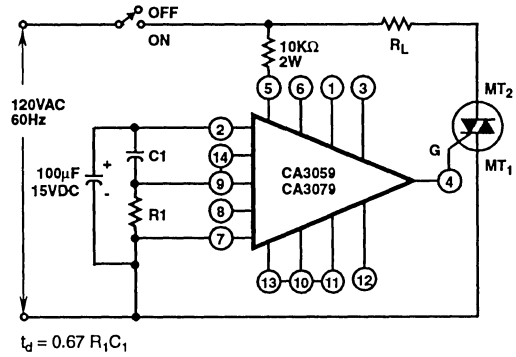
FIGURE 12. OPERATING REGIONS FOR BUILT-IN PROTECTION CIRCUIT FOR CA3059



$t_{ON} = 0.67\ R_1C_1$

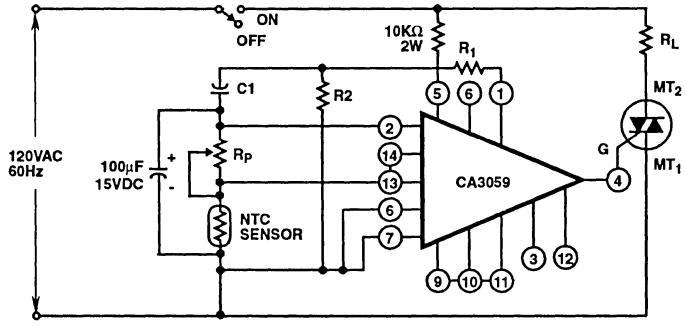
R_1(max. value allowable) = 1mΩ

FIGURE 13. LINE-OPERATED ONE-SHOT TIMER



$t_d = 0.67\ R_1C_1$

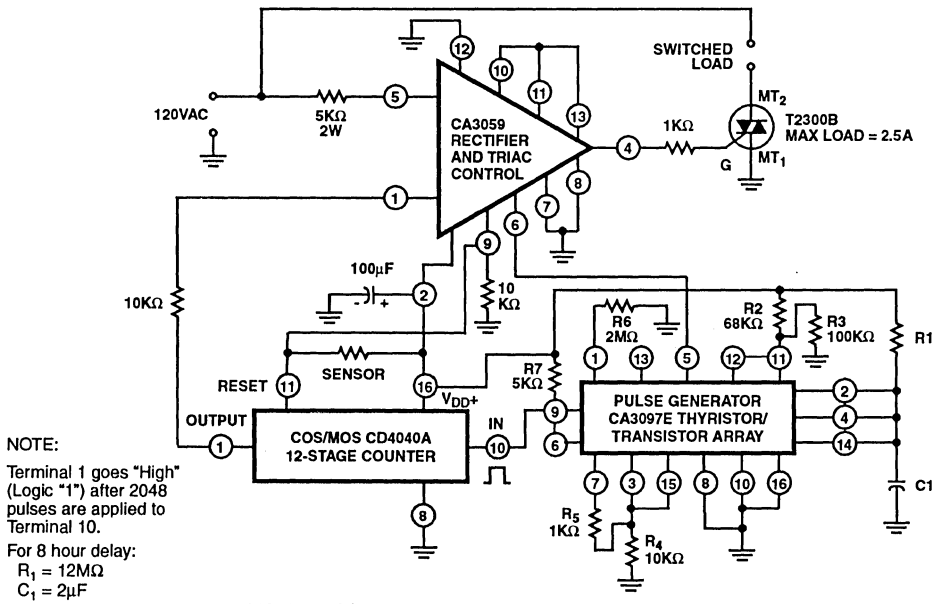
FIGURE 14. LINE-OPERATED THYRISTOR CONTROL TIME DELAY TURN-ON CIRCUIT



$t_d = R_TC_1$

$R_T = \dfrac{R_1R_2}{R_1 + R_2}$

FIGURE 15. ON/OFF TEMPERATURE CONTROL CIRCUIT WITH DELAYED TURN-ON



NOTE:

Terminal 1 goes "High" (Logic "1") after 2048 pulses are applied to Terminal 10.

For 8 hour delay:

$R_1 = 12M\Omega$

$C_1 = 2\mu F$

FIGURE 16(a). LINE-OPERATED IC TIMER FOR LONG TIME PERIODS

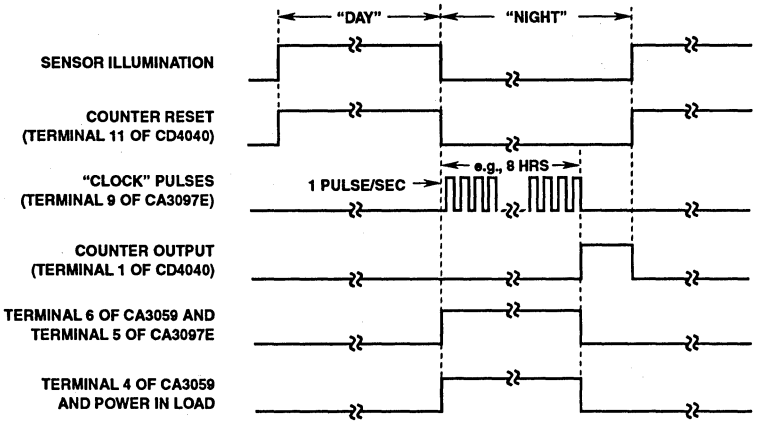


FIGURE 16(b). TIMING DIAGRAM FOR FIGURE 16(a)

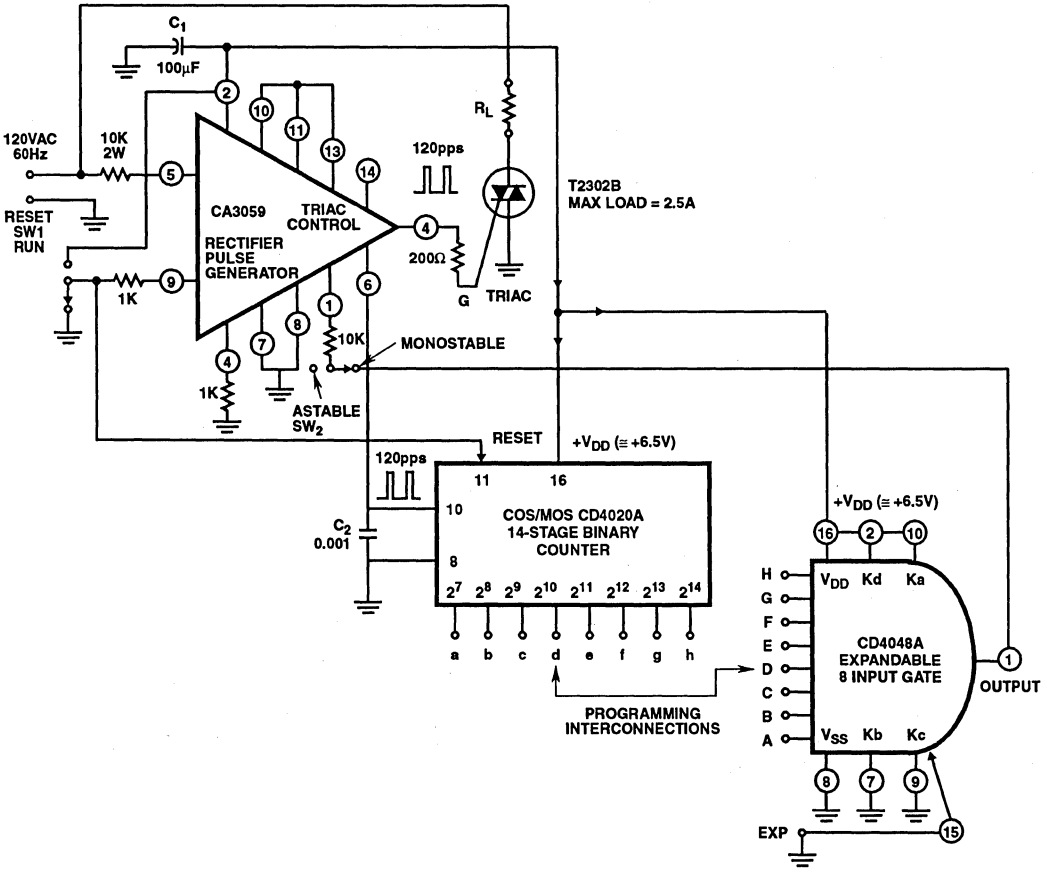


FIGURE 17(a). PROGRAMMABLE ULTRA-ACCURATE LINE-OPERATED TIMER.

TIME PERIODS (t = 0.5333 s)								
1t	2t	4t	8t	16t	32t	64t	128t	t_O
CD4020A TERMINALS								
a	b	c	d	e	f	g	h	
CD4048A TERMINALS								
A	B	C	D	E	F	G	H	
C	NC	NC	NC	NC	NC	NC	NC	1t
NC	C	NC	NC	NC	NC	NC	NC	2t
C	C	NC	NC	NC	NC	NC	NC	3t
NC	NC	C	NC	NC	NC	NC	NC	4t
C	NC	C	NC	NC	NC	NC	NC	5t
NC	C	C	NC	NC	NC	NC	NC	6t
C	C	C	NC	NC	NC	NC	NC	7t
NC	NC	NC	C	NC	NC	NC	NC	8t
C	NC	NC	C	NC	NC	NC	NC	9t
NC	C	NC	C	NC	NC	NC	NC	10t
C	C	NC	C	NC	NC	NC	NC	11t
NC	NC	C	C	NC	NC	NC	NC	12t
C	NC	C	C	NC	NC	NC	NC	13t
NC	C	C	C	NC	NC	NC	NC	14t
C	C	C	C	NC	NC	NC	NC	15t
C	C	C	C	NC	C	C	NC	111t
NC	NC	NC	NC	C	C	C	NC	112t
C	NC	NC	NC	C	C	C	NC	113t
C	C	C	C	C	C	C	C	255t

NOTES:

1. t_O = Total time delay = $n_1 t + n_2 t + \ldots n_n t$.
2. C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.
3. NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to $+V_{DD}$ bus.

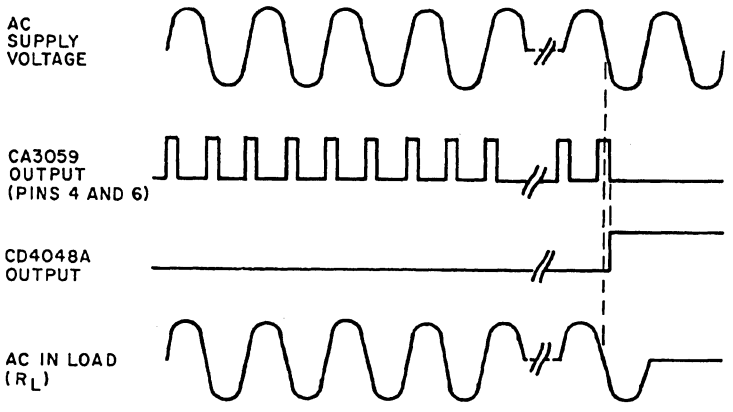


FIGURE 17(b). "PROGRAMMING" TABLE FOR FIGURE 17(a).

Operating Considerations

Power Supply Considerations for CA3059 and CA3079

The CA3059 and CA3079 are intended for operation as self-powered circuits with the power supplied from and AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figures 2(b) and 2(c).

Power Supply Considerations for CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Figure 4 for the peak output current characteristics.) When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Figure 5(a).

Operation of Built-In Protection for the CA3059

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in the Functional Block Diagram. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2mA with a 5kΩ dropping resistor.
2. Set the value of R_P and sensor resistance (R_X) between 2kΩ and 100kΩ.
3. The ratio of R_X to R_P typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

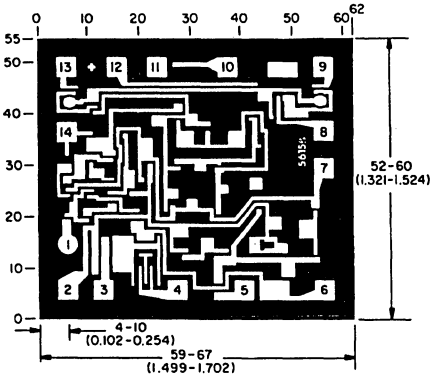
If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Figure 12.

External Inhibit Function for the CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2V at 10μA will remove drive from the thyristor. This required level is compatible with DTL or T^2L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is par of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

DIMENSIONS AND PAD LAYOUT FOR CA3059H AND CA3079H

INTELLIGENT POWER ICs 6

FULL BRIDGES

Full Bridge Selection Guide

PART NUMBER	DESCRIPTION	PEAK OUTPUT CURRENT EACH DRIVE	SUPPLY VOLTAGE	NO LOAD MAXIMUM SUPPLY CURRENT
CA3275	Dual H-Drive	±150mA	8V to 16V	20mA
HIP4010	Power H-Switch	0.5A	+4V to 15V or ±2V to ±7.5V	15mA
HIP4011	3 Phase Motor Controller	5A	10.4V to 13.2V	15mA
HIP4080	H-Bridge Drive	2A	8V to 16V	20mA

HARRIS SEMICONDUCTOR

CA3275

May 1992

Dual-H Driver

Features

- Dual-H Drivers on One IC
- ± 150mA Maximum Current
- Logic Controlled Switching
- Direction Control
- PWM I_{OUT} Control
- 18V Over-Voltage Protection
- 300mA Short-Circuit Protection
- Nominal 10V to 16V Operation
- Internal Voltage Regulation With Bandgap Reference

Applications

- Dual H-Switch For Air Core Gauge Instrumentation
- µP Controlled Sensor Data Displays
- Speedometer Displays
- Tachometer Displays
- Stepper Motors
- Slave Position Indicators

Description

The CA3275 Dual-H Driver is intended for general-purpose applications requiring Dual-H drive or switching, including direction and pulse-width modulation for position control. While all features of the IC may not be utilized or required, they would normally be used in instrumentation systems with quadrature coils, such as air-core gauges, where the coils would be driven at frequencies ranging from 200Hz to 400Hz. The coils are wrapped at 90° angles for independent direction control. Coils wound in this physical configuration are controlled by pulse width modulation, where each coil drive is a function of the sine or cosine versus degrees of movement. The direction control is used to change the direction of the current in the H-Driver coil.

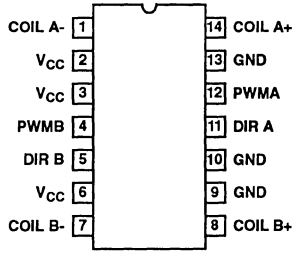
The switch rate capability of the IC is typically 30kHz regardless of the inductive load. Over-current limiting is used to limit short circuit current. Over-voltage protection (in the range of 18V to 40V) causes the device to shut down the output current drive. Thermal shutdown limits power dissipation on the chip. The CA3275 is supplied in a 14 lead dual-in-line plastic package.

Ordering Information

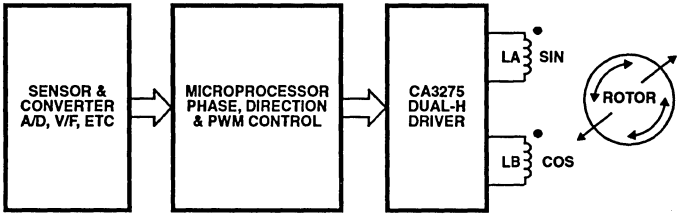
PART	TEMPERATURE	PACKAGE
CA3275E	-40°C to +85°C	14 Lead Plastic DIP

Pinout

14 LEAD DUAL-IN-LINE PLASTIC PACKAGE (E SUFFIX)
TOP VIEW



Block Diagram



6 FULL BRIDGE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2159.1**

Absolute Information (T_C = +25°C) Unless Otherwise Specified

Operating V_{CC} 16V
Transient V_{CC}, 30 Seconds Maximum 24V
Peak V_{CC}, 0.4 Seconds Maximum 40V
Maximum Continuous Output Current, Each Drive ..... ±100mA
Maximum PWM Output Switching Current, Each Drive ..... ±150mA
Power Dissipation, P_D
Up to +70°C 750mW
Above +70°C ..... Derate Linearly at 11.1mW/°C

Ambient Temperature Range
Operating ..... -40°C to +85°C
Storage ..... -55°C to +150°C
Lead Temperature (During Soldering) ..... +265°C
At distance 1/16 ± 1/32" (1.59 ± 0.79mm) from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications At T_A = +25°C, V_{CC} = 16V Unless Otherwise Specified

PARAMETERS	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage Range	V_{CC}	8	-	16	V
Supply Current (Note 1)	I_{CC}	-	8	20	mA
INPUT LEVELS					
Logic Input, Low Voltage	V_{IL}	-	-	0.8	V
Logic Input, High Voltage	V_{IH}	3.5	-	-	V
Logic Input, Low Current, V_{IL} = 0V	I_{IL}	-10	-	-	µA
Logic Input, High Current, V_{IH} = 5V	I_{IH}	-	-	10	µA
OUTPUT: RLA = RLB = 138Ω					
Maximum Source Saturated Voltage	V_{SAT} - High	-	1.2	1.75	V
Maximum Sink Saturated Voltage	V_{SAT} - Low	-	0.25	0.5	V
Differential V_{SAT} Voltage, Both Outputs Saturated	Diff - V_{SAT}	-	10	100	mV

Switching Specifications

PARAMETERS	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
SOURCE CURRENT (See Figure 3)					
Turn-Off Delay	T_{SC-OFF}	-	-	2	µs
Fall Time	T_{SC-F}	-	-	2.2	µs
Turn-On Time	T_{SC-ON}	-	-	1	µs
Rise Time	T_{SC-R}	-	-	0.4	µs
SINK CURRENT (See Figure 4)					
Turn-Off Delay	$T_{SCK-OFF}$	-	-	1.6	µs
Fall Time	T_{SCK-F}	-	-	0.4	µs
Turn-On Time	T_{SCK-ON}	-	-	0.6	µs
Rise Time	T_{SCK-R}	-	-	0.2	µs

NOTE:
1. No load, PWMA = PWMB = 5V, DIR A = DIR B = 0V

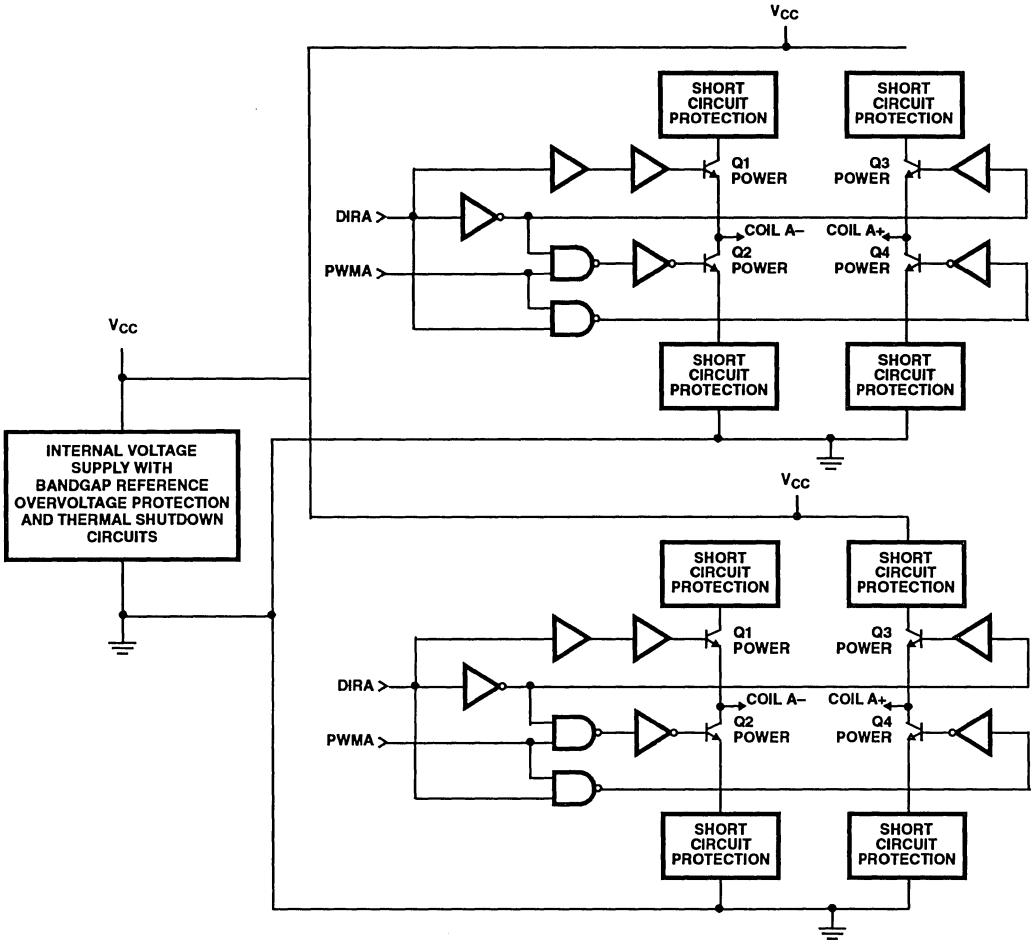


FIGURE 1. CA3275 DUAL-H DRIVER SCHEMATIC

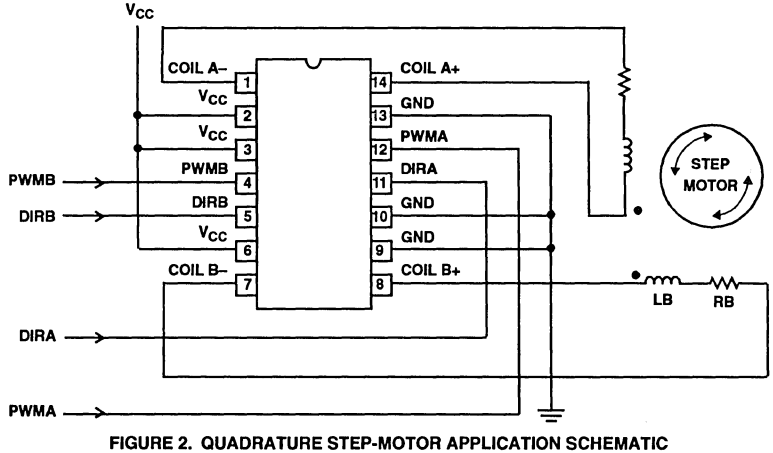
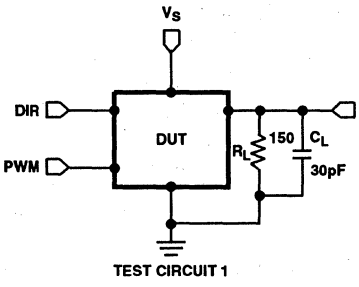


FIGURE 2. QUADRATURE STEP-MOTOR APPLICATION SCHEMATIC



TEST CONDITIONS: PWM = 0V, V_S = 16V
DIR PULSE PARAMETERS:
F = 1kHz, W = 100µs, TR = TF = 1µs, AMPL = 4V

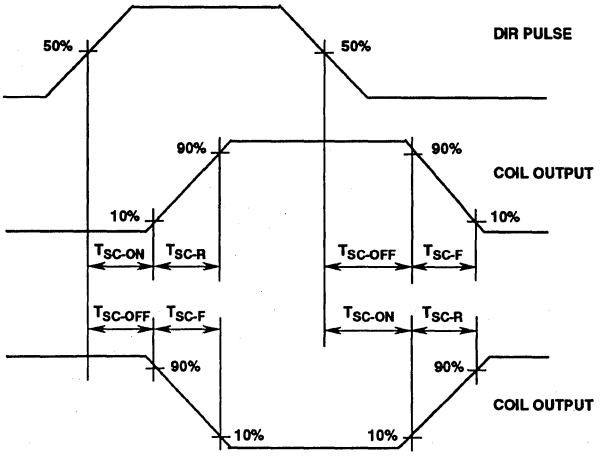
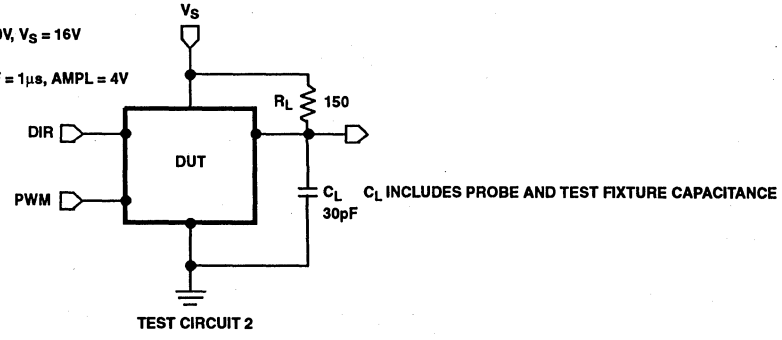


FIGURE 3. SOURCE SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

TEST CONDITIONS: PWM = 0V, V_S = 16V
DIR PULSE PARAMETERS:
F = 1kHz, W = 100µs, TR = TF = 1µs, AMPL = 4V



PWM PULSE PARAMETERS:
F = 1kHz, W = 100µs, TR = TF = 1µs, AMPL = 4V

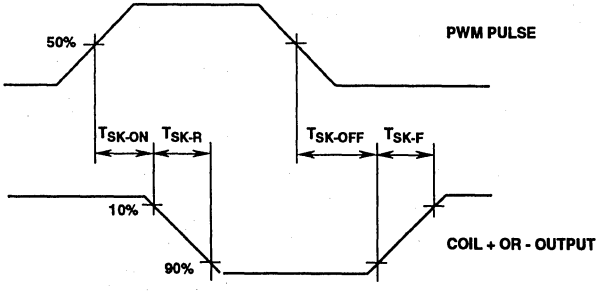


FIGURE 4. SINK SWITCHING TEST CIRCUIT AND VOLTAGE WAVEFORMS

HARRIS SEMICONDUCTOR

HIP4010

ADVANCE INFORMATION

May 1992

Power H-Switch

Features

- Two Independent 1/2 H-Switch Drivers
- Single Supply . . . . . +4V to +15V
- Dual Supplies . . . . . ±2V to ±7.5V
- Switching Capabilities 0.5A
- CMOS Input (TTL Compatible)
- Complementary (CMOS) Switching Circuit
- Over-Temperature Protection
- Current-Overload Protection
- "Dynamic Braking" Circuit
- Rds_{ON} . . . . . 0.5Ω per Switching MOSFET

Applications:

- Motor Control
- Relay Driver
- Solenoid Driver
- Stepper Motors

Description

In the Functional Block Diagram of the HIP4010 the four switches and a load are arranged in an H-configuration so that the polarity of the dc supply voltage (from terminals V_{DDA} and V_{SSA}) applied to the load can be selected by switching; thereby directing the flow of load current in either direction. This is commonly known as 4-quadrant load control. As drawn in the Functional Block Diagram, switches P1 and N2 are "closed;" when current flows from V_{DDA} through P1, through the load, and then through N2 to terminal V_{SSA}; where load terminal OUT1 is at a positive potential with respect to OUT2. Switches P1 and N2 are operated synchronously by the control logic. The control logic switches P2 and N1 to an "open" state when P1 and N2 are "ON". When the switch states are reversed, P1 and N2 are open and N1 and P2 are closed. Consequently, current then flows from V_{DDA} through P2, through the load, and through N1 to terminal V_{SSA}, where load terminal OUT2 is then at a positive potential with respect to OUT1.

The HIP4010 POWER H-Switch is designed in a high speed BiMOS-E technology, using both CMOS and bipolar transistors. The BiMOS-E process adds a drain extension implant to 3μ poly-gate CMOS transistors, enhancing the device voltage capabilities. Vertical bipolar transistors, having high gain-bandwidth and transconductance, are standard in the BiMOS-E technology.

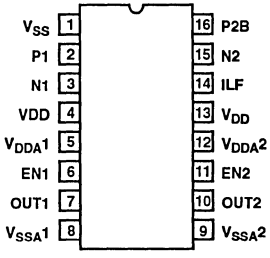
The HIP4010 POWER H-Switch is available in a 16 Lead Dual-In-Line Plastic Package with heat spreading frame construction to enhance thermal dissipation. Under normal conditions, the HIP4010 can dissipate 1.5W (typ.) in free air at +60°C and can dissipate 1.5W (typ.) at +105°C with a PC-Board as a heat-sink.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE & LEAD FORM
HIP4010MP	-55°C to +125°C	16 Lead DIP

Pinout

16 LEAD DUAL-IN-LINE PLASTIC PACKAGE
TOP VIEW



NOTE: Terminals 4, 5, 12 and 13 are interconnected

Functional Truth Table

HIP4010 H-SWITCH

SWITCH DRIVER 1				SWITCH DRIVER 2			
INPUTS			OUTPUT	INPUTS			OUTPUT
P1	N1	EN1	OUT1	P2B	N2	EN2	OUT2
H	L	H	OH	L	L	H	OH
L	L	H	OL	H	L	H	OL
H	H	H	OL	L	H	H	OL
L	H	H	OL	H	H	H	OL
X	X	L	Z	L	H	H	OL

L = Low logic level; H = High logic level
Z = High Impedance (off state)
OH = Output High (sourcing current to the output terminal)
OL = Output Low (sinking current from the output terminal)
X = Don't care

7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3176

Absolute Maximum Ratings

DC Supply Voltage (Between $V_{DDA}1$ and $V_{SSA}1$ Terminals).... 16V
DC Supply Voltage (Between $V_{DDA}2$ and $V_{SSA}2$ Terminals).... 16V
DC Supply Voltage (Between V_{DD} and V_{SS} Terminals) 16V
DC Input Voltage 16V
Input Terminal Current 1mA
Recommended DC Operating Voltage Range
(V_{DD} to V_{SS}, $V_{DDA}1$ to $V_{SSA}1$, $V_{DDA}2$ to $V_{SSA}2$) .... +4V to +15V
Operating Temperature Range..... -55°C to +125°C
Junction Temperature, T_J..... +150°C
Lead Temperature (During Soldering) ..... +265°C

Power Dissipation (P_D)
Up to +60°C (Free Air)..... 1.5W
Above +60°C ..... Derate linearly at 16.6mW/°C
Up to +90°C, with Heat Sink (PC Board)..... 1.5W
Above +90°C ..... Derate linearly at 25mW/°C
Maximum Thermal Resistance (Free Air*) Junction-to-Air .... +60°C/W
* In free air, the junction-to-air thermal resistance ($R_{\theta JA}$) is typically +50°C/W. This coefficient can be lowered to 40°C/W by suitable design of the PC board to which the HIP4010 package is soldered.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Typical Values Intended Only for Design Guidance

T_A = +25°C, $V_{DDA}1$, $V_{DDA}2$, and V_{DD} = +12V; $V_{SSA}1$, $V_{SSA}2$, and V_{SS} = 0V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	TYPICAL VALUES	UNITS
Output Current			0.5	A
Input Resistance			0.5	TΩ
Saturation Voltage I_{SINK} = 0.5A	V_{SAT}		0.25	V
Response Time Rise	t_r	C_L = 5pF R_L = 1MΩ	1.0	µs
Response Time Fall	t_f		0.2	µs

Electrical Specifications

T_A = +25°C, $V_{SSA}1$, $V_{SSA}2$, and V_{SS} = 0V, Unless Otherwise Specified

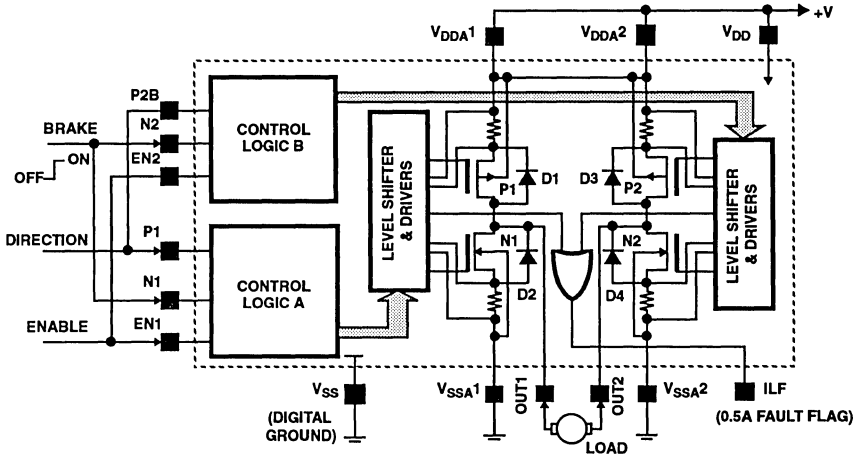
PARAMETERS	SYMBOL	LIMITS			UNITS
		MIN	TYP	MAX	
$V_{DDA}1$, $V_{DDA}2$, and V_{DD} = +12V:					
Input Current	CI1	-	40	50	pA
Input Voltage Range	VI	0.0	-	12.0	V
Idle Supply Current; I_{OUT} = 0	I_{SUPPLY}	-	10	15	mA
Output Voltage High; (V_{SAT}) I_{SOURCE} = 0.5A	V_{OH}	11.65	11.7	11.75	V
Output Voltage Low; (V_{SAT}) I_{SINK} = 0.5A	V_{OL}	0.25	0.30	0.35	V
Response Time Rising Edge	t_{DR}	-	1.0	TBE	µs
Response Time Falling Edge	t_{DF}	-	0.1	TBE	µs
Output Source Current		-	500	530	mA
Output Sink Current		450	500	530	mA
$V_{DDA}1$, $V_{DDA}2$, and V_{DD} = +5V:					
Input Current	CI1	-	40	50	pA
Input Voltage Range	VI	0.0	-	5.0	V
Idle Supply Current; I_{OUT} = 0	I_{SUPPLY}	-	3.0	4.0	mA
Output Voltage High; I_{SOURCE} = 0.5A	V_{OH}	4.55	4.6	4.65	V
Output Voltage Low; (V_{SAT}) I_{SINK} = 0.5A	V_{OL}	0.35	0.40	0.45	V
Response Time Rising Edge	t_{DR}	-	1.0	TBE	µs
Response Time Falling Edge	t_{DF}	-	0.1	TBE	µs
Output Source Current		450	500	530	mA
Output Sink Current		450	500	530	mA

Application

The Functional Block Diagram shows an application block diagram of a motor-driver circuit using HIP4010 as a "Full" H-Switch. The "left" and "right" H-Switch's are driven from the control input terminals to the output switching transistors of the HIP4010. The circuit is intended to safely start, stop, and provide control of rotational direction for a motor requiring no more than 0.5 A of supply current. The stop function includes a "dynamic braking" feature.

With the "ENABLE" terminal LOW, MOSFET Switches P1 and P2 are "off;" i.e., supply current is cut off. With the "BRAKE" terminal LOW and "ENABLE" transitioned HIGH, either P1, N2 or P2, N1 can be driven into conduction; the CMOS-pair chosen for conduction is determined by the logic level applied to the "DIRECTION" terminal; resulting in either clockwise (CW) or counterclockwise (CCW) shaft rotation. When the "BRAKE" terminal is transitioned HIGH (while holding ENABLE at HIGH), the gates of both N1 and N2 are driven HIGH. Thus, if current was flowing through N1 (from the motor terminal OUT1) at the moment of "dynamic braking," it would continue to flow through N1 to the $V_{SSA}1/V_{SSA}2$ external ground tie, then continue through diode D4 to motor terminal OUT2; the resistance of the motor winding (and the series-connected path) dissipates the kinetic energy stored in the system. Reversing rotation, current flowing through N2 (from the motor terminal OUT2), at the moment of "dynamic braking", would continue to flow through N2 to the $V_{SSA}2/V_{SSA}1$ tie, then continue through diode D2 to the motor terminal OUT1, to dissipate the stored kinetic energy as previously described.

Functional Block Diagram



Terminal Assignment Information

$V_{DDA}1$	Positive terminal-pin for power-supply; $V_{DDA}1$ is internally connected to $V_{DDA}2$ and V_{DD}.
$V_{DDA}2$	Positive terminal-pin for power-supply; $V_{DDA}2$ is internally connected to $V_{DDA}1$ and V_{DD}.
V_{DD}	Positive terminal-pin for power-supply suited to digital circuits; V_{DD} is internally connected to $V_{DDA}1$ and $V_{DDA}2$.
$V_{SSA}1$	Negative terminal-pin for power-supply; used in conjunction with Switch Driver 1.
$V_{SSA}2$	Negative terminal-pin for power-supply; used in conjunction with Switch Driver 2.
V_{SS}	Negative terminal-pin for power-supply suited for digital circuits.
P1, P2B	Input pins used to control the direction of output current flow in Switch Driver 1 and Switch Driver 2, respectively.
N1, N2	Input pins used to activate the Dynamic Braking of Switch Driver 1 and Switch Driver 2, respectively.
EN1, EN2	Input pins used to enable Switch Driver 1 and Switch Driver 2, respectively.
OUT1, OUT2	Output pins for Switch Driver 1 and Switch Driver 2, respectively.
ILF	Output pin (flag); high logic level signify that Switch Driver1, Switch Driver2, or both are in "Current Limit" state

NOTES:

1. Terminals P1, P2, N1, N2, P2B, EN1 and EN2 are internally connected to protection circuits intended to guard the CMOS gate-oxides against damage due to electrostatic discharge. However, these devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.
2. For maintenance of performance and reliability, Harris Semiconductor strongly recommends that the "IC Handling Procedures", located in Section 1 of the current Analog Products Data Book, be followed closely by any activity involved with IC products.

HARRIS SEMICONDUCTOR

HIP4011

PRELIMINARY

May 1992

Three-Phase Brushless DC Motor Controller

Features

- 3A DC, 5A Peak Output Current
- 16V Max. Rated Supply Voltage
- Built-in "Free-Wheeling" Diodes
- Output dv/dt Limited to Reduce EMI
- External Dynamic Brake Control Switch With Undervoltage Sense
- Thermal & Current Limiting Protects Against Locked Rotor Conditions
- Provides Analog Current Sense & Reference Inputs
- Decode Logic with Illegal Code Rejection

Applications

- Drive Spindle Motor Controller
- 3ϕ Brushless DC Motor Controller
- Brushless DC Motor Driver for 12V Battery Powered Appliances
- Phased Driver for 12V DC Applications
- Logic Controlled Driver for Solenoids, Relays & Lamps

Description

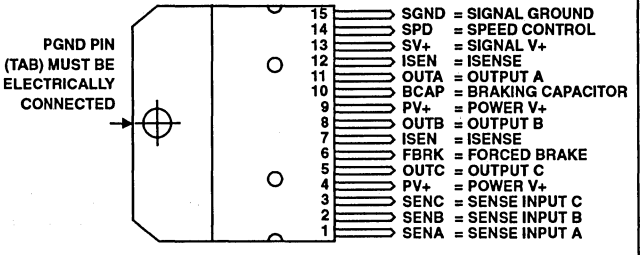
The HIP4011 motor driver is intended for three phase brushless motor control at continuous output currents up to 3A. It accepts inputs from buffered Hall effect sensors and drives three motor windings, regulating the current through an external current sensing resistor, according to an analog control input. Output "freewheeling" diodes are built in and output dv/dt is limited to decrease the generated EMI. Thermal and current limiting are used to protect the device from locked rotor conditions. A brake control input forces all outputs to ground simultaneously to provide dynamic braking, and an internal voltage sensor does the same when the supply drops below a predetermined switch point. Power down braking energy is stored in an external capacitor.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP4011IS	-40°C to +85°C	15 Lead Power SIP

Pinout

15 LEAD POWER SIP
TOP VIEW



OUTPUT TRUTH TABLE

SENSOR INPUTS			FORCE BRAKE INPUT*	OUTPUTS		
A	B	C	FBRK	A	B	C
0	0	0	0	OFF	OFF	OFF
1	0	0	0	1	OFF	0
0	1	0	0	0	1	OFF
1	1	0	0	OFF	1	0
0	0	1	0	OFF	0	1
1	0	1	0	1	0	OFF
0	1	1	0	0	OFF	1
1	1	1	0	OFF	OFF	OFF
X	X	X	1	0	0	0

* Undervoltage and Force Brake logic truth table entries are identical.

"X" = Don't Care

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2939.1**

Absolute Maximum Ratings

Supply Voltage, SV+ or PV+ . . . . . -1V to +16V
Referred to SGND or PGND (Note 1)
Output Current, Continuous 3A
Output Current, Peak (Note 2) 5A
Substrate (PGND) Current 1A
Logic Input Current . . . . . -20mA to +20mA
(Clamped to SV+ and SGND)

Dissipation/Temperature Ratings

Power Dissipation (Note 3) 25W
Junction Temperature Range, Operating . . . . . +150°C
Storage Temperature Range . . . . . -55°C to +150°C

NOTES:

1. PV+ and SV+ are to be tied together, as are PGND and SGND.
2. Operating above the continuous current rating causes a decrease in operating life.
3. Derate power dissipation above case temperature of +75°C at 0.33 Watts/°C.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified

CHARACTERISTIC	TEST CONDITION	LIMITS			UNITS
		MIN	TYP	MAX	
SUPPLY (SV+) CURRENT					
No Drive	Outputs Off			10	mA
With Drive	Outputs On			15	mA
LOGIC INPUT CURRENT					
Sensor Inputs	SENA, SENB & SENC = 0V to 3V	-0.5		-1.5	mA
Brake Input	FBRK = 0.8V to 2.4V	50		150	µA
LOGIC INPUT THRESHOLDS					
Sensor Inputs	Logic "0" Input Voltage			1.8	V
Sensor Inputs	Logic "1" Input Voltage	3			V
Brake Input	Logic "0" Input Voltage			0.8	V
Brake Input	Logic "1" Input Voltage	2.4			V
AMPLIFIER INPUT (SPD)					
Bias Current				700	nA
Offset Voltage				3	mV
Input Range (Linear)		0		1	V
Input Impedance		1			MΩ
SYSTEM BANDWIDTH	(Note 1)		35		kHz
CURRENT LIMIT	Rsense = 0.20Ω		5		A
THERMAL LIMIT					
Threshold			155		°C
Hysteresis			40		°C
OUTPUT DRIVERS					
On Saturation (See Note 5)	Iout = 3A, Vpmos + Vnmos			2.2	V
On Saturation (See Note 5)	Iout = 0.6A, Vpmos + Vnmos			0.44	V
Off Leakage	PV+ > Vout > PGND or Isen			1	mA
Slew Rate	(See Note 2)		0.5		V/µS
FREEWHEEL DIODES					
Forward Drop	Iout = 1A			1.5	V

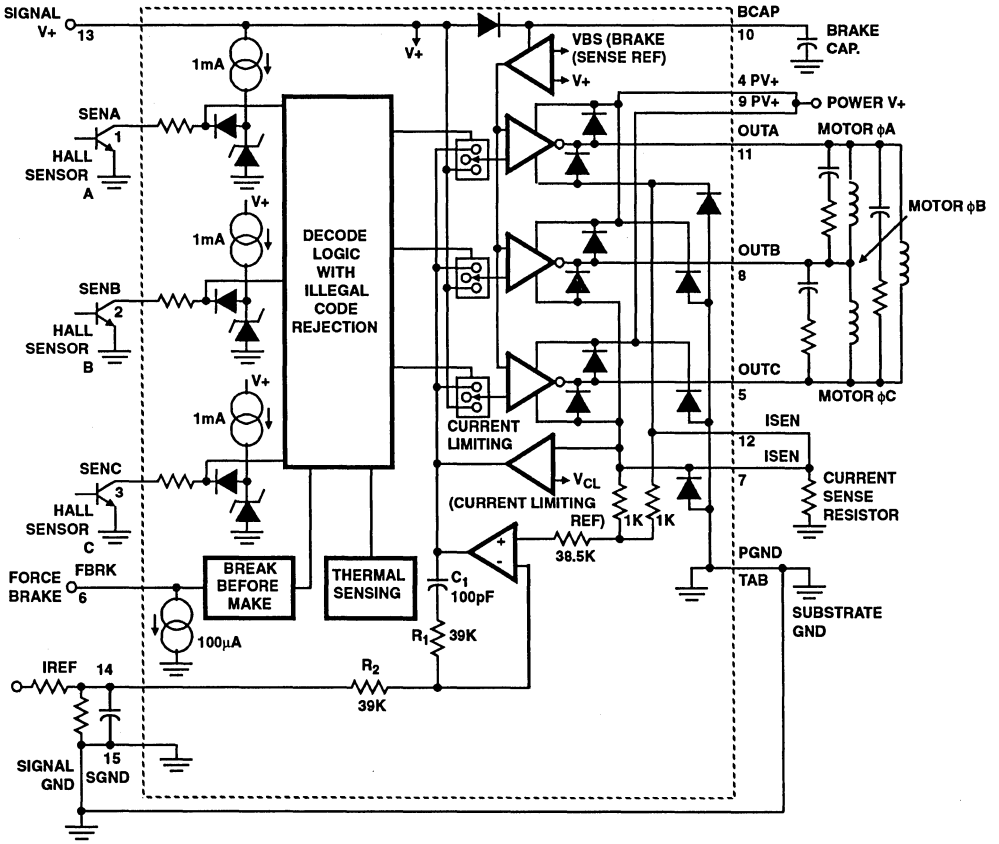
Electrical Specifications T_A = +25°C and SV+ = PV+ = 10.4V to 13.2V, Unless Otherwise Specified (Continued)

CHARACTERISTIC	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
INTERNAL BRAKE DRIVER					
Undervoltage Trip Point, PV+	(See Note 3)	2.7		3.3	V
Hysteresis	(See Note 4)	40		60	%
On Saturation	Each Nmos, Iout = 3A			0.4	V
BRAKE CAPACITOR (BCAP)					
Discharge Leakage	SV+ = PV+ = 3V to 12V, BCAP = 10V			5	µA

NOTES:

1. The system bandwidth is fixed by an internal RC network around the amplifier.
2. Internal limiting of turn on and turn off drive is used to limit output dv/dt.
3. The braking action starts at the given trip point with a falling supply voltage.
4. Hysteresis causes the brake to be removed at a higher trip point with a rising supply voltage.
5. This value includes the combined voltage drops of one upper plus one lower switch at the indicated current.

Functional Block Diagram



THREE-PHASE BRUSHLESS CONTROLLER

HARRIS SEMICONDUCTOR

HIP4080

ADVANCE INFORMATION

May 1992

High Frequency H-Bridge Driver

Features

- High Voltage Capability; Bootstrap Supply Max Voltage to 95VDC
- Bus Voltage .....80V (Max)
- Small Surface Mount Package
- Drives 1000pF Load at 450KHz in Free Air at 50°C with Rise and Fall Times of Typically 10ns
- User-Programmable Dead Time
- Drives 4 N-Channel Devices in H-Bridge Configuration
- On-chip Charge-Pumps Maintain Bootstrap Supplies
- HEN Pin can PWM Upper Switches Only
- HEN (High Enable) and DIS (Disable) Pins Override Input Control
- Proprietary Circuitry Minimizes On-Chip Switching Losses
- Input Logic Thresholds Compatible with 5 and 15 volt Logic Levels
- On-Chip Control Circuit Initializes Bootstrap Capacitors upon Chip Enable

Applications

- Medium/Large Voice Coil Motors
- H-Bridge Power Supplies
- Digital Power Amplifiers for Hi-Fi systems
- High Speed Stepper Motor controls

Description

The HIP4080 is a high frequency, medium voltage H-Bridge N-Channel MOSFET driver IC, packaged in a 20 or 24 pin plastic SOIC. Due to its ability to switch at frequencies greater than 500KHz,the HIP4080 is particularly well suited for driving Voice Coil Motors for medium and large computer disk drives, switching amplifiers in high-efficiency switching audio amplifiers and H-Bridge power supplies depending on load and cooling techniques.

Short propagation delays of approximately 70ns and dead times of typically 40ns coupled with "minimum on times" of about 100ns allow a nearly distortionless, ripple-free current waveform and maximum control loop crossover frequencies providing rapid, fine control of the driven load.

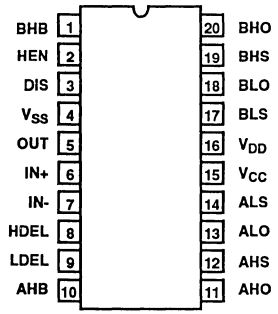
HIP4080 can also drive any small, medium voltage brush motor, and two HIP4080s can be used to drive high performance stepper motors, since the short minimum "on-time" can provide fine micro-stepping capability.

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
HIP4080IP	-40°C to +85°C	20 Pin Plastic DIP
HIP4080IB	-40°C to +85°C	20 Pin Plastic SOIC

Pinout

20 PIN PLASTIC DIP
20 PIN SOIC
TOP VIEW

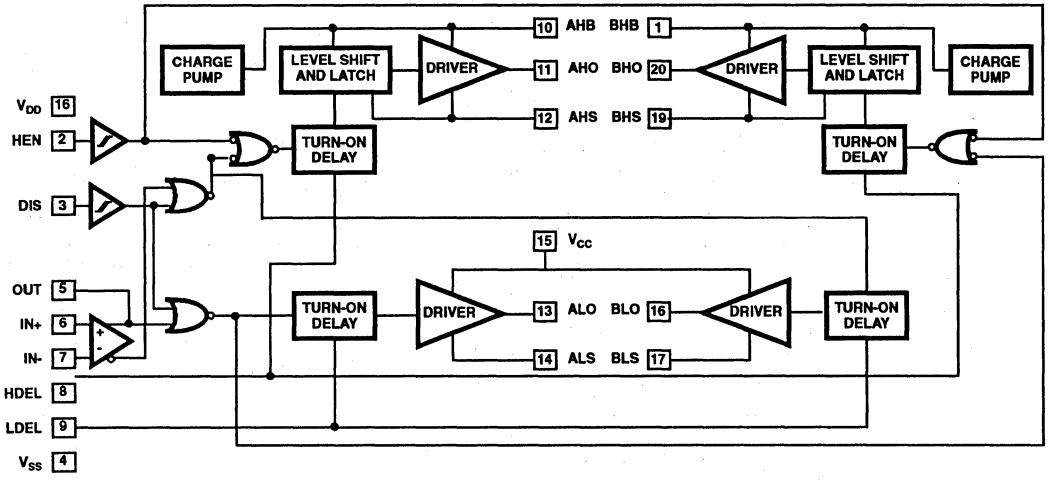


6 FULL BRIDGE

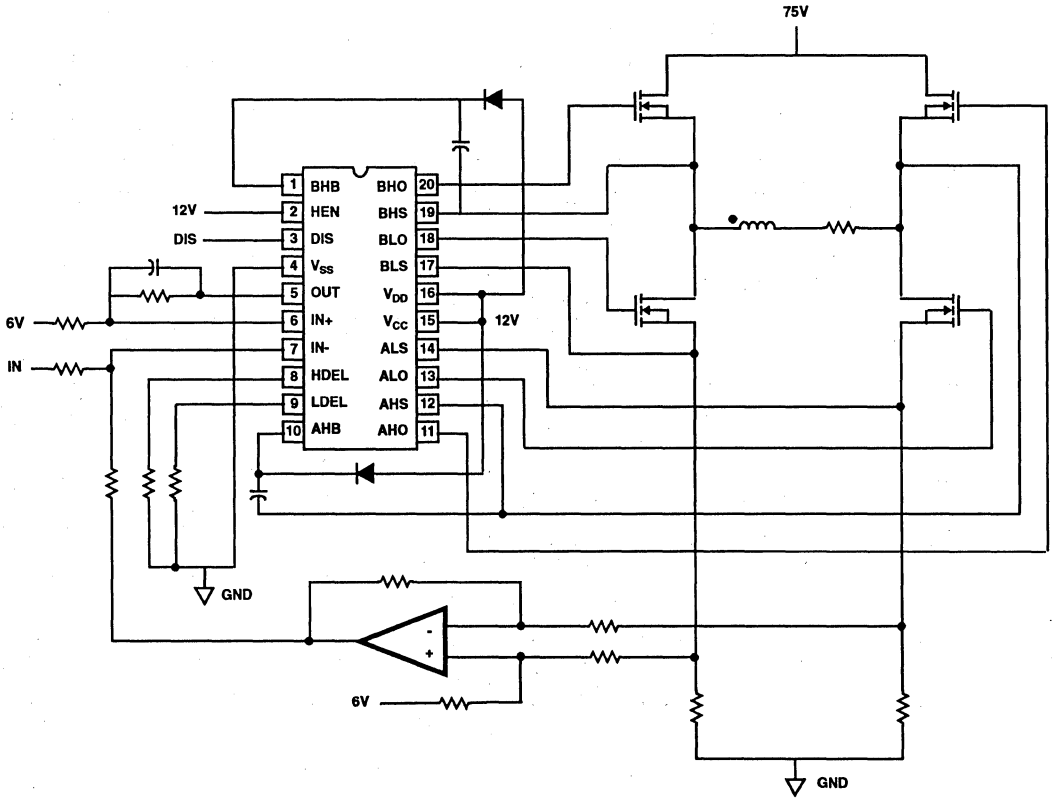
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3178**

Functional Block Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{DD} and V_{CC} ..... -0.3V to 16V
Input, Output or I/O Voltage ..... -0.3V to V_{DD}+0.3V
Voltage on AHS, BHS ..... -2.0V (Transient) to 80V
Voltage on ALS, BLS ..... -2.0V (Transient) to +2.0V (Transient)
Voltage on AHB, BHB ..... $V_{AHS, BHS}$-0.3V to $V_{AHS, BHS}$+16V
Voltage on ALO, BLO ..... $V_{ALS, BLS}$-0.3V to V_{CC}+0.3V
Voltage on AHO, BHO ..... $V_{AHS, BHS}$-0.3V to $V_{AHB, BHB}$+0.3V
Input Current, HDEL and LDEL ..... -5mA to 0mA
Phase Slew Rate 20V/ns
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Maximum Package Power Dissipation at +25°C (Note 1)
SOIC Package 750mW

NOTE:

1. Derate power dissipation above ambient temperature of 25°C by 7mW/°C. $P_{diss} = 0.144 + 0.2e^{-6} f_{PWM} + 2 V_{CC}^2 C_L (f_{PWM} + f_{DIR})$ where f_{PWM} = pwm frequency and f_{DIR} = direction change frequency (in Hertz) C_L = load capacitance (in Farads)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage, V_{DD} and V_{CC} ..... +10V to +15V
Voltage on ALS, BLS ..... -1.0V +1.0V
Voltage on AHS, BHS ..... -1V to 75V
Voltage on AHB, BHB ..... $V_{AHS, BHS}$+10V to $V_{AHS, BHS}$+15V
Input Current, HDEL and LDEL ..... -500µA to -50µA
Operating Temperature Range ..... 0°C to +125°C

Electrical Specifications

Specifications apply over recommended operating conditions, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
QUIESCENT SUPPLY CURRENTS (specified with static inputs that fully switch outputs)						
V_{DD} Current	I_{DD}		8	12	20	mA
V_{CC} Current	I_{CC}	$I_{ALO} = I_{BLO} = 0$	0	100	200	µA
AHB Current	I_{AHB}	$I_{AHO} = 0$	-40	-20	0	µA
BHB Current	I_{BHB}	$I_{BHO} = 0$	-40	-20	0	µA
AHS Current	I_{AHS}	$I_{AHO} = 0$	-5	0	1	µA
BHS Current	I_{BHS}	$I_{BHO} = 0$	-5	0	1	µA
INPUT COMPARATOR						
Offset Voltage	V_{OS}		-5	0	+5	mV
Input Bias Current	I_{IB}		0	1	4	µA
Input Offset Current	I_{OS}		-1	0	+1	µA
Input Common Mode Voltage Range	CMVR		1	-	V_{DD}-1.5	V
Voltage Gain	AVOL		10	25	-	V/mV
OUTPUT (OUT)						
High Level Output Voltage	V_{OH}	IN+>IN-, I_{OH} = -300µA	V_{DD}-0.4	-	-	V
Low Level Output Voltage	V_{OL}	IN+<IN-, I_{OL} = 300µA	-	-	0.4	V
High Level Output Current	I_{OH}	$V_{OUT}=V_{DD}/2$	-	-	-2.4	mA
Low Level Output Current	I_{OL}	$V_{OUT} = V_{DD}/2$	4.5	-	-	mA
DIS, HEN						
Low Level Input Threshold Voltage	V_{TL}		1.4	2.1	-	V
High Level Input Threshold Voltage	V_{TH}		-	2.4	2.7	V
Input Hysteresis	V_{HYS}		-	0.3	-	V
GATE DRIVER OUTPUTS						
Peak Pullup Current	I_{O+}	V_{CC} = 12V	-	2	-	A
Peak Pulldown Current	I_{O-}	V_{CC} = 12V	-	2	-	A

Switching Specifications

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Minimum Input Pulse Width	T_{PWIN}	IHDEL = -100 µA ILDEL = -50 µA	-	100	-	ns
Mimimum Output Pulse Width	T_{PWOUT}	IHDEL = -100 µA ILDEL = -50 µA	-	100	-	ns
HEN Prop. Delay	T_{PHEN}	IHDEL = -100 µA ILDEL = -50 µA	-	70	-	ns
Upper Prop. Delay (Turn-Off)	T_{PH}	IHDEL = -100 µA ILDEL = -50 µA	-	70	-	ns
Lower Prop. Delay (Turn-t_{OFF})	T_{PL}	IHDEL = -100 µA ILDEL = -50 µA	-	70	-	ns
DISable Prop. Delay	T_{PDIS}	IHDEL = -100 µA ILDEL = -50 µA	-	150	-	ns
Dead Time	T_{DTLH}	IHDEL = -100 µA ILDEL = -50 µA Lower off toUpper on, C_L = 1000 pF	-	40	-	ns
Dead Time	T_{DTHL}	IHDEL = -100 µA ILDEL = -50 µA Upper off toLower on, C_L = 1000 pF	-	40	-	ns
Rise Time	T_R	C_L=2500pf	-	20	-	ns
		C_L=1000pf	-	10	-	ns
Fall Time	T_F	C_L=2500pf	-	20	-	ns
		C_L=1000pf	-	10	-	ns

INTELLIGENT POWER ICs 7

REGULATORS/POWER SUPPLIES

Selection Guide

POWER SUPPLY CIRCUITS

DEVICE	DESCRIPTION	INPUT VOLTAGE RANGE	OUTPUT VOLTAGE RANGE	MAXIMUM OUTPUT CURRENT	SWITCHING FREQUENCY	QUIESCENT CURRENT	TEMP. RANGE
CA723	Linear Voltage Regulators	9.5V to 40V	2V to 37V	150mA	-	3.5mA	-55°C to +125°C
CA723C						4.0mA	0°C to +70°C
CA1523	Variable Internal Pulse Regulator for Switch Mode Power Supplies	11V to 15V	5.9V to 7.5V*	50mA	≈ 200kHz	34mA	0°C to +70°C
CA1524	Pulse Width Modulators	8V to 40V	4.8V to 5.2V*	100mA Max Rating for Each Output Driver	1kHz to 300kHz	10mA	-55°C to +125°C
CA2524			4.8V to 5.2V*				0°C to +70°C
CA3524			4.6V to 5.4V*				0°C to +70°C
CA3085	Linear Voltage Regulators	7.5V to 30V	1.8V to 26V	12mA to 100mA	-	4.5mA at V_{IN} = 30V	-55°C to +125°C
CA3085A		7.5V to 40V	1.7V to 36V	12mA to 100mA		5.0mA at V_{IN} = 40V	
CA3085B		7.5V to 50V	1.7V to 46V	12mA to 100mA		7.0mA at V_{IN} = 50V	
CA3277	Smart Microprocessor Dual-Fixed 5V Regulator, Overvoltage Shutdown, Thermal Shutdown, Current Limited	6.2V to 18V (Shutdown)	Output 1 - Full Time 5V ± 0.25V Output 2 - Switched 5V ± 0.25V	Output 1 - 50mA Output 2- 80mA	-	400µA	-40°C to +85°C
HIP5060	Single Chip, Low Side Switch, Current Controlled PWM	16V to 45V	Determined by External Circuitry	Power DMOS Transistor 60V - 10A	1MHz Internal, External Input	20mA	0°C to +85°C
HIP5062	Single Chip, Dual Low Side Switch Current Controlled PWM	16V to 42V	Determined by External Circuitry	Two Power DMOS Transistors 60V - 5A	1MHz Latched External Loop	25mA	0°C to +85°C
HIP5063	Basic Single Chip, Low Side Switch Current Controlled PWM	12V to 60V	Determined by External Circuitry	Power DMOS Transistor	External Clock	14mA	0°C to +85°C
HIP5500	Half Bridge Power Supply Regulator	10V to 15V	-VBS to 500V	2.3A peak, 200mA cont.	30kHz to 300kHz	7mA	-40°C to +150°C
ICL7644**	Low Voltage Boost Type Step-Up Converters	1.15V to 4.0V	4.5V to 5.5V	150mA	18kHz	80µA	-40°C to +85°C 0°C to +70°C
ICL7645		1.15V to 5.6V	4.5V to 5.5V			40µA	
ICL7646		1.15V to 4.0V	4.5V to 5.5V			80µA	
ICL7647		2.0V to 3.6V	2.7V to 3.3V			80µA	
ICL7660SM	Super Voltage Converter (Charge Pump Type)	3V to 12V	-12V to 22.8V	45mA	10kHz to 35khZ	200µA	-55°C to +125°C
ICL7660SI						180µA	-25°C to +85°C
ICL7660SC						180µA	0°C to +70°C
ICL7662M	Voltage Converter (Charge Pump Type)	4.5V to 20V	-4.5V to -20V	90mA	10kHz	250µA	-55°C to +125°C
ICL7662C						200µA	0°C to +70°C
ICL7663SA	Linear Voltage Regulators	1.0V to 16V	1.3V to 16V	40mA - V_{OUT2} R_{ON} - 100 V_{OUT1}	-	10µA	-25°C to +85°C
ICL7663S						12µA	0°C to +70°C

* Reference Voltages - Output Voltage Limited by External Device

** The ICL76XX Series have an Additional Shutdown Feature; In Shutdown Mode Quiescent Current < 5µA

VOLTAGE MONITORING CIRCUITS

DEVICE	DESCRIPTION	VOLTAGE RANGE	QUIESCENT CURRENT	OUTPUT CURRENT	INPUT TRIP VOLTAGE	TEMPERATURE RANGE
ICL7665SAI	CMOS Micropower Over/ Under Voltage Detector	1.8V to 16V	10µA	2mA	1.3 ± 2%	-25°C to +85°C
ICL7665SAC					1.3 ± 8%	0°C to +70°C
ICL7665SI					1.3 ± 2%	-125°C to +85°C
ICL7665SC					1.3 ± 8%	0°C to +70°C
ICL7673I	Automatic Battery Back-up Switch	2.5V to 15V	5µA	38mA	50mV*	-25°C to +85°C
ICL7673C						0°C to +70°C
ICL8211M	Programmable Voltage Detectors	1.8V to 30V	350µA	3mA	1.15 + 3.5% 1.15 - 6.0%	-55°C to +125°C
ICL8211C						0°C to +70°C
ICL8212M				9mA	1.15 + 3.5% 1.15 - 13%	-55°C to +125°C
ICL8212C						0°C to +70°C

* Primary to Back-up Source Voltage Differential

HARRIS SEMICONDUCTOR

CA723
CA723C

Voltage Regulators Adjustable from 2V to 37V at Output Currents Up to 150mA Without External Pass Transistors

May 1992

Features

- Up to 150mA Output Current
- Positive and Negative Voltage Regulation
- Regulation in Excess of 10A with Suitable Pass Transistors
- Input and Output Short-Circuit Protection
- Load and Line Regulation.....0.03%
- Direct Replacement for 723 and 723C Industry Types
- Adjustable Output Voltage .....2V to 37V

Applications

- Series and Shunt Voltage Regulator
- Floating Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Temperature Controller

Ordering Information

PART	TEMPERATURE	PACKAGE
CA723E	-55°C to +125°C	14Lead Plastic DIP
CA723T	-55°C to +125°C	10 Lead Can
CA723CE	-55°C to +125°C	14 Lead Plastic DIP
CA723CT	-55°C to +125°C	10 Lead CAN

Description

The CA723 and CA723C are silicon monolithic integrated circuits designed for service as voltage regulators at output voltages ranging from 2V to 37V at currents up to 150 milliamperes.

Each type includes a temperature-compensated reference amplifier, an error amplifier, a power series pass transistor, and a current-limiting circuit. They also provide independently accessible inputs for adjustable current limiting and remote shutdown and, in addition, feature low standby current drain, low temperature drift, and high ripple rejection.

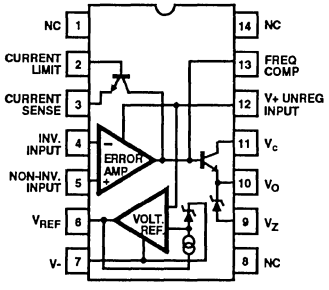
The CA723 and CA723C may be used with positive and negative power supplies in a wide variety of series, shunt, switching, and floating regulator applications. They can provide regulation at load currents greater than 150mA and in excess of 10A with the use of suitable n-p-n or p-n-p external pass transistors.

The CA723 and CA723C are supplied in the 10 lead TO-5 style package (T suffix), and the 14 lead dual-in-line plastic package (E suffix), and are direct replacements for industry types 723, 723C, mA723, and mA723C in packages with similar terminal arrangements. They are also available in chip form ("H" suffix).

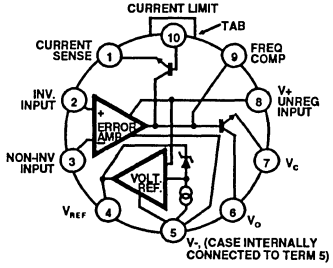
All types are rated for operation over the full military-temperature range of -55°C to +125°C.

Pinouts

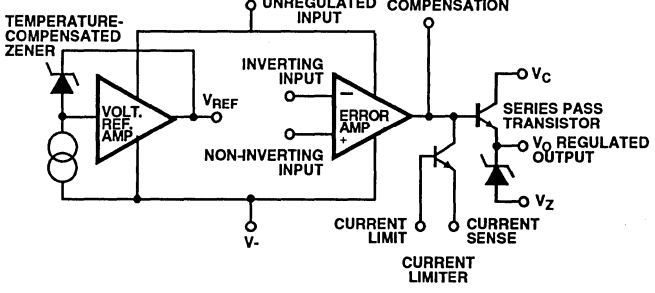
14 PIN PLASTIC DIP (E SUFFIX)
TOP VIEW



10 PIN CAN (T SUFFIX)
TOP VIEW



Functional Block Diagram



7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 788.2

Absolute Maximum Ratings

DC Supply Voltage 40V
(Between V+ and V- Terminals)
Pulse Voltage for 50ms
Pulse Width (Between V+ and V- Terminals) 50V
Differential Input-Output Voltage..... 40V
Differential Input Voltage
Between Inverting and Noninverting Inputs..... ±5V
Between Noninverting Input and V- 8V
Current From Zener Diode Terminal (V_Z) 25mA
Device Dissipation
CA723T, CA723CT, Up to T_A = +25°C 800mW
CA723E, CA723CE, Up to T_A = +25°C..... 1000mW
CA723T, CA723CT, Above T_A = +25°C..... 6.3mW/°C
CA723E, CA723CE, Above T_A = +25°C ..... 8.3mW/°C

Operating Conditions

Ambient Temperature Range
Operating Temperature Range .....-55°C to +125°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature, During Soldering .....+265°C
At a distance 1/16" ± 1/32" (1.59mm ± 0.79mm) from case for 10s max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

T_A = +25°C, V+ = V_C = V_I = 12V, V- = 0, V_O = 5V, I_L = 1mA, C_1 = 100pF, C_{REF} = 0, R_{SCP} = 0, Unless Otherwise Specified. Divider impedance $R_1R_2 \div R_1 + R_2$ at noninverting input, Terminal 5 = 10kΩ (Figure 20)

PARAMETERS	TEST CONDITION	CA723			CA723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Quiescent Regulator Current, I_Q	I_L = 0, V_I = 30V	-	2.3	3.5	-	2.3	4	mA
Input Voltage Range, V_I		9.5	-	40	9.5	-	40	V
Output Voltage Range, V_O		2	-	37	2	-	37	V
Differential Input-Output Voltage, V_I - V_O		3	-	38	3	-	38	V
Reference Voltage, V_{REF}		6.95	7.15	7.35	6.8	7.15	7.5	V
Line Regulation (Note 1)	V_I = 12V to 40V	-	0.02	0.2	-	0.1	0.5	% V_O
	V_I = 12V to 15V	-	0.01	0.1	-	0.01	0.1	% V_O
	V_I = 12V to 15V, T_A = -55°C to +125°C	-	-	0.3	-	-	-	% V_O
	V_I = 12V to 15V, T_A = 0°C to +70°C	-	-	-	-	-	0.3	% V_O
Load Regulation (Note 1)	I_L = 1mA to 50mA	-	0.03	0.15	-	0.03	0.2	% V_O
	I_L = 1mA to 50mA, T_A = -55°C to +125°C	-	-	0.6	-	-	-	% V_O
	I_L = 1mA to 50mA, T_A = 0°C to +70°C	-	-	-	-	-	0.6	% V_O
Output-Voltage Temperature Coefficient, ΔV_O	T_A = -55°C to +125°C	-	0.002	0.015	-	-	-	%/°C
	T_A = 0°C to +70°C	-	-	-	-	0.003	0.015	%/°C
Ripple Rejection (Note 2)	f = 50Hz to 10kHz	-	74	-	-	74	-	dB
	f = 50Hz to 10kHz, C_{REF} = 5μF	-	86	-	-	86	-	dB
Short Circuit Limiting Current, I_{LIM}	R_{SCP} = 10Ω, V_O = 0	-	65	-	-	65	-	mA
Equivalent Noise RMS Output Voltage, V_N (Note 2)	BW = 100Hz to 10kHz, C_{REF} = 0	-	-20	-	-	20	-	μV
	BW = 100Hz to 10kHz, C_{REF} = 5μF	-	2.5	-	-	2.5	-	μV

NOTES:

1. Line and load regulation specifications are given for condition of a constant chip temperature. For high dissipation condition, temperature drifts must be separately taken into account.
2. For C_{REF} (See Figure 20)

Typical Performance Curves (CA723)

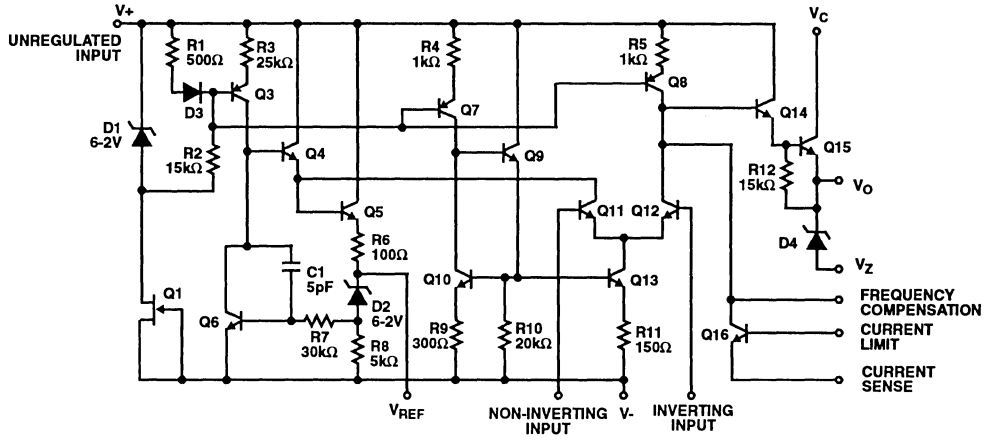


FIGURE 1. EQUIVALENT SCHEMATIC DIAGRAM OF THE CA723 AND CA723C

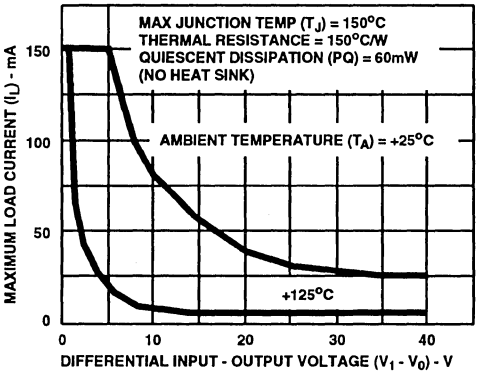


FIGURE 2. MAX LOAD CURRENT vs. DIFFERENTIAL INPUT-OUTPUT VOLTAGE

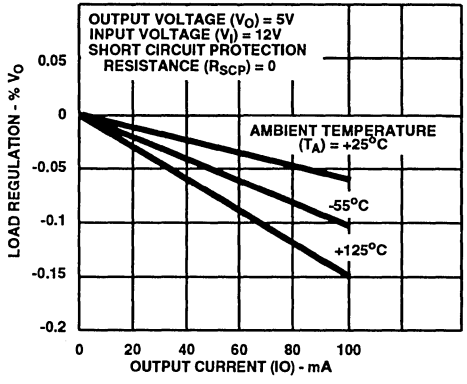


FIGURE 3. LOAD REGULATION WITHOUT CURRENT LIMITING

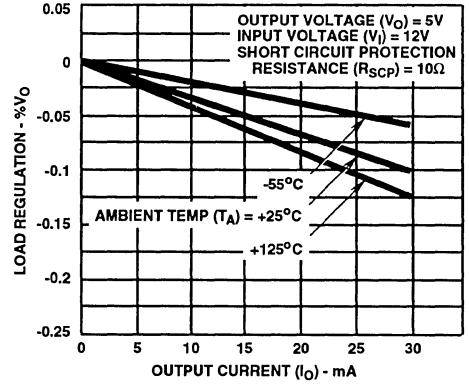


FIGURE 4. LOAD REGULATION WITH CURRENT LIMITING

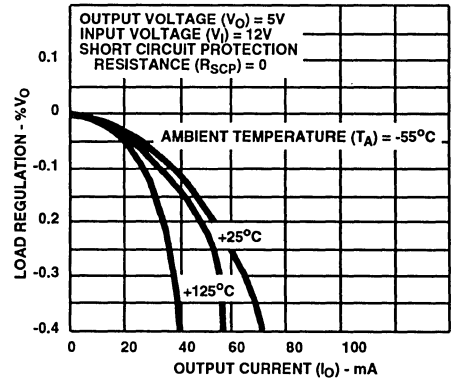


FIGURE 5. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

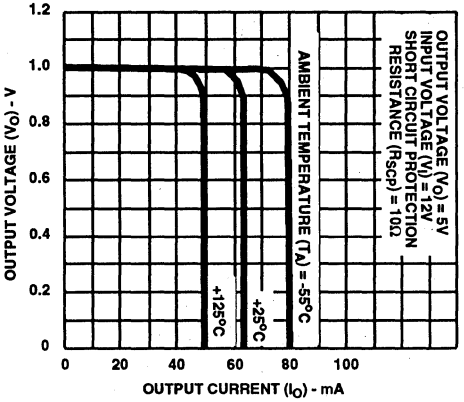


FIGURE 6. CURRENT LIMITING CHARACTERISTICS

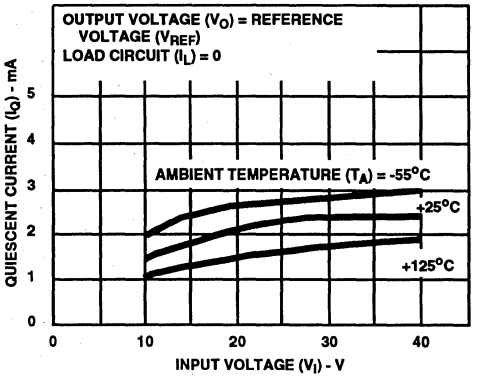


FIGURE 7. QUIESCENT CURRENT vs. INPUT VOLTAGE

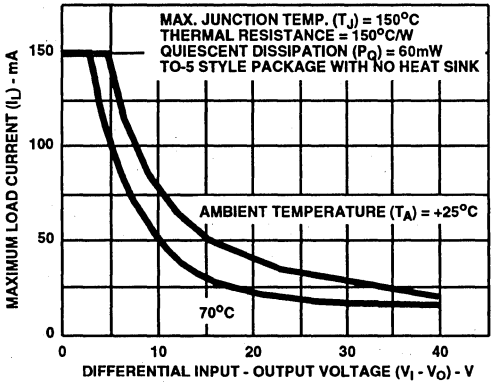


FIGURE 8. MAX LOAD CURRENT vs. DIFFERENTIAL INPUT-OUTPUT VOLTAGE

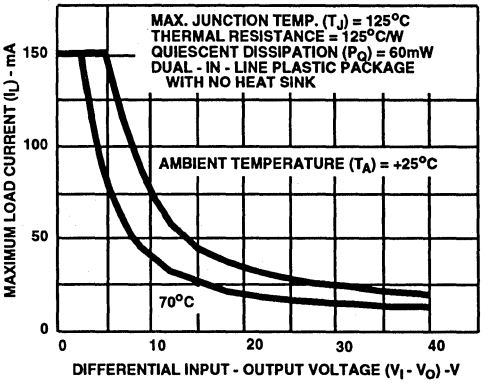


FIGURE 9. MAX LOAD CURRENT vs. DIFFERENTIAL INPUT-OUTPUT VOLTAGE FOR CA723CE

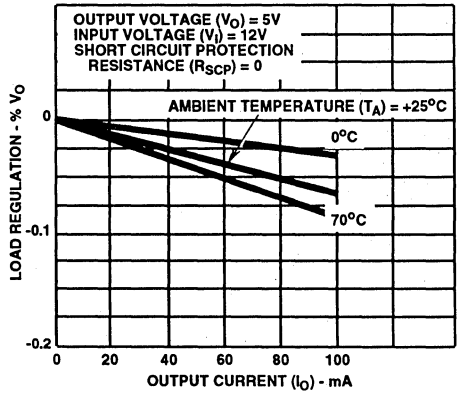


FIGURE 10. LOAD REGULATION WITHOUT CURRENT LIMITING

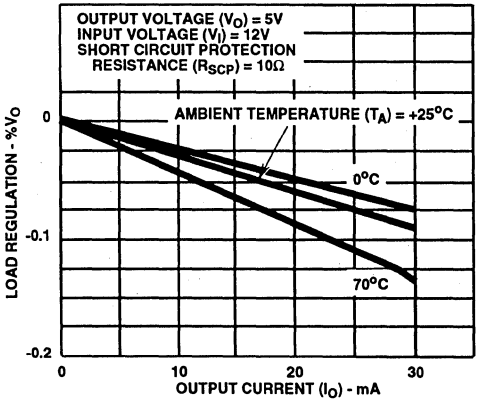


FIGURE 11. LOAD REGULATION WITH CURRENT LIMITING

Typical Performance Curves (CA723) (Continued)

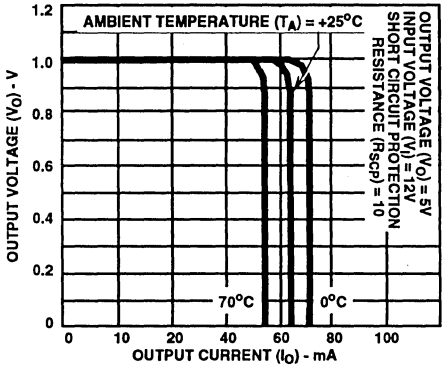


FIGURE 12. CURRENT LIMITING CHARACTERISTICS

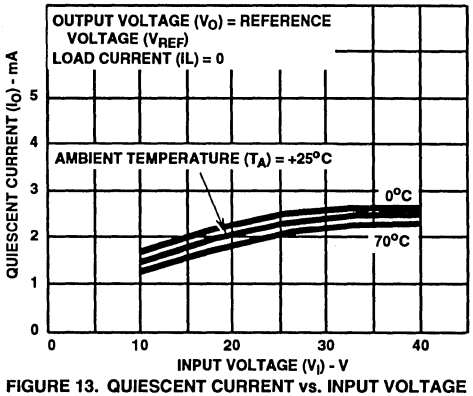


FIGURE 13. QUIESCENT CURRENT vs. INPUT VOLTAGE

Typical Performance Curves (CA723 and CA723C)

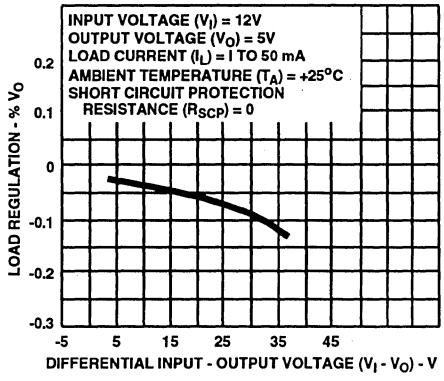


FIGURE 14. LOAD REGULATION vs. DIFFERENTIAL INPUT-OUTPUT VOLTAGE

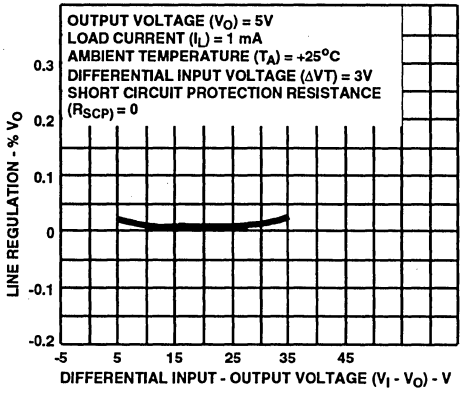


FIGURE 15. LINE REGULATION vs. DIFFERENTIAL INPUT-OUTPUT VOLTAGE

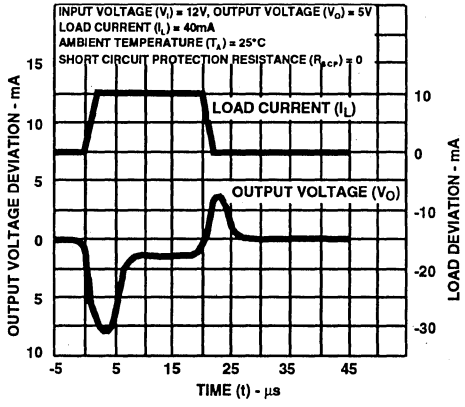


FIGURE 16. LINE TRANSIENT RESPONSE

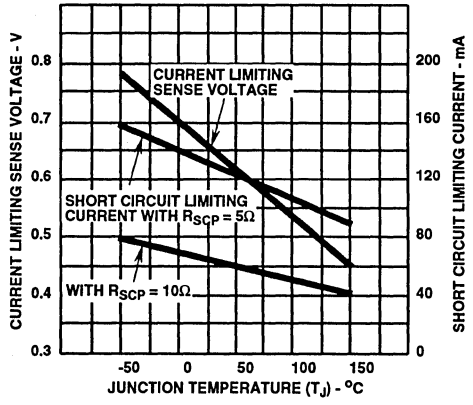


FIGURE 17. CURRENT LIMITING CHARACTERISTIC vs. JUNCTION TEMPERATURE

Typical Performance Curves (CA723 and CA723C) (Continued)

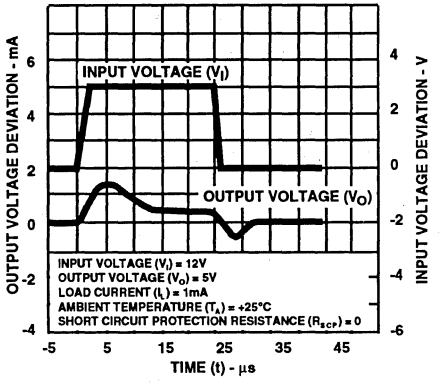


FIGURE 18. LOAD TRANSIENT RESPONSE

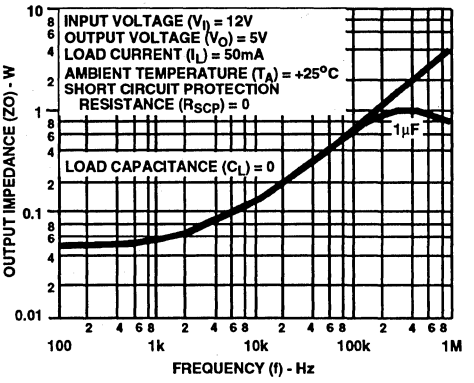
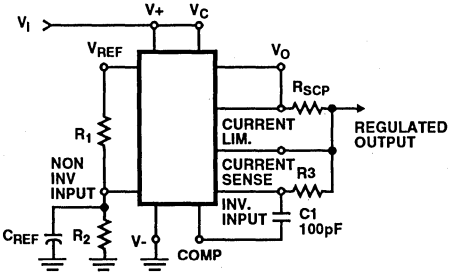


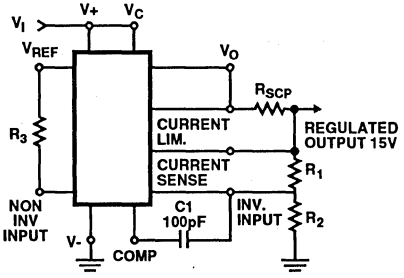
FIGURE 19. OUTPUT IMPEDANCE vs. FREQUENCY

Typical Application Circuits



Circuit Performance Data:
Regulated Output Voltage 5V
Line Regulation (ΔV_I= 3V) 0.5mV
Load Regulation (ΔI_L = 50mA) 1.5mV
Note: R3 = $\frac{R1\,R2}{R1 + r2}$ For Minimum Temperature Drift

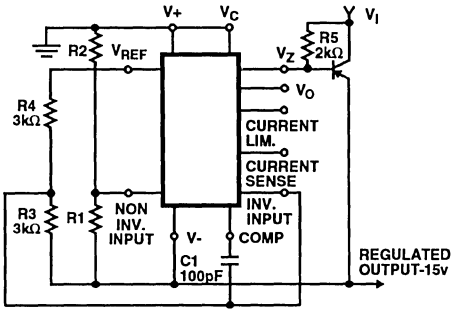
FIGURE 20. LOW VOLTAGE REGULATOR CIRCUIT (V_O = 2V TO 7V)



Circuit Performance Data:
Line Regulation (ΔV_I = 3V) 1.5mV
Load Regulation (ΔI_L = 50mA) 4.5mV
Note: R3 = $\frac{R1\,R2}{R1 + R2}$ For Minimum Temperature Drift
R3 May Be Eliminated For Minimum Component Count

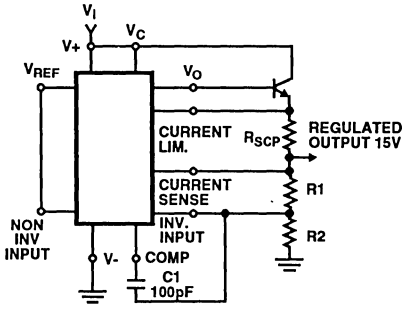
FIGURE 21. HIGH VOLTAGE REGULATOR CIRCUIT (V_O = 7V TO 37V)

Typical Application Circuits (Continued)



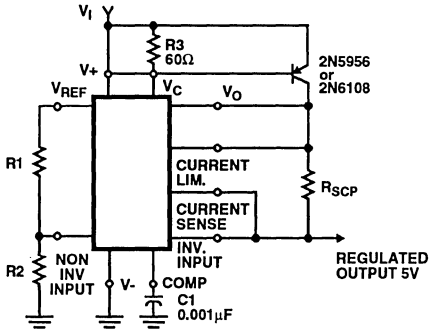
Circuit Performance Data:
Line Regulation (Δv_I = 3V) 1mV
Load Regulation (ΔI_L = 100mA) 2mV
Note: For Applications Employing the TO-5 Style Package and Where V_Z Is Required, An External; 6.2V Zener Diode Should be Connected in Series with V_O (Terminal 6).

FIGURE 22. NEGATIVE VOLTAGE REGULATOR CIRCUIT



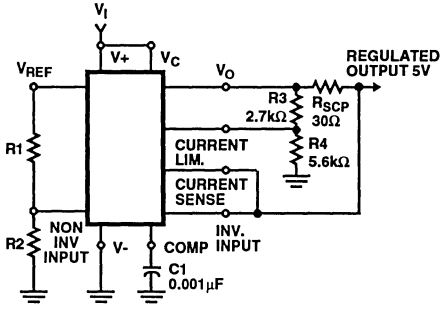
Circuit Performance Data:
Line Regulation (Δv_I= 3V) 1.5mV
Load Regulation (ΔI_L = 1A) 15mV

FIGURE 23. POSITIVE VOLTAGE REGULATOR CIRCUIT (WITH EXTERNAL n-p-n PASS TRANSISTOR)



Circuit Performance Data:
Line Regulation (Δv_I= 3V) 0.5mV
Load Regulation (ΔI_L = 1A) 5mV

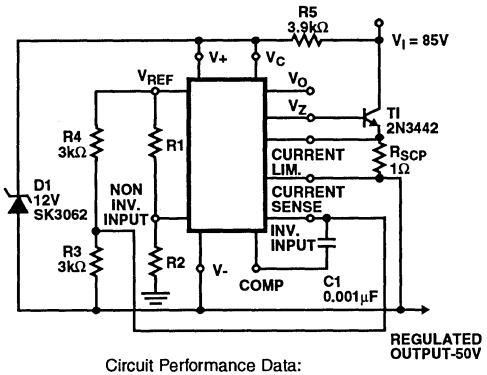
FIGURE 24. POSITIVE VOLTRAGE REGULATOR CIRCUIT (WITH EXTERNAL p-n-p PAS TRANSISTOR



Circuit Performance Data:
Line Regulation (Δv_I= 3V) 0.5mV
Load Regulation (ΔI_L = 10mA) 1mV
Short Circuit Current 20mA

FIGURE 25. FOLDBACK CURRENT LIMITING CIRCUIT

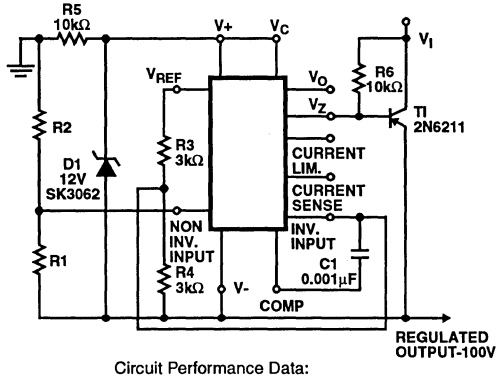
Typical Application Circuits (Continued)



Circuit Performance Data:
Line Regulation (ΔV_I= 20V) 15mV
Load Regulation (ΔI_L = 50mA) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

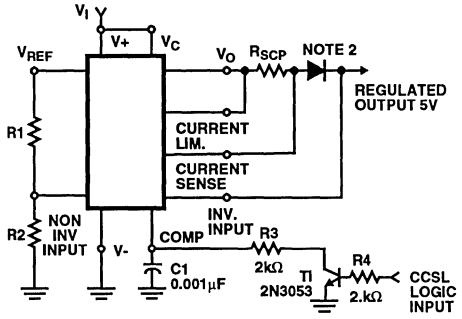
FIGURE 26. POSITIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
Line Regulation (ΔV_I= 20V) 30mV
Load Regulation (ΔI_L =100mA) 20mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6)

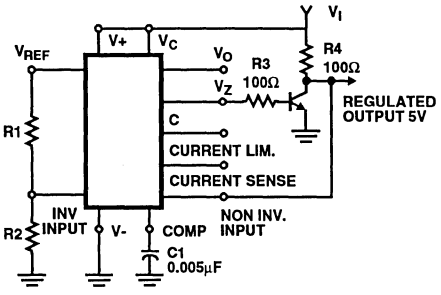
FIGURE 27. NEGATIVE FLOATING REGULATOR CIRCUIT



Circuit Performance Data:
Line Regulation (ΔV_I= 3V) 0.5mV
Load Regulation (ΔIL = 50mA) 1.5mV
Short Circuit Current 20mA

NOTE: 1. A current limiting transistor may be used for shutdown if current limiting is not required.
2. Add a diode if V_O > 10V.

FIGURE 28. REMOTE SHUTDOWN REGULATOR CIRCUIT WITH CURRENT LIMITING



Circuit Performance Data:
Line Regulation (Δv_I = 10V) 0.5mV
Load Regulation (ΔI_L = 100mA) 1.5mV

NOTE: For applications employing the TO-5 Style Package and where V_Z is required, an external 6.2V zener diode should be connected in series with V_O (terminal 6).

FIGURE 29. SHUNT REGULATOR CIRCUIT

HARRIS SEMICONDUCTOR

CA1523

Voltage Regulator Control Circuit For Variable Switching Regulator

May 1992

Features

- Operates up to 200kHz
- Pins ESD Protected
- Remote ON/OFF
- Slow Start with Reset
- Overcurrent Sensing
- Lower Peak Currents than PWM Regulator:
  - Less Prone to Magnetic Saturation

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA1523E	0°C to +70°C	14 Lead Plastic DIP

Description

The CA1523* monolithic silicon integrated circuit is a variable interval pulse regulator designed to provide the control circuitry for use in switching regulator circuits. It operates from 11 volts to 15 volts.

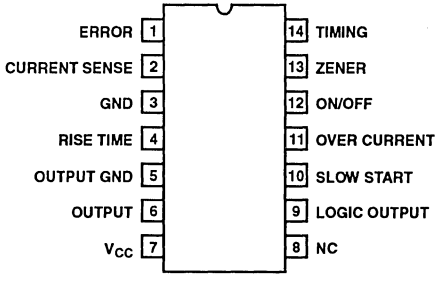
The regulator provides a single output drive capable of 300mA source/200mA sink. The maximum operating frequency is better than 200kHz. An attractive feature of the CA1523 is that the timing capacitor charge and discharge current is set up externally via a single resistor. The ratio of charge to discharge current is internally set at a maximum of 2 to 1 allowing simultaneous change in output pulse width with increased frequency at higher load. The pulse width variation at higher frequencies effectively compensates for the losses in magnetics and thereby increases the power supply efficiency at higher load end by as much as 20 percent.

The CA1523 is supplied in a 14-lead dual-in-line plastic package (E suffix).

* Formerly RCA Developmental Type No. TA11977

Pinout

14 LEAD PLASTIC DIP
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1785.1**

Absolute Maximum Ratings

DC Supply Voltage 15V
Supply Current:
$I_{6(MAX)}$ . . . . . ±50mA
$I_{6(MAX)}$, 1µs,1800pF Load . . . . . +300, -200 mA
Device Dissipation:
Up to T_A= 70°C 530mW
Above T_A = 70°C . . . . . Derate Linearly at 6.7 mW/°C

Ambient Temperature Range:
Operating . . . . . 0°C to +70°C
Storage . . . . . -55°C to +150°C
Lead Temperature (During Soldering):
At distance $^1/_{16}$ ± in. (1.59 ± 0.79mm) from
case for 10s max . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, Refer to condition shown in test circuit; V_7 = 13V, V_1 = 5.9V Unless Otherwise Specified

PARAMETERS	PIN	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
POWER SUPPLY, V_{CC} (PIN 7)						
Supply Voltage	7	-	9.5	13	-	V
Supply Current	7	V_{CC} = +13V	20	27	34	mA
Zener Voltage	13	-	7.8	8.4	8.9	V
OUTPUT PULSE (PIN 6)						
Maximum Pulse Width	6	Measured at 6V Threshold Level	5.5	6.5	7.5	µs
Minimum Pulse Width	6	Measured at 6V Threshold Level	2	3	4	µs
Output High Voltage	6	I_6 = 0mA, V_4 = 0V	11.1	12	12.6	V
Output Low Voltage	6	I_6 = 50mA, V_{12} = 0V	0.6	1	1.3	V
Rise Time	6	Measured at 1.8 and 10V Threshold Levels	250	600	1250	ns
Fall Time	6	Measured at 1.8 and 10V Threshold Levels	50	200	350	ns
ERROR VOLTAGE RANGE (PIN 1)						
Error Voltage Reference	1	Adjust R_T; Observe Pin 6 Min/Max Frequency Range	5.9	6.8	7.5	V
CHARGE CURRENT (PIN 14)						
Charge Current	14	Adjust R_T, V_1 = 7.5V; Set V_{14} = 0V, then V_{14} = 2.5V	190	220	250	µA
Discharge Current	14	Adjust R_T = 5.9V; Set V_{14} = 5.5V, then 5V	95	110	125	µA
Slow Start Discharge Current	14	Maintain V_{14} = 5V, V_{10} = 5.5V Set V_{10} = 5.5V, Measure I_{14} (Hi) Set V_{10} = 4V, Measure I_{14} (Lo) Limits = $\frac{I_{14}\text{ (Hi)} - I_{14}\text{ (Lo)}}{1.5}$	20	30	40	µA/V
LOGIC TESTS						
Discharge Voltage	10	Pin 12 = 1kΩ to GND	1.7	2.4	3.2	V
Output Inhibit Voltage	7	Increase V_7 until $V_9 \geq 2V$	7.9	8.4	9.1	V
Overcurrent Trip Voltage	11	V_{12} = 5V; V_{10} = 0V; Increase V_{11} until $V_9 \leq 0.5V$	1.1	1.25	1.4	V

Other Desirable Features

Other desirable features along with various circuit block function explanations are listed below.

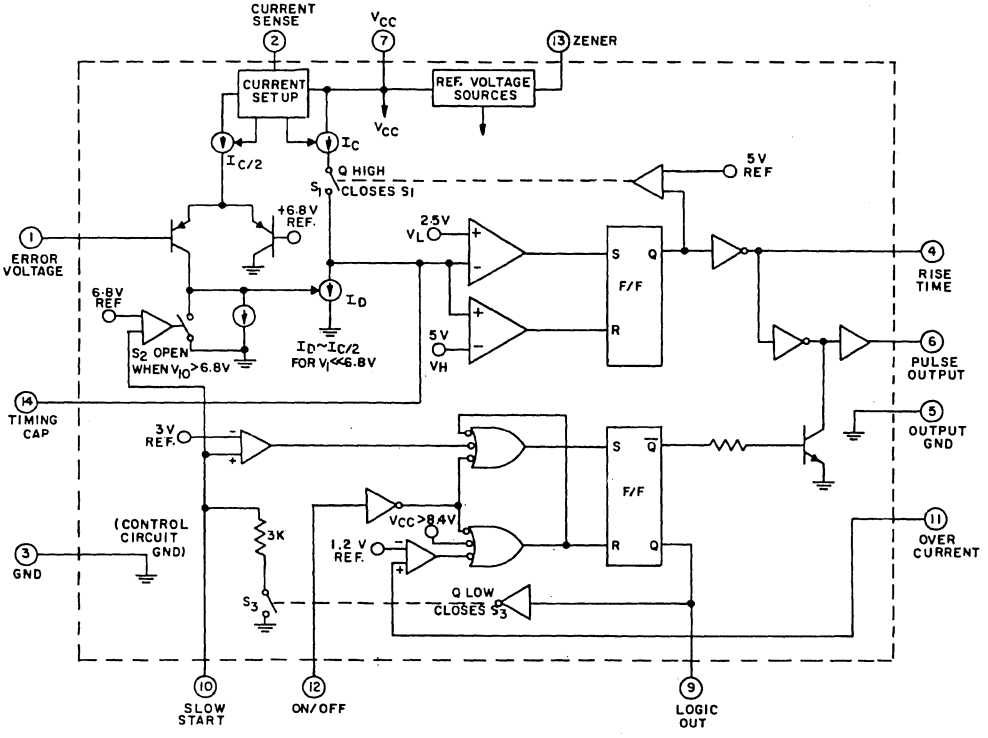
- The **Oscillator** is a sawtooth generator whose charge (rise) cycle determines the output pulse width and discharge which is continuously variable from very low to maximum of I_{CHARGE}.

  Charge $I_{CHARGE} = I_O - I_{DISCHARGE}$ giving 2 to 1 pulse-width control

  Discharge $I_{DISCHARGE}$ = approximately 0 to 1/2 I_O to frequency control

- **Pulse Shaping:** Applied to the oscillator output via RS Flip-Flop with parallel inhibit controlled by slow-start overcurrent sense, supply voltage monitor and ON/OFF functions.
- **Pulse Rise Time:** Modified to meet RFI requirements by external slow-down capacitor.
- **Slow Start with Reset:** Externally programmed against internal 3V reference. Reset is initiated upon Inhibit ensuring soft start at power up and restart.
- **Over Current Sense:** Internal stable thresholds of 1.2V.
- **Supply Voltage Monitors:** Locks out the drive until V_{SUPPLY} has reached 8-9V.
- **ON/OFF:** Activates regulator independent of raw DC.
- **Error Amplifier:** Compares output against a stable 6.8V internal reference and controls the discharge current sink on the timing capacitor.
- **Band-Gap:** Reference voltage (internal) provides temperature compensated 1.2V and 6.8V references.
- **Separate GND:** The power GND is separated from circuit ground for improved noise.
- **ESD Protection:** Pins are protected against ESD.

Block Diagram



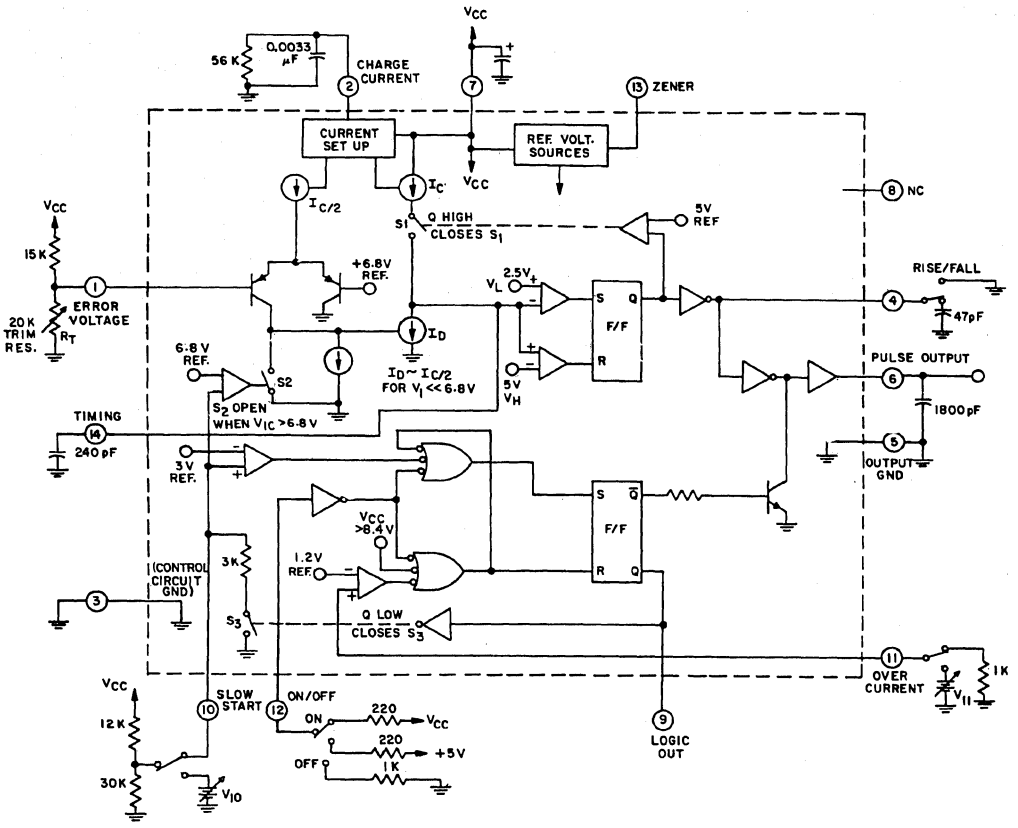


FIGURE 1. TEST CIRCUIT FOR THE CA1523

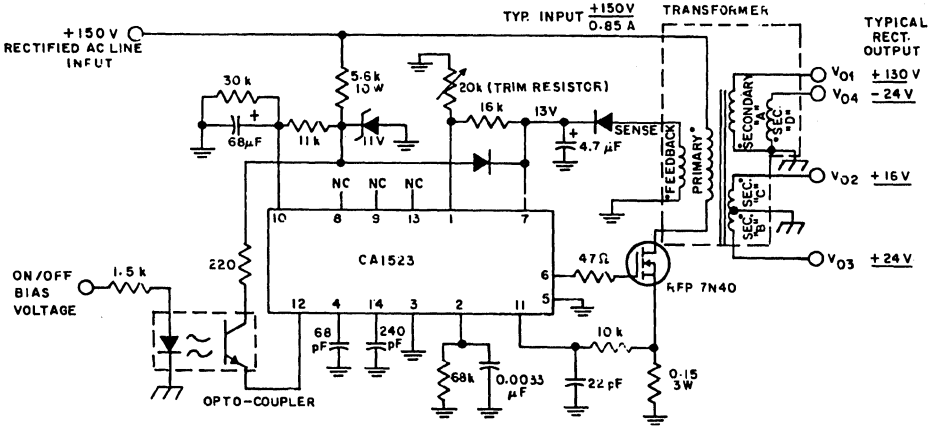


FIGURE 2. TYPICAL APPLICATION CIRCUIT OF THE CA1523

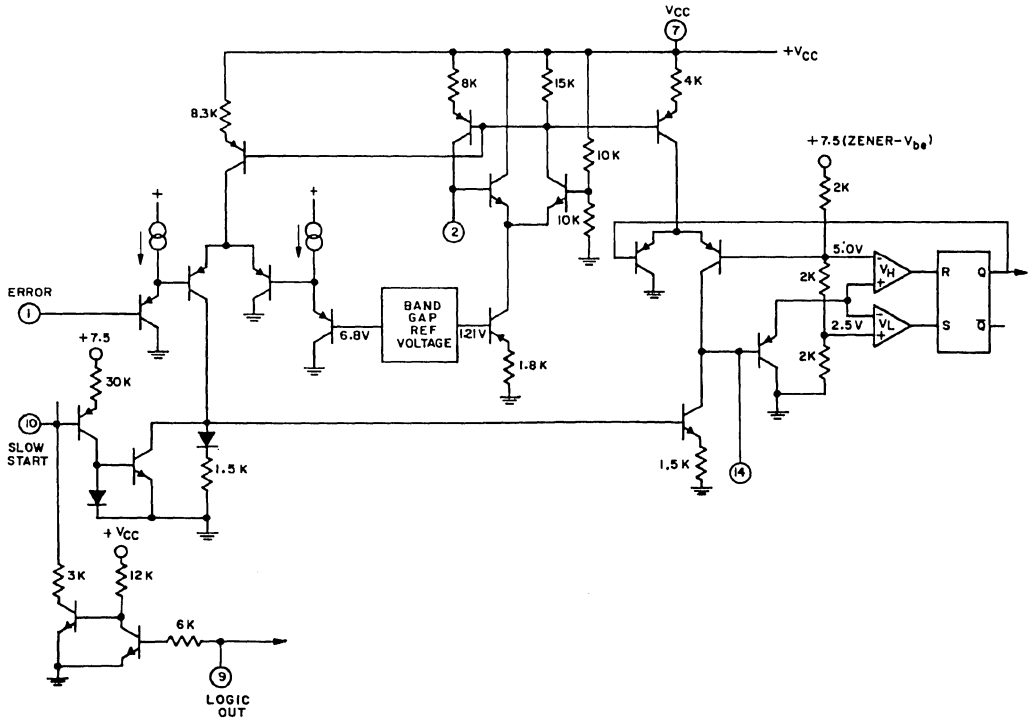


FIGURE 3. TIMING CIRCUIT FOR CA1523

HARRIS SEMICONDUCTOR

CA1524, CA2524 CA3524

Regulating Pulse Width Modulator

May 1992

Features

- Complete PWM Power Control Circuitry
- Separate Outputs for Single-Ended or Push-Pull Operation
- Line and Load Regulation..... 0.2% (Typ)
- Internal Reference Supply with 1% (Max) Oscillator and Reference Voltage Variation Over Full Temperature Range
- Standby Current of Less Than 10mA
- Frequency of Operation Beyond 100kHz
- Variable-Output Dead Time of 0.5μs to 5μs
- Low $V_{CE(sat)}$ Over the Temperature Range

Applications

- Positive and Negative Regulated Supplies
- Dual-Output Regulators
- Flyback Converters
- DC-DC Transformer-Coupled Regulating Converters
- Single-Ended DC-DC Converters
- Variable Power Supplies

Description

The CA1524, CA2524, and CA3524 are silicon monolithic integrated circuits designed to provide all the control circuitry for use in a broad range of switching regulator circuits.

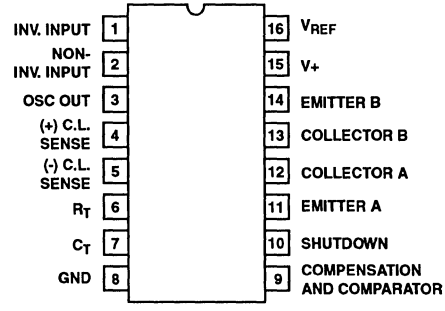
The CA1524, CA2524, and CA3524 have all the features of the industry types SG1524, SG2524, and SG3524, respectively. A block diagram of the CA1524 series is shown in Figure 1. The circuit includes a zener voltage reference, transconductance error amplifier, precision R-C oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches, and current-limiting and shutdown circuitry. This device can be used for switching regulators of either polarity, transformer-coupled dc-dc converter, transformerless voltage doublers, dc-ac power inverters, highly efficient variable power supplies, and polarity converter, as well as other power-control applications.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA1524E	-55°C to +125°C	16 Lead Plastic DIP
CA1524F	-55°C to +125°C	16 Lead Ceramic DIP
CA2524E	0°C to +70°C	16 Lead Plastic DIP
CA2524F	0°C to +70°C	16 Lead Ceramic DIP
CA3524E	0°C to +70°C	16 Lead Plastic DIP
CA3524F	0°C to +70°C	16 Lead Ceramic DIP
CA3524H	0°C to +70°C	DICE

Pinout

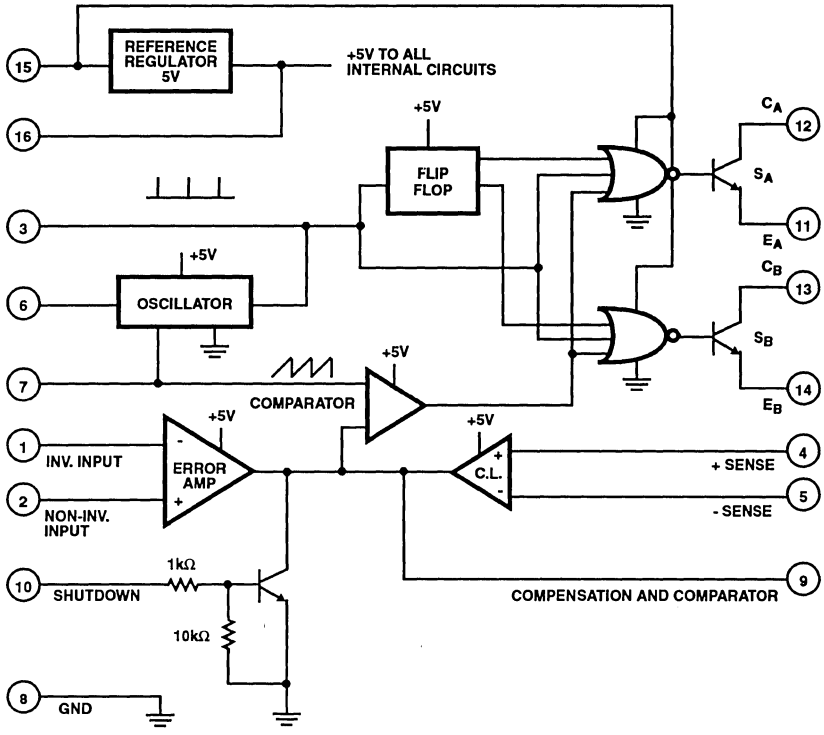
16 LEAD DUAL-IN-LINE PACKAGE
TOP VIEW



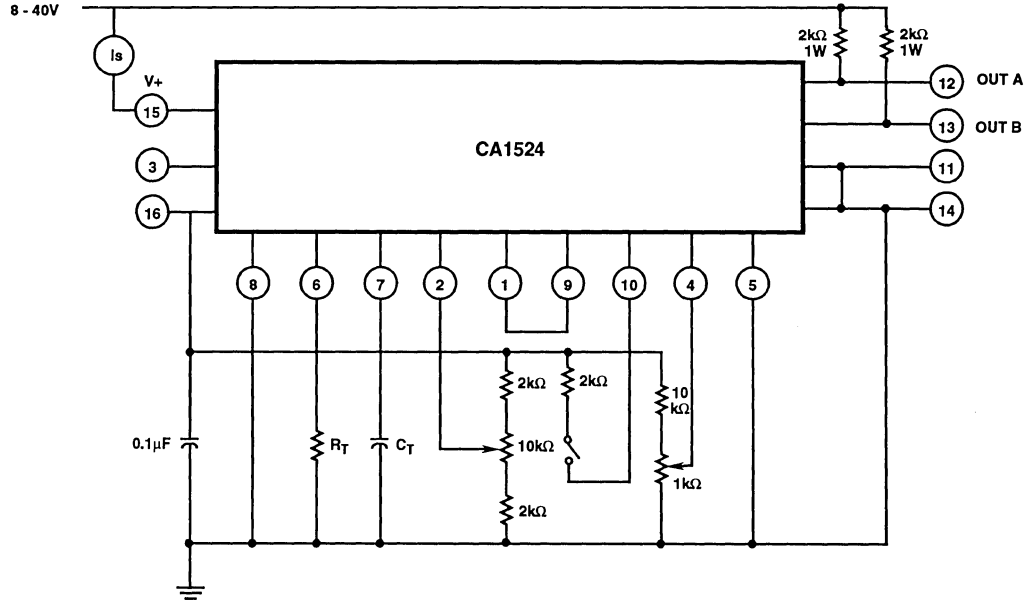
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1239.2**

Functional Block Diagram



Test Circuit



Absolute Maximum Ratings

Input Voltage (Between V_{IN} and GND Terminals) 40V
Operating Voltage Range (V_{IN} to GND) ..... 8 to 40V
Output Current Each Output:
(Terminal 11, 12 or 13, 14) 100mA
Output Current (Reference Regulator) 50mA
Oscillator Charging Current 5mA

Device Dissipation:
Up to T_A = 25°C 1W
Above T_A = 25°C ..... Derate linearly 8mW/°C
Operating Temperature Range ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

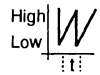
T_A = -55°C to +125°C for CA1524, 0°C to +70°C for the CA2524 and CA3524; V+ = 20V and f = 20kHz, Unless Otherwise Stated.

PARAMETER	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE SECTION								
Output Voltage		4.8	5	5.2	4.6	5	5.4	V
Line Regulation	V+ = 8 to 40V	-	10	20	-	10	30	mV
Load Regulation	I_L = 0 to 20mA	-	20	50	-	20	50	mV
Ripple Rejection	f = 120Hz, T_A = 25°C	-	66	-	-	66	-	db
Short Circuit Current Limit	V_{REF} = 0, T_A = 25°C	-	100	-	-	100	-	mA
Temperature Stability	Over Operating Temperature Range	-	0.3	1	-	0.3	1	%
Long Term Stability	T_A = 25°C	-	20	-	-	20	-	mV/khr
OSCILLATOR SECTION								
Maximum Frequency	C_T = 0.001µF, R_T = 2KΩ	-	300	-	-	300	-	kHz
Initial Accuracy	R_T and C_T Constant	-	5	-	-	5	-	%
Voltage Stability	V+ = 8 to 40V, T_A = 25°C	-	-	1	-	-	1	%
Temperature Stability	Over Operating Temperature Range	-	-	2	-	-	2	%
Output Amplitude	Terminal 3, T_A = 25°C	-	3.5	-	-	3.5	-	V
Output Pulse Width (Pin 3)	C_T = 0.01µF, T_A = 25°C	-	0.5	-	-	0.5	-	µs
Ramp Voltage Low (Note 1)	Pin 7	-	0.6	-	-	0.6	-	V
Ramp Voltage High (Note 1)	Pin 7	-	3.5	-	-	3.5	-	V
Capacitor Charging Current Range	Pin 7 (5-2 V_{BE})/R_T	0.03	-	2	0.03	-	2	mA
Timing Resistance Range	Pin 6	1.8	-	120	1.8	-	120	kΩ
Charging Capacitor Range	Pin 7	0.001	-	0.1	0.001	-	0.1	µF
Dead Time Expansion Capacitor on Pin 3 (when a small osc. cap is used)	Pin 3	100	-	1000	100	-	1000	pF
ERROR AMPLIFIER SECTION								
Input Offset Voltage	V_{CM} = 2.5V	-	0.5	5	-	2	10	mV
Input Bias Current	V_{CM} = 2.5V	-	1	10	-	1	10	µA
Open Loop Voltage Gain		72	80	-	60	80	-	dB
Common Mode Voltage	T_A = 25°C	1.8	-	3.4	1.8	-	3.4	V
Common Mode Rejection Ratio	T_A = 25°C	-	70	-	-	70	-	dB
Small Signal Bandwidth	A_V = 0dB, T_A = 25°C	-	3	-	-	3	-	MHz
Output Voltage	T_A = 25°C	0.5	-	3.8	0.5	-	3.8	V

Electrical Characteristics T_A = -55°C to +125°C for CA1524, 0°C to +70°C for the CA2524 and CA3524; V+ = 20V and f = 20kHz, Unless Otherwise Stated. (Continued)

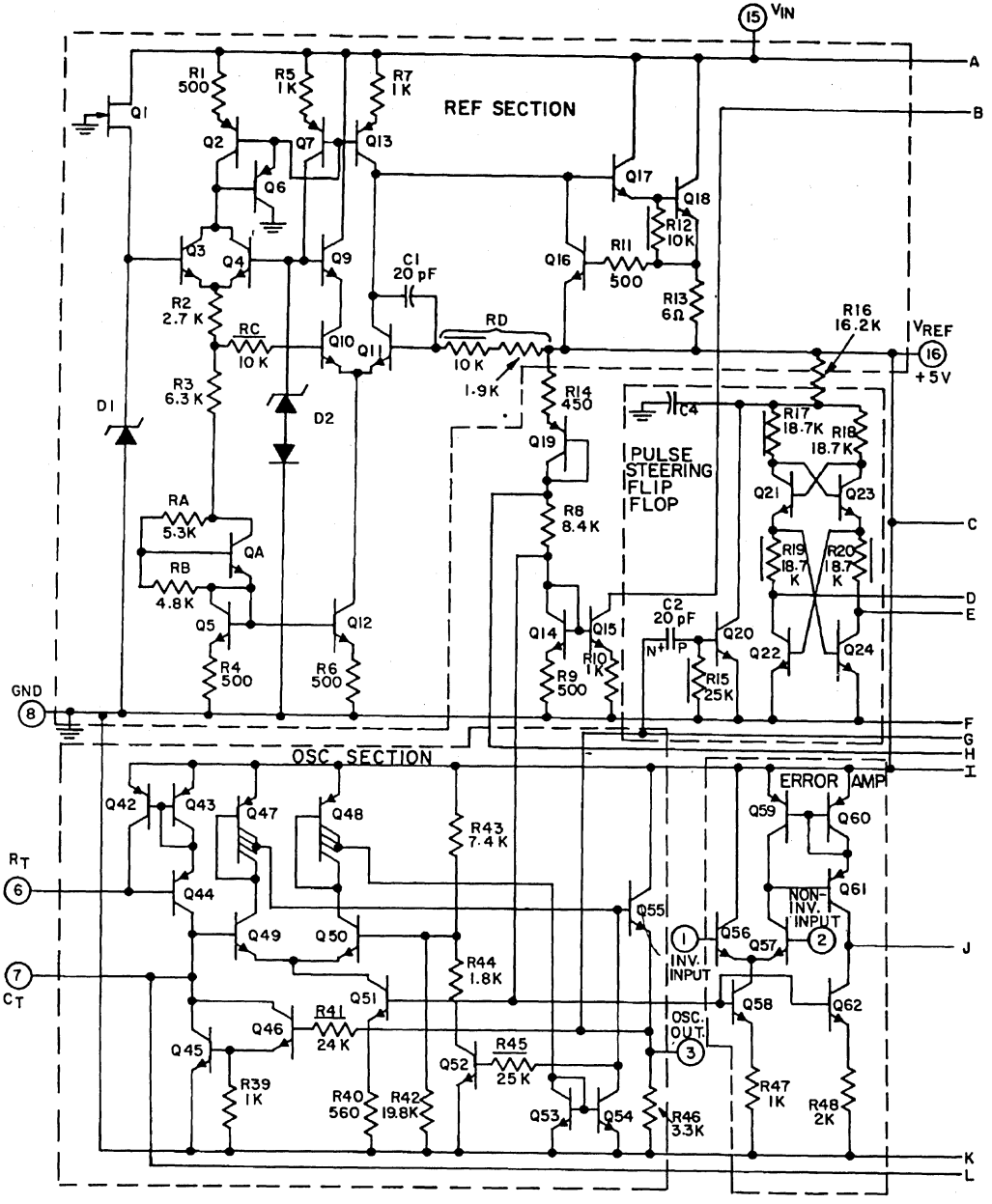
PARAMETER	TEST CONDITIONS	LIMITS						UNITS
		CA1524, CA2524			CA3524			
		MIN	TYP	MAX	MIN	TYP	MAX	
Amplifier Pole		-	250	-	-	250	-	Hz
Pin 9 Shutdown Current	External Sink	-	200	-	-	200	-	µA
COMPARATOR SECTION								
Duty Cycle	% Each Output On	0	-	45	0	-	45	%
Input Threshold	Zero Duty Cycle	-	1	-	-	1	-	V
Input Threshold	Max. Duty Cycle	-	3.5	-	-	3.5	-	V
Input Bias Current		-	1	-	-	1	-	µA
CURRENT LIMITING SECTION								
Sense voltage for 25% Output Duty Cycle	Terminal 9 = 2V with Error Amplifier Set for Max Out, T_A = 25°C	190	200	210	180	200	220	mV
Sense Voltage T.C.		-	0.2	-	-	0.2	-	mV/°C
Common Mode Voltage		-1	-	+1	-1	-	+1	V
Rolloff Pole of R51 C3 + Q64		-	300	-	-	300	-	Hz
OUTPUT SECTION (EACH OUTUT)								
Collector-Emitter Voltage		40	-	-	40	-	-	V
Collector Leakage Current	V_{CE} = 40V	-	0.1	50	-	0.1	50	µA
Saturation Voltage	V+ = 40V, I_C = 50mA	-	0.8	2	-	0.8	2	V
Emitter Output Voltage	V+ = 20V	17	18	-	17	18	-	V
Rise Time	R_C = 2KΩ, T_A = 25°C	-	0.2	-	-	0.2	-	µs
Fall Time	R_C = 2KΩ, T_A = 25°C	-	0.1	-	-	0.1	-	µs
Total Standby Current: (Note 2) I_S	V+ = 40V	-	4	10	-	4	10	mA

NOTES:

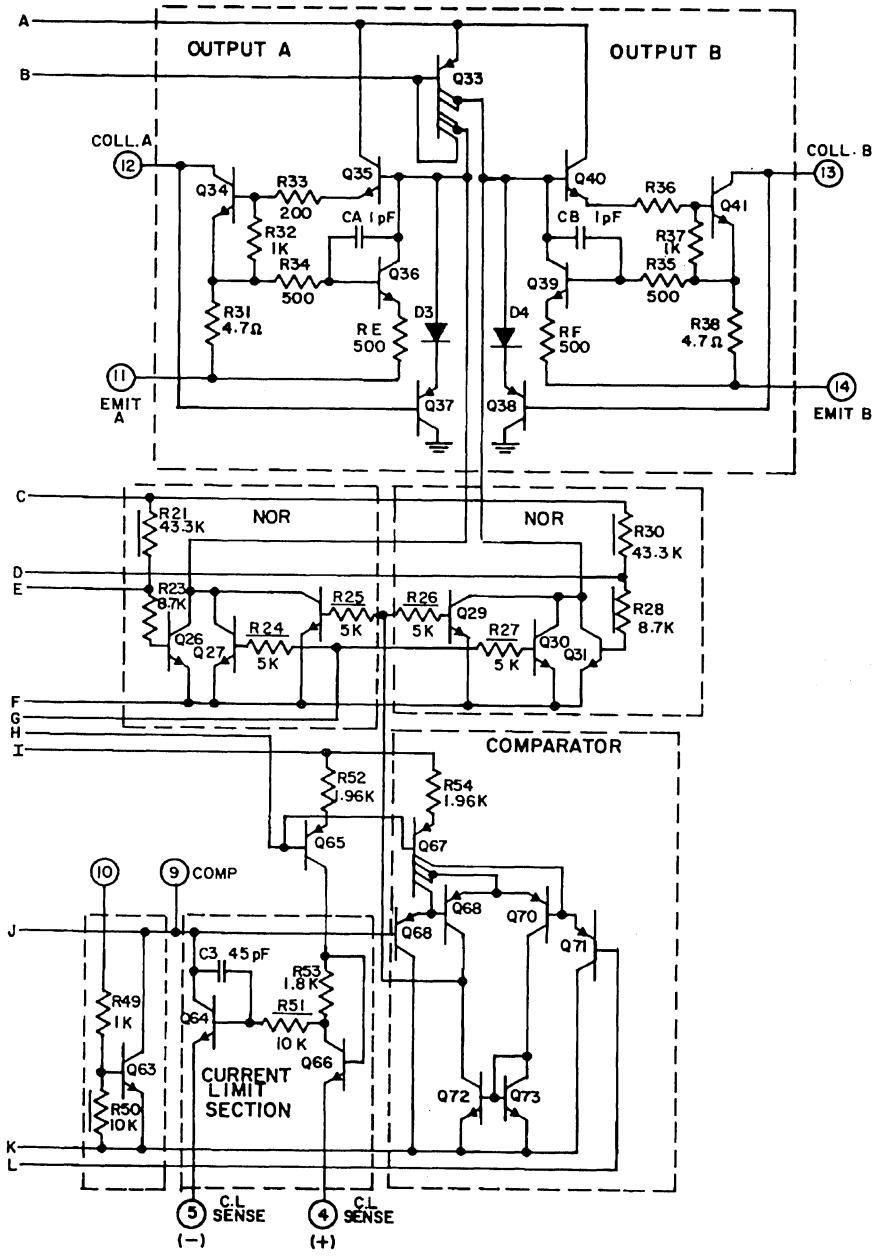
1. Ramp voltage at Pin 7 

where t = OSC period in microseconds
$t \cong R_T C_T$ with C_T in microfarads and R_T in ohms.
Output frequency at each output transistor is half OSC frequency when each output is used separately and is equal to the OSC frequency when each output is connected in parallel.
2. Excluding oscillator charging current, error and current limit dividers, and with outputs open.

Schematic Diagram



Schematic Diagram (Continued)



Circuit Description

Voltage Reference Section

The CAI524 series contains an internal series voltage regulator employing a zener reference to provide a nominal 5-volt output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal I6 and is capable of supplying up to 50mA output current.

Figure 1 shows the temperature variation of the reference voltage with supply voltages of 8 to 40 volts and load currents up to 20mA. Load regulation and line regulation curves are shown in Figures 2 and 3, respectively.

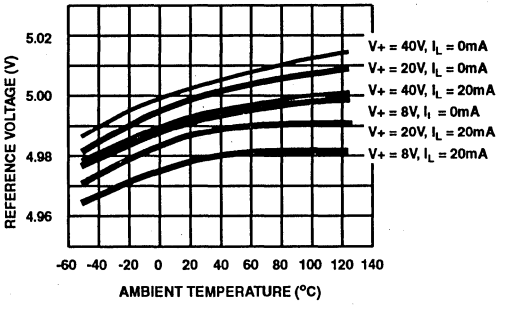


FIGURE 1. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

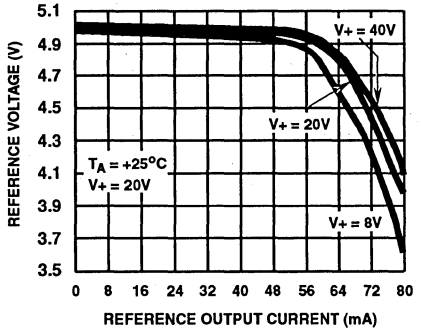


FIGURE 2. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF REFERENCE OUTPUT CURRENT

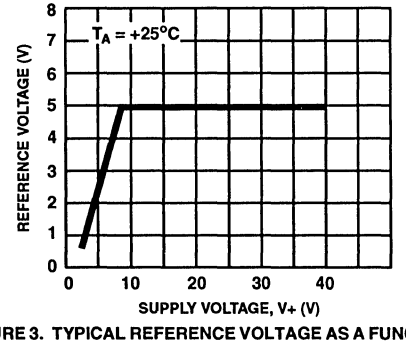


FIGURE 3. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has a value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to $(5\text{-}2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30pA to 2mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5µs to 5µs for a capacitor range of 0.001 to 0.1µF. The pulse has two internal uses: as a dead-time control of blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which controls the switching of the output between the two output channels. The output dead-time relationship is shown in Figure 4. Pulse widths less than 0.5µs may allow false triggering of one output by removing the blanking pulse prior to a stable state in the flip-flop.

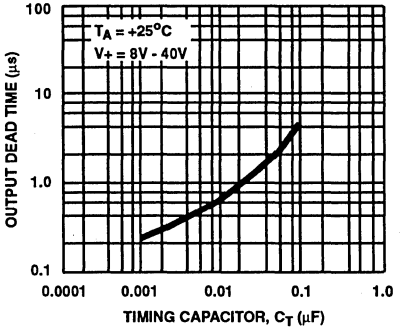


FIGURE 4. TYPICAL OUTPUT STAGE DEAD TIME AS A FUNCTION OF TIMING CAPACITOR VALUE

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100pF but no greater than 1000pF, from terminal 3 to ground. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2-KΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_TC_T$, where R_T is in ohms, C_T is in µF, and t is in µs. Excess lead lengths, which produce stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals. Figure 5 provides curves for selecting these values for a wide range of oscillator periods. For series regulator applications, the two outputs can be connected in parallel for an effective 0-90% duty cycle with the output stage frequency the same as the oscillator frequency. Since the outputs are separate, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0-45%

and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Figure 7. To synchronize two or more CAI524's, one must be designated as master, with R_T C_T set for the correct period. Each of the remaining units (slaves) must have a C_T of 1/2 the value used in the master and approximately a 1010 longer R_TC_T period than the master. Connecting terminal 3 together on all units assures that the master output pulse, which occurs first and has a wider pulse width, will reset the slave units.

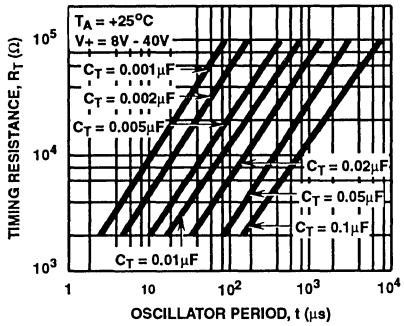


FIGURE 5. TYPICAL OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

Error Amplifier Section

The error amplifier consists of a differential pair (Q56,Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{OUT}, terminal 9, is very high (≅ 5MΩ).

The gain is:

$$A_V = g_mR = 8\ I_C\ R/2KT = 10^4,$$

$$\text{where } R = \frac{R_{OUT}\ R_L}{R_{OUT} + R_L},\ R_L = \infty,\ A_V \propto 10^4$$

Since R_{OUT} is extremely high, the gain can be easily reduced from a nominal 10^4 (80dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Figure 6.

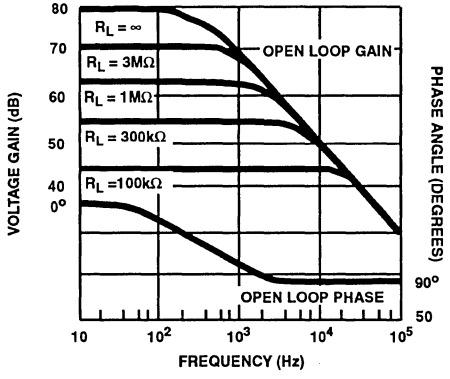


FIGURE 6. OPEN-LOOP ERROR AMPLIFIER RESPONSE CHARACTERISTICS.

The output amplifier terminal is also used to compensate the system for ac stability. The frequency response and phase shift curves are shown in Figure 7. The uncompensated amplifier has a single pole at approximately 250Hz and a unity gain cross-over at 3MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000-pF capacitor and a variable series 50-KΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200μA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Figure 8. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

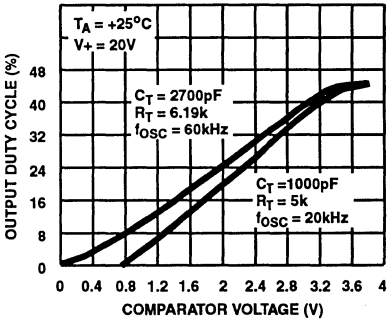


FIGURE 7. TYPICAL DUTY CYCLE AS A FUNCTION OF COMPARATOR VOLTAGE (AT TERMINAL 9).

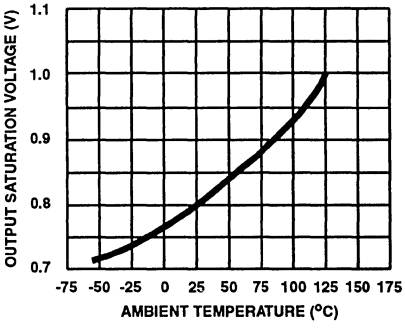


FIGURE 8. TYPICAL OUTPUT SATURATION VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE.

Output Section

The CA1524 series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor has antisaturation circuitry that enables a fast transient response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100mA for each output and 100mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figures 8 and 9, respectively. There area number of output configurations possible in the application of the CA1524 to voltage regulator circuits which fall into three basic classifications:

1. Capacitor-diode coupled voltage multipliers
2. Inductor-capacitor single-ended circuits
3. Transformer-coupled circuits

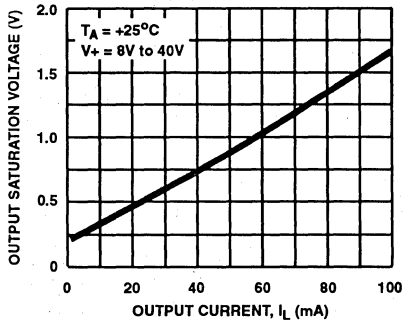


FIGURE 9. TYPICAL OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

Device Application Suggestions

For higher currents, the circuit of Figure 10 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5-volt supply by connecting both terminals 15 and 16 to the input voltage, which must not exceed 6 volts.

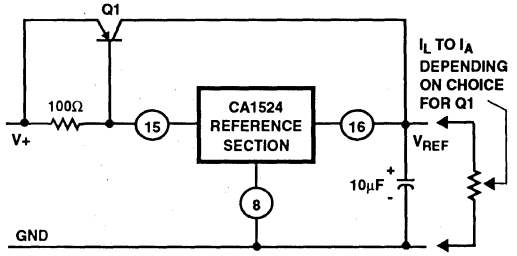


FIGURE 10. CIRCUIT FOR EXPANDING THE REFERENCE CURRENT CAPABILITY

The internal 5-volt reference can be used for conventional regulator applications if divided as shown in Figure 11. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

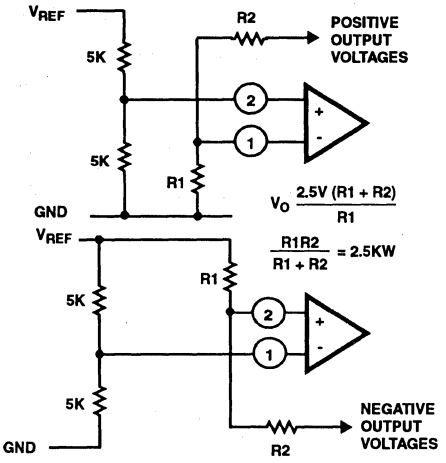
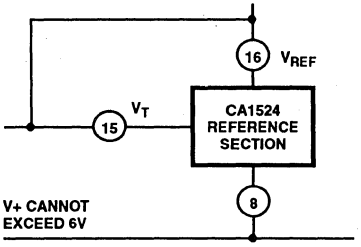


FIGURE 11. ERROR AMPLIFIER BIASING CIRCUITS



NOTE: V+ Should Be in the 5V Range And Must Not Exceed 6V

FIGURE 12. CIRCUIT TO ALLOW EXTERNAL BYPASS OF THE REFERENCE REGULATION

To provide an expansion of the dead time without loading the oscillator, the circuit of Figure 13 may be used.

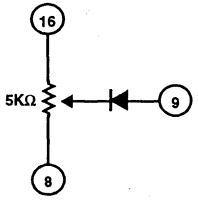


FIGURE 13. CIRCUIT FOR EXPANSION OF DEAD TIME, WITHOUT USING A CAPACITOR ON PIN 3 OR WHEN A LOW VALUE OSCILLATOR CAPACITOR IS USED

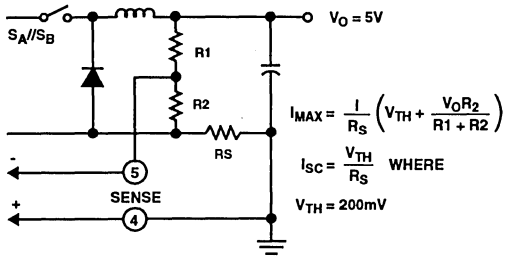
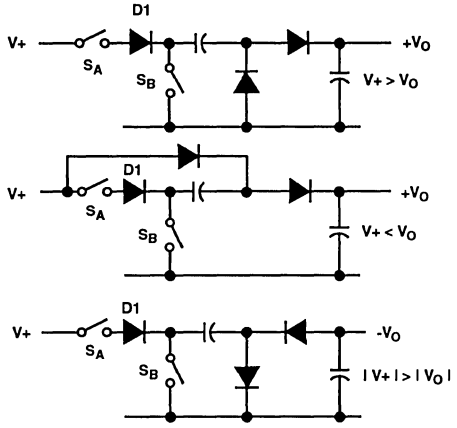


FIGURE 14. FOLDBACK CURRENT-LIMITING CIRCUIT USED TO REDUCE POWER DISSIPATION UNDER SHORTED OUTPUT CONDITIONS



NOTE: Diode D1 Is Necessary To Prevent Reverse Emitter-Base Breakdown of Transistor Switch S_A

FIGURE 15. CAPACITOR-DIODE COUPLED VOLTAGE MULTIPLIER OUTPUT STAGES

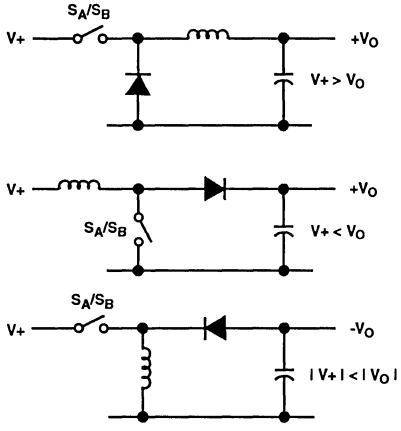


FIGURE 16. SINGLE-ENDED INDUCTOR CIRCUITS WHERE THE TWO OUTPUTS OF THE 1524 ARE CONNECTED IN PARALLEL

TABLE 1. INPUT vs. OUTPUT VOLTAGE, AND FEEDBACK RESISTOR VALUES FOR I_L=40mA (FOR CAPACITOR-DIODE OUTPUT CIRCUIT IN FIGURE 18)

V_O (V)	R_2 (KΩ)	V+ (Min.) (V)
-0.5	6	8
-2.5	10	9
-3	11	10
-4	13	11
-5	15	12
-6	17	13
-7	19	14
-8	21	15
-9	23	16
-10	25	17
-11	27	18
-12	29	19
-13	31	20
-14	33	21
-15	35	22
-16	37	23
-17	39	24
-18	41	25
-19	43	26
-20	45	27

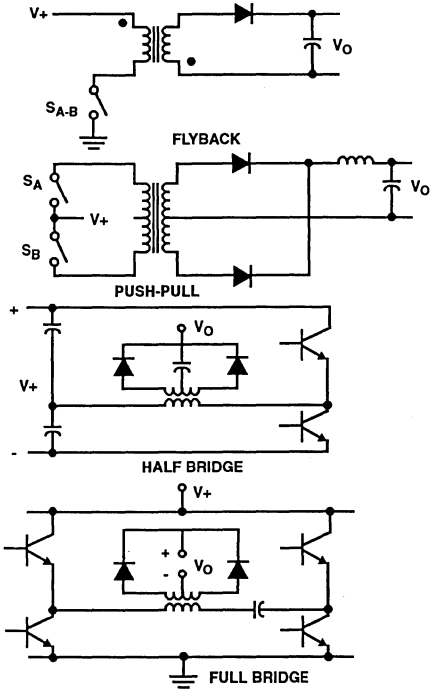


FIGURE 17. TRANSFORMER-COUPLED OUTPUTS

Applications*

A capacitor-diode output filter is used in Figure 19 to convert +15Vdc to -5Vdc at output currents up to 50mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table 1 gives the required minimum input voltage and feedback resistor values, R2, for an output voltage.

Capacitor-Diode Output Circuit

A capacitor-diode output filter is used in Figure18 to convert +15Vdc to -5Vdc at output currents up to 50mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table 1 gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5V to -20V with an output current of 40mA.

Single-Ended Switching Regulator

The CA1524 in the circuit of Figure 19 has both output stages connected in parallel to produce an effective 0% - 90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 and R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9 amperes by the sense resistor R3.

* For additional information on the application of this device and a further explanation of the circuits below, see RCA Application Note ICAN-691 5 "Application of the CA1524 series PWM IC".

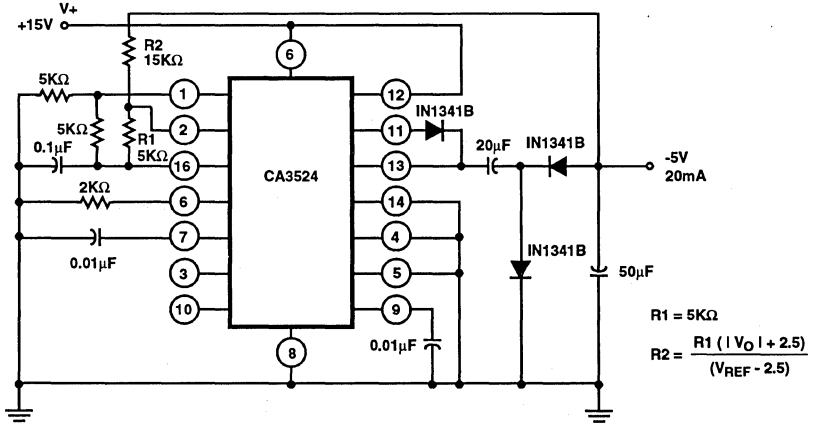


FIGURE 18. CAPACITOR-DIODE OUTPUT CIRCUIT

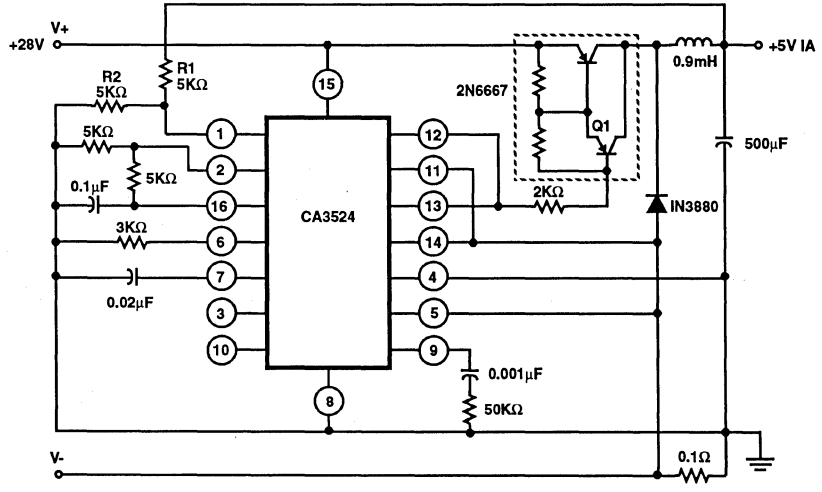


FIGURE 19. SINGLE-ENDED LC SWITCHING REGULATOR CIRCUIT

Flyback Converter

Figure 20 shows a flyback converter circuit for generating a dual 15-volt output at 20mA from a 5-volt regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft-start circuit.

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Figure 21. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low-Frequency Pulse Generator

Figure 22 shows the CA1524 being used as a low-frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5-V (or 2.5-V) pulse of 0% - 45% (or 0% - 90%) on time is possible over a frequency range of 150 to 500Hz. Switch S1 is used to go from a 5-V output pulse (S1 closed) to a 2.5-V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75Hz to 250Hz, respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0%-90% with the output frequency range from 150 to 500Hz. The frequency is adjusted by R1; R2 controls duty cycle.

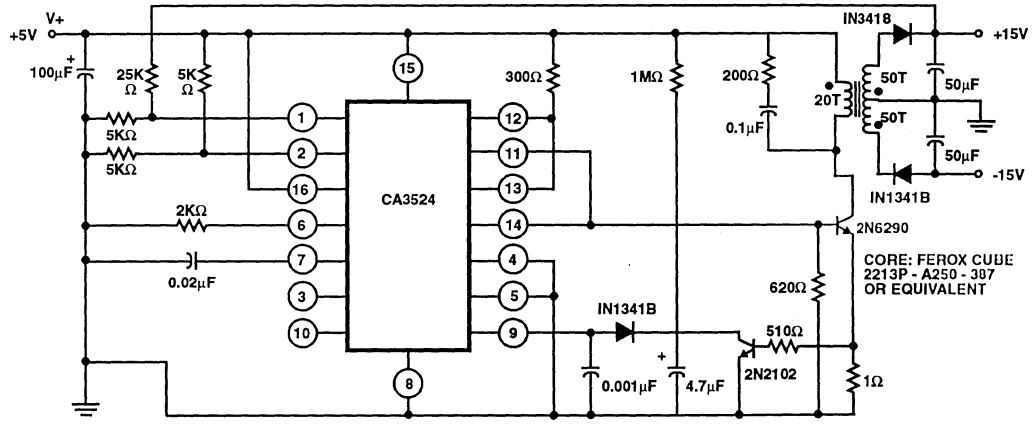


FIGURE 20. FLYBACK CONVERTER CIRCUIT

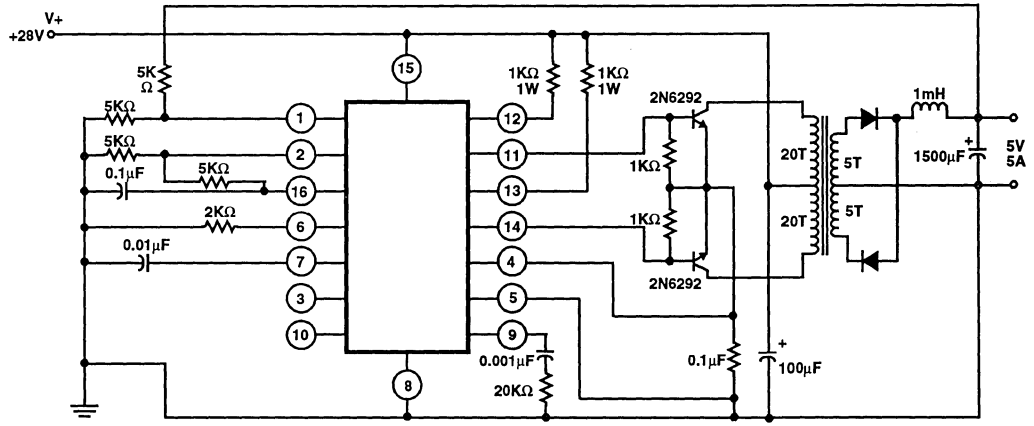
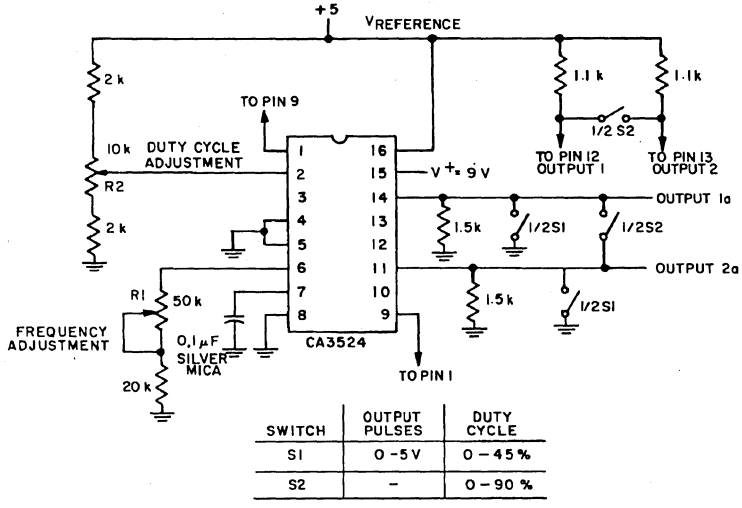


FIGURE 21. PUSH-PULL TRANSFORMER-COUPLED CONVERTER



SWITCH	OUTPUT PULSES	DUTY CYCLE
S1	0 -5 V	0 – 45 %
S2	-	0 – 90 %

FIGURE 22. LOW-FREQUENCY PULSE GENERATOR

The Variable Switcher

The circuit diagram of the CA1524, used as a variable output voltage power supply is shown in Figure 23. By connecting the two output transistors in parallel, the duty cycle is doubled, i.e., 0% - 90%. As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage.

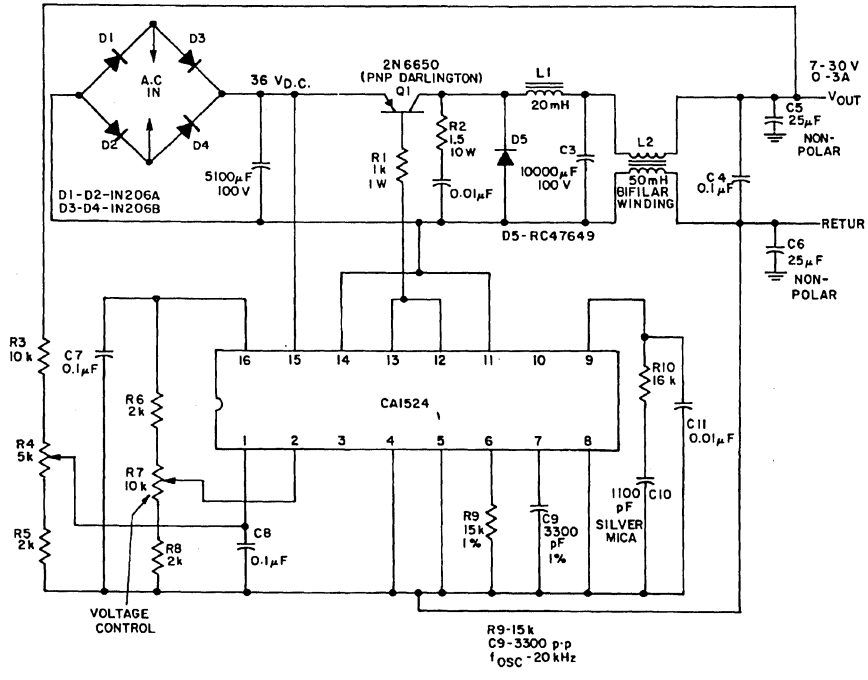


FIGURE 23. THE CA1524 USED AS A 0-5A, 7-30 V LABORATORY SUPPLY

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figures 24 and 25 uses half (Q2) of the CA1524 output in a low-voltage switching regulator (2.2V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5-volt internal regulator and a wide operating range of 8 to 40 volts, a single 9-volt battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse-width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge-type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the ac amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 ac amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a dc voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

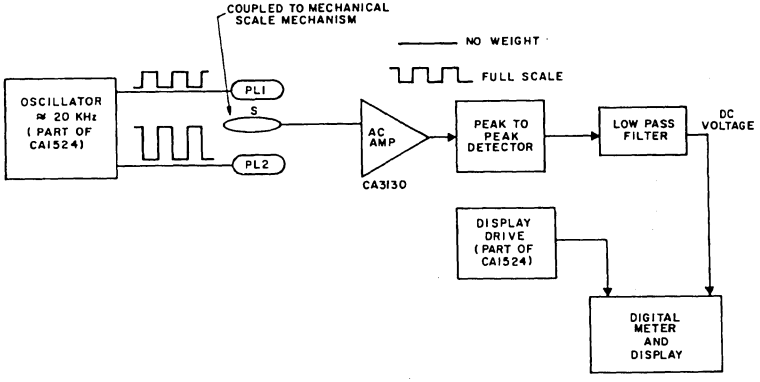


FIGURE 24. BASIC DIGITAL READOUT SCALE

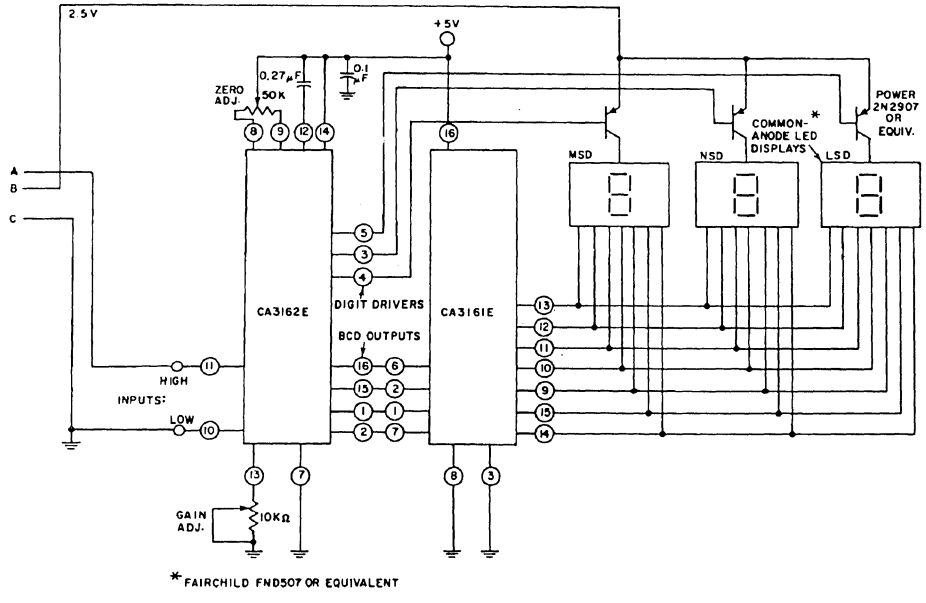


FIGURE 25. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE (CONT'D)

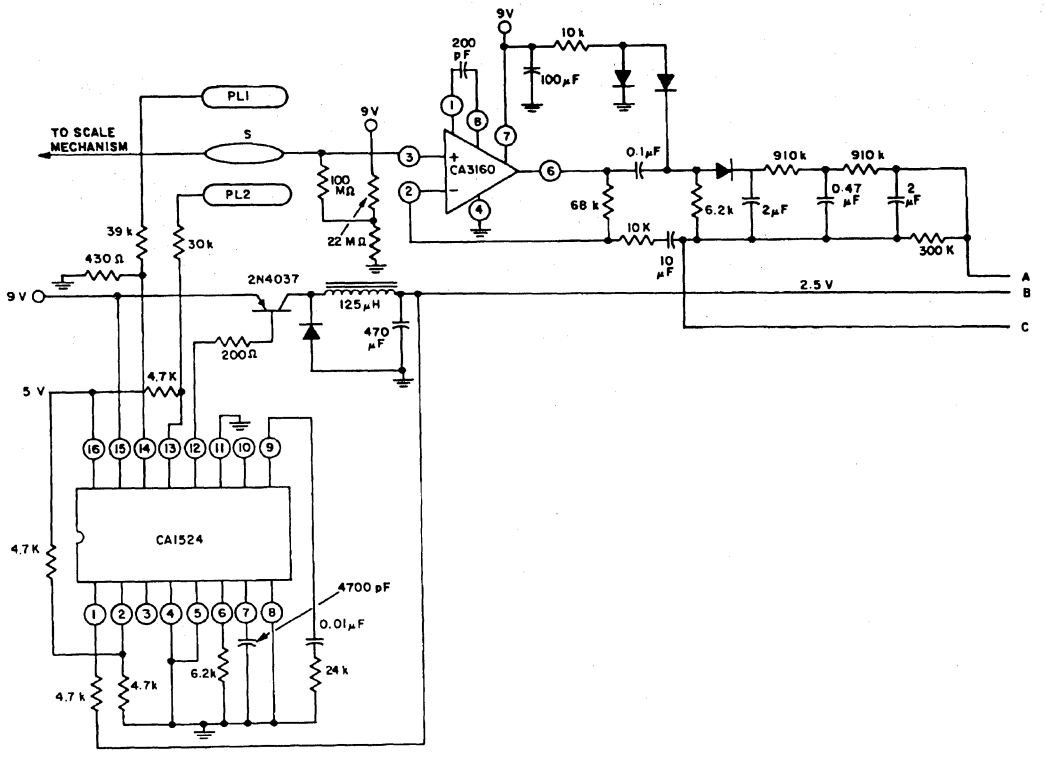
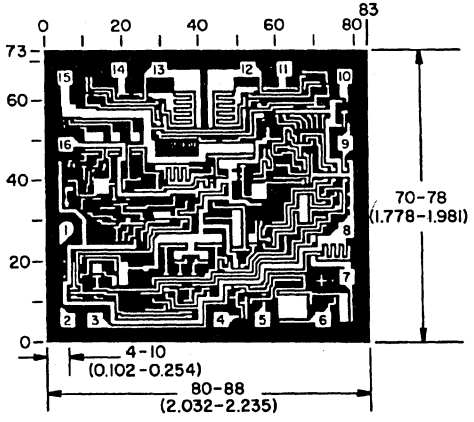


FIGURE 26. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE



DIMENSIONS AND PAD LAYOUT FOR CA3524RH CHIP

NOTE: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch). The layout represents a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

HARRIS SEMICONDUCTOR

CA3085, CA3085A CA3085B

Positive Voltage Regulators from 1.7V to 46V at Currents Up to 100mA

May 1992

Features

- Up to 100mA Output Current
- Input and Output Short-Circuit Protection
- Load and Line Regulation 0.025%
- Pin Compatible with LM100 Series
- Adjustable Output Voltage

Applications

- Shunt Voltage Regulator
- Current Regulator
- Switching Voltage Regulator
- High-Current Voltage Regulator
- Combination Positive and Negative Voltage Regulator
- Dual Tracking Regulator

TYPE	V_{IN} RANGE V	V_{OUT} RANGE V	MAX I_{OUT} mA	MAX LOAD REGULATION $\%V_{OUT}$
CA3085	7.5 to 30	1.8 to 26	12*	0.1
CA3085A	7.5 to 40	1.7 to 36	100	0.15
CA3085B	7.5 to 50	1.7 to 46	100	0.15

* This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

Description

The CA3085, CA3085A, and CA3085B are silicon monolithic integrated circuits designed specifically for service as voltage regulators at output voltages ranging from 1.7V to 46V at currents up to 100 milliamperes.

A block diagram of the CA3085 Series is shown. The diagram shows the connecting terminals that provide access to the regulator circuit components. The voltage regulators provide important features such as: frequency compensation, short-circuit protection, temperature-compensated reference voltage, current limiting, and booster input. These devices are useful in a wide range of applications for regulating high-current, switching, shunt, and positive and negative voltages. They are also applicable for current and dual-tracking regulation.

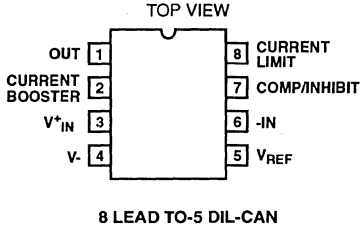
The CA3085A and CA3085B have output current capabilities up to 100mA and the CA3085 up to 12mA without the use of external pass transistors. However, all the devices can provide voltage regulation at load currents greater than 100mA with the use of suitable external pass transistors. The CA3085 Series has an unregulated input voltage ranging from 7.5V to 30V (CA3085), 7.5V to 40V (CA3085A), and 7.5V to 50V (CA3085B) and a minimum regulated output voltage of 26V (CA3085), 36V (CA3085A), and 46V (CA3085B).

Ordering Information

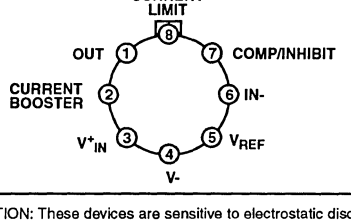
PART NUMBER	TEMPERATURE	PACKAGE
CA8085, A, B	-55°C to +125°C	8 Lead TO-5
CA3085S, AS, BS	-55°C to +125°C	8 Lead TO-5
CA3085E, AE, BE	-55°C to +125°C	8 Lead TO-5 "DIL-CAN"
CA3085H	+25°C	Die Form

Pinouts

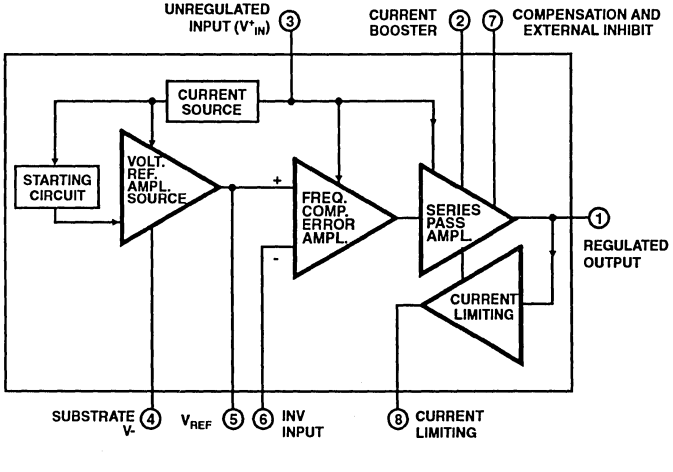
8 LEAD PLASTIC DIP
TOP VIEW



8 LEAD TO-5 DIL-CAN
8 LEAD TO-5 STYLE
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 491.2

Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Unregulated Input Voltage
CA3085 . . . . . 30V
CA3085A 40V
CA3085B 50V
Storage Temperature Range . . . . . -65°C to +150°C
Junction Temperature . . . . . +175°C
Lead Temperature (Soldering 10s) . . . . . +265°C

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	15°C/W

Maximum Package Power Dissipation
Plastic Mini-DIP (Without Heat Sink)
Up to T_A = 55°C 630mW
Above T_A = 55°C . . . . . Derate Linearly at 6.67mW/°C
TO-5 Package (With Heat Sink)
Up to T_C = 55°C 1.6W
Above T_C = 55°C . . . . . Derate Linearly at 16.7mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +1.7V to +46V
Operating Temperature Range . . . . . -55°C to +125°C

Maximum Voltage Ratings

The following chart gives the range of voltages which can be applied to the terminal listed verticaly with respect to the terminals listed horizontally. For example, the voltage range between vertical Terminal Number 7 and horizontal Terminal Number 1 is +3 to -10 volts.

TERMINAL NUMBER	5	6	7	8	1	2	3	4
5	-	+5 -5	Note 1	Note 1	Note 1	Note 1	Note 1	+10 0
6	-	-	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
7	-	-	-	+3 -10	-103	Note 1	Note 1	+ (Note 2 0)
8	-	-	-	-	+5 -1	Note 1	Note 1	Note 1
1	-	-	-	-	-	+10 - (Note 2)	0 - (Note 2)	+ (Note 2) 0
2	-	-	-	-	-	-	0 -	+ (Note 2) 0
3	-	-	-	-	-	-	-	+ (Note 2) 0
4	-	-	-	-	-	-	-	Substrate and Case

NOTES:

1. Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.
2. 30V (CA3085); 40V (CA3085A; 50V (CA3085B)

Maximum Current Ratings

TERMINAL NUMBER	I_{IN} mA	I_{OUT} mA
5	10	1.0
6	1.0	-0.1
7	1.0	-0.1
8	0.1	10
1	20	150
2	150	60
3	150	60
4	-	-

DC Electrical Specifications T_A = 25°C, Unless Otherwise Specified

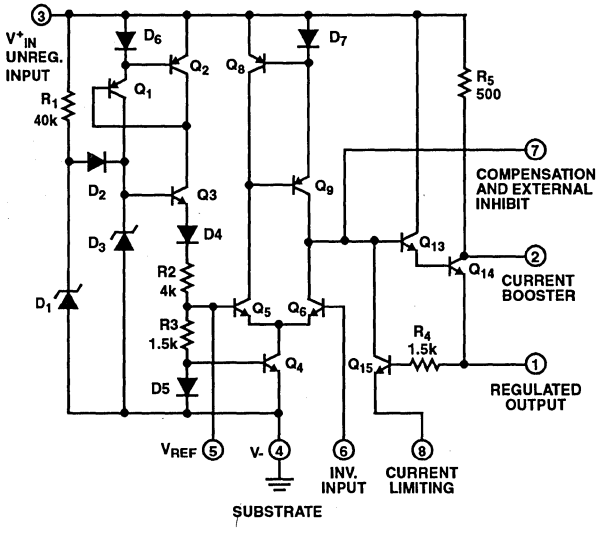
PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS									UNITS
			CA3085			CA3085A			CA3085B			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS												
Reference Voltage	V_{REF}	V^+_{IN} = 15V (Figure 3)	1.4	1.6	1.8	1.5	1.6	1.7	.15	1.6	1.7	V
Quiescent Regulator Current	$I_{quiescent}$	V^+_{IN} = 30V (Figure 3)	-	3.3	4.5	-	-	-	-	-	-	mA
		V^+_{IN} = 40V (Figure 3)	-	-	-	-	3.65	5	-	-	-	mA
		V^+_{IN} = 50V (Figure 3)	-	-	-	-	-	-	-	4.05	7	mA
Input Voltage Range	$V_{IN(range)}$		7.5	-	30	7.5	-	40	7.5	-	50	V
Maximum Output Voltage	$V_{O(MAX)}$	V^+_{IN} = 30, 40, 50V (Note 1); R_L = 365Ω; Term. No. 6 to GND (Figure 3)	26	27	-	36	37	-	46	47	-	V
Maximum Output Voltage	$V_{O(MIN)}$	V^+_{IN} = 30V (Figure 3)	-	1.6	1.8	-	1.6	1.7	-	1.6	1.7	V
Input - Output Voltage Differential	V_{IN}-V_{OUT}		4	-	28	4	-	38	3.5	-	48	V
Limiting Current	I_{LIM}	V^+_{IN} = 16V, V^+_{OUT} = 10V, RSCP = 6Ω (Note 2) (Figure 6)	-	96	120	-	96	120	-	96	120	mA
Load Regulation (Note 3)		I_L = 1 to 100mA, R_{SCP} = 0	-	-	-	-	0.025	0.15	-	0.025	0.15	%V_{OUT}
		I_L = 1 to 100mA, R_{SCP} = 0, T_A = 0°C to +70°C	-	-	-	-	0.035	0.6	-	0.035	0.6	%V_{OUT}
		I_L = 1 to 12mA, R_{SCP} = 0	-	0.003	0.1	-	-	-	-	-	-	%V_{OUT}
Line Regulation (Note 4)		I_L = 1mA, R_{SCP} = 0	-	0.025	0.1	-	0.025	0.075	-	0.025	0.04	%/V
		I_L = 1mA, R_{SCP} = 0, T_A = 0°C to +70°C	-	0.04	0.15	-	0.04	0.1	-	0.04	0.08	%/V
Equivalent Noise Output Voltage	V_{NOISE}	V^+_{IN} = 25V (Figure 10), C_{REF} = 0	-	0.5	-	-	0.5	-	-	0.5	-	mVp-p
		V^+_{IN} = 25V (Figure 10), C_{REF} = 0.22µF	-	0.3	-	-	0.3	-	-	0.3	-	mVp-p
Ripple Rejection		V^+_{IN} = 25V, f = 1kHz (Figure 11), C_{REF} = 0	-	50	-	-	50	-	45	50	-	dB
		V^+_{IN} = 25V, f = 1kHz (Figure 11), C_{REF} = 2µF	-	56	-	-	56	-	50	56	-	dB
Output Resistance	r_O	V^+_{IN} = 25V, f = 1kHz (Figure 11)	-	0.075	1.1	-	0.075	0.3	-	0.075	0.3	Ω
Temperature Coefficient of Reference and Output Voltages	V_{REF}, V_O (Note 4)	I_L = 0, V_{REF} = 1.6V	-	0.0035	-	-	0.0035	-	-	0.0035	-	%/°C

DC Electrical Specifications T_A = 25°C, Unless Otherwise Specified **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS									UNITS
			CA3085			CA3085A			CA3085B			
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
LOAD TRANSIENT RECOVERY TIME												
Turn On	t_{ON}	V^+_{IN} = 25V, +50mA Step (Figure 16)	-	1	-	-	1	-	-	1	-	µs
Turn Off	t_{OFF}	V^+_{IN} = 25V, -50mA Step (Figure 16)	-	3	-	-	3	-	-	3	-	µs
LOAD TRANSIENT RECOVERY TIME												
Turn On	t_{ON}	V^+_{IN} = 25V, f = 1kHz, 2V Step	-	0.8	-	-	0.8	-	-	0.8	-	µs
Turn Off	t_{OFF}		-	0.4	-	-	0.4	-	-	0.4	-	µs

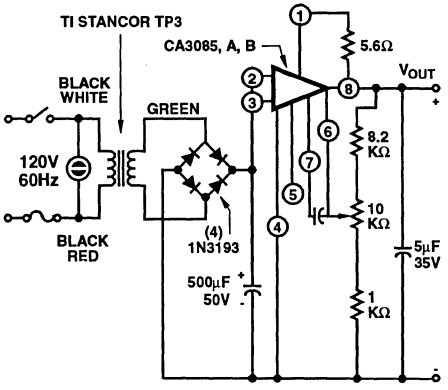
NOTES:

1. 30V (CA3085), 40V (CA3085A), 50V (CA3085B)
2. R_{SCP}: Short Circuit Protection Resistance
3. Load Regulation = $[\Delta V_{OUT} \div V_{OUT}(initial)] \times 100\%$
4. Line Regulation = $[\Delta V_{OUT} \div V_{OUT}(initial)(\Delta V_{IN})] \times 100\%$



All Resistance Values are in Ohms

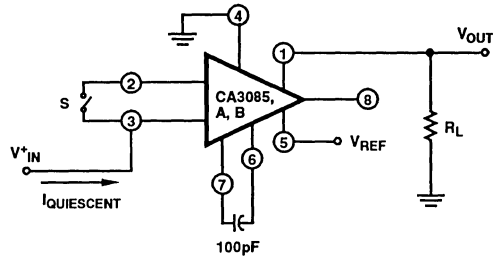
FIGURE 1. SCHEMATIC DIAGRAM OF CA3085 SERIES



V_{OUT} = 3.5V to 20V (0 to 90mA)
Regulation = 0.2% (Line and Load)
Ripple < 0.5mV at Full Load

FIGURE 2. APPLICATION OF THE CA3085 SERIES IN A TYPICAL POWER SUPPLY

Test Circuits and Typical Characteristics Curves



TEST	R_L	V_{IN}	CONNECT TERM NO. 6	S
V_{REF}	∞	+1.6	Open	Open
$I_{QUIESCENT}$	∞	+40	Open	Open
$V_{OUT(MAX)}$	365Ω	+40	Ground	Closed
$V_{OUT(MIN)}$	10k	+30	Terminal No.1	Open

FIGURE 3. TEST CIRCUIT FOR V_{REF}, $I_{QUIESCENT}$, $V_{OUT(MAX)}$, $V_{OUT(MIN)}$

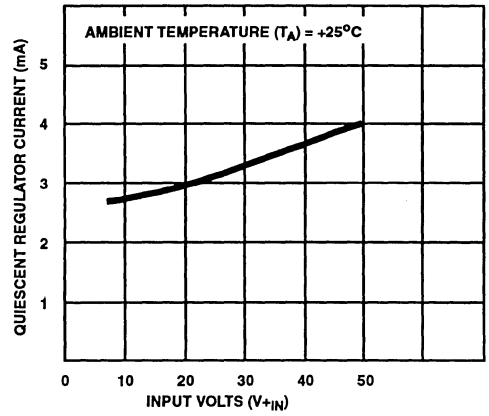


FIGURE 4. $I_{QUIESCENT}$ VS. V^+_{IN}

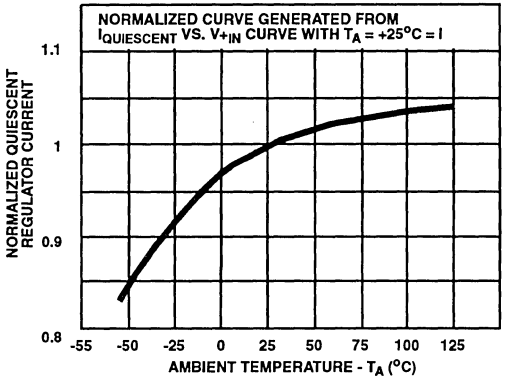
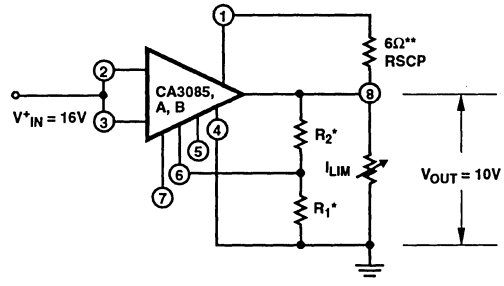


FIGURE 5. NORMALIZED $I_{QUIESCENT}$ VS. T_A



* $V_{OUT} = 1.6 \times (R_1 + R_2 + R_1)$
** The limits current is inversely proportional to R_{SCP}

FIGURE 6. TEST CIRCUIT FOR LIMITING CURRENT

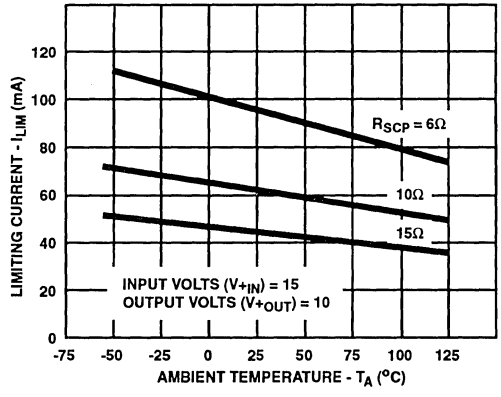


FIGURE 7. I_{LIM} VS. T_A

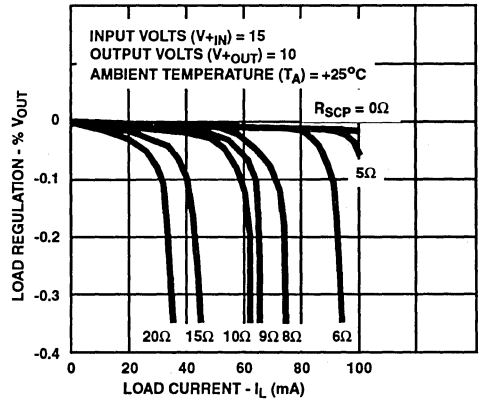


FIGURE 8. LOAD REGULATION CHARACTERISTICS

Test Circuits and Typical Characteristics Curves (Continued)

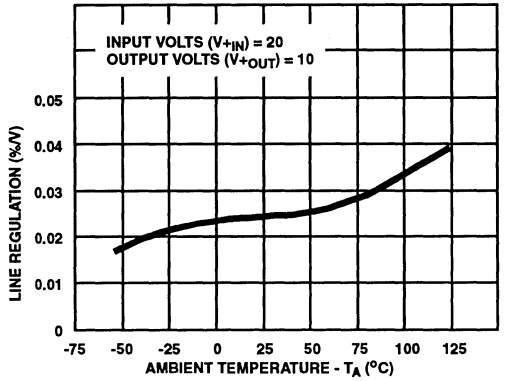


FIGURE 9. LINE REGULATION TEMPERATURE CHARACTERISTICS

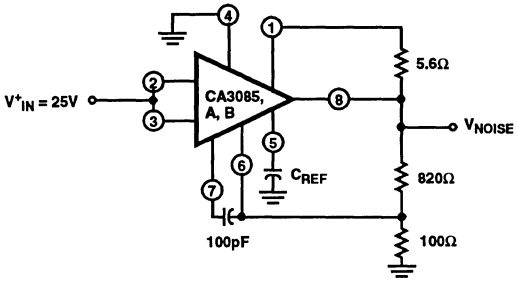


FIGURE 10. TEST CIRCUIT FOR NOISE VOLTAGE

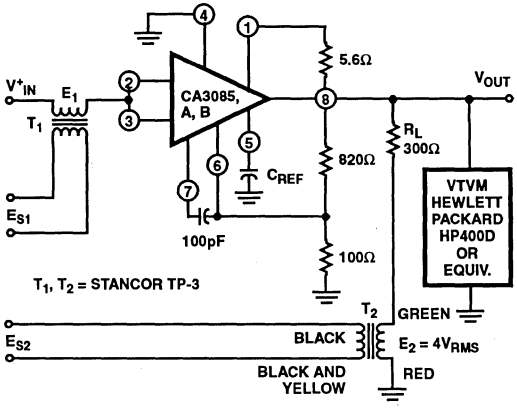


FIGURE 11. TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

TEST PROCEDURES FOR TEST CIRCUIT FOR RIPPLE REJECTION AND OUTPUT RESISTANCE

Output Resistance

Conditions

1. V_{IN} = +25V, C_{REF} = 0, Short E_1
2. Set E_{S2} at 1kHz so that $E_2 = 4V_{RMS}$
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or Equivalent
4. Calculate R_{OUT} from $R_{OUT} = V_{OUT}(R_L/E_2)$

Ripple Rejection - I

Conditions

1. V_{IN} = +25V, C_{REF} = 0, Short E_2
2. Set E_{S1} at 1kHz so that $E_1 = 3V_{RMS}$
3. Read V_{OUT} on a VTVM, such as a Hewlett-Packard, HP400D or Equivalent
4. Calculate Ripple Rejection from 20 log (E_1/V_{OUT})

Ripple Rejection - II

Conditions

1. Repeat Ripple Rejection I with C_{REF} = 2µF

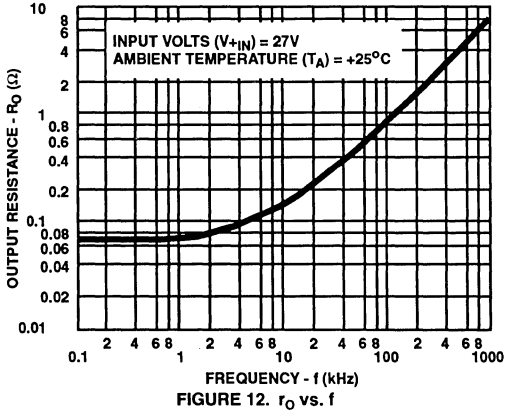


FIGURE 12. r_O vs. f

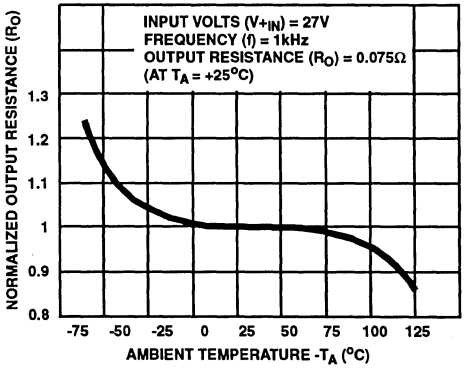


FIGURE 13. NORMALIZED r_O vs. T_A

Test Circuits and Typical Characteristics Curves (Continued)

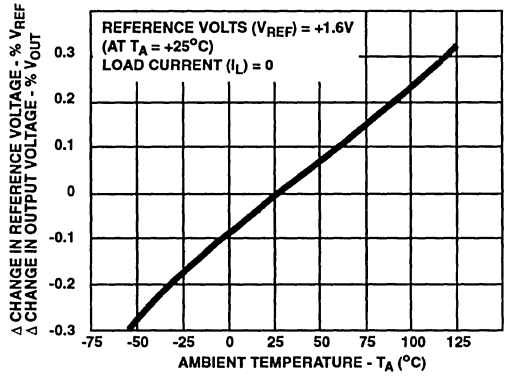


FIGURE 14. TEMPERATURE COEFFICIENT OF V_{REF} AND V_{OUT}

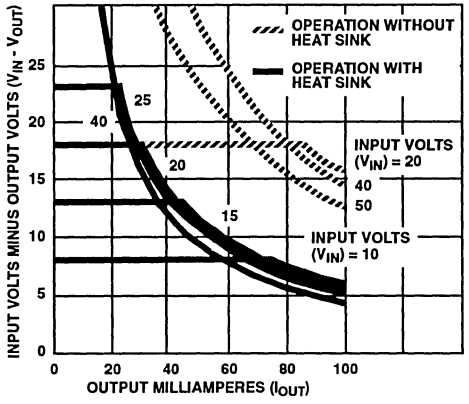


FIGURE 15. DISSIPATION LIMITATION (V_{IN} - V_{OUT} vs. I_{OUT})

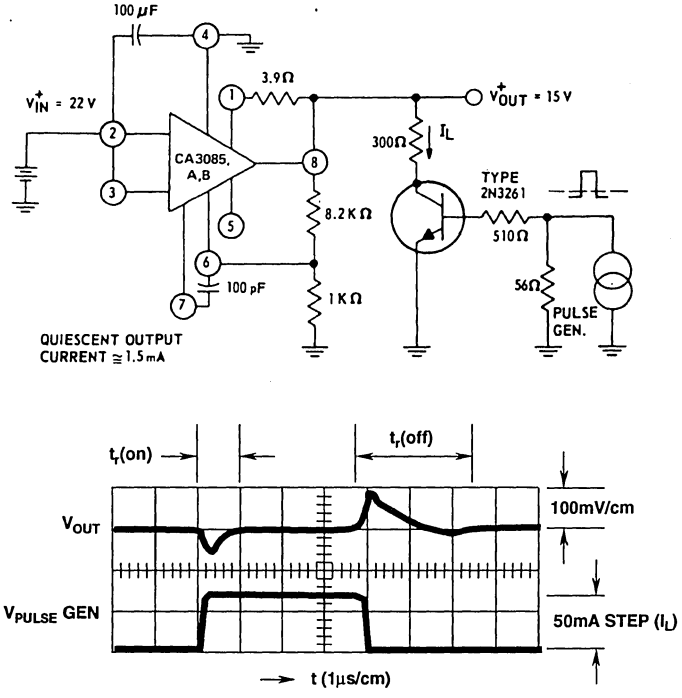


FIGURE 16. TURN-ON AND TURN-OFF RECOVERY TIME TEST CIRCUIT WITH ASSOCIATED WAVEFORMS

See Application Note 6157 for further information

Typical Regulator Circuits

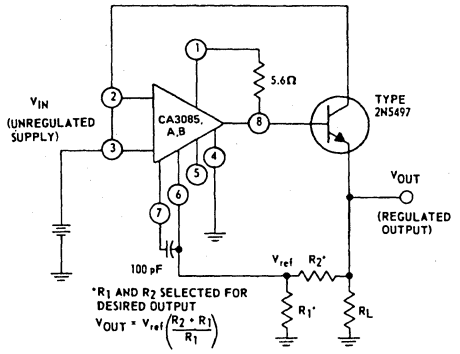
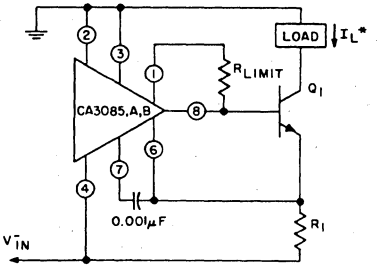
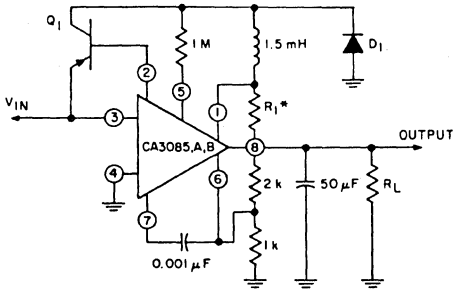


FIGURE 17. TYPICAL HIGH CURRENT VOLTAGE REGULATOR CIRCUIT



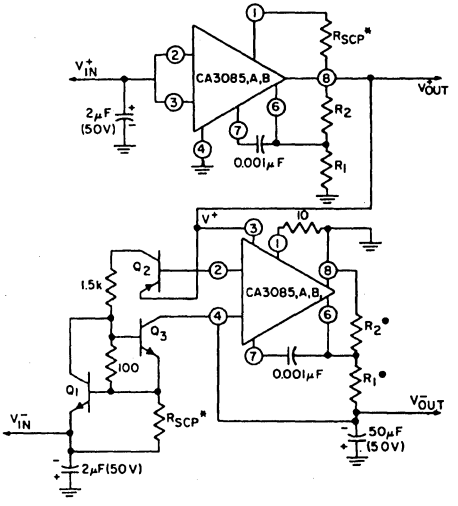
*IL = 1.6 ÷ R1, 200mA ≤ 2A
Q1: Any N-P-N Silicon Transistor that can handle a 2A Load Current such as RCA-2N3772 or Equivalent

FIGURE 18. TYPICAL CURRENT REGULATOR CIRCUIT



All Resistance Values are in Ohms
D_1: RCA-1N1763A or Equivalent
Q_1: RCA-2N5322 or Equivalent
*$R_1 = 0.7I_L$ (Max)

FIGURE 19. TYPICAL SWITCHING REGULATOR CIRCUIT



All Resistance Values are in Ohms
Q1: RCA-2N2102 or Equivalent
Q2: Any P-N-P Silicon Transistor (RCA-2N5322 or Equivalent)
Q3: Any N-P-N Silicon Transistor that can handle the deisred Load Current (RCA-2N3772 or Equivalent)
*$V_{OUT} = (R_1 + R_2) \div R_1$
*R_{SCP}: Short Circuit Protection Resistance

FIGURE 20. COMBINATION POSITIVE AND NEGATIVE VOLTAGE REGULATOR CIRCUIT

HARRIS SEMICONDUCTOR

CA3277

PRELIMINARY

May 1992

Dual 5V Regulator With Logic Controlled Startup for Microcontroller Applications

Features

- Dual 5V Regulator
  - $V_{OUT}1$ 5V 50mA - Standby
  - $V_{OUT}2$ 5V 80mA - Enabled
  - Regulated 6.2V to 18V
  - Bandgap Voltage References
- Overvoltage Shutdown
- Short Circuit Current Limiting
- Thermal Shutdown Protection
- Power ON Delayed Reset Control
- Ignition Comparator & Logic Switch
- Data Comparator & Logic Switch
- 100x Current Multiplier/Amplifier

Applications

- Automotive Dual 5V Supply
- Radio, TV, CATV
- Industrial Controls
- µP, Memory Supply

Description

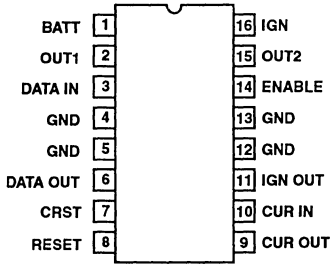
The CA3277 is a Dual 5 Voltage Regulator IC intended for microprocessor and logic controller applications. It is supplied with features that are commonly specified for shutdown and startup requirements of microcontrollers. Overvoltage shutdown, short circuit current limiting and thermal shutdown features are provided for protection in the harsh environmental applications of industrial and automotive systems. The CA3277 functions are complementary to the needs of microcontroller and memory circuits. The ignition comparator provides a switched output to the microcontroller port input and the microcontroller provides a logic switched output to the regulator enable input. The standby output of the regulator supplies the microcontroller/memory circuits. Other functions of the CA3277 include a data comparator and a logic switch to transfer remote data to the microcontroller at a 5V logic level (RDI input). Data is transmitted from the microcontroller (TDO output) to the input of the CA3277 current amplifier which amplifies and translates the signal to a high level from the output of an npn transistor open collector.

Ordering Information

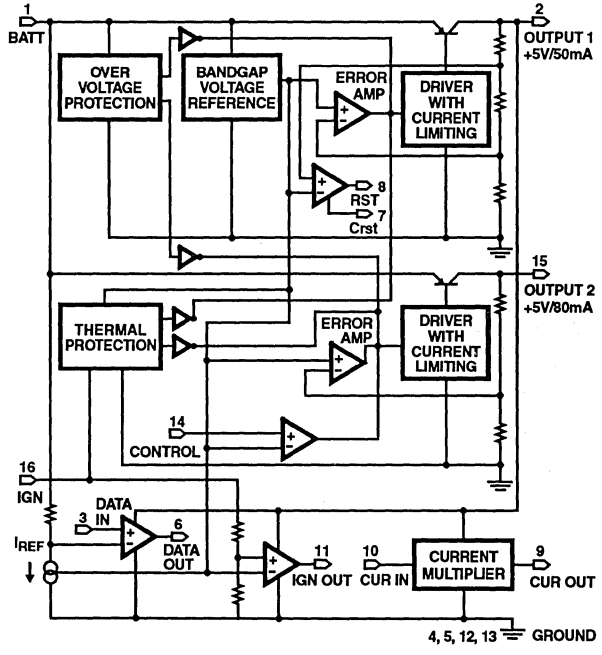
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3277E	-40°C to +85°C	16 Lead Plastic DIP

Pinout

16 LEAD DUAL-IN-LINE PACKAGE
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2792.2**

Absolute Maximum Ratings

V_{BATT} (Short Duration) ..... -14V to 26V
V_{BATT} Maximum Operation ..... 18V Max.
Maximum Output 1 Load Current ..... 50mA Max.
Maximum Output 2 Load Current ..... 80mA Max.

Power Dissipation Ratings

Up to 60°C ..... 1.5W Max.
Derate Above 60°C ..... 16.6mW/°C Max.
Ambient Operating Temperature ..... -40°C to +85°C
Storage Temperature Range ..... -55°C to +150°C
Maximum Junction Temperature ..... +150°C
Lead Temperature (During Soldering)
$^1/_{16}$" ± $^1/_{32}$" from case, 10s max ..... 265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, OUT1 = 50mA, OUT2 = 80mA Unless Otherwise Specified

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
REG OUTPUT 1					
Output Voltage	V_{BATT} = 9V to 16V	4.75	5.0	5.25	V
Dropout Voltage		-	150	800	mV
Line Reg	V_{BATT} = 6.2V to 16V	-	-	40	mV
Load Reg.	0.5mA to 50mA	-	-	60	mV
Current Limit	Short Output 1 to 3V	-	-	200	mA
REG OUTPUT 2					
Output Voltage	V_{BATT} = 9V to 16V	4.75	5.0	5.25	V
Line Reg.	V_{BATT} = 6.2V to 16V	-	-	40	mV
Load Reg.	0.5mA to 80mA	-	-	60	mV
Current Limit	Short Output 2 to 3V	-	-	225	mA
Idle Current	At 12.6 V_{BATT}, No Loads, V_{ENABLE} = V_{IGN} = 0V	-	400	800	µA
Enable On Current	At 5V	-	-	100	µA
Data Out V_{OL}	V_{BATT} = 16V, Data In = V_{BATT} -5V	-	-	150	mV
Data Out V_{OH}	V_{BATT} = Data In = 16V	V_{OUT} -0.15	-	-	V
Current Out	Current In = -200µA	16	-	25	mA
Voltage Shutdown	V_{BATT}, V_{IGN} Thd	19	-	23	V
Data Comp Thd	V_{BATT} = 13.5V, Measure to Batt	-3.4	-2.9	-2.4	V
Data Comp Hysteresis		-	200	-	mV
Ign Comp Thd	V_{BATT} = 13.5V	5.5	6.0	6.5	V
Ign Comp Hysteresis		-	200	-	mV
Ripple Rejection	OUT1, OUT2, at 3KHz	45	-	-	dB

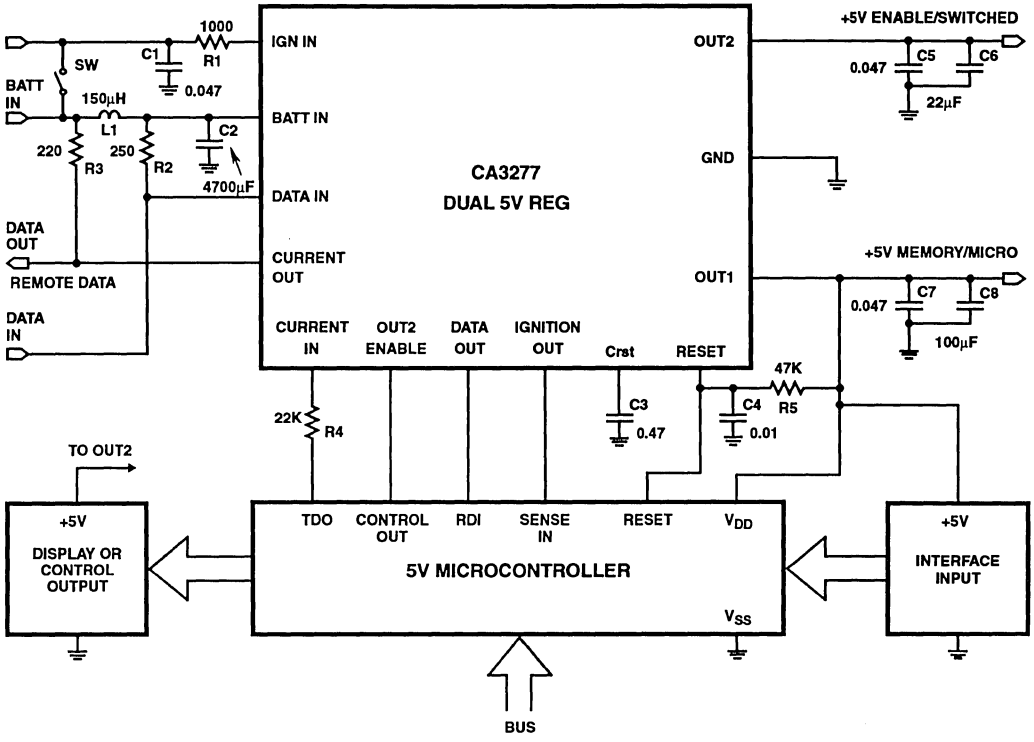


FIGURE 1. TYPICAL APPLICATION CIRCUIT

HARRIS SEMICONDUCTOR

HIP5060

Power Control IC
Single Chip Power Supply

May 1992

Features

- Single Chip Current Mode Control IC
- 60V, 10A On-chip DMOS Transistor
- Thermal Protection
- Over-Voltage Protection
- Over-Current Protection
- 1MHz Operation or External Clock
- Synchronization Output
- On-Chip Reference Voltage - 5.1V
- Output Rise and Fall Times ~ 3ns
- Designed for 27V to 45V Operation

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters

Description

The HIP5060 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC. Both the standard "Boost" and the "SEPIC" (Single-Ended Primary Inductance Converter) power supply topologies are easily implemented with this single control IC.

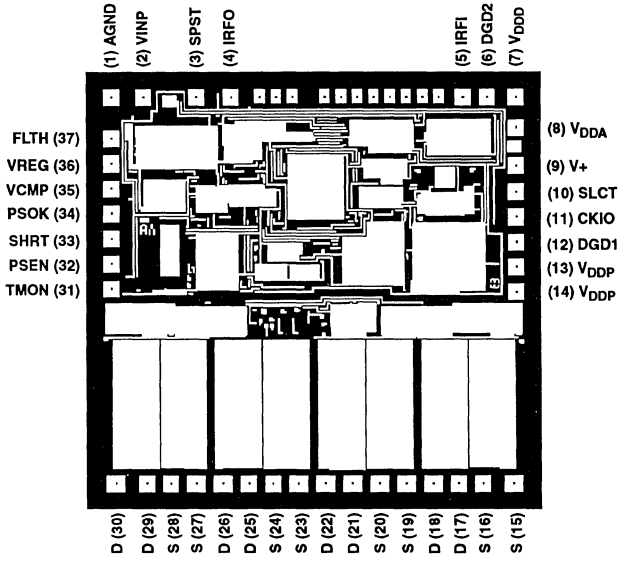
Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Moreover, over-temperature and over-voltage detection circuitry is incorporated within the IC to monitor the chip temperature and the actual power supply output voltage. These circuits can disable the drive to the power transistor to protect both the transistor and, most importantly, the load from over-voltage.

As a result of the power DMOS transistor's current and voltage capability (10A and 60V), power supplies with output power capability up to 100 watts are possible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5060DY	0°C to +85°C	37 Pad Chip
HIP5060DW	0°C to +85°C	Wafer

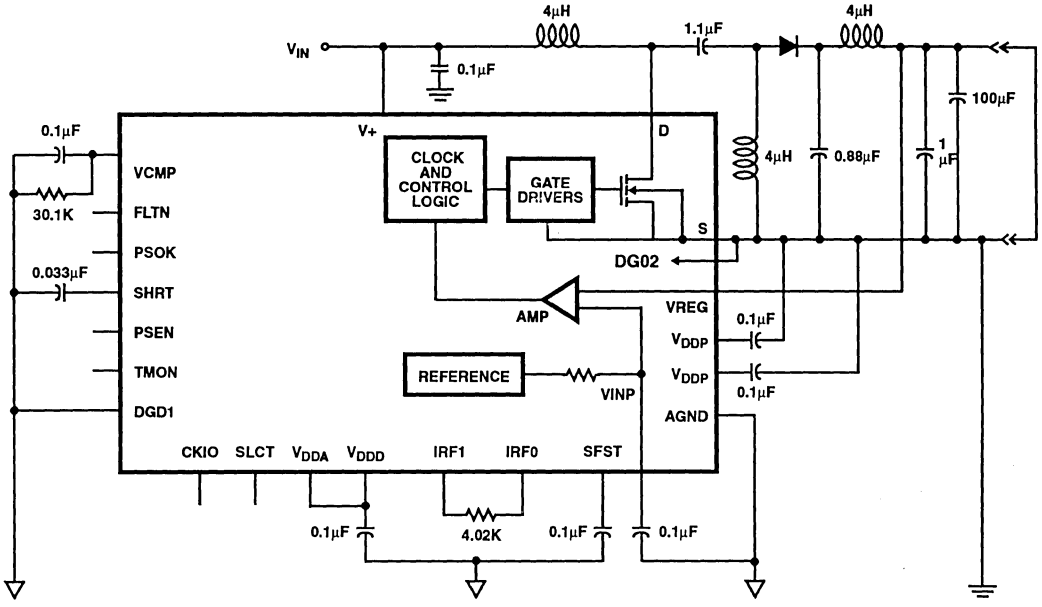
Chip



NOTE: Unused pads are for trim and test.
153 mils x 165 mils (3.88mm x 4.19mm)

File Number 3207

Simplified Block Diagram



TYPICAL SEPIC CONFIGURATION

Absolute Maximum Ratings

DC Supply Voltage, V+ ..... -0.3V to 45V
DMOS Drain Voltage ..... -0.3V to 60V
DMOS Drain Current 20A
DC Logic Supply ..... -0.3V to 16V
Output Voltage, Logic Outputs ..... -0.3V to 16V
Input Voltage, Analog and Logic ..... -0.3V to 16V
Operating Junction Temperature Range ..... 0°C to +110°C
Storage Temperature Range ..... -55°C to +150°C

Thermal Information

Thermal Resistance Junction-to-Case θ_{jc}
(Eutectic Mounting to Heat Sink ..... 3°C/W Max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics

V+ = 36V, T_J = 0°C to +110°C; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DEVICE PARAMETERS						
I+	Supply Current	PSEN = 12V	-	19.5	32	mA
V_{DDA}	Internal Regulator Output Voltage	V+ = 15V to 45V, I_{OUT} = 10mA	11.0	-	13.2	V
VINP	Reference Voltage	I_{VINP} = 0mA	5.01	5.1	5.19	V
R_{VINP}	VINP Resistance	VINP = 0	-	900	-	Ω
ERROR AMPLIFIERS						
$\lvert V_{IO} \rvert$	Input Offset Voltage (VREG - VINP)	I_{VCMP} = 0mA	-	-	10	mV
R_{IN} VREG	Input Resistance to GND	VREG = 5.1V	-	56	-	kΩ
g_m (VREG)	VREG Transconductance I_{VCMP}/(VREG - VINP)	VCMP = 1V to 8V, SFST = 11V	15	30	50	mS
g_m (SFST)	SFST Transconductance I_{VCMP}/(VREG - SFST)	V_{SFST} < 4.9V	0.8	-	6	mS
I_{VCMP}	Maximum Source Current	VREG = 4.95V, VCMP = 8V	-2.5	-	-0.75	mA
I_{VCMP}	Maximum Sink Current	VREG = 5.25V, VCMP = 0.4V	0.75	-	2.5	mA
OVTH	Over-Voltage Threshold	Voltage at VREG for FLTN to be latched	6.2	-	6.7	V
CLOCK						
fq	Internal Clock Frequency	SLCT = 0V, V_{DDD} = 12V	0.9	1.0	1.1	MHz
V_{TH} CKIN	External Clock Input Threshold Voltages	SLCT = 12V	33	-	66	%V_{DDD}
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 5A, T_J = +25°C	-	-	0.13	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	µA
CURRENT CONTROLLED PWM						
$\lvert V_{IO} \rvert$ VCMP	Buffer Offset Voltage (VCMP - V_{IRFO})	IRFO = 0mA to -5mA, VCMP = 0.2V to 7.6V	-	-	125	mV
V_{TH} IRFO	Voltage at IRFO that disables PWM. This is due to low load current		100	-	270	mV

Electrical Characteristics V+ = 36V, T_J = 0°C to +110°C; Unless Otherwise Specified **(Continued)**

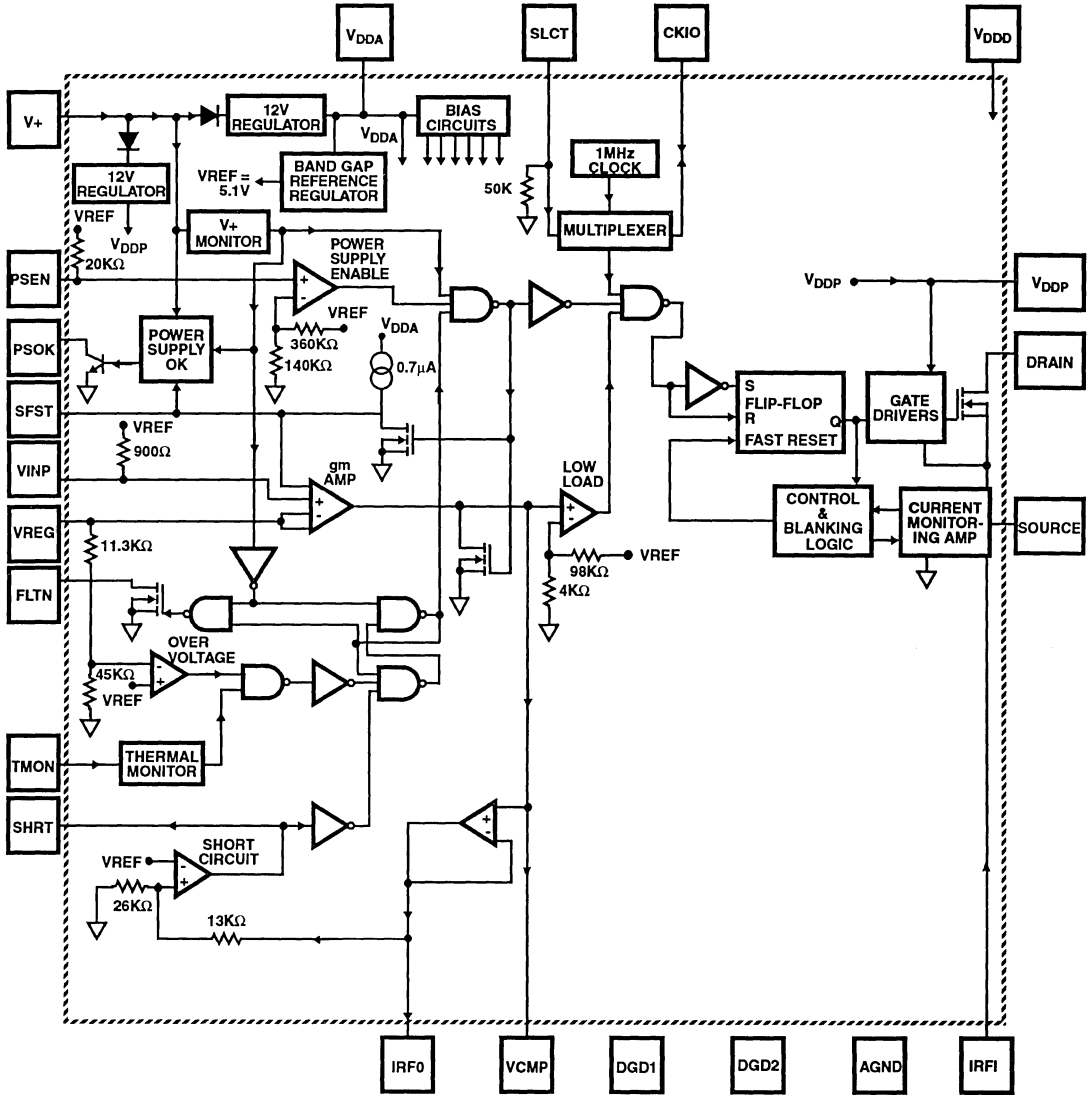
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
CURRENT CONTROLLED PWM (Continued)						
I_{TH} IRFO	Voltage at IRFO to enable SHRT output current. This is due to Regulator Over Current Condition		7.4	-	8.0	V
I_{SHRT}	SHRT Output Current, During Over-Current	V_{IRFO} = 8.1V	-37	-	-17	µA
V_{TH} SHRT	Threshold voltage on SHRT to set FLTN latch		4	6	8	V
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	3.8	-	4.9	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{IRFI} = 2mA	150	-	360	Ω
t_{RS}*	Current Comparator Response Time	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/µs	-	30	-	ns
MCPW*	Minimum Controllable Pulse Width		25	50	100	ns
MCPI*	Minimum Controllable DMOS Peak Current		200	400	800	mA
START-UP						
V+	Rising V+ Power-On Reset Voltage		22	-	27	V
V+	Falling V+ Power-Off Set Voltage		-	15	-	V
V+	V+ Power-On Hysteresis		9	-	12	V
V_{TH} PSEN	Voltage at PSEN to Enable Supply		0.8	-	2.0	V
r_{PSEN}	Internal Pull-Up Resistance, to 5.1V		-	20	-	KΩ
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 0V to 10V	-1.0	-0.7	-0.4	µA
I_{PSOK}	PSOK High-State Leakage Current	SFST = 0V, PSOK = 12V	-1	-	1	µA
V_{PSOK}	PSOK Low-State Voltage	SFST = 11V, I_{PSOK} = 1mA	-	-	0.4	V
V_{TH} SFST	PSOK Threshold, Rising V_{SFST}		9.4	-	11	V
THERMAL MONITOR						
TEMP*	Substrate Temperature for Thermal Monitor to Trip	TMON pin open	105	-	135	°C

* Determined by design, not a measured parameter.

Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1	AGND	Analog ground.
2	VINP	Internal 5.1V reference.
3	SFST	Controls the rate of rise of the output voltage. Time is determined by an internal 0.7µA current source and an external capacitor.
4	IRFO	A resistor placed between this pad and IRFI converts the VCMP signal to a current for the current sense comparator. The maximum current is set by the value of the resistor, according to the equation: I_{PEAK} = 32/R. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 17.8A. This assumes VCMP is 7.3V. Maximum output current should be kept below 20A.
5	IRFI	See IRFO
6	DGD2	Ground of the DMOS gate driver. This pad is used for bypassing.
7	V_{DDD}	Voltage input for the chip's digital circuits. This pad also allows decoupling of this supply.
8	V_{DDA}	This is the analog supply and internal 12V regulator output.
9	V+	This is the main supply voltage input pad to the regulator IC. Because of the high peak currents this pad must be well bypassed with at least a 0.7µF capacitor and may be composed of seven, single 0.1µF chip capacitors.
10	SLCT	This pad provides for the option of using either internal 1MHz operation of for an external clock. Floating or grounding this pad will place the internal clock at the CKIO pad. Returning this terminal to V_{DDD} or 12V will allow application of an external clock to the IC via the CKIO pad. There is an internal 50K pull down
11	CKIO	Clock output when SLCT is floated or grounded. External clock input when SLCT is returned to 12V.
12	DGD1	This pad is the return for the digital supply.
13 & 14	V_{DDP}	These pads are used to decouple the high current pulses to the output driver transistors. The capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
15, 16, 19, 20, 23, 24, 27, 28	S	Source pads of the DMOS power transistor.
17, 18, 21, 22, 25, 26, 29, 30	D	Drain pads of the DMOS power transistor.
31	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to 12V the function is disabled. Returning this pad to ground will put the IC into the thermal shutdown state. Normally, this pad is left floating. Thermal shutdown occurs at a nominal junction temperature of +125°C.
32	PSEN	This terminal is provided to activate the converter. This terminal may be left open or returned to 5V for normal operation. When the input is low, the DMOS driver is disabled.
33	SHRT	25µA is internally applied to this node when there is an over-current condition.
34	PSOK	This pad provides a delayed positive indication when the supply is enabled.
35	VCMP	Output of the transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
36	VREG	Input to the transconductance error amplifier is available on this pad. The other input is internally connected to the 5.1V reference, VINP, Pad 2.
37	FLTN	This is an open drain output that remains low when V+ is too low for proper operation. This node and PSEN are useful in multiple converter configurations. This pad will be latched low when over-temperature, over-voltage or over-current is experienced.

Functional Block Diagram



HARRIS SEMICONDUCTOR

HIP5062

Power Control IC
Single Chip Dual Switching Power Supply

May 1992

Features

- Two Current Mode Control Regulators
- Two 60V, 5A On-chip DMOS Transistors
- Thermal Protection
- Over-Voltage Protection
- Over-Current Protection
- 1MHz Operation or External Clock
- Synchronization Output
- On-Chip Reference Voltage - 5.1V
- Output Rise and Fall Times ~ 3ns
- Designed for 26V to 42V Operation

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters

Description

The HIP5062 is a complete power control IC, incorporating two high power DMOS transistors, CMOS logic and two low level analog control circuits on the same Intelligent Power IC. Both the standard "Boost" and the "SEPIC" (Single-Ended Primary Inductance Converter) power supply topologies are easily implemented with this single control IC.

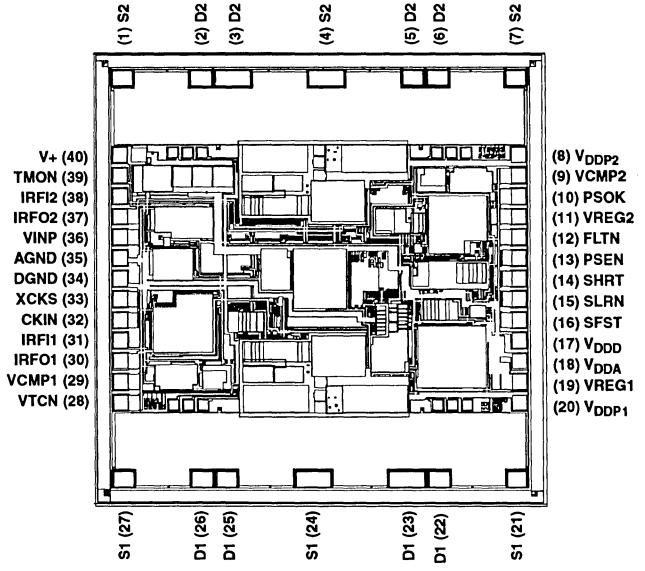
Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Moreover, over-temperature and over-voltage detection circuitry is incorporated within the IC to monitor the chip temperature and the actual power supply output voltage. These circuits can disable the drive to the power transistor to protect both the transistor and, most importantly, the load from over-voltage.

As a result of the power DMOS transistor's current and voltage capability (5A and 60V), multiple output power supplies with total output power capability up to 100W are possible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5062DY	0°C to +85°C	40 Pad Chip
HIP5062DW	0°C to +85°C	WAFER

Chip

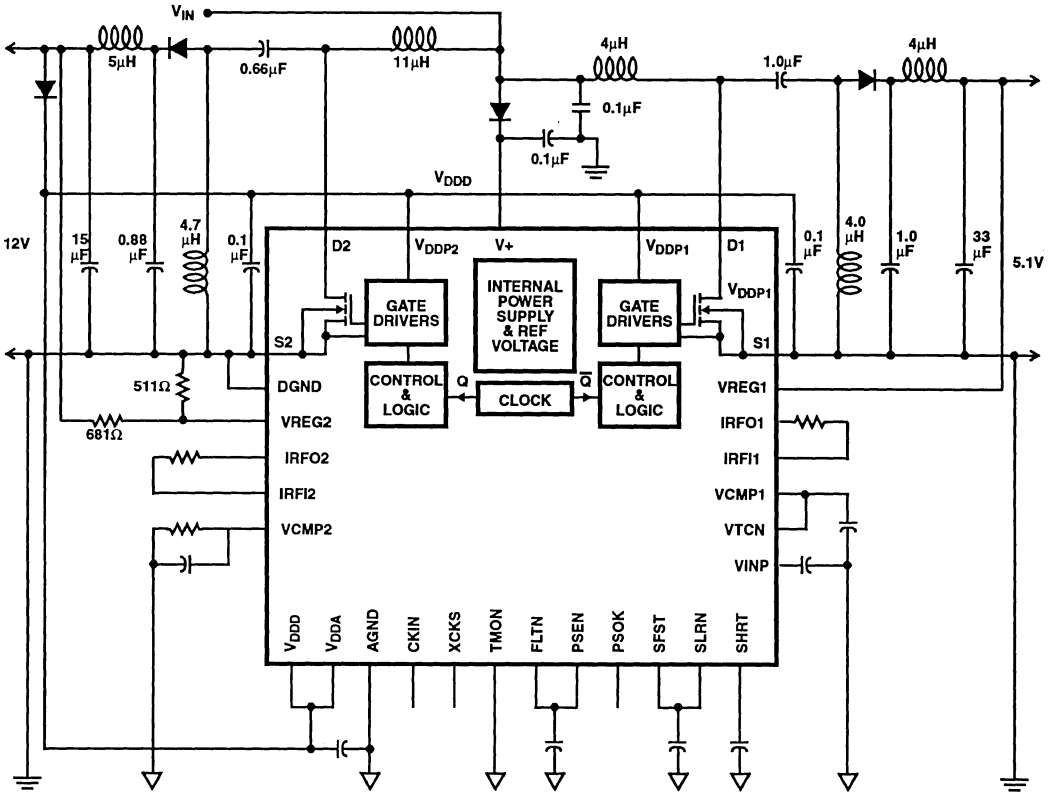


175 mils x 175 mils (4.44mm x 4.44mm)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3208

Simplified Block Diagram



TYPICAL SEPIC CONFIGURATION

Absolute Maximum Ratings

DC Supply Voltage, V+ ..... -0.3V to 42V
DMOS Drain Voltage ..... -0.3V to 60V
DMOS Drain Current 10A
DC Logic Supply ..... -0.3V to 16V
Output Voltage, Logic Outputs ..... -0.3V to 16V
Input Voltage, Analog and Logic ..... -0.3V to 16V
Operating Junction Temperature Range ..... 0°C to +110°C
Storage Temperature Range ..... -55°C to +150°C

Thermal Information

Thermal Resistance Junction-to-Case θ_{jc}
(Eutectic Mounting to Heat Sink ..... 3°C/W Max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics V+ = 36V, Channels 1 and 2, T_J = 0°C to +110°C; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DEVICE PARAMETERS						
I+	Supply Current	V+ = 42V, PSEN = 12V	-	24.7	30	mA
V_{DDA}	Internal Regulator Output Voltage	V+ = 30V to 42V, I_{OUT} = 0mA	11.7	-	13.3	V
		V+ = 30V to 42V, I_{OUT} = 30mA	11.5	-	13.3	V
		SLRN = 12V, I_{OUT} = 0mA	11.5	-	13.3	V
VINP	Reference Voltage	VDDA = SLRN = 12V, I_{VINP} = 0mA	5.01	5.1	5.19	V
R_{VINP}	VINP Resistance	VINP = 0	-	900	-	Ω
ERROR AMPLIFIERS						
$\lvert V_{IO} \rvert$	Input Offset Voltage (REG - VINP)	I_{VCMP} = 0mA	-	-	10	mV
R_{IN} VREG	Input Resistance to GND	VREG = 5.1V	39	-	85	kΩ
g_m (VREG)	VREG Transconductance (I_{VCMP}/(VREG - VINP)	VCMP = 1V to 8V, SFST = 11V	15	30	50	mS
g_m (SFST)	SFST Transconductance I_{VCMP}/(VREG - SFST)	V_{SFST} < 4.9V	0.8	-	6	mS
I_{VCMP}	Maximum Source Current	VREG = 4.95V, VCMP = 8V	-2.5	-	-0.75	mA
	Maximum Sink Current	VREG = 5.25V, VCMP = 0.4V	0.75	-	2.5	mA
OVTH	Over-Voltage Threshold	Voltage at VREG for FLTN to be latched	6.05	-	6.5	V
CLOCK						
fq	Internal Clock Frequency	XCKS = 12V, V_{DDD} = 12V	0.9	1.0	1.1	MHz
V_{TH} CKIN	External Clock Input Threshold Voltages		33	-	66	%V_{DDD}
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 2.5A, V_{DDD} = 11V, T_J = +25°C	-	-	0.22	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	µA

Electrical Characteristics V+ = 36V, Channels 1 and 2, T_J = 0°C to +110°C; Unless Otherwise Specified **(Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
CURRENT CONTROLED PWM						
$\|V_{IO}\|$ VCMP	Buffer Offset Voltage (VCOMP - V_{IFRO})	IFRO = 0mA to -5mA, VTCN = 0.2V to 7.6V, VCMP2 = 0.2V to 7.6V	-	-	125	mV
V_{TH} IFRO	Voltage at IRFO that disables PWM. This is due to low load current		116	-	250	mV
I_{TH} IFRO	Voltage at IRFO to enable SHRT output current. This is due to Regulator Over Current Conditions		6.85	-	7.65	V
I_{SHRT}	SHRT Output Current, During Over-Current	V_{IRFO} = 7.7V	-75	-	-33	µA
V_{TH} SHRT	Threshold voltage on SHRT to set FLTN latch	V_{DDD} = 11V	-	5	-	V
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	2.0	-	3.2	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{IRFI} = 2mA	150	-	360	Ω
t_{RS}*	Current Comparator Response Time	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/µs	-	30	-	ns
MCPW*	Minimum Controllable Pulse Width		25	50	100	ns
MCPI*	Minimum Controllable DMOS Peak Current		125	250	500	mA
START-UP						
V+	Rising V+ Power-On Reset Voltage		23	-	26.3	V
	Falling V+ Power-Off Set Voltage		-	15	-	V
	V+ Power-On Hysteresis		9.5	-	11.8	V
V_{TH} PSEN	Voltage at PSEN to Enable Supply	V_{DDD} = 11V	3.6	-	6.5	V
r_{PSEN}	Internal Pull-Up Resistance, to V_{DDD}		-	12	-	KΩ
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 0V to 11V	-1.5	-1.0	-0.65	µA
I_{PSOK}	PSOK High-State Leakage Current	SFST = 11V, PSOK = 12V	-1	-	1	µA
V_{PSOK}	PSOK Low-State Voltage	SFST = 0V, I_{PSOK} = 1mA	-	-	0.4	V
V_{TH} SFST	PSOK Threshold, Rising V_{SFST}	V_{DDD} = 11V	8.1	-	9.9	V
THERMAL MONITOR						
TEMP*	Substrate Temperature for Thermal Monitor to Trip	TMON = 0V	105	-	135	°C

* Determined by design, not a measured parameter.

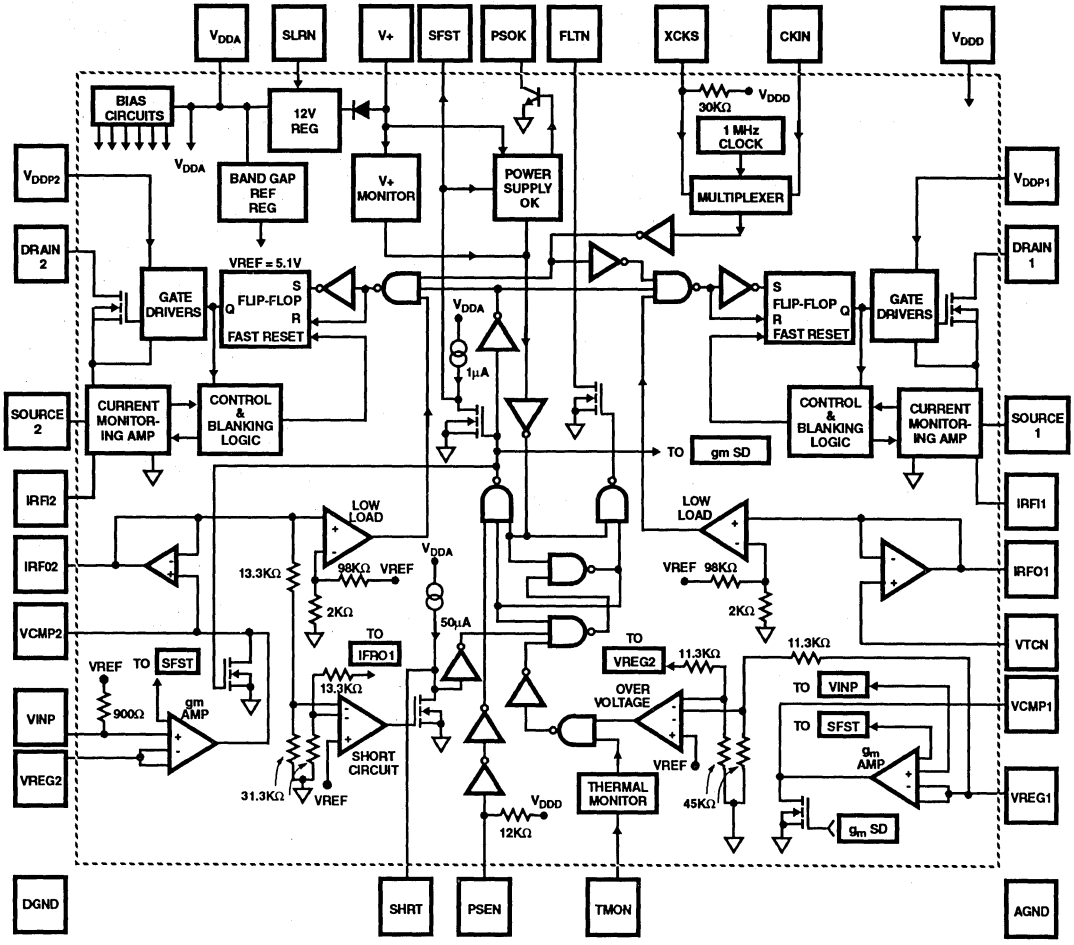
Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1, 4, 7	S2	Source pads for the channel 2 regulator.
2, 3, 5, 6	D2	Drain pads for the channel 2 regulator.
8	V_{DDP2}	This pad is the power input for the channel 2 DMOS gate driver and also is used to decouple the high current pulses to the output driver transistors. The decoupling capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
9	VCMP2	Output of the second channel transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
10	PSOK	This pad provides delayed positive indication when both supplies are enabled.
11	VREG2	Input to the transconductance error amplifier. The other common input for both amplifiers is VINP, Pad 36.
12	FLTN	This is an open drain output that remains low when V+ is too low for proper operation. This node and PSEN are useful in multiple converter configurations. This pad will be latched low when over-temperature, over-voltage or over-current is experienced. V+ must be powered down to reset.
13	PSEN	This terminal is provided to activate the converter. When the input is low, the DMOS drivers are disabled. There is an internal 12K pull-up resistor on this terminal.
14	SHRT	50µA is internally applied to this node when there is an over-current condition.
15	SLRN	Control input to internal regulator that is used during the "start-up" of the supply. In normal operation this terminal starts at 0V and shuts down the internal regulator at approximately 9V. This pad is usually connected to SFST, pad 16.
16	SFST	Controls the rate of rise of both output voltages. Time is determined by an internal 1µA current source and an external capacitor.
17	V_{DDD}	Voltage input for the chip's digital circuits. This pad also allows decoupling of this supply.
18	V_{DDA}	This is the analog supply and internal 12V regulator output usually used only during the start-up sequence. The internal regulator reduced to a nominal 9.2V when SLRN is returned to 12V. Output current capability is 30mA at both voltages.
19	VREG1	Input to channel one transconductance error amplifier. The other, common input for both amplifiers is VINP, pad 36.
20	V_{DDP1}	This pad is the power input for the channel 1 DMOS gate driver and also is used to decouple the high current pulses to the output driver transistors. The decoupling capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
22, 23, 25, 26	D1	Drain pads for the channel 1 regulator.
21, 24, 27	S1	Source pads for the channel 1 regulator.
28	VTCN	Input to transconductance amplifier buffer for channel 1 only. Normally connected to VCMP1, pad 29.
29	VCMP1	Output of the first channel transconductance amplifier. This node is used for both gain and frequency compensation of the loop.
30	IRFO1	A resistor placed between this pad and IRFI1 converts the VCMP1 signal to a current for the current sense comparator. The maximum current is set by the value of the resistor, according to the equation: $I_{PEAK} = 16/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 8.8A. This assumes VCMP1 is 7.3V. Maximum output current should be kept below 10A.
31	IRFI1	See IRFO1.
32	CKIN	Clock input when XCKS is grounded.

Pin Descriptions (Continued)

PAD NUMBER	DESIGNATION	DESCRIPTION
33	XCKS	Grounding this terminal provides for the application of an external clock to CKIN input terminal. For normal internal clock operation, this terminal may be left floating or returned to 12V. There is an internal 30K pull-up resistor on this terminal.
34	DGND	Ground of the DMOS gate drivers. This pad is used for bypassing.
35	AGND	Analog ground.
36	VINP	Internal 5.1V reference. This point is usually bypassed.
37	IRFO2	A resistor placed between this pad and IRFI2 converts the VCMP2 signal to a current for the current sense comparator. The maximum current set by the value of the resistor, according to the equation: $I_{PEAK} = 16/R$. Where R is the value of the external resistor in KΩ and must be greater than 1.5KΩ but less than 10KΩ. For example, if the resistor chosen is 1.8K, the peak current will be 8.8A. This assumes VCMP2 is 7.3V. Maximum output current should be kept below 10A.
38	IRFI2	See IRFO2
39	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to V_{DDA} or 12V the function is disabled. Returning this pad to ground will put the IC into the thermal shutdown state. Thermal shutdown occurs at a nominal junction temperature or +120°C. This terminal is normally returned to ground.
40	V+	This is the main supply voltage input pad to the regulator IC. Because of the high peak currents this pad must be well bypassed with at least a 0.1µF capacitor.

Functional Block Diagram



HARRIS SEMICONDUCTOR

HIP5063

Power Control IC
Single Chip Power Supply

May 1992

Features

- Single Chip Current Mode Control IC
- 60V, 10A On-chip DMOS Transistor
- Thermal Protection
- 1MHz Operation - External Clock
- Output Rise and Fall Times ~ 3ns
- Simple Implementation of High-Speed Current Mode Controlled Regulators and Power Amplifiers
- Designed for 10V to 45V Operation

Applications

- Single Chip Power Supplies
- Current Mode PWM Applications
- Distributed Power Supplies
- Multiple Output Converters
- Wideband Power Amplifiers for Motor Control

Description

The HIP5063 is a complete power control IC, incorporating both the high power DMOS transistor, CMOS logic and low level analog circuitry on the same Intelligent Power IC.

This IC allows the user maximum flexibility in implementing high frequency current controlled power supplies and other power sources.

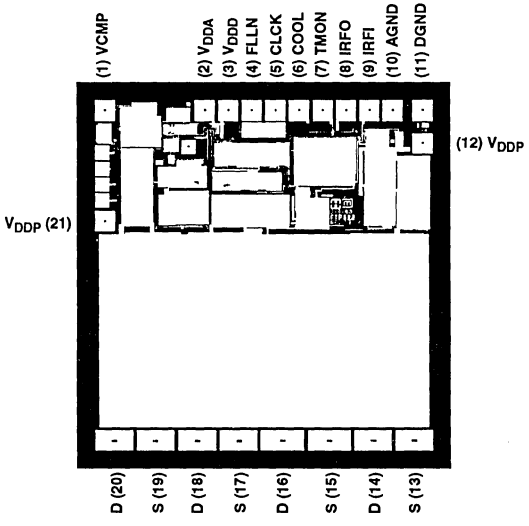
Special power transistor current sensing circuitry is incorporated that minimizes losses due to the monitoring circuitry. Over-temperature detection circuitry is incorporated within the IC to monitor the chip temperature.

As a result of the power DMOS transistor's current and voltage capability (10A and 60V), power supplies with output power capability up to 100 watts are possible.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5063DY	0°C to +85°C	21 Pad Chip
HIP5063DW	0°C to +85°C	Wafer

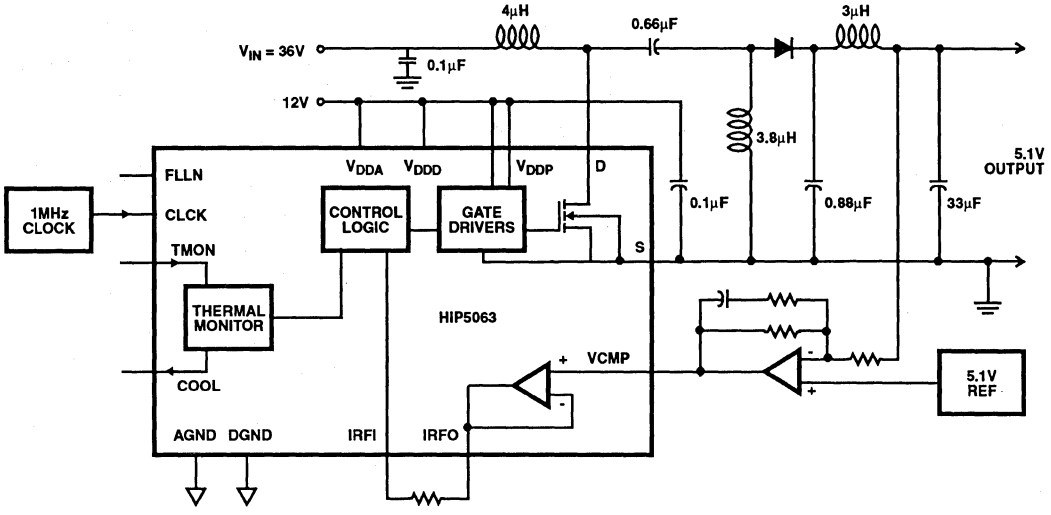
Chip



NOTE: Unused pads are for trim and test.
122 mils x 126 mils (3.1mm x 3.2mm)

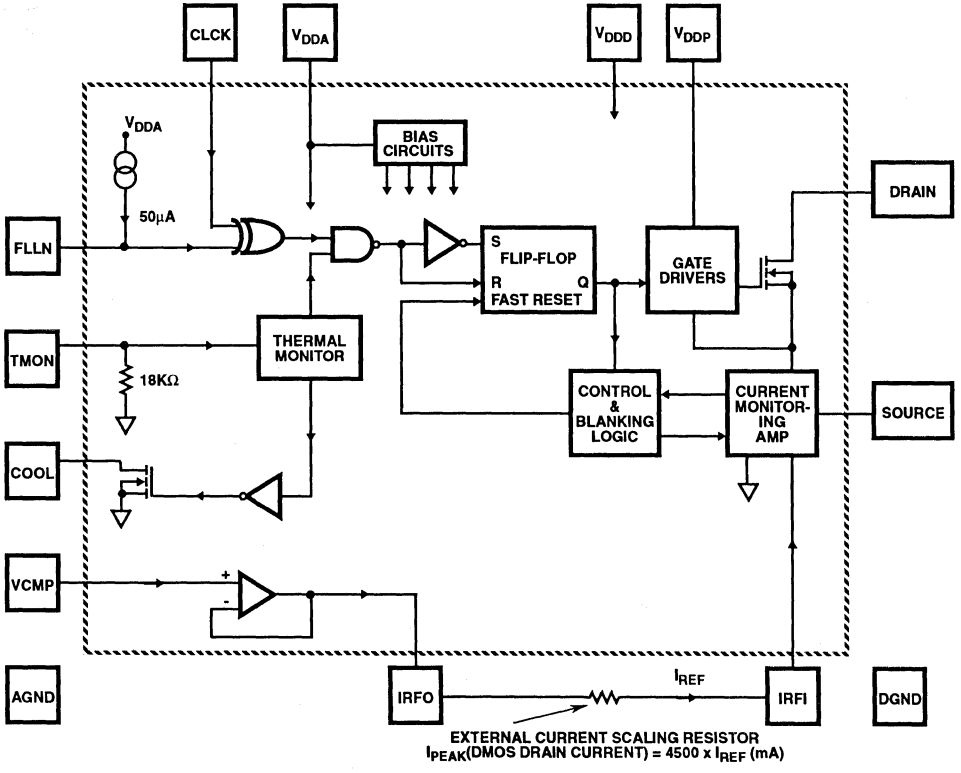
7 REGULATORS/ POWER SUPPLIES

Simplified Block Diagram



TYPICAL SEPIC APPLICATION CONFIGURATION

Functional Block Diagram



Absolute Maximum Ratings

DMOS Drain Voltage ..... -0.3V to 60V
DMOS Drain Current 20A
DC Logic Supply ..... -0.3V to 16V
Output Voltage, Logic Outputs ..... -0.3V to 16V
Input Voltage, Analog and Logic ..... -0.3V to 16V
Operating Junction Temperature Range ..... 0°C to +110°C
Storage Temperature Range ..... -55°C to +150°C

Thermal Information

Thermal Resistance Junction-to-Case (θ_{jc})
(Eutectic Mounting to Heat Sink ..... 3°C/W Max

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Characteristics $V_{DDA} = V_{DDD} = V_{DDP} = 12V$, $T_J = 0°C$ to $+110°C$; Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
DEVICE PARAMETERS						
I+	Supply Current	External Clock Input = 1MHz	-	14	-	mA
DMOS TRANSISTORS						
$r_{DS(on)}$	Drain-Source On-State Resistance	I Drain = 5A, $T_J = +25°C$	-	-	0.13	Ω
I_{DSS}	Drain-Source Leakage Current	Drain to Source Voltage = 60V	-	1	100	µA
CURRENT CONTROLLED PWM						
$\lvert V_{IO}\rvert$ VCMP	Buffer Offset Voltage (VCMP - V_{IRFO})	IRFO = 0mA to -5mA, VCMP = 0.2V to 7.6V	-	-	125	mV
I_{GAIN}	I_{PEAK} ($DMOS_{DRAIN}$)/I_{IRFI}	ΔI ($DMOS_{DRAIN}$)/Δt = 1A/ms	3.8	-	4.9	A/mA
R_{IRFI}	IRFI Resistance to GND	I_{RFI} = 2mA	150	-	360	Ω
t_{RS}*	Current Comparator Response Time	ΔI ($DMOS_{DRAIN}$)/Δt > 1A/ms	-	30	-	ns
MCPW*	Minimum Controllable Pulse Width		25	50	100	ns
MCPI*	Minimum Controllable DMOS Peak Current		200	400	800	mA
CLOCK						
V_{TH} CLCK	CLCK Input Threshold Voltage		4	-	8	V
V_{TH} FLLN	FLLN Input Threshold Voltage		4	-	8	V
I_{FLLN}	FLLN Pull-Up Current	VFLLN = 0V	-70	-50	-30	µA
THERMAL MONITOR						
TEMP*	Substrate Temperature for Thermal Monitor to Trip	TMON pin open	105	-	135	°C
I_{LEAK} COOL	COOL Leakage Current	V_{COOL} = 12V	-	-	1	µA
V_{COOL}	COOL Low-State Voltage	I_{COOL} = 2mA, T_J > +125°C	-	-	0.4	V

* Determined by design, not a measured parameter.

Pin Descriptions

PAD NUMBER	DESIGNATION	DESCRIPTION
1	VCMP	This is the input terminal from an external error amplifier. A MOS input voltage follower buffers this terminal. The buffer output is the IRFO terminal. The external error amplifier may be either an operational amplifier or a transconductance amplifier like the CA3080. This node may be used for both gain and frequency compensation of the control loop.
2	V_{DDA}	This is the analog supply input. An external 12V supply is required.
3	V_{DDD}	Voltage input for the chip's digital circuits.
4	FLLN	One pad of two clocking terminals. This terminal has an external 50µA pull-up current that allows the terminal to be floated or be left open. With FLLN high, (open or tied to V_{DDD}), the ON cycle will start wiith the falling edge of the CLCK input. With FLLN low or grounded, the DMOS ON cycle will start on the rising edge of the CLCK input.
5	CLCK	The other clock input pad. An external clock is applied to this terminal. This terminal has no pull-up current or resistance. See FLLN above for phasing information.
6	COOL	Over-temperature indication is provided at this pad. When the chip temperature is below the thermal threshold, the open drain DMOS transistor is in the high impedance state. When the thermal threshold is exceeded, COOL is held low.
7	TMON	This is the thermal shut down pad than can be used to disable the thermal shutdown circuit. By returning this pad to V_{DDA} or 12V the function is disabled. Returning this pad to ground will enable the thermal monitor function. Thermal threshold occurs at a nominal junction temperature of +125°C.
8	IRFO	A resistor placed between this pad and IRFI converts the VCMP signal to a reference current for the current sense comparator. The cycle by cycle peak current is set by the value to this resistor according the the equation: I_{PEAK} = 4500 x VCMP/R. Where I_{PEAK} is in amperes and R is the value of the external resistor in ohms. A maximum VCMP of 8V and a resistor of 1800Ω will keep the drain current below the absolute maximum specification of 20A.
9	IRFI	See IRFO.
10	AGND	Analog ground.
11	DGND	Digital ground.
12 & 21	V_{DDP}	These pads are used to decouple the high current pulses to the output driver transistors. The capacitor should be at least a 0.1µF chip capacitor placed close to this pad and the DMOS source pads.
13, 15, 17, 19	S	Source pads of the DMOS power transistor.
14, 16, 18, 20	D	Drain pads of the DMOS power transistor.

HARRIS SEMICONDUCTOR

HIP5500

ADVANCE INFORMATION

May 1992

High Voltage IC Half Bridge Gate Driver

Features

- 500V Maximum Rating
- Ability to Interface and Drive N-Channel Power Devices
- Complimentary Outputs for Buffered FETs
- Fault Output
- Over 300KHz Oscillator Range
- Adjustable Deadtime Control
- Softstart Capability
- Undervoltage Holdoff
- Low Current Standby State
- Overcurrent Detection
- Sleep Mode

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP5500IP	-40°C to +125°C	20 Plastic DIP
HIP5500IB	-40°C to +125°C	24 Plastic SOIC

Description

The HIP5500 is a high voltage integrated circuit (HVIC) half-bridge gate driver for standard power MOSFETs, IGBTs, and the new Harris Buffered MOSFETs. It can be employed in a wide variety of switching regulator circuits.

While the HO and LO outputs drive the MOSFETs main gate, the inverted $\overline{HO}$ and $\overline{LO}$ outputs drive the turn-off device within the New Harris Buffered MOSFETs. The use of Buffered FETs provides for faster turn-off of the power devices with a resulting reduction in switching losses.

The HIP5500 incorporates a precision oscillator, adjustable through choice of an external resistor and capacitor. The resistor sets the capacitor charging current and the capacitor sets the integration time of a triangle wave. A second resistor connected to the DIS pin adjusts the fall time of the triangle wave, which can be tailored to the application. An internal 1/3 - 2/3 comparator regulates the triangle-wave minimum and maximum inflection points. The result is a 50% duty-cycle waveform, half of which turns on the upper half of the half-bridge and half which turns on the lower half.

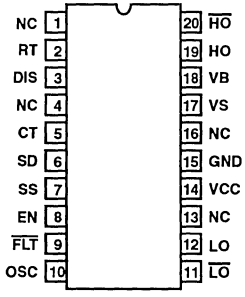
SD, short-detect, and SS, soft-start, inputs provide alternative means for regulating the duty cycle below 50% symmetrically for both half cycles. A capacitor on the SD input will begin charging up once the EN input is made high and no "under-voltage" condition exists. This will cause the duty cycle of each half-cycle to begin at a minimum and ramp up to a maximum (ie 50% each half cycle).

The SD input can be used to sense current, providing a means of shortening the duty cycle even below that imposed by the SS input.

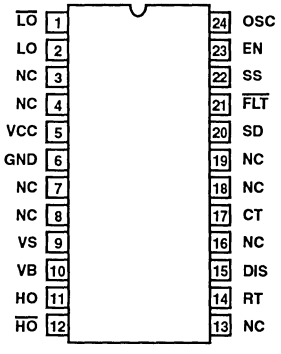
Special circuits in the HIP5500 are included to "match" upper and lower turn-on and turn-off times so as to minimize flux imbalance when driving transformer loads.

Pinout

20 PIN PLASTIC DIP
TOP VIEW



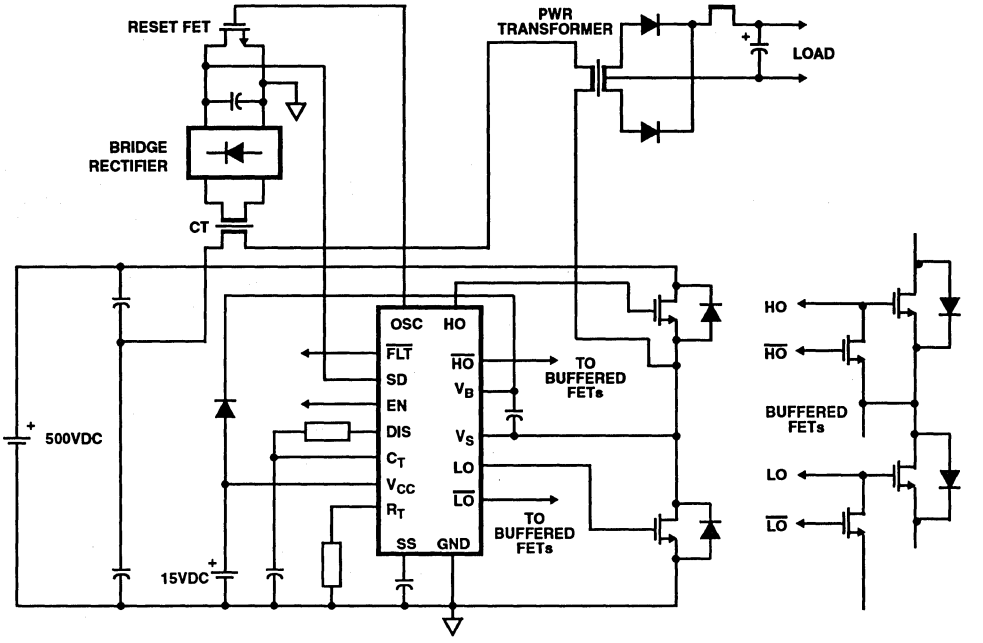
24 PIN SOIC (WIDE BODY)
TOP VIEW



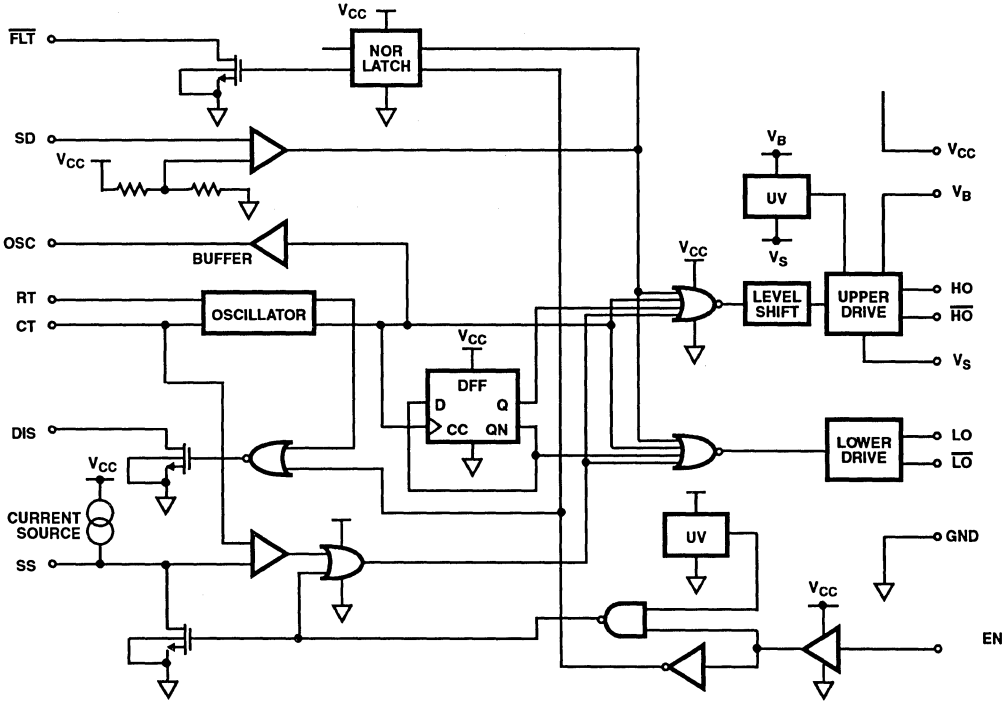
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3210

Typical Application Block Diagram



Functional Block Diagram



Absolute Maximum Ratings

Offset Supply Voltage, V_S ..... $-V_{BS}$ to 500V
Floating Supply Voltage (V_B to V_S) ..... -0.3 to 16V
High Side Channel Output Voltage, V_{HO},V_{NHO} ... V_S-0.5 to V_B+0.5
Fixed Supply Voltage, V_{CC} ..... -0.5 to 16V
Low Side Channel Output Voltage ..... -0.5 to V_{CC}+0.5V
All Other Pin Voltages
(SD, RT, CT, DIS, SS, EN and FLT) ..... -0.5 to V_{CC}+0.5V
Storage Temperature Range ..... -40°C to +150°C
Junction Temperature ..... +125°C
Lead Temperature (Soldering 10s) ..... +300°C
Offset Supply Maximum dv/dt, dV_S/dt 50V/ns
ESD Classification ..... Class 1

Thermal Information

Thermal Resistance	θ_{jc}	θ_{ja}
Plastic DIP Package	68°C/W	85°C/W
Plastic SOIC Package	80°C/W	X°C/W

Linear Derating Factor (0W at T_J = +125°C)
Plastic DIP Package ..... 15mW/°C
Plastic SOIC Package ..... 13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions (T_J = 0°C to 125°C Unless Otherwise Noted, All Voltages Referenced to V_{SS} Unless Noted)

Offset Supply Voltage, V_S ..... -2.0V to 400V
Floating Supply Voltage, V_{BS} (V_B to V_S) ..... 10 to 15V
High Side Channel Output Voltage, V_{HO},V_{NHO} ..... 0 to V_{BS}
Fixed Supply Voltage, V_{CC} ..... 10 to 15V
Low Side Channel Output Voltage, V_{LO},V_{NLO} ..... 0 to V_{CC}
All Other Pin Voltages (SD,RT,CT,DIS,SS,FLT and EN) ..... 0 to V_{CC}

Discharge R_{dis} · C_t Product ..... 100ns Min.
Discharge Resistor Range, R_{dis} ..... 100KΩ to 50KΩ
Charging Resistor Range, R_T ..... 6.8KΩ to 400KΩ
Oscillator Capacitor Range. C_T ..... 100pF to 0.1μF
Oscillator Frequency Range ..... 300kHz Max.
Oscillator Capacitor Charge Current Range, I_{RT} ..... 21μA to TBD

Static Electrical Characteristics (V_{CC} = V_{BS} = 10V to 15V, GND = 0V and T_J = 0°C to +125°C, Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
I_{QCC}	Quiescent V_{CC} Current		-	7	-	mA
I_{QBS}	Quiescent V_{BS} Current		-	400	-	μA
I_{STBY}	Standby V_{CC} Current	R_T = 120K	-	700	-	μA
$I_{SFT/PWM}$	SS Current Source	$1/3V_{CC} < V_{SFT} < 2/3V_{CC}$	71	-	147	μA
V_{EN}	Input Threshold		-	$V_{CC}/2$	-	V
V_{EN-HYS}	Input Hysteresis		-	2	-	V
V_{UV}	Undervoltage Threshold		7.3	-	9.2V	V
V_{SD}	Short Detect Threshold		-	$V_{CC}/4$	-	V
I_{CT}	Oscillator Capacitor Charge Current	I_{RT} = 100μA, $V_{CC}/3 < V_{CT} < 2/3V_{CC}$	-	100	-	μA
V_{OL}	Drive Output Low Level	I_{SINK} = 67mA	-	-	0.4	V
I_O+	Drive Output Sourcing Current	LO, HO Tied Low	1.9	2.3	-	A
I_O-	Drive Output Sinking Current	LO, HO Tied High	2.0	2.5	-	A
I_{BUF}+	Drive NOT Output Sourcing Current	LO, HO Tied Low	-	200	-	mA
I_{BUF}-	Drive NOT Output Sinking Current	LO, HO Tied High	-	200	-	mA

Dynamic Electrical Characteristics $V_{CC} = V_{BS} = 10V$ to 15V, GND = 0V and $T_J = 0°C$ to +125°C, Unless Otherwise Specified

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
DRIVE CHANNEL (HO AND LO)						
tdr	Turn-On Rise Time	$C_L = 2000pF$	-	-	50	ns
tdf	Turn-Off Fall Time	$C_L = 2000pF$	-	-	50	ns
DRIVE NOT CHANNEL (HO AND LO)						
tdnr	Turn-On Rise Time	$C_{BUF} = 200pF$	-	25	35	ns
tdnf	Turn-Off Fall Time	$C_{BUF} = 200pF$	-	25	35	ns
tsd	Short Detect Propagation Delay		-	950	-	ns
	Oscillator Frequency Tolerance		-	5	-	%
t_{DTMIN}	Minimum Dead Time	Rdis • $C_T = 100ns$, $R_T = 120K$, $V_{CC} = 12V$	150	-	270	ns
t_{DBUF}	BufferFET-Off to MainFET-On Delay Time	$C_L = 2000pF$, $C_{BUF} = 200pF$	-	165	-	ns
	Oscillator Output Buffer Delay Time		70	-	115	ns
t_{SSDLY}	Soft-Start Propagation Delay Time		-	1.15	-	µs

HARRIS SEMICONDUCTOR

ICL7644, ICL7645 ICL7646, ICL7647

May 1992

Low Voltage Step-Up Converters

Features

- +5V at 40mA From a 1.5V Source
- +5V at 150mA From a 3V Source (See Table 1)
- Guaranteed Start-up at 1.15V
- Standby Mode 80μA Quiescent Current
- Low Battery Indication
- Power Ready Function
- Shutdown Feature 5μA Max Quiescent
- Pin to Pin Compatible to MAX65X Series
- Efficiency 75% at 1.2V Input

Applications

- Battery Powered Devices
- Single Cell Instruments
- Solar Powered Systems
- Pagers and Radio Controlled Receivers
- Portable Instruments
- 4-20mA Loop Powered Instruments

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL764XCPD	0°C to +70°C	14 Pin Plastic DIP
ICL764XCBD	0°C to +70°C	14 Pin SOIC
ICL764XIPD	-40°C to +85°C	14 Pin Plastic DIP
ICL764XIBD	-40°C to +85°C	14 Pin SOIC

Description

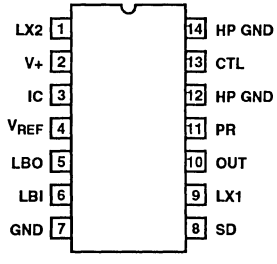
The ICL7644, ICL7645 and ICL7646 are low power fixed +5V output step-up DC-DC converters designed for operation from very low input voltages. All control functions and a power FET are contained in the ICL7644, ICL7645 and ICL7647, minimizing external components. The ICL7646 contains an output pin to drive an external FET when higher output currents are required. A control pin changes between high power and low power standby modes. Standby mode allows operating for extended periods with minimum battery drain, and a power ready function is available for controlling external devices when the device is switched between standby and high power. In high power mode, the output current is approximately 40mA; in standby mode, it is about 500μA.

Minimum startup voltage is 1.15V, but once started the device will operate to lower voltages as the battery discharges. A separate low battery monitor is available; it can be used at its default value of 1.17V or may be adjusted by the designer to any higher voltage.

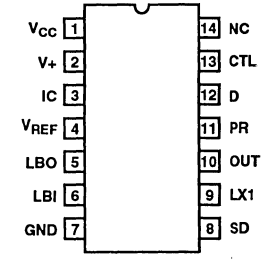
The ICL7644, ICL7646 and ICL7647 are optimized for single cell (1.15V to 1.6V) battery operation and can also be used with input voltages up to 4.0V. The ICL7645 is designed for two cell (or single lithium cell) operation with typical battery voltages of 2.0V to 3.6V. The ICL7647 is identical to the ICL7644 except its output voltage is preset to +3V. The ICL764X series of products also offer a shutdown feature. In the shutdown mode the quiescent current is less than 5μA.

Pinouts

ICL7644, ICL7645 & ICL7647
TOP VIEW



ICL7646
TOP VIEW



7 REGULATORS/ POWER SUPPLIES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2781.2**

Absolute Maximum Ratings

Peak Voltage at LX1 Pin ..... +16V
Peak Voltage at LX2 or V_{CC} Pin ..... +6.6V
Supply Voltage to L1 ..... +15V
Supply Voltage to L2, V_{CC} ..... +5.6V
Peak Current, LX1 ..... 50mA
Peak Current, LX2 ..... 1.6A
LBO Output Current 50mA
Input Voltage, CTL, LBI (See Note) ..... -0.3V to (V^+ +0.3V)

Storage Temperature ..... -65°C to +160°C
Lead Temperature (Soldering, 10 Sec) ..... +300°C
Power Dissipation:
Plastic DIP (Derate 10mW/°C above +70°C) 800mW
SOIC (Derate 8.7mW/°C above +70°C) 695mW

NOTE: V^+ is generated at LX1. In low current mode, it is 4.5V to 5.6V (2.6V to 3.6V on ICL7646); in high current mode, it is 10V to 15V.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range:
ICL764XCXX ..... 0°C to +70°C ICL764XIXX ..... -40°C to +85°C

Electrical Specifications

ICL7644, ICL7646, ICL7647 (GND = 0V, V_{BATT} = 1.2V, T_A = 25°C, Unless Otherwise Specified.)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Voltage	V_{OUT}	ICL7644, ICL7646 T_A = Over Temp.*	4.5	5.0	5.5	V
		ICL7647 T_A = Over Temp.*	2.7	3.0	3.3	V
Minimum Input Voltage to LX1	V_{LX1}	I_L = 0µA (Note 1)	-	0.9	1.0	V
Minimum Startup Voltage to LX1	V_{LX1}	I_L = 0µA	-	0.9	1.15	V
Input Voltage to LX2	V_{LX2}		0.5	-	5.6	V
Peak LX2 Switch Current	I_{LX2}	ICL7644, ICL7647 (Note 1)	-	-	1.5	A
Standby Current	I_Q	I_L = 0µA, CTL = Open	-	80	-	µA
Switching Frequency	f_O	V_{BATT} = 1.0 to 1.6V	15.5	18	24	kHz
LX2, D Switch Duty Cycle	%ON	ICL7644, ICL7646	66	75	80	%
		ICL7647	50	66	75	%
LX2, D Switch On Time	t_{ON}	ICL7644, ICL7646	27	42	49	µs
		ICL7647	20	37	47	µs
LX2 On Resistance	R_{DSON}	ICL7646, ICL7647 (Note 1)	0.40	-	0.67	Ω
D Output Saturation Current		ICL7646, Source Sink (Short Circuit Current)	-	-25	-	mA
			-	100	-	mA
Low Battery Input Threshold Voltage	V_{LBI}		1.12	-	1.18	V
Low Battery Input Threshold Tempco			-	-0.5	-	mV/°C
Low Battery Input Bias Current	I_{LBI}		-	0.01	10	nA
Low Battery Output	V_{LBO}	V_{LBI} < 1.12V, I_{LBO} = 1.6mA	-	-	0.4	V
		V_{LBI} > 1.18V, I_{LBO} = -1µA	V^+-1	-	-	V
Power Ready	V_{PR}	PR High, I_{PR} = -1µA	-	V_{OUT} -0.2	-	V
		PR Low, I_{PR} = 1µA	-	0.3	-	V
CTL Input Threshold	V_{CTL}		-	0.07	-	V
Efficiency		5mA ≤ I_{LOAD} ≤ 40mA	-	75	-	%

NOTE:

1. Not tested, guaranteed by design and characterization.

* Commercial Temperature Range = 0°C to +70°C
Industrial Temperature Range = -40°C to +85°C

Electrical Specifications ICL7645 (GND = 0V, V_{BATT} = 2.4V, T_A = +25°C, Unless Otherwise Specified.)

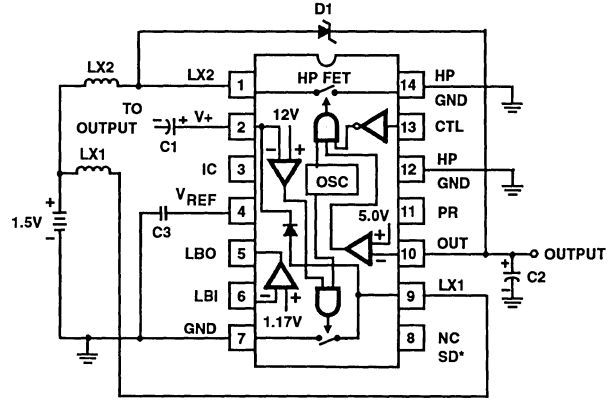
PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Voltage	V_{OUT}	T_A = Over Temperature*	4.5	5.0	5.5	V
Minimum Input Voltage to LX1	V_{LX1}	I_L = 0µA	-	0.9	1.0	V
Minimum Startup Voltage to LX1	V_{LX1}	I_L = 0µA (Note 1)	-	0.8	1.15	V
Input Voltage to LX2	V_{LX2}		-	-	5.6	V
Peak LX2 Switch Current	I_{LX2}	(Note 1)	-	-	1.5	A
Standby Current	I_Q	I_L = 0µA, CTL = Open	-	40	-	µA
Switching Frequency	f_O	V_{BATT} = 2.0 to 3.2V	15.5	18	24	kHz
Switch Duty Cycle	%ON		40	50	60	%
Switch On Time	t_{ON}		15	28	38	µs
LX2 On Resistance	R_{DSON}	(Note 1)	0.40	-	0.67	Ω
Low Battery Input Threshold Voltage	V_{LBI}		1.12	-	1.18	V
Low Battery Input Threshold Tempco			-	-0.5	-	mV/°C
Low Battery Input Bias Current	I_{LBI}		-	0.01	10	nA
Low Battery Output	V_{LBO}	V_{LBI} < 1.12V, I_{LBO} = 1.6mA	-	-	0.4	V
		V_{LBI} > 1.18V, I_{LBO} = -1µA	V^+-1	-	-	V
Power Ready	V_{PR}	PR High, I_{PR} = -1µA	-	V_{OUT} -0.2	-	V
		PR Low, I_{PR} = 1mA	-	0.3	-	V
Input Threshold	V_{CTL}		-	0.7	-	V
Efficiency		5mA ≤ I_{LOAD} ≤ 150mA	-	75	-	%

NOTE:

1. Not tested, guaranteed by design and characterization.

* Commercial Temperature Range = 0°C to +70°C
Industrial Temperature Range = -40°C to +85°C

Functional Block Diagram



Pin Description

PIN NUMBER		SYMBOL	FUNCTION
ICL7646	ICL7644, ICL7645, ICL7647		
-	1	LX2	Output drain of high power N-channel MOSFET.
1	-	V_{CC}	Connect to battery positive terminal.
-	2	V+	Output of low power up converter; 10 to 15V in high power mode. 4.5V to 5.5V in standby mode.
2	-	V+	Output of low power up converter. 10 to 15V in high power mode. 2.6 to 3.6V in standby mode.
3	3	I/C	Internal Connection. Leave this pin unconnected. "Do not ground."
-	7	GND	Low power ground.
4	4	V_{REF}	1.295V bandgap reference output; should be decoupled with a capacitor to pin 7. This terminal is high impedance and cannot source or sink current.
5	5	LBO	Low battery monitor output. Sinks 1.6mA when LBI is less than 1.17V, otherwise sources 1µA from V+.
6	6	LBI	Low battery monitor input. Very high input impedance.
8*, 14	8*	NC *SD	*Shutdown pin. Allows user to turn part off by grounding pin 8.
9	9	LX1	Output (drain) of low power N-channel power driver.
10	10	OUT	+5V (+3V on ICL7647). Feedback (input) pin for high power operation; output pin in standby mode.
11	11	PR	Power ready output; high (+5V on ICL7644, 7645, 7646; +3V on ICL7647) when high power converter is ready to supply power.
7	12, 14	HP, GND	High power ground.
13	13	CTL	Control mode switch input; open circuit or high for standby mode, ground for high power mode.
12	-	D	Driver output to external FET. Output voltage swings from GND to V_{OUT}.

Low Voltage Step-Up Converters

Operating Principle

The ICL7644, ICL7645, ICL7646 and ICL7647 are flyback, or boost converters: energy from the battery is first stored in a coil and then discharged to the load. Essentially, the circuit consists of a battery in series with a coil, a high power FET, rectifier, and filter, as shown in Figure 1. When the switch is closed, current builds up in the coil, creating a magnetic field. During the second half, or flyback part of the cycle, the power FET opens, the magnetic field collapses and the voltage across the inductor reverses polarity, adding to the voltage of the battery and discharging through the rectifier into the load.

The switch is controlled by a constant frequency oscillator whose output is gated on and off by a comparator that monitors the output voltage. When the output voltage is above the comparator threshold, the power FET skips an entire cycle of the oscillator. This pulse skipping technique varies the average duty cycle to achieve regulation, rather than varying the period or duty cycle of each cycle of the power FET; it eliminates a number of linear circuits that would otherwise add both circuit complexity and quiescent operating current. The key to operating CMOS circuitry from a 1V supply depends on a technique called bootstrapping. A specially designed oscillator starts itself up on a very low voltage and builds up (or bootstraps) a higher voltage that in turn is used as the supply for further operation. This supply yields higher efficiency because the bootstrapped voltage drives the gate of the internal power FET transistor to lower on resistance.

When power is first applied, the circuit is very inefficient (for the first cycle) until a higher voltage is generated on the flyback half of the first cycle. This higher voltage is rectified and filtered, and powers the whole IC (and thus the oscillator) for the next cycle. Since each cycle generates a higher voltage for the next cycle, the voltage builds up very rapidly. An internal regulator limits the voltage to about 12V. The load for this supply is only the CMOS chip itself, so the requirements for the components, particularly the external inductor L1, are very broad. This voltage is brought out to the V+ pin and is connected to a tantalum capacitor for filtering.

This bootstrapped 12V drives an internal N-channel power FET that furnishes the switching power for the load. Since the gate of this FET is driven from a 12V supply, it has a very low on resistance and can efficiently switch high currents through a second inductor, L2. It is the power stored in this second inductor that is delivered to the 5V load via an external Schottky diode. The rectified and filtered 5V output is connected back to the OUT pin to provide feedback. The ICL7644/7645/7646/7647 thus has two separate switching circuits and uses two separate inductors.

Circuit Details

A typical application circuit is shown in Figure 2. The higher value inductor, L1, is typically 4.7mH, and may have fairly high losses. It is used for the low power section of the circuit and is rectified by an internal diode and routed to pin 2, V+, where it is filtered by an external capacitor, C1. The second inductor, L2, varies from 39µH to 500µH, depending on input voltage and load current. It must have low series resistance and sufficient core material to handle the load power without saturating. The inductor is connected to pin 1 (LX2), the drain of the Low Power FET, and is rectified by an external Schottky diode, D1, and filtered by an external capacitor, C2. This is the main +5V output (+3V on the ICL7647), and it is connected to OUT, pin 10, which is the feedback input in high power mode. Figure 3 shows a similar circuit for the ICL7646 using an external FET for higher power output.

Low Power Standby Mode

A control pin (CTL) is available for putting the device into standby mode to conserve power. When this pin is held low, the IC operates in the high power mode, if it is driven high or left open the following occurs: the POWER READY (PR) pin is driven low, the high power FET is gated off, the 12V (V+) switching supply is reduced to 5V (+3V on the ICL7647) and is connected to the V_{OUT} pin.

By lowering the internal 12V supply to 5V, the leakage currents of the CMOS circuits and the losses associated with its voltage reference and oscillator are reduced to a minimum. The internal low power 5V supply can furnish up to 500µA, and it is connected to the normal 5V output pin (OUT) to supply current to the load, keeping alive standby circuits.

Power Ready Output Pin

During initial start up (and when placed in standby mode), the ICL7644/7645/7646/7647 internal voltages are too low to drive the power FET efficiently. A separate comparator determines when this voltage has reached a high enough value to drive the FET. The output of this comparator gates the FET drive voltage. This scheme extends battery life in standby mode and prevents the power FET from stalling when switching to high power mode. The comparator output is also brought out to the POWER READY (PR) pin and can be used to control external circuits, further reducing battery drain.

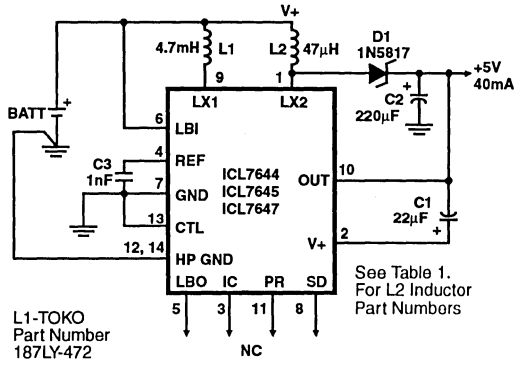
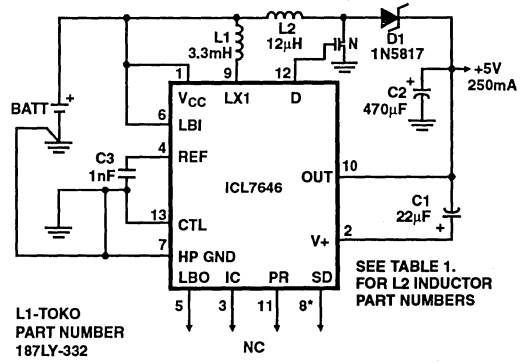


FIGURE 2. ICL764X TYPICAL APPLICATION



* Pin 8 used on 7646 series only

FIGURE 3. ICL7646 TYPICAL APPLICATION

Start Up and Mode Considerations

The ICL7644/7645/7646/7647 may be started up in either the low power (standby) or high power mode. When starting in the high power mode, both the low power switch and the high power switch start immediately. Whether or not the load is connected, the output voltage will rise to 5V in the first few cycles. The OUT pin becomes an input for feedback to control regulation.

If the high power load (greater than about 500µA) is connected to the OUT pin and the device is placed in the low power mode (CTL pin driven high or left open), the low power oscillator will have to furnish all of the 5V power via the OUT pin, and the low power oscillator will stall. **It is, therefore, important to disconnect any load currents (greater than 500µA) whenever the low power or standby mode is selected.** The POWER READY (PR) pin may be used to disconnect the load via an external transistor. This way the mode and connection of the high power load are both controlled through the CTL input.

Input Filtering

It is important to limit the rate of rise of the battery voltage when the circuit is first turned on with a mechanical switch or the installation of the battery(ies). A simple R-C network made up of the battery internal resistance and a 10µF tantalum capacitor placed at the battery side of L2 input is sufficient for this purpose. This capacitor also helps to absorb the (relatively) high peak currents that are drawn from the battery in the high power mode.

Output Filtering

It is also important to limit the speed at which V+ decreases to 5V when the mode is switched from high power to standby. This is accomplished by putting a 22µF capacitor between the V+ and OUT pins. Also, a 220µF capacitor placed on the OUT pin provides both filtering and serves to hold up the 5V during the switchover period. Without these capacitors, the 5V may spike negatively during the switchover.

Low Battery Function

A completely independent low battery monitor is built into the ICL764X series. Its input (LBI) is the + input of a CMOS comparator whose - input is connected to the internal 1.17V bandgap reference. This input can be connected directly to the battery in single cell circuits or connected to a high resistance voltage divider for higher voltage monitoring. The output (LBO) can sink 1.6mA or source several microamperes from V+.

Shutdown Function

The ICL764X series is equipped with a shutdown feature. Pin 8 is used to power the part down. During shutdown the part draws less than 5µA quiescent current. The part can be shutdown by grounding pin 8.

Inductor Selection

Low Power Coil

The choice of the low power inductor, L1, is not critical. A 4.7mH coil with a DC resistance of less than 40Ω is adequate for most applications. In general, higher inductance values allow lower start up voltages, while lower resistances yield lower quiescent current in standby mode. If the inductance is made too high, the low power (V+) output voltage and current are reduced. This in turn reduces the efficiency of the power section, so the +5V output (in standby mode) supplied less current. Lower values of inductance raise the minimum start up voltage.

High Power Coil

The high power coil, L2, must store most of the energy that flows into the load. Accordingly, it should have a powdered iron or ferrite core and should have low resistance to minimize losses. It also must have an adequate current rating to prevent saturation.

Calculating the worst case inductor for the high power section (LX2) of the ICL7644/7645/7646/7647 is a two step process:

1. Determine the smallest inductor value that will not cause the circuit to exceed the peak current rating of the ICL7644/7645/7647 with the highest expected input voltage (V_{INMAX}), the longest on time (t_{ONMAX}), and the lowest total resistance ($R_{(MIN)}$). $R_{(MIN)}$ is the sum of the minimum coil and FET resistances. Note that this peak current relates to the inductor and the FET switch and is several times the load current.

The following example assumes the minimum frequency $f_{O(MIN)}$ and the maximum % $ON_{(MAX)}$ for the calculation of $t_{ON(MAX)}$. Although the calculated value for $t_{ON(MAX)}$ is above that specified in the electrical characteristics table (49µs), the illustration is still a valid one that yields a worst case minimum inductor value.

NOTE: Units with both $f_{O(MIN)}$ and $\%_{ON(MAX)}$ values near the ends of the allowed distributions will be rejected for $t_{ON(MAX)}$.

From the Electrical Characteristics table:

I_{PK} LX2 = 1.5A

$R_{DSON(MIN)} = 0.4\Omega$

$f_{O(MIN)}$ = 15.500Hz

Duty Cycle Maximum, $\%ON_{(MAX)} = 0.8$

then:

$$t_{ON(MAX)} = \%ON_{(MAX)}/f_{O(MIN)} = 0.8/15500 = 51.6\mu s$$

Assume that the minimum coil resistance. $R_{COIL(MIN)}$ is:

$R_{COIL(MIN)} = 0.1\Omega$

The minimum total resistance, $R_{(MIN)}$ is:

$$R_{(MIN)} = R_{DSON(MIN)} + R_{COIL(MIN)} = 0.4 + 0.1 = 0.5\Omega$$

then:

$$I_{PK} = 1.5A = \frac{V_{IN(MAX)}}{R_{(MIN)}} \times \left[1 - e^{\frac{-R_{(MIN)} \times t_{ON(MAX)}}{L_{(MIN)}}}\right]$$

or:

$$L_{(MIN)}\ (\mu H) = \frac{-R_{(MIN)}\ t_{ON(MAX)}}{\ln\left[(1 - R_{(MIN)} \times I_{PK}/V_{IN(MAX)})\right]}$$

For a maximum input voltage of 1.56V (single alkaline cell), and a minimum coil resistance of 0.1Ω, the minimum permissible inductance for the ICL7644/7645/7647 is 39.37µH.

2. Having determined the minimum inductance ($L_{(MIN)}$) that keeps the peak current below the individual component ratings, we next calculate a new peak current (I'_{PK}) using the highest resistance ($R_{(MAX)}$), the lowest input voltage ($V_{IN(MIN)}$) and the shortest on time ($t_{ON(MIN)}$). Using these parameters, we will calculate the minimum available output (DC) current.

From the Electrical Characteristics table:

$R_{DSON(MAX)} = 0.67\Omega$

$f_{O(MAX)} = 24kHz$

Duty Cycle Minimum, $\%_{ON(MIN)} = 0.66$

then:

$tON(MIN) = \%ON(MIN)/f_{O(MAX)} = 0.66/24000 = 27.5\mu s$

Assume that the maximum coil resistance, $R_{COIL(MAX)}$ is:

$R_{COIL(MAX)} = 0.15\Omega$

The maximum total charging resistance, $R_{(MAX)}$ is:

$R_{(MAX)} = R_{DSON(MAX)} + R_{COIL(MAX)} = 0.82\Omega$

At the end of the ON period:

$$I'_{PK} = \frac{V_{IN(MAX)}}{R_{(MAX)}} \times 1\text{-}e^{-R_{(MAX)} \times t_{ON(MIN)}/L_{(MIN)}}$$

The energy stored in the coil is:

$$E_{COIL} = \frac{L_{(MIN)} \times I'^{2}_{PK}}{2}$$

And the power put into the coil is:

$$P_{COIL} = f_{O(MAX)} \times E_{COIL} = \frac{L_{(MIN)} \times I'^{2}_{PK} \times f_{O(MAX)}}{2}$$

The minimum DC output current, I_{OUT}, is:

$$I_{OUT(MIN)} = \frac{P_{LOAD}}{V_{LOAD}} = \frac{P_{COIL} - P_{LOSS}}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}} = \frac{P_{COIL} - I'^{2}_{PK} \times (R_{COIL(MAX)}/3) \times (1 - \%ON_{(MIN)})}{V_{OUT(MAX)} + V_{DIODE} - V_{IN(MIN)}}$$

Using a 47 ± 10% µH coil with a resistance of 0.15Ω, an input voltage of 1.1V, and the worst case highest output voltage of 5.5V. The calculated minimum DC output current is 32mA. This assumes a 0.3V forward drop in the 1N5818 diode.

When selecting a coil, care should be exercised to insure that the minimum inductance value, including all the manufacturing tolerances, is never lower than the calculated inductance, or the peak current rating of LX2 may be exceeded. In addition, the current rating of the coil should be greater than the peak current used in the calculation (1.5A, normally), to avoid saturating the core.

If the worst case output current is too small, then either the minimum input voltage must be increased or the maximum input voltage should be decreased. It is always desirable to decrease the ratio between maximum and minimum input voltages. The coil resistance also has a significant effect on the output current, so selecting a lower coil resistance will increase the output current and increase the overall efficiency.

If no satisfactory value of inductance can be found for the desired current, the ICL7646 may be used with an external FET whose peak current exceeds 1.5A. The calculations are similar for the ICL7644 except the external FETs R_{DSON} and current rating should be substituted in the above equations.

If the worst case output current is significantly higher than the required load current, a higher inductance value may be used. This will tend to reduce the peak current and the ripple voltage. Be sure to adjust the coil resistance and recalculate all the values.

When the maximum battery voltage exceeds 1.65V, the ICL7645 should be used. Calculations for the ICL7645 are identical to the ICL7644 calculations, except that different values must be used for the maximum and minimum duty cycles.

In general, if a choice of batteries is available, higher input voltages are preferred for two reasons. First, as the input voltage approaches 1V, the load on the battery increases while the losses increase. The losses become so dominant that efficiency suffers and little output current can be maintained. Second, certain losses, such as the coil resistance and the FET on resistance are less significant with higher input voltages. This means not only higher efficiency, but a greater range of input voltages are tolerable; this in turn means that more of the chemical energy can be converted into electricity. For example, three NiCd cells, with a fully charged voltage of 4.05V, may still be used down to 1.1V (with about 5mA of 5V output current), far beyond the normal life expectancy.

The inductance values for commonly encountered battery operated power supplies are tabulated in Table 1.

TABLE 1. MINIMUM INDUCTANCE FOR COMMON BATTERIES

BATTERY TYPE	BATTERY VOLTAGE		OUTPUT		COIL SPECIFICATIONS (L2) TOKO 8RBS 262LYF SERIES		
	MIN	MAX			µH*	OHMS	PART NO.
1 NiCads (ICL7644)	1.15V	1.35V	5V	43mA	39	0.09	-0087K
1 Alkaline (ICL7644)	1.20V	1.55V	5V	43mA	47	0.10	-0088K
2 Alkaline (ICL7644)	2.5V	3.5V	5V	150mA	33	0.80	-0086K
2 NiCads (ICL7645)	2.30V	2.70V	5V	64mA	68	0.16	-0090K
2 Alkalines (ICL7645)	2.40V	3.10V	5V	62mA	82	0.17	-0091K
1 Lithium (ICL7645)	2.60V	3.60V	5V	64mA	100	0.22	-0092K
1 NiCad (ICL7646)**	1.15V	1.35V	5V	250mA	12	0.049	-0081K
1 Alkaline (ICL7646)**	1.20V	1.55V	5V	275mA	6.8	0.037	-0079M
1 Alkaline (ICL7647)	1.20V	1.55V	3V	60mA	39	0.09	-0087K

* Coils are from Toko. Inductance (µH) is the MINIMUM allowed for the listed battery voltage range (Battery Voltage: MIN, MAX). Lower values are not recommended, except when using the 7646 converters since they use an external MOSFET. If less current than listed in the Output column is needed, a higher inductance coil will reduce losses. The optimum inductance varies inversely with required output current if all other conditions are unchanged.

** These ICL7646 circuits use an external current switch. Peak switch current is typically 3.5A.

Capacitor Selection

The high current fast rise-time pulses associated with switching power supplies demand good grounding and bypassing techniques. The ICL7644/7645/7647 have 3 ground pins to improve grounding. In addition, the internal voltage reference is brought out for connection to an external 1nF capacitor, minimizing noise and modulation on the reference.

The two output voltages, V+ and +5V should be filtered with tantalum capacitors, or other capacitors with low effective series resistance, to minimize transients. If aluminum electrolytic capacitors are used, they should be paralleled with 0.1µF disc ceramics.

Selecting Low Power Switching Diodes

The ICL7644/7645/7646/7647 use one external diode, and this diode must be a Schottky. A common Schottky type that performs well is the 1N5818.

In applications where standby current must be minimized, the diode's reverse leakage characteristics are especially important. The ICL7644/7646/7647 (40µA for the ICL7645) standby current is typically 80µA, while the reverse current of some Schottky rectifiers can exceed this value, particularly at high temperature. If necessary, diode leakage can be reduced with higher voltage Schottky types such as 1N5817. If standby mode is not used or is used only for short periods, then diode leakage is not a significant additional loss compared to the normal load current and need not be considered.

Rectifier Selection

The ICL7644-7647 use one external rectifier. To achieve specified performance at low voltage, a Schottky type, such as the 1N5818, is recommended because it combines low forward voltage drop with fast switching speed. This maximizes power conversion efficiency and output current when the DC-DC converter is in high power mode. One drawback of Schottky rectifiers is relatively high reverse leakage current (at 5V reverse, 1N5818 leakage is typically 60µA at +25°C and 450µA at +75°C), which is quite large with respect to the circuit's quiescent current in standby mode (typical standby current ICL7644/7646/7647 and ICL7644/7646/7647: 80µA, ICL7645: 40µA). If standby mode is not used or used only for short periods, reverse leakage is not a significant additional loss compared to the normal load current, and need not be considered.

If quiescent operating current is a primary concern, or if the ICL7644-7647 spends most of its time in standby mode, a silicon rectifier such as the 1N4933 or Unitrode UES1001 may be preferred. Silicon rectifiers have less reverse leakage current than do Schottky rectifiers (1N4933 leakage current is typically 1µA at +25°C and 50µA at +100°C). In circuits where the standby mode is the predominant mode of operation, battery life may be extended by trading conversion efficiency for lower standby quiescent current.

Output Current vs. Input Voltage

Figures 4 through 7 show output current versus input voltage using typical inductor values for each part in the ICL7644-7647 series. Where curves end in the middle of the graphs, the peak current limit of the internal LX2 switch has been reached. A higher input voltage than indicated by that line (for the given inductor) may damage the device. Figure 6 assumes that an IRF541 MOSFET is used (0.085V maximum on resistance).

Dashed lines indicate regions where the LX2 current limit hasn't been exceeded, but the current rating of the selected coil has. The actual voltages where lines end or become dashed are indicated by arrows on the graphs. The output currents indicated by dashed lines can be achieved only with inductors of higher current rating than the indicated coil. The coils used in Figures 4, 5 and 7 are as follows:

INDUCTOR	TOKO PART NUMBER
33µH	-0086K
47µH	-0088K
100µH	-0092K
150µH	-0094K
220µH	-0096K

The coils used in Figure 6 are the Toko series inductors.

The graphs in Figures 4-7 were calculated using worst case data, so individual circuits may supply more current than indicated. If the coils' current ratings are not exceeded, smaller, lower-cost coils than those indicated may be used in low-current applications. Use the equations in the text to calculate worst case peak coil/switch current to be sure that a particular coil's current rating is sufficient.

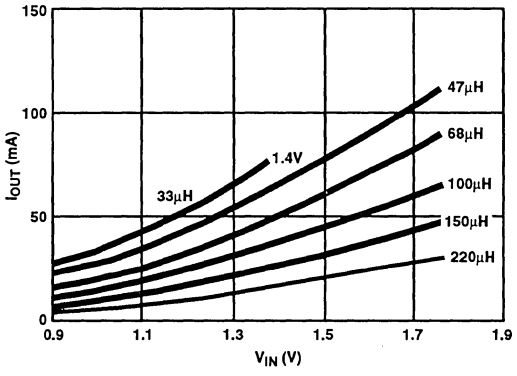


FIGURE 4. ICL7644, I_{OUT} vs. V_{IN} (V_{OUT} = 5V)

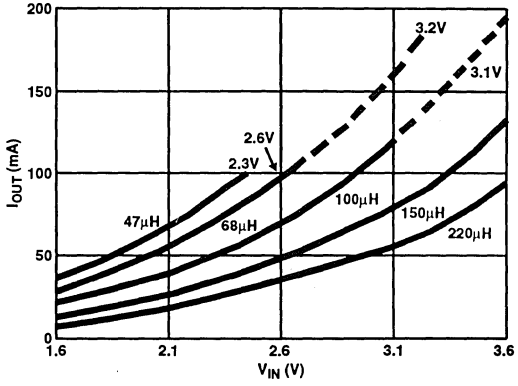


FIGURE 5. ICL7645, I_{OUT} vs. V_{IN} (V_{OUT} = 5V)

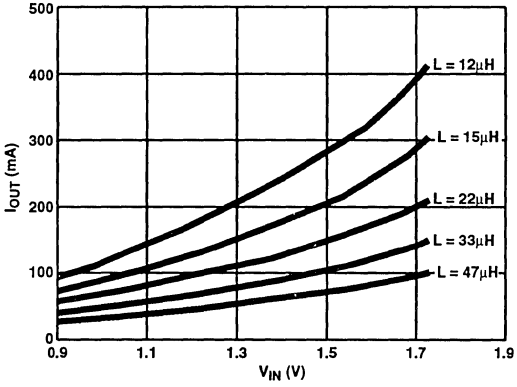


FIGURE 6. ICL7646, I_{OUT} vs. V_{IN} (V_{OUT} = 5V)

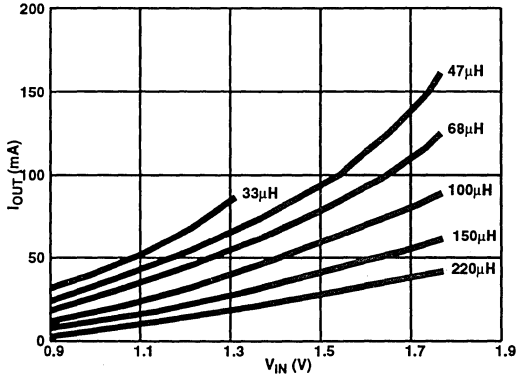


FIGURE 7. ICL7647, I_{OUT} vs. V_{IN} (V_{OUT} = 3V)

HARRIS SEMICONDUCTOR

ICL7660

May 1992

CMOS Voltage Converter

Features

- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication ($V_{OUT} = (-) nV_{IN}$)
- Typical Open Circuit Voltage Conversion Efficiency 99.9%
- Typical Power Efficiency 98%
- Wide Operating Voltage Range 1.5V to 10.0V
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- No External Diode Over Full Temperature and Voltage Range

Applications

- On Board Negative Supply for Dynamic RAMs
- Localized µProcessor (8080 Type) Negative Supplies
- Inexpensive Negative Supplies
- Data Acquisition Systems

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
ICL7660CTV	0°C to +70°C	TO-99 Can
ICL7660CBA	0°C to +70°C	8 Lead SOIC
ICL7660CPA	0°C to +70°C	8 Lead Mini-DIP
ICL7660MTV*	0°C to +70°C	TO-99 Can

* Add /883B to part number if 883B processing is required.

Description

The Harris ICL7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7660 performs supply voltage conversion from positive to negative for an input range of +1.5V to +10.0V, resulting in complemetary output voltages of -1.5V to -10.0V. Only 2 non-critical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660 can also be connected to function as a voltage doubler and will generate output voltages up to +18.6V with a +10V input.

Contained on the chip are a series DC supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

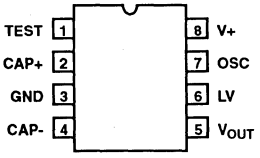
The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+3.5 volts to +10.0 volts), the LV pin is left floating to prevent device latchup.

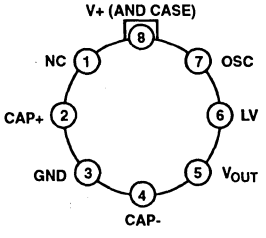
An enhanced direct replacement for this part, the ICL7660S, is now available and should be used for all new designs.

Pinouts

8 LEAD SOIC AND MINI-DIP
TOP VIEW



8 LEAD TO-99 CAN
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3072**

Absolute Maximum Ratings

Supply Voltage ..... +10.5V
LV and OSC Input Voltage ..... -0.3V to (V+ +0.3V) for V+ < 5.5V
(Note 1) (V+ -5.5V) to (V+ +0.3V) for V+ > 5.5V
Current into LV (Note 1) ..... 20μA for V+ > 3.5V
Output Short Duration ($V_{SUPPLY} \leq 5.5V$) ..... Continuous

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10sec) ..... 300°C
Power Dissipation (Note 2)
ICL7660CTV 500mW
ICL7660CPA 300mW
ICL7660MTV 500mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL7660M ..... -55°C to +125°C ICL7660C ..... 0°C to +70°C

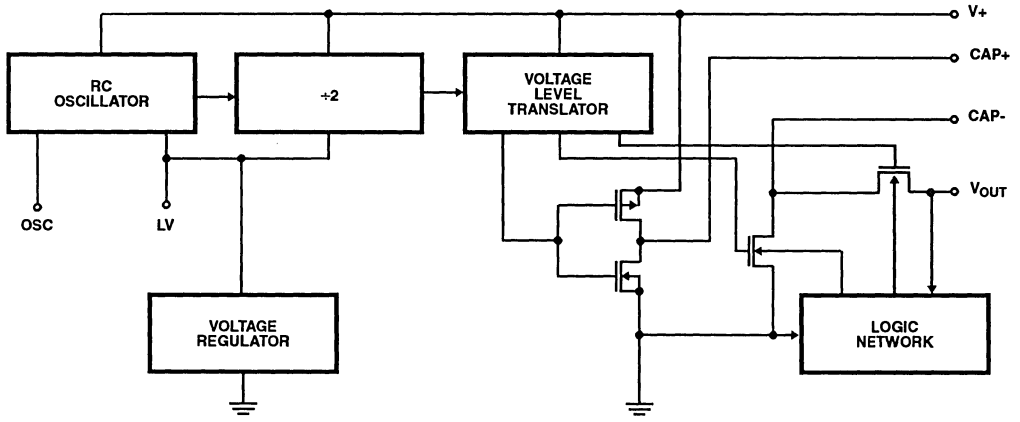
Electrical Specifications

$V^+ = 5V$, $T_A = +25°C$, $C_{OSC} = 0$, Test Circuit Figure 1 (Unless Otherwise Specified)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
I+	Supply Current	$R_L = \infty$		170	500	μA
V_L+	Supply Voltage Range - Lo	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to GROUND	1.5		3.5	V
V_H+	Supply Voltage Range - Hi	MIN ≤ T_A ≤ MAX, R_L = 10kΩ, LV to Open	3.0		10.0	V
R_{OUT}	Output Source Resistance	I_{OUT} = 20mA, T_A = +25°C		55	100	Ω
		I_{OUT} = 20mA, 0°C ≤ T_A ≤ +70°C			120	Ω
		I_{OUT} = 20mA, -55°C ≤ T_A ≤ +125°C			150	Ω
		V^+ = 2V, I_{OUT} = 3mA, LV to GROUND 0°C ≤ T_A ≤ +70°C			300	Ω
		V+ = 2V, I_{OUT} = 3mA, LV to GROUND, -55°C ≤ T_A ≤ +125°C			400	Ω
f_{OSC}	Oscillator Frequency			10		kHz
P_{Ef}	Power Efficiency	R_L = 5kΩ	95	98		%
$V_{OUT\ Ef}$	Voltage Conversion Efficiency	$R_L = \infty$	97	99.9		%
Z_{OSC}	Oscillator Impedance	V+ = 2 Volts		1.0		MΩ
		V = 5 Volts		100		kΩ

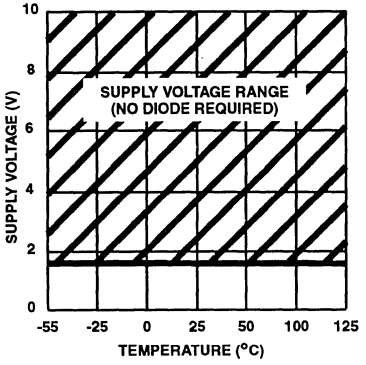
NOTES:
1. Connecting any input terminal to voltages greater than V+ or less than GROUND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the ICL7660.
2. Derate linearly above +50°C by 5.5mW/°C.

Functional Block Diagram

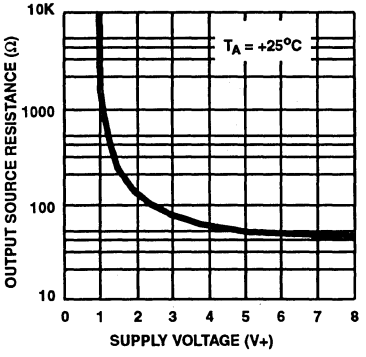


Typical Performance Characteristics (Test Circuit of Figure 1)

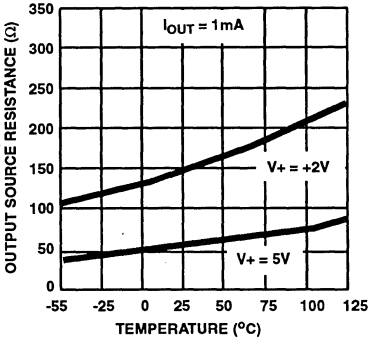
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE OF TEMPERATURE



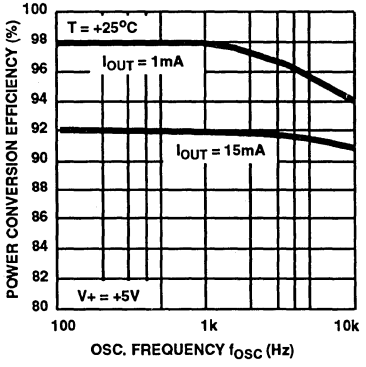
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



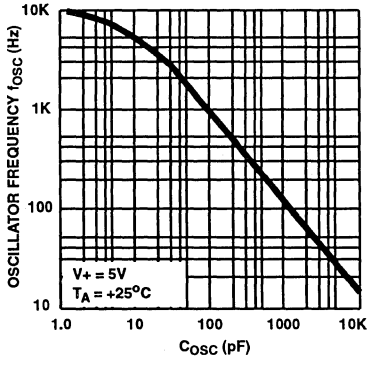
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



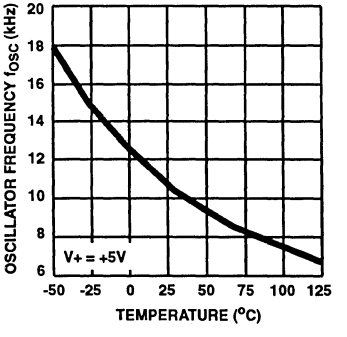
POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE

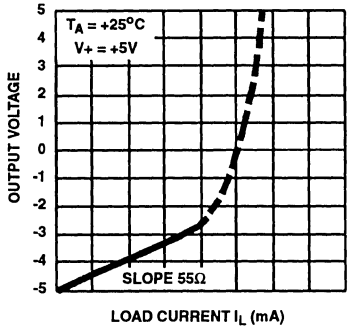


UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

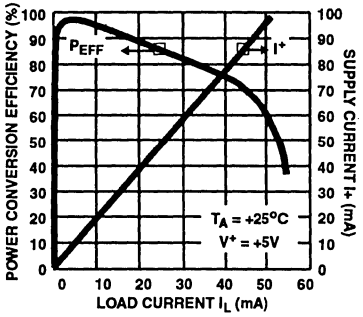


Typical Performance Characteristics (Continued) (Test Circuit of Figure 1)

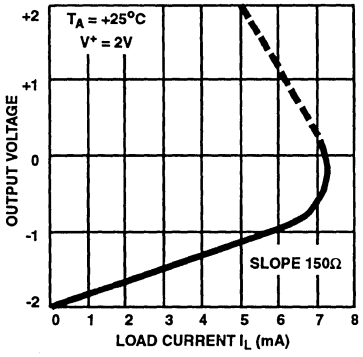
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



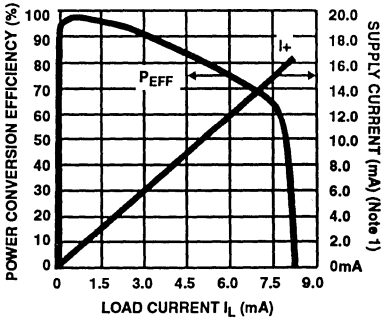
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



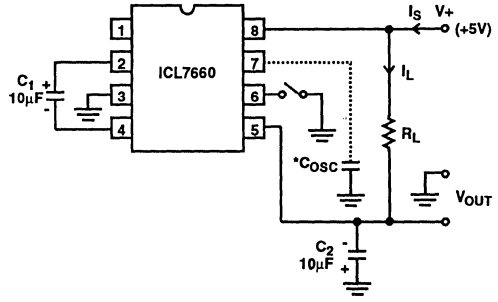
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



NOTE 3. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.



NOTE: For large values of C_{OSC} (>1000pF) the values of C_1 and C2 should be increased to 100µF.

FIGURE 1. ICL7660 TEST CIRCUIT

Detailed Description

The ICL7660 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7660 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL 7660, the 4 switches of Figure 2 are MOS power switches; S_1 is a P-channel device and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start-up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

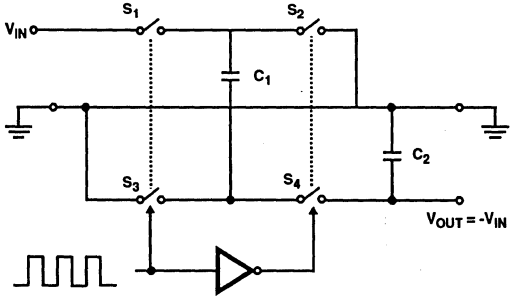


FIGURE 2. IDEALIZED NEGATIVE VOLTAGE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage converter can approach 100% efficiency if certain conditions are met.

A The driver circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

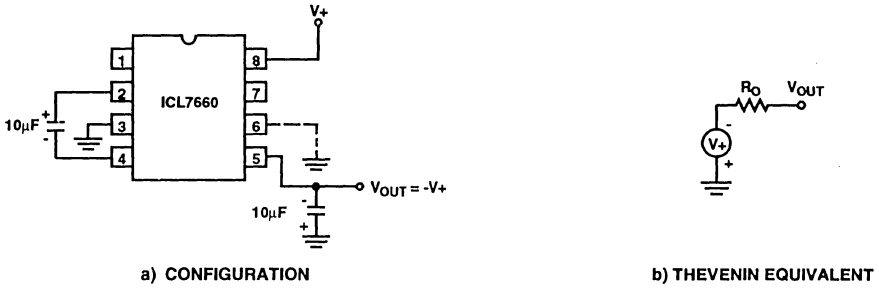
The ICL7660 approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's And Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 3.5 volts.
3. Do not short circuit the output to V+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GROUND.
5. If the voltage supply driving the ICL7660 has a large source impedance (25Ω - 30Ω), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions. A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 6).



a) CONFIGURATION

b) THEVENIN EQUIVALENT

FIGURE 3. SIMPLE NEGATIVE CONVERTER

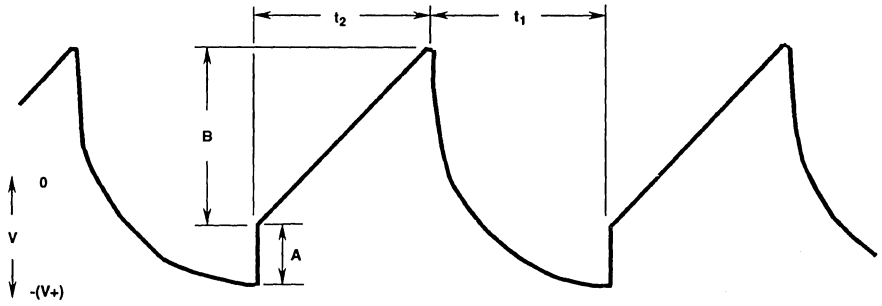


FIGURE 4. OUTPUT RIPPLE

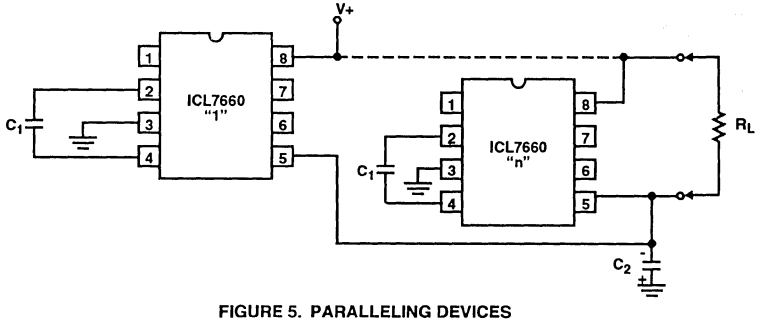


FIGURE 5. PARALLELING DEVICES

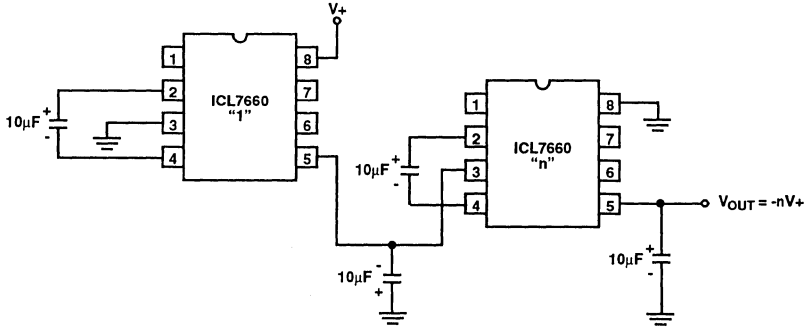


FIGURE 6. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660 for generation of negative supply voltages. Figure 3 shows typical connections to provide a negative supply negative (GND) for supply voltages below 3.5 volts.

The output characteristics of the circuit in Figure 3a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 3b. The voltage source has a value of -V+. The output impedance (R_o) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C1 and C2. A good first order approximation for R_o is:

$$R_0 \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{(f_{PUMP})(C1)} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2}, R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_0 \cong 2(R_{SW}) + \frac{1}{(f_{PUMP})(C1)} + 4(ESR_{C1}) + ESR_{C2}$$

RSW, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω @ 25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \bullet C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \bullet C1)$ term, but may have the side effect of a net increase in output impedance when $C_1 > 10\mu F$ and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where $f_{OSC} = 10kHz$ and $C = C_1 = C_2 = 10\mu F$:

$$R_0 \cong 2(23) + \frac{1}{(5 \bullet 10^3)(10^{-5})} + 4(ESR_{C1}) + ESR_{C2}$$

$$R_0 \cong 46 + 20 + 5(ESR_C)$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \bullet C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

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Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 4. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flow into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is $2 \bullet I_{OUT}$, hence the total drop is $2 \bullet I_{OUT} \bullet eSR_{C2}$ volts. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current to the load. The drop at B is $I_{OUT} \bullet t2/C_2$ volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{ripple} \cong \left[\frac{1}{2(f_{PUMP})(C2)} + 2(ESR_{C2}) \right] Iout$$

Again, a low ESR capacitor will reset in a higher performance output.

Paralleling Devices

Any number of ICL7660 voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of ICL7660)}}{n \text{ (number of devices)}}$$

Cascading Devices

The ICL7660 may be cascaded as shown to produced larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660 R_{OUT} values.

Changing the ICL7660 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

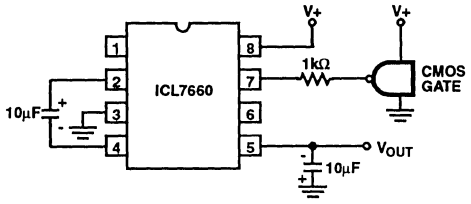


FIGURE 7. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the ICL7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C_1 and C_2 (from 10µF to 100µF).

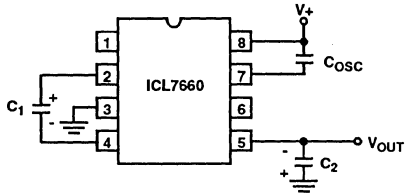


FIGURE 8. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7660 may be employed to achieve positive voltage doubling using the circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7660 are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) - (2VF) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 5 Volts and an output current of 10mA it will be approximately 60 ohms.

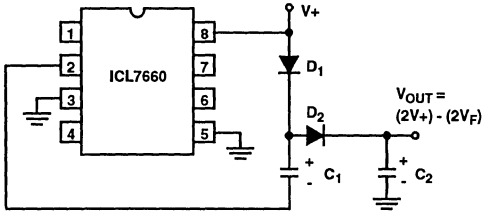


FIGURE 9. POSITIVE VOLTAGE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 10 combines the functions shown in Figures 3 and Figure 9 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

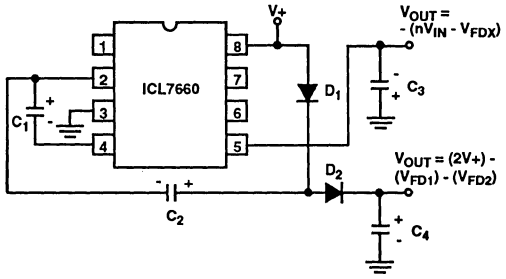


FIGURE 10. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15V can be converted (via +7.5, and -7.5) to a nominal -15V, although with rather high series output resistance (~250Ω).

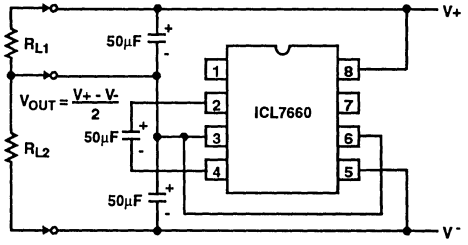


FIGURE 11. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7660 can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

Other Applications

Further information on the operation and use of the ICL7660 may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

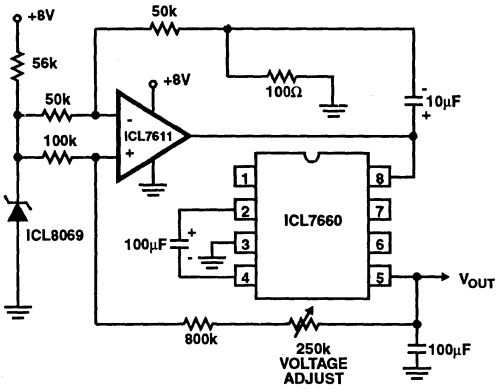


FIGURE 12. REGULATING THE OUTPUT VOLTAGE

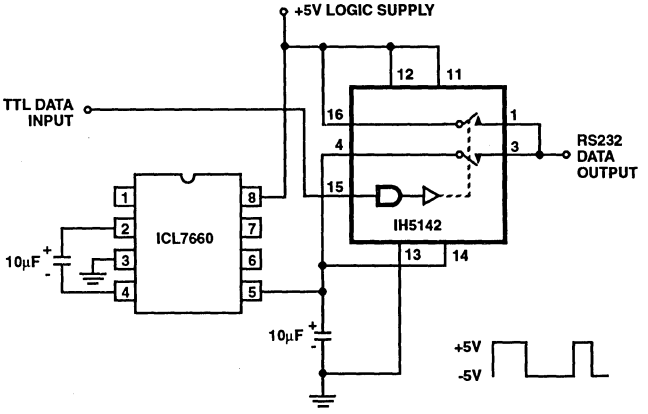


FIGURE 13. RS232 LEVELS FROM A SINGLE 5V SUPPLY

HARRIS SEMICONDUCTOR

ICL7660S

May 1992

Super Voltage Converter

Features

- Guaranteed Lower Max Supply Current for All Temperature Ranges
- Guaranteed Wider Operating Voltage Range 1.5V to 12V
- No External Diode Over Full Temperature and Voltage Range
- Boost Pin (Pin 1) for Higher Switching Frequency
- Guaranteed Minimum Power Efficiency of 96%
- Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%
- Improved SCR Latchup Protection
- Simple Conversion of +5V Logic Supply to ±5V Supplies
- Simple Voltage Multiplication $V_{OUT} = (-)nV_{IN}$
- Easy to Use - Requires Only 2 External Non-Critical Passive Components
- Improved Direct Replacement for Industry Standard ICL7660 and Other Second Source Devices

Applications

- Simple Conversion of +5V to ±5V Supplies
- Voltage Multiplication $V_{OUT} = \pm nV_{IN}$
- Negative Supplies for Data Acquisition Systems and Instrumentation
- RS232 Power Supplies
- Supply Splitter, $V_{OUT} = \pm V_S/2$

Description

The ICL7660S Super Voltage Converter is a monolithic CMOS voltage conversion IC that guarantees significant performance advantages over other similar devices. It is a direct replacement for the industry standard ICL7660 offering an ***extended*** operating supply voltage range up to 12V, with ***lower*** supply current. ***No external diode*** is needed for the ICL7660S. In addition, a ***Frequency Boost pin*** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in the Electrical Characteristics section. ***Critical parameters are guaranteed over the entire commercial, industrial and military temperature ranges.***

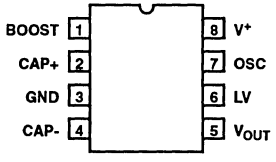
The ICL7660S performs supply voltage conversion from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of -1.5V to -12V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7660S can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. It can also be used as a voltage multiplier or voltage divider.

The chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

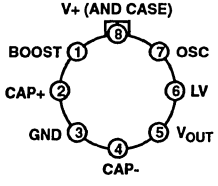
The "LV" terminal may be tied to GND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

Pinouts

8 LEAD SOIC AND MINI-DIP
TOP VIEW



TO-99 CAN
TOP VIEW



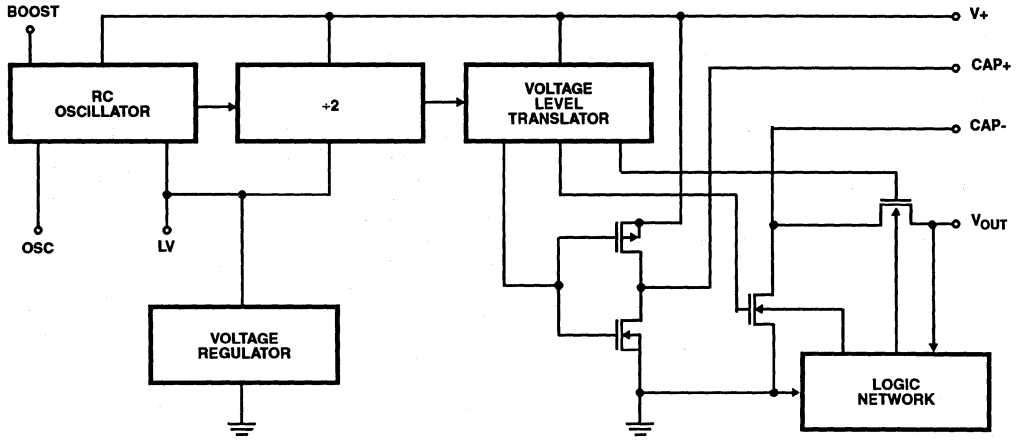
Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
ICL7660SCBA	0°C to +70°C	8 Lead SOIC
ICL7660SCPA	0°C to +70°C	8 Lead Mini-DIP
ICL7660SIBA	-25°C to +85°C	8 Lead SOIC
ICL7660SCTV	0°C to +70°C	TO-99
ICL7660SIPA	-25°C to +85°C	8 Lead Mini-DIP
ICL7660SITV	-25°C to +85°C	TO-99
ICL7660SMTV*	-55°C to +125°C	TO-99

* Add /883B to part number if 883B processing is required

File Number 3179

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage ..... +13.0V
LV and OSC Input Voltage (Note 1)
V+ < 5.5V ..... -0.3V to V+ + 0.3V
V+ > 5.5V ..... V+ -5.5V to V+ +0.3V
Current into LV (Note 1)
V+ > 3.5V 20µA
Output Short Duration
$V_{SUPPLY} \leq 5.5V$ ..... Continuous
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Power Dissipation (Note 2)
ICL7660SCTV 500mW
ICL7660SCPA 300mW
ICL7660SCBA 300mW
ICL7660SITV 500mW
ICL7660SIPA 300mW
ICL7660SIBA 300mW
ICL7660SMTV 500mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL7660SM ..... -55°C to +125°C
ICL7660SI ..... -25°C to +85°C
ICL7660SC ..... 0°C to +150°C

Electrical Specifications

$V^+ = 5V$, $T_A = +25°C$, OSC = Free running, Test Circuit Figure 2, Unless Otherwise Specified

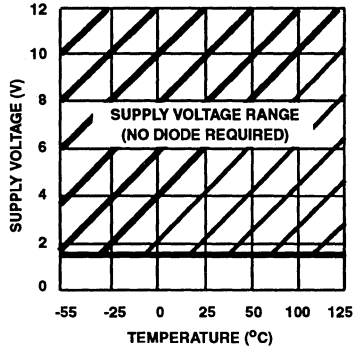
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Supply Current (Note 3)	I+	$R_L = \infty$, +25°C	-	80	160	µA
		0°C < T_A < 70°C	-	-	180	µA
		-25°C < T_A < +85°C	-	-	180	µA
		-55°C < T_A < +125°C	-	-	200	µA
Supply Voltage Range - High (Note 4)	V^+_H	R_L = 10K, LV Open, $T_{MIN} < T_A < T_{MAX}$	3.0	-	12	V
Supply Voltage Range - Low	V^+_L	R_L = 10K, LV to GND, $T_{MIN} < T_A < T_{MAX}$	1.5	-	3.5	V
Output Source Resistance	R_{OUT}	I_{OUT} = 20mA	-	60	100	Ω
		I_{OUT} = 20mA, 0°C < T_A < +70°C	-	-	120	
		I_{OUT} = 20mA, -25°C < T_A < +85°C	-	-	120	
		I_{OUT} = 20mA, -55°C < T_A < +125°C	-	-	150	
		I_{OUT} = 3mA, V^+ = 2V, LV = GND, 0°C < T_A < +70°C	-	-	250	
		I_{OUT} = 3mA, V^+ = 2V, LV = GND, -25°C < T_A < +85°C	-	-	300	
		I_{OUT} = 3mA, V^+ = 2V, LV = GND, -55°C < T_A < +125°C	-	-	400	
Oscillator Frequency	f_{OSC}	C_{OSC} = 0, Pin 1 Open or GND Pin 1 = V^+	5	10 35	-	kHz
Power Efficiency	P_{Eff}	R_L = 5kΩ $T_{MIN} < T_A < T_{MAX}$	96 95	98 97	-	%
Voltage Conversion Efficiency	$V_{OUT}Eff$	$R_L = \infty$	99	99.9	-	%
Oscillator Impedance	Z_{OSC}	V^+ = 2V	-	1	-	mΩ
		V^+ = 5V	-	100	-	kΩ

NOTES:

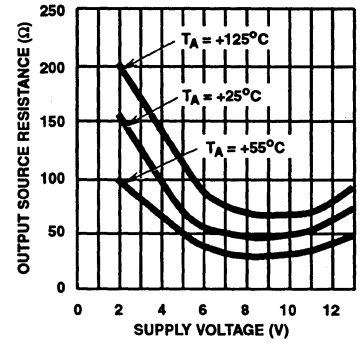
1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660s.
2. Derate linearly above 50°C by 5.5mW/°C
3. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, of the order of 5pF.
4. The Harris ICL7660S can operate without an external diode over the full temperature and voltage range. This device will function in existing designs which incorporate an external diode with no degradation in overall circuit performance.
5. All significant improvements over the industry standard ICL7660 are highlighted.

Typical Performance Characteristics (Test Circuit Figure 1)

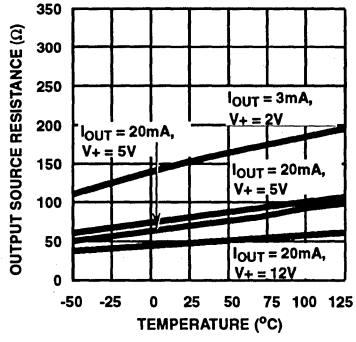
OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



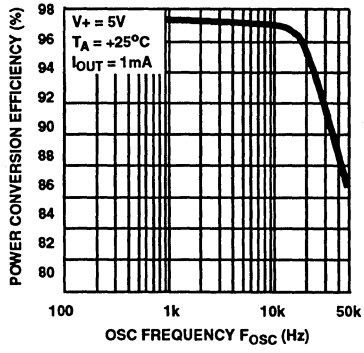
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



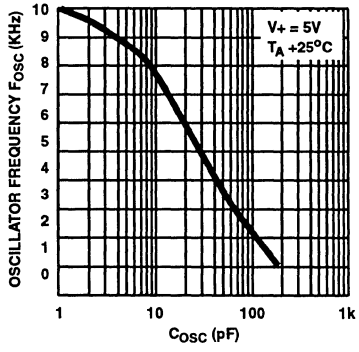
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



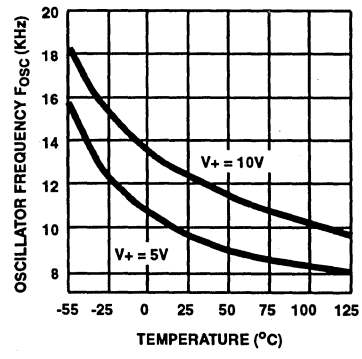
POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSCILLATOR FREQUENCY



FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE

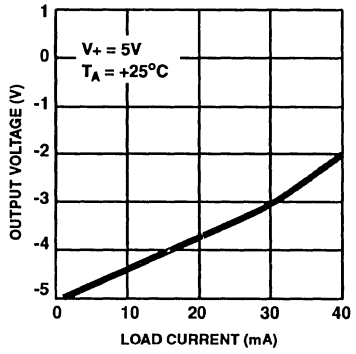


UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

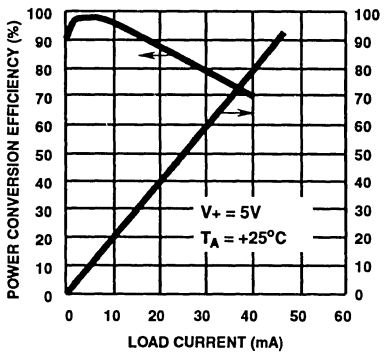


Typical Performance Characteristics (Test Circuit Figure 1) (Continued)

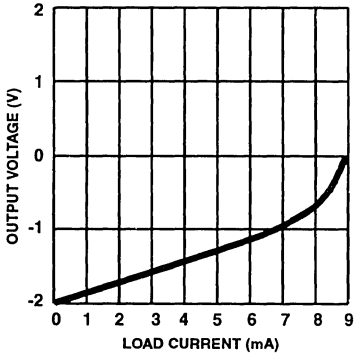
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



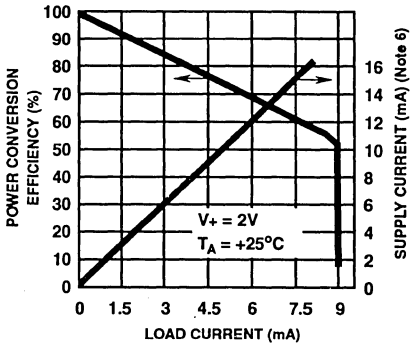
SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



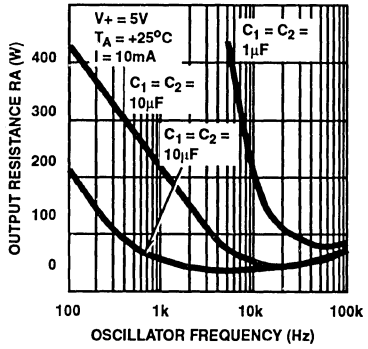
OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



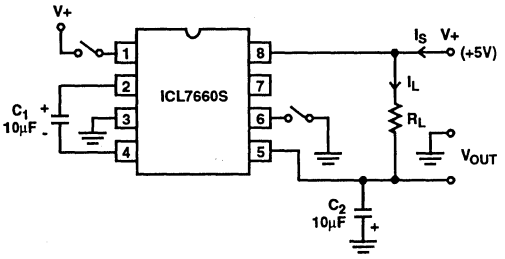
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



NOTE 6. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660, to the negative side of the load. Ideally, $V_{OUT} \simeq 2V_{IN}$, $I_S \simeq 2I_L$, so $V_{IN} \times I_S \simeq V_{OUT} \times I_L$.

Detailed Description

The ICL7660S contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic types. The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7660S approaches this ideal situation more closely than existing non-mechanical circuits.



NOTE: For large values of C_{OSC} (>1000pF) the values of C_1 and C_2 should be increased to 100µF

FIGURE 1. ICL7660S TEST CIRCUIT

In the ICL7660S, the 4 switches of Figure 2 are MOS power switches; S_1 is a P-channel devices and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start up, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7660S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660S is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

Theoretical Power Efficiency Considerations

In theory a voltage converter can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power.

B The output switches have extremely low ON resistance and virtually no offset.

C The impedance of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660S approaches these conditions for negative voltage conversion if large values of C_1 and C_2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = {}^1/_2C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

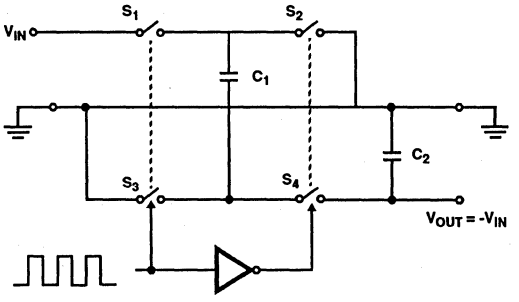


FIGURE 2. IDEALIZED NEGATIVE VOLTAGE CONVERTER

Do's and Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GND for supply voltage greater than 3.5 volts.
3. Do not short circuit the output to V^+ supply for supply voltages above 5.5 volts for extended periods, however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of C_1 must be connected to pin 2 of the ICL7660 and the + terminal of C_2 must be connected to GND.
5. If the voltage supply driving the 7660S has a large source impedance (25 - 30 ohms), then a 2.2µF capacitor from pin 8 to ground may be required to limit rate of rise of input voltage to less than 2V/µs.
6. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

   A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 6).

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660S for generation of negative supply voltages. Figure 3 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltage below 3.5 volts.

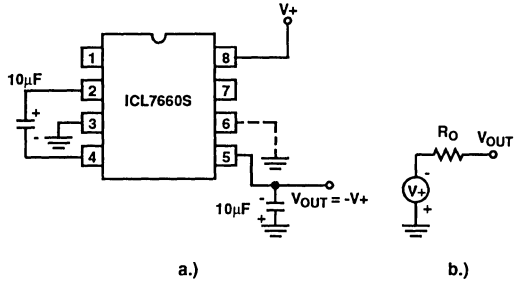


FIGURE 3. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

The output characteristics of the circuit in Figure 3 can be approximated by an ideal voltage source in series with a resistance as shown in Figure 3b. The voltage source has a value of -(V+). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C_1 and C_2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW}4 + ESR_{C1}) + \frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2},\ R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that:

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESR_{C1} + ESR_{C2}\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 23Ω at +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C_1)$ component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/f_{PUMP} \times C_1)$ term, but may have the side effect of a net increase in output impedance when C_1 > 10µF and these is not longer enough time to fully charge the capacitors every cycle. In a typical application where f_{OSC} = 10kHz and C = C_1 = C_2 = 10µF:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4 \times ESR_{C1} + ESR_{C2}$$

$$R_O \cong 46 + 20 + 5 \times ESR_C\Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/f_{PUMP} \times C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as 10Ω.

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 4. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flowing into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is 2 x I_{OUT}, hence the total drop is 2 x I_{OUT} x ESR_{C2} volts. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current the load. The drop at B is $I_{OUT} \times t_2/C_2$ volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left(\frac{1}{2 \times f_{PUMP} \times C_2} + 2\ ESRC_2 \times I_{OUT} \right)$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7660S voltage converters may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7660S})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7660S may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660S R_{OUT} values.

Changing the ICL7660S Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods described below.

By connecting the Boost Pin (Pin 1) to V+, the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately $3^1/_2$ times. The result is a decrease in the output impedance and ripple. This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller capacitors, e.g. 0.1µF, can be used in conjunction with the

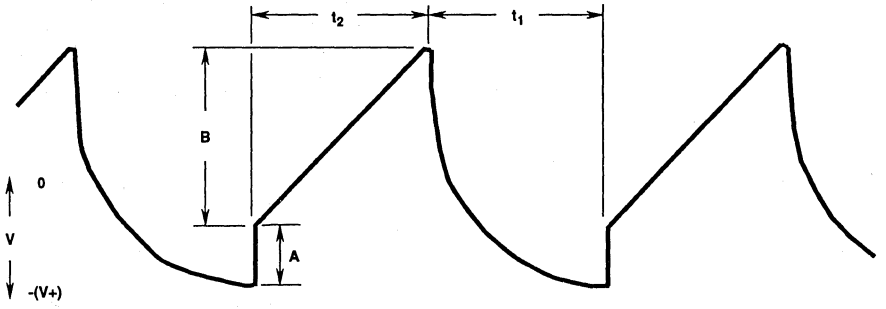


FIGURE 4. OUTPUT RIPPLE

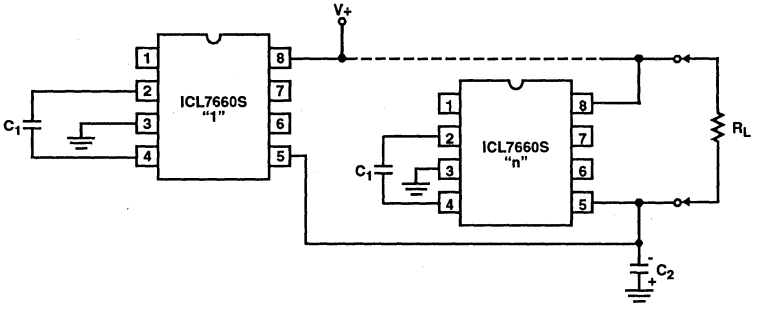
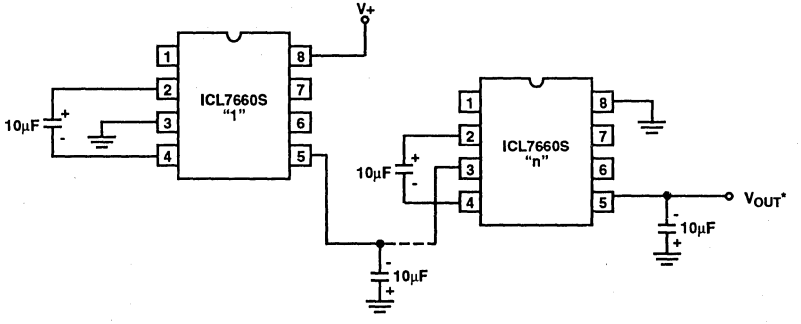


FIGURE 5. PARALLELING DEVICES



* V_{OUT} = -nV for 1.5V ≤ V+ ≤ 12V

FIGURE 6. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Boost Pin in order to achieve similar output currents compared to the device free running with $C_1 = C_2 = 10\mu F$ or $100\mu F$. (Refer to graph of Output Source Resistance as a Function of Oscillator Frequency).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent device latchup, a $1k\Omega$ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a $10k\Omega$ pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be $^1/_2$ of the clock frequency. Output transitions occur on the positive going edge of the clock.

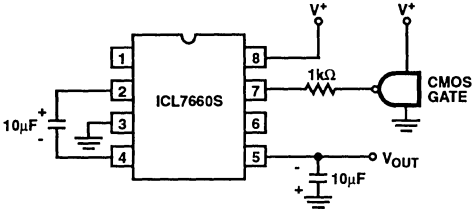


FIGURE 7. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the ICL7660S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and reservoir (C_2) capacitors; this is overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (Osc and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate corresponding increase in the value of C_1 and C_2 (from $10\mu F$ to $100\mu F$).

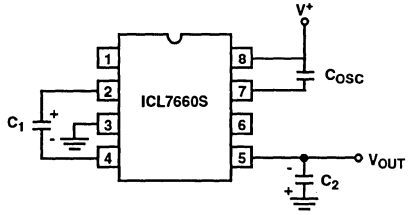
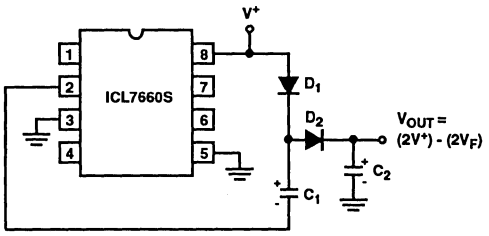


FIGURE 8. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7660S may be employed to achieve positive voltage doubling using he circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7660S are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage on C_1 plus the supply voltage (V+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) - ($2V_F$) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 5V and an output current of 10mA it will be approximately 60 ohms.



NOTE: D_1 and D_2 can be any suitable diode

FIGURE 9. POSITIVE VOLTAGE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 10 combines the functions shown in Figure 3 and 9 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

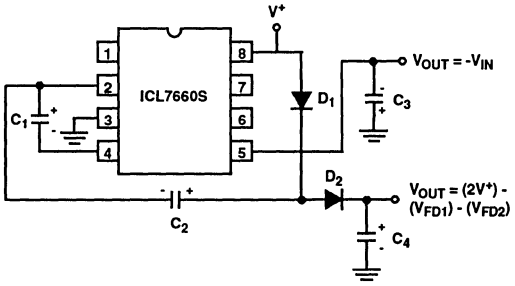


FIGURE 10. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

Voltage Splitting

The bidirectional characteristics can also be used to split a high supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents

can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15V can be converted (via +7.5, and -7.5 to a nominal -15V, although with rather high series output resistance (~250Ω).

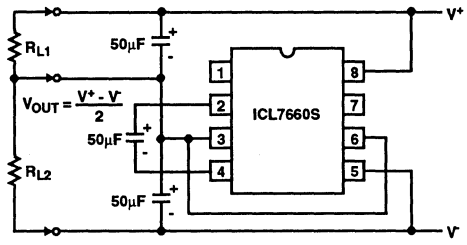


FIGURE 11. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In Some cases, the output impedance of the ICL7660S can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660S's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the 7660S, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

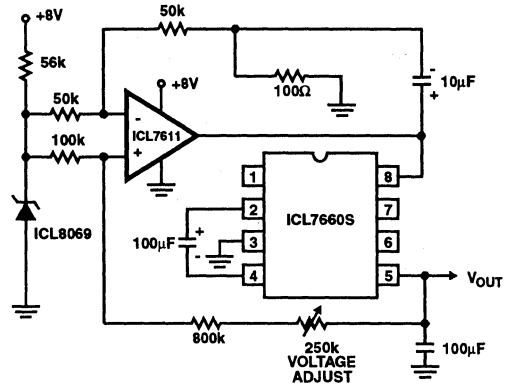


FIGURE 12. REGULATING THE OUTPUT VOLTAGE

Other Applications

Further information on the operation and use of the ICL7660S may be found in A051 "Principals and Applications of the ICL7660 CMOS Voltage Converter".

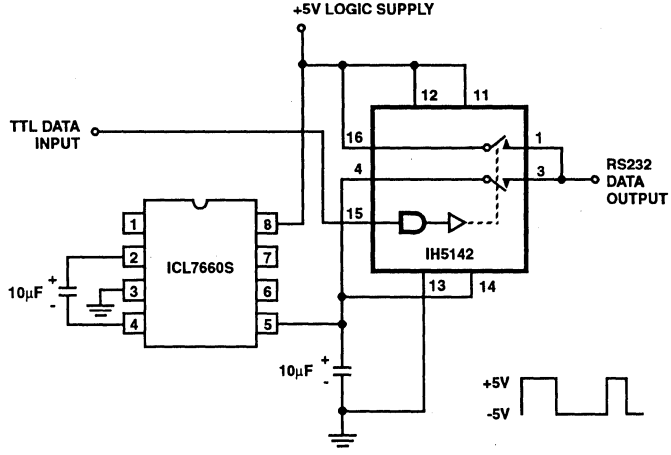


FIGURE 13. RS232 LEVELS FROM A SINGLE 5V SUPPLY

HARRIS SEMICONDUCTOR

ICL7662

May 1992

CMOS Voltage Converter

Features

- **No External Diode Needed Over Entire Temperature Range**
- **Pin Compatible With ICL7662**
- **Simple Conversion of +15V Supply to -15V Supply**
- **Simple Voltage Multiplication ($V_{OUT} = (-)nV_{IN}$)**
- **99.9% Typical Open Circuit Voltage Conversion Efficiency**
- **96% Typical Power Efficiency**
- **Wide Operating Voltage Range 4.5V to 20.0V**
- **Easy to Use - Requires Only 2 External Non-Critical Passive Components**

Applications

- **On Board Negative Supply for Dynamic RAMs**
- **Localized µProcessor (8080 Type) Negative Supplies**
- **Inexpensive Negative Supplies**
- **Data Acquisition Systems**
- **Up to -20V for Op Amps**

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7662CTV	0°C to +70°C	TO-99 Can
ICL7662CPA		8 Pin Mini-DIP
ICL7662CBD		14 Pin SOIC
ICL7662MTV*	+55°C to +125°C	TO-99 Can

Description

The Harris ICL7662 is a monolithic high-voltage CMOS power supply circuit which offers unique performance advantages over previously available devices. The ICL7662 performs supply voltage conversion from positive to negative for an input range of +4.5V to +20.0V, resulting in complementary output voltages of -4.5V to -20V. Only 2 noncritical external capacitors are needed for the charge pump and charge reservoir functions. The ICL7662 can also function as a voltage doubler, and will generate output volt- ages up to + 38.6V with a + 20V input.

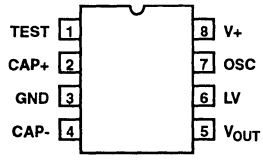
Contained on chip are a series DC power supply regulator, RC oscillator, voltage level translator, four output power MOS switches. A unique logic element senses the most negative voltage in the device and ensures that the output N-channel switch source-substrate junctions are not forward biased. This assures latchup free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 15.0V. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be overdriven by an external clock.

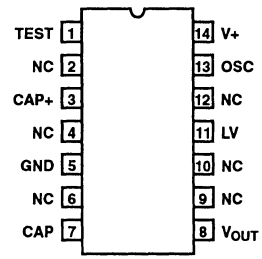
The "LV" terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (+10V to +20V), the LV pin is left floating to prevent device latchup.

Pinouts

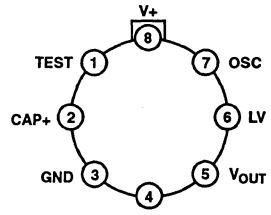
8 LEAD MINI-DIP
TOP VIEW



14 LEAD SOIC
TOP VIEW



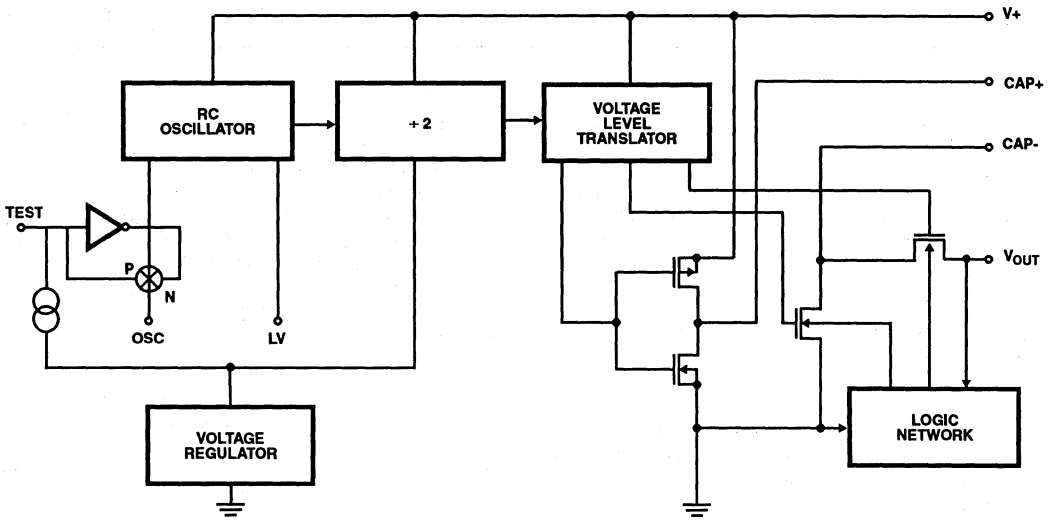
8 LEAD TO-99 CAN
TOP VIEW



7 REGULATORS/ POWER SUPPLIES

File Number **3181**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage 22V
Oscillator Input Voltage..... -0.3V to (V+ +0.3V) for V+ < 10V
..... (V+ -10V) to (V+ +0.3V) for V+ > 10V
(Note 1)
Current into LV (Note 1) .....20µA for V+ > 10V
Output Short Duration ..... Continuous

Power Dissipation (Note 2)
ICL7662CTY 500mW
ICL7662CPA 300mW
ICL7662MTY 500mW
Lead Temperature (Soldering, 10s)..... 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 15V, T_A = +25°C, C_{OSC} = 0, Unless Otherwise Stated. Refer to Figure 1.

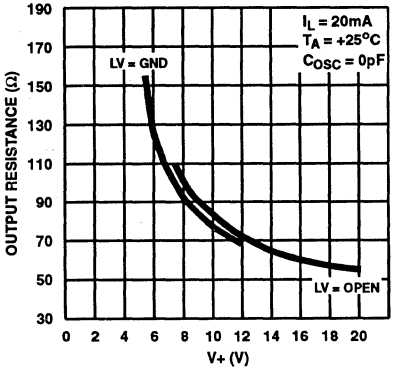
PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Supply Voltage Range - Lo	V+L	R_L = 10kΩ, LV = GND	Min < T_A < Max	4.5	-	11	V
Supply Voltage Range - Hi	V+H	R_L = 10kΩ, LV = Open	Min < T_A < Max	9	-	20	V
Supply Current	I+	R_L = ∞, LV = Open	T_A = +25°C	-	0.25	0.60	mA
			0°C < T_A < +70°C	-	0.30	0.85	mA
			-55°C < T_A < +125°C	-	0.40	1.0	mA
Output Source Resistance	R_O	I_O = 20mA, LV = Open	T_A = +25°C	-	60	100	Ω
			0°C < T_A < +70°C	-	70	120	Ω
			-55°C < T_A < +125°C	-	90	150	Ω
Supply Current	I+	V+ = 5V, R_L = ∞, LV = GND	T_A = +25°C	-	20	150	µA
			0°C < T_A < +70°C	-	25	200	µA
			-55°C < T_A < +125°C	-	30	250	µA
Output Source Resistance	R_O	V+ = 5V, I_O = 3mA, LV = GND	T_A = +25°C	-	125	200	Ω
			0°C < T_A < +70°C	-	150	250	Ω
			-55°C < T_A < +125°C	-	200	350	Ω
Oscillator Frequency	FOSC			-	10	-	kHz
Power Efficiency	P_{eff}	R_L = 2KΩ	T_A = +25°C	93	96	-	%
			Min < T_A < Max	90	95	-	%
Voltage Conversion Efficiency	VoEf	R_L = ∞	Min < T_A < Max	97	99.9	-	%
Oscillator Sink or Source Current	I_{OSC}	V+ = 5V (V_{OSC} = 0V to +5V)		-	0.5	-	µA
		V+ = 15V (V_{OSC} = +5V to +15V)		-	4.0	-	µA

NOTES:

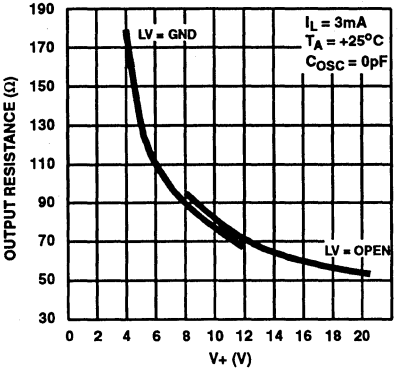
1. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660s.
2. Derate linearly above 50°C by 5.5mW/°C.
3. Pin 1 is a Test pin and is not connected in normal use. When the TEST pin is connected to V+, an internal transmission gate disconnects any external parasitic capacitance from the oscillator which would otherwise reduce the oscillator frequency from its nominal value.

Performance Curves (See Figure 1, Test Circuit)

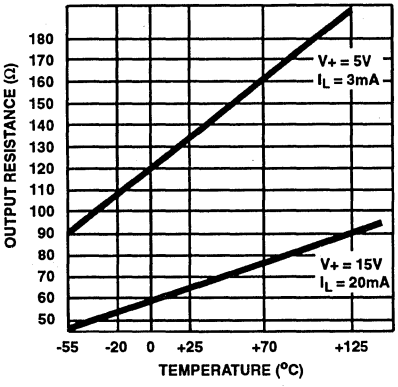
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



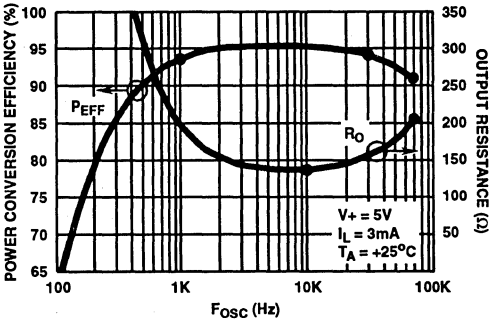
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



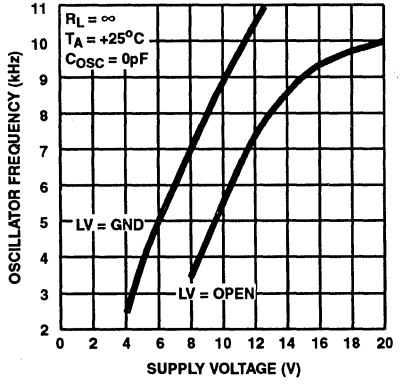
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



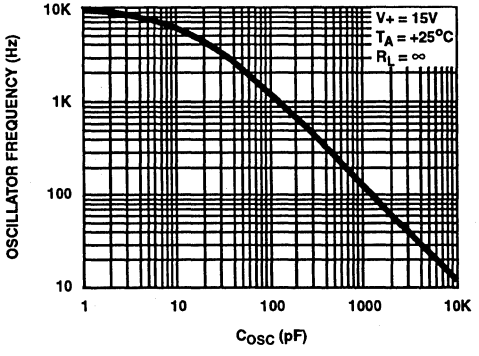
POWER CONVERSION EFFICIENCY AND OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY



OSCILLATOR FREQUENCY vs. SUPPLY VOLTAGE



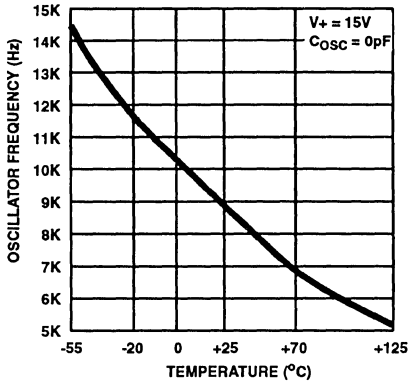
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE



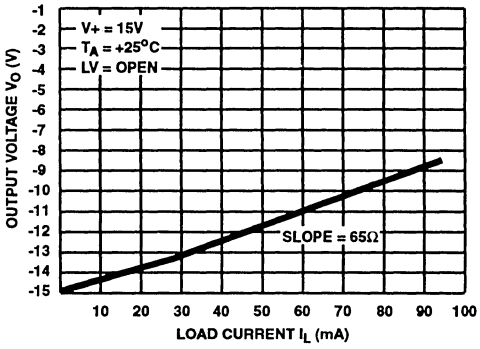
NOTE: All typical values have been characterized but are not tested.

Performance Curves (See Figure 1, Test Circuit) (Continued)

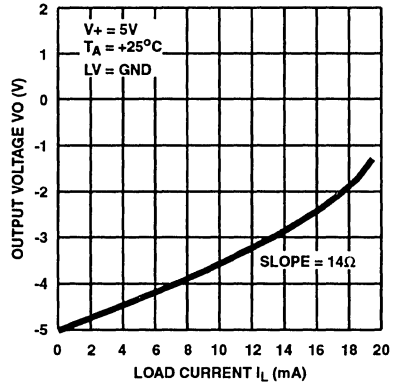
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



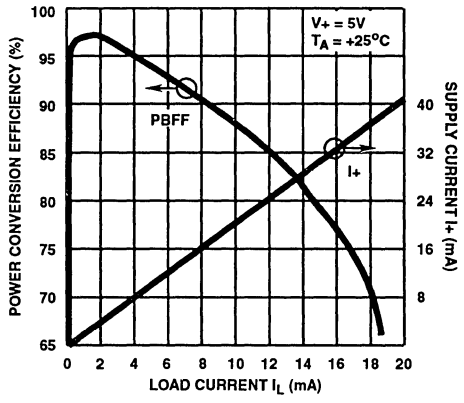
OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



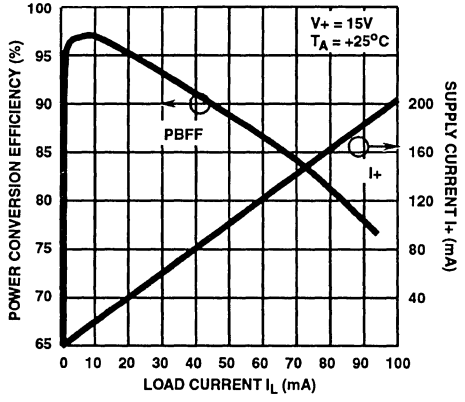
OUTPUT VOLTAGE AS A FUNCTION OF LOAD CURRENT



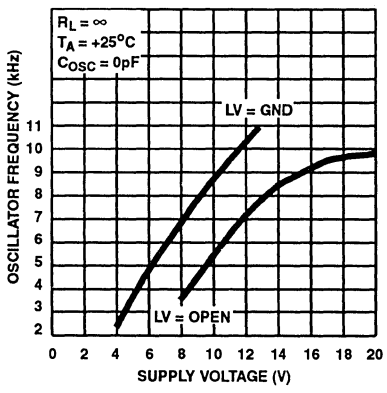
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD



SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

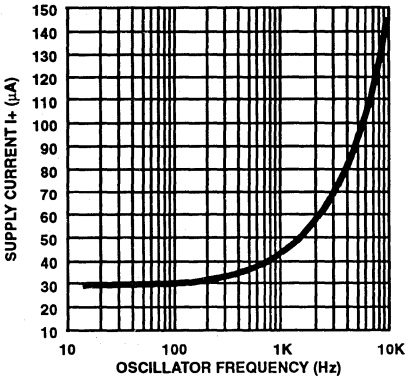


FREQUENCY OF OSCILLATION AS A FUNCTION OF SUPPLY VOLTAGE



Performance Curves (See Figure 1, Test Circuit) (Continued)

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY



NOTE 4. These curves include in the supply current that current fed directly into the load R_L from the V+ (See Figure 1). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7662, to the negative side of the load. Ideally, $V_{OUT} = 2V_{IN}$, $I_S = 2I_L$, so $V_{IN} \times I_S = V_{OUT} \times I_L$.

Circuit Description

The ICL7662 contains all the necessary circuitry to complete a negative voltage converter, with the exception of 2 external capacitors which may be inexpensive 10µF polarized electrolytic capacitors. The mode of operation of the device may be best understood by considering Figure 2, which shows an idealized negative voltage converter. Capacitor C_1 is charged to a voltage, V+, for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V+ volts. Charge is then transferred from C_1 to C_2 such that the voltage on C_2 is exactly V+, assuming ideal switches and no load on C_2. The ICL7662 approaches this ideal situation more closely than existing non-mechanical circuits.

In the ICL7662, the 4 switches of Figure 2 are MOS power switches; S_1 is a P-channel device and S_2, S_3 & S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 & S_4 must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit startup, and under output short circuit conditions (V_{OUT} = V+), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latchup.

This problem is eliminated in the ICL7662 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 & S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7662 is an integral part of the anti-latchup circuitry, however its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation the "LV" pin should be connected to GROUND, disabling the regulator. For supply voltages greater than 11 volts the LV terminal must be left open to insure latchup proof operation, and prevent device damage.

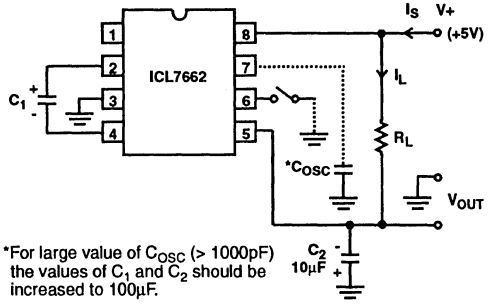


FIGURE 1. ICL7662 TEST CIRCUIT

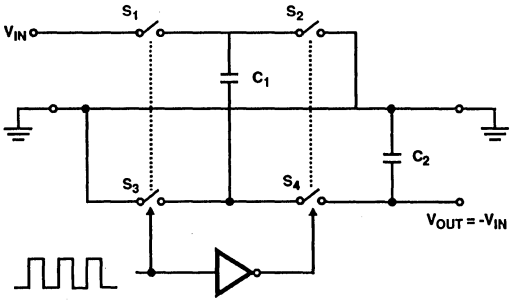


FIGURE 2. IDEALIZED NEGATIVE CONVERTER

Theoretical Power Efficiency Considerations

In theory a voltage multiplier can approach 100% efficiency if certain conditions are met:

A The drive circuitry consumes minimal power

B The output switches have extremely low ON resistance and virtually no offset.

C The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7662 approaches these conditions for negative voltage multiplication if large values of C1 and C2 are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined by:

$$E = 1/2C_1 (V_1^2 - V_2^2)$$

where V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L, there will be a substantial difference in the voltages V_1 and V_2. Therefore it is not only desirable to make C2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Do's And Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GROUND for supply voltages greater than 17 volts.
3. When using polarized capacitors, the + terminal of C1 must be connected to pin 2 of the ICL7662 and the + terminal of C2 must be connected to GROUND.
4. If the voltage supply driving the 7662 has a large source impedance (25W - 30W), then a 2.2mF capacitor from pin 6 to ground may be required to limit rate of rise of input voltage to less than 2V/ms.
5. User should insure that the output (pin 5) does not go more positive than GND (pin 3). Device latch up will occur under these conditions.

A 1N914 or similar diode placed in parallel with C_2 will prevent the device from latching up under these conditions. (Anode pin 5, Cathode pin 6).

Typical Applications

Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7662 for generation of negative supply voltages. Figure 3 shows typical connections to provide a negative supply where a positive supply of +4.5V to 20.0V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltages below 11 volts.

The output characteristics of the circuit in Figure 3a can be approximated by an ideal voltage source in series with a resistance as shown in Figure 3b. The voltage source has a value of -(V+). The output impedance (R_O) is a function of the ON resistance of the internal MOS switches (shown in Figure 2), the switching frequency, the value of C_1 and C_2, and the ESR (equivalent series resistance) of C_1 and C_2. A good first order approximation for R_O is:

$$R_O \cong 2(R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1}) + \frac{1}{f_{PUMP} \times C_1} + ESR_{C2}$$

$$(f_{PUMP} = \frac{f_{OSC}}{2} \quad R_{SWX} = \text{MOSFET switch resistance})$$

Combining the four R_{SWX} terms as R_{SW}, we see that

$$R_O \cong 2 \times R_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4 \times ESR_{C1} + ESR_{C2}\Omega$$

R_{SW}, the total switch resistance, is a function of supply voltage and temperature (See the Output Source Resistance graphs), typically 24Ω @ +25°C and 15V, and 53Ω @ +25°C and 5V. Careful selection of C_1 and C_2 will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the $1/(f_{PUMP} \times C_1)$ component, and low FSR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the $1/(f_{PUMP} \times C_1)$ term, but may have the side effect of a net increase in output impedance when $C_1 > 10\mu F$ and there is no longer enough time to fully charge the capacitors every cycle. In a typical application where $f_{OSC} = 10kHz$ and $C = C_1 = C_2 = 10\mu F$:

$$R_O \cong 2 \times 23 + \frac{1}{(5 \times 10^3 \times 10 \times 10^{-6})} + 4\ ESRC1 + ESRC2$$

$$R_O \cong 46 + 20 + 5 \times ESR_C\Omega$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low $1/(f_{PUMP} \times C_1)$ term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have FSRs as high as 10Ω.

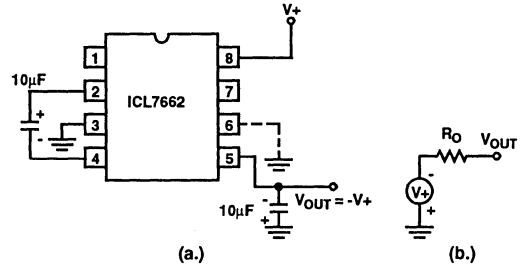


FIGURE 3. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

Output Ripple

ESR also affects the ripple voltage seen at the output. The total ripple is determined by 2 voltages, A and B, as shown in Figure 4. Segment A is the voltage drop across the ESR of C_2 at the instant it goes from being charged by C_1 (current flowing into C_2) to being discharged through the load (current flowing out of C_2). The magnitude of this current change is 2 x I_{OUT}, hence the total drop is 2 x I_{OUT} x ESR_{C2} volts. Segment B is the voltage change across C_2 during time t_2, the half of the cycle when C_2 supplies current the load. The drop at B is I_{OUT} x t_2/C_2 volts. The peak-to-peak ripple voltage is the sum of these voltage drops:

$$V_{RIPPLE} \cong \left(\frac{1}{2 \times f_{PUMP} \times C_2} + 2\ ESRC_2 \times I_{OUT} \right)$$

Again, a low ESR capacitor will result in a higher performance output.

Paralleling Devices

Any number of ICL7662 voltage converters may be paralleled (Figure 5) to reduce output resistance. The reservoir capacitor, C_2, serves all devices while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\ (\text{of ICL7662})}{n\ (\text{number of devices})}$$

Cascading Devices

The ICL7662 may be cascaded as shown in Figure 6 to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n(V_{IN}),$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7662 R_{OUT} values.

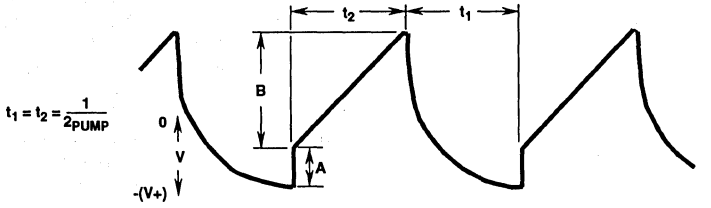


FIGURE 4. OUTPUT RIPPLE

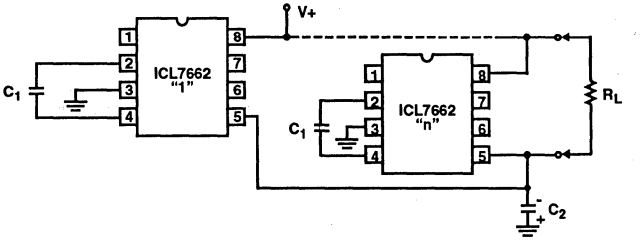


FIGURE 5. PARALLELING DEVICES

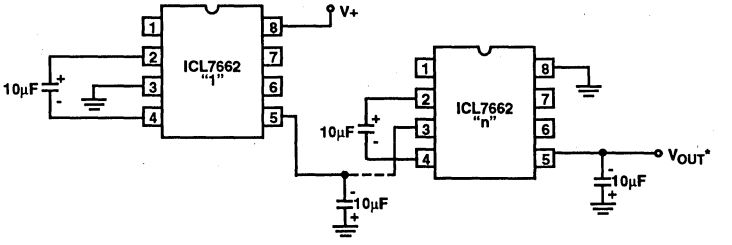


FIGURE 6. CASCADING DEVICES FOR INCREASED OUTPUT VOLTAGE

Changing the ICL7662 Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latchup, a 1kW resistor must be used in series with the clock output. In the situation where the designer has generated the external clock frequency using TTL logic, the addition of a 1OkW pullup resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the ICL7662 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, COSC, as shown in Figure 8. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C1) and reservoir (C2) capacitors; this is overcome by increasing the values of C1 and C2 by the same factor that the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC) and V+ will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of C1 and C2 (from 10mF to 1OOmF).

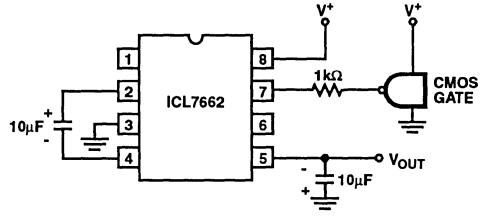


FIGURE 7. EXTERNAL CLOCKING

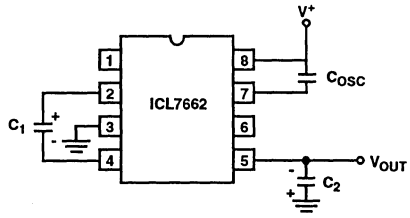
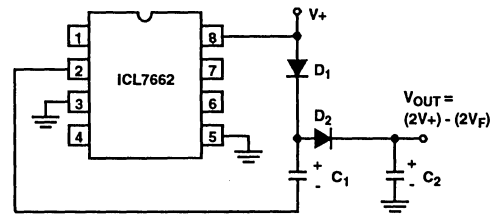


FIGURE 8. LOWERING OSCILLATOR FREQUENCY

Positive Voltage Doubling

The ICL7662 may be employed to achieve positive voltage doubling using the circuit shown in Figure 9. In this application, the pump inverter switches of the ICL7662 are used to charge C_1 to a voltage level of V+ -V_F (where V+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V+) is applied through diode C_2 to capacitor C_2. The voltage thus created on C_2 becomes (2V+) ($2V_F$) or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for V+ = 15 volts and an output current of 10mA it will be approximately 70 ohms.



NOTE: D_1 and D_2 can be any suitable diode.

FIGURE 9. POSITIVE VOLTAGE DOUBLER

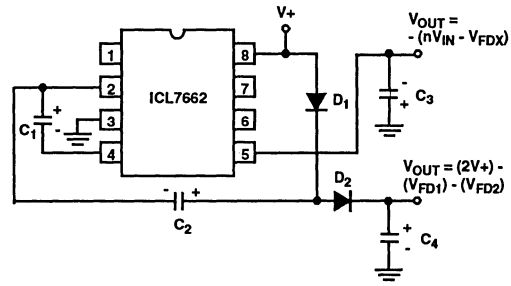


FIGURE 10. COMBINED NEGATIVE CONVERTER AND POSITIVE DOUBLER

Combined Negative Voltage Conversion and Positive Supply Doubling

Figure 10 combines the functions shown in Figures 3 and Figure 9 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be, for example, suitable for generating +9 volts and -5 volts from an existing +5 volt supply. In this instance capacitors C_1 and C_3 perform the pump and reservoir functions respectively for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir respectively for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

Voltage Splitting

The bidirectional characteristics can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides and, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +30V can be converted (via +15V, and -15V) to a nominal -30V, although with rather high series output resistance (~250Ω).

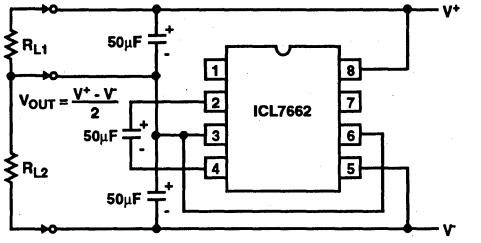


FIGURE 11. SPLITTING A SUPPLY IN HALF

Regulated Negative Voltage Supply

In some cases, the output impedance of the ICL7662 can be a problem, particularly if the load current varies substantially. The circuit of Figure 12 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7662's output does not respond instantaneously to a change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7662, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provides an output impedance of less than 5Ω to a load of 10mA.

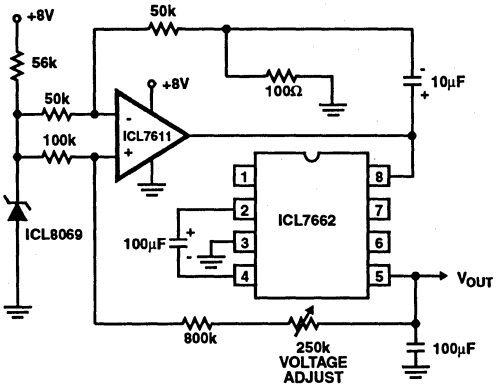


FIGURE 12. REGULATING THE OUTPUT VOLTAGE

Other Applications

Further information on the operation and use of the ICL7662 may be found in A051 "Principles and Applications of the ICL7660 CMOS Voltage Converter".

HARRIS SEMICONDUCTOR

ICL7663S

CMOS Programmable Micropower Positive Voltage Regulator

May 1992

Features

- *Guaranteed* 10μA Maximum Quiescent Current Over *All* Temperature Ranges
- *Wider* Operating Voltage Range - 1.6V to 16V
- *Guaranteed* Line and Load Regulation Over *Entire* Operating Temperature Range *Optional*
- 1% Output Voltage Accuracy (ICL7663SA)
- Output Voltage Programmable from 1.3V to 16V
- *Improved* Temperature Coefficient of Output Voltage
- 40mA Minimum Output Current with Current Limiting
- Output Voltages with Programmable Negative Temperature Coefficients
- Output Shutdown via Current-Limit Sensing or External Logic Level
- Low Input-to-Output Voltage Differential
- Improved Direct Replacement for Industry Standard ICL7663B and Other Second-Source Products

Applications

- Low-Power Portable Instrumentation
- Pagers
- Handheld Instruments
- LCD Display Modules
- Remote Data Loggers
- Battery-Powered Systems

Description

The ICL7663S Super Programmable Micropower Voltage Regulator is a low power, high efficiency positive voltage regulator which accepts 1.6V to 16V inputs and provides adjustable outputs from 1.3V to 16V at currents up to 40mA.

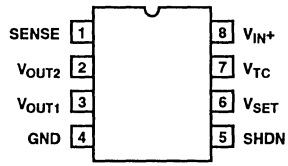
It is a direct replacement for the industry standard ICL7663B offering ***wider*** operating voltage and temperature ranges, ***improved*** output accuracy (ICL7663SA), better temperature coefficient, ***guaranteed*** maximum supply current, and guaranteed line and load regulation. All improvements are highlighted in the electrical characteristics section. ***Critical parameters are guaranteed over the entire commercial and industrial temperature ranges.*** The ICL7663S/SA programmable output voltage is set by two external resistors. The 1% reference accuracy of the ICL7663SA eliminates the need for trimming the output voltage in most applications.

The ICL7663S is well suited for battery powered supplies, featuring 4 μA quiescent current, low V_{IN} to V_{OUT} differential, output current sensing and logic input level shutdown control. In addition, the ICL7663S has a negative temperature coefficient output suitable for generating a temperature compensated display drive voltage for LCD displays.

The ICL7663S is available in either an 8-pin Plastic DIP, Ceramic DIP, or SOIC package.

Pinout

8 LEAD DIP & SOIC
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7663SCBA	0°C to +70°C	8 Lead SOIC
ICL7663SCPA		8 Lead Mini-DIP
ICL7663SCJA		8 Lead Ceramic DIP
ICL7663SACPA		8 Lead Mini-DIP
ICL7663SACJA		8 Lead Ceramic DIP
ICL7663SIBA	-25°C to +85°C	8 Lead SOIC
ICL7663SIPA		8 Lead Mini-DIP
ICL7663SIJA		8 Lead Ceramic DIP
ICL7663SAIPA		8 Lead Mini-DIP
ICL7663SAIJA		8 Lead Ceramic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Absolute Maximum Ratings

Input Supply Voltage ..... +18V
Any Input or Output Voltage (Note 1)
  Terminals 1, 2, 3, 5, 6, 7 ..... V_{IN}+0.3V to GND-0.3V
Output Source Current
  Terminal 2 ..... 50mA
  Terminal 3 ..... 25mA
Output Sinking Current
  Terminal 7 ..... -10mA

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Operating Temperature Range
Total Power Dissipation (Note 2)
  Ceramic DIP Package 500mW
  Mini-DIP Package 200mW
  SOIC 200mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
  ICL7663SC ..... 0°C to +70°C
  ICL7663SI ..... -25°C to +85°C

Electrical Specifications

Specifications below applicable to both ICL7663S and ICL7663SA, Unless Otherwise Specified. $V+_{IN}$ = 9V, V_{OUT} = 5V, T_A = +25°C, Unless Otherwise Specified. See Test Circuit, Figure 1

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Voltage	$V+_{IN}$	ICL7663S	T_A = +25°C	1.5	-	16	V
			0°C < T_A < +70°C	1.6	-	16	V
			-25°C < T_A < +85°C	1.6	-	16	V
		ICL7663SA	0°C < T_A < +70°C	1.6	-	16	V
			-25°C < T_A < +85°C	1.6	-	16	V
Quiescent Current	I_Q	1.4V ≤ V_{OUT} ≤ 8.5V, No Load					
		$V+_{IN}$ = 9V	0°C < T_A < +70°C	-	-	10	µA
			-25°C < T_A < +85°C	-	-	10	µA
		$V+_{IN}$ = 16V	0°C < T_A < +70°C	-	-	12	µA
			-25°C < T_A < +85°C	-	-	12	µA
Reference Voltage	V_{SET}	I_{OUT1} = 100µA, V_{OUT} = V_{SET}					
		ICL7663S	T_A = +25°C	1.2	1.3	1.4	V
		ICL7663SA	T_A = +25°C	1.275	1.29	1.305	V
Temperature Coefficient	$\frac{\Delta V_{SET}}{\Delta T}$	0°C < T_A < +70°C		-	100	-	ppm
		-25°C < T_A < +85°C		-	100	-	ppm
Line Regulation	$\frac{\Delta V_{SET}}{V_{SET}\,\Delta V_{IN}}$	2V < V_{IN} < 15V	0°C < T_A < +70°C	-	0.03	-	%/V
			-25°C < T_A < +85°C	-	0.03	0.3	%/V
V_{SET} Input Current	I_{SET}	0°C < T_A < +70°C		-	0.01	10	nA
		-25°C < T_A < +85°C		-	0.01	10	nA
Shutdown Input Current	I_{SHDN}			-	±0.01	10	nA
Shutdown Input Voltage	V_{SHDN}	V_{SHDN} HI: Both V_{OUT} Disabled		1.4	-	-	V
		V_{SHDN} LO: Both V_{OUT} Enable		-	-	0.3	V
Sense Pin Input Current	I_{SENSE}			-	0.01	10	nA
Sense Pin Input Threshold	V_{CL}			-	.5	-	V
Input-Output Saturation Resistance (Note 3)	R_{SAT}	$V+_{IN}$ = 2V, I_{OUT1} = 1mA		-	170	350	W
		$V+_{IN}$ = 9V, I_{OUT1} = 2mA		-	50	100	W
		$V+_{IN}$ = 15V, I_{OUT1} = 5mA		-	35	70	W
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	1mA < I_{OUT2} < 20mA		-	1	3	W
		50µA < I_{OUT1} < 5mA		-	2	10	W
Available Output Current (V_{OUT2})	I_{OUT2}	3V ≤ V_{IN} ≤ 16V, V_{IN} - V_{OUT2} = 1.5V		40	-	-	mA

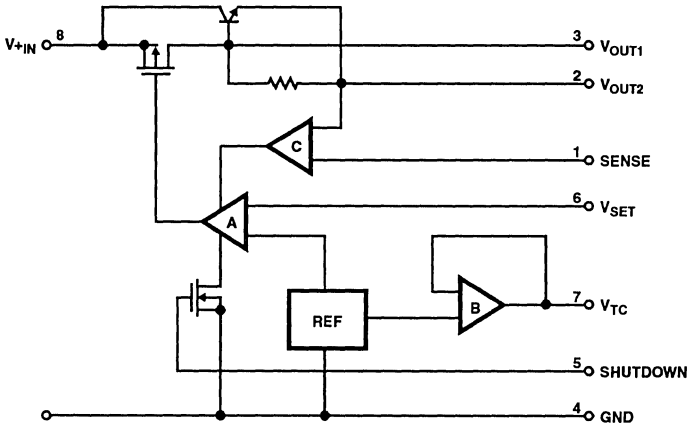
Electrical Specifications Specifications below applicable to both ICL7663S and ICL7663SA, Unless Otherwise Specified. $V+_{IN}$ = 9V, V_{OUT} = 5V, T_A = +25°C, Unless Otherwise Specified. See Test Circuit, Figure 1 **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Negative Tempco Output (Note 4)	V_{TC}	Open Circuit Voltage		-	0.9	-	V
	I_{TC}	Maximum Sink Current		0	8	2.0	mA
Temperature Coefficient	$\frac{\Delta V_{TC}}{\Delta T}$	Open Circuit		-	+2.5	-	mV/°C
Minimum Load Current	$I_{L(MIN)}$	Includes V_{SET} Divider	T_A = +25°C	-	-	1.0	µA
			0°C < T_A < +70°C	-	0.2	5.0	µA
			-25°C < T_A < +85°C	-	0.2	5.0	µA

NOTES:

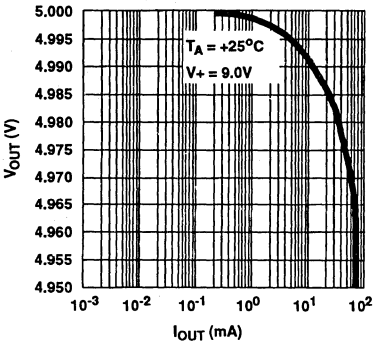
1. Connecting any terminal to voltages greater than ($V+_{IN}$ + 0.3V) or less than (GND - 0.3V) may cause destructive device latch-up. It is recommended that no inputs from sources operating on external power supplies be applied prior to ICL7663S power-up.
2. Derate linearly above +50°C at 5mW/°C for Plastic Mini-DIP, 7.5mW/°C for TO-99 can, and 10mW/°C for Ceramic DIP.
3. This parameter refers to the saturation resistance of the MOS pass transistor. The minimum input-output voltage differential at low current (under 5mA), can be determined by multiplying the load current (including set resistor current, but not quiescent current) by this resistance.
4. This output has a positive temperature coefficient. Using it in combination with the inverting input of the regulator at V_{SET}, a negative coefficient results in the output voltage. See Figure 3 for details. Pin will not source current.
5. All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V.
6. All significant improvements over the industry standard ICL7663 are highlighted.

Functional Diagram

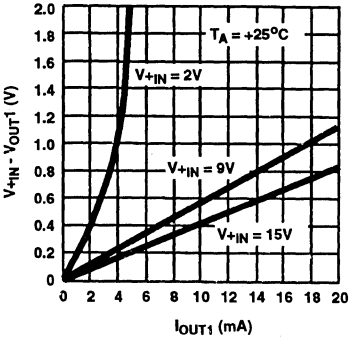


Typical Performance Characteristics

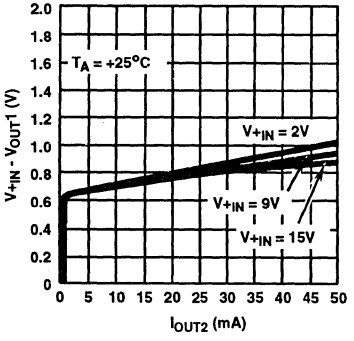
V_{OUT2} OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



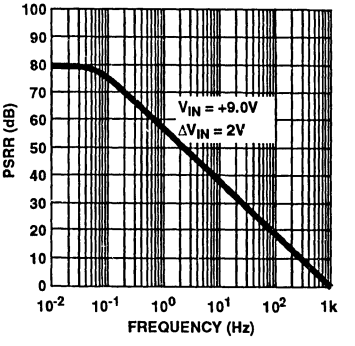
V_{OUT1} INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



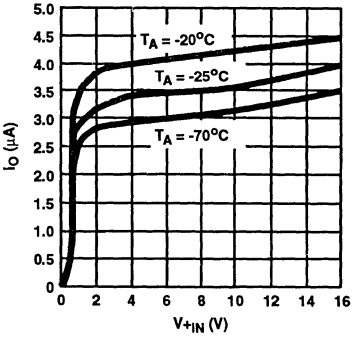
V_{OUT2} INPUT-OUTPUT DIFFERENTIAL vs. OUTPUT CURRENT



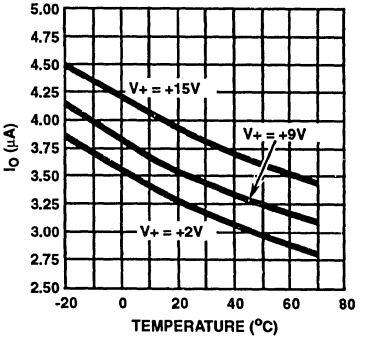
INPUT POWER SUPPLY REJECTION RATIO



QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



QUIESCENT CURRENT AS A FUNCTION OF TEMPERATURE



Detailed Description

The ICL7663S is a CMOS integrated circuit incorporating all the functions of a voltage regulator plus protection circuitry on a single monolithic chip. Referring to the Functional Diagram, the main blocks are a bandgap-type voltage reference, an error amplifier, and an output driver with both PMOS and NPN pass transistors.

The bandgap output voltage, trimmed to 1.29V ± 15mV for the ICL7663SA, and the input voltage at the V_{SET} terminal are compared in amplifier A. Error amplifier A drives a P-channel pass transistor which is sufficient for low (under about 5mA) currents. The high current output is passed by an NPN bipolar transistor connected as a follower. This configuration gives more gain and lower output impedance.

Logic-controlled shutdown is implemented via a N-channel MOS transistor. Current-sensing is achieved with comparator C, which functions with the V_{OUT2} terminal. The ICL7663S has an output (V_{TC}) from a buffer amplifier (B), which can be used in combination with amplifier A to generate programmable-temperature-coefficient output voltages.

The amplifier, reference and comparator circuitry all operate at bias levels well below 1µA to achieve extremely low quiescent current. This does limit the dynamic response of the circuits, however, and transients are best dealt with outside the regulator loop.

Basic Operation

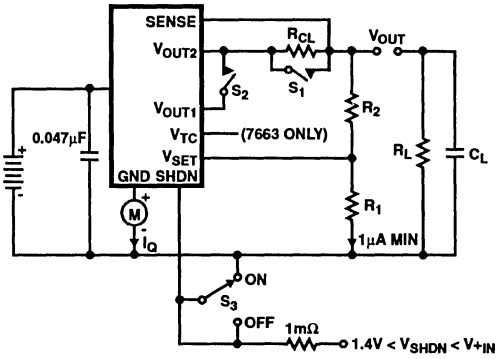
The ICL7663S is designed to regulate battery voltages in the 5V to 15V region at maximum load currents of about 5mA to 30mA. Although intended as low power devices, power dissipation limits must be observed. For example, the power dissipation in the case of a 10V supply regulated down to 2V with a load current of 30mA clearly exceeds the power dissipation rating of the Mini-DIP:

$$(10 - 2)\ (30)\ (10^{-3}) = 240mW$$

The circuit of Figure 2 illustrates proper use of the device.

CMOS devices generally require two precautions: every input pin must go somewhere, and maximum values of applied voltages and current limits must be rigorously observed. Neglecting these precautions may lead to, at the least, incorrect or nonoperation, and at worst, destructive device failure. To avoid the problem of latchup, do not apply inputs to any pins before supply voltage is applied.

Input Voltages - The ICL7663S accepts working inputs of 1.5V to 16V. When power is applied, the rate-of-rise of the input may be hundreds of volts per microsecond. This is potentially harmful to the regulators, where internal operating currents are in the nanoampere range. The 0.047µF capacitor on the device side of the switch will limit inputs to a safe level around 2V/µs. Use of this capacitor is suggested in all applications. In severe rate-of-rise cases, it may be advisable to use an RC network on the SHutDowN pin to delay output turn-on. Battery charging surges, transients, and assorted noise signals should be kept from the regulators by RC filtering, zener protection, or even fusing.



NOTES:

1. S_1 when closed disables output current limiting.
2. Close S_2 for V_{OUT1}, open S_2 for V_{OUT2}.
3. $V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET}$.
4. IQ quiescent currents measured at GND pin by meter M.
5. S_3 when ON, permits normal operation, when OFF, shuts down both V_{OUT1} and V_{OUT2}.

FIGURE 1. ICL7663S TEST CIRCUIT

Output Voltages - The resistor divider R_2/R_1 is used to scale the reference voltage, V_{SET}, to the desired output using the formula $V_{OUT} = (1 + R_2/R_1)\ V_{SET}$. Suitable arrangements of these resistors, using a potentiometer, enables exact values for V_{OUT} to be obtained. In most applications the potentiometer may be eliminated by using the ICL7663SA. The ICL7663SA has V_{SET} voltage guaranteed to be 1.29V ±15mV and when used with ±1% tolerance resistors for R_1 and R_2 the initial output voltage will be within ±2.7% of ideal.

The low leakage current of the V_{SET} terminal allows R_1 and R_2 to be tens of megohms for minimum additional quiescent drain current. However, some load current is required for proper operation, so for extremely low-drain applications it is necessary to draw at least 1µA. This can include the current for R_2 and R_1.

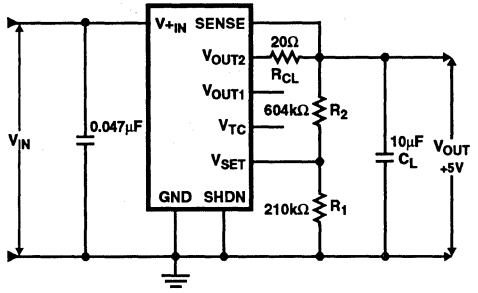
Output voltages up to nearly the V_{IN} supply may be obtained at low load currents, while the low limit is the reference voltage. The minimum input-output differential in each regulator is obtained using the V_{OUT1}, terminal. The input-output differential increases to 1.5V when using V_{OUT2}.

Output Currents - Low output currents of less than 5mA are obtained with the least input-output differential from the V_{OUT1} terminal (connect V_{OUT2} to V_{OUT1}). Where higher currents are needed, use V_{OUT2} (V_{OUT1}, should be left open in this case).

High output currents can be obtained only as far as package dissipation allows. It is strongly recommended that output current-limit sensing be used in such cases.

Current-Limit Sensing - The on-chip comparator (C in the Functional Diagram) permits shutdown of the regulator

output in the event of excessive current drain. As Figure 2 shows, a current-limiting resistor, R_{CL}, is placed in series with V_{OUT2} and the SENSE terminal is connected to the load side of R_{CL}. When the current through R_{CL} is high enough to produce a voltage drop equal to V_{CL} (0.5V) the voltage feedback is by-passed and the regulator output will be limited to this current. Therefore, when the maximum load current (I_{LOAD}) is determined, simply divide V_{CL} by I_{LOAD} to obtain the value for R_{CL}.



$$V_{OUT} = \frac{R_2 + R_1}{R_1} V_{SET} = 5V$$

$$I_{CL} = \frac{V_{CL}}{R_{CL}} = 25mA$$

FIGURE 2. POSITIVE REGULATOR WITH CURRENT LIMIT

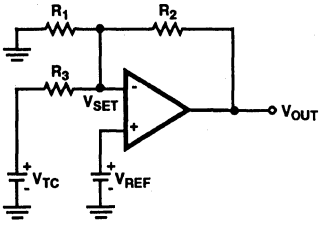
Logic-Controllable Shutdown - When equipment is not needed continuously (e.g., in remote data-acquisition systems), it is desirable to eliminate its drain on the system until it is required. This usually means switches, with their unreliable contacts. Instead, the ICL7663S can be shut down by a logic signal, leaving only I_Q (under 4µA) as a drain on the power source. Since this pin must not be left open, it should be tied to ground if not needed. A voltage of less than 0.3V for the ICL7663S will keep the regulator ON, and a voltage level of more than 1.4V but less than $V+_{IN}$ will turn the outputs OFF. If there is a possibility that the control signal could exceed the regulator input ($V+_{IN}$) the current from this signal should be limited to 100µA maximum by a high value (1MΩ) series resistor. This situation may occur when the logic signal originates from a system powered separately from that of the regulator.

Additional Circuit Precautions - This regulator has poor rejection of voltage fluctuations from AC sources above 10Hz or so. To prevent the output from responding (where this might be a problem), a reservoir capacitor across the load is advised. The value of this capacitor is chosen so that the regulated output voltage reaches 90% of its final value in 20ms. From:

$$I = C\frac{\Delta V}{\Delta t}, C = I_{OUT}\frac{(20 \times 10^{-3})}{0.9V_{OUT}} = 0.022\frac{I_{OUT}}{V_{OUT}}$$

In addition, where such a capacitor is used, a current-limiting resistor is also suggested (see "Current-Limit Sensing").

Producing Output Voltages with Negative Temperature Coefficients - The ICL7663S has an additional output which is 0.9V relative to GND and has a tempco of +2.5mV/°C. By applying this voltage to the inverting input of amplifier A (i.e., the V_{SET} pin), output voltages having negative TC may be produced. The TC of the output voltage is controlled by the R_2/R_3 ratio (see Figure 3 and its design equations).



EQ. 1: $V_{OUT} = V_{SET}\left(1 + \frac{R_2}{R_1}\right) + \frac{R_2}{R_3}(V_{SET} - V_{TC})$

EQ. 2: $TC\ V_{OUT} = -\frac{R_2}{R_3}(TC\ V_{TC})$ in mV/°C

Where: $V_{SET} = 1.3V$
$V_{TC} = 0.9V$
$TCV_{TC} = +2.5mV/°C$

FIGURE 3. GENERATING NEGATIVE TEMPERATURE COEFFICIENTS

Applications

Boosting Output Current with External Transistor

The maximum available output current from the ICL7663S is 40mA. To obtain output currents greater than 40mA, an external NPN transistor is used connected as shown in Figure 4.

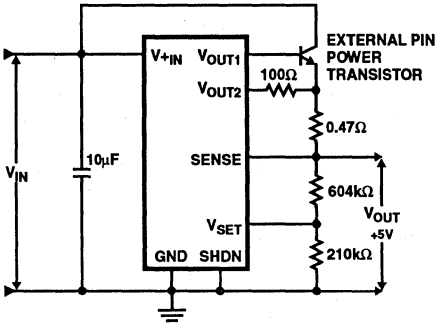


FIGURE 4. BOOSTING OUTPUT CURRENT WITH EXTERNAL TRANSISTOR

Generating a Temperature Compensated Display Drive Voltage

Temperature has an important effect in the variation of threshold voltage in multiplexed LCD displays. As temperature rises, the threshold voltage goes down. For applications where the display temperature varies widely, a temperature compensated display voltage, V_{DISP} can be generated using the ICL7663S. This is shown in Figure 5 for the ICM7233 triplexed LCD display driver.

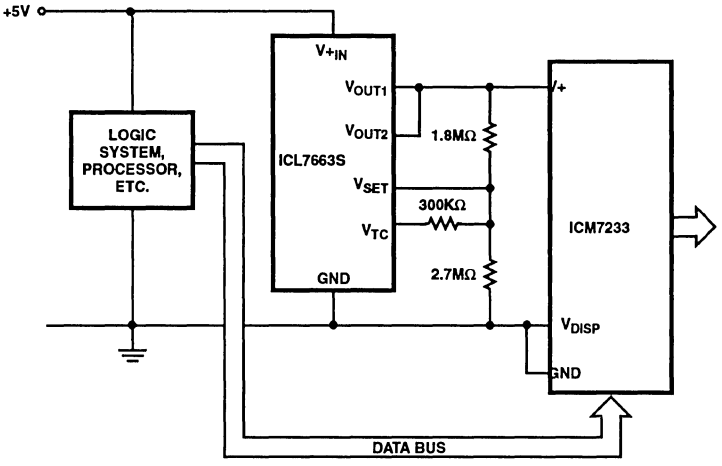


FIGURE 5. GENERATING A MULTIPLEXED LCD DISPLAY DRIVE VOLTAGE

HARRIS SEMICONDUCTOR

ICL7665S

CMOS Micropower Over/Under Voltage Detector

May 1992

Features

- **Guaranteed 10μA Maximum Quiescent Current Over Temperature**
- **Guaranteed Wider Operating Voltage Range Over Entire Operating Temperature Range**
- **2% Threshold Accuracy (ICL7665SA)**
- **Dual Comparator with Precision Internal Reference**
- **100ppm/°C Temperature Coefficient of Threshold Voltage**
- ***Improved* Direct Replacement for Industry Standard ICL7665B and Other Second Source Devices**
- **Output Current Sinking Ability..... Up to 20mA**
- **Individually Programmable Upper and Lower Trip Voltages and Hysteresis Levels**

Applications

- **Pocket Pagers**
- **Portable Instrumentation**
- **Charging Systems**
- **Memory Power Back-Up**
- **Battery Operated Systems**
- **Portable Computers**
- **Level Detectors**

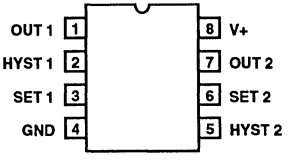
Description

The ICL7665S Super CMOS Micropower Over/Under voltage Detector Contain two low power, individually programmable voltage detectors on a single CMOS chip. Requiring typically 3μA for operation, the device is intended for battery-operated systems and instruments which require high or low voltage warnings, settable trip points, or fault monitoring and correction. The trip points and hysteresis of the two voltage detectors are individually programmed via external resistors. An internal bandgap-type reference provides an accurate threshold voltage while operating from any supply in the 1.6V to 16V range.

The ICL7665S, Super Programmable Over/Under voltage Detector is a direct replacement for the industry standard ICL7665B offering ***wider*** operating voltage and temperature ranges, ***improved*** threshold accuracy (ICL7665SA), and temperature coefficient, and ***guaranteed*** maximum supply current. All improvements are highlighted in the electrical characteristics section. ***All critical parameters are guaranteed over the entire commercial and industrial temperature ranges.***

Pinouts

8 LEAD DIP AND SOIC
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7665SCBA	0° to +70°C	8 Lead SOIC
ICL7665SCPA		8 Lead Mini-DIP
ICL7665SCJA		8 Lead CERDIP
ICL7665SACPA		8 Lead Mini-DIP
ICL7665SACJA		8 Lead CERDIP
ICL7665SIBA	-25°C to +85°C	8 Lead SOIC
ICL7665SIPA		8 Lead Mini-DIP
ICL7665SIJA		8 Lead CERDIP
ICL7665SAIPA		8 Lead Mini-DIP
ICL7665SAIJA		8 Lead CERDIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3182**

Absolute Maximum Ratings

Supply Voltage (Note 2) ..... -0.3 to +18V
Output Voltages OUT1 and OUT2 ..... -0.3V to 18V (with respect to GND) (Note 2)
Output Voltages HYST1 and HYST2 ..... -0.3V to +18V (with respect to V+) (Note 2)
Input Voltages SET1 and SET2 .....(GND-0.3V) to (V+ V- +0.3V) (Note 2)
Maximum Sink Output OUT1 and OUT2 ..... 25mA
Maximum Source Output Current
HYST1 and HYST2 ..... -25mA
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Maximum Package Power Dissipation at +125°C
SOIC 200mW
Mini-DIP..... 200mW
CERDIP..... 500mW

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL7665SC ..... 0°C to +70°C ICL7665SI ..... -25°C to +85°C

Electrical Specifications The specifications below are applicable to both the ICL7665S and ICL7665SA. V+ = 5V, T_A = +25°C, Test Circuit Figure 1. Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Supply Voltage	V+	ICL7665S	T_A = +25°C	1.6	-	16	V
			0°C ≤ T_A ≤ +70°C	1.8	-	16	V
			-25°C ≤ T_A ≤ +85°C	1.8	-	16	V
		ICL7665SA	0°C ≤ T_A ≤ +70°C	1.8	-	16	V
			-25°C ≤ T_A ≤ +85°C	1.8	-	16	V
Supply Current	I+	GND ≤ V_{SET1}, V_{SET2} ≤ V+, All Outputs Open Circuit					
		0°C ≤ T_A ≤ +70°C	V+ = 2V	-	2.5	10	µA
			V+ = 9V	-	2.6	10	µA
			V+ = 15V	-	2.9	10	µA
		-25°C ≤ T_A ≤ +85°C	V+ = 2V	-	2.5	10	µA
			V+ = 9V	-	2.6	10	µA
			V+ = 15V	-	2.9	10	µA
Input Trip Voltage	V_{SET1}	ICL7665S		1.15	1.30	1.45	V
	V_{SET2}			1.20	1.30	1.40	V
	V_{SET1}	ICL7665SA		1.275	1.30	1.325	V
	V_{SET2}			1.225	1.30	1.375	V
Temperature Coefficient of V_{SET}	$\frac{\Delta V_{SET}}{\Delta T}$	ICL7665S		-	200	-	ppm
		ICL7665SA		-	100	-	ppm
Supply Voltage Sensitivity of V_{SET1}, V_{SET2}	$\frac{\Delta V_{SET}}{\Delta V_S}$	R_{OUT1}, R_{OUT2}, R_{HYST1}, R_{2HYST2} = 1MΩ, 2V ≤ V+ ≤ 10V		-	0.03	-	%/V
Output Leakage Currents of OUT and HYST	I_{OLK}	VSET = 0V or VSET ≥ 2V		-	10	200	nA
	I_{HLK}			-	-10	-100	nA
	I_{OLK}	V+ = 15V, T_A = +70°C		-	-	2000	nA
	I_{HLK}			-	-	-500	nA
Output Saturation Voltages	V_{OUT1}	V_{SET1} = 2V, I_{OUT1} = 2mA	V+ = 2V	-	0.2	0.5	V
			V+ = 5V	-	0.1	0.3	V
			V+ = 15V	-	0.06	0.2	V

Electrical Specifications The specifications below are applicable to both the ICL7665S and ICL7665SA. V+ = 5V, T_A = +25°C, Test Circuit Figure 1. Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Saturation Voltages	V_{HYST1}	V_{SET1} = 2V, I_{HYST1} = -0.5mA	V+ = 2V	-	-0.15	-0.30	V
			V+ = 5V	-	-0.05	-0.15	V
			V+ = 15V	-	-0.02	-0.10	V
Output Saturation Voltages	V_{OUT2}	V_{SET2} = 0V, I_{OUT2} = 2mA	V+ = 2V	-	0.2	0.5	V
			V+ = 5V	-	0.15	0.3	V
			V+ = 15V	-	0.11	0.25	V
Output Saturation Voltages	V_{HYST2}	V_{SET2} = 2V	V+ = 2V, I_{HYST2} = -0.2mA	-	-0.25	-0.8	V
			V+ = 5V, I_{HYST2} = -0.5mA	-	-0.43	-1.0	V
			V+ = 15V, I_{HYST2} = -0.5mA	-	-0.35	-0.8	V
V_{SET} Input Leakage Current	I_{SET}	GND ≤ V_{SET} ≤ V+		-	0.01	10	nA
Δ Input for Complete Output Change	ΔV_{SET}	R_{OUT} = 4.7kΩ, R_{HYST} = 20kΩ, V_{OUT}LO = 1% V+, V_{OUT}HI = 99%V+	ICL7665S	-	1.0	-	mV
			ICL7665SA	-	0.1	-	mV
Difference in Trip Voltages	V_{SET1} - V_{SET2}	R_{OUT}, R_{HYST} = 1mW		-	±5	±50	mV
Output/Hysteresis Difference		R_{OUT}, R_{HYST} = 1mW	ICL7665S	-	±1	-	mV
			ICL7665SA	-	±0.1	-	mV

NOTES:

1. Derate above +25°C ambient temperature at 4mW/°C
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than (V+ +0.3V) or less than (GND - 0.3V) may cause destructive device latchup. For these reasons, it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICL7665S be turned on first. If this is not possible, current into inputs and/or outputs must be limited to ±0.5mA and voltages must not exceed those defined above.
3. All significant improvements over the industry standard ICL7665 are highlighted.

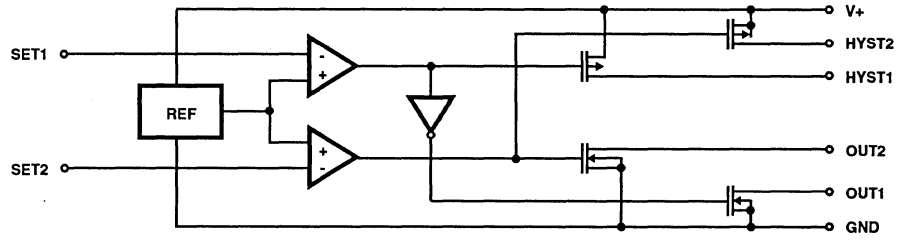
AC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
OUTPUT DELAY TIMES						
Input Going HI	t_{SO1d}	V_{SET} Switched between 1.0V to 1.6V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ, C_L = 12pF	-	85	-	µs
	t_{SH1d}		-	90	-	µs
	t_{SO2d}		-	55	-	µs
	t_{SH2d}		-	55	-	µs
Input Going LO	t_{SO1d}	V_{SET} Switched between 1.6V to 1.0V, R_{OUT} = 4.7kΩ, C_L = 12pF, R_{HYST} = 20kΩ, C_L = 12pF	-	75	-	µs
	t_{SH1d}		-	80	-	µs
	t_{SO2d}		-	60	-	µs
	t_{SH2d}		-	60	-	µs

AC Electrical Specifications **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Output Rise Times	t_{O1r}	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF	-	0.6	-	µs
	t_{O2r}		-	0.8	-	µs
	t_{H1r}		-	7.5	-	µs
	t_{H2r}		-	0.7	-	µs
Output Fall Times	t_{O1f}	V_{SET} Switched between 1.0V to 1.6V R_{OUT} = 4.7kΩ, C_L = 12pF R_{HYST} = 20kΩ, C_L = 12pF	-	0.6	-	µs
	t_{O2f}		-	0.7	-	µs
	t_{H1f}		-	4.0	-	µs
	t_{H2f}		-	1.8	-	µs

Functional Block Diagram

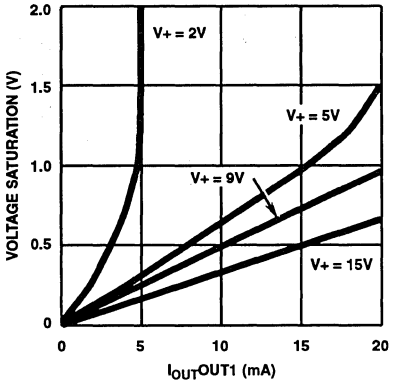


CONDITIONS*
V_{SET1} > 1.3V, OUT1 Switch ON, HYST1 Switch ON
V_{SET1} > 1.3V, OUT1 Switch OFF, HYST1 Switch OFF
V_{SET2} > 1.3V, OUT2 Switch OFF, HYST2 Switch ON
V_{SET2} > 1.3V, OUT2 Switch ON, HYST2 Switch OFF

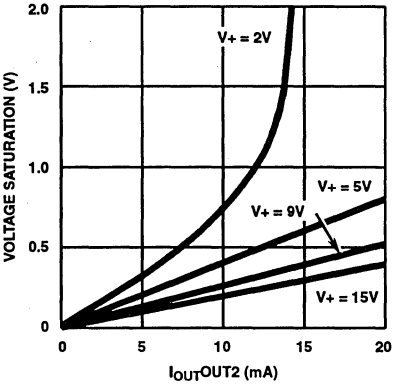
*See Operating Characteristics for exact thresholds.

Typical Performance Characteristics

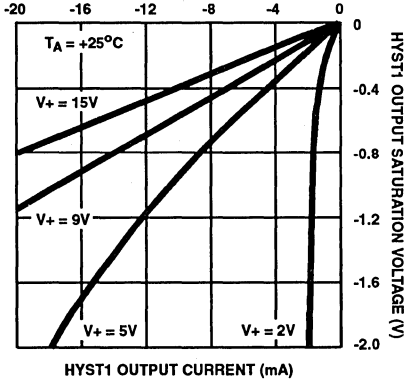
OUT1 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



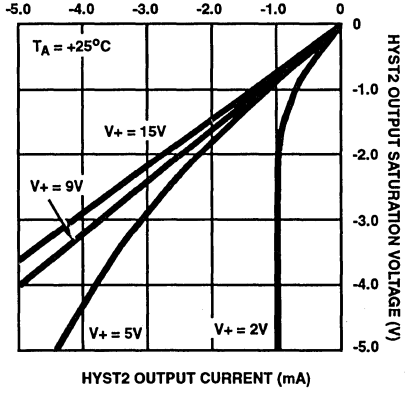
OUT2 SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



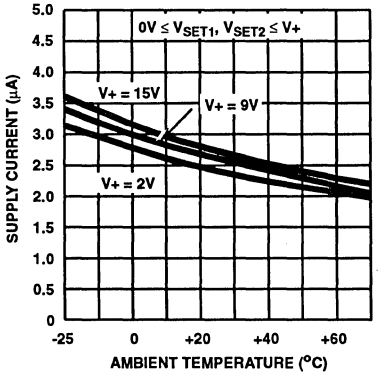
HYST1 OUTPUT SATURATION VOLTAGE vs. HYST1 OUTPUT CURRENT



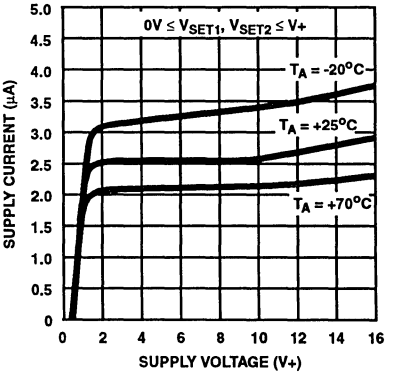
HYST2 OUTPUT SATURATION VOLTAGE vs. HYST2 OUTPUT CURRENT



SUPPLY CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



Detailed Description

As shown in the Functional Diagram, the ICL7665S consists of two comparators which compare input voltages on the SET1 and SET2 terminals to an internal 1.3V bandgap reference. The outputs from the two comparators drive open-drain N-channel transistors for OUT1 and OUT2, and open-drain P-channel transistors for HYST1 and HYST2 outputs. Each section, the Under Voltage Detector and the Over Voltage Detector, is independent of the other, although both use the internal 1.3V reference. The offset voltages of the two comparators will normally be unequal so V_{SET1} will generally not quite equal V_{SET2}.

The input impedance of the SET1 and SET2 pins are extremely high, and for most practical applications can be ignored. The four outputs are open-drain MOS transistors, and when ON behave as low resistance switches to their respective supply rails. This minimizes errors in setting up the hysteresis, and maximizes the output flexibility. The operating currents of the bandgap reference and the comparators are around 100nA each.

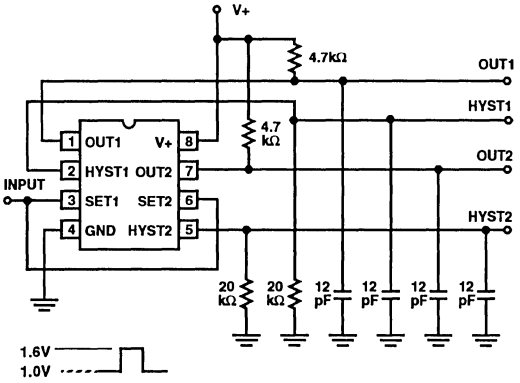


FIGURE 1. TEST CIRCUITS

Precautions

Junction isolated CMOS devices like the ICL7665S have an inherent SCR or 4-layer PNPN structure distributed throughout the die. Under certain circumstances, this can be triggered into a potentially destructive high current mode. This latchup can be triggered by forward-biasing an input or output with respect to the power supply, or by applying excessive supply voltages. In very low current analog circuits, such as the ICL7665S, this SCR can also be triggered by applying the input power supply extremely rapidly ("instantaneously"), e.g. through a low impedance battery and an ON/OFF switch with short lead lengths. The rate-of-rise of the supply voltage can exceed 100V/µs in such a circuit. A low impedance capacitor (e.g., 0.05µF disc ceramic) between the V+ and GND pins of the ICL7665S can be used to reduce the rate-of-rise of the supply voltage in battery applications. In line operated systems, the rate-of-rise of the supply is limited by other considerations, and is normally not a problem.

If the SET voltages must be applied before the supply voltage V+, the input current should be limited to less than 0.5mA by appropriate external resistors, usually required for voltage setting anyway. A similar precaution should be taken with the outputs if it is likely that they will be driven by other circuits to levels outside the supplies at any time. See M011 for some other protection ideas.

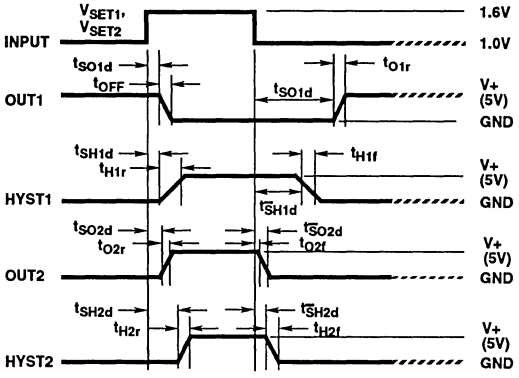


FIGURE 2. SWITCHING WAVEFORMS

Simple Threshold Detector

Figure 3 shows the simplest connection of the ICL7665S for threshold detection. From the graph (b), it can be seen that at low input voltage OUT1 is OFF, or high, while OUT2 is ON, or low. As the input rises (e.g., at power-on) toward V_{NOM} (usually the eventual operating voltage), OUT2 goes high on reaching V_{TR2}. If the voltage rises above V_{NOM} as much as V_{TR1}, OUT1 goes low. The equation giving V_{SET1} and V_{SET2} are from Figure 3(a):

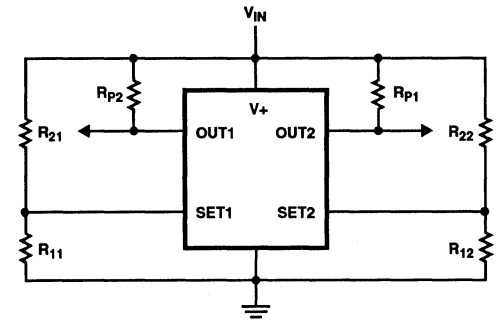
$$V_{SET1} = V_{IN}\frac{R_{11}}{(R_{11}+R_{21})}\ ;\ V_{SET2} = V_{IN}\frac{R_{12}}{(R_{12}+R_{22})}$$

Since the voltage to trip each comparator is nominally 1.3V, the value V_{IN} for each trip point can be found from

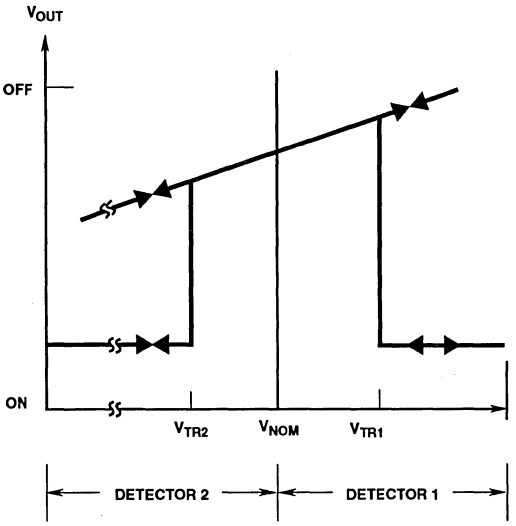
$$V_{TR1} = V_{SET1}\frac{(R_{11}+R_{21})}{R_{11}} = 1.3\frac{(R_{11}+R_{21})}{R_{11}} \quad \text{for detector 1}$$

and

$$V_{TR2} = V_{SET2}\frac{(R_{12}+R_{22})}{R_{12}} = 1.3\frac{(R_{12}+R_{22})}{R_{12}} \quad \text{for detector 2}$$

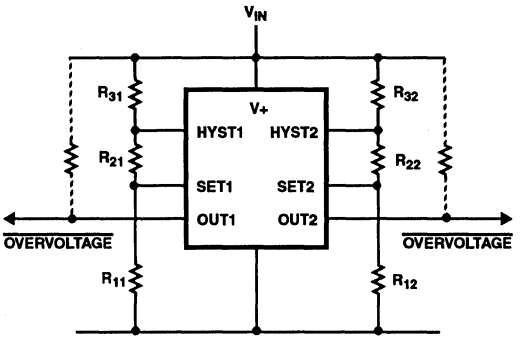


a.) Circuit Configuration

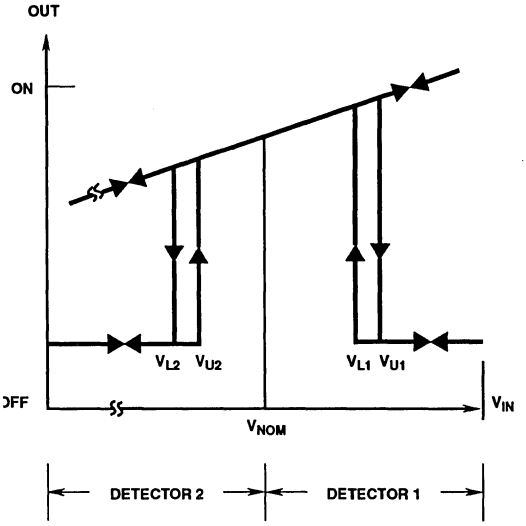


b.) Transfer Characteristics

FIGURE 3. SIMPLE THRESHOLD DETECTOR



a.) Circuit Configuration



b.) Transfer Characteristics

FIGURE 4. THRESHOLD DETECTOR WITH HYSTERESIS

Either detector may be used alone, as well as both together, in any of the circuits shown here.

When V_{IN} is very close to one of the trip voltage, normal variations and noise may cause it to wander back and forth across this level, leading to erratic output ON and OFF conditions. The addition of hysteresis, making the trip points slightly different for rising and falling inputs, will avoid this condition.

Threshold Detector with Hysteresis

Figure 4(a) shows how to set up such hysteresis, while Figure 4(b) shows how the hysteresis around each trip point produces switching action at different points depending on whether V_{IN} is rising or falling (the arrows indicated direction of change. The HYST outputs are basically switches which short out R_{31} or R_{32} when V_{IN} is above the respective trip point. Thus if the input voltage rises from a low value, the trip point will be controlled by R_{1n}, R_{2n}, and R_{3n}, until the trip point is reached. As this value is passed, the detector changes state, R_{3n} is shorted out, and the trip point becomes controlled by only R_{1n} and R_{2n}, a lower value. The input will then have to fall to this new point to restore the initial comparator state, but as soon as this occurs, the trip point will be raised again.

An alternative circuit for obtaining hysteresis is shown in Figure 5. In this configuration, the HYST pins put the extra resistor in parallel with the upper setting resistor. The values of the resistors differ, but the action is essentially the same. The governing equations are given in Table 1. These ignore the effects of the resistance of the HYST outputs, but these can normally be neglected if the resistor values are above about 100kΩ.

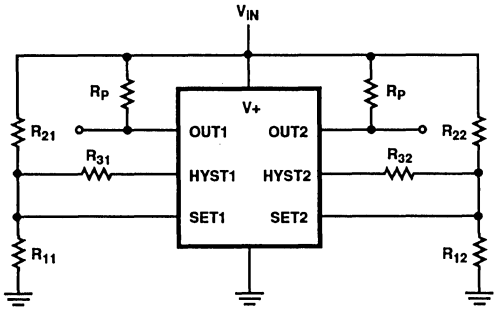


FIGURE 5. AN ALTERNATIVE HYSTERESIS CIRCUIT

TABLE 1. SET-POINT EQUATIONS

NO HYSTERESIS
Over-Voltage $V_{TRIP} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Over-Voltage $V_{TRIP} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
HYSTERESIS PER FIGURE 4(a)
$V_{U1} = \frac{R_{11} + R_{21} + R31}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}
$V_{L1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
$V_{U2} = \frac{R_{12} + R_{22} + R_{32}}{R_{12}} \times V_{SET2}$
Under-Voltage V_{TRIP}
$V_{L2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
HYSTERESIS PER FIGURE 5
$V_{U1} = \frac{R_{11} + R_{21}}{R_{11}} \times V_{SET1}$
Over-Voltage V_{TRIP}
$V_{L1} = \frac{R_{11} + \frac{R_{21}R_{31}}{R_{21} + R_{31}}}{R_{11}} \times V_{SET1}$
$V_{U2} = \frac{R_{12} + R_{22}}{R_{12}} \times V_{SET2}$
Over-Voltage V_{TRIP}
$V_{L2} = \frac{R_{12} + \frac{R_{22}R_{32}}{R_{22} + R_{32}}}{R_{12}} \times V_{SET2}$

Applications

Single Supply Fault Monitor

Figure 6 shows an over/under voltage fault monitor for a single supply. The over voltage trip point is centered around 5.5V and the under voltage trip point is centered around 4.5V. Both have some hysteresis to prevent erratic output ON and OFF conditions. The two outputs are connected in a wired OR configuration with a pullup resistor to generate a power OK signal.

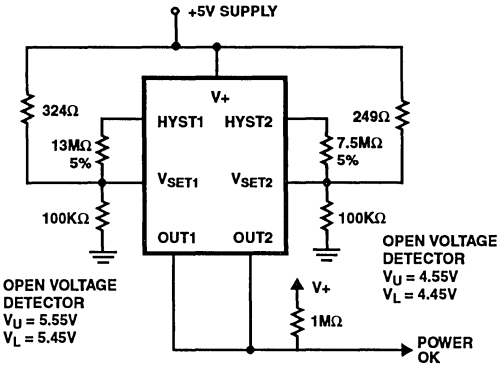


FIGURE 6. FAULT MONITOR FOR A SINGLE SUPPLY

Multiple Supply Fault Monitor

The ICL7665S can simultaneously monitor several supplies when connected as shown in Figure 7. The resistors are chosen such that the sum of the currents through R_{21A}, R_{21B}, and R_{31} is equal to the current through R_{11} when the two input voltage are at the desired low voltage detection point. The current through R_{11} at this point is equal to 1.3V/R_{11}. The voltage at the V_{SET} input depends on the voltage of both supplies being monitored. The trip voltage of one supply while the other supply is at the nominal voltage will be different that the trip voltage when both supplies are below their nominal voltages.

the other side of the ICL7665S can be used to detect the absence of negative supplies. The trip points for OUT1 depend on both the negative supply voltages and the actual voltage of the +5V supply.

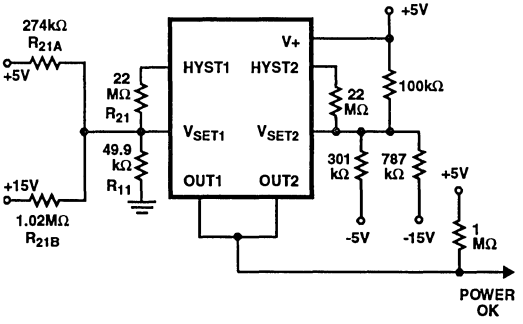


FIGURE 7. MULTIPLE SUPPLY FAULT MONITOR

Combination Low Battery Warning and Low Battery Disconnect

When using rechargeable batteries in a system, it is important to keep the batteries from being overdischarged. The circuit shown in Figure 8 provides a low battery warning and also disconnects the low battery from the rest of the system to prevent damage to the battery. OUT1 is used to shutdown the ICL7663S when the battery voltage drops to the value where the load should be disconnected. As long as V_{SET1} is greater than 1.3V, OUT1 is low, but when V_{SET1} drops below 1.3V, OUT1 goes high shutting off the ICL7663S. OUT2 is used for low battery warning. When V_{SET2} is greater than 1.3V, OUT2 is high and the low battery warning is on. When V_{SET2} drops below 1.3V, OUT2 is low and the low battery warning goes off. The trip voltage for low battery warning can be set higher than the trip voltage for shutdown to give advance low battery warning before the battery is disconnected.

Power Fail Warning and Powerup/Powerdown Reset

Figure 9 shows a power fail warning circuit with powerup/powerdown reset. When the unregulated DC input is above the trip point, OUT1 is low. When the DC input drops below the trip point, OUT1 shuts OFF and the power fail warning goes high. The voltage on the input of the 7805 will continue to provide 5V out at 1A until V_{IN} is less than 7.3V, this circuit will provide a certain amount of warning before the 5V output begins to drop.

The ICL7665S OUT2 is used to prevent a microprocessor from writing spurious data to a CMOS battery backup memory by causing OUT2 to go low when the 7805 5V output drops below the ICL7665S trip point.

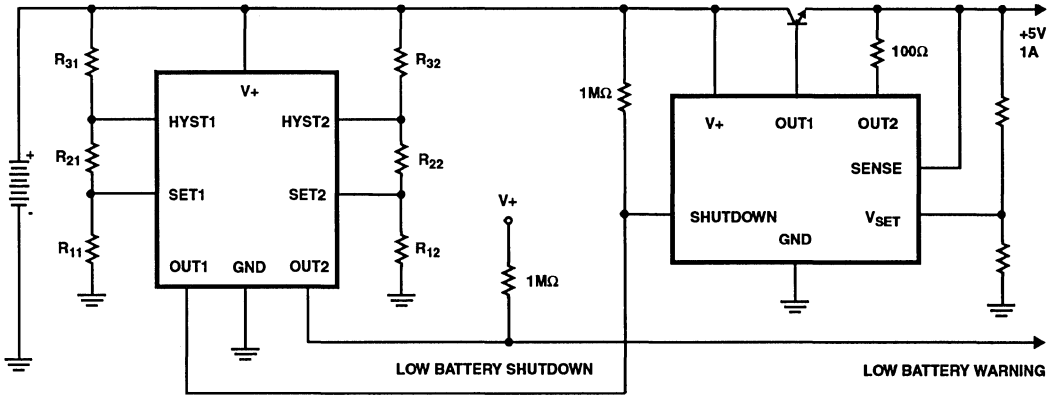


FIGURE 8. LOW BATTERY WARNING AND LOW BATTERY DISCONNECT

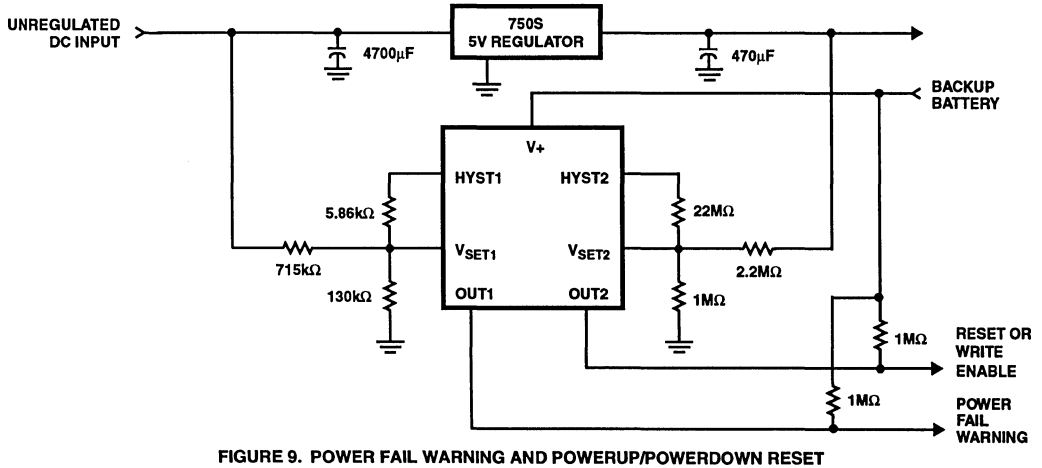


FIGURE 9. POWER FAIL WARNING AND POWERUP/POWERDOWN RESET

Simple High/Low Temperature Alarm

Figure 10 illustrates a simple high/low temperature alarm which uses the ICL7665S with an NPN transistor. The voltage at the top of R_1 is determined by the V_{BE} of the transistor and the position of R_1's wiper arm. This voltage has a negative temperature coefficient. R_1 is adjusted so that V_{SET2} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the high temperature alarm. When this occurs, OUT2 goes low. R_2 is adjusted so that V_{SET1} equals 1.3V when the NPN transistor's temperature reaches the temperature selected for the low temperature alarm. When the temperature drops below this limit, OUT1 goes low.

AC Power Fail and Brownout Detector

Figure 11 shows a circuit that detects AC undervoltage by monitoring the secondary side of the transformer. The capacitor, C_1, is charged through R_1 when OUT1 is OFF. With a normal 100 VAC input to the transformer, OUT1 will discharge C_1 once every cycle, approximately every 16.7ms. When the AC input voltage is reduced, OUT1 will stay OFF, so that C_1 does not discharge. When the voltage on C_1 reaches 1.3V, OUT2 turns OFF and the power fail warning goes high. The time constant, R_1C_1, is chosen such that it takes longer than 16.7ms to charge C_1 1.3V.

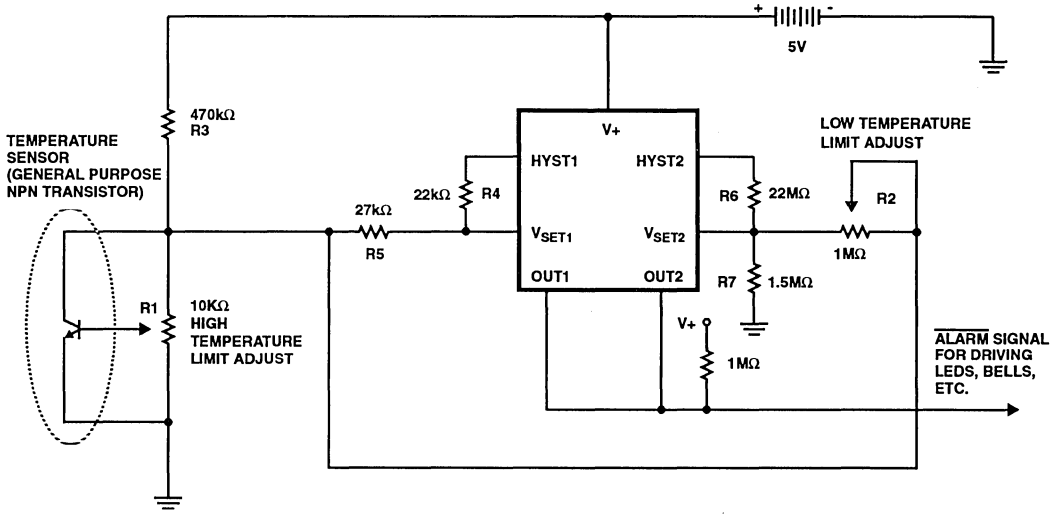


FIGURE 10. SIMPLE HIGH/LOW TEMPERATURE ALARM

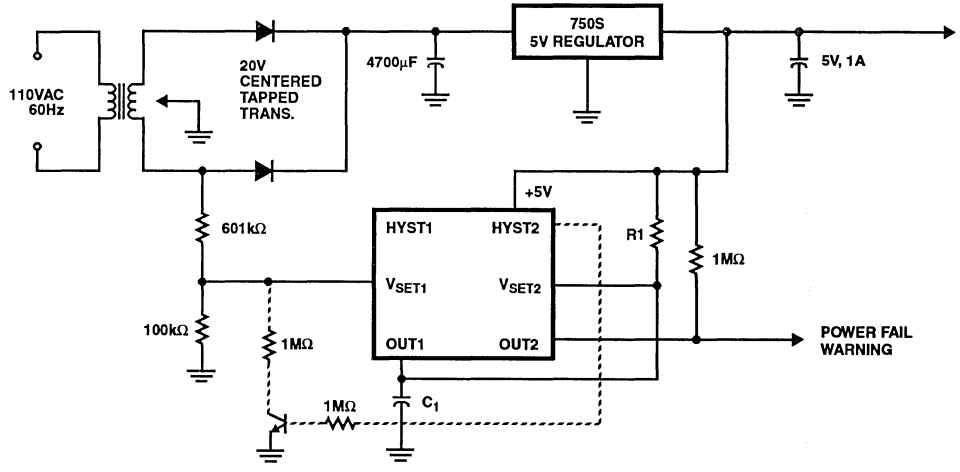


FIGURE 11. AC POWER FAIL AND BROWNOUT DETECTOR

HARRIS SEMICONDUCTOR

ICL7673

May 1992

Automatic Battery Back-Up Switch

Features

- Automatically Connects Output to the Greater of Either Input Supply Voltage
- If Main Power to External Equipment is Lost, Circuit Will Automatically Connect Battery Backup
- Reconnects Main Power When Restored
- Logic Indicator Signaling Status of Main Power
- Low Impedance Connection Switches
- Low Internal Power Consumption
- Wide Supply Range: ..... 2.5V to 15V
- Low Leakage Between Inputs
- External Transistors May Be Added if Very Large Currents Need to Be Switched

Applications

- On Board Battery Backup for Real-Time Clocks, Timers, or Volatile RAMs
- Over/Under Voltage Detector
- Peak Voltage Detector
- Other Uses:
  - Portable Instruments, Portable Telephones, Line Operated Equipment

Description

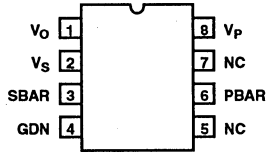
The Harris ICL7673 is a monolithic CMOS battery backup circuit that offers unique performance advantages over conventional means of switching to a backup supply. The ICL7673 is intended as a low-cost solution for the switching of systems between two power supplies; main and battery backup. The main application is keep-alive-battery power switching for use in volatile CMOS RAM memory systems and real time clocks. In many applications this circuit will represent a low insertion voltage loss between the supplies and load. This circuit features low current consumption, wide operating voltage range, and exceptionally low leakage between inputs. Logic outputs are provided that can be used to indicate which supply is connected and can also be used to increase the power switching capability of the circuit by driving external PNP transistors.

Ordering Information

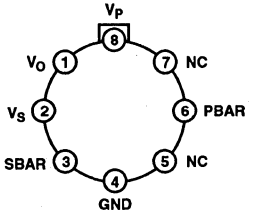
PART NUMBER	TEMPERATURE	PACKAGE
ICL7673CPA	0°C to +70°C	8 Lead Mini-DIP
ICL7673CBA	0°C to +70°C	8 Lead SOIC
ICL7673ITV	-25°C to +85°C	9 Lead TO-99

Pinouts

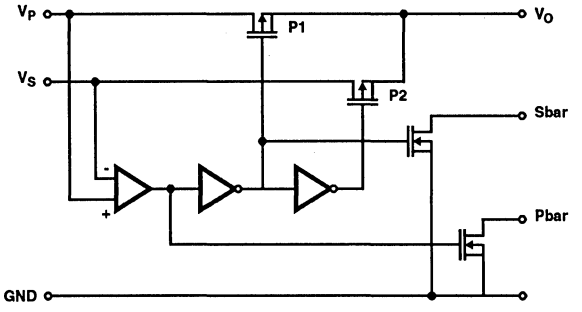
8 LEAD SOIC AND MINI-DIP
TOP VIEW



8 LEAD TO-99
TOP VIEW



Functional Block Diagram



VP > VS, P1 SWITCH ON AND Pbar SWITCH ON
VS > VP, P2 SWITCH ON AND Sbar SWITCH ON

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3183

Absolute Maximum Ratings

Input Supply (V_P or V_S) Voltage ..... GND - 0.3V to +18V
Output Voltages P_{bar} and S_{bar} ..... GND - 0.3V to +18V
Peak Current
- Input V_P (at V_P = 5V) See Note 38mA
- Input V_S (at V_S = 3V) 30mA
- Pbar or Sbar 150mA

Continuous Current
- Input V_P (at V_P = 5V) See Note 38mA
- Input V_S (at V_S = 3V) 30mA
- Pbar or Sbar 50mA

Package Dissipation 300mW
Derate ..... 6.1mW/°C

NOTE: Derate above +25°C by 0.38mA/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range:
ICL7673C ..... 0°C to +70°C
ICL7673I ..... -25°C to +85°C
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... 300°C

Electrical Specifications (T_A = +25°C Unless Otherwise Specified)

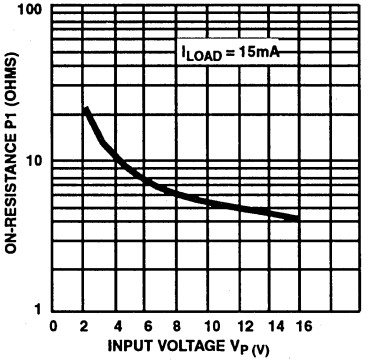
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Input Voltage	V_P	V_S = 0V, I_{LOAD} = 0mA	2.5	-	15	V
	V_S	V_P = 0V, I_{LOAD} = 0mA	2.5	-	15	V
Quiescent Supply Current	I+	V_P = 0V, V_S = 3V, I_{LOAD} = 0mA	-	1.5	5	µA
Switch Resistance P1 (Note 1)	$R_{ds(on)}$P1	V_P = 5V, V_S = 3V, I_{LOAD} = 15mA	-	8	15	Ω
		At T_A = 85°C	-	16	-	Ω
		V_P = 9V, V_S = 3V, I_{LOAD} = 15mA	-	6	-	Ω
		V_P = 12V, V_S = 3V, I_{LOAD} = 15mA	-	5	-	Ω
Temperature Coefficient of Switch Resistance P1	$T_{C(P1)}$	V_P = 5V, V_S = 3v, I_{LOAD} = 15mA	-	0.5	-	%/°C
Switch Resistance P2 (Note 1)	$R_{ds(on)}$P2	V_P = 0V, V_S = 3V, I_{LOAD} = 1mA	-	40	100	Ω
		At T_A = 85°C	-	60	-	Ω
		V_P = 0V, V_S = 5V, I_{LOAD} = 1mA	-	26	-	Ω
		V_P = 0V, V_S = 9V, I_{LOAD} = 1mA	-	16	-	Ω
Temperature Coefficient of Switch Resistance P2	$T_{C(P2)}$	V_P = 0V, V_S = 3V, I_{LOAD} = 1mA	-	0.7	-	%/°C
Leakage Current (V_P to V_S)	$I_{L(PS)}$	V_P = 5V, V_S = 3V, I_{LOAD} = 10mA	-	0.01	20	nA
		At T_A = 85°C	-	35	-	nA
Leakage Current (V_P to V_S)	$I_{L(SP)}$	V_P = 0V, V_S = 3V, I_{LOAD} = 10mA	-	0.01	50	nA
		at T_A = 85°C	-	120	-	nA
Open Drain Output Saturation Voltages	V_{OPbar}	V_P = 5V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	85	400	mV
		At T_A = 85°C	-	120	-	mV
		V_P = 9V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	50	-	mV
		V_P = 12V, V_S = 3V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	40	-	mV

Electrical Specifications (T_A = +25°C Unless Otherwise Specified) **(Continued)**

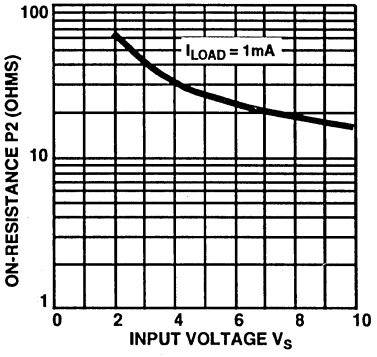
PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Open Drain Output Saturation Voltages	V_{OSbar}	V_P = 0V, V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 0mA	-	150	400	mV
		at T_A = 85°C	-	210	-	mV
		V_P = 0V, V_S = 5V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	85	-	mV
		V_P = 0V, V_S = 9V, I_{SINK} = 3.2mA I_{LOAD} = 0mA	-	50	-	mV
Output Leakage Currents of P_{bar} and S_{bar}	I_{LPbar}	V_P = 0V, V_S = 15V, I_{LOAD} = 0mA	-	50	500	nA
		at T_A = 85°C	-	900	-	nA
	I_{LSbar}	V_P = 15V, V_S = 0V, I_{LOAD} = 0mA	-	50	500	nA
		at T_A = 85°C	-	900	-	nA
Switchover Uncertainty for Complete Switching of Inputs and Open Drain Outputs	V_P - V_S	V_S = 3V, I_{SINK} = 3.2mA, I_{LOAD} = 15mA	-	±10	±50	mV

NOTE:
1. The Minimum input to output voltage can be determined by multiplying the load current by the switch resistance.

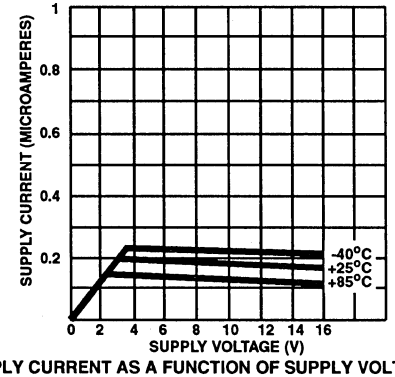
Typical Performance Characteristics



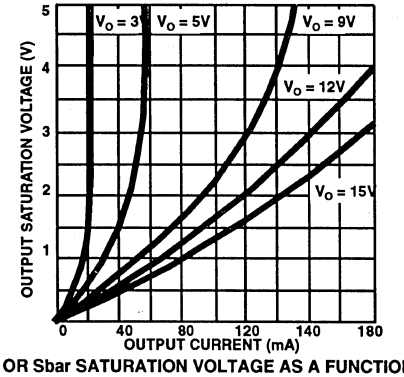
ON-RESISTANCE SWITCH P1 AS A FUNCTION OF INPUT VOLTAGE V_P



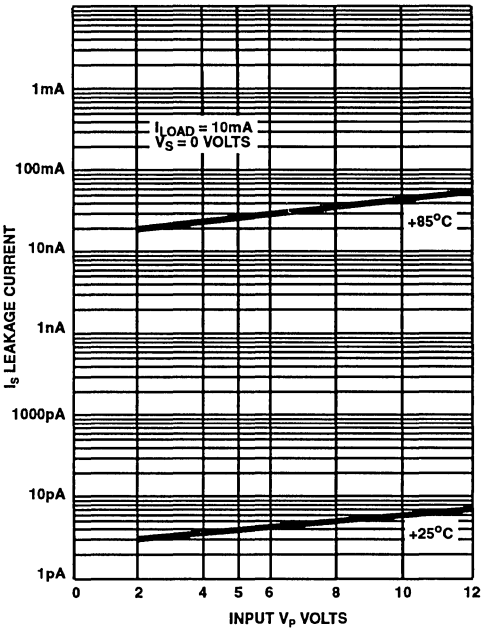
ON-RESISTANCE SWITCH P2 AS A FUNCTION OF INPUT VOLTAGE V_S



SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



Pbar OR Sbar SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



I_S LEAKAGE CURRENT V_P TO V_S AS A FUNCTION OF INPUT VOLTAGE

Detailed Description

As shown in the functional diagram (Figure 1), the ICL7673 includes a comparator which senses the input voltages V_P and V_S. The output of the comparator drives the first inverter and the open-drain N-channel transistor P_{bar}. The first inverter drives a large P-channel switch, P1, a second inverter, and another open-drain N-channel transistor, S_{bar}. The second inverter drives another large P-channel switch P2. The ICL7673, connected to a main and a backup power supply, will connect the supply of greater potential to its output. The circuit provides break-before-make switch action as it switches from main to backup power in the event of a main power supply failure. For proper operation, inputs V_P and V_S must not be allowed to float, and, the difference in the two supplies must be greater than 50 millivolts. The leakage current through the reverse biased parasitic diode of switch P_2 is very low.

Output Voltage

The output operating voltage range is 2.5 to 15 volts. The insertion loss between either input and the output is a function of load current, input voltage, and temperature. This is due to the P-channels being operated in their triode region, and, the ON-resistance of the switches is a function of output voltage V_O. The ON-resistance of the P-channels have positive temperature coefficients, and therefore as temperature increases the insertion loss also increases. At low load currents the output voltage is nearly equal to the greater of the two inputs. The maximum voltage drop across switch P1 or P2 is 0.5 volts, since above this voltage the body-drain parasitic diode will become forward biased. Complete switching of the inputs and open-drain outputs typically occurs in 50 microseconds.

Input Voltage

The input operating voltage range for VP or VS is 2.5 to 15 volts. The input supply voltage (VP or VS) slew rate should be limited to 2 volts per microsecond to avoid potential harm to the circuit. In line-operated systems, the rate-of-rise (or fall) of the supply is a function of power supply design. For battery applications it may be necessary to use a capacitor between the input and ground pins to limit the rate-of-rise of the supply voltage. A low-impedance capacitor such as a 0.047µF disc ceramic can be used to reduce the rate-of-rise.

Status Indicator Outputs

The N-channel open drain output transistors can be used to indicate which supply is connected, or can be used to drive external PNP transistors to increase the power switching capability of the circuit. When using external PNP power transistors, the output current is limited by the beta and thermal characteristics of the power transistors. The application section details the use of external PNP transistors.

Applications

A typical discrete battery backup circuit is illustrated in Figure 3. This approach requires several components, substantial printed circuit board space, and high labor cost. It also consumes a fairly high quiescent current. The ICL7673 battery backup circuit, illustrated in Figure 4, will often replace such discrete designs and offer much better performance, higher reliability, and lower system manufacturing cost. A trickle charge system could be implemented with an additional resistor and diode as shown in Figure 5. A complete low power AC to regulated DC system can be implemented using the ICL7673 and ICL7663S micropower voltage regulator as shown in Figure 6.

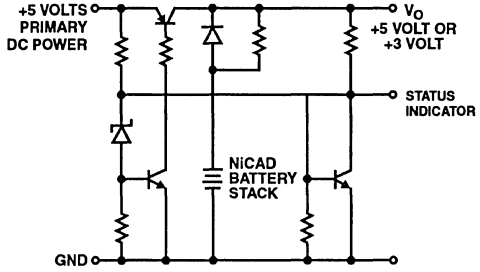


FIGURE 1. DISCRETE BATTERY BACKUP CIRCUIT

Applications for the ICL7673 include volatile semiconductor memory storage systems, real-time clocks, timers, alarm systems, and over/under the voltage detectors. Other systems requiring DC power when the master AC line supply fails can also use the ICL7673.

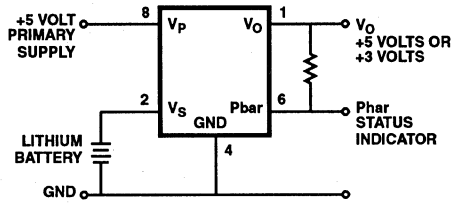


FIGURE 2. ICL7673 BATTERY BACKUP CIRCUIT

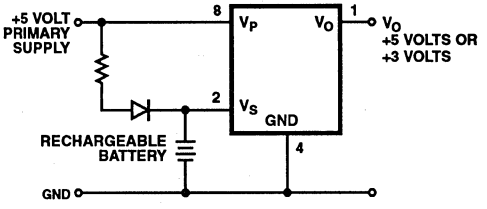


FIGURE 3. APPLICATION REQUIRING RECHARGEABLE BATTERY BACKUP

A typical application, as illustrated in Figure 7, would be a microprocessor system requiring a 5 volt supply. In the event of primary supply failure, the system is powered down, and a 3 volt battery is employed to maintain clock or volatile memory data. The main and backup supplies are connected to V_P and V_S, with the circuit output V_O supplying power to the clock or volatile memory. The ICL7673 will sense the main supply, when energized, to be of greater potential than V_S and connect, via its internal MOS switches, V_P to output V_O. The backup input, V_S will be disconnected internally. In the event of main supply failure, the circuit will sense that the backup supply is now the greater potential, disconnect V_P from V_O, and connect V_S.

Figure 8 illustrates the use of external PNP power transistors to increase the power switching capability of the circuit. In this application the output current is limited by the beta and thermal characteristics of the power transistors.

If hysteresis is desired for a particular low power application, positive feedback can be applied between the input V_P and open drain output S_{bar} through a resistor as illustrated in Figure 9. For high power applications hysteresis can be applied as shown in Figure 10.

The ICL7673 can also be used as a clipping circuit as illustrated in Figure 11. With high impedance loads the circuit output will be nearly equal to the greater of the two input signals.

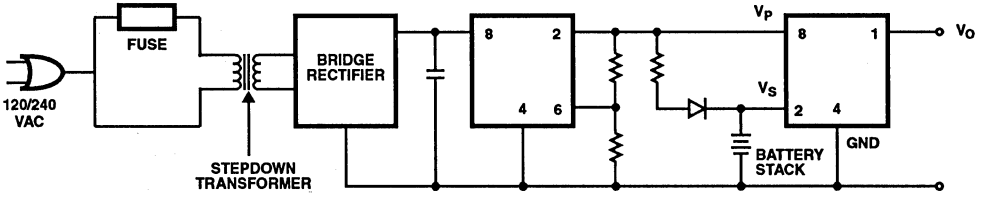


FIGURE 4. POWER SUPPLY FOR LOW POWER PORTABLE AC TO DC SYSTEMS

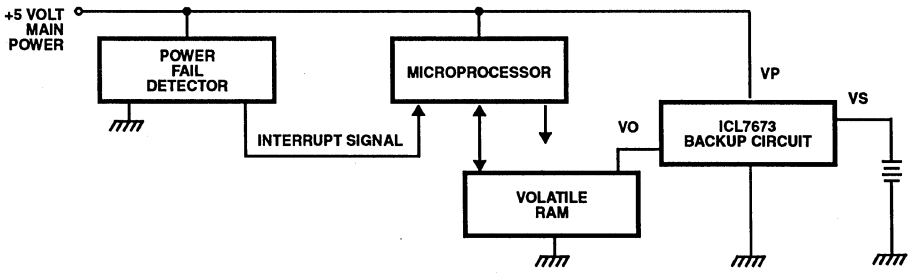


FIGURE 5. TYPICAL MICROPROCESSOR MEMORY APPLICATION

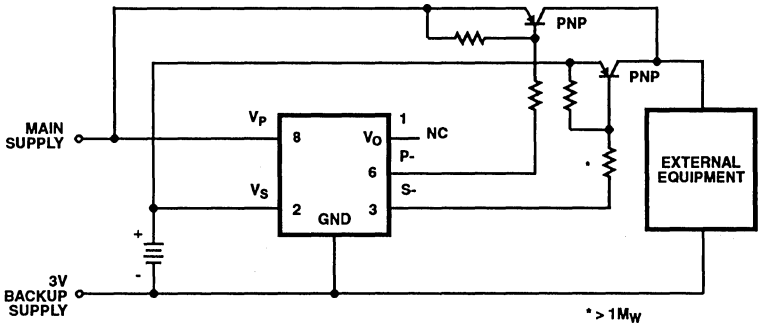


FIGURE 6. HIGH CURRENT BATTERY BACKUP SYSTEM

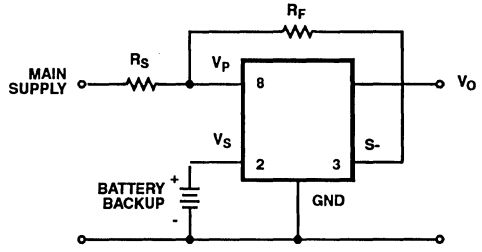


FIGURE 7. LOW CURRENT BATTERY BACKUP SYSTEM WITH HYSTERESIS

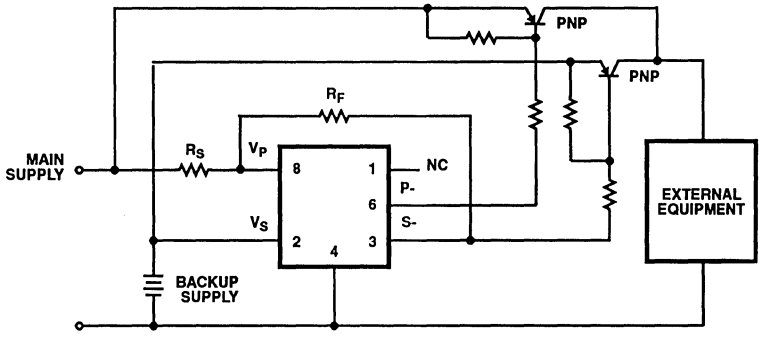


FIGURE 8. HIGH CURRENT BACKUP SYSTEM WITH HYSTERESIS

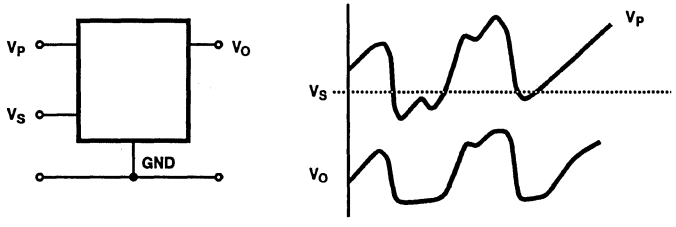


FIGURE 9. CLIPPLING CIRCUITS

HARRIS SEMICONDUCTOR

ICL8211
ICL8212

May 1992

Programmable Voltage Detectors

Features

- High Accuracy Voltage Sensing and Generation
- Internal Reference 1.15V Typical
- Low Sensitivity to Supply Voltage and Temperature Variations
- Wide Supply Voltage Range Typ. 1.8V to 30V
- Essentially Constant Supply Current Over Full Supply Voltage Range
- Easy to Set Hysteresis Voltage Range
- Defined Output Current Limit ICL8211
- High Output Current Capability ICL8212

Applications

- Low Voltage Sensor/Indicator
- High Voltage Sensor/Indicator
- Nonvolatile Out-of-Voltage Range Sensor/Indicator
- Programmable Voltage Reference or Zener Diode
- Series or Shunt Power Supply Regulator
- Fixed Value Constant Current Source

Description

The Harris ICL8211/8212 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7mA current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15V (the internal reference). The ICL8212 requires a voltage in excess of 1.15V to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

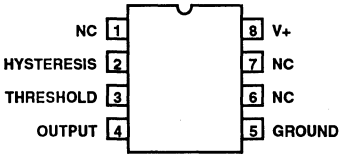
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL82IICPA	0°C to +70°C	8 Lead Mini-DIP
ICL8211CBA	0°C to +70°C	8 Lead SOIC
ICL8211CTY	0°C to +70°C	TO-99 Can
ICL8211MTY*	-55°C to +125°C	TO-99 Can
ICL8212CPA	0°C to +70°C	8 lead Mini-DIP
ICL8212CBA	0°C to +70°C	8 lead SOIC
ICL8212CTY	0°C to +70°C	TO-99 Can
ICL8212MTY*	-55°C to +125°C	TO-99 Can

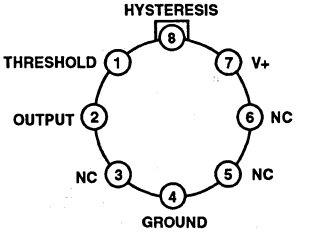
* Add /883B to part number if 883B processing is required

Pinouts

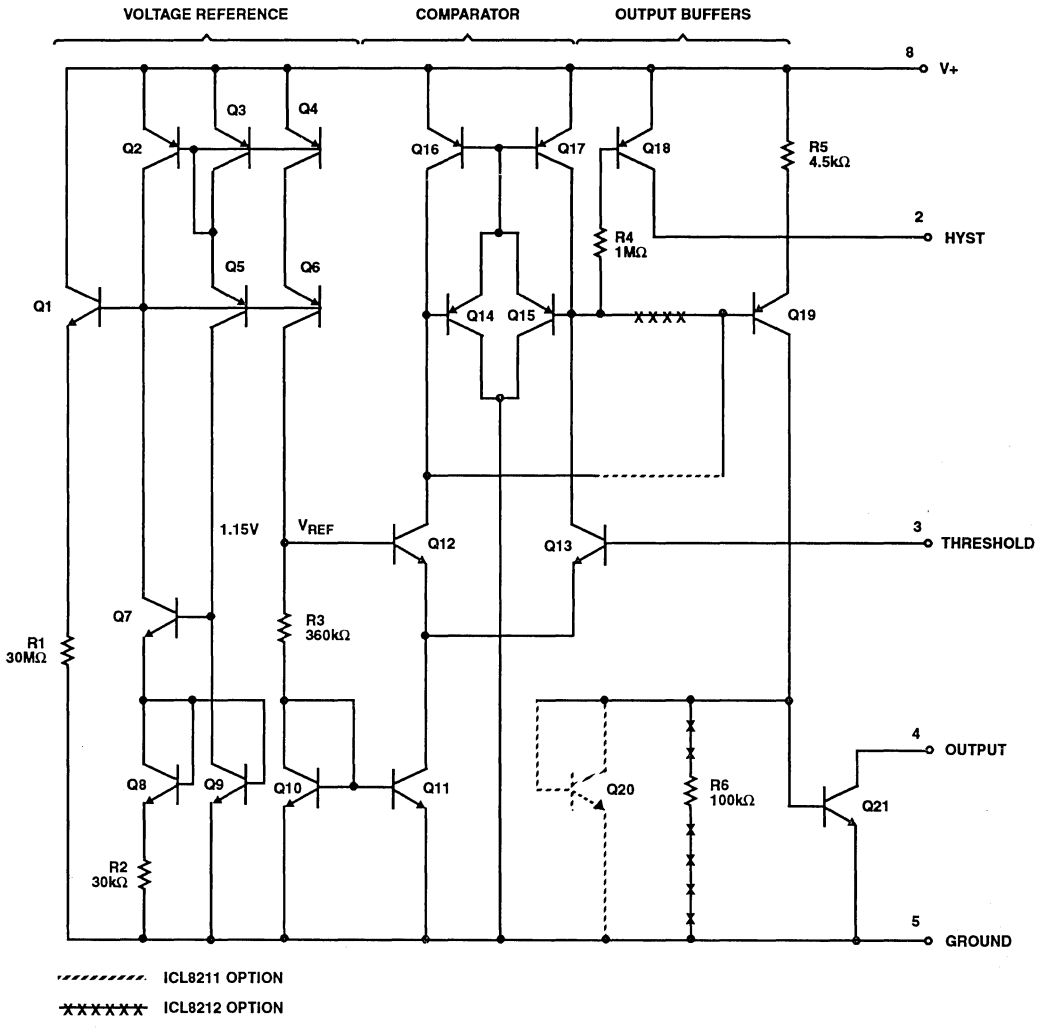
8 LEAD MINI-DIP AND SOIC
TOP VIEW



8 LEAD TO-99 CAN
TOP VIEW



Functional Diagram



Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +30V
Output Voltage ..... -0.5V to +30V
Hysteresis Voltage ..... +0.5V to -10V
Threshold Input Voltage .....+30V to -5V with respect to GROUND and +0V to -30V with respect to V+
Current into Any Terminal ..... ± 30mA

Lead Temperature (Soldering, 10s)..... 300°C
Current into Any Terminal ..... ± 30mA
Lead Temperature (Soldering, 10s) 300°CMaximum Package Power Dissipation (Notes 1 and 2)..... 300mW

NOTES:

1. Rating applies for case temperatures to +125°C to ICL8211 MTY/8212MTY products. Derate linearly at -10mW/°C for ambient temperatures above 100°C.
2. Derate linearly above 50°C by -10mW/°C for ICL8211C/ICL8212C products. The threshold input voltage may exceed 17V for short periods of time. However, for continuous operation this voltage must be maintained at a value less than 7V.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Temperature Range
ICL8211M/8212M ..... -55°C to +125°C
ICL8211C/8212C ..... 0°C to +70°C

StorageTemperature Range ..... -65°C to +150°C

Electrical Specifications $V+ = 5V$, $T_A = +25°C$ Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		ICL8211			ICL8212			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Supply Current	I+	2.0 < V+ < 30	V_{TH} = 1.3V	10	22	40	50	110	250	µA
			V_{TH} = 0.9V	50	140	250	10	20	40	µA
Threshold Trip Voltage	V_{TH}	I_{OUT} = 4mA, V_{OUT} = 2V	V+ = 5V	0.98	1.15	1.19	1.00	1.15	1.19	V
			V+ = 2V	0.98	1.145	1.19	1.00	1.145	1.19	V
			V+ = 30V	1.00	1.165	1.20	1.05	1.165	1.20	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	I_{OUT} = 4mA, I_{HYST} = 7mA, V_{OUT} = 2V, V_{HYST} = 3V		-	-0.8	-	-	-0.5	-	mV
Guaranteed Operating Supply Voltage Range (Note 5)	V_{SUPPLY}	+25°C		2.0	-	30	2.0	-	30	V
		0°C to +70°C		2.2	-	30	2.2	-	30	V
Minimum Operating Supply Voltage Range	V_{SUPPLY}	+25°C		-	1.8	-	-	1.8	-	V
		+125°C		-	1.4	-	-	1.4	-	V
		-55°C		-	1.5	-	-	2.5	-	V
Threshold Voltage Temperature Coefficient	$\Delta V_{TH}/\Delta T$	I_{OUT} = 4mA, V_{OUT} = 2V		-	± 200	-	-	± 200	-	ppm/°C
Variation of Threshold Voltage with Supply Voltage	$\Delta V_{TH}/\Delta V+$	ΔV+ = 10% at V+ = 5V		-	1.0	-	-	1.0	-	mV
Threshold Input Current	I_{TH}	V_{TH} = 1.15V		-	100	250	-	100	250	nA
		V_{TH} = 1.00V		-	5	-	-	5	-	nA
Output Leakage Current	I_{OLK}	V_{OUT} = 30V	V_{TH} = 0.9V	-	-	-	-	-	10	µA
			V_{TH} = 1.3V	-	-	10	-	-	-	µA
		V_{OUT} = 5V	V_{TH} = 0.9V	-	-	-	-	-	1	µA
			V_{TH} = 1.3V	-	-	1	-	-	-	µA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 4mA	V_{TH} = 0.9V	-	0.17	0.4	-	-	-	V
			V_{TH} = 1.3V	-	-	-	-	0.17	0.4	V

Electrical Specifications V+ = 5V, T_A = +25°C Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		ICL8211 MIN	ICL8211 TYP	ICL8211 MAX	ICL8212 MIN	ICL8212 TYP	ICL8212 MAX	UNITS
Max Available Output Current	I_{OH}	(Notes 3 & 4) V_{OUT} = 5V	V_{TH} = 0.9V	4	7.0	12	-	-	-	mA
			V_{TH} = 1.3V	-	-	-	15	35	-	mA
Hysteresis Leakage Current	I_{LHYS}	V+ = 10V, V_{HYST} = GND	V_{TH} = 1.0V	-	-	0.1	-	-	0.1	mA
Hysteresis Sat Voltage	$V_{HYS(MAX)}$	I_{HYST} = -7mA, measured with respect to V+	V_{TH} = 1.3V	-	-0.1	-0.2	-	-0.1	-0.2	V
Max Available Hysteresis Current	$I_{HYS\ (MAX)}$		V_{TH} = 1.3V	-15	-21	-	-15	-21	-	mA

NOTES:

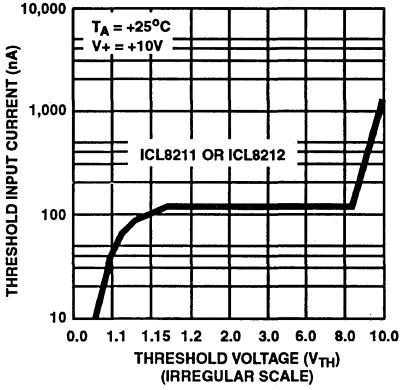
3. The maximum output current of the ICL8211 is limited by design to 15mA under any operating conditions. The output voltage may be sustained at any voltage up to +30V as long as the maximum power dissipation of the device is not exceeded.
4. The maximum output current of the ICL8212 is not defined. And systems using the ICL8212 must therefore ensure that the output current does not exceed 30mA and that the maximum power dissipation of the device is not exceeded.
5. Threshold Trip Voltage is 0.80V(min) to 1.30V(mas). At I_{OUT} = 3mA.

Electrical Specifications **ICL8211MTY/8212MTY** V+ = 5V, T_A = -55°C to +125°C

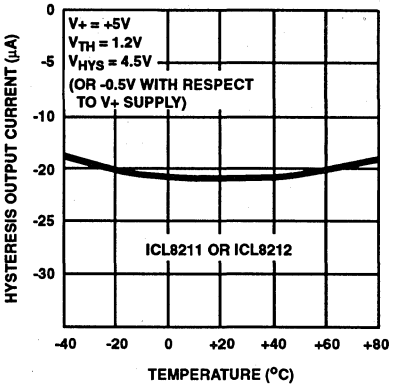
PARAMETER	SYMBOL	TEST CONDITIONS		ICL8211 MIN	ICL8211 TYP	ICL8211 MAX	ICL8212 MIN	ICL8212 TYP	ICL8212 MAX	UNITS
Supply Current	I+	2.8 < V+ < 30		-	-	-	-	-	-	-
		V_T = 1.3V		-	-	100	-	350	350	mA
		V_T = 0.8V		-	-	350	-	100	100	mA
Threshold Trip Voltage	V_{TH}	I_{OUT} = 2mA V_{OUT} = 2V	V+ = 2.8V	0.80	-	1.30	0.80	-	1.30	V
			V+ = 30V	0.80	-	1.30	0.80	-	1.30	V
Guaranteed Operating Supply Voltage Range	V_{SUPPLY}	(Note 5)		2.8	-	30	2.8	-	30	V
Threshold Input Current	I_{TH}	V_{TH} = 1.15V		-	-	400	-	-	400	nA
Output Leakage Current	I_{OLK}	V_{OUT} = 30V	V_{TH} = 0.8V	-	-	-	-	-	20	mA
			V_{TH} = 1.3V	-	-	20	-	-	-	mA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 3mA	V_{TH} = 0.8V	-	-	0.5	-	-	-	V
			V_{TH} = 1.3V	-	-	-	-	-	0.5	V
Max Available Output Current	I_{OH}	(Notes 3 & 4) V_{OUT} = 5V	V_{TH} = 0.8	3	-	15	-	-	-	mA
			V_{TH} = 1.3V	-	-	-	9	-	-	mA
Hysteresis Leakage Current	I_{LHYS}	V+ = 10V V_{HYST} = GND	V_{TH} = 0.8V	-	-	0.2	-	-	0.2	mA
Hysteresis Saturation Voltage	$V_{HYS(MAX)}$	I_{HYST} = -7mA measured with respect to V+	V_{TH} = 1.3V	-	-	0.3	-	-	0.3	V
Max Available Hysteresis Current	$I_{HYS\ (MAX)}$		V_{TH} = 1.3V	10	-	-	10	-	-	mA

Typical Performance Characteristics (ICL8211 and ICL8212)

THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE

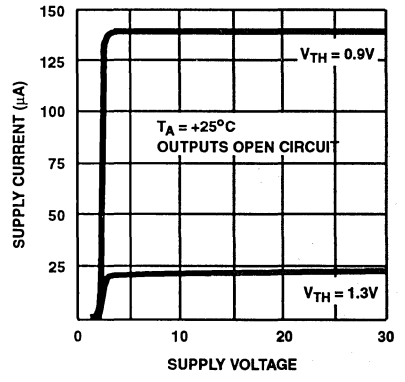


HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

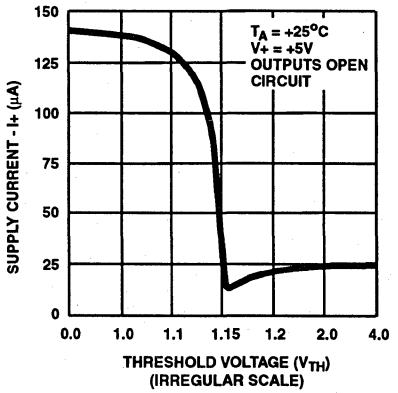


Typical Performance Characteristics (ICL8211 ONLY)

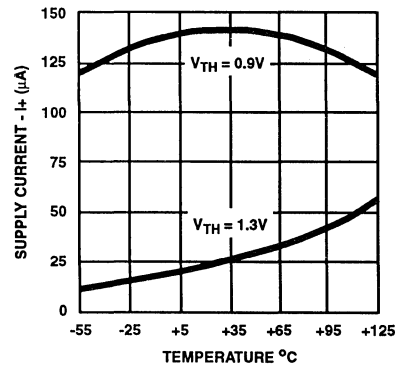
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



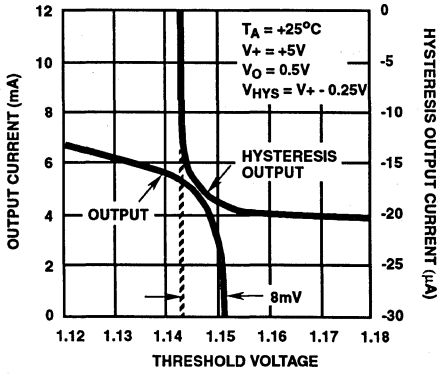
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

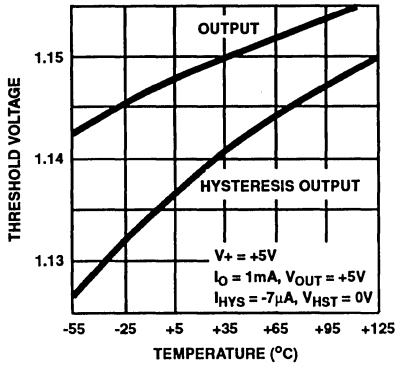


OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE

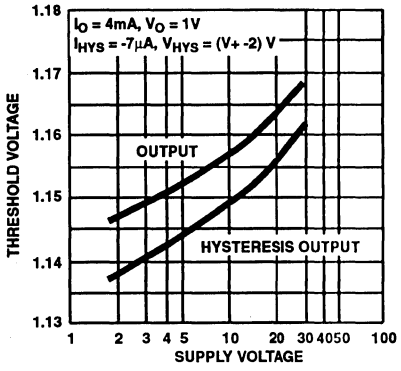


Typical Performance Characteristics (ICL8211 ONLY) (Continued)

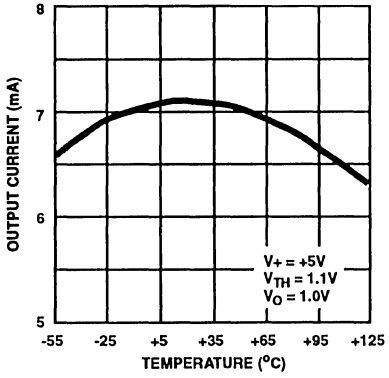
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



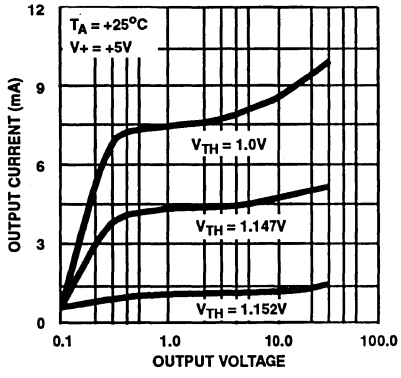
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



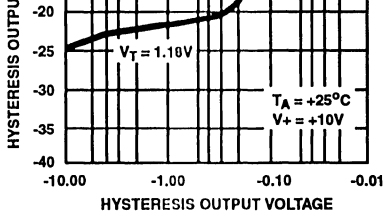
OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

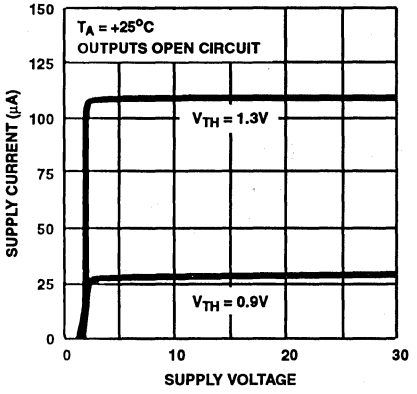


HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE

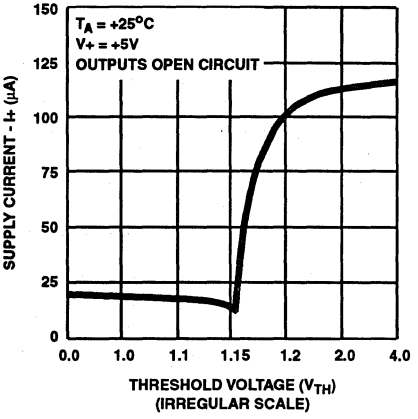


Typical Performance Characteristics (ICL8212 ONLY)

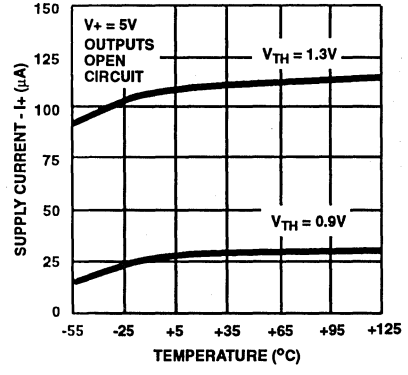
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



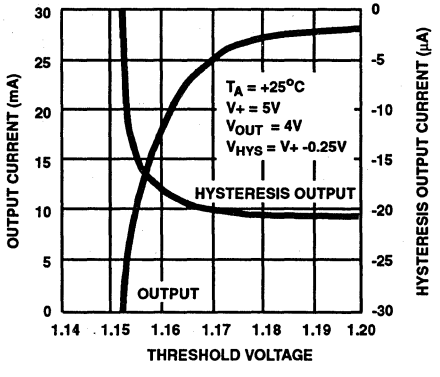
SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE



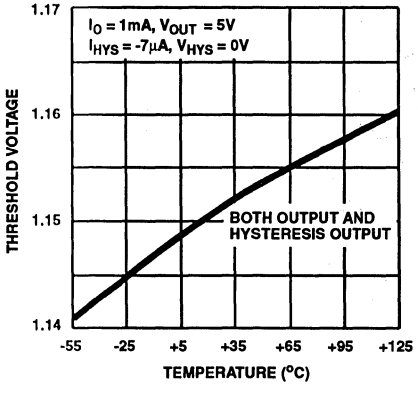
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



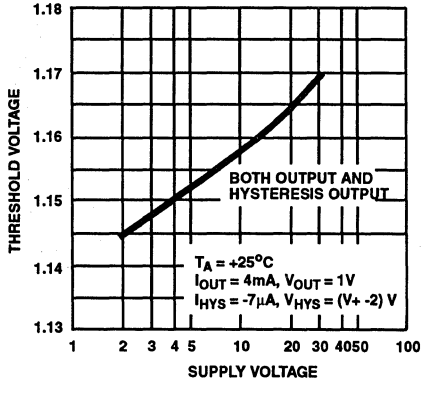
OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE



THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE



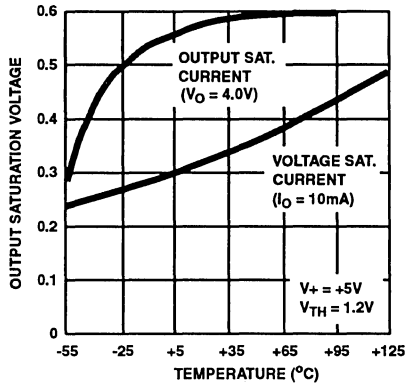
THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE



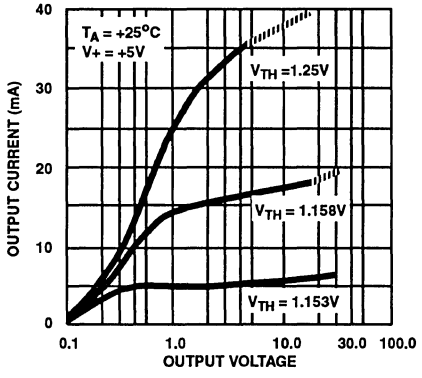
Typical Performance Characteristics

(ICL8212 ONLY) **(Continued)**

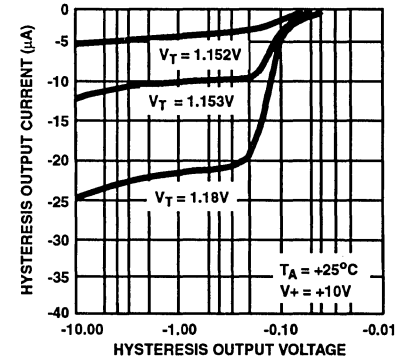
OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE



OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE



HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE



Detailed Description

The ICL8211 and ICL8212 use standard linear bipolar integrated circuit technology with high value thin film resistors which define extremely low value currents.

Components Q_1 through Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15V. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (-5000 ppm per °C).

Components Q_2 through Q_9 and R_2 make up a constant current source; Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9, and due to the current mirror, the collector currents of Q_8 and Q_9 are forced to be equal and it can be shown that the collector current in Q_8 and Q_9 is

$$IC\ (Q_8 \text{ or } Q_9) = \frac{1}{R2} \times \frac{kT}{q} \ln 7$$

or approximately 1µA at +25°C

Where k = Boltzman's Constant
q = Charge on an Electron
and T = Absolute Temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the V_{CE} of Q_3, Q_4, and Q_9 remain constant with supply voltage variations. This ensures a constant current supply free from variations.

The base current of Q_1 provides sufficient start up current for the constant source; there being two stable states for this type of circuit - either ON as defined above, or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; Q_{10} is matched to Q_9. Thus the IC and V_{BE} of Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage, it is necessary to sum a voltage equal to the base emitter voltage of Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densties.

$$\text{Thus } 1.5 = V_{BE}\ (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q}$$

$$\text{which provides: } \frac{R3}{R2} = 12 \text{ (approximately.)}$$

The total supply current consumed by the voltage reference section is approximately 6µA at room temperature. A voltage at the THRESHOLD input is compared to the reference 1.15V by the comparator consisting of transistors Q_{11} through Q_{17}. The outputs from the comparator are limited to two diode drops less than V+ or approximately 1.1V. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100µA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximately 7mA, whereas for the ICL8212

almost all the collector current of Q_{19} is available for base drive to Q_{21}, resulting in a maximum available collector current of the order of 30mA. It is advisable to externally limit this current to 25mA or less.

Applications

The ICL8211 and ICL8212 are similar in many respects, especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices, and where differences occur they are clearly noted.

General Information

Threshold Input Considerations

Although any voltage between -5V and V+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6V since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

The outputs change states with an input THRESHOLD voltage of approximately 1.15V. Input and output waveforms are shown in Figure 1 for a simple 1.15V level detector.

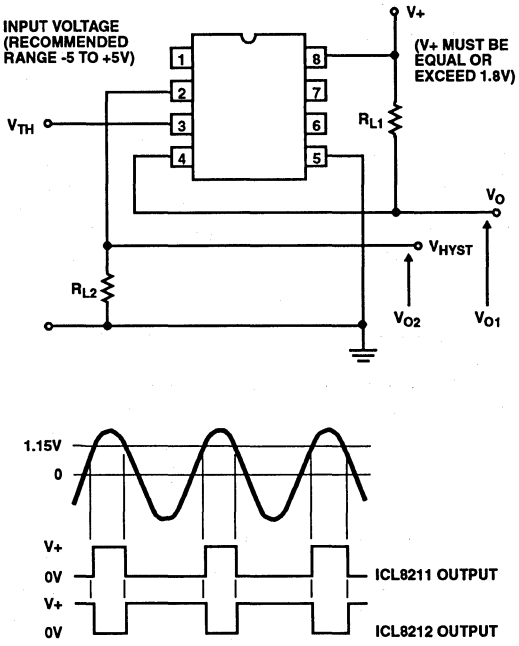


FIGURE 1. VOLTAGE LEVEL DETECTION

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10µA or less.

The regular OUTPUT's from either the ICL8211 or ICL8212 may be used to drive most of the common logic families such as TTL or CMOS using a single pullup resistor. There is a guaranteed TTL fanout of 2 for the ICL8211 and 4 for the ICL8212.

A principal application of the ICL8211 is voltage level detection, and for that reason the OUTPUT current has been limited to typically 7mA to permit direct drive of an LED connected to the positive supply without a series current limiting resistor.

On the other hand the ICL8212 is intended for applications such as programmable zener references, and voltage regulators where output currents well in excess of 7mA are desirable. Therefore, the output of the ICL8212 is not current limited, and if the output is used to drive an LED, a series current limiting resistor must be used.

In most applications an input resistor divider network may be used to generate the 1.15V required for V_{TH}. For high accuracy, currents as large as 50µA may be used, however for those applications where current limiting may be desirable, (such as when operating from a battery) currents as low as 6mA may be considered without a great loss of accuracy. 6mA represents a practical minimum, since it is about this level where the device's own input current becomes a significant percentage of that flowing in the divider network.

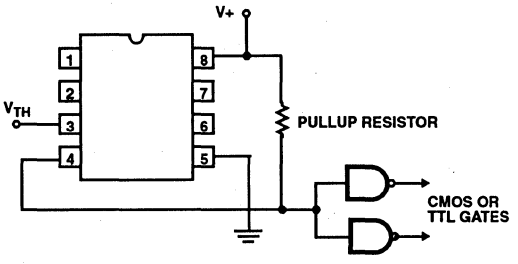


FIGURE 2. OUTPUT LOGIC INTERFACE

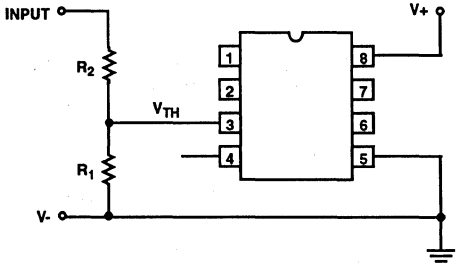


FIGURE 3. INPUT RESISTOR NETWORK CONSIDERATIONS

Case 1. High accuracy required, current in resistor network unimportant Set I = 50µA for V_{TH} = 1.15V $\therefore$ $R_1 \rightarrow$ 20kΩ

Case 2. Good accuracy required, current in resistor network important Set I = 7.5µA for V_{TH} = 1.15V $\therefore$ $R_1 \rightarrow$ 150kΩ

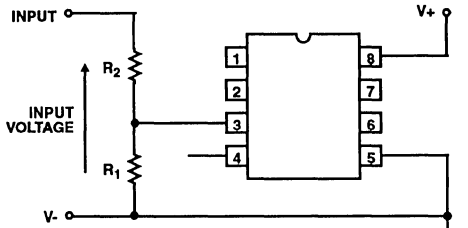


FIGURE 4. RANGE OF INPUT VOLTAGE GREATER THAN +1.15 VOLTS

Setup Procedures For Voltage Level Detection

Case 1. Simple voltage detection no hysteresis

Unless an input voltage of approximately 1.15V is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 5 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity.

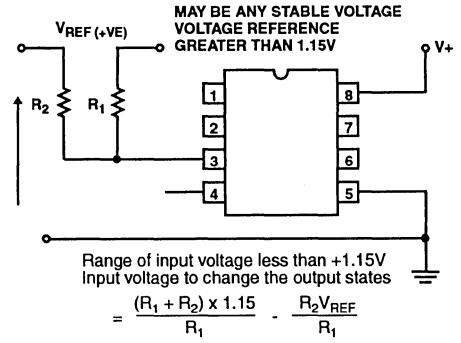


FIGURE 5. INPUT RESISTOR NETWORK SETUP PROCEDURES

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 6.

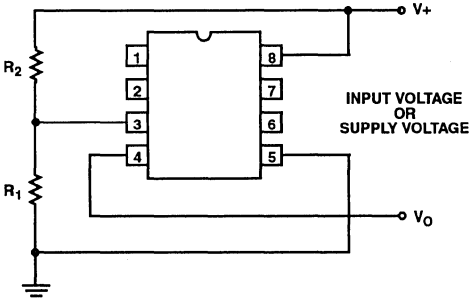


FIGURE 6. COMBINED INPUT AND SUPPLY VOLTAGES

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range where the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications-refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 7.

The circuit (a) of Figure 7 requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output, whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis, circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance between the THRESHOLD and GROUND when the OUTPUT is switched on.

Practical Applications

a) Low Voltage Battery Indicator (Figure 8)

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35µA which will increase to 7mA when the lamp is turned on. R_3 will provide hysteresis if required.

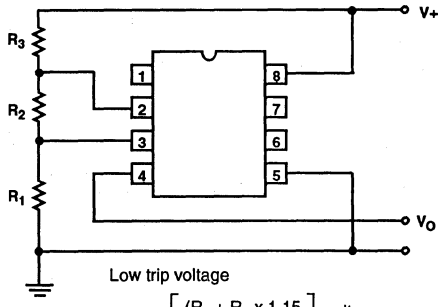
b) Nonvolatile Low Voltage Detector (Figure 9)

In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S_1 the operating point changes to B and will remain at B until the supply voltage drops below VTR1, at which time the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

c) Nonvolatile Power Supply Malfunction Recorder. (Figures 10 and 11)

In many systems a transient or an extended abnormal (or absence of a)) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

It is, therefore, necessary to be able to detect and store the fact that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. Upon power up to the normal

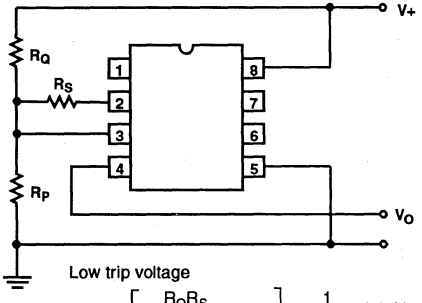


Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2 \times 1.15}{R_1)}\right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15V$$



Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + RP\right] \times \frac{1}{RP} \times 1.15V$$

High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15V$$

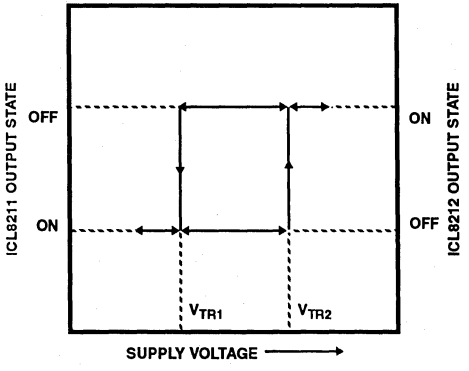
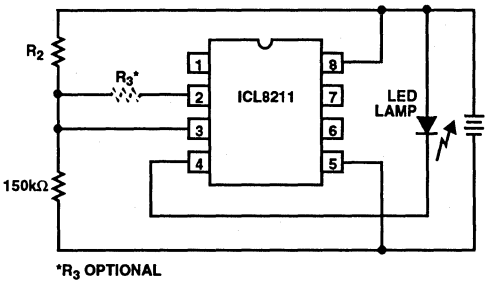
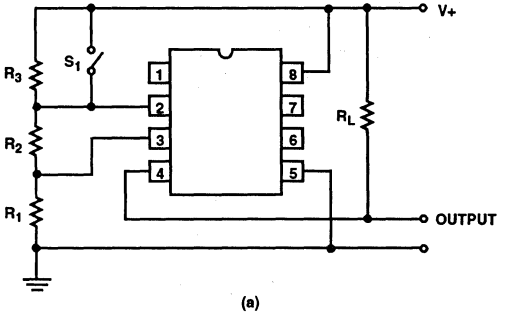


FIGURE 7. TWO ATERNATIVE VOLTAGE DETECTION CIRCUITS EMPLOYING HYSTERESIS TO PROVIDE PAIRS OF WELL DEFINED TRIP VOLTAGES

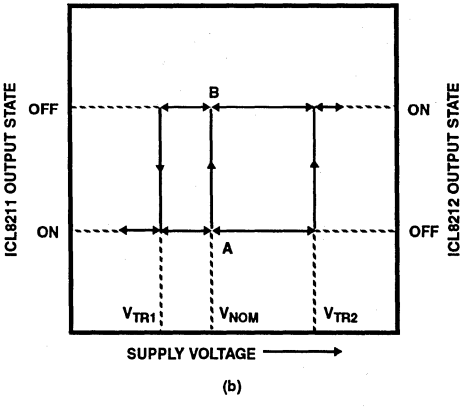


*R3 OPTIONAL

FIGURE 8. LOW VOLTAGE BATTERY INDICATOR



(a)



(b)

FIGURE 9. NON-VOLATILE LOW VOLTAGE INDICATOR

operating voltage this record must have been retained and easily interrogated. This could be important in the case of a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30V without exceeding the maximum ratings of the ICs. The two voltage limits defining the in range supply voltage may be set to any value between 2.0V and 30V.

The ICL8212 is used to detect a voltage, V2, which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range, V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 - the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R3 for values of supply voltage between V_1 and V_2.

d) Constant Current Sources (Figure 12)

The ICL8212 may be used as a constant current source of value of approximately 25µA by connecting the THRESHOLD terminal to GROUND. Similarly the ICL8211 will provide a 130µA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2V to 30V. These constant current sources may be used to provide basing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

e) Programmable Zener Voltage Reference (Figure 13)

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage

$$V_{ZENER} = \frac{(R_1 + R_2)}{R_1} \times 1.15V.$$

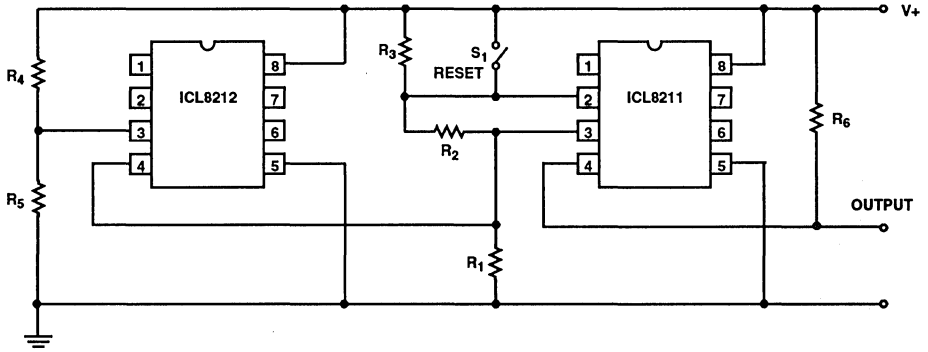


FIGURE 10. NON-VOLATILE POWER SUPPLY MALFUNCTION RECORDER

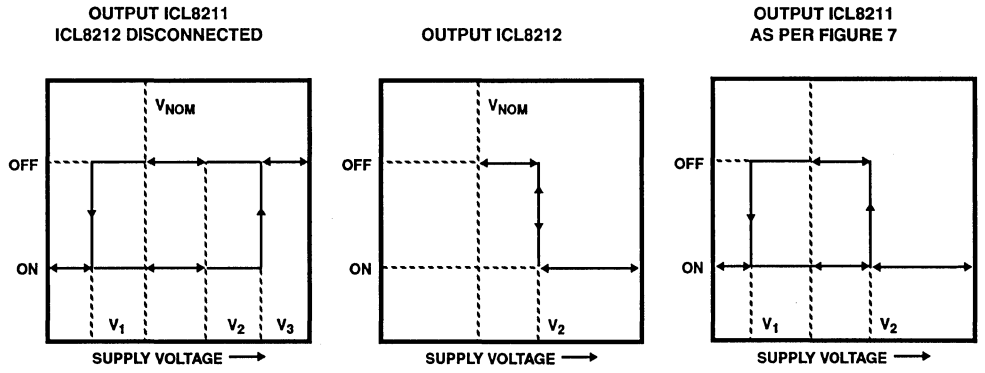


FIGURE 11. OUTPUT STATES OF THE ICL8211 AND ICL8212 AS A FUNCTION OF THE SUPPLY VOLTAGE

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2V to 30V may be programmed and typical impedance values between 300μA and 25μA will range from 4Ω to 7Ω. The knee is sharper and occurs at a significantly lower current than other similar devices available.

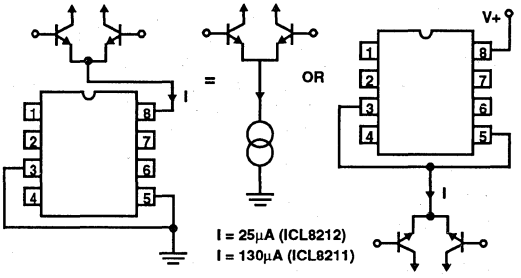


FIGURE 12. CONSTANT CURRENT SOURCE APPLICATIONS

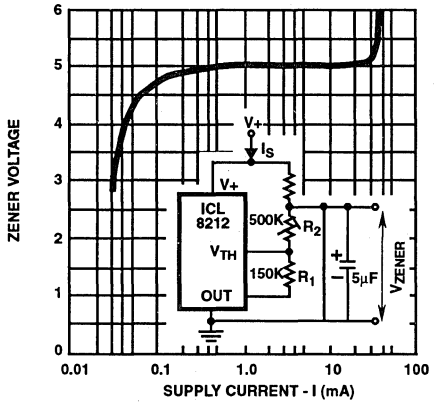
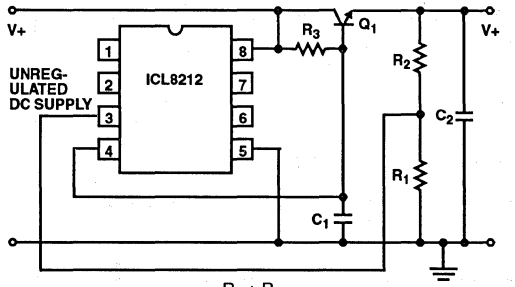


FIGURE 13. PROGRAMMABLE ZENER VOLTAGE REFERENCE

f) Precision Voltage Regulator (Figure 14)

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed, using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.



$$V_{OUT} = \frac{R_2 + R_1}{R_1} \times 1.15V$$

FIGURE 14. PRECISION VOLTAGE REGULATOR

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

g) High Supply Voltage Dump Circuit (Figure 15)

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5mA this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

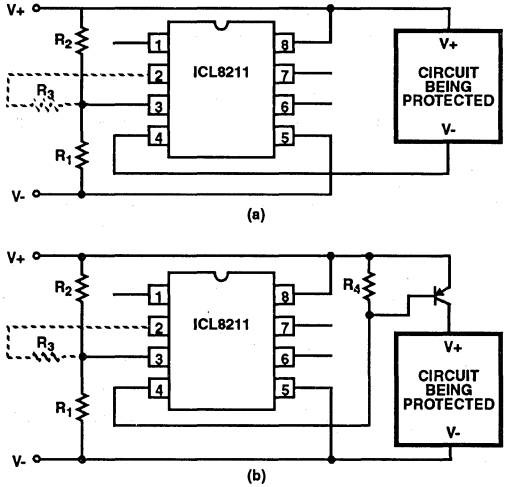


FIGURE 15. HIGH VOLTAGE DUMP CIRCUITS

h) Frequency Limit Detector (Figure 16)

Simple frequency limit detectors providing a GO/NO-GO output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/8212. In the application shown, the first ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3. The time constant of R_7 C_3 is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies, either an ICL8211 or an ICL8212 may be used as the output driver.

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

i) Switch Bounce Filter (Figure 17)

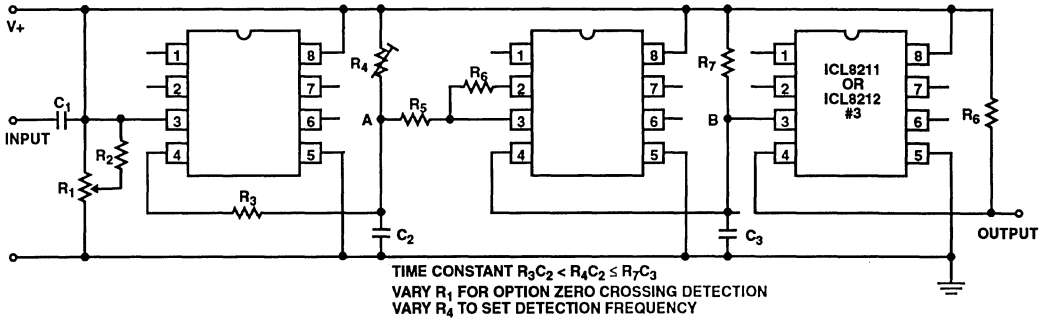
Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches.

SPST switches range from push button and slide types to calculator keyboards. A major problem with the use of switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times. The circuit shown in Figure 17 provides a rapid charge up of C1 to close to the positive supply voltage (V1) on a switch closure and a corresponding slow discharge of C1 on a switch break. By proportioning the time constant of R1 C1 to approximately the manufacturer's bounce time the output as terminal #4 of the ICL8211/8212 will be a single transition of state per desired switch closure

j) Low Voltage Power Disconnect (Figure 18)

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9V causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9V and turn the power supply off to the LM199 heater section below that voltage.

For further applications, see AO27 "Power Supply Design using the ICL8211 and ICL8212."



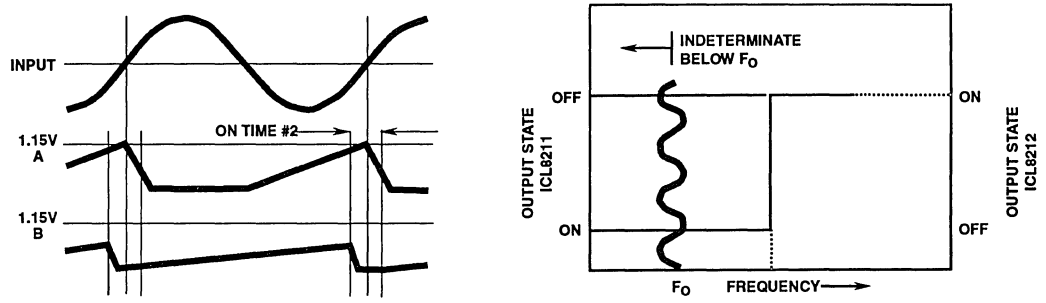


FIGURE 16. FREQUENCY LIMIT DETECTOR

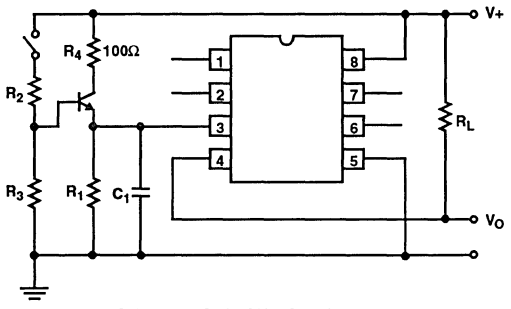


FIGURE 17. SWITCH BOUNCE FILTER

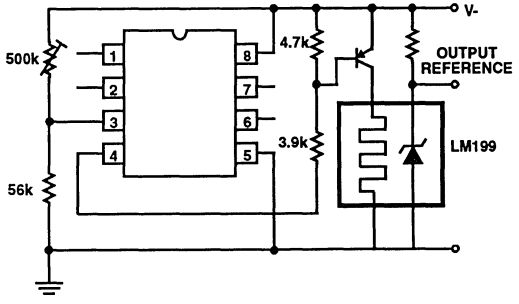


FIGURE 18. LOW VOLTAGE POWER SUPPLY DISCONNECT

INTELLIGENT POWER ICs 8

PROTECTION CIRCUITS

Protection Circuits Selection Guide

PART NUMBER	DESCRIPTION	VCC	TURN-ON THRESHOLD	TEMPERTURE RANGE
SP710	Protection Power Switch	4V to 16V	16V to 18.5V	-40°C to +105°C
SP720	Protection Array	5V to 30V	$+V_{BE}$ Above V_{CC} or $-V_{BE}$ Below GND	-40°C to +125°C

HARRIS SEMICONDUCTOR

SP710

Protected Power Switch With Transient Suppression

May 1992

Features

- ±90V Transient Suppression
- 4V to 16V Operating Voltage
- 0.8A Current Load Capability
- Over-Voltage Shutdown Protected
- Short-Circuit Current Limiting
- Over-Temperature Shutdown Protected Thermal Shutdown at 150°C (Tj)
- -40°C to +105°C Operating Temperature Range

Applications

- Electronic Circuit Breaker
- Transient Suppressor
- Overvoltage Monitor

Description

The SP710 is a Power Integrated Circuit designed to suppress potentially damaging overvoltage transients up to ±90V in amplitude. The device is designed to be operated in a pass-thru mode which allows the current to flow through the IC with minimal voltage drop. The protected load circuit is connected to the output of the SP710. As such, the protected power switch IC is designed to operate as a transient suppressor which is capable of driving resistive, inductive or lamp loads with minimum risk of damage under stress conditions of over voltage or over current. The SP710 is supplied in a 3 lead TO-220AB package.

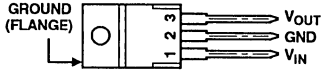
"The SP710 was formerly Harris Developmental No. TA13349"

Ordering Information

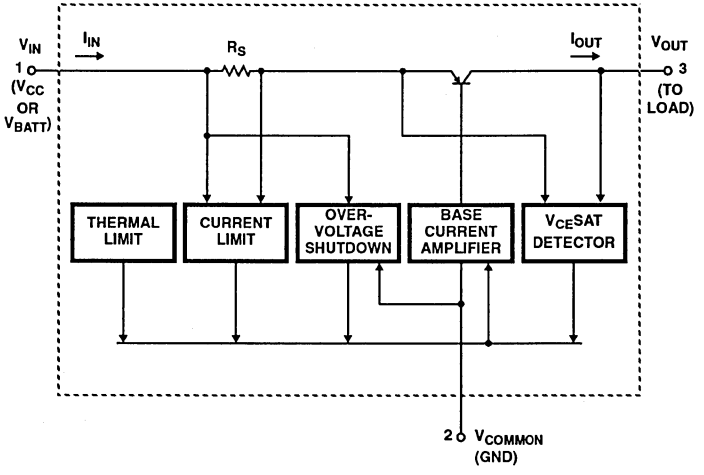
PART NUMBER	TEMPERATURE RANGE	PACKAGE
SP710AS	-40°C to +105°C	TO-220AB

Pinout

TO-220AB
TOP VIEW



Functional Block Diagram



8 PROTECTION CIRCUITS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2789.3

Absolute Maximum Ratings

Input Voltage, V_{IN} 24V
Load Current, I_{OUT} 800mA
Transient Max Voltage, V_{IN} (15ms) ..... ±90V

NOTE: Pd = $(V_{IN} - V_O)$ (I_O) + (V_{IN}) (I_{COMMON})
$T_J = T_A$ + (Pd) (Thermal Resistance)

Power Dissipation and Thermal Ratings

Thermal Resistance, θ_{JC} ..... 4°C/W
Junction Temperature ..... 150°C
Ambient Operating Temperature ..... -40°C to +105°C
Storage Temperature ..... -40°C to +150°C
Lead Temperature (During Solder) ..... 265°C
$^1/_{16} \pm {}^1/_{32}$" (1.59 ± 0.79mm) from case for 10s maximum

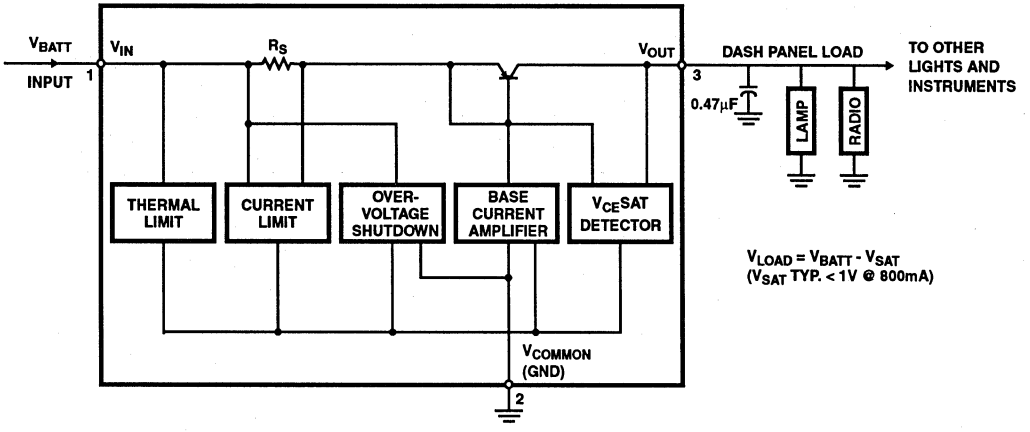
CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(T_A = -40°C to +105°C, V_{IN} = 4V to 16V), Unless Otherwise Specified

PARAMETER	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Input Operating Voltage	V_{IN}		4	-	16	V
Shutdown Voltage	V_{SHSD}		16	-	18.5	V
Shutdown Temperature			-	150	-	°C
Transient Pulse	I_{OUT}	V_{IN} = ±90V for 15ms Pin 3 = 14V, Pin 2 = GND	-20	-	+20	mA
Short Circuit Current			1	-	2	A
V_{SAT} (Input-to-Output)		V_{IN} = 4V, I_{OUT} = 175mA	-	-	0.25	V
		V_{IN} = 9V, I_{OUT} = 500mA	-	-	0.65	V
		V_{IN} = 16V, I_{OUT} = 800mA	-	-	1.05	V
Common Current	I_{COM}	V_{IN} = 16V, I_{OUT} = 100mA	-	-	25	mA
		V_{IN} = 16V, I_{OUT} = 800mA	-	-	50	mA

Typical Application



HARRIS SEMICONDUCTOR

SP720

May 1992

ESD & Overvoltage Protection Array

Features

- ±2A Peak Current Capability
- Single-Ended Voltage Range to +30V
- Differential Voltage Range to +15V
- Designed to Provide Over-Voltage Protection
- Fast Switching - 6ns Risetime
- Low Input Leakages of 1nA Typical
- Low Input Capacitance of 3pF Typical
- An Array of 14 SCR/Diode Pairs
- Proven Interface for ESD
- Operating Temperature Range . . . . . -40°C to +105°C

Applications

- Microprocessor/Logic Input Protection
- Data Bus Protection
- Analog Device Input Protection
- Voltage Clamp

Description

The SP720 is an array of SCR/Diode bipolar structures for ESD and over-voltage protection to sensitive input circuits. The SP720 has 2 protection SCR/Diode device structures per input. A total of 14 available inputs can be used to protect up to 14 external signal or bus lines. Over voltage protection is from the IN (pins 1-7 & 9-15) to V+ or V-. The SCR structures are designed for fast triggering at a threshold of one $+V_{be}$ diode threshold above V+ (Pin 16) or a $-V_{be}$ diode threshold below V- (Pin 8). From an IN input, a clamp to V+ is activated if a transient pulse causes the input to be increased to a voltage level greater than V+; a similar clamp to V- is activated if a negative pulse is applied to the IN input.

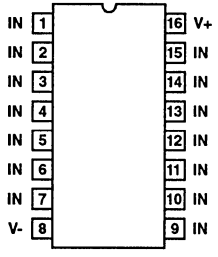
NOTE: The SP720 was formerly Harris Dev. No. TA14987

Ordering Information

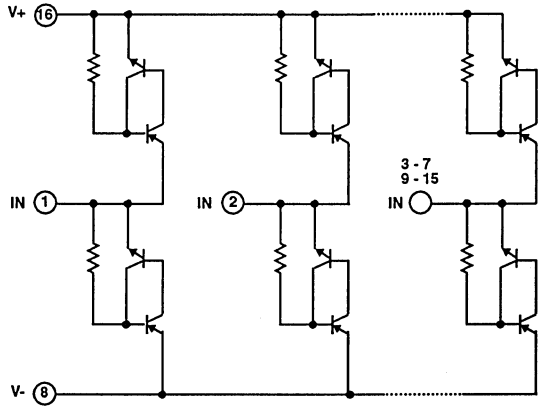
PART NUMBER	TEMPERATURE	PACKAGE
SP720AP	-40°C to +105°C	16 Lead DIP
SP720AB	-40°C to +105°C	16 Lead SOIC

Pinout

16 LEAD DIP & 16 LEAD SOIC PLASTIC PACKAGES
TOP VIEW



Functional Block Diagram



8 PROTECTION CIRCUITS

File Number 2791.2

Absolute Maximum Ratings

Continuous Supply Voltage, (V+) - (V-) ..... +35V
Input Peak Current, I_{IN} ..... ±2A
Transient Ratings - See NOTE 2
Maximum Package Power Dissipation at +125°C:
Plastic DIP Package 500mW
Plastic SOIC Package 270mW

Thermal Resistance, θ_{ja}:
16 Lead DIP Package ..... 90°C/W
16 Lead SOIC Package ..... 170°C/W
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +150°C
Lead Temperature (Soldering 10s) ..... +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A= -40°C to +105°C; V_{IN} = 0.5V_{CC} Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Operating Voltage Range, V_{SUPPLY} = [(V+) - (V-)]	V_{SUPPLY}		4.5		30	V
Forward Voltage Drop: IN to V- IN to V+	 V_{fwdL} V_{fwdH}	I_{IN} = 1A (Peak Pulse)		 2 2		V
Input Leakage Current	I_{IN}		-20	5	20	nA
Quiescent Supply Current	$I_{Quiescent}$			50	200	nA
Input Capacitance	C_{IN}			3		pF
Input Switching Speed	t_{ON}			6		nS

NOTES:

1. In automotive and battery operated systems, the power supply lines should be externally protected for load dump and reverse battery. When the V+ and V- pins are connected to the same supply voltage source as the device or control line under protection, a current limiting resistor should be connected in series between the supply and the SP720 pins to limit reverse battery current to within the rated maximum limits. Bypass capacitors of typically 0.01pF from the V+ and V- pins to ground are recommended.
2. For ESD testing of the SP720 to Mil-Std-3015.7 Human Body Model, the results are better than 6kV protection. For ESD testing to EIAJ IC1Z1 Machine Model, the results are better than 1kV protection. These values were measured by AT&T ESD Lab using the component testing procedures of both standards. Transient and ESD capability is highly dependent on the application. Conditions for an in circuit method of ESD testing in a normal application where the V+ and V- pins have a return path to ground, the ESD capability is typically greater than 15KV from 100pF through 1.5KΩ or 9KV from 200pF through 1.5KΩ with 6ns risetime.

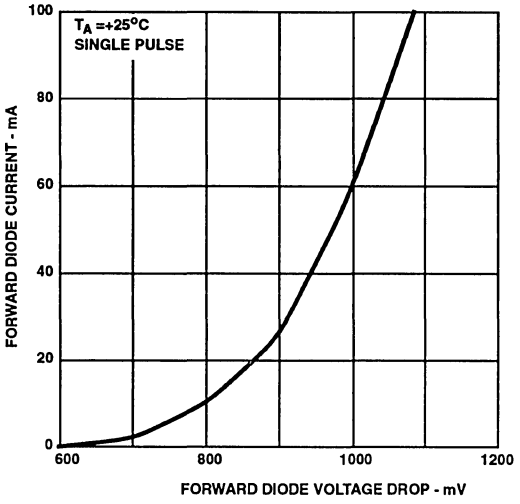


FIGURE 1. LOW CURRENT DIODE/SCR FORWARD VOLTAGE DROP CHARACTERISTIC

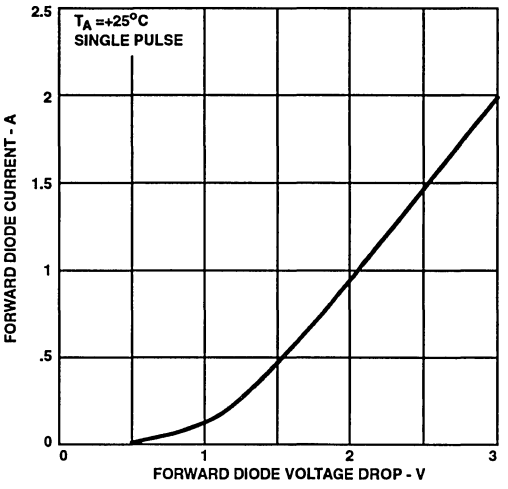


FIGURE 2. HIGH CURRENT DIODE/SCR FORWARD VOLTAGE DROP CHARACTERISTIC

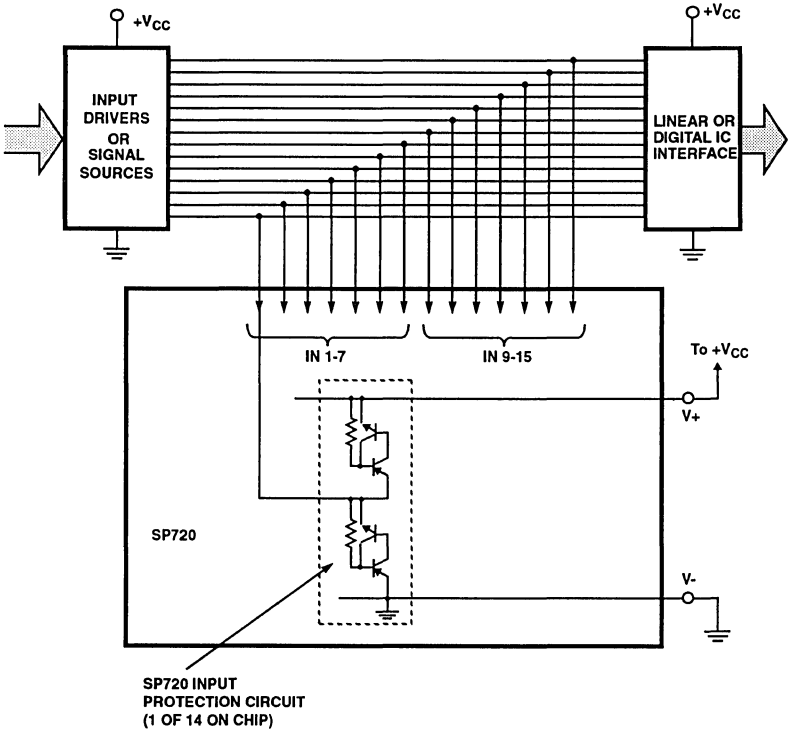


FIGURE 3. TYPICAL APPLICATION OF THE SP720 AS AN INPUT CLAMP FOR OVER-VOLTAGE, GREATER THAN 1 Vbe ABOVE V+ OR LESS THAN -1 Vbe BELOW V-

INTELLIGENT POWER ICs

9

SPECIAL FUNCTIONS

Special Function IC Selection Guide

PART NUMBER	DESCRIPTION	MAX SUPPLY VOLTAGE	MAX SUPPLY CURRENT	SENSOR/INPUT RANGE	I_{OUT} MAX	V_{OUT} MAX
CA3165E CA3165E1	Electronic Switching Circuits for Ignition and Proximity Sensing in General Purpose Control Circuits Using Q-Loaded Inductive Sensor (Multiple Outputs)	24 V	18.4 mA	Q-Loaded Self-Osc. Coil Pickup (~100 mH)	120mA (Sink)	24V
CA3228	Speed Control System for Cruise Control and General Purpose Rate or Motion Control Feedback Applications. Self-Contained Controller with 9 bit D/A Memory. (Multiple Inputs and Outputs)	9 V	30 mA	Inductive Pickup with 3.5V to 15V Range (Ext. RC Filter, 8.2kΩ/0.05μF Interface)	8mA (Sink)	9V
CA3237	IR (Infra-Red) Remote Control Amplifier/Detector for TV and General Purpose Applications. High Sensitivity & Gain (upto 90 dB) with Signal Limiting, Detection and Schmitt Trigger Amplifier/Driver.	14.4 V	10 mA	$100\mu V_{RMS}$ typ, $500\mu V_{RMS}$ max. (From Ext. IR Detector)	(22kΩ Signal Output Source Imped.)	5V CMOS/ TTL Logic Level Output
CA3274	Power Switch with Current Limiting Feedback Control and Current Limiter Sense Flag. Used for Ignition and Current Controlled Switching Applications.	16 V	25 mA	0.4V to 2V Input Switching Thresholds (w/hysteresis)	200mA (Sink/ Source)	16V
HIP9020AP HIP9020AB	Vehicle Speed Sensor (VSS) Buffer IC's with Pre and Post Scaler Dividers for processing Sinusoidal Waveforms from Magnetic Pickup Sensors with divide by 1,6-11 Prescaling & 1, 2 Post Scaling Options. (Multiple Outputs)	Shunt Regulator ~5.6V with Series Forward Diode/Resistor to Power Supply (V_{BATT}); or Use Ext. 5 ± 0.3 V Power Supply (Max. I_{CC} = 12 mA)		±(0.25 to 100)V with 40 kΩ Ext. Series Current Limiting Resistor to Input	15mA (Sink)	24V

HARRIS SEMICONDUCTOR

CA3165

May 1992

Electronic Switching Circuit

Features

- Switching Initiated by Damping of Internal Oscillator
- Proximity Sensing of Rotational Motion
- Repeatable Timing of Switching States
- Five Outputs - Two Complementary Pairs and One Non-Inverting Output CA3165E1
- Two Outputs - One Complementary Pair CA3165E

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3165E	-40°C to +85°C	8 Lead Plastic DIP
CA3165E1	-40°C to +85°C	14 Lead Plastic DIP

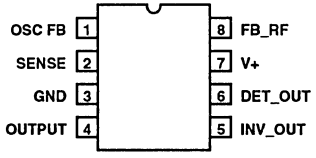
Description

The CA3165 is a single chip electronic switching circuit intended primarily for ignition applications. It includes an oscillator that is amplitude-modulated by the rotor teeth of a distributor, a detector that develops the positive going modulation envelope, a Schmitt trigger that eliminates switching uncertainties. Both types include two complementary high current switched outputs for driving power transistors requiring up to 120 milliamperes. The CA3165E also includes two complementary low current outputs that incorporate internal current limiting and a non-inverting output amplifier with uncommitted input capable of switching 27 milliamperes.

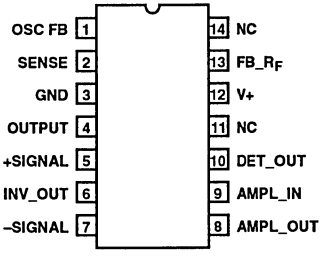
The CA3165 is supplied in the 8 lead dual-in-line plastic package (Mini-DIP, E suffix) and in the 14 lead dual-in-line plastic package (E1 suffix). Refer to ICAN-6352 for additional information.

Pinouts

8 LEAD PLASTIC DIP
TOP VIEW



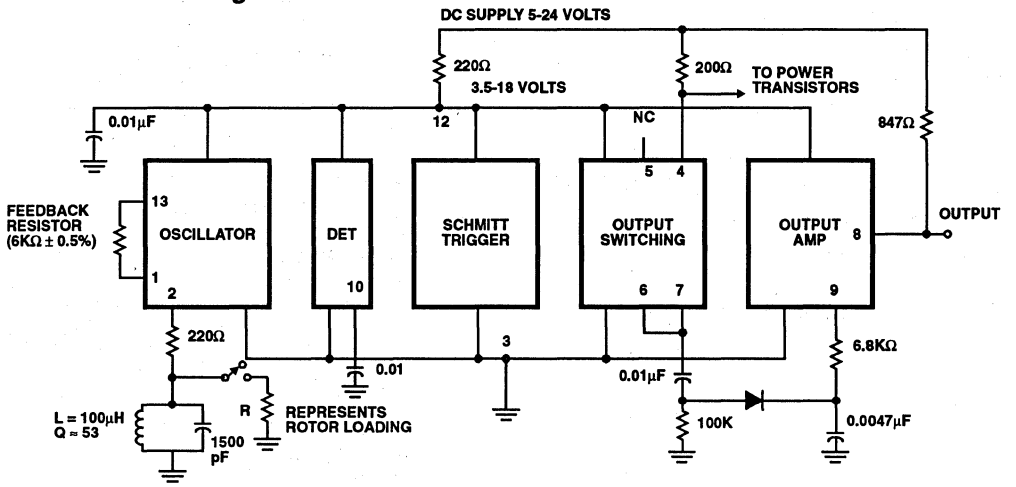
14 LEAD PLASTIC DIP
TOP VIEW



9 SPECIAL FUNCTIONS

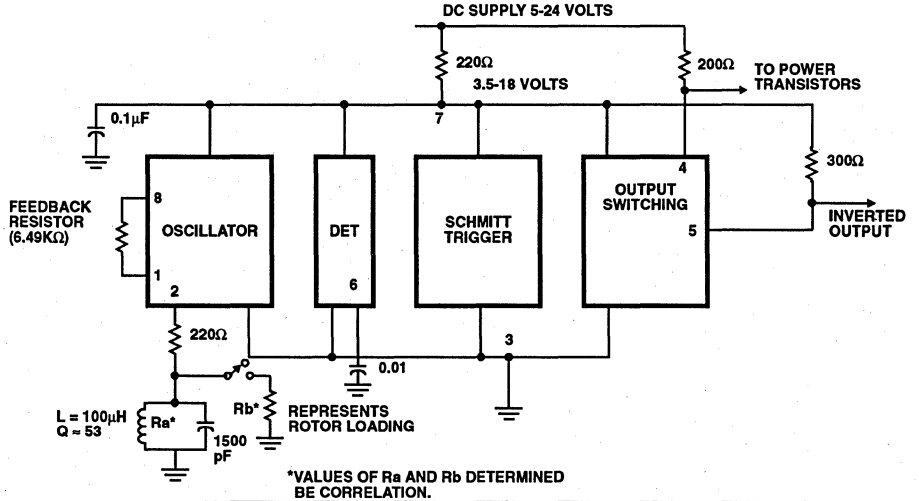
File Number **1278.1**

Functional Block Diagram



OSCILLATOR CONDITION	TERMINAL 10	TERMINAL 4	TERMINAL 5	TERMINAL 6	TERMINAL 7	TERMINAL 8
Unloaded	Low	High	High	Low	Low	Low
Loaded	High	Low	Low	High	High	High

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM FOR CA3165E1



*VALUES OF Ra AND Rb DETERMINED BE CORRELATION.

OSCILLATOR CONDITION	TERMINAL 4	TERMINAL 5	TERMINAL 6
Unloaded	High	High	Low
Loaded	Low	Low	High

FIGURE 2. FUNCTIONAL BLOCK DIAGRAM FOR CA3165E

Absolute Maximum Ratings

	CA3165E1	CA3165E	
DC Voltage (With reference to terminal 3):			
Terminal	4, 6, 8	4, 5	24V
Terminal	5, 7, 12	7	18V
Terminal	9	-	1.5V
Current (At terminals indicated):			
Terminal	4, 6	4, 5	120mA
Terminal	5, 7	-	-0.1 to 0.1mA
Terminal	8	-	30mA
Device Dissipation:			
Up to T_A = 55°C			600mW
Above T_A = 55°C (derate linearly at)			6.67 mW/°C
Ambient Temperature Range:			
Operating			-40°C to +85°C
Storage			-65°C to +150°C
Lead Temperature (During Soldering):			
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10 seconds max			265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

At T_A = +25°C, V+ = 13V, Measured in the circuit of Figure 5 (CA3165E1) or Figure 6 (CA3165E)

PARAMETERS	SYMBOL	TEST CONDITIONS	CA3165E1			CA3165E			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Current at Term.*	Δ	Dwell Spark	- -	18.4 17.5	- -	- -	18.4 17.5	- -	mA
Output Voltage at Term. 4	V_4	Dwell Spark	12.8 -	- -	- 0.5	12.8 -	- -	- 0.5	V
Output Volatge at Term. 7	V_7	Dwell	-	-	1	-	-	-	V
Output Voltage at Term. 8	V_8	Dwell Portion of Spark	- 1.2	- -	0.9 -	-	-	-	V
Oscillator Voltage at Term. 2	V_2	Dwell Spark	- -	4.4 0.6	- -	- -	4.4 0.6	- -	Vp-p

* Δ

CA3165E at Term. 7 I7

CA3165E1 at Term. 12 I12

Schematic Diagrams

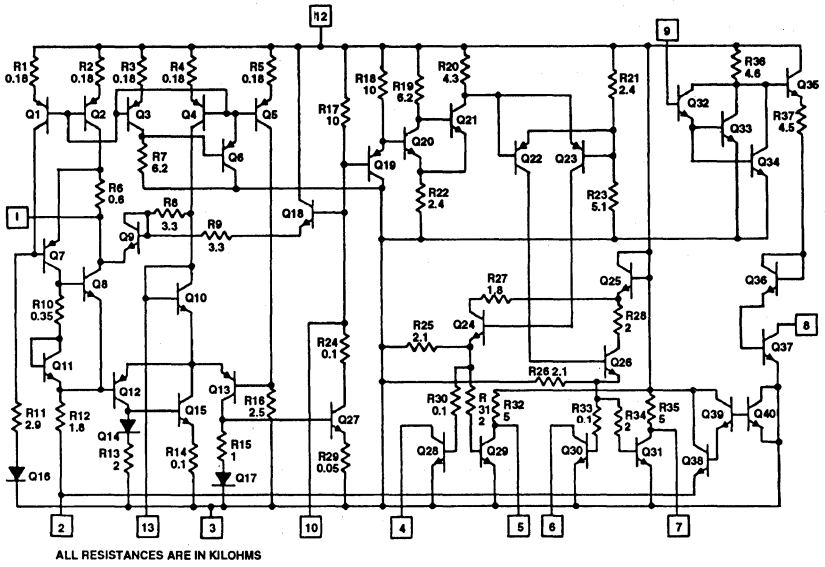


FIGURE 3. SCHEMATIC DIAGRAM FOR CA3165E1

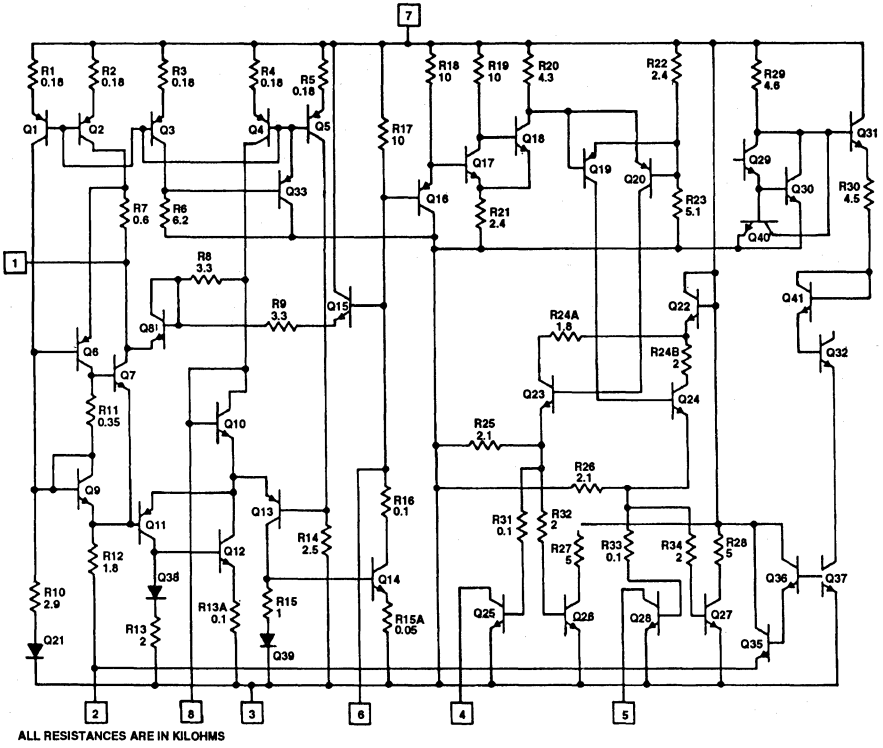


FIGURE 4. SCHEMATIC DIAGRAM FOR CA3165E

Application Information Figure 5 and Figure 6 show the application of the CA3165 in a typical ignition system.

TERMINAL DESCRIPTIONS		
TERMINAL		FUNCTION
CA3165E1	CA3165E	
1	1	Oscillator Feedback Resistor, R_f
2	2	220Ω Protective Resistor To Tank Circuit
3	3	Ground
4	4	Direct Output - R_7 load resistor 200Ω ± 5%, and R_8 to power Darlington 15Ω ± 10%
5	-	Direct Output - Low Current - Not Connected
6	5	Inverted High Current Output
7	-	Inverted Low Current Output Through C_1 (0.01μF) to D_3 and R_3 (100kΩ)
8	-	Output Amplifier Output - Through R_6 and R_5 (27Ω and 820Ω to Supply)
9	-	Output Amplifier Input - through R_4 (6800Ω) to D_3 and C_5 (0.0047μF)
10	6	Detector Output - C_2 to Ground (0.0022μF)
11	-	No Connection
12	7	Circuit Supply Voltage Through R_1 (220Ω Protective Resistor) to Automotive Supply
13	8	Oscillator Feedback Resistor R_f to Terminal 1
14	-	No Connection

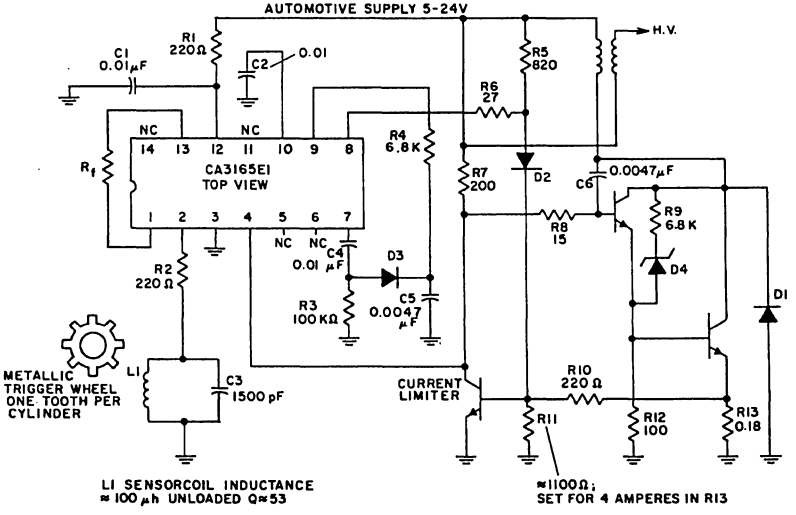


FIGURE 5. TYPICAL IGNITION SYSTEMS USING THE CA3165E1

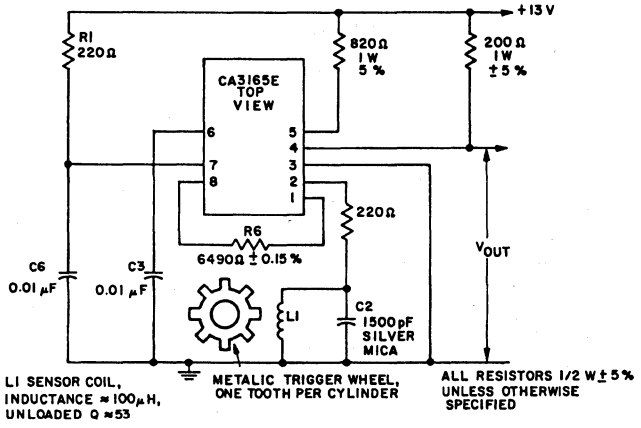


FIGURE 6. TYPICAL IGNITION SYSTEM USING THE CA3165E

Application Information

Figure 5 and Figure 6 show the application of the CA3165 in a typical ignition system. The oscillator on the chip operates at about 400kHz as determined by the tuned circuit L1, C3. The amplitude of the oscillation is detected on the chip and applied to a Schmitt trigger which sets the terminal voltage as shown in the chart in Figure 1 and Figure 2 for the unloaded condition of the oscillator. As a metallic tooth in the rotor passes the coil L1 eddy-current losses occur which reduce the Q of the resonant circuit and decrease the amplitude of the oscillations to a level below that of a reference in the detector circuit. The output terminals are then switched to states as shown in the chart in Figure 1 and Figure 2 for the loaded condition of the oscillator. The oscillation is maintained at this lower amplitude by switching in additional feedback in the oscillator circuit. The fact that the oscillator continues to operate at some minimum level during this dwell period eliminates timing variations which would occur if the oscillator had to be restarted by random noise.

Spark occurs as terminal 4 is switched from high to low. The output amplifier clamps terminal 4 low through the regulator during the duration of the spark.

The Dwell period represents the time that terminal 10 (CA3165E1) or terminal 6 (CA3165E) is high, terminal 4 is low, and the coil is charged.

The value of the oscillator feedback, resistor, R_f, is selected to set the dwell period. With a sintered-iron 8 f-tooth rotor, a typical value of Rf is 6500 ohms for 28.5 degrees of dwell out of a 45 degree cycle. For a star-type rotor and a particular coil in a typical distributor, the feedback resistor would be larger (typically 8800 ohms) depending on clearances, coil geometry and tooth shape.

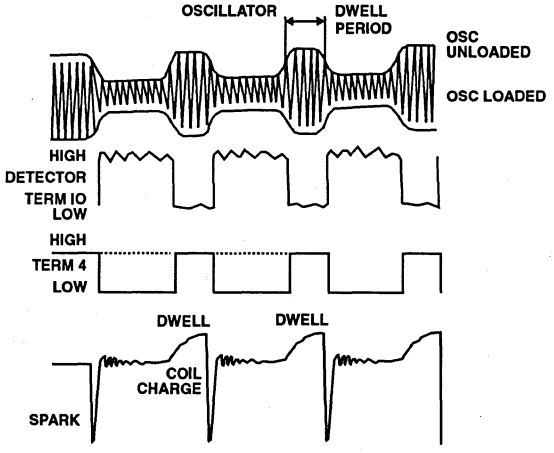


FIGURE 7. TIMING SEQUENCE

HARRIS SEMICONDUCTOR

CA3228

May 1992

Speed Control System with Memory

Features

- Low Power Dissipation
- I^2L Control Logic
- Power-On Reset
- On-Chip Oscillator for System Time Reference
- Single Input Line for Operator Commands
- Amplitude Encoded Control Signals
- Transient Compensated Input Commands
- Controlled Acceleration Mode
- Internal Redundant Brake and Low-Speed Disable
- Braking Disable

Applications

- Automotive Speed Control
- Residential and Industrial Heating and Cooling Controls
- Industrial AC and DC Motor Speed Control
- Applications Requiring Acceleration and Deceleration Control

Description

The CA3228* is a monolithic integrated circuit designed as an automotive speed-control system.

The system monitors vehicle speed and compares it to a stored reference speed. Any deviation in vehicle speed causes a servo mechanism to open or close the engine throttle as required to eliminate the speed error. The reference speed, set by the driver, is stored in a 9-bit counter.

The reference speed can be altered by the ACCEL and COAST driver commands. The ACCEL command causes the vehicle to accelerate at a controlled rate; the COAST command disables the servo, thereby forcing the vehicle to slowdown. Application of the brake disables the servo and places the system in the standby mode while the RESUME command returns the vehicle to the last stored speed.

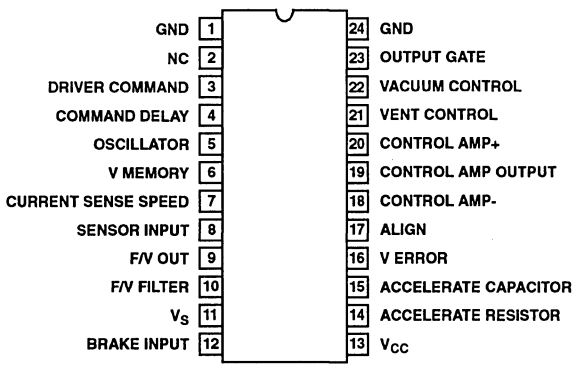
Vehicle speed and driver commands are inputs to the integrated circuit via external sensors. Actuators are needed to convert the output signals into the mechanical action necessary to control vehicle speed.

The CA3228 is supplied in a 24-lead dual-in-line plastic package (E suffix). Refer to ICAN-7326 for application information.

* Formerly RCA Developmental Type No. TA10768.

Pinout

24 LEAD DIP
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3228E	-40°C to +85°C	24 Lead Plastic DIP

9 SPECIAL FUNCTIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **1436.1**

Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... +9.0V
Supply Current, I_{CC} 30mA
Driver Command Input (I_{CMD}), Pin 3 ..... 2mA
Brake Input (I_{BRAKE}), Pin 12 ..... 2mA
Storage Temperature Range ..... -65°C to +150°C
Junction Temperature ..... +175°C

Thermal Information

Power Dissipation Per Package
For T_A = -40°C to +70°C 695mW
For T_A Above +70°C ..... Derate Linearly at 8.7mW/°C
Lead Temperature (Soldering 10s) ..... +265°C
Operating Temperature Range ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Typical Switching Characteristics

Driver Command Input Hold Times (Based on 0.68µF on Pin 4):
ACCEL 50ms
COAST 50ms
RESUME 330ms
ON 50ms
OFF 50ms
Internal Oscillator Frequency, F_{OSC} 10kHz
(Based on 0.001µF at Pin 5)

System Performance F_{OSC} = 50kHz, f_S/Speed Ratio = 2.22Hz/mph

Speed Sensor Input Frequency Range, f_s at Pin 8...62Hz to 222Hz
Speed Resolution ..... 0.45 mph
Minimum Operating Speed ..... 25 mph
Maximum Stored Speed ..... 100 mph
Redundant Brake Speed ..... 11 mph

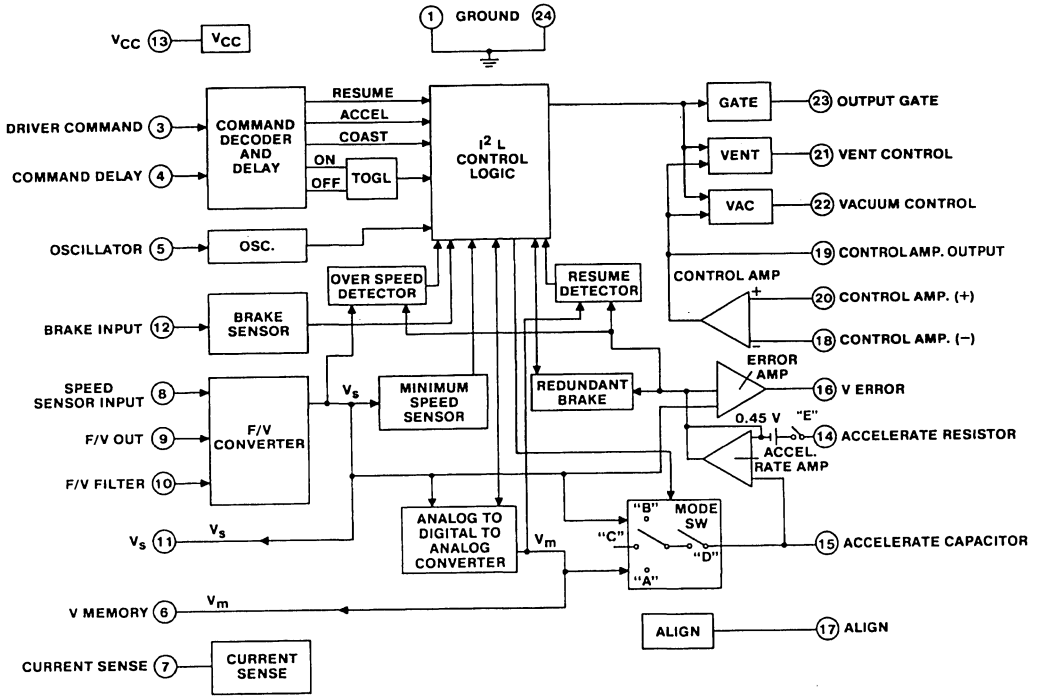
DC Electrical Specifications T_A = +25°C, V_{CC} = 8.20V, Unless Otherwise Specified (Refer to Figures 2 and 3)

PARAMETERS	SYMBOLS	TEST PIN	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Operating Voltage	V_{CC}	13		7.40	9.00	V
Speed Sensor Input Voltage Amplitude		T.P.B.	62Hz ≤ f_S ≤ 222Hz	3.50	15.0	Vpp
V_{CC} Supply Current	I_{CC}	13		7.50	30.0	mA
Current Sense Voltage	V_7	7	43KΩ to Ground	4.85	5.95	V
Align Voltage	V_{17}	17	41KΩ to Ground	4.00	4.20	V
Command Idle Voltage	V_{3IDLE}	3	S1, S2, S3, S4, S5 Open	7.6	7.9	V
RESUME Command Voltage	V_{3RES}	3	S2 Closed	5.95	6.56	V
ACCEL Command Voltage	V_{3ACCEL}	3	S3 Closed	3.95	4.91	V
COAST Command Voltage	V_{3COAST}	3	S4 Closed	1.22	2.23	V
OFF Voltage	V_{3OFF}	3	S5 Closed	0	0.77	V
ON Voltage	V_{3ON}	T.P.A.	S1 Closed	9.2	28	V
Brake Input Voltage	V_{BRAKE}	12	S6 Closed	5.4	28	V
OUTPUT VOTLAGE						
Gate	V_{OL}	23	4.7KΩ to V_{CC}	-	300	mV
	V_{OH}			8	-	V
VAC	V_{OL}	22	1.2KΩ to V_{CC}	-	400	mV
	V_{OH}			8	-	V
VENT	V_{OL}	21	1.2KΩ to V_{CC}	-	400	mV
	V_{OH}			8	-	V

DC Electrical Specifications T_A = +25°C, V_{CC} = 8.20V, Unless Otherwise Specified (Refer to Figures 2 and 3)

PARAMETERS	SYMBOLS	TEST PIN	TEST CONDITIONS	LIMITS		UNITS
				MIN	MAX	
Memory Set Error	$V_6 - V_{10}$	6, 10		-77	67	mV
Deadband Range (VAC and VENT Outputs Off)	V_{DB}	21, 22	Sweep Pin 19, Voltage at 1V/sec	0.96	1.43	V
Control Amplifier Gain	A_{CNTL}	16, 19	A_{CNTL} = V19/V16	74	-	Ratio
D/A Voltage Range	V_M	6	Set Mode	6	7.50	V

Functional Block Diagram



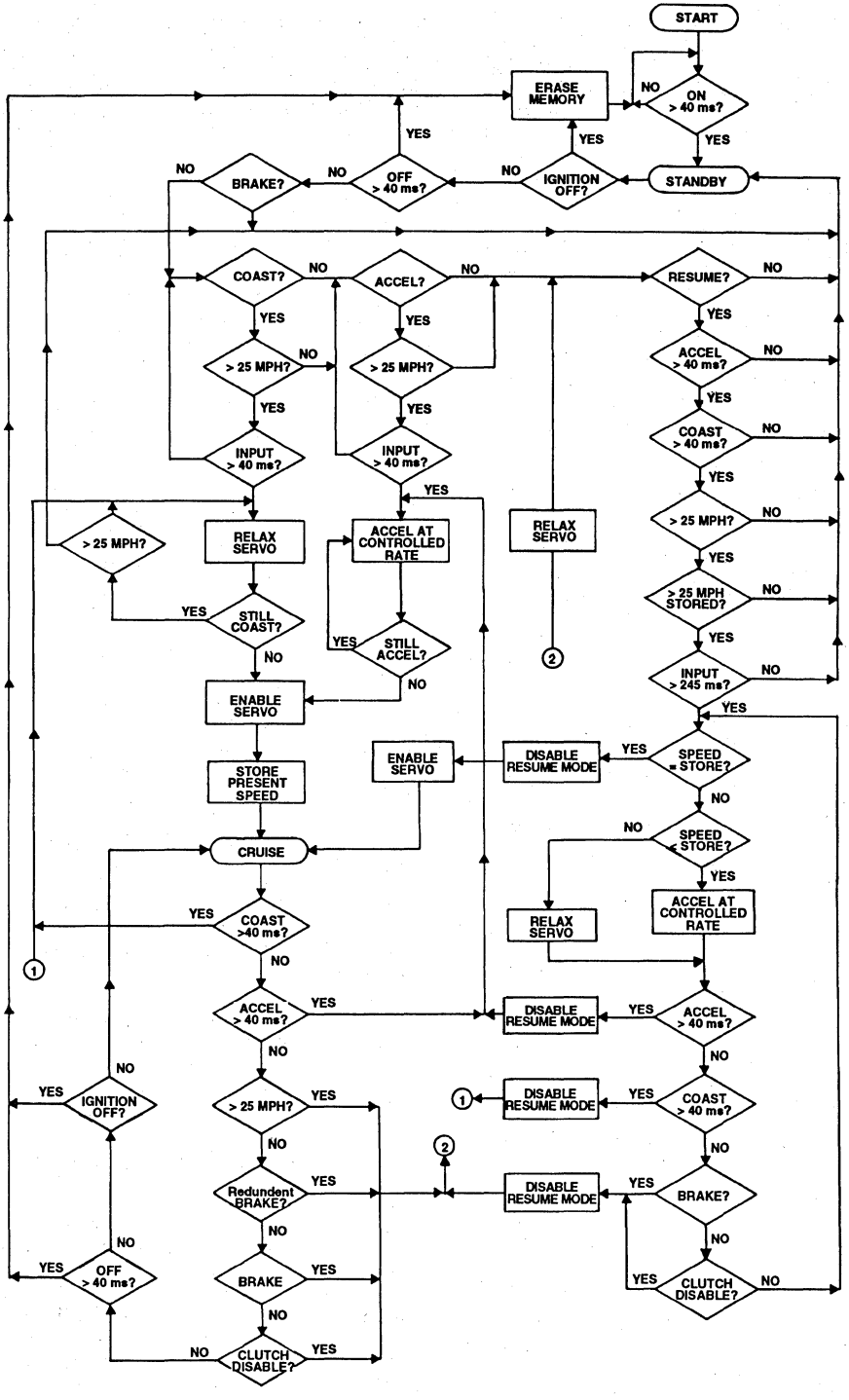
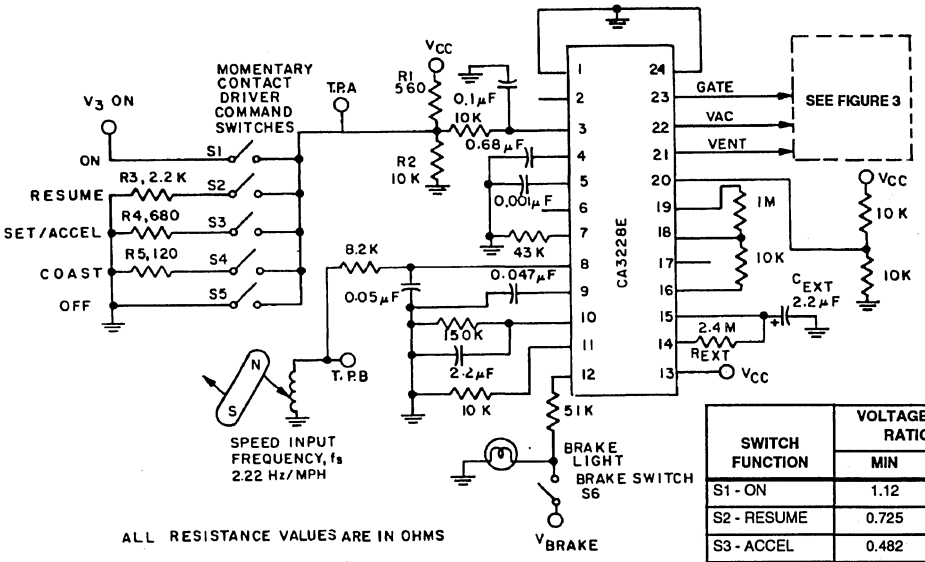


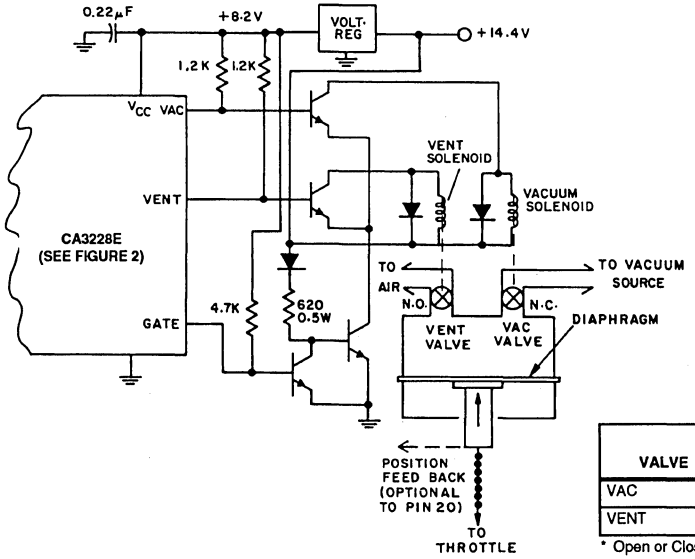
FIGURE 1. SPEED CONTROL FLOW CHART



SWITCH FUNCTION	VOLTAGE AT TERM. 3 RATIO TO V_{CC}	
	MIN	MAX
S1 - ON	1.12	-
S2 - RESUME	0.725	0.8
S3 - ACCEL	0.482	0.599
S4 - COAST	0.148	0.272
S5 - OFF	0	0.094
IDLE*	0.93	0.96

* All Switches Open

FIGURE 2. TYPICAL AUTOMOTIVE SPEED CONTROL APPLICATION



VALVE	SYSTEM MODE		
	ACCEL	CRUISE	COAST
VAC	Open	NC*	NC
VENT	Close	Close*	NC

* Open or Closed as Required to Maintain Set Speed Error

	ACCEL	CRUISE	COAST	BRAKE	REDUNDANT BRAKE	HI-SPEED DROPOUT	LO-SPEED DROPOUT
VAC (Pin 22)	H	L	L	L	L	L	L
VENT (Pin 21)	H	H	L	L	L	L	L
GATE (pin 23)	L	L	L	H	H	H	H

FIGURE 3. SOLENOID DRIVERS AND SERVO VACUUM CONTROL MECHANISM TYPICAL APPLICATION

Device Description and Operation

The functional block diagram and Figures 1, 2 show the speed- control flow chart, and a typical automotive speed-control application, respectively.

Command Decoder and Delay Logics (Pins 3,4)

Driver commands are input to pin 3 through the Driver Command Line. These signals are encoded on a single line as voltage levels selected by switches which adjust a resistor divider network.

The voltage level established is compared to a reference level which decodes the command. A command level greater than V_{CC} + 0.8V turns the system On, enabling dynamic control. Once the system is enabled, a voltage level of $0.88V_{CC}$, $0.66V_{CC}$, and $0.38V_{CC}$ decodes the RESUME, ACCEL, and COAST command, respectively. A driver command of $0.12V_{CC}$ or less turns the system Off.

The Driver Command Delay established by the current sources and a capacitor at pin 4 assures that ON, OFF, ACCEL, and COAST commands are considered valid only if longer than 50ms. The time for RESUME is 330ms.

Control Logic

The Control Logic accepts signals from the command decoder and other sensors. It causes the memory to be updated when operating in ACCEL and COAST modes. It will put the system in Standby mode if brakes are applied, if the speed error exceeds 11mph, or if the vehicle speed drops below the minimum Speed Lockout (25mph). It will return the vehicle to the previous set memory speed when a RESUME command is given.

Frequency to Voltage Converter (Pins 8-11)

The speed sensor input f_S at pin 8 is an AC signal whose frequency is directly proportional to the vehicle speed at approximately 2.22Hz/mph The current sources, capacitor and comparators at pin 9 cause equal rise and fall times to occur at pin 9 on the positive- and negative-going slopes of the sensor input. Pulse currents of time duration equal to the rise and fall times are used to charge the parallel resistor capacitor combination at pin 10 to give a voltage (V_S) at pin 10 proportional to frequency at approximately 27mV/Hz. The f_S frequency range may be altered by changing the values of the filter capacitors at pins 8 and 9. However, the maximum-to-minimum frequency ratio will remain fixed.

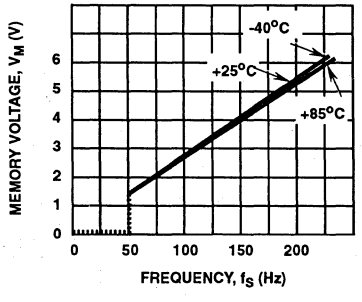


FIGURE 4. TYPICAL D/A MEMORY VOLTAGE, V_M vs. FREQUENCY

Memory Voltage, V_M (Pin 6)

Upon release of the ACCEL or COAST switches the voltage, representing vehicle speed V_S determined by the output from the frequency-to-voltage converter, is stored as a binary number in a 9 bit counter. A memory update comparator allows clocking of the counter until memory voltage V_M equals V_S. The output of the counter controls a ladder network which provides memory voltage V_M at pin 6.

Analog Accelerate and Resume Generator (Pins 14,15)

Numerous functions are combined in what is called the Analog Accelerate and Resume Generator. The circuit switches the signal output at pin 15 depending on the mode of operation. In the Accelerate and Resume mode the capacitor at pin 15 is charged at a fixed rate [450mV/(R_{EXT}) (C_{EXT})]. In the Cruise mode pin 15 follows the memory voltage (V_M) and in the On, Off, Brake, Redundant Brake, Minimum Speed Lockout, and Coast modes, pin 15 follows the voltage representing vehicle speed (V_S).

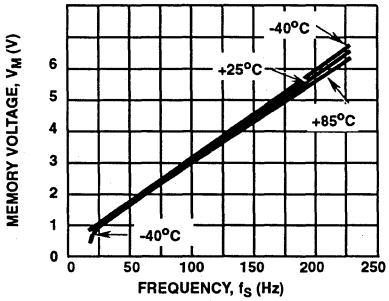


FIGURE 5. TYPICAL CHARACTERISTIC F/V CONVERTER OUTPUT, V_S vs. FREQUENCY

Error Amplifier (Pin 16)

In the Cruise mode the Error Amplifier determines the difference between the set memory speed (V_M) and the actual speed (V_S). This error signal is fed to the control amplifier where it defines whether VAC or VENT is required. The error signal represents deviation in vehicle speed from the memory or set speed condition. The Error signal is also used to control the Redundant Brake feature.

Redundant Brake Comparator

When the error output drops below approximately $0.42V_{CC}$, the Redundant Brake output is activated. Redundant Brake causes the chip to go into the Standby mode.

Control Amplifier (Pins 18, 20)

The Control Amplifier is an op amp using external components to set the gain. Inputs to the Control Amplifier are from the Error Amplifier output, servo position sensor and align output. The output of the Control Amplifier controls the VAC and VENT outputs.

VAC, VENT and Gate-Driver Outputs (Pins 21, 22, 23)

The VAC, VENT and Gate Outputs are open collector devices used to control the throttle position. For the system to be able to supply vacuum, the gate output must be low. If

the output from the Control Amplifier exceeds $0.573V_{CC}$, vacuum is supplied to the servo unit. If the output of the Control Amplifier is between $0.573V_{CC}$ and $0.427V_{CC}$ the vacuum is held in the servo unit and vehicle speed is maintained. If the output from the Control Amplifier drops below $0.427V_{CC}$ or if the gate output is high, the servo unit vacuum is vented.

Overspeed Detector Comparator

The Overspeed Detector circuit is used when the following sequence of events occur: A speed is set in memory, the vehicle is manually accelerated (foot pedal) to a higher speed and then the ACCEL switch is activated.

During vehicle acceleration V_S voltage is greater than the V_M voltage into the memory update comparator. When the ACCEL command is given, the capacitor at pin 15 rapidly charges to within 60mV of V_S before switching the comparator output low and starting the fixed acceleration rate from the present vehicle speed. The 60mV of offset is required to insure that the output of the overspeed detector is low under normal operating conditions. Hysteresis is also designed into the comparator to eliminate noise problems which may prevent the chip from going into the Acceleration mode.

End of Resume Comparator

The Resume Comparator is used when the following sequence of events occurs: A speed is set in memory, the brake applied, causing the vehicle to go to a lower speed, and the RESUME switch is activated.

Activation of the RESUME switch causes a fixed acceleration rate from the lower speed until the capacitor voltage at pin 15 is equal to the V_M voltage. A filter circuit contained in the output of the resume comparator insures that noise doesn't reset the comparator until V_{PIN} actually equals V_M.

Align Voltage Source (Pin 17)

The Align Voltage Source is a X1 buffer with an output of $0.5V_{CC}$.

Brake Input Comparator (Pin 12)

When the Brake Input exceeds $0.55V_{CC}$, the chip will go into the Standby mode from Cruise.

Minimum Speed Lockout

Assures that the system remains in a Standby mode if vehicle speed V_S is below $0.183V_{CC}$. It causes the system to revert to the Standby mode if V_S drops below $0.183V_{CC}$ in the Cruise mode.

Digital Filter for Redundant Brake and Minimum Speed Lockout

A 4 bit shift register with an all '1's output decode is used to filter transients and electromagnetic interference. The filter prevents false signals from putting the system into Standby from Cruise.

Ramp Oscillator (Pin 5)

The Ramp Oscillator at pin 5 nominally varies between amplitudes of 4.1V and 6.1V. The discharge rate is approximately 4X the charge rate. With a capacitor of 0.001µF on pin 5, the nominal oscillator frequency is 50kHz.

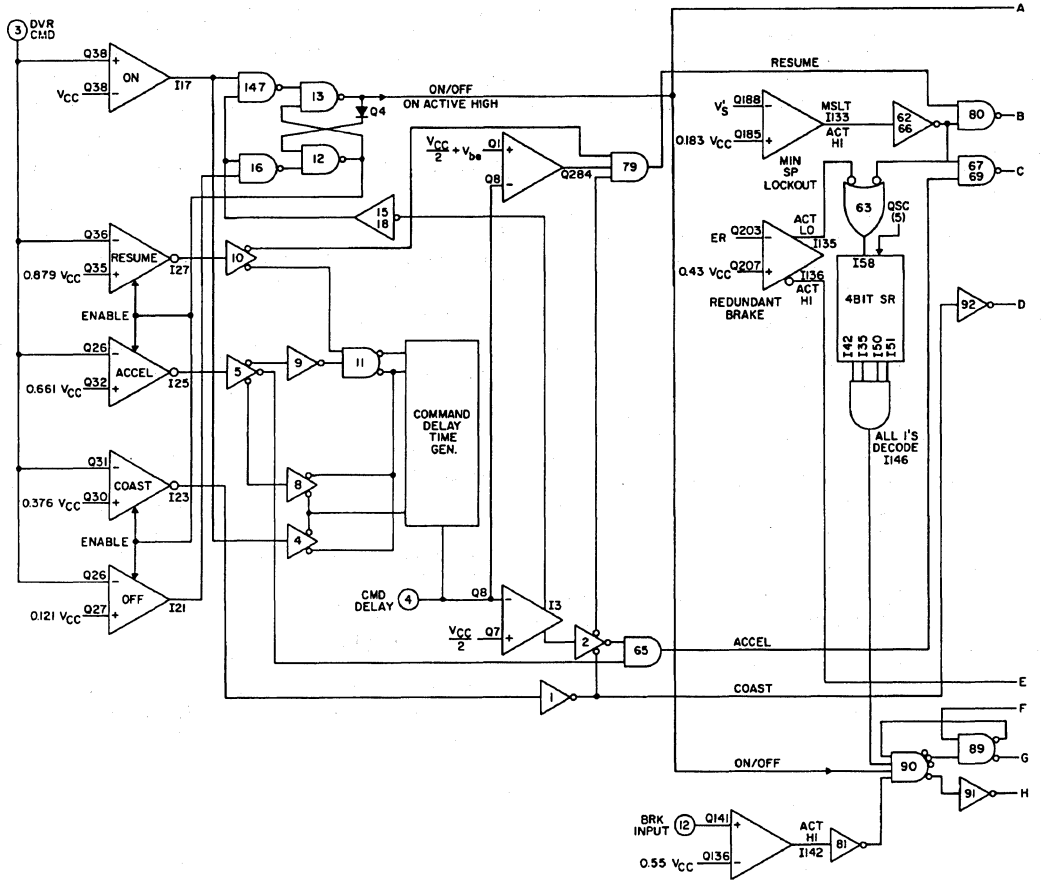


FIGURE 6. FUNCTIONAL BLOCK DIAGRAM FOR SPEED CONTROL (Continued on Next Page)

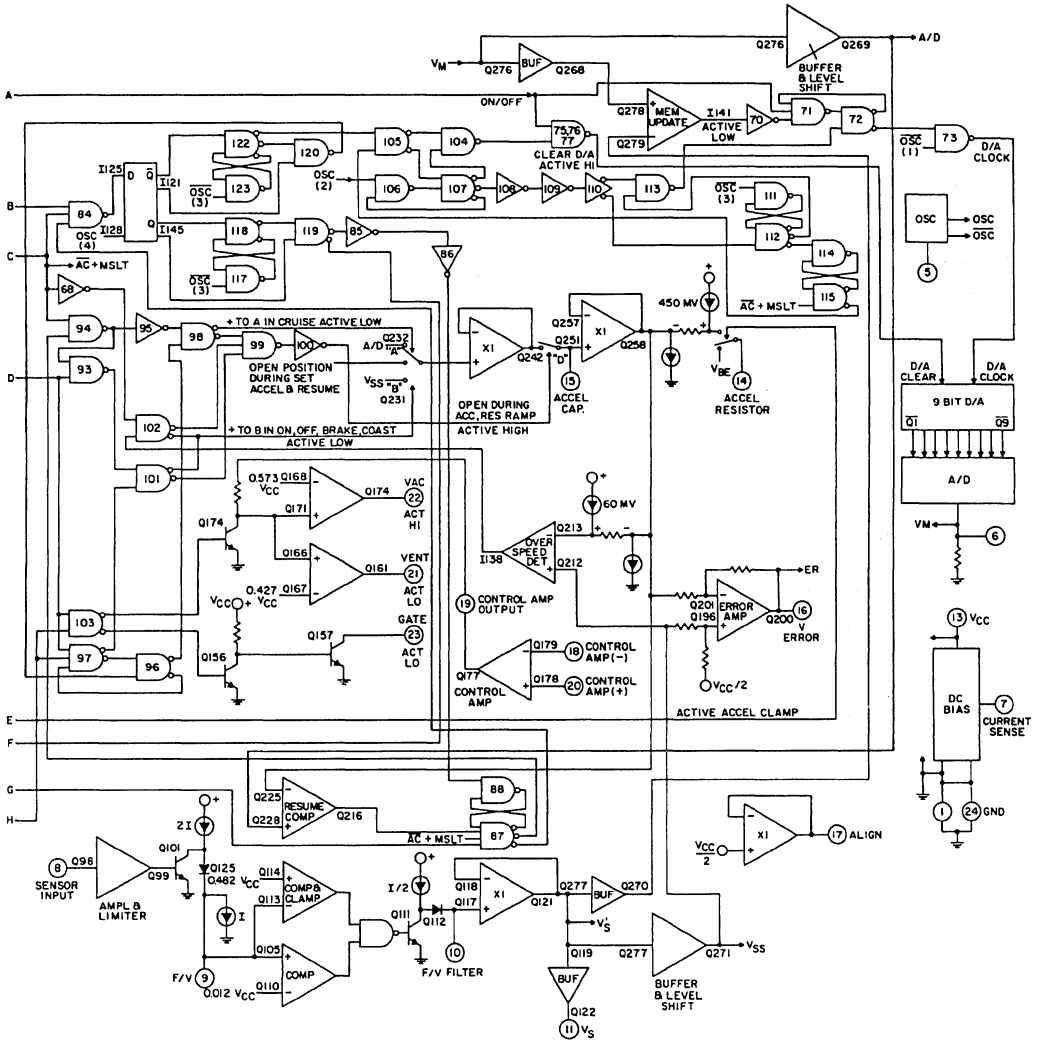


FIGURE 6. FUNCTIONAL BLOCK DIAGRAM FOR SPEED CONTROL (Continued)

HARRIS SEMICONDUCTOR

CA3237

May 1992

IR Remote-Control Amplifier

Features

- Integrated Circuit Package - 9-Pin SIP
- Excellent Overload Characteristics
- High-Gain Amplifiers
- Schmitt Trigger Switching
- 12 Volt Power Supply
- Low Power Dissipation
- Internal Regulation
- Nominal 100μV Sensitivity
- Nominal 50K Input Impedance

Description

The CA3237* is a linear integrated circuit intended for infrared remote control receiver applications for TV receivers. The sensor for the remote control receiver consists of a photo-diode that senses the 40kHz pulse code modulated control signal from the infrared carrier. The other functional parts of the system include an amplifier-limiter, a narrow band filter, a detector, a Schmitt trigger, and a decoder. The CA3237 provides the amplifier limiter and the Schmitt trigger. The amplifier limiter consists of two stages. Both stages have externally accessible feedback points for external gain programming. Internal voltage regulation is provided.

The CA3237 is supplied in nine lead Single-In-Line Package (SIP). The CA3237 is pin-for-pin compatible with the AN5020.

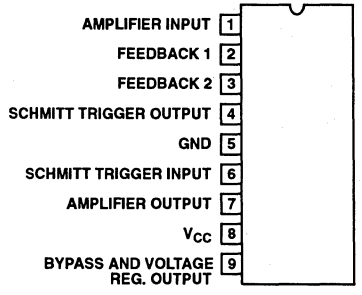
* Formerly developmental type TA11167

Ordering Information

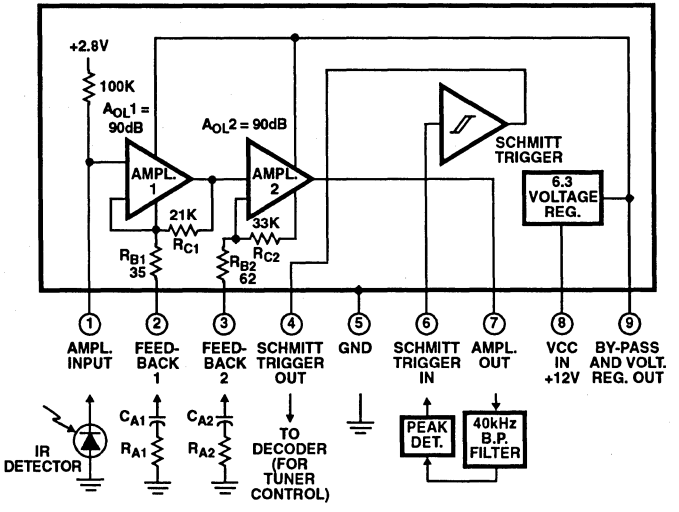
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3237E	-40°C to +85°C	9 Lead Plastic SIP

Pinout

9-LEAD PLASTIC SIP
TOP VIEW



Block Diagram



Absolute Maximum Ratings

T_A = +25°C Unless Otherwise Specified

DC Supply Voltage (V_{CC}) 14.4V
DC Supply Current (I_{CC}) 25mA
Maximum Package Power Dissipation
Up to T_A = +85°C 360mW

NOTE: Recommended supply voltage range (VCC) is 9.6V to 14.4V.

Operating Temperature Range . . . . . -40°C to +85°C
Storage Temperature Range . . . . . -55°C to +150°C
Maximum Junction Temperature . . . . . +150°C
Lead Temperature (During Soldering)
At a distance not less than $^1/_{16}$" (1.59mm) from
case for 10s max . . . . . +260°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V_{CC} = 12V, Unless Otherwise Specified. See Figure 2 for Test Circuit

PARAMETERS	TEST CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
DC SPECIFICATIONS, Switch 1 Open, Switch 2 in Position 3 (Input Open)					
Supply Current	V_{CC} = 14.4V	-	6	10	mA
Balance Voltage, Pin 3		-	2.5	-	V
Bias Voltage, Pin 2		-	2.8	-	V
Regulator Voltage, Pin 9		-	6.3	-	V
Op-Amp Bias Voltage, Pin 7		-	-	1.7	V
AC SPECIFICATIONS, Switch 1 Open Unless Otherwise Specified					
Amplifier High Level, (Pin 7 Out)	V_1 In = $5V_{P-P}$, Freq. = 40kHz, Switch 2 in Position 1	2.5	-	-	V_{P-P}
Amplifier Gain (V_1 In)	Pin 7 Out = $800mV_{P-P}$, Freq. = 40kHz, Switch 2 in Position 1	-	-	500	μV_{P-P}
Schmitt Trigger Output Voltage High (Pin 4 Out)	Pin 6 = $1.5V_{DC}$, Switch 2 in Position 3 (Input Open)	4	-	5	V_{DC}
Schmitt Trigger Output Voltage Low (Pin 4 Out)	Pin 6 = $0.3V_{DC}$, Switch 2 in Position 3 (Input Open)	0	-	0.8	V_{DC}
Schmitt Trigger High Trip Voltage (Pin 6 In)	Pin 4 Out = $4V_{DC}$, Switch 2 in Position 3 (Input Open)	-	-	1.3	V_{DC}
Schmitt Trigger Low Trip Voltage (Pin 6 In)	Pin 4 Out = $0.8V_{DC}$, Switch 2 in Position 3 (Input Open)	0.5	-	-	V_{DC}
Functional Test (Pin 4 Out)	V_{CC} = 9.6V, 12V or 14.4V, V_1 In = $5V_{P-P}$, Freq. = 40kHz, Switch 1 Closed, Switch 2 In Position 1	2	-	-	V_{DC}
Output Noise (at T.P.A.)	Switch 2 in Position 2 (Input Grounded)	-	-	10	mV_{RMS}

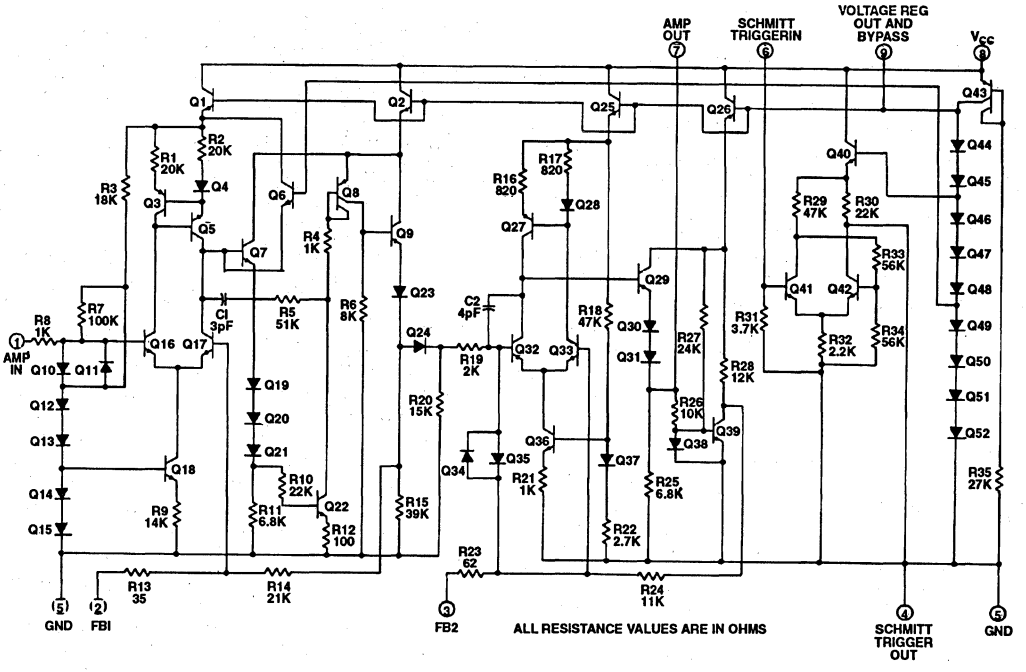


FIGURE 1. SCHEMATIC DIAGRAM FOR CA3237

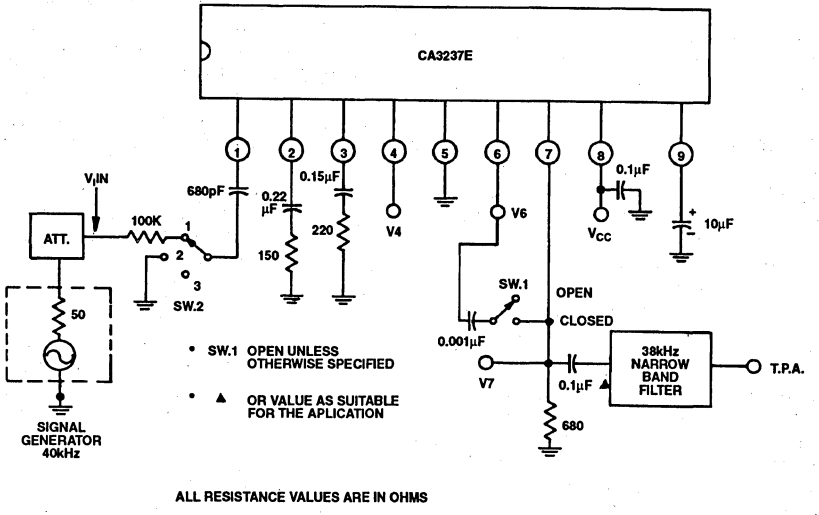


FIGURE 2. TEST CIRCUIT FOR CA3237

General Application

The CA3237 is intended for use in an infrared (IR) remote-control receiver or other comparable application. As shown in Figure 1, this IC consists of two cascaded amplifiers, a Schmitt-trigger circuit, and an internal 6.3-volt regulator. The VCC power-supply input may range from 8 to 14 volts.

Feedback-Amplifier Characteristics

The first amplifier has an open loop gain (A_{OL}) of approximately 90dB, and the second amplifier which is internally cascaded with the first amplifier has an open-loop gain of approximately 60dB. The feedback ratio of the first amplifier is set by the addition of a resistor (Ra1) and an isolation capacitor (Ca1) at pin 2; the gain of the second amplifier is controlled from pin 3 in the same manner. The closed-loop gain Afb, is determined from the general feedback equation:

$$A_{fb} = A_{OL}/[1 + A_{OL} \times B]$$

where B is the feedback ratio

For the non-inverting amplifier the feedback ratio is given by

$$B = 1 + R_c/(Z_a + R_b)$$

where $Z_a = R_a + 1/j\omega C_a$.

If C_a is sufficiently large Z_a is approximately equal to R_a. For large values of A_{OL}, the closed-loop gain is approximately $1 + R_c/(R_c + R_b)$, a good approximation for the first amplifier. For the second amplifier, which has an A_{OL} of 60dB the closed-loop gain is slightly less than the value given by the simplified approximation.

For the feedback circuit values in the test circuit of Figure 2, the simplified gain equation may be used to calculate the first stage gain as follows:

$$A_{fb1}, = 1 + 21k\Omega/(35+150)\ \Omega = 114.5 = 41.2dB$$

This numerical gain corresponds to 41.2 dB.

For the second stage, and using the same approximation, the gain is calculated to be

$$A_{fb2} = 1 + 33\ k\Omega/(62+220)\ \Omega = 118 \text{or } 41.4dB.$$

The total gain from pin 1 to the pin 7 output is

$$\text{Gain} = 41.2+41.4=82.6dB$$

The worst-case conditions allow for Z_{in} and A_{OL} variations. The gain specification from the Electrical Characteristic table is 0.8V for 500µV input. This specification dictates a minimum gain of 1600 (or 64dB) minimum, including input attenuation losses due to the 100-kilohm source resistor. The Figure 2 circuit is specified as a test condition, but is not a limited use of the CA3237. Using circuit layout care and some shielding, it is possible to achieve over 90dB of stable gain.

Amplifier Input/Output Impedance

The input impedance of the first amplifier is typically 50 kilohm and is the combination of the internal 100-kilohm biasing resistor and the input impedance of the first amplifier stage.

If the source impedance of the signal source is high compared to the input impedance of the amplifier, there will be a proportional attenuation at the input signal. For the Figure 2 test circuit, the source impedance is 100 kilohm and the input loss is typically 9dB.

The output drive signal from the second amplifier (at pin 7) is from the emitter follower Q29 and series Q30 and Q31, shown in Figure 1. As shown in the test circuit of Figure 2, it is possible to stiffen the source impedance by additional dc loading at pin 7. It is recommended that the output load be greater than 500Ω.

Amplifier Limiting and Bandwidth

The amplifiers are designed to provide signal limiting over a wide dynamic range with little effect on the duty cycle. In the IC circuit diagram of Figure 1, the Q10 and Q11 back-to-back diodes limit the peak-to-peak drive; additional control is provided by the Q6 emitter at the output of the first differential stage. Limiting starts as low as 50µV. The limiting range continues to a level greater than 1 volt of signal-input capability with typically less than 10% change in duty cycle.

The bandwidth characteristic of the CA3237 is matched to the 40kHz center frequency range commonly used by IR remote systems. For this reason, the roll-off characteristic of the amplifier is optimized for use in the 10kHz to 100kHz area. The 3dB linear signal roll-off is approximately 70kHz and is controlled by internal compensating capacitors on the chip. However, the circuit may function as a limiting-amplifier up to frequencies as high as 1MHz.

Schmitt-Trigger Circuit

The Schmitt trigger is designed to provide a digitally switched signal from a peak detected burst. Use of the Schmitt trigger is recommended as a means of shaping the detected signal at pin 7 before it is input to a decoder circuit.

It is important to note that the Schmitt trigger input has 3.7 kilohm input impedance but drops to a much lower value when the input transistor switches to saturation. The low impedance provides noise immunity during the low (OFF) state. In Figure 1, transistor Q41 and Q42 form the differential switching circuit. The threshold for switching at pin 6 is approximately 1 volt (ON) and 0.8 volt (OFF). The bias supply for the switching differential is determined by the internally regulated supply, which is tapped at 4.2 volts on the stack of reference diodes.

IR Remote Amplifier Application

The circuit diagram of Figure 3 shows a typical application as an IR remote control receiver. The biased IR detector receives transmitted impulses from the remote unit, from which the signal is ac coupled into pin 1 of the CA3237. An optional variation of feedback control of gain is used at pin 3 making the gain of the second stage 50dB.

The amplified signal output at pin 7 goes to the transistor Q1 which acts as buffer to drive a tuned high Q transformer. The

selectivity of this circuit provides noise immunity and rejection of unwanted signals. The signal is normally transmitted in 40kHz pulse bursts, such as illustrated in the waveforms of Figure 3a. This circuit illustrates only one of many possible pulse-code-modulation methods used for data transmission. As many as 20 pulses, 25µs in width, form a burst. The detected burst is one bit of pulse code data. After the first pulse code, a "1" or "0" state is determined by the sequential order of the pulse-code data shown.

In Figure 3, the detection of the pulse code bit is done with a diode peak-detector circuit following the tuned transformer.

The waveforms of Figure 3b illustrate the CA3237 signal. The pin 1 waveform is an IR signal burst and, in this case, is shown as the modulation signal. The output signal at pin 7 is the burst signal with a background level of noise when the burst is not present. The detected signal that is returned to the pin 6 input of the Schmitt trigger is a diode/RC integrated pulse with an exponential rise and fall edge. The saturated switch of the Schmitt trigger has low impedance and clamps the positive edge of the detected pulse. The waveform at pin 4 is the Schmitt trigger output with squared edges, and is 5 volt logic compatible to TTL and CMOS.

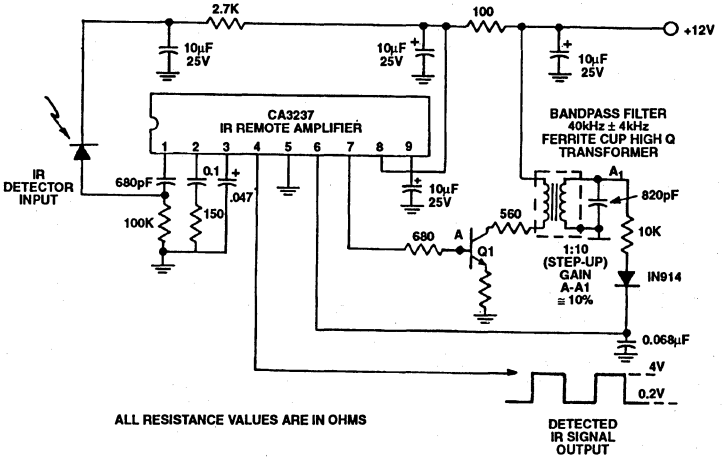


FIGURE 3. TYPICAL IR-REMOTE AMPLIFIER APPLICATION CIRCUIT

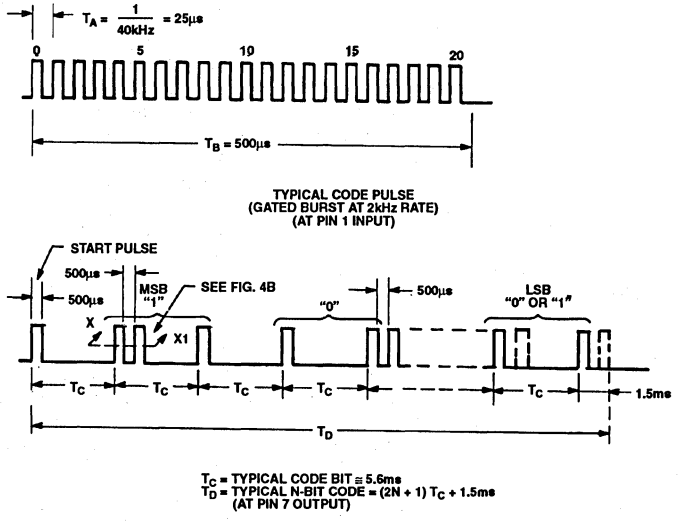


FIGURE 3(a). TYPICAL CODE DATA CONSTRUCTION FOR PULSE CODE MODULATION

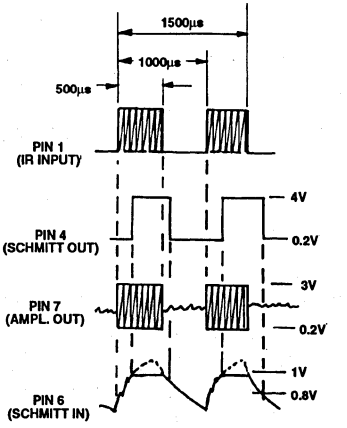


FIGURE 3(b). X-X' WAVEFORMS DETAIL, SEE FIGURE 4a

HARRIS SEMICONDUCTOR

CA3274

Current Limiting Power Switch With Current Limiter Sense Flag

May 1992

Features

- Drive-Current Limiting at Output
- Current-Sense Buffer and Reference
- 200mA Driver Current Capability
- Logic-Level Control Input
- Current Limiting Flag Output
- 50dB Minimum PSRR
- 5μS Typical Switch Time
- Separate Signal and Power Grounds

Applications

- Solenoid Switch Driver
- Relay Driver
- Lamp Control Switch
- Ignition Coil Pre-Driver
- Constant Current Driver
- Current Limiting Switch
- Fault Output Sense Appliance
- Power Supply Fault Mode Control

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3274E	-40°C to +85°C	8 Lead Plastic DIP

Description

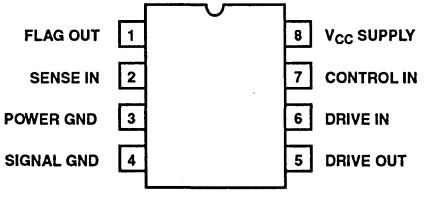
The CA3274 is a controlled current switch and may be used in general purpose switching applications that require specified maximum levels of current. The functional block diagram of the CA3274 is shown and a typical application circuit is shown in Figure 1. An internal emitter follower has 200mA of source drive output capability. The Control Input is a Schmitt trigger buffer amplifier for noise immunity in the environments typical of industrial and automotive control systems.

Current sensing in the emitter circuit of a power-darlington output stage is fed back from a sampling resistor to the sense input of the CA3274 which has a 335mV typical offset. For the example shown in Figure 1, a sampling resistor of 0.056 ohm permits 6.0 amperes (0.335/0.056) of current in the emitter of the output driver. When the current limiter is activated, the flag output changes state conditionally. If the control input is the "0" state, the flag output will remain in a "1" state. If the control input is in the "1" state and the sense input is less than the voltage reference level of 335mV, the flag output will remain in the "1" state. If the control input is the "1" state and the sense input is equal to or greater than the 335mV reference level, the flag output goes to the "0" state. The output flag switch may be used to accurately establish dwell timing in automotive applications. When the control input goes to "0", the flag is reset to "1". Noise-immunity hold-off is used to prevent pre-triggering of the flag output and is noted as td in the timing diagram of Figure 2.

The flag output may be used for diagnostic feedback via the current sense input to detect a fault mode. In this case the sampled drive current is either from the emitter of the CA3274 internal power transistor or an external output amplifier, such as a darlington power transistor or power-FET output stage. The CA3274 has separate power and signal grounds to minimize transient-loop feedback to the input ground and thus prevent false triggering of the output. Optionally, the output from the CA3274 may be taken from the open collector (DRIVE IN) at pin 6. An external resistor at pin 6 may be used to set the level at which Q2 will saturate, providing additional limiting protection for the maximum forward-drive from the CA3274.

Pinout

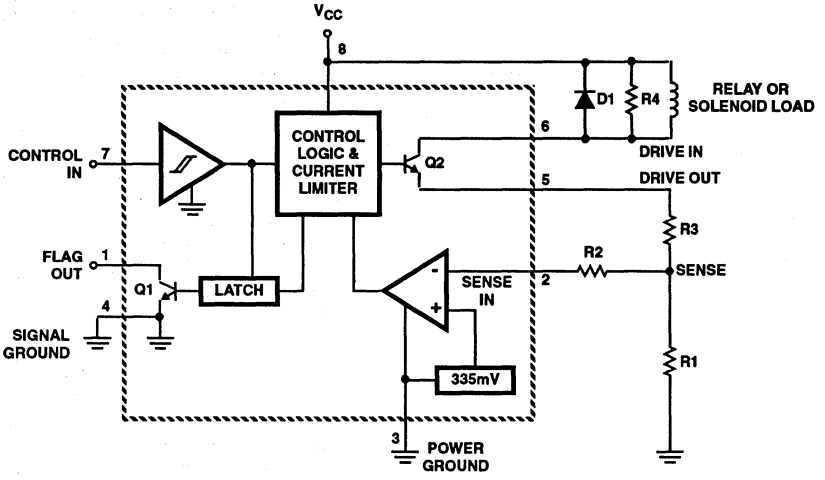
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE (E SUFFIX)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2222.1

Block Diagram



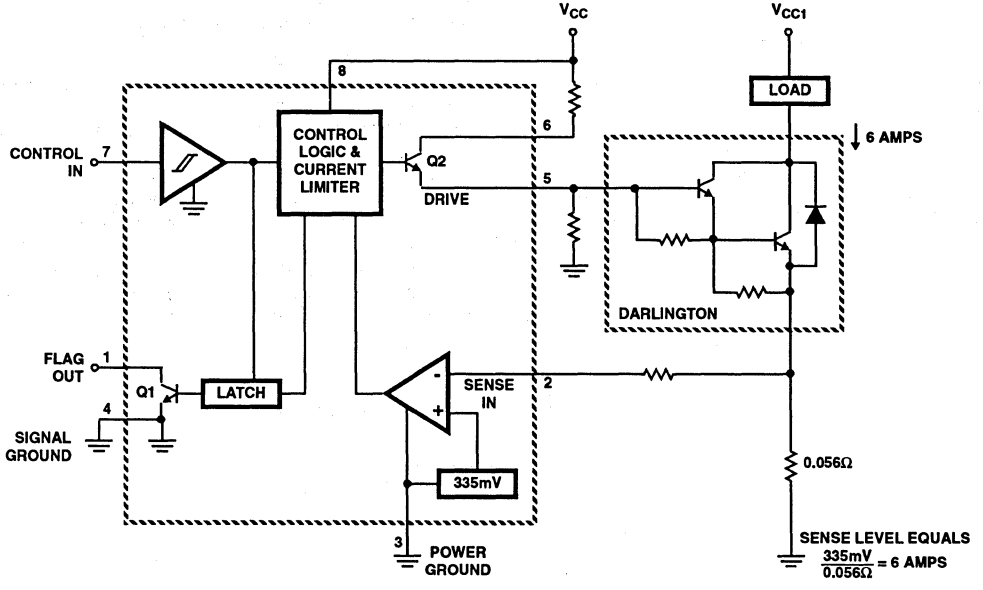


FIGURE 1. TYPICAL APPLICATION AS A POWER SWITCH PRE-DRIVER SWITCH

Absolute Maximum Ratings

Operating Drive Supply, V_{CC} 16V
Maximum Output Current, I_O 200mA
Control, Sense Input..... Gnd - 0.5V, V_{CC} + 0.5V
Signal, Power Differential Ground Voltage..... ±1V
Power Dissipation, P_D
Up to 70°C 630mW
Above 70°C..... Derate linearly at 7.7mW/°C

Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -55°C to +150°C
Lead Temperature (During Soldering)
At distance $^1/_{16}$" (1.59 ± 0.79mm) from case for 10s max..... +250°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

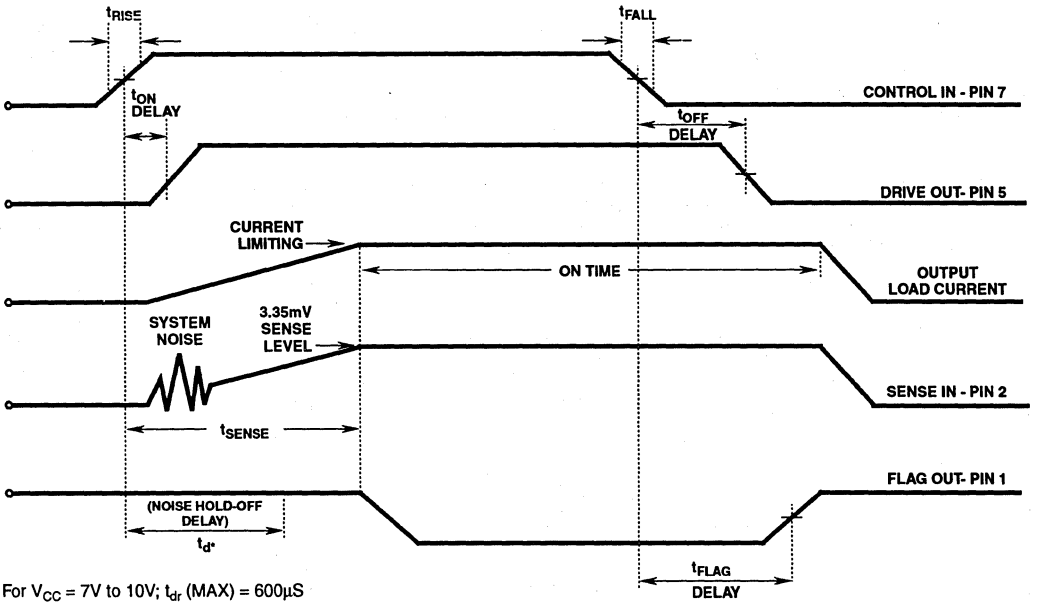
Electrical Specifications

At T_A = -40°C to +85°C, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Power Supply Current: S1 = 2	I_{CCH}	Control = High (Output On)	-	-	25	mA
	I_{CCL}	Control = Low (Output Off)	-	-	5	mA
Control Input: S1 = 3	V_{thdH}	Thd. Voltage, High	-	-	3.5	V
	V_{thdL}	Thd. Voltage, Low	0.9	-	-	V
	V_{thdH}-V_{thdL}	Hystersis	0.4	0.65	2.0	V
	I_{IL}	Leakage, 0.0 to 5.5V	-20	-	+20	µA
Driver In, Out (Pin 6, 5): S1 = 3	V_{sat}	Output Saturation Voltage, I_{CC1} = 200mA, $V_{CONTROL}$ = High	-	-	0.5	V
	I_{LEAK}	Collector Output Leakage, $V_{CONTROL}$ = Low	-	-	100	µA
Flag Output Low: S1 = 2	V_{fsat}	V_{SENSE} = High, I_{FLAG} = 3mA	-	-	0.8	V
Flag Output High: S1 = 3	V_{fleak}	Output Leakage, V_{CC} = V_{FLAG} = 10V	-	-	10	µA
Prop. Delay: S1 = 1	t_{on}, t_{off}	Control In to Drive Out	-	5	-	µs
	t_{FLAG}	Drive Off to Flag Off	-	10	-	µs
	t_d	Flag Delay from Control In	150	-	600	µs
Sense Input Thd. Level: S1 = 1	V_{senthd}		310	335	360	mV
Power Supply Rejection Ratio	PSSR		50	-	-	dB

NOTES:

1. Refer to Figure 3 Test Diagram for electrical test connections.
2. Refer to Figure 2 Timing Diagram for logic switching and prop delay.
3. Unless otherwise specified: V_{CC} = V_{CC1} = V_{CC2} = 7 to 10 volts;
V_{SENSE} = "Low"; $V_{CONTROL}$ = "Low";
Control in levels are defined as "Low" equals 0.0V and "High" equals 5.0V.



* For V_{CC} = 7V to 10V; t_{dr} (MAX) = 600µS if Control In = High, Sense In = High; Pin 1, Flag Out can go low only if $t_{SENSE} \geq t_d$

FIGURE 2. CA3274 TIMING DIAGRAM

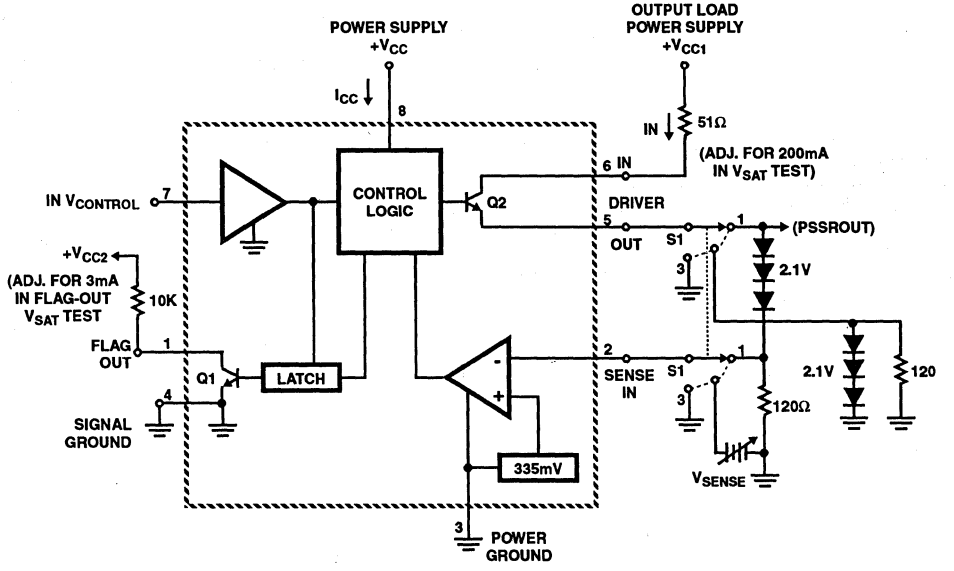


FIGURE 3. CA3274 TEST CIRCUIT

HARRIS SEMICONDUCTOR

HIP9020

PRELIMINARY

May 1992

Programmable Quad Buffer with Pre and Post Scaler Dividers

Features

- Sine Wave Speedometer Input
- Input Limiting.....±0.25 to ±100V (with 40kΩ)
- Over Voltage Protection
- Current Limiting
- Programmable Prescaler 1, 6 - 11
- Post Scaler Frequency Divide by 1 or 2
- Drivers with 15mA/24V Capability
- Outputs 4 Separate Square Waves
- Internal Regulator and Bias Source
- 0kHz to 6kHz Input Signal Range
- -40°C to +125°C Operating Temperature Range

Applications

- Prescaler
- Buffer/Limiter
- Signal Interface
- Automotive Speedometer
- Automotive Speed Control
- Automotive Tachometer

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIP9020AP	-40°C to +125°C	14 Lead Plastic DIP
HIP9020AB	-40°C to +125°C	20 Lead Plastic SOIC

Description

The HIP9020 is a Vehicle Speed Sensor (VSS) Buffer IC. It receives sinusoidal vehicle speed information from a speedometer signal source. The signal is amplified and squared before frequency processing is done. The circuit provides pin programmable integer prescaler and postscaler dividers to scale the output frequencies. The prescaler divider output of the frequency doubler is mode selected for 1 and 6 through 11. The postscaler mode is selected to the Output 3 with a divide by 1 or 2. The four V_{OX} outputs are open collector drivers.

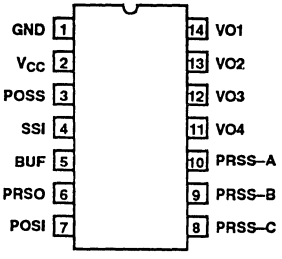
Speed Sensor Input (SSI) - When current limited with a 40 kohm source impedance from the vehicle speed sensor, the SSI input is capable of functioning over a wide range of input signal. The limiter and squaring action is derived from the zero crossing of the input signal. The signal is converted into a square wave with a controlled hysteresis squaring amplifier.

Power Supply - The power supply pin 2 input is intended to operate from a 5.0V ± 0.3V source. The internal reference sources are derived from a temperature stable bandgap; including an optional 5.7V shunt reulator which may be used as shown in Figure 2.

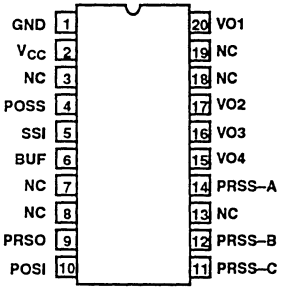
Output Drivers - Each output driver is an open NPN collector with a zener clamp level of typically 35 volts and short circuit current limiting. Each output is capable of sinking 15mA of current.

Pinouts

14 LEAD PLASTIC DIP
TOP VIEW



20 LEAD PLASTIC SOIC
TOP VIEW

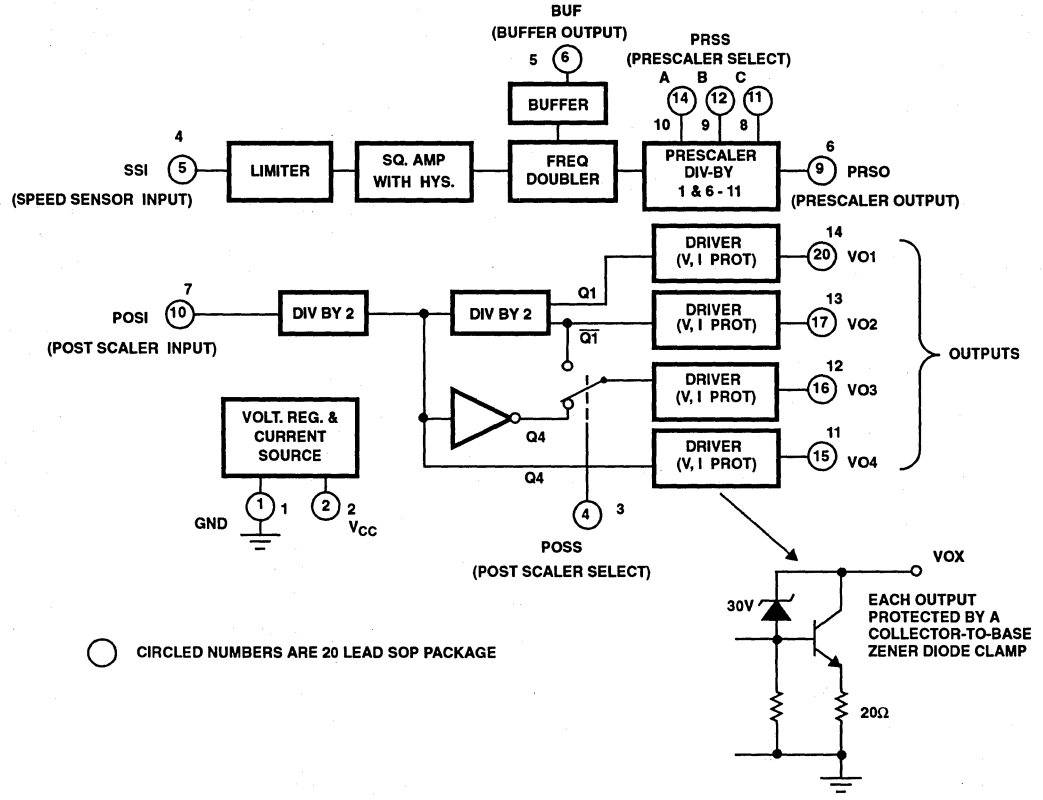


9 SPECIAL FUNCTIONS

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2790.1**

Programmable Quad Buffer Functional Block Diagram



LOGIC SELECT FOR INPUT (SSI) TO OUTPUT (VOX) DIV-BY NUMBER

PRSS-A	PRSS-B	PRSS-C	VO1, VO2, VO3 (POSS HIGH) DIV-BY	VO4 (POSS HIGH) DIV-BY	VO1, VO2 (POSS LOW) DIV-BY	VO3, VO4 (POSS LOW) DIV-BY
0	0	0	2	1	2	1
0	0	1	12	6	12	6
0	1	0	14	7	14	7
0	1	1	16	8	16	8
1	0	0	18	9	18	9
1	0	1	20	10	20	10
1	1	0	22	11	22	11

Absolute Maximum Ratings

Supply Voltage to Pin 2, V_{CC} (Shunt Regulator). . . . . +24V_{DC} Maximum through 300 ohms and a series diode (1N4005 or equiv.) or +5.3 V Maximum direct voltage supply source to V_{CC}.
Output Voltage (Sustained) to V01,V02,V03,V04. . . . . +24V
Output Load Current (Sink) . . . . . +15mA
Input Voltage (Through 40 KΩ, See Figure 1) . . . . . ±100V

Plastic 14 Pin DIP & 20 PIN SOP Package
Thermal Resistance, θ_{ja} . . . . . 90°C/W
Maximum Package Power Dissipation up to +85°C 610mW
Derate above 85°C . . . . . 11.1mW/°C
Operating Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range. . . . . -65°C to +150°C
Maximum Junction Temperature. . . . . +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = -40°C to +125°C, V_{CC} = 5V ± 0.3V, Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Power Supply (V_{CC})					
Supply Current	I_{CC}		-	12	mA
SSI Input (Test Point - T.P.A., See Figure 1)					
Max. Operating Frequency	$f_{S(MAX)}$	40kΩ Source, 0.01µF Input Shunt	-	6	kHz
Input Signal Range		40kΩ Source, 0.01µF Input Shunt	±0.25	±100	V
Input Hysteresis		40kΩ Source, 0.01µF Input Shunt	0.15	0.45	V
Input Bias Current		40kΩ Source, 0.01µF Input Shunt	-0.5	+0.5	µA
Other Inputs (PRSS, POSS, POSI - See Function Block Diagram)					
Input Low Voltage	V_{IL}		-	1.5	V
Input High Voltage	V_{IH}		3.5	-	V
Input Current High	I_{IH}	$V_{CC} = V_{IN} = 4.7V$	-	10	µA
Input Current Low	I_{IL}	$V_{CC} = 5.3$; $V_{IN} = 0.4V$	-10	-	µA
PRSO Output					
Output Voltage Low	V_{OL}	V_{CC} = 5V		0.4	V
Output Voltage High	V_{OH}	V_{CC} = 5V	4.6	-	V
Driver Outputs (V01, V02, V03, V04)					
Output Clamp Voltage		I_{CC} = 1mA	24	45	V
Output Current Limit		I_{SC} Current Pulsed	15	30	mA
Output Leakage		V_{OUT} = 24V	-	30	µA
Ouptut Saturation Voltage	V_{SAT}	I_{OUT} = 15mA	-	1	V
		I_{OUT} = 1mA	-	0.4	V

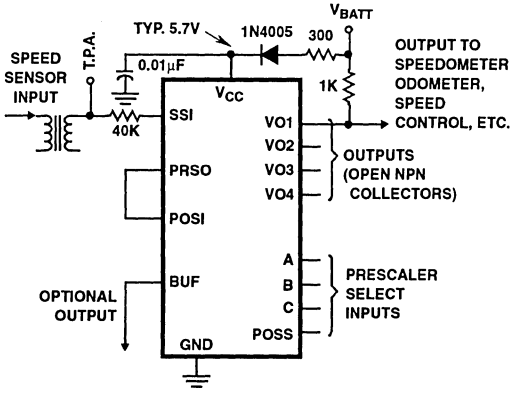


FIGURE 1. TYPICAL AUTOMOTIVE APPLICATION CIRCUIT

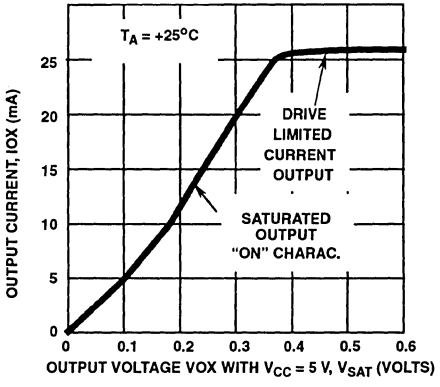


FIGURE 2. TYPICAL OUTPUT DRIVER SATURATED "ON" CHARACTERISTIC

INTELLIGENT POWER ICs 10

APPLICATION NOTES

APPNOTE

No. 6157 May 1992

Harris Intelligent Power

APPLICATIONS OF THE CA3085 SERIES MONOLITHIC IC VOLTAGE REGULATORS

Authors: A.C.N. Sheng and L.R. Avery

The Harris CA3085, CA3085A, and CA3085B monolithic IC's are positive-voltage regulators capable of providing output currents up to 100 milliamperes over the temperature range from -55°C to +125°C. They are supplied in 8 lead TO-5 type packages. The following tabulation shows some key characteristics and salient differences between devices in the CA3085 Series.

TYPE	V_{IN} (V_I) RANGE V	V_{OUT} (V_O) RANGE V	MAX. I_{OUT} (I_O) mA	MAX LOAD REGULATION % V_O
CA3085	7.5 - 30	1.8 - 26	12*	0.1
CA3085A	7.5 - 40	1.7 - 36	100	0.15
CA3085B	7.5 - 50	1.7 - 46	100	0.15

*This value may be extended to 100mA; however, regulation is not specified beyond 12mA.

In addition to these differences, the range of some specified performance parameters is more tightly controlled in the CA3085B than in the CA3085A, and more in the CA3085A than in the CA3085.

This note describes the basic circuit of the CA3085 series devices and some typical applications that include a high current regulator, constant current regulations, a switching regulator, a negative-voltage regulator, a dual-tracking regulator, high-voltage regulators, and various methods of providing current limiting, A circuit in which the CA3085 is used as a general-purpose amplifier is also shown.

Circuit Description

The block diagram of the CA3085 series circuits is shown in Figure 1. Fundamentally, the circuit consists of a frequency compensated error-amplifier which compares an internally generated reference voltage with a sample of the output voltage and controls a series-pass amplifier to regulate the output. The starting circuit assures stable latch-in of the voltage-reference circuitry. The current-limiting portion of the circuit is an optional feature that protects the IC in the event of overload.

Terminal 5 provides a source of stable reference voltage for auxiliary use; a current of about 250 microamperes can be supplied to an external circuit without significantly disturbing reference-voltage stability. If necessary, filtering of the inherent noise of the reference-voltage circuit can be accomplished by connecting a suitable bypass capacitor between terminals 5 and 4.

Terminal 6 (the "inverting input" in accordance with operational-amplifier terminology) is the input through which a sample of the regulated output voltage is applied.

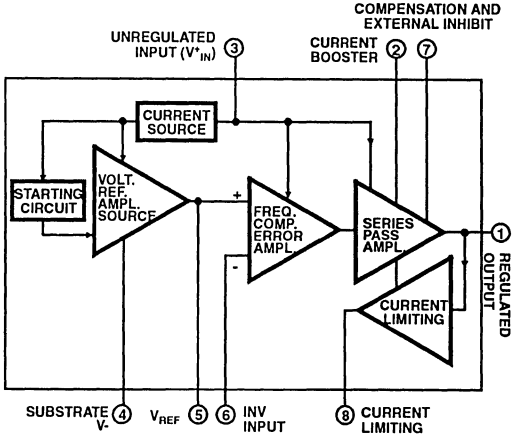


FIGURE 1. BLOCK DIAGRAM OF CA3085 SERIES

The collector of the series-pass output transistor is brought out separately at terminal 2 ("current booster") to provide base drive for an external p-n-p transistor; this approach is one method of regulating currents greater than 100 milliamperes.

Because the voltage regulator is essentially an operational amplifier having considerable feedback, frequency compensation is necessary in some circuits to prevent oscillations. Terminal 7 is provided for if external frequency compensation is necessary. Terminal 7 can also be used to "inhibit" (strobe, squelch, pulse, key) the operation of the series-pass amplifier.

Brief Description of CA3085 Schematic Diagram

The schematic diagram of the CA3085 series circuits is shown in Figure 2. The left-hand section includes the starting circuit, the voltage reference circuit, and the constant-current circuit. The center section is basically an elementary operational amplifier which serves as the voltage-error

amplifier controling the series-pass. Darlington pair (Q13, Q14) shown in the right-hand section when controlled by an appropriate external sensing network, transistor Q15, serves to provide protective current-limiting characteristics by diverting base drive from the series pass circuit. For operation at the highest current levels, terminals 2 and 3 are tied together to eliminate the voltage drop which would otherwise be developed across resistor R5.

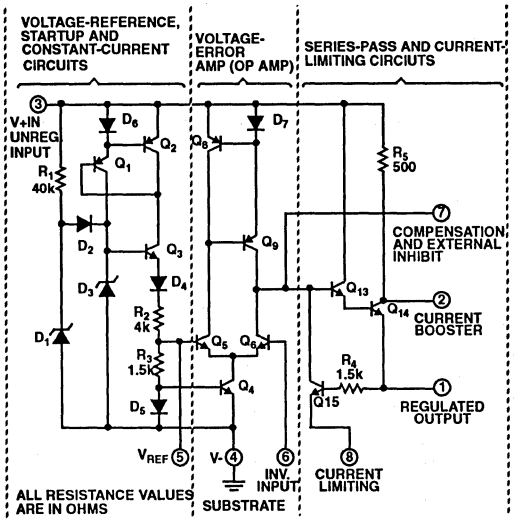


FIGURE 2. SCHEMATIC DIAGRAM OF CA3085 SERIES

Voltage Reference Circuits

The basic voltage referenced element used in the CA3085 is zener diode D3. It provides a nominal reference voltage of 5.5 volts and exhibits a positive temperature coefficient of approximately 2.5 millivolts/°C. If this reference voltage were used directly in conjunction with the error-amplifier (Q5, Q6, etc.), the IC would exhibit two major undesirable characteristics: (1) its performance with temperature variations would be poor, and (2) its use as a regulator would be restricted to circuits in which the minimum regulated output voltages are in excess of 5.5 volts. Consequently, it is necessary to provide means of compensating for the positive temperature coefficient of D3 and at the same time provide for obtaining a stable source of lower reference voltage. Both temperature compensation and the reduction of the reference voltage are accomplished by means of the series divider network consisting of the base-emitter junction of Q3, diode D4, resistors R2 and R3, and diode 5.

The voltage developed across D3 drives the divider network and a voltage of approximately 4 volts is developed between the cathode of D4 and the cathode of D5 (terminal 4). The current through this divider network is held nearly constant with temperature because of the combined temperature coefficients of the zener diode (D3), Q3 base-emitter junction, D4, D5, and the resistors R2 and R3. This constant current through the diode D5 and the resistor R3 produces a voltage drop between terminals 4 and 5 that results in the reference voltage (≈ 1.6 volts) having an effective temperature coefficient of about 0.0035 per cent/°C.

The reference diode D3 receives a currant of approximately 620 microamperes from a constant-current circuit consisting of Q3 and the current-mirror* D6, Q1, and Q2. Current to start-up the constant-current source initially is provided by auxiliary zener diode D1 and R1. Diode D2 blocks current from the R1-D1 source after latch-in of the constant-current source establishes a stable reference potential, and thereby prevents modulation of the reference voltage by ripple voltage on the unregulated input voltage.

Voltage-Error Amplifier

Transistors Q5 and Q6 comprise the basic differential amplifier that is used as a voltage-error amplifier to compare the stable reference voltage applied at the base of Q5 with a sample of the regulator output voltage applied at terminal 6. The D5-Q4 combination is a current-mirror which maintains essentially constant-current flow to Q5 and Q6 despite variations in the unregulated input voltage. The Q8, Q9, and D7 network provides a "mirrored" active collector load for Q5 and Q6 and also provides a variable single-ended drive to the Q13 and Q14 series-pass transistors in accordance with the difference signal developed between the bases of Q5 and Q6. The open-loop gain of the error-amplifier is greater than 1000.

Series-Pass and Current-Limiting Circuits

In the normal mode of operation, or in the current-boost mode when terminals 2 and 3 are tied together, the Darlington pair Q13-Q14 performs the basic series-pass regulating function between the unregulated input voltage and the regulated output voltage at terminal 1. In the current-limiting mode transistor Q15 provides current-limiting to protect the CA3085 and.or limit the load current. To provide current-limiting protection, a resistor (e.g., 5 ohms) is connected between terminals 1 and 8; terminal 8 becomes the source of regulated output voltage. As the voltage drop across this resistor increases, base drive is supplied to transistor Q15 so that it becomes increasingly conductive and diverts base drive from the Q13-Q14 pass transistor to reduce output current accordingly. Resistor R4 is provided to protect Q15 against overdrive by limiting its base current under transient and load-short conditions.

Because the CA3085 regulator is essentially an op-amp having considerable feedback, frequency compensation may be required to prevent oscillations. Stability must also be maintained despite line and load transients, even during operation into reactive loads (e.g., filter capacitors). Provisions are included in the CA3085 so that a small-value capacitor may be connected between terminals 6 and 7 to compensate the regulator, when necessary, by "rolling-off" the amplifier frequency-response. Terminal 7 is also used to externally "inhibit" operation of the CA3085 by diverting base current supplied to Q13-Q14, thereby permitting the use of keying, strobing, programming, and/or auxiliary overload-protection circuits.

Applications

A Simple Voltage Regulator

Figure 3 shows the schematic diagram of a simple regulated power supply using the CA3085. The ac supply voltage is stepped down by T1, full-wave rectified by the diode bridge circuit, and smoothed by the large electrolytic capacitor C1 to provide unregulated dc to the CA3085 regulator circuit. Frequency compensation of the error-amplifier is provided by capacitor C2. Capacitor C3 bypasses residual noise in the reference-voltage source, and thus decreases the incremental noise-voltage in the regulator circuit output.

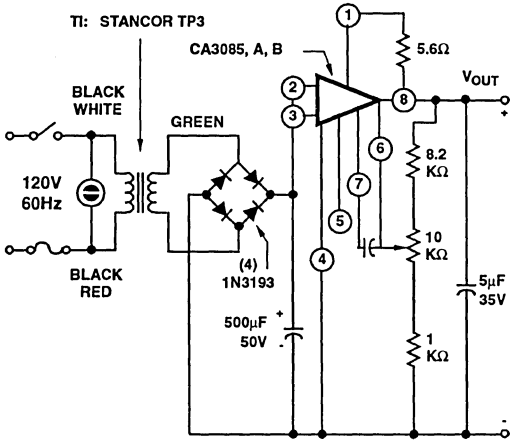


FIGURE 3. BASIC POWER SUPPLY

Because the open-loop gain of the error-amplifier is very high (greater than 1000), the output voltage may be directly calculated from the following expression:

$$V_O = \frac{(R2 + R1)}{R1} V_{ref} \qquad (1)$$

In the circuit shown in Figure 3, the output voltage can be adjusted from 1.8 volts to 20 volts by varying R2. The maximum output current is determined by RSC; load-regulation characteristics for various values of RSC are shown in Figure 4.

When this circuit is used to provide high output currents at low output voltages, care must be exercised to avoid excessive IC dissipation. In the circuit of Figure 3, this dissipation control can be accomplished by increasing the primary-to-secondary transformer ratio (a reduction in V_I) or by using a dropping resistor between the rectifier and the CA3085 regulator. Figure 5 gives data on dissipation limitation ($V_I - V_O$ vs. I_O) for CA3085 series circuits. The short-circuit current is determined as follows:

$$I_{SC} \quad \frac{V_{SE}}{R_{SC}} \approx \frac{0.7}{R_{SC}} \text{ amperes} \qquad (2)$$

The line-and-load regulation characteristics for the circuit shown in Figure 3 are approximately 0.05 percent of the output voltage.

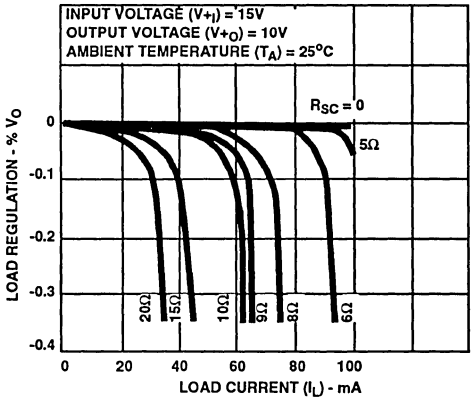


FIGURE 4. LOAD REGULATION CHARACTERISTICS FOR CIRCUIT OF FIGURE 3.

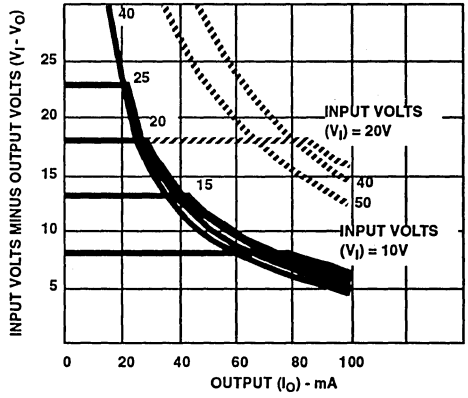
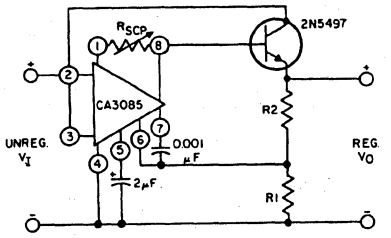


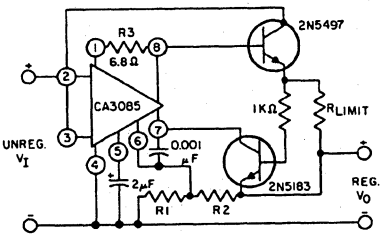
FIGURE 5. DISSIPATION LIMITATION ($V_I - V_O$ vs. I_O) FOR CA3085 SERIES CIRCUITS

High-Current Voltage Regulator

When regulated voltages at currents greater than 100 milliamperes are required, the CA3085 can be used in conjunction with an external n-p-n pass transistor as shown in the circuits of Figure 6. In these circuits the output current available from the regulator is increased in accordance with the h_{FE} of the external n-p-n pass transistor. Output currents up to 8 amperes can be regulated with these circuits. A Darlington power transistor can be substituted for the 2N5497 transistor when currents greater than 8 amperes are to be regulated



(a) WITH SIMPLIFIED SHORT-CIRCUIT PROTECTION



(b) WITH AUXILLIARY SHORT-CIRCUIT PROTECTION

FIGURE 6. HIGH-CURRENT VOLTAGE REGULATOR USING n-p-n PASS TRANSISTOR

A simplified method of short circuit protection is used in connection with the circuit of Figure 6(a). The variable resistor R_{SCP} serves two purposes: 1) it can be adjusted to optimize the base drive requirements (hFE) of the particular 2N5497 transistor being used, and 2) in the event of a short circuit in the regulated output voltage the base drive current in the 2N5497 will increase, thereby increasing the voltage drop across R_{SCP}. As this voltage drop increases the short circuit protection system within the CA3085 correspondingly reduces the output current available at terminal 8, as described previously. It should be noted that the degree of short circuit protection depends on the value of R_{SCP}, i.e., design compromise is required in choosing the value of R_{SCP} to provide the desired base drive for the 2N5497 while maintaining the desired short circuit protection. Figure 6(b) shows an alternate circuit in which an additional transistor (2N2102) and two resistors have been added as an auxiliary short circuit protection feature. Resistor R3 is used to establish the desired base drive for the 2N5497, as described above. Resistor R_{limit} now controls the short circuit output current because, in the event of a short circuit, the voltage drop developed across its terminals increases sufficiently to increase the base drive to the 2N2102 transistor. This increase in base drive results in reduced output from the CA3085 because collector current flow in the 2N2102 diverts base drive from the Darlington output stage of the CA3085 (see Figure 2) through terminal 7. The load regulation of this circuit is typically 0.025 per cent with 0 to 3 ampere load-current variation; line regulation is typically 0.025 percent/volt change in input voltage.

Voltage Regulator with Low V_I - V_O Difference

In the voltage regulators described in the previous section, it is necessary to maintain a minimum difference of about 4 volts between the input and output voltages. In some applications this requirement is prohibitive. The circuit shown in Figure 7 can deliver an output current in the order of 2 amperes with a V_I - V_O difference of only one volt.

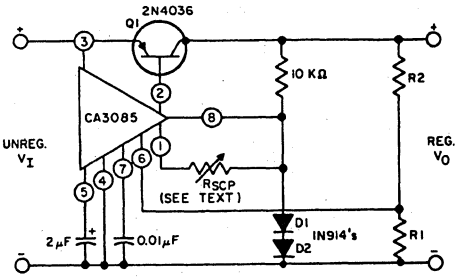


FIGURE 7. VOLTAGE REGULATOR FOR LOW V_I - V_O DIFFERENCE

It employs a single external p-n-p transistor having its base and emitter connected to terminals 2 and 3, respectively, of the CA3085. In this circuit, the emitter of the output transistor (Q14 in Figure 2) in the CA3085 is returned to the negative supply rail through an external resistor (RSCP) and two series-connected diodes (D1, D2). These forward biased diodes maintain Q6 in the CA3065 within linear-mode operation. The choice of resistors R1 and R2 is made in accordance with Eq. (1). Adequate frequency compensation for this circuit is provided by the 0.01 microfarad capacitor connected between terminal 7 of the CA3085 and the negative supply rail.

Figure 8 which shows the output impedance of the circuit of Figure 7 as a function of frequency, illustrates the excellent ripple-rejection characteristics of this circuit at frequencies below 1kHz. Lower output impedances at the higher frequencies can be provided by connecting an appropriate capacitor across the output voltage terminals. The addition of a capacitor will, however, degrade the ability of the system to react to transient-load conditions.

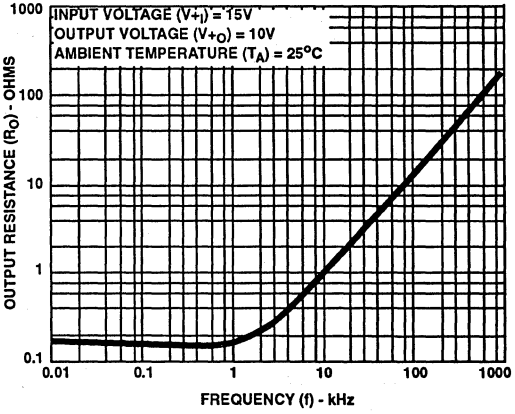


FIGURE 8. OUTPUT RESISTANCE vs. FREQUENCY FOR CIRCUIT OF FIGURE 7

High Voltage Regulator

Figure 9 shows a circuit that uses the CA3085 as a voltage reference and regulator control device for high-voltage power supplies in which the voltages to be regulated are well above the input-voltage ratings of the CA3085 series circuits. The external transistors Q1 and Q2 require voltage ratings in excess of the maximum input voltage to be regulated, Series-pass transistor Q2 is controlled by the collector current of Q1, which in turn is controlled by the normally regulated current output supplied by the CA3085. The input voltage for the CA3085 regulator at terminal 3 is supplied through dropping resistor R3 and the clamping zener diode D1. The values for resistor R1 and R2 are determined in accordance with Eq. (1).

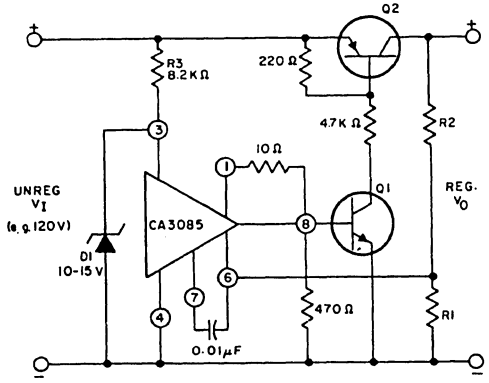


FIGURE 9. HIGH VOLTAGE REGULATOR

Negative Voltage Regulator

The CA3085 is used as a negative-supply voltage regulator in the circuit shown in Figure 10. Transistor Q3 is the series pass transistor. It should be noted that the CA3085 is effectively connected across the load side of the regulated system. Diode D1 is used initially in a "circuit-starter" function; transistor Q2 "latches" D1 out of its starter-circuit function so that the CA3085 can assume its role in controlling the pass transistor Q3 by means of Q1.

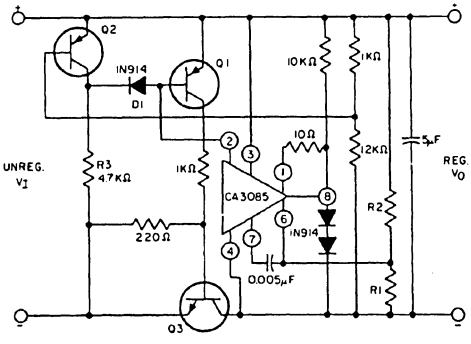


FIGURE 10. NEGATIVE VOLTAGE REGULATOR

Operation of the circuit is as follows: current through R3 and D1 provides base drive for Q1, which in turn provides base drive for the pass-transistor Q3. By this means operating potential for the CA3085 is developed between the collector of Q3 (terminal 4 of the CA3085) and the positive supply-rail (terminal 3 of the CA3085). When the output voltage has risen sufficiently to maintain operation of the CA3085 (approx. 7.5 volts), transistor Q2 is driven into conduction by the base drive supplied from the 1 kilohm-12 kilohm voltage divider. As Q2 becomes conductive, it diverts the base drive being supplied to Q1 through the R3-D1 path, and diode D1 ceases to conduct. Under these conditions, base -current drive to Q1 through terminal 2 of the CA3085 regulates the base drive to Q3. Values of R1 and R2 are determined in accordance with Eq. (1).

The circuit shown in Figure 11 is similar to that of Figure 10, except for the addition of a constant-current limiting circuit consisting of transistor Q4, a 1-kilohm resistor, and resistor RSCP. When the load current increases above a particular design value, the corresponding increase in the voltage drop across resistor RSCP provides additional base drive to transistor Q4. Thus, as transistor Q4 becomes increasingly conductive, its collector current diverts sufficient base drive from Q3 to limit the current in the pass transistor feeding the regulated load. With the types of transistors shown in Figures 10 and 11, maximum currents in the order of 5 amperes can be regulated.

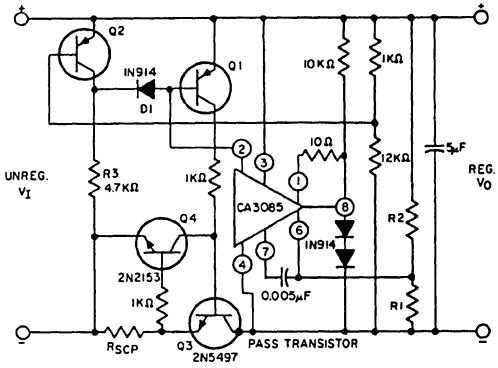


FIGURE 11. NEGATIVE VOLTAGE REGULATOR WITH CONSTANT CURRENT LIMITING CIRCUIT

High-Output-Current Voltage Regulator With "Foldback" Current-Limiting (Also known as "Switch-Back" Current-Limiting)

In high-current voltage regulators employing constant current limiting (e.g., Figures 6 and 7), it is possible to develop excessive dissipation in the series-pass transistor when a short circuit develops across the output terminals. This situation can be avoided by the use of the "foldback" current-limiting circuitry as shown in Figure 12. In this circuit, terminal 8 of the CA3085 senses the output voltage, and terminal 1 is tied to a tap on a voltage-divider network connected

between the emitter of the pass-transistor (Q3) and ground. The current-foldback trip-point is established by the value of resistor RSC.

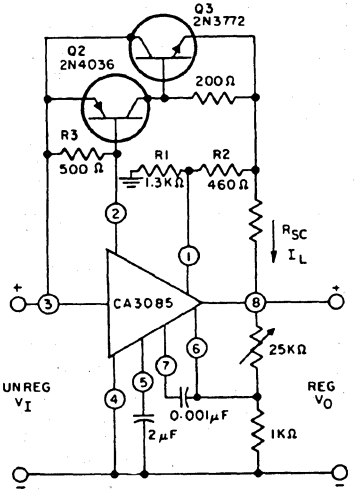


FIGURE 12. HIGH OUTPUT CURRENT VOLTAGE REGULATOR WITH "FOLDBACK" CURRENT LIMITING

The protective tripping action is accomplished by forward-biasing Q15 in the CA3085 (see Figure 2). Conditions for tripping circuit operation are defined by the following expressions:

$$V_{SE(Q15)} = \text{(voltage at terminal 1) - (output voltage)}$$

$$= \left[(V_O + I_L R_{SC}) \frac{R1}{R1 + R2} \right] - V_O \qquad (3)$$

$$\text{If } \frac{R1}{R1 + R2} = K, \text{ then}$$

$$V_{SE(Q15)} = (V_O + I_L R_{SC})\, K - V_O = KV_O + KI_L R_{SC} - V_O$$

and therefore

$$RSC = \frac{V_O + V_{SE(Q15)} - KV_O}{KI_L} \qquad (4)$$

Under load short-circuit conditions, terminal 8 is forced to ground potential and current flows from the emitter of Q14 in the CA3085, establishing terminal 1 at one V_{SE}-drop [≅0.7V] above ground and Q15 in a partially conducting state. The current through Q14 necessary to establish this one V_{SE} condition is the sum of currents flowing to ground through R1 and [R2 + R_{SC}]. Normally R_{SC} is much smaller than R2 and can be ignored; therefore, the equivalent resistance R_{eq} to ground is the parallel combination of R1 and R2.

The Q14 current is then given by:

$$I_{Q14} = \frac{V_{SE(Q15)}}{R_{eq}} = \frac{V_{SE(Q15)}}{\frac{R1R2}{R1 + R2}} = \frac{0.7\,[1.3 + 0.46]}{1.3 \times 0.46} \quad 2.06\text{mA}$$

This current provides a voltage between terminals 2 and 3 as follows:

$$V_{2\text{-}3} = I_{Q14} \times 250\text{ohms} = 2.06 \times 10^{-3} \times 250 = 0.515\text{volt}$$

The effective resistance between terminals 2 and 3 is 250 ohms because the external 500-ohm resistor R3 is in parallel with the internal 500-ohm resistor R5. It should be understood that the $V_{2\text{-}3}$ potential of 0.515 volt is insufficient to maintain the external p-n-p transistor Q2 in conduction, and, therefore, Q3 has no base drive. Thus the output current is reduced to zero by the protective circuitry. Figure 13 shows the foldback characteristic typical of the circuit of Figure 12.

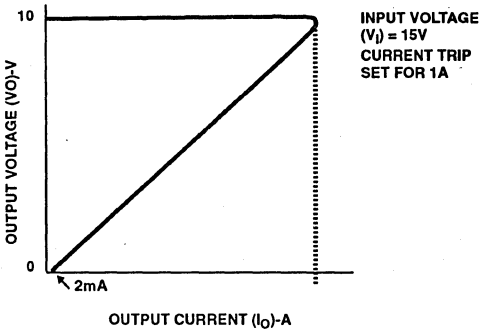


FIGURE 13. TYPICAL "FOLDBACK" CURRENT-LIMITING CHARACTERISTIC FOR CIRCUIT OF FIGURE 12

An alternative method of providing "foldback" current-limiting is shown in Figure 14. The operation of this circuit is similar to that of Figure 12 except that the foldback-control transistor Q2 is external to the CA3085 to permit added flexibility in protection-circuit design.

Under low load conditions Q2 is effectively reverse-biased by a small amount, depending upon the values of R3 and R4. As the small amount, depending upon the values of R3 and R4. As the load current increases the voltage drop across R_{trip} increases, thereby raising the voltage at the base of Q1, and Q2 starts to conduct. As Q2 becomes increasingly conductive it diverts base current from transistors Q13 and Q14 in the CA3085, and thus reduces base drive to the external pass-transistor Q1 with a consequent reduction in the output voltage. The point at which current-limiting occurs, I_{tnp}, is calculated as follows:

$V_{BE(Q1)}$ = voltage at terminal 8 - V_O (assuming a low value for R_{trip})

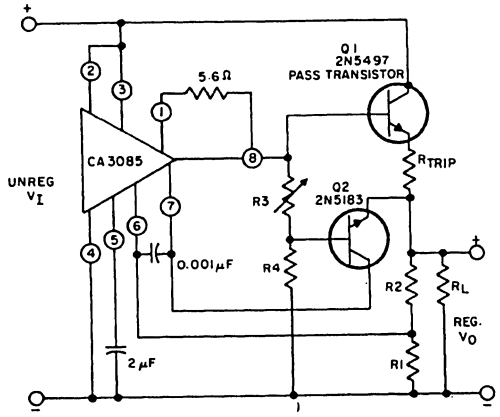


FIGURE 14. HIGH-OUTPUT-CURRENT VOLTAGE REGULATOR USING AUXILIARY TRANSISTOR TO PROVIDE "FOLDBACK" CURRENT LIMITING

$$V_{BE(Q2)} = \text{voltage at terminal 0} \left(\frac{R4}{R3+R4} \right) - V_O$$

$$= \left[V_O + I_L R_{trip} + V_{BE(Q1)} \right] \left[\frac{R4}{R3+R4} \right] - V_O$$

$$\text{if } K = \frac{R4}{R3+R4}, \text{ then the trip current is given by:}$$

$$I_{trip} = \frac{V_{BE(Q2)} - K[V_O + V_{BE(Q1)}]}{KR_{trip}} \quad (7)$$

In the circuit in Figure 12 the load current goes to zero when a short circuit occurs. In the circuit of Figure 14 the load current is significantly reduced but does not go to zero. The value for I_{SC} is computed as follows:

$$V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)} \right] R1 = V_{BE(Q1)} + I_{SCRtrip}$$

$$V_{BE(Q2)} + \left[\frac{V_{BE(Q2)}}{R2} + I_{B(Q2)} \right] R1 = V_{BE(Q1)}$$

$$I_{SC} = \frac{}{R_{trip}} \quad (8)$$

Figure 15 shows that the transfer characteristic of the load current is essentially linear between the "trip-point" and the "short-circuit" point.

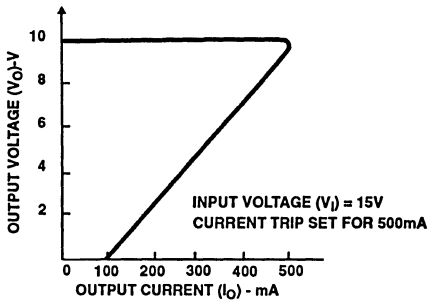


FIGURE 15. TYPICAL FOLDBACK CURRENT-LIMITING CHARACTERISTIC FOR CIRCUIT OF FIGURE 14

High-Voltage Regulator Employing Current "Snap-Back" Protection

In high-voltage regulators (e.g., see Figure 9), "foldback" current-limiting cannot be used safely because the high voltage across the pass transistor can cause second breakdown despite the reduction in current flow. To adequately protect the pass transistor in this type of high-voltage regulator, the so-called "snap-back" method of current limiting can be employed to reduce the current to zero in a few microseconds, and thus prevent second-breakdown destruction of the device.

The circuit diagram of a high-voltage regulator employing current "snap-back" protection is shown in Figure 16. The basic regulator circuit is similar to that shown in Figure 9. The additional circuitry in the circuit of Figure 16 quickly interrupts base drive to the pass transistor in event of load fault. The point of current-trip is established as follows:

$$I_{trip} = \frac{V_{BE(Q1)}}{R_{SC}} \quad (9)$$

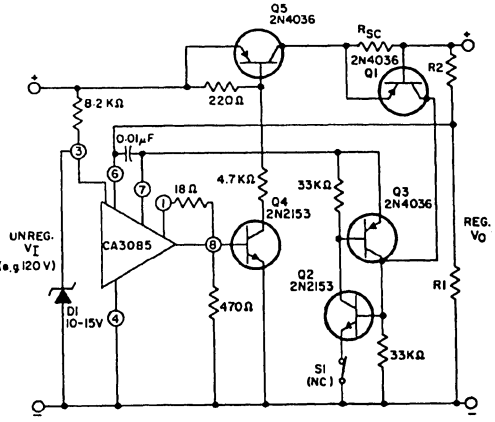


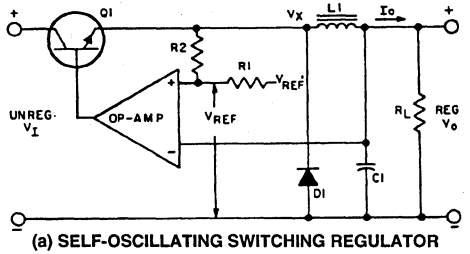
FIGURE 16. HIGH-VOLTAGE REGULATOR INCORPORATING CURRENT "SNAP-BACK" PROTECTION

Thus, when a sufficient voltage drop is developed across R_{SC}, transistor Q1 becomes conductive and current flows into the base of Q2 so that it also becomes conductive. Transistor Q3, in turn, is driven into conduction, thereby latching the Q2-Q3 combination (basic SCR action) so that it diverts (through terminal 7) base drive from the output stage (Q13, Q14) in the CA3085. By this means, base drive is diverted from Q4 and the pass transistor Q5. To restore regulator operation, normally closed switch S1 is momentarily opened and unlatches Q2-Q3.

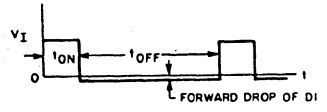
Switching Regulator

When large input-to-output voltage differences are necessary, the regulators described above are inefficient because they dissipate significant power in the series-pass transistor. Under these conditions, high-efficiency operation can be achieved by using a switching-type regulator of the generic type shown in Figure 17(a). Transistor Q1 acts as a keyed switch and operates in either a saturated or cut-off condition to minimize dissipation. When transistor Q1 is conductive, diode D1 is reversed-biased and current in the inductance L1 increases in accordance with the following relationship:

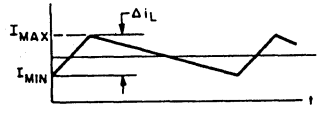
$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt \qquad (10)$$



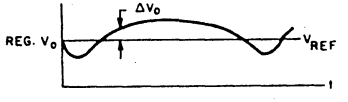
(a) SELF-OSCILLATING SWITCHING REGULATOR



(b) VOLTAGE AT POINT V_X



(c) INDUCTOR CURRENT I_{LI}



(d) OUTPUT VOLTAGE

FIGURE 17. SWITCHING REGULATOR AND ASSOCIATED WAVEFORMS

Where V is the voltage across the inductance L1. The current through the inductance charges the capacitor C1 and supplies current to the load. The output voltage rises until it slightly exceeds the reference voltage V_{ref}. At this point the op-amp removes base drive to Q1 and the unregulated input voltage V1 is "switched off". The energy stored in the inductor L1 now causes the voltage at V_x to swing in the negative direction and current flows through diode D1, while continuing to supply current into the load R_L. As the current in the inductor falls below the load current, the capacitor C1 begins to discharge and V_O decreases. When V_O falls slightly below the value of V_{ref}, the op-amp turns on Q1 and the cycle is repeated. It should be apparent that the output voltage oscillates about V_{ref} with an amplitude determined by R1 and R2. Actually, the value of V_{ref} varies from being slightly more positive than V_{ref} when Q1 is conducting, to being slightly more negative than V_{ref} when D1 is conducting. The voltage and current waveforms are shown in Figure 17(b), (c), and (d).

Design Example

The following specifications are used in decomputations for a switching regulator:

$V_I = 30V$, $V_O = 5V$, $I_O = 500mA$,
switching frequency = 20kHz,
output ripple = 100mV

If it is assumed that transistor Q1 is in steady-state saturated operation with a low voltage-drop, the current in the inductor is given by Eq.10, as follows:

$$i_L = \frac{1}{L}\int_{t_o}^{t_1} V dt = \left(\frac{V_I - V_O}{L_1}\right) t_{on} \qquad (11)$$

When transistor Q1 is off, the current in the inductor is given by:

$$i_L \cong \frac{(V_O + V_{D1})\, t_{off}}{L1} \qquad (12)$$

From Eq. 11,

$$L_1 = \frac{(V_I - V_O)}{i_L} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \qquad (13)$$

If i_{max} is 1.3 I_L, then during t_{on} the current in the inductor (i_L) will be 0.5A x 1.3 = 0.65A; therefore, $\Delta i_L = 0.15A$.

Substitution in Eq. 13 yields

$$L_1 = \frac{(30 - 5)}{0.15} \cdot \frac{1}{(20 \times 10^3)} \cdot \frac{5}{30} \cdot \quad 1.4\ mH \qquad (14)$$

Current discharge from the capacitor C1 is given by:

$$i_C = C\frac{dv}{dt}$$

$$\text{Thus, } \Delta i_c = C\frac{\Delta v}{\Delta t} \quad \text{or } C = \frac{\Delta i_C\, \Delta t}{\Delta v}$$

Since $i_c = i_L$ and $\Delta t = t_{off}$, then

$$C = \frac{\Delta i_L \, t_{off}}{\Delta v} \quad (15)$$

Substitution for the value of iL from Eq. 13 yields

$$C = \frac{\left(\frac{V_I - V_O}{L1}\right) \cdot \frac{1}{f} \cdot \left(\frac{V_O}{V_I}\right) \cdot t_{off}}{\Delta v} \quad (16)$$

The total period $T = t_{off} + t_{on}$, and $T = \frac{1}{f}$ Therefore,

$$t_{off} = \frac{1}{f} - t_{on} \quad (17)$$

For optimum efficiency t_{on} should be

$$\cong \left(\frac{V_O}{V_I}\right) T \cong \left(\frac{V_O}{V_I}\right) \frac{1}{f} \quad (18)$$

Substitution for t_{on} in Eq. 18 yields

$$t_{off} = \frac{1}{f} - \left(\frac{V_O}{V_I}\right) \frac{1}{f} = \frac{1}{f}\left(1 - \frac{V_O}{V_I}\right) \quad (19)$$

Substitution for t_{on} in Eq. 16 yields

$$C = \frac{\frac{(V_I \cdot V_O)}{L_1} \cdot \frac{1}{f} \cdot \frac{V_O}{V_I} \cdot \frac{1}{f} \cdot \left(1 - \frac{V_O}{V_I}\right)}{\Delta v} \quad (20)$$

Substitution of numerical values in Eq. 20 produces the following value for C:

$$C = \frac{\frac{30-5}{1.4 \times 10^{-3}} \cdot \frac{1}{20 \times 10^{3}} \cdot \frac{5}{30} \cdot \frac{1}{20 \times 10^{3}} \cdot \left(1 - \frac{5}{30}\right)}{10^{-1}} = 63\mu F$$

A switching-regulator circuit using the CA3085 is shown in Figure 18. The values of L and C (1.5 millihenries and 50 microfarads, respectively) are commercially available components having values approximately equal to the computed values in the previous design example.

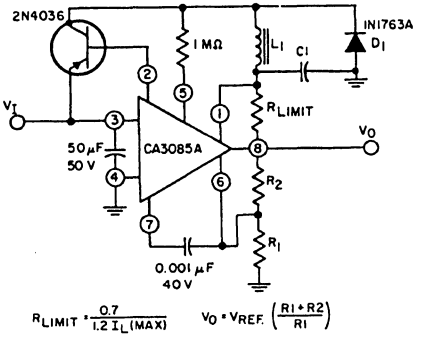
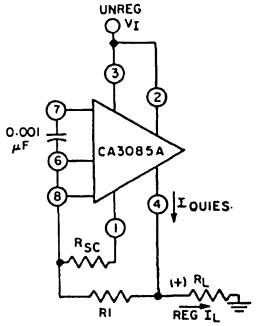


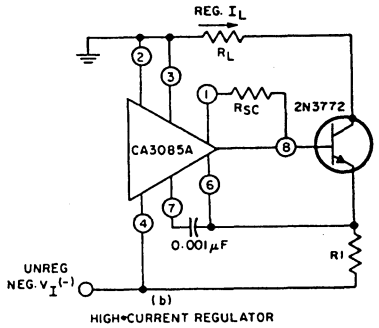
FIGURE 18. TYPICAL SWITCHING REGULATOR CIRCUIT

Current Regulators

The CA3085 series of voltage regulators can be used to provide a constant source or sink current. A regulated-current supply capable of delivering up to 100 milliamperes is shown in Figure 19(a). The regulated load current is controlled by R1 because the current flowing through this resistor must establish a voltage difference between terminals 6 and 4 that is equal to the internal reference voltage developed between terminals 5 and 4.



(a) CURRENT REGULATOR



(b) HIGH-CURRENT REGULATOR

FIGURE 19. CONSTANT CURRENT REGULATORS

The actual regulated current, reg I_L is the sum of the quiescent regulator current and the current through R1, i.e.,

$$\text{reg } I_L = I_{quiescent} + I_{R1}$$

Figure 19(b) shows a high-current regulator using the CA3085 in conjunction with an external n-p-n transistor to regulate currents up to 3 amperes. In this circuit the quiescent regulator current does not flow through the load and the output current can be directly programmed by R1, i.e.,

$$\text{Reg } I_L = \frac{V_{ref}}{R1}$$

With this regulator currents between 1 milliampere and 3 amperes can be programmed directly. At currents below 1 milliampere inaccuracies may occur as a result of leakage in the external transistor.

A Dual-Tracking Voltage Regulator

A dual-tracking voltage regulator using a CA3085 and a CA3094A* is shown in Figure 20. The CA3094A is basically an op amp capable of supplying 100 milliamperes of output current

The positive output voltage is regulated by a CA3085 operating in a configuration essentially similar to that described in connection with Figure 3. Resistor R is used as a vernier adjustment of output voltage. The negative output voltage is regulated by the CA3094A, which is "slaved" to the regulated positive voltage supplied by the CA3085. It should be noted that the non-inverting input of the CA3094A and the negative supply terminal of the CA3085 are connected to a common ground reference. The "slaving" potential for the CA3094A is derived from an accurate 1:1 voltage-divider network comprised of two 10-kilohm resistors connected between the +15 volt and the -15 volt output terminals. The junction of these two resistors is connected to the inverting input of the CA3094A. The voltage at this junction is compared with the voltage at the non-inverting input, and the CA3094A then automatically adjusts the output current at the negative terminal to maintain a negative regulated output voltage essentially equal to the regulated positive output voltage. Typical performance data for this circuit are shown in Figure 20.

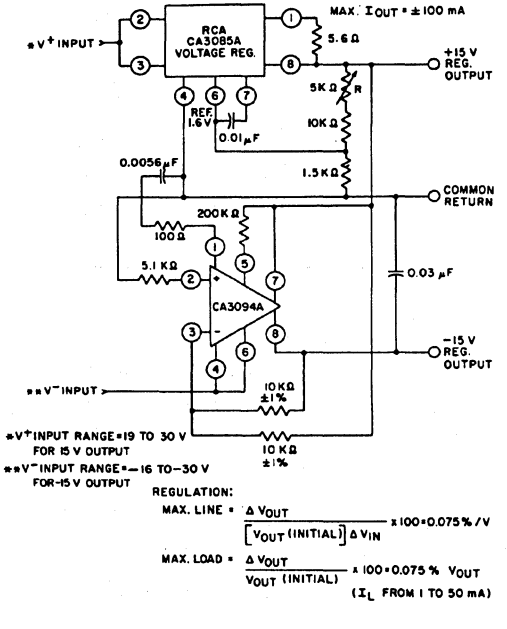
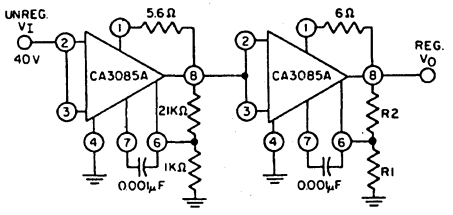


FIGURE 20. DUAL-VOLTAGE TRACKING REGULATOR

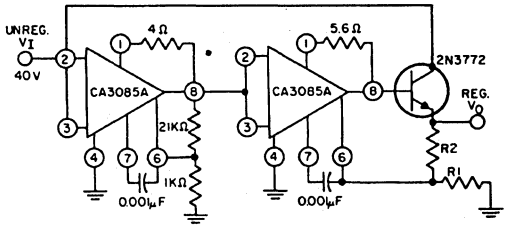
The basic circuit of Figure 20 can be modified to regulate dissimilar positive and negative voltages (e.g., +15V, -5V) by appropriate selection of resistor ratios in the voltage-divider network discussed previously. As an example, to provide tracking of the -15V and -5V regulated voltages with the circuit of Figure 20, it is only necessary to replace the 10-kilohm resistor connected between terminals 3 and 8 of the CA3094A with a 3.3-kilohm resistor.

Regulators With High Ripple Rejection

When the reference-voltage source in the CA3085 is adequately filtered, the typical ripple rejection provided by the circuit is 56dB. It is possible to achieve higher ripple-rejection performance by cascading two stages of the CA3085, as shown in Figure 21. The voltage-regulator circuit in Figure 21(a) provides 90dB of ripple rejection. The output voltage is adjustable over the range from 1.8 to 30 volts by appropriate adjustment of resistors R1 and R2. Higher regulated output currents up to 1 ampere can be obtained with this circuit by adding an external n-p-n transistor as shown in Figure 21(b).



(a) VOLTAGE REGULATOR WITH HIGH RIPPLE REJECTION



(b) HIGH-CURRENT VOLTAGE REGULATOR WITH HIGH RIPPLE REJECTION

FIGURE 21. REGULATORS WITH HIGH RIPPLE REJECTION

The CA3085 As A Power Source For Sensors

Certain types of sensor applications require a regulated power source. Additionally, low-impedance sensors can consume significant power. An example of a circuit with these requirements, in which a CA3085 provides regulated power for a low-impedance sensor and the CA3059* zero-voltage switch, is shown in Figure 22. Terminal 12 on the CA3059 provides the ac trigger-signal which actuates the zero-voltage switch synchronously with the power line to control the load-switching triac.

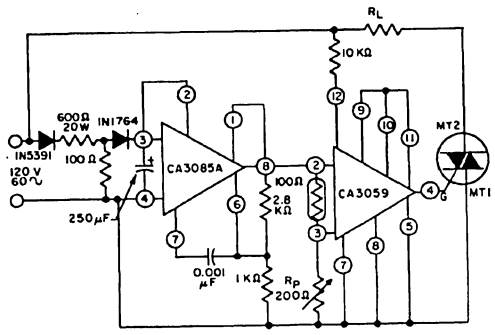


FIGURE 22. VOLTAGE REGULATOR FOR SENSOR AND ZERO-VOLTAGE SWITCH

The CA3085 As A General-Purpose Amplifier

As described above, the CA3085 series regulators contain a high-gain linear amplifier having a current-output capability up to 100 milliamperes. The premium type (CA3085B) can operate at supply voltages up to 50 volts. When equipped with an appropriate radiator or heat sink, the TO-5 package of these devices can dissipate up to 1.6 watts at 55°C. A very stable internal voltage-reference source is used to bias the high-gain amplifier and/or provide an external voltage-reference despite extreme temperature or supply-voltage variations. These factors, plus economics, prompt consideration of this circuit for general-purpose uses, such as amplifiers, relay controls, signal-lamp controls, and thyristor firing.

As an example, Figure 23 shows the application of the CA3085 in a general-purpose amplifier. Under the conditions shown, the circuit has a typical gain of 70bB with a flat response to at least 100kHz without the RC network connected between terminals 6 and 7. The RC network is useful as a tone control or to "roll-off" the amplifier response for other reasons. Current limiting is not used in this circuit. The network connected between terminals 8 and 6 provides both dc and ac feedback. This circuit is also applicable for directly driving an external discrete n-p-n power transistor.

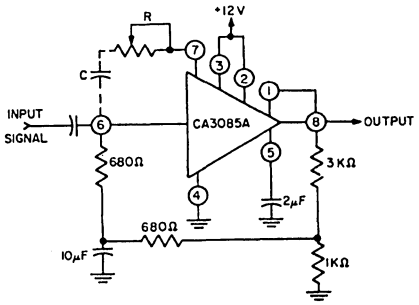


FIGURE 23. GENERAL-PURPOSE AMPLIFIER USING CA3085A

Harris Semiconductor

APPNOTE

No. 6182 May 1992

Harris Intelligent Power

FEATURES AND APPLICATIONS OF INTEGRATED CIRCUIT ZERO-VOLTAGE SWITCHES (CA3058, CA3059, AND CA3079)

Authors: A.C.N. Sheng, G.J. Granieri, J. Yellin, and T. McNulty

CA3058, CA3059 and CA3079 zero-voltage switches are monolithic integrated circuits designed primarily for use as trigger circuits for thyristors in many highly diverse AC power control and power switching applications. These integrated circuit switches operate from an AC input voltage of 24, 120, 208 to 230, or 277V at 50, 60, or 400Hz.

The CA3059 and CA3079 are supplied in a 14 terminal dual-in-line plastic package. The CA3058 is supplied in a 14 terminal dual-in-line ceramic package.

Zero-voltage switches (ZVS) are particularly well suited for use as thyristor trigger circuits. These switches trigger the thyristors at zero-voltage points in the supply voltage cycle. Consequently, transient load current surges and radio frequency interference (RFI) are substantially reduced. In addition, use of the zero-voltage switches also reduces the rate of change of on state current (di/dt) in the thyristor being triggered, an important consideration in the operation of thyristors. These switches can be adapted for use in a variety of control functions by use of an internal differential comparator to detect the difference between two externally developed voltages. In addition, the availability of numerous terminal connections to internal circuit points greatly increases circuit flexibility and further expands the types of AC power control applications to which these integrated circuits may be adapted. The excellent versatility of the zero-voltage switches is demonstrated by the fact that these circuits have been used to provide transient free temperature control in self cleaning ovens, to control gun muzzle temperature in low temperature environments, to provide sequential switching of heating elements in warm air furnaces, to switch traffic signal lights at street intersections, and to effect other widely different AC power control functions.

Functional Description

Zero-voltage switches are multistage circuits that employ a diode limiter, a zero crossing (threshold) detector, an on/off sensing amplifier (differential comparator), and a Darlington output driver (thyristor gating circuit) to provide the basic switching action. The DC operating voltages for these stages is provided by an internal power supply that has sufficient current capability to drive external circuit elements, such as transistors and other integrated circuits. An important feature of the zero-voltage switches is that the output trigger pulses can be applied directly to the gate of a triac or a silicon controlled rectifier (SCR). The CA3058 and CA3059 also feature an interlock (protection) circuit that inhibits the application of these pulses to the thyristor in the event that the external sensor should be inadvertently opened or shorted. An external inhibit connection (terminal No. 1) is also available so that an external signal can be used to inhibit the output drive. This feature is not included in the CA3079; otherwise, the three integrated circuit zero-voltage switches are electrically identical.

Overall Circuit Operation

Figure 1 shows the functional interrelation of the zero-voltage switch, the external sensor, the thyristor being triggered, and the load elements in an on/off type of AC power control system. As shown, each of the zero-voltage switches incorporates four functional blocks as follows:

Limiter Power Supply - Permits operation directly from an AC line.

Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional control capability may easily be implemented in this section.

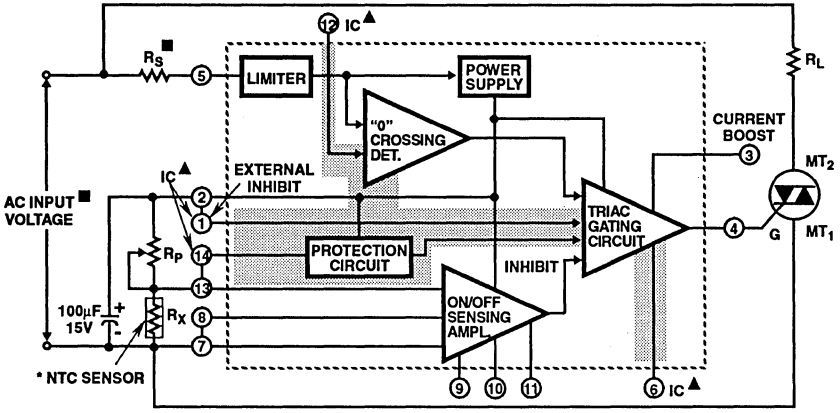
Zero Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at a zero-voltage point and thereby eliminates radio frequency interference (RFI) when used with resistive loads.

Triac Gating Circuit - Provides high current pulses to the gate of the power controlling thyristor.

In addition, the CA3058 and CA3059 provide the following important auxiliary functions (shown in Figure 1):

1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to terminal 1.
3. High power DC comparator operation is provided by overriding the action of the zero crossing detector. This override is accomplished by connecting terminal 12 to terminal 7. Gate current to the thyristor is continuous when terminal 13 is positive with respect to terminal 9.

Figure 2 shows the detailed circuit diagram for the integrated circuit zero-voltage switches. (The diagrams shown in Figures 1 and 2 are representative of all three zero-voltage switches, i.e., the CA3058, CA3059, and CA3079; the shaded areas indicate the circuitry that is not included in the CA3079.)



* NEGATIVE TEMPERATURE COEFFICIENT

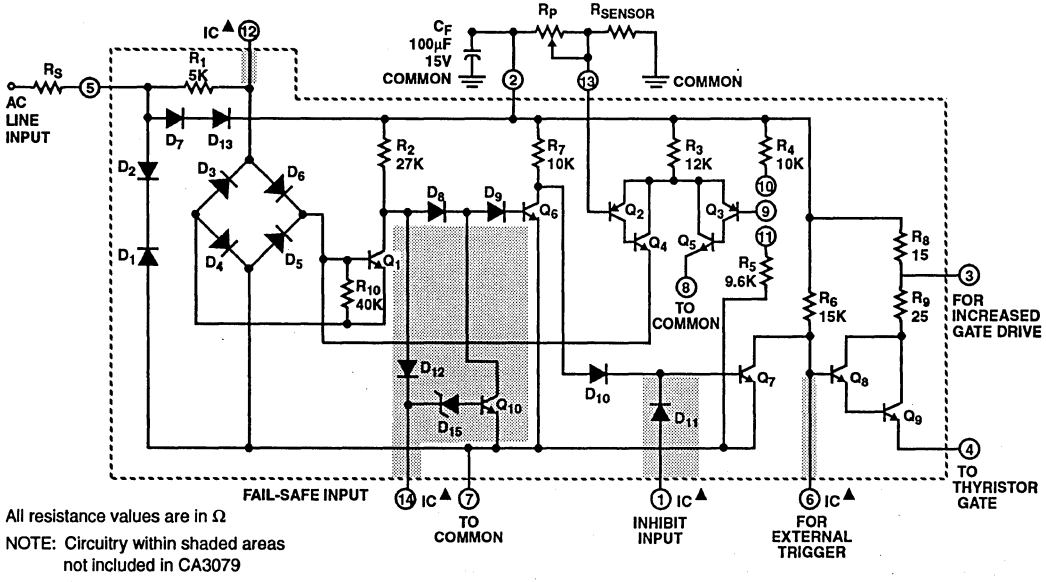
AC INPUT VOLTAGE (50/60 OR 400Hz) V AC	INPUT SERIES RESISTOR (R_S) kΩ	DISSIPATION RATING FOR R_S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE: Circuitry within shaded areas, not included in CA3079 (Terminal restriction applies only to CA3079)

■ See chart

▲ IC = Internal connection - DO NOT USE

FIGURE 1. FUNCTIONAL BLOCK DIAGRAMS OF THE ZERO-VOLTAGE SWITCHES CA3058, CA3059, AND CA3079



All resistance values are in Ω

NOTE: Circuitry within shaded areas not included in CA3079

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)

FIGURE 2. SCHEMATIC DIAGRAM OF ZERO-VOLTAGE SWITCHES CA3058, CA3059 AND CA3079

The limiter stage of the zero-voltage switch clips the incoming AC line voltage to approximately ±8V. This signal is then applied to the zero-voltage crossing detector, which generates an output pulse each time the line voltage passes through zero. The limiter output is also applied to a rectifying diode and an external capacitor, C_F, that comprise the DC power supply. The power supply provides approximately 6V as the V_{CC} supply to the other stages of the zero-voltage switch. The on/off sensing amplifier is basically a differential comparator. The thyristor gating circuit contains a driver for direct triac triggering. The gating circuit is enabled when all the inputs are at a "high" voltage, i.e., the line voltage must be approximately zero volts, the sensing amplifier output must be "high", the external voltage to terminal 1 must e a logical "0", and, for the CA3058 and CA3059, the output of the fail-safe circuit must be "high". Under these conditions, the thyristor (triac or SCR) is triggered when the line voltage is essentially zero volts.

Thyristor Triggering Circuits

The diodes D_1 and D_2 in Figure 2 form a symmetrical clamp that limits the voltages on the chip to ±8V; the diodes D_7 and D_{13} form a half-wave rectifier that develops a positive voltage on the external storage capacitor, C_F.

The output pulses used to trigger the power switching thyristor are actually developed by the zero crossing detector and the thyristor gating circuit. The zero crossing detector consists of diodes D_2 and through D_6, transistor Q_1, and the associated resistors shown in Figure 2. Transistors Q_1 and Q_6 through Q_9 and the associated resistors comprise the thyristor gating circuit and output driver. These circuits generate the output pulses when the AC input is at a zero-voltage point so that RFI is virtually eliminated when the zero-voltage switch and thyristor are used with resistive loads.

The operation of the zero crossing detector and thyristor gating circuit can be explained more easily if the on state (i.e., the operating state in which current is being delivered to the thyristor gate through terminal 4) is considered as the operating condition of the gating circuit. Other circuit elements in the zero-voltage switch inhibit the gating circuit unless certain conditions are met, as explained later.

In the on state of the thyristor gating circuit, transistors Q_8 and Q_9 are conducting, transistor Q_7 is off, and transistor Q_6 is on. Any action that turns on transistor Q_7 removes the drive from transistor Q_8 and thereby turns off the thyristor. Transistor Q_7 may be turned on directly by application of a minimum of ±1.2V at 10μA to the external inhibit input, terminal 1. (If a voltage of more than 1.5V is available, an external resistance must be added in series with terminal 1 to limit the current to 1 milliampere.) Diode D_{10} isolates the base of transistor Q_7 from other signals when an external inhibit signal is applied so that this signal is the highest priority command for normal operation. (Although grounding of terminal 6 creates a higher priority inhibit function, this level is not compatible with normal DTL or TTL logic levels.) Transistor Q_7 may also be activated by turning off transistor Q_6 to allow current flow from the power supply through resistor R_7 and diode D_{10} into the base of Q_7. Transistor Q_6 is normally maintained in conduction by current that flows into its base through resistor R_2 and diodes D_8 and D_9 when transistor Q_1 is off.

Transistor Q_1 is a portion of the zero crossing detector. When the voltage at terminal 5 is greater than +3V, current can flow through resistor R_1, diode D_6, the base-to-emitter junction of transistor Q_1, and diode D_4 to terminal 7 to turn on Q_1. This action inhibits the delivery of a gate-drive output signal at terminal 4. For negative voltages at terminal 5 that have magnitudes greater than 3V, the current flows through diode D_5, the emitter-to-base junction of transistor Q_1, diode D_3, and resistor R_1, and again turns on transistor Q_1. Transistor Q_1 is off only when the voltage at terminal 5 is less than the threshold voltage of approximately ±2V. When the integrated circuit zero-voltage switch is connected as shown in Figure 2, therefore, the output is a narrow pulse which is approximately centered about the zero-voltage time in the cycle, as shown in Figure 3. In some applications, however, particularly those that use either slightly inductive or low power loads, the thyristor load current does not reach the latching current value* by the end of this pulse. An external capacitor C_X connected between terminal 5 and 7, as shown in Figure 4, can be used to delay the pule to accommodate such loads. The amount of pulse stretching and delay is shown in Figures 5(a) and 5(b).

* The latching current is the minimum current required to sustain conduction immediately after the thyristor is switched from the off to the on state and the gate signal is removed.

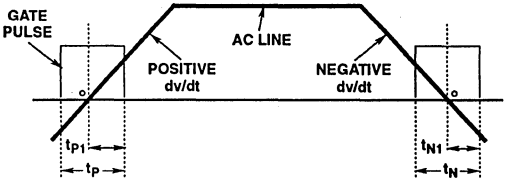


FIGURE 3. WAVEFORM SHOWING OUTPUT PULSE DURATION OF THE ZERO-VOLTAGE SWITCH.

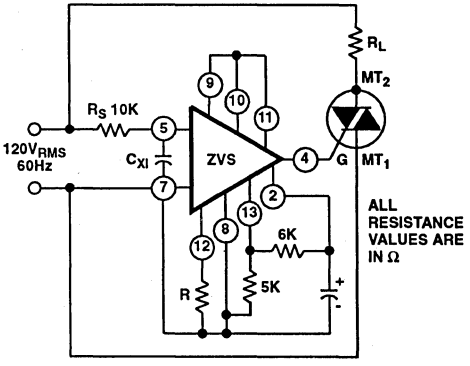
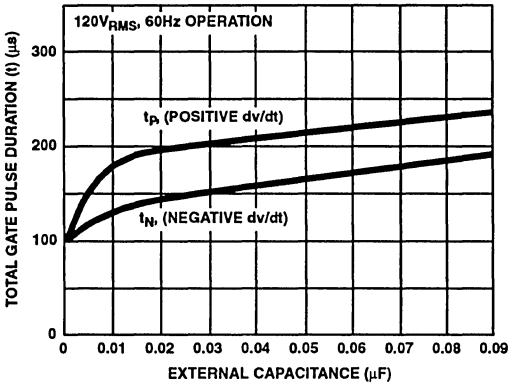
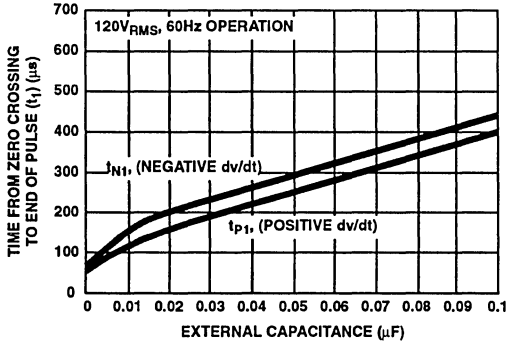


FIGURE 4. USE OF A CAPACITOR BETWEEN TERMINALS 5 AND 7 TO DELAY THE OUTPUT PULSE OF THE ZERO-VOLTAGE SWITCH



(a)

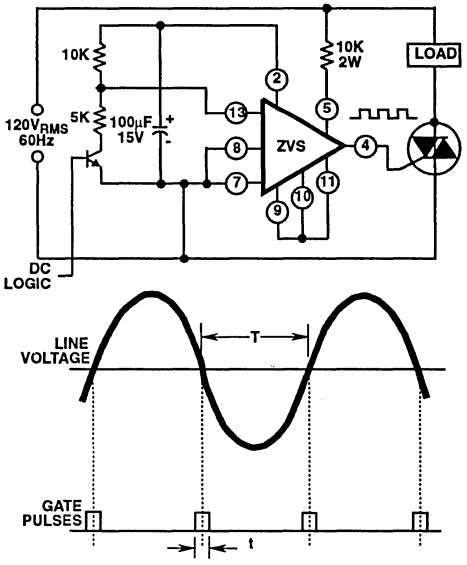


(b)

FIGURE 5. CURVES SHOWING EFFECT OF EXTERNAL CAPACITANCE ON (a) THE TOTAL OUTPUT PULSE DURATION, AND (b) THE TIME FROM ZERO CROSSING TO THE END OF THE PULSE

Continuous gate current can be obtained if terminal 12 is connected to terminal 7 to disable the zero crossing detector. In this mode, transistor Q_1 is always off. This mode of operation is useful when comparator operation is desired or when inductive loads must be switched. (If the capacitance in the load circuit is low, most RFI is eliminated.) Care must be taken to avoid overloading of the internal power supply in this mode. A sensitive gate thyristor should be used, and a resistor should be placed between terminal 4 and the gate of the thyristor to limit the current, as pointed out later under **Special Application Considerations.**

Figure 6 indicates the timing relationship between the line voltage and the zero-voltage switch output pulses. At 60Hz, the pulse is typically 100µs wide; at 400Hz, the pulse width is typically 12µs. In the basic circuit shown, when the DC logic signal is "high", the output is disabled; when it is "low", the gate pulses are enabled.



FREQ. (Hz)	T (ms)	t (µs)
60	8.3	100
400	1.25	12

FIGURE 6. TIMING RELATIONSHIP BETWEEN THE OUTPUT PULSES OF THE ZERO-VOLTAGE SWITCH AND THE AC LINE VOLTAGE

On/Off Sensing Amplifier

The discussion thus far has considered only cases in which pulses are present all the time or not at all. The differential sense amplifier consisting of transistors Q_2, Q_3, Q_4, and Q_5 (shown in Figure 2) makes the zero-voltage switch a flexible power control circuit. The transistor pairs Q_2-Q_4 and Q_3-Q_5 form a high beta composite p-n-p transistors in which the emitters of transistors Q_4 and Q_5 act as the collectors of the composite devices. These two composite transistors are connected as a differential amplifier with resistor R_3 acting as a constant current source. The relative current flow in the two "collectors" is a function of the difference in voltage between the bases of transistors Q_2 and Q_3. Therefore, when terminal 13 is more positive than terminal 9, little or no current flows in the "collector" of the transistor pair Q_2-Q_4. When terminal 13 is negative with respect to terminal 9, most of the current flows through that path, and none in terminal 8. When current flows in the transistor pair Q_2-Q_4, through the base emitter junction of transistor Q_1, and finally through the diode D_4 to terminal 7. Therefore, when V_{13} is equal to or more negative than V_9, transistor Q_1 is on, and the output is inhibited.

In the circuit shown in Figure 1, the voltage at terminal 9 is derived from the supply by connection of terminals 10 and 11 to form a precision voltage divider. This divider forms one side of a transducer bridge, and the potentiometer R_P and the negative temperature coefficient (NTC) sensor form the other side. At

low temperatures, the high resistance of the sensor causes terminal 13 to be positive with respect to terminal 9 so that the thyristor fires on every half cycle, and power is applied to the load. As the temperature increases, the sensor resistance decreases until a balance is reached, and V_{13} approaches V_9. At this point, the transistor pair Q_2-Q_4 turns on and inhibits any further pulses. The controlled temperature is adjusted by variation of the value of the potentiometer R_P. For cooling service, either the positions of R_P and the sensor may be reversed or terminals 9 and 13 may be interchanged.

The low bias current of the sensing amplifier permits operation with sensor impedances of up to 0.1MΩ at balance without introduction of substantial error (i.e., greater than 5 percent). The error may be reduced if the internal bridge elements, resistors R_4 and R_5, are not used, but are replaced with resistances which equal the sensor impedance. The minimum value of sensor impedance is restricted by the current drain on the internal power supply. Operation of the zero-voltage switch with low impedance sensors is discussed later under Special Application Considerations. The voltage applied to terminal 13 must be greater than 1.8V at all times to assure proper operation.

Protection Circuit

A special feature of the CA3058 and CA3059 zero-voltage switches is the inclusion of an interlock type of circuit. This circuit removes power from the load by interrupting the thyristor gate drive if the sensor either shorts or opens. However, use of this circuit places certain constraints upon the user. Specifically, effective protection circuit operation is dependent upon the following conditions:

1. The circuit configuration of Figure 1 is used, with an internal supply, no external load on the supply, and terminal 14 connected to terminal 13.
2. The value of potentiometer R_P and of the sensor resistance must be between 2000Ω and 0.1MΩ.
3. The ratio of sensor resistance and R_P must be greater than 0.33 and less than 3.0 for all normal conditions. (If either of these ratios is not met with an unmodified sensor, a series resistor or a shunt resistor must be added to avoid undesired activation of the circuit.)

The protective feature may be applied to other systems when operation of the circuit is understood. The protection circuit consists of diodes D_{12} and D_{15} and transistor Q_{10}. Diode D_1 activates the protection circuit if the sensor shown in Figure 1 shorts or its resistance drops too low in value, as follows: Transistor Q_6 is on during an output pulse so that the junction of diodes D_8 and D_{12} is 3 diode drops (approximately 2V) above terminal 7. As long as V_{14} is more positive or only 0.15 volt negative with respect to that point, diode D_{12} does not conduct, and the circuit operates normally. If the voltage at terminal 14 drops to 1 volt, the anode of diode D_8 can have a potential of only 1.6 to 1.7V, and current does not flow through diodes D_8 and D_9 and transistor Q_6. The thyristor then turns off.

The actual threshold is approximately 1.2V at room temperature, but decreases 4μV per degree C at higher temperatures. As the sensor resistance increases, the voltage at terminal 14 rises toward the supply voltage. At a voltage of approximately 6V, the zener diode D_{15} breaks down and turns on transistor Q_{10}, which then turns off transistor Q_6 and the thyristor. If the supply voltage is not at least 0.2 volt more positive than the breakdown voltage of diode D_{15}, activation of the protection circuit is not possible. For this reason, loading the internal supply may cause this circuit to malfunction, a may selection of the wrong external supply voltage. Figure 7 shows a guide for the proper operation of the protection circuit when an external supply is used with a typical integrated circuit zero-voltage switch.

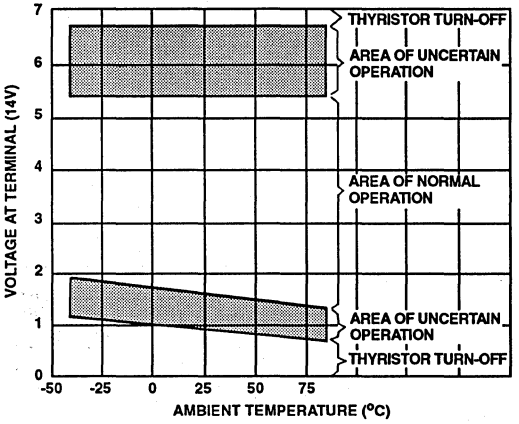


FIGURE 7. OPERATING REGIONS FOR BUILT-IN PROTECTION CIRCUITS OF A TYPICAL ZERO-VOLTAGE SWITCH.

Special Application Considerations

As pointed out previously, the Harris integrated circuit zero-voltage switches (CA3058, CA3059 and CA3079) are exceptionally versatile units than can be adapted for use in a wide variety of power control applications. Full advantage of this versatility can be realized, however, only if the user has a basic understanding of several fundamental considerations that apply to certain types of applications of the zero-voltage switches.

Operating Power Options

Power to the zero-voltage switch may be derived directly from the AC line, as shown in Figure 1, or from an external DC power supply connected between terminals 2 and 7, as shown in Figure 8. When the zero-voltage switch is operated directly from the AC line, a dropping resistor R_S of 5,000Ω to 10,000Ω must be connected in series with terminal 5 to limit the current in the switch circuit. The optimum value for this resistor is a function of the average current drawn from the internal DC power supply, either by external circuit elements or by the thyristor trigger circuits, as shown in Figure 9. The chart shown in Figure 1 indicates the value and dissipation rating of the resistor R_S for AC line voltages 24, 120, 208 to 230, and 277V.

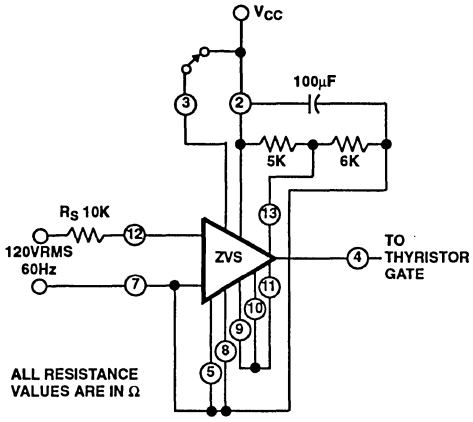


FIGURE 8. OPERATION OF THE ZERO-VOLTAGE SWITCH FROM AN EXTERNAL DC POWER SUPPLY CONNECTED BETWEEN TERMINALS 2 AND 7.

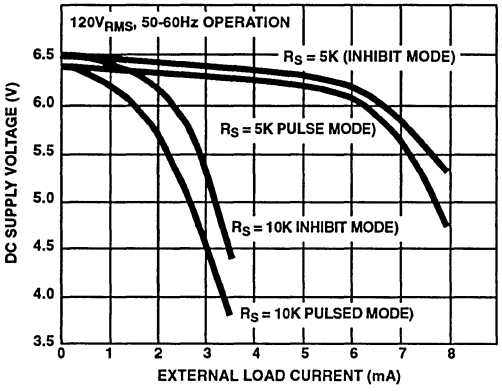


FIGURE 9. DC SUPPLY VOLTAGE AS A FUNCTION OF EXTERNAL LOAD CURRENT FOR SEVERAL VALUES

Half Cycling Effect

The method by which the zero-voltage switch senses the zero crossing of the AC power results in a half cycling phenomenon at the control point. Figure 10 illustrates this phenomenon. The zero-voltage switch senses the zero-voltage crossing every half cycle, and an output, for example pulse No. 4, is produced to indicate the zero crossing. During the remaining 8.3ms, however, the differential amplifier in the zero-voltage switch may change state and inhibit any further output pulses. The uncertainty region of the differential amplifier, therefore, prevents pulse No. 5 from triggering the triac during the negative excursion of the AC line voltage.

When a sensor with low sensitivity is used in the circuit, the zero-voltage switch is very likely to operate in the linear mode. In this mode, the output trigger current may be sufficient to trigger the triac on the positive going cycle, but insufficient to trigger the device on the negative going cycle of the triac supply voltage. This effect introduces a half cycling phenomenon, i.e., the triac is turned on during the positive half cycle and turned off during the negative half cycle.

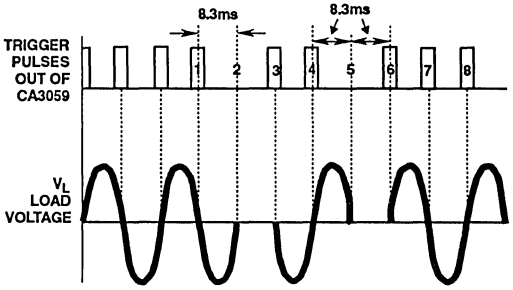
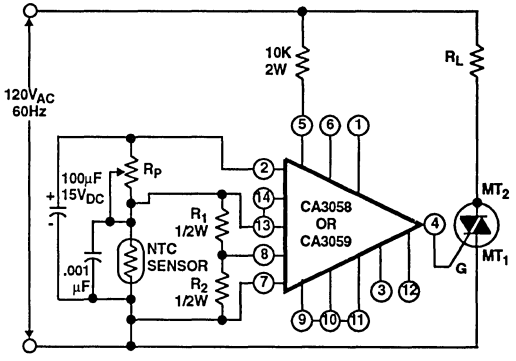


FIGURE 10. HALF CYCLING PHENOMENON IN THE ZERO-VOLTAGE SWITCH

Several techniques may be used to cope with the half cycling phenomenon. If the user can tolerate some hysteresis in the control, then positive feedback can be added around the differential amplifier. Figure 11 illustrates this technique. The tabular data in the figure lists the recommended values of resistors R1 and R2 for different sensor impedances at the control point.



THERMISTOR →

NTC	R1	R2
5K	12K	12K
12K	68K	12K
100K	200K	18K

FIGURE 11. CA3058 OR CA3059 ON-OFF CONTROLLER WITH HYSTERESIS

If a significant amount (greater than ±10%) of controlled hysteresis is required, then the circuit shown in Figure 12 may be employed. In this configuration, external transistor Q_1 can be used to provide an auxiliary timed delay function.

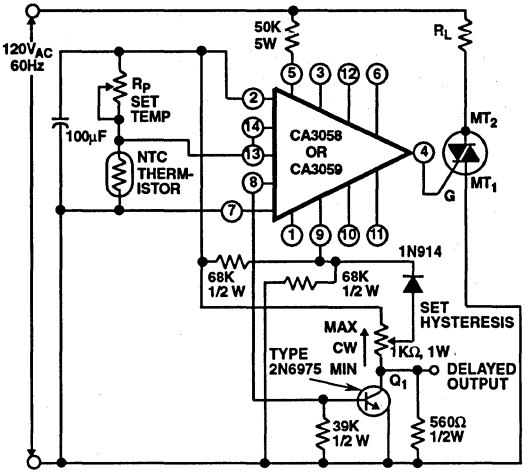


FIGURE 12. CA3058 OR CA3059 ON/OFF CONTROLLER WITH CONTROLLED HYSTERESIS

For applications that require complete elimination of half cycling without the addition of hysteresis, the circuit shown in Figure 13 may be employed. This circuit uses a CA3098E integrated circuit programmable comparator with a zero-voltage switch. A block diagram of CA3098E is shown in Figure 14. Because the CA3098E contains an integral flip-flop, its output will be in either a "0" or "1" state. Consequently the zero-voltage switch cannot operate in the linear mode, and spurious half cycling operation is prevented. When the signal input voltage at terminal 8 of the CA3098E is equal to or less than the "low" reference voltage (LR), current flows from the power supply through resistor R_1 and R_2, and a logic "0" is applied to terminal 13 of the zero-voltage switch. This condition turns off the triac. The triac remains off until the signal input voltage rises to or exceeds the "high" reference voltage (HR), thereby effecting a change in the state of the flip-flop so that a logic "1" is applied to terminal 13 of the zero-voltage switch, and triggers the triac on.

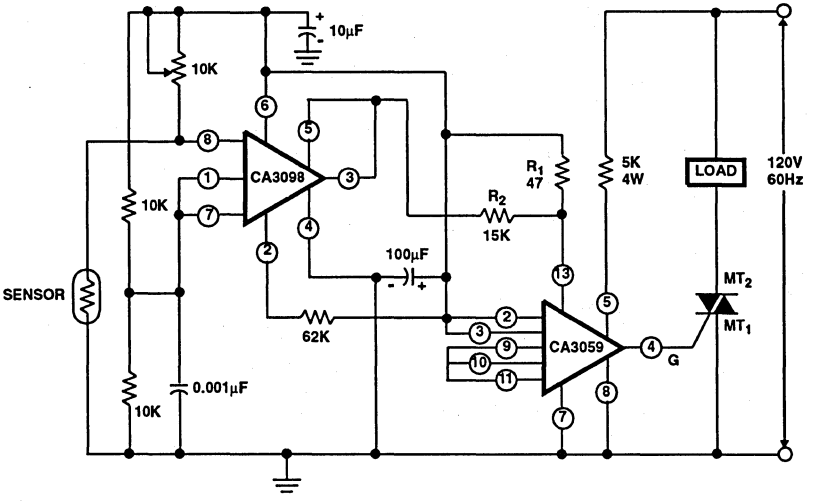


FIGURE 13. SENSITIVE TEMPERATURE CONTROL

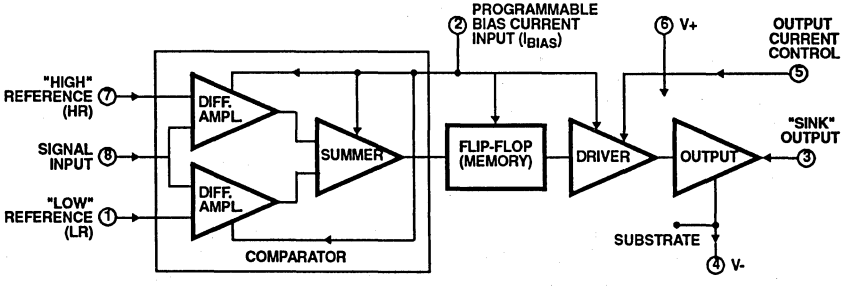
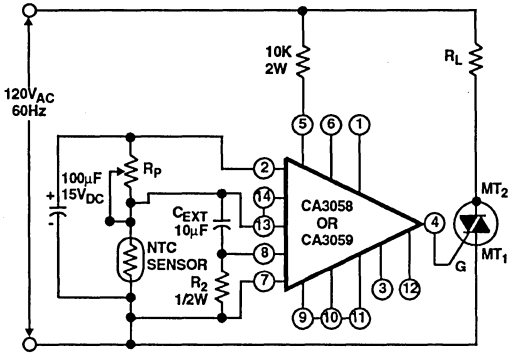


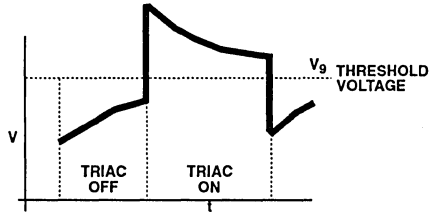
FIGURE 14. BLOCK DIAGRAM OF CA3098 PROGRAMMABLE SCHMITT TRIGGER

"Proportional Control" Systems

The on/off nature of the control shown in Figure 1 causes some overshoot that leads to a definite steady state error. The addition of hysteresis adds further to this error factor. However, the connections shown in Figure 15(a) can be used to add proportional control to the system. In this circuit, the sense amplifier is connected as a free running multivibrator. At balance, the voltage at terminal 13 is much less than the voltage at terminal 9. The output will be inhibited at all times until the voltage at terminal 13 rises to the design differential voltage between terminals 13 and 9; then proportional control resumes. The voltage at terminal 13 is as shown in Figure 15(b). When this voltage is more positive than the threshold, power is applied to the load so that the duty cycle is approximately 50 percent. With a 0.1MΩ sensor and values of R_P = 01.MΩ, R_2 = 10,000Ω, and C_{EXT} = 10μF, a period greater than 3 seconds is achieved. This period should be much shorter than the thermal time constant of the system. A change in the value of any of these elements changes the period, as shown in Figure 16. As the resistance of the sensor changes, the voltage on terminal 13 moves relative to V_9. A cooling sensor moves V_{13} in a positive direction. The triac is on for a larger portion of the pulse cycle and increases the average power to the load.



(a)



(b)

FIGURE 15. USE OF THE CA3058 OR CA3059 IN A TYPICAL HEATING CONTROL WITH PROPORTIONAL CONTROL: (a) SCHEMATIC DIAGRAM, AND (b) WAVEFORM OF VOLTAGE AT ERMINAL 13

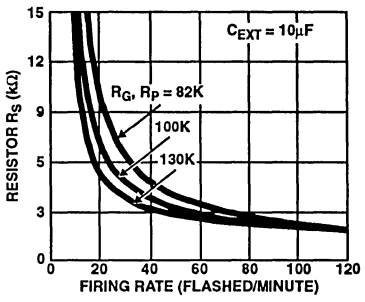


FIGURE 16. EFFECT OF VARIATIONS IN TIME CONSTANT ELEMENTS ON PERIOD

As in the case of the hysteresis circuitry described earlier, some special applications may require more sophisticated systems to achieve either very precise regions of control or very long periods.

Zero-voltage switching control can be extended to applications in which it is desirable to have constant control of the temperature and a minimization of system hysteresis. A closed loop top burner control in which the temperature of the cooking utensil is sensed and maintained at a particular value is a good example of such an application; the circuit for this control is shown in Figure 17. In this circuit, a unijunction oscillator is outboarded from the basic control by means of the internal power supply of the zero-voltage switch. The output of this ramp generator is applied to terminal 9 of the zero-voltage switch and establishes a varied reference to the differential amplifier. Therefore, gate pulses are applied to the triac whenever the voltage at terminal 13 is greater than the voltage at terminal 9. A varying duty cycle is established in which the load is predominantly on with a cold sensor and predominantly off with a hot sensor. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system but longer than the period of the 60Hz line. Figure 18, which contains various waveforms for the system of Figure 17, indicates that a typical variance of ±0.5°C might be expected at the sensor contact to the utensil. Overshoot of the set temperature is minimized with approach, and scorching of any type is minimized.

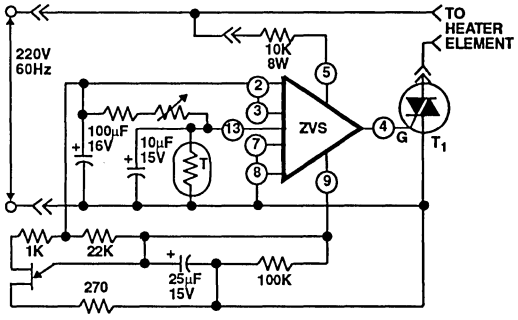


FIGURE 17. SCHEMATIC DIAGRAM OF PROPORTIONAL ZERO-VOLTAGE SWITCHING CONTROL

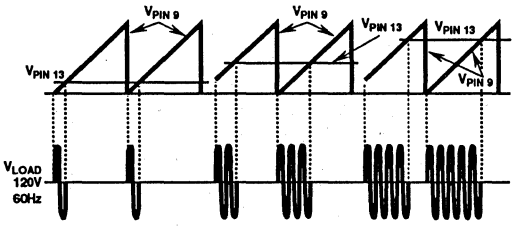


FIGURE 18. WAVEFORMS FOR THE CIRCUIT OF FIGURE 17.

Effect of Thyristor Load Characteristics

The zero-voltage switch is designed primarily to gate a thyristor that switches a resistive load. Because the output pulse supplied by the switch is of short duration, the latching current of the triac becomes a significant factor in determining whether other types of loads can be switched. (The latching current value determines whether the triac will remain in conduction after the gate pulse is removed.) Provisions are included in the zero-voltage switch to accommodate inductive loads and low power loads. For example, for loads that are less than approximately $4A_{rms}$ or that are slightly inductive, it is possible to retard the output pulse with respect to the zero-voltage crossing by insertion of the capacitor C_X from terminal 5 to terminal 7. The insertion of capacitor C_X permits switching of triac loads that have a slight inductive component and that are greater than approximately 200W (for operation from an AC line voltage of $120V_{rms}$). However, for loads less than 200W (for example, 70W), it is recommended that the user employ the T2300B* sensitive gate triac with the zero-voltage switch because of the low latching current requirement of this triac.

* Formerly RCA 40526

For loads that have a low power factor, such as a solenoid valve, the user may operate the zero-voltage switch in the DC mode. In this mode, terminal 12 is connected to terminal 7, and the zero crossing detector is inhibited. Whether a "high" or "low" voltage is produced at terminal 4 is then dependent only upon the state of the differential comparator within the integrated circuit zero-voltage switch, and not upon the zero crossing of the incoming line voltage. Of course, in this mode of operation, the zero-voltage switch no longer operates as a zero-voltage switch. However, for may applications that involve the switching of low current inductive loads, the amount of RFI generated can frequently be tolerated.

For switching of high current inductive loads, which must be turned on at zero line current, the triggering technique employed in the dual output over-under temperature controller and the transient free switch controller described subsequently in this Note is recommended.

Switching of Inductive Loads

For proper driving of a thyristor in full cycle operation, gate drive must be applied soon after the voltage across the device reverses. When resistive loads are used, this reversal occurs as the line voltage reverses. With loads of other power factors, however, it occurs as the current through the load becomes zero and reverses.

There are several methods for switching an inductive load at the proper time. If the power factor of the load is high (i.e., if the load is only slightly inductive), the pulse may be delayed by addition of a suitable capacitor between terminals 5 and 7, as described previously. For highly inductive loads, however, this method is not suitable, and different techniques must be used.

If gate current is continuous, the triac automatically commutates because drive is always present when the voltage reverses. This mode is established by connection of terminals 7 and 12. The zero crossing detector is then disabled so that current is supplied to the triac gate whenever called for by the sensing amplifier. Although the RFI eliminating function of the zero-voltage switch is inhibited when the zero crossing detector is disabled, there is no problem if the load is highly inductive because the current in the load cannot change abruptly.

Circuits that use a sensitive gate triac to shift the firing point of the power triac by approximately 90 degrees have been designed. If the primary load is inductive, this phase shift corresponds to firing at zero current in the load. However, changes in the power factor of the load or tolerances of components will cause errors in this firing time.

The circuit shown in Figure 19 uses a CA3086 integrated circuit transistor array to detect the absence of load current by sensing the voltage across the triac. The internal zero crossing detector is disabled by connection of terminal 12 to terminal 7, and control of the output is made through the external inhibit input, terminal 1. The circuit permits an output only when the voltage at point A exceeds two V_{BE} drops, or 1.3V. When A is positive, transistors Q_3 and Q_4 conduct and reduce the voltage at terminal 1 below the inhibit state. When A is negative, transistors Q_1 and Q_2 conduct. When the voltage at point A is less than ±1.3V, neither of the transistor pairs conducts; terminal 1 is then pulled positive by the current in resistor R_3, and the output is inhibited.

The circuit shown in Figure 19 forms a pulse of gate current and can supply high peak drive to power triacs with low average current drain on the internal supply. The gate pulse will always last just long enough to latch the thyristor so that there is no problem with delaying the pulse to an optimum time. As in other circuits of this type, RFI results if the load is not suitable inductive because the zero crossing detector is disabled and initial turn on occurs at random.

The gate pulse forms because the voltage at point A when the thyristor is on is less than 1.3V; therefore, the output of the zero-voltage switch is inhibited, as described above. The resistor divider R_1 and R_2 should be selected to assure this condition. When the triac is on, the voltage at point A is approximately one third of the instantaneous on state voltage (V_T) of the thyristor. For most Harris thyristors, V_T (max) is less than 2V, and the divider shown is a conservative one. When the load current passes through zero, the triac commutates and turns off. Because the circuit

is still being driven by the line voltage, the current in the load attempts to reverse, and voltage increases rapidly across the "turned-off" triac. When this voltage exceeds 4V, one portion of the CA3086 conducts and removes the inhibit signal to permit application of gate drive. Turning the triac on causes the voltage across it to drop and thus ends the gate pulse. If the latching current has not been attained, another gate pulse forms, but no discontinuity in the load current occurs.

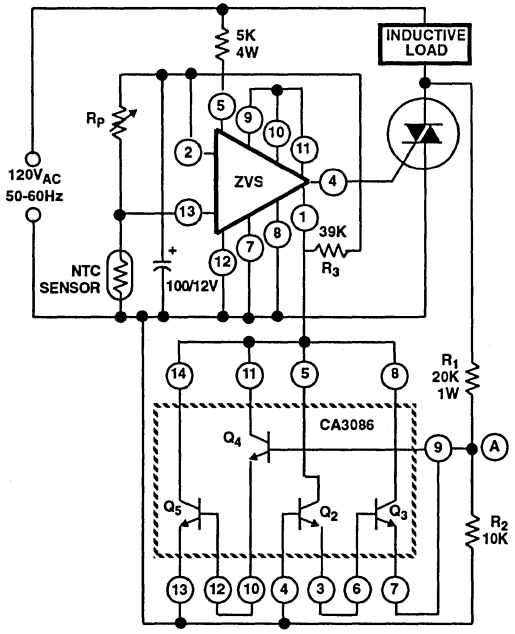
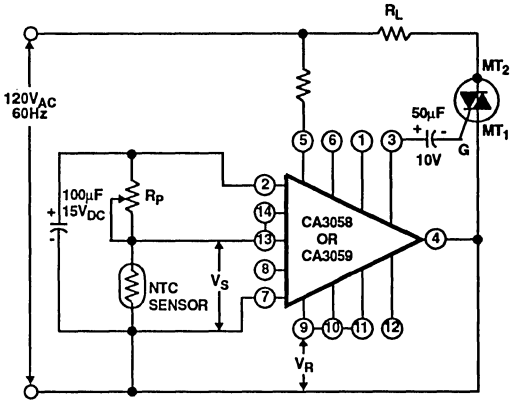


FIGURE 19. USE OF THE CA3058 OR CA3059 TOGETHER WITH 3086 FOR SWITCHING INDUCTIVE LOADS

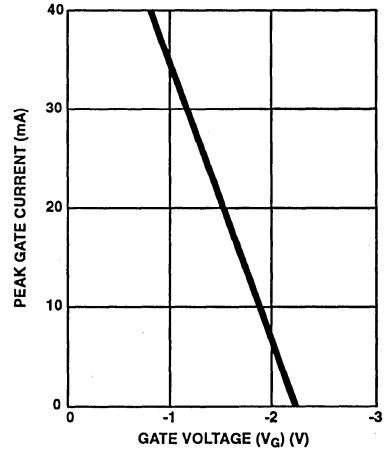
Provision of Negative Gate Current

Triacs trigger with optimum sensitivity when the polarity of the gate voltage and the voltage at the main terminal 2 are similar (I+ and II- modes). Sensitivity is degraded when the polarities are opposite (I- and III+ modes). Although Harris triacs are designed and specified to have the same sensitivity in both I- and III+ modes, some other types have very poor sensitivity in the III+ condition. Because the zero-voltage switch supplies positive gate pulses, it may not directly drive some high current triacs of these other types.

The circuit shown in Figure 20(a) uses the negative going voltage at terminal 3 of the zero-voltage switch to supply a negative gate pulse through a capacitor. The curve in Figure 20(b) shows the approximate peak gate current as a function of gate voltage V_G. Pulse width is approximately 80µs.



(a)



(b)

FIGURE 20. USE OF THE CA3058 OR CA3059 TO PROVIDE NEGATIVE GATE PULSES: (a) SCHEMATIC DIAGRAM; (b) PEAK GATE CURRENT (FAT TERMINAL 3) AS A FUNCTION OF GATE VOLTAGE

Operation with Low Impedance Sensors

Although the zero-voltage switch can operate satisfactorily with a wide range of sensors, sensitivity is reduced when sensors with impedances greater than 20,000Ω are used. Typical sensitivity is one percent for a 5000Ω sensor and increases to three percent for a 0.1MΩ sensor.

Low impedance sensors present a different problem. The sensor bridge is connected across the internal power supply and causes a current drain. A 5000Ω sensor with its associated 5000Ω series resistor draws less than 1mA. On the other hand, a 300Ω sensor draws a current of 8 to 10mA from the power supply.

Figure 21 shows the 600Ω load line of a 300Ω sensor on a redrawn power supply regulation curve for the zero-voltage switch. When a 10,000Ω series resistor is used, the voltage

across the circuit is less than 3V and both sensitivity and output current are significantly reduced. When a 500Ω series resistor is used, the supply voltage is nearly 5V, and operation is approximately normal. For more consistent operation, however, a 400Ω series resistor is recommended.

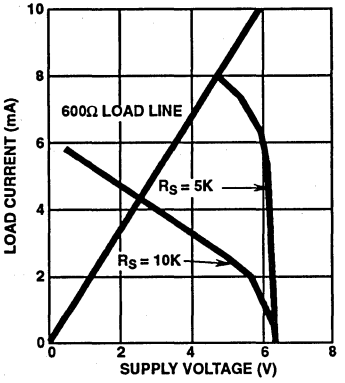


FIGURE 21. POWER SUPPLY REGULATION OF THE CA3058 OR CA3059 WITH A 300Ω SENSOR (600Ω LOAD) FOR TWO VALUES OF SERIES RESISTOR.

Although positive temperature coefficient (PTC) sensors rated at 5kΩ are available, the existing sensors in ovens are usually of a much lower value. The circuit shown in Figure 22 is offered to accommodate these inexpensive metal wound sensors. A schematic diagram of the CA3080 integrated circuit operation transconductance amplifier used in Figure 22, is shown in Figure 23. With an amplifier bias current, I_{ABC}, of 100μA, a forward transconductance of 2mΩ is achieved in this configuration. The CA3080 switches when the voltage at terminal 2 exceeds the voltage at terminal 3. This action allows the sink current, I_S, to flow from terminal 13 of the zero-voltage switch (the input impedance to terminal 13 of the zero-voltage switch is approximately 50kΩ); gate pulses are no longer applied to the triac because Q_2 of the zero-voltage switch is on. Hence, if the PTC sensor is cold, i.e., in the low resistance state, the load is energized. When the temperature of the PTC sensor increases to the desired temperature, the sensor enters the high resistance state, the voltage on terminal 2 becomes greater than that on terminal 3, and the triac switches the load off.

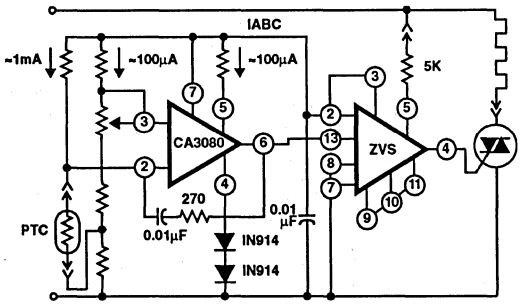


FIGURE 22. SCHEMATIC DIAGRAM OF CIRCUIT FOR USE WITH LOW RESISTANCE SENSOR.

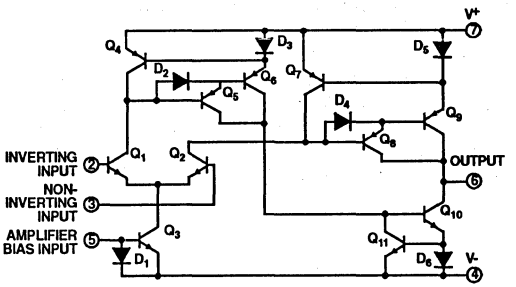


FIGURE 23. SCHEMATIC DIAGRAM OF THE CA3080

Further cycling depends on the voltage across the sensor. Hence, very low values of sensor and potentiometer resistance can be used in conjunction with the zero-voltage switch power supply without causing adverse loading effects and impairing system performance.

Interfacing Techniques

Figure 24 shows a system diagram that illustrates the role of the zero-voltage switch and thyristor as an interface between the logic circuitry and the load. There are several basic interfacing techniques. Figure 25(a) shows the direct input technique. When the logic output transistor is switched from the on state (saturated) to the off state, the load will be turned on at the next zero-voltage crossing by means of the interfacing zero-voltage switch and the triac. When the logic output transistor is switched back to the on state, zero crossing pulses from the zero-voltage switch to the triac gate will immediately cease. Therefore, the load will be turned off when the triac commutates off as the sine wave load current goes through zero. In this manner, both the turn-on and turn-off conditions for the load are controlled.

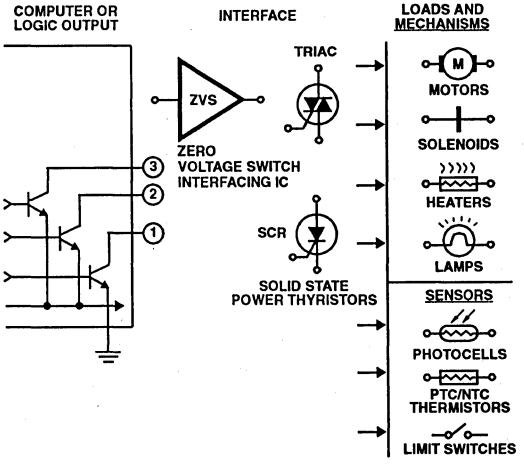
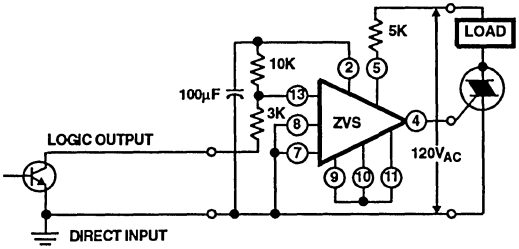


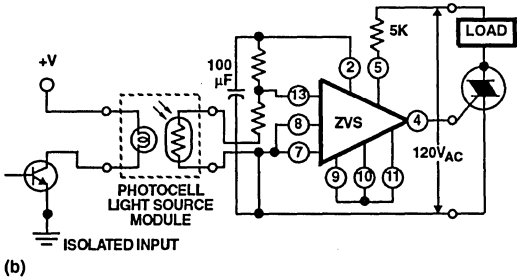
FIGURE 24. THE ZERO-VOLTAGE SWITCH AND THYRISTOR AS AN INTERFACE

When electrical isolation between the logic circuit and the load is necessary, the **isolated-input** technique shown in Figure 25(b) is used. In the technique shown, optical coupling is used

to achieve the necessary isolation. The logic output transistor switches the light source portion of the isolator. The light sensor portion changes from a high impedance to a low impedance when the logic output transistor is switched from off to on. The light sensor is connected to the differential amplifier input of the zero-voltage switch, which senses the change of impedance at a threshold level and switches the load on as in Figure 25(a)



(a)



(b)

FIGURE 25. BASIC INTERFACING TECHNIQUES: (a) DIRECT INPUT; (b) ISOLATED INPUT

Sensor Isolation

In many applications, electrical isolation of the sensor from the AC input line is desirable. Several isolation techniques are shown in Figures 26, 27, and 28.

Transformer Isolation - In Figure 26, a pulse transformer is used to provide electrical isolation of the sensor from incoming AC power lines. The pulse transformer T_1 isolates the sensor from terminal No. 1 of the triac Y_1, and transformer T_2 isolates the CA3058 or CA3059 from the power lines. Capacitor C_1 shifts the phase of the output pulse at terminal No. 4 in order to retard the gate pulse delivered to triac Y_1 to compensate for the small phase shift introduced by transformer T_1.

Many applications require line isolation but not zero-voltage switching. A line isolated temperature controller for use with inductive or resistive loads that does not include zero-voltage switching is shown in Figure 27.

In temperature monitoring or control applications the sensor may be a temperature dependent element such as a resistor, thermistor, or diode. The load may be a lamp, bell, horn, recorder or other appropriate device connected in a feedback relationship to the sensor.

For the purpose of the following explanation, assume that the sensor is a resistor having a negative temperature coefficient and that the load is a heater thermally coupled to the sensor, the object being to maintain the thermal coupling medium at a desired reference temperature. Assume initially that the temperature at the coupling medium is low.

The operating potentials applied to the bridge circuit produce a common mode potential, V_{CM}, at the input terminals of the CA3094. Assuming the bridge to have been initially balanced (by adjustment of R_4), the potential at point A will

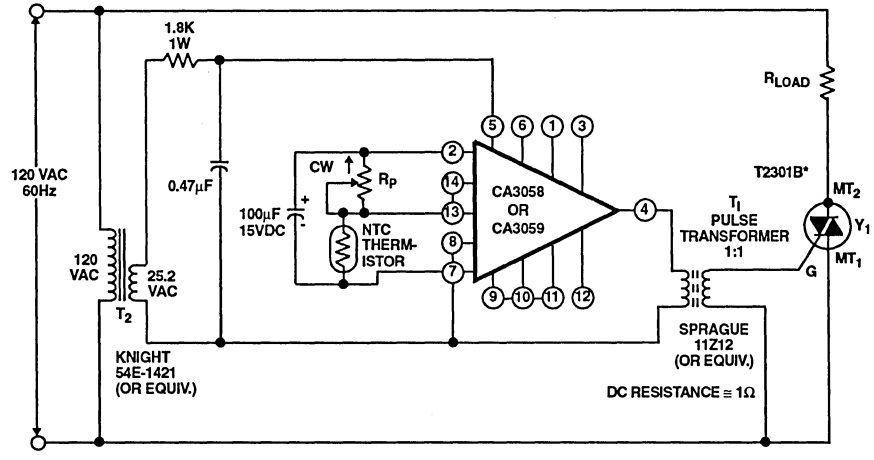


FIGURE 26. ZERO-VOLTAGE SWITCH, ON/OFF CONTROLLER WITH AN ISOLATED SENSOR

increase when temperature is low since it was assumed that the sensor has a negative temperature coefficient. The potential at the noninverting terminal, being greater than that at the inverting terminal at the amplifier, causes the multivibrator to oscillate at approximately 10kHz. The oscillations are transformer coupled through a current limiting resistor to the gate of the thyristor, and trigger it into conduction.

When the thyristor conducts, the load receives AC input power, which tends to increase the temperature of the sensor. This temperature increase decreases the potential at point A to a value below that at point B and the multivibrator is disabled, which action, in turn, turns off the thyristor. The temperature is thus controlled in an of/off fashion.

Capacitor C_1 is used to provide a low impedance path to ground for feedback induced signals at terminal No. 5 while blocking the direct current bias provided by resistor R_1. Resistor R_2 provides current limiting. Resistor R_3 limits the secondary current of the transformer to prevent excessive current flow to the control terminal of the CA3094.

Photocoupler Isolation - In Figure 28, a photocoupler provides electrical isolation of the sensor logic from the incoming AC power lines. When a logic "1" is applied at the input of the photocoupler, the triac controlling the load will be turned on whenever the line voltage passes through zero. When a logic "0" is applied to the photocoupler, the triac will turn off and remain off until a logic "1" appears at the input of the photocoupler.

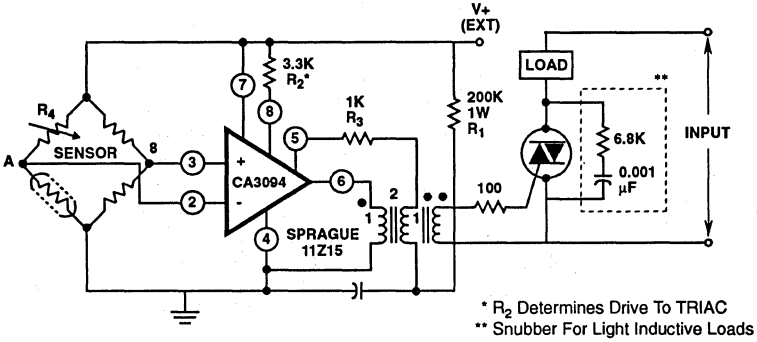


FIGURE 27. A LINE ISOLATED TEMPERATURE CONTROLLER FOR USE WITH INDUCTIVE OR RESISTIVE LOADS; THIS CONTROLLER DOES NOT INCLUDE ZERO-VOLTAGE SWITCHING.

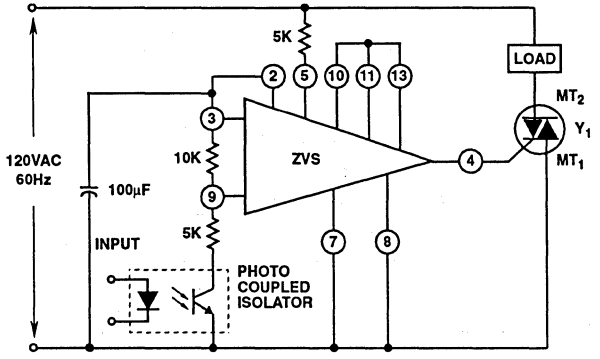


FIGURE 28. ZERO-VOLTAGE SWITCH, ON/OFF CONTROLLER WITH PHOTOCOUPLER

Temperature Controllers

Figure 29 shows a triac used in an of/off temperature controller configuration. The triac is turned on at zero-voltage whenever the voltage V_S exceeds the reference voltage V_R. The transfer characteristic of this system, shown in Figure 30(a), indicates significant thermal overshoots and undershoots, a well known characteristic of such a system. The differential or hysteresis of this system, however, can be further increased, if desired, by the addition of positive feedback.

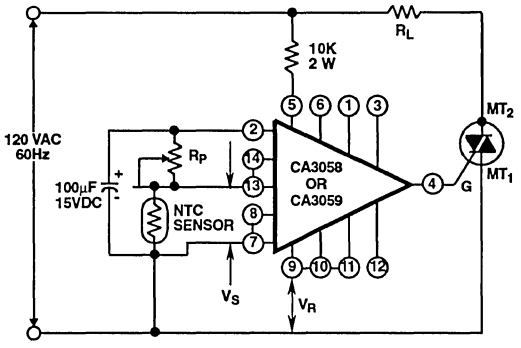


FIGURE 29. CA3058 OR CA3059 ON/OFF TEMP. CONTROLLER

For precise temperature control applications, the proportional control technique with synchronous switching is employed. The transfer curve for this type of controller is shown in Figure 30(b). In this case, the duty cycle of the power supplied to the load is varied with the demand for heat required and the thermal time constant (inertia) of the system. For example, when the temperature setting is increased in an of/off type of controller, full power (100 percent duty cycle) is supplied to the system This effect results in significant temperature excursions because there is no anticipatory circuit to reduce the power gradually before the actual set temperature is achieved. However, in a proportional control technique, less power is supplied to the load (reduced duty cycle) as the error signal is reduced (sensed temperature approaches the set temperature).

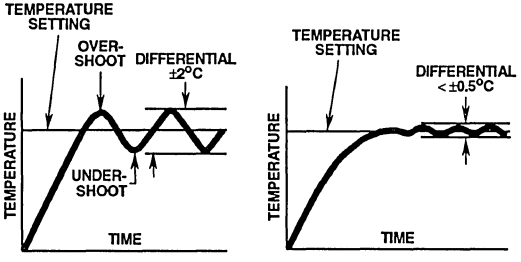


FIGURE 30. TRANSFER CHARACTERISTICS OF (a) ON/OFF AND (b) PROPORTIONAL CONTROL SYSTEMS

Before such a system is implemented, a time base is chosen so that the on time of the triac is varied within this time base. The ratio of the on-to-off time of the triac within this time interval depends on the thermal time constant of the system and the selected temperature setting. Figure 31 illustrates the principle of proportional control. For this operation, power is supplied to the load until the ramp voltage reaches a value greater than the DC control signal supplied to the opposite side of the differential amplifier. The triac then remains off for the remainder of the time base period. As a result, power is "proportioned" to the load in a direct relation to the heat demanded by the system.

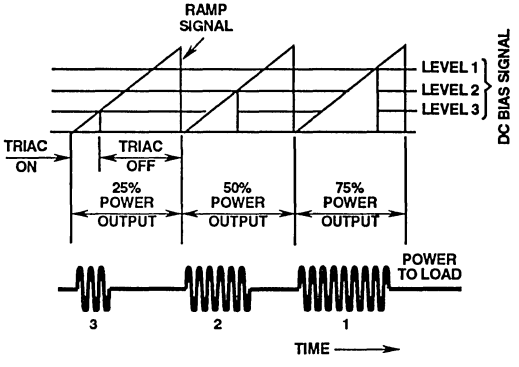
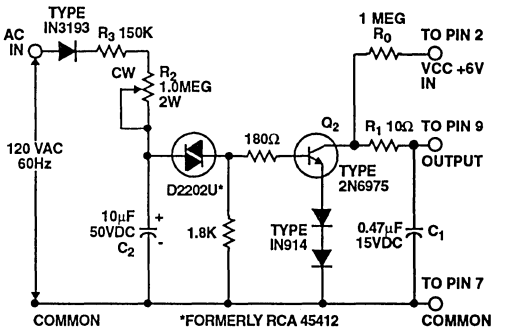


FIGURE 31. PRINCIPLES OF PROPORTIONAL CONTROL

For this application, a simple ramp generator can be realized with a minimum number of active and passive components. A ramp having good linearity is not required for proportional operation because of the nonlinearity of the thermal system and the closed loop type of control. In the circuit shown in Figure 32, the ramp voltage is generated when the capacitor C_1 charges through resistors R_0 and R_1. The time base of the ramp is determined by resistors R_2 and R_3, capacitor C_2, and the breakover voltage of the D3202U* diac.



All Resistors 1/2 Watt Unless Otherwise Specified

Pin Connections Refer To CA3058 OR CA3059

FIGURE 32. RAMP GENERATOR

When the voltage across C_2 reaches approximately 32V, the diac switches and turns on the 2N697S transistor and 1N914 diode. The capacitor C_1 then dishcarges through the collector-to-emit-

junction of the transistor. This discharge time is the retrace or flyback time of the ramp. The circuit shown can generate ramp times ranging from 0.3 to 2.0 seconds through adjustment of R_2. For precise temperature regulation, the time base of the ramp should be shorter than the thermal time constant of the system, but long with respect to the period of the 60Hz line voltage. Figure 33 shows a triac connected for the proportional mode.

Figure 34(a) shows a dual output temperature controller that drives two triacs. When the voltage V_S developed across the temperature sensing network exceeds the reference voltage V_{R1}, motor No. 1 turns on. When the voltage across the network drops below the reference voltage V_{R2}, motor No. 2 turns on. Because the motors are inductive, the currents I_{M1} lag the incoming line voltage. The motors, however, are switched by the triacs at zero current, as shown in Figure 34(b).

The problem of driving inductive loads such as these motors by the narrow pulses generated by the zero-voltage switch is solved by use of the sensitive gate Harris 40526 triac. The high sensitivity of this device (3mA maximum) and low latching current (approximately 9mA) permit synchronous operation of the temperature controller circuit. In Figure 34(a), it is apparent that, though the gate pulse V_G of triac Y_1 has elapsed, triac Y_2 is switched on by the current through R_{L1}. The low latching current of the Harris 40526 triac results in dissipation of only 2W in R_{L1}, as opposed to 10 to 20W when devices that have high latching currents are used.

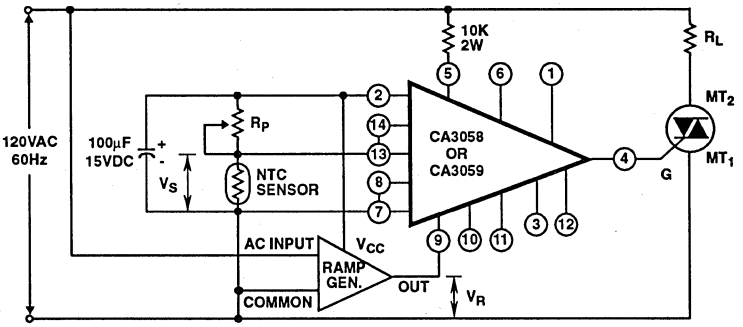


FIGURE 33. CA3058 OR CA3059 PROPORTIONAL TEMPERATURE CONTROLLER

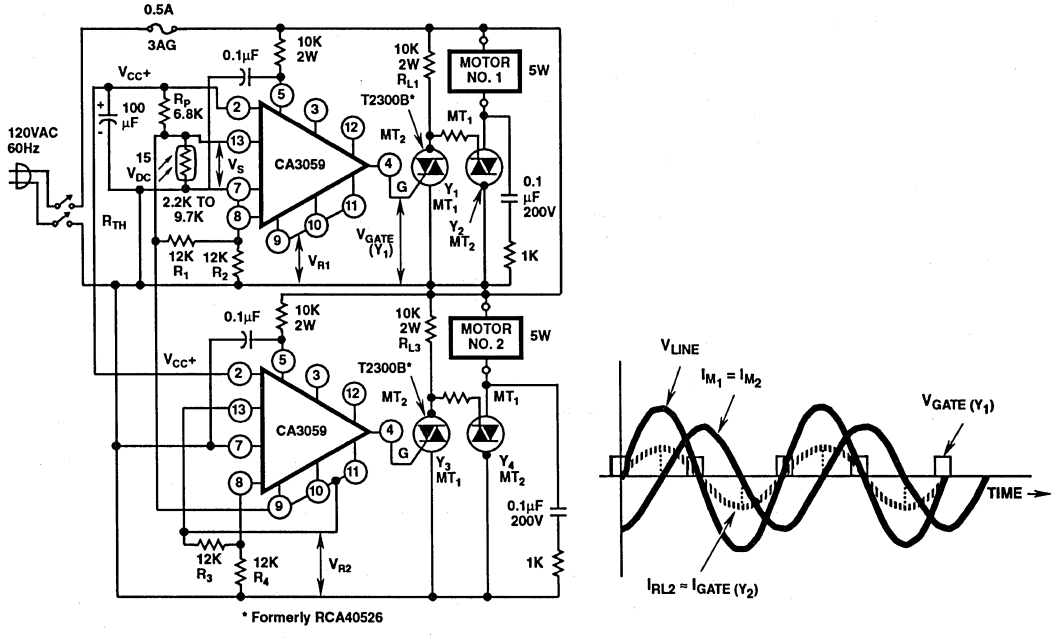


FIGURE 34. DUAL OUTPUT, OVER-UNDER TEMPERATURE CONTROLLER (a) CIRCUIT, (b) VOLTAGE AND CURRENT WAVEFORMS

Electric Heat Application

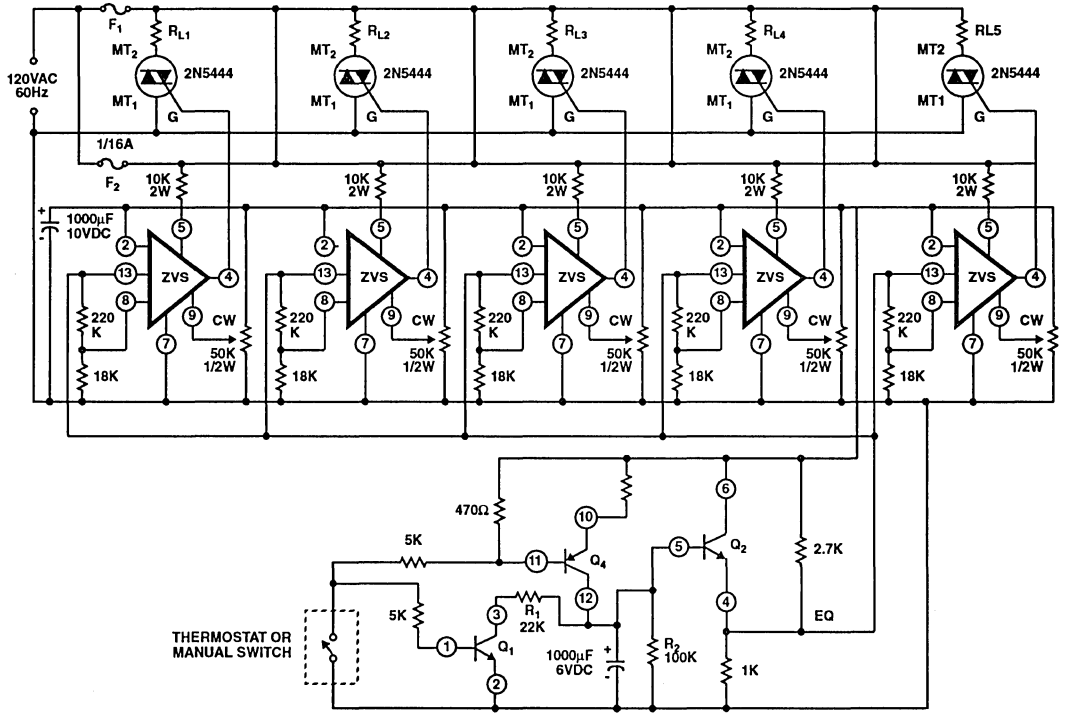
For electric heating applications, the 2N5444 40A triac and the zero-voltage switch constitute an optimum pair. Such a combination provides synchronous switching and effectively replaces the heavy-duty contactors which easily degrade as a result of pitting and wearout from the switching transients. The salient features of the 2N5444 40A triac are as follows:

1. 300A single surge capability (for operation at 60Hz).
2. A typical gate sensitivity of 20mA in the I(+) and III(+) modes.
3. Low on state voltage of 1.5V maximum at 40A.
4. Available V_{DROM} equal to 600V.

Figure 35 shows the circuit diagram of a synchronous switching heat staging controller that is used for electric heating systems. Loads as heavy as 5kW are switched sequentially at zero-voltage to eliminate RFI and prevent a dip in line voltage that would occur if the full 25kW were to be switched simultaneously.

Transistor Q_1 and Q_4 are used as a constant current source to charge capacitor C in a linear manner. Transistor Q_2 acts as a buffer stage. When the thermostat is closed, a ramp voltage is provided at output E_O. At approximately 3 second intervals, each 5kW heating element is switched onto the power system by its respective triac. When there is no further demand for heat, the thermostat opens, and capacitor C discharges through R1 and R2 to cause each triac to turn off in the reverse heating sequence. It should be noted that some half cycling occurs before the heating element is switched fully on. This condition can be attributed to the inherent dissymmetry of the triac and is further aggravated by the slow rising ramp voltage applied to one of the inputs. The timing diagram in Figure 36 shows the turn-on and turn-off sequence of the heating system being controlled.

Seemingly, the basic method shown in Figure 35 could be modified to provide proportional control in which the number of heating elements switched into the system, under any given thermal load, would be a function of the BTU's required by the system or the temperature differential between an indoor and outdoor sensor within the total system environment. That is, the closing of the thermostat would not switch in all the heating elements within a short time interval, which inevitable results in undesired temperature excursions, but would switch in only the number of heating elements required to satisfy the actual heat load.



All Resistors 1/2W, Unless Otherwise Specified.
Transistors Q_1, Q_2 and Q_4 are Part of CA3096E Integrated Circuit N-P-N/P-N-P Transistor Array.

FIGURE 35. SYNCHRONOUS SWITCHING HEAT STAGING CONTROLLER USING A SERIES OF ZERO-VOLTAGE SWITCHES

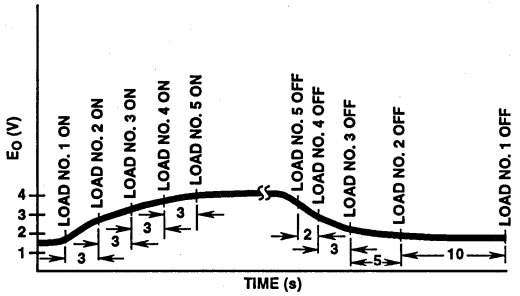


FIGURE 36. RAMP VOLTAGE WAVEFORM FOR THE HEAT STAGING CONTROLLER

Oven/Broiler Control

Zero-voltage switching is demonstrated in the oven control circuit shown in Figure 37. In this circuit, a sensor element is included in the oven to provide a closed loop system for accurate control of the oven temperature.

As shown in Figure 37, the temperature of the oven can be adjusted by means of potentiometer R_1, which acts, together with the sensor, as a voltage divider at terminal 13. The voltage at terminal 13 is compared to the fixed bias at terminal 9 which is set by internal resistors R_4 and R_5. When the oven is cold and the resistance of the sensor is high, transistors Q_2 and Q_4 are off, a pulse of gate current is applied to the triac, and heat is applied to the oven. Conversely, as the desired temperature is reached, the bias at terminal 13 turns the triac off. The closed loop feature then cycles the oven element on and of' maintain the desired temperature to approximately ±2°C of the set value. Also, as has been noted, external resistors between terminals 13 and 8, and 7 and 8, can be used to vary this temperature and provide hysteresis. In Figure 11, a circuit that provides approximately 10 percent hysteresis is demonstrated.

In addition to allowing the selection of a hysteresis value, the flexibility of the control circuit permits incorporation of other features. A PTC sensor is readily used by interchanging terminals 9 and 13 of the circuit shown in Figure 37 and substituting the PTC for the NTC sensor. In both cases, the sensor element is directly returned to the system ground or common, as is often desired. Terminal 9 can be connected by external resistors to provide for a variety of biasing, e.g., to match a lower resistance sensor for which the switching point voltage has been reduced to maintain the same sensor current.

To accommodate the self-cleaning feature, external switching, which enables both broiler and oven units to be paralleled, can easily be incorporated in the design. Of course, the potentiometer must be capable of a setting such that the sensor, which must be characterized for the high, self-clean temperature, can monitor and establish control of the high temperature, self-clean mode. The ease with which this self-clean mode can be added makes the overall solid state systems cost competitive with electromechanical systems of comparable capability. In addition, the system incorporates solid-state reliability while being neater, more easily calibrated, and containing less costly system wiring.

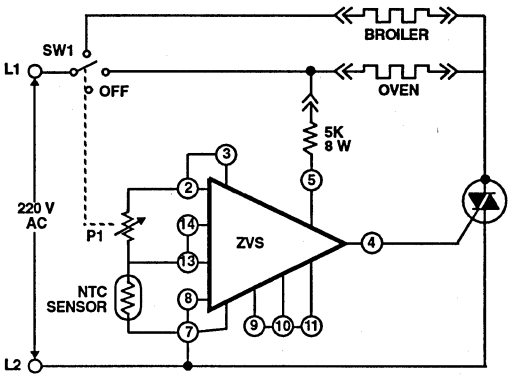


FIGURE 37. SCHEMATIC DIAGRAM OF BASIC OVEN CONTROL

Integral Cycle Temperature Controller (No half cycling)

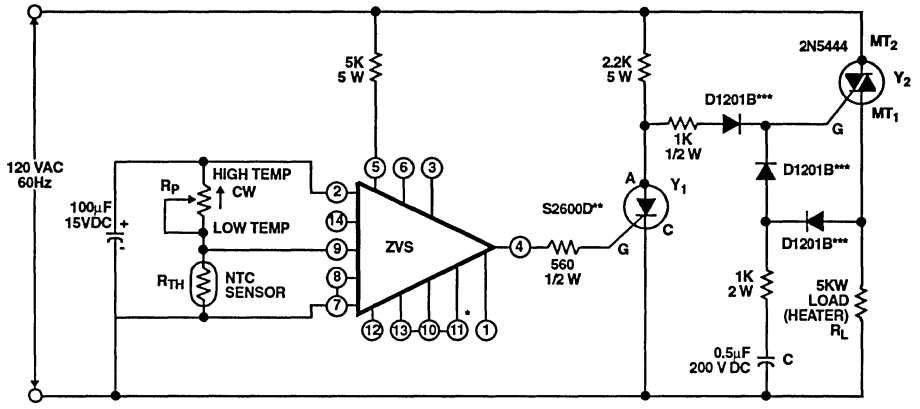
If a temperature controller which is completely devoid of half cycling and hysteresis is required, then the circuit shown in Figure 38 may be used. This type of circuit is essential for applications in which half cycling and the resultant DC component could cause overheating of a power transformer on the utility lines.

In the integral cycle controller, when the temperature being controlled is low, the resistance of the thermistor is high, and an output signal at terminal 4 of zero volts is obtained. The SCR (Y_1), therefore, is turned off. The triac (Y_2) is then triggered directly from the line on positive cycles of the AC voltage. When Y_2 is triggered and supplies power to the load R_L, capacitor C is charged to the peak of the input voltage. When the AC line swings negative, capacitor C discharges through the triac gate to trigger the triac on the negative half cycle. The diode-resistor-capacitor "slaving network" triggers the triac on negative half cycle to provide only integral cycles of AC power to the load.

When the temperature being controlled reaches the desired value, as determined by the thermistor, then a positive voltage level appears at terminal 4 of the zero-voltage switch. The SCR then starts to conduct at the beginning of the positive input cycle to shunt the trigger current away from the gate of the triac. The triac is then turned off. The cycle repeats when the SCR is again turned OFF by the zero-voltage switch.

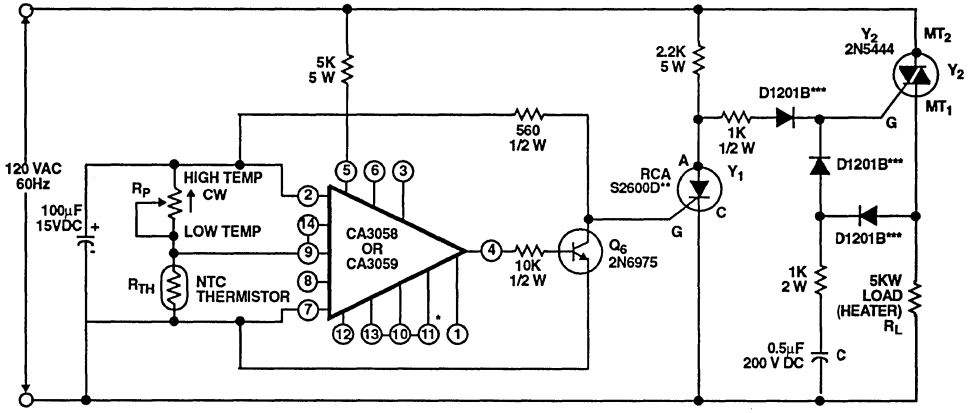
The circuit shown in Figure 39 is similar to the configuration in Figure 38 except that the protection circuit incorporated in the zero-voltage switch can be used. In this new circuit, the NTC sensor is connected between terminals 7 and 13, and transistor Q_0 inverts the signal output at terminal 4 to nullify the phase reversal introduced by the SCR (Y_1). The internal power supply of the zero-voltage switch supplies bias current to transistor Q_0.

Of course, the circuit shown in Figure 39 can readily be converted to a **true proportional integral cycle temperature controller** simply by connection of a positive going ramp voltage to terminal 9 (with terminals 10 and 11 open), as previously discussed in this Note.



* For proportional operation open terminals 10, 11 and 13, and connect positive ramp voltage to terminal 13.
** Selected for I_{GT} = 6mA maximum, formerly RCA 40655.
*** Formerly RCA 44003.

FIGURE 38. INTEGRAL CYCLE TEMPERATURE CONTROLLER IN WHICH HALF CYCLING EFFECT IS ELIMINATED



* For proportional operation open terminals 9, 10 and 11, and connect positive ramp voltage to terminal 9.
** Selected for I_{GT} = 6mA maximum, formerly RCA 40655.
*** Formerly RCA 44003.

FIGURE 39. CA3058 OR CA3059 INTEGRAL CYCLE TEMPERATURE CONTROLLER THAT FEATURES A PROTECTION CIRCUIT AND NO HALF CYCLING EFFECT

Thermocouple Temperature Control

Figure 40 shows the CA3080A operating as a preamplifier for the zero-voltage switch to form a zero-voltage switching circuit for use with thermocouple sensors.

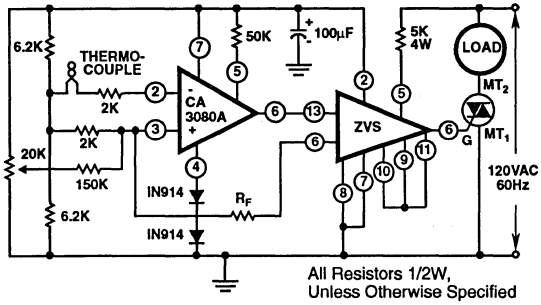
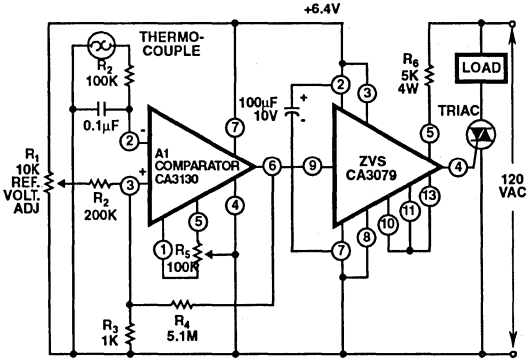


FIGURE 40. THERMOCOUPLE TEMPERATURE CONTROL WITH ZERO-VOLTAGE SWITCHING

Thermocouple Temperature Control with Zero-Voltage Load Switching

Figure 41 shows the circuit diagram of a thermocouple temperature control system using zero-voltage load switching. It should be noted that one terminal of the thermocouple is connect to one leg of the supply line. Consequently, the thermocouple can be "ground referenced", provided the appropriate leg of the AC line is maintained at ground. The comparator, A_1 (a CA3010), is powered from a 6.4V source of potential provided by the zero-voltage switch (ZVS) circuit (a CA3079). The ZVS, in turn, is powered off-line through a series dropping resistor R_6. Terminal 4 of the ZVS provides trigger pulses to the gate of the load switching triac in response to an appropriate control signal at terminal 9.



Hysteresis = R3/R4 x 6.4V = 1K/5.1M x 6.4V = 1.25mV

FIGURE 41. THERMOCOUPLE TEMPERATURE CONTROL WITH ZERO-VOLTAGE SWITCHING

The CA3130 is an ideal choice for the type of comparator circuit shown in Figure 41 because it can "compare" low voltages (such as those generated by a thermocouple) in the proximity of the negative supply rail. Adjustment of potentiometer R_1 drives the voltage divider network R_3, R_4 so that reference voltages over the range of 0 to 20mV can be applied to noninverting terminal 3 of the comparator. Whenever the voltage developed by the thermocouple at terminal 2 is more positive than the reference voltage applied at terminal 3, the comparator output is toggled so as to sink current from terminal 9 of the ZVS; gate pulses are then no longer applied to the triac. As shown in Figure 41, the circuit is provided with a control point "hysteresis" of 1.25mV.

Nulling of the comparator is performed by means of the following procedure: Set R_1 at the low end of its range and short the thermocouple output signal appropriately. If the triac is in the conductive mode under these conditions, adjust nulling potentiometer R_5 to the point at which triac conduction is interrupted. On the other hand, if the triac is in the nonconductive mode under the conditions above, adjust R_5 to the point at which triac conduction commences. The thermocouple output signal should then be unshorted, and R_1 can be set to the voltage threshold desired for control circuit operation.

Machine Control and Automation

The earlier section on interfacing techniques indicated several techniques of controlling AC loads through a logic system. Many types of automatic equipment are not complex enough or large enough to justify the cost of a flexible logic system. A special circuit, designed only to meet the control requirements of a particular machine, may prove more economical. For example, consider the simple machine shown in Figure 42; for each revolution of the motor, the belt is advanced a prescribed distance, and the strip is then punched. The machine also has variable speed capability.

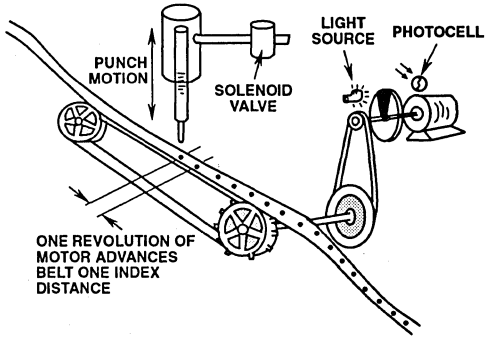


FIGURE 42. STEP-AND-PUNCH MACHINE

The typical electromechanical control circuit for such a machine might consist of a mechanical cambank driven by a separate variable speed motor, a time delay relay, and a few logic and power relays. Assuming use of industrial grade controls, the control system could get quite costly and large. Of greater importance is the necessity to eliminate transients generated each time a relay or switch energizes and deenergizes the solenoid and motor. Figure 43 shows such transients, which might not affect the operation of this machine, but could affect the more sensitive solid-state equipment operating in the area.

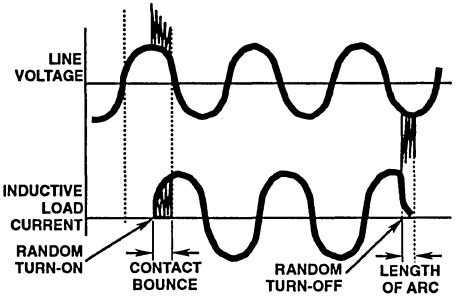


FIGURE 43. TRANSIENTS GENERATED BY RELAY CONTACT BOUNCE AND NONZERO TURN OFF OF INDUCTIVE LOAD.

A more desirable system would use triacs and zero-voltage switching to incorporate the following advantages:

1. Increased reliability and long life inherent in solid-state devices as opposed to moving parts and contacts associated with relays.
2. Minimized generation of EMI/RFI using zero-voltage switching techniques in conjunction with thyristors.
3. Elimination of high voltage transients generated by relay contact bounce and contacts breaking inductive loads, as shown in Figure 42.
4. Compactness of the control system.

The entire control system could be on one printed circuit board, and an overall cost advantage would be achieved. Figure 44 is a timing diagram for the proposed solid-state machine control, and Figure 45 is the corresponding control schematic. A variable speed machine repetition rate pulse is set up using either a unijunction oscillator or a transistor astable multivibrator in conjunction with a 10ms one shot multivibrator. The first zero voltage switch in Figure 45 is used to synchronize the entire system to zero-voltage crossing. Its output is inverted to simplify adaptation to the rest of the circuit. The center zero-voltage switch is used as an interface for the photocell, to control one revolution of the motor. The gate drive to the motor triac is continuous DC, starting at zero voltage crossing. The motor is initiated when both the machine rate pulse and the zero-voltage sync are at low voltage. The bottom zero-voltage switch acts as a time delay for pulsing the solenoid. The inhibit input, terminal 1, is used to assure that the solenoid will not be operated while the motor is running. The time delay can be adjusted by varying the reference level (50K potentiometer) at terminal 13 relative to the capacitor charging to that level on terminal 9. The capacitor is reset by the SCR during the motor operation. The gate drive to the solenoid triac is direct current. Direct current is used to trigger both the motor and solenoid triacs because it is the most desirable means of switching a triac into an inductive load. The output of the zero-voltage switch will be continuous DC by connecting terminal 12 to common. The output under DC operation should be limited to 20mA. The motor triac is synchronized to zero crossing because it is a high current inductive load and there is a change of generating RFI. The solenoid is a very low current inductive load, so there would be little chance of generating RFI; therefore, the initial triac turn-on can be random which simplifies the circuitry.

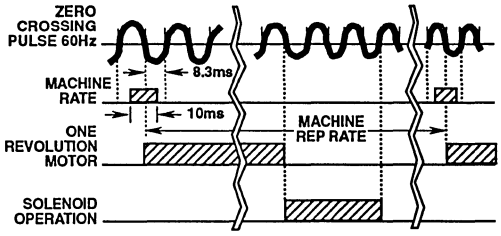


FIGURE 44. TIMING DIAGRAM FOR SOLID-STATE MACHINE CONTROL

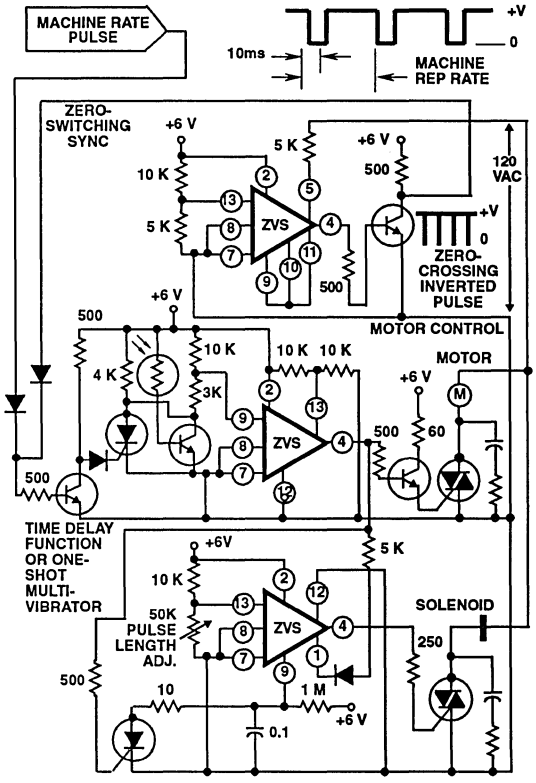


FIGURE 45. SCHEMATIC OF PROPOSED SOLID-STATE MACHINE CONTROL

This example shows the versatility and advantages of the Harris zero-voltage switch used in conjunction with triacs as interfacing and control elements for machine control.

400Hz Triac Applications

The increased complexity of aircraft control systems, and the need for greater reliability than electromechanical switching

can offer, has led to the use of solid-state power switching in aircraft. Because 400Hz power is used almost universally in aircraft systems, Harris offers a complete line of triacs rated for 400Hz applications. Use of the Harris zero-voltage switch in conjunction with these 400Hz triacs results in a minimum of RFI, which is especially important in aircraft.

Areas of application for 400Hz triacs in aircraft include:

1. Heater controls for food warming ovens and windshield defrosters
2. Lighting controls for instrument panels and cabin illumination
3. Motor controls and solenoid controls
4. Power supply switches

Lamp dimming is a simple triac application that demonstrates an advantage of 400Hz power over 60Hz power. Figure 46 shows the adjustment of lamp intensity by phase control of the 60Hz line voltage. RFI is generated by the step functions of power each half cycle, requiring extensive filtering. Figure 47 shows a means of controlling power to the lamp by the zero-voltage switching technique. Use of 400Hz power makes possible the elimination of complete or half cycles within a period (typically 17.5ms) without noticeable flicker. Fourteen different levels of lamp intensity can be obtained in this manner. A line synced ramp is set up with the desired period and applied to terminal No. 9 of the differential amplifier within the zero-voltage switch, as shown in Figure 48. The other side of the differential amplifier (terminal No. 13) uses a variable reference level, set by the 50K potentiometer. A change of the potentiometer setting changes the lamp intensity.

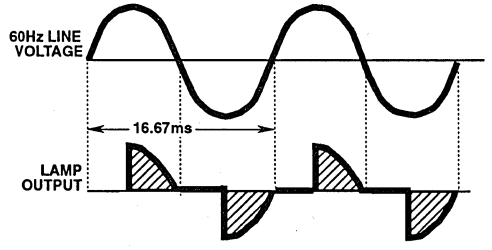


FIGURE 46. WAVEFORMS FOR 60Hz PHASE CONTROLLED LAMP DIMMER

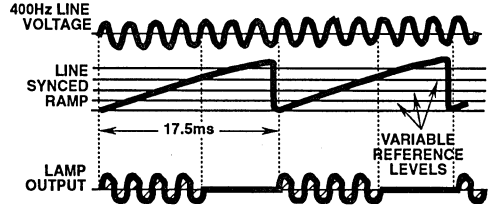


FIGURE 47. WAVEFORMS FOR 400Hz ZERO-VOLTAGE SWITCHED LAMP DIMMER

In 400Hz applications it may be necessary to widen and shift the zero-voltage switch output pulse (which is typically 12ms wide and centered on zero-voltage crossing), to assure that sufficient latching current is available. The 4K resistor (terminal No. 12 to common) and the 0.015µF capacitor (terminal No. 5 to common) are used for this adjustment.

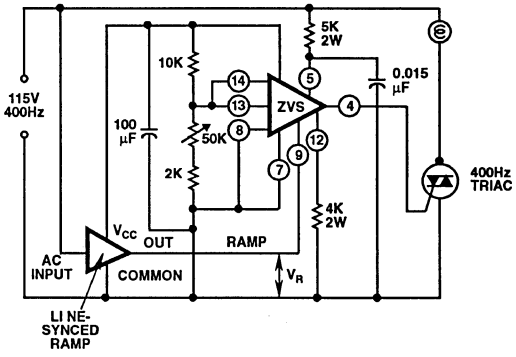


FIGURE 48. CIRCUIT DIAGRAM FOR 400Hz ZERO-VOLTAGE SWITCHED LAMP DIMMER

Solid-State Traffic Flasher

Another application which illustrates the versatility of the zero-voltage switch, when used with Harris thyristors, involves switching traffic control lamps. In this type of application, it is essential that a triac withstand a current surge of the lamp load on a continuous basis. This surge results from the difference between the cold and hot resistance of the tungsten filament. If it is assumed that triac turn-on is at 90 degrees from the zero-voltage crossing, the first current surge peak is approximately ten times the peak steady state rms value.

When the triac randomly switches the lamp, the rate of current rise di/dt is limited only by the source inductance. The triac di/dt rating may be exceeded in some power systems. In many cases, exceeding the rating results in excessive current concentrations in a small area of the device which may produce a hot spot and lead to device failure. Critical applications of this nature require adequate drive to the triac gate for fast turn on. In this case, some inductance may be required in the load circuit to reduce the initial magnitude of the load current when the triac is passing through the active region. Another method may be used which involves the switching of the triac at zero line voltage. This method involves the supply of pulses to the triac gate only during the presence of zero voltage on the AC line.

Figure 49 shows a circuit in which the lamp loads are switched at zero line voltage. This approach reduces the initial di/dt, decreases the required triac surge current ratings, increases the operating lamp life, and eliminates RFI problems. This circuit consists of two triacs, a flip-flop (FF-1), the zero-voltage switch, and a diac pulse generator. The flashing rate in this circuit is controlled by potentiometer R, which provides between 10 and 120 flashes per minute. The state of FF-1 determines the triggering of triacs Y_1 or Y_2 by the output pulses at terminal 4 generated by the zero crossing circuit. Transistors Q_1 and Q_2 inhibit these pulses to the gates of the triacs until the triacs turn on by the logical "1" (V_{CC} high) state of the flip-flop.

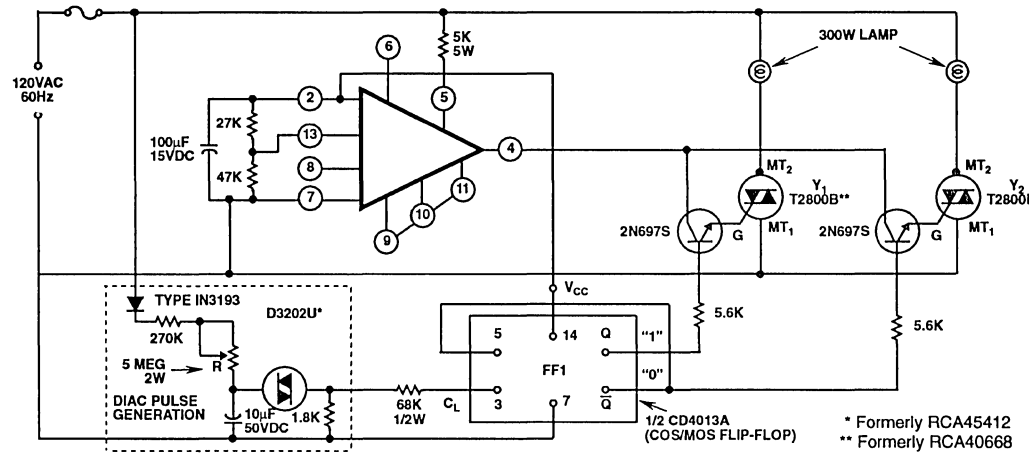


FIGURE 49. SYNCHRONOUS SWITCHING TRAFFIC FLASHER

The arrangement describe can also be used for a synchronous, sequential traffic controller system by addition of one triac, one gating transistor, a "divide-by-three" logic circuit, and modification in the design of the diac pulse generator. Such a system can control the familiar red, amber, and green traffic signals that are found at many intersections.

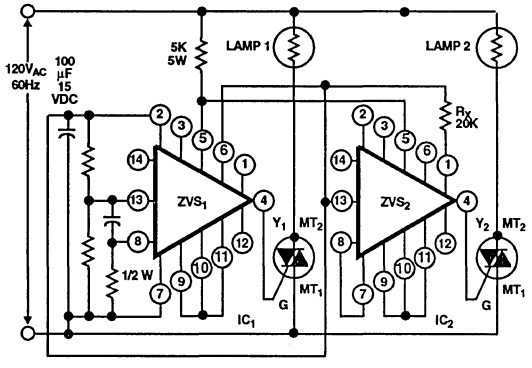


FIGURE 50. SYNCHRONOUS LIGHT FLASHER

Synchronous Light Flasher

Figure 50 shows a simplified version of the synchronous switching traffic light flasher shown in Figure 49. Flash rate is set by use of the curve shown in Figure 16. If a more precise flash rate is required, the ramp generator described previously may be used. In this circuit, ZVS_1 is the master control unit and ZVS_2 is slaved to the output of ZVS_1 through its inhibit terminal (terminal 1). When power is applied to lamp No. 1, the voltage of terminal 6 on ZVS_1 is high and ZVS_2 is inhibited by the current in R_X. When lamp No. 1 is off, ZVS_2 is not inhibited, and triac Y_2 can fire. The power supplies operate in parallel. The on/off sensing amplifier in ZVS_2 is not used.

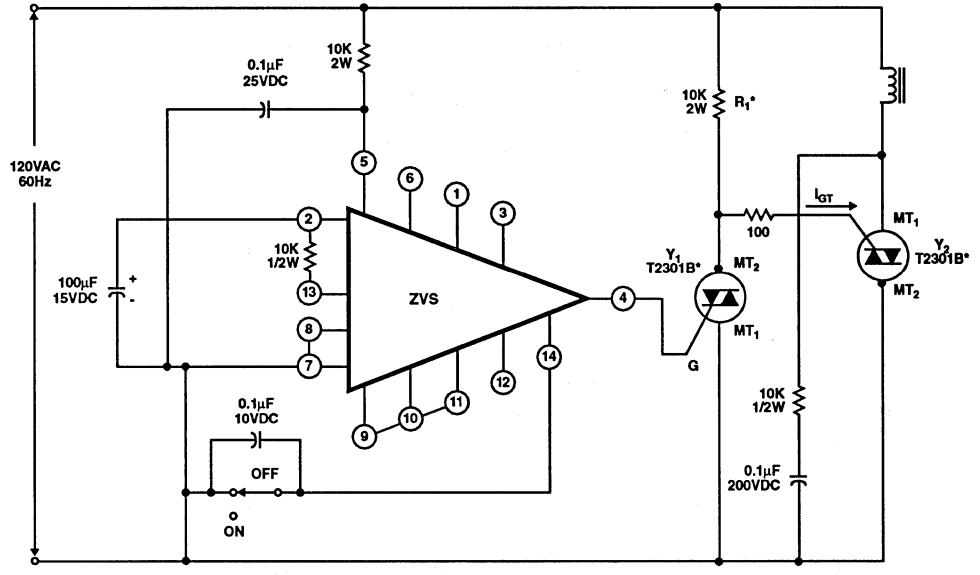
Transient Free Switch Controllers

The zero-voltage switch can be used as a simple solid-state switching device that permits AC currents to be turned on or off with a minimum of electrical transients and circuit noise.

The circuit shown in Figure 51 is connected so that, after the control terminal 14 is opened, the electronic logic waits until the power line voltage reaches a zero crossing before power is applied to the load Z_L. Conversely, when the control terminals are shorted, the load current continues until it reaches a zero crossing. This circuit can switch a load at zero current whether it is resistive or inductive.

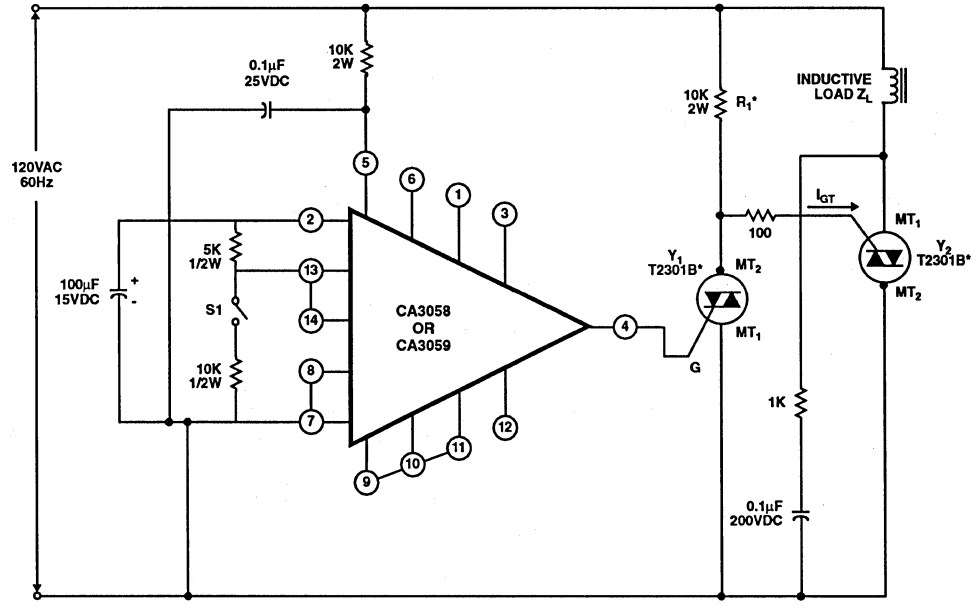
The circuit shown in Figure 52 is connected to provide the opposite control logic to that of the circuit shown in Figure 51. That is, when the switch is closed, power is supplied to the load, and when the switch is opened, power is removed from the load.

In both configurations, the maximum rms load current that can be switched depends on the rating of triac Y_2. If Y_2 is a 2N5444 triac, an rms current of 40A can be switched.



* If Y_2, For Example, is a 40A TRIAC, then R_1 must be Decreased to Supply Sufficient I_{GT} for Y_2

FIGURE 51. ZERO-VOLTAGE SWITCH TRANSIENT FREE SWITCH CONTROLLER IN WHICH POWER IS SUPPLIED TO THE LOAD WHEN THE SWITCH IS OPEN



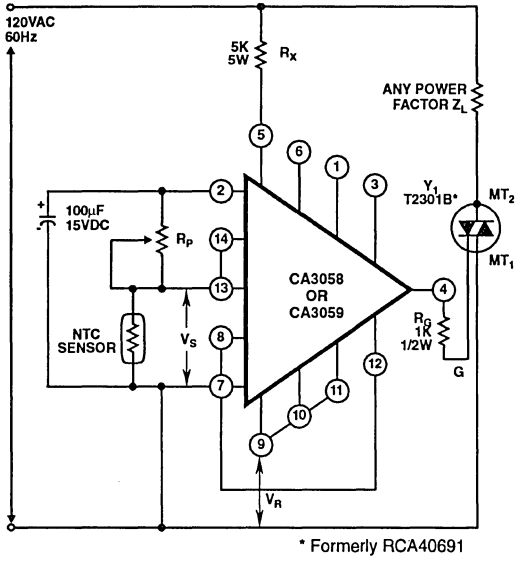
* If Y_2, For Example, is a 40A TRIAC, then R_1 mustbe Decreased to Supply Sufficient I_{GT} for Y_2

FIGURE 52. ZERO-VOLTAGE SWITCH TRANSIENT FREE SWITCH CONTROLLER IN WHICH POWER IS APPLIED TO THE LOAD WHEN THE SWITCH IS CLOSED

Differential Comparator for Industrial Use

Differential comparators have found widespread use as limit detectors which compare two analog input signals and provide a go/no-go, logic "one" or logic "zero" output, depending upon the relative magnitudes of these signals. Because the signals are often at very low voltage levels and very accurate discrimination is normally required between them, differential comparators in many cases employ differential amplifiers as a basic building block. However, in many industrial control applications, a high performance differential comparator is not required. That is, high resolution, fast switching speed, and similar features are not essential. The zero-voltage switch is ideally suited for use in such applications. Connection of terminal 12 to terminal 7 inhibits the zero-voltage threshold detector of the zero-voltage switch, and the circuit becomes a differential comparator.

Figure 53 shows the circuit arrangement for use of the zero-voltage switch as a differential comparator. In this application, no external DC supply is required, as is the case with most commercially available integrated circuit comparators; of course, the output current capability of the zero-voltage switch is reduced because the circuit is operating in the DC mode. The 1000Ω resistor R_G, connected between terminal 4 and the gate of the triac, limits the output current to approximately 3mA.



* Formerly RCA40691

FIGURE 53. DIFFERENTIAL COMPARATOR USING THE CA3058 OR CA3059 INTEGRATED CIRCUIT ZERO-VOLTAGE SWITCH

When the zero-voltage switch is connected in the DC mode, the drive current for terminal 4 can be determined from a curve of the external load current as a function of DC voltage from terminals 2 and 7. Of course, if additional output current is required, an external DC supply may be connected between terminals 2 and 7, and resistor R_X (shown in Figure 53) may be removed.

The chart below compares some of the operating characteristics of the zero-voltage switch, when used as a comparator, with a typical high performance commercially available integrated circuit differential comparator.

PARAMETERS	ZERO-VOLTAGE SWITCH (TYP. VALUE)	TYP. INTEGRATED CIRCUIT COMPARATOR (710)
Sensitivity	30mV	2mV
Switching Speed (Rise Time)	>20µs	90ns
Output Drive Capability	*4.5V at ≤4mA	3.2V at ≤5.0mA

* Refer to Figure 20; R_X equals 5000Ω

Power One Shot Control

Figure 54 shows a circuit which triggers a triac for one complete half cycle of either the positive or negative alternation of the AC line voltage. In this circuit, triggering is initiated by the push button PB-1, which produces triggering of the triac near zero voltage even though the button is randomly depressed during the AC cycle. The triac does not trigger again until the button is released and again depressed. This type of logic is required for the solenoid drive of electrically operated stapling guns, impulse hammers, and the like, where load current flow is required for only one complete half cycle. Such logic can also be adapted to keyboard consoles in which contact bounce produces transmission of erroneous information.

In the circuit of Figure 54, before the button is depressed, both flip-flop outputs are in the "zero" state. Transistor Q_G is biased on by the output of flip-flop FF-1. The differential comparator which is part of the zero-voltage switch is initially biased to inhibit output pulses. When the push button is depressed, pulses are generated, but the state of Q_G determines the requirement for their supply to the triac gate. The first pulse generated serves as a "framing pulse" and does not trigger the triac but toggles FF-1. Transistor Q_G is then turned off. The second pulse triggers the triac and FF-1 which, in turn, toggles the second flip-flop FF-2. The output of FF-2 turns on transistor Q_7, as shown in Figure 55, which inhibits any further output pulses. When the push-button is released, the circuit resets itself until the process is repeated with the button. Figure 56 shows the timing diagram for the described operating sequence.

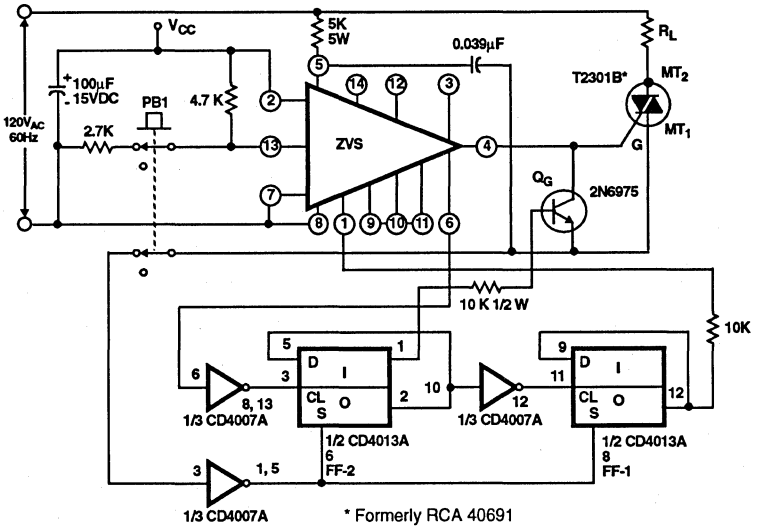


FIGURE 54. BLOCK DIAGRAM OF A POWER ONE SHOT CONTROL USING A ZERO-VOLTAGE SWITCH

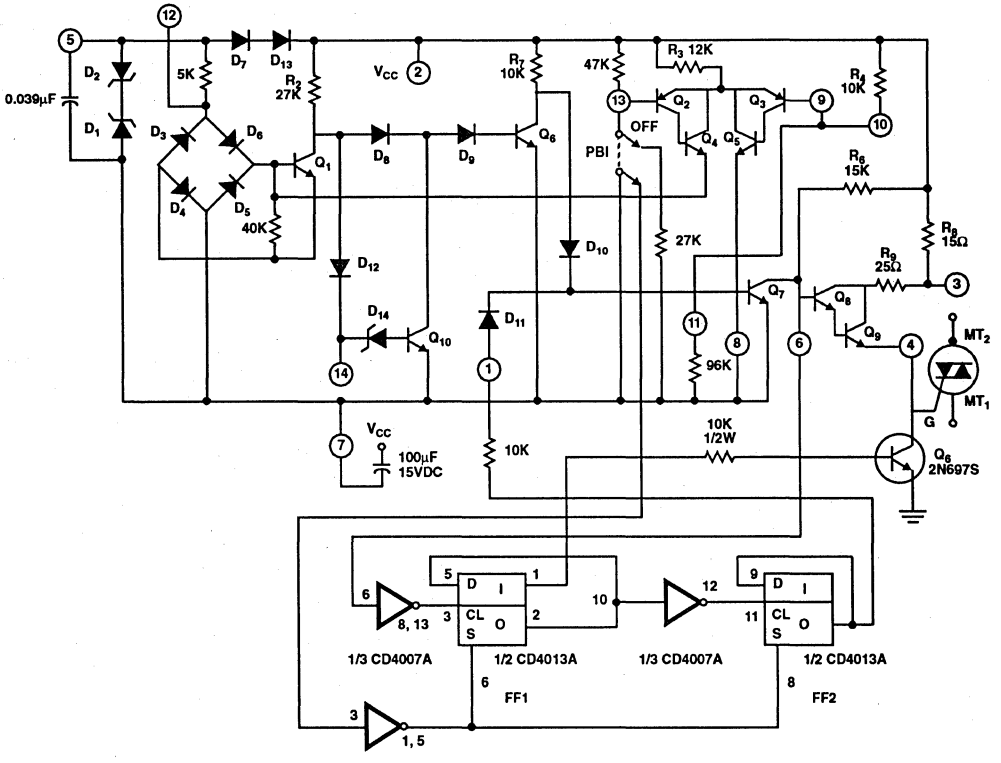


FIGURE 55. CIRCUIT DIAGRAM FOR THE POWER ONE SHOT CONTROL

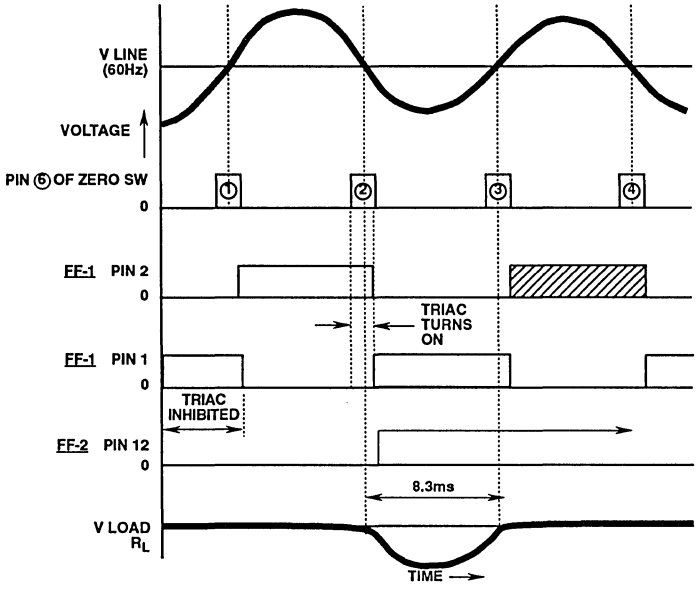
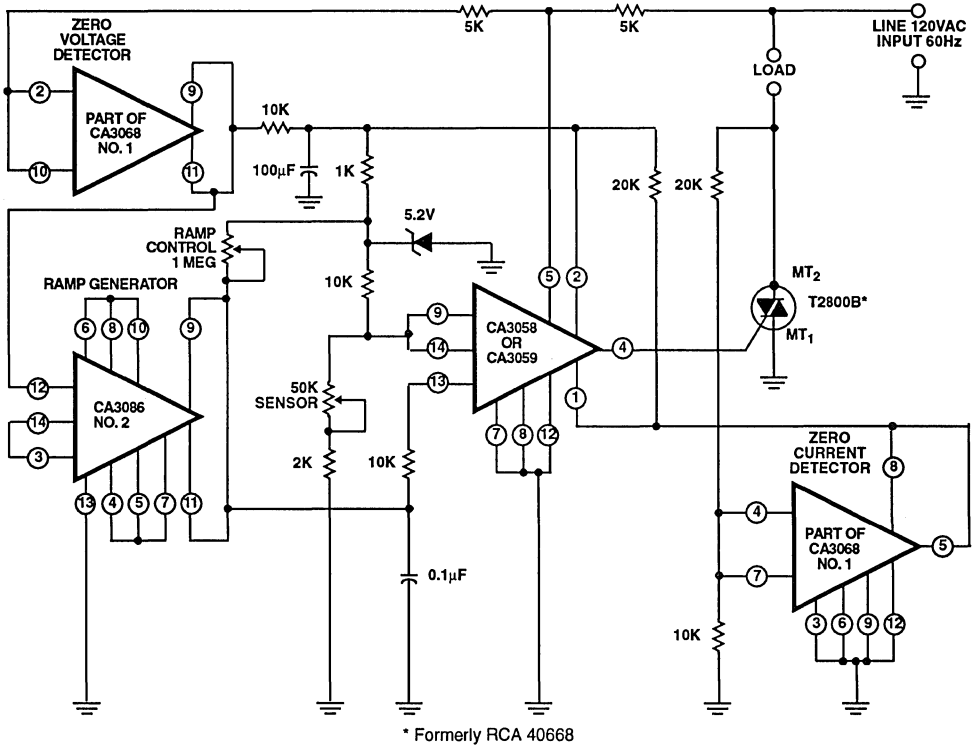


FIGURE 56. TIMING DIAGRAM FOR THE POWER ONE SHOT CONTROL



* Formerly RCA 40668

FIGURE 57. PHASE CONTROL CIRCUIT USING A CA3058 OR CA3059 AND TWO CA3086 INTEGRATED CIRCUITS

Phase Control Circuit

Figure 57 shows a circuit using a CA3058 or CA3059 zero-voltage switch together with two CA3086 integrated circuit arrays to form a phase control circuit. This circuit is specifically designed for speed control of AC induction motors, but may also be used as a light dimmer. The circuit, which can be operated from a line frequency of 50Hz to 400Hz, consists of a zero-voltage detector, a line synchronized ramp generator, a zero current detector, and a line derived control circuit (i.e., the zero-voltage switch). The zero-voltage detector (part of CA3086 No. 1) and the ramp generator (CA3086 No. 2) provide a line synchronized ramp voltage output to terminal 13 of the zero-voltage switch. The ramp voltage, which has a starting voltage of 1.8V, starts to rise after the line voltage passes the zero point. The ramp generator has an oscillation frequency of twice the incoming line frequency. The slope of the ramp voltage can be adjusted by variation of the resistance of the 1MΩ ramp control potentiometer. The output phase can be controlled easily to provide 180° firing of the triac by programming the voltage at terminal 9 of the zero-voltage switch. The basic operation of the zero-voltage switch driving a thyristor with an inductive load was explained previously in the discussion on switching of inductive loads.

On/Off Touch Switch

The on/off touch switch shown in Figure 58 uses the CA3240E to sense small currents flowing between two contact points on a touch plate consisting of a PC board metallization "grid". When the on plate is touched, current flows between the two halves of the grid, causing a positive shift in the output voltage (terminal 7) of the CA3240E. These positive transitions are fed into the CA3059, which is used as a latching circuit and zero crossing triac driver. When a positive pulse occurs at terminal No. 7 of the CA3240E, the triac is turned on and held on by the CA3059 and associated positive feedback circuitry (51kΩ resistor and 36kΩ/42kΩ voltage divider). When the pulse occurs at terminal No. 1, the triac is turned off and held off in a similar manner. Note that power for the CA3240E is derived from the CA3059 internal power supply. The advantage of using the CA3240E in this circuit is that it can sense the small currents associated with skin conduction while maintaining sufficiently high circuit impedance to protect against electrical shock.

Triac Power Controls for Three Phase Systems

This section describes recommended configurations for power control circuits intended for use with both inductive and resistive balanced three phase loads. The specific design requirements for each type of loading condition are discussed.

In the power control circuits described, the integrated circuit zero-voltage switch is used as the trigger circuit for the power triacs. The following conditions are also imposed in the design of the triac control circuits:

1. The load should be connected in a three wire configuration with the triacs placed external to the load; either delta or wye arrangements may be used. Four wire loads in wye configurations can be handled as three independent single phase systems. Delta configurations in which a triac is connected within each phase rather than in the incoming lines can also be handled as three independent single phase systems.
2. Only one logic command signal is available for the control circuits. This signal must be electrically isolated from the three phase power system.
3. Three separate triac gating signals are required.
4. For operation with resistive loads, the zero-voltage switching technique should be used to minimize any radio frequency interference (RFI) that may be generated.

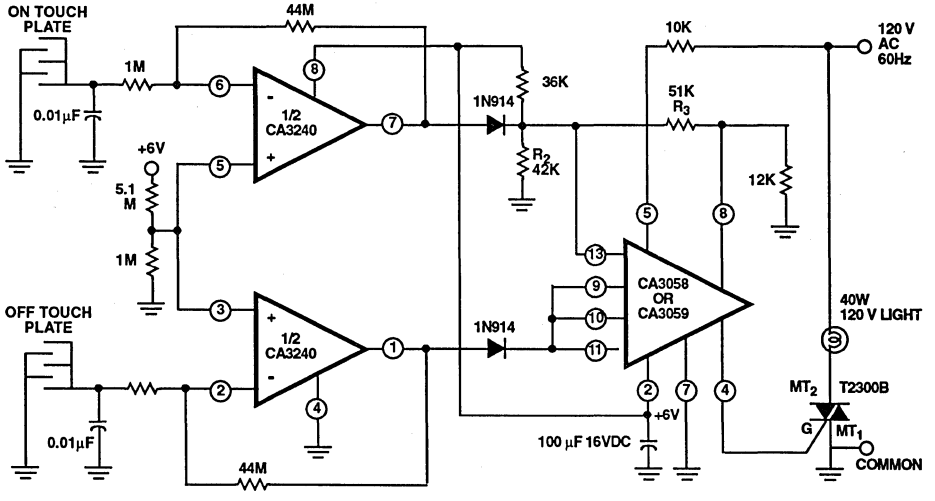


FIGURE 58. ON/OFF TOUCH SWITCH

Isolation of DC Logic Circuitry

As explained earlier under **Special Application considerations**, isolation of the DC logic circuitry* from the AC line, the triac, and the load circuit is often desirable even in many single phase power control applications. In control circuits for polyphase power systems, however, this type of isolation is essential, because the common point of the DC logic circuitry cannot be referenced to a common line in all phases.

* The DC logic circuitry provides the low level electrical signal that dictates the state of the load. For temperature controls, the DC logic circuitry includes a temperature sensor for feedback. The Harris integrated circuit zero-voltage switch, when operated in the DC mode with some additional circuitry, can replace the DC logic circuitry for temperature controls.

In the three phase circuits described in this section, photo optic techniques (i.e., photo coupled isolators) are used to provide the electrical isolation of the DC logic command signal from the AC circuits and the load. The photo coupled isolators consist of an infrared light emitting diode aimed at a silicon photo transistor, coupled in a common package. The light emitting diode is the input section, and the photo transistor is the output section. The two components provide a voltage isolation typically of 1500V. Other isolation techniques, such as pulse transformers, magnetoresistors, or reed relays, can also be used with some circuit modifications.

Resistive Loads

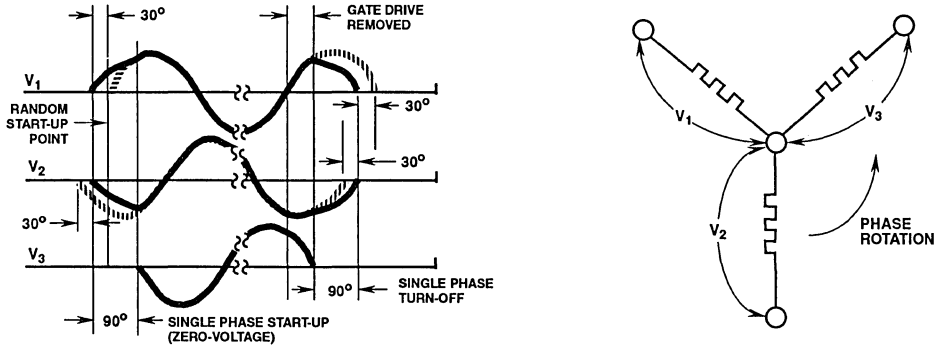
Figure 59 illustrates the basic phase relationships of a balanced three phase resistive load, such as may be used in heater applications, in which the application of load power is controlled by zero-voltage switching. The following conditions are inherent in this type of application:

1. The phases are 120 degrees apart; consequently, all three phases cannot be switched on simultaneously at zero voltage.
2. A single phase of a wye configuration type of three wire system cannot be turned on.
3. Two phases must be turned on for initial starting of the system. These two phases form a single phase circuit which is out of phase with both of its component phases. The single phase circuit leads on phase by 30 degrees and lags the other phase by 30 degrees.

These conditions indicate that in order to maintain a system in which no appreciable RFI is generated by the switching action from initial starting through the steady state operating condition, the system must first be turned on, by zero-voltage switching, as a single phase circuit and then must revert to synchronous three phase operation.

Figure 60 shows a simplified circuit configuration of a three phase heater control that employs zero-voltage synchronous switching in the steady state operating condition, with random starting. In this system, the logic command to turn on the system is given when heat is required, and the command to turn off the system is given when heat is not required. Time proportioning heat control is also possible through the use of logic commands.

The three photo coupled inputs to the three zero-voltage switches change state simultaneously in response to a "logic command". The zero-voltage switches then provide a positive pulse, approximately 100µs in duration, only at a zero-voltage crossing relative to their particular phase. A balanced three phase sensing circuit is set up with the three zero-voltage switches each connected to a particular phase on their common side (terminal 7) and referenced at their high side (terminal 5), through the current limiting resistors R_4, R_5, and R_6, to an established artificial neutral point. This artificial neutral point is electrically equivalent to the inaccessible neutral point of the wye type of three wire load



(a) (b)

NOTE: The dashed lines indicate the normal relationship of the phases under steady state conditions. The deviation at start up and turn off should be noted.

FIGURE 59. VOLTAGE PHASE RELATIONSHIP FOR A THREE PHASE RESISTIVE LOAD WHEN THE APPLICATION OF LOAD POWER IS CONTROLLED BY ZERO-VOLTAGE SWITCHING: (a) VOLTAGE WAVEFORMS, (b) LOAD CIRCUIT ORIENTATION OF VOLTAGES.

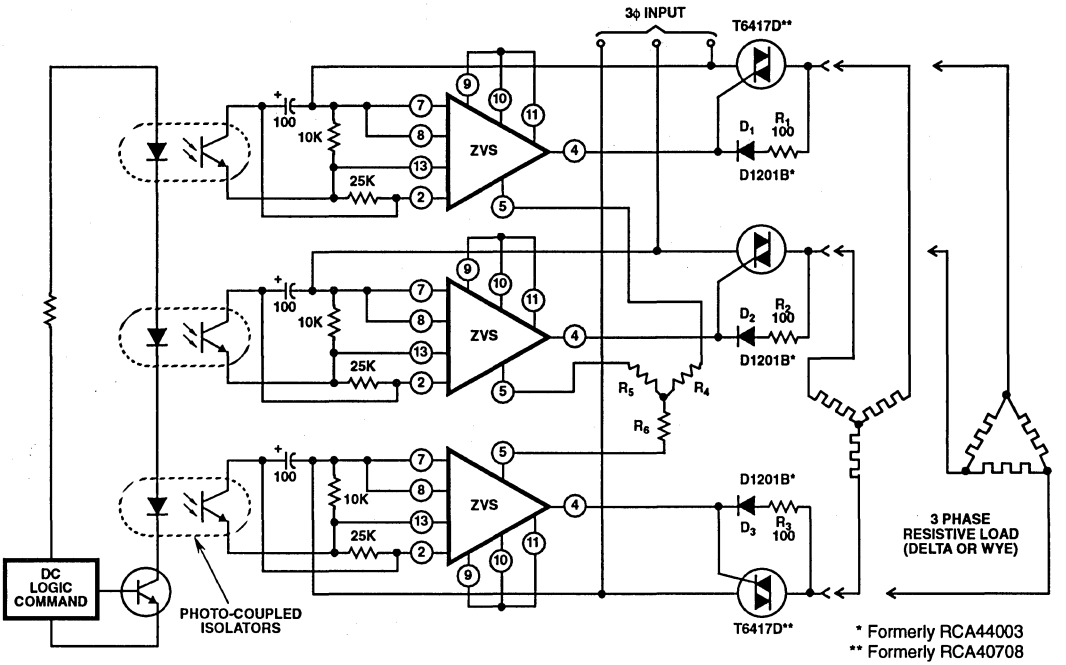


FIGURE 60. SIMPLIFIED DIAGRAM OF A THREE PHASE HEATER CONTROL THAT EMPLOYS ZERO-VOLTAGE SYNCHRONOUS SWITCHING IN THE STEADY STATE OPERATING CONDITIONS

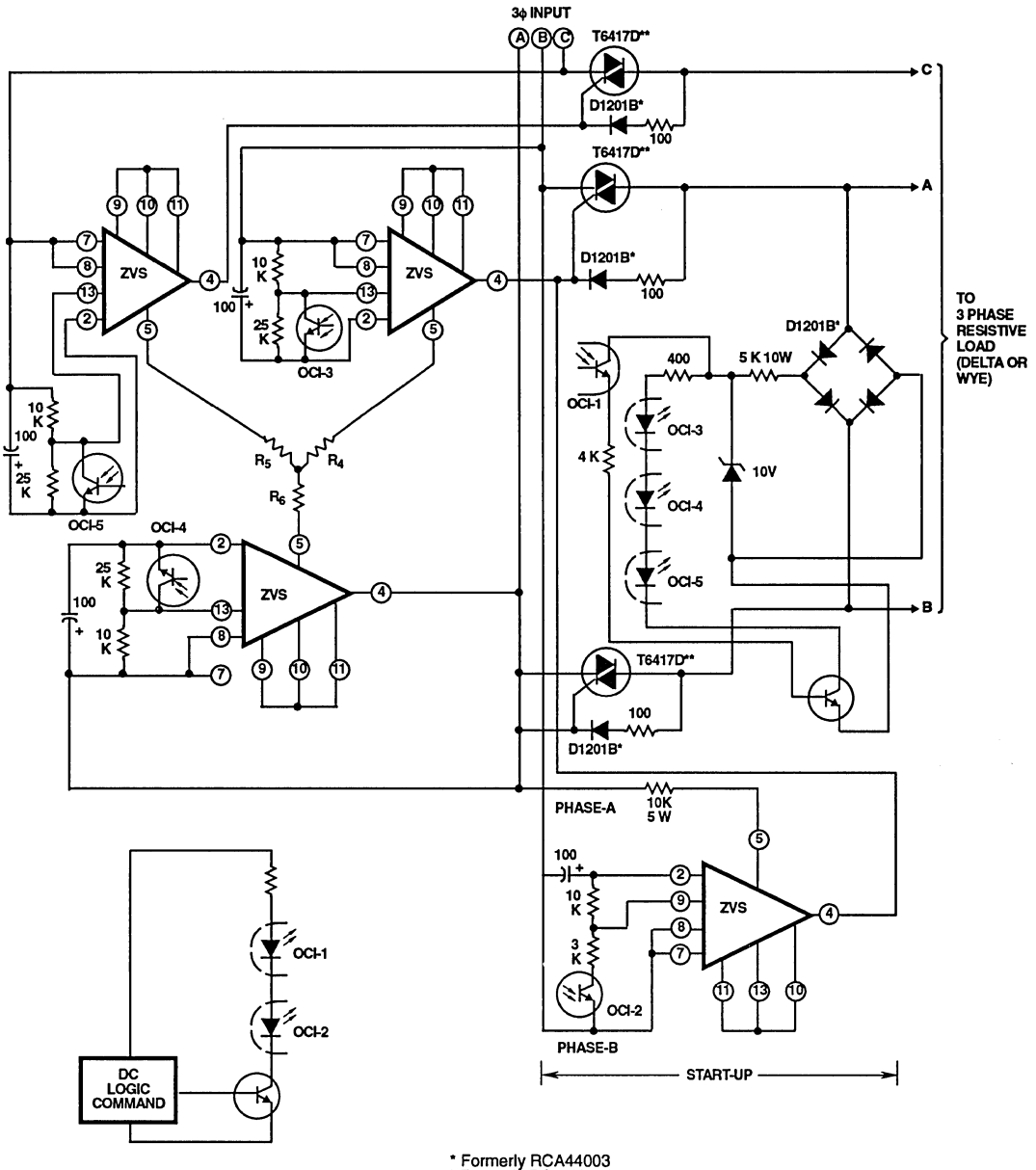
and, therefore, is used to establish the desired phase relationships. The same artificial neutral point is also used to establish the proper phase relationships for a delta type of three wire load. Because only one triac is pulsed on at a time, the diodes (D_1, D_2, and D_3) are necessary to trigger the opposite polarity triac, and, in this way, to assure initial latching on of the system. The three resistors (R_1, R_2, and R_3) are used for current limiting of the gate drive when the opposite polarity triac is triggered on by the line voltage.

In critical applications that require suppression of all generated RFI, the circuit shown in Figure 61 may be used. In addition to synchronous steady state operating conditions, this circuit also incorporates a zero-voltage starting circuit. The start up condition is zero-voltage synchronized to a single phase, 2 wire, line-to-line circuit, comprised of phases A and B. The logic command engages the single phase start up zero-voltage switch and three phase photo coupled isolators OC13, OC14, OC15 through the photo coupled isolators OC11 and OC12. The single phase zero-voltage switch, which is synchronized to phases A and B, starts the system at zero voltage. As soon as start up is accomplished, the three photo coupled isolators OC13, OC14, and OC15 take control, and three phase synchronization begins. When the "logic command" is turned off, all control is ended, and the triacs automatically turn off when the sine wave current decreases to zero. Once the first phase turns off, the other two will turn off simultaneously, 90° later, as a single phase line-to-line circuit, as is apparent from Figure 59.

Inductive Loads

For inductive loads, zero-voltage turn on is not generally required because the inductive current cannot increase instantaneously; therefore, the amount of RFI generated is usually negligible. Also, because of the lagging nature of the inductive current, the triacs cannot be pulse fired at zero voltage. There are several ways in which the zero-voltage switch may be interfaced to a triac for inductive load applications. The most direct approach is to use the zero-voltage switch in the DC mode, i.e., to provide a continuous DC output instead of pulses at points of zero-voltage crossing. This mode of operation is accomplished by connection of terminal 12 to terminal 7, as shown in Figure 62. The output of the zero-voltage switch should also be limited to approximately 5mA in the DC mode by the 750Ω series resistor. Use of a triac such as the T2301D* is recommended for this application. Terminal 3 is connected to terminal 2 to limit the steady state power dissipation within the zero-voltage switch. For most three phase inductive load applications, the current handling capability of the 40692 triac (2.5A) is not sufficient. Therefore, the 40692 is used as a trigger triac to turn on any other currently available power triac that may be used. The trigger triac is used only to provide trigger pulses to the gate of the power triac (one pulse per half cycle); the power dissipation in this device, therefore, will be minimal.

Simplified circuits using pulse transformers and reed relays will also work quite satisfactorily in this type of application. The RC networks across the three power triacs are used for suppression of the commutating dv/dt when the circuit operates into inductive loads.



* Formerly RCA44003
** Formerly RCA 40708

FIGURE 61. THREE PHASE POWER CONTROL THAT EMPLOYS ZERO-VOLTAGE SYNCHRONOUS SWITCHING BOTH FOR STEADY STATE OPERATION AND FOR STARTING

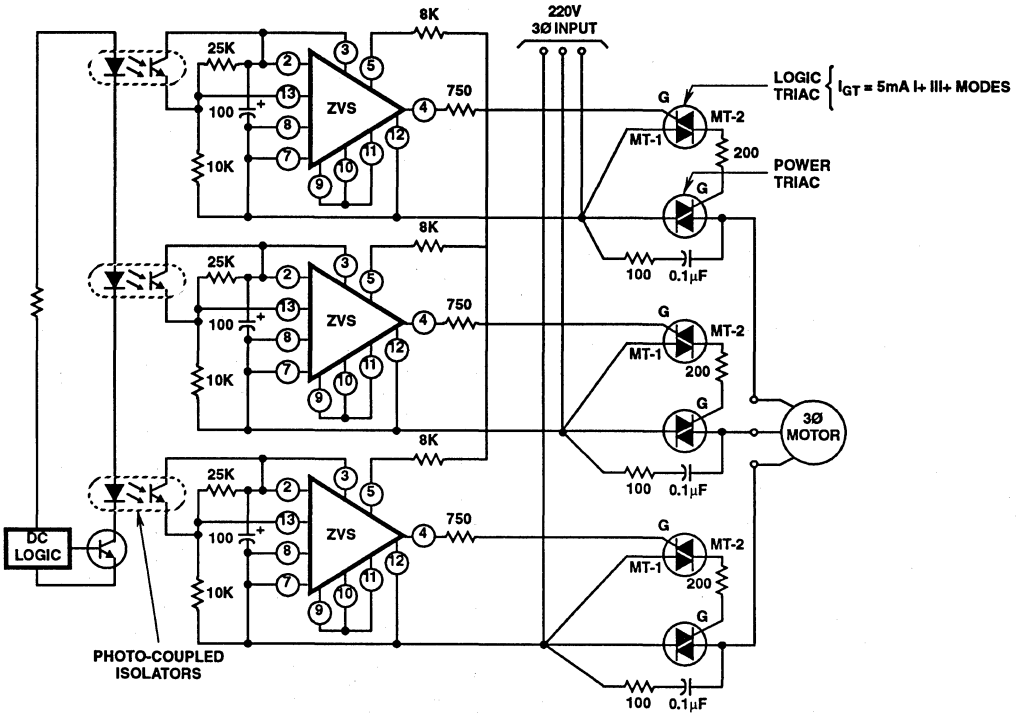


FIGURE 62. TRIAC THREE PHASE CONTROL CIRCUIT FOR AN INDUCTIVE LOAD, i.e., THREE PHASE MOTOR

Harris Semiconductor

APPNOTE

No. 6915 May 1992

Harris Intelligent Power

APPLICATION OF THE CA1524 SERIES PULSE-WIDTH MODULATOR ICs

Author: Carmine Salerno

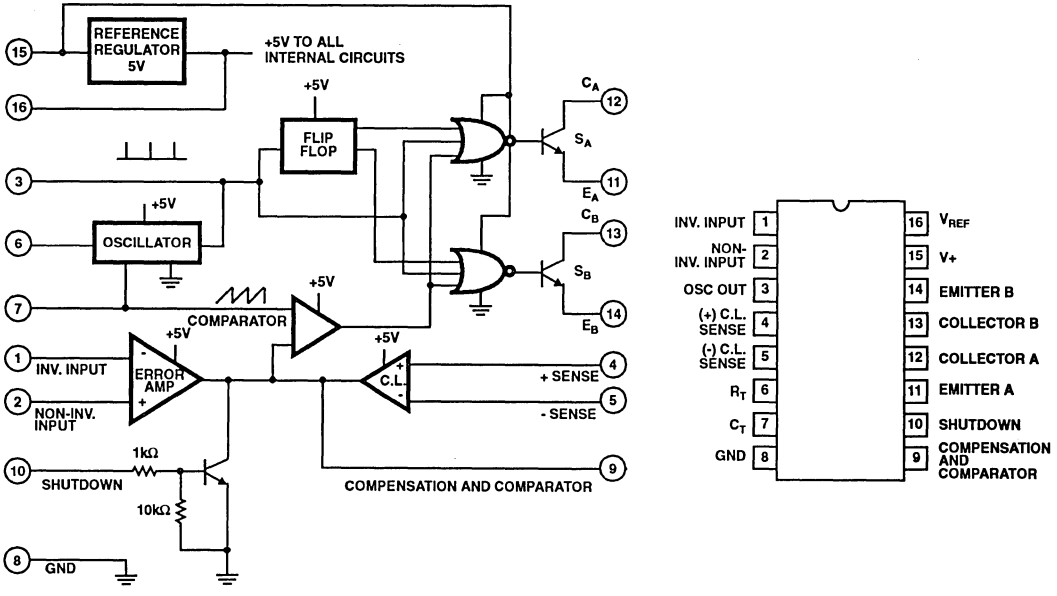
This application note reviews pulse-width modulated (PWM) circuits, and the CA1524 series of pulse-width modulator ICs particularly intended for this type of application. It also includes descriptions of basic switching-regulator circuits, the generic CA1524 Series IC, its use in a variable switched power supply application, together with a variety of its unique circuit applications.

The CA1524, CA2524, and CA3524 Series, a family of integrated circuits containing a pulse-width modulator and related control circuits, are particularly applicable to switching regulators, flyback converters, dc-to-dc converters and the like. These ICs operate with a power supply in the 8V to 40V range for use in both low and high power regulators. The CA1524 series ICs contain the following circuit functions: 5V temperature compensated zener reference, precision RC oscillator, transconductance error amplifier, current-limiting amplifier, control comparator, shutdown circuit, and dual output transistor switches. These circuit functions make these devices attractive for a wide variety of other applications; e.g., low frequency pulse generators, automotive temperature voltage regulators, battery chargers, electronic bathroom scales, etc.

The CA1524 family of ICs is supplied in 16 lead plastic and ceramic (frit) packages, and is also available in chip form.

CA1524 Series IC Features

The CA1524 PWM on-chip functions shown in the functional block diagram of Figure 1 include an error amplifier, a comparator, an oscillator, a flip-flop, and a voltage regulator. The error amplifier senses the difference between the actual and the desired regulator output and applies this signal to the comparator's positive input. The output of this stage is in turn a function of the error signal and the oscillator's ramp voltage.



a) FUNCTIONAL BLOCK DIAGRAM

b) TERMINAL CONNECTION DIAGRAM

FIGURE 1. CA1524 SERIES ICs

The oscillator's output pulses alternately trigger the flip-flop, whose output ultimately provides the circuits push-pull drive signal via the NOR-gates and the output transistors. The other NOR-gate inputs control the duration of the output pulses. Depending upon the oscillator's output level (high or low) and the comparator's high or low status, the "on" duty-cycle of the NOR gate can vary from 0 to 45 percent. It should be noted, that the NOR gates are on alternately. Thus, by connecting the output transistors in parallel, an effective on time of 0% to 90% and a wide voltage regulation range can be attained.

Comparative Operating Efficiencies in Series-Pass and PWM Types of Voltage Regulators

The series-pass circuit is a classical means of implementing the voltage regulator function; its simple and easy to design, but comparatively inefficient when required to operate over a range of supply voltages and output currents. The need to improve operational efficiency, in recent years, has been one of the major factors motivating engineers to use the PWM type of voltage regulator despite its greater circuit complexity.

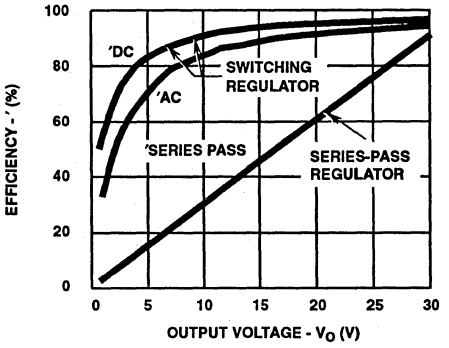
Figure 2 shows the high operating efficiency of the PWM type of voltage regulator design e.g., using CA1524 and compares it with that of a conventional linear series-pass circuit. In a series-pass type of regulated power supply, the pass transistor is biased in the linear region, to permit good line and load regulation and dynamic response, but at a sacrifice in efficiency. This loss in efficiency occurs as a result of the power dissipated in the pass transistor, i.e., the product of the voltage drop and the current flowing through it. In a series-pass regulator, the output current is about equal to the input current, therefore, the overall efficiency ≅ the ratio V_O/V_{IN}.

It is, therefore, apparent that the input/output voltage differential must be kept at a minimum if high efficiency is to be achieved. Dissipation in the pass device is $(V_{IN} - V_{DD})$ I_{PASS}, $(V_{IN} - V_O)$ is typically 2V to 3V. There are additional small operating losses in the IC itself. By way of contrast, the pass transistor for a switching-regulator control circuit is driven between two states, "on" and "off", and since the linear region is not used, loss is essentially limited to the product of the saturation voltage and the current flowing through the pass transistor during its on state. There is a small additional loss that occurs during the on/off transitions.

Additional losses in the switching regulator include diode-voltage losses, inductor-transformer core losses, and copper losses. The overall efficiency is essentially independent of input voltage or input current. A worst case theoretical value of the AC switching and DC transistor losses approaches a value equal to $V_O/(V_O + 2V)$ (assuming a diode V_{BE} and transistor V_{CE}(s) of 1V each). Therefore, a minimum input voltage of $V_O + 2V$ is needed to operate a switching regulator.

Circuit Description

The CA1524, CA2524, and CA3524 monolithic integrated circuits are designed to provide all of the control circuitry necessary for a broad range of switching regulator applications. On-chip functional blocks, shown in Figure 1, include a zener voltage reference, transconductance error amplifier, precision RC oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches, and current limiting and shutdown circuitry. A complete schematic is shown in Figure 4



Pulse Width Modulator (PWM) Switching	Regulator Linear	Series-Pass Regulator

$$\eta_{DC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_{O1}} = \frac{V_O}{V_O + 1} \qquad \eta = \frac{P_O}{P_{IN}}$$

$$\eta_{AC} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_{O2}} = \frac{V_O}{V_O + 2} \qquad \eta = \frac{V_O I_O}{V_{IN} I_{IN}} \cong \frac{V_O}{V_{IN}}$$

FIGURE 2. EFFICIENCY CURVES FOR LINEAR (SERIES-PASS) REGULATOR AND PULSE-WIDTH MODULATED SWITCHING REGULATOR (PWM)

Voltage Reference Section

The CA1524 Series devices contain an internal series voltage regulator employing a zener reference to provide a nominal 5 volts output, which is used to bias all internal timing and control circuitry. The output of this regulator is available at terminal 16 and is capable of supplying up to 50mA output current. For higher currents, the circuit of Figure 3 may be used with an external p-n-p transistor and bias resistor. The internal regulator may be bypassed for operation from a fixed 5V supply by connecting both terminal 15 and 16 to the input voltage, which must not exceed 6V.

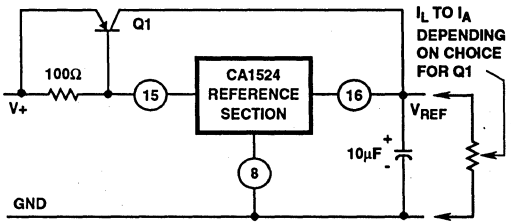


FIGURE 3. CIRCUIT FOR EXPANDING THE REFERENCE CURRENT CAPABILITY

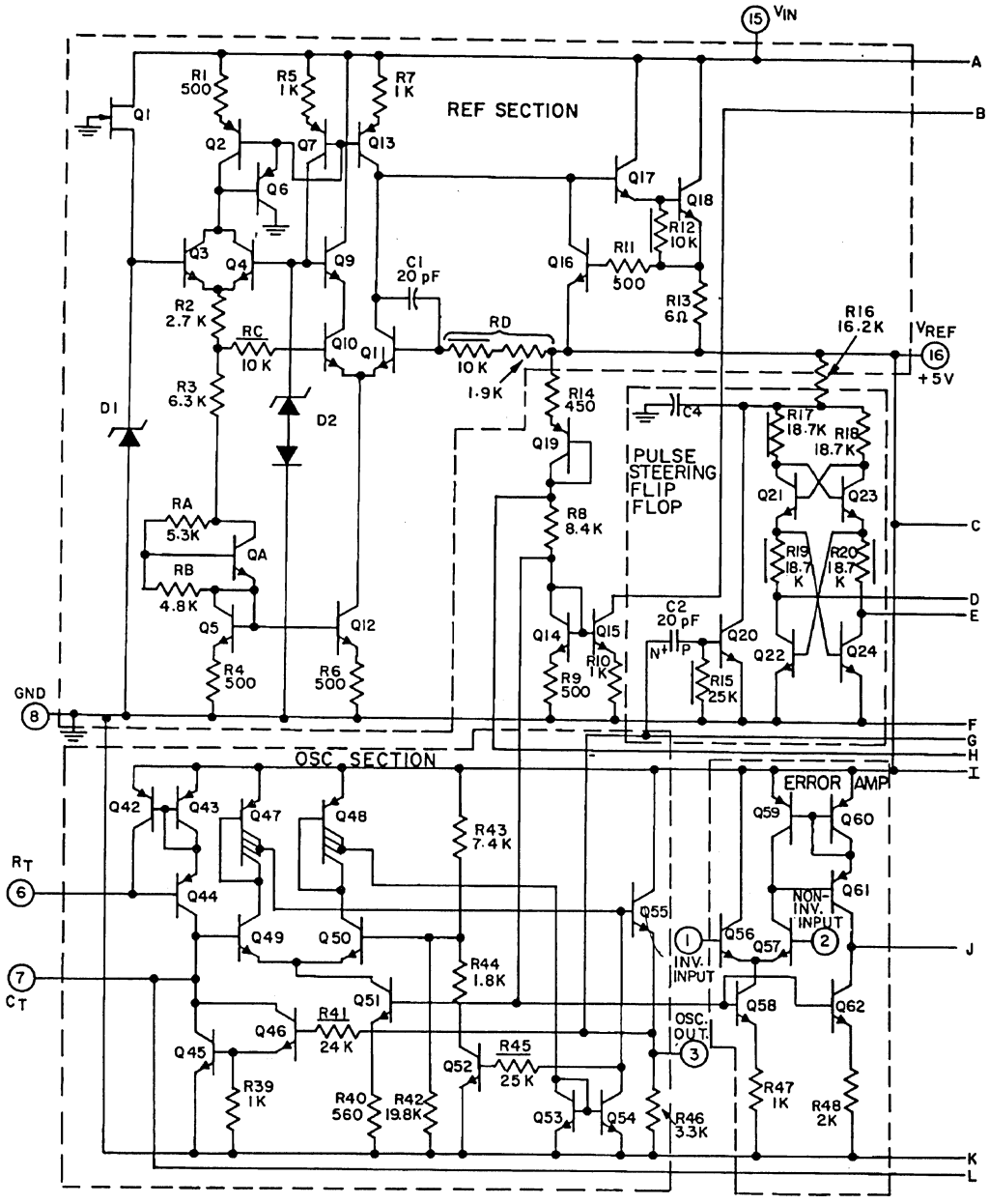


FIGURE 4. SCHEMATIC DIAGRAM OF CA1524 SERIES IC

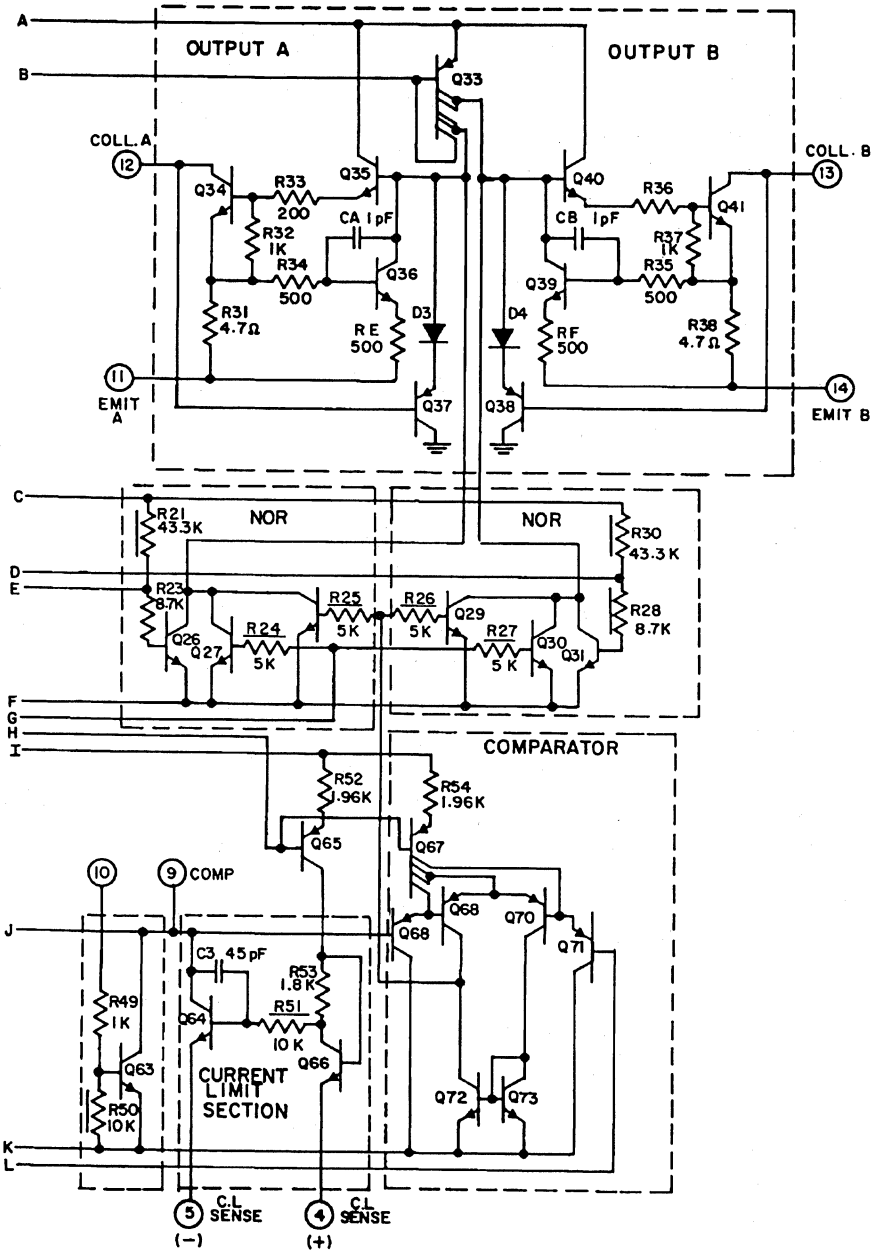


FIGURE 4. SCHEMATIC DIAGRAM OF CA1524 SERIES IC (Continued)

Figure 5 shows the temperature variation of the reference voltage with supply voltages of 8V to 40V and load currents up to 20mA. Load regulation and line regulation curves are shown in Figures 6 and 7, respectively.

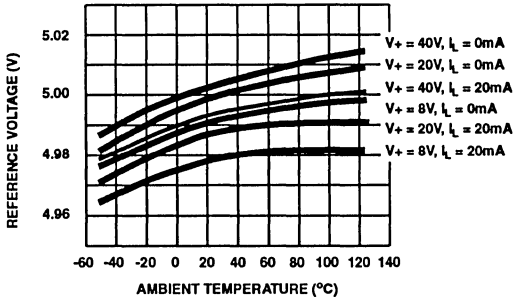


FIGURE 5. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

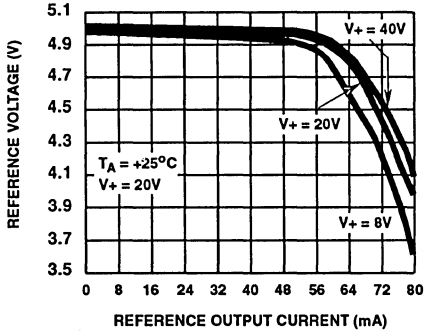


FIGURE 6. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF REFERENCE OUTPUT CURRENT

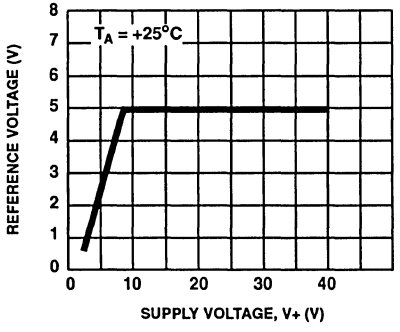


FIGURE 7. TYPICAL REFERENCE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

Oscillator Section

Transistors Q42, Q43 and Q44, in conjunction with an external resistor R_T, establishes a constant charging current into an external capacitor C_T to provide a linear ramp voltage at terminal 7. The ramp voltage has value that ranges from 0.6 to 3.5 volts and is used as the reference for the comparator in the device. The charging current is equal to $(5\text{-}2V_{BE})/R_T$ or approximately $3.6/R_T$ and should be kept within the range of 30µA to 2mA by varying R_T. The discharge time of C_T determines the pulse width of the oscillator output pulse at terminal 3. This pulse has a practical range of 0.5µs to 5µs for a capacitor range of 0.001 to 0.1µF. The pulse has two internal uses: as a dead-time control or blanking pulse to the output stages to assure that both outputs cannot be on simultaneously and as a trigger pulse to the internal flip-flop which alternately enables the output transistors. The output dead-time relationship is shown in Figure 8, a curve which is useful when a value of dead time for a particular switching transistor has to be established. A larger value of dead time will assure that both output transistors in push-pull, bridge, or forward converter configurations will not conduct simultaneously.

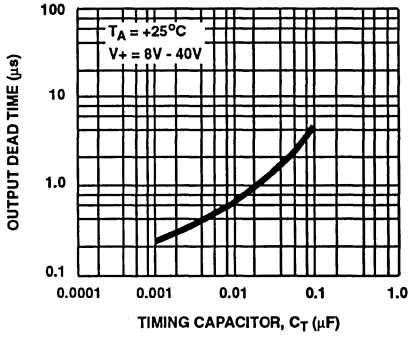


FIGURE 8. TYPICAL OUTPUT STAGE DEAD TIME AS A FUNCTION OF TIMING CAPACITOR VALUE

If a small value of C_T must be used, the pulse width can be further expanded by the addition of a shunt capacitor in the order of 100pF (but no greater then 1000pF), from terminal 3 to ground.

This shunt capacitor will expand the dead time from 0.5µs to 5.0µs when required. When the oscillator output pulse is used as a sync input to an oscilloscope, the cable and input capacitances may increase the pulse width slightly. A 2kΩ resistor at terminal 3 will usually provide sufficient decoupling of the cable. The upper limit of the pulse width is determined by the maximum duty cycle acceptable. To provide an expansion of the dead time without loading the oscillator, the circuit of Figure 9 may be used.

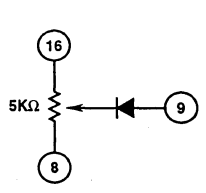


FIGURE 9. CIRCUIT FOR EXPANSION OF DEAD TIME

This diode clamp will limit the output voltage of the error amplifier; it also limits the error amplifier's source output current to about 200µA. Curves for selecting the values of the oscillator resistor (R_T) and the oscillator capacitor (C_T), as a function of oscillator period (t), are shown in Figure 10.

The oscillator period is determined by R_T and C_T, with an approximate value of $t = R_TC_T$, where R_T is in ohms, C_T is in µF, and t is in µs. Excess lead lengths, which product stray capacitances, should be avoided in connecting R_T and C_T to their respective terminals.

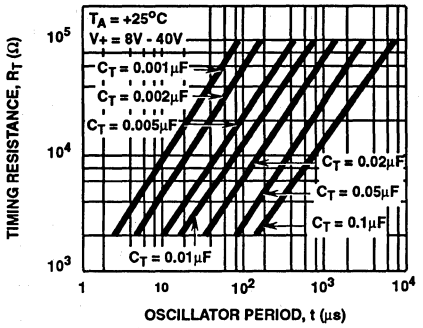


FIGURE 10. TYPICAL OSCILLATOR PERIOD AS A FUNCTION OF R_T AND C_T

For example, to obtain an oscillator period (t), select C_1 = 0.1µF and R_T = 10kΩ. Based on these values the output dead time is 0.7µs. For series regulator applications, the two outputs can be connected in parallel to provide an effective 0% - 90% duty cycle with the output stage frequency being equal to that of the oscillator. Since separate output terminals are provided, push-pull and flyback applications are possible. The flip-flop divides the frequency such that the duty cycle of each output is 0% - 45% and the overall frequency is half that of the oscillator. Curves of the output duty cycle as a function of the voltage at terminal 9 are shown in Figure 11.

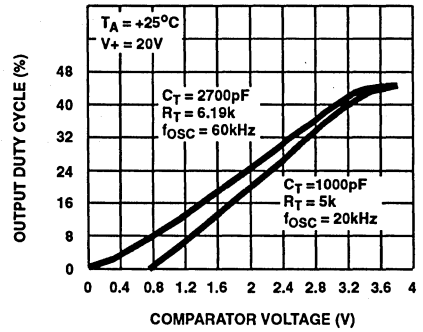


FIGURE 11. TYPICAL DUTY CYCLE AS A FUNCTION OF COMPARATOR VOLTAGE (AT TERMINAL 9)

Error Amplifier Section

The error amplifier consists of a differential pair (Q56, Q57) with an active load (Q61 and Q62) forming a differential transconductance amplifier. Since Q61 is driven by a constant current source, Q62, the output impedance R_{OUT}, terminal 9, is very high (≅ 5MΩ). The gain is:

$$Av = gmR = 8\ Ic\ R/2KT = 10^4,$$

$$\text{where } R = \frac{R_{OUT}R_L}{R_{OUT} = R_L}\ R_L = \infty,\ Av \cong 10^4$$

Since R_{OUT} is extremely high, the gain can be easily reduced from a nominal 10^4 (80dB) by the addition of an external shunt resistor from terminal 9 to ground as shown in Figure 12. The output amplifier terminal is also used to compensate the system for AC stability. The frequency response and phase shift curves are shown in Figure 12. The uncompensated amplifier has a single pole at approximately 250Hz and a unity gain crossover at 3MHz.

Since most output filter designs introduce one or more additional poles at a lower frequency, the best network to stabilize the system is a series RC combination at terminal 9 to ground. This network should be designed to introduce a zero to cancel out one of the output filter poles. A good starting point to determine the external poles is a 1000pF capacitor and a variable series 50kΩ potentiometer from terminal 9 to ground. The compensation point is also a convenient place to insert any programming signal to override the error amplifier. Internal shutdown and current limiting are also connected at terminal 9. Any external circuit that can sink 200µA can pull this point to ground and shut off both output drivers.

While feedback is normally applied around the entire regulator, the error amplifier can be used with conventional operational amplifier feedback and will be stable in either the inverting or non-inverting mode. Input common-mode limits must be observed; if not, output signal inversion may result. The internal 5V reference can be used for conventional regulator applications if divided as shown in Figure 13. If the error amplifier is connected as a unity gain amplifier, a fixed duty cycle application results.

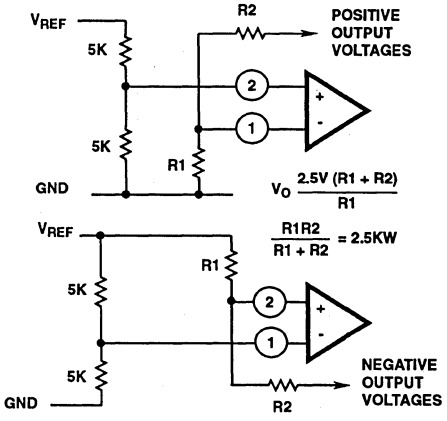


FIGURE 13. ERROR AMPLIFIER BIASING CIRCUITS

Current Limiting Section

The current limiting section consists of two transistors (Q64, Q66) connected to the error amplifier output terminal. By matching the base-to-emitter voltages of Q64 and Q66 and assuming negligible voltage drop across R51:

$$V_{THRESHOLD} = V_{BE}(Q64) + I(Q65)R53 - V_{BE}(Q66)$$
$$= I(Q65)R53 \cong 200mV$$

Although this circuit provides a small threshold with a negligible temperature coefficient, some limitations to its use must be considered. The circuit has a 11 volt common mode range which requires sensing in the ground line. The other factor to consider is that the frequency compensation provided by R51, C3 and Q64 produces a roll-off pole at approximately 300Hz.

Due to the low gain of this circuit, there is a transition region as the current limit amplifier takes over pulse width control from the error amplifier. For testing purposes, the threshold is defined as the input voltage to the current limiting amplifier to get 25% duty cycle with the error amplifier signaling maximum duty cycle.

In addition to constant current limiting, terminal 4 and 5 may also be used in transformer coupled circuits to sense primary current and shorten an output pulse, should transformer saturation occur (See Figure 37). Another application is to ground terminal 5 and use terminal 4 as an additional shutdown terminal: i.e. the output will be off with terminal 4 open and on when it is grounded. Finally, foldback current limiting can be provided with the network of Figure 14. This circuit can reduce the short circuit current (I_{SC}) to approximately 1/3 the maximum available output current (I_{MAX}).

Output Section

The CA1524 Series outputs are two identical n-p-n transistors with both collectors and emitters uncommitted. Each output transistor response for the wide range of oscillator frequencies. Current limiting of the output section is set at 100mA for each output and 100mA total if both outputs are paralleled. Having both emitters and collectors available provides the versatility to drive either n-p-n or p-n-p external transistors. Curves of the output saturation voltage as a function of temperature and output current are shown in Figures 15 and 16 respectively.

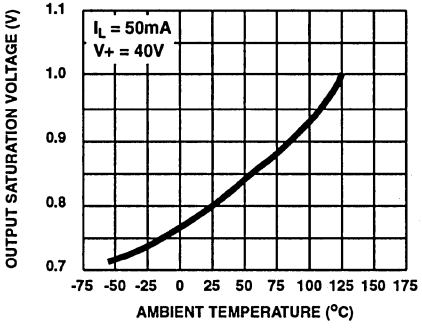


FIGURE 15. TYPICAL OUTPUT SATURATION VOLTAGE AS FUNCTION OF AMBIENT TEMPERATURE

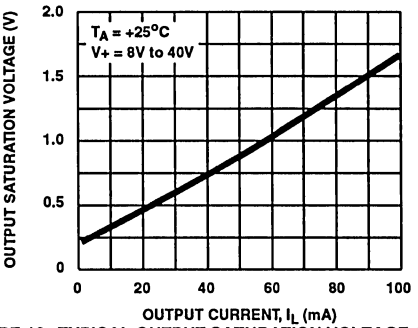


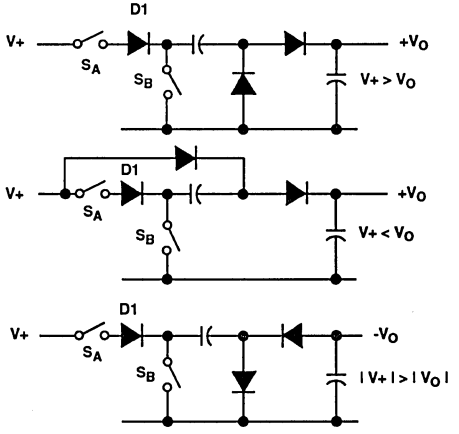
FIGURE 16. TYPICAL OUTPUT SATURATION VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

There are a number of possible output configurations in the application of the CA1524 to voltage regulator circuits, they fall into three basic classifications:

1. Capacitor diode coupled voltage multipliers
2. Inductor capacitor single ended circuits
3. Transformer coupled circuits

Examples of these configurations are shown in Figures 17, 18 and 19. In each case, the switches can be either the output transistors in the CA1524 or added external transistors, depending on the load current requirements.

Capacitor diode coupled voltage multipliers are particularly useful in those low-power applications where inductive components are undesirable. Although the efficiencies of these voltage multipliers may not be as good as their inductive component counterparts, they are more efficient than the series-pass circuit.



NOTE: Diode D1 Is Necessary To Prevent Reverse Emitter-Base Breakdown of Transistor Switch S_A

FIGURE 17. CAPACITOR-DIODE COUPLED VOLTAGE MULTIPLIER OUTPUT STAGES

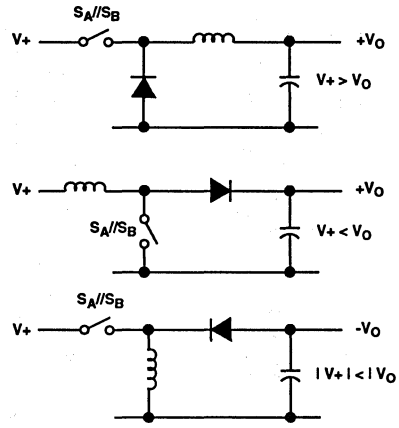


FIGURE 18. SINGLE-ENDED INDUCTOR CIRCUITS WHERE THE TWO OUTPUTS ARE CONNECTED IN PARALLEL

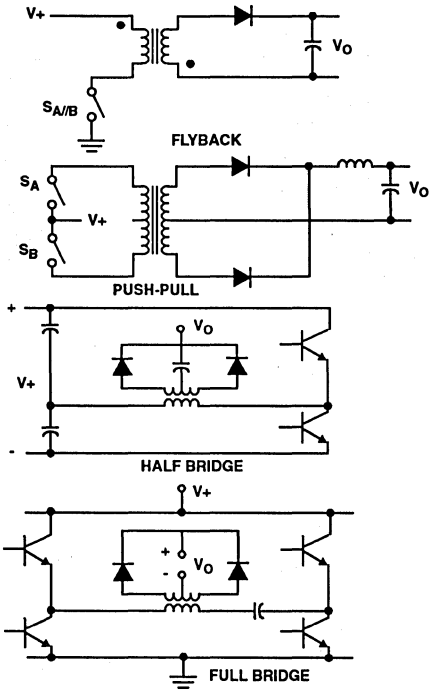


FIGURE 19. TRANSFORMER-COUPLED OUTPUTS

General Applications Considerations

The CA1524, in addition to having all the control circuits for switching regulator applications, employs two output NPN transistors. These transistors are internally current limited and can be used in a variety of switching regulator configurations.

Three such modes are:

1. Single-ended single stage configurations for forward and flyback converters.
2. Single-ended parallel output stages for switching regulators
3. Dual or individual stage configurations for push-pull, 1/2 bridge circuits, etc.

Single-Ended Applications

The single-ended configuration provides for simple regulator designs in which an LC and diode filter network provide the DC output voltage. The PWM controlled duty cycle can vary from 0% to 45%.

The duty cycle variation depends on the divided reference voltage applied to the error amplifier terminals. This voltage, in turn, adjusts the comparator's trip level to control the ON time. Figure 11 shows the duty cycle variation vs. the error amplifier output voltage (pin 9) for the CA1524.

If the outputs are connected in parallel, the duty cycle can range from 0% to 90% a normal mode for switching regulators. For flyback operation, care must be taken to prevent the on time from exceeding 45% to allow for retrace in the flyback transformer.

Dual-Ended Applications

The dual-ended configuration can be used for the following applications:

1. Push-Pull circuits
2. Voltage Multipliers; (capacitor diode filters)
3. Half or full bridge circuits

The oscillator has a dead band feature to ensure against both output transistors conducting simultaneously. This dead band applies not only to the internal transistors, but for any additional drivers used for push-pull applications.

When using push-pull and bridge circuits, the dead time becomes important. Since the frequency of the oscillator is $1/R_TC_T$, a good method for establishing dead band time is to select f first, C_T second, and then R_T. The value of C_T determines the dead time or discharging rate of C_T. The curves in Figures 8 and 10 are used for this purpose. The oscillator provides a ramp at the C_T terminal with an equivalent dead time pulse at Pin 3 for slaving multiple units. This terminal can also be used as an oscilloscope sync. With an output resistance of 2KΩ at Pin 3, capacitive loading of this terminal will be adequate for most applications, but for larger systems some type of external dead time adjustment must be employed. To provide an expansion of the dead time without loading the oscillator, the simple 5kΩ potentiometer and diode arrangement shown in Figure 9 can be used. The output frequency of each individual output stage is approximately half that of the oscillator frequency. When the stages are connected in parallel, $f_{OSC} = f_{OUT}$.

The selection of components - capacitors, diodes, inductors, transformer cores, etc., depends primarily on the operating frequency of the switching regulator. It is important, therefore, that care be exercised in the selection of these components. Capacitors should have low equivalent series resistance (ESR) and low equivalent series inductance (ESL), because high ESR is the principal cause of capacitor ripple, and high ESL causes high frequency ringing in the MHz region. Most capacitor manufacturers rate capacitance at 120Hz, a frequency quite different from the 20kHz - 100kHz operating frequency of PWM regulator circuits. Because the characteristics of capacitors may change with change in frequency, the careful selection of close tolerance capacitors will tend to offset any degradation in PWM regulator performance resulting from the difference in the frequency rating of capacitor vs. PWM regulator circuit operating frequency.

Free-wheeling diode clamps must have fast turn on and low distributed capacitance. The DC resistance of inductors should be kept low to minimize the effects of added losses that may occur at high load currents. In addition, the selection of the size and type of transformer core will also depend on the input voltage range and on the output voltage and current requirements.

Basic Switching Regulators

Figure 20 shows the basic switching regulator, the Buck or Step-Down type. In this type of regulator V_O is always $\leq V_{IN}$. The simplified waveforms for this regulator are shown in Figure 21.

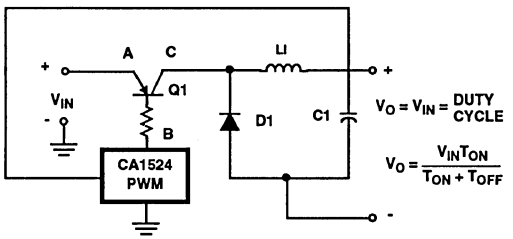


FIGURE 20. BUCK (STEP-DOWN) REGULATOR

The Buck Regulator shown in Figure 20 operates by chopping an unregulated DC voltage. The frequency of the circuit waveforms remains constant but the duty cycle is varied to effect regulation. The output LC filter, together with the free-wheeling diode D1, smooths the chopped waveform. With V_O set at some selected level by means of the reference voltage, the sample of the output voltage applied t the input of the CA1524 error amplifier adjusts the duty cycle in response to changes in load currents. When transistor Q1 is turned on diode D1 is nonconductive and current flows from V_{IN} through L1 to $+V_O$. When Q1 is off, the reserve energy in C1 provides the necessary current to the load. The overall output regulation depends primarily on the characteristics of the CA1524 and on the design of the output filter.

Switching regulator circuits are categorized for single-ended and dual-ended (bridge) applications. The basic circuits shown in Figures 22 through 30 include an inductive element. In these circuits SA represents transistor A, SB transistor B, and SA/SB indicated that both transistors can be connected in parallel. A description of the single-ended and dual-ended bridge configuration is given in subsequent pages.

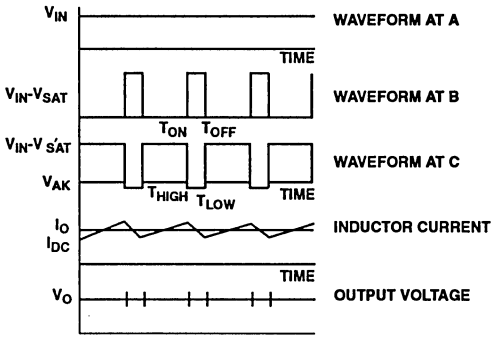


FIGURE 21. SIMPLIFIED WAVEFORM FOR BUCK (STEP-DOWN) REGULATOR

Single-Ended Applications

For low-power applications up to 100 watts.

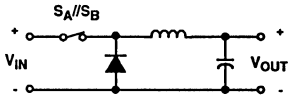


FIGURE 22. BUCK OR STEP-DOWN REGULATOR

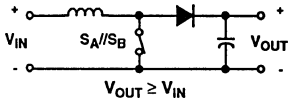


FIGURE 23. BOOST OR STEP-UP REGULATOR

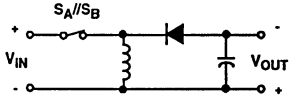
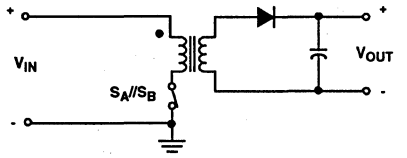


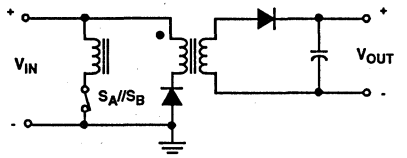
FIGURE 24. VARIATION OF THE BOOST OR STEP-UP REGULATOR RESEMBLES THE FLYBACK REGULATOR AND CAN BE EITHER STEP-UP OR STEP-DOWN

The clamp winding returns excess stored energy to the line, thereby preventing avalanche in the switching transistor.

For low-power applications from 50 to 100 watts.



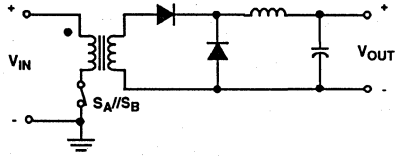
FLYBACK CONVERTER



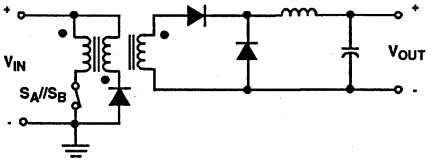
FLYBACK CONVERTER WITH CLAMP WINDING

FIGURE 25. FLYBACK CONVERTER (OPERATING MODEL FOR THIS CONVERTER IS THE BOOST REGULATOR)

For low-to-medium-power applications from 100 to 200 watts.



FORWARD CONVERTER



FORWARD CONVERTER WITH DIODE CLAMP

FIGURE 26. FORWARD CONVERTER (OPERATING MODEL FOR THIS CONVERTER IS THE BUCK REGULATOR)

Dual-Ended (Bridge) Applications

For low-to-medium-power applications from 100 to 200 watts.

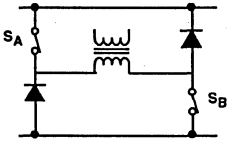


FIGURE 27. FLYBACK OR FORWARD CONVERTER WITH A CLAMP WINDING

For Medium-power applications from 200 to 500 watts.

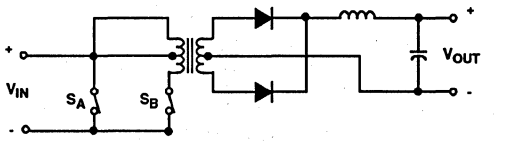


FIGURE 28. PUSH-PULL OR DC-TO-DC CONVERTER

Capacitor C_C (1.0µF to 5.0µF range) minimizes transformer saturation problems. Diode clamps can be used across each transistor to reduce the effects of destructive switching transients.

For medium-to-high power applications from 200 to 1000 watts.

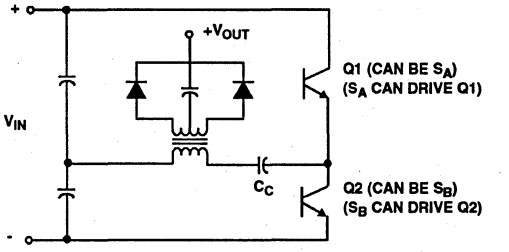


FIGURE 29. HALF-BRIDGE CIRCUIT

Capacitor C_C and diode clamps have same function as in the half-bridge circuit. In the full-bridge circuit full line voltage can be applied to the primary winding to approximately double the power output of the half-bridge circuit.

For high-power applications from 500 to 2000 watts.

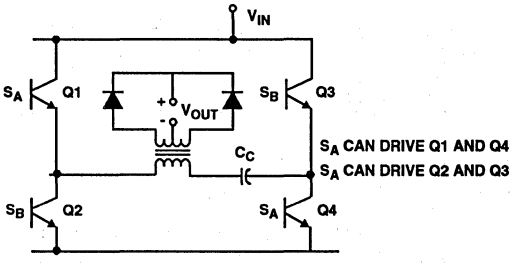


FIGURE 30. FULL-BRIDGE CIRCUIT

Regulator Applications

The Variable Switcher

The following review of some of the characteristics and unique design features of a variable switching pulse-width-modulated (PWM) circuit will provide the equipment designer with some of the basic principles of a PWM circuit and its associated circuitry, and a better understanding of the CA1524 Series ICs intended for this type of application.

Although most switching regulator designs and applications imply a fixed output voltage, the CA1524 Series can be applied to a variable-output-voltage power supply.

This type of circuit provides many advantages:

1. Excellent overall efficiency for the full output range; generates less heat, thereby reducing cooling requirements.
2. Input current level ≈ maximum output current level.
3. Limited dependence on V_{IA} (i.e., $V_{IN} \geq V_{OUT}$ max. +2) at the power supply's maximum output current level.
4. Light weight due to small, light cores.
5. Space saver.

and some disadvantages:

1. Low output voltage due to the limited lower end range of the error amplifier (i.e., V_{OUT} min ≠ 0, but = 7V in this particular application).
2. Losses in efficiency when output current levels are within the range of the no load dissipation for the IC and pass transistor.
3. Time lag in changing voltage levels at no load or light loads. This time lag is due to two conditions:
   A. V_C cannot change instantaneously; and
   B. C_T remains charged since it is not performing its function of supply current to the output load when the free wheeling diode conducts.

Basic Circuit Operation

The circuit diagram of the CA1524, used as a variable output voltage power supply is shown in Figure 31. By connecting the two output transistors in parallel, the duty cycle is doubled i.e.; 0° to 90°. Transistor Q1, 8203B PNP Darlington Transistor, is used as the switching pass element. Its base is driven by the CA1524's outputs. Variability is obtained by fist presetting the error amplifier inverting input (terminal 1) to 3.4V by appropriate selection of values for resistor network R_3, R_4 and R_5, in accordance with the maximum output voltage desired, e.g.; this particular supply was adjusted so that V_{OUT} (max.) = 30V. By varying the internal reference voltage at the comparator input (Pin 9) or 0.5V to 3.8V is achieved. This output voltage will cause the ON time of the output section to vary accordingly. As the reference voltage level is varied, the feedback voltage will track that level and cause the output voltage to change according to the change in reference voltage. The operating frequency of the regulator with R_T = 16KΩ and C_T = 3300pF is 23KHz (T = 43.5μs). The output voltage is directly related to the duty cycle and can be determined by the following equation:

$$V_O = \frac{V_{IN} - V_{(SAT)}\, t_{ON}}{T}$$

where t_{ON} is the "on" time in μs, T is the oscillator period in μs; and Q1 is operating in a saturated mode.

The following table shows both the calculated and measured data for the regulator circuit of Figure 31.

V_O (I_{LOAD} = 3A) (V)	V_{IN}-V_{SAT} (V)	t (μs)	t_{ON} (CALC.) (μs)	t_{ON} (MEAS.) (μs)
30	32.5	43.5	40.15	40.50
20	32.5	43.5	26.77	26.45
10	32.5	43.5	13.88	13.70

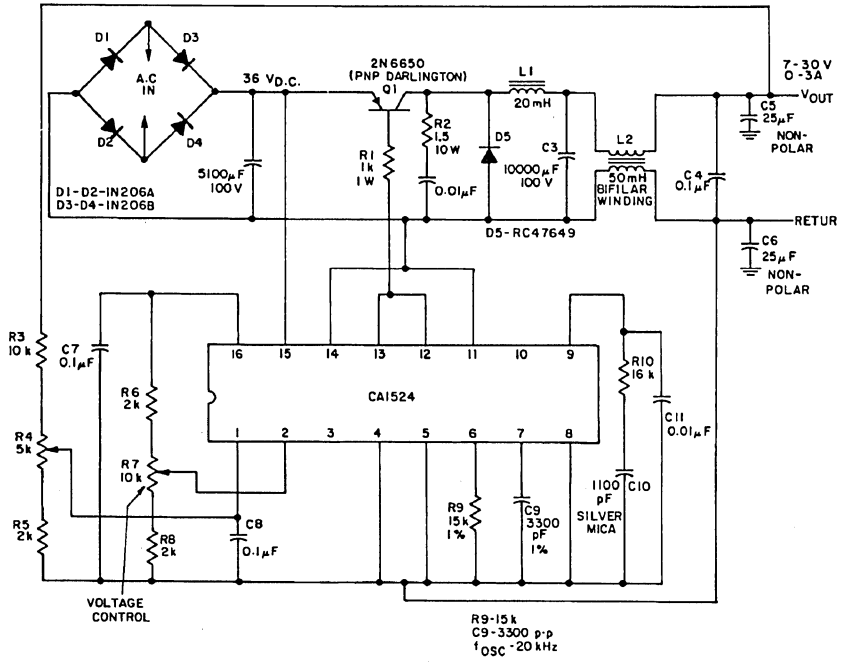


FIGURE 31. THE CA1524 USED AS A 0A TO 5A 7V TO 30V LABORATORY SUPPLY

As the load current increases, the level of the input voltage to the D5-L1-C3 filter network decreases slightly due to an increase in the saturation voltage of Q1. this change in load causes the ON time of Q1's base to increase in proportion to the decrease in voltage at Q1's collector. This decrease in voltage, in turn, adjusts the output voltage at C_3. Resistor R_7 controls the output voltage level.

The efficiency curve for the variable output voltage power supply is shown in Figure 32 at load currents in the range of 0.5A to 3A over the full output voltage range (7V - 30V). The efficiency of the variable switcher falls short of the ideal due to the losses incurred during the fall time of Q1's collector voltage. Use of a lower frequency would improve efficiency, but would require more expensive inductive and capacitive components. Even though the efficiency values shown in Figure 32 are appreciably lower at the lower output voltages, the overall efficiency of the PWM variable supply is superior to that of the linear variable supply.

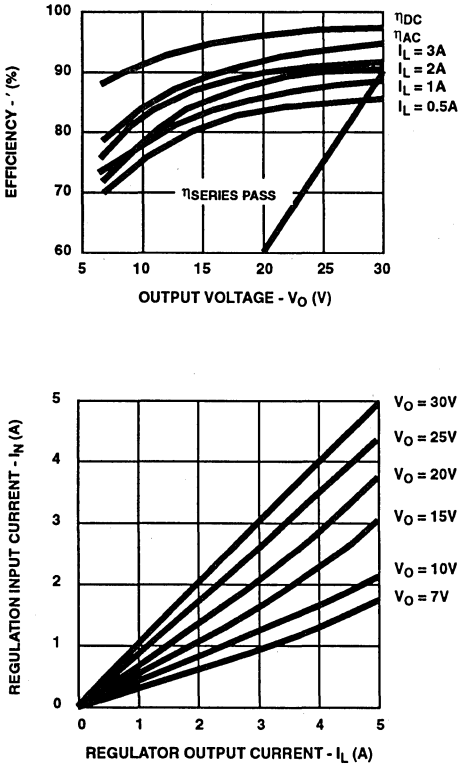


FIGURE 32. EFFICIENCY CURVE FOR THE VARIABLE OUTPUT VOLTAGE POWER SUPPLY SHOWN IN FIGURE 31

A major factor in the improved efficiency of the switching regulator is that output current does not have to be equal to input current as the output voltage swings between the end points of its range. The curves in Figure 32 (b) show the relationship between the output current and the input current over the full voltage range and demonstrated how the switching regulator accomplishes its high level of efficiency. At some combinations of output voltages and currents, the large reservoir energy capacitor (C_3) supplies the difference between the required load current and available input current (see Figure 31). Note that the switching regulator has a higher efficiency for DC than AC - due primarily to the additional losses caused by the input bridge rectifiers D1 through D4 in Figure 31. However, the advantage of the linear regulator is also apparent, it can provide output voltage down to nearly zero volts.

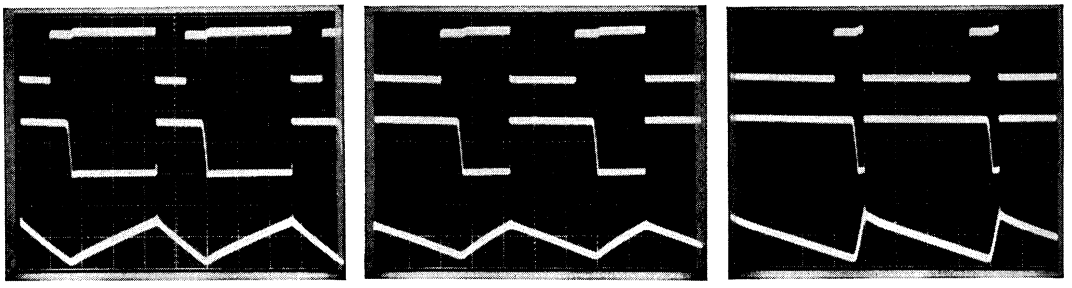
Figure 33 shows the variation in ON time as a function of output loadings as measured at the base and collector of Q1 respectively. The regulated output voltages are 30, 20, and 10V, respectively with load currents of from 3A to 1A. The lower curve is the inductor current for the same voltages and loads. Note the change in the duty cycle and inductor current level waveforms in response to the short ON time required to supply the 30V output voltage level.

Radio frequency interference (RFI) is usually generated with any switching regulator and certain networks must be added to minimize this interference. R_2 and C_2 (Figure 31) provide a snubber network for the switching current transients of diode D5 to reduce the level of the RFI generated. The output filter network L2 and C4 through C6 provides a bifilar coil which additionally suppresses the switching noise. Varistors and input L-C filters can also be employed.

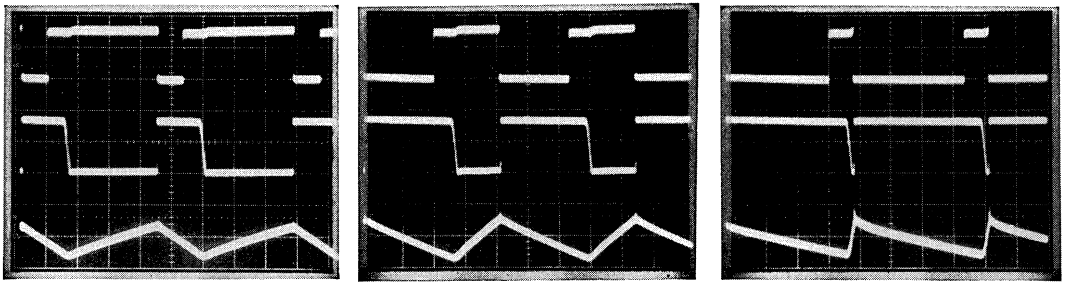
Pulse-Width Modulator (PWM) Supply Details

The CA1524 provides all sense and control functions in the variable output voltage power supply design of Figure 31. In this application, the ICs two alternately switched output stages (pins 12 and 13) are connected in parallel to drive the switching transistor (Q1). The PWM IC provides an "on" drive signal to Q1 that, in effect, spans a 0% to 90% duty cycle. (The ICs output transistors can each provide a 0% to 45% duty cycle during their alternate "on" periods, but when the outputs are connected in parallel their separate "on" times effectively add serially.) This 0% to 90% duty cycle span makes possible the design's wide output voltage/current range without manual switching.

Other supply features include high operating efficiency (70% to 80%) over the full output voltage/current range. This high efficiency leads to fewer heat dissipation problems; therefore, the design is easier to cool and its reliability is higher than that of conventional linear designs. Additionally, because the circuit switches at a relatively high frequency (approximately 23KHz), circuit capacitors and inductors are small, and the combination of small size components with low power dissipation permits a compact overall design.



(a) I_{OUT} = 1A, V_{OUT} = 10V (b) V_{OUT} = 20V (c) V_{OUT} = 30V



(d) I_{OUT} = 3A, V_{OUT} = 10V (e) V_{OUT} = 20V (f) V_{OUT} = 30V

NOTES:

All Photos: V_{IN} = 33Vdc, Horizontal - 10μs/Div
Vertical Scale Factors:
Upper Trace: CA1524 Output Voltage (Pins 12, 13) = 20V/Div
Middle Trace: Q1 Collector Voltage = 20V/Div
Lower Trace: L_1 Current = 0.5A/Div, (a), (b), (d), (e); 0.1A/Div, (c), (f)

Variable output switching power supply design employ pulse width modulation techniques to achieve high performance. Note that "on" times of Q1 and the CA1524 are more dependent on the circuit's output voltage than by the output current to the load.

FIGURE 33. TYPICAL VOLTAGE AND CURRENT WAVEFORMS FOR CA1524 PWM REGULATOR OPERATED WITH P-N-P PASS TRANSISTOR AND SERIES LC AND DIODE FILTER NETWORK

The PWM supply does present a few disadvantages. For example, output voltages of less than 7V cannot be attained because the on-chip error amplifier of the PWM device has a limited low-end range. And efficiency suffers when the output load current levels are low enough to nearly equal the active devices' no-load dissipation levels. In addition, a time lag occurs in voltage regulation with no load or light loads because C3 does not supply load current when the commutating diode D5 tries to conduct.

Component and Wiring Considerations

Besides being simple in concept, the regulator in Figure 31 is easy to construct and align. Layout isn't critical except in the ground returns where high circulating currents could cause problems. Note the indicated chassis and earth grounding points. The circuit diagram shows two separate return lines, one for all components in the power section and one for the control section. This arrangement is essential to assure good line and load regulation as well as minimal output noise. Keep the DC output well away from the switching circuits (switching occurs at 23kHz).

To align the supply of Figure 31, first set the PWM error amplifier's inverting input (pin 2) to approximately 33V by means of R7. (This voltage is the maximum value for the voltage control potentiometer). Then adjust the output of R4 to pin 1 to 3.4V. This value yields a maximum supply output of 30V. When the voltage control potentiometer is varied from minimum to maximum, the ICs comparator input voltage at pin 9 varies from 0.5V to 3.8V. This voltage controls the PWMs on-to-off ratio and, therefore, the conduction time of switching transistor Q1. During operation, the control voltage is set to the desired supply output voltage, and the output to the PWM feedback network consisting of R3 through R5 controls the timing.

Other Applications

Single-Ended Switching Regulator

The CA1524 in the circuit of Figure 34 has both output stages connected in parallel to produce an effective 0% - 90% duty cycle. Transistor Q1 is pulsed on and off by these output stages. Regulation is achieved from the feedback provided by R1 and R2 to the error amplifier which adjusts the on-time of the output transistors according to the load current being drawn. Various output voltages can be obtained by adjusting R1 ad R2. The use of an output inductor requires an R-C phase compensation network to stabilize the system. Current limiting is set at 1.9A by the sense resistor R3.

Capacitor Diode Output Circuit

A capacitor diode output filter is used in Figure 35 to convert +15Vdc to -5Vdc at output currents up to 50mA. Since the output transistors have built-in current limiting, no additional current limiting is needed. Table 1 gives the required minimum input voltage and feedback resistor values, R2, for an output voltage range of -0.5V to -20V with an output current of 40mA.

Flyback Converter

Figure 36 shows a flyback converter circuit for generating a dual 15V output at 20mA from a 5V regulated line. Reference voltage is provided by the input and the internal reference generator is unused. Current limiting in this circuit is accomplished by sensing current in the primary line and resetting the soft start circuit.

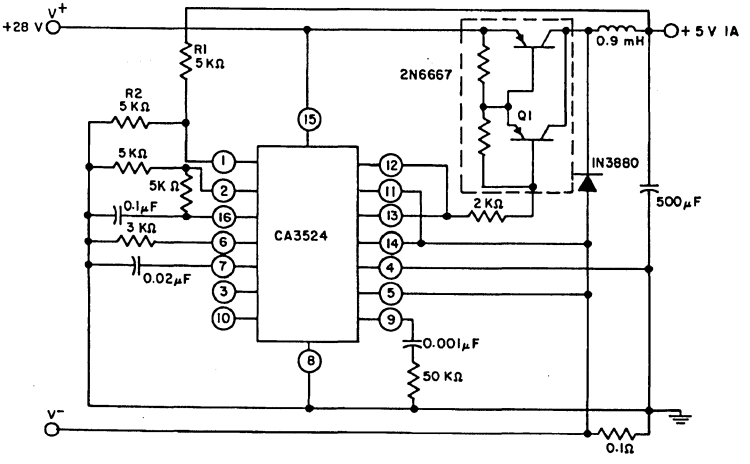


FIGURE 34. SINGLE-ENDED LC SWITCHING REGULATOR CIRCUIT

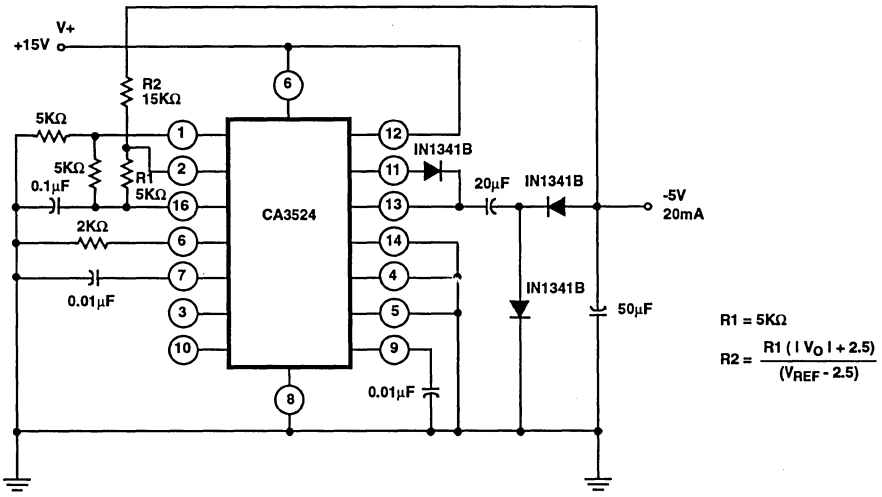


FIGURE 35. CAPACITOR DIODE OUTPUT CIRCUIT

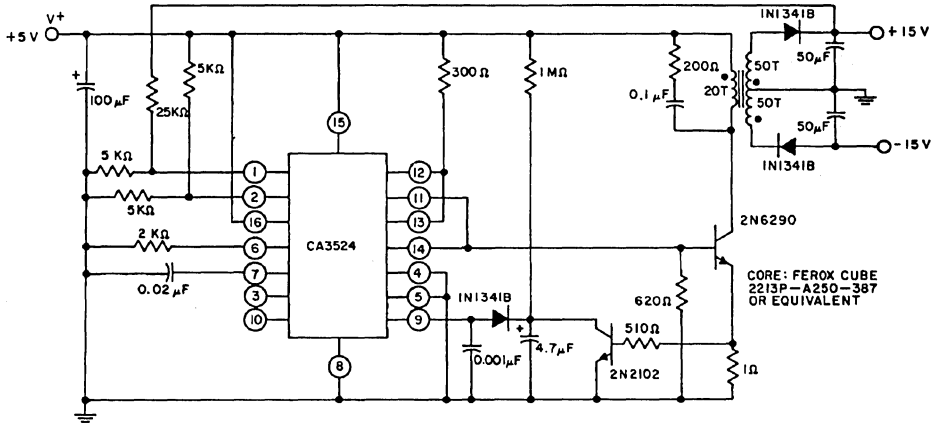


FIGURE 36. FLYBACK CONVERTER CIRCUIT

TABLE 1. INPUT vs. OUTPUT VOLTAGE AND FEEDBACK RESISTOR VALUES FOR I_L = 40mA
(For capacitor diode output circuit shown in Figure 35)

V_O (V)	R2 (kΩ)	V+ (Min) (V)	V_O (V)	R2 (kΩ)	V+ (Min) (V)
-0.5	6	8	-11	27	18
-2.5	10	9	-12	29	19
-3.0	11	10	-13	31	20
-4.0	13	11	-14	33	21
-5.0	15	12	-15	35	22
-6.0	17	13	-16	37	23
-7.0	19	14	-17	39	24
-8.0	21	15	-18	41	25
-9.0	23	16	-19	43	26
-10	25	17	-20	45	27

Push-Pull Converter

The output stages of the CA1524 provide the drive for transistors Q1 and Q2 in the push-pull application of Figure 37. Since the internal flip-flop divides the oscillator frequency by two, the oscillator must be set at twice the output frequency. Current limiting for this circuit is done in the primary of transformer T1 so that the pulse width will be reduced if transformer saturation should occur.

Low Frequency Pulse Generator

Figure 38 shows the CA1524 being used as a low frequency pulse generator. Since all components (error amplifier, oscillator, oscillator reference regulator, output transistor drivers) are on the IC, a regulated 5V (or 2.5V) pulse of 0% to 45% (or 0% to 90%) on time is possible over a frequency range of 150Hz to 500Hz. Switch S1 is used to go from a 5V output pulse (S1 closed) to a 2.5V output pulse (S1 open) with a duty cycle range of 0% to 45%. The output frequency will be roughly half of the oscillator frequency when the output transistors are not connected in parallel (75Hz to 250Hz respectively). Switch S2 will allow both output stages to be paralleled for an effective duty cycle of 0% to 90% with the output frequency range from 150Hz to 500Hz. The frequency is adjusted by R_1; R_2 controls duty cycle.

Digital Readout Scale

The CA1524 can be used as the driving source for an electronic scale application. The circuit shown in Figures 39 and 40 uses half (Q2) of the CA1524 output in a low voltage switching regulator (2.2V) application to drive the LED's displaying the weight. The remaining output stage (Q1) is used as a driver for the sampling plates PL1 and PL2. Since the CA1524 contains a 5V internal regulator and a wide operating range of 8V to 40V, a single 9V battery can power the total system. The two plates, PL1 and PL2, are driven with opposite phase signals (frequency held constant but duty cycle may change) from the pulse width modulator IC (CA1524). The sensor, S, is located between the two plates. Plates PL1, S and PL2 form an effective capacitance bridge type divider network. As plate S is moved according to the object's weight, a change in capacitance is noted between PL1, S and PL2. This change is reflected as a voltage to the amplifier (CA3160). At the null position the signals from PL1 and PL2 as detected by S are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal as S becomes greater. The CA3160 AC amplifier provides a buffer for the small signal change noted at S. The output of the CA3160 is converted to a DC voltage by a peak-to-peak detector. A peak-to-peak detector is needed, since the duty cycle of the sampled waveform is subject to change. The detector output is filtered further and displayed via the CA3161E and CA3162E digital readout system, indicating the weight on the scale.

References

For additional information concerning regulator designs and pulse width modulator applications, and for a list of integrated circuits and power transistors suitable for series switching applications, refer to the following publications:

1. "CA1524 Series ICs Offer Efficiency in Power Supply Design".
2. Data Sheet for the CA1524, Regulating Pulse Width Modulator, File Number 1239.2
3. Application Note, ICAN-6605, "Power Devices in Off-the-Line High-Frequency Inverter/Converter Circuits". R Minton, I. Martin, and J. Vara.
4. Application Note, ICAN-6743, "900 Watt, Off-the-Line, Half-Bridge Converter Using Only Two 15A Switch Max High Voltage Power Transistors", R.B. Jarl and K.R. Kemp.
5. Application Note, ICAN-6843, "A 450 Watt, 40kHz, 240VAC to 5VDC Forward Converter Using a New Type of Transistor", R.B. Jarl and W.R. Witte
6. EDN Design Ideas, EDN Publication, December 16, 1981, "Pulse Width Modulators Measure Weights", C.P. Salerno and P.J. Stabile, RCA Solid State Division, Somerville, N.J.
7. EDN Design Ideas, EDN Publication, August 19, 1981, "Apply Pulse Width Modulators to Produce Variable DC Voltages", C. Field, R. Jarl, C. Salerno, RCA Solid State Division, Somerville, N.J.
8. "A General Unified Approach to Modeling Switching Converter Power Stages:, R.D. Middlebrook and S. Cun, IEEE Proceedings, June 1976.
9. "Switching and Linear Power Converter Design", A.I. Pressman, Hayden Publications, 1977.
10. "Linear/Switching Voltage Regulator Handbook", Second Edition, Motorola.

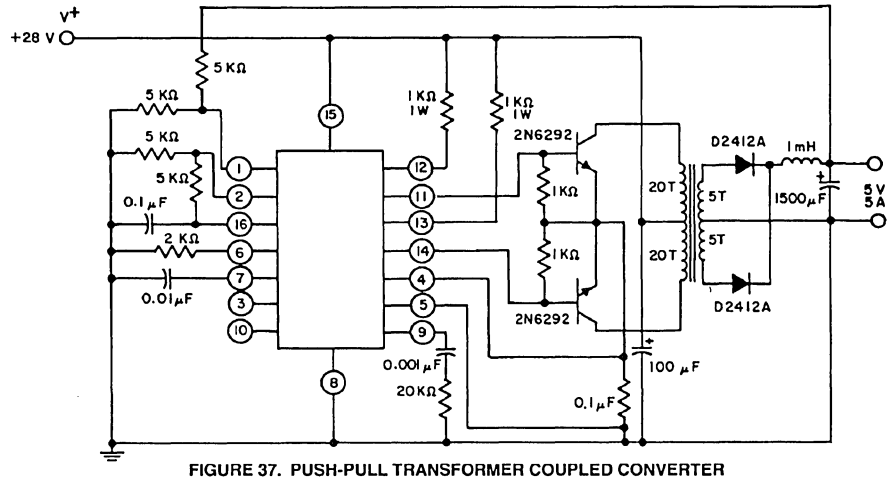
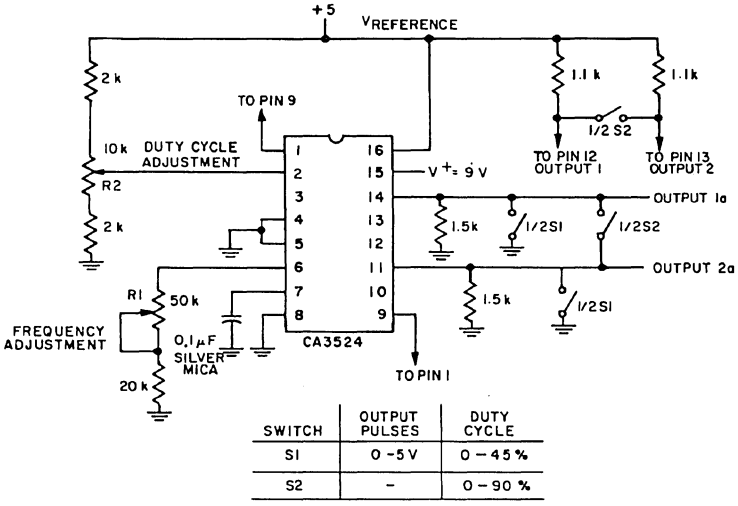


FIGURE 37. PUSH-PULL TRANSFORMER COUPLED CONVERTER



SWITCH	OUTPUT PULSES	DUTY CYCLE
S1	0 -5 V	0 – 45 %
S2	-	0 – 90 %

FIGURE 38. LOW FREQUENCY PULSE GENERATOR

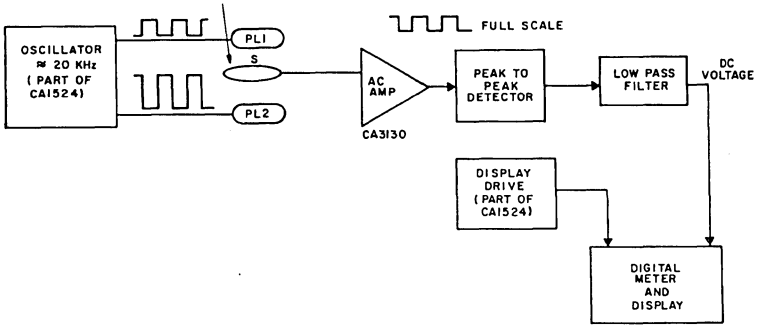


FIGURE 39. BLOCK DIAGRAM - DIGITAL READOUT SCALE CIRCUIT

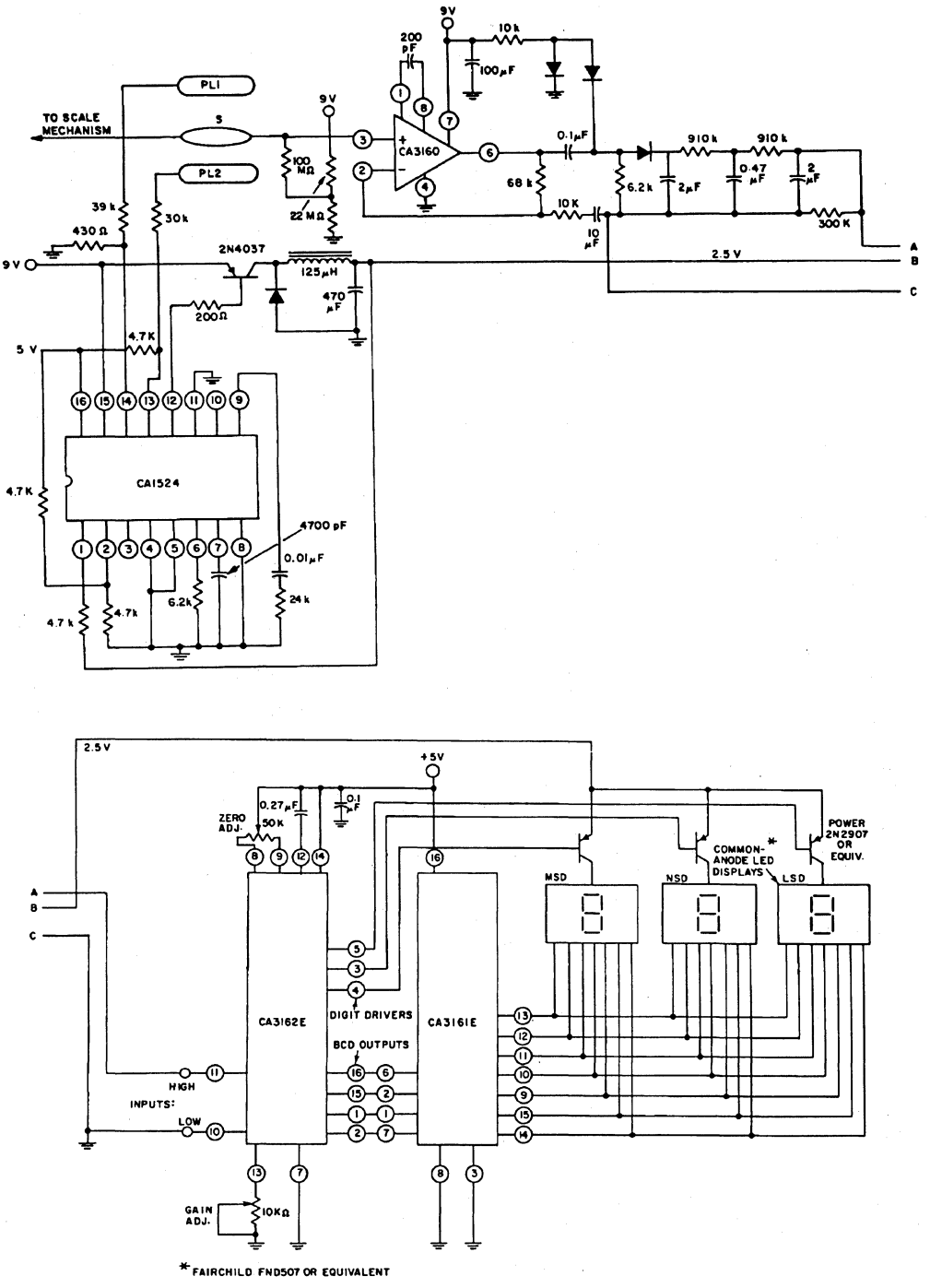


FIGURE 40. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE

APPNOTE

No. 7174 May 1992

Harris Intelligent Power

THE CA1524E PULSE-WIDTH MODULATOR-DRIVER FOR AN ELECTRONIC SCALE

Authors: C.P. Salerno and P.J. Stabile

The CA1524E pulse-width modulator integrated circuit presently in use in voltage-regulator applications can also be employed as the driving source for an electronic scale. As shown in the block and schematic diagrams of Figures 1 and 2, half of the output of the CA1524E, Q2, is used in a low-voltage (2.2 volts) switching regulator that drives the LEDs displaying the weight measured. The remaining output stage, Q1, is used as a driver for the sampling plates PL1 and PL2. Since the CA1524E contains a 5V internal regulator and is able to operate over a wide voltage range, 8V to 40V, a single 9V battery is sufficient to power the total system. The two sampling plates, PL1 and PL2, are driven by oppositely phased signals (the frequency is held constant but the duty cycle may change) from the pulse-width modulator integrated circuit CA1524E. The sensor, S, located between the two plates forms with them an effective divider network of the capacitance bridge type.

As the plate S is moved, the amount of movement depending on the weight of the object on the scale, a change in capacitance occurs. This change is reflected as a voltage to the AC amplifier, the integrated circuit CA3160. At the null position, the signals for PL1 and PL2, as detected at S, are equal in amplitude, but opposite in phase. As S is driven by the scale mechanism down toward PL2, the signal at S becomes greater. The CA3160 AC amplifier provides a buffer fro the small signal change noted at S. The output of the CA3160 is converted to a DC voltage by peak-to-peak detector. A detector of this type is needed because the duty cycle of the sampled waveform is subject to change. The detector signal is filtered further and displayed, by means of the CA3161E and the CA3162E digital readout system, as the weight of the object on the scale.

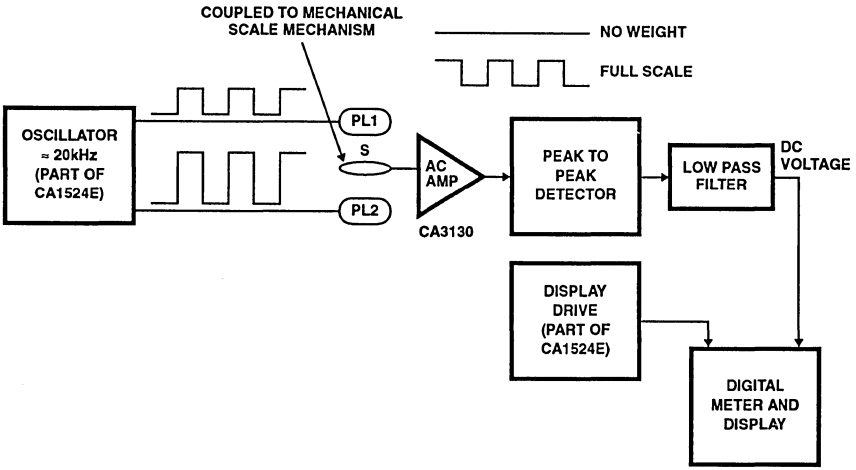
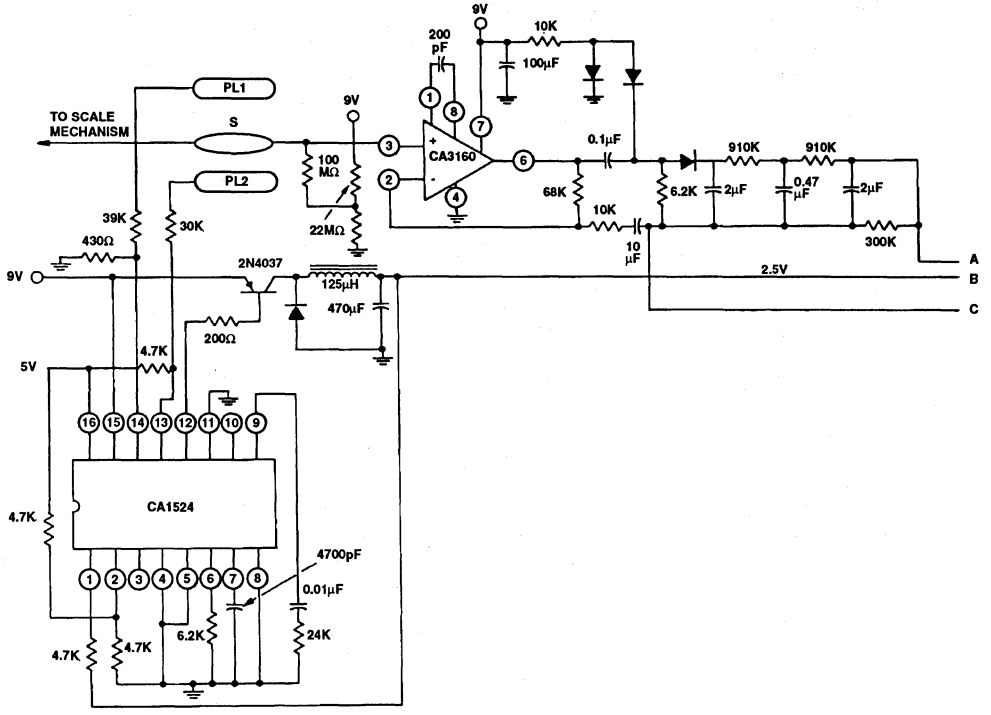
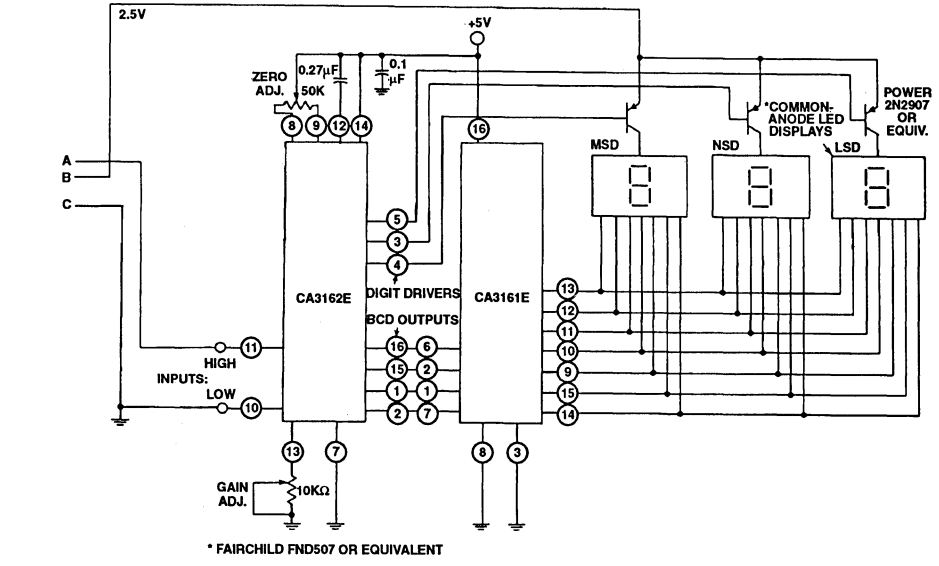


FIGURE 1. BLOCK DIAGRAM - DIGITAL READOUT SCALE CIRCUIT



2(a)



2(b)

FIGURE 2. SCHEMATIC DIAGRAM OF DIGITAL READOUT SCALE

APPNOTE

No. 7244.1 May 1992

UNDERSTANDING POWER MOSFETs

Author: Tom McNulty

Power MOSFETs (Metal Oxide Semiconductor, Field Effect Transistors) differ from bipolar transistors in operating principles, specifications, and performance. In fact, the performance characteristics of MOSFETs are generally superior to those of bipolar transistors: significantly faster switching time, simpler drive circuitry, the absence of a second-breakdown failure mechanism, the ability to be paralleled, and stable gain and response time over a wide temperature range. This note provides a basic explanation of general MOSFET characteristics, and a more thorough discussion of structure, thermal characteristics, gate parameters, operating frequency, output characteristics, and drive requirements.

General Characteristics

A conventional n-p-n bipolar power transistor is a current-driven device whose three terminals (base, emitter, and collector) are connected to the body by silicon contacts. Bipolar transistors are described as minority-carrier devices in which injected minority carriers recombine with majority carriers. A drawback of recombination is that it limits the device's operating speed. And because of its current-driven base-emitter input, a bipolar transistor present a low-impedance load to its driving circuit. In most power circuits, this low-impedance input requires somewhat complex drive circuitry.

By contrast, a power MOSFET is a voltage-driven device whose gate terminal, Figure 1(a), is electrically isolated from its silicon body by a thin layer of silicon dioxide (SiO_2). As a majority-carrier semiconductor, the MOSFET operates at much higher speed than its bipolar counterpart because there is no charge-storage mechanism. A positive voltage applied to the gate of an n-type MOSFET creates an electric field in the channel region beneath the gate; that is, the electric charge on the gate causes the p-region beneath the gate to convert to an n-type region, as shown in Figure 1(b). This conversion, called the surface-inversion phenomenon, allows current to flow between the drain and source through an n-type material. In effect, the MOSFET ceases to be an n-p-n device when in this state. The region between the drain and source can be represented as a resistor, although it does not behave linearly, as a conventional resistor would. Because of this surface-inversion phenomenon, then, the operation of a MOSFET is entirely different from that of a bipolar transistor, which always retain its n-p-n character.

By virtue of its electrically-isolated gate, a MOSFET is described as a high-input impedance, voltage-controlled device, whereas a bipolar transistor is a low-input-impedance, current-controlled device. As a majority-carrier semiconductor, a MOSFET stores no charge, and so can switch faster than a bipolar device. Majority-carrier semiconductors also tend to slow down as temperature increases. This effect, brought about by another phenomenon called carrier mobility (where mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) makes a MOSFET more resistive at elevated temperatures, and much more immune to the thermal-runaway problem experienced by bipolar devices.

A useful by-product of the MOSFET process is the internal parasitic diode formed between source and drain, Figure 1(c). (There is no equivalent for this diode in a bipolar transistor other than in a bipolar darlington transistor.) Its characteristics make it useful as a clamp diode in inductive-load switching.

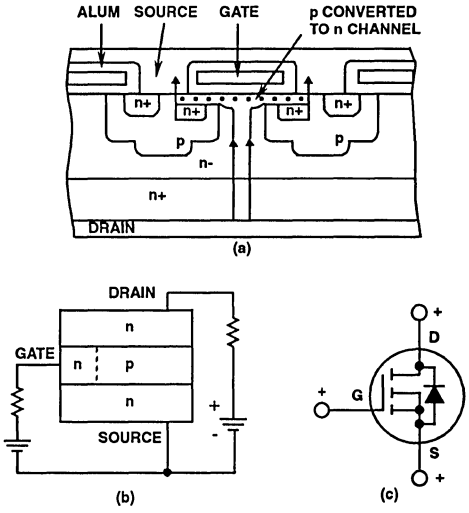


FIGURE 1. THE MOSFET, A VOLTAGE-CONTROLLED DEVICE WITH AN ELECTRICALLY ISOLATED GATE, USES MAJORITY CARRIERS TO MOVE CURRENT FROM SOURCE TO DRAIN (A). THE KEY TO MOSFET OPERATION IS THE CREATION OF THE INVERSION CHANNEL BENEATH THE GATE WHEN AN ELECTRIC CHARGE IS APPLIED TO THE GATE (B). BECAUSE OF THE MOSFETs CONSTRUCTION, AN INTEGRAL DIODE IS FORMED ON THE DEVICE (C), AND THE DESIGNER CAN USE THIS DIODE FOR A NUMBER OF CIRCUIT FUNCTIONS.

Structure

Harris Power MOSFETs are manufactured using a vertical double-diffused process, called VDMOS or simply DMOS. A DMOS MOSFET is a single silicon chip structured with a large number of closely packed, hexagonal cells. The number of cell varies according to the dimensions of the chip. For example, a 120-mil^2 chip contains about 5,000 cells; a 240-mil^2 chip has more than 25,000 cells.

One of the aims of multiple-cells construction is to minimize the MOSFET parameter $r_{DS(ON)}$, or resistance from drain to source, when the device is in the on-state. When $r_{DS(ON)}$ is minimized, the device provides superior power-switching performance because the voltage drop from drain to source is also minimized for a given value of drain-to-source current.

Since the path between drain and source is essentially resistive, because of the surface-inversion phenomenon, each cell in the device can be assumed to contribute an amount, R_n, to the total resistance. An individual cell has a fairly low resistance, but to minimize $r_{DS(ON)}$, it is necessary to put a large number of cells in parallel on a chip. In general, therefore, the greater the number of paralleled cells on a chip, the lower its $r_{DS(ON)}$ value:

$r_{DS(ON)} = R_N/N$, where N is the number of cells.

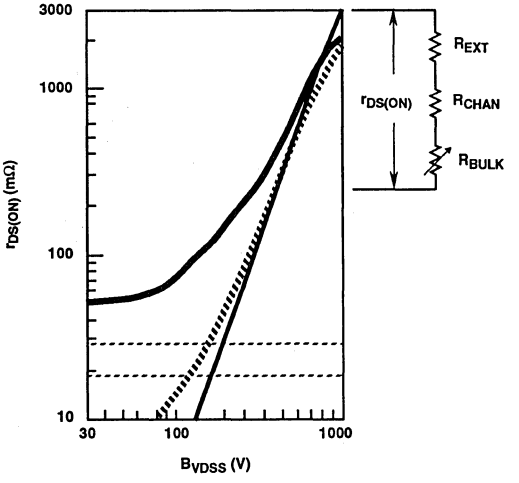


FIGURE 2. THE DRAIN-TO-SOURCE RESISTANCE ($r_{DS(ON)}$ OF A MOSFET IS NOT ONE BUT THREE SEPARATE RESISTANCE COMPONENTS)

TABLE 1. PERCENTAGE RESISTANCE COMPONENTS FOR A TYPICAL CHIP

B_{VDSS}	40V	150V	500V
$R_{CHANNEL}$	50%	23%	2.4%
R_{BULK}	35%	70%	97%
$R_{EXTERNAL}$	15%	7%	<1%

In reality, $r_{DS(ON)}$ is composed of three separate resistances. Figure 2 shows a curve of the three resistive components for a single cell and their contributions to the overall value of $r_{DS(ON)}$. The value of $r_{DS(ON)}$ at any point of the curve is found by adding the values of the three components at that point:

$$r_{DS(ON)} = R_{BULK} + R_{CHAN} + R_{EXT}$$

where R_{CHAN} represents the resistance of the channel beneath the gate, and R_{EXT} includes all resistances resulting from the substrate, solder connections, leads, and the package. R_{BULK} represents the resistance resulting from the narrow neck of n material between the two players, as shown in Figure 1(a), plus the resistance of the current path below the neck and through the body of the device to the drain.

Note in Figure 2 that R_{CHAN} and R_{EXT} are completely independent of voltage, while R_{BULK} is highly dependent on applied voltage. Note also that below about 150 volts, $r_{DS(ON)}$ is dominated by the sum of R_{CHAN} and R_{EXT}. Above 150 volts, $r_{DS(ON)}$ is increasingly dominated by R_{BULK}. Table 1 gives a percentage breakdown of the contribution of each resistance for three values of voltage.

Two conclusions, inherent consequences of the laws of semiconductor physics, and valid for any DMOS device, can be drawn from the preceding discussion: First, $r_{DS(ON)}$ obviously increases with increasing breakdown-voltage capability of a MOSFET. Second, minimum $r_{DS(ON)}$ performance must be sacrificed if the MOSFET must withstand ever-higher breakdown voltages.

The significance of R_{BULK} in devices with a high voltage capability is due to the fact that thick, lightly doped epi layers are required for the drain region in order to avoid producing high electric fields (and premature breakdown) within the device. And as the epi layers are made thicker and more resistive to support high voltages, the bulk component of resistance rapidly increases (see Figure 2) and begins to dominate the channel and external resistance. The $r_{DS(ON)}$ therefore, increases with increasing breakdown voltage capability, and low $r_{DS(ON)}$ must be sacrificed if the MOSFET is to withstand even higher breakdown voltages.

There is a way around these obstacles. The $r_{DS(ON)}$ in Figure 2 holds only for a relatively small chip. Using a larger chip results in a lower value for $r_{DS(ON)}$ because a large chip has more cells (See Figure 3). A larger chip also increases MOSFET breakdown voltage capability.

The penalty for using a larger chip, however, is an increase in cost, since chip size is a major cost factor. And because chip area increases exponentially, not linearly, with voltage, the additional cost can be substantial. For example, to obtain a given $r_{DS(ON)}$ at a breakdown voltage twice as great as the original, the new chip requires an area four or five times larger than the original. Although the cost does not rise exponentially, it is substantially more than the original cost.

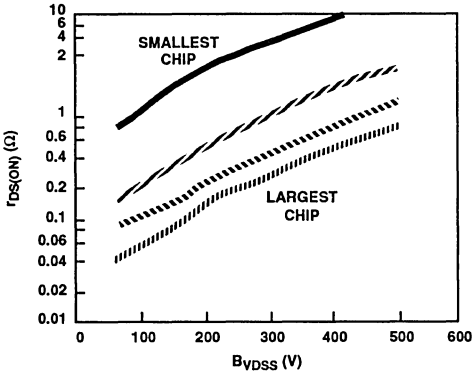


FIGURE 3. AS CHIP SIZE INCREASES, $r_{DS(ON)}$ DECREASES, & VOLTAGE HANDLING CAPABILITY INCREASES

Effects of Temperature

The high operating temperatures of bipolar transistors area frequent cause of failure. The high temperatures are caused by hot-spotting, the tendency of current in a bipolar device to concentrate in areas around the emitter. Unchecked, this hot-spotting results in the mechanism of thermal runaway, and eventual destruction of the device. MOSFETs do not suffer this disadvantage because their current flow is in the form of majority carriers. The mobility of majority carriers (where, again, mobility is a term that defines the average velocity of a carrier in terms of the electrical field imposed on it) is temperature dependent in silicon: mobility decreases with increasing temperature. This inverse relationship dictates that the carriers slowdown as the chip gets hotter. In effect, the resistance of the silicon path is increased, which prevents the concentrations of current that lead to hot spots. In fact, if hot spots do attempt to form in a MOSFET, the local resistance increases and defocuses or spreads out the current, rerouting it to cooler portions of the chip.

Because of the character of its current flow, a MOSFET has a positive temperature coefficient of resistance, as shown by the curves of Figure 4.

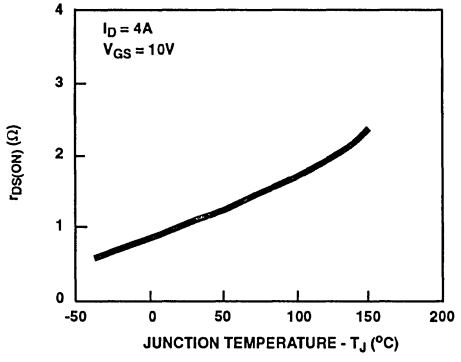


FIGURE 4. MOSFETs HAVE A POSITIVE TEMPERATURE COEFFICIENT OF RESISTANCE, WHICH GREATLY REDUCES THE POSSIBILITY OF THERMAL RUNAWAY AS TEMPERATURE INCREASES

The positive temperature coefficient of resistance means that a MOSFET is inherently stable with temperature fluctuation, and provides its own protection against thermal runaway and second breakdown. Another benefit of this characteristic is that MOSFETs can be operated in parallel without fear that one device will rob current from the others. If any device begins to overheat, its resistance will increase, and its current will be directed away to cooler chips.

Gate Parameters

To permit the flow of drain-to-source current in an n-type MOSFET, a positive voltage must be applied between the gate and source terminals. Since, as described above, the gate is electrically isolated from the body of the device, theoretically no current can flow from the driving source into the gate. In reality, however, a very small current, in the range of tens of nanoamperes, does flow, and is identified on data sheets as a leakage current, I_{GSS}. Because the gate current is so small, the input impedance of a MOSFET is extremely high (in the megohm range) and, in fact, is largely capacitive rather than resistive (because of the isolation of the gate terminal).

Figure 5 illustrates the basic input circuit of a MOSFET. The elements are equivalent, rather than physical, resistance, R, and capacitance, C. The capacitance, called C_{ISS} on MOSFET data sheets, is a combination of the device's internal gate-to-source and gate-to-drain capacitance. The resistance, R, represents the resistance of the material in the gate circuit. Together, the equivalent R and C of the input circuit determine the upper frequency limit of MOSFET operation.

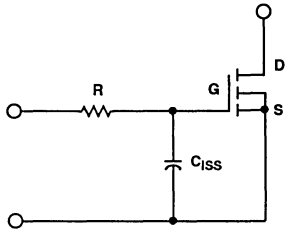


FIGURE 5. A MOSFETs SWITCHING SPEED IS DETERMINED BY ITS INPUT RESISTANCE R AND ITS INPUT CAPACITANCE C_{ISS}

Operating Frequency

Most DMOS processes develop the polysilicon gate structure rather than the older metal-gate type. If the resistance of the gate structure (R in Figure 5) is high, the switching time of the DMOS device is increased, thereby reducing its upper operating frequency. Compared to a metal gate, a polysilicon gate has a higher gate resistance. This property accounts for the frequent use of metal-gate MOSFET in high-frequency (greater than 20MHz) applications, and polysilicon-gate MOSFETs in higher-power but lower-frequency systems.

Since the frequency response of a MOSFET is controlled by the effective R and C of its gate terminal, a rough estimate can be made of the upper operating frequency from

datasheet parameters. The resistive portion depends on the sheet resistance of the polysilicon-gate overlay structure, a value of approximately 20W/□. But whereas the total R value is not found on datasheets, the C value (C_{ISS}) is; it is recorded as both a maximum value and in graphical form as a function of drain-to-source voltage. The value of C_{ISS} is closely related to chip size; the larger the chip, the greater the value. Since the RC combination of the input circuit must be charged and discharged by the driving circuit, and since the capacitance dominates, larger chips will have slower switching times than smaller chips, and are, therefore, more useful in lower-frequency circuits. In general, the upper frequency limit of most power MOSFETs spans a fairly broad range, from 1MHz to 10MHz.

Output Characteristics

Probably the most used MOSFET graphical data is the output characteristics or plot of drain-to-source voltage (V_{DS}) as a function of drain-to-source current (I_D). A typical characteristic, shown in Figure 6, gives the drain current that flows at various V_{DS} values as a function of the gate-to-source voltage (gs). The curve is divided into two regions: a linear region in which V_{DS} is small and drain current increases linearly with drain voltage, and a saturated region in which increasing drain voltage has no effect on drain current (the device acts as a constant-current source). The current level at which the linear portion of the curve joins with the saturated portion is called the pinch-off region.

Drive Requirements

When considering the V_{gs} level required to operate a MOSFET, note, from Figure 6, that the device is not turned on (no drain current flows) unless V_{gs} is greater than a certain level (called the threshold voltage). In other words, the threshold voltage must be exceeded before an appreciable increase in drain current can be expected. Generally V_{gs} for many types of DMOS devices is at least 2V. This is an important consideration when selecting devices or designing circuits to drive a MOSFET gate: the gate-drive circuit must provide at least the threshold-voltage level, but preferably, a much higher one.

As Figure 6 shows, a MOSFET must be driven by a fairly high voltage, on the order of 10V, to ensure maximum saturated drain-current flow. However, integrated circuits, such as TTL types, cannot deliver the necessary voltage levels unless they are modified with external pull-up resistors. Even with a pull-up to 5V, a TTL driver cannot fully saturate most MOSFETs. Thus, TTL drivers are most suitable when the current to be switched is far less than the rated current of the MOSFET. CMOS ICs can run from supplies of l0V, and these devices are capable of driving a MOSFET into full saturation. On the other hand, a CMOS driver will not switch the MOSFET gate circuit as fast as a TTL driver. The best results, whether TTL or CMOS ICs provide the drive, are achieved when special buffering chips are inserted between the IC output and gate input to match the needs of the MOSFET gate.

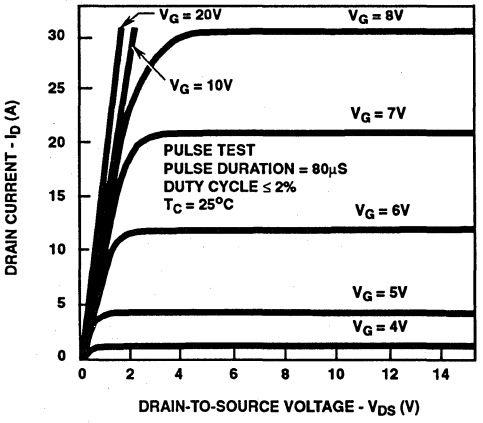


FIGURE 6. MOSFETs REQUIRE A HIGH INPUT VOLTAGE (AT LEAST 10V) IN ORDER TO DELIVER THEIR FULL RATED DRAIN CURRENT

SWITCHING WAVEFORMS OF THE L²FET: A 5 VOLT GATE-DRIVE POWER MOSFET

Author: C. Frank Wheatley, Jr. and Harold R. Ronan, Jr.

The switching waveforms of a newly announced series of power MOSFET devices called Logic Level FETs (L^2FETs) and featuring a 5V gate drive are presented and contrasted with those of the more conventional 10V gate drive devices. A new method of characterizing MOSFET switching performance is discussed in which the MOSFET is treated as a vertical JFET driven in cascade from a low voltage lateral MOS. The 2:1 advantage in rise and fall time and the 4:1 reduction in switching "dynamic $V_{(SAT)}$" dissipation with constant drive power of the L^2FET over the 10V MOSFET are demonstrated and discussed

Background

A new series of power MOSFET devices called Logic Level FETs, or L^2FETs, is compatible with the 5V power supply used for logic circuitry. L^2FETs retain the on resistance, drain current, and blocking voltage ratings of their 10V predecessors, but operate from a much less costly 5V supply.

The reduction in gate drive voltage is the result of halving the thickness of the gate insulator from the industry standard 100nm to 50nm (500Å). Since the surface inversion of the MOS channel is determined by the gate insulator voltage field, halving the insulator thickness halves the applied gate voltage without compromising drain characteristics.

The apparent conclusion from a study of the switching waveforms of the new device that halving the gate oxide thickness would double the gate capacitance and halve the switching speed does not prove true. Measurements demonstrate empirically a 2:1 increase in switching speed for the L^2FET over its 100nm predecessor, where gate drive power is the same for both devices. The "dynamic $V_{(SAT)}$" dissipation is lowered by a factor of four. The apparent anomalies are explained with the aid of a new method of switching characterization developed by treating the power MOSFET as a grounded gate, depletion mode, vertical JFET driven in cascade by a grounded source, enhancement mode, lateral MOS. The waveforms and switching characterization methods are described in detail below.

L^2FET Characteristics Compared to Standard Types - A Brief Review

Thirty-two different power MOSFETs of the L^2FET structure have been announced. These devices were designed to be totally interchangeable with the standard power MOSFET with respect to output characteristics, while offering twice the gate sensitivity, as shown in Figures 1, 2, and 3, which are comparisons of the industry standard RFM10N15 with its Logic Level FET counterpart, the RFM10N15L. (Although the L suffix notation in the type number will ultimately be valid for the entire product matrix, the L^2FET product currently available is limited to n-channel devices handling 200V or less, with 15A ratings or less.)

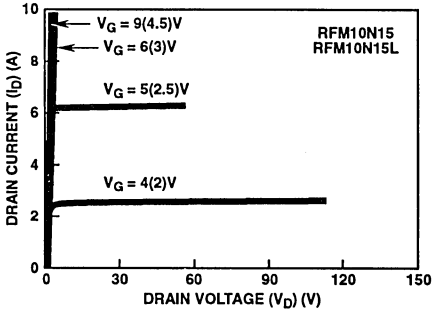


FIGURE 1. DRAIN CURRENT vs. DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES

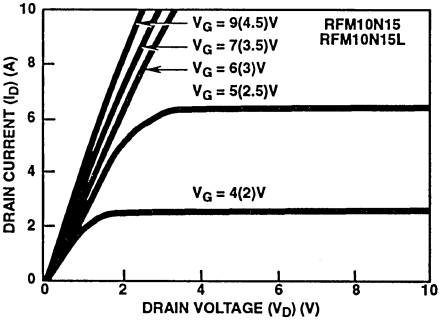


FIGURE 2. DRAIN CURRENT vs. LOW DRAIN VOLTAGE CURVES FOR REPRESENTATIVE STANDARD AND L^2FET DEVICES DEMONSTRATING THAT R_{ON} HAS NOT BEEN SACRIFICED IN THE L^2FET

Figures 1 and 2 are plots of drain current versus drain voltage with gate voltage as the running parameter. The L^2FET gate voltage is in parenthesis. The low drain voltage curves of Figure 2 demonstrate that RON has not been sacrificed in the L^2FET. Figure 3 is the transfer characteristic comparison

for three different temperatures. The abscissa has two scales to reflect the different gate sensitivities; again, L values are in parenthesis. It is evident from the curve that:

1. The threshold voltage is scaled down by a factor of two for the L^2FET.
2. The thresholf voltage temperature coefficient in mV/°C is scaled down.
3. The current level for zero temperature coefficient is unchanged.
4. The transconductance is scaled up by a factor of two.

All other L^2FETs have similar relationships to their respective predecessors.

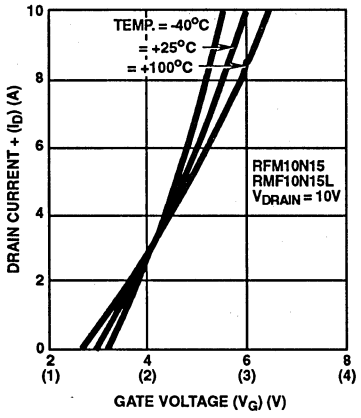


FIGURE 3. TRANSFER CHARACTERISTIC

Switching Waveforms with Conventional Drive

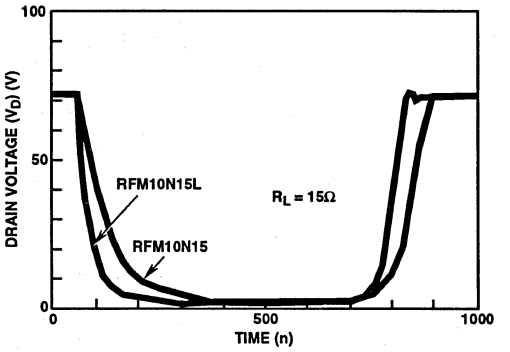
The first concern when comparing devices with such a large difference of transfer sensitivity is one of "other things being equal". If the standard device is driven between zero and ten volts with an R_G of 25Ω, impedance transformation dictates that the L^2FET should be driven between zero and five volts with an R_G of $6^1/_4$ Ω, thereby transforming open circuit voltage and short circuit current by factors of 2 (or $^1/_2$). With these parameters, either drive system will supply a peak R_G, or generator dissipation, of one watt.

Figure 4 displays the drain voltage versus time of the RFM10N15 and the RFM10N15L when each is driven as described above with a 5A, 75V resistive load line. The time scale is 100ns per division. The table under the graph compares on delay time, rise time, off delay time, and fall time for each device. The times are measured in the normal manner, that is, involving the 10% and 90% points of the input voltage and output voltage waveforms.

Note that:

1. The rise and fall times are not symmetrical
2. The is L^2FET faster
3. There is a "dynamic $V_{(SAT)}$" type of behavior
4. The "dynamic $V_{(SAT)}$" is of a lesser amplitude for the L^2FET

These observations are discussed below.



TYPE	GATE DRIVE	R_G (Ω)	$t_{D(ON)}$ (ns)	$t_{(RISE)}$ (ns)	$t_{D(OFF)}$ (ns)	$t_{(FALL)}$ (ns)
RFM10N15 (100nm)	0-10V	25	15	120	123	73
RFM10N15L (50nm)	0-5V	6.25	11	57	104	62

FIGURE 4. DRAIN VOLTAGE vs. TIME CURVES FOR REPRESENTATIVE STANDARED AND L^2FET DEVICES

Switching Waveforms with Constant Current Drive

The power MOSFET is a current driven device during transitions due to the charging or discharging of capacitances. In actual applications, most drive circuits exhibit a first order approximation to a constant current where the voltage compliance is determined by ground potential or the drive circuit power supply voltage. The on current may not equal the off current; this situation is addressed below.

Figure 5 presents the curves for the RFM10N15 and RFM10N15L when each is driven from a current generator whose $I_{G1} = I_{G2}$, with gate voltage limits of zero and 10 or (5) volts. The drive current is kept the same for both devices in this case even though the L^2FET receives less drive power or energy. The value for I_{G1} and I_{G2} was chosen as 5mA; the time scale is 1μs/division.

Note that:

1. The rise and fall times of a given device are the same with current drive.
2. The two devices have similar output waveforms in most regions.
3. There is a persistent "dynamic $V_{(SAT)}$" even at slow switching speeds.

4. The "dynamic $V_{(SAT)}$" curves are symmetrical during the low drain voltage portion of the turn on and turn off portion.
5. The "dynamic $V_{(SAT)}$" curves are lower in amplitude by a factor of approximately two for the L^2FET.

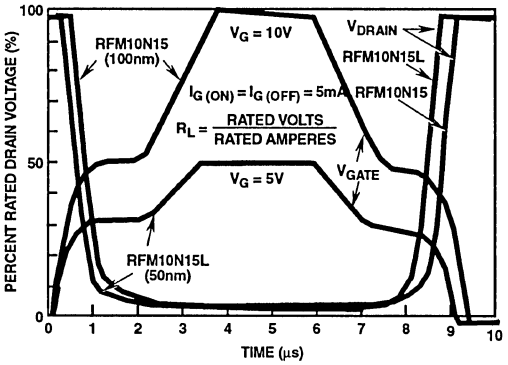


FIGURE 5. CHARACTERIZATION CURVES FOR REPRESENTATIVE DEVICES DRIVEN FROM A CURRENT GENERATOR

Large Signal Equivalent Circuit of the MOSFET

If we are to understand the differences and similarities of the L^2FET relative to the conventional power MOSFET, the conventional poer MOSFET must first be understood. Figure 6 shows a properly proportioned cross sectional view of the power MOSFET.

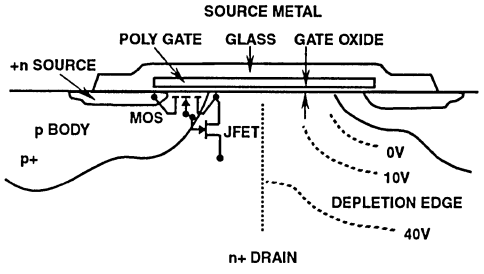


FIGURE 6. CROSS SECTION OF POWER MOSFET

When the drain voltage is very low and the gate is forward biased, an accumulation layer exists for the n- region beneath the gate. This layer may be thought of as serving the function of the drain for the lateral MOS. In addition, it serves as a source for a vertical depletion mode JFET. The gate of the JFET is formed by the body diffusion, particularly in the neck region. The JFET drain is the n+ region usually though of as being the MOSFET drain. This situation is shown in Figure 6, where the cross sectional view of the MOSFET is shown. The lateral MOS and the vertical JFET are schematically implied by the left half of Figure 6. The right half indicates the edge of the depletion width for several drain voltges. Note how the JFET pinches off, such that increased drain voltage is supported predominately by the JFET. This structure is schematically represented as shown in Figure 7. Note that the third quadrant diode is caused by the p-n junction associated with the gate and drain characteristic (common to all JFETs). A parasitic n-p-n transistor is not shown, nor is it discussed in this Note. Voltage node (4) is within the device, and is not precisely a single node, as represented.

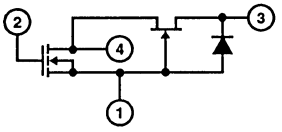


FIGURE 7. SCHEMATIC REPRESENTATION OF THE CROSS SECTION OF FIGURE 6

Interelectrode Capacitance

The equivalent circuit of Figure 7 contains four voltage nodes. Therefore, six capacitors will exist to couple these nodes. The switching waveforms are determined by these capacitors and the samll signal equivalent circuit of the MOS and JFET. Of course, the MOS and JFET small signal equivalent circuits are nonlinear functions of voltage and current and invarient with frequency. Similarly, the capacitors are nonlinear with voltage and current.

Industry data sheets show three terminal characterization of this four node network at zero drain current. Under this condition, the transconductance and output resistance are zero and infinity for both the MOS and the JFET. This condition reducesthe power MOSFET to the capactor network of Figure 8, which may be replaced by three capacitors. Note that this situation is valid only when no MOSFET current flows.

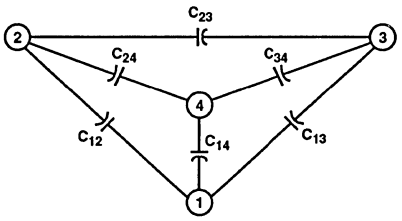


FIGURE 8. CAPACITOR NETWORK REPRESENTATION OF THE POWER MOSFET

When current does flow, node (4) of Figure 7 is a low impedance node due to the source follower characteristic of the JFET. Similarly, nodes (1) and (3) are generally low impedance nodes by virtue of the ground reference and the load resistance. Therefore, capacitive currents will usually be significant only to the input node, (2). Capacitors C_{12}, C_{23}, and C_{24} are examined below over most of the switching regime when current is flowing.

Gate to Source Capacitance, C_{12}

When all of the die except the actual MOSFET cells are ignored, Figure 6 shows that the gate to source capacitance (C_{12}) is that from the poly gate upward through the thick oxide to the source metal. In addition, there is a contribution from the poly gate to the n+ source through the thin gate oxide. Additionaly a fringing capacitance exists at the edge of the polysil gate. These components of C_{12} are invariant with voltage and current. There is a fourth component from the poly gate to a region about half way along the MOS channel through the gate oxide. This component is actually distributed, and varies somewhat with current and voltage.

Gate to Drain Capacitance, C_{23}

Capacitor C23 exists only when no accumulation layer is present beneath the poly gate. Otherwise, the accumulation layer acts as an electrostatic shield. This layer exists whenever the drain voltage immediately beneath the gate oxide is essentially negative relative to the poly gate. In addition, the capacitive coupling from drain to gate diminishes greatly when the JFET is pinched off. Therefore, C23 exists for only a small range of drain voltage. In addition, it should decrease rapidly as the pinch-off voltage level is approached because the effective area of concern is closed off similarly to the aperture of a camera (for a hex cell).

Gate to Internal Electrode Capacitance, C_{24}

Capacitor C_{24} is rather large for positive gate voltages. It is made up of that area between the poly gate and the accumulation layer, plus some of the area between the poly gate and the moddle of the MOS channel. In both cases, the dielectric is the thin gate oxide. So long as the gate voltage is positive relative to the n- layer beneath the poly gate, the accumulation layer exists and C_{24} is invariant. This accumulatin layer ceases to exist when the external drain voltage minus the IR drop through the n- neck region approximately equals the gate voltage. The area associated with the accumulation layer (JFET cathode) rapidly decreases with increased drain voltage. In addition, a depletion layer may now form, leading to a further reduction of C_{24}.

Waveforms Expected from the Model

The following discussion relates the prior model discussion to the waveforms of Figure 5. The discussion begins with the gate voltage at +5V or +10V and the gate current equal to zero. This condition corresponds to saturated behavior, where the drain current is approximately equal to I_D(max) and the drain voltage equals I_D(max) times R_{DS}(ON).

Gate Voltage Slope - t_{OFF} Delay

As time progresses, I_G = -5mA, which must flow through C_{12} + C_{23} + C_{24} of Figure 8 because the MOS and JFET are both heavily biased into conduction. Therefore, $dV_4/dt = dV_3/dt$ = nearly 0. With large positive gate bias and drain voltage near zero, C_{23} is zero and C_{12} and C_{24} are constant. As a result, the gate voltage should be a straight line with a slope equal to:

$$dV_G/dt = I_G/(C_{12} = C_{24}) \quad (1)$$

Gate Voltage Plateau

As the gate voltage decreases, the drain voltage will increase imperceptibly at first until the gate voltage drops enough to bias the MOS into its constant current mode. At this point, the very high transconductance of the MOS is consistent with very little change in gate voltage to reduce the current by several percent. Several percent change in drain current corresponds to many volts in drain voltage. As a result, the gate current no longer flows from C12 during the constant gate voltage plateau.

Drain Voltge Shallow Slope

Since C23 is still zero, all gate current must flow from C24. Assuming that the gate voltage is plateaued and that the JFET is still heavily forward biased, node 4 of Figure 7 must ramp at linear rate. Therefore, the JFET must also ramp at this same rate.

$$dV_D/dt = I_G/C_{24} \quad (2)$$

Again this curve will approximate a straight line.

Drain Transition Voltage

As mentioned above, C_{24} rapidly decreases once the drain voltage is slightly greater than the gate voltage. (Actually, this voltage is the n- voltage directly beneath the gae oxide, and differs from the drain voltage by an amount nearly equal to $I_D r_{DS}$(on).)

Since the drain voltage is still firly low and the drain current has not changed much, the gate plateau voltage still exists. Equation 2 still applies except that the value of C_{24} has materially decreased and C_{23} has become finite. This situation results in a substantial increase in dV_D/dt.

JFET Pinch Off Voltage - Drain Voltage Steep Slope

As the drain voltage approaches the pinch off voltage of the JFET, the JFET comes out of saturation and starts to support MOSFET drain voltage. The voltage gain of the active JFET permits large changes in the JFET drain voltage for small changes in its source-to-gate voltage. But the JFET sour-to-gate voltage is the lateral MOS drain-to-source voltage, which is dominated by equation 2 (but for low values of C_{24}).

Gate Voltage Curvature from Plateau

As the drain voltage increases, the drain current decreases. This condition requires significant decrease in gate voltage until the gate threshold is approached. A significant portion of the gate current must now flow through C_{12}. This flow produces a gradual transition in the gate voltage and some slowing of the drain voltage waveform.

Gate Voltage Slope - $t_{(ON)}$ Delay

When the drain is totally off, most of the gate current flows from C12. Again,this capacitance is constant, so that the waveform is a straight line with a slope equal to:

$$dV_G/dt = I_G/C_{12} \quad (3)$$

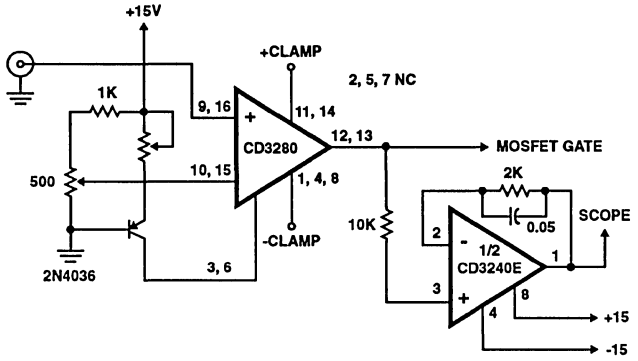


FIGURE 9. TEST CIRCUIT

New Switching Characterization for Power MOSFETs

The above discussion suggests that a new method of characterization may be provided for resistive switching with power MOSFETs, where constant current gate drive is employed during the transition time.[1] The below method bears some similarity to the gate charge concept.[2] The state of the gate charge is a continuous plot in this work, however, rather than a single point. This approach permits a knowledge of all waveforms with any drive dircuitry, rather than just the total elapsed time. In addition, the total elapsed time is fixed (at just under 50 microseconds) by choosing the required value of constant gate current. Circuit designers are usually more comfortable with milliamperes and microseconds (although the product is charged in nanocoulombs).

Test Circuit - Drive

A test circuit is shown in Figure 9. The heart of this circuit is the Harris CA3280 integrated circuit. This is an operational transconductance amplifier (OTA) operated as a comparator. An OTA is a current output circuit where the output current and output transconductance are programmed by the amplifier bias current (I_{ABC}). Internal chip circuit feedback assures an extremely high output impedance within a compliance range established by the supply voltages. The circuit of Figure 9 is actually two OTA's in parallel. The linearizing diodes on this chip are not used.

A value of I_{ABC} is established from the collector of the 2N4036. The current into the load (the gate of the MOSFET under test) may be varied between $+I_{ABC}$ and $-I_{ABC}$ times a constant of proportionality (approximaetly 0.9). The actual value depends upon the input differential input voltage. As a comparator, the differential voltage is large resulting in saturated behavior of $\pm I_{ABC}$. If the gate voltage comes within a volt of the rail voltages, this current goes to zero, producing a clamping voltage. For the purposes of this Note, these supply voltages are adjusted to clamp 0 volts and +10 volts for the normal n-channel MOSFET. The behavior of this IC is excellent from submicroamperes to about 2.5mA. Higher current may be achieved by stacking many CA3280 packages one on top of another and soldering the leads to aprallel the chips rather than wiring many sokets. However, this arrangement may require an increase in the bypass capacitor values.

A CA3240E MOS input op amp is used as a unity gain follower. Otherwise, the 1mΩ or 10mΩ shunting impedance of the scope would load the high impedance circuitry associated with the MOSFET gate.

Testing Conditions

A pulse generator is set for 50µs on time duration and approximately 25ms repetition rate (about 0.2% duty cycle). The ± clamp voltages are set to the appropriate values. The power MOSFET load resistor is chosen to equal the maximum rated voltage divided by the maximum rated current.

With a low value of drain supply voltage, observe the gate voltage while adjusting I_{ABC}. A convenient set f conditions occurs when a short dwell time of several µs exists at the +10V level. Minor adjustments may be desired for IABC as the drain supply voltage is increased to maximum rated value. The L^2FETs would be tested at +5V gate clamp.

Figure 10 exhibits the pertinent waveforms for an RFM15N15. All power MOSFETs have similar waveforms. Figure 10(a) is the 3V signal to the CA3280. Figure 10(b) is the power MOSFET gate current. In this example, the amplitude is ±1mA with a third state of 0mA. Figure 10(c) displays the gate voltage and the drain voltage, 10V peak-to-peak and 150V peak-to-peak. Figure 10(d) is a piece wise linear approximation of Figure 10(c). The datum line is zero volts and applies to both waveforms. The time scale of the waveforms of Figure 10 is 100µs full scale.

There are some features of the gate and drain voltage waveforms that should be noted. These features are consistent with the equivalent model discussion.

1. The waveforms during the positive gate current time are symmetrical to those during the negative gate current time. Exceptions will occur for very fast or very slow switching, and for nonsymetrical current drive. These exceptions are discussed in the following.

2. The drain voltage waveform contains a rather steep slope with a fairly constant dv/dt over most of the drain voltage excursion.
3. The drain voltage contains a rather shallow slope with a fairly constant dv/dt over the remainder of the drain voltage excursion.
4. The drain transition voltage (defined as the intercept of the above two near straight lines) typically occurs when the drain voltage equals the sum of the gate voltage (at that instant of time) plus the product of the drain current times $r_{DS}(on)$.
5. The gate voltage waveform contains three near straight line segments during the positive gate current transition time.

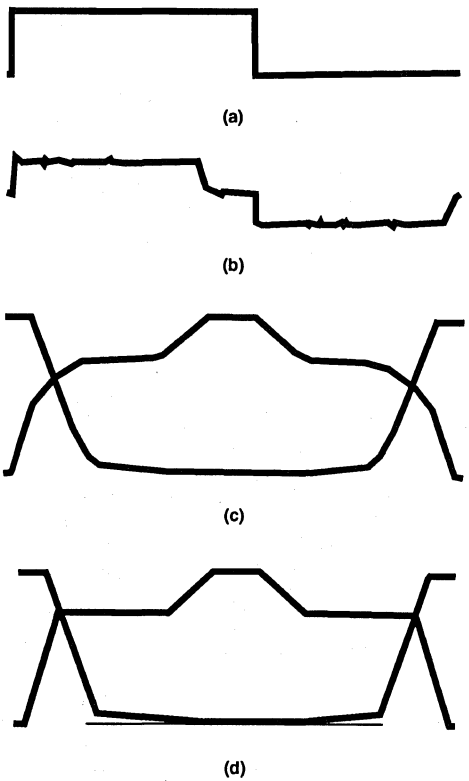


FIGURE 10. (a) 3V SIGNAL TO THE CA3280, (b) POWER MOSFET GATE CURRENT, (c) GATE AND DRAIN VOLTAGE, (d) PIECE WISE LINEAR APPROXIMATION OF 10(c)

Application of the Switching Data

Figure 11 is a family of curves similar to Figure 10(c), where the drain supply voltage is fixed at four values. Note that the ordinate is 10V full scale for the gate voltage, while it is normalized to 100% of maximum-rated drain voltage for the drain-voltage curves. All four sets of curves are taken with a predetermined gate current, $\pm I_T$. The abscissa is also normalized to 100 (I_T/I_G) microseconds full scale, where I_G is the actual gate drive current. With this characteristic curve, switching behavior may be readily predicted for almost any driving circuit, provided the load is resistive.

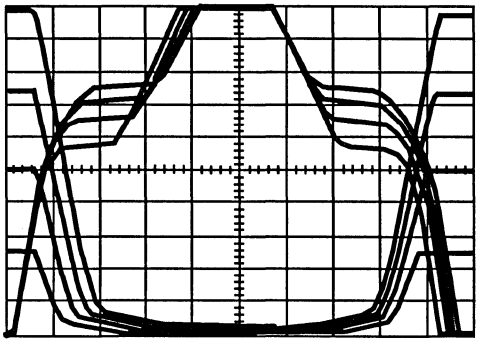


FIGURE 11. CURVES SIMILAR TO THOSE OF FIGURE 10(c) WITH DRAIN SUPPLY VOLTGE FIXED AT FOUR VALUES

Symmetrical Current Drive

Waveforms of Figure 11 will scale in an inverse manner with gate current. Driving current was varied from ±200mA to ±2μA for the device of Figure 1l. Measurements of delay time (on), rise time, delay time (off), and fall time are plotted in Figure 12 and compared to the inverse scaling suggested by Figure 11.

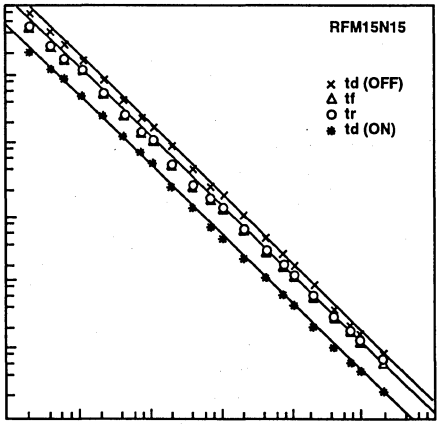


FIGURE 12. VARIOUS TIME MEASUREMENTS COMPARED TO THE INVERSE SCALING SUGGESTED BY FIGURE 11.

It is anticipated that very slow switching (in the millisecond region) will result in the chip thermally tracking the power dissipation, which would cause some deviation from the

inverse scaling. This condition was not noted on Figure 12 for gate currents as low as ±2μA.

Large gate currents result in very fast switching waveforms. The gate of each hex cell is accessed through a gate pad and gate runners, which are of a low resistivity metal followed by buried polysilicon of a moderate resistivity. Asa result, the high gate currents cause a propagation delay to exist for those cells far removed from the gate runners. This effect is not seen in Figure 12, even though the gate current was increased to ±200mA.

Asymmetrical Current Drive

The positive and negative gate drive will often be dissimilar. Of course, the scaling must reflect this situation. At other times the gate current varies with amplitude. This condition is always true when driving from a pulse generator of fixed resistance. Piecewise linear methods will yield the gate current, which will permit the proper piecewise linear scaling. This calculation could be done in the following manner:

1. Mark eleven small x's along the gate waveform of Figure 11 dividing it into 10 equal voltage segments; for example, V_G = 0, 1, 2, . . . 9, 10V.
2. Draw a vertical line through each x the full height of the figure, creating 10 time segments.
3. If the driving-pulse amplitude is 0 to 10 volts with an internal resistance of 100 ohms, calculate the piecewise linear gate current for each time segment. I_{G1} = (10 - 0.5)/100 = 95mA, I_{G2} = (10 -1.5)/100 = 85mA, etc.
4. Then scale each waveform within the pertinent time segment by the proper gate current.
5. Smooth the curves.
6. Create 10 more time segments for the right half of Figure 11 corresponding to an average gate voltage of 9.5,8.5, . . . 1.5, 0.5 volts. Call these segments 11,12,... 19,20.
7. In that the pulse-generator voltage is now zero volts, calculate I_G as:
   I_{G11} = (0-9.5)/100 = -95mA, I_{G12} = (0-8.5)/100 = -85mA, etc.
8. Repeat 4 and 5. L^2FETs would be treated with smaller voltage segments.

Generally, the gate-voltage plateau of Figure 11 will not be located at the middle of the pulse-generator amplitude (5 volts). As a result, rise and fall times measured this way experience differing gate currents and are "nonsymmetrical". This type of measurement will also lead one to observe temperature sensitivities, load-current sensitivities, and device-to-device variability, all of which are more circuit dependent than device dependent.

Source-Lead Inductance

The gate-voltage waveforms may be corrected by the voltage across the source-lead inductance and external inductance, which may be mutually common to the input and output current loops. This voltage, L di/dt, may be approximated and applied to the gate-voltage waveform after scaling Figure 12 for the actual gate currents. Generally, this effect is not appreciable for gate current small relative to ±100mA. A very loose circuit wiring arrangement with inches of mutually common source wire will exaggerate this effect.

Gate Voltage Propagation Effects

Most power MOSFET applications need switch no faster than tenths of a microsecond, but should faster switching be required, this section will become important. It must be understood that the power MOSFET appears as a distributed network of many cells when used for very fast switching.

The thousands of individual MOSFET cells are connected in parallel with highly conductive metal for the sources and drains. However, the gates are paralleled with a moderately conductive film of doped polysilicon. As a result, a very steep voltage wavefront applied to the gate pad will bias those cells close by, but a delay will occur for turn on or turn off. Because of the nonlinear "input capacitance" of each cell, the delay cannot be characterized by a pure number of so many nanoseconds.

Presently, most manufacturers characterize typical switching speed for a single test condition. The test conditions are usually chosen to present the most favorable result, usually near the upper limit of usefulness.

Figures 13(a), (b), and (c) show the increasing effect of gate voltage propagation. The gate waveform is the only one shown because the drain is not affected so drastically. This is true because some cells are overdriven, offsetting the effect of the starved cells. Care must be exercised when operating with large gate effects similar to those of Figure 13(c).

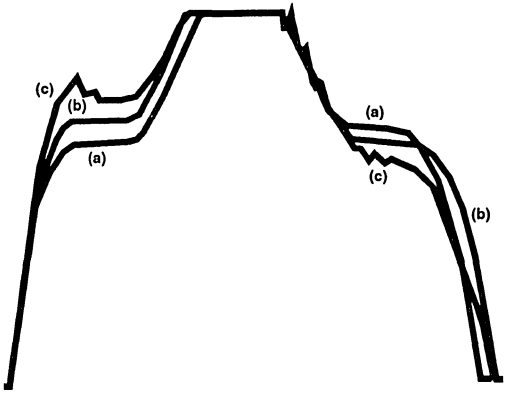


FIGURE 13. CURVES SHOWING THE INCREASING EFFECT OF GATE VOLTAGE PROPAGATION

Gate-propagation effects may be reduced by the following design methods:

1. Many gate runners.
2. More conductive polysilicon.
3. Silicide rather than polysilicon gates.
4. Less cells (resulting in lower transconductance and higher R_{ON}).
5. Substantially different lateral and vertical structure.
6. High-frequency packaging.

None of the above methods will yield "breakthrough" devices unless used in combination.

Any of the previous methods require trade-offs which would not be attractive to the needs of most components users. These trade-offs are in the realm of:

1. Reduction of R_{ON} per unit area.
2. Decreased yield.
3. Added cost (beyond the cost of yield impact).
4. RFI, self-oscillation, and other problems characteristic of very fast devices.

References

1. "Power MOSFET Switching Waveforms - A New Insight," H. R. Ronan, Jr., and C. F. Wheatley, Jr., Proc. Powercon 11, April 1984.
2. "Correlating the Charge-Transfer Characteristics of Power MOSFETs with Switching Speed," E. Oxner, Proc. Powercon 9, April 1982.

APPNOTE

No. 7260.1 May 1992

POWER MOSFET SWITCHING WAVEFORMS: A NEW INSIGHT

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The examination of power MOSFET voltage and current waveforms during switching transitions reveals that the device characterization now practiced by industry is inadequate. In this Note, device waveforms are explained by considering the interaction of a vertical JFET driven in cascode from a lateral MOSFET in combination with the interelectrode capacitances. Particular attention is given to the drain-voltage waveform and its dual-slope nature. The three terminal capacitances now published by the industry are shown to be valid only for zero drain current. For cases where the gate drive is a voltage step generator with internal fixed resistance, the drain voltage characteristics are inferred from the gate current drive behavior and compared to observed waveforms. The nature of the "asymmetric switching times" is explained.

A waveform family is proposed as a more descriptive and accurate method of characterization. This new format is a plot of drain voltage and gate voltage versus normalized time. A family of curves is presented for a constant load resistance with V00 varied. Gate drive during switching transitions is a constant current with voltage compliance limits of 0 and 10 volts. Time is normalized by the value of gate driving current. The normalization shows excellent agreement with data over five orders of magnitude, and is bounded on one extreme by gate propagation effects and on the other by transition time self-heating (typically tens of nanoseconds to hundreds of microseconds).

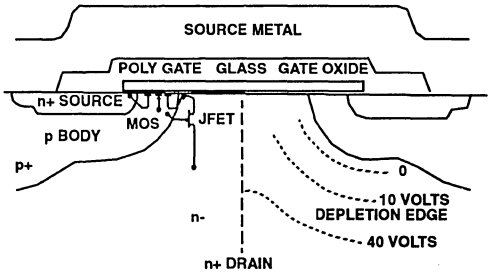


FIGURE 1. CROSS-SECTIONAL VIEW OF MOSFET SHOWING EQUIVALENT MOS TRANSISTOR AND JFET

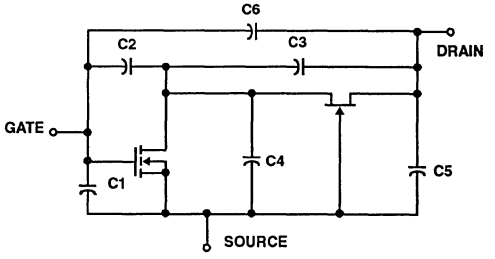


FIGURE 2. MOS TRANSISTOR WITH CASCODE-CONNECTED JFET AND ALL CAPACITORS

Device Models

The keystone of an understanding of power MOSFET switching performance is the realization that the active device is bimodal and must be described using a model that accounts for the dual nature. Buried in today's power MOSFET devices is the equivalent of a depletion layer JFET that contributes significantly to switching speed.Figurei is a cross-sectional view of a typical power MOSFET, with MOSFET/JFET symbols superimposed on the structure.

Figure 2 is obtained by taking the lateral MOS and vertical JFET from this conception and adding all the possible node-to-node capacitances. Computed values of the six capacitances for a typical device structure suggest that device behavior may be adequately modeled using only three capacitors in the manner of Figure 3. This is the model to be employed for analysis and study

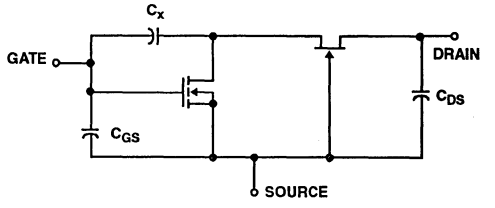


FIGURE 3. FIGURE 2 SIMPLIFIED

Gate Drive: Constant Voltage Or Constant Current

Before moving on to the study of the equivalent circuit states of the model, a gate-drive forcing function which is easy to represent, relates to reality, and best illustrates device behavior must be chosen. The choice may be immediately narrowed to two:

(1) An instantaneous step voltage with internal resistance R, Figure 4.

(2) An instantaneous step current with infinite internal resistance, Figure 5.

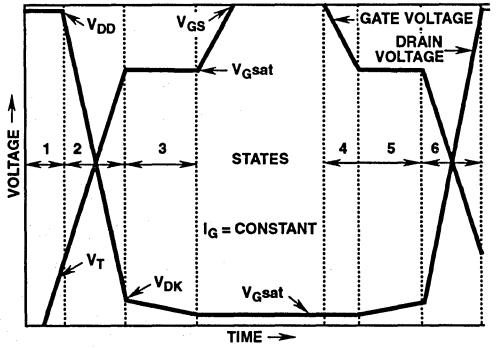


FIGURE 4. IDEALIZED POWER MOSFET WAVEFORMS

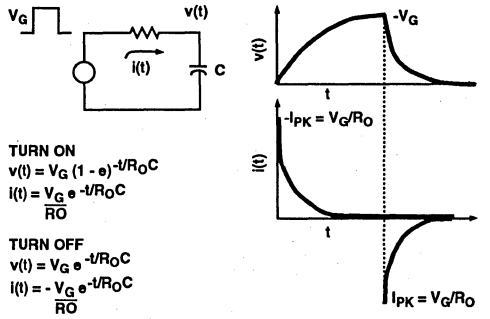


FIGURE 5. STEP-VOLTAGE FORCING FUNCTION

Power MOSFET devices are highly capacitive in nature; hence, simple capacitor responses to the forcing functions offer a good vehicle for comparison. The advantageous choice is immediately obvious: Figure 5. Voltage/time responses dominated by capacitance are straight lines (when constant current is used). The slope of these lines is

proportional to current and inversely proportional to capacitance. Analytically, then, constant current is most convenient. It is quite another matter, however, to build a bidirectional current drive that is accurate across the many decades of both current and time required to establish experimental verification.

Six States

To completely characterize power MOSFET switching waveforms, the six states that a device assumes, Figure 6, must be addressed:

STATE	MOS	JFET
Turn-on 1	Off	Off
Turn-on 2	Active	Active
Turn-on 3	Active	Saturated*
Turn-off 4	Saturated	Saturated
Turn-off 5	Active	Saturated
Turn-off 6	Active	Active

*The term saturated is taken to mean a constant low-voltage drain-source condition.

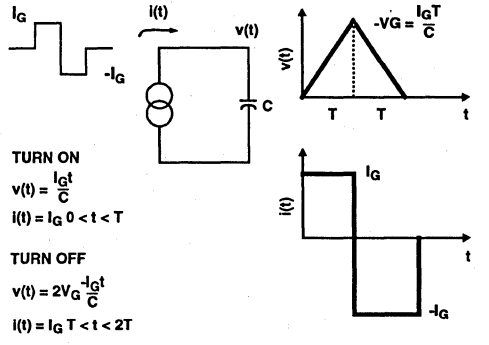
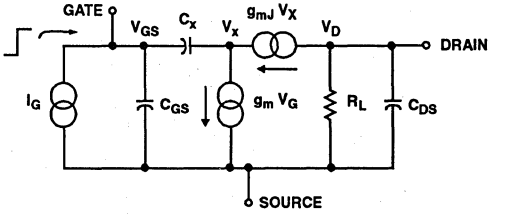


FIGURE 6. STEP CURRENT FORCING FUNCTION

Equivalent Circuit

The lumped-parameter model of Figure 3, with the cascode-connected JFET, can now be reduced to the linear equivalent circuit of Figure 7, and the six device states investigated from full off to full on.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_m	- MOSFET Transconductance
V_D	- Drain Voltage	g_{mJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_x	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE 7. POWER MOSFET EQUIVALENT CIRCUIT

State 1: MOS Off, JFET Off

In a power-MOSFET device, no drain current will flow until the device gate threshold voltage, V_T, is reached. During this time, the gate current drive is only charging the gate source capacitance. More accurately, I_G is charging C_{iss} ($C_{iss} = C_{GS} + C_{GD}$, C_{DS} shorted), the capacitance designation published by the industry.

The current generators, $g_m v_g$ and $g_{mJ} V_x$ are open circuits for zero drain current, and R_L is presumed to be so low as to represent a short circuit (generally true for practical applications). This is academic however since C_{GS} is very much larger that C_6. The time to reach threshold, then, is simply:

$$T = \frac{C_{iss} V_T}{I_G}$$

State 2: MOS Active, JFET Active

This state graphically illustrates the dramatic influence that the JFET has on the power MOSFET drain-voltage wave- form. Instead of having to discharge C_x from V_{DD} to ground, the lateral MOSFET need only swing v_X to ground, a much smaller voltage thanks to the grounded gate JFET. Since the interaction of R_L with the device capacitances has a second-order effect on the drain voltage, the equivalent circuit of Figure 7 predicts a drain voltage change of:

$$dv_G/dt = g_m R_L I_G/[C_{GS} + C_X(1 + g_m/g_{mj})]$$

In all but the smallest power-MOSFET devices, C_x is several thousand picofarads and g_m/g_{mj} is of the order of 3:1. Power-MOSFET devices exhibit a high dv_D/dt switching rate because of the cascode-connected J FET, not because C_{rss} ($C_{rss} = C_{GD}$) is a small value, as zero-drain-current data- sheet capacitance values might lead one to believe. If C_{rss} were, in actuality, small, long drain voltage tails would not exist. The tail response is a direct result of JFET saturation. In order to delineate the transition from state 2 to state 3, a drain voltage at which the transition occurs must be defined. V_{DK} is the knee voltage at which linear extrapolations of drain-voltage slopes intersect. The time duration of state 2 is:

$$t = (V_{DD} - V_{DK})[C_{GS} + C_X(1 + g_m/g_{mJ})]/g_m R_L I_G$$

State 3: MOS Active, JFET Saturated

When the JFET saturates, the $g_{mJ} V_x$ current generator becomes a short circuit and the equivalent circuit predicts:

$$dv_D/dt = g_m R_L I_G/[C_{GS} + C_X(1 + g_m R_L)]$$

This is the Miller effect so often referred to in older texts that describe the behavior of grounded-cathode vacuum-tube amplifier circuits. Allowing for the fact that $1 + g_m R_L$ is approximately equal to $g_m R_L$ and $C_x(1 + g_m R_L)$ is very much larger than C_{GS}, the expression for drain-voltage tail time is:

$$t = (V_{DK} - V_D[sat])C_x/I_G$$

State 4: MOS Saturated, JFET Saturated (Turn-Off)

In this state, in addition to $g_{mj} V_x$ being shorted, the $g_m V_G$ current generator is shorted, and I_G is occupied with charging C_x and C_{GS}, in parallel, from the peak value of V_G to V_G(sat). The time required for this is:

$$t = (V_G - V_G(sat))(C_{GS} + C_x)/I_G$$

Since a value for C_{GS} may be measured independently of switching time, the method described is the simplest way of determining C_x.

On turn-off, the state time equations are equally applicable, but in reverse order (states 5 and 6); see the idealized waveform of Figure 4.

Experimental Verification

The four switching states just analyzed indicate that for a given device, all four switching state times are inversely proportional to the magnitude of the gate drive current. Figure 8 illustrates the switching performance of a typical power MOSFET across three decades of gate drive current and time. In each case the data slope is almost a perfect -1.

A New Device Characterization

Figure 8 could not be a reasonable device data sheet presentation because it does not give the designer any information on a typical value for C_x, nor does it convey how V_{DK}, g_m, g_m/g_{mJ}, and V_G(sat) vary with drain current. What would be of enormous value to the designer is a plot of $v_D(t)$, $v_G(t)$ for selected values of V_{DD} and I_D within device ratings.

A reasonable characterization would be as follows:

1. The x axis would be normalized in terms of gate current drive.
2. The y axis would be normalized in terms of percent maximum rated V_D (0 to 100%).
3. $R_L = V_D(max)/I_D(max)$ would define the drain load resistance.
4. Four plots of $v_D(t)$, $v_G(t)$ at 100%, 75%, 50%, and 25% V_D(max) would be shown.

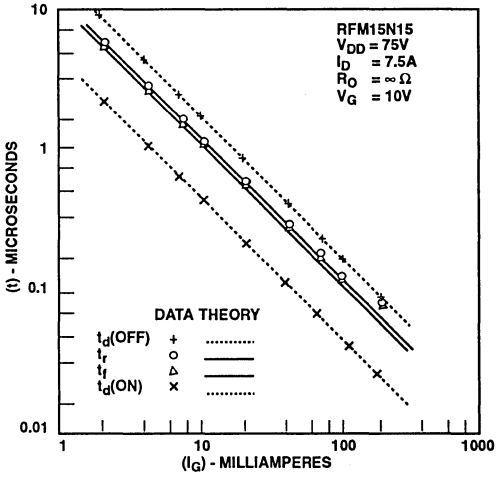


FIGURE 8. CONSTANT GATE CURRENT SWITCHING TIME

Figure 9 is such a plot for the RFM15N15 power MOSFET. With such a plot, a designer can estimate device switching performance under any resistive gate/drain conditions.

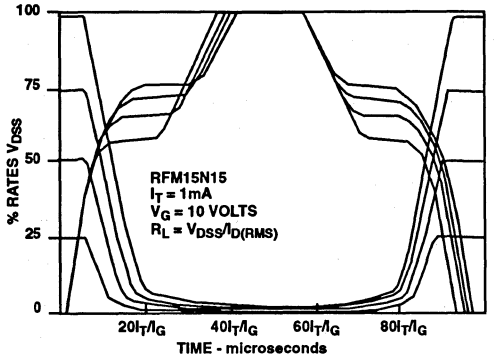


FIGURE 9. NORMALIZED RFM15N15 SWITCHING WAVEFORMS FOR CANSTANT GATE-CURRENT DRIVE.

Step-Voltage Gate Drive

The majority of power MOSFET applications employ a step gate-voltage input with a finite source resistance R_O.Often R_O for turn-on is not the same as R_O for turn-off. How can switching times for these situations be estimated using the switching characterization curves just described? The analysis for resistive step voltage inputs, which is complex because the gate current is no longer constrained to be constant, but is a function of device gate-voltage response, is covered in Appendix A. (A second, shorter appendix, B, has been added to illustrate the estimation of R0 for some practical gate drive circuits.) Table I summarizes the common switching equations, and indicates the appropriate 1G to be used in each state for relating step voltage drives to the characterization curves.

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus 1/R0 to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figs. 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current VU/R0 equalling the constant 1G, t6(on), t, td(off), and t1 will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t, t1 switching symmetry is disrupted by the use of a step voltage with source resistance R0. For states 2 and 6 the time ratio is:

TABLE 1. COMMON SWITCHING EQUATIONS

	CONSTANT CURRENT	STATE 1: MOS OFF, JFET OFF	CONSTANT VOLTAGE
TURN ON	$t = \frac{C_{iss} V_T}{I_G}$		$t = R_O C_{iss} \ln \frac{[1]}{[1 - V_T/G_V]}$
	$I_G = I_T$	STATE 2: ACTIVE, ACTIVE	$I_G = (V_G - V_T)/R_O$
	$t = \frac{[V_{DD} - V_D K][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		
	$I_G = I_T$	STATE 3: ACTIVE, SATURATED	$I_G = (V_G - V_{Gsat})/R_O$
	$t = \frac{(V_{DK} - V_{Dsat})C_x}{I_G}$		
TURN OFF	$I_G = I_T$	STATE 4: SATURATED, SATURATED	$I_G = -V_G/R_O$
	$t = \frac{(C_{GS} + C_x)(V_G - V_{Gsat})}{I_G}$		$t = R_O(C_{GS} + C_x) \ln (V_G/V_{Gsat})$
	$I_G = I_T$	STATE 5: ACTIVE, SATURATED	$I_G = (V_G - V_{Gsat})/R_O$
	$t = \frac{(V_{DK} - V_{Dsat})C_x}{I_G}$		
	$I_G = I_T$	STATE 6: ACTIVE, ACTIVE	$I_G = (V_G - V_{Gsat})/R_O$
	$t = \frac{[V_{DD} - V_D K][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_G}$		

Experimental Verification

Since the switching equations for step currents and voltages differ only by gate-current magnitudes for the same device type, one would expect a plot of switching time versus $1/R_O$ to be of the same form as those obtained for a step current drive. This is exactly the case, as Figure 10 is merely a variation of Figure 8. Using the relationships of Table I, the observed differences between Figs. 7 and 9 can be pinpointed. The two sets of experimental curves confirm that, on the basis of the short-circuit drive current V_G/R_O equalling the constant I_G, $t_d(on)$, t_r, $t_d(off)$, and t_f will all be longer, as predicted by the ratios of the gate drive currents of Table 1. Notice also that t_r, t_f switching symmetry is disrupted by the use of a step voltage with source resistance R_O. For states 2 and 6 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_T}$$

For states 3 and 5 the time ratio is:

$$\frac{t_{turn\text{-}on}}{t_{turn\text{-}off}} = \frac{V_G(sat)}{V_G - V_G(sat)}$$

Utilization of available maximum gate drive voltage and current can be optimized for fastest power MOSFET switching speed through the use of constant-current gate drive at the expense of increased gate-drive circuit complexity.

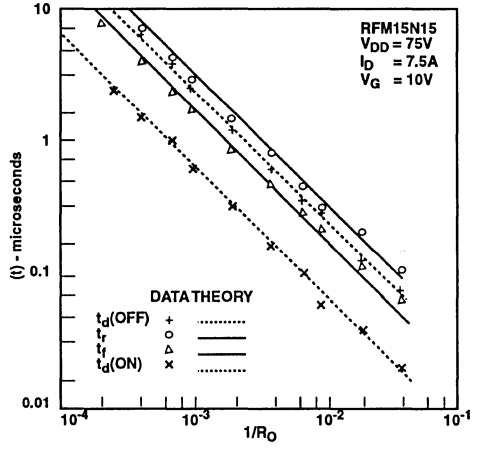


FIGURE 10. CONSTANT GATE VOLTAGE SWITCHING TIME

Using The Characterization Curves, Figure 9

To estimate the switching times for an RFM15N15 power MOSFET under the conditions V_G = 10V, V_{DD} = 75V, R_O = 100 ohms, and R_L = 10 ohms, precedes as follows:

State 1: MOS Off, JFET Off

This time can be estimated without recourse to the curves

$t = 100(1200 \times 10^{-12})$ in [1/(1 - 4/10)]

$t = 61$ ns

State 2: MOS Active, JFET Active

$I_G = (10 - 4)/100 = 60mA$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{60} = \frac{9}{60} = 150\ ns$$

State 3: MOS Active, JFET Saturated

$I_G = (10 - 7)/100 = 30mA$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{30} = \frac{14}{30} = 467\ ns$$

State 4: MOS Saturated, JFET Saturated

$C_{GS} + C_x$ = (gate voltage slope)(test current)

= $(1.5 \times 10^{-6}s/5\ volts)(10mA)$

= 3000pF

$t = 100(3000 \times 10^{-12})$ in [10/6.6]

$t = 125ns$

State 5: MOS Active, JFET Saturated

$I_G = 6.6/100 = 66mA$

$$t = \frac{(\text{curve divisions}) \times I_T\ \mu s}{66} = \frac{8}{66} = 121\ ns$$

Figure 11 shows RFM15N15 waveforms using the conditions specified in the example.

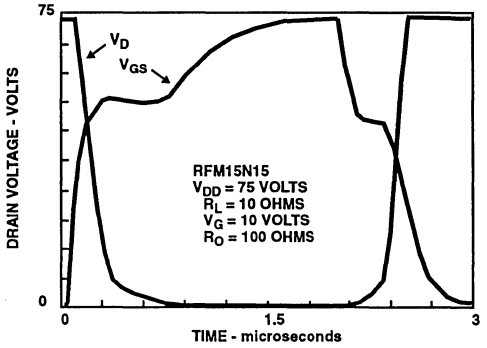


FIGURE 11. STEP GATE VOLTAGE INPUT TO AN RFM15N15

STATE	CALCULATED TIME	MEASURED TIME	RATIO
	(t_c, ns)	(t_m, ns)	(t_c/t_m)
1	61	60	1.02
2 + 3	671	670	0.92
4	125	137	0.91
5 + 6	318	375	0.85

For peak gate voltages other than 10 volts, and load resistances other than $V_{DSS}/I_{D(rms)}$, the equations of Table 1 may be used in conjunction with slope estimates from the characterization curves for C_x and $C_{GS} + C_x(1 + g_m/g_{mJ})$ at the appropriate drain-current level.

Characterization-Curve Limits

The switching-time range over which the characterization can be applied is very impressive. For gate currents of the order of microamperes, device dissipation is the limiting factor. For gate currents of the order of amperes, the device response will be slowed by gate propagation delay. This delay, of course, degrades the linear switching relationship to gate current. However, as Figure 12 graphically shows, the characterization is valid across five decades of gate current and switching time, allowing all but a very few switching applications to be described by the characterization curves of Figure 9.

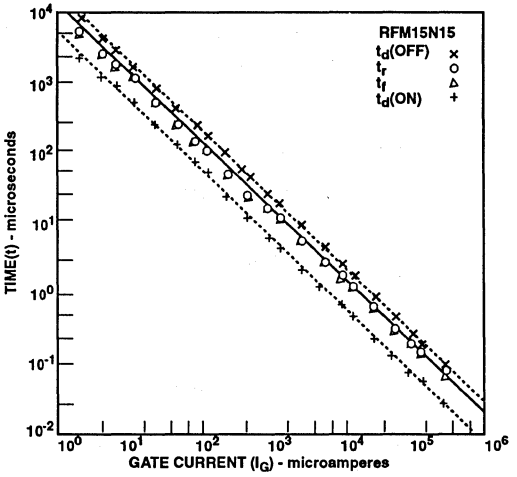


FIGURE 12. FIVE DECADES OF LINEAR RESPONSE

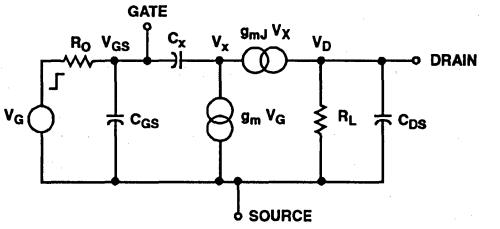
Conclusions

The viability of the proposed characterization curves using constant current has been demonstrated and the limits of application defined. The existence of a vertical JFET in a power MOSFET makes data-sheet capacitances of little use for estimating switching times. The classical method of defining switching time by 10% and 90% is a poor representation for power MOSFETs because of the dual- slope nature of the drain waveforms. Switching influences are masked because the 10% level is controlled by one mechanism and the 90% level by another. Device comparisons based on the classical switching definition can be very misleading.

Appendix A - Analysis For Resistive Step Voltage Inputs

Step Voltage Gate Drive

To obtain the necessary relationships, six device switching states must be examined using the same device equivalent circuit as was used for the constant-gate-current case, but with the forcing function replaced with a step voltage with internal resistance R_0, Figure A-1.



LEGEND

V_{GS}	- Gate Voltage	C_{DS}	- Drain Source Capacitance
V_X	- JFET Driving Voltage	g_m	- MOSFET Transconductance
V_D	- Drain Voltage	g_{mJ}	- JFET Transconductance
C_{GS}	- Gate Source Capacitance	R_L	- Drain Load Resistance
C_x	- MOSFET Feedback Capacitance	I_G	- Constant Current Amplitude

FIGURE A-1. POWER MOSFET EQUIVALENT CIRCUIT

State 1: Mos Off, JFet Off

As before, both current generators are open circuits, reducing the equivalent circuit to simply charging C_{iss} through R_0.

$$t = R_O C_{iss} \ln(1/(1 - V_T/V_G))]$$

$$t = V_G/R_O$$

State 2: Mos Active, JFet Active

Before proceeding, it is wise to examine an actual device response and make use of available simplifications. Figure A-2 shows $i_G(t)$ and $i_D(t)$ for a typical power MOSFET driven by a step gate voltage. For truly resistive switching, realize that these waveforms are only mirror images of their voltage counterparts $v_G(t)$ and $v_D(t)$. Using Figure A-2, applicable gate currents for each of the device states may be listed.

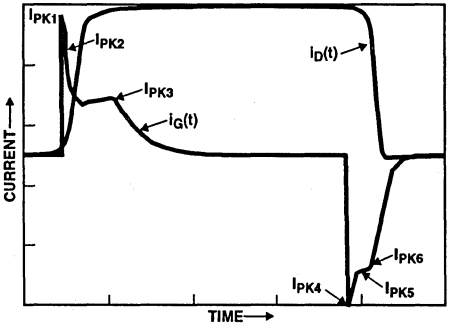


FIGURE A-2. $I_G(t)$ AND $i_D(t)$ FOR A TYPICAL POWER MOSFET DRIVEN BY A STEP GATE VOLTAGE

Turn-On

State 1: MOS Off, JFET Off

$I_{PK1} = V_G/R_O$

State 2: MOS Active, JFET Active

$I_{PK2} = (V_G - V_T)/R_O$

State 3: MOS Active, JFET Saturated

$I_{PK3} = (V_G - V_G(sat))/R_O$

Turn-Off

State 4: MOS Saturated, JFET Saturated

$I_{PK4} = V_G/R_O$

State 5: MOS Active, JFET Saturated

$I_{PK5} = V_G(sat)/R_O$

State 6: MOS Active, JFET Active

$I_{PK6} = V_G(sat)/R_O$

The equivalent circuit of Figure A-1 predicts that:

$$dv_D/dt = -g_m R_L(V_G - V_T)e^{-t/T1}/T1$$

where $T1 = R_O C_{GS} + (1 + g_m/g_{mJ})R_O C_x$

Note that $g_m R_L(V_G - V_T)$ is usually an order of magnitude greater than V_{DD}, indicating that the drain voltage is discharging toward a very large negative value. The device operation, then, is on the early, almost linear, portion of the exponential, where $e^{-t/T1}$ approximates unity. The drain current of Figure A-2, and hence the drain voltage, does indeed exhibit a linear decrease with time.

Thus, for state 2:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PK2}}$$

where $I_{PK2} = (V_G - V_T)/R_O$

State 3: Mos Active, JFet Saturated

Because of the Miller effect, the gate voltage and, hence, the gate current, is almost constant during the tail time. The equivalent circuit then predicts:

$$\frac{dV_D}{dt} = \frac{g_m R_L I_G}{C_{GS} + (1 + g_m R_L)C_x} = \frac{I_G}{C_x}$$

$$I_G = I_{PK3} = (V_G - V_G(sat))/R_O$$

and $$t = \frac{(V_{DK} - V_D[sat])C_x}{I_{PK3}}$$

State 4: Mos Saturated, JFet Saturated (Turn-off)

Both equivalent-circuit generators are short circuits, and the gate drive is discharging C_x in parallel with C_{GS} through R_O.

$$t = R_O(C_{GS} + C_x)\ \ln[V_G/V_G(sat)]$$

$$I_{PK4} = V_G/R_O$$

State 5: Mos Active, JFet Saturated

The JFET current generator $V_x g_{mJ}$, is operative.

$$t = \frac{[V_{DK} - V_D[sat])C_x}{I_{PK5}}$$

$I_{PK5} = V_G(sat)/R_O$

State 6: Mos Active, JFet Active

The Miller effect is now reduced by the activation of $V_G g_{mJ}$, and the equivalent circuit predicts:

$$t = \frac{[V_{DD} - V_{DK}][C_{GS} + C_x(1 + g_m/g_{mJ})]}{g_m R_L I_{PAK6}}$$

$I_{PAK6} = V_G(sat)/R_O$

Appendix B - Estimating R_O For Some Typical Gate-Drive Circuits

Case 1: Typical Pulse-Generator Drive, Figure B-1

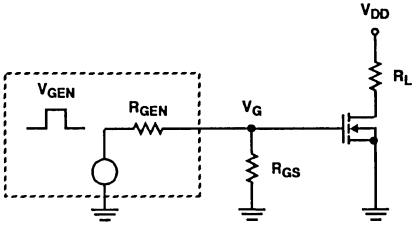


FIGURE B-1. TYPICAL PULSE-GENERATOR DRIVE CIRCUIT

Turn-On and Turn-Off

$$R_O = R_{GEN}R_{GS}/(R_{GEN} + R_{GS})$$

For the typical case where $R_{GEN} = 50\Omega$, and a coaxial-cable termination of 50 ohms, $R_O = 25\Omega$ and $V_G = V_{GEN}/2$.

Case 2: Voltage-Follower Gate Drive, Figure B-2

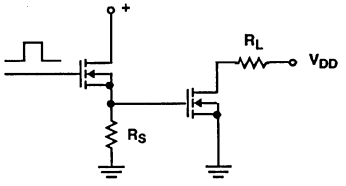


FIGURE B-2. VOLTAGE-FOLLOWER GATE-DRIVE CIRCUIT

Turn-On

R_O is approximately equal to $1/g_m$ for R_S very much greater than $1/g_m$.

gm = transconductance of driving MOSFET transistor.

Turn Off

$R_O = R_S$

Case 3: Common-Source Gate Drive, Figure B-3

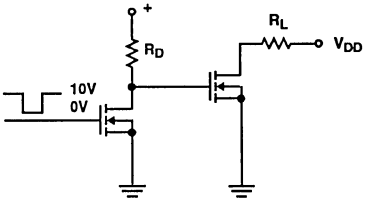


FIGURE B-3. COMMON-SOURCE GATE-DRIVE CIRCUIT

Turn-On

$R_O = R_D$ (drain-to-ground capacitance of driving device adds to C_{GS} of driven MOSFET.)

Turn Off

$R_O = R_{DS}(on)$ of driving MOSFET

R_D is very much greater than $R_{DS}(on)$

Harris Semiconductor

APPNOTE

No. 7326 May 1992

Harris Intelligent Power

APPLICATIONS OF THE CA3228E SPEED CONTROL SYSTEM

by W. Austin

The CA3228E Speed Control System[1] is a monolithic integrated circuit originally designed for automotive cruise control systems; its block diagram is shown in Figure 1. The completeness and self-contained nature of the circuit can be appreciated by examination of the typical automotive application shown in Figure 2. Both I^2L logic and linear circuit design are combined to provide the primary functions, feature enhancements and safety backup necessary for a high-performance cruise control system. But its fully facilitated feedback system makes the CA3228E useful in a wider range of applications. The information provided in this Note will aid the user in applying the circuit to applications such as electric motor speed controls, engine speed controls, and rate controls for manufacturing systems. In fact, any powered system may be controlled with the CA3228E's accelerate or coast to a set speed adjustment and resume speed after braking (or safety stop) adjustment. Special features of the CA3228E include a single command line control and controlled PLL acceleration.

Overview

As shown in the detailed block diagram of the CA3228E in Figure 1, the primary function of the circuit interface to the logic control section is to provide a complement of capability in both linear and logic design. The command decode circuit

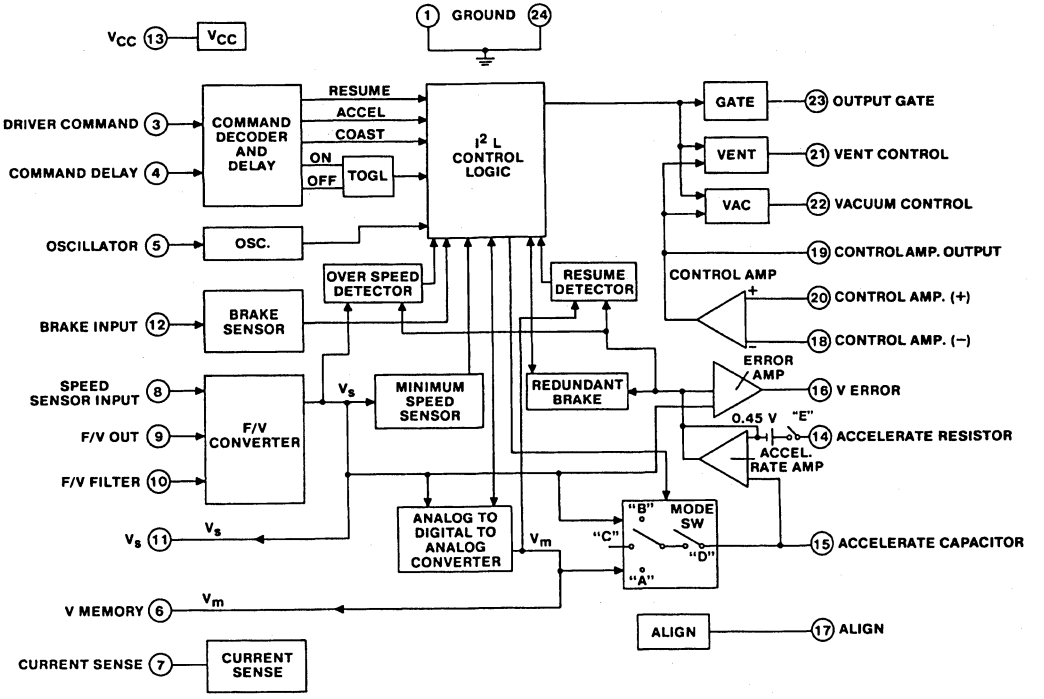


FIGURE 1. BLOCK DIAGRAM OF THE CA3228E SPEED CONTROL SYSTEM

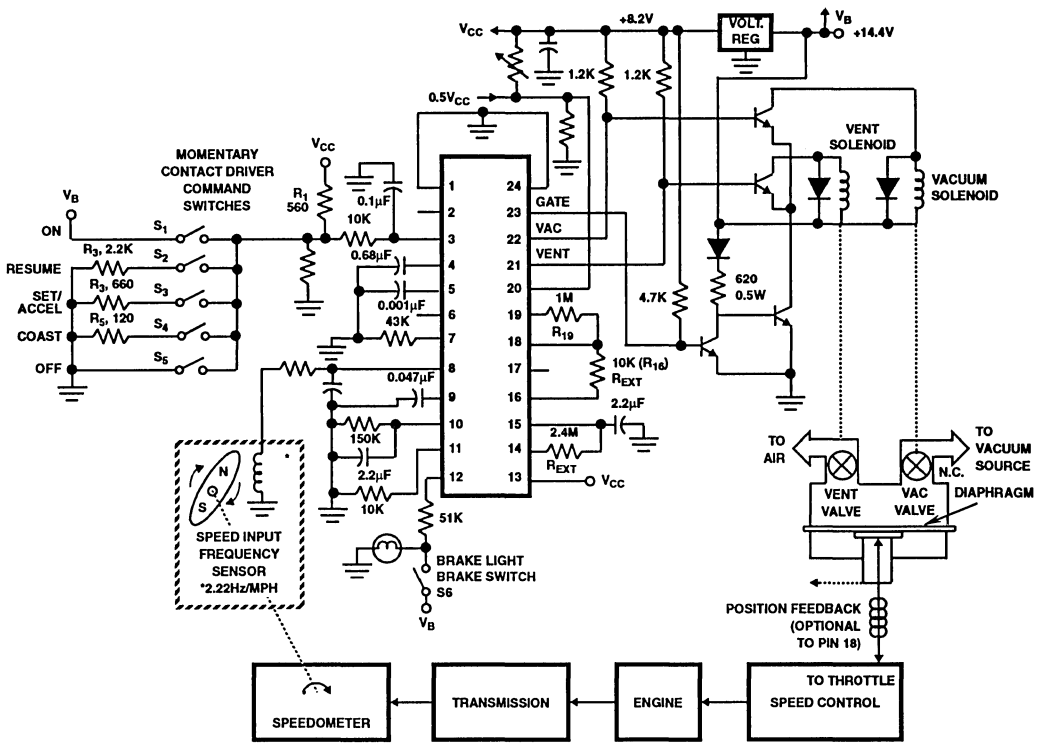


FIGURE 2. A TYPICAL APPLICATION OF THE CA3228E IN AN AUTOMOTIVE CRUISE CONTROL SYSTEM

determines which of five possible commands will be sent to the control logic. The frequency-to-voltage converter (F/V) accepts changing frequency signals and converts them to their linear representation in DC voltage.

An important feature of the circuit is a 9-bit A/D-D/A circuit, which stores a selected speed after the set/accel or coast command signal is sent to the command decoder. Within the constraints of speed-range and brake-sensing conditions, a mode switch activates an acceleration rate amplifier to maintain a cruise condition or to control a manual acceleration override condition. Any detected errors are amplified and routed to the control amplifier, which drives the output switching circuits;abuilt-indeadband eliminates overlap in the activation of the servo controls.

The A/D-D/A circuit consists of a 9-bit shift register which is clocked by an on-chip oscillator and current generators that sum the result of the stored bit information. The current is converted to voltage in a resistive load, and can be monitored at pin 6 as the V_M of the IC. The V_M output voltage is also sent to a memory update comparator where it is compared to the F/V output voltage, V_S. When a set/accel or coast command is finished and a return to idle is established (no switch contacts), the D/A clocks until $V_M = V_S$. The memory update comparator stops the clock when $V_M = V_S$, and the speed is stored in the bit register.

The broader prospects for use of the CA3228E are apparent if one considers all the electromechanical system possibilities that are adaptable. Some of these possibilities are:

- Automotive cruise control
- AC or DC motor speed control
- Master/slave engine or motor speed controls
- Manufacturing conveyor rate control (with safety/overload cutout)
- Oscillator frequency reset
- Wire/ribbon processing rate control
- Air or fluid rate movement control
- Air or fluid temperature control

The characterization of the F/V converter circuit given below shows the many features of the CA3228E that permit a flexible interface between it and a variety of sensor conditions. Because of the many combinations of user input/output conditions that may be used for control, it is important to note that a single control wire provides the input for the five major commands (nonmetallic chassis requires a ground wire). This feature provides a cost savings along with design flexibility.

Command and Control Functions

The speed control functions and their descriptions are listed in the following table. (An asterisk following a control function denotes momentary switch closure.)

CONTROL	FUNCTION
OFF*	Deactivates the device logic and erases memory. $V_3 \leq 0.094\ V_{CC}$
ON*	Activates device logic and initiates a standby mode, $V_3 \geq 1.1\ V_{CC}$ or +100μA followed by $V_3 = 0.95\ V_{CC}$ (open switches).
SET/ACCEL	Momentary switch closure sets the current speed in memory. Acceleration continues at a constant rate when the switch is held closed. $V_3 = 0.54\ V_{CC}$. V_S must be greater than 1.5 V, the minimum speed lockout (MSLT), discussed below, which is approximately 25mph in the system of Figure 2.
COAST	Momentary switch closure sets the current speed in memory. When the switch is held closed, the servo disengages, causing the vehicle to slow-down. When the switch is released, the new speed is stored. During switch contact, $V_3 = 0.21\ V_{CC}$.
RESUME*	Resumes a cruise condition if the speed is greater than MSLT, a speed has been stored after an on command, and the brake or redundant brake have not been activated. If the speed is greater than the stored memory speed, the coast function will continue until $V_S = V_M$. $V_3 = 0.76\ V_{CC}$.
Other control functions that directly affect the operating mode of command setting are:	
BRAKE	At approximately 0.55 V_{CC} or more, the brake input, V_{12}, will place the system in standby, but a stored memory speed will be retained. A resume command will return the vehicle to cruise and the previous speed condition.
CLUTCH DISABLE	Same input as brake (for manual transmission).
MSLT (Minimum Speed Lockout)	Minimum Speed Lockout is a low-speed inhibit. This is an internal function that samples the F/V converter output V_S. For V_S approximately equal to 0.183 V_{CC} or less, the set/accel, coast, and resume commands cannot be set. In the typical automotive application of Figure 2, MSLT is 25mph.
REDUNDANT BRAKE	If the error amplifier output voltage V_{16} drops below 0.42 V_{CC}, an internal comparator causes the system to go into the standby mode. This action assures that an excessive error in the servo loop will not cause an unsafe condition by providing an error speed dropout. In the application of Figure 2, the error speed is approximately 11mph.
COMMAND DELAY	To provide immunity to noise and short duration pulses, the set/accel, coast, and on and off switch input hold times are delay controlled to 50ms by a 0.68mF capacitor at pin 4. For each command, a current charge delay is used to counteract switch bounce and to enhance noise immunity. A delay of 330ms is used for the resume command.

In addition to the braking and command delay safety features, a gate enable output is available at pin 23. The output at this pin remains low during normal operation of the accel, coast and cruise modes; however, it goes high for the brake, redundant brake, and low speed lockout (MSLT) commands, and during the high speed dropout condition of the resume mode. The normal applied circuit use of this feature is shown in Figure 2, where a low on the gate output at pin 23 permits the vent and vacuum drivers for the solenoid actuators to conduct through a saturated transistor common to the emitter of each driver. Should either the vacuum or vent driver transistor fail, the gate transistor would act as a safety backup, since it would be cut off and thereby mandate a standby condition.

Command Decoder Input Circuit

The command decoder input circuit is shown in Figure 3. Driver commands and their ranges of control are shown in Figure 4. Initially, the logic must be activated to an on and active standby state. This is done by setting the input emitter of 038 at pin 3 to a higher voltage level than the V_{CC} supply line in the IC. The current should be safely limited by using a 10kΩ resistor in series with pin 3. A current of 100μA is more than sufficient to cause Q_{38} to conduct current to Q_{37}, the transistor switch that activates the on state condition. A bias divider at pin 3 (shown in Figure 2) of 560Ω and 10kΩ establishes the command idle position after each momentary switch closure is completed.

When switch contact is made and the pin 3 bias levels are properly set, four comparators select the resume, accel, coast and off driver commands. An internal resistive divider is used to bias one input of each comparator, while the other input is biased from pin 3. As shown for the off comparator, in which I_{20} and I_{21} interface to the I^2L logic, each of the comparators drives the I^2L logic through switching transistor gates. The logic section of the IC determines all further control requirements from the state of the four comparators.

The control switching time is affected by the command delay circuit associated with pin 4 (Figure 1) and the charging time of the 0.68mF capacitor at pin 4. The 0.68μF capacitor sets command delays of 50ms, except for the resume command which is 330μs. The delay time is determined from two states of constant current drive to pin 3. Longer or shorter times may be set by changing the value of the pin 4 capacitor, but the ratio of other command delays to resume will remain the same. To calculate the capacitor value needed to change the time delay to the one desired, use the following equation:

$$V = It/C \text{ or } C = It/V$$

where V is voltage, I is current, C is capacitance, and t is time. Since V and I remain fixed, equation matching yields:

$$C1/C2 = t1/t2$$

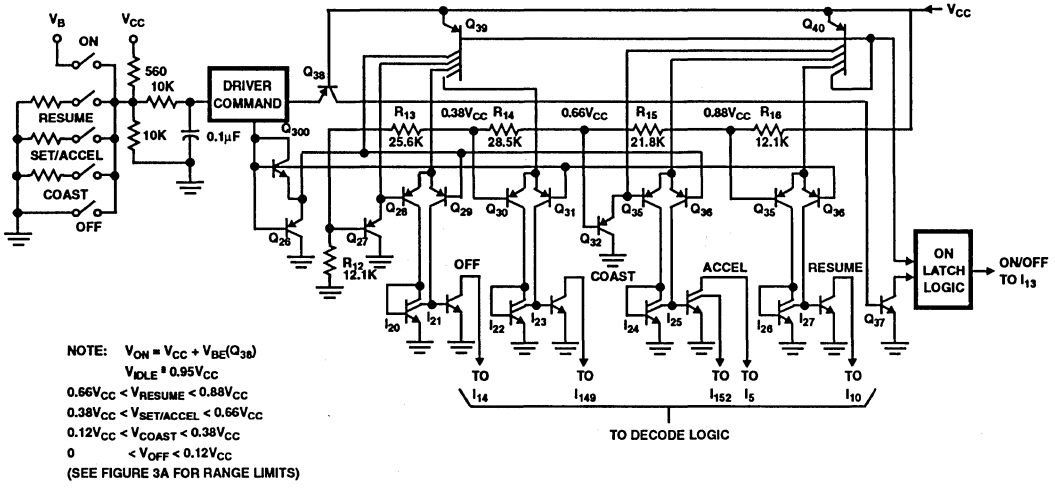


FIGURE 3. DRIVER COMMAND INPUT COMPARATOR CIRCUIT AND LOGIC OUTPUT TO COMMAND DECODE

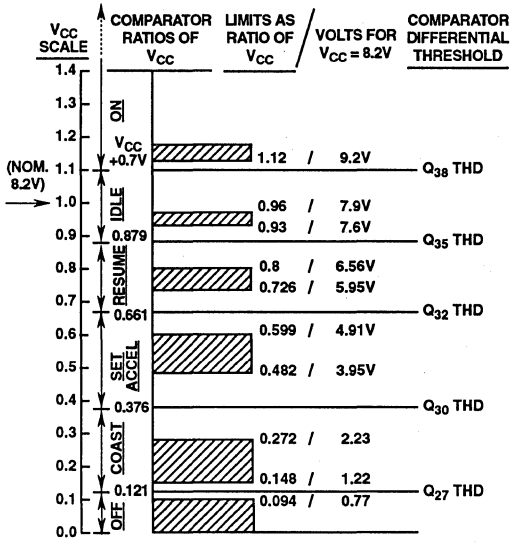


FIGURE 4. DRIVER COMMANDS AND THEIR RANGES OF CONTROL

Frequency-to-Voltage (F/V) Converter Operation

The schematic of Figure 5 shows the circuit of the F/V converter portion of the CA3228E. The input at pin 8 is normally the speed input from a speed sensor of the moving system. In normal use of the operating system, a frequency is applied at pin 8, which is a scale multiplier of the controlled system speed. For the circuit of Figure 2, the scale is 2.22Hz/mph and, with the components shown biasing the F/V converter, the conversion gain from pin 8 to pin 10 is typically 27mV/Hz. Under these conditions, the system performance parameters of the data sheet apply, including a normal speed-control range of 62 to 222Hz. In calibrating a normal range of F/V control for the V_S (pin 10) output, the frequency range in terms of voltage becomes 1.67 to 6V. Typical voltage range values of 1.5V minimum to 6.8V maximum are possible at the V_S output.

Figure 6 demonstrates the flexibility and range of design capability of the converter function by showing converter range possibilities for various values of C8 and C9; the capacitors are selected to accommodate a given range of input frequencies. The capacitor at pin 8 is chosen primarily as a filter to provide good noise immunity. Resistor R_8 and capacitor C8 provide both DC and AC overvoltage protection. The normal range of sensor input voltage is 3.5 V_{PP} minimum to 15 V_{PP} maximum.

As indicated by the capacitance versus frequency plot of Figure 6, the range of input frequencies may be changed; however, the minimum to maximum frequency ratio will always remain approximately the same. As an example, assume that it is desired to center the range of input frequencies at approximately 1000Hz. At this frequency, C9 should be approximately 0.005µF and C8 approximately 0.01µF. For these values, the minimum frequency at a V_S of 1.5V is 500Hz; the maximum frequency at a V_S of 6.8V is 2400Hz.

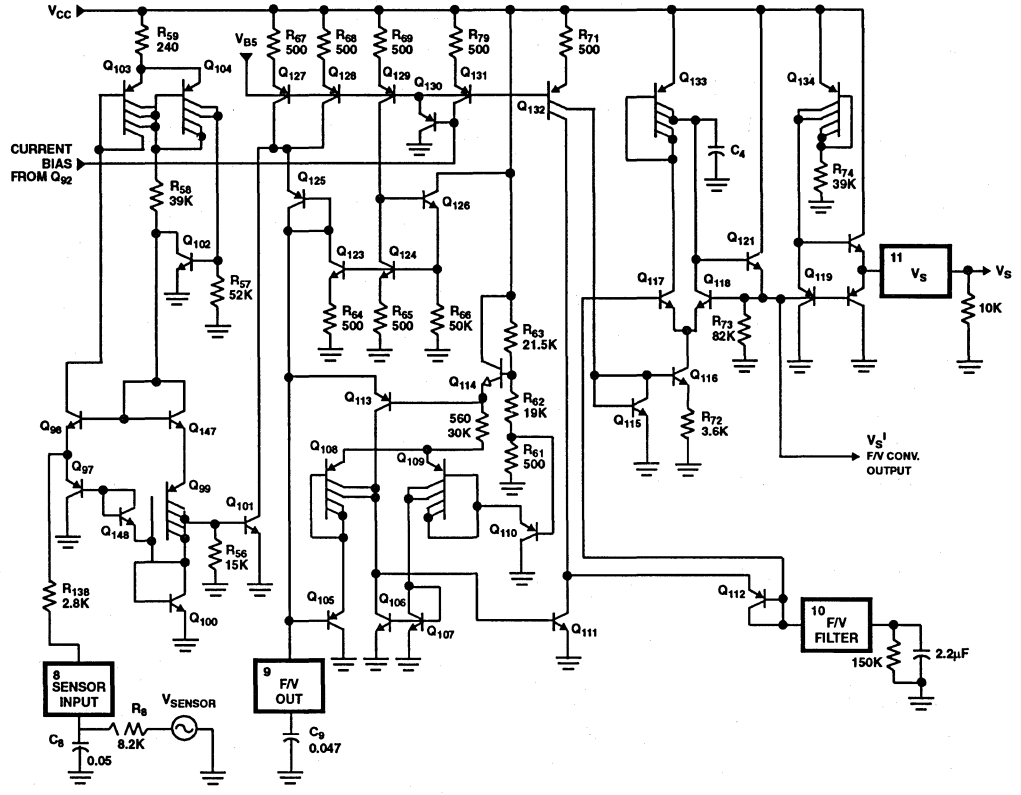


FIGURE 5. FREQUENCY TO VOLTAGE (F/V) CONVERTER CIRCUIT

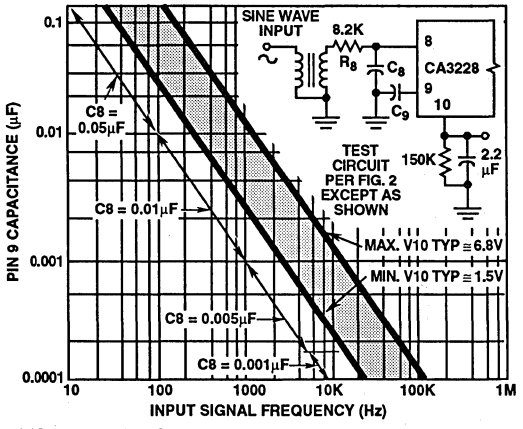


FIGURE 6. F/V CONVERTER RANGE EXTENSION WITH ADJUSTMENT OF C8 AND C9

It is possible to extend the frequency range of the F/V converter to frequencies as low as 10Hz and as high as 500kHz. However, the loop stability of the lower frequencies may be difficult to control. Higher values become very dependent on stray capacitance, causing some loss of output linearity where the internal circuit becomes bandwidth limited.

Input signal requirements at pin 8 are characterized by the voltage versus current characteristic of Figure 7. While the VI curve may appear to be complex, the drive requirement is explained simply by noting that the pin 8 input shown in Figure 5 is made through a 2.8kΩ resistor to the emitters of an n-p-n and a p-n-p transistor. When the signal input voltage polarity goes negative, Q_{98} conducts and changes the state of a latched current mirror (Q_{102}, Q_{103}, and Q_{104}). The changing mode of the current source reflects back to the base of the input n-p-n transistor Q_{98}, changing the DC level at pin 8. This change of state occurs when pin 8 is slightly negative (approximately 1 V_{BE}). The abrupt change to a positive voltage of approximately 2 V_{BE} is normal.

The requirements of this change of state have some influence on the design of the source input drive to pin 8. For the F/V converter input stage to switch properly, a current source drive such as an inductive pickup device ora transformer coupled signal source is preferred. In any case, it is important to note that the signal should swing negative to fully activate the change of state. It is also preferred that the input signal be nearly centered with respect to the voltage zero

crossing. The external series 8.2kΩ resistor at pin 8 must be used to limit peak currents, particularly when inductive pickup sensors are used. Inductively coupled circuits may produce transient pulses if any intermittent condition exists.

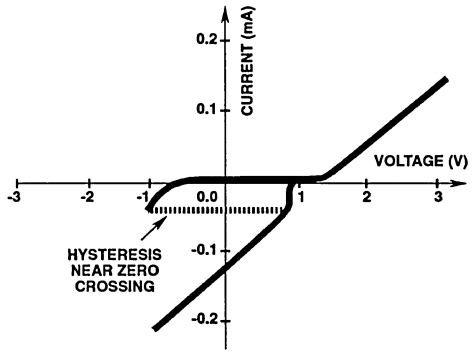


FIGURE 7. F/V CONVERTER INPUT CHARACTERISTIC PIN 8 VOLTAGE vs. CURRENT

As shown in the functional diagram of Figure 8, the second stage of the F/V converter is a pair of current generators that are used to produce both positive and negative ramp slopes when driven by the square-wave signal from the output of the first stage (at the collector of Q_{101}). The capacitor at pin 9 is charged and discharged by the fixed current sources which develop a truncated ramp signal of approximately 4 V_{PP}, Figure 9. The ramping signal is applied to a window comparator with reference points of 0.482 V_{CC} at the emitter of Q_{113} and 0.012V_{CC} at the base of Q_{105} (see Figure 5). When the ramp is in the transition range between these voltage levels, a high output pulse (from an equivalent 2 input NAND gate) drives the base of Q_{111}. The comparator levels are determined from a resistor divider: R_{61}, R_{62}, and R_{63}. The peak signal level is approximately 4V, while the minimum signal swing is nearly at ground level. The pulse width provided at the collector of Q_{111} is a function of the ramp transition time.

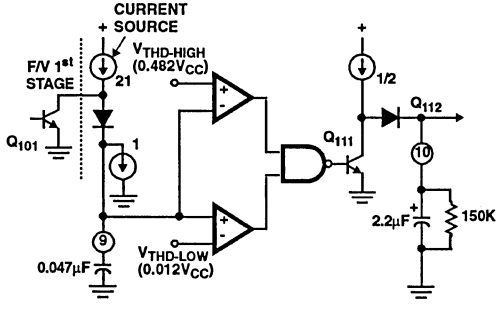


FIGURE 8. F/V CONVERTER COMPARATOR STAGE

Since a pulse of fixed width is generated on each positive and negative transition of the input signal at pin 8, it remains to integrate the pulses to produce a DC voltage proportional to the input frequency. The integration is accomplished in the RC filter circuit of pin 10. Diode Q_{112} rectifies the current-driven pulses developed at the collector of Q_{111}.

Another important characteristic of the F/V converter is the absence of pulses from Q_{111} when no signal is present at pin 8. Diode Q_{112} remains reversed biased by any positive DC voltage applied to pin 10. Therefore, it is also possible to use a DC voltage signal input at pin 10 to directly control the servo feedback system. In many PLL control systems, a DC voltage signal is easily generated from position indicators. In the CA3228E, this capability provides the user with an alternative to some of the restrictions that apply to the use of the F/V converter, restrictions that may require frequency dividing to accommodate the desired frequency range and bandwidth limitations on the chip.

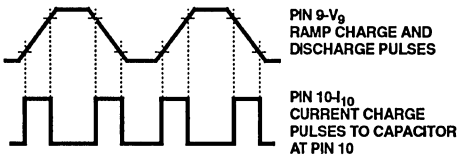


FIGURE 9. PIN 9 F/V OUTPUT AND F/V FILTER SIGNAL AT PIN 10

The range of the applied signal at pin 10 should be approximately 2V to 6V. The input impedance at pin 10 is quite high due to the source follower stage that follows the pin 10 input and drives Pin 11 plus the V_S' output to the A/D converter and mode switch circuits. Pin 11 is a sample test point for the F/V converter output, V_S. The V_S, signal is separately buffered and output to the A/D converter and mode switch circuits.

To provide a stable temperature characteristic for the F/V converter voltage, external control of the current-source generator has been provided. In the CA3228E, pin 7, Figure 10, represents a temperature-stable external sensitivity control point for the F/V converter output voltage V_S. The 43kΩ temperature-stable metal-film resistor used to bias pin 7 drives the F/V converter current sources. The current drive generated in the emitter of Q_{92} by this resistor provides a mirror-current bias to the F/V converter current-ramp circuits.

A/D Converter and Memory Update Comparator

The signal V_S', derived from the F/V converter output, Figure 5, and the D/A converter signal, V_M, are internally fed to the memory-update comparator circuit of Figure 11. The V_M signal may be monitored at pin 6. As noted in Figure 5, the V_S' signal is also fed to pin 11 through a buffer amplifier. The signal at pin 11 is the F/V converter output, V_S, and has a close tracking relation to V_S, when pin 11 is biased with a 10kΩ resistor to ground. In Figure 11, the V_M and V_S' signals drive buffer amplifiers Q_{276} and Q_{277}, respectively. From Q_{274} and Q_{271} the V_S' signal is sent to the error amplifier, overspeed detector and mode switch. The V_M signal is sent to the mode switch via Q_{275} and Q_{269}. The V_S' mode switch input (Figure 13) is at Q_{231} and the V_M input is at Q_{232}. Transistors Q_{269} and Q_{271} also drive Q_{268} and Q_{270}, the memory update comparator input transistors.

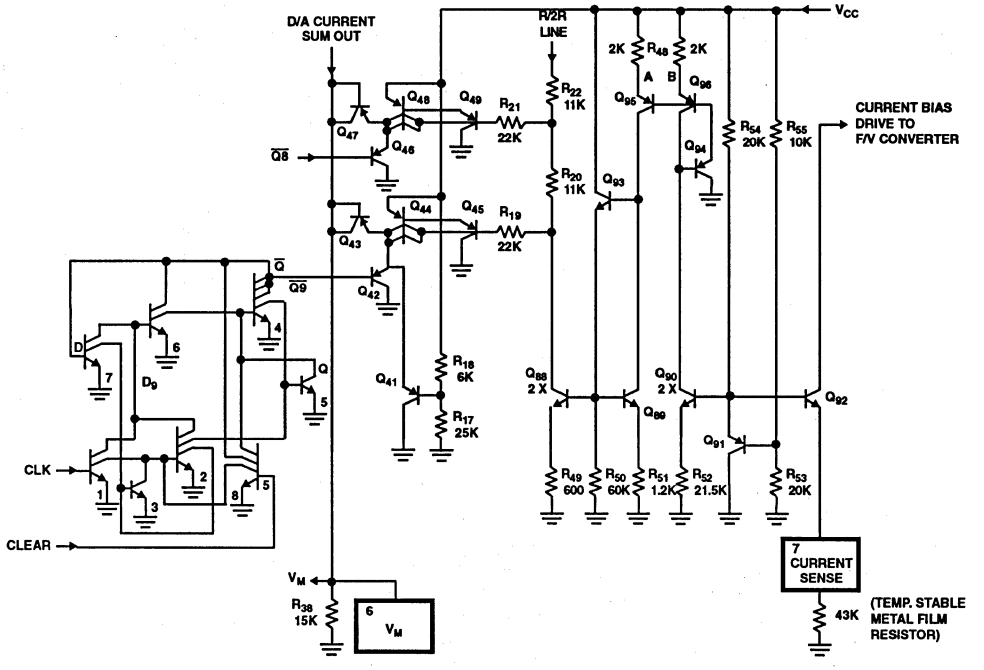


FIGURE 10. 1 OF 9 RIPPLE COUNTERS AND 2 OF 9 D/A CURRENT SUM OUTPUT CIRCUITS SHOWN WITH THE R/2R CURRENT SINK BIAS AND F/V CONVERTER CURRENT BIAS CIRCUIT

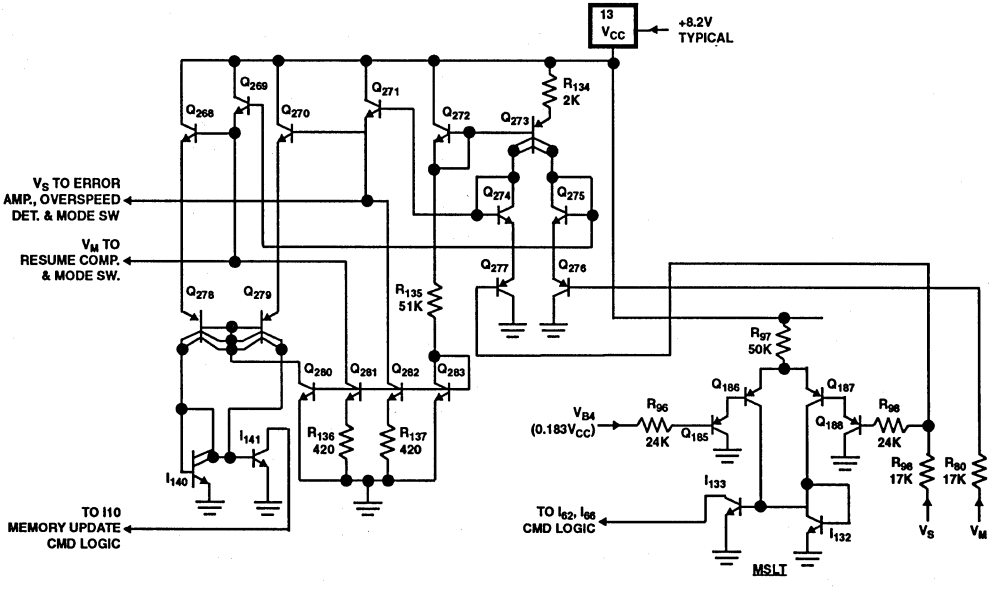


FIGURE 11. V_S' AND V_M BUFFERS WITH MEMORY UPDATE COMPARATOR AND MINIMUM SPEED LOCKOUT COMPARATOR (MSLT)

The block diagram of Figure 12 provides a broader perspective on the total operation of the D/A converter and stored memory operation by showing the signal flow by function. In Figure 12, the voltage developed by the F/V converter is V_S at the pin 11 monitor output, and is labeled as V_S, at the internal input to the memory update comparator. When, at a chosen speed, the accel/set or coast switch is depressed and then released, the command logic clears the register and initiates clocking in the ripple counter. Clocking continues and successively increases the D/A converter current output in increasing stair step increments until the V_M voltage resulting from the product of the current and the R_{38} resistor value is equal to V_S'.

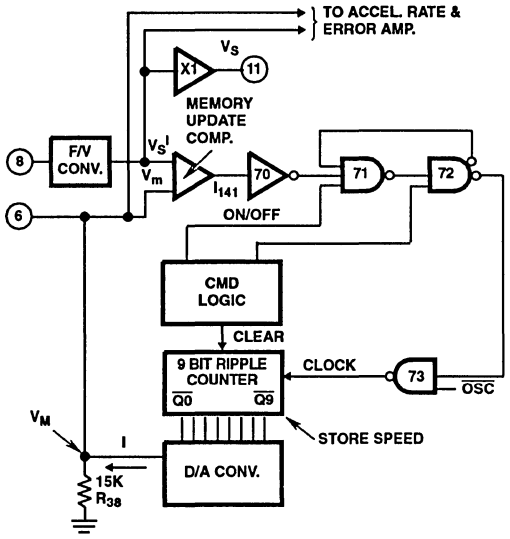


FIGURE 12. MEMORY UPDATE COMPARATOR WITH MEMORY AND D/A CIRCUITS

When $V_M = V_S'$, the memory update comparator changes state and sends a signal through output I_{141} to the logic circuit to stop the clocking of the 9-bit ripple counter. The stored bits in the ripple counter continue to bias the D/A converter to produce the memory set V_M speed reference. Anyfurther changes in V_S, are compared to the V_M output of the D/A converter, which then provides the error signal for the servo control. (Refer to the Command and Control Functions section of this Note, above, for complete details of the command inputs that affect the stored speed setting.)

The circuit of Figure 10 shows a portion of the 9-bit ripple counter and the D/A circuit driven by the counter. Each cell of the 9-bit counter has a $\overline{Qx}$ output that drives its respective 2* divided current source. When the counter is active, the summed outputs of the D/A converter driven current generators are present on the V_M line and at pin 6.

Mode Switch and Acceleration Control

The mode switch of Figure 13 is that portion of the CA3228E whose inputs for V_S' and V_M are Q_{231} and Q_{232}, and whose output is through pin 15. Logic commands control the mode switch by controlling Q_{248}, switch A; Q_{237}, switch B; and Q_{250}, switch D. When switch A is activated, Q_{248} is off, which allows Q_{232}, Q_{240}, Q_{241}, and Q_{245} to conduct the V_M signal to pin 15 and the base of Q_{251}. Similarly, V_S' is conducted to pin 15 via Q_{231}, Q_{233}, Q_{234} and Q_{244} when switch B (Q_{237} off) is activated.

In the accel mode, switch D is open, allowing the acceleration-rate amplifier to dictate a controlled rate of acceleration. A switch D open corresponds to an active high signal from I_{100}, which causes Q_{250} to conduct, and which, in turn, causes Q_{243} to conduct. The Q_{243} output to Q_{242} is then at an emitter-base saturation level and Q_{242} is cut off, which prevents Q_{244} and Q_{245} from conducting V_S, or V_M to pin 15 and Q_{251}.

Switch D is also open during resume ramp conditions. Note that V_S, and V_M are in tracking modes when Q_{250} is open and Q_{242} is conducting. The V_M tracking mode is the closed-loop cruise mode. The V_S, tracking mode applies to conditions other than cruise, accelerate, and resume. In the V_S' or V_M tracking modes, Q_{235} or Q_{246} supplies current to the base of Q_{242}. The Q_{242} collector output supplies the current that charges the capacitor at pin 15.

The acceleration-rate amplifier controls a fixed rate of acceleration by providing an internal charging voltage and an external RC time constant at pins 14 and 15. When the acceleration circuit is active, Q_{135} is off and current source 0261 conducts current through Q_{266}. Current-mirror circuits also control current through R_{132} and produce a fixed voltage offset in the signal path from pin 14 through Q_{266}, R_{132}, and Q_{263}. In the active accelerate mode, an offset voltage is present at the bases of Q_{251} (pin 15) and Q_{257}. The offset signal that is present at the base of Q_{257} is also the output of the acceleration rate unity gain source follower amplifier. The voltage generated across resistor R_{132} is approximately 0.45V, and is the charging voltage for the external resistor and capacitor. The typical values of the external R and C are 2.4mΩ and 2.2mF. Since the acceleration voltage that charges the external circuit is constant, linear approximations to the rate of change may be used. Using the equation:

$$V = It/C$$

$$V/t = I/C \equiv 0.45/RC$$

Since V in the equations represents a fixed velocity-error voltage, V/t = 0.45/RC represents a fixed rate of acceleration. It is therefore possible to change the acceleration rate by adjusting the RC values. The desired rate of acceleration is based on system factors associated with the servo feedback loop. The values shown in this Note are for a typical automotive application. Since very low currents are used, the capacitor must also have a low leakage. For the conditions shown in Figure 2, charging current is 0.188μA.

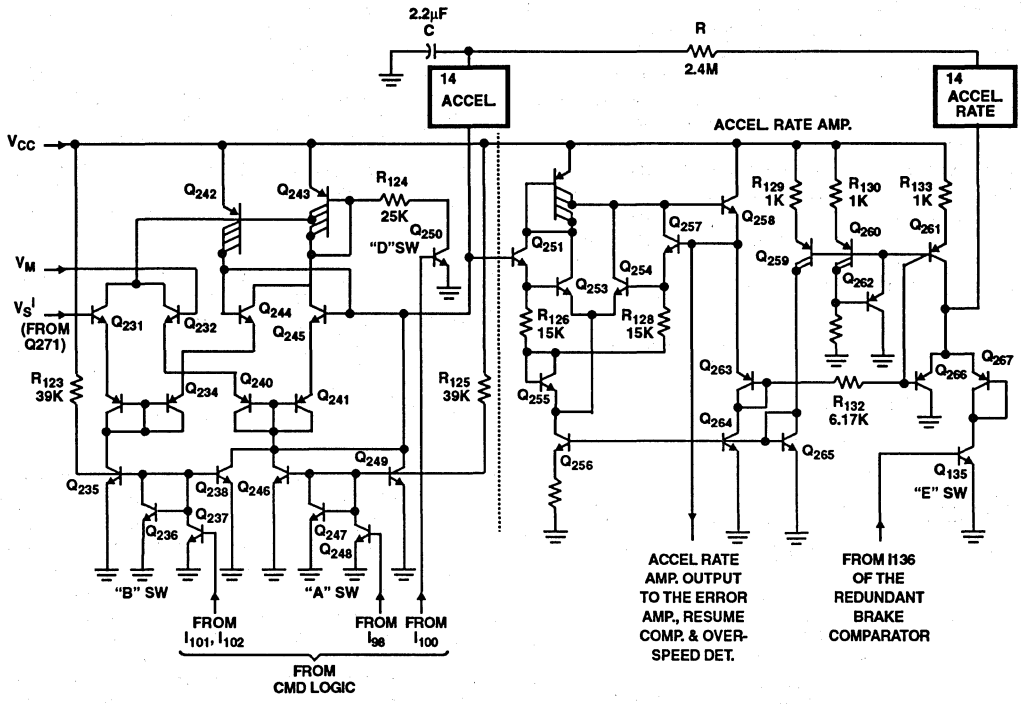


FIGURE 13. MODE SWITCH AND ACCELERATION-RATE AMPLIFIER CIRCUIT

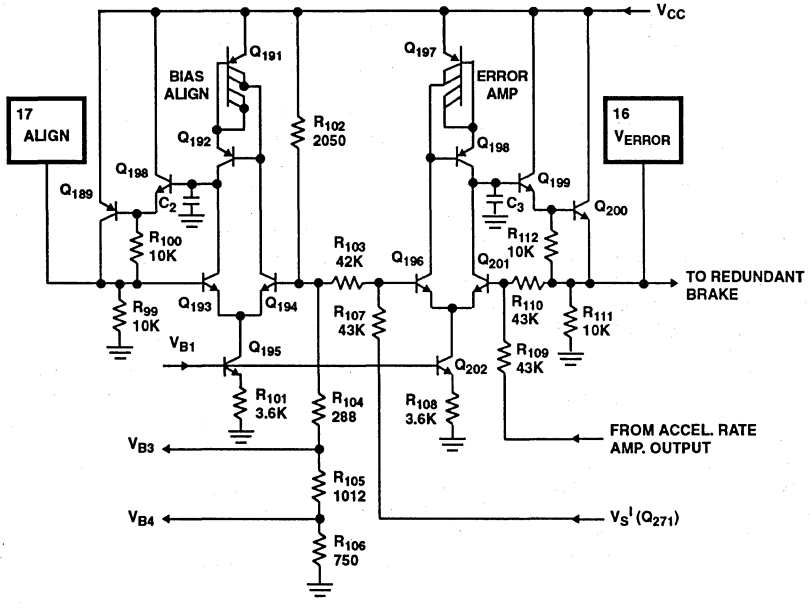


FIGURE 14. ERROR AMPLIFIER SHOWN WITH BIAS "ALIGN" SETUP CIRCUIT

Error Amplifier

The output signal of the acceleration rate amplifier is fed to the error amplifier, the overspeed detector, and the resume comparator. Under normal cruise conditions, the error amplifier continues to correct speed errors when V_S' deviates from V_M.

The error amplifier, Figure 14, is a part of the signal flow path of the feedback loop. The amplifier has an internal differential input and an output at pin 16. When the system is in a V_S' tracking mode, V_S' is present at both inputs. When the system is in a V_M tracking mode, the error signal is present at pin 16. The output signal of the error amplifier is externally coupled to the control amplifier at pin 18. Internally, the error amplifier output is fed to the redundant brake comparator. The error amplifier serves the error summing function of the servo loop and, as such, is a unity gain source follower.

The bias "align" function circuit is shown with the error amplifier circuit in Figure 14. The output at pin 17 is 0.5 V_{CC} and may be used for bias and setup. Current drain at pin 17 should not exceed 1mA.

Control Amplifier

The control amplifier shown in Figure 15 receives the signal from the error amplifier output at pin 16. Pin 18 is the negative input with respect to the control-amplifier output at pin 19, and pin 20 is the positive input with respect to the same output. The control amplifier may be regarded as a normal op amp whose gain is controlled with external feedback. However, the output signal is also internally coupled to the output vent, vacuum, and gate driver circuits. The open-loop gain, A_{OL}, of the control amplifier is typically 800. Figure 16 shows the control-amplifier bias configuration with pin 20 connected to an external divider at approximately 0.5V_{CC} and a variable feedback to pin 18. In the normal input circuit for pin 18, as noted in Figure 2, R_{16} and R_{19} are typically 10kΩ and 1MΩ, respectively.

Because the vent and vacuum driver amplifiers have a gain dependent controlled deadband, the feedback versus gain characteristic of the control amplifier is as shown in the curve of Figure 16. The curve follows the classic feedback gain equation and is approximately equal to R_{19}/R_{16} for ratios less than 50. However, the approximation is less accurate for ratios in the 100 range where the error is 15%. The feedback versus gain characteristic of the application circuit of Figure 2 is typically centered at a ratio of 100. Figure 17 shows the deadband of the output vent and vacuum amplifiers as a function of the R_{19}/R_{16} ratio; the output drive circuits are discussed in further detail in the following.

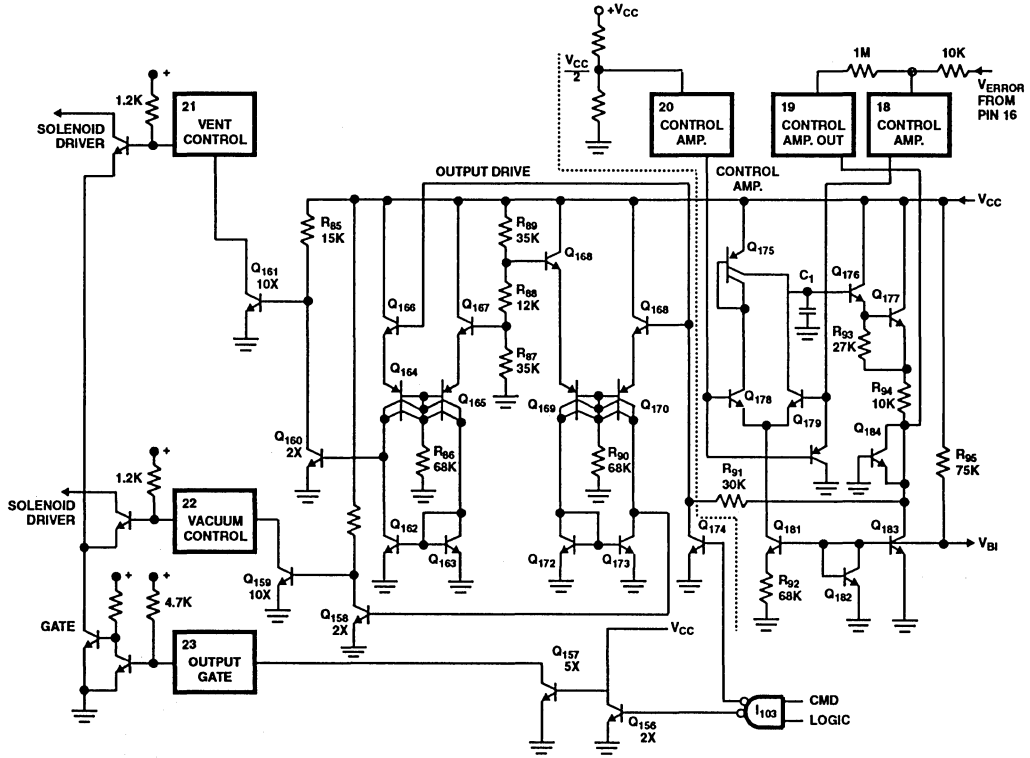


FIGURE 15. CONTROL AMPLIFIER AND OUTPUT DRIVERS

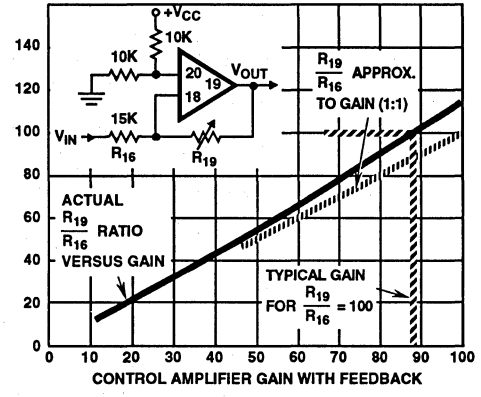


FIGURE 16. CA3228E FEEDBACK RATIO VERSUS CONTROL AMPLIFIER GAIN (WITH FEEDBACK)

Output Drive Circuits

The nomenclature of the output-drive circuits has been chosen to represent a normal vacuum-controlled actuator. Vacuum control of the actuator is intended to provide acceleration while vent control provides a relaxation or coast function. The output-drive circuits consist of amplifier drivers for the vent, vac (vacuum), and gate-output terminals at pins 21,22, and 23, respectively, as shown in Figure 15.

A single input from the control amplifier controls the vacuum and vent outputs. The signal is passed through R_{91}, a 30kΩ resistor, and the base of Q_{171} to a differential amplifier that controls the vacuum output. The base of Q_{171} is also common to the base of Q_{166}, which is thedifferential-amplifierinputthat controls the vent output. The differential amplifiers for the vacuum and vent functions have reference inputs tied to a resistor divider composed of R_{87}, R_{88}, and R_{89}.

The tap ratio for the Q_{168} input (comparator reference for the vacuum output) is at 57%. The tap ratio for the Q_{167} input (comparator reference for the vent output) is at 43%. When the control amplifier input is less than 0.43 V_{CC}, both vacuum and vent drivers are switched low or remain in a saturated on state. They remain on as long as the divider tap voltages are higher than the control amplifier input voltage. This situation defines a relaxed servo or coast mode.

When the control amplifier input voltage exceeds the 0.43 V_{CC} tap level, the Q_{166} differential input voltage forces the base of Q_{160} and the collector of Q_{161} at the vent out put to switch high. While the vent output is high and the vacuum output low, the system is in the deadband, which is the normal cruise mode. However, as the control-amplifier input voltage is further increased to the 0.57 V_{CC} tap level, both the vent and the vacuum outputs are switched high. The vacuum output switches to the high state when the base input of 0171 exceeds the 57% tap reference for 0168 and causes 0159 to switch off. When both the vent and vacuum outputs are high, the system is in a state of acceleration. As noted on Figure 2, the state of each mode is dependent on the external normally open (N.C.) and normally closed (N.C.) solenoid polarities.

The above action assumes that the gate output is low, permitting the external drive circuits of Figure 2 to function normally. The gate output remains low for acceleration, cruise, and coast functions. For brake, redundant brake, overspeed and minimum speed conditions, the gate output is high, which prevents acceleration and forces the system into a noncontrolling state. The gate output is forced high, and the vacuum and vent outputs low, by an internal logic switch, I_{103}, that disables the output drivers.

The deadband of the output drive circuit is fixed by resistor ratio, but can be controlled through the gain of the control amplifier. It should be noted that measurement of the deadband or tap ratio points requires forcing of the drive voltage to the control amplifier and measuring of the voltage at pin 19 when the vacuum and vent outputs change state. The circuit of Figure 2 was used to generate the curve in Figure 17, which shows the variation of the deadband range when the gain of the control amplifier is changed by changing external feedback. The deadband range is shown in Figure 17 in a mV spread as a V_S reading at pin 11. As the control amplifier gain is made to approach unity, the deadband approaches the actual tap voltage separation of 1.19V when V_{CC} equals 8.2V.

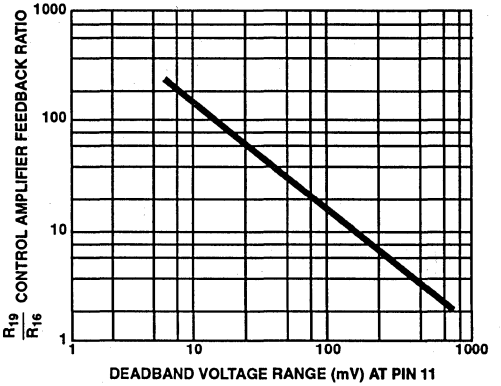


FIGURE 17. DEADBAND VOLTAGE RANGE IN OUTPUT CIRCUIT AS A FUNCTION OF CONTROL AMPLIFIER FEEDBACK RATIO (GAIN ADJUSTMENT) REFERENCED TO VS AT PIN 11

Redundant Brake

When the speed-control system is in the cruise mode, the redundant brake comparator (shown in Figure 18) may become active if significant error voltage develops at the output of the error amplifier. Specifically, if loading or braking is causing the speed of the system to be reduced, the redundant brake comparator senses that the speed is falling off. When the error developed reaches a difference speed of 11mph, the redundant brake comparator switches logic gate I_{136}, which causes the system to go to the standby mode. More generally, when the voltage at pin 16 drops below 42% of the V_{CC} supply voltage, I_{136} switches state. There is an additional output from the redundant brake through I_{135}; this output remains high during cruise and acceleration modes. I_{136} inhibits the acceleration rate amplifier by controlling the E switch. (Also see Figure 11.)

The conditions that determine the operation of the brake and redundant brake can be determined from the acceleration and sensitivity factors discussed above. The sensitivity of the F/V converter is approximately 27mV/Hz. For the system of Figure 2, the system magnetic speed sensor ratio is 2.22Hz/mph. Multiplication of these factors yields a ratio of 59.94mV/mph. Dividing this ratio into the 450mV offset designed into the acceleration rate amplifier provides a result of 7.5mph. Comparison of this result to the 11mph error allowed before the redundant brake becomes effective indicates that there is a wide enough safety margin to prevent redundant braking during acceleration.

A special feature of the CA3228E prevents extraneous noise from switching the redundant brake output and causing the system to go into standby. This feature is provided by a 4-bit shift register that is used as a digital filter to clock all four outputs of the shift register to 1's before a 4-input AND gate can switch the logic to standby.

Brake Input Comparator

The brake input comparator, also shown in Figure 18, is a comparator amplifier driving an inverter logic gate (1142). When the brake input is greater than 0.55 V_{CC}, as determined by the resistor divider composed of R_{77} of 20kΩ and R_{75} of 24.5kΩ, the I_{142} gate output changes state. The' brake input is normally connected through a current limiting resistor to the brake switch, and is in parallel with the brake light. The change of state at the output of the brake input comparator drives the command decoder which places the system in standby.

Minimum Speed Lockout

The minimum speed lockout (MSLT) comparator shown in Figure 11 senses the speed voltage V_S, and compares it to the output of a fixed resistor divider. When V_S' drops to less than 1.5V, the comparatorswitches, which sends a signal to the control logic that places the system in standby. If V_S' is initially less than 1.5V, the system cannot be set in the cruise mode. Thedivider ratio of 0.183V_{CC} is approximately 1.5 V for a normal V_{CC} of 8.2V. For a speed sensitivity factor of 59.94mV/mph, 1.5V is equivalent to 25mph.

Overspeed Detector and Resume Comparator

The associated functions of over speed detector and resume comparator are shown in Figure 19. From the normal condition, where a speed is set in memory and cruise is being maintained, it may be desired to increase speed and then return to the cruise mode. If the range of speed increase is large, it is best not to use the accel mode but to manually accelerate to the higher speed and then press the set/accel switch. An over speed detector comparator compares V_S' and V_M and controls the logic to assure a smooth transition.

During acceleration, V_S' is greater than V_M. When the set/accel command is given, the logic turns on 0250 (Figure 13) and the capacitor at pin 15 is rapidly charged. When the voltage at pin 15 is within 60mV of V_S', the over speed detector output is switched low. At that point, further V_S' correction is assumed by the acceleration-rate amplifier under fixed-rate conditions. The overspeed detector maintains the 60mV off-

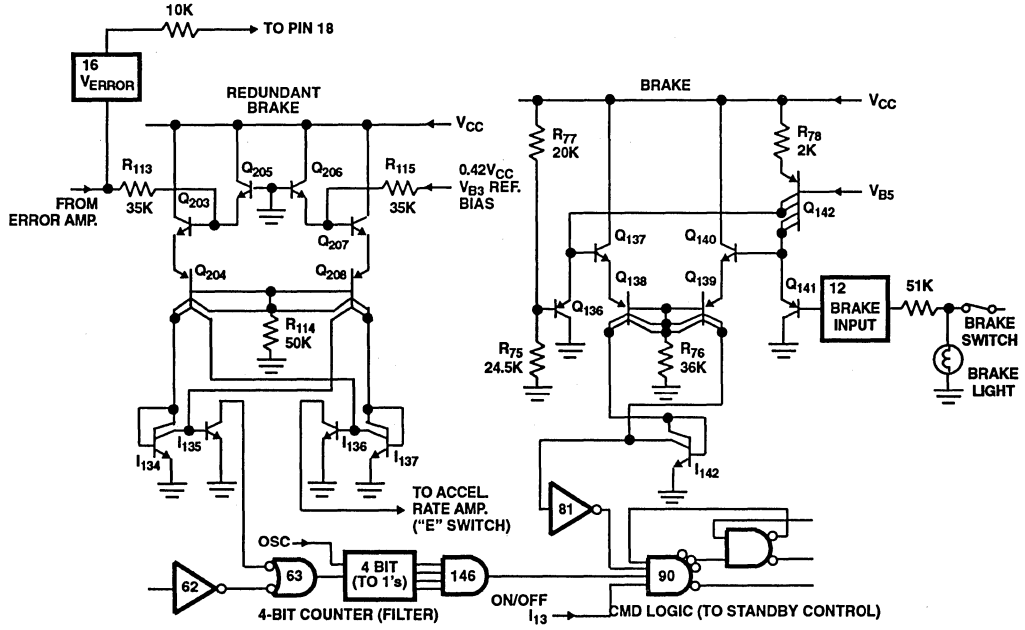


FIGURE 18. BRAKE AND REDUNDANT BRAKE

set along with a sufficient amount of hysteresis to assure noise immunity. When cruise conditions have been disrupted by braking action, and it is desired to return to cruise, the driver presses the switch for resume. The resume comparator samples V_S' and V_M and determines the fixed acceleration required for return to the speed previously stored in memory. An internal filter is used at the output of the comparator to prevent noise from resetting the comparator before V_S' reaches V_M.

Oscillator (Clock) Circuit

The circuit of Figure 20 shows the RC oscillator circuit used for internal clocking of the 9-bit ripple counter and the 4-bit counter that serves as a digital filter for the redundant brake. Various other elements of the command logic require oscillator control for the toggling of flip-flops. The oscillator frequency is an independent internal function on the chip, and has no relation to the frequency of the F/V converter input. A single capacitor at pin 5 determines the oscillator frequency. However, the fixed current source noted as V_{B5} also has an effect. The V_{B5} current source is derived from the same bias line that controls the F/V converter current sense drive from a 43kΩ resistor at pin 7. While the oscillator frequency may be changed by adjusting the resistor at pin 7, this adjustment will also change the F/V converter sensitivity. Since the voltage bias at pin 7 is approximately 5.5V, Q_{130} and Q_{131} are driven by 128mA through Q_{92} in the F/V converter (see Figure 5). The base bias line for Q_{131} is V_{B5}, and is mirror connected to Q_{84} and Q_{85} in the oscillator. A charge current of 128mA goes to the 0.001mF capacitor at pin 5 from p-n-p transistor Q_{85}. A 4x current mirror n-p-n transistor, Q_{86}, discharges current at 512mA from the capacitor at pin 5. The resistor divider at the base of Q_{81} switches between 4.1V and 6.1V as I_{144} and Q_{85} are toggled on and off in the return feedback loop. With a charge current of 128mA and a discharge current of 512mA and using the equation:

$$t = VC/I$$

the clocking time, t, (and hence oscillator frequency) can be calculated using the 2V change for V, a 0.001mF capacitor value for C, and the charge and discharge currents for I. The result is 15.6 plus 3.9µs or a frequency of approximately 51kHz.

Operation and Performance

Table 1 defines the voltage values for the pins of the CA3228E IC. The annotations cover pins where conditions may be expected to vary. For further detail on the functions of the V_M and V_S voltages at pins 6 and 11, respectively, refer to the CA3228E data sheet.[1]

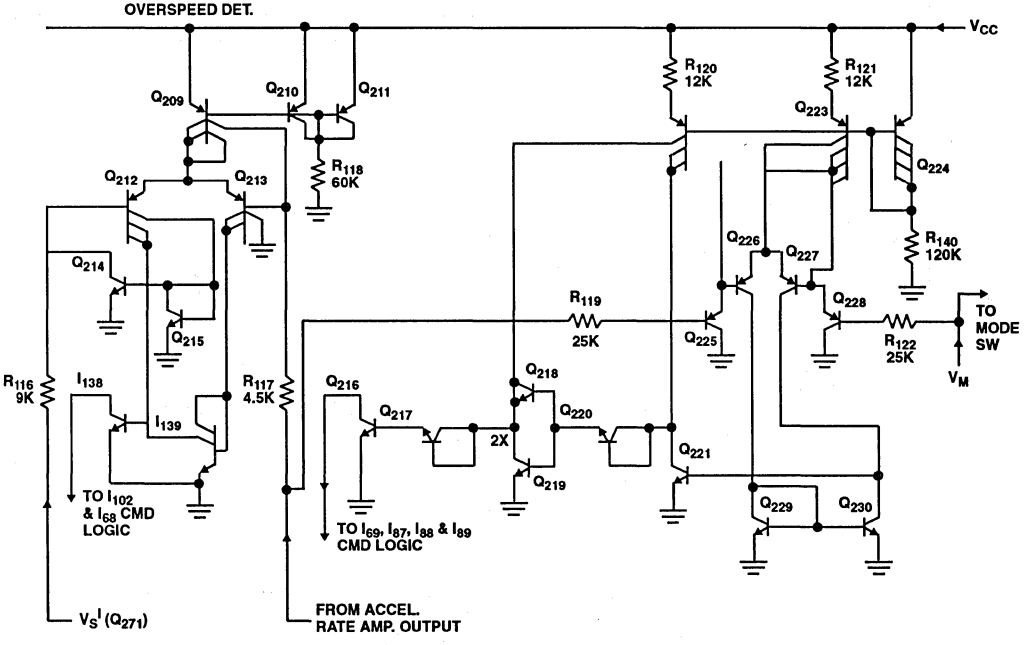


FIGURE 19. OVERSPEED DETECTOR AND RESUME COMPARATOR

TABLE 1. NORMAL CRUISE-MODE PIN VOLTAGES FOR THE CA3228E*

PIN NO.	VOLTAGE	PIN NO.	VOLTAGE
1	Ground	13	8.2V normal V_{CC} supply voltage
2	No connection	14	4.55V
3	7.76V (idle)	15	4.1V, 0.45 less than V_{15} in accelerate mode
4	0.01V	16	4.1V
5	5.2 V_{DC}, V_{AC} sawtooth 4.1 to 6.1V	17	4.1V
6	1.5 to 6.5V, speed dependent (0V without memory set)	18	4.1V
7	5.45V	19	4.1V (product of error voltage and gain)
8	$\cong 0V_{DC}$, $\cong 2.5V_{AC}$	20	4.1V
9	4V peak AC signal	21	8.2V, active low
10	0V to 6.5V, speed dependent, equal to V_6 in cruise mode	22	0.06V, active high
11	Same as V_{10}	23	0.025V
12	0.01V with brake switch open	24	Ground

*V_{CC} = 8.2V, speed set at 60mph (V_6 = 3.6V)

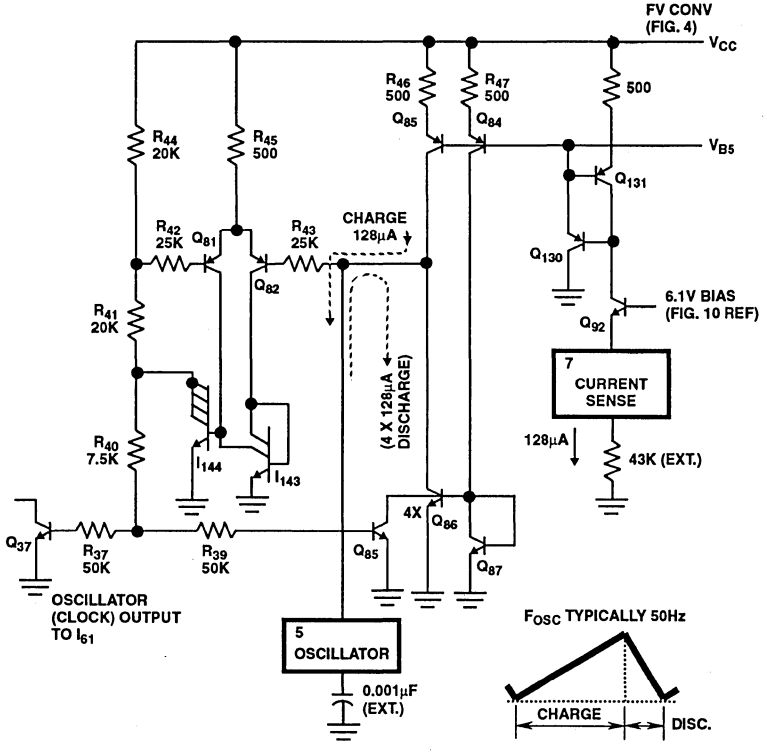


FIGURE 20. OSCILLATOR CIRCUIT USED FOR INTERNAL D/A CLOCK DRIVE

Note that the D/A converter cannot be set at low speeds and will remain at or near 0V until the frequency at pin 8 is near 50Hz (for the conditions of Figure 2). Dynamic signals are present at pins 5, 8, and 9. Speed dependent voltages are present at pins 6, 10, and 11. Error dependent signals have a notable effect on control amplifier output at pin 6 and the driver output pins 21 and 22. The command input at pin 3, the brake input at pin 12, and the gate output at pin 23 are mode dependent. The table does not reflect all of these changes since the conditions are noted only for a normal cruise setup at approximately 60mph. Again, the data sheet has further details on the various mode and state changes.

It is important to remember that the mode inputs are momentary touch switches except for the hold down condition of the accel and the coast switches. If pin 4 is monitored during the command input changes, it will be noted that delay switching times noted in the data sheet will be reflected at this pin.

Measures of the operating performance of the CA3228E are the wide power supply and temperature-operating ranges. The curve of Figure 21 shows the dynamic range of the power supply input V_{CC} at pin 13 over the temperature range of -40°C to +120°C. The normal V_{CC} specified is +8.2V ±0.8V or approximately 10% tolerance. The curves of Figure 21 also demonstrate a wide tolerance in the minimum to maximum range over which the device functions. A failure, as noted in the figure, is defined as a phase-locked-loop malfunction. Note that even with the wide range shown for power supply tolerance, it is still recommended that an external zener regulator or equivalent be used at the V_{CC} power supply input. Vehicular power supply conditions typically range from 9V to 16V, a range that exceeds the maximum range and rating for the operation of the CA3228E. While some applications may work at lower voltages than the recommended 7.4V minimum, operating conditions should not exceed the 9V power supply maximum rating.

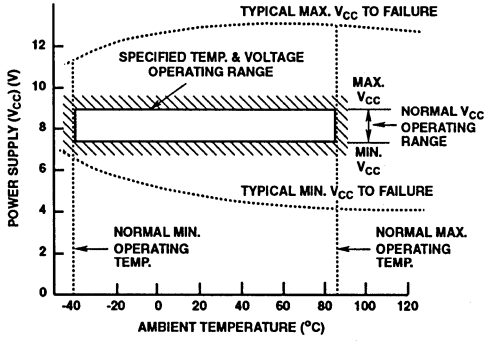


FIGURE 21. V_{CC} OPERATING RANGE OF THE CA3228E

Figure 22 shows another wide-range capability of the CA3228E when the temperature is varied. The V_S and V_M voltages are plotted versus temperature from -60°C to +100°C. Both the voltages for V_S and V_M are shown along with the equivalent speed condition for the typical application of Figure 2. For the 59.94mV/mph quoted above, the voltages of 4.3 to 4.5 are 72 to 75mph, respectively. It should be noted that Figure 22 is a measured curve from -55°C to +90°C with an equivalent 73.5 ±1.5mph error. Over the same range, the V_S and V_M readings typically tracked within 130mV while maintaining a cruise mode.

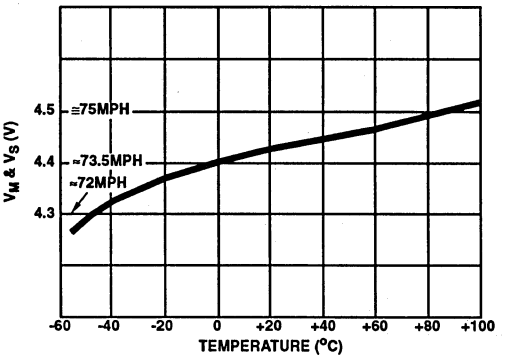


FIGURE 22. TYPICAL CHARACTERISTIC OF THE F/V CONVERTER OUTPUT, V_S, AND D/A OUTPUT, V_M, TRACKING vs. TEMPERATURE IN THE CIRCUIT OF FIGURE 2

General Applications

A CD4046 CMOS VCO (voltage controlled oscillator) may be used in the external loop to drive the sensor input at pin 8. In the closed-loop circuit shown in Figure 23, the CA3228E will respond to the accelerate, cruise and coast conditions and provide the appropriate drive at the vacuum and vent outputs. From an idle mode after turn-on, the frequency may be adjusted by the 1MΩ potentiometer. The adjustable range of the potentiometer output to the VCO input at pin 9 is ground on the low end to V_{CC} on the high end. The 0.047mF capacitor between pins 6 and 7 and the 100kΩ resistor at pin 1 were chosen to accommodate a frequency range of 50 to 250Hz.

When a VCO frequency representing a given speed is set by the frequency control and applied to the sensor input at pin 8, the set value may be entered into the CA3228E D/A memory with the set/accel command. Changing the switch at pin 9 of the CD4046 to the loop position then closes the servo loop with the VCO set frequency retained in the D/A memory. The PLL of the CA3228E will maintain the frequency of the VCO, and any conditions that force the VCO off frequency will be corrected by cruise or resume mode control.

While the VCO closed-loop circuit was used to demonstrate the capability of the CA3228E, it is also apparent that many applications of the referenced circuit or variations of this circuit may exist.

Sketches of various application possibilities for the speed control system are shown in the functional diagrams of

Figure 24. These applications have not been reduced to practice but are only suggested possible circuits. Since the MSLT and redundant brake affect the low end settings, a diode bias clamp of 1.6V should be used at pin 11 to keep V_S higher than the minimum speed lockout level. Pseudo DC voltage levels can be applied to pin 10 to set a V_S level for the D/A memory.

Further potential for use of the speed control system includes its combination with the CDP1800 and CDP6800 series microprocessor control systems with added memory and D/A control.

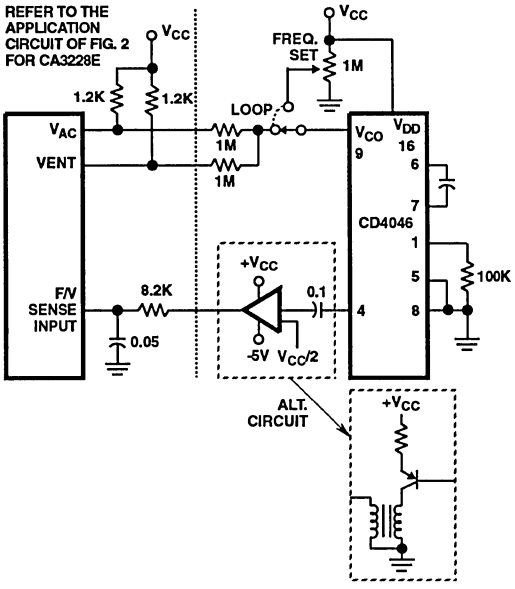


FIGURE 23. PLL OSCILLATOR FREQUENCY CONTROL CIRCUIT

References and Bibliography:

1. "CA3228E Speed Control System," Harris Data Sheet, File No. 1436.
2. "New Chips That Simplify Motor Control," L.J. Hadley, Machine Design, Feb. 12,1981.
3. "A Monolithic Speed-Control Micro-System For Automotive Applications," R.B. Jarret and W.D. Pace, ISSCC, 1978.

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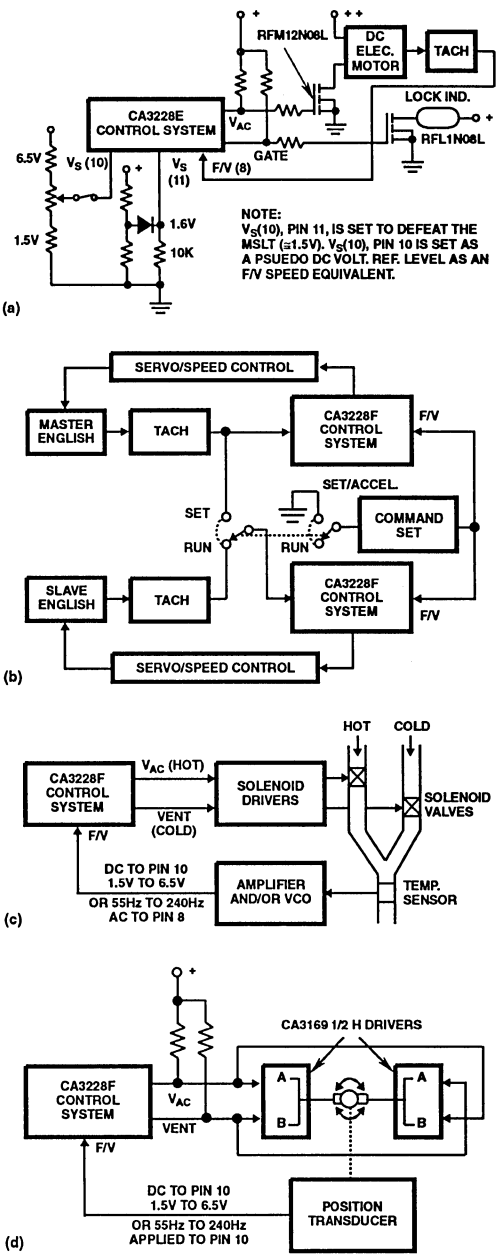

FIGURE 24. SUGGESTED APPLICATIONS OF THE CA3228E: (a) DC MOTOR SPEED CONTROL, (b) MASTER/SLAVE ENGINE SPEED CONTROL. SWITCH TO SET/ACCEL TO STORE MASTER SPEED IN SLAVE D/A MEMORY, THEN SWITCH TO "RUN". (c) AIR OR FLUID TEMPERATURE CONTROL. (SEE (a) FOR V_S SETUP CIRCUIT.) (d) DC MOTOR POSITION CONTROLLER. (SEE (a) FOR V_S SETUP CIRCUIT.)

Harris Semiconductor

APPNOTE

No. 7332.1 May 1992

Harris Power MOSFETs

THE APPLICATION OF CONDUCTIVITY-MODULATED FIELD-EFFECT TRANSISTORS

Author: Jack Wojslawowicz

Summary

The development of conductivity-modulated field-effect transistors, FETs, makes available to the system designer another solid-state device that can be used to implement power switching control. This paper reviews differences between the standard and the newly developed FET. It shows the significant advantages that the conductivity-modulated FET has over the standard FET. Several applications are presented to show that this new type of device works well in practical situations. The relative inmaturity of the conductivity-modulated FET may limit its initial utilization. But as the family grows and product innovation and refinement takes place, this newest member of the power semiconductor family will become a viable alternative to the other members.

General Considerations

The development of the power field-effect transistor has made available to the power-stage designer an entire new family of power semiconductors. Over the past 5 to 6 years, the breadth of product has grown to encompass the requirements of a large number of applications. A limiting factor that has slowed the utilization of power FETs in the high-current, high-voltage applications is the fact that the on-state resistance ($R_{DS(ON)}$) in a standard FET is related to its breakdown voltage (B_{VDSS}) by a nearly cubic power, i.e., $R_{DS(ON)} \approx B_{VDSS}$ 2.8. What this implies, as Figure 1 shows, is that as the breakdown voltage increases, the on-state resistance climbs even faster.

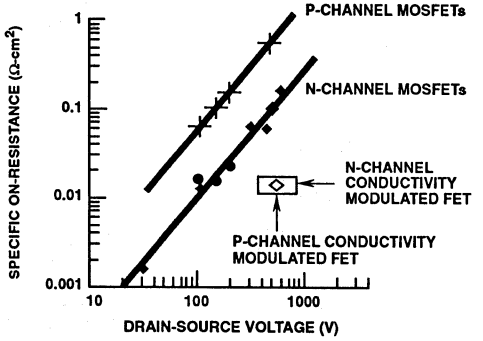

FIGURE 1. SPECIFIC ON-RESISTANCE OF P AND N-CNANNEL MOSFETS AND CONDUCTIVITY-MODULATED FETS vs. FORWARD BLOCKING VOLTAGE.

The MOSFET on-state resistance is contributed to primarily by three components of the transistor: the MOS channel, the neck region, and the extended drain region. The extended drain region contributes the most to the on-state resistance in high-voltage MOSFETs. To achieve a lower on-state resistance at a given blocking voltage, the usual technique is simply to make the die larger. However, increasing the die size has its limitations from a manufacturing point of view, since MOSFETs, with their very fine horizontal geometries, are highly defect-yield sensitive. As die size increases, the likelihood of a defect resulting in a nonfunctional part increases exponentially. This tendency, combined with a smaller number of parts per wafer, limits the availability of low-on-state-resistance, high-voltage MOSFETs.

A change in the horizontal geometry of the MOSFET can lower the specific on-state resistance per unit area. By using more channel width with smaller source cells placed closer together, a reduction in on-state resistance can be achieved. A limitation on how close these cells can be placed arises from a possible localization of field concentrations that will limit the voltage breakdown of the structure to less than the theoretical rating due only to mpurity concentrations. Therefore, for a given breakdown voltage, there exists a minimum spacing of the cell structure. Generally, the higher the required breakdown voltage, the further apart the cells must be placed.

As stated earlier, the extended drain region of the MOSFET generally contributes the most to the on-state resistance in high-voltage MOSFETs. As the required blocking voltage is increased, this region must be made thicker and more lightly doped to be able to support the desired voltage. It is this region's contribution to on-state resistance that the condictivity-modulated field-effect transistor drastically reduces. This reduction occurs as the result of the injection of minority carriers from the substrate and, in specific on-state resistance per unit area, is about 10 times less than in a standard MOSFET at the 400V BV_{DSS} level, as shown in Figure 1.

Further analysis has shown that the specific on-state resistance may be nearly independent of blocking-voltage level. This finding implies that at a BV_{DSS} of 1000V, the reduction in conductivity-modulated FETs over the standard MOSFETs could be perhaps 50 to 1. These reductions in on-state resistance per unit area that the conductivity-modulated FETs can achieve present the possibility that

high-voltage high-current FET-type devices can become more readily available because of the smaller die sizes associated with conductivity-modulated FETs.

Comparison of Standard and Conductivity-Modulated FETs

Standard and conductivity-modulated FETs share some characteristics, but are substantially different in others. Shown in Table 1 is a listing of the major characteristics that make the conductivity-modulated FETs unique among power semiconductor families. Foremost, it is a voltage-gated device; its input characteristics are similar to standard power MOSFETs of comparable chip size. Very little drive power is required at low to moderate switching frequencies. The device remains under the control of the gate within its normal operating conditions. It exhibits the normal linear mode as well as the fully saturated on-state of conventional power MOSFETs. When the gate voltage is removed, the device turns off, unlike the thyristor family of power semiconductors, which must be either externally or naturally (internally) commutated.

TABLE 1. CONDUCTIVITY-MODULATED FET CHARACTERISTICS

Voltage Gated	Small gate power required. Similar to standard power MOSFET.
Turn Off	When gate drive is removed... Unlike an SCR!
Nonlinear On-State Voltage drop	Like that of an SCR.
Turn On Speed	Fast! Comparable to a standard power MOSFET.
Turn-Off Speed	Slow! Comparable to a bipolar transistor.
Temperature Independent On-State Voltage Drop	Unlike the typical 2x variation of a power MOSFET.

The on-state voltage drop or resistance characteristic of a conductivity-modulated FET is markedly different from that of a standard power MOSFET, and is similar to that of a thyristor family member, the SCR. There is an offset voltage component (typically 0.6V) due to the p-n junction on the drain side, and a somewhat nonlinear resistive component, both of which are in series between the drain and source terminals. This series arrangement results in a highly nonlinear equivalent resistance, unlike the linear resistive characteristic of $V_{DS(ON)}$ of a standard FET.

The structure of the conductivity-modulated FET operates during its turn on just as a standard FET does, hence its turn-on speed is very similiar to that of a standard FET. With its high input impedance and its short propagation delay, the turn-on transistion of the conductivity-modulated FET, as well as the standard power FET, is easily controlled by the gate driving circuit. This characterstic allows the designer the ability to control EMI and RPI generation easily. With other power semiconductors, it may be necessary to employ elaborate circuit schemes to limit rapidly rising in-rush currents.

A significant characteristic that must be considered in power switching applications is that of turn-off speed. The internal action that makes the conductivity-modulated FET such a silicon-efficient device also makes it an inherently slower device during turn-off. The injection of the minority carriers during the on-state conduction of current results in these carriers being present at the moment of turn-off. Without any way of removing these carriers by external means, they must recombine within the structure itself before the device can revert to its fully off-state condition. The quantity of these carriers and how fast they can deplete themselves determines the turn-off switching speed of the conductivity-modulated FET. This process of recombination is considerably slower than the simple discontinuance of majority carrier flow by which the standard power FET turns off. Hence, again, the conductivity-modulated FET is an inherently slower device. Its turn-off speed lies somewhere between the performance ofathyristorand that of a bipolar transistor.

The final characteristic that makes the conductivity-modulated FET different from a conventional FET is the variance of on-state voltage with temperature. The characteristic of the conductivity-modulated FET is similar to that of an SCR, varying about -0.6mV/°C. The conventional FET has a positive temperature coefficient such that on high-voltage devices the $R_{DS(ON)}$ will double from its 25°C value when the junction temperature reaches 150°C. The system designer must take this characteristic into consideration when the heat sink is being designed for the system.

It is these similarities and differences that make the conductivity-modulated FET a unique member of the family of power-semiconductor switching devices. Applications of this alternative power switching device invariably make use of one or more of its unique characteristics.

Applications

Automotive Ignition

An application that can take advantage of the low drive-power capability of the conductivity-modulated FET is the electronic automotive ignition system. In Figure 2, the control IC takes the signal from the pickup coil located in the distributor and regulates the current through the ignition coil. At the proper time, the IC removes base drive from the bipolar transistor, which all systems currently employ as their coil driver. This removal of base drive allows the transistor to shut off which, in turn, causes a rapid decrease in the ignition-coil primary current. As the primary current decreases to zero, the energy stored in the field surrounding the primary is transferred to the secondary coil. The secondary coil, consisting of many more turns than the primary, transforms this energy into a higher voltage, resulting in a spark being generated in the cylinder. The control IC determines when this spark occurs, so as to derive usable power. With the use of a bipolar transistor, it is estimated that approximately two-thirds of the power dissipation that occurs in the control IC is the result of the need to be able to drive the required base current of the ignition output transistor. The high-impedance input of the

conductivity-modulated FET virtually eliminates the base-current drive dissipation of the control IC.

With improved silicon usage, the conductivity-modulated FET brings to power semiconductor switching devices the die size necessary to attain the required voltage and current-handling capabilities of the electronic ignition. This smaller-sized die makes possible smaller modules, whether they be hybrid or standard PC-based systems, than those currently implemented with bipolar-transistor technology.

Brushless DC Motors

Another emerging application that can make use of conductivity-modulated FETs is the emerging field of brushless DC motors. In this class of application, the solid-state devices are used to electronically switch the voltage to the multiplicity of windings that are employed. The motor consists of an armature that has a number of N and S poles consisting of high-strength permanent magnets. The stator is made up of the multiplicity of windings that were mentioned above; the windings are spaced incrementally about the outside frame of the housing. The voltages to these windings are all electronically switched to create a rotating magnetic field. The armature then rotates to maintain its relative position within the moving magnetic field. The switching of the voltage on the stator windings is done by means of power semiconductor devices. A basic block diagram of such a system is shown in Figure 3.

The control logic provides the proper sequence of drive signals based on the rotation direction desired, the speed desired, and the enable input. These requirements are combined with the inputs from the hall-effect sensors to determine which power devices should be activated. Since the current through the stator windings must be bidirectional, the half-bridge or totem-pole output configuration is used to steer the current. This circuit implementation is generally performed with complementary devices, although single-polarity devices can be used with increased circuit complexity.

In a typical 120V off-line system, like the one shown in Figure 3, the switching devices must have a 300V to 400V blocking capability. For larger size motors, where larger currents are necessary, the use of power FETs generally implies the use of large die to achieve a low power dissipation to meet the heat-dissipation capability of the packaging. The conductivity-modulated FET, with its temperature-independent on-state-voltage-drop characteristic, helps this situation by keeping the dissipation lower than can be achieved with a standard power FET because of the increasing $R_{DS(ON)}$ characteristic of that device. The small die size of the conductivity-modulated FET, the result of better silicon utilization, again makes them the practical choice in motor control not only because of their electrical characteristics, but also because of the lower manufacturing cost of the die.

As stated above, system complexity can be reduced with complementary devices. Although p-channel conductivity-modulated FETs are not yet commerically available, laboratory samples have been fabricated which offers better silicon utilization efficiency than their conventional p-channel counterparts. This statement is based on the fact that p-channel MOSFETs require a 2.5 times larger area than an n-channel device for the same $R_{DS(ON)}$. The easier

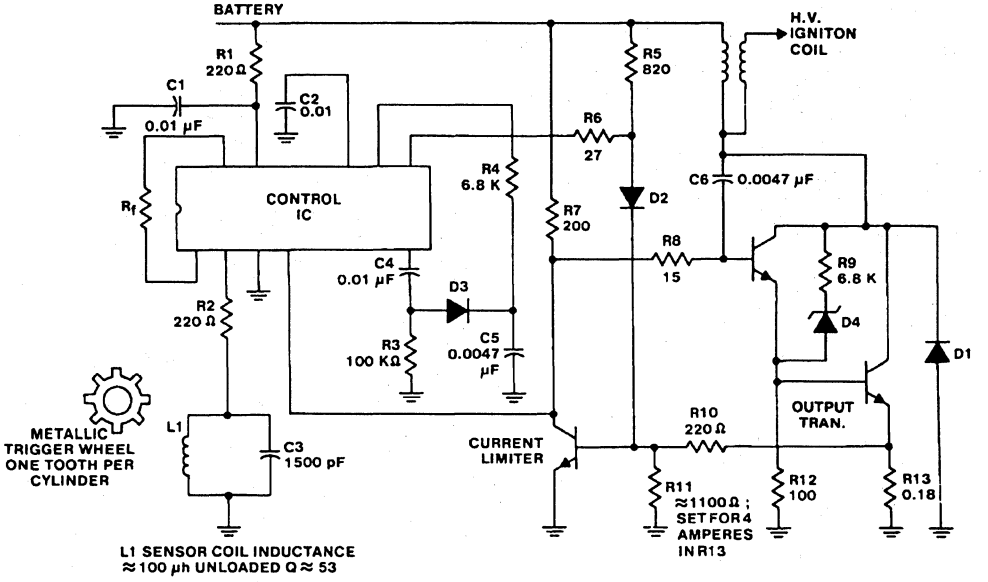

FIGURE 2. TYPICAL IGNITION SYSTEM

drive requirements for the n-channel (directly driven from the control IC) and the simplified voltage-translation circuit for driving the p-channel devices, combined with the smaller die size with potentially lower device cost for comparable power handling capability, makes the conductivity-modulated FET a natural for the brushless DC motor application.

Switching Power Supply

One final application that has the potential for conductivity-modulated FET usage is the switching power supply. A half bridge configuration implementation is presented in Figure 4. The system shown uses astandard PWM control IC to drive the conductivity-modulated FETs through the T2 transformer. The voltage drive characteristic of these devices makes the design of transformer T2 quite simple. The control IC is more lightly loaded because it does not have to supply a continuous base drive, as would be necessary with bipolar transistors.

The operating frequency and the "dead time" are the limitations placed on this system when conductivity-modulated FETs are used. The inherent lower switching speeds of these types of devices make these limitations necessary. The system is currently limited to the 20kHz to 30kHz range, with dead times as low as 1 to 2 microseconds. This characteristic is comparable to many existing bipolar systems.

Improvements in switching speeds will occur as the conductivity-modulated FET matures. It is, however, unlikely that they will ever have the same switching speeds as standard power FETs. This limitation prohibits their use in some of the newer higher-frequency power supplies being designed now with conventional FETs. However, in higher-power supplies, where conventional FETs must be paralled to achieve a low enough $R_{DS(ON)}$ for good efficiency, the conductivity-modulated FET may present a viable alternative with its smaller die size. Although the operating frequency of the system may have to be compromised to use them.

Conclusion

The conductivity-modulated FET represents a progression in the ever-advancing state-of-the-art development that occurs in the world of solid-state devices. The unique structure of these devices presents characteristics that make them equivalent in many ways to conventional FETs but superior in other ways. The system designer must take into account these similar and dissimilar characteristics to properly use them. The capabilities of the conductivity-modulated FETs allow them to make inroads into applications currently served by bipolar transistors, and in some cases conventional power FETs. As the devices mature through innovation and product refinement, conductivity-modulated FETs will become vital members of the family of solid-state power-semiconductor devices.

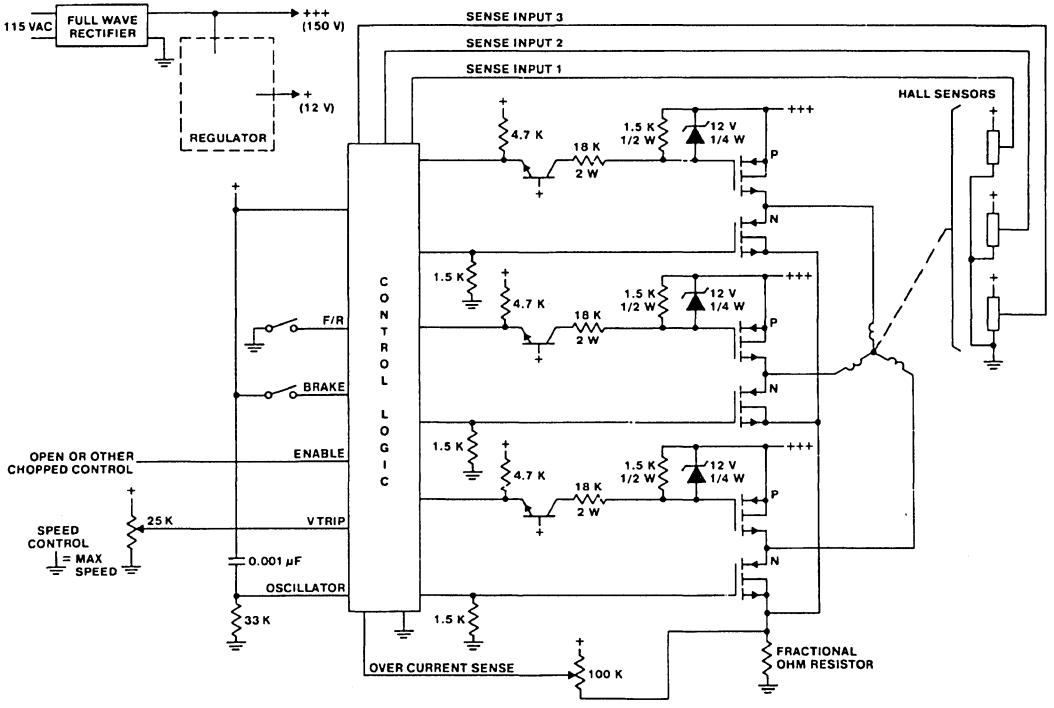

FIGURE 3. CONTROL CIRCUIT FOR THREE-PHASE BRUSHLESS DC MOTOR

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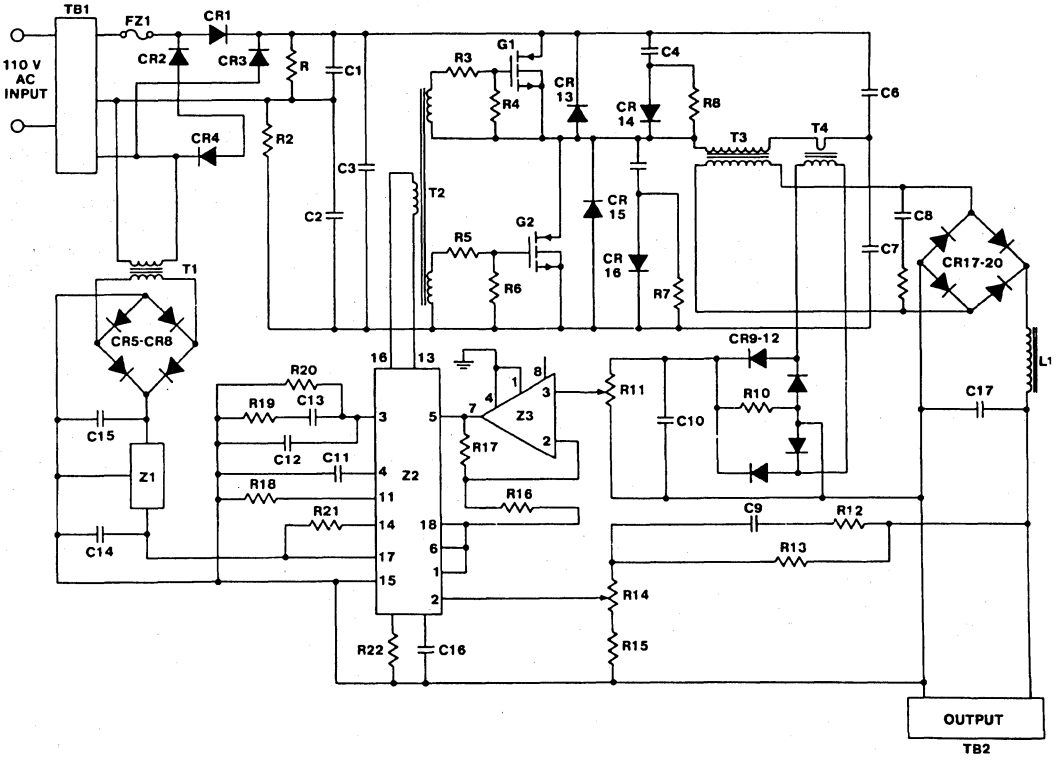


FIGURE 4. HALF-BRIDGE SWITCHING POWER SUPPLY

Harris Semiconductor

APPNOTE

No. 8602.1 May 1992

Harris Power MOSFETs

THE IGBTs - A NEW HIGH CONDUCTANCE MOS-GATED DEVICE

Author: J.P. Russell, A.M. Goodman, L.A. Goodman and J.M. Neilson

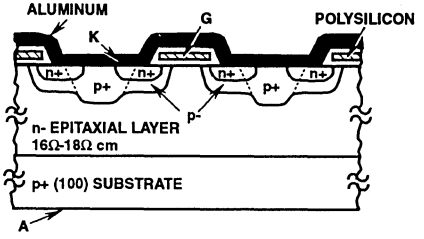
Abstract

A new MOS gate-controlled power switch with a very low on-resistance is described. The fabrication process is similar to that of an n-channel power MOSFET but employs an n^--epitaxial layer grown on a p^+ substrate. In operation, the epitaxial region is conductivity modulated (by excess holes and electrons) thereby eliminating a major component of the on-resistance. For example, on-resistance values have been reduced by a factor of about 10 compared with those of conventional n-channel power MOSFETs of comparable size and voltage capability.

Introduction

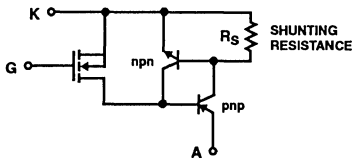
Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times, and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. In this letter, we describe the fabrication and characteristics of a new vertical power MOSFET structure that provides an on-resistance value about 10 times smaller than that of conventional power MOSFETs of the same size and voltage capability. In this device, the conductivity of the epitaxial drain region of a conventional MOSFET is dramatically increased (modulated) by injected carriers; this mechanism results in a significant reduction in the device on-resistance and leads to the acronym IGBTs (Insulated Gate Bipolar Transistor).

This device, while similar in structure to the MOS-gated thyristor,[4,5] is different in a fundamental way; it maintains gate control (doesn't latch) over a wide range of anode current and voltage.[6] The structure and the equivalent circuit for the IGBTs are shown in Figure 1(a) and (b); they are similar to those of an MOS-gated thyristor, except for the presence of the shunting resistance R_S in each unit cell. The fabrication is like that of a standard n-channel power MOSFET except that the n^--epitaxial Si layer is grown on a p^+ substrate instead of an n+ substrate. The heavily doped p^+ region in the center of each unit cell, combined with the sintered aluminum contact shorting the n^+ and p^+ regions, provides the shunting resistance shown in Figure 1(b). This has the effect of lowering the current gain of the n-p-n transistor (αn-p-n) so that $\alpha n\text{-}p\text{-}n + \alpha p\text{-}n\text{-}p < 1$. Thus latching is prevented and gate control is maintained within a large operating range of anode voltage and current.[6]



REGION	THICKNESS (μm)
EPI	60 - 62
n^+	1.0 - 1.5
p^-	3.5 - 4.0
p^+	5.0 - 5.5

a.) Structure



B.) EQUIVALENT CIRCUIT

In the remainder of this note we describe the operation and characteristics of this device.

Device Operation

The IGBT is a four-layer (n-p-n-p) device with an MOS-gated channel connecting the two n-type regions. In the normal mode of operation, a positive voltage is applied to the anode (A) relative to the cathode (K). When the gate (G) is at zero potential with respect to K, no anode current (i_A) flows for anode voltage V_A below the breakdown level V_{BF}. When $V_A < V_{BF}$ and the gate voltage is larger than the threshold value V_{gt}, electrons pass into the n^--region (base of the p-n-p transistor). These electrons lower the potential of the n^--region, forward biasing the p^+ - n^- (substrate-epi-layer) junction, thereby causing holes to be injected from the p+ substrate into the n^- epi-layer region. The excess electrons and holes modulate the conductivity of the high-resistivity n-region, which dramatically reduces the on-resistance of the

device. During normal operation, the shunting resistor (R_S) keeps the emitter current of the n-p-n transistor very low, which keeps αn-p-n very low. However, for sufficiently large i_A, significant emitter injection may occur in the n-p-n transistor, causing αn-p-n to increase; in this case the four-layer device may latch, accompanied by loss of control by the MOS gate. In this event, the device may be turned off by lowering i_A below some "holding" value, as is typical of a thyristor.

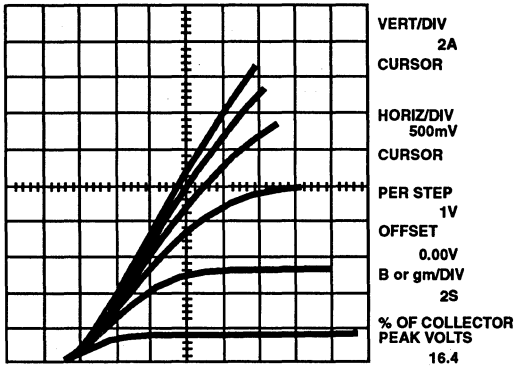
Device Characterization

Two different lots of IGBT structures, consisting of about 10 wafers/lot, have been successfully prepared to date. From these wafers, 1.5mm and 3mm square devices were fabricated using a standard HEXFET geometry[7] with a polysilicon gate electrode over an SiO_2 gate dielectric. Several hundred IGBT were mounted in standard TO-3 and TO-66 packages and characterized under DC and pulsed conditions, as described below.

With zero gate bias, the forward characteristic of a IGBTs shows very low current (<1nA) up to about 390V, where it breaks up sharply to much larger current levels with only a slight increase in voltage. If the internal junction between the p^+ substrate and the n^- epitaxial layer had been edge-passivated, a similar reverse breakdown characteristic would be expected. The actual reverse breakdown voltage for our devices was about 100V because edge passivation was not used.

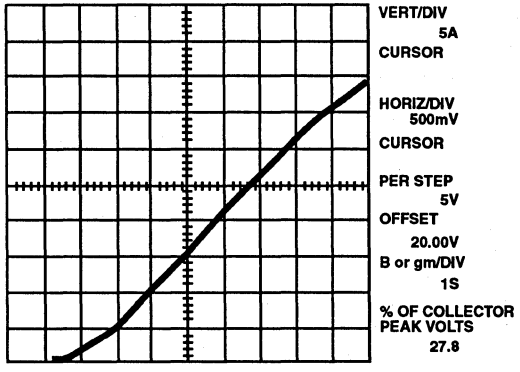
Figure 2(a) shows the MOSFET-like transfer characteristics of an IGBT in the low gate-voltage region. A noteworthy feature of the IGBT characteristic is the ~0.7V offset, from the origin, of the steeply rising portion of the i(v) characteristics. This offset is the voltage required to forward bias the p^+ - n^- (substrate-epi-layer) junction, and is an integral characteristic of the present device.

Figure 2(b) shows the i(v) characteristic of an IGBT with V_g = 20V, and demonstrates the low on-resistance of the device (~0.084Ω at 20A). The on-resistance values of nearly all of the many IGBT fabricated to date have been less than 0.1Ω (at 20A) for the 3mm square devices. Such values compare very favorably with those of conventional power MOS structures, as illustrated in Figure 3. Here, the open data points (and the upper curve) are from data sheet specifications of commercial power MOSFETs (Harris, IRC, and Motorola). The solid data points (and the lower curve) are those of Baliga, which he labelled "state-of-the-art",[3] supplemented with some of the "best" of Harris' commercial and developmental MOSFETs. Note that the on-resistance of the IGBT is approximately l0 times less than that of a 400V state-of-the-art MOSFET. Moreover, similarly low on-resistance values should be obtainable from IGBT designed for higher drain-source voltages. This is due to the fact that the resistance of the modulated region is determined by the concentrations and mobilities of the excess carriers (as in a p-i-n diode)[8] rather than by the background doping of the layer. In particular, the epi-layer doping and thickness of our present IGBT structures were designed for 600V, but V_{BF} was limited to 400V by the edge design of the device. An improved edge design should provide a blocking capability closer to bulk breakdown, without altering the on-resistance of the device. This would make the IGBTs on-resistance of less than 0.1Ω even more attractive for high-voltage applications.



PULSE TEST: PULSE WIDTH = 250μs, DUTY CYCLE < 0.5%

a.)



PULSE TEST: PULSE WIDTH = 250μs, DUTY CYCLE < 0.5%

b.)

FIGURE 2 - (a) MOSFET - Like Characteristic (b) IGBT i(v) with V_g = 20V

Transient Response Measurement

Switching time measurements under pulsed gate-voltage operation were used to characterize the transient operation of the device. The response of the anode current to a square-wave gate-voltage pulse is comprised of a rapid turn-on (with a typical time less than 1μs) and a somewhat slower turn-off. We observed that the turn-off transient consists of an initial "fast" component, followed by a "slow" tail, as shown in Figure 4.

We believe that the initial rapid decay is due to the turn-off of the MOS portion of the equivalent circuit, and the turn-off tail is due to the time required for the excess carriers in the epitaxial drain region to decay. In general, turn-off times in the range of 5μs to 20μs were observed, with the precise value depending on circuit conditionsand the turn-off time of the gate pulse.

The n-p-n-p structure of the IGBTs is similar to that of a thyristor and can be forced to latch under sufficiently high drive conditions. We have observed latching currents in the range 10A - 30A in 3mm square chips. The magnitude of the latching current has been found to depend on both anode voltage and temperature, decreasing with increasing anode voltage or increasing temperature.

More interestingly, the latching current is also strongly influenced by the gate voltage turn-off time. Slow gate turn-off (~10μs) permits anode currents up to 30A without latching. However, rapid gate turn-off (≤ 1μs) leads to latching at a much lower anode current level (~10A) in the same device. We believe that latching during rapid turn-off of the gate voltage is due to current being forced through the n-p-n transistor causing αn-p-n to increase, and leading to the condition for latching, αn-p-n + αp-n-p = 1. Slow turn-off of the gate voltage prevents this, since the induced channel turns off slowly and partially shunts the n-p-n transistor; the small current through this transistor keeps αn-p-n sufficiently low to avoid latching.

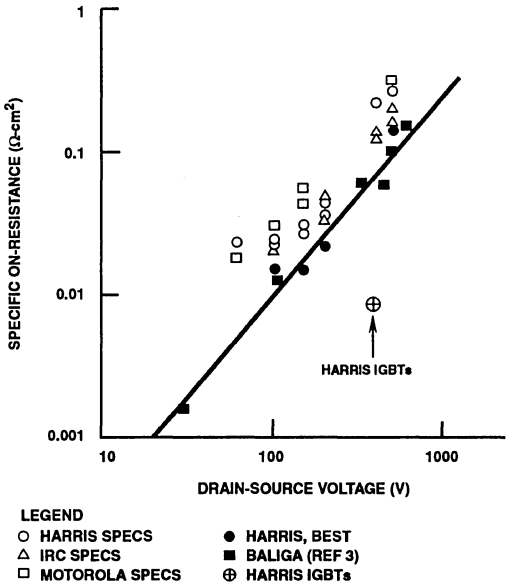


FIGURE 3. SPECIFIC ON-RESISTANCE vs. DRAIN-SOURCE VOLTAGE CAPABILITY FOR STATE-OF-THE-ART POWER MOSFETS AND THE IGBTs

Summary

A new MOS-gate-controlled power device, the IGBTs, has been described. The device has the desirable feature of a very low on-resistance similar to that of a thyristor, but is capable of maintaining gate control of the anode current over a wide range of operating conditions. The low on- resistance is due to conductivity modulation of the n epitaxial layer equivalent to the extended drain in a power MOSFET; this carries with it the penalty of slow switching compared with that of a conventional power MOSFET.

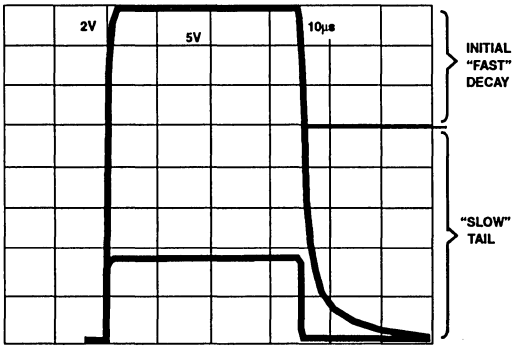


FIGURE 4. GATE VOLTAGE (LOWER TRACE) AND ANODE CURRENT (UPPER TRACE) WAVEFORMS FOR I_A(MAX) = 8A

Acknowledgment

The authors gratefully acknowledge the various helpful contributions of C. Nuese, D. Bergman, R. Ford, R. Jarl, G. Looney, P. Robinson, W. Romito, L. Skurkey, R. Stolzenberger, C. Wheatley, J. Wojslawowicz, and the staff of the Integrated Circuit Technology Center at RCA Laboratories. Added Note: Following submission of this Note, a similar device was described by B. J. Baliga in a presentation on December 14, 1982 at the International Electron Devices Meeting in San Francisco, CA. (B. J. Baliga et al., "The Insulated Gate Rectifier (IGR): A New Power-Switching Device", in IEDM Tech. Dig. 1982, pp 264-267.

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Harris Semiconductor

APPNOTE

No. 8603.1 May 1992

Harris Power MOSFETs

IMPROVED IGBTs WITH FAST SWITCHING SPEED AND HIGH-CURRENT CAPABILITY

Author: A.M. Goodman, J.R. Russell, L.A. Goodman, C.J. Nuese and J.M. Neilson

Abstract

Conventional vertical power MOSFETs are limited at high voltages (>500V) by the appreciable resistance of their epitaxial drain region. In a new MOS-gate controlled device called a IGBT, this limitation is overcome by modulating the conductivity of the resistive drain region, thereby reducing the on-resistance of the device by a factor of at least 10. However, the device previously described is slow in turnoff, having a fall time in the range 8 to 40μs. The purpose of our present work has been to reduce the fall time significantly and to increase the latching current level of the IGBTs, while retaining its desirable features. By modification of the epitaxial structure and addition of recombination centers, we have achieved fall times as low as 0.1μs and latching currents as high as 50A, while retaining on-resistance values <0.2Ω for a 0.09cm^2 chip area. The techniques used for the introduction of recombination centers include electron, gamma-ray, and neutron irradiation, as well as heavy metal doping. For a series of IGBTss (with forward-blocking voltage capabilities of 400-600V), the fall time can be reduced by more than one order of magnitude with a penalty of less than a 20% increase in on-resistance.

Introduction

Vertical MOSFETs have become increasingly important in discrete power device applications due primarily to their high input impedance, rapid switching times and low on-resistance. However, the on-resistance of such devices increases with increasing drain-source voltage capability,[1-3] thereby limiting the practical value of power MOSFETs to applications below a few hundred volts. This limitation has been effectively overcome by the development of a new MOS power device in which the conductivity of the n-type epitaxial drain region is greatly increased (modulated) by the injection of minority carriers from a p-type substrate. We have called this device a COMFET-an acronym for COnductivity Modulated Field Effect Transistor;[4] the device has also been called an IGBT or Insulated Gate Bipolar Transistor.

The devices, as originally described, had most of the advantages of conventional power MOSFETs; in addition, they exhibited more than an order-of-magnitude reduction in high current on-resistance values, permitting improved utilization of silicon chip area. However, they also had two disadvantages:

When a IGBT is turned off, the injected minority carriers that remain in the epitaxial drain region decay by recombination with majority carriers at a rate determined by the minority-carrier lifetime, t. Large values of t resulted in anode-current fall time, tF, in the range 8-40 ms. 4,5

The maximum operating current is limited by latchup of the parasitic thyristor that is inherent in the device structure. Typical latching current levels of IL, ≤ 10A were observed in 0.09cm2 area devices when the gate voltage was turned off rapidly (<1ms); for slower gate voltage turnoff (~10ms), IL values as high as ~30A were observed.

The purpose of the present work has been to reduce tF and to increase IL while retaining the desirable features of the device. By modifying the epitaxial structure and adding recombination centers to the epitaxial drain region, we have achieved tF values as low as 100ns and IL values as high as 50A with rapid gate voltage turnoff.

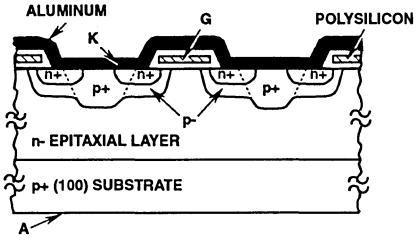
Modified Structure

A schematic diagram of the original IGBT structure[4] is shown in Figure 1(a), and the equivalent circuit is shown in Figure 1(b); they are similar to those of an MOS-gated thyristor except for the presence of the shunting resistance Rs in each unit cell. The fabrication is like that of a standard n-channel power MOSFET, except that the n--epitaxial layer is grown on a p+ substrate instead of an n+ substrate. The heavily doped p+ region in the center of each unit cell, combined with the aluminum contact shorting the n+ and p+ regions, provides the shunting resistance RS. This has the effect of lowering the current gain of the n-p-n transistor in the equivalent circuit so that anpn + apnp <1, thereby preventing latching over a large operating range of anode voltage VA and anode current iA. However, for sufficiently large iA, emitter injection in the n-p-n transistor will increase, accompanied by an increase in anpn. When anpn + apnp increases to 1, the four-layer device will latch; the level of iA at which this occurs is the latching current level, IL. Thus, it

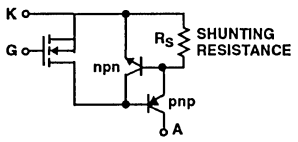
can be seen that a structure modification that lowers apnp will allow a greater range of iA (and anpn) without latching; that is, a reduction in apnp corresponds to an increase in IL.

The modified structure shown in Figure 1(c) differs from that in Figure 1(a) by the addition of a thin (~10mm) layer of n+ silicon in the epitaxial structure between the n- region and the p+ substrate. This n+ layer lowers the emitter injection efficiency of the p-n-p transistor in the equivalent circuit, and results in an increase in IL by a factor of 2 to 3. In addition, there is also a reduction in tF.

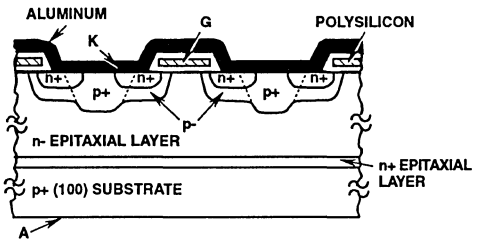
These results are illustrated in Figure 2, in which t_F, is plotted versus i_A for each device structure. It should be noted that IGBTss with the modified structure can block high voltage only in the forward voltage direction since the emitter junction (p+ - n+) of the p-n-p transistor breaks down at a low level when the polarity of the applied voltage is reversed.



(a) ORIGINAL STRUCTURE



(b) EQUIVALENT CIRCUIT



(c) MODIFIED STRUCTURE

FIGURE 1. (a) SCHEMATIC DIAGRAM OF ORIGINAL IGBTs STRUCTURE. (b) EQUIVALENT CIRCUIT (c) SCHEMATIC DIAGRAM OF MODIFIED STRUCTURE

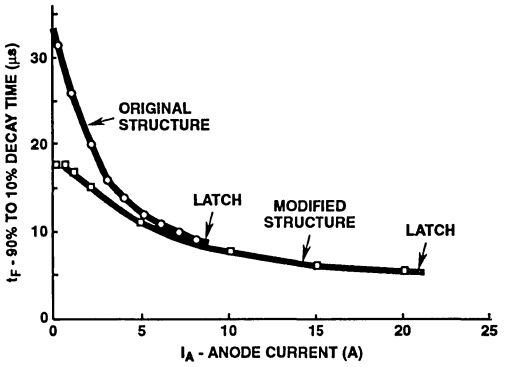


FIGURE 2. ANODE-CURRENT FALL TIME t_F VERSES ANODE CURRENT FOR ORIGINAL STRUCTURE AND MODIFIED STRUCTURE.

Addition Of Recombination Centers

We have used a variety of techniques to add recombination centers to IGBTss; these include high energy electron, gamma ray, and fast neutron irradiation, as well as heavy metal doping. The irradiations were carried out after completion of all of the high-temperature processing steps, but in each case an additional heat treatment was necessary to stabilize the devices by annealing out gate oxide charge, as well as those radiation induced defects in the silicon (recombination centers) that would otherwise anneal out slowly at the device operating temperature.[7] Typical values of t_F of the order of 1µs or less were achievable using any of the techniques.

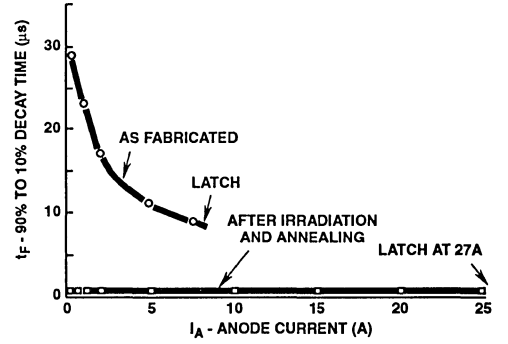
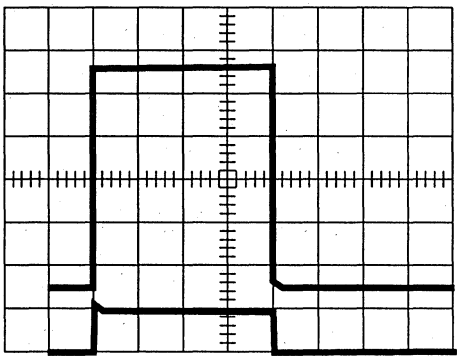
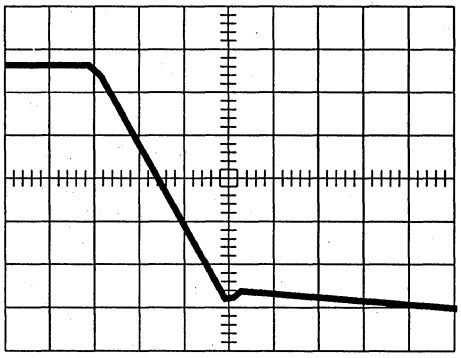


FIGURE 3. ANODE-CURRENT FALL TIME t_F VERSUS ANODE CURRENT FOR AN AS-FABRICATED DEVICE AND AFTER 14MeV NEUTRON IRRADIATION (10^{13}n/cm^2) FOLLOWED BY ANNEALING AT +300°C.

An example of the variation of t_F, with i_A (1) as fabricated and (2) after irradiation with 14MeV neutrons and annealing is shown in Figure 3. Here, the neutron fluence was ~10^{13}n/cm^2; this was followed by annealing at +300°C. Note that t_F, has not only been drastically reduced, but is virtually constant at ~0.6µs; i.e., almost independent of i_A.



TOP: ANODE CURRENT, 5A/DIV
BOTTOM: GATE VOLTAGE, 20V/DIV
5μs/DIV



ANODE CURRENT ON
EXPANDED TIME SCALE
5A/DIV
100ns/DIV
t_{FALL} ~ 160ns

FIGURE 4. IGBTs ANODE CURRENT AND GATE VOLTAGE WAVEFORMS

It is possible to lower tf, still further by appropriate irradiation and annealing or by heavy metal doping procedures, although this is not necessarily desirable for reasons that are discussed below. The smallest values of t_F that we have obtained for fully stabilized IGBT is in the range 100ns to 200ns. This is illustrated in Figure 4.

The reduction in minority carrier lifetime that allows faster switching also carries with it a penalty higher forward voltage drop when the device is turned on; i.e., higher on-resistance. Since, in the forward conduction of an IGBT, current and voltage are not linearly related, it is necessary to specify a current level at which to compare on-resistance values of different devices. In Figure 5 we plot the on-resistance (at i_A = 20A) of a series of devices with 0.09cm^2 chip area against their t_F values after irradiation and annealing. All t_F values shown were obtained at i_A = 5A; for the devices with short switching times, t_F is virtually independent of i_A. Clearly, there is a trade-off involved, and the optimum choice of a value for t_F and the corresponding on-resistance value will depend, to some extent, on the intended application. However, even for the shortest switching times shown (100ns), the on-resistance value of 0.2Ω is approximately an order-of-magnitude less than that of comparably sized n-channel MOSFETs.

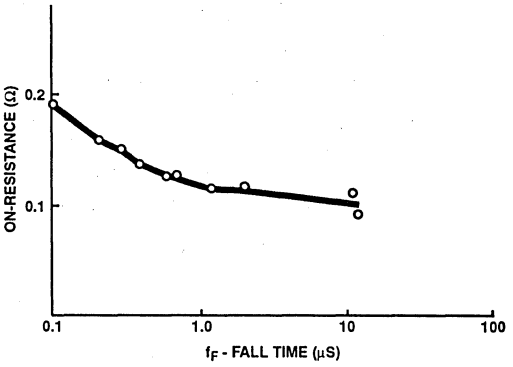


FIGURE 5. ON-RESISTANCE vs. ANODE-CURRENT FALL TIME t_F FOR A SERIES OF IGBTsS AFTER VARIOUS IRRADIATION AND ANNEALING TREATMENTS

Temperature Dependence Of T_f And I_l

All of the device performance data presented thus far have been measured at room temperature. However, power devices are often operated at elevated temperatures, and it is important to determine how their performance varies with temperature. In Figure 6 the variation of t_F and I_L for a device that has been irradiated and annealed is plotted versus temperature in the range +25°C to +150°C. This behavior is typical of all of the devices we have tested; i.e., tf increases and I_L decreases with increasing temperature, both by a factor of between 2 and 3 in the interval +25°C to +150°C.

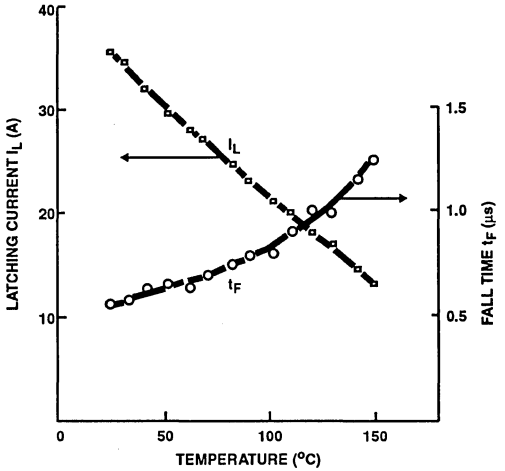


FIGURE 6. VARIATION OF ANODE-CURRENT FALL TIME t_F AND LATCHING CURRENT I_L WITH TEMPERATURE

Summary

By modification of the epitaxial structure of the IGBT and the addition of recombination centers, we have achieved anode-current fall times as low as 100ns in IGBT with latching currents as high as 50A for a 0.09cm^2 chip area. We have described the trade-off between on-resistance and anode-current fall time that may be obtained, and have demonstrated the variation of anode-current fall time and latching current with operating temperature.

Acknowledgment

The authors are indebted to D. Bergman, R. Ford, F. DiGeronimo, G. Looney, P. Robinson, W. Romito, L. Skurkey, M. Snowden, R. Stolzenberger, and the staff of the Integrated Circuit Technology Center at RCA Laboratories for their various contributions to the fabrication and characterization of the IGBTss. A special thank you goes to F. Taft, Z. Streletz, and H. Hendel who carried out the device irradiations.

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7. 7. S. K. Ghandi, Semlconductor Power Devices (John Wiley, New York, 1977) p 296.

Harris Semiconductor

APPNOTE

No. 8610.1 May 1992

Harris Power MOSFETs

SPICING-UP SPICE II SOFTWARE FOR POWER MOSFET MODELING

Author: C.F. Wheatley, Jr., H.R. Ronan, Jr., G.M. Dolny

The SPICE II simulation software package is familiar to most designers working in computer-aided design of integrated circuits. Developed by L. W. Nagel in 1973, SPICE II has become a widely available, well-understood design tool for IC modeling and analysis. But, SPICE II has a shortcoming: its standard simulation programs were developed when all MOSFETs were low-power devices. Power MOS devices are growing in use today, both as discrete components and, potentially, as output stages of power integrated circuits. SPICE II in its current form doesn't recognize these new developments. Its built-in FET models aren't able to simulate all the modes of new power MOS device operation. For example, SPICE II doesn't recognize the way a power MOSFET's internal capacitances change with bias conditions, the presence of a cascode JFET that complicates both static and dynamic operation, or the presence of a parasitic body diode that affects operation in the third quadrant. Without this information, SPICE II will predict power MOSFET performance that is incorrect.

Since SPICE II's internal device models can't be easily changed for all existing copies, we looked for another approach to update the capabilities of this widely used simulation package in its standard form. Adding a "subcircuit" of external components that complement the devices within the SPICE II software, so as to form a true, equivalent circuit of a power MOSFET, is the answer.

The subcircuit works nicely with the standard SPICE II software, providing a model with all the terminal characteristics of a power MOSFET. Parameters of the subcircuit model can be determined from simple terminal measurements or from standard data sheets, using the algorithmic and empirical approach described below. Once these parameters are in place, SPICE II can be used to accurately simulate either p-channel or n-channel power MOSFET devices over a wide range of currents and voltages. The subcircuit functions as an embedded subroutine, so it can be used repetitively for any number of power MOSFETs in a design. This technique can be used to model power MOSFETs with any version of the SPICE II program presently available, without any modifications to its internal source code. The technique can also be used with other commercially available or in-house-developed circuit simulators.

Modeling The Power MOSFET

A cross-sectional view of a cell of a Harris IRF130 power MOSFET is shown in Figure 1. The easiest way to understand its electrical characteristics is to think of it as a vertical JFET, driven in cascode from a low-voltage lateral MOSFET.[1, 2] When the gate is positively biased with respect to the n-bulk, an accumulation layer forms in the n-region beneath the gate. This layer acts as the drain of the lateral MOSFET, as well as the source of the vertical JFET. The JFET channel is then-region between the two p-type body diffusions, which act as the gate of the JFET. The JFET drain is the n+ bulk, usually thought of as the power MOSFET drain.

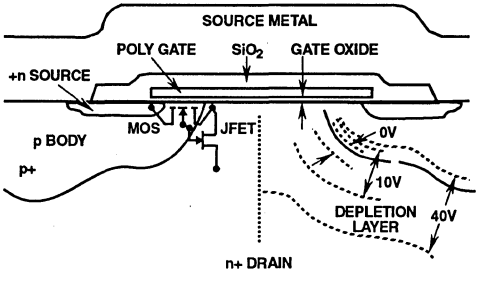

FIGURE 1. A CROSS-SECTIONAL VIEW SHOWS THE PHYSICAL MAKEUP OF THE LATERAL LOW-VOLTAGE MOSFET AND VERTICAL JFET THAT OPERATE IN CASCODE AS THE POWER MOSFET.

When you look at the power MOSFET this way, it becomes possible to use the standard SPICE II built-in device models, because SPICE II can simulate both the vertical JFET and the lateral MOSFET. When we use the subcircuit to add the rest of the Harris IRF130 power MOSFET to these SPICE II-simulated devices, we get a satisfactory equivalent circuit, shown in Figure 2.

The gate-to-source capacitance of the Harris IRF130 power MOSFET is represented by C_{21}. It is really a composite of two capacitances. The first is formed between the polysilicon gate and source metal (with the thick oxide as a dielectric). The second is formed between the gate and the n+ source (with the thin oxide acting as the dielectric). The value of C_{21} is essentially unchanged by voltage or current.

Capacitor C_{24} is formed between the power MOSFET gate and the accumulation layer, with the thin gate oxide as a dielectric. So long as the gate is positive with respect to the n-neck region, the accumulation layer exists and C_{24} doesn't

change. But, if the external drain voltage (less their voltage drop across then-drift region) approaches the gate voltage, the accumulation layer starts to disappear. When that happens, C_{24} abruptly drops in value. This sudden change has to be taken into consideration.

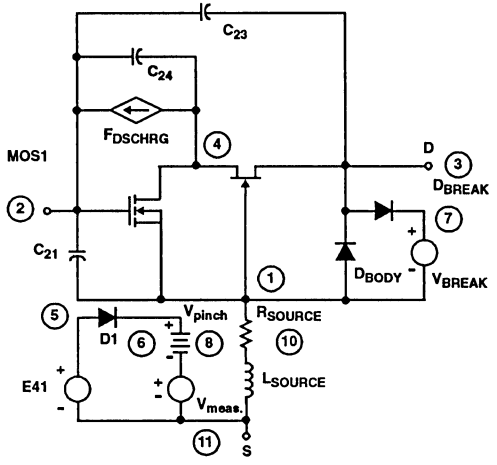

FIGURE 2. THE EQUIVALENT CIRCUIT OF THE POWER MOSFET IS MADE BY COMBINING SPICE II MODEL ELEMENTS WITH SOFTWARE SPECIFIED COMPONENTS ON A "SUBCIRCUIT."

Capacitor C_{23} represents the gate-to-drain capacitance of the Harris IRF130 power MOSFET. Because the accumulation layer normally acts as an electrostatic shield, C_{23} has no significance until the layer ceases to exist under the conditions just described. When it does disappear, the effect upon C_{23} is abrupt, and also has to be taken into consideration. The sudden changes in C_{24} and C_{23} cannot be easily modeled with the standard SPICE II software.

Figure 2 illustrates what happens: If the JFET source voltage (node 4) is very low compared to its pinch-off voltage, the JFET will be highly conductive, tightly coupling C_{24} to the JFET drain (which is also the drain of the Harris IRF130 power MOSFET). However, as the node 4 voltage approaches the pinch-off voltage (V_{PINCH}) of the JFET, it operates in a constant-current mode. This action decouples C_{24} from the JFET drain, making possible a much faster slew-rate, determined by C_{23}. If the node 4 voltage is allowed to exceed V_{PINCH} of the JFET, errors will exist in the output waveforms predicted by the standard SPICE II model.

To correct the situation, the added subcircuit includes a current-controlled current source, F_{DSCHRG}, and a current-sense network containing D1. If node 4 voltage begins to exceed V_{PINCH} of the JFET, D1 conducts, and its current is sensed at V_{MEAS}. The high-gain current source F_{DSCHRG} is turned-on rapidly and partially discharges C_{24}, pinning node 4 voltage at the pinch-off voltage of the JFET. In setting up the parameters of the subcircuit, the ideality factor of D1 is set at 0.03 to assure that node 4 voltage will never exceed V_{PINCH} of the JFET by more than a few millivolts. This condition results in waveform predictions from the SPICE II model that represent the true characteristics of the power MOSFET.

The body diode (D_{BODY} in Figure 2) is formed by the drain-to-body diffusion pn junction of the Harris IRF130 power MOSFET. D_{BODY} is added as an external component in the subcircuit because the built-in gate-to-drain diode of the SPICE II JFET model is inconvenient when it comes to modeling third-quadrant conduction of a power MOSFET. We want most of the third-quadrant current to flow in D_{BODY}. So, we effectively delete the SPICE II model's built-in diode by setting its saturation current parameter to an artificially low value, such as 10^{-20} ampere.

To round-out the subcircuit, a resistor value is chosen for the JFET drain of the SPICE II model to represent the series resistance of the n-drain region of the Harris IRF130 power MOSFET.[3] We also add resistor R_{SOURCE} to represent the series source resistance of the Harris IRF130 power MOSFET: a composite of resistances in the n+ source region, contact resistance, and source-metal series resistance. Finally, we add inductor L_{SOURCE} to represent the source inductance of the power MOSFET contributed by the source metallization and bond wires.

Choosing Parameters to Simulate A Power MOSFET

To accurately simulate the terminal characteristics of the physical power MOSFET you are working with, you will need to adjust the SPICE II model parameters and select subcircuit component values. Look first at adjustment of the SPICE II model. The static current-voltage characteristics of the power MOSFET are determined by the low-voltage lateral MOSFET included in the SPICE II model; Figure 2. In saturation (large values of V_{DS}), the lateral MOSFET device is modeled according to the following equation:

$$I_{DS} = \frac{(K_P)W\,(V_{GS} - V_{TO})^2}{2L}$$

where

K_P = Process Transconductance Parameter

V_{TO} = Threshold Voltage

W = L = 1μm (Fixed In This Note For Convenience)

I_{DS} = MOSFET Drain Current

V_{GS} = MOSFET Gate-To-Source Voltage

Continuing with the example device, the Harris IRF130 power MOSFET, a plot of the square root of I_{DS} versus gate voltage (V_{GS}) provides the curves shown in Figure 3 for V_{DS} = 10 volts. These curves provide the process transconductance parameter, $(K_P/2)^{0.5}$, and threshold voltage, V_{TO}, directly. This data can then be used to find the value of source resistance, R_{SOURCE}. This series resistance is important because it causes the curve produced by plotting the square root of I_{DS} versus V_{GS} to depart from linearity at high current levels. Departure at very low current levels is caused by subthreshold conduction, which we ignore in this model.

To find the JFET drain resistance, we use the value of source resistance, R_{SOURCE}, and plots of I_{DS} versus V_{DS} for operation in the linear region, as shown in Figure 4.

To find the current, resistance and capacitance parameters of the body diode (D_{BODY} in Figure 2), first plot log I_{DS} versus V_{DS}, as shown in Figure 5, holding the gate voltage, V_{GS}, negative for third-quadrant operation; i.e., where V_{DS} is less than 0. This plot gives the saturation current and resistance of D_{BODY}. The minority-carrier transit-time parameter (TT) of the SPICE II program is chosen to provide the best fit to measured transient reverse-recovery data. The junction capacitance value of D_{BODY} is equal to the power MOSFET device output capacitance, C_{OSS}, at zero volts. This value can be obtained from the device data sheet, or by bridge measurement. It is usually specified at 25 volts, and may be converted to zero volts by multiplying by 6.

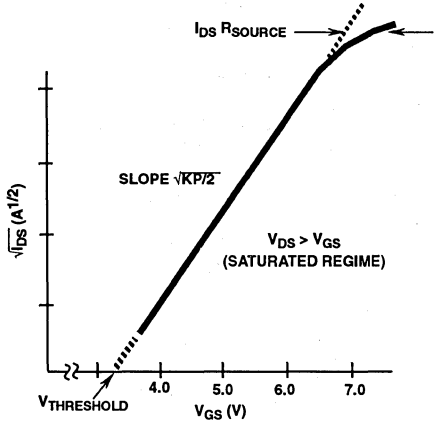

FIGURE 3. THIS PLOT OF THE SQUARE ROOT OF DRAIN CURRENT vs. GATE VOLTAGE DEFINES THE THRESHOLD VOLTAGE, V_{TO}, $(K_P/2)^{0.5}$, AND R_{source}, FOR THE POWER MOSFET.

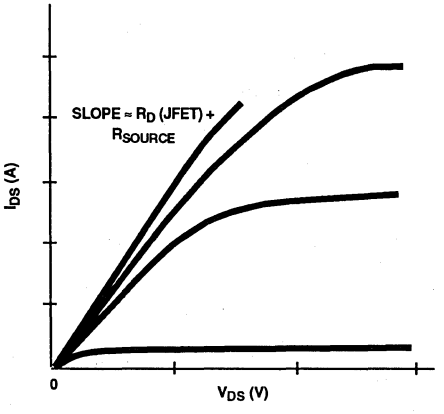

FIGURE 4. DRAIN CURRENT vs. DRAIN VOLTAGE OF THE POWER MOSFET PLOTTED USING CONSTANT GATE VOLTAGES. THIS CURVE DEFINES THE ON RESISTANCE OF THE DEVICE.

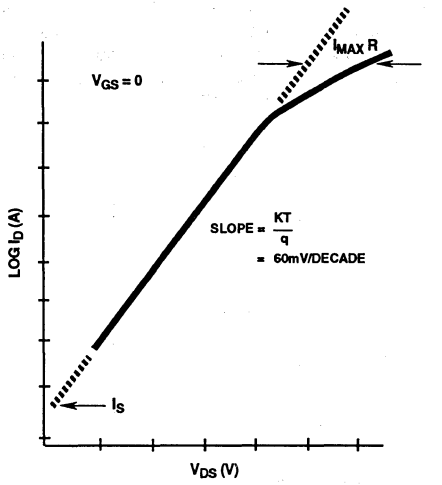

FIGURE 5. THIS PLOT OF LOG I_D VS V_{DS} IN THIRD-QUADRANT OPERATION OF THE POWER MOSFET DEFINES I_S AND R_S, OF THE PARASITIC BODY DIODE, D_{BODY}.

To properly simulate avalanche breakdown voltage with the added clamp circuit (diode D_{BREAK} and voltage source V_{break} in Figure 2), first set the voltage level of V_{BREAK} equal to the measured value of drain breakdown voltage. Then, adjust the SPICE II model parameters I_S, N, and R_S for D_{break} to obtain the best fit to the measured breakdown voltage curve.

Selection of capacitors C_{21}, C_{23}, and C_{24}, and the parameters of the JFET (all shown in Figure 2), can be made using the curves of Figure 6. This is a plot of drain and gate voltage versus time for a power MOSFET driven with constant

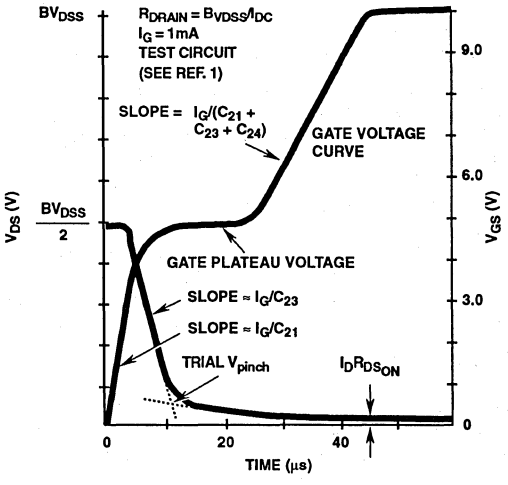

FIGURE 6. PLOTTING DRAIN AND GATE VOLTAGES OF THE POWER MOSFT VS TIME DETERMINES THE VALUES OF C_{21}, C_{23}, C_{24}, AND V_{pinch}.

gate current (I_G).[1] The initial slope of the V_{GS} curve defines C_{21} (since for any value of gate voltage, V_{GS}, less than threshold voltage, V_{TO}, the power MOSFET is in its off-state, so that the gate-to-source capacitance, C_{21}, charges linearly under constant-current conditions). As V_{TO} is reached, the low-voltage lateral MOSFET (Figure 2) turns on, and its drain voltage drops toward its minimum value.

At the outset, the JFET is operating beyond pinch-off, and the slope of the V_{DS}-versus-time curve is controlled by C_{23}. However, when the drain voltage falls below V_{PINCH}, the JFET conducts, strongly coupling C_{24} to the JFET drain and greatly reducing the drain voltage slew rate. Thus, the value of C_{23} can be approximated from the steep slope of the VDS curve in Figure 6, while the value of $C_{21}+C_{23}+C_{24}$ corresponds to the labelled V_{GS} slope. These values can be adjusted slightly to give the best slope fit. A trial value of V_{PINCH} (and V_{TO}) is given by the labelled intercept of the V_{DS} curve. Adjustments of this value will control the length of the gate plateau voltage needed to complete the curve fit.

Table I lists the preferred algorithm for parameter extraction; Table II summarizes the required empirical inputs. Together, these tables will aid in setting up the parameters for evaluation of a power MOSFET with SPICE II and the subcircuit. As an example, Table 3 summarizes the input parameters for the SPICE II model and subcircuit, determined for the Harris IRF130 power MOSFET, using the approach just described. The IRF130 is rated at 14 amperes and has a 100-volt blocking capability.

TABLE 1. PREFERRED ALGORITHM FOR PARAMETER EXTRACTION

1.	Determine K_P of lateral MOS
2.	Determine V_{TO} of lateral MOS
3.	Determine C_{21}
4.	Determine $C_{21} + C_{23} + C_{24}$
5.	Determine Rsource and JFET drain resistance
6.	Assign beta of JFET = 100 x K_P of lateral MOS
7.	Use trial V_{PINCH}
8.	Use trial C_{23} and calculate C_{24}
9.	Curve fit for slope by repeating step 8 with different values of C_{23}.
10.	Adjust V_{PINCH} and V_{TO} of JFET to fix gate-voltage plateau

TABLE 2. EMPIRICAL INPUTS

MOSFET	Enhancement mode:W = L = 1µm; K_P (Figure 3); V_{TO} (Figure 3); C's = 0; T_{OX} = 1E6µm
JFET	Depletion mode; area factor = 1; Beta = 100K_P (Figure 3); V_{TO} = -V_{pinch} (Figure 6); C's = diode lifetime = 0; diode ideality factor = 1.0; Is = 1E - 20; R_D (Figure 4)
D_{BODY}	I_S from Figure 5; Ideality Factor = 1.0; R_S from Figure 5 (must be very much smaller than R_D); C (from C_{OSS}); lifetime = best fit to T_{RR}
D_{BREAK}	I_S = arbitrary; C = lifetime = 0; ideality factor = best low-current fit; R = best high-current fit
D1	I_S = 1E - 13; C = lifetime = 0; ideality factor = 0.03; R_S = 1
R_{SOURCE}	Figure 3
L_{SOURCE}	Approx. (5L)ln(4L/d) nH; L and d are source wire inches
V_{PINCH}	Figure 6
V_{BREAK}	Avalanche voltage
C_{21}	Figure 6
C_{23}	Figure 6
C_{24}	Figure 6

TABLE 3 - INPUT PARAMETERS OF IRF130 TO SPICE MODEL

SPICE PARAMETER	HARRIS IRF130 VALUE
LATERAL MOS	
Model Level	1
T_{OX}	1E06µ
V_{TO}	3.4V
K_P	6.4A/V^2
W, L	1.0µ
VERTICAL JFET	
JMOD Area	1
V_{TO}	-6.4V
Beta	640
I_S	10^{-20}
R_D	42.15 x $10^{-3}\Omega$
D_{BODY}	
CJO	1650pF
IT	70 x 10^{-9}
I_S	3 x 10^{-12}
R_S	2.5 x $10^{-3}\Omega$
PASSIVE ELEMENTS	
C_{21}	900pF
C_{23}	40pF
C_{24}	1360pF
R_{SOURCE}	17.5 x $10^{-3}\Omega$
L_{SOURCE}	7.5 x 10^{-9}H
V_{BREAK}	117V

Implementing The Subcircuit in SPICE II

Table IV is the input listing for the implementation of the power MOSFET subcircuit in SPICE II software. Nodes are identified for drain, gate, and source of the power MOSFET. The subcircuit then "hooks" to these nodes wherever specified in the SPICE II simulation. Any number of power MOSFETs can be specified. The parameters listed are for an IRF130 power MOSFET.

The Results

The real test oftheenhanced SPICE II model is how closely its predicted performance compares with actual measurements. Using the input parameters for the Harris IRF130 device example given in Table III, we calculated transfer and output curves for the model. These curves were then compared against measured static data. Figures 7 and 8 show the precise fit between predicted and measured static data, even at low values of drain voltage.

To see how the model performs in dynamic prediction, we simulated first-quadrant operation (including avalanche mode) and third-quadrant operation for the Harris IRF130 power MOSFET. Once again, the predicted performance of the enhanced SPICE II model fits actual measurements satisfactorily over the entire operating range of the Harris IRFI30, as shown in Figures 9 and 10.

To compare calculated switching performance versus actual measurement on the Harris IRF130, we used the enhanced SPICE II model to generate switching curves. Figure11 shows drain and gate voltages versus time with a constant gate-current drive. Figure 12 shows drain and gate voltages versus time for a step gate-voltage input. Actual measured data was then taken and overlaid on the points predicted by the enhanced SPICE II model. Again, the fit was accurate in each case.

TABLE 4 - INPUT LISTING OF SUBCIRCUIT MODEL
Listed Parameters Valid for a Harris IRFI30 Power MOSFET

```
* THIS IS THE POWER MOS SUBCIRCUIT
* NODE 3 IS THE POWERMOS DRAIN
* NODE 2 IS THE POWERMOS GATE
* NODE 11 IS THE POWERMOS SOURCE
*
*
.OPTIONS NOMOD NOLIST NOACCT NONODE LIMPTS=250 GMIN=1.0E-20
.SUBCKT POWMOS 3 2 11
.C21 2 1 900P
.C23 2 3 40P
.C24 2 4 1360P
.FDSCHRG 4 2 VMEAS 1.0
.MOS1 4 2 11 MOSMOD L=1U W=1U
.JFET 3 1 4 JMOD AREA=1
.DBODY 1 3 DMOD2
.RSOURCE 1 10 17.5E-03
.LSOURCE 10 11 7.5N
.E41 5 11 4 1 1.0
.D1 5 6 DMOD
.VPINCH 6 8 DC 6.4
.VMEAS 8 11 DC 0.0
.DBREAK 3 7 DMOD3
.VBREAK 7 1 DC 117
.MODEL MOSMOD NMOS VTO=3.4 KP=6.40 TOX=1.0E+06U
.MODEL JMOD NJF VTO=-6.4 BETA=640 IS=1.0E-20 RD=42.5E-03
.MODEL DMOD D IS=1.0E-13 N=0.03 RS=1.0
.MODEL DMOD2 D CJO=1650P TT=70N IS=3.0E-12 RS=2.5E-03
.MODEL DMOD3 D IS=1E-13 RS=2.0 N=1.0
.ENDS
*
*
```

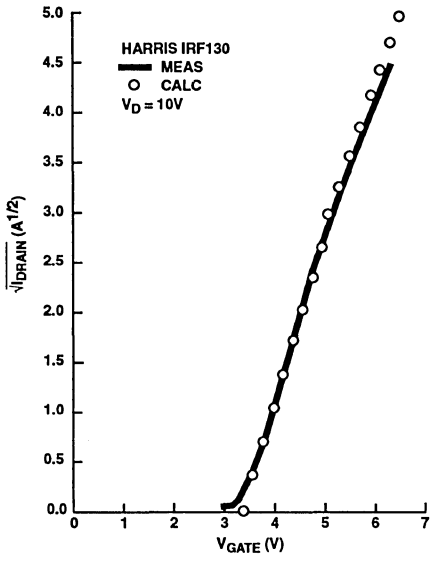

FIGURE 7. MEASURED SQUARE ROOT OF DRAIN CURRENT (DRAIN VOLTS = 10) vs. GATE VOLTAGE FOR THE HARRIS IRF130 POWER MOSFET IS PLOTTED ALONG WITH THE CALCULATED VALUES FOR THE ENHANCED SPICE II MODEL. AN EXCELLENT FIT IS OBTAINED.

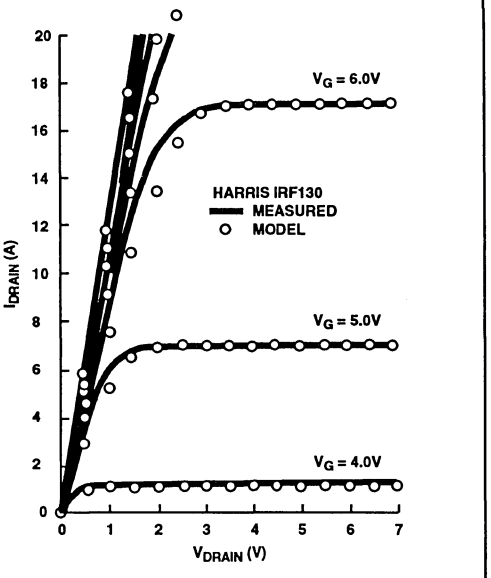

FIGURE 8. PLOTS OF DRAIN CURRENTvs. DRAIN VOLTAGE FOR THE HARRIS IRF130 POWER M0SFET SHOW AN EXCELLENT FIT BETWEEN MEASURED VALUES AND THOSE CALCULATED BY THE ENHANCED SPICE II MODEL FOR VARIOUS VALUES OF CONSTANT GATE VOLTAGE.

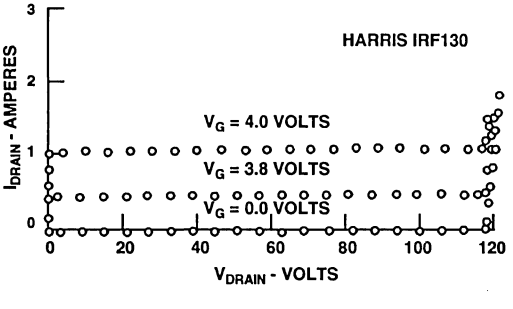

FIGURE 9. FIRST QUADRANT DRAIN CURRENT vs. DRAIN VOLTAGE WITH V_{GS} HELD CONSTANT IS CALCULATED BY THE ENHANCED SPICE II MODEL OF THE HARRIS IRF130 POWER M0SFET. NOTE THAT THE MODEL PREDICTS AVALANCHE BREAKDOWN.

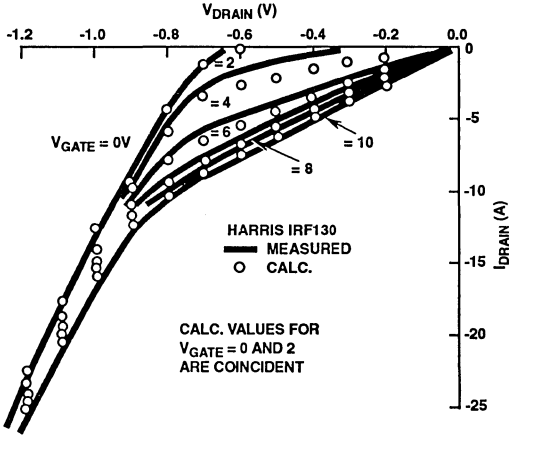

FIGURE 10. THIRD-QUADRANT OPERATION OF THE HARRIS IRF130 SHOWS AGREEMENT BETWEEN THE PREDICTED VALUES OF THE ENHANCED SPICE II MODEL AND ACTUAL MEASURED VALUED OF DRAIN CURRENT vs DRAIN VOLTAGE AT DIFFERENT VALUED OF CONSTANT GATE VOLTAGE.

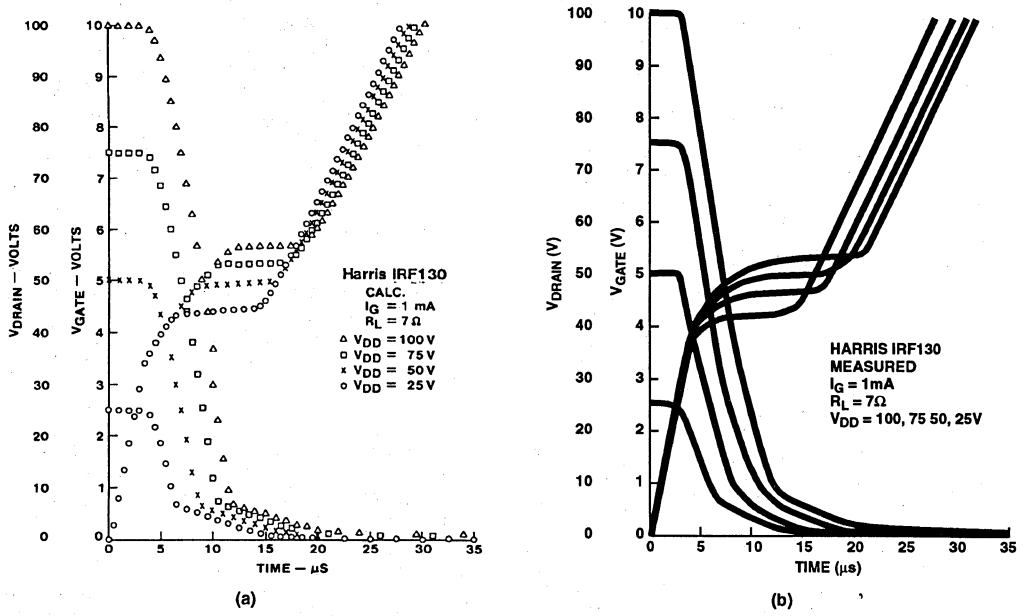

FIGURE 11. THESE PLOTS OF DRAIN AND GATE VOLTAGES vs. TIME FOR CONSTANT GATE CURRENT SHOW AGREEMENT BETWEEN THE PREDICTIONS OF THE ENHANCED SPICE II MODEL (a) AND MEASURED PERFORMANCE OF THE HARRIS IRF130 POWER MOSFET (b).

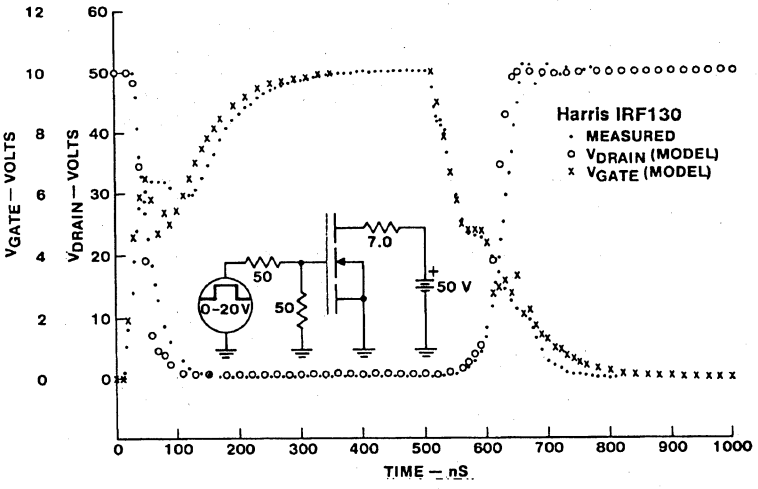

FIGURE 12. SWITCHING PERFORMANCE OF THE HARRIS IRF130 POWER MOSFET IS CLOSELY PREDICTED BY THE ENHANCED SPICE II MODEL IN THIS PLOT OF MEASURED AND CALCULATED VALUES OF DRAIN AND GATE VOLTAGES vs. TIME IN A STANDARD SWITCHING CIRCUIT.

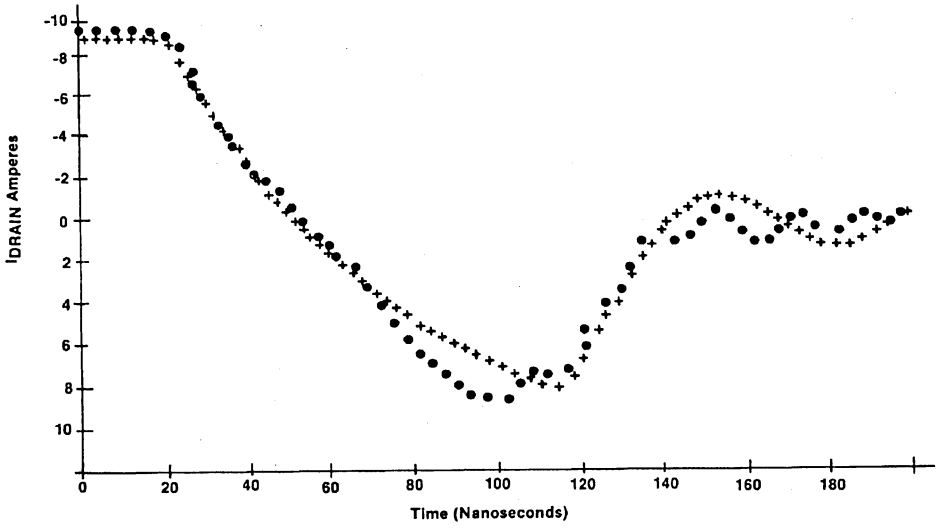

FIGURE 13. THE CALCULATED THIRD-QUADRANT DIODE RECOVERY WAVEFORM OF THE ENHANCE SPICE II MODEL SHOWS GOOD AGREEMENT WITH THAT ACTUALLY MEASURED FOR THE HARRIS IRF130 POWER MOSFET

Finally, the enhanced model was used to compare calculated and measured body diode (D_{BODY} in Figure 2) recovery time curves in third-quadrant operation of the Harris power MOSFET. Figure 13 shows the good agreement between predicted and actual results.

This approach provides excellent results when there is a need to model the performance of a power MOSFET. Not only will the approach update SPICE II (or other circuit simulation CAD program) so that it will simulate the latest state-of-the-art in MOS power, but it will allow quick analysis of every static and dynamic characteristic for suitability in a proposed design.

References

1. Wheatley, Jr., C.F. and Ronan Jr., H.R., "Switching Waveforms of the L^2FET: A 5-Volt Gate Drive Power MOSFET," Power Electronic Specialist Conference Record, June 1984, p. 238.
2. Ronan Jr., H.R. and Wheatley Jr., C.F., "Power MOSFET Switching Waveforms: A New Insight," Proceedings of Powercon 11, April 1984, p. C3.
3. Niehaus, H.A., Bowers, J.C. and Herren Jr., P.C., "A High Power MOSFET Computer Model," Power Conversion International, January 1982, p. 65.

Harris Semiconductor

APPNOTE

No. 8614 May 1992

Harris Intelligent Power

THE CA1523 VARIABLE INTERVAL PULSE REGULATOR (VIPUR) FOR SWITCH MODE POWER SUPPLIES

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The CA1523, Variable Interval, Pulse Interval Regulator (VIPUR) is a monolithic integrated circuit designed for use in switch mode power supply (SMPS) systems. The advantages of both pulse interval modulation (PIM) and pulse width modulation (PWM) are combined in the VIPUR circuit. Figure 1 shows the block diagram and external circuit used in a typical CA1523 switching regulator circuit.

The special features of the CA1523, including a slow-start controlled power-up and mode sensitive logic control of the output pulse, provide several advantages in power supply applications. Intrinsic controls for adjustment of the pulse and frequency modulation range allow easy use of the CA1523 in a variety of SMPS systems, but especially those where line isolation is required.

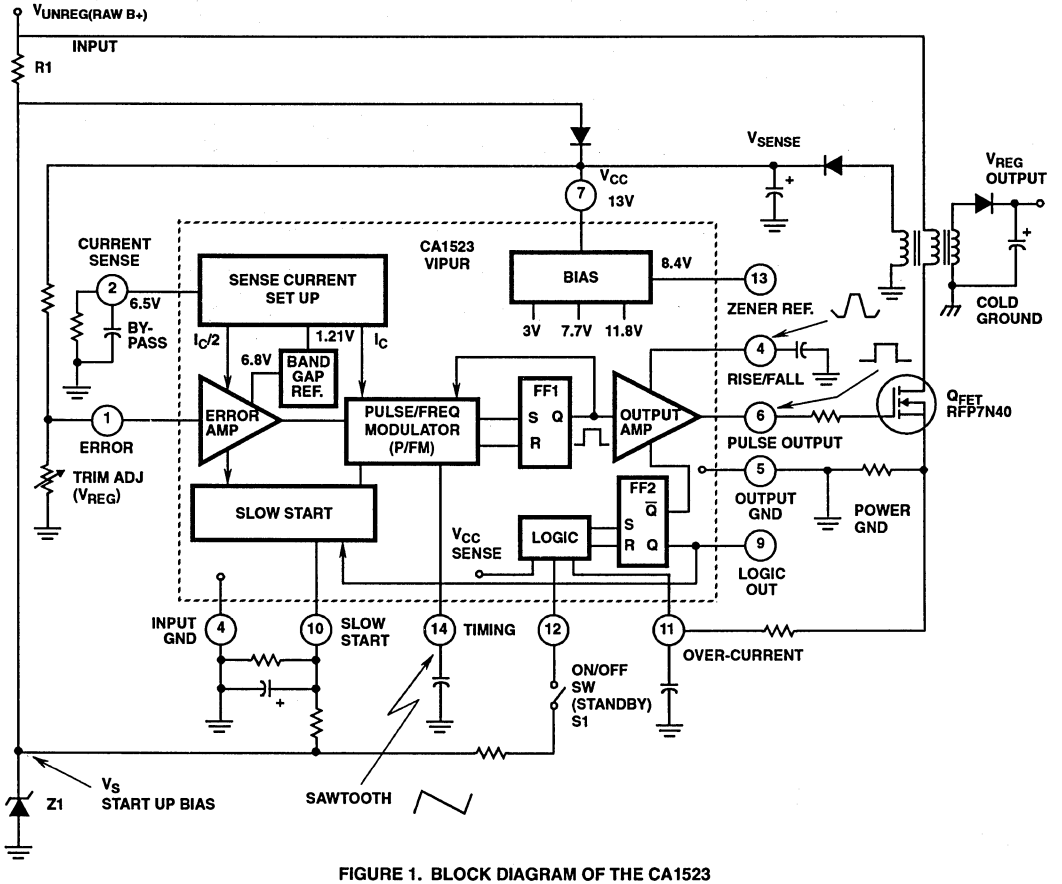
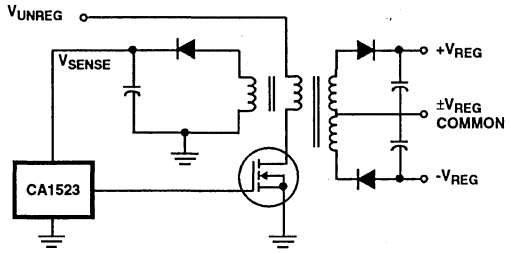
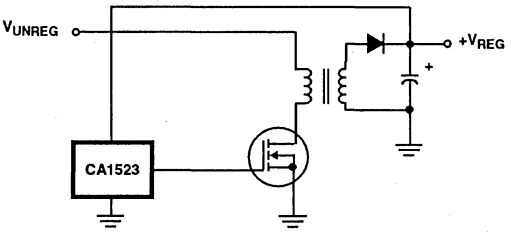


FIGURE 1. BLOCK DIAGRAM OF THE CA1523

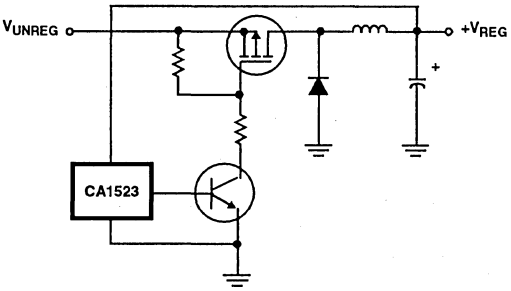
Systems that require line-isolated power supply voltages may be powered with the CA1523 regulator in a transformer flyback-converter system like the one shown in Figure 2(a). This system is particularly useful in meeting rigid safety standards when interfacing between workstation equipment or modular consumer audio and video instruments is required. Less stringent interface requirements may permit the use of regulators with a common ground for both the switching controller and power supply outputs; examples of these regulators are the flyback converter of Figure 2(b) or the buck converter regulator of Figure 2(c). However, the application of most interest is the line isolated type shown in Figure 2(a).



a) Line Isolated Flyback Converter



b) Non-Isolated Flyback Converter



c) Buck Converter Regulator

FIGURE 2. THE CA1523 IN SWITCH MODE POWER SUPPLY SYSTEMS

The PWM system is a popular mode of control in switching power supplies, as noted in the wide use of the CA1524. The counterpart of this mode of control, the PM system, was used extensively in the early period of switching power supply development. Both methods of control have their advantages and disadvantages. PWM offers effective control over a wide range of power supply loads. However, at the lower end of the load range, the PWM becomes limited because of the minimum pulse width, T_{ON}, required. In addition, the rise and fall time of the drive pulse of the power switching transistor must be slowed down to meet RFI and EMI requirements. On the other hand, the PIM can handle low loads better because the duty cycle is reduced by increasing the pulse interval. However, the low range of the operating frequency may cause filtering-related problems in audio or other sensitive instruments. Another problem with PIM at the low-frequency end is the related conversion losses.

The CA1523 is primarily a PIM controller with built-in PWM correction over a 2-to-1 pulse width range. For a frequency f and an associated period T, the pulse width reduces from a maximum width of T/2 (50% duty cycle), corresponding to the highest frequency at the maximum load limit, and approaches T/4 at the lowest frequency and minimum load.

The combination of both PIM and PWM control effectively compresses the operating frequency range over that of a pure PIM control for a given range of load. The combined CA1523 VIPUR advantages at minimum frequency include reduced losses and low ripple with improved efficiency and regulation. Pulse-width correction done simultaneously with pulse-interval correction produces an inherent gain magnitude of approximately 2 at 50% duty cycle under high-load conditions. This feature helps in keeping the error-amplifier gain low, and improves stability without the addition of expensive external components.

Features of the CA1523

As shown in Figure 1, the output drive pulse of the CA1523 is modulated and mode-controlled by several system features:

1. The output drive pulse has a maximum continuous ±50mA capability into an 1800pF load.
2. The peak transient load is +300mA and -200mA for a maximum of 1µs.
3. The maximum pulse width can be controlled by choice of the timing capacitance at pin 14 and the current-sense resistance at pin 2.
4. The output-pulse rise and fall time can be controlled by choice of the rise/fall-time capacitor at pin 4.
5. The slow-start threshold of the pulse output is controlled by choice of the resistance at pin 2.
6. The output-pulse interval is rate controlled during power-up by the slow-start RC-charge time constant at pin 10.
7. Maximum output frequency is in excess of 200kHz, and is user controlled.

8. Output pulse interval and width corrections are maintained by the error voltage feedback to pin 1.
9. The standby on/off switch between pins 7 (V_{CC}) and 12 controls the output pulse. As an option, the on/off function may be controlled by logic-level switching at pin 12 or by line-isolated switching using an optical coupler.
10. Overcurrent shutdown may be controlled by using a sense resistor in the load circuit to shut down the output drive pulse.

Other features of the CA1523 include:

1. A substantial level of ESD (electrostatic discharge) protection designed into the interfacing pin terminals of the chip.
2. An 8.4V internal zener voltage reference for the on-chip bias circuits.
3. A 1.21V bandgap that provides a stable voltage reference for bias to the timing circuit and error amplifier.
4. NOR logic control of shutdown of the output pulse under fault conditions for low V_{CC}, on/off, and overcurrent. Pin 9 is a monitor or output indicator of a fault condition.
5. Availability in an economical 14 pin DIP package.

Control Structure Of The CA1523

The CA1523 has five primary circuit functions:

1. Error amplification
2. Pulse/frequency modulation
3. Pulse driver/output amplification
4. Slow-start power-up control
5. System logic control

The block diagram of Figure 1 shows the interrelated functions of the circuit. When the system raw B+ is switched on, the slow-start function controls the pulse/frequency modulator, P/FM, until the voltage at pin 10 is greater than 7V.

Standby conditions then exist until switch S1 is closed. In the standby mode, the P/FM maintains a maximum frequency output with a 50% duty cycle. After switch S1 is turned on, the output amplifier is enabled and the P/FM response is a function of the error voltage at pin 1. The error amplifier accepts error-correction inputs and controls the pulse and frequency modulation. The P/FM output pulse is then amplified in the driver and output stage.

Figure 3 shows the timing-circuit schematic of the CA1523. For a given timing capacitance, C_T, the maximum frequency of the P/FM circuit is determined by the current-sense bias at pin 2. The current-sense level, I_S, is set by the fixed resistor at pin 2, R_S, which goes to ground. A resistor divider reference at the base of Q92 of differential amplifier Q91, Q92, is approximately $V_{CC}/2$. The differential amplifier feeds back, via Q17C, any error in the balance of Q91 and Q92, while holding the pin 2 voltage at the $V_{CC}/2$ reference level. The differential emitter current is supplied by Q93, and is determined by the bandgap bias voltage of 1.21V at the base of Q93.

The differential emitter current is approximately equal to the collector current of Q17C; the collector currents of Q17A and Q17B are current mirrors to the collector current of Q17C. The currents $I_C/2$ and I_C provide the P/FM charge and discharge timing, and are, respectively, the collector currents of Q17A and Q17B. The current ratio is $^1/_2$-to-1 to accommodate a 50% duty cycle at maximum frequency and load conditions. When start-up conditions exist, and the pin 1 error voltage is low, Q6 passes all of the $I_C/2$ current to Q11. Since Q11 and Q18 are current mirrors, the collector of Q18 discharges the timing capacitor, C_T, at pin 14. The state of the flip-flop, FF1, determines whether Q15 will conduct current I_C from Q17B into the timing capacitor.

When Q18 is discharging current from C_T at an $I_C/2$ rate, and Q15 is charging C_T at an I_C rate, the net charge current is $I_C/2$. This is an FF1 high state for the Q output, and Q16 is cut off while Q15 is conducting current I_C. The positive voltage ramp at pin 14 increases until the V_h comparator toggles at the 5V reference to the inverting input, resetting FF1, with the Q output going low. When Q is low, Q15 is cut off, and no charge current passes to C_T. Timing capacitor C_T is then discharged by Q18 at a maximum rate of $I_C/2$. The discharge ramp continues until the voltage at pin 14 reaches 2.5V, when the V_l comparator toggles the S input of FF1 to a high state. The cycle of charge/discharge to timing capacitor C_T is complete when the Q output of FF1 goes high in response to the high at the S input.

The above operation occurs when the error voltage is lower than the 6.8V differential input reference, a condition that allows the full $I_C/2$ discharge of C_T by the Q11 and Q18 current mirror. After being turned on from the line power source, the slow-start function shunts Q6 collector current through Q2. As a result, the Q11,Ql8 current mirror initially receives little or no forward bias current, and C_T cannot be discharged. As the slow-start voltage increases, the current in Q2 decreases, allowing Q11 and Q18 to discharge C_T at an increasing rate. As long as the error voltage at pin 1 remains below the 6.8V reference level, the charge and discharge rate is at the 50% duty cycle condition.

In reference to the slow-start circuit of Figure 3, an increase of the slow-start bias on capacitor C2 at start-up exercises a decreasing degree of control over the discharge timing. If the current-sense adjustment at pin 2 is typically less than 100μA, there will be a full frequency range of slow-start control, and the range of increasing pulse width will be 2 to 1. Higher pin 2 bias currents will reduce the range of frequency control. The input to pin 10 drives the base of p-n-p transistor Q34. A 30kΩ emitter resistor, R22, is returned from Q34 to an internal 7.7V bias source. Transistors Q1 and Q2 mirror the Q34 collector current and shunt the Q6 collector current away from Q11, reducing the discharge current in the timing control circuit. As an example, with 4V at pin 10, there are approximately 3V across emitter resistor R22. This arrangement allows the discharge current to be controlled over a range of 100μA. A bias resistor in the range of 56kΩ to 68kΩ between pin 2 and ground is suggested for a full range of slow-start control. Higher levels of pin 2 sense current increase the $I_C/2$ current beyond the full range of the slow-start bias control at pin 10.

When a power-on condition has been established, slow-start completed, and S1 switched on, the CA1523 begins normal regulation through error-voltage control as follows. When S1 is switched on, maximum energy conversion occurs in the switched transformer. The supply voltage approaches normal regulation level, and the error voltage increases toward the 6.8V reference level. The error voltage is set by a resistive divider ratio determined from the rectified voltage of the transformer sense winding. The Q5, Q6, Q7, and Q8 differential controls the Q6 current to the Q11, Q18 current mirror, decreasing Q6 current as the error voltage increases. A portion of the $I_C/2$ current from Q17A is passed by Q6. This current controls the P/FM output pulse and maintains regulation at the desired level, as determined by adjustment of the divider at pin 1. Pulse output continues from FF1 during regulation, but at a reduced rate and with reduced pulse width. The Q output of FF1 is always high during the positive ramp at pin 14, a condition of maximum charge current to C_T. At minimum load, the pin 1 voltage increases, and the net charge current for the positive ramp is higher because Q18 is discharging less current. For example, if the error voltage at pin 1 is forcing half of the $I_C/2$ current to Q7, the Q6 current is $I_C/4$, and the net positive ramp charge current at pin 14 is:

$$I_C - I_C/4 = 3I_C/4$$

The net negative-ramp discharge current is then $I_C/4$. What had been a maximum charge and discharge rate of $I_C/2$ at start-up is now pulse-interval and pulse-width modulated to provide a 3 to 1 charge/discharge ratio.

To generalize, we can establish the range of error correction by assigning a k factor to the decimal portion of the Q17A collector current that is shifted from Q6 to Q7. Let k = 0 when V_1 (pin 1 voltage) is low and all Q17A current ($I_C/2$) flows through Q6 to discharge pin 14. k = I when all Q17A current is shifted to Q7 and there is no discharge current to pin 14. The maximum rate of charge and discharge is established by the sense current, I_S at pin 2; I_S is approximately $I_C/2$.

Since:

$$v = (1/C) \times \int i dt$$

For a constant rate of charge (or discharge) current:

$$V_h - V_l = I_{charge} \text{ (or } I_{discharge}) \times (t_2 - t_1)/C.$$

And:

$$T_{ON(MAX)} = (V_h - V_l)C_T/I_S.$$

From Figure 3, the range of (V_h - V_l) is approximately (5.0 - 2.5), or 2.5V, and I_S is approximately equal to $V_{CC}/2$ divided by R_S.

The above information is used to establish the pulse interval or system frequency. The frequency is the reciprocal of T_{ON}(charge) plus T_{OFF}(discharge). As V_1 increases, k increases. The positive ramp charge current to pin 14 and C_T is:

$$I_{charge} = I_C - (I_C/2)(1 - k) = 2I_S - I_S(1 - k) = I_S(1 + k).$$

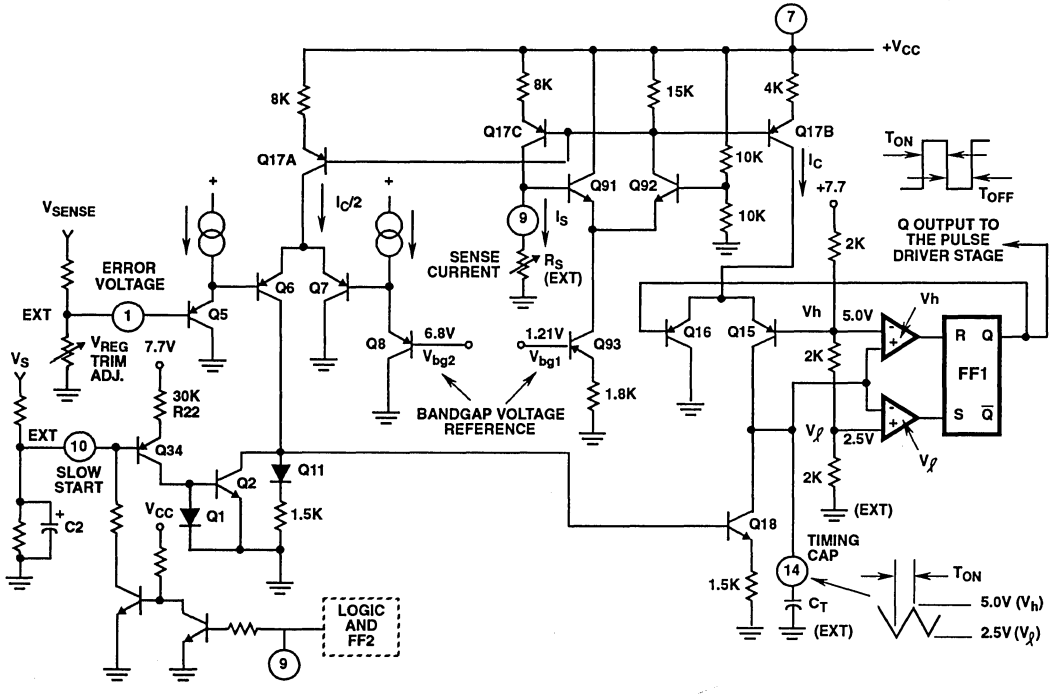


FIGURE 3. PULSE/FREQUENCY MODULATION AND TIMING CIRCUIT FOR THE CA1523

Since I_C is cut off during discharge:

$I_{discharge} = I_S(I - k)$

Therefore, during charge:

$T_{ON} = [(V_h - V_I)C_T]/[I_S(1 + k)] = T_{ON}(max)/(1 + k)$

and, during discharge:

$T_{OFF} = [(V_h - V_I)C_T]/[I_S(1 - k)] = T_{ON}(max)/(1 - k)$

Note that T_{ON} approaches $T_{ON}(max)/2$ as k approaches 1. This is the condition of minimum power supply load. With the time conditions for T_{ON} and T_{OFF} established, the frequency, f, can be defined as:

$f = 1/(T_{ON} + T_{OFF}) = (1 - k^2)/2T_{ON}(Max)$

Since the maximum frequency occurs at k = 0:

$f_{MAX} = 1/2T_{ON}(Max)$ and

$f = f_{MAX}(1 - k^2) = (1 - k^2)/2T_{ON}(Max)$.

The duty cycle is $T_{ON}/(T_{ON} + T_{OFF})$ which, by substitution, is:

$D = (1 - k)/2$

Since k is the current split ratio of the input differential amplifier, the differential equation applies, that is:

$k \equiv 1/(1 + e^{\Delta V/h})$

where e is the natural log value of 2.718, h is KT/q (≅26mV), and ΔV is V_1-V_{REF}. The equation for k is approximate, but provides a reasonably accurate transfer function for the CA1523 when output pulse width, frequency, and duty cycle may be calculated for given values of (V_1 - V_{REF}).

As k goes to 1, the frequency goes to zero, implying a no-load condition on the power supply. This is an improbable condition; however, the lowest system frequency is always determined by the minimum power supply load.

The timing circuit of the VIPUR is a stand-alone pulse generator in which the Q output of FF1 is amplified by the driver output circuit of Figure 4, subject to the logic control of transistor Q33 and the proper logic-state control for the slow start (SST), ON, V_{CC}, and overcurrent (OC) inputs shown in Figure 5.

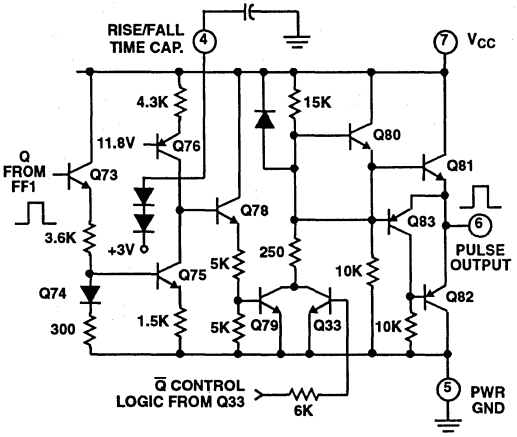


FIGURE 4. CA1523 DRIVER AND OUTPUT STAGE

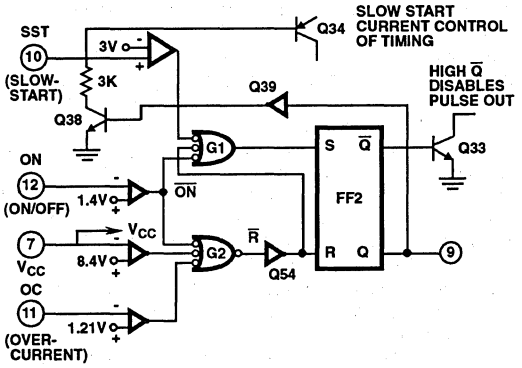


FIGURE 5. CA1523 LOGIC CONTROL DIAGRAM

The test circuit of Figure 6 demonstrates the pin 2 current sense (I_S) range using timing capacitance values of 100pF, 240pF, and 470pF. Figure 7 shows the frequency versus I_S current at pin 2. Figures 8 and 9 show the range of pin 6 pulse width and duty cycle. Since the curves of Figures 7, 8, and 9 were determined with V_1 at approximately 5.9V (much less than the 6.8V reference) maximum frequency conditions apply to all Figure 6 curves. With the rise/fall-time capacitance of 68pF at pin 4, the rise/fall delay will affect the duty cycle when the frequency is greater than 120kHz. Removing the pin 4 capacitance will extend the maximum frequency to well above 200kHz. However, use of the rise/fall-time delay function is important to the control of EMI and RFI. The optimum rise/fall capacitance value is chosen to assure a 50% duty cycle at the maximum frequency with a reasonable margin in design tolerance and, for the system requirements, to ensure compliance with EMI and RFI requirements.

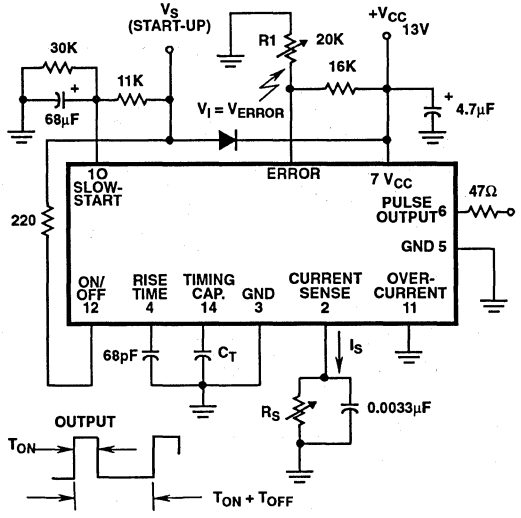


FIGURE 6. VARIABLE-INTERVAL SWITCHING-REGULATOR TEST CIRCUIT USED TO OBTAIN TIMING CURVES OF FIGURES 7, 8, AND 9

Where there are no external system restrictions on the operation of the CA1523, and the function is that of a pulse generator, very large values of capacitance may be used at pin 14 to achieve very low pulse frequencies. External resistor loading at pin 14 will contribute a nonlinear slope to the otherwise linear sawtooth there. This nonlinear contribution can also be noted in the waveform at pin 14 if the timing capacitor has less than 10MΩ leakage. Very low values of I_S are not recommended because the balance of charge and discharge currents is, to some degree, affected by base bias and junction leakage currents. As noted by the degradation of duty cycle balance in Figure 9, and for practical reasons, I_S should be greater than 20μA. The upper limit for I_S is determined by the maximum available collector current from Q17C, which is typically 350μA.

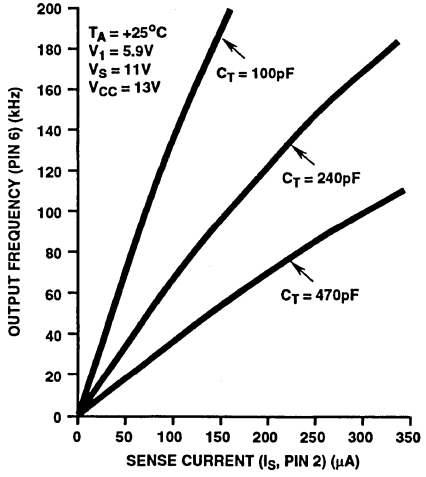


FIGURE 7. PULSE/FREQUENCY MODULATOR CHARACTERISTIC OF FREQUENCY vs. TIMING CAPACITOR C_T AND SENSE CURRENT I_S (T_A = +25°C, V_1 =5.9V, V_5 = 11V, V_{CC}= 13V.)

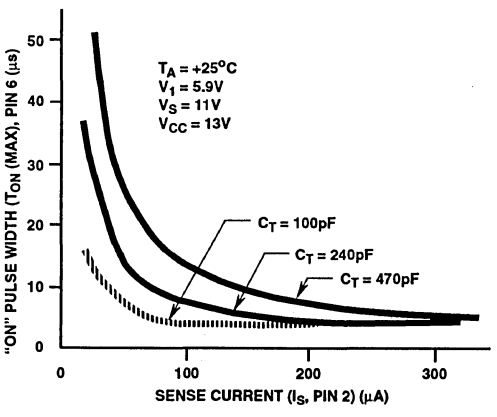


FIGURE 8. PULSE/FREQUENCY MODULATOR CHARACTERISTIC T_{ON}(MAX) OUTPUT PULSE WIDTH (PIN 6) vs. CURRENT SENSE (PIN 2). (T_A = 25°C, V_1 = 5.9V, V_5 = 11V, V_{CC} = 13V.)

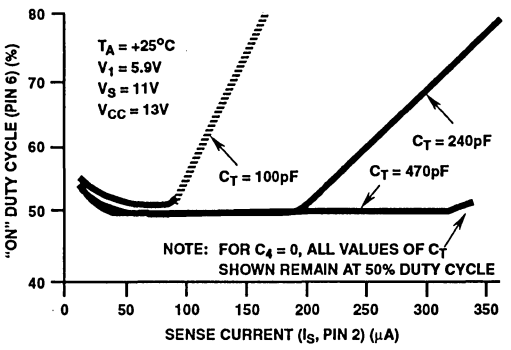


FIGURE 9. PULSE/FREQUENCY MODULATOR CHARACTERISTIC "ON" DUTY CYCLE (PIN 6) vs. CURRENT SENSE (PIN 2).

CA1523 Generated Waveforms And Delays

The signal waveforms of the CA1523 are shown in Figure 10, and are based on the test circuit of Figure 6, where R_S is adjusted fora maximum frequency of 100kHz. Because the sink and source current drivers of the timing capacitor, C_T, are constant current generators, the waveform at pin 14 is a very linear sawtooth. As noted in Figure 4, the waveform at pin 4 is derived from the Q75 sink and Q76 source drive currents, but is normally clipped at the top and bottom. The positive tip of the pin 4 signal is set by a positive clamp from two series diodes to an internal 3V bias source, providing a clamp level of approximately 4.5V. The bottom, or negative, truncation is the result of a current sink depletion of the charge on the rise/fall-time capacitor at pin 4. The degree of waveform clipping is determined by the maximum operating frequency and the value of the rise/fall time capacitor at pin 4.

In Figure 4, the rise, delay, and fall times of the input drive signal, Q, are controlled by the capacitance at pin 4, amplified, and output at pin 6. The Q input, a square wave output pulse from the timing generator (Figure 3), drives the rise/fall capacitor via the Q73 buffer and the Q74, Q75 current mirror. Rise time is determined by the Q76 constant current source. As such, the sink and source currents control the voltage at pin 4. Capacitance loading at pin 4 provides a controlled rise and fall delay time. With the 68pF capacitance shown in Figure 6, plus 10.5pF probe capacitance, the waveforms are as shown in Figure 10. A rise-time delay of 1.6μs is noted at the 2.1V point on the pin 4 waveform. The signal at pin 4 drives the base of Q78 and, through a resistor divider, Q79. Approximately 2.1V is required at pin 4 to switch Q79 and set the delay, which can be calculated from the rise time equation for constant currents. The source current from Q76 is approximately 100μA, and the delay, T_d, is:

$$T_d = VC/I = [(2.1V)(68 + 10.5pF)]/(100\mu A) = 1.6\mu s$$

If the rise time capacitor at pin 4 is too large, the peak voltage will be reduced below the positive clamp level. This condition will cause the on-time duty cycle at pin 6 to be increased. The rise ti me capacitor at pin 4 must be adjusted to restore the duty cycle to 50% at the maximum frequency

condition. When no external capacitor is used at pin 4, maximum operating frequencies in excess of 300kHz are possible. An example of the typical CA1523 pulse output capability at high frequency conditions is provided below.

Using the circuit conditions of Figure 6 with no pin 4 capacitor, I_S = 160µA, and C_T = 50pF, the pin 6 output pulse is:

$$t_r = 250ns$$

$$f_{(MAX)} = 312kHz$$

$$T_{ON}(Max) = 1.6\mu s$$

$$T_{ON}(Min) = 0.8\mu s$$

Additional delay in the pin 6 output drive pulse may result from the conditions of loading. The normal specifications for the CA1523 are given for a 68pF rise/fall-time capacitance at pin 4 and an 1800pF output capacitance loading to reflect typical drive requirements for a power-FET switch transistor. The rise and fall times for 1.8V and 10V thresholds at the V6 output are typically t_r = 600ns and t_f = 200ns.

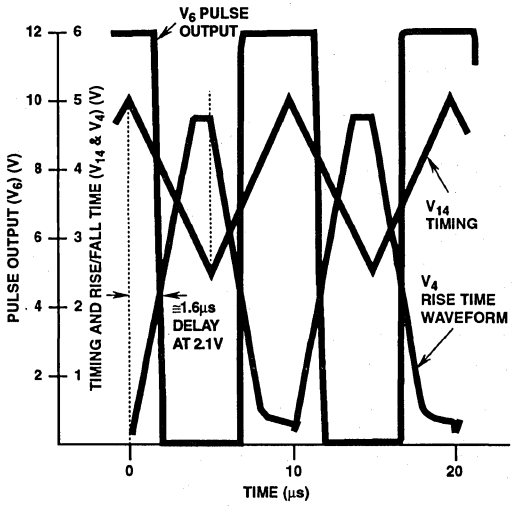


FIGURE 10. SIGNAL WAVEFORMS OF THE CIRCUIT OF FIGURE 4 (WITH 10.5pF TEST-PROBE LOADING). (C_T = 240pF, R_S APPROXIMATELY 39kΩ, $F_{(MAX)}$ = 200kHz.)

Application Circuits

TV Monitor Flyback Converter

Figure 11 shows a typical television receiver application of the CA1523. Line isolation permits use of the TV receiver as an RGB or composite-video DC-coupled monitor. In this system, the switching transformer isolates the power line from the signal circuits of the TV receiver. As shown in the block diagram of Figure 11, 120V_{AC} is connected through a fuse to the bridge rectifier and a step-down transformer, T2. The rectified output of the step-down transformer is used as a 16V standby power supply for the TV control module. The control module, in response to the user input control, switches Q2 on and off to control turn-on of the VIPUR regulator through the optoisolator. The bridge rectifier supplies a +150V raw B+ to the VIPUR start-up circuit and to the primary of the switching transformer, T1. After start-up, the run supply provides a regulated +V_{CC} for the CA1523 from the sense feedback circuit. In normal regulation, the VIPUR drives the Q1 power MOSFET, which switches the primary of T1. T1 converts regulated power to the cold 20V, 25V, and 50V levels required for the power supply outputs and the run-supply circuit.

Figure 12 explains the on/off operation of the switching power-supply portion of the converter application. The logic function maintains control of the on/off operation of the system. In the off state, the system remains in a standby mode as long as the 120V_{AC} is connected. Standby power is supplied via the start-up circuit, which consists of R2 and the 11V zener diode CR3. Continuous start-up bias is supplied to the +V_{CC} function at pin 7, the on/off input at pin 12 via the optoisolator, and the slow-start circuit at pin 10. The 11V source is connected to the pin 7 +V_{CC} function via the forward biased diode, CRI3. The logic function inputs (as previously noted in Figure 5) are the B+ sense from pin 7, the slow-start function at pin 10, the on/off function at pin 12, and the overcurrent function at pin 11. The logic function responds to a voltage level for each input and, if the voltage range of a required input is not met, shuts down the output amplifier, so that no pulses appear at pin 6. After start-up, normal operation is resumed when the on/off input is greater than 2.5V, the peak overcurrent input is less than 1.2V, and the B+ sense has determined that +V_{CC} is greater than 8.4V. The slow-start function controls the gradual start-up of the pulse and frequency modulation functions such that a slow RC rise time at pin 10 is synonymous with a slow decrease of the pulse interval. As the pin 10 voltage increases, the slow-start allows a gradual increase of the $I_C/2$ discharge current. As the voltage at pin 10 increases from 3V to 7V, the full range of slow-start control over the P/FM changes from zero to maximum frequency. The RC time constant consisting of R1, C7, and R3 controls the slow-rise voltage at pin 10. The slow increase controls the power-up rate and limits the start-up dissipation in power MOSFET Q1.

The on/off function could be controlled by an insulated manual switch or a relay. However, the optoisolator has the advantage in that it can be remotely controlled with low standby power. The overcurrent shutdown voltage is sampled from the source terminal of the power MOSFET, Q1, to assure that peak currents in the transformer primary circuit will be fault-mode limited. When start-up is complete, the run B+ is greater than the start-up supply voltage from the 11V zener diode, and CR13 is reverse biased. The on/off and slow-start input circuits remain under the control of the 11V start-up source, but the VIPUR power supply is transferred to the well-regulated run B+ supply derived from the sense winding of the transformer.

Figure 13 shows the VIPUR switching-regulator output operation as it functions in a normal feedback mode. As explained above, the error amplifier at pin 1 is differentially compared to a 6.8V internal reference. The error amplifier supplies the correction signal for the P/FM. Pulse and frequency modulation is

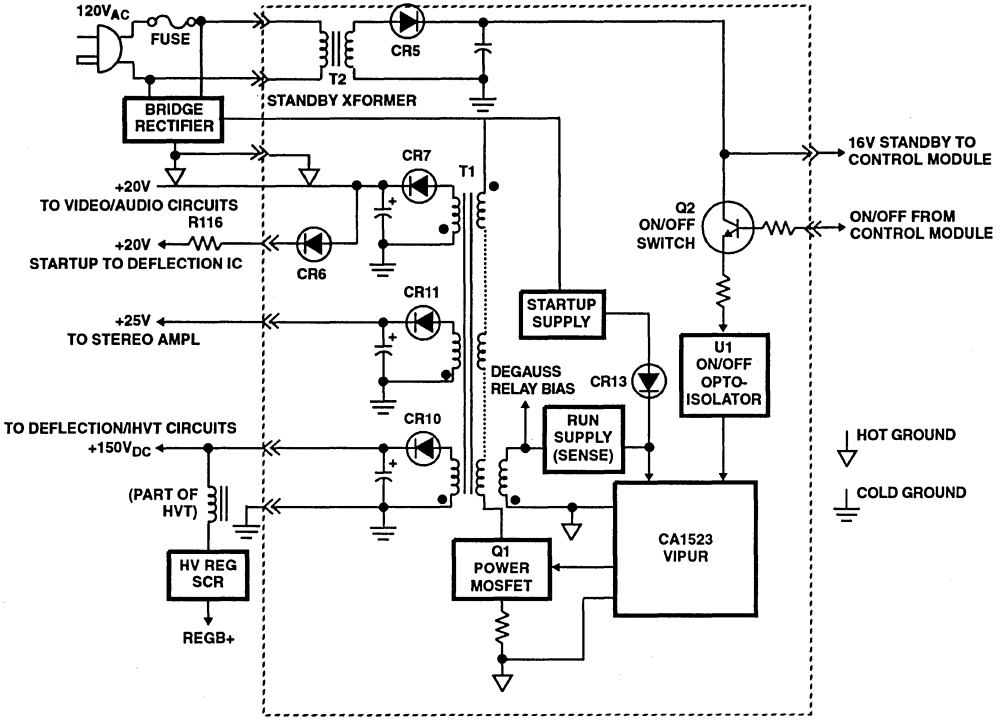


FIGURE 11. GENERAL TV MONITOR APPLICATION OF THE CA1523

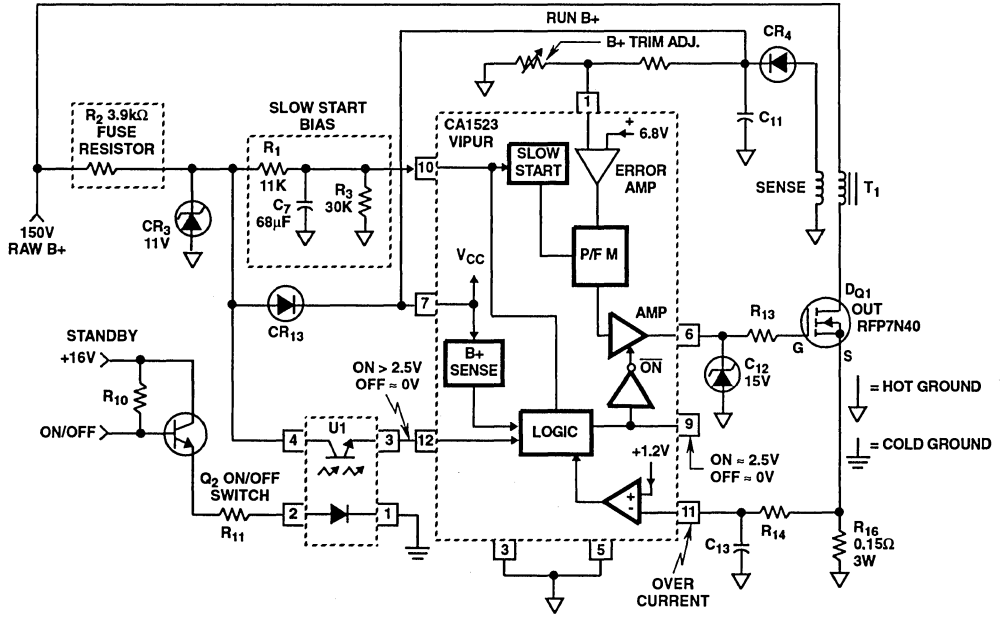


FIGURE 12. SWITCHING POWER SUPPLY ON/OFF OPERATION

controlled by timing-capacitor C15 and sense-current resistor R9. The output amplifier is controlled by the logic input; its rise time is controlled by capacitor C14. Zener-diode CR12 and resistor R13 are used to protect the gate of power MOSFET Q1. As Q1 switches the raw B+ current through the primary of the ferrite transformer, T1, power is supplied to the output windings and the sense winding. The pulse in the sense winding is rectified, and supplies run power to the CA1523 and error feedback to pin 1 through the resistor divider. The ratio of resistor R8 to the parallel trim resistors R4, R5, R6 and R7 sets the output voltage of the CA1523. The required output voltage of the regulator is determined by clipping resistors from the PC board.

A limited-range potentiometer adjustment may be used to control the regulator output, but this approach can be potentially dangerous if the high voltage of the CRT is not limited in some way. The fixed resistor-divider network is preferred for safety reasons. Because of the tight coupling of the transformer windings, the sense winding reflects the input-voltage changes and output-loading conditions. The preferred run B+ is 12V to 13V. The product of the resistor-divider ratio and the run B+ voltage should be, typically, 6.8V. When working with direct AC line power supplies, an isolation transformer must be used for hot AC line protection. Figure 14 joins together the circuits referenced in Figures 11, 12, and 13. The parts of the circuit connected to the "hot" line are identified at the center of the schematic. In addition to the circuitry discussed above, Figure 14 shows various chokes, bypass capacitors, and ferrite beads used in conjunction with the diode-rectifier filtering. These components are normally required to improve filtering and to reduce EMI and RFI.

CA1523 Buck Converter Switching Regulator

Figure 15 is the circuit schematic of a buck-type regulator useful in lower-voltage applications with a nominal raw B+ of 28V and an input tolerance range of 18V to 38V. This circuit has been chosen to illustrate some of the special capabilities of the VIPUR circuit; but, for the most part, these features are applicable to any other circuit controlled by the CA1523. The circuit of Figure 15 has special start-up features that minimize standby current in zener diode Z1 and make use of the internal zener diode for slow-start control. As shown, the error feedback voltage has been made adjustable over a typical range of 6.8V to 13.5V. The pulse frequency range is typically 25kHz to 75kHz, and the regulation at a nominal 12V output is typically 0.3%.

This circuit normally requires an output transformer only when it is desirable to isolate the output from the input. The pulse output of the CA1523 is inverted in a 2N2102 and used to drive an RFP8P10 p-channel enhancement mode power FET. The power FET is driven by the 2N2102 through a resistive divider that limits the maximum source-to-gate voltage. In the drain circuit of the power-FET output there is a shunt RUR-820 fast-switching catch diode followed by a filtering circuit comprising a 0.5mH choke and a 470µF capacitor.

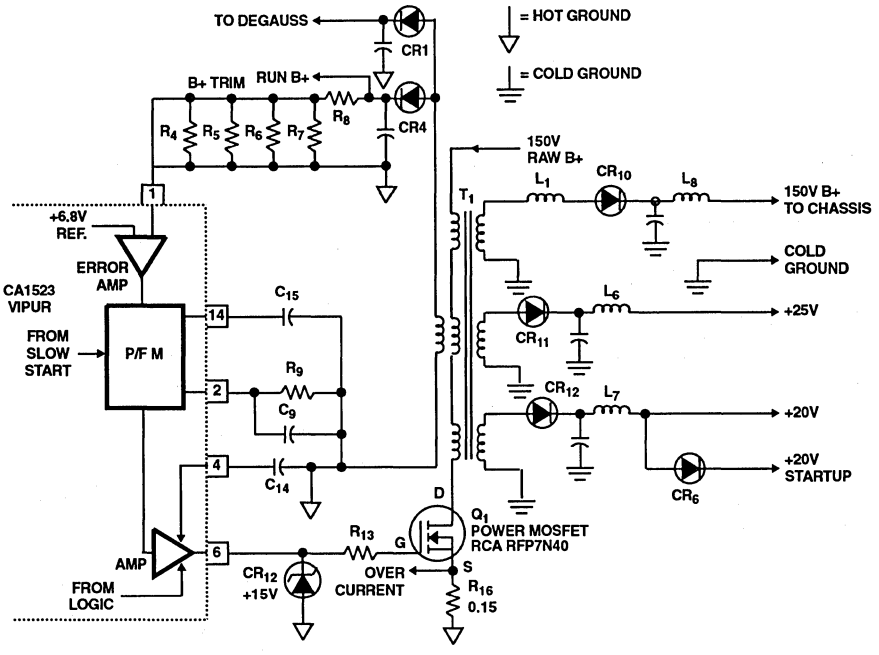


FIGURE 13. SWITCHING REGULATOR OUTPUT OPERATION

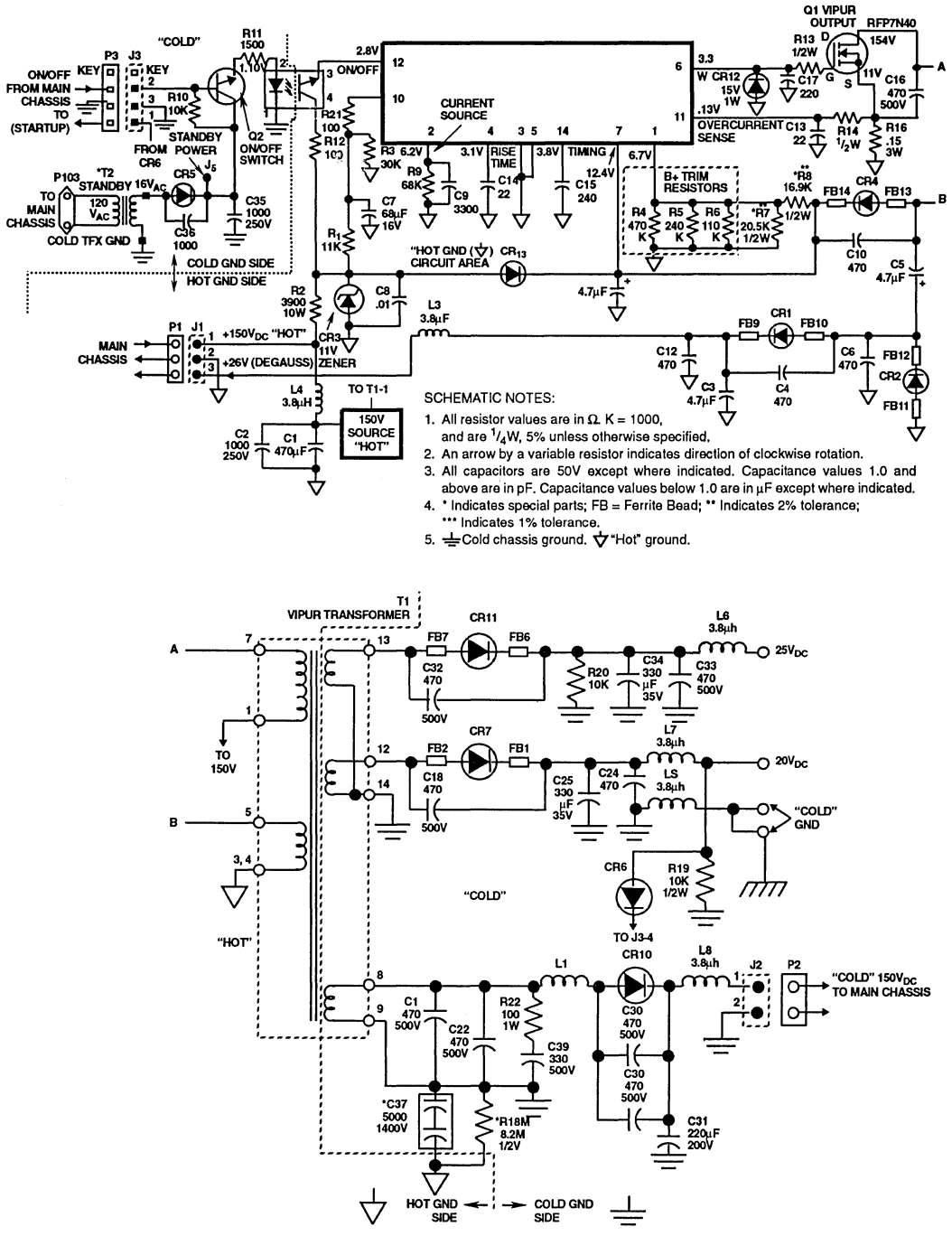


FIGURE 14. APPLICATION OF THE CA1523 VIPUR IN RCA CTC-130 TELEVISION CHASSIS POWER SUPPLY MODULE (SEE 1985 CTC-130C SERVICE NOTES)

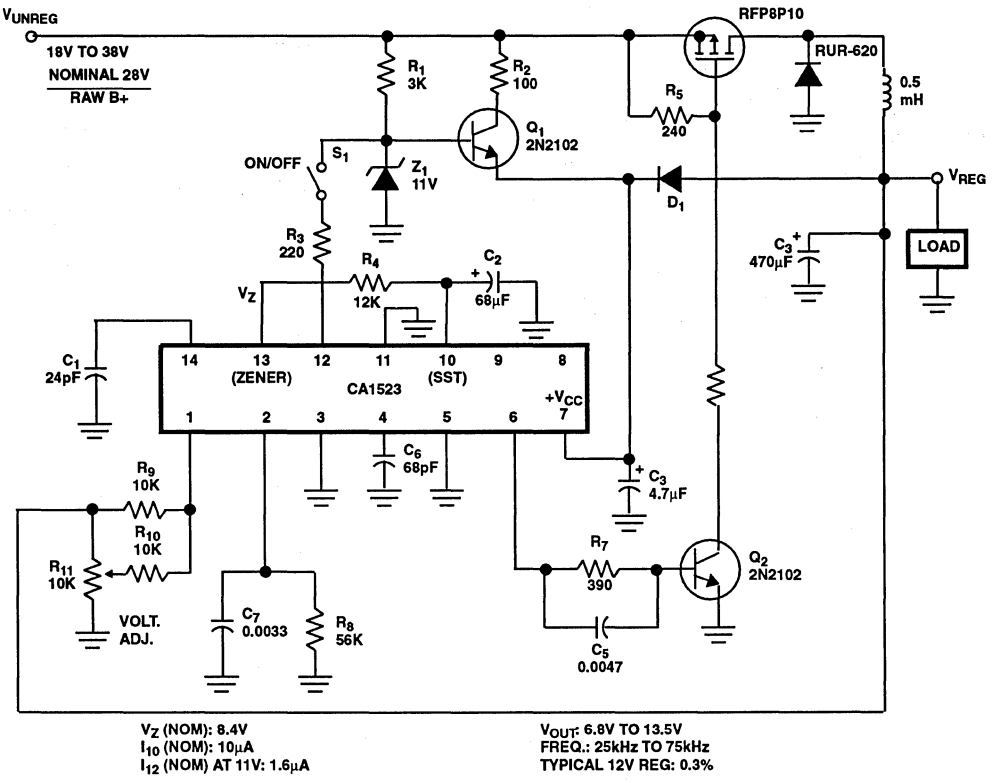


FIGURE 15. BUCK REGULATOR FEATURING ADJUSTABLE OUTPUT VOLTAGE AND SLOW START USING CA1523 ZENER

The raw B+ input may be a 28V battery source or the filtered output of a bridge rectifier supplied from a line isolated step-down transformer. The start-up components are substantially different from those shown in the transformer-isolated flyback-converter circuit, although, as noted, the start-up circuit shown here may be applied in either system. If the output voltage range of the regulator is chosen, as it is typically, to be 11V to 13V, transistor Q1 conducts only for a brief period after S1 is closed. The run B+ is supplied through diode D1 to $+V_{CC}$ at pin 7, and the emitter of Q1 is reverse biased after the power-up cycle is complete. This situation substantially reduces the continuous running dissipation of zener Z1 and resistor R1.

Even when the V_{REG} voltage is less than the zener voltage level, the base current to Q1 is a fraction of a milliampere in a normal run mode. However, more base current is required to charge C4 at line turn on. After start-up is complete and the standby on/off switch is closed, approximately 1.6mA of current is supplied to pin 12. Typically, less than 2mA are needed to sustain idle current to zener Z1. The difference in these losses for the circuit conditions shown in Figure 15 versus those shown in Figure 14 is approximately 2mA versus 35mA. A number of bias options are available for implementing the error-voltage feedback; most of the options are adaptable to either the buck regulator or the transformer flyback-converter system. Either system must feed back a sense return voltage of approximately 6.8V to pin 1. It is not required that the CA1523 be powered by the sense return voltage, but if it is, the voltage should be approximately 11V to 13V. The CA1523 will operate over a supply-voltage range of 9.5V to 15V.

The buck regulator circuit of Figure 15 shows an output voltage adjustment range ratio of 2 to 1. The adjustment range is from the typical 6.8V error-reference level to 2 times the error-reference level. If diode D1 is removed and Q1 used with zener Z1 to supply the run B+ for regulated $+V_{CC}$, higher levels of output can be set by reducing the divider ratio, R1O (R9 + R10). With a ratio of 3 to 1, the typical output voltage will be 3 times 6.8V or 20.4V. Of course, under this condition, the V_{UNREG} input voltage must be higher than 20.4V by the amount of the saturated voltage drop in the power FET. If the error input to pin 1 is directly connected to the V_{REG} output, the typical output voltage is 6.8V. V_{REG} output voltage levels less than 6.8V cause two concerns. First, the return resistor divider that sets the output voltage level must be referenced to a positive voltage greater than 6.8V. Although a concern, this condition is feasible. The second concern, that of using the 11V zener supply, is more serious. When the Z1 reference is used, a power-down condition may allow the V_{REG} output voltage to increase when zener voltage collapses. When that happens, pin 1 voltage will decrease and the error voltage will increase the pulse output drive, increasing V_{REG}. A proper choice of components can avoid the turn off output voltage peaking problem when the raw B+ collapses, and even extend the low voltage regulation range.

The circuit of Figure 16 shows the use of the internal zener diode at pin 13 as a reference for the return divider from the output V_{REG} voltage source. An optional adjustment method using the start-up zener, Z_1, is also shown. For the circuit of Figure 16, the range of this adjustment is 2V to 13V.

Using the CA1523 as a VCO Pulse Generator and Driver

The uses of the CA1523 VIPUR discussed above are application specific to a switch-mode controller for power supplies. Figure 17 shows the CA1523 as a general-purpose V_{CO} pulse generator and driver circuit with a minimum of external components. The V_{CO} control input is at the base of the external transistor Q1, which provides a linear current drive to the current sense, pin 2. For a given timing capacitance at pin 14, a 50% duty cycle pulse frequency at pin 6 is controlled by the pin 2 current. The frequency is linear, with the V_{CO} input to Q1. The pin 1 error voltage is biased low, but may be gated to provide synchronous burst control of the V_{CO} output. Some of the typical characteristics and features of this circuit are listed in Table 1. The drive capability of the pulse output from pin 6 has been noted to be as much as +50mA continuous for an 1800pF load. The internal zener bias and bandgap reference sources keep the frequency output very stable over a power-supply range of 10V to 15V.

TABLE 1. TYPICAL CHARACTERISTICS AND FEATURES OF VCO PULSE GENERATOR AND DRIVER CIRCUIT

CHARACTERISTIC	VALUE
V_{CC}	12V
V_{CC} Range	10V to 15V
I_{CC}	23mA
V_{CO} Input Range	1V to 4V
V_{CO} Sensitivity	53.3kHz/V
$f_{(MAX)}$	200kHz (for C_{14} = 240pF)
$f_{(MAX)}$	500kHz (C_{14} = Stray Capacitance)
V_O Output	11V
t_R	300ns (0V to 8V)
t_F	100ns (11V to 2V)

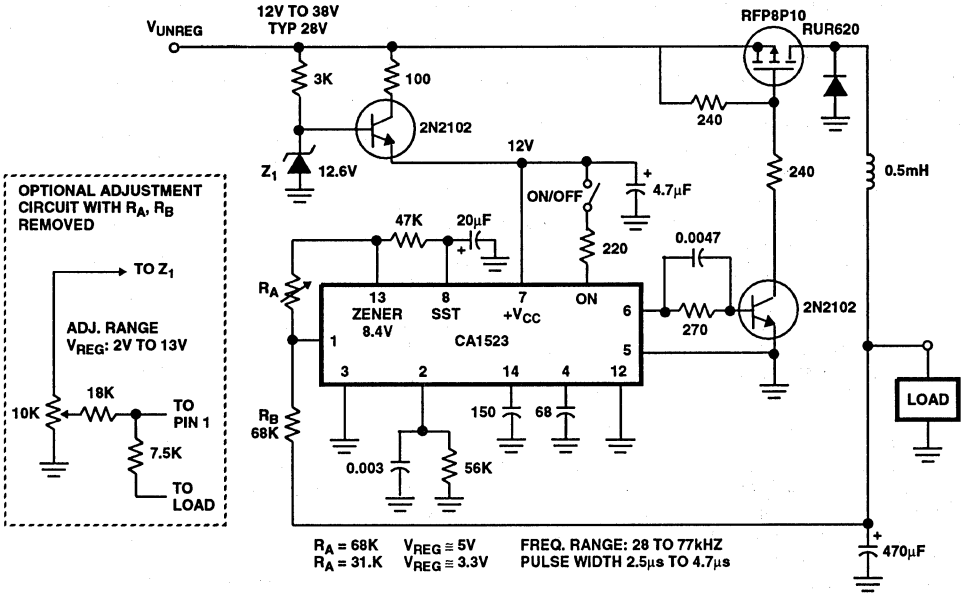


FIGURE 16. LOW VOLTAGE SUPPLY VARIATION IN THE BUCK CONVERTER CIRCUIT

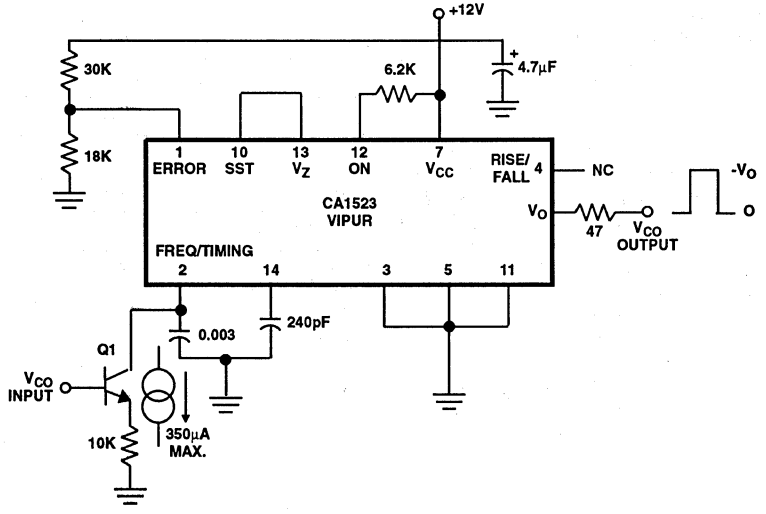


FIGURE 17. V_{CO} PULSE GENERATOR AND DRIVER CIRCUIT

Harris Semiconductor

APPNOTE

No. 8829.1 May 1992

Harris Intelligent Power Products

SP600 AND SP601 AN HVIC MOSFET/IGT DRIVER FOR HALF-BRIDGE TOPOLOGIES

Author: Dean F. Henderson

The interfacing of low-level logic to power half-bridge configurations can be accomplished by an $500V_{DC}$ intelligent IC, the SP600 series driver, which is designed for up to $230V_{AC}$ line rectified operation. The primary function of the high voltage integrated circuit (HVIC) is to drive n-channel MOS gated power devices in totem pole configuration. Compatible with current-sensing MOSFETs/IGTs, this HVIC provides overcurrent shutdown, simultaneous conduction protection, and undervoltage lockout. Logic level inputs provide noise immune control of power element switching.

The SP600 has demonstrated high frequency (130 kHz) operation as well as the ability to withstand high dv/dt. Its semicustom design flexibility makes it easily adaptable to a wide range of single and multiple phase applications. Other salient features of the device are described below.

Technology Overview

BiMOS structures are implemented in a junction-isolation process, known as "lateral charge control",[1] that supports high voltage laterally. By the use of this thin epi process, low voltage analog and digital circuitry can be combined monolithically with high voltage transistors. Low voltage circuits can be constructed to float up to $500V_{DC}$ with respect to the substrate. Additionally, $500V_{DC}$ NMOS and n-p-n transistors can also be fabricated.[2] Since this process conforms to mainstream low voltage IC manufacturing, it is cost effective.

Totem Pole Drivers

Historically, designers have been faced with awkward decisions regarding the upper-rail drive of bridge topologies. P-channel MOSFETs, while easy to drive, are more than twice as expensive as equivalent n-channel devices having the same rds(on). Economic barriers and product availability generally prohibit design beyond $200V_{DC}$. On the other hand, the driving of upper rail n-channel MOS gated devices requires a floating gate supply that must be 5 to $20V_{DC}$ greater than the upper rail link. While several discrete approaches for implementing this floating supply are known, the designer is burdened with additional components and potential dv/dt problems associated with voltage translation.

The SP600 series driver provides the economical solution as an intelligent totem pole n-channel driver. With the addition of as few as five, user defined, external, passive components (three if current detection isn't employed) a functional half-bridge driver can be built that has the following features:

- Creation and management of a $15V_{DC}$ upper-rail power supply
- Ability to interface and drive standard and current sensing n-channel MOSFETs/IGTs
- Shoot-through protection
- Overcurrent protection
- Undervoltage lockout
- CMOS logic-level input compatibility
- Semicustom flexibility through metal-mask changes
- Standard 22-pin DIP packaging

Theory of Operation

Figure 1 is the basic block diagram of the SP600. CMOS logic compatible input signals are filtered to ensure reliable operation when the device is subjected to noisy industrial environments. Digital commands at TOP and BOTTOM inputs cause the upper or lower drivers, respectively, to turn on or off. The $I_{TRIP\ SELECT}$ input provides a higher than nominal current limit on a pulse-by-pulse basis. The input signals are decoded to drive the appropriate output device. High voltage translation is provided by current mirror pulses used to communicate upward to the top gate driver to initiate turn on or off (I_{ON}/I_{OFF} pulses). These momentary pulses are captured by local latches to maintain the desired state. This feature minimizes power dissipation in the level shifter and provides added noise immunity as well. The bottom gate driver circuitry is similar. The floating bootstrap power supply is provided by low voltage capacitor C_F and high voltage diode D_F. Each time the V_{OUT} node goes low, C_F charges to roughly a diode drop less than Vdd ($15V_{DC}$). This situation prevails each time the lower output device is activated or, in the case of an inductive load, whenever the upper device is switched off and freewheeling load current forces the output node to a diode drop below ground. In either case, D_F is forward biased, allowing C_F to charge through the current limiting resistor R_{BS} to approximately V_{DD}. Noise dropping resistor R_{ND}, along with capacitor C_{DD}, provides localized filtering of the bias supply and bypasses bias supply series inductance facilitating fast and complete bootstrap refresh.

Each output device is protected on a pulse-by-pulse basis from overcurrent (OC) by sense resistor R_S, which is connected to 100mV comparators. This arrangement permits the designer to take advantage of nearly lossless current-sensing MOSFETs or IGTs.

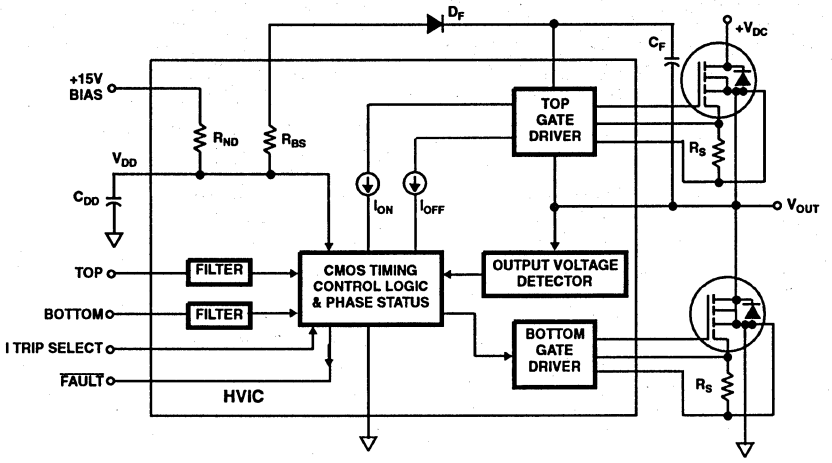


FIGURE 1. BLOCK DIAGRAM OF THE HVIC

Upon detection of any OC, the output is immediately disabled. In the case of the lower switch, a FAULT is directly detected and reported. Upper rail OC FAULTs are indirectly reported via the output voltage monitor when it detects an output state not in agreement with the commanded TOP input signal. With local OC detection and shutdown of the upper device, an inductive load will force V_{OUT} low due to freewheeling. This "out of status" detector recognizes a fault when V_{OUT} is typically less than $5.5V_{DC}$.

Logic And Timing

Figure 2 is a detailed functional circuit of the SP600. The filtered inputs, TOP, BOTTOM, and $I_{TRIP\ SELECT}$, ignore pulse widths less than typically 400ns to prevent false triggering. During the generation of I_{ON} and I_{OFF} pulses, the control logic ignores further changes in the input signal. For each I_{ON} pulse, an I_{OFF} pulse is simultaneously sent to the opposite driver, thus eliminating the possibility of spurious shoot

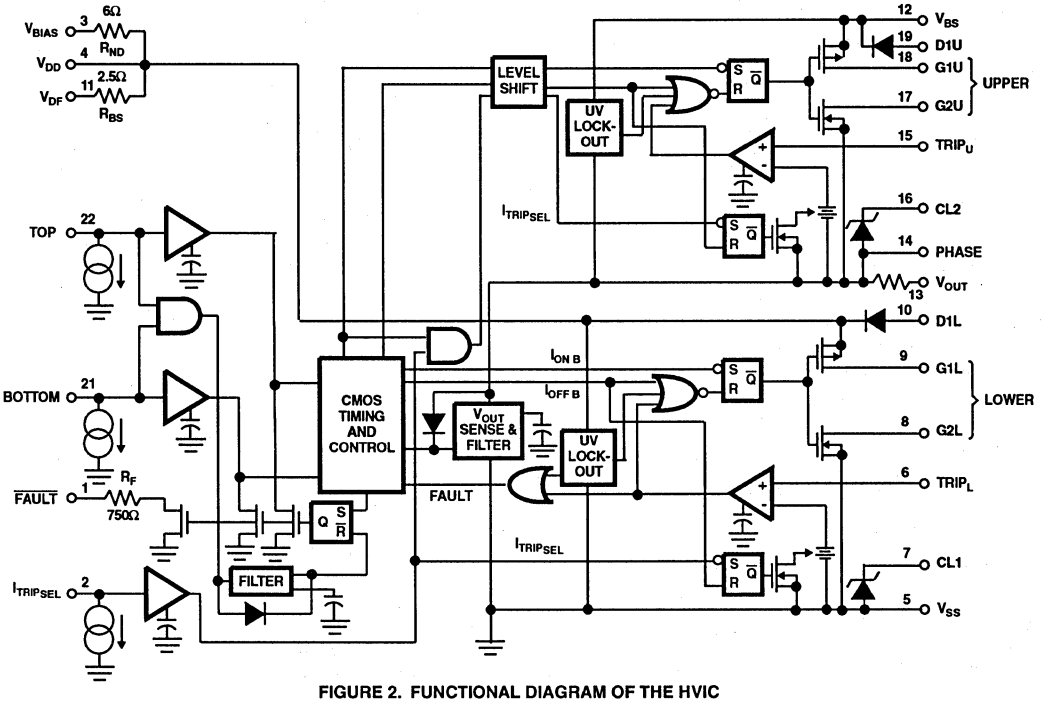


FIGURE 2. FUNCTIONAL DIAGRAM OF THE HVIC

through caused by high voltage, high-speed switching. These features aid in providing predictable operation of the floating upper rail driver section, which is capable of slewing over 10,000 volts per µs.

PHASE serves as a common reference for the floating bootstrap supply (V_{BS}) and all upper rail logic. V_{OUT}, for all practical purposes, is at the same potential as PHASE, being separated from it electrically by only a few Ω (R_O). This additional series output resistance helps to limit the peak current being drawn from the HVIC when an external lower flyback diode, undergoing forward recovery, forces V_{OUT} negative.

An automatic refresh algorithm is generated by the CMOS timing and control block to ensure that the bootstrap capacitor remains charged. As mentioned above, C_F is refreshed each time the V_{OUT} node swings to common. At power up, with zero voltage on C_F, there are two ways to refresh the bootstrap capacitor. The first is by initially commanding the bottom device to turn on, forcing V_{OUT} low. The second occurs when an automatic refresh is invoked if the TOP has been commanded on for longer than 200µs to 500µs. The logic momentarily ignores the inputs, and turns on the lower output (subsequent to an I_{OFF} TOP) for typically 2.0µs, charges C_F and finally restores control to the input commands. Automatic refresh is overridden at switching rates greater than 5kHz, the minimum refresh timer period.

A dual level current limit provision allows for a 30% higher current trip point (above nominal) on a pulse-by-pulse basis. A logic level 1 applied to $I_{TRIP\ SELECT}$ provides a boosted current limit suited for applications like uninterruptable power supplies (UPS), which may have occasional shifted peak power requirements. This feature may allow for a more optimally selected output device. Benefits of current boost have been demonstrated in an off-line PWM motor controller where $I_{TRIP\ SELECT}$ is momentarily applied to overcome the inertia associated with rotor start-up.[3]

Both outputs are disabled and a FAULT reported as a result of:

- Overcurrent
- V_{DD} (lower bias) and V_{BS} (upper bias) undervoltage
- V_{OUT}/PHASE out-of-status
- Simultaneously commanded TOP and BOTTOM input (outputs disabled, no FAULT reported)

The fault can be cleared by a logic 0 at both TOP and BOTTOM inputs for the required fault reset delay time of 3.4µs to 6.6µs.

Power Driver Section

The upper and lower driver output sections are nearly identical, Figure 3.[4] Separate sink and source transistors are separately bonded out for application specific designs requiring additional series gate impedance(s) for slower charge and discharge rates. This circuit property becomes particularly important with IGTs, where a minimum turn-off impedance of 100Ω may be required to ensure full SOA. Regardless of the switching element used, companion flyback diode characteristics may necessitate slower turn-on to reduce peak reverse recovery current by increasing the gate impedance by means of R_{CHARGE}.

A nominal 100mV_{DC} comparator provides overcurrent (OC) protection when used with either current sensing IGTs or MOSFETS. OC can also be implemented by using low impedance shunts with noncurrent sensing power output devices, Figure 4.

Clamp CL1 in Figure 4 provides overvoltage protection for current sensing structures during switching intervals, and protects the comparator from any voltage transients due to external lead inductances. To avoid nuisance OC trips caused by reverse recovery current during turn-on transitions, the comparator's output is blanked for approximately 3µs.

System Performance

The half-bridge test circuit in Figure 5 was built to demonstrate the SP600 as a high frequency driver of MOSFETs. The load is referenced to one-half the battery voltage, allowing bidirectional load current. This circuit characteristic emulates power configurations of half bridges with split supply or full bridges implemented with multiple HVICs.

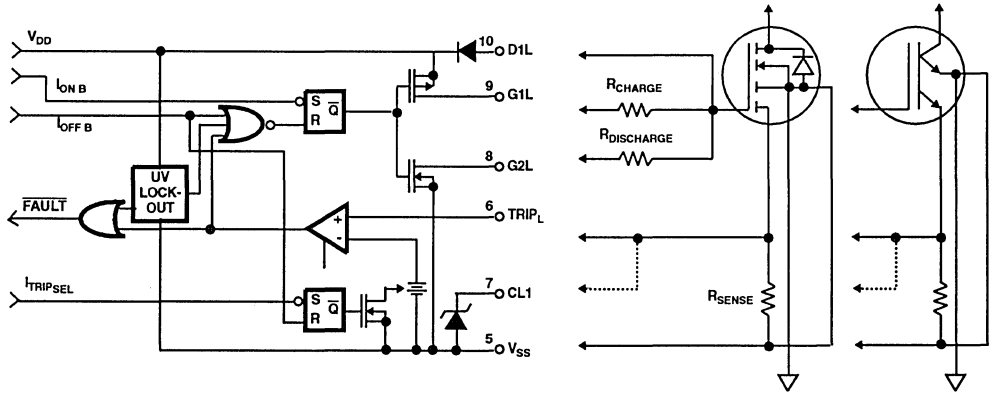


FIGURE 3. POWER-OUTPUT SECTION INTERFACING WITH CURRENT SENSING MOSFET OF IGT.

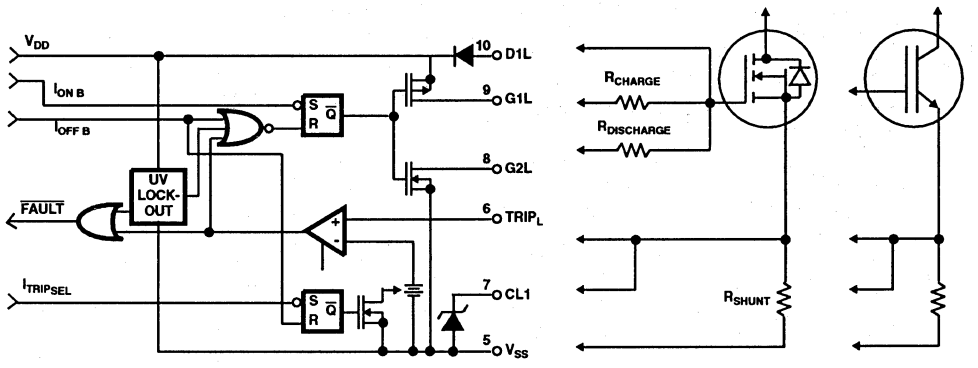


FIGURE 4. POWER OUTPUT SECTION INTERFACING WITH NONCURRENT SENSING MOSFET OR IGT.

For ultimate switching speed, no additional series gate impedances were used. Peak MOSFET gate charge and discharge current waveforms of 400 and 510mA$_{DC}$, respectively, were observed, Figure 6.

High frequency, high voltage operation requires that upper rail drive and level translator circuitry be immune to high dv/dt, as this section floats with respect to V_{OUT}/PHASE. Interjunction capacitance can dynamically inject displacement currents, raising havoc in circuit performance or even causing catastrophic failures, including the breakdown of voltage isolation tubs or latch-up in adjacent four layer structures.

At rail voltages of 200V$_{DC}$ to 400V$_{DC}$, rise and fall transitions of V_{OUT}/PHASE were measured in the 20ns to 35ns region. The HVIC operated flawlessly while being subjected to output swings beyond 11,000V per µs. Figure 7 demonstrates the HVIC's ability to sustain such dv/dt when driving IRF820 devices.

IRF 842s were driven at 130kHz in this same half-bridge circuit, Figure 8. The ultimate switching speed of the SP600 series HVIC will depend on gate capacitance and the duty cycle limits dictated by the minimum I_{ON} and I_{OFF} times. A minimum I_{ON} time (1.6µs to 3.1µs) ensures time for refresh, while a minimum I_{OFF} time (1.3µs to 3.4µs) prevents simultaneous conduction by allowing for gate discharge prior to an opposite I_{ON} pulse. The same promising technology has been shown to operate a half-bridge resonant converter at frequencies up to 600kHz.[6]

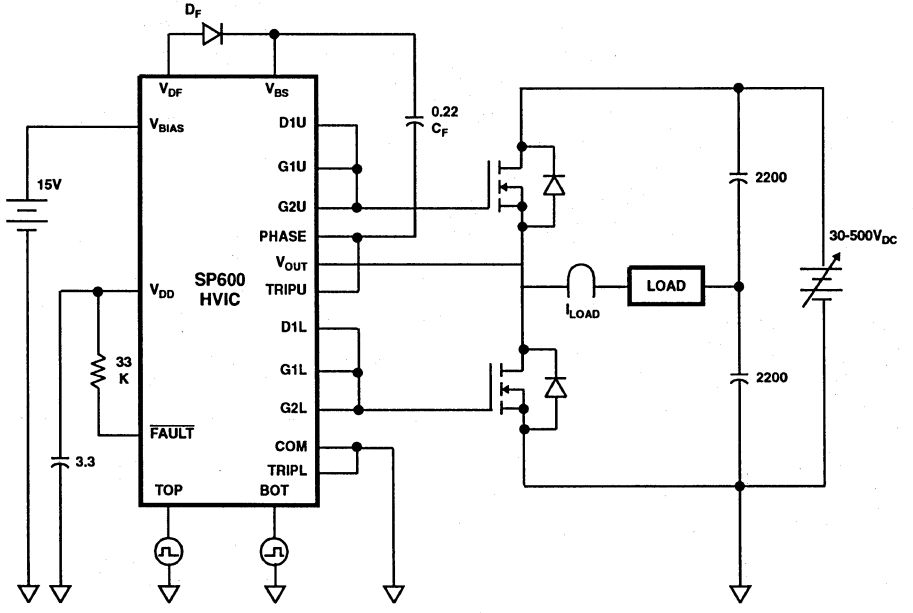
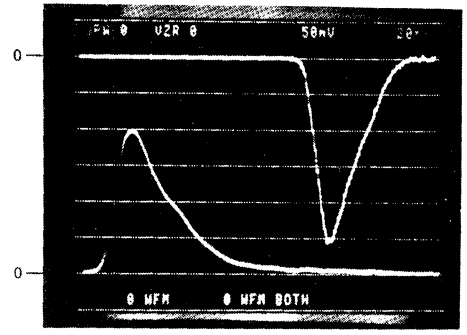
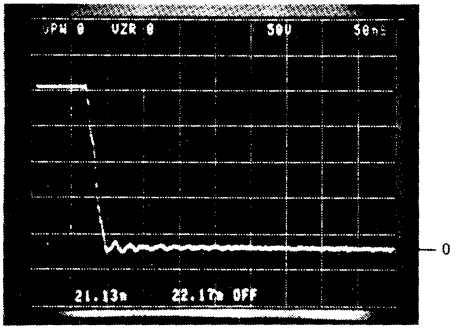


FIGURE 5. HALF-BRIDGE TEST CIRCUIT



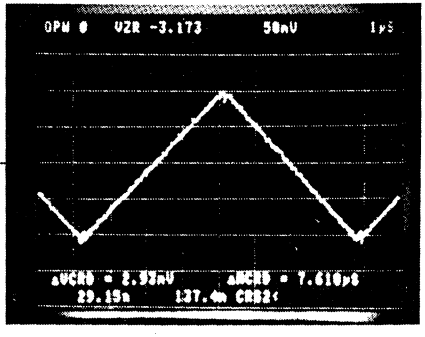
Top: Turn Off Vertical: 100mA/div
Bottom: Turn On Horizontal: 20ns/div

FIGURE 6. GATE-CURRENT WAVEFORMS DRIVING AN IRF820



Vertical: 50V/div
Horizontal: 50ns/div

FIGURE 7. V_{OUT} TRANSITION AT TURN ON OF LOWER IRF820



Vertical: 50V/div
Horizontal: 50ns/div

FIGURE 8. OUTPUT LOAD CURRENT AT 130kHz USING IRF842s

Semicustom Capability

The SP600 family can be customized by inexpensive, final metal mask alterations. Application specific designs are possible for variations in the following parameters:

- Minimum I_{ON}/I_{OFF} pulses
- OC trip response time
- Input signal conditioning filters
- OC trip level
- Inclusion of $R_{CHARGE/DISCHARGE}$
- $I_{TRIP\ SELECT}$ boost level
- FAULT reset timer

Other system related options include:

- Input protocol
- Automatic FAULT reset
- Ability to disable the automatic refresh algorithm

References

1. E. J. Wildi, et al, "New High Voltage IC Technology," IEDM 84 Conference proc, pp 262-265.
2. E. J. Wildi, et al, "500V BiMOS Technology and its Applications," Electro 85 paper #24/2.
3. J. G. Mansmann, et al, "ASIC Like HVIC for Interfacing to Half-Bridge Based Power Circuits," PESC March 88.
4. J. G. Mansmann, et al "A Flexible High Voltage Controller Core for Half "He" N-Channel Bridge Operation," MOTORCON proc, Sept '87, pp 194-205.
5. D. J. MacIntyre, "Motor Control Applications of Second Generation IGT Power Transistors," GE PESD Application Note 200.95.
6. R. L. Steigerwald, et al, "A High-Voltage Integrated Circuit for Power Supply Applications", APEC proc, Mar '87, pp 221-229.

Appendix

Timing Waveforms (See page 6)

Although both SP600 and SP601 timing diagrams are shown the SP601 was chosen to provide further explanation.

$t_0 < t < t_1$ At t_0, with the enable high, the outputs are simultaneously commanded to switch from lower to upper which is also known as Bistate operation. After delay t_{OFFD}, the lower is turned off, followed by the uppers turned on. Dead time, $t_{D.T.}$, the difference between the lower off transition to the upper on transition is internally set. Since this timing sets the margin of safety for simultaneous conduction, it's the user's responsibility to ensure that proper external gate impedance is selected to ensure ample time for power transistor charging/discharging.

$t_1 < t < t_2$ The lower is turned on at t_1 and continues for a relatively long period, long enough that at t_2 an automatic refresh will be invoked.

$t_2 < t < t_3$ The HVIC has blinded itself to the logic inputs during this refresh mode. The upper is turned off, with its associated turn off delay, t_{OFFD}. After the fixed dead time, $t_{D.T.}$, the lower is briefly turned on, ton, providing a charge refresh path for the bootstrap capacitor, C_F. Once again the dead time is observed before turning the upper back on again and restoring control to the user inputs. This refresh cycle can be detected as a few µs wide pulse of lower MOSFET/ IGT current.

$t_3 < t < t_5$ The upper remains commanded on for a period of time less than t_{REF}. At t_4, the UP/$\overline{DOWN}$ time is brought low, commanding a lower turn on. Similar to the t_0-t_1 interval, the upper turns off after delay t_{OFFD} and the lower turns on after the dead time, $t_{D.T.}$

$t_5 < t < t_7$ The SP601 is disabled by the ENABLE line low at t_5. Previously conducting lower turns off after its delay, t_{OFFD}. Since the ENABLE line was previously brought low and neither output transistors are conducting, termed as tristate mode. The state of the output phase waveform remains unknown. At t_6, the ENABLE is once again pulled high. The lower turns on after delay, t_{ONDB}.

$t_7 < t < t_9$ At t_7, the SP601 is disabled and the UP/ DOWN line is toggled to the upper position. The lower turns off and the power devices go into a tristate mode. At t_8, upper turn on sequence begins. Since the auto one shot hasn't timed out yet, the turn on delay, t_{ONDB}, is relatively short.

$t_9 < t < t_{11}$ The chip shuts off as the ENABLE line is brought low at t_9, and is enabled again at t_{10} as the UP/DOWN line had remained high. Since the disable period was long and the refresh one shot had timed out, the turn on delay, t_{ONDT}, is slow. Keep in mind that the delay time includes the time for automatic refresh. In an attempt to not further complicate the drawing, the detailed refresh cycle isn't actually shown.

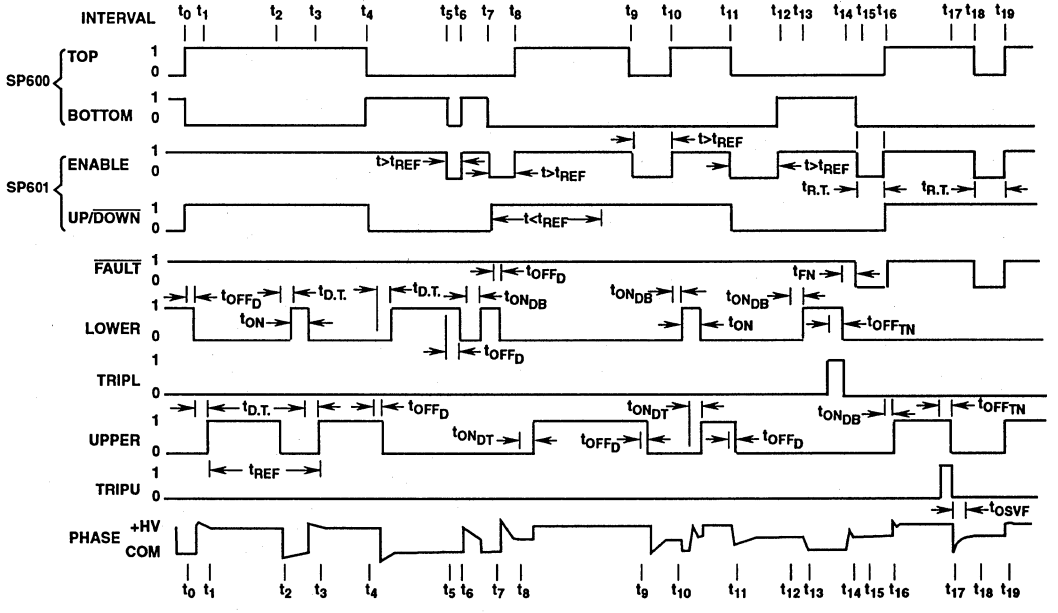
$t_{11} < t < t_{13}$ Both inputs are brought low at t_{11} for a duration longer than t_{REF}. At t_{13} the ENABLE is restored, initiating the turn on sequence for the lower. This follows a long period of time where the one shot had timed out, but in this case the lower is commanded on. Since it doesn't need the refresh algorithm, the turn on delay, t_{ONDB}, is fast.

$t_{11} < t < t_{13}$ This sequence of events depicts the detection of a lower overcurrent trip. Between t_{13}-t_{14}, the lower is on. Beyond the filter delay, t_{OFFTN}, the overcurrent trip shuts off the lower driver. A fraction of a µs later, t_{FN}, the flag report delay, FAULT goes low.

$t_{15} < t < t_{16}$
$t_{18} < t < t_{19}$ By holding both ENABLE and UP/DOWN lines low for the required fault filter reset time, $t_{R.T.}$, the fault is cleared.

$t_{16} < t < t_{17}$ The upper is turned on and an overcurrent trip begins. Beyond the filter delay, t_{OFFTN}, the overcurrent comparator shuts off the upper drive at t_{17}. Since the control logic can only communicate upwards, there is no direct means of reporting an upper trip. As the fault has been remotely captured by the floating upper section, shutdown has occurred. The Phase or V_{OUT} node will quickly fall to a diode drop below common due to inductive flyback current. Via the V_{OUT}/V_{PHASE} monitor this is detected as not being in agreement with the commanded input and reports the fault. Reporting this phase out of status delay is t_{OSVF}.

SP600 Series Timing Diagram



Harris Semiconductor

APPNOTE

No. 9010.2 May 1992

Harris Intelligent Power

HIP2500 HIGH VOLTAGE ($500V_{DC}$) HALF-BRIDGE DRIVER IC

Author: George E. Danz

Introduction

The HIP2500 is a high voltage, high speed dual driver for MOS gated power devices. The drivers are isolated from each other, each controlled by an independent input line referenced to the system common voltage. The HIP2500 was designed using the same proprietary technology which was started more than 5 years ago, resulting in the first products in the HVIC family, the SP600/SP601 Half-Bridge Drivers. Many of the benefits of the SP600/SP601 family also apply to the HIP2500. For example, these HVICs offer a very inexpensive means for driving an n-channel power switch from low side referenced logic without special isolation circuitry, such as optocoupler (not known for extreme reliability) or transformer means (often too expensive). Highly integrated low level logic and high-level drive circuitry minimize propagation delays, allowing higher switching frequencies and often lower switching losses than would be attainable using more conventional techniques. In addition to cost savings and performance increases, the HVIC simplifies and reduces the effort needed to design an efficient driver for MOS gated high and low side switches. Features specific to the HIP2500 are discussed below.

The HIP2500 enjoys some features which the SP600/SP601 lacks. These are a smaller 14 pin dip package, significantly higher output drive capability (2A peak) and lower transport delays from input to output. In order to maintain noise immunity, CMOS Schmitt triggered inputs with pull down are incorporated on all inputs. By shedding some of the features of the SP600/601 family such as over-current trip and shoot-through protection, the HIP2500 can operate at PWM frequencies as high as 500KHz depending on bus voltage, having gate rise and fall times of typically 23ns into 1000pF load.

The blocking voltage of the HIP2500 has been increased to $500V_{DC}$ in keeping with industry requests for 600V blocking capability for bridge components for use on rectified $230V_{AC}$ lines.

While the burden of shoot-through protection is now squarely with the user, the added flexibility of precise user gate control allows some other interesting circuit topologies. For example the double forward converter configuration popular with power supply, stepper motor control and switched reluctance motor control can now be implemented. Capacitor C_F must be fully charged before turning the upper switch on the first time by holding the lower switch on long enough to charge C_F through the load impedance. See Figure 1.

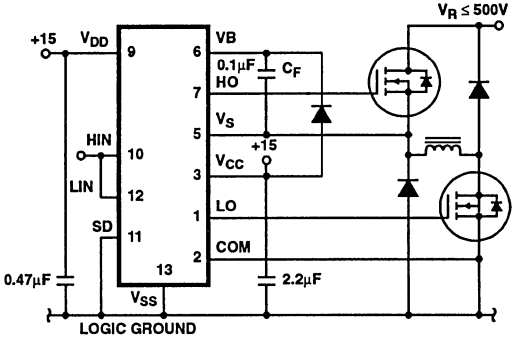


FIGURE 1. DOUBLE FORWARD CONVERTER SCHEMATIC

Also with the HIP2500 it is possible to drive a high side switch which can be switched independently from the low side switch. The load itself could supply initial bootstrap voltage and an appropriate flyback diode would be required in parallel with the load to avoid severe negative excursions of the power switch's source lead. An example of this is shown in Figure 2.

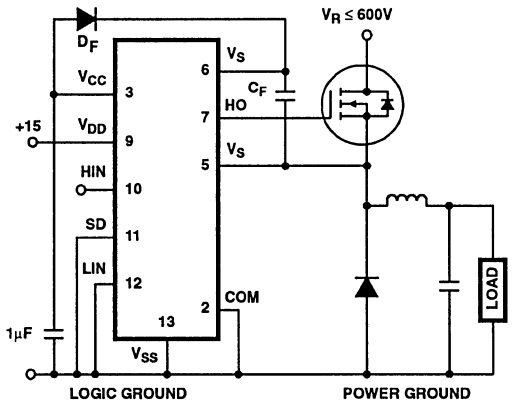


FIGURE 2. HIGH SIDE SWITCH OR "BUCK CONVERTER"

Description of the HIP2500

The block diagram of the HIP2500 is shown in Figure 3. The HIP2500 is comprised of a ground referenced gate drive circuit and a high voltage bus referenced (floating) gate drive circuit. The input logic circuit for the high side driver incorporates level translation circuitry to interface between the low voltage logic section and the high voltage logic section which controls the upper (or floating) gate driver.

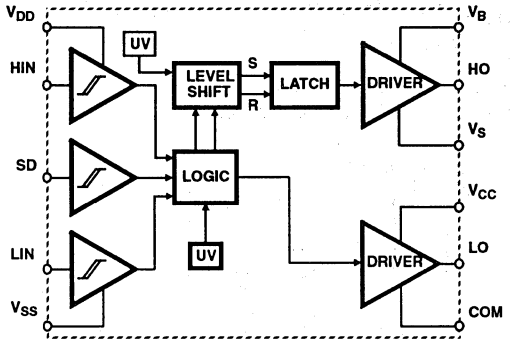


FIGURE 3. HIP2500 FUNCTIONAL BLOCK DIAGRAM

Input Logic

There are three inputs to the HIP2500; HIN controls the floating high side driver, LIN controls the low side (ground referenced) driver and SD which controls the "shutdown" function. All inputs pass through Schmitt buffers employing hysteresis with transition thresholds proportional to the logic supply V_{DD}. Slower or ramped inputs therefore are squared up before being passed to the level translation circuits, which translate the logic level inputs to signal levels compatible with the fixed driver (10V to 15V) supply. The level translation circuit allows the ground reference of the logic supply (V_{SS} on pin 13) to swing plus or minus by a couple of volts with respect to the power ground (COM on pin 2) thereby enhancing noise immunity.

Each channel, including the shutdown input, is independently controlled. The gate drive responds within a short (typically 400ns) propagation delay of the input signal. In applications where deadtime is required to prevent conduction overlap or "shoot-through", the HI and LO input commands must be spaced by external circuitry. For example in a half-bridge configuration, where the upper and lower switches are series connected between the high and low sides of the power bus, effort must be taken to turn off each of the switches in advance of turning on the other. The designer must ensure that one switch is completely off before trying to turn on the other or high currents can flow through both, possibly leading to destruction of one or both power switches. Often a few passive components added to delay switch turn-on without delaying turn-off can effectively control shoot-through (see the diode resistor parallel combination in Figure 4). As power levels and power switch devices become larger, passive techniques may become a more appropriate means to provide turn-on blanking of one switch while the other switch is turning off.

Shutdown is accomplished by a logic level 1 at the SD input. This input must be at logic level 0 to "gate" the HIN and LIN inputs to their respective drivers. The SD logic also removes bias to the high voltage translation pulse circuits, thereby reducing bias current to the HIP2500 when in shutdown mode.

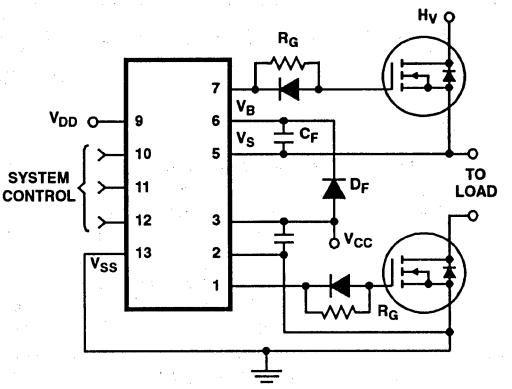


FIGURE 4. SIMPLIFIED SHOOT-THROUGH CONTROL

Protection Features

The HIP2500 is protected internally from insufficient bootstrap supply voltage (in the case of the upper floating driver) and insufficient bias supply voltage (in the case of the lower driver). Also circuitry is provided which allows the high voltage power to be applied prior to the low voltage control power without inducing false gating from the HIP2500.

The undervoltage circuitry functions differently for upper and lower drivers. The lower undervoltage lockout blocks drive to both upper and lower power switches. Upon reestablishment of proper lower supply voltage levels the drive signals are unblocked and gate drive to both upper and lower switches is reestablished provided the appropriate LIN and HIN signals are enabled. The upper undervoltage circuit controls only the gating of the upper (floating) switch which is latched off when an undervoltage is sensed. Latching is released when the upper undervoltage circuit is satisfied. A subsequent "on" pulse from the HIN terminal is necessary to trigger the upper switch. The HIN terminal must have previously gone low since all communications with the upper driver are "edge" triggered. The purpose for latching either driver off in the event of an undervoltage condition is to ensure direct control from the HIN input. Without latching, the undervoltage circuit could cycle at a frequency dependent upon the size of the bootstrap capacitor, gate capacitance, and undervoltage hysteresis levels. Latching the undervoltage detector provides in essence an "alarm" that an undervoltage condition has occurred. The circuit designer must pick values of bootstrap capacitance which avoids undervoltage triggering at the PWM design frequency. Guidance on choosing the right value can be found under "Floating Supply Considerations" later in this note.

Driver Circuits

The driver circuits for the upper and lower gate drives are identical. Since it is desirable to provide the greatest possible gate drive voltage consistent with the user supplied voltage, p-channel mosfets have been used in the output stage of the drivers for sourcing gate current to the power device. Likewise, n-channel devices have been employed for sinking current from the gates of the power devices. This approach allows complete utilization of the V_{CC} voltage and changes in mosfet threshold voltages with temperature will not reduce power device gate bias levels.

The sink and source currents of the gate drivers are fully capable of supplying peak currents of at least 2.0A, which means that a power mosfet device with 3000pF gate source capacitance can be fully charged in 25ns. Discharge of the gate source capacitance will be slightly more rapid, since R_{DSon} of the sink driver is about 10% less than the source driver.

The high side driver section is built into an "isolation tub" which is capable of floating $+500V_{DC}$ above substrate potential with respect to power ground (COM pin 2). Pin 6 (V_S) is the common potential for the upper drive circuitry and is the most negative voltage within the floating tub. V_B (pin 5) is the positive rail within the floating tub and is usually +15 above V_S. The gate drive output, HO (pin 7) swings between V_S and V_B according to the state of the HIN input pin.

Floating Supply Considerations

The floating supply which ties between V_B and V_S is supplied typically by a capacitor, C_F, referred to as the bootstrap capacitor. A fast recovery, low leakage diode, D_F, refreshes or charges this capacitor whenever the V_S terminal swings to common (see Figure 4). A low leakage, fast recovery diode should be chosen for the bootstrap diode and should exhibit low reverse recovery charge. Accomplish this by choosing a diode with a blocking voltage rating greater than $500V_{DC}$. For example, the Harris A114P diode is a high voltage 1A, fast recovery diode rated at 1000V blocking. It is used with great success on rectified $230V_{AC}$ circuits where normally a 500V or 600V diode would be used. The high voltage diode results in a naturally lower junction capacitance than would be attainable in a comparable low voltage diode.

The refresh charging "loop" is a circuit beginning at the V_{CC} node and comprising the bootstrap diode (forward biased), the bootstrap capacitor, either the lower power device or the flyback diode and the COM terminal. Normally V_S voltage will be one diode drop below the COM terminal whenever the upper power switch is turned off due to the inductive nature of the load current commutating from the upper switch to the lower flyback (or body) diode around the lower power switch. When no inductive load current is flowing through the lower flyback diode, then the V_S terminal voltage will operate at a voltage above the COM terminal determined by the lower power device's forward voltage drop. The ultimate voltage attained on the bootstrap capacitor is dependent on whether it was refreshed through the flyback diode or the lower power switch device. Lead inductance associated with the flyback diode can actually cause the V_S terminal to transiently go 5V to 20V below COM depending on dv/dt. This occurs when the upper switch is turned off very rapidly and the load current is rapidly commutated to the lower flyback diode. Although this can help to dump some charge very quickly onto the bootstrap capacitor, it can cause trouble with the HVIC if allowed to exceed more than about 4 volts. It is wise to minimize this inductance by tight power circuit layout practices.

A number of considerations in the implementation of this bootstrap arrangement which must be kept in mind. The series inductance in the loop comprised of the bootstrap diode, capacitor and the V_{CC} supply and COM return path must be kept very low. Ideally under normal conditions the charging time for refreshing the capacitor is short. This must be so when very high PWM duty cycles are desired. In fact overmodulation must be avoided so that approximately 1 to 2 µsecs is reserved for refreshing the bootstrap capacitor. The actual time required depends on the series resistance of the bootstrap loop, the series inductance (hopefully near zero) and the size of the bootstrap capacitor. An upper limit on the PWM frequency is then given by:

$$f_{PWM} \leq \frac{(1 - DC)}{t_{REF}}$$

where:

DC = Duty cycle fraction

t_{REF} = refresh time (sec.)

t_{PWM} = PWM frequency (Hz)

Another consideration in the design of the bootstrap circuit concerns the sizing of the bootstrap capacitor. If it is assumed that all of the gate charge comes from the bootstrap capacitor, which is a good assumption, then enough charge must be placed on the bootstrap capacitor such that when it "dumps" the turn-on gate charge to the power switch, there is still enough voltage on the bootstrap capacitor such that undervoltage lockout is not triggered. For turn-on gate charge of Q_G, flying capacitor of C_F, supply voltage V_{CC} and final gate voltage V_G (which must be greater than the maximum value for the undervoltage trip threshold), the minimum bootstrap capacitor is given by:

$$C_F > \frac{Q_G}{V_{CC} - V_G}$$

The above assumes an inductive load which would tend to cause the bootstrap diode drop to be approximately cancelled by the drop associated with the body diode (mosfet) or flyback diode in parallel with an IGBT. If the load is not somewhat inductive, the bootstrap diode drop must be subtracted from V_{CC} along with any drop associated with the lower switch. The effects of leakage current in the reverse biased bootstrap diode and the small quiescent bias current of the upper driver circuit must be taken into account when sizing C_F. Therefore the sum of the above currents and the charge removed from C_F in charging the gate capacitance, Q_G, determines the minimum size of C_F. Therefore:

$$C_F > \frac{Q_G + (I_{QBS} + I_R) \bullet t_{ON}(max)}{V_{CC} - V_G}$$

The previous discussion on refreshing has been made with a half-bridge or "totem-pole" configuration of the power switches in mind. Other topologies are of interest such as the "double forward converter" configuration shown in Figure 1. Once current is established in the inductor of the double forward converter, simply turning off the switches causes the inductor current to freewheel through the commutating diodes. The V_S lead will be pulled to approximately a diode drop below COM while the inductor current ramps to zero.

This action will charge the bootstrap capacitor in all cases but those wherein the inductor current is minute. During start-up when there is no current in the inductor, it is necessary to precharge the bootstrap capacitor. This can be accomplished in a number of ways, but one can simply turn on the lower MOSFET or IGBT long enough to charge up the capacitor. Voltage overshoot due to the resulting series RLC circuit will be clamped by the internal zener clamps and/or the substrate diode within the HIP2500. Alternatively, a small auxiliary MOSFET can be placed around the lower flyback diode and driven by an inverted LO gate drive signal. When the lower is turned "off", the auxiliary MOSFET will be turned "on" thereby supplying a charging path for the bootstrap capacitor.

The buck converter (Figure 2) is another possible application for the HIP2500. With this type of converter configuration, as soon as the HIP2500 bias supply power is applied, the bootstrap capacitor will be charged through the load impedance. After having waited for complete charging of the capacitor, it is then possible to operate the HIP2500 normally. Subsequent refreshing will occur each time the buck converter switch is turned off which it must do in order to refresh the bottstrap capacitor.

Level Shifting Circuits

As shown in Figure 4, the high side channel input commands require level shifting from a level near COM to a level near that at which the high voltage tub is floating, which can be 500V. The on/off commands for the high side are transformed into narrow current source commands which sink current through burden resistors in the high side circuit. After squaring up these pulses they are "and" gated with the output from the under voltage circuit and latched before being sent to the driver section.

Switching dv/dt as high as 50V/ns is possible with the HIP2500. Also, when the upper switch is turned off, the short lived negative excursions of the V_S terminal due to so-called "forward recovery" and lead wire inductance in series with the upper and lower power switches will not cause problems with HIP2500 operation.

Power Dissipation

Power dissipation in the HIP2500 results from static losses and switching losses. The static losses are due to the bias supply in both upper and lower driver sections and leakage losses in the high voltage level translation transistors. The sum of all these losses at 15V is approximately 19.5mW at +25°C. At +125°C these losses are not normally over 30mW.

The dynamic losses are due to low voltage and high voltage switching losses. The low voltage switching losses derive primarily from the upper and lower driver output stages. The energy required in charging and discharging the gate of the power switches must flow through the resistance in the gates of the power devices, the R_{DSon} of the driver output stage, and all of the lumped wiring and connection and supply sources resistances. The sharing of these resistances between the HIP2500 and the external source and switch devices must be known before an accurate calculation of losses can be attempted. The maximum total loss can easily be calculated once the PWM frequency, supply voltage and power device gate charge is known:

$$P_{driver} \cong 2 \bullet f_{PWM} \bullet Q_G \bullet V_{CC} \text{ Watts.}$$

The high voltage switching losses are due predominantly to the level translation transistors. These losses are a function of the PWM frequency, the level translation current and pulse width and the bus and V_{CC} voltages. The level translation power dissipation then is:

$$P_{level\ trans.} = f_{PWM} \bullet (V_S + V_{CC}) \bullet 8 \times 10^{-9} \text{ Watts}$$

$$P_{TOTAL} = P_{STATIC} + P_{DRIVER} + P_{LEVEL\ TRANS}$$

APPNOTE

No. 9105.1 May 1992

Harris Intelligent Power

HVIC/IGBT HALF-BRIDGE CONVERTER EVALUATION CIRCUIT

The HVIC high voltage integrated circuit is designed to drive n-channel IGBTs or MOSFETs in a half-bridge configuration up to $500V_{DC}$. Power supply and motor control inverters can be configured for voltages up to $230V_{AC}$ using the HVIC, IGBTs and a few other components.

A few precautions should be taken in using the circuit. Lead lengths between the external power circuit (including gate and pilot leads), the 15V bypass capacitor (C_{DD}), the bootstrap diode (D_F) and capacitor (C_F) and the HVIC should be minimized.

The basic components required to evaluate the features of the SP601 are shown in the simplified schematic. The recommended load is largely resistive so that the largest current component will flow through the IGBTs, IGT1 and IGT2.

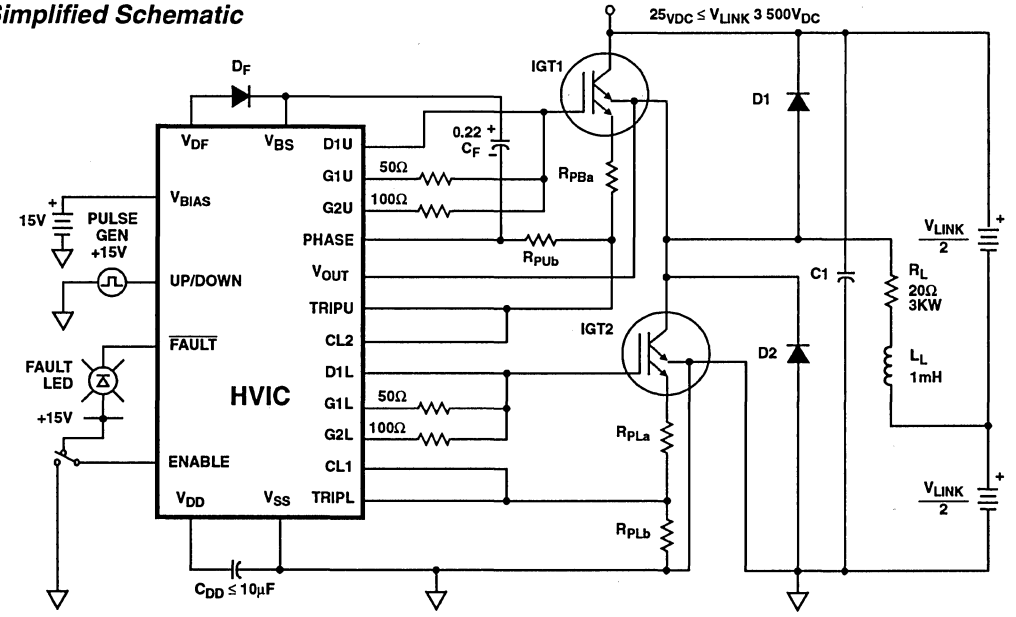
The flyback diodes, D1 and D2, rated 8A, will carry a much smaller flyback current component. A small amount of load inductance will cause the switching waveforms to simulate the conditions which would normally be observed with motor or transformer loads, while limiting the current carried by the lower rated flyback diodes in this circuit.

The values for R_{PUa}, R_{PUb}, etc., have been chosen to result in overcurrent trip at approximately 25Apk. At this level of current, heat sinking for the IGTs and flyback diodes is required. The series resistance of the upper and lower pilot resistor dividers would be approximately 1KΩ; the divider ratio should cause 0.1V at the tap at the desired trip current.

When first energizing your evaluation circuit, begin with a reduced bus voltage of about $20V_{DC}$ to $30V_{DC}$ to verify proper circuit operation before proceeding to higher voltages.

More specific information can be found in File Number 2428 and File Number 2429 Half-Bridge $500V_{DC}$ Driver data sheets and in the Application Note, AN-8829.1.

Simplified Schematic



HVIC - Harris Part # SP601 (Formerly GS601)
IGT1, 2 - Harris Part # HGTA24N60D1C
D1, 2 - Harris Part # RUR860
D_F - Harris Part # A114M
R_{PUa}, R_{PLa} - 910Ω, 1.8W
R_{PUb}, R_{PLb} - 68Ω, 1.8W
C1 - 0.1µF, $600V_{DC}$
R_L - 20Ω, 3KW 13 -50

Harris Semiconductor

APPNOTE

No. 9201 May 1992

Harris Intelligent Power™

PROTECTION CIRCUITS FOR QUAD AND OCTAL LOW SIDE POWER DRIVERS

Overview

Normally, the defined requirements for a Quad or Octal Driver are very much affected by the type of protection circuits used on the chip. Fault protection for an open or shorted load is an interactive function, making it important in the decision process of specifying the proper IC for an application. The various types of on-chip features may include protection for over-current, over-voltage and over-temperature. The response action to a fault condition may be either limiting or shutdown. Shutdown methods may include hysteresis and may require a logic reset. On-chip clamp diodes provide current steering to an external zener diode clamp as over-voltage protection from inductive switching pulses. Internal Zener diodes are also used to limit the output voltage on the output driver of the IC. In addition, fault detection is available with diagnostic feedback, including serial bus (SPI) control. All of the protection features noted are represented in the following list of Quad and Octal Low Side Drivers:

TABLE 1. QUAD & OCTAL LOW SIDE POWER DRIVERS

TYPE	DESCRIPTION	KEY FEATURES
CA3242	Quad Gated Inverting Power Dr.	Over-Current Latch-Off, Fast Fault Shut-Down, Output Protection Diodes
CA3262	Quad Gated Inverting Power Dr.	Over-Current Limiting, Over-Temperature Limiting
CA3262A	Quad Gated Inverting Power Dr.	Same as CA3262 plus +125°C Max. T_A
CA3272	Quad Gated Inverting Power Dr. with Fault Mode Diag. Flag Output	Over-Current & Temp. Limiting, Fault Flag Output, +125°C T_A
CA3282	Octal Driver with SPI Logic Control	Full Range of Protection & Fault Mode Feedback/Control with -40°C to +125°C T_A Range
CA3292	Quad Gated Inverting Power Dr. with Fault Mode Diag. Flag Output	Fault Flag Output, +125°C Max. T_A similar to the CA3272 except for added Over-Volt. Clamp Diodes
HIP0080	Quad Gated Inverting Power Drs.	Over-Current (Latch-Off), Over-Temperature (Gates-Off), Open Load & Output Ground Short Detection with Fault Mode Feedback/Control and -40°C to +110°C T_A Range
HIP0081	Quad Gated Inverting Power Drs.	Same Features as HIP0080 except higher rated current drive

While the CA3282 Octal Driver is quite different from the quad drivers, it is included here because it is used in similar applications. The CA3282, HIP0080 and HIP0081 feature Power BiMOS with MOSFET Output Drivers for higher current and voltage capability. Because of the additional dissipation associated with these drivers, the CA3282 and HIP0081 are provided in a 15 pin SIP power package. The other Quad Drivers are available in the 16 pin DIP and/or 28 lead PLCC packages which have special construction for improved heat dissipation. All of these Low Side Switches generally share a common characteristic of 5V input CMOS or TTL logic level control.

The Quad and Octal Power Drivers include a wide variation of choice in selecting a device type. The available types are listed in TABLE 1 which also highlights the key parameters for most applications. By-type, the protection features of the Quad and Octal Drivers are listed in the table and are explained in the following detail of this IC Application Note to assist the user in making an intelligent device selection for the application of interest.

CA3242 Quad-Gated Inverting Power Driver

In normal use, the supply voltage is applied through a load to an NPN open collector output of the CA3242 quad driver. The functional block diagram is shown in Figure 1. The maximum current rating of 1 Amp does not distinguish between average and peak. Each output is independently protected and latches "OFF" when the load current exceeds the latch-off threshold in the "ON" state. The CA3242E feature of short circuit protection is a responsive high-speed shutdown of the output drive to a shorted load. Under worse-case shorted load conditions, the supply voltage is applied direct to the output device. The latch-off threshold is typically 1.3V ($I_{SC}R_{ON}$), where R_{ON} is the saturated "on" resistance of the output. The CA3242 latches "OFF" at a typical short circuit current of 1.2A with 25µs nominal delay. The ENABLE or the IN pin of the latch-tripped channel must be toggled to reset the latch.

TABLE 1. QUAD AND OCTAL DRIVER FEATURES

TYPE NO.	CA3242	CA3262	CA3262A	CA3272	CA3292	HIP0080	HIP0081	CA3282 (OCTAL DR)
TYPE OF OUTPUT	**INVERTING**	**INVERTING**	**INVERTING**	**INVERTING**	**INVERTING**	**INVERTING**	**INVERTING**	**LOGIC SELECT**
Output Current Rating V_{SAT} @ Current Rating R_{ON} Output Resistance	0.6A 0.8V	0.7A 0.6V	0.7A 0.6V	0.4A 0.4V	0.4A 0.4V	0.5A 1.0Ω	1.0A 0.5Ω	0.5A 0.5V
Voltage Rating (V_{CC})sus	$35V_{DC}$	$35V_{DC}$	$40V_{DC}$	$40V_{DC}$	$32V_{DC}$ (Clamp)	$35V_{DC}$ typ.	$79V_{DC}$ typ.	$32V_{DC}$ (Clamp)
Load Dump Voltage (V_{PEAK})	$80V_{PEAK}$	$80V_{PEAK}$	$80V_{PEAK}$	$80V_{PEAK}$	$80V_{PEAK}$	$80V_{PEAK}$	$80V_{PEAK}$	TBD
Output Current Limiting	No	@1.4A	@1.3A	@1.2A	@1.2A	1.5A	3A	@1.5A
Short-Circuit Protection	Yes Latches-OFF	No	No	No	No	Yes Latches-OFF	Yes Latches-OFF	Yes Latches-OFF
Thermal-Limiting	No	@ Tj= +155°C	@ T_J = +155°C	No	No	No	No	No
Thermal Shutdown	No	No	No	@ T_J = +165°C	@ T_J = +165°C	@ T_J = +150°C	@ T_J = +150°C	@ T_J = +170°C
Fault Indicator Flag	No	No	No	Yes	Yes	Yes	Yes	Yes
Diagnostic Feedback	No	No	No	No	No	Yes	Yes	Yes
Temperature Range -40°C to +85°C -40°C to +125°C	X	X	 X	 X	 X	 X	 X	 X
Package Options: 16 DIP (Std) 15 SIP 28 PLCC	 X X	 X	 X X	 X	 X	 X X	 X	 X

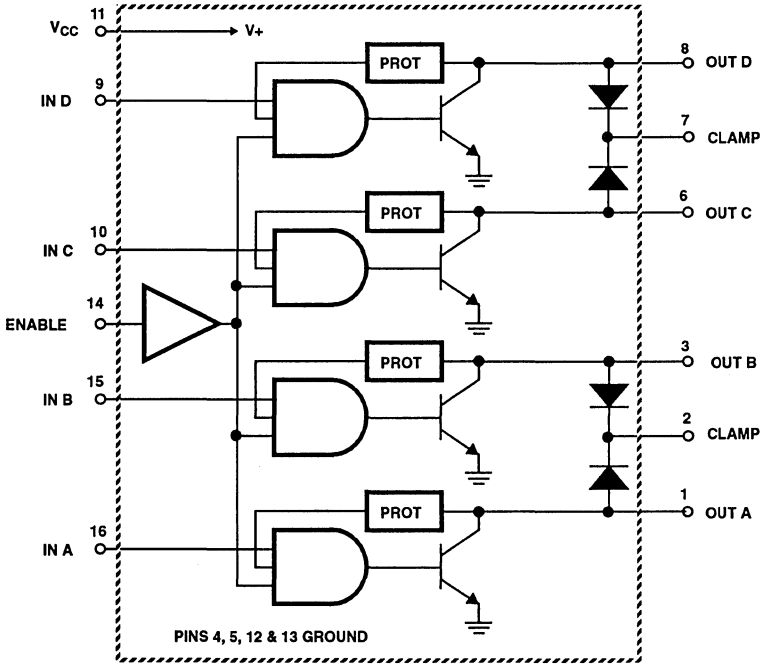


FIGURE 1. CA3242 FUNCTIONAL BLOCK DIAGRAM

Proper application of the CA3242E will aid in the save turnoff under shorted load conditions. Observation of wide ranging conditions have been done to test the shutdown behavior and has revealed several pitfalls that should be addressed to assure safe shutdown. One should be aware that a forced short circuit test condition may be considerably more severe than a normal application shorted load. In either case, two problems arise that affect the severity of the overload during shutdown. These are:

1. A shorted load is inductive and causes the generation of voltage spikes, exposing the output device to at least 2 times the value of the V+ supply voltage.
2. Lack of bypassing can provoke severe oscillations during the delay period before shutdown is complete. This is typically less than 25µs.

The result of this oscillation with an inductive load is to alternately stress the output device in both a forward and reverse direction at rates as high as 1mHz, lasting until shutdown occurs. This problem is compounded in some applications when 2 or more devices are used in parallel to increase drive output. In this case, a short may now draw twice the current of one driver which, in turn, results in almost twice the unclamped voltage spike developed across each output transistor.

To suppress oscillations during shutdown requires some attention to the use of adequate bypassing of both the +5V V_{CC} supply and the battery or output supply voltage. Bypassing the output supply will minimize both the transient oscillations and the voltage spike effects of lead inductance. Then, the shorted output is stressed in the forward bias mode with the shorted current determined by voltage source, duration of short, line resistance and the resistance of the saturated output. In a practical application, the load and any potential short may occur in a remote location. As such, bypassing the output supply may not be practical. Bypassing the d+5V supply with a 0.1µF capacitor closely wired to pins 11 and 12 of the CA3242E constitutes adequate bypassing of the +5V supply.

Because voltage spikes are normal to the application, a 30V zener "clamp" diode is needed to limit the device output voltage spikes to less than the maximum rating of 35V. The zener clamp diode protection should be closely wired to pins of the output divide in order to avoid any delay in the voltage clamping action. Alternatively, the on-chip diodes may be used in a free wheeling mode by connecting the CLAMP pins to the supply voltage if it does not exceed 30V during transients. Zener diode clamp protection is preferred over the power supply clamp option, primarily because the power supply may be subject to large transient changes.

CA3262 & CA3262A Quad-Gated Inverting Power Driver

The CA3262 is a quad-gated inverting low-side driver capable of switching 700mA load currents (at +25°C) in each output without interaction between the outputs. Shown in Figure 2, each output is independently protected with overcurrent limiting and over temperature limiting features. If an output load is shorted, the remaining three outputs function normally unless the junction temperature of their output device exceeds the over temperature limiting threshold of +155°C (typical). Current limiting prevents the output current from exceeding a value determined by the design (1.2A typical), independent of the load condition. The power dissipation of the shorted output driver is equal to the product of the limiting value of current and the applied output collector voltage. If this value causes the junction temperature to exceed +155°C (typical), the base drive to the output transistor, and thereby it's collector current, is reduced until the resulting power dissipation is equal to that value which maintains the junction temperature at the thermal limit value. The current which flows in the output transistor in a short circuit mode is therefore a function of the ambient temperature, the thermal resistance of the package in the application, the total power dissipated in the package. If the short is removed, normal operation resumes automatically.

In order to clamp high voltage pulses which may be generated by switching inductive energy in the load circuit, zener diodes with a value not greater than 30V should be connected to the CLAMP pins. On-chip diodes are connected from each output to one of the two CLAMP pins and are intended for use as steering diodes to provide a path for the clamped pulse current to a CLAMP pin; allowing the use of one zener diode to clamp all outputs. Alternatively, the on-chip diodes may be used in a free-wheeling mode by connecting the CLAMP pins to the supply voltage if it does not exceed 30V during transients. Zener diode clamp protection is preferred over the power supply clamp option, primarily because the power supply voltage may be subject to large transient changes. Note that the rate of change of the output current during switching is very fast. Therefore, even small values of inductance (such as the inductance of several meters of wire) in the load circuit can generate voltage spikes of considerable amplitude on the output terminals and may require clamping to prevent damage.

The CA3262A is a lower V_{SAT} version of the CA3262 and is rated for +125°C ambient temperature applications. The CA3262 is limited to about +100°C (data sheet rating at +85°C) ambient temperatures. Otherwise, the protection features described here apply to both versions. Figure 2 shows a functional block diagram for the CA3262 & CA3262A. Each type has independent current limiting and thermal limiting protection for each output driver. The maximum current rating of each output is specified as 1A. However, this is not a users choice rating, the current limiting is typically 1.2A with specified range limits of 0.7A to 1.8A.

The CA3262 and CA3272 will typically survive when shorted if the output supply voltage is less than 18V. This potential for failure is flagged in the data sheet as a note under the Electrical Characteristics table. It takes a few milliseconds to shutdown when the output is short circuited. During shutdown the dissipation may be excessive and is primarily determined by I_{SC} which is the limiting current. The short-circuit current will be limited by the CA3262 but the voltage that the shorted output sees may approach V_{SUPPLY}. Not considering transient effects, the worst case dissipation would be $P_D = (V_{SUPPLY})x(I_{SC})$. Normally, a shorted solenoid or relay will have a few Ω of impedance which should prevent cata-

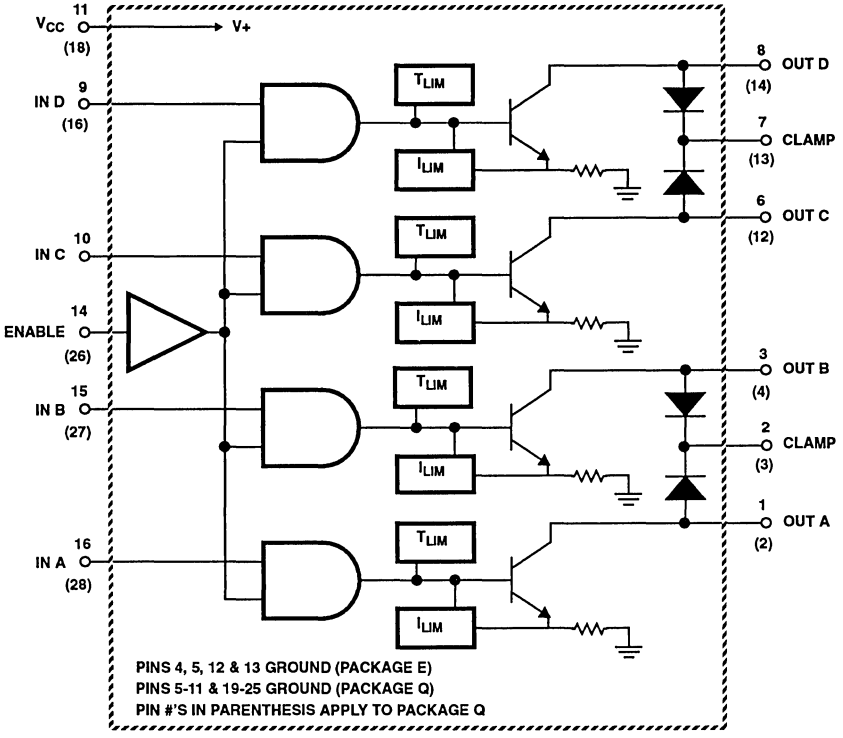


FIGURE 2. CA3262 AND CA3262A FUNCTIONAL BLOCK DIAGRAM

strophic IC failure in 12V automotive applications. A typical value for I_{SC} is 1.2A. R_{ON} is the saturated collector resistance of the output transistor with a typical value of 1Ω. V_{SUPPLY} is normally 9V to 16V in automotive applications. The thermal shutdown could be made faster but the circuit would not be able to effectively drive lamps which have a very low resistance in a cold start-up. Lamp drive capability is a common application use for the CA3262 and CA3262A.

CA3272 & CA3292 Quad-Gated Inverting Power Drivers with Fault Mode Flag

The CA3272 and CA3292 are quad-gated inverting low-side power drivers with a fault diagnostic flag output. Both circuits are rated for +125°C ambient temperature applications and have current limiting and thermal shutdown. As shown in Figure 3, they differ from the CA3262A by not having output clamp diodes but do have the diagnostic short-circuit flag outputs. Each output driver is capable of switching 400mA load currents at +125°C ambient without interaction between the outputs. Current limiting functions in the same manner as the CA3262 with a typical limit value of 1A. The current limiting range is set for 0.7A to 1.6A. While the thermal shutdown characteristics differ from the CA3262 by having hysteresis, the same precaution applies for potential damage from high transient dissipation during thermal shutdown. The CA3272Q and CA3292Q Quad Driver are provided in the 28 pin web-leadframe PLCC package. This package has slightly lower thermal resistance than the 16 pin web-leadframe package.

The CA3292 is equivalent to the CA3272 except that it has internal clamp diodes on the outputs to handle inductive switching pulses from the output load. Expanded functional block diagram detail of the fault logic is similar to that of the CA3272 as shown in Figure 4(b) with the exceptions noted in the output driver circuit. The structure of each output, shown in Figure 4(a), includes a zener diode from collector-to-base of the output transistor. This is a different form of protection than the CA3242 or CA3262 which have current steering clamp diodes on each output, paired to one of two "CLAMP" output pins. The CA3292 output transistor will turn-on at the clamp voltage threshold which is typically 35V and the output transistor will dump the pulse energy through the output driver to ground.

Each of the output are independently protected with overcurrent limiting and over-temperature shutdown with thermal hysteresis. If an output is shorted, the remaining outputs function normally unless the temperature rise of the other output devices can be made to exceed their shutdown temperature of +165°C (typical). When the junction temperature of a driver exceeds the +165°C thermal shutdown value, that output is turned off. When and output is shutdown, the resulting decrease in power dissipation allows the junction

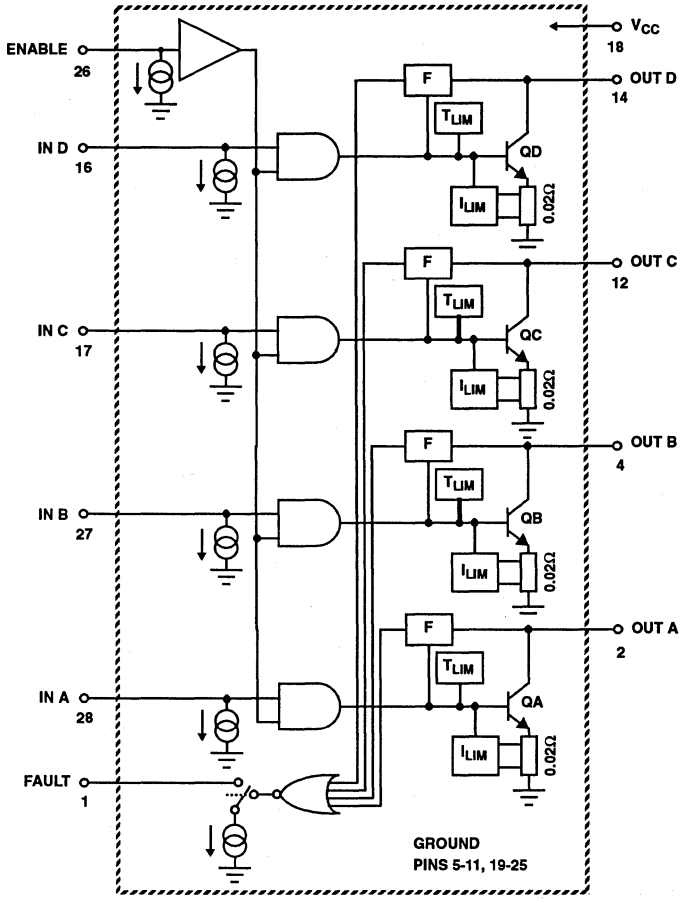
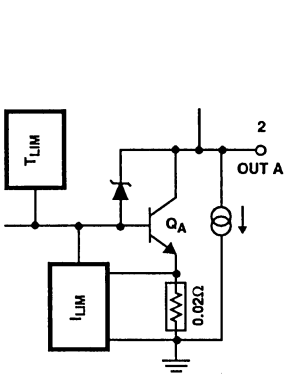


FIGURE 3. CA3272 FUNCTIONAL BLOCK DIAGRAM

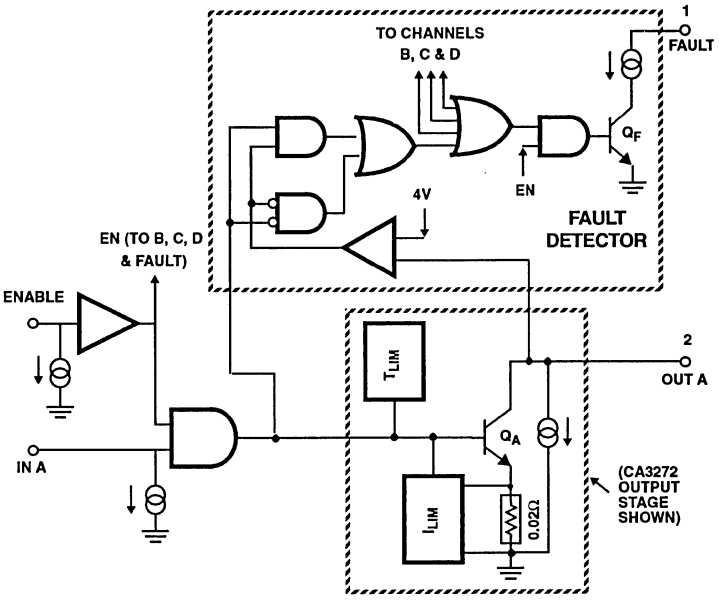
temperature to decrease. When the junction temperature decreases by approximately +15°C, the output is turned on. The output will continue to turn on and off for as long as the shorted condition exists or until shutdown by the input logic. The resulting frequency and duty cycle of the output current flow is determined by the ambient temperature, the thermal resistance of the package in the application, the total power dissipation in the package. Since each output is independently protected, the frequency and duty cycle of the current flow into multiple shorted outputs will not be related in time. Long lead lengths in the load circuit may lead to oscillatory behavior if more than two output loads are shorted.

A diagnostic flag indicates when an output is shorted. This information can be used as input to a microprocessor or dedicated logic circuit to provide a fast switch-off when a short occurs and also to determine by sequence action, which output is shorted. A fault condition in any output load will cause the FAULT output to switch to a logic "low". Added detail of the fault logic is shown in Figure 4(b). Since a fault condition will be indicated during switching, use of an appropriate size capacitor to filter the FAULT output is recommended (see data sheet). This will prevent the FAULT output voltage from reaching a logic level "0" within the maximum switching time. The FAULT detection circuitry compares the state of the input and the state of the output. The output is considered to be in a high state if the voltage exceeds the typical FAULT threshold reference voltage, V_{THD} of 4V. If the output voltage is less than V_{THD}, the output is considered to be in a low state. For example, if the input is high and the output is less than V_{THD}, a normal "ON" condition exists and the FAULT output is high. If the input is high and the output is greater than V_{THD}, a shorted load condition is indicated and the FAULT output is low. When the input is low and the output is greater than V_{THD}, a normal "OFF" condition is indicated and the FAULT output is high. If the input is low and the output is less than V_{THD}, an open load condition exists and the FAULT output is low. The FAULT output is disabled when the ENABLE input logic level is low.



(a) CA3292 OUTPUT STAGE

The CA3292 is similar to the CA3272 except that each output stage has a zener diode voltage clamp to limit inductive switching pulses



(b)

The FAULT DETECTOR of the CA3272Q is shown here in an equivalent logic block diagram form. Channel A is one of 4 power switching functions displayed in the diagram. Transistor Q_A is the protected power transistor switch that drives the "OUT A" terminal. The dotted block illustrates the logic block associated with the FAULT DETECTOR. The ENABLE input is common to each of the 4 power switches and also disables the FAULT output when it is low. From the "IN A" input to the "OUT A" output, the switch condition is inverting (NAND). When IN is high, OUT is low. The FAULT DETECTOR senses the IN and OUT states and switches QF "ON" if a fault is detected. Transistor Q_F activates a sink current source to pull-down the FAULT pin to a 0 (low) state when the fault is detected. Both shorted and open load conditions are detected.

FIGURE 4. FAULT DETECTION FUNCTIONAL BLOCK DIAGRAM OF THE CA3272 & CA3292

To detect an open load, each output has an internal low-level current sink which acts as a pull-down under open load fault conditions and is always active. The magnitude of this current plus any leakage associated with the output transistor will always be less than 100µA. (The data sheet specification for I_{CEX} includes this internal low-level sink current). The output load resistance must be chosen such that the voltage at the output will not be less than V_{THD} when the I_{CEX} sink current flows through it under worse case conditions with minimum supply voltage. For example, assume a 6V minimum driver output supply voltage, a FAULT threshold reference voltage of V_{THD} = 5V and an output current sink of I_{CEX} = 100µA. Calculate the maximum load resistance that will not result in a FAULT output low state when the output is OFF.

$$R_{LOAD}(max) = [V_{SUPPLY}(min) - V_{THD}(max)] / I_{CEX}(max)$$

$$R_{LOAD}(max) = (6V - 5V) / 100\mu A = 10K\Omega$$

Since the CA3272 does not have on-chip diodes to clamp voltage spikes which may be generated during inductive switching of the load circuit, external zener diodes (30V or less) should be connected between the output terminal and ground. Only those outputs used to switch inductive loads require this protection. Note that since the rate of change of output current is very high, even small values of inductance can generate voltage spikes of considerable amplitude on the output terminals which may require clamping. External free-wheeling diodes returned to the supply voltage are generally not acceptable as inductive clamps if the supply voltage exceeds 30V during transients.

CA3282 Power BiMOS Driver with a Serial Peripheral Interface

The CA3282 is a logic controlled Power Driver with a Serial Peripheral Interface (SPI). The chip is fabricated in a Power BiMOS process with high voltage and current drive capability. A functional block diagram is shown in Figure 5. There is an extensive amount of logic circuitry to provide individual diagnostic feedback; including which output may be shorted. Each of the open collector output drivers has individual protection for over-current and overvoltage; and, each output has sepa-

rate output latch control. The current limiting of the CA3282 is set for a range of 1A to 2A (1A min.). In the normal ON state, each output driver is in a saturated low state. Comparators in the diagnostic circuit monitor the drain of the output drivers to determine if an out-of-saturation condition exists. If a comparator senses a voltage higher than the threshold trip level of 3V typical, the latch control circuit is reset (unlatched) and the respective output driver is shutdown. The on-chip current limiting protection is independent of the diagnostic feedback loop. If an over-current condition exists, the condition may be sustained unless the diagnostic circuit senses a fault condition or the over-temperature shutdown threshold is exceeded.

Maximum current ratings allow all eight outputs to be turned on to a level of 0.5A. This is allowed because the CA3282 chip is packaged in 15 pin SIP power package with 3°C/W typical junction-to-case thermal resistance, allowing high dissipation capability in ambient temperatures up to 125°C. The thermal shutdown junction temperature threshold is set for 165°C. The CA3282 has on-chip thermal limiting, but not on an independent output basis. The limited physical separation of 8 outputs on a chip does not afford the same convenient and economical spacing needed for individual thermal sensing and shutdown circuits that is achieved on the quad driver chips. The CA3282 output driver structure consists of an N-FET with a zener diode feedback from the drain to gate, forming an overvoltage clamp structure for protection from voltage spikes generated when switching inductive loads. The pulse energy is shunted to ground through the N-FET output driver.

HIP0080 & HIP0081 Quad Power MOSFET Output Drivers with Diagnostic Interface

The HIP0080 & HIP0081 are low side power switches fabricated in a Power BiMOS process technology. They can typically sustain higher voltage and current capability than that which can be achieved in Power Bipolar. Except for package and pinout differences, both circuits are functionally the same and are shown in the functional block diagram of Figure 6. The HIP0080 is intended to sustain 0.5A of drive with all outputs "ON" while the HIP0081 can sustain 1A of output drive with all outputs "ON" and 3A maximum on each output. The output drivers are voltage rated up to the clamp level set by drain-to-gate zener diodes and typically clamp at 80V. A 15 pin SIP power package is used to achieve maximum capability for the HIP0081 while the HIP0080 is available in the 28 pin PLCC WEB lead frame package.

The diagnostic monitoring and feedback process of the HIP0080 & HIP0081 is different from the CA3272 & CA3292 and the CA3282. Each output device is independently toggled on or off through a driver interface circuit that is, in part, controlled by over-current and over-temperature diagnostic feedback. The conditions on each output device are monitored to sense over-current, over-temperature, open-load and output-ground shorting. Four separate bits for each of the four outputs are loaded into a 16 bit serial diagnostic register. The diagnostic information is accessed with a low on the chip select pin and the clock input. Both datain and dataout pins are available to allow cascade operation. The first bit in the data readout is a fault error flag which is high if any one of the following 16 bits indicate a fault condition. When chips are cascaded, the error flags are cascaded and a fault condition is immediately evident if there is a fault on any chip. Although, all bits must be read to determine where, if any, the fault condition exists.

Another part of the diagnostic feedback circuits provides for digital delay filtering to prevent short transient over-current and output voltage readings from loading the diagnostic register with false data. Each output is sensed with a window comparator to determine whether the output is high, low or centered. A resistor divider consisting of two 10KΩ resistors set a centered (V_{CC} 1/2) output voltage level for reference. When a centered reading is detected with the driver output off. The centered reading is sensed as a no load condition on the output. If the window comparator senses a low reading when the driver output is off, the result is interpreted as a short to ground. The results are passed through a digital delay filter and are transmitted to the diagnostic shift register. The over-current sense

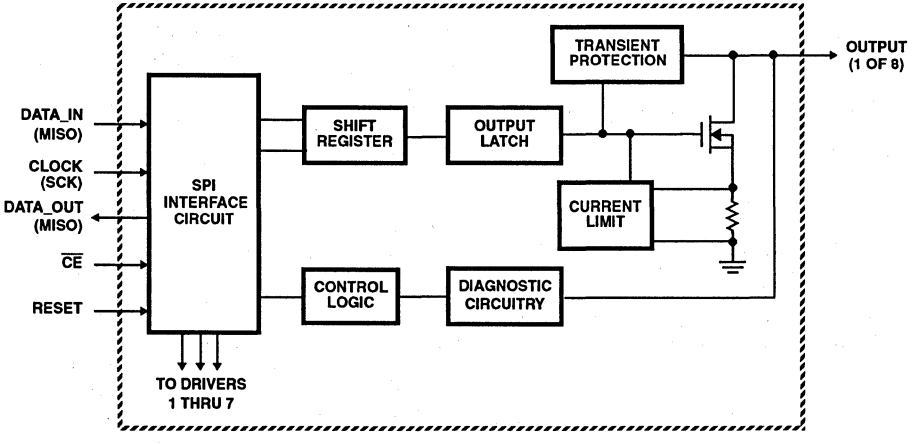


FIGURE 5. CA3282 BLOCK DIAGRAM FOR ONE OF EIGHT DRIVER STAGES

level is read from a metal source-to-ground resistance in each output by a comparator that senses the voltage as a current. When an over-current level is detected, the result is sent through a digital delay filter to the diagnostic shift register and also toggles a latch circuit in the drive control which cuts-off drive to the output stage. Where a shorted condition exists, the short must be removed and the input toggled off and on to reset normal operation. If an over-temperature condition is sensed, the feedback result is fed directly back to the input control stage to gate-off drive to the output stage while also loading the diagnostic shift register. Normal chip operation may resume when the chip is sufficiently cooled. There is a typical +15°C hysteresis shift intended by design to provide a cooling cutoff period.

Summary

While this information on the protective structures of the Quad & Octal Power Drivers should be helpful, it must also be recognized that the design of the application circuit should be consistent with performance requirements. Generally, the data sheets define parameters in terms of each separate switch. Although the data sheets do not specify parallel switch ratings and limits, the switches may be used in parallel to increase current drive capability. Also, there are a number of design considerations that will impact the continuing performance and reliability of the IC. The protective features of the Quad & Octal Drivers discussed here provide for a substantial gains by reducing the potential for catastrophic failure in the application. To gain a better insight into the device on-chip functions, the function block diagrams have been included here. Additional detail can be found in the data sheet for each type.

References

1. CA3262, CA3272 "Mission Possible" and "MAP" distributed Automotive Brochures provided a document titled "Quad Power Drivers", No. BR-002. This publication gives additional information on quad drivers, including curves on thermal limiting and shutdown for the CA3262 and CA3272 with detail on survival time versus voltage on the power output drivers.
2. CA3262 - PCIM June 1988 article titled "Current and Temperature Limiting Protect Power Switch Driver Outputs" which has shutdown timing information to show the independent action of shutdown plus other application detail.

For reference, the data sheet file numbers are listed by type as follows:

TYPE	NO.	TYPE	NO.
CA3242	1561	CA3282	2767
CA3262, CA3262A	1836	CA3292	2946
CA3272	2223	HIP0080, HIP0081	3018

Acknowledgments

The material presented here has been written by Wayne Austin, Intelligent Power Product Applications of the Harris Automotive Design Center, Somerville, NJ with contributions from Tom DeShazo, Lou Pennisi, Bob Kumbatovic.

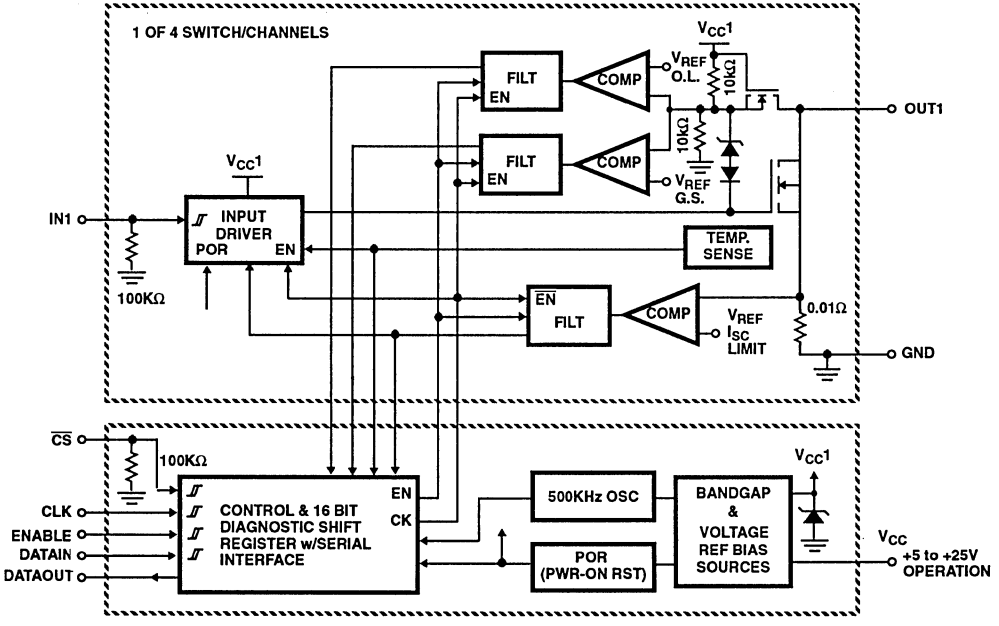


FIGURE 6. FUNCTIONAL BLOCK DIAGRAM OF THE HIP0080 AND HIP0081

INTELLIGENT POWER ICs 11

HARRIS QUALITY AND RELIABILITY

Harris Quality & Reliability

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of The Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX programs and working with manufacturing to establish control charts, Quality professionals are involved in the measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

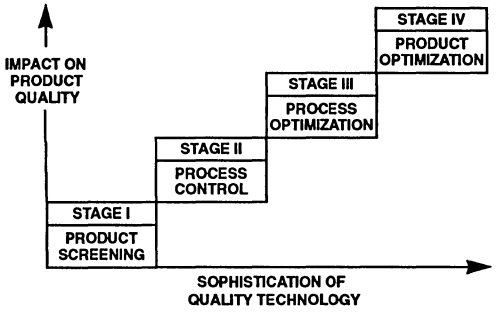


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage II to Stage III, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

Harris Standard Flows

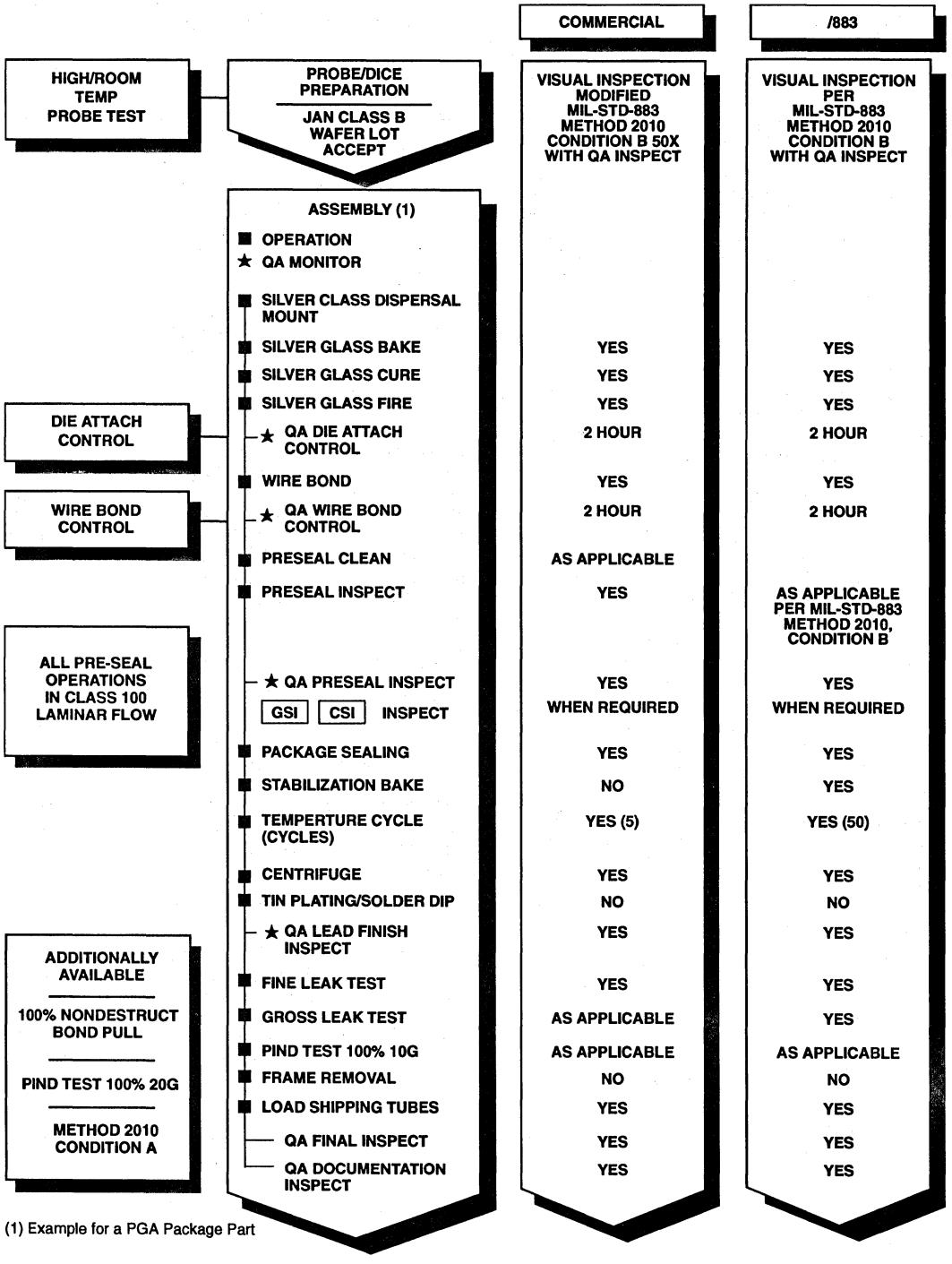
Harris Semiconductor offers a variety of standard product flows which cover the myriad of application environments our customers experience. These flows run the gamut of low cost commercial parts to fully qualified JAN microcircuits. All of these grades have one thing in common. They result from meticulous attention to quality, starting with design decisions made during product development and ending with the labeling of shipping containers for delivery to our customers. The standard flows offered are:

Commercial: Electrical performance guaranteed from $0^{o}C$ to $+70^{o}C$

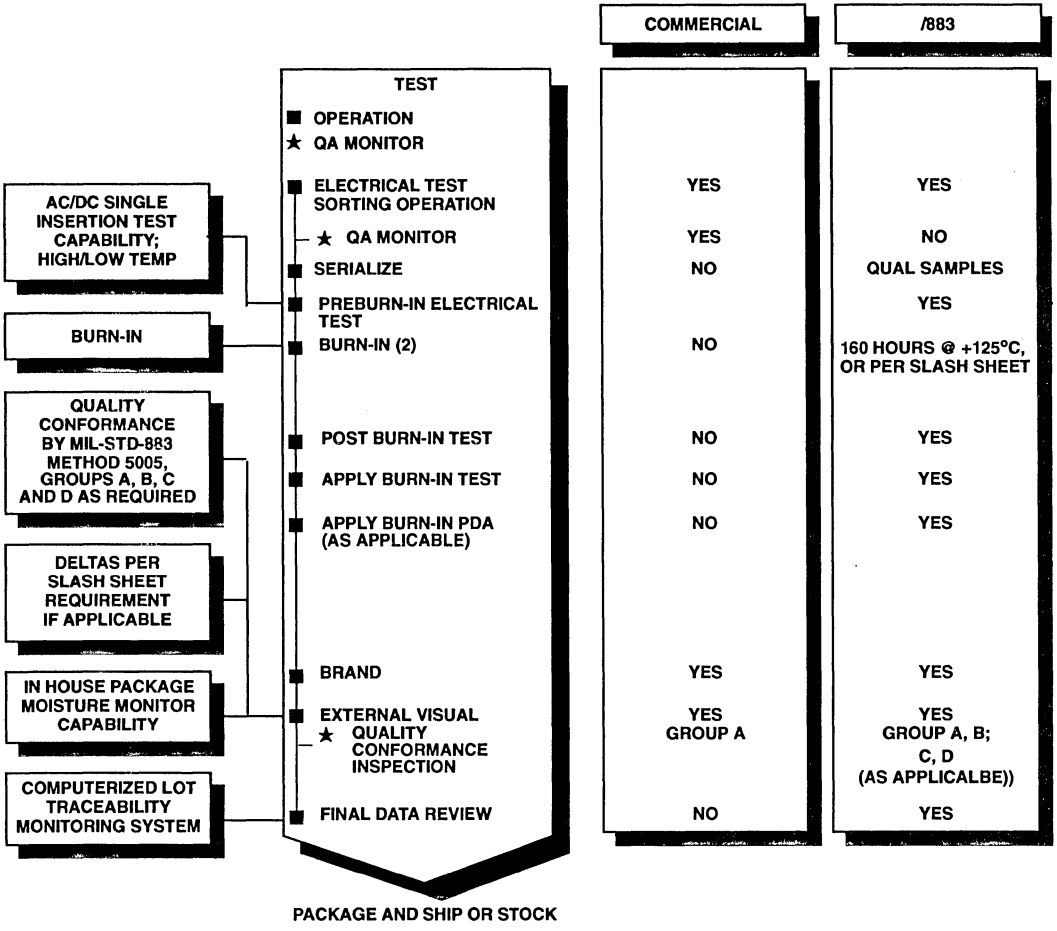
/883: Mil-Std-883 compliant product: contact the factory or local Harris Sales Office for details on availability and specifications

Details of the individual process requirements are contained in the flow charts on the following pages.

Harris Semiconductor Standard Processing Flows



(1) Example for a PGA Package Part



(2) Burn-in test temperatures can be increased and time reduced per regression tables in Mil-Std-883, Method 1015

Advantages of Standard Flows

Wherever feasible, and in accordance with good value engineering practice, the IC user should specify device grades based on one of the five standard Harris manufacturing flows. These are more than adequate for the overwhelming majority of applications and may be utilized quite effectively if the user engineer bases designs on the standard data sheet, military drawing or slash sheet (as applicable) electrical limits.

Some of the more important advantages gained by using standard as opposed to custom flows are as follows:

- Lower cost than the same or an equivalent flow executed on a custom basis. This results from the higher efficiency achieved with a constant product flow and the elimination of such extra cost items as special fixturing, test programs, additional handling and added documentation.
- Faster delivery. The manufacturer often can supply many items from inventory and, in any case, can establish and maintain a better product flow when there is no need to restructure process and/or test procedures.
- Increased confidence in the devices. A continuing flow of a given product permits the manufacturer to mointor trends which may bear on end-product performance or reliability and to implement corrective action, if necessary.

Reduction of risk. Since each product is processed independent of specific customer orders, the manufacturer absorbs production variability within its scheduling framework without major impact on deliveries. In a custom flow, a lot failure late in the production cycle can result in significant delays in delivery due to the required recycling time.

Despite the advantages of using standard flows, there are cases where a special or custom flow is mandatory to meet design or other requirements. In such cases, the Harris Marketing groups stand ready to discuss individual customer needs and, where indicated, to accomodate appropriate custom flows.

Measurement

Analytical Services Laboratory

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies. The capabilities of each area are shown below.

SPECTROSCOPIC METHODS: Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

CHROMATOGRAPHIC METHODS: Gas Chromatography, Ion Chromatography.

THERMAL METHODS: Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

PHYSICAL METHODS: Profilometry, Microhardness, Rheometry.

CHEMICAL METHODS: Volumetric, Gravimetric, Specific Ion Electrodes.

ELECTRON MICROSCOPE: Transmission Electron Microscopy, Scanning Electron Microscope.

X-RAY METHODS: Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

SURFACE ANALYSIS METHODS: Scanning Auger Microprobe, Electron Spectroscope/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories, and can obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

Calibration Laboratory

Another important resource in the product assurance system is Harris Semiconductor's Calibration Lab. This area is responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both the production and engineering areas. The accuracy of instruments used at Harris in calibration is traceable to the National Bureau of Standards. The lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Field Return Product Analysis System

The purpose of this system is to enable Harris' Field Sales and Quality operations to properly route, track and respond to our customers' needs as they relate to product analysis. The Product Failure Analysis Solution Team (PFAST) consists of the group of people who must act together to provide timely, accurate and meaningful results to customers on units returned for analysis. This team includes the salesman or applications engineer who gets the parts from the customer, the PFAST controller who coordinates the response, the Product or Test Engineering people who obtain characterization and/or test data, the analysts who failure analyze the units, and the people who provide the ultimate corrective action. It is the coordinated effort of this team, through the system described in this document that will drive the Customer responsiveness and continuous improvement that will keep Harris on the forefront of the semiconductor business.

The system and procedures define the processing of product being returned by the customer for analysis performed by Product Engineering, Reliability Failure Analysis and/or Quality Engineering. This system is designed for processing "sample" returns, not entire lot returns or lot replacements.

The philosophy is that each site analyzes its own product. This applies the local expertise to the solutions and helps toward the goal of quick turn time.

Goals: quick, accurate response, uniform deliverable (consistent quality) from each site, traceability.

The PFAST system is summarized in the following steps:

1) Customer calls the sales rep about the unit(s) to return.
2) Fill out PFAST Action Request see the PFAST form in this section. This form is all that is required to process a Field Return of samples for failure analysis. This form contains essential information necessary to perform root cause analysis. (See Figure 2).
3) The units must be packaged in a manner that prevents physical damage and prevents ESD. Send the units and PFAST form to the appropriate PFAST controller. This location can be determined at the field sales office or rep using "look-up" tables in the PFAST document.
4) The PFAST controller will log the units and route them to ATE testing for data log.
5) Test results will be reviewed and compared to customer complaint and a decision will be made to route the failure to the appropriate analytical group.
6) The customer will be contacted with the ATE test results and interim findings on the analysis. This may relieve a line down situation or provide a rapid disposition of material. The customer contact is valuable in analytical process to insure root cause is found.
7) A report will be written and sent directly to the customer with copies to sales, rep, responsible individuals with corrective actions and to the PFAST controller so that the records will capture the closure of the cycle.

8) Each report will contain a feedback form (stamped and preaddressed) so that the PFAST team can assess their performance based on the customers assessment of quality and cycle time.

9) The PFAST team objectives are to have a report in the customers hands in 28 days, or 14 days based on agreements. Interim results are given realtime.

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. (See Figures 3 and 4). Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

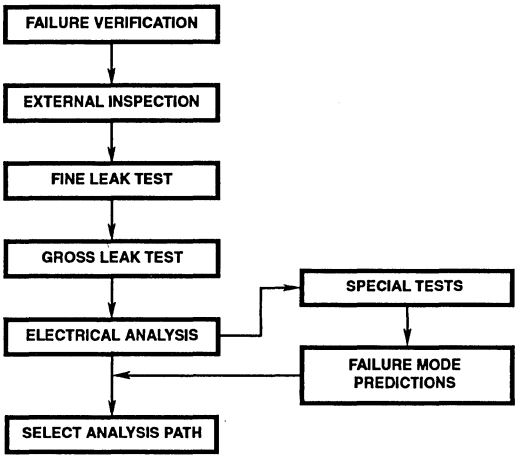


FIGURE 3. NON-DESTRUCTIVE

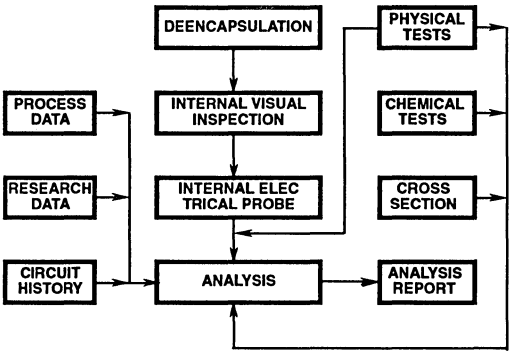


FIGURE 4. DESTRUCTIVE

HARRIS SEMICONDUCTOR

Request # _____
Customer Analysis # _____

PFAST ACTION REQUEST

Date: _____

ORIGINATOR _____	CUSTOMER _____
LOCATION/PHONE NO. _____	LOCATION _____
DEVICE TYPE/PART NO. _____	PURCHASE ORDER NO. _____
NO. SAMPLES RETURNED _____	QUANTITY RECEIVED _____

THE COMPLETENESS AND TIMELY RESPONSE OF THE EVALUATION IS DIRECTLY RELATED TO THE COMPLETENESS OF THE DATA PROVIDED. PLEASE PROVIDE ALL PERTINENT DATA. ATTACH ADDITIONAL SHEETS IF NECESSARY.

TYPE OF PROBLEM

1. ☐ INCOMING INSPECTION
   - ☐ 100% SCREEN ☐ SAMPLE INSPECTION
   - NO. TESTED _____ NO. OF REJECTS _____
   - ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   - ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF EVALUATION AND RESULTS ATTACHED
2. ☐ IN PROCESS/MANUFACTURING FAILURE
   - ☐ BOARD CHECKOUT ☐ SYSTEM CHECKOUT
   - ☐ FAILED ON TURN-ON
   - ☐ FAILED AFTER _____ HOURS OPERATION
   - WAS UNIT RETESTED UNDER INCOMING INSPECTION CONDITIONS? ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF HOW FAILURE WAS ISOLATED TO COMPONENT ATTACHED
3. ☐ FIELD FAILURE
   - FAILED AFTER _____ HOURS OPERATION
   - ESTIMATED FAILURE RATE _____% PER 1000 HOURS
   - END USER _____ LOCATION _____
   - AMBIENT TEMPERATURE _____ C
   - MIN. _____ C MAX. _____ C
   - REL. HUMIDITY _____ %
   - ☐ END USER FAILURE CORRESPONDENCE ATTACHED

ACTION REQUESTED BY CUSTOMER

SPECIFIC ACTION REQUESTED _____

IMPACT OF FAILED UNITS ON CUSTOMER'S SITUATION: _____

CUSTOMER CONTACTS WITH SPECIFIC KNOWLEDGE OF REJECTS

NAME _____

POSITION _____ PHONE _____

DETAILS OF REJECT

(Where appropriate serialize units and specify for each)

TEST CONDITIONS RELATING TO FAILURE
- ☐ TESTER USED (MFGR/MODEL) _____
- ☐ TEST TEMPERATURE _____
- ☐ TEST TIME: ☐ CONTINUOUS TEST ☐ ONE SHOT (T = _____ SEC)
- ☐ DESCRIPTION OF ANY OBSERVED CONDITION TO WHICH FAILURE APPEARS SENSITIVE: _____

1. ☐ DC FAILURES
   - ☐ OPENS ☐ SHORTS ☐ LEAKAGE ☐ STRESS
   - ☐ POWER DRAIN ☐ INPUT LEVEL ☐ OUTPUT LEVEL
   - ☐ LIST OF FORCING CONDITIONS AND MEASURED RESULTS FOR EACH PIN IS ATTACHED
   - ☐ POWER SUPPLY SEQUENCING ATTACHED
2. ☐ AC FAILURES
   - LIST FAILING CHARACTERISTICS _____
   - ADDRESS OF FAILING LOCATION (IF APPLICABLE) _____
   - ATTACHED:
   - ☐ LIST OF POWER SUPPLY AND DRIVER LEVELS (Include pictures of waveforms).
   - ☐ LIST OF OUTPUT LEVELS AND LOADING CONDITIONS
   - ☐ INPUT AND OUTPUT TIMING DIAGRAMS
   - ☐ DESCRIPTION OF PATTERNS USED (If not standard patterns, give very complete description including address sequence).
3. ☐ PROM PROGRAMMING FAILURES
   - ADDRESS OF FAILURES _____
   - PROGRAMMER USED (MFG/MODEL/REV. NO.) _____
4. ☐ PHYSICAL/ASSEMBLY RELATED FAILURES
   - ☐ SEE COMMENTS BELOW ☐ SEE ATTACHED

Additional Comments:

FIGURE 2. PFAST ACTION REQUEST

Reliability

Reliability Assessment and Enhancement

At Harris Semiconductor, reliability is built into every product by emphasizing quality throughout manufacturing. This starts by ensuring the excellence of the design, layout, and manufacturing process. The quality of the raw materials and workmanship is monitored using statistical process control (SPC) to preserve the reliability of the product. The primary and ultimate goal of these efforts is to provide full performance to the product specification throughout its useful life. Product reliability is maintained through the following sources: Qualifications, In-Line Reliability Monitors, Failure Analysis.

Qualifications

Qualifications at Harris de-emphasize the sole dependence on production product which is only available late in the development cycle. The focus is primarily on the use of test vehicles to establish design ground rules for the product and the process that will eliminate any wearout mechanisms during the useful life of the product. However, to comply with the military requirements concerning reliability, product qualifications are performed. (See Figure 5).

In-line Reliability Monitors

In-line reliability monitors provide immediate feedback to manufacturing regarding the quality of workmanship, quality of raw materials, and the ultimate reliability implications. The rudimentary implementation of this monitoring is the "First Line of Defense," which is a pass/ fail acceptance procedure based on control charts and trend analysis. The second level of monitoring is referred to as the "Early Warning System" and incorporates wafer level reliability concepts for extensive diagnostic and characterization capabilities of various components that may impact the device reliability or stability. The quick feedback from these schemes allows more accurate correlation to process steps and corrective actions.

Product/Package Reliability Monitors

Reliability of finished product is monitored extensively under a program called Matrix I, II, III monitor. All major technologies are monitored.

Matrix I Has a higher sampling size and rate per week and uses short duration test, usually less than 48 hours to assess day to day, week to week reliability. High volume types are prevalent in this data. Stresses Operating Life, Static Life and HAST. T_A = +125°C to +200°C

Matrix II Longer duration test, much like requalification. The sample sizes are reduced in number and frequency, yet meet or exceed the JEDEC Standard 29. Stresses Operating Life, Storage, THB, Autoclave, Temp Cycle, and Thermal Shock.

Matrix III Package specific test. Tests Solderability, Lead Fatigue, Physical Dimensions, Brand Adhesion, Flammability, Bond Pull, Constant Acceleration, and Hermeticity. Data from these Monitor Stress Test provides the following information:

- Routine reliability monitoring of products by die technology and package styles.
- Data base for determining FIT Rates and Failures Mode trends used drive Continuous Improvement.
- Major source of reliability data for customers.
- Customers have used this data to qualify Harris products.

Reliability Fundamentals

Reliability, by its nature, is a mixture of engineering and probability statistics. This combination has derived a vocabulary of terms essential for describing the reliability of a device or system. Since reliability involves a measurement of time, it is necessary to accelerate the failures which may occur. This, then, introduces terms like "activation energy" and "acceleration factor," which are needed to relate results of stressing to normal operating conditions (see Table 1). Also, to assess product reliability requires failures. Therefore, only a statistical sample can be used to determine the model of the failure distribution for the entire population of product.

Failure Rate Calculations

Reliability data for products may be composed of several different failure mechanisms and requires careful combining of diverse failure rates into one comprehensive failure rate. Calculating the failure rate is further complicated because failure mechanisms are thermally accelerated at varying rates and thereby have differing accelerating factors. Additionally, this data is usually obtained a variety of life tests at unique stress temperatures. The equation below accounts for these considerations and then inserts a statistical factor to obtain the confidence interval for the failure rate.

$$FIT = \left(\sum_{i=1}^{B} \frac{X_i}{k \sum_{j=1} TDH_j \; AF_{ij}} \right) \times 10^9 \times M$$

B = # of distinct possible failure mechanisms

K = # of life tests being combined

Xi = # of failures for a given failure mechanism i = 1, 2, . . . B

TDGj = Total device hours of test time (unaccelerated) for Life Testj

AFij = Acceleration factor for appropriate failure mechanism i = 1, 2, . . . K

M = Statistical factor for calculating the upper confidence limit (M is a function of the total number of failures and an estimate of the standard deviation of the failure rates)

In the failure rate calculation, Acceleration Factors (AF_{ij}) are used to derate the failure rate from thermally accelerated Life Test conditions to a failure rate indicative of use temperatures. Though no standards exist, a temperature of +55°C has been popular and allows some comparison of product failure rates. All Harris Semiconductor Reliability Reports will derate to +55°C at both the 60% and 95% confidence intervals.

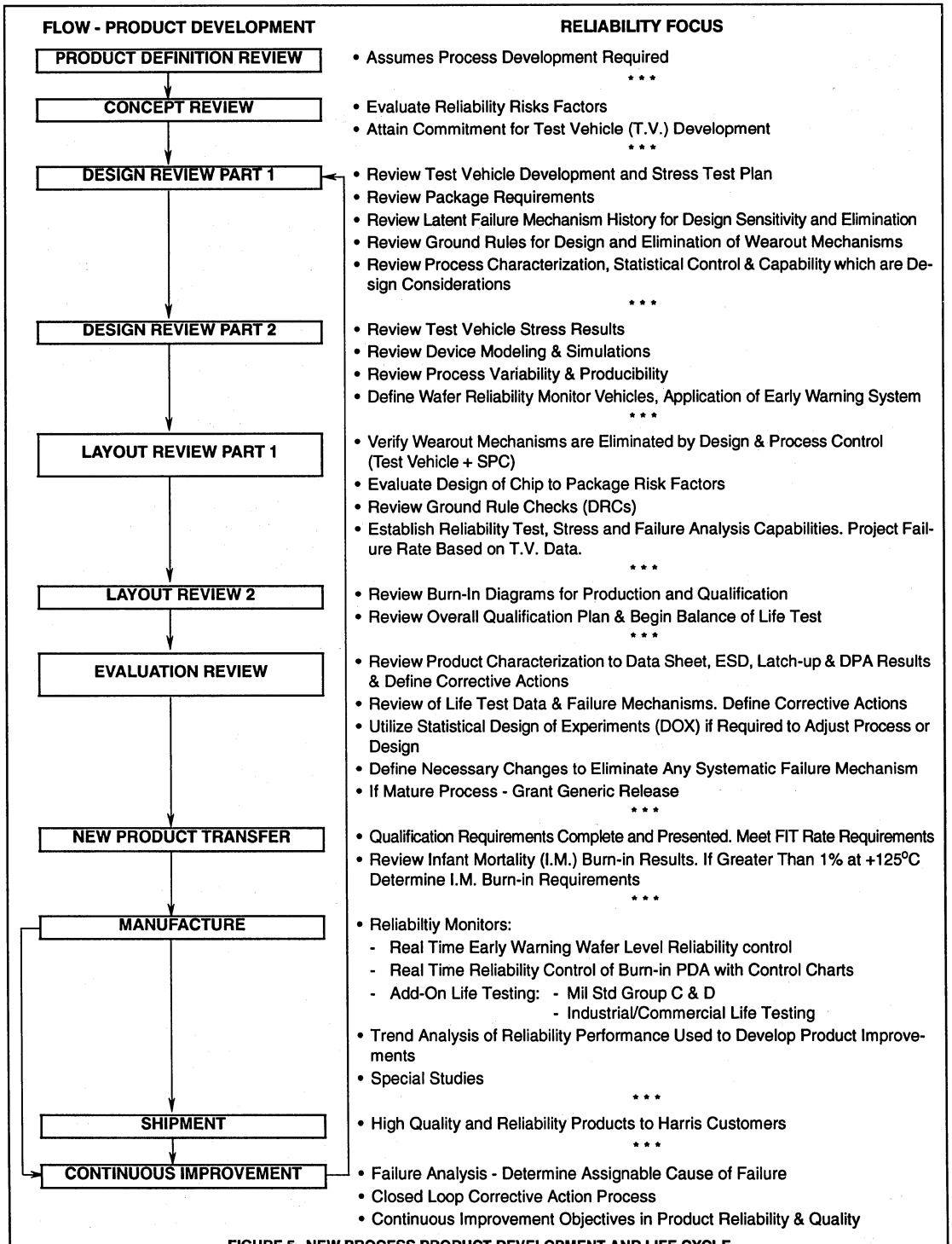


FIGURE 5. NEW PROCESS PRODUCT DEVELOPMENT AND LIFE CYCLE

Acceleration Factors

The Acceleration Factors (AF) are determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and is an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP \left[\frac{Ea}{K} \left(\frac{1}{T_{use}} - \frac{1}{T_{stress}} \right) \right]$$

AF = Acceleration Factor

E_a = Thermal Activation Energy in eV from Table 8

K = Boltzmann's Constant (8.62×10^{-5} eV/°K)

Both Tuse and Tstress (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature. With the use of the Arrhenius Equation, the thermal Activation Energy (Ea) term is a major influence on the result. This term is usually empirically derived and can vary widely.

TABLE 1. FAILURE RATE PRIMER

GLOSSARY OF TERMS

TERMS/DEFINITIONS	UNITS/DESCRIPTION
FAILURE RATE λ For Semiconductors, usually expressed in FITs. Represents useful life failure rate (which implies a constant failure rate). FITs are not applicable for infant mortality or wearout failure rate expressions.	**FIT - Failure In Time** 1 FIT - 1 failure in 10^9 device hours. Equivalent to 0.0001%/1000 hours FITs = $\frac{\#\ \text{Failures}}{\#\ \text{Devices x \# hours stress x AF}} \times 10^9 \times m$ m - Factor to establish Confidence Interval 10^9 - Establishes in terms of FITs AF - Acceleration Factor at temperature for a given failure mechanism
MTTF - Mean Time To Failure For semiconductors, MTTF is the average or mean life expectancy of a device. If an exponential distribution is assumed then the mean time to fail of the population will be when 63% of the parts have failed.	Mean Time is measured usually in hours or years. 1 Year = 8760 hours When working with a constant failure rate the MTTF can be calculated by taking the reciprocal of the failure rate. MTTF = $1/\lambda$ (exponential model) Example: =10 FITs at +55°C The MTTF is: MTTF = $1/\lambda = 0.1 \times 10^9$ hours = 100M hours
CONFIDENCE INTERVAL (C. I.) Establishes a Confidence Interval for failure rate predictions. Usually the upper limit is most significant in expressing failure rates.	Example: "10 FITs @ a 95% C. I. @ 55°C" means *only* that you are 95% certain the the FITs <10 at +55°C use conditions.

Activation Energy

To determine the Activation Energy (Ea) of a mechanism (see Table 2) you must run at least two (preferably more) tests at different stresses (temperature and/or voltage). The stresses will provide the time to failure (Tf) for the populations which will allow the simultaneous solution for the Activation Energy by putting the experimental results into the following equations.

$$\ln (t_{f1}) = C + \frac{E_a}{KT_1} \qquad \ln (tf_2) = C + \frac{E_a}{KT_2}$$

Then, by subtracting the two equations, the Activation Energy becomes the only variable, as shown.

$$\ln(t_{f1}) - \ln(t_{f2}) = E_a/k(1/T1-1/T2)$$

$$E_a = K^* ((\ln(t_{f1}) - \ln(t_{f2}))/(1/T1 - 1/T2))$$

The Activation Energy may be estimated by graphical analysis plots. Plotting ln time and ln temperature then provides a convenient nomogram that solves (estimates) the Activation Energy.

Table 3 is a summary for the L7 process.

All Harris Reliability Reports from qualifications and Group C1 (all high temperature operating life tests) will provide the data on all factors necessary to calculate and verify the reported failure rate (in FITs) using the methods outlined in this primer.

Qualification Procedures

New products are reliably introduced to market by the proper use of design techniques and strict adherence to process layout ground rules. Each design is reviewed from its conception through early production to ensure compliance to minimum failure rate standards. Ongoing monitoring of reliability performance is accomplished through compliance to 883C and standard Quality Conformance Inspection as defined in Method 5005.

New process/product qualifications have two major requirements imposed. First is a check to verify the proper use of process methodology, design techniques, and layout ground rules. Second is a series of stress tests designed to accelerate failure mechanisms and demonstrate the reliability of integrated circuits.

From the earliest stages of a new product's life, the design phase, through layout, and in every step of the manufacturing process, reliability is an integral part of every Harris Semiconductor product. This kind of attention to detail "from the ground up" is the reason why our customers can expect the highest quality for any application.

TABLE 2. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles Statistical Process Control or photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test (EWS) and HTOL.	Statistical Process Control C-V data, oxide/interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

TABLE 3. HIGH TEMPERATURE OPERATING LIFE TEST SUMMARY

GENERIC GROUP	GROUP NAME	PROCESS DESCRIPTION	QUANITY	QUANTITY FAILURE	HOURS @ 125°C	FAILURE RATE FITs @ 55°C 60% CI
C-105-5	Microprocessor and Peripherals	SAJI CMOS L7	1452	0	5.72 E + 06	2

Harris High Reliability Product Specification Highlights

Harris Semiconductor is a leading supplier of high reliability integrated circuits to the military and aerospace community and takes pride in offering products tailored to the most demanding applications requirements. Our Manufacturing facilities are JAN-Certified to MIL-M-38510 and provide JAN-qualified and MIL-STD-883 compliant products as standard data book items. This DSP Data Book contains detailed information on high-reliability integrated circuits presently available from Harris Semiconductor.

The intent of the /883 data sheet is to provide to our customers a clear understanding of the testing being performed in conformance with MIL-STD-883 requirements. Additionally, it is our intent to provide the most effective and comprehensive testing feasible.

Document Control

Harris has established each of the /883 data sheets as an internally revised controlled document. Any product revision or modification must be approved and signed-off throughout the manufacturing and engineering sections. Harris has made every effort to ensure accuracy of the information in this data book through quality control methods. Harris reserves the right to make changes to the products contained in this data book to improve performance, reliability and producibility. Each data sheet will use the printed date as the revision control identification. Contact Harris for the latest available specifications and performance data.

/883 Data Sheet Highlights

Each specific /883 data sheet documents the features, description, pinouts, tested electrical parameters, test circuits, burn-in circuits, die characteristics, packaging and design information. The following are notes and clarifications that will help in applying the information provided in the data sheet.

Absolute Maximum Ratings: These ratings are provided as maximum stress ratings and should be taken into consideration during system design to prevent conditions which may cause permanent damage to the device. Operation of the device at or above the "Absolute Maximum Ratings" is not intended, and extended exposure may affect the device reliability.

Reliability Information: Each /883 data sheet contains thermal information relating to the package and die. This information is intended to be used in system design for determining the expected device junction temperatures for overall system reliability calculations.

Packaging: Harris utilizes MIL-M-38510, Appendix C for packages used for /883 products. The mechanical dimensions and materials used are shown for each individual product to complete each data sheet as a self contained document.

D.C. and A.C. Electrical Parameters: Tables 1 and 2 define the D.C. and A.C. Electrical Parameters that are 100% tested in production to guarantee compliance to MIL-STD-883. The subgroups used are defined in MIL-STD-883, Method 5005 and designated under the provisions of Paragraph 1.2.1a. Test Conditions and Test Circuits are provided for specific parameter testing.

Table 3 provides additional device limits that are guaranteed by characterization of the device and are not directly tested in production. Characterization takes place at initial device design and after any major process or design changes. The characterization data is on file and available demonstrating the test limits established.

Table 4 provides a summary of the test requirements and the applicable MIL-STD-883 subgroups.

Burn-in Circuits: The Burn-in circuits defined in the individual data sheets are those used in the actual production process. Burn-in is conducted per MIL-STD- 883, Method 1015.

Design Information Sections: Harris provides an additional Design Information Section in many of the data sheets to assist in system application and design. This information may be in the form of applications circuits, typical device parameters, or additional device related user information such as programming information. While this information cannot be guaranteed, it is based on actual characterization of the product and is representative of the data sheet device.

High Reliability Products Information

Harris' High Reliability Products are all produced in accordance with military specifications and standards, primarily MIL-M-38510 (General Specifications for Microcircuits) and MIL-STD-883 (Test Methods and Procedures for Microelectronics).

MIL-STD-883 contains test methods and procedures for various electrical, mechanical and environmental tests as well as requirements for screening, qualification and quality conformance inspection. Method 5004 of MIL-STD-883 lists the 100% screening tests which are required for each of the product assurance classes defined above.

Following the device screening, samples are removed from the production lot(s) for Quality Conformance Inspection testing. This testing is divided into four inspection groups: A, B, C and D, which are performed at prescribed intervals per MIL-M-38510 to assure the processes are in control and to ensure the continued quality level of the product being produced.

Group A electrical inspection involves dynamic, static, functional and switching tests at maximum, minimum and room operating temperatures. Sample sizes and specific tests performed depend upon the particular product assurance class chosen. Electrical test sampling is performed on all subgroups as defined in MIL-STD-883, Method 5005.

Group B inspection includes tests for marking permanency, internal visual and mechanical correctness, bond strength, and solderability. It is intended to provide assurance of the absence of lot-to-lot fabrication and manufacturing variances. Group B tests are again defined in test Method 5005.

Group C is oriented toward die integrity and consists of operating life testing as defined in MIL-STD-883, Method 5005.

Group D environmental testing is provided to verify die and package reliability. Among the Group D tests are lead integrity, hermeticity, temperature cycling, thermal and mechanical shock, and constant acceleration.

MIL-M-38510 requires that Group A and Group B inspection be performed on each lot, while Group C inspection must be done every 3 months and Group D every 6 months to be in compliance with MIL-M-38510 JAN requirements. To limit the amount of testing, MIL-M-38510 allows the multitude of micro- circuits to be grouped by technology, commonly known as "generic families". Thus, one group C performed will cover all parts included in that generic family for three months. For Group D, which is package related, although there are some restrictions, one Group D performed on a 24-pin ceramic dual-in-line packaged part will cover all devices in the same package regardless of the technology group.

For MIL-STD-883 products, Groups A and B are required on each lot, Groups C and D are required every 52 weeks by generic die family and package fabricated and manufactured from the same plant as the die and package represented.

General Test Philosophy

The general philosophy for test set development is to supply test software that guarantees the high performance and quality of the products being designed and manufactured by Harris. The general final test set includes a guardbanded initial test program and a QA test program for the quality test step. Characterization software is an additional test program that parametrically measures and records the performance of the device under test. This test set is used to evaluate the performance of a product and to determine the acceptability of non-standard Source Control Drawings. BSPEC and RSPEC test programs are custom final test programs written to conform to customer specifications.

The general test development strategy is to develop software using a "shell" programming technique which creates standard test program flows, and reduces test development and execution times. Statistically derived guardbands are utilized in the "shell" programs to null out test system variability. High performance hardware interface designs are incorporated for maximized test effectiveness, and efficient fault graded vector sets are utilized for functional and AC testing.

The initial step in generating the test set is the test vector generation. The test vectors are the binary stimulus applied to the device under test to functionally test the operation of the product. The vectors are developed against a behavioral model that is a software representation of the device functionality. The output of the behavioral model can be translated directly to ATE test vectors or prepared for CAD simulation.

The philosophy in the generation of test vectors is to develop efficient fault graded patterns with a goal of greater than 90% fault coverage. There is no intent to generate a worst case or best case noise vector set. The intent is to maximize fault coverage through efficient vector use. Generally only one vector set will be required to enable complete test coverage within a given test program.

Exceptions to this would be vector generation to test certain identified critical AC speed paths or DC vectors for testing VIH/VIL parameters. These vector sets typically will not increase fault coverage and can not be substituted for fault graded vector sets.

The ultimate goal for testing all /883 products is data sheet compliancy, thoroughness, and quality of testing. By taking this approach to test set generation, Harris is capable of supplying high performance semiconductors of the highest quality to the marketplace.

Non-Standard Product Offerings

Harris understands the need for customer generated Source Control Drawings with non-standard parameter and/or screening requirements. A Customer Engineering Department is responsible for efficiently expediting your SCDs through a comprehensive review process. The Customer Engineering Group compares your SCD to its closest equivalent grade device type and works closely with the Product Engineer, Manufacturing Engineer, Design Engineer, or applicable individual to compare Harris' screening ability against your non-standard requirement(s). For product processed to non-standard requirements, a unique part number suffix is assigned.

Harris shares the military's objective to utilize standards wherever possible. We recommend using our /883 data sheet as the guideline for your SCD's. In instances where an available military specification or Harris /883 datasheet is inappropriate, it is Harris' sincerest wish to work closely with the buyer in establishing an acceptable procurement document. For this reason, the customer is requested to contact the nearest Harris Sales Office or Representative before finalizing the Source Control Drawing. Harris looks forward to working with the customer prior to implementation of the formal drawing so that both parties may create a mutually acceptable procurement document.

IC Handling Procedures

Harris IC processes are designed to produce the most rugged products on the market. However, no semiconductor is immune from damage resulting from the sudden application of many thousands of volts of static electricity. While the phenomenon of catastrophic failure of devices containing MOS transistors or capacitors is well known, even bipolar circuits can be damaged by static discharge, with altered electrical properties and diminished reliability. None of the common IC internal protection networks operate quickly enough to positively prevent damage.

It is suggested that all semiconductors be handled, tested, and installed using standard "MOS handling techniques" of proper grounding of personnel and equipment. Parts and subassemblies should not be in contact with untreated plastic bags or wrapping material. High impedance IC inputs wired to a P.C. connector should have a path to ground on the card.

Handling Rules

Since the introduction of integrated circuits with MOS structures and high quality junctions, a safe and effective means of handling these devices has been of primary importance. One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry. In addition, most compensation networks in linear circuits are located at high impedance nodes, where protection networks would disturb normal circuit operation. If static discharge occurs at sufficient magnitude (2kV or more), some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment. Thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. It is evident, therefore, that proper handling procedures or rules should be adopted.

Elimination or reduction of static charge can be accomplished as follows:

- Use static-free work stations. Static-dissipative mats on work benches and floor, connected to common point ground through a 1MV resistor, help eliminate static build-up and discharge. Do not use metallic surfaces.
- Ground all handling equipment.
- Ground all handling personnel with a conductive bracelet through 1MV to ground (the 1MV resistor will prevent electroshock injury to personnel). Transient product personnel should wear grounding heel straps when conductive flooring is present.
- Smocks and clothing of certain insulating materials (notably nylon) should not be worn in areas where devices are handled. These materials, highly dielectric in nature, will hold, or aid in the generation of a static charge. Where they cannot be eliminated, natural materials such as cotton should be used to minimize charge generation capacity. Conductive smocks are also available as an alternative.
- Control relative humidity to as high a level as practical. 50% is generally considered sufficient. (Operations should cease if R.H. falls below 25%).
- Ionized air blowers reduce charge build-up in areas where grounding is not possible or practical.
- Devices should be in conductive static-shielded containers during all phases of transport. Leads may be shorted by tubular metallic carriers, conductive foam, or foil.
- In automated handling equipment, the belts, chutes, or other surfaces should be of conducting non-metal material. If this is not possible, ionized air blowers or ionizing bars may be a good alternative.

ESD Handling Procedures

Harris has developed a static control program that enables employees to detect problems generated by static electricity whether on site, in transit, or in the field. Controlling the requirements, methods, materials, and training for static protection of our products is ongoing and updated with new developments in electrostatic prevention. Harris has responded with controls and procedures as part of daily operations to be followed in all areas.

The challenge is to insure all electrostatic control procedures are followed throughout the system - from manufacturing through end use. Unprotected integrated circuits can be destroyed or functionally altered by merely passing them through the electrostatic field of something as simple as Styrofoam<tm> or human contact.

Measures of Protection and Prevention

When handling static sensitive devices, three standard procedures must be followed:

1. Prior to any handling of static-sensitive components, the individual must be properly grounded.
2. All static-sensitive components must be handled at static safeguarded work stations.
3. Containers and packing materials that are static-protective must be used when transporting all static-sensitive components.

Special handling equipment (static-safeguarded work stations, conductive wrist straps, static-protected packaging, ionized air blowers) should be used to reduce damaging effects of electrostatic fields and charges.

Static-safeguarded work station is an area that is free from all damaging electricity, including people. To accomplish this, static on conductors and nonconductors must be controlled.

Controlling electrically conductive items can be accomplished by bonding and grounding techniques. The human body is considered a conductor of electricity and is by far the greatest generator of static electricity. Personnel handling ICs must use conductive wrist straps to ground themselves. Simple body moves act like a variable capacitor, and can create static charges. In addition, conductive clothing is recommended for minimizing electrostatic build up.

Static protective packaging prevents electric field from influencing or damaging ICs. An effective static-protective package exhibits three types of features:

1. Antistatic protection that prevents triboelectric or frictional charging,
2. Dielectric protection that insulates discharging, and
3. Shielding or Faraday cage protection that prevents transient field penetration.

Harris uses only packaging that exhibits all three features. Employees are required to adhere to the same static-protective packaging techiques during handling and shipment to assure device integrity is maintained.

Ionized air blowers aid in neutralizing charges on nonconductors such as synthetic clothing, plastics, and Styrofoam™. The blowers are placed at the work site and in close proximity to the IC handling area, since nonconductors do not lose or drain charges using normal grounding techniques.

By using wrist straps, static-protected work stations and static-protected containers, Harris product quality is maintained throughout the product cycle.

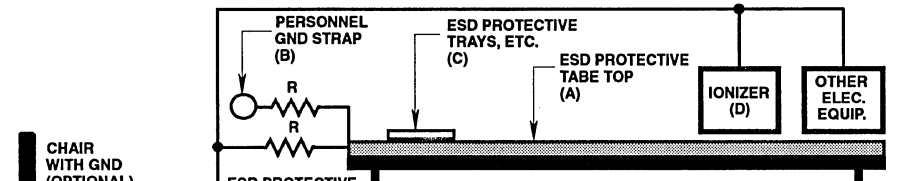


FIGURE 2. STATIC-SAFEGUARDED WORK STATION

NOTES:

1. All electrical equipment on the conductive table top must be hard grounded and isolated from the table top.
2. Earth ground is not computer ground or RF ground or any other limited ground.

Styrofoam™ is a trademark of Dow Chemical Corporation

Harris Semiconductor

TechBrief

No. 52 March 1992

Harris Digital

ELECTROSTATIC DISCHARGE CONTROL A GUIDE TO HANDLING INTEGRATED CIRCUITS

This paper discusses methods and materials recommended for protection of ICs against ESD damage or degradation during manufacturing operations vulnerable to ESD exposure. Areas of concern include dice prep and handling, dice and package inspection, packing, shipping, receiving, testing, assembly and all operations where ICs are involved.

All integrated circuits are sensitive to electrostatic discharge (ESD) to some degree. Since the introduction of integrated circuits with MOS structures and high quality junctions, safe and effective means of handling these devices have been of primary importance.

If static discharge occurs at a sufficient magnitude, 2kV or greater, some damage or degradation will usually occur. It has been found that handling equipment and personnel can generate static potentials in excess of 10kV in a low humidity environment; thus it becomes necessary for additional measures to be implemented to eliminate or reduce static charge. Avoiding any damage or degradation by ESD when handling devices during the manufacturing flow is therefore essential.

ESD Protection and Prevention Measures

One method employed to protect gate oxide structures is to incorporate input protection diodes directly on the monolithic chip. However, there is no completely foolproof system of chip input protection in existence in the industry.

In areas where ICs are being handled, certain equipment should be utilized to reduce the damaging effects of ESD. Typically, equipment such as grounded work stations, conductive wrist straps, conductive floor mats, ionized air blowers and conductive packaging materials are included in the IC handling environment. Any time an individual intends to handle an IC, in any way, they must insure they have been grounded to eliminate circuit damage.

Grounding personnel can, practically, be performed by two methods. First, grounded wrist straps which are usually made of a conductive material, such as Velostat or metal. A resistor value of 1 megohm (1/2 watt) in series with the strap to ground completes a discharge path for ESD when the operator wears the strap in contact with the skin. Another method is to insure direct physical contact with a grounded, conductive work surface.

This consists of a conductive surface like Velostat, covering the work area. The surface is connected to a 1 megohm (1/2 watt) resistor in series with ground.

In addition to personnel grounding, areas where work is being performed with ICs, should be equipped with an ionized air blower. Ionized air blowers force positive and negative ions simultaneously over the work area so that any nonconductors that are near the work surface would have their static charge neutralized before it would cause device damage or degradation.

Relative humidity in the work area should be maintained as high as practical. When the work environment is less than 40% RH, a static build-up condition can exist on nonconductors allowing stored charges to remain near the ICs causing possible static electricity discharge to ICs.

Integrated circuits that are being shipped or transported require special handling and packaging materials to eliminate ESD damage. Dice or packaged devices should be in conductive carriers during all phases of transport and handling. Leads of packaged devices can be shorted by tubular metalic carriers, conductive foam or foil.

Do's and Don'ts for Integrated Circuit Handling

Do's

Do keep paper, nonconductive plastic, plastic foams and films or cardboard off the static controlled conductive bench top. Placing devices, loaded sticks or loaded burn-in boards on top of any of these materials effectively insulates them from ground and defeats the purpose of the static controlled conductive surface.

Do keep hand creams and food away from static controlled conductive work surfaces. If spilled on the bench top, these materials will contaminate and increase the resistivity of the work area.

Do be especially careful when using soldering guns around conductive work surfaces. Solder spills and heat from the gun may melt and damage the conductive mat.

Do check the grounded wrist strap connections daily. Make certain they are snugly fitted before starting work with the product.

Do put on grounded wrist strap before touching any devices. This drains off any static build-up from the operator.

Do know the ESD caution symbols.

Do remove devices or loaded sticks from shielding bags only when grounded via wrist strap at grounded work station. This also applies when loading or removing devices from the antistatic sticks or the loading on or removing from the burn-in boards.

Do wear grounded wrist straps in direct contact with the bare skin never over clothing.

Do use the same ESD control with empty burn-in boards as with loaded boards if boards contain permanently mounted ICs as part of driver circuits.

Do insure electrical test equipment and solder irons at an ESD control station are grounded and only uninsulated metal hand tools be used. Ordinary plastic solder suckers and other plastic assembly aids shall not be used.

Do use ionizing air blowers in static controlled areas when the use of plastic (nonconductive) materials cannot be avoided.

Don'ts

Don't allow anyone not grounded to touch devices, loaded sticks or loaded burn-in boards. To be grounded they must be standing on a conductive floor mat with conductive heel straps attached to footwear or must wear a grounded wrist strap.

Don't touch the devices by the pins or leads unless grounded since most ESD damage is done at these points.

Don't handle devices or loaded sticks during transport from work station to work station unless protected by shielding bags. These items must never be directly handled by anyone not grounded.

Don't use freon or chlorinated cleaners at a grounded work area.

Don't wax grounded static controlled conductive floor and bench top mats. This would allow build-up of an insulating layer and thus defeating the purpose of a conductive work surface.

Don't touch devices or loaded sticks or loaded burn-in boards with clothing or textiles even though grounded wrist strap is worn. This does not apply if conductive coats are worn.

Don't allow personnel to be attached to hard ground. There must always be 1 megohm series resistance (1/2 watt between the person and the ground).

Don't touch edge connectors of loaded burn-in boards or empty burn-in boards containing permanently mounted driver circuits when not grounded. This also applies to burn-in programming cards containing ICs.

Don't unload stick on a metal bench top allowing rapid discharge of charged devices.

Don't touch leads. Handle devices by their package even though grounded.

Don't allow plastic "snow or peanut" polystyrene foam or other high dielectric materials to come in contact with devices or loaded sticks or loaded burn-in boards.

Don't allow rubber/plastic floor mats in front of static controlled work benches.

Don't solvent-clean devices when loaded in antistatic sticks since this will remove antistatic inner coating from sticks.

Don't use antistatic sticks for more than one throughput process. Used sticks should not be reused unless recoated.

Recommended Maintenance Procedures

Dally:

Perform visual inspection of ground wires and terminals on floor mats, bench tops, and grounding receptacles to ensure that proper electrical connections via 1 megohm resistor (1/2 watt) exist.

Clean bench top mats with a soft cloth or paper towel dampened with a mild solution of detergent and water.

Weekly:

Damp mop conductive floor mats to remove any accumulated dirt layer which causes high resistivity.

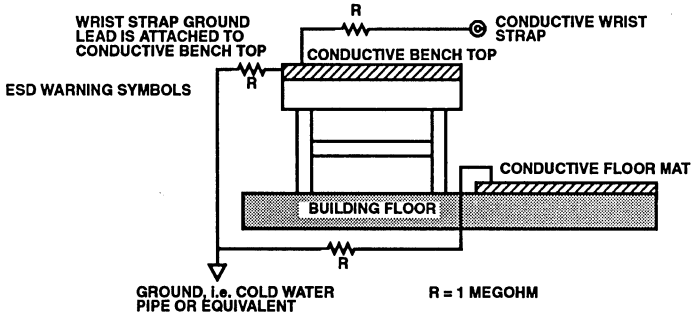
Annually:

Replace nuclear elements for ionized air blowers.

Review ESD protection procedures and equipment for updating and adequacy.

Static Controlled Work Station

The figure below shows an example of a work bench properly equipped to control electro-static discharge. Note that the wrist strap is connected to a 1 megohm resistor. This resistor can be omitted in the setup if the wrist strap has a 1 megohm assembled on the cable attached.



RR001.1 April 1992

Reliability Report

HIGH VOLTAGE INTEGRATED CIRCUIT (HVIC) RELIABILITY QUALIFICATION

By Erwin A. Herr

Strategy

The application requirements of the SP600 and the SP601 HVIC in a general industrial environment were reviewed and the desired properties of the HVIC to meet these requirements were identified. These properties were grouped into four main categories:

1. Semiconductor die bulk and surface stability,
2. Sealed junction integrity,
3. Thermal, mechanical and environmental stability,
4. Long term reliability.

It was desirable to demonstrate these properties of the HVIC with several key accelerated tests on a timely basis.Therefore, an analysis was made of several accelerated stresses that would assure the properties. Based on this analysis and previous experience the stresses chosen included: High Temperature Bias (HTB), High Temperature Storage, Damp Heat Bias, Temperature Cycling and Vibration Fatigue. The device properties and the accelerated stresses to assure them are shown in Figure 1. The objectives of each of the accelerated tests are shown in Figure 2. Also this analysis was used to design the Qualification Plan. A description of the accelerated tests used in this plan and the results of the tests are shown in Figure 3.

DEVICE PROPERTIES	HIGH TEMP BIAS	HIGH TEMP STORAGE	DAMP HEAT BIAS	TEMP CYCLE	VIBRATION FATIGUE
Die Bulk and Surface Stability	X	X	X		
Sealed Junction Integrity	X		X	X	
Thermal, Mechanical Environmental Stability	X	X	X	X	X
Long Term Reliability	X	X	X	X	X

FIGURE 1. TESTS REQUIRED TO ASSURE DEVICE PROPERTIES

Production of the HVIC's was initiated as a result of passing these qualifications. A Quarterly Product Monitor Plan was implemented to measure and control the reliability of the product during production. The tests in this plan are illustrated in Figure 4.

Technical Approach Taken to Determine the Expected Annual Field Failure Rate

There was also a need to determine the expected reliability in field applications based on these accelerated test results. An estimate of the expected annual field failure rate at application conditions was calculated for the first year. This was based on the favorable results of the accelerated qualification tests and the expected results from the quarterly monitor tests. The acceleration multipliers between the HTB stress levels and the application stress levels were determined by multi-level testing. This is an example of how these accelerated results can be used to predict the product reliability under application conditions.

In order to calculate the expected annual reliability or field failure rate the following information is needed:

1. Application stress conditions,
2. Reliability model to be used,
3. The acceleration multipliers between the test and the application conditions.

ACCELERATED STRESSES	STRESS OBJECTIVES
High Temperature Bias (HTB)	Die bulk and surface stability under electrical bias and elevated temperature conditions.
High Temperature Storage	Device physical and chemical stability under accelerated high temperature.
Damp Heat Bias (DHB)	Device physical and surface stability and package material compatibility under accelerated electrical bias, temperature and humidity.
Temperature Cycling	Device mechanical strength and durability under accelerated conditions of thermal expansion and contraction.
Vibration Fatigue	Ability of the mechanical parts of the device to withstand accelerated forces and low frequency vibration.

FIGURE 2. OBJECTIVES OF THE ACCELERATED STRESSES

STRESS HIGH TEMPERATURE BIAS V = 400V, 15V. T_J = +125°C	SAMPLES FROM PRODUCTION LOTS	CUMULATIVE FAILURES/SAMPLE SIZE HOURS UNDER STRESS			
		168	500	1000	2000
(1991)	120	0/120	0/120	0/120	--
	400	1/400 (Note 3) --	2/400 (Note 3) --	2/400 (Note 3) 1/400 (Note 4)	--
	240	0/240	1/240 (Note 4)	1/240 (Note 4)	1/240 (Note 4)
SUB TOTAL	760 (Note 1)	--	--	--	--
V = 450V,15V. T_J = +125°C (1990)	90 (Note 2)	0/90	0/90	0/90	0/90
HIGH TEMPERATURE STORAGE T_A = +150°C	100 (Note 2)	0/100	0/100	0/100	--
DAMP HEAT BIAS(DHB) V = 300V,15V. +85°C, 81% RH	100 (Note 2)	1/100 (Note 5)	1/100 (Note 5)	1/100 (Note 5)	--
TEMPERATURE CYCLING -40°C/+25°C/+150°C 27/3/27 minutes		CYCLES OF STRESS			
		100	500		
	100 (Note 2)	0/100	0/100		
VIBRATION FATIGUE X1,Y1,Z1 planes 10 g's, 32 hours per plane		PLANES OF STRESS			
		X_1	Y_1	Z_1	
	10 (Note 2)	0/10	0/10	0/10	

NOTES:

1. Random samples from eight production lots.
2. Random samples from three production lots except for Vibration Fatigue which had samples from one lot.
3. High voltage leakage failure: corrective action is defined and implemented.
4. Failed on test: corrective action is defined and implemented.
5. Parametric failure.

FIGURE 3. QUALIFICATION TEST RESULTS

STRESS CONDITIONS	SAMPLES FROM 3 RANDOM PRODUCTION LOTS	HOURS/ CYCLES UNDER STRESS	NO. OF FAILURES ALLOWED PER LOT
HIGH TEMPERATURE BIAS (HTB)			
V = 400V, 15V T_j = +125°C	50/Lot Total 150	1000	0
HIGH TEMPERATURE STORAGE			
T_A = +150°C	20/Lot Total 60	1000	0
DAMP HEAT BIAS (DHB)			
V = 300V, 15V: +85°C 81%RH	20/Lot Total 60	1000	1
TEMPERATURE CYCLE			
-40°C/+25°C/ +150°C 27/3/27 Minutes	20/Lot Total 60	500	0

FIGURE 4. QUARTERLY PRODUCT MONITORING TESTS

The application conditions are: V = 350V, 15V. T_J = 100°C Operating time is 8760 hours per year.

The model used for predicting the product reliability is based on a negative exponential failure distribution with a constant failure rate. This can be expressed with the following equation:

P_S = exp [-t / MTBF] (1)

where: P_S is the reliability or probability of survival.

t is the operating time in hours.

MTBF is the Mean Time Between Failure in hours.

The Probability of Failure (P_F) is: $P_F = 1 - P_S$ (2)

Extensive reliability studies and accelerated tests have been conducted on discrete semiconductors and integrated circuits for a number of years.[1] Based on this experience it was decided to use the High Temperature Bias test as the primary accelerating stress for predicting the reliability of the HVIC under application conditions. It was found that matrix testing of devices under several levels of high temperature reverse bias led to the development of an accelerated reverse voltage model and an accelerated temperature model i.e. the Arrhenius model.[2] This information enables a quantitative extrapolation of the results from high level accelerated tests to the expected results at the lower stress levels found in applications.

Voltage Multiplier:

The reverse voltage model of response is shown on page 211 of the second reference.[2] This was used to determine the Voltage Multiplier (M_V) for derating from high to low voltage stress levels. This relationship is shown in the following equation:

$M_V =$ $[V1/V2]^{1.6534}$ (3)

where V1 and V2 are given in volts

Temperature Multiplier:

The predominant failure mechanisms found in semiconductors during operation are related to temperature and often fit the Arrhenius Model of response. This model can be expressed by the equation:

$\lambda =$ $\exp [A + B/T]$ (4)

$\lambda =$ $A' \exp [-E/(kT)]$

λ failure rate

T absolute temperature (°Kelvin)

A, B empirically derived constants from life test data.

A′ exp (A)

k Boltsman's constant, 8.62×10^{-5}eV/K

E activation energy, empirically derived from: E = -kB. The slope B is negative.

The temperature acceleration multiplier (M_T) between a high temperature test and a lower temperature test can be obtained from the ratio of the failure rates at the two temperatures. This results in:

$M_T =$ $\exp [B/T_2] / \exp [B/T_1]$ (5)

where: T_1 is the low temperature in °K.

T_2 is the high temperature in °K.

Total Multiplier:

The total multiplier (M) is equal to the product of M_V and M_T:

$M =$ $M_V M_T$ (6)

A test was performed to determine the capability of the HVIC over a temperature range of +21.7°C to +150°C. The high voltage leakage current (I_{LKG}) vs temperature was measured on a sample of HVIC'S. The average value at each temperature was plotted on an Arrhenius graph resulting in a reasonable fit to the model. A computer program was used to transform the data and plot the natural Log I_{LKG} vs 1000/T_{ABS} and this is shown in Figure 5. A linear regression analysis of the data gave this general equation:

$y =$ $22.81178 - 6.900413z$ (7)

This has a correlation coefficient of 0.998 which is very good. From this data "E" was calculated to be 0.595eV. This was used to determine the temperature multiplier (M_T) of the HVIC.

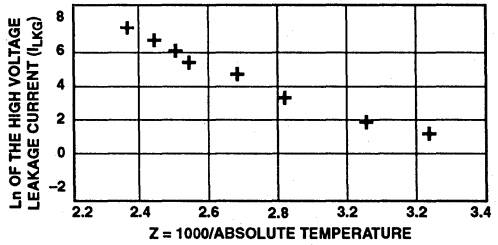


FIGURE 5. PLOT OF Ln OF LEAKAGE CURRENT (I_{LKG}) vs 1000/T_{ABS}

Estimated Annual Field Failure Rate

The calculation of the expected annual field failure rate at application conditions is outlined below. This is based on the results of the HTB tests included in the qualification tests performed in 1990 and in 1991 as well as the favorable results expected on the quarterly monitor tests. A calculation of the acceleration multipliers is shown below:

Voltage Multiplier:

The voltage multipliers between the two HTB test voltages and the application voltage, from equation (3), are:

$M_{V1} =$ $[400/350]^{1.6534}$ $= 1.2471$

$M_{V2} =$ $[450/350]^{1.6534}$ $= 1.5152$

Temperature Multiplier:

From the Arrhenius equation (4) the activation energy E = -kB. Also from the test on high voltage leakage current vs temperature it was found that E was 0.595eV. Solving the above equation, E = -kB, for B results in:

$B =$ -6902.55.

The temperature multiplier between the HTB test at +125°C and the application condition of +100°C, from (5), is:

$M_T =$ $\exp [-6902.55/398] / \exp [-6902.55/373]$

$M_T =$ 3.198

Total Multiplier:

The total multipliers between the two HTB test conditions and the application conditions, from (6), are:

M1 = [1.247] [3.198] = 3.98791

M2 = [1.515] [3.198] = 4.8450

Unit Test Hours

TESTS	HTB UNIT HOURS 400V, +1 25°C	M	APPLICATION UNIT HOURS 350V, +100°C
Qualification (1991)	1006760	3.98791	4014868.3
Quarterly Monitor	600000	3.98791	2392746.0
Qualification (1990)	HTB 450V, +125°C 180000	4.8450	872100.0
	TOTAL		7279714.3

Failure Calculation:

For zero failures and at a 50% confidence level the expected average failure rate would be:

$\lambda =$ $0.7[10^5] /$ Unit Hours

$\lambda =$ $0.7[10^5] / 7279714.3$ $= 0.009616\%/1000$ hours

MTBF = $1[10^5] / 0.009616$ $= 10,399,591.9$ hours

The probability of failure in the first year from equation (2) would be:

$P_F =$ $1 - \exp - [8760/10,399,591.9]$

$P_F =$ 0.00084 or 0.084% per year

The improvement in the HVIC reliability when the operating chip temperature is lowered in the application is shown in Figure 6. For example, this shows that the annual reliability is improved about 4 to 1 when the operating chip (die) temperature is lowered to +75°C instead of +100°C. Similarly there is an improvement of over 12 to 1 when the operating chip temperature is lowered to +55°C.

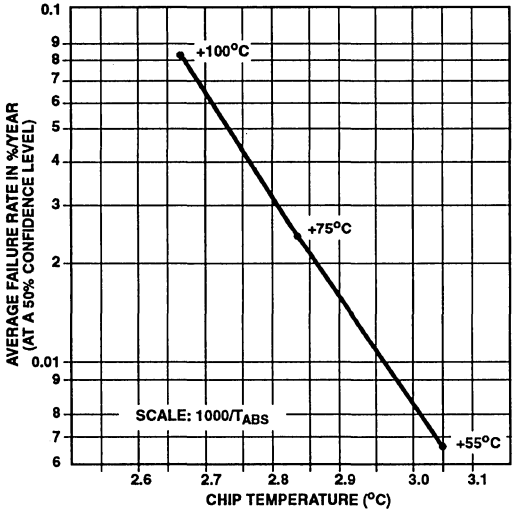


FIGURE 6. RELIABILITY IMPROVEMENT WITH A DECREASE IN OPERATING CHIP TEMPERATURE

Conclusions

1. The average failure rate during the first year is expected to be 0.00962%/1000 hours or 96.2 FITs when the application operating chip temperature is at +100°C and 25.4 FITs at +75°C and 7.6 FITs at +55°C. Note: 1 FIT = 1 Failure/10^9 hours.
2. Similarly, with continued favorable quarterly monitoring test results, the expected average failure rate would decrease from 96.2 to 72.4 FITs after the second year and to 58 FITs after the third year at a chip temperature of +100°C.
3. There is a good chance that the reliability could be better than the predictions since short term evaluation tests showed that samples of HVIC's are capable of withstanding leakage current measurements at V = 500V and +150°C. This is 150 volts and +50°C above the application operating conditions of 350V and +100°C.

Acknowledgment

The author wishes to acknowledge the analytical contributions and encouragement for this report from Pete Shafer, Ray Dyer, and Jack Essom.

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RR002 April 1992

Reliability Report

CONCURRENT DESIGN, TEST AND RELIABILITY ENGINEERING OF POWER ASICs

By Erwin A. Herr

Introduction

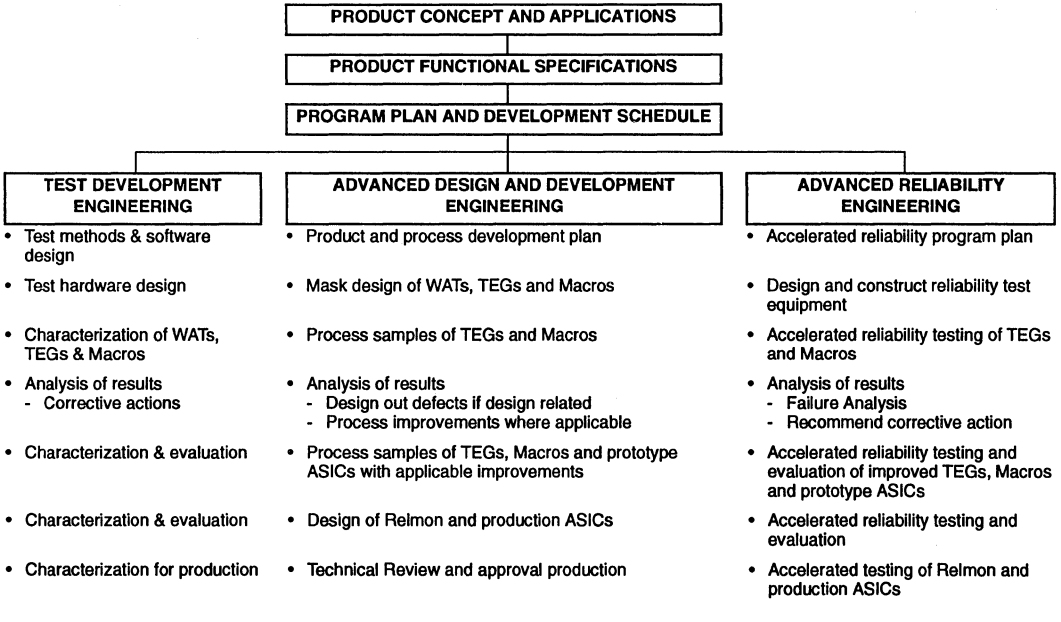
A program was initiated in July 1987 to develop a new Intelligent Power ASIC™ chip technology using state-of-the-art type components and processing. This process utilized mixed signal technology that was optimized for motor/motion control, power supply and interface applications. The first application chosen was a DC/DC converter chip which was mounted in a module with an output of 5 VDC and a current of 10 amperes continuous and 20 amperes peak. The environment for this application was to be in office equipment, for commercial and industrial usage.

The reliability objective of this product was very aggressive in terms of both operating conditions and failure rate. Accelerated testing techniques were used to demonstrate that the failure rate objective was achieved.

Technical Strategy for Design, Test and Reliability Engineering

The Intelligent Power ASIC™ technology had to produce chips which could be designed and developed in a minimum of time, be cost effective, easily manufactured as well as being very reliable. Normally this would be accomplished with mature designs and products that had been manufactured over a period of time with known capabilities and established reliability. However, since this was to be a state-of-the-art technology a new approach had to be taken in order to meet the required time table. These requirements led to the concept of concurrent product, test and reliability development.

An overview of the major activities of this program is illustrated in Figure 1. It is to be noted that this starts with product concept phase and sequences through a number of the major steps up to the production phase. It can also be seen that there were early and concurrent activities in Design, Test and Reliability Engineering. This required the ultimate in communication, cooperation, team work and leadership in many technical areas. This resulted in parallel actions in several areas which traditionally were performed in series. The concurrent action approach not only saved time and cost but it inspired commitment for success from the contributors.



DEVICE PROPERTIES	HIGH TEMPERATURE BIAS	OPERATING LIFE AND POWER CYCLING	DAMP HEAT BIAS	TEMPERATUR E CYCLE	ELECTRO-MIGRATION
Die Bulk and Surface Stability	X	X	X		
Sealed Junction Integrity	X	X	X	X	
Thermal, Mechanical Environmental Stability	X	X	X	X	X
Long Term Reliability	X	X	X	X	X

FIGURE 2. TESTS REQUIRED TO ASSURE DEVICE PROPERTIES

This concept of Concurrent Engineering meant that, as the building blocks of the Power ASIC™ technology were being developed, they were independently characterized and assessed for reliability under accelerated test conditions. These building blocks included new component structures as well as new Macro circuits for the primary functions of the chip. In order to evaluate these building blocks under accelerated test conditions an analysis was made of the desired properties and the accelerated stresses that would assure them. The test matrix in Figure 2 shows the stresses chosen on this program. The objectives of each of the accelerated stresses are shown in Figure 3. Based on this analysis and previous experience the stresses chosen included High Temperature Bias (HTB), Operating Life, Power Cycling, Damp Heat Bias (DHB), Temperature Cycling and Electromigration testing. The overall objective of this early testing was to provide rapid reliability information feed- back to the designers so that they could select the most reliable structures for the new Macro designs.

The approach taken was to use Test Element Groups (TEGs)[1], that were packaged in a manner similar to that which was planned to be used in production. These TEGs included structures of elements such as NPN & PNP bipolar transistors, NMOS and PMOS transistors, LDMOS power FET, zener diodes and electromigration test sites.

As the program progressed these elements were fabricated on the same semiconductor wafers as the Macro and the ASIC circuits. After packaging, the TEG devices were subjected to the same type of stresses that they would normally see in the ASIC circuit. However, the stress levels were usually higher in order to obtain accelerated test results. For example, samples of the components were subjected to multi-level accelerated stresses of high temperature bias for 1000 to 2000 hours. High Humidity Bias or Damp Heat Bias stresses for 1000 to 2000 hours were also used. Temperature cycling was performed to 3000 cycles. Measurements were made of the critical characteristics of the isolated structures initially and at several times after hours of stress. Analyses were made of the distribution of the characteristics and the changes in critical characteristics with stress. The objective was to stress the TEGs to destruction so as to have sufficient failures for failure analysis. This allowed isolation and identification of the failure modes and mechanisms which suggested corrective actions. These led to improvements in design and processing.

The Macros were similarly packaged as the TEGs and submitted to accelerated high temperature bias at +125°C and +150°C for 1000 to 2000 hours. Analysis of the failures from these tests brought out any failure mechanisms that could occur between the combination of structures in the functional circuit. This allowed an in-depth evaluation of the building block circuits for the final ASIC chip.

The production Intelligent Power ASIC™ chip was constructed from the building block Macros and power switching functions. Samples of this type of chip were mounted in several types of packages to evaluate the capability of the chip to withstand electrical, temperature and environmental stresses. One group of Power ASIC™ samples was subjected to accelerated conditions of a dynamic operating life of Vin = 20VDC, Vout = 5V at 10 amperes DC. The junction temperature at the chip was +125°C and the duration of the test was 2000 hours. Another group was subjected to a power cycling test for 2000 hours at maximum operating life conditions with a 10 minute "on" and a 10 minute "off" cycle. In a third group the chip was similarly packaged and these devices were subjected to 1000 to 2000 hours of Damp Heat Bias at

ACCELERATED STRESSES	STRESS OBJECTIVES
High Temperature Bias (HTB)	Die bulk and surface stability under electrical bias and elevated temperature conditions
Operating life and Power cycling	Die bulk and surface stability under electrical operation and elevated temperature conditions
Damp Heat Bias (DHB)	Device physical and surface stability and package material compatibility under accelerated electrical bias, temperature and humidity.
Temperature Cycling	Device mechanical strength and durability under accelerated conditions of thermal expansion and contraction.
Electromigration	Capability of metallization runs to withstand current in power integrated circuits

FIGURE 3. OBJECTIVES OF THE ACCELERATED STRESSES

+85°C 81% RH and 45 volts. A fourth group was subjected to a temperature cycle test of 3000 cycles. In a fifth case samples were subjected to a high temperature bias test of 60 volts on the power section and 42 volts on the control section at a junction temperature of +150°C for 500 hours duration. This series of multi-level stresses was used to evaluate the combined functions of the Macros and the power switching sections of the final Power ASIC™. Reliability predictions are made based on the HTB, operating life, power cycling and DHB test results.

The process technologies used on this program included low and high speed bipolar and complementary MOS signal processing designs as well as combinations of bipolar and MOS power structures. The semiconductor chips were processed with a two level metallization system that is compatible with plastic packaging.

Accelerated Test Results on Components, Macros and Power ASICs

Accelerated testing was used on this Concurrent Engineering Program in order to obtain an early reliability evaluation of the building blocks to be used to construct the Power ASIC™ chip. It was imperative to obtain this information in a minimum time in order to have an efficient design cycle. Care was taken to choose stress levels that would accelerate the changes in characteristics caused by failure mechanisms that exist at lower stress levels. Analysis was made of the initial distribution of critical characteristics as well as changes in the distribution with time under stress. Comparisons were made of the accelerated test results of the components and Macros to gain the maximum information. This helped identify the failure mechanisms for a thorough analysis of any failures obtained. It also allowed the selection and use of semiconductor structures and processes in the final ASIC design that were free from these sensitive mechanisms. This enabled the accelerated reliability information and corrective actions to be in phase with the normal test characterization of the building blocks which resulted in an optimized design and process development cycle.

A general summary of the accelerated constant stress-in-time program conducted during the concurrent product, process and reliability development cycle is given in Figure 4. This includes the number of units tested, the unit hours of stress and the number of failures obtained each year for the components, Macros and ASICs. The constant stress-in-time tests included high temperature bias, operating life, power cycling and a damp heat bias test. Some interesting observations and conclusions can be drawn from this information. It points out the inherent advantages of this Concurrent Engineering Program in the development of a state-of-the-art Power ASIC™ semiconductor chip.

- About 24% of all the test vehicles were stressed during 1988. In the traditional serial development cycle only minimal reliability tests would occur in the first year. This saved at least a year of program time.
- Forty three percent of all the vehicles tested were the less complex structures; namely, TEGs or Macros. This allowed a more thorough and effective analysis of failures which made it easier to isolate failure mechanisms and implement corrective actions.
- Corrective actions were implemented in the first year when the cost of making design changes and process improvements was at a minimum.
- Test systems for the measurement of device parameters and accelerated stress equipment were developed and procured early in the cycle.
- The general testing trend showed that the majority of the Components and Macros were tested during the first year. Long term accelerated testing (2000 hours) of the Power ASIC™ chips was completed during the second year.
- A total of 11385 vehicles were tested under acclerated conditions during the program. A distribution of the vehicles showed that there were 25% components, 18% Macros and 57% Power ASICs™.
- The trend in failure occurrence was highest in the early years of development, but decreased dramatically in subsequent years. This gave a favorable reliability growth pattern.
- This accelerated program enabled production ASICs to be shipped during the second year.

The accelerated tests used to evaluate components or TEGs included high temperature bias at +125°C and +150°C, damp heat bias and temperature cycling. The duration of the high temperature and damp heat bias tests was 1000 to 2000 hours. The general plan for the evaluation of the semiconductor structures used was to stress the structures in the components at the highest bias level (20V), in the Macros at an intermediate level (16V) and in the ASIC circuits at the use level (12.5V).

As previously mentioned the extensive unit hours of testing during the initial evaluation phase are summarized in Figure 4. During the latter part of this evaluation qualification tests were run. The criteria for qualification of components was to pass the appropriate bias tests at the accelerated temperature of +125°C for at least 1000 hours with zero failures out of a sample of twenty. The results of these tests on bipolar transistors, MOS transistors, the LDMOS power FET as well as the zener diodes are summarized in Figure 5. Bias tests at +150°C were also performed to assess the temperature margin for reliability on these components.

Component sample groups of transistors, zeners and the power FETs were subjected to the accelerated test of Damp Heat Bias at +85°C, 81% RH and the appropriate bias for 1000 to 2000 hours. Samples of these devices were also subjected to temperature cycling for 1000 cycles at -40°C to +150°C. Other general evaluation tests were conducted on special structures to measure their capability to withstand electromigration, ESD and latch up stresses.

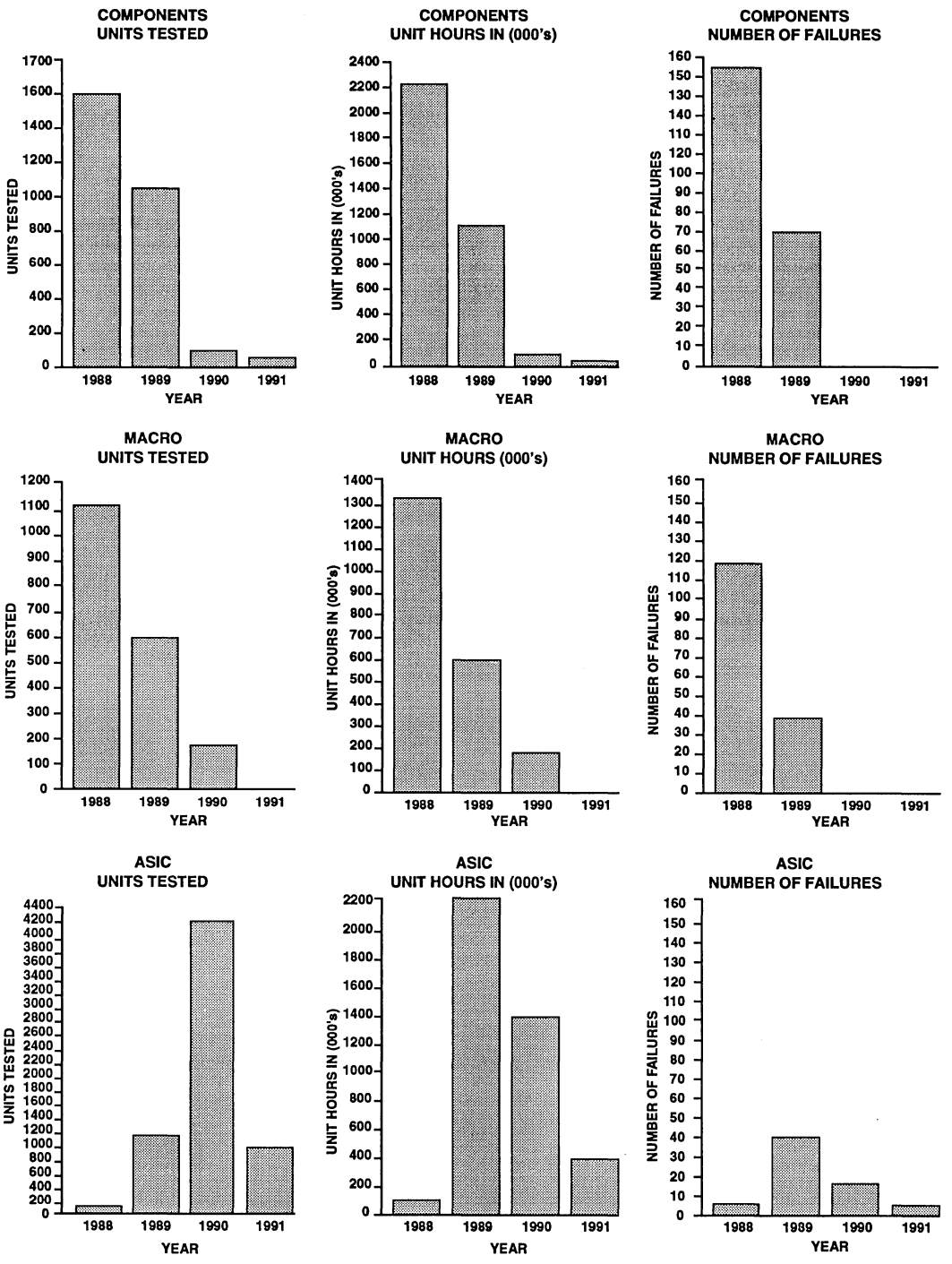


FIGURE 4. CONCURRENT PRODUCT, PROCESS AND RELIABILITY DEVELOPMENT

TEGs	PACKAGE	HIGH TEMPERATURE BIAS (HTB)	1000 HOURS FAILURES/SAMPLE	
			HTB AT +125°C	HTB AT +150°C
NPN	16 Pin DIP	HTB, 20V	0/39	0/20
PNP	16 Pin DIP	HTB, 20V	0/20	0/20
PMOS	16 Pin DIP	HTB, 20V	0/20	0/20
	16 Pin DIP	HTGB, 25V	0/20	0/20
NMOS	16 Pin DIP	HTB, 20V	0/40	3/20
	16 Pin DIP	HTGB, 20V	-	0/20
	16 Pin DIP	HTGB, 25V	0/20	-
Zener-A	16 Pin DIP	0.5mA	-	0/20
Zener-B	16 Pin DIP	1.0V	-	0/20
Zener-C	16 Pin DIP	HTB, 100mA	0/20	0/20
Zener-D	16 Pin DIP	HTB, 6.5V	0/20	0/20
	16 Pin DIP	HTB, 100mA	0/20	1/20
5A LDMOS	TO 218	HTB, 60V	0/20	1/20
	TO 218	HTGB, 20V	0/20	0/20
		TOTAL	0/259	5/260

FIGURE 5. COMPONENT TEG QUALIFICATION

MACRO TYPES	PACKAGE	HIGH TEMPERATURE BIAS (HTB)	1000 HOURS FAILURES/SAMPLE	
			HTB AT +125°C	HTB AT +150°C
Bandgap Voltage Reference	16 Pin DIP	16V, +125°C/+150°C	0/60	0/60
MOS OPAMP A	16 Pin DIP	16V, +125°C/+150°C	0/20	0/20
MOS OPAMP B	16 Pin DIP	16V, +125°C/+150°C	0/20	0/20
Reference Current Generator	16 Pin DIP	16V, +125°C/+150°C	0/20	0/20
Comparator A	16 Pin DIP	16V, +125°C/+150°C	0/20	0/20
Comparator B	16 Pin DIP	16V, +125°C/+150°C	0/20	1/20
Transconductance Amplifier	16 Pin DIP	16V, +125°C/+150°C	0/20	0/20
Comparator C	16 Pin DIP	16V, +125°C/+150°C	0/20	0/8
Gate Driver	16 Pin DIP	16V, +125°C/+150°C	0/20	0/20
Oscillator	16 Pin DIP	16V, +125°C/+150°C	0/20	0/20
Voltage Regulator	16 Pin DIP	45V/5V, +125°C/+150°C	0/20	0/20
		TOTAL	0/260	1/248

FIGURE 6. MACRO QUALIFICATION

The eleven Macro types listed in Figure 6 were also subjected to the same type of general bias tests at elevated temperature and damp heat that were used on the components. These are summarized in Figure 4. They were also subjected to temperature cycling for 1000 cycles at -40°C to +150°C. Again the criteria for qualification was to pass the appropriate bias tests at the accelerated temperature of +125°C for at least 1000 hours with zero failures out of a sample of twenty. The elevated temperature margin for reliability was assessed at +150°C. The results of these tests are summarized in Figure 6.

The failures generated during the early phase of the accelerated tests on components and Macros were particularly important for identifying failure mechanisms for product design and process improvements. The corrective actions included improvements in design resulting from the selection of the most reliable structures based on test results. This timely information was used to establish practical and robust design rules. These rules, based on early component results, were used to design the Macros. Progressively the design rules were further improved from the results of accelerated testing of the Macros. These improvements were implemented into the final ASIC design.

If the failure analysis indicated that the failure mechanisms were process related then process improvements were implemented. These were monitored by testing the Wafer Acceptance Test (WAT) structures on subsequent wafers to demonstrate the improvement. From this information control limits were established on key parameters to maintain statistical process control.

YEAR	STRESS	SAMPLES	HOURS OF STRESS	FAILURES
1989	HTOP & HTB at +125°C, Power cycling up to +125°C	732	2000	1 (100 Hrs)
	Damp Heat Bias +85°C, 81% RH	231	2000	1 (24 Hrs)
	TOTAL	963		3
1990	HTB at +125°C	400	1020	1 (484 Hrs)
	HTB at +125°C	1450	143	0
	HTB at +150°C	217	190	1 (170 Hrs)
	HTB at +150°C	494	505	1 (118 Hrs)
	HTB at +150°C	965	122	0
	TOTAL	3526		3
1991	HTB at +125°C	443	126	0
	HTB at +125°C	179	1010	1 (112 Hrs)
	HTB at +150°C	100	500	1 (182 Hrs)
	HTB at +150°C	248	126	0
	TOTAL	970		2
	Grand Total	5459		8

FIGURE 7. POWER ASIC™ QUALIFICATION

The evaluation of the Power ASIC™ chips included tests on high temperature bias and operating life at a chip temperature of +125°C, damp heat bias at +85°C, 81% RH and temperature cycling of 3000 cycles to the package limits of -5°C to +105°C. The results from high temperature bias, high temperature operating life (HTOP), power cycling and damp heat bias were considered the primary stresses the chip would have to endure in the application. This testing is illustrated in Figure 7. Failure analysis was used to confirm any failures that occurred. Corrective actions were determined, implemented and demonstrated for most of the failures. The remaining failures, for which corrective action had not been determined, were used in the failure rate calculation. This information, as shown in Figure 7, was used to assess the reliability of the Power ASIC™ under the application conditions.

Power ASIC Reliability Assurance

A reliability database ages very rapidly unless it is kept current. Even if no known changes are made, the database needs a continuous flow of current data. To meet this need, a device called the Relmon (Reliability monitor) was designed. This device is a functional part number which is made part of every mask set. The Relmon is used to periodically sample the process and thus update the database with data resulting from improvements such as design rules for more efficient layout, circuit design innovations, and process modifications. The library based Power ASIC design approach enables these types of changes to be made and the database to be maintained. The volume of new part numbers, most containing both "old" Macros and components as well as some "new" Macros and components, allows the qualification work on the new part number to "bridge" the new elements to the existing database. The need to merge data relating to changes such as design rules and process improvements is met by utilizing the Relmon as the vehicle to bridge the data.

Every Power ASIC part which is shipped is tied to the reliability database with four connections: The qualification testing was performed on the part number. This testing is designed to address any aspects of the part number which are outside the bounds of the existing reliability database, for example:

- New components or Macros.
- Components or Macros applied in a new way.
- New packaging or environmental conditions.
- Process improvements. The part number testing is performed on every part. This testing is designed to address three elements of reliability:
- Functional test coverage to assure that all customer specifications are guaranteed.
- Reliability test coverage to assure that all accessible portions of the chip are tested and appropriate voltage margins are applied.
- Parameter limits All parameter limits are examined to assure that limits reflect no more than expected variations.

The WAT (Wafer Acceptance Test) testing is performed on every wafer. This is a set of tests which must be passed for a wafer to be accepted for part number probing. This testing is designed to address three elements related to reliability:

Process control monitors These structures assure that the process is within acceptable bounds.

Representative devices These structures assure at the device level that the wafer has been appropriately processed.

Representative topology test elements These structures assure that aspects such as step coverage are under control. The Relmon (present on every wafer) is used in two ways to assure reliability:

Reliability monitoring Every week a sample of Relmons is subjected to 100 hours of stress testing to continuously monitor the process. Every quarter a sample is subjected to 1000 hours of stress.

Yield analysis In an ASIC product line there can be a great variety of part numbers in various stages of product life cycle. The Relmon is a constant reference that can be used to understand yield variations.

The reliability of the Power ASIC™ chip, operating at +90°C, was determined from the test data given in Figure 7. Since a large part of the testing was performed at accelerated chip temperatures of +125°C and +150°C it was necessary to transform this information to equivalent times at +90°C. This was accomplished by using the Arrhenius model of response[2]. The activation energy used in this model was 0.5425 electron-volts which is based in the Macro test data in Figure 6. From this information a Weibull model was used to calculate the expected failure rate at 60,000 operating hours at a chip temperature of +90°C. This failure rate was found to be 0.018% per thousand hours at a 50% confidence level. Also from the Weibull model it was found that beta was about 0.5 which means that these devices had a decreasing failure rate with time.

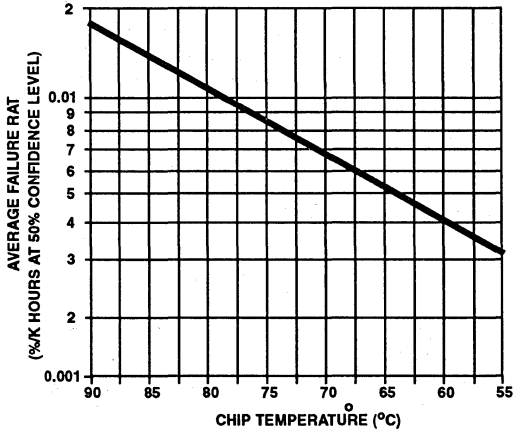


FIGURE 8. RELIABILITY OF POWER ASIC™ CHIP AT 60,000 OPERATING HOURS

The improvement in reliability of the power ASIC chip, when the operating chip temperature is lowered in the application, is shown in Figure 8. For example, this shows that the reliability is improved 2 to 1 when using a chip temperature of +75°C and 6 to 1 when using +55°C instead of +90°C.

Conclusion

This was a program to develop state-of-the-art Intelligent Power ASIC™ products. The concept of Concurrent Engineering proved to be very beneficial in the execution of this program. The following general observations and conclusions can be made:

1. A complex power integrated circuit was fabricated in record time on a semiconductor chip, which included over 23 types of Macros and assemblies plus a power switching section.
2. Concurrent activities and communication in Test Development Engineering, Advanced Design and Development Engineering and Advanced Reliability Engineering assured a timely and successful product development cycle.
3. Excellent teamwork that required the ultimate in communication, cooperation, commitment and leadership enabled shipment of production chips in the second year.
4. Over 11,000 test vehicles, which included TEGs or Components, Macros and ASIC circuits, were stressed under accelerated conditions as the product was developed.
5. Reliability was designed into the product early and evaluated concurrently which enabled us to exceed the expected reliability goal by a factor of about three to one.
6. The Relmon was developed to monitor reliability and update the data base.

Acknowledgment

The author wishes to acknowledge the analytical contributions and encouragement for this report from Peter Shafer, Ray Dyer, Jack Essom and Paulette Gaillard.

References

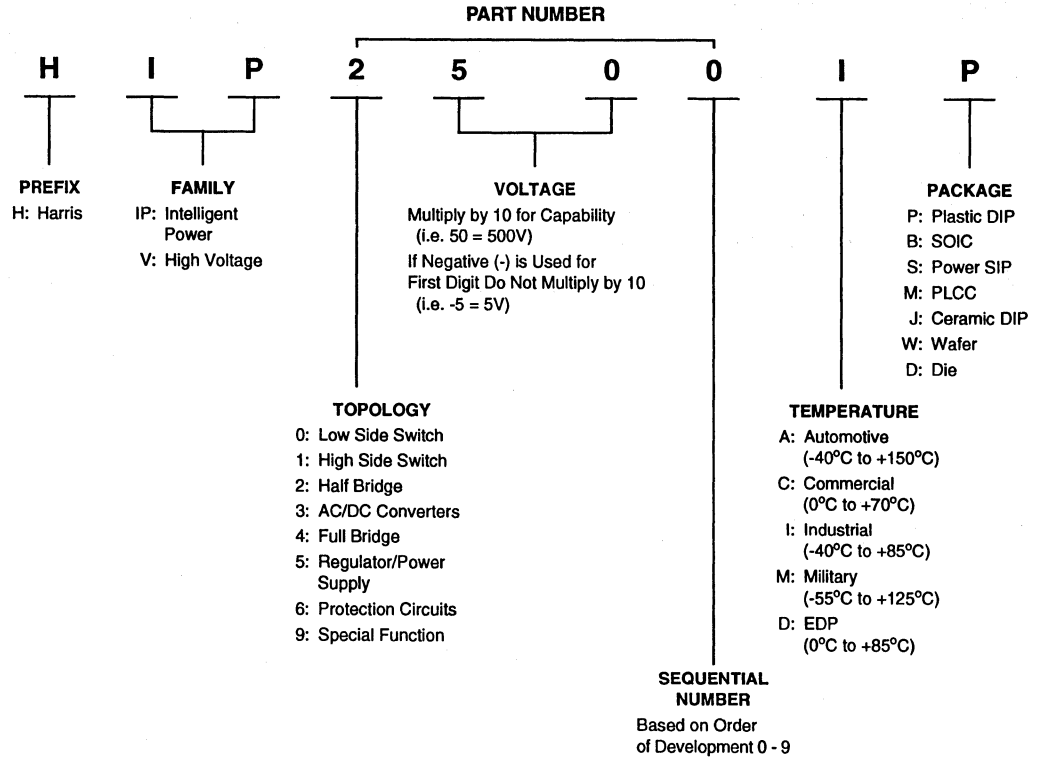
1. E.A. Herr et al "Techniques for the Control of Integrated Circuit Quality and Reliability", Technical Report AFM-LTR-67-147, June 1967 Air Force Materials Laboratory, Wright Patterson AFB, Ohio 45433.
2. E.A. Herr, A. Poe and A. Fox "Reliability Evaluation and Prediction for Discrete Semiconductors," IEEE Transactions on Reliability, August 1980, Volume R-29 Number 3, Catalogue No. ISSN-0018-9529, pp 208-216. 7

INTELLIGENT POWER ICs 12

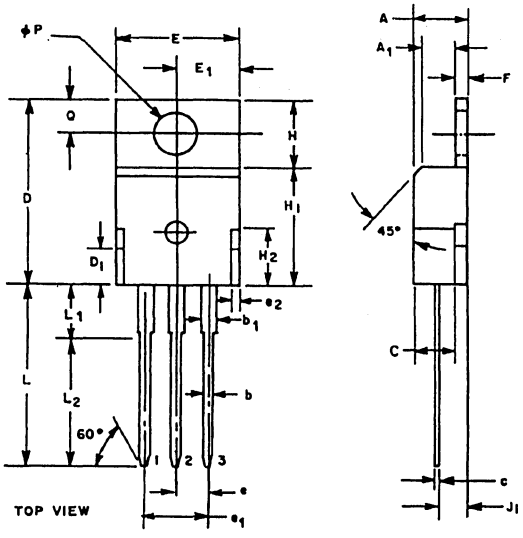
PACKAGING AND ORDERING INFORMATION

Harris Intelligent Power Packaging and Ordering Information

HIP HARRIS PRODUCT CODE EXAMPLE



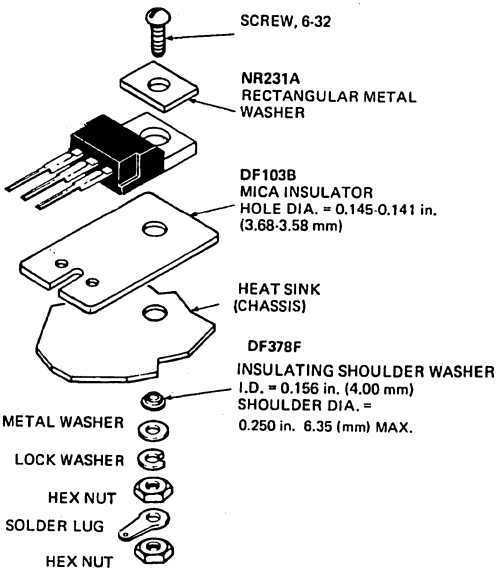
Single-in-Line Plastic Packages (SIP)



3 LEAD SINGLE-IN-LINE FLANGE MOUNTED PLASTIC PACKAGE (JEDEC TO-220AB)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.140	0.190	3.56	4.82	1
A_1	0.080	0.085	2.03	2.16	1
b	0.020	0.045	0.51	1.14	1
b1	0.045	0.070	1.14	1.77	1
C	-	0.125	-	3.18	1
c	0.015	0.025	0.38	0.63	1
D	0.560	0.625	14.23	15.87	1
D_1	-	0.100	-	2.54	1
E	0.380	0.420	9.66	10.66	1
e	0.090	0.110	2.29	2.79	1
e_1	0.190	0.210	4.83	5.33	1
e_2	-	0.030	-	0.76	1
F	0.045	0.055	1.14	1.39	1
H	0.230	0.270	5.85	6.85	1
H_1	0.355	0.370	9.02	9.40	1
H_2	-	0.160	-	4.06	1
J_1	0.080	0.115	2.04	2.92	1
L	0.500	0.562	12.70	14.27	1
L_1	-	0.250	-	6.35	1
L_2	0.400	0.410	10.16	10.41	1
øP	0.139	0.161	3.531	4.089	1
Q	0.100	0.120	2.54	3.04	1

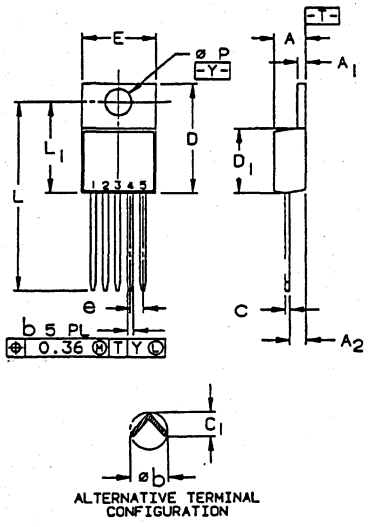
NOTE:
1. Position of lead to be measured 0.250 inch - 0.255 inch (6.350mm - 6.477mm) from case.



NOTE: Maximum torque applied to mounting flange is 8 inch/pound (0.09 kgf/m)

SUGGESTED MOUNTING HARDWARE FOR JEDEC -TO-220AB

Single-in-Line Plastic Packages (SIP)
(Continued)

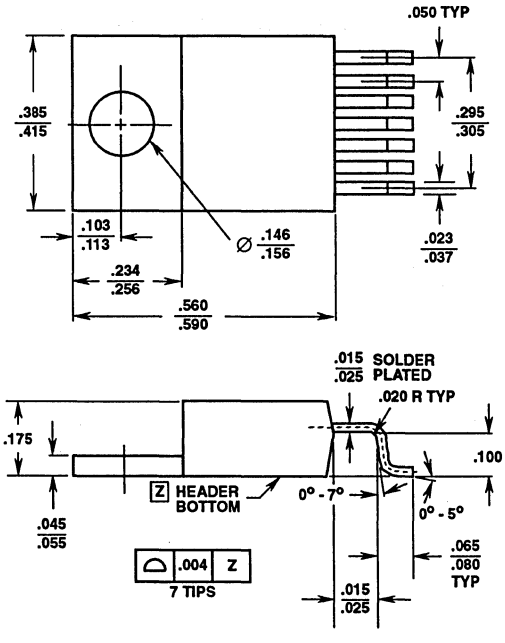


5 LEAD SINGLE-IN-LINE FLANGE MOUNTED PLASTIC PACKAGE (JEDEC TS-001)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.190	4.19	4.82	1, 2, 3
A_1	0.035	0.055	0.89	1.39	1, 2, 3
A_2	0.085	0.115	2.16	2.92	1, 2, 3
b	0.020	0.040	0.51	1.01	1, 2, 3
øb	0.020	0.045	0.51	1.14	1, 2, 3
c	0.012	0.025	0.31	0.63	1, 2, 3
c_1	0.012	0.045	0.31	1.14	1, 2, 3
D	0.570	0.625	14.48	15.87	1, 2, 3
D_1	0.330	0.370	8.39	9.39	1, 2, 3
e	0.067 BSC		1.70 BSC		1, 2, 3
E	0.390	0.415	9.91	10.54	1, 2, 3
L	0.945	1.045	24.00	26.54	1, 2, 3
L_1	0.465	0.539	11.81	13.69	1, 2, 3
P	0.139	0.156	3.53	3.96	1, 2, 3

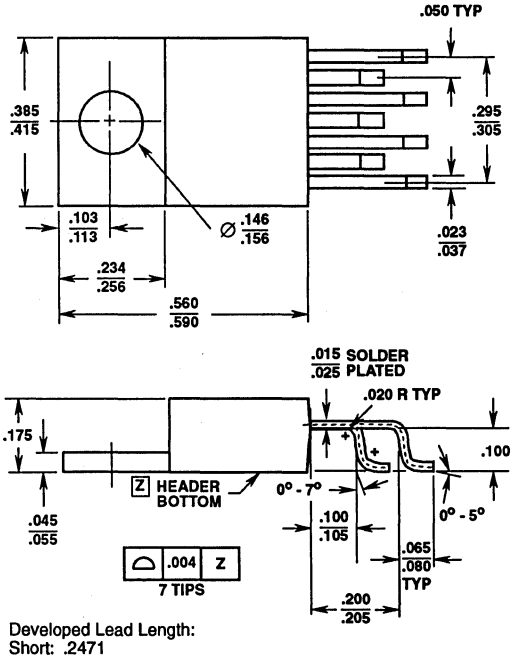
NOTES:
1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M, 1982.
3. Controlling dimension: inch.

7 LEAD SINGLE-IN-LINE SURFACE MOUNT PACKAGE



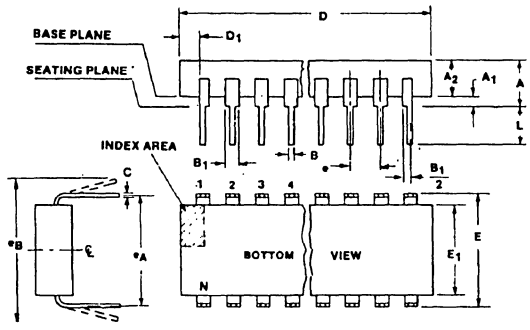
Developed Lead Length: .2471

7 LEAD SINGLE-IN-LINE SURFACE MOUNT PACKAGE



Developed Lead Length:
Short: .2471
Long: .3479

Dual-In-Line Plastic Packages (DIP)



(JEDEC MS-001-AB)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	0.348	0.430	8.84	10.92	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	8		8		11

(JEDEC MS-001-AC)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	0.725	0.795	18.42	20.19	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

(JEDEC MS-001-AA)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

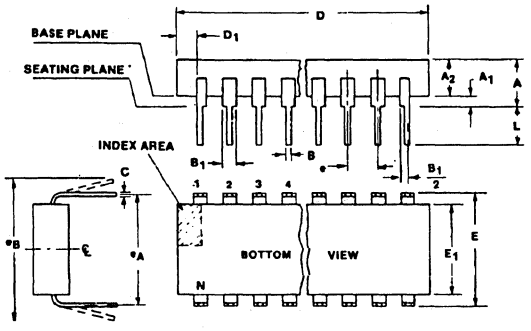
SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	0.745	0.840	18.93	21.33	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

NOTES:
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 inch (0.25mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N \quad \frac{N}{2} \quad \frac{N}{2} + 1$$

4. Dimension D does not include mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be noncumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 inch (0.25mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 inch (0.76mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Dual-In-Line Plastic Packages (DIP)
(Continued)



(JEDEC MS-010-AA)
22 LEAD DUAL-IN-LINE PLASTIC PACKAGE

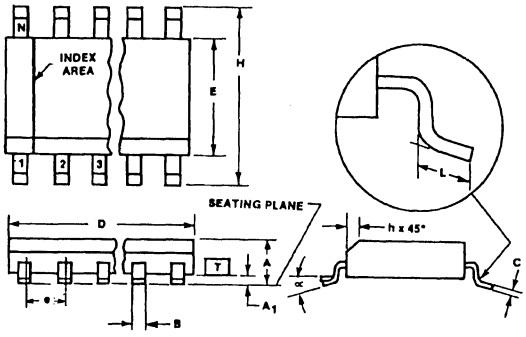
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.330	9
A_1	0.015	-	0.390	-	9
A_2	0.125	0.195	3.180	4.950	-
B	0.014	0.022	0.356	0.558	-
B_1	0.030	0.070	0.770	1.770	3
C	0.008	0.015	0.204	0.381	-
D	1.050	1.120	26.670	28.440	4
D_1	0.005	-	0.130	-	12
E	0.390	0.425	9.910	10.790	5
E_1	0.330	0.380	8.390	9.650	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.400 BSC		10.16 BSC		9
e_B	-	0.500	-	12.700	10
L	0.115	0.160	2.930	4.060	9
N	22		22		11

NOTES:
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 inch (0.25mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N \quad \frac{N}{2} \quad \frac{N}{2} + 1$$

4. Dimension D does not include mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be noncumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 inch (0.25mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 inch (0.76mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Small-Outline Packages (SOIC)



NOTES:
1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 inch)
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006 inch).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimension: Millimeter

(JEDEC MS-012-AB) (Notes 1, 2, 3, 8, 9)
14 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A_1	0.0040	0.0098	0.10	0.25	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

(JEDEC MS-012-AC) (Notes 1, 2, 3, 8, 9)
16 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A_1	0.0040	0.0098	0.10	0.25	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

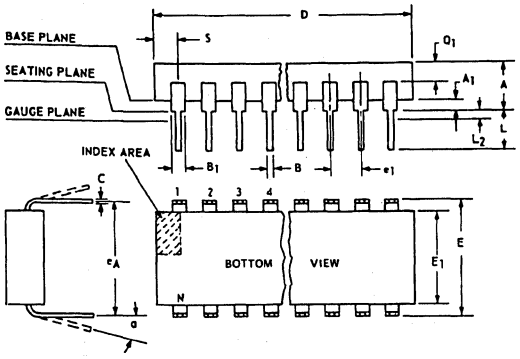
(JEDEC MS-012-AA) (Notes 1, 2, 3, 8, 9)
8 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0532	0.0688	1.35	1.75	-
A_1	0.0040	0.0098	0.10	0.25	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

(JEDEC MS-013-AA) (Notes 1, 2, 3, 8, 9)
16 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.0926	0.1043	2.35	2.65	-
A_1	0.0040	0.0118	0.10	0.30	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Dual-in-Line Frit-Seal Ceramic Packages (DIP)



(JEDEC MO-001-AB)
14 LEAD FRIT-SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.290	3.94	5.08	-
A_1	0.020	0.050	0.51	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.050	0.065	1.27	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	-
E	0.300	0.325	7.62	8.25	-
E_1	0.240	0.260	6.10	6.60	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.00	0.76	-
α	0°	15°	0°	15°	4
N	14		14		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.065	0.090	1.66	2.28	-

(JEDEC MO-001-AC)
16 LEAD FRIT-SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.200	3.94	5.08	-
A_1	0.020	0.050	0.51	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.035	0.065	0.89	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.745	0.785	18.93	19.93	-
E	0.300	0.325	7.62	8.25	-
E_1	0.240	0.260	6.10	6.60	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.00	0.76	-
α	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.015	0.060	0.39	1.52	-

18 LEAD FRIT-SEAL DUAL-IN-LINE CERAMIC PACKAGE

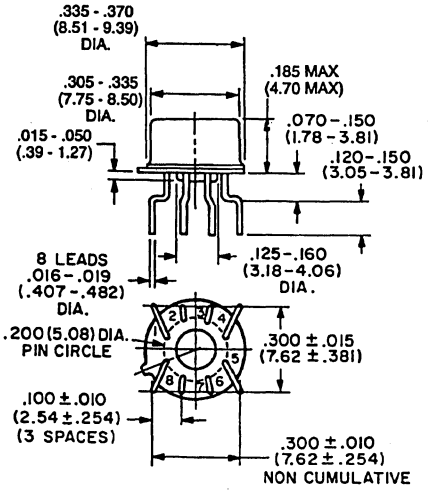
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.200	3.94	5.08	-
A_1	0.020	0.050	0.508	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.035	0.065	0.89	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.845	0.885	21.47	22.47	-
E_1	0.240	0.260	6.10	6.60	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.00	0.76	-
α	0°	15°	0°	15°	4
N	18		18		5
N_1	0		0		6
S	0.015	0.060	0.39	1.52	-

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 inch (0.33mm).
2. Leads within 0.005 inch (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

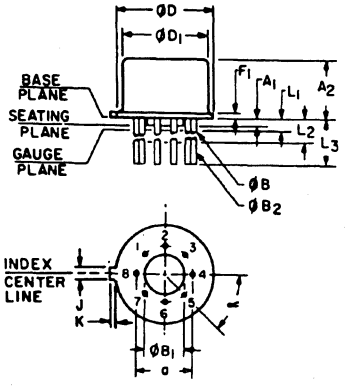
TO-5 Style Packages

8 LEAD TO-5 STYLE WITH DUAL-IN-LINE FORMED LEADS (DILCAN)



All Dimensions Given in: Inches / (Millimeters)

TO-5 Style Packages (Continued)



(JEDEC MO-002-AL)
8 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
a	0.200 TP		5.88 TP		2
A_1	0.010	0.050	0.26	1.27	-
A_2	0.165	0.185	4.20	4.69	-
$ø_B$	0.016	0.019	0.407	0.482	3
$øB_1$	0.125	0.160	3.18	4.06	-
$øB_2$	0.016	0.021	0.407	0.482	3
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	0.020	0.040	0.51	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.000	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	45° TP		45° TP		-
N	8		8		6
N_1	3		3		5

(JEDEC MO-006-AF)
10 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	-
A_2	0.165	0.185	4.19	4.70	-
$ø_B$	0.016	0.019	0.407	0.482	3
$øB_1$	0	0	0	0	-
$øB_2$	0.016	0.021	0.407	0.533	3
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	0.020	0.040	0.51	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.000	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	36° TP		36° TP		-
N	10		10		6
N_1	1		1		5

(JEDEC MO-006-AG)
12 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	-
A_2	0.165	0.185	4.19	4.70	-
$ø_B$	0.016	0.019	0.407	0.482	3
$øB_1$	0	0	0	0	-
$øB_2$	0.016	0.021	0.407	0.533	3
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	0.020	0.040	0.51	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.000	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	30° TP		30° TP		-
N	12		12		6
N_1	1		1		5

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. Leads at gauge plane within 0.007 inch (0.178mm) radius of True Position (TP) at maximum material condition.
2. ØB applies between L_1 and L_2. ØB2 applies between L_2 and 0.500 inch (12.70mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500 inch (12.70mm).
3. Measure from maximum ØD.
4. N_1 is the quantity of allowable missing leads.
5. N is the maximum quantity of lead positions.

CA-Type Packaging and Ordering Information

Linear (CA Series)

Linear ICs are available in a wide variety of package designs. These packages are identified by suffix letters indicated in the chart below. When ordering Linear devices, it is important that the appropriate suffix letter be affixed to the type number as indicated on the price schedule.

PACKAGE	CA SERIES
Dual-in-Line Ceramic	D
Dual-in-Line Plastic	E
Frit-Seal Dual-in-Line Ceramic	F
Quad-in-Line Plastic	Q
Plastic Lead Chip Carrier	Q
Plastic Lead Chip Carrier	Q
Dual-in-Line Formed Lead TO-5	S
TO-5 Style Package	T
Small Outline (SO) Plastic	M

Extra Value Screening

Linear product with extra value screening has an X added to the standard type number in the price list, and is also branded as such. A white dot will indicate location of Pin 1.

Example:

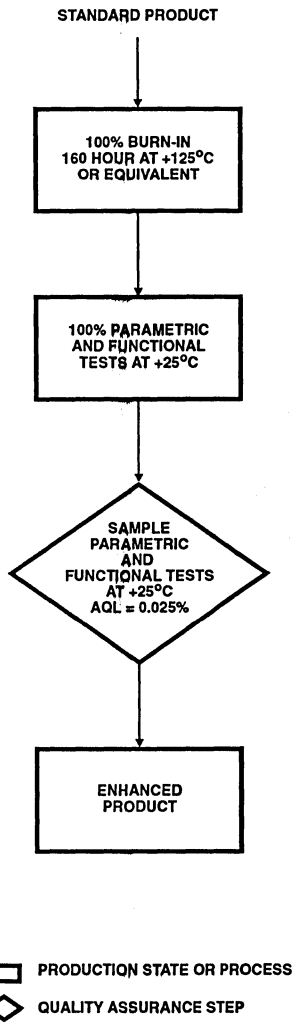
A CA3080E with Extra Value screening is designated CA3080EX in the price list. It is branded CA3080EX plus a white dot at pin number 1.

Tape and Reel for Small-Outline Packages

With the introduction of small-outline packages, Harris now offers its customers the convenient tape and reel style packaging. Small-outline devices, which can be tape and reeled, are denoted with the suffix "M96" or "AM96" in the linear and high speed logic product lines. Devices must be ordered in multiples of quantities listed below. Any returns must be full and unopened reels.

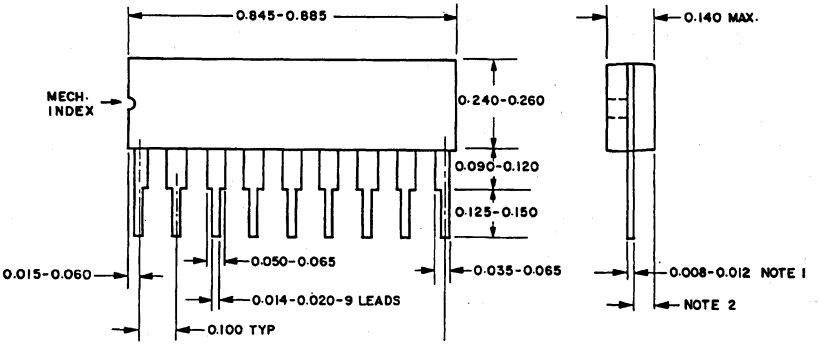
LEAD COUNT	TAPE WIDTH (mm)	REEL SIZE (INCHES)	DEVICES PER REEL
8	12	13	2500
14	16	13	2500
16	16	13	2500
24	24	13	1000

Product Flow



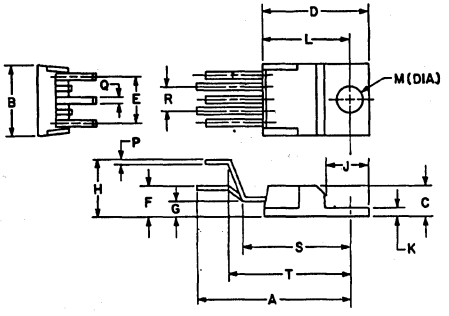
Single-in-Line Plastic Packages (SIP)

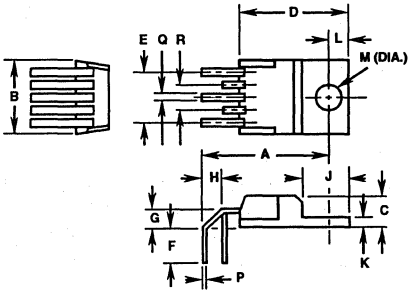
9 LEAD SINGLE-IN-LINE PLASTIC



NOTES:
1. A maximum of 0.013 inch on the lead thickness is to be maintained after solder coating on the narrow portion of the lead.
2. Lead within 0.010 inch radius of true position (TP) with maximum material condition.

TO-220 Style Plastic Packages





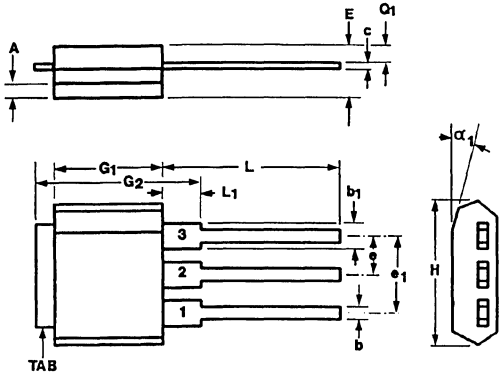
(S1) SUFFIX (VERSA-VI, VERTICAL MOUNT)
5 LEAD PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.876	0.896	22.25	22.75
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.168	0.188	4.268	4.775
G	0.100	0.104	2.540	2.641
H	0.320	0.340	8.128	8.638
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.496	0.508	12.60	12.90
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.015	0.020	0.381	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530
S	0.600	0.630	15.24	16.00
T	0.680	0.710	17.27	18.03

(S2) SUFFIX (VERSA-VI, HORIZONTAL MOUNT)
5 LEAD PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.726	0.746	18.44	18.94
B	0.396	0.408	10.06	10.36
C	0.173	0.182	4.395	4.622
D	0.604	0.619	15.35	15.72
E	0.263	0.273	6.681	6.934
F	0.221	0.251	5.614	6.375
G	0.100	0.104	2.540	2.641
H	0.143	0.163	3.633	4.140
J	0.246	0.254	6.249	6.451
K	0.046	0.054	1.169	1.371
L	0.107	0.114	2.718	2.895
M	0.140	0.150	3.556	3.810
N	5		5	
P	0.014	0.020	0.356	0.406
Q	0.033	0.040	0.839	1.016
R	0.129	0.139	3.277	3.530

Single-in-Line Plastic Packages (Power SIP)



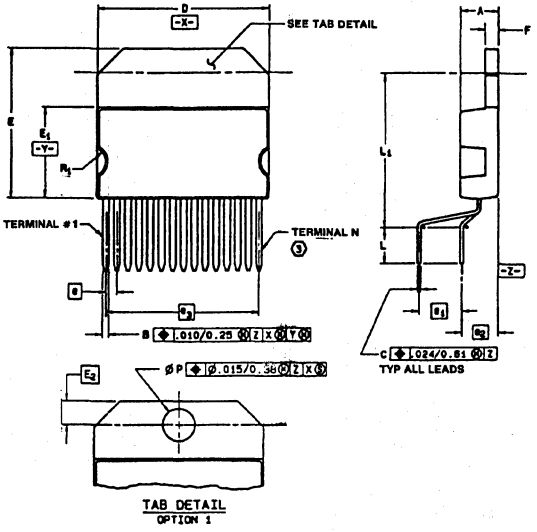
TO-202 MODIFIED
3 LEAD SINGLE-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.050	-	1.270	1
b	0.023	0.029	0.584	0.736	-
b_1	0.045	0.055	1.143	1.397	1
c	0.018	0.026	0.457	0.660	-
E	0.130	0.150	3.302	3.810	-
e	0.095	0.105	2.413	2.667	-
e_1	0.190	0.210	14.826	5.334	-
G_1	0.220	0.260	5.588	6.624	-
G_2	-	0.090	-	2.285	-
H	0.330	0.380	8.362	9.652	-
L	0.390	0.450	9.906	11.43	-
L_1	-	0.110	-	2.794	1, 2
Q_1	0.039	0.050	0.990	1.270	-
α_1	-	50°	-	50°	1

NOTES:
1. Package contour optional within dimensions specified.
2. Lead dimensions uncon trolled in this zone.

Single-in-Line Plastic Packages (SIP)

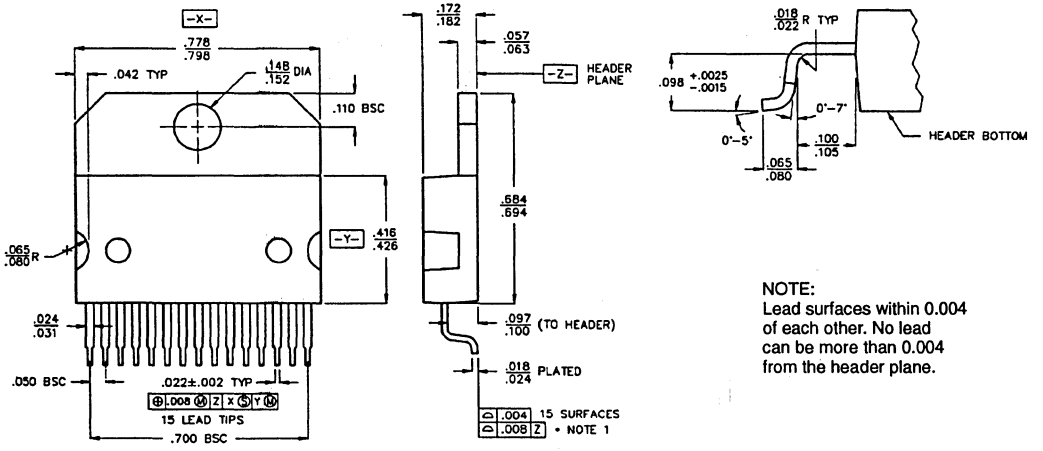
(Z) SUFFIX (JEDEC MO-048 AB)
15 LEAD PLASTIC SINGLE-IN-LINE PACKAGE
STAGGERED VERTICAL LEAD FORM



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.172	0.182	4.37	4.62
B	0.024	0.031	0.060	0.79
C	0.014	0.024	0.36	0.61
D	0.778	0.798	19.76	20.27
E	0.684	0.694	17.37	17.63
E_1	0.416	0.426	10.57	10.82
E_2	0.110 BSC		2.79 BSC	
e	0.050 BSC		1.27 BSC	
e_1	0.200 BSC		5.08 BSC	
e_2	0.169 BSC		4.29 BSC	
e_3	0.700 BSC		17.78 BSC	
F	0.057	0.063	1.45	1.60
L	0.150	0.176	3.81	4.47
L_1	0.690	0.710	17.53	18.03
N	15		15	
P	0.148	0.152	3.76	3.86
q	-	-	-	-
q_1	-	-	-	-
T	-	-	-	-
T_1	-	-	-	-
R_1	0.065	0.080	1.65	2.03

NOTES:
1. Refer to series symbol list, JEDEC Publication No. 95.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1982.
3. N is the number of terminals.
4. Controlling dimension: Inch.

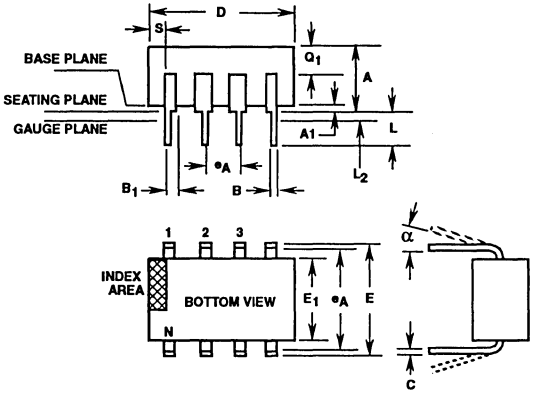
PLASTIC 15 LEAD SINGLE-IN-LINE PACKAGE SURFACE MOUNT 'GULLWING' LEAD FORM



NOTE:
Lead surfaces within 0.004 of each other. No lead can be more than 0.004 from the header plane.

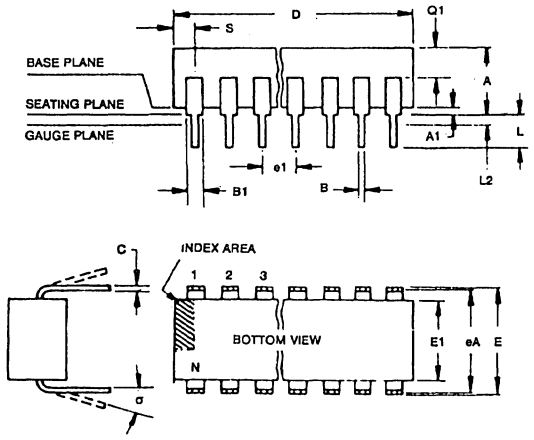
NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

Dual-in-Line Plastic Packages (DIP)



(E) SUFFIX
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE (MINI-DIP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.200	3.94	5.08	-
A_1	0.020	0.050	0.508	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.035	0.065	0.889	1.65	-
C	0.008	0.012	0.203	0.304	1
D	0.370	0.400	9.40	10.16	-
E	0.300	0.325	7.62	8.25	-
E_1	0.240	0.260	6.10	6.60	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.000	0.762	-
α	0°	15°	0°	15°	4
N	8		8		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.015	0.060	0.381	1.52	-

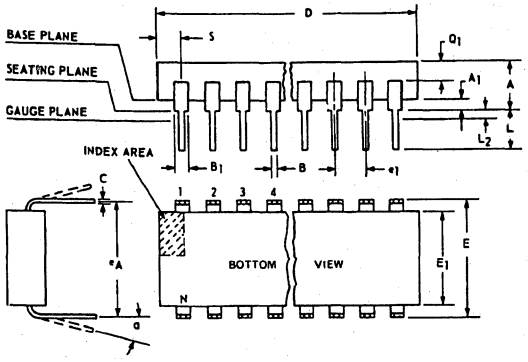


(E) SUFFIX (JEDEC MO-001-AB)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE (MINI-DIP)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.200	3.94	5.08	-
A_1	0.020	0.050	0.51	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.050	0.065	1.27	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	-
E	0.300	0.325	7.62	8.25	-
E_1	0.240	0.260	6.10	6.60	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.000	0.76	-
α	0°	15°	0°	15°	4
N	14		14		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.065	0.090	1.66	2.28	-

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 inch (0.33mm).
2. Leads within 0.005 inch (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

Dual-in-Line Plastic Packages (DIP)
(Continued)



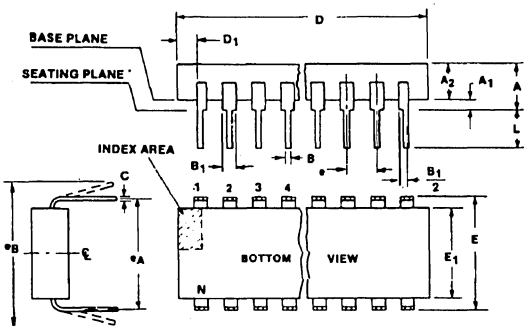
(E) SUFFIX (JEDEC MO-015-AA)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.120	0.250	3.10	6.30	-
A_1	0.020	0.070	0.51	1.77	-
B	0.016	0.020	0.407	0.508	-
B_1	0.028	0.070	0.72	1.77	-
C	0.008	0.012	0.204	0.304	1
D	1.20	1.29	30.48	32.76	-
E	0.600	0.625	15.24	15.87	-
E_1	0.515	0.580	13.09	14.73	-
e_1	0.100 TP		2.54 TP		2
e_A	0.600 TP		15.24 TP		2, 3
L	0.100	0.200	2.54	5.00	-
L_2	0.000	0.030	0.000	0.76	-
α	0°	15°	0°	15°	4
N	24		24		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.040	0.100	1.02	2.54	-

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 inch(0.33mm).
2. Leads within 0.005 inch (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

Dual-In-Line Plastic Packages (DIP)
(Continued)



(E) SUFFIX (JEDEC MS-001-AB)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	0.348	0.430	8.84	10.92	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	8		8		11

(E) SUFFIX (JEDEC MS-001-AC)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	0.725	0.795	18.42	20.19	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	14		14		11

(E) SUFFIX (JEDEC MS-001-AA)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

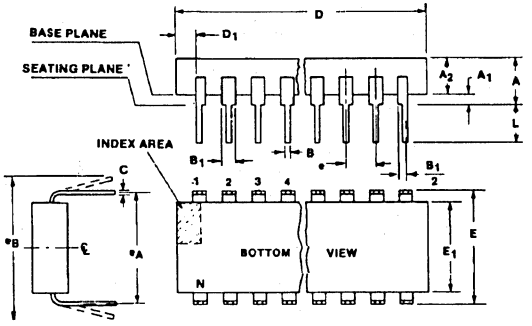
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	0.745	0.840	18.93	21.33	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	16		16		11

NOTES:
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 inch (0.25mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N \quad \frac{N}{2} \quad \frac{N}{2} + 1$$

4. Dimension D does not include mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be noncumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 inch (0.25mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 inch (0.76mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Dual-In-Line Plastic Packages (DIP)
(Continued)



(E) SUFFIX (JEDEC MS-001-AD)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	0.845	0.925	21.47	23.49	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	18		18		11

(E) SUFFIX (JEDEC MS-001-AF)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	9
A_1	0.015	-	0.39	-	9
A_2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	-
D	1.125	1.275	28.6	32.3	4
D_1	0.005	-	0.13	-	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	-	0.430	-	10.92	10
L	0.115	0.160	2.93	4.06	9
N	24		24		11

(E) SUFFIX (JEDEC MS-011-AA)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

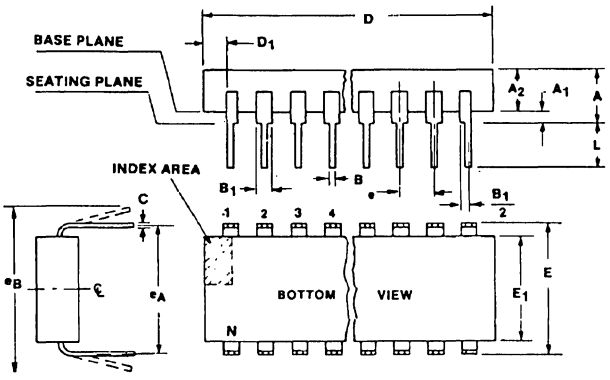
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	9
A_1	0.015	-	0.39	-	9
A_2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	4
D_1	0.005	-	0.13	-	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	-	0.700	-	17.78	10
L	0.115	0.200	2.93	5.08	9
N	24		24		11

NOTES:
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 inch (0.25mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N \quad \frac{N}{2} \quad \frac{N}{2} + 1$$

4. Dimension D does not include mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be noncumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 inch (0.25mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 inch (0.76mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Dual-in-Line Plastic Packages (DIP) (Continued)



(E) SUFFIX (JEDEC MS-011-AB)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	9
A_1	0.015	-	0.39	-	9
A_2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	4
D_1	0.005	-	0.13	-	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	-	0.700	-	17.78	10
L	0.115	0.200	2.93	5.08	9
N	28		28		11

(E) SUFFIX (JEDEC MS-011-AC)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

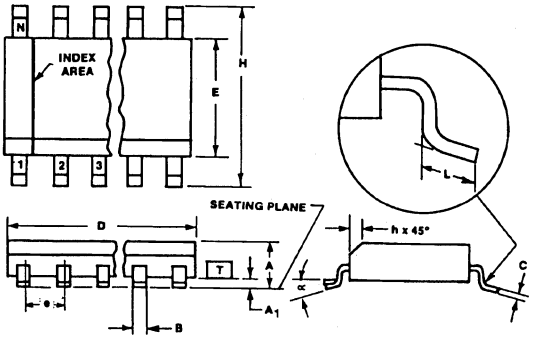
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	9
A_1	0.015	-	0.39	-	9
A_2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B_1	0.030	0.070	0.77	1.77	3
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	4
D_1	0.005	-	0.13	-	12
E	0.600	0.625	15.24	15.87	5
E_1	0.485	0.580	12.32	14.73	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.600 BSC		15.24 BSC		9
e_B	-	0.700	-	17.78	10
L	0.115	0.200	2.93	5.08	9
N	40		40		11

NOTES:
1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 inch (0.25mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

$$1, N \quad \frac{N}{2} \quad \frac{N}{2} + 1$$

4. Dimension D does not include mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be noncumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 inch (0.25mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 inch (0.76mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

Small-Outline Packages (SOIC)



(M) SUFFIX (JEDEC MS-012-AB) (Notes 1, 2, 3, 8, 9)
14 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.0040	0.0098	0.10	0.25	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

NOTES:
1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions and gate burrs shall not exceed 0.15mm (0.006 inch)
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm (0.006 inch).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimension: Millimeter

(M) SUFFIX (JEDEC MS-012-AC) (Notes 1, 2, 3, 8, 9)
16 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.0040	0.0098	0.10	0.25	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

(M) SUFFIX (JEDEC MS-012-AA) (Notes 1, 2, 3, 8, 9)
8 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

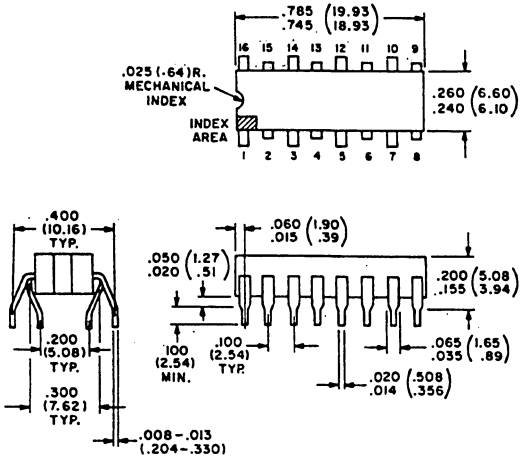
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A_1	0.0040	0.0098	0.10	0.25	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0o	80	0o	8o	-

(M) SUFFIX (JEDEC MS-013-AA) (Notes 1, 2, 3, 8, 9)
16 LEAD DUAL-IN-LINE SURFACE MOUNT PLASTIC PACKAGE

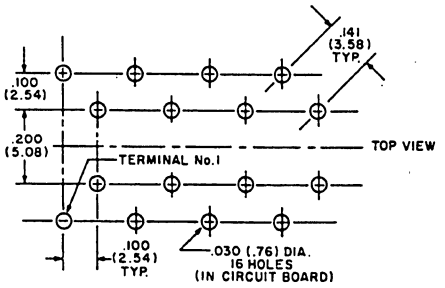
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A_1	0.0040	0.0118	0.10	0.30	-
B	0.0138	0.0192	0.35	0.49	-
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	4
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Quad-in-Line Plastic Packages

(Q) SUFFIX, 16 LEAD



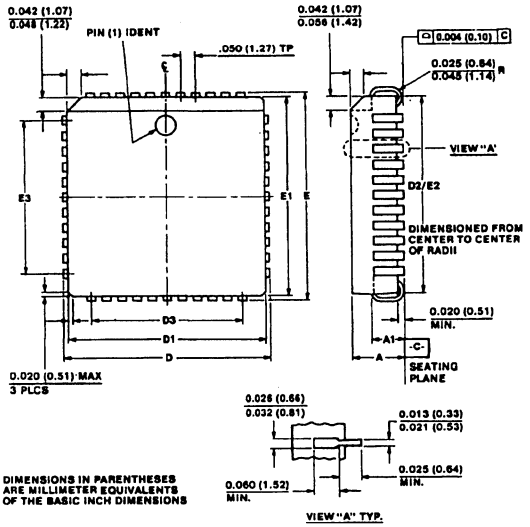
RECOMMENDED MOUNTING HOLE DIMENSIONS AND SPACING



NOTES:
1. Body width is measured 0.040 inch (1.02mm) from top surface.
2. Seating plane defined a the junction of the angle with the narrow portion of the lead.

All dimensions given in: Inches / (Millimeters)

Plastic Chip Carrier Packages

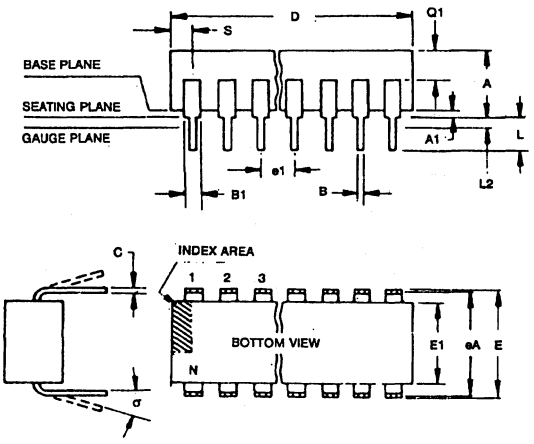


(Q) SUFFIX (JEDEC MO-047-AC)
44 LEAD SQUARE SURFACE-MOUNT PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A_1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D_1	0.650	0.656	16.510	16.662	2
D_2	0.590	0.630	14.99	16.00	1
D_3	0.500 REF		12.70 BSC		-
E	0.685	0.695	17.40	17.65	-
E_1	0.650	0.656	16.510	16.662	2
E_2	0.590	0.630	14.99	16.00	1
E_3	0.500 REF		12.70 BSC		-
N	44		44		3

NOTES:
1. To be determined at seating plane.
2. Dimensions D_1 and E_1 do not include mold protrusions. Allowable mold protrusion is 0.254mm/0.010 inch.
3. "N" is the number of terminal positions.
4. Controlling dimenstion: inch.
5. All leads at seating plane to be coplanar within 0.004 inch.

Dual-In-Line Welded-Seal Ceramic Package



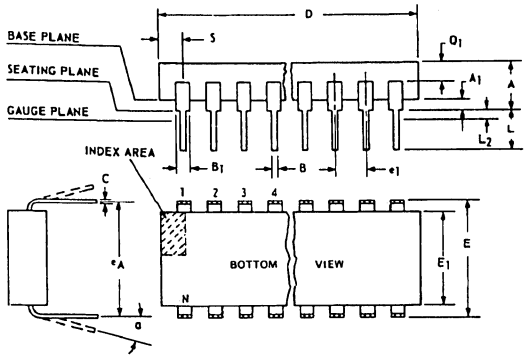
(D) SUFFIX
16 LEAD DUAL-IN-LINE WELDED-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.120	0.160	3.05	4.06	-
A_1	0.020	0.065	0.51	1.65	-
B	0.014	0.020	0.356	0.508	-
B_1	0.050	0.065	1.27	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.745	0.840	18.93	21.33	-
E	0.300	0.325	7.62	8.25	-
E_1	0.240	0.260	6.10	6.60	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.00	0.76	-
α	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q_1	0.050	0.085	1.27	2.15	-
S	0.065	0.090	1.66	2.28	-

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 inch(0.33mm).
2. Leads within 0.005 inch (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

Dual-in-Line Frit-Seal Ceramic Packages



(F) SUFFIX (JEDEC MO-001-AB)
14 LEAD FRIT-SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.200	3.94	5.08	-
A_1	0.020	0.050	0.51	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.050	0.065	1.27	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.745	0.770	18.93	19.55	-
E	0.300	0.325	7.62	8.25	-
E_1	0.265	0.285	6.73	7.24	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.00	0.76	-
α	0°	15°	0°	15°	4
N	14		14		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.065	0.090	1.66	2.28	-

(F) SUFFIX (JEDEC MO-001-AC)
16 LEAD FRIT-SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.200	3.94	5.08	-
A_1	0.020	0.050	0.51	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.035	0.065	0.89	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.745	0.785	18.93	19.93	-
E	0.300	0.325	7.62	8.25	-
E_1	0.265	0.285	6.73	7.24	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
L_2	0.000	0.030	0.00	0.76	-
α	0°	15°	0°	15°	4
N	16		16		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.015	0.060	0.39	1.52	-

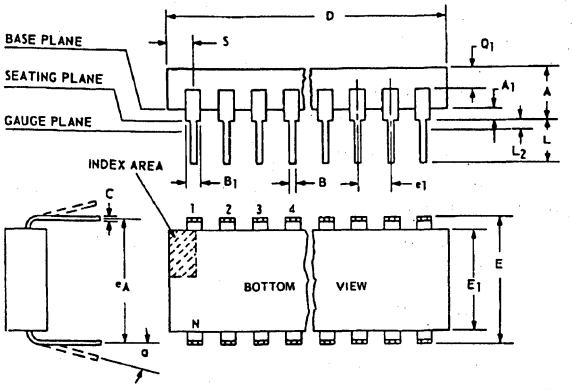
(F) SUFFIX
18 LEAD FRIT-SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.155	0.200	3.94	5.08	-
A_1	0.020	0.050	0.508	1.27	-
B	0.014	0.020	0.356	0.508	-
B_1	0.035	0.065	0.89	1.65	-
C	0.008	0.012	0.204	0.304	1
D	0.845	0.885	21.47	22.47	-
E_1	0.240	0.260	6.10	6.60	-
e_1	0.100 TP		2.54 TP		2
e_A	0.300 TP		7.62 TP		2, 3
L	0.125	0.150	3.18	3.81	-
α	0°	15°	0°	15°	4
N	18		18		5
N_1	0		0		6
S	0.015	0.060	0.39	1.52	-

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 inch(0.33mm).
2. Leads within 0.005 inch (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

Dual-in-Line Frit-Seal Ceramic Package (DIP) (Continued)



NOTES:

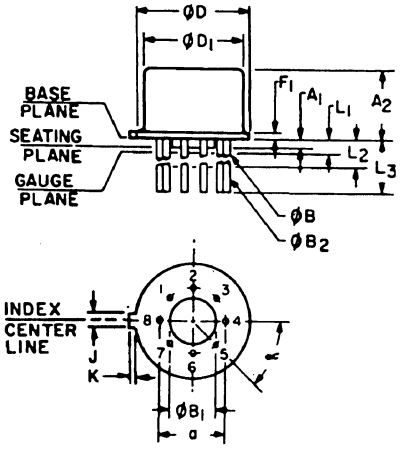
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. When this device is supplied solder-dipped, the maximum lead thickness (narrow portion) will not exceed 0.013 inch(0.33mm).
2. Leads within 0.005 inch (0.12mm) radius of True Position (TP) at gauge plane with maximum material condition and unit installed.
3. e_A applies in zone L_2 when unit installed.
4. α applies to spread leads prior to installation
5. N is the maximum quantity of lead positions.
6. N_1 is the quantity of allowable missing leads.

(F) SUFFIX
24 LEAD FRIT-SEAL DUAL-IN-LINE CERAMIC PACKAGE

	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	0.120	0.250	3.10	6.30	-
A_1	0.020	0.070	0.51	1.77	-
B	0.016	0.020	0.407	0.508	-
B_1	0.028	0.070	0.72	1.77	-
C	0.008	0.012	0.204	0.304	1
D	1.200	1.290	30.48	32.76	-
E_1	0.515	0.580	13.09	14.73	-
e_1	0.100 TP		2.54 TP		2
e_A	0.600 TP		15.24 TP		2, 3
L	0.100	0.200	2.54	5.00	-
L_2	0.000	0.030	0.00	0.76	-
α	0°	15°	0°	15°	4
N	24		24		5
N_1	0		0		6
Q_1	0.040	0.075	1.02	1.90	-
S	0.040	0.100	1.02	2.54	-

TO-5 Style Packages



(T) SUFFIX (JEDEC MO-002-AL)
8 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
a	0.200 TP		5.88 TP		2
A_1	0.010	0.050	0.26	1.27	-
A_2	0.165	0.185	4.20	4.69	-
$ø_B$	0.016	0.019	0.407	0.482	3
$øB_1$	0.125	0.160	3.18	4.06	-
$øB_2$	0.016	0.021	0.407	0.482	3
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	0.020	0.040	0.51	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.000	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	45°TP		45° TP		-
N	8		8		6
N_1	3		3		5

(T) SUFFIX (JEDEC MO-006-AF)
10 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	-
A_2	0.165	0.185	4.19	4.70	-
$ø_B$	0.016	0.019	0.407	0.482	3
$øB_1$	0	0	0	0	-
$øB_2$	0.016	0.021	0.407	0.533	3
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	0.020	0.040	0.51	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.000	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	36°TP		36° TP		-
N	10		10		6
N_1	1		1		5

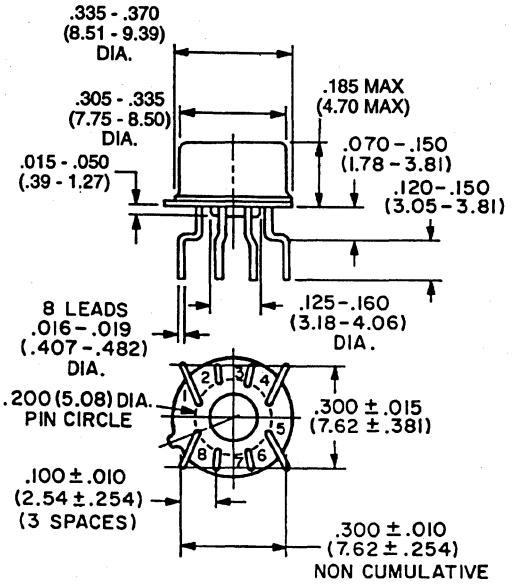
(T) SUFFIX (JEDEC MO-006-AG)
12 LEAD TO-5 STYLE PACKAGE

SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX	NOTES
a	0.230 TP		5.84 TP		2
A_1	0	0	0	0	-
A_2	0.165	0.185	4.19	4.70	-
$ø_B$	0.016	0.019	0.407	0.482	3
$øB_1$	0	0	0	0	-
$øB_2$	0.016	0.021	0.407	0.533	3
øD	0.335	0.370	8.51	9.39	-
$øD_1$	0.305	0.335	7.75	8.50	-
F_1	0.020	0.040	0.51	1.01	-
J	0.028	0.034	0.712	0.863	-
K	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.000	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	30°TP		30° TP		-
N	12		12		6
N_1	1		1		5

NOTES:
Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.
1. Leads at gauge plane within 0.007 inch (0.178mm) radius of True Position (TP) at maximum material condition.
2. ØB applies between L1 and L2. ØB2 applies between L2 and 0.500 inch (12.70mm) from seating plane. Diameter is uncontrolled in L1 and beyond 0.500 inch (12.70mm).
3. Measure from maximum ØD.
4. N1 is the quantity of allowable missing leads.
5. N is the maximum quantity of lead positions.

TO-5 Style Packages (Continued)

(S) SUFFIX
8 LEAD TO-5 STYLE WITH DUAL-IN-LINE FORMED LEADS
(DILCAN)



All Dimensions Given in: Inches / (Millimeters)

ICL-Type Packaging and Ordering Information

Ordering Information

Device Family Prefixes

PREFIX	DEVICE FAMILY
ICL	Linear IC
LM	National Semiconductor Alternate Source

Temperature Range Designators

SUFFIX	TEMPERATURE RANGE
C	Commercial: 0°C to +70°C
I	Industrial: Either -25°C to +85°C or -40°C to +85°C (Specified on Datasheet)
M	Military: -55°C to +125°C

Package Type Designators

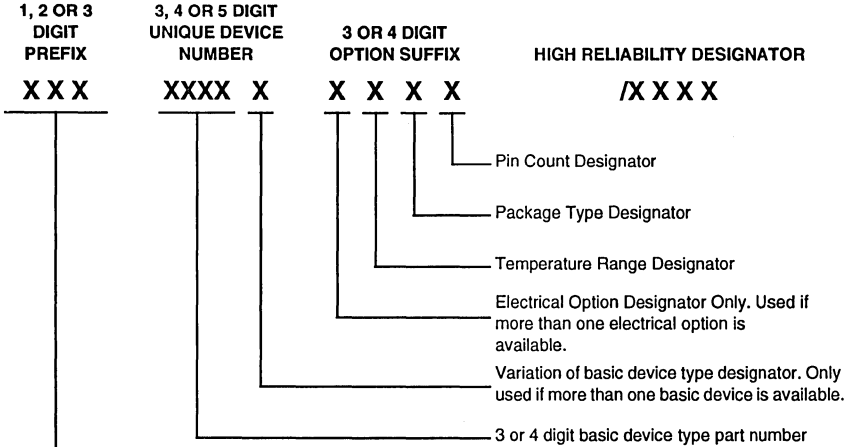
SUFFIX	PACKAGE
B	Small Outline IC (SOIC)
J	Ceramic Dual-In-Line
P	Plastic Dual-In-Line
T	TO-99, TO-100

Pin Count Designator

SUFFIX	PIN COUNT	DIAMETER
A	8	
B	10	
C	12	
D	14	
E	16	
V	8	(0.200" pin circle, isolated case)
W	10	(0.230" pin circle, isolated case)
X	10	(0.230" pin circle, case to pin 5)
Y	8	(0.200" pin circle, case to pin 4)
Z	8	(0.230" pin circle, case to pin 5)

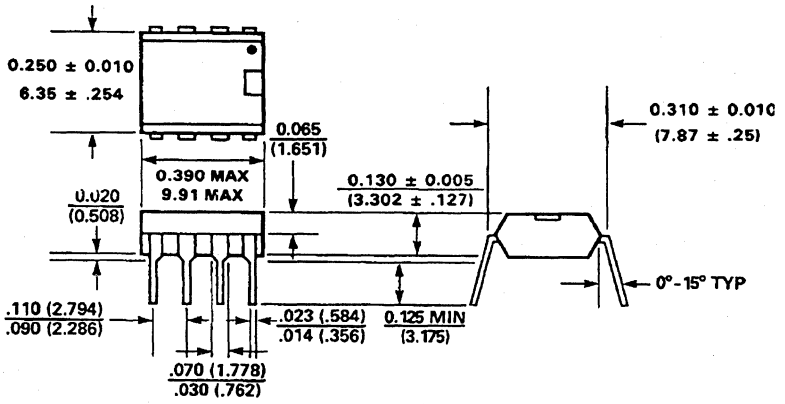
Part Numbering System

All Intersil Part Numbers consist of a Device Family Prefix, a Basic Numeric Part Number, and an Option Suffix, as follows:

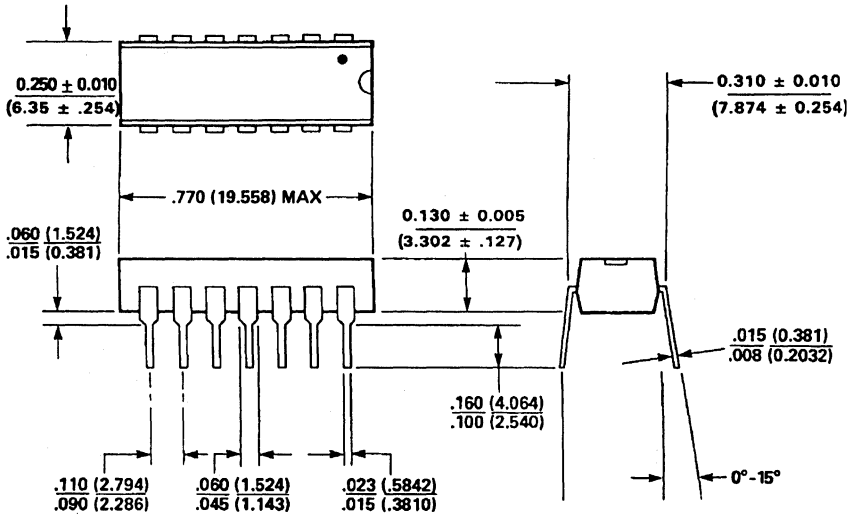


Package Outlines

PA **8 LEAD PLASTIC DUAL-IN-LINE**

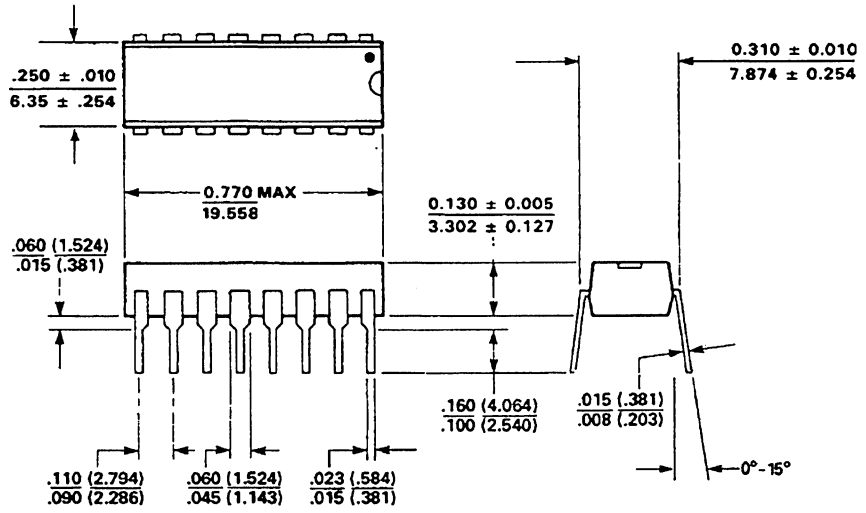


PD **14 LEAD PLASTIC DUAL-IN-LINE**



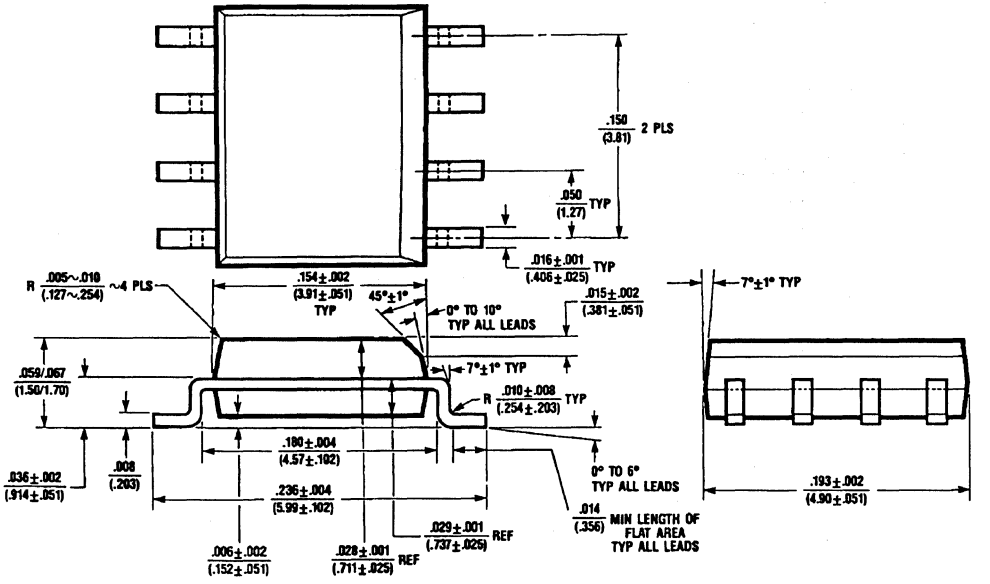
All Dimensions Given in: Inches / (Millimeters)

PE | **16 LEAD PLASTIC DUAL-IN-LINE**

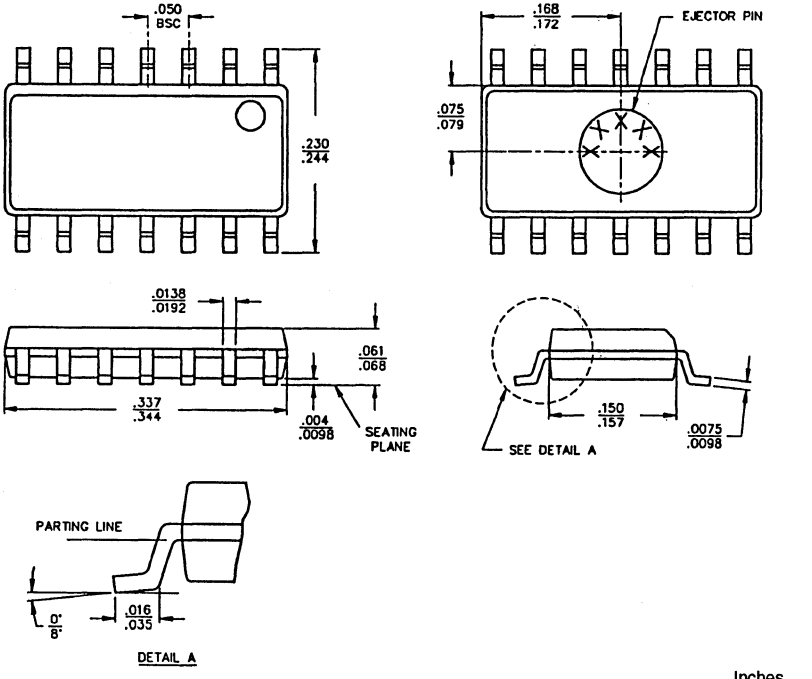


All Dimensions Given in: Inches / (Millimeters)

BA 8 LEAD SMALL OUTLINE (SOIC)

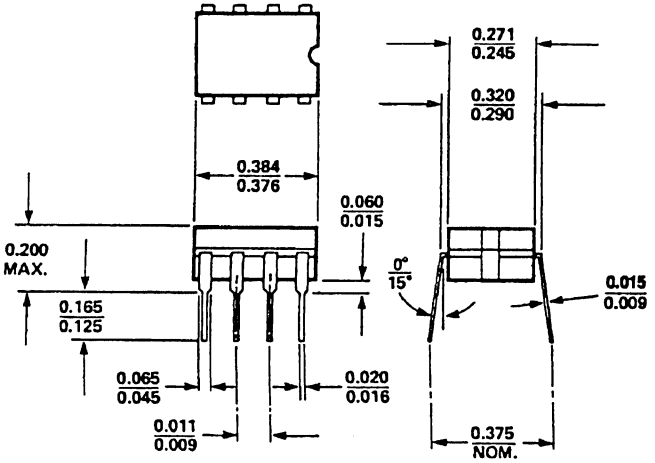


BD 14 LEAD SMALL OUTLINE (SOIC)

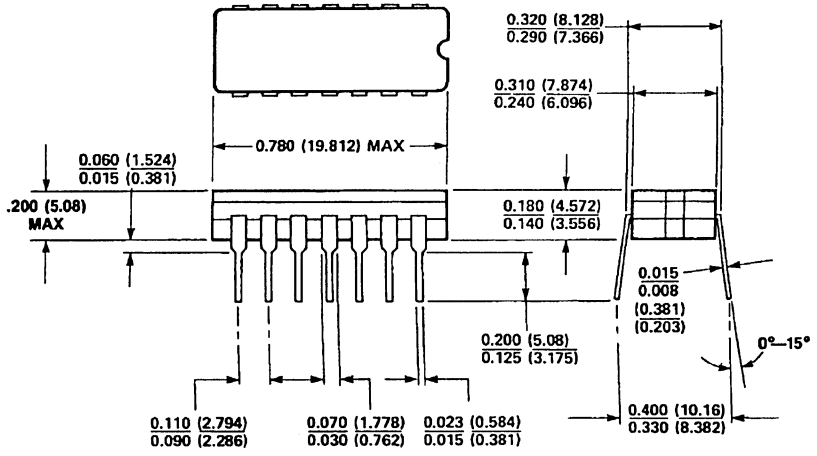


All Dimensions Given in: Inches / (Millimeters)

JA **8 LEAD CERAMIC DUAL-IN-LINE**

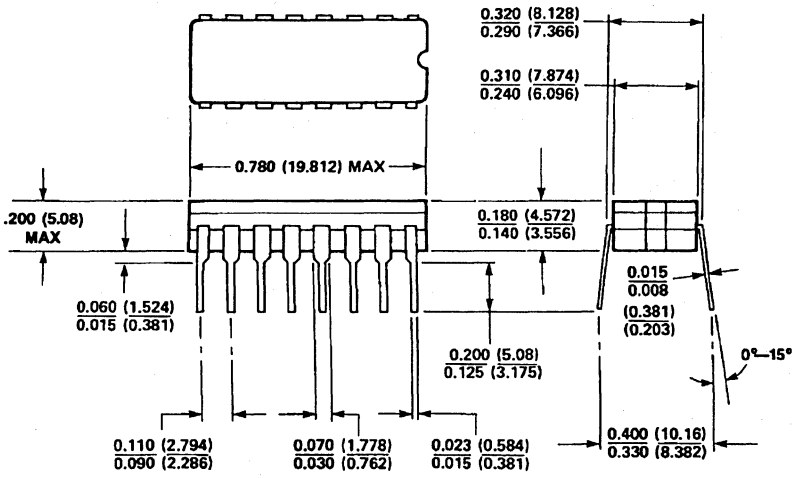


JD **14 LEAD CERAMIC DUAL-IN-LINE**

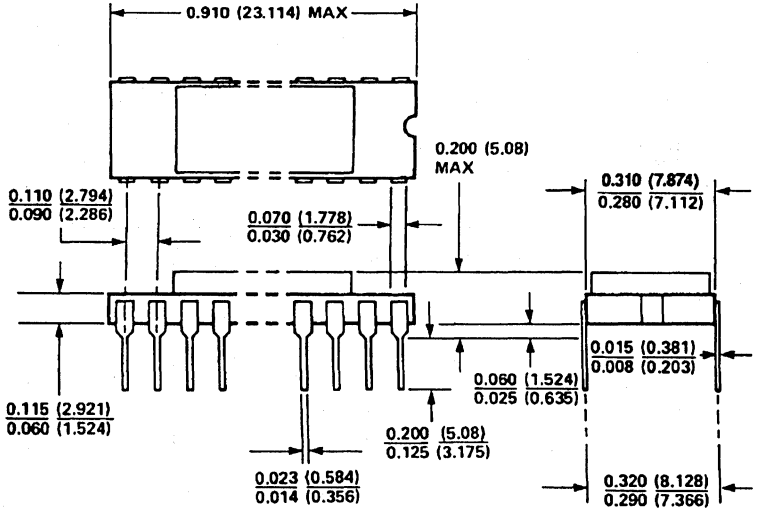


All Dimensions Given in: Inches / (Millimeters)

JE 16 LEAD CERAMIC DUAL-IN-LINE

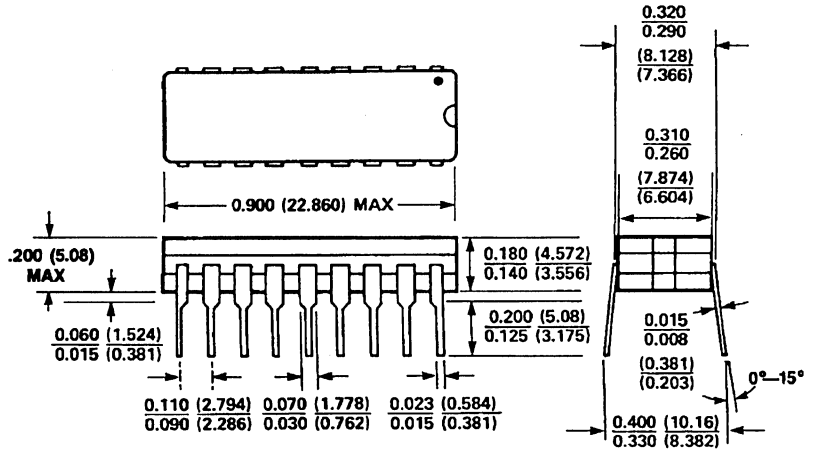


DN 18 LEAD CERAMIC DUAL-IN-LINE



All Dimensions Given in: Inches / (Millimeters)

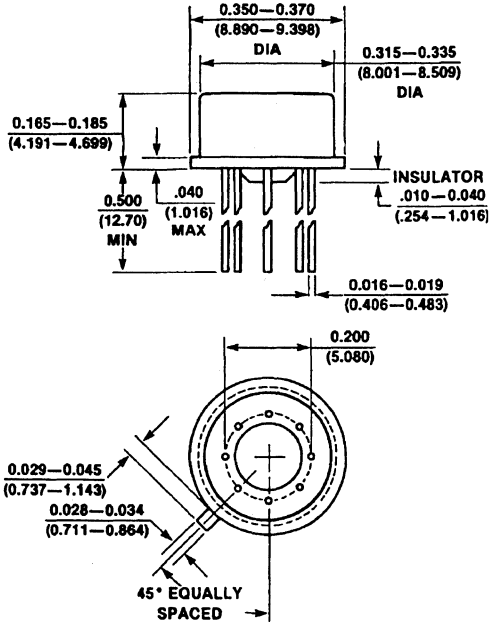
JN | **18 LEAD CERAMIC DUAL-IN-LINE**



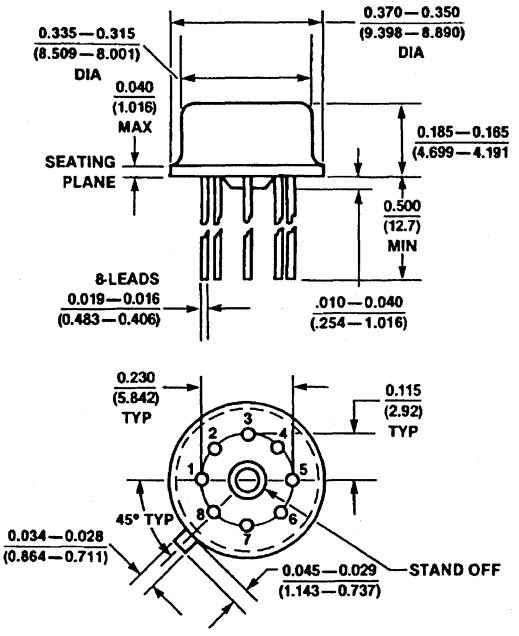
All Dimensions Given in: Inches / (Millimeters)

Package Outlines

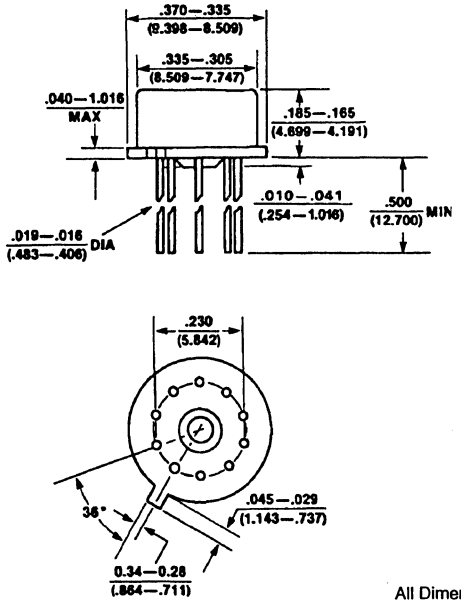
TV | TY | 8 LEAD TO-99 METAL CAN



TZ | 8 LEAD 0.230 PCD TO-99 METAL CAN



TW | TX | 10 LEAD TO-99 METAL CAN



All Dimensions Given in: Inches / (Millimeters)

INTELLIGENT POWER ICs 13

SALES OFFICES

A complete and current listing of all Harris Sales, Representative and Distributor locations worldwide is available. Please order the "Harris Sales Listing" from the Literature Center (see page i).

HARRIS HEADQUARTER LOCATIONS BY COUNTRY:

U.S. HEADQUARTERS
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TEL: (407) 724-3000

EUROPEAN HEADQUARTERS
Harris Semiconductor
Mercure Centre
Rue de la Fusse 100
1130 Brussels, Belgium
TEL: (32) 2-246-21.11

SOUTH ASIA
Harris Semiconductor H.K. Ltd
13/F Fourseas Building
208-212 Nathan Road
Tsimshatsui, Kowloon
Hong Kong
TEL: (852) 3-723-6339

NORTH ASIA
Harris K.K.
Shinjuku NS Bldg. Box 6153
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Shinjuku-Ku, Tokyo 163 Japan
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	GEORGIA	Norcross 404-447-9022
	ILLINOIS	Schaumburg 708-240-3499
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	NEW YORK	Great Neck..... 516-829-9441
	TEXAS	Dallas..... 214-733-0800
INTERNATIONAL	**FRANCE**	Paris..... 33-1-346-54046
	GERMANY	Munich..... 49-8-963-8130
	HONG KONG	Kowloon..... 852-723-6339
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