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Design Guide for LXT914 Quad Ethernet Repeater with the LXT901/904/907 and Motorola MC68EN360

General Description

This application note describes a method for integrating the LXT914 Quad Ethernet Repeater into existing and new architectures using the MC68EN360 (QUICC) device. It also includes the design notes for the MC68EN360 and the LXT901/7 found in Application Note 35 for new users of Level One devices who also use the QUICC interface. The LXT914 has a new advanced feature set which allows integration of the repeater function with existing QUICC/LXT901/7 designs.

The QUICC/LXT90X/LXT914 device combination demonstrates Level One's commitment to supplying highly integrated solutions to meet our customers' ever increasing requirements for advanced new products.

LXT914 Advanced Feature Set

- Three new LED operating modes
- Selectable AUI interface (DTE/MAU)
- Four integrated 10BASE-T transceivers
- Integrated transmit and receive filters
- Seven integrated LED drivers
- Synchronous or Asynchronous inter-repeater backplane operation
- Inter-repeater backplane supports glueless cascading of repeater devices for maximum port count
- Serial port interface for initial port configuration
- Packaged in both 68-pin PLCC and 100-pin PQFP

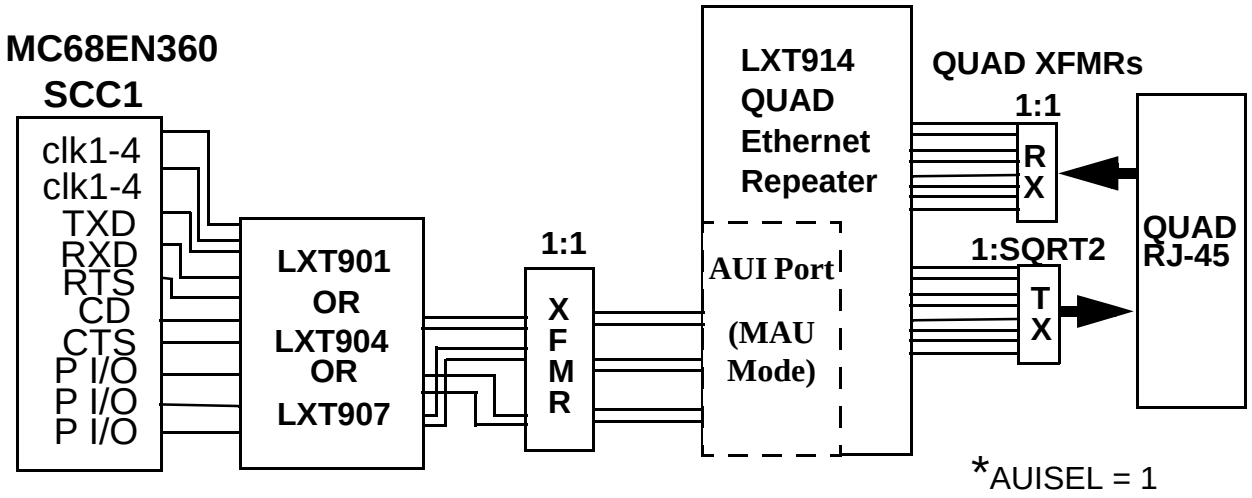
Application Overview

The LXT914 Flexible Quad Ethernet Repeater can be used to increase the connectivity of your current and future designs, including Routers, Bridges, Print Servers, etc. Any single port Ethernet design can be upgraded to a multi-port repeated network simply and easily using the LXT914 device with the new advanced feature set.

The LXT914's advanced feature set includes three new LED modes and the selectable AUI interface (DTE/MAU).

The LXT914 AUISEL pin allows the designer to select the MAU interface mode of operation. The MAU mode allows for the connection of the DTE interface of the LXT901/4/7 with the MAU interface of the LXT914. This application will increase the connectivity of the product from one port to 4, 8, or 12 TP ports. The LXT914 advanced feature set also allows for growth from LED managed to a fully managed solution.

LXT914 Integrated Ethernet Repeater Block Diagram



DESIGN REQUIREMENTS

LXT90X - QUICC Compatibility

The LXT901, LXT904 and LXT907 devices are each available in a 44-pin PLCC package. There are functional differences between the three devices, but each product has all of the features required for compatibility with the QUICC in this application. The LXT907, for example, uses pin 37 for the DSQE function, allowing the designer to make SQE a programmable option in the design. The LXT901 uses pin 37 for UTP/STP media selection. These device-specific options apply to the use of the TP port which is unused in this application. The LXT904 device has only the single AUI port—the only port required for this application. Refer to the Level One data sheet for the specific device to fit your individual requirements.

LXT90X - LXT914 Connections

The LXT901/4/7 device should be set up in a fixed mode of operation. This fixed mode of operation reduces the number of required programmable pins. The mode selected for operation with the LXT914 is: Autoselect disabled, LI disabled, and PAUI set (for AUI only operation).

The actual connection between the LXT901/4/7 and the LXT914 is shown in Figures 1 and 2, which detail the two interface options: capacitive coupling and isolation transformers, respectively. Capacitive coupling is used for like-biased devices. Some devices will require transformers. The AUI circuitry has voltage biasing on all lines and requires isolation when transmitting between devices. Either option also requires the 78.7 Ω termination resistors on both sides of the transformer or the capacitive coupling as shown in Figures 1 and 2.

NOTE

Some existing designs may require reprogramming.
The programmable pins should be set as follows:
AUTOSEL = Low: Auto Port Select disabled
LI = Low: Link Integrity Test disabled
PAUI = High: AUI Port selected
MD0 = Low: Controller Mode 1 selected
MD1 = Low: Controller Mode 1 selected

The following pins on the LXT901/4/7 connect to MC68EN360 SCC1 signals.

Table 1: Connections to QUICC SCC1

LXT90X Pin #	LXT90X Signal Name	Motorola QUICC MC68EN360 SCC1 Signal
28	RCLK	CLK1-4[1]
11	TCLK	CLK1-4[1]
12	TXD	TXD
26	RXD	RXD
13	TEN	RTS
27	CD	CD
16	COL	CTS
22	LBK	PI/O1[2]
4	NTH	PI/O2[2]
37	UTP(901)	PI/O3[2]
37	DSQE(907)	PI/O3[2]

1. The design must provide separate clocks for TCLK & RCLK. Any of the clocks on the QUICC will do.
2. Please refer to the Motorola specification for the correct connections and desired results. These pins should be programmable output pins for use with TTL inputs. Check the pin's state at reset and power up for compatibility with Level One devices.

Setting QUICC Parameters

Refer to the Motorola MC68EN360 Quad Integrated Communications Controller User's Manual for settings required to operate the QUICC properly. Here are some points to be aware of when setting up the QUICC's internal registers:

- Use SCC1 for the LAN connection, and use another SCC or a parallel port for another remote connection. (Only the SCC1 has Ethernet communications capability.)
- Bypass both the Digital Phase -Locked Loop (DPLL) and Manchester Encoding/Decoding functions for Ethernet operations (This is integrated into the LXT901/4/7).
- Set the TCI (Time Clock Invert) bit high to allow the QUICC to clock the data out to the LXT901 or LXT907 device on the rising edge of the clock pulse. This improves data setup time at the 10 Mbps speed used by Ethernet. TCI is bit 28 of the General SCC Mode Register (GSMR).
- Set the MODE bits (0-3) must to 1, 1, 0, 0. Set both the Transparent Receiver (TRX) and Transparent Transmitter (TTX), bits 43 & 44, to 0 for Normal Operation, or a 1 for Transparent Operation. Do not mix the two signals, set them for the same mode. We recommend the 0 setting: In this mode the QUICC does not manipulate the protocols in the data stream.
- Set the Transmit FIFO Length (TFL) bit & the Receive FIFO Width (RFW) bits to 0.
- Set the bits to 0, 1 (Ethernet operation) for a repeating (1,0,1,0,...) pattern as a preamble. GSMR bits 19-20 are Transmit Preamble Pattern (TPP) bits.

LXT914 Configuration

The following is a complete list of the settings as shown in Figure 3. Some of these settings are optional. Select the settings which will be best for your product.

- LOC/$\overline{\text{EXT}}$: Set this bit High (1) for Local Management. (Use External Management to meet the requirement for managed TP port statistics, SNMP protocol or RMON operation with a EMD device.)
- A/$\overline{\text{SYNC}}$: Select Asynchronous mode High (1) to eliminate the need for an external clock source. The Asynchronous and Synchronous modes of operation determine the relationship between the System Clock and the IRB Clock. The IRB clock is internally generated in Asynchronous mode only.
- AUISEL/LEDJM: Pull this pin High (1) for this application. (This pin can be an external LED driver or used as an input to select MAU mode for the AUI port.)
- LEDM1/0: Set these pins for one of four possible LED modes. The available modes are shown in Table 2. In the MAU configuration, Mode 0 and the LEDJM driver are not available with the PLCC package.
- DSQE: Set the disable SQE pin High (1) to disable the SQE function or Low (0) to enable the SQE function.
- FPS: Set the first position pin High (1).
- SDI: Tie this pin Low for the default settings of the internal setup register used here. (Use an external EEPROM to customize the port settings. Refer to the LXT914 data sheet for further information.)
- SCLKIO, $\overline{\text{SENO}}$, $\overline{\text{SENI}}$: Leave the remaining serial management pins floating.
- TEST: Tie this pin Low (0).

Figure 1: AUI Capacitive Coupling Interface

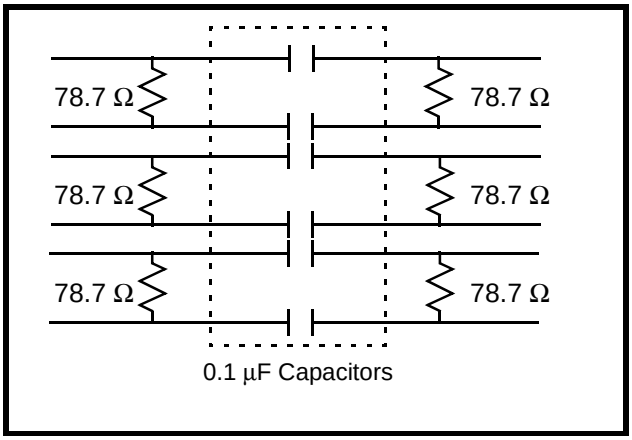


Figure 2: Isolation Transformer Interface

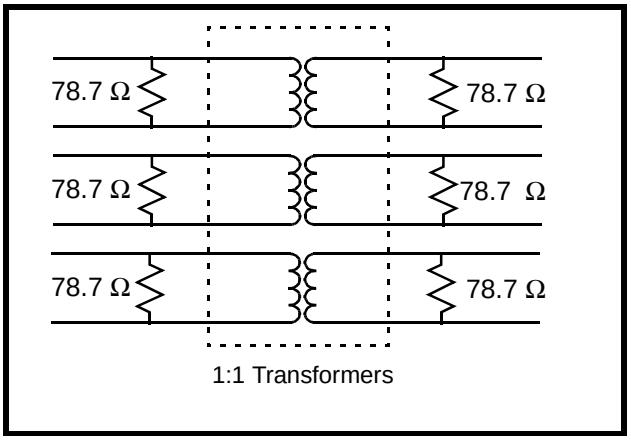


Table 2: LED Modes Available in the LXT914

Condition (LEDM0, 1)	LEDTP 1-4	LEDAUI	LEDCF
MODE 1 (0, 1)			
1 Steady High	Rx Link Pulse	*n/a*	MJLP
2 Blink High	*n/a*	*n/a*	*n/a*
3 Steady Low	*n/a*	*n/a*	Collision
4 Blink Low	Rx Packet	Rx Packet	*n/a*
MODE 2 (1, 0)			
1 Steady High	Rx Link Pulse	*n/a*	MJLP
2 Blink High	Partition Out	Partition Out	*n/a*
3 Steady Low	*n/a*	*n/a*	Collision
4 Blink Low	Rx Packet	Rx Packet	*n/a*
MODE 3 (1, 1)			
1 Steady High	Rx Link Pulse	*n/a*	MJLP
2 Blink High	Rx Packet	Rx Packet	*n/a*
3 Steady Low	Partition Out	Partition Out	Collision
4 Blink Low	*n/a*	*n/a*	*n/a*

Inter-Repeater Bus (IRB)

The IRB connects multiple LXT914 devices on a single repeated segment. Each repeater device distributes recovered and retimed data to other repeaters on the IRB simultaneously. This simultaneous rebroadcast allows the multiple devices to act as a single large repeated segment.

- $\overline{\text{IRENA}}$, IRDAT, $\overline{\text{IRCOL}}$, $\overline{\text{IRCFS}}$: These four signals must each be pulled up through a single 330 Ω 1% resistor.
- $\overline{\text{IRDEN}}$: This signal controls the transceivers for synchronous mode of operation. The synchronous mode is required for a fully managed solution.

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Table 3: Four TP Port BOM (*see Figure 3*)

#	Qty	Description
1	6	.1 µF caps *AC Coupling only*
2	4	120 pF capacitors
3	8	24.9 Ω 1% resistor
4	4	100 Ω resistors
5	4	330 Ω resistors
6	2	12.4 kΩ resistors
7	4	1 kΩ resistors
8	1	1:1 XFMR, *No AC coupling*
9	1	1:1 Rx XFMR (quad)
10	1	1:1.41 Tx XFMR (quad)
11	1	20 MHz Oscillator (or 20 MHz system clock)
12	-	LEDs, user defined

LAYOUT REQUIREMENTS

The Twisted-Pair Interface

The four twisted-pair output circuits are identical. Each TPDOP/TPDON output pair has a 24.9 Ω, 1% resistor in series at each output pin and a 120 pF capacitor across the output lines. These signals go directly to a 1:$\sqrt{2}$ transformer creating the necessary 100 Ω termination for the cable. The TPDIP/TPDIN signals have a 100 Ω resistor across the differential pairs to terminate the 100 Ω signal from the line. To calculate the impedance on the output line interface, use the formula:

$$(24.9\ \Omega + 24.9\ \Omega) * \sqrt{2}^2 \approx 100\ \Omega.$$

Table 4 lists available quad and single port transformers with manufacturers and their part numbers. This information was valid as of the printing date of this document. Before committing to a specific component, designers should review the specifications for any device to be used in the design.

The layout of the twisted-pair ports is critical in complex designs. Run the differential pairs directly from the device to the discrete termination components (located close to the transformers).

The transformer isolation voltage rating should be 2 kV to protect the circuitry from static voltages across the connectors and cables. The signals running from the transformers to the connector should run in close pairs directly to the connector. Be careful not to cross the transmit and receive pairs. One way to avoid a problem is to run the receive pairs on the component side and the transmit pairs on the solder side.

The PCB layout should have no ground or power planes from the transformers to the connectors. The receive and transmit signals should be the only traces in this area. Place the chassis ground for the connectors near the edge of the PCB, away from the signals, connecting the connector shield within the wide etch of the chassis ground.

RBIAS Pins

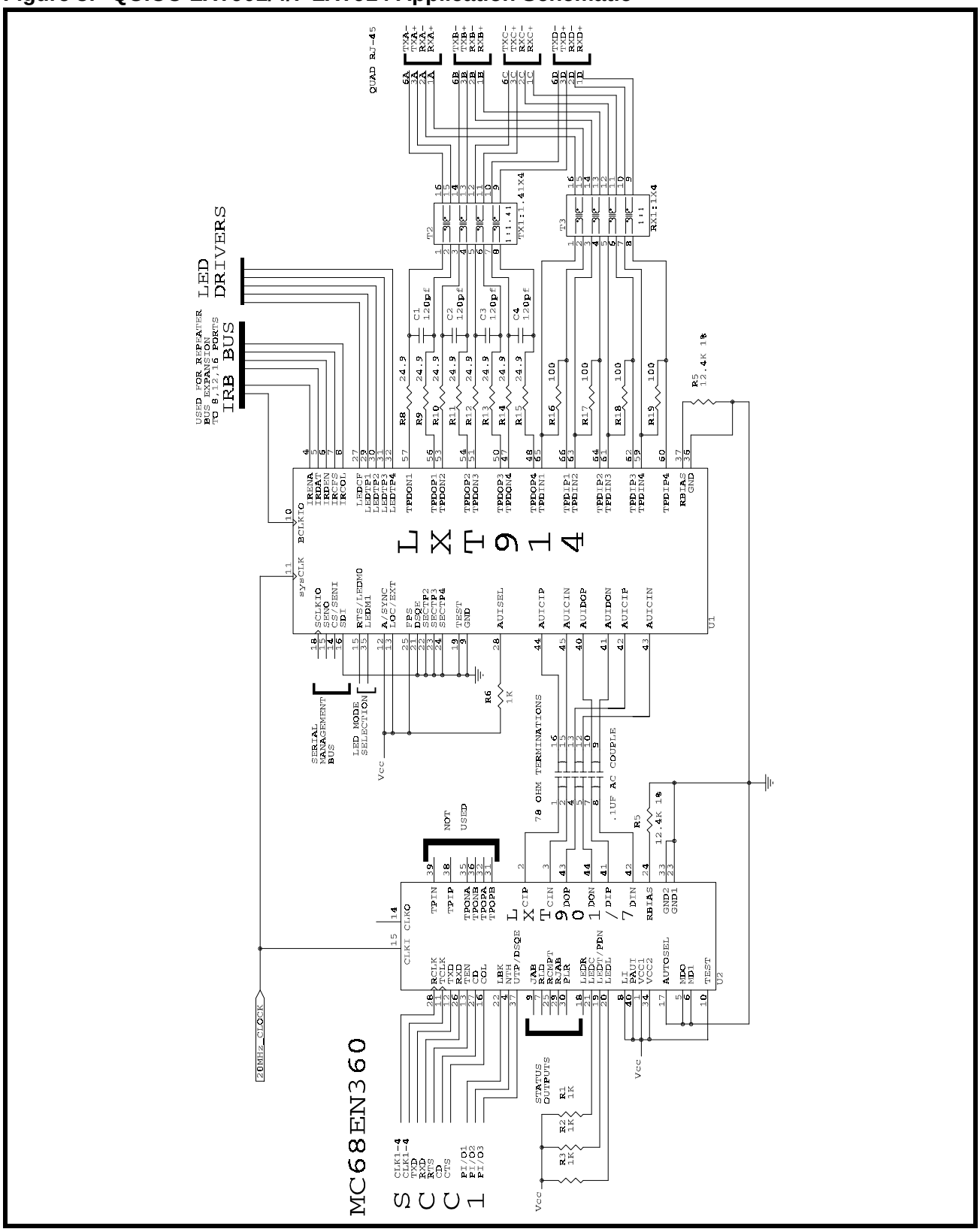
The RBIAS resistor for the LXT901/4/7 devices should be placed as close to the pin as possible with no vias between the device and the resistor (SMT). The other side should share the via with GND1 (pin 23). There should be no other signals running through or under this area. The RBIAS signal sets the levels for the output drivers of the device. Emissions or common mode noise entering the device here will be seen on the output signals.

Lay out the LXT914 device with a 12.4 kΩ, 1% resistor directly connected to pin 37. The ground signals from pins 36 & 38 should come directly off of the device to surround the resistor and pin forming a partition between the RBIAS resistor and the other signals on the PCB.

Table 4: Manufacturers Magnetics List

Manufacturer	Quad Transmit	Quad Receive	Tx/Rx Pairs
Bell Fuse	S553-5999-02	S553-5999-03	
Fil-Mag	23Z338	23Z339	
HALO (Octal)	TD54-1006L1 TG54-1006N2	TD01-1006L1 TG01-1006N2	TD42-2006Q TD43-2006K TG42-1406N1 TG43-1406N TG44-S010NX
Kappa	TP4003P	TP497P101	
Nanopulse	5976	5977	
PCA	EPE6009	EPE6010	
VALOR	PT4116	PT4117	PT4069N1 PT4068N1 ST7011S2 ST7010S2

Figure 3: QUICC-LXT901/4/7-LXT914 Application Schematic



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Revision	Date	Status
1.1	07/97	Corrected schematic to pull 901/907 TEST pin High.
1.0	04/96	Initial Release

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