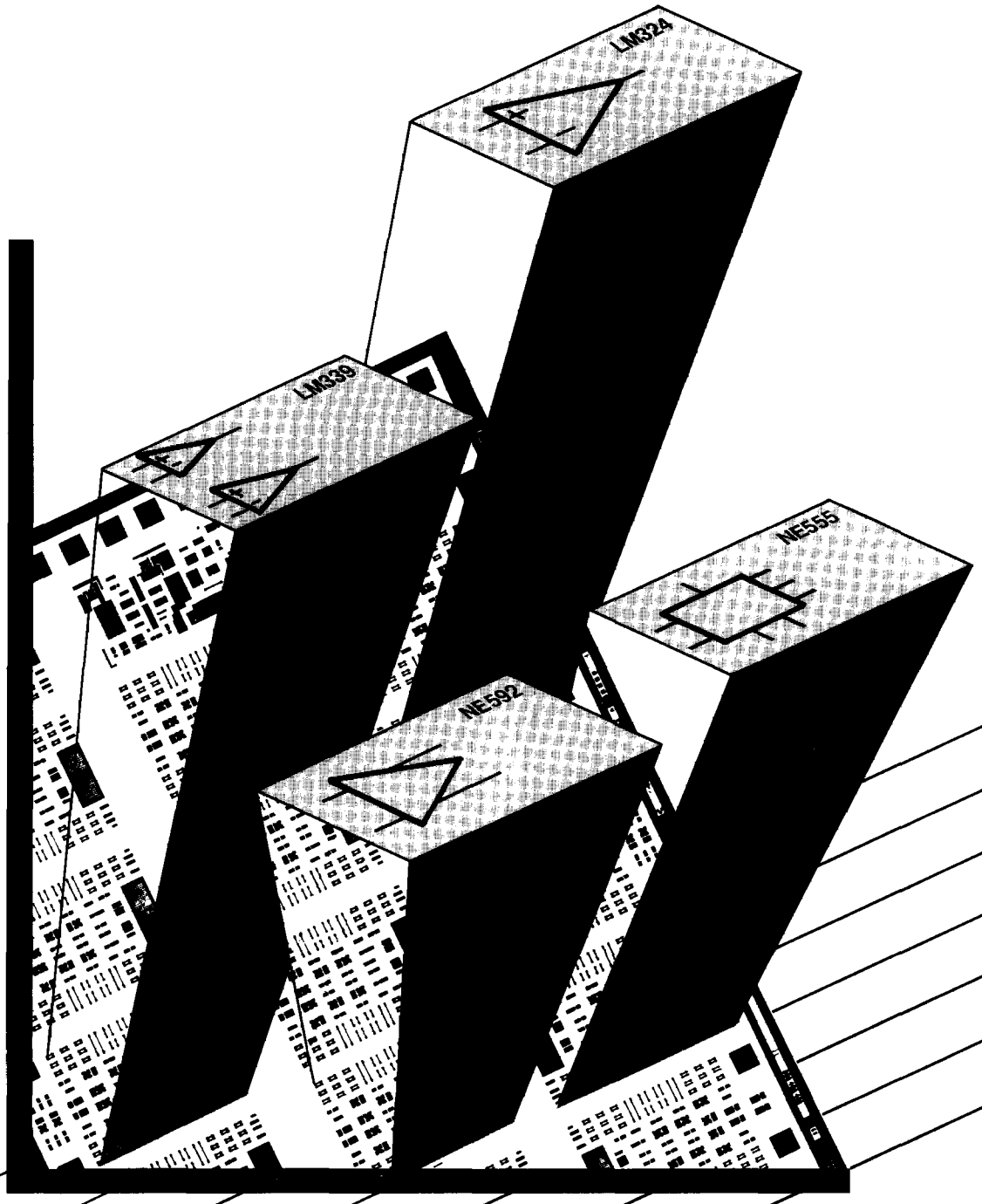
FB 300

TILE ARRAY FAMILY



Micro Linear

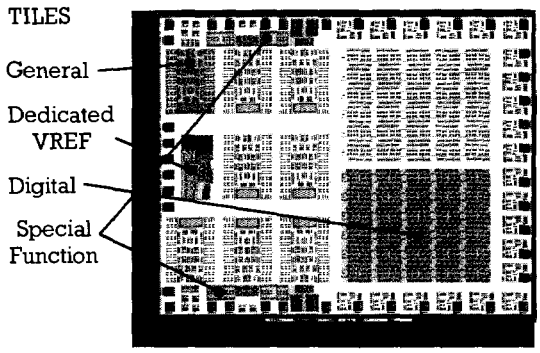
FB300

INTRODUCTION

Micro Linear's FB300 family of TILE ARRAYS offer the first true building block approach to linear integrated circuit design. The dual-metal TILE ARRAY is a collection of repeated tiles, each tile being an array of components such as transistors, resistors, and capacitors. Each tile can be "programmed" into standard analog functions using the MLC300 macro cells. The TILE ARRAY provides for a system approach to IC design while maintaining complete design flexibility.

By using the MLC300 Macro Cells, a tile can be configured into a "standard product" functional block. The macro cell family contains such familiar functions as the μA741, LM324, NE592, LM339, LM360, and a growing number of others. The macro cell is pre-characterized and is a pre-defined metalization pattern. Most importantly, a rapid and successful first time integration is expected since the macro cell layouts are already defined and they have been integrated and tested.

THE FB330 TILE ARRAY

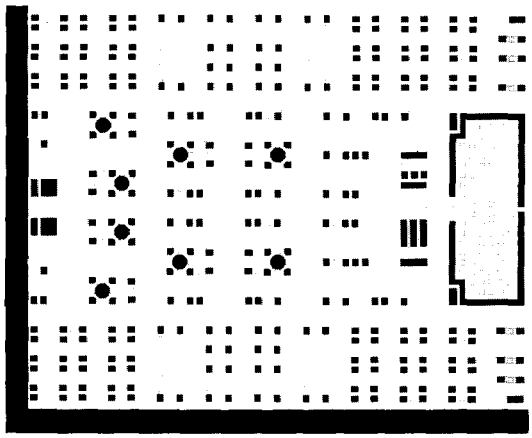


Besides the "general" analog tiles, a "dedicated" Vref tile and "special purpose" tiles are incorporated on each FB300 family array. A special "digital" tile is also used on the FB330 array, as shown above.

Contact Micro Linear for additional information on the FB330.

The tile architecture on Micro Linear's FB300 TILE ARRAY is carefully engineered to afford state-of-the-art performance and maximum versatility. The tile's component mix permits modern current source biasing for high performance with low power. The components that are used for the input stage of the macro cell op amps and comparators are grouped for the best possible matching to minimize offsets and thermal drift. The capacitor on the tile eliminates external compensation capacitors for op amps. This results in a savings of components, board space, and package pin count, and increases reliability. Ion implanted resistors have been included; these high resistor values in a small silicon area simplify low power designs. Dual layer metal greatly simplifies interconnection and power supply bussing.

GENERAL PURPOSE ANALOG TILE



The FB300 family of arrays is supported on Micro Linear IBM PC-XT-AT based work station, LINEAR CAD.

	FB308	FB312	FB315	FB330
Tiles				
general	7	10	13	8
dedicated	1	1	1	1
special function	1	1	1	1
digital				2*
Transistors				
npn	173	238	307	188**
pnp	79	138	181	108**
Resistance				
diffused	440k	623k	796k	490k**
implant	2240k	3200k	4160k	2560k**
Capacitance	70pF	100pF	130pF	80pF
Total components	993	1426	1847	1168 + 142 gates
Bonding pads	24	28	44	42

*142 logic gates.
**not including logic gates.

LINEAR CAD

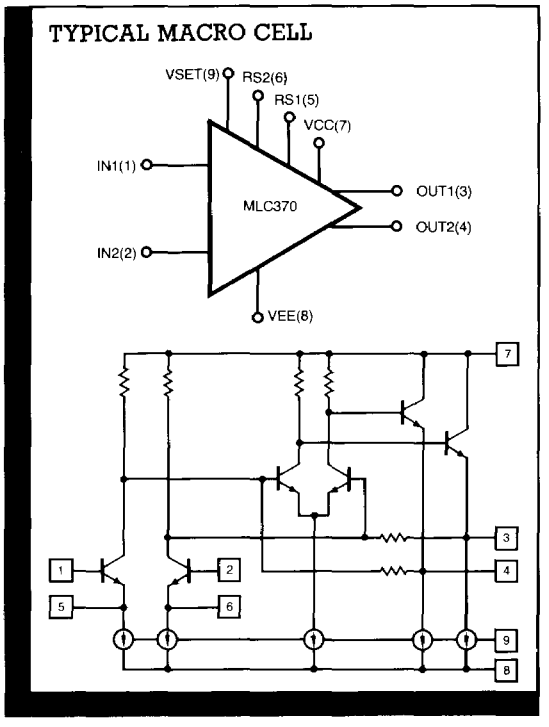
COMPUTER AIDED DESIGN

LINEAR CAD is the first personal computer software package to convert the IBM PC into a CAE workstation for the design of semi-custom/custom linear integrated circuits. Its full-feature graphics editor enables a circuit designer to create schematic diagrams directly on the IBM PC monitor.

Graphic symbols for electronic components are taken from component libraries and arranged on the screen until the desired schematic is created. An interface program then generates a netlist file from the schematic for use with powerful circuit simulation tools such as SPICE and ASPEC.

COMPONENT LIBRARIES

There are two types of component libraries included with the LINEAR CAD package. The first is the library of standard components such as resistors, capacitors, inductors, transistors, current sources, voltage sources, batteries and ground symbols. The second consists of Micro Linear's macro cells and model parameters. Macro cells are called up as components and appear as blocks with numbered pins on the screen. The user is spared the internal complexity of the cell; the software keeps track of the circuitry inside the block and integrates it into the final net list.



DETAILED MODELING INFORMATION

Effective use of any computer simulation tool requires valid model parameters. All of Micro Linear's cells are integrated and characterized to ensure that the specifications and model parameters that are published are accurate. Our goal is to make simulation results a true representation of the finished IC's performance.

The FB300 macro cell library diskette contains all necessary model parameters to support a complete circuit simulation. LINEAR CAD also includes a version of SPICE that runs directly on the IBM PC. A hard copy of the finished schematic can be generated on a dot matrix printer or a pen plotter.

SYSTEM SPICE

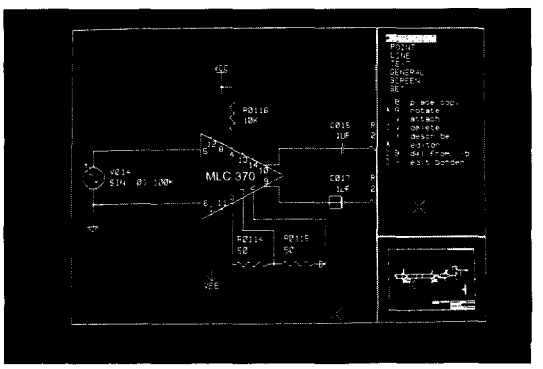
LINEAR CAD comes complete with a version of the circuit simulator SPICE that runs directly on the IBM PC or the IBM PC-XT equipped with at least 512k bytes of RAM, the 8087 co-processor and the MS DOS 2.1 operating system. This SPICE package uses the same input files and commands that are required when running SPICE on mainframes. The analyses that LINEAR CAD can perform are:

DC sweep
Bias point
Small signal transfer function
Sensitivities
AC analysis
Noise analysis
Transient (time) response
Fourier components

All of these analyses can be done at any temperature or range of temperatures. SPICE on LINEAR CAD allows the designer to build and evaluate "computer breadboards" of circuits with up to 140 transistors without touching a single piece of hardware.

COMPUTER SERVICES

The SPICE files that LINEAR CAD yields are suitable for input to most versions of SPICE that are available on computer timeshare services or in-house computers running Berkeley SPICE. The use of computer services for simulations is attractive for large circuits or for reducing the run time for very long and detailed analyses.



GENERAL SPECIFICATIONS

GENERAL SPECIFICATIONS

The analog arrays are fabricated on a high-density bipolar 12V process. Customization of the prefabricated base layers is achieved with dual layer metallization. The components included in the programmable linear tile are listed in the table below:

CONTENTS OF LINEAR TILE

COMPONENT DESCRIPTION	QUANTITY
Minimum geometry npn transistor	14
Dual emitter npn transistor	2
Circular emitter npn transistor	2
Minimum geometry vertical pnp	4
Quad collector lateral pnp	8
Tri-emitter npn transistor	1
Medium geometry vertical pnp	1
Capacitor (programmable up to 10pF)	1
850 ohm p-base resistor	72
35 ohm n-emitter resistor	6
5k ohm p-implant resistor	8
10k ohm p-implant resistor	8
25k ohm p-implant resistor	8
Resistor epi contact	2
Substrate contact	1

The process yields typical NPN transistor beta of 150 with a 1 GHz f_t and pnp beta of 20 with a 5MHz f_t. The absolute resistance and capacitance tolerances are ± 20% with resistance matching ± 2% on the same tile. The temperature coefficient for the p-base resistor is 1500 ppm/°C and 2000ppm/°C for the p-implant resistor.

Where room permits on the arrays, extra transistor clusters have been added adjacent to the linear programmable tiles. These provide additional resources. One such transistor cluster has six minimum geometry npn transistors and two quad collector lateral pnp transistors. A simple unity-gain buffer can be made with these devices. Another cluster contains four circular emitter npn transistors, which can be used in conjunction with a neighboring programmable tile to create a quad-connected npn input stage or low-noise input stage.

Each FB300 array contains a dedicated voltage reference tile and a special function tile. The voltage reference tile provides optimized temperature stability due to the tight resistor and Vbe matching. Most custom analog designs require this stable voltage reference for internal biasing. All of the macro cells require a 2.5V reference from this cell.

VOLTAGE REFERENCE CELL SPECIFICATIONS

Reference voltage	VEE + 2.5 or 5.0V
Maximum current sourcing	10mA
Thermal stability	< 100 ppm/deg. C

SPECIAL FUNCTION TILE

COMPONENT DESCRIPTION	QUANTITY
Large geometry npn (400mA)	4
Low base resistance npn	4
< 1% matched 450 p-base resistor	20

Components on the special function tile add to the arrays capability. The large geometry npn devices are ideal for current output requirements. Low input-noise circuits are also possible with the low base resistance of the high current npn's. Even an eight-bit DAC can be constructed by using the 450 ohm resistors (and two general analog tiles).

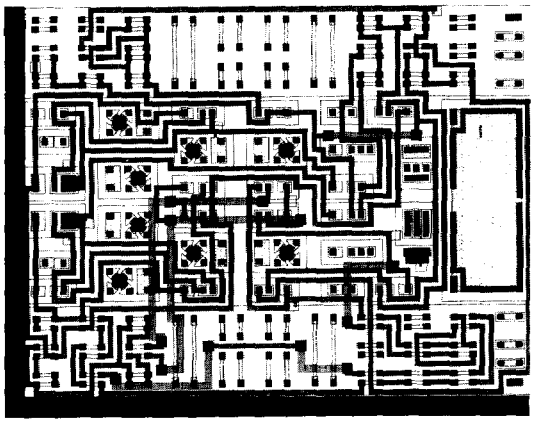
The FB300 family architectural arrangement allows a flexible system design. Any combination of tile components or pre-defined macro cell functions can be used to develop an analog or analog/digital system on a single integrated circuit.

MACRO CELLS

INTRODUCTION

The component arrangement of the FB300 family array tiles allows the layout of the macro cells to be predefined. This unique feature reduces the development time significantly since routing is then limited to interblock connections. Because all general purpose tiles in the FB300 family are identical, macro cell performance characteristics are highly predictable and reproducable from tile to tile. Macro cells MLC300 through MLC330 (not listed) are discrete devices and are useful in developing additional functional blocks. New cells and mask-programmable options are continuously added to the library.

GENERAL PURPOSE ANALOG TILE WITH PRE-DEFINED MLC370 MACRO CELL METALIZATION



MACRO CELLS DEMO PARTS

Packaged macro cells are available for breadboarding and characterization purposes. These are DIP packages containing one or more macro cells fabricated using standard FB300 arrays. Packaged macro cells allow the designer to construct a highly integrated breadboard of the circuit under development. With all critical nodes of the circuit already integrated, artificial capacitive loading of the sensitive nodes is removed, resulting in a more accurate representation of the circuit after integration. For more information, or to order packaged macro cells please contact Micro Linear's Applications Department.

FB300 MACRO CELLS

Micro Linear's macro cells are predesigned, fully tested and characterized functional blocks. A data sheet for each macro cell contains a complete description, electrical specification, and application information for the cell. Most of the macro cells are developed as equivalents to well known commercially available discrete devices. The system designer's familiarity with the discrete devices are carried directly over to his application of the macro cells.

ANALOG MACRO CELLS

CELL	DESCRIPTION	EQUIVALENT
MLC340	2.5V Bandgap voltage ref.	
MLC341	5.0V Bandgap voltage ref.	
MLC345	50 mA Output op amp	
MLC346	Open collector TTL output buffer	
MLC347	Single totem pole TTL output buffer	
MLC349	50 MHz Voltage controlled oscillator	
MLC350	pnp input op-amp	LM324
MLC351	npn input op-amp	μA741
MLC352	Transconductance (gm) op-amp	NE13600
MLC353	Externally compensated op amp	
MLC354	10 V/μS Hi-slew op amp	
MLC360	Ground sensing comparator	LM339
MLC361	High speed, latching comparator (25ns)	LM360
MLC370	Video amplifier	LM592/733
MLC371	Low power video amplifier	
MLC372	Double balanced mod/demodulator	MC1496
MLC373	AGC amplifier	LM1350
MLC381	Timer	NE555
MLC390	Sample and hold buffer	

MICRO LINEAR

CUSTOMIZABLE LSI SOLUTIONS FOR THE LINEAR/DIGITAL WORLD

INTRODUCTION

Micro Linear offers a complete portfolio of customizable LSI solutions for systems designers. Micro Linear's product families and tools such as LINEAR CAD are designed to accomodate a wide range of possible circuit complexities. Our goal is to provide systems designers with a choice of technologies to help them achieve optimum circuit cost/performance. Micro Linear's solutions include the ability to design with functional blocks rather than components for rapid and inexpensive prototyping cycles. A brief description of each of Micro Linear's product families is given below.

FIXED ARRAY

A fixed array is a combination of uncommitted active and passive components (such as transistors and resistors) that are arranged on a chip for ease of inter-connection. Once the circuit design is finalized, a metal pattern is designed to connect the components. Circuits can be simulated by computer analysis and with the traditional breadboard. Micro Linear supports fixed arrays with kit parts, design aids, complete characterization data, modeling information and optional macro cells of frequently used functional blocks.

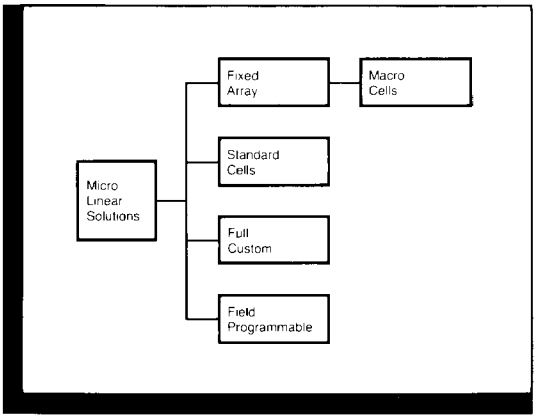
MACRO CELL

Macro cells are predefined and characterized circuit blocks that have been derived from the components available on the fixed arrays. Micro Linear's family of macro cells allows systems designers to design custom ICs at a higher level using functional blocks.

Macro cells offer a multitude of advantages because their performance characteristics are known in actual IC form. In addition to being offered with LINEAR CAD, macro cells are available as packaged parts. If a breadboard is required, a relatively complex one can be constructed with fewer packages and connections using these functional blocks. By using macro cells in breadboards, circuit nodes that are sensitive to stray capacitance won't be artificially loaded by pins and wiring, leaving the designer to guess about the performance of the circuit once it is integrated. The custom IC designed with macro cells has a far better chance of functioning to expectations than one designed completely with uncommitted components.

STANDARD CELL

Standard cells are predesigned, tested and characterized circuit blocks. Unlike a macro cell, however, the components and circuit connection of a standard cell are optimized to achieve the highest possible performance and density for a given function. Standard cells are unique on all layers, not just the interconnect layer as with macro cells. A custom IC is made from standard cells by stacking them together like building blocks. The major drawback to the standard cell approach is the increased fab cycle time for prototypes since all layers must be processed. The standard cell approach is suitable for automatic placement and routing.



FULL CUSTOM

This is the traditional "handcrafted" custom IC. Both the circuit blocks and the interconnection of the blocks are optimized for high performance and the ultimate in silicon area efficiency. This technique is usually cost effective only when production volumes are very high. Full custom linear design is not amenable to automation and is very manpower intensive.

FIELD PROGRAMMABLE SYSTEMS

These circuits are of system-level complexity, with the final configuration, operating mode and performance programmed by the user via software control or permanently fixed by fusible links. This represents the state-of-the-art of application specific linear integrated circuits.

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