MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

Advance Information

MC68(7)05P SERIES

8-BIT MICROCOMPUTERS

OCTOBER, 1984

TABLE OF CONTENTS

TABLE OF CONTENTS
(Continued)

TABLE OF CONTENTS
(Continued)

TABLE OF CONTENTS
(Concluded)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS
(Concluded)

LIST OF TABLES

SECTION 1
INTRODUCTION

The M6805 Family of low-cost single-chip microcomputers was designed for the user who needs an economical microcomputer with the proven capabilities of the M6800-based instruction set. This rapidly expanding family includes a number of memory and package sizes with various I/O functions in both HMOS and CMOS.

The four 8-bit, high-density, N-channel, silicon-gate (HMOS) microcomputers that comprise the MC68(7)05P series are described in this document. These devices are listed below:

MC6805P2 MC6805P4
MC6805P6 MC68705P3

These 8-bit HMOS microcomputers are available in 28-pin, dual-in-line packages.

1.1 DEVICE FEATURES

The following tables summarize the hardware and software features of each device. Differences between the devices will be highlighted throughout this document when applicable.

HARDWARE FEATURES

Features	MC6805P2	MC6805P4	MC6805P6	MC68705P3
8-Bit Architecture	X	X	X	X
RAM (Bytes)	64	112	64	112
User ROM (Bytes)	1100	1100	1796	–
User EPROM (Bytes)	–	–	–	1804
Standby RAM Size is Mask Programmable	–	0	–	–
Standby RAM Power Pin	–	X	–	–
On Chip Clock	X	X	X	X
Memory Mapped I/O	X	X	X	X
Internal 8-Bit Timer with 7-Bit Prescaler	X	X	X	X
Programmable Prescaler	0	0	0	X
Programmable Timer Input Modes	0	0	0	X
External Timer Input	0	0	0	X
Vectored Interrupts	0	0	0	X
Zero-Cross Detection	X	X	X	X
20 TTL/CMOS Compatible Bi-directional I/O Lines				
8 Lines LED Compatible	X	X	X	X
8 Lines CMOS Compatible	0	0	0	X
Master Reset	X	X	X	X
Complete Development System Support on EXORciser	X	X	X	X
Bootstrap Program in ROM	–	–	–	X

EXORciser is a registered trademark of Motorola Inc.

HARDWARE FEATURES (Continued)

Features	MC6805P2	MC6805P4	MC6805P6	MC68705P3
Crystal or Low-Cost Resistor Oscillator	0	0	0	X
Open Drain Port on Ports B and C	0	0	0	–
Open Drain Port on Port B	–	–	0	–
Self-Check Mode	X	X	X	–
5 V Single Supply*	X	X	X	X
Low Voltage Inhibit	0	0	0	–

*Normal Operation

KEY: X = Available; 0 = User Selectable Option; – = Not Available

SOFTWARE FEATURES

Features	MC6805P2	MC6805P4	MC6805P6	MC68705P3
Similar to M6800 Family	X	X	X	X
Byte Efficient Instruction Set	X	X	X	X
Easy to Program	X	X	X	X
True Bit Manipulation	X	X	X	X
Bit Test and Branch Instruction	X	X	X	X
Versatile Interrupt Handling	X	X	X	X
Versatile Index Register	X	X	X	X
Powerful Indexed Addressing for Tables	X	X	X	X
Full Set of Conditional Branches	X	X	X	X
Memory Usable as Register/Flags	X	X	X	X
Single Instruction Memory Examine/Change	X	X	X	X
10 Powerful Addressing Modes	X	X	X	X
All Addressing Modes Apply to ROM, RAM, I/O	X	X	X	–
All Addressing Modes Apply to EPROM, RAM, I/O	–	–	–	X

KEY: X = Available; – = Not Available

1.2 HARDWARE

Every M6805 Family microcomputer contains hardware common to all versions plus a combination of options unique to a particular version. Figures 1-1 through 1-4 illustrate the unique options available on the four versions described in this document.

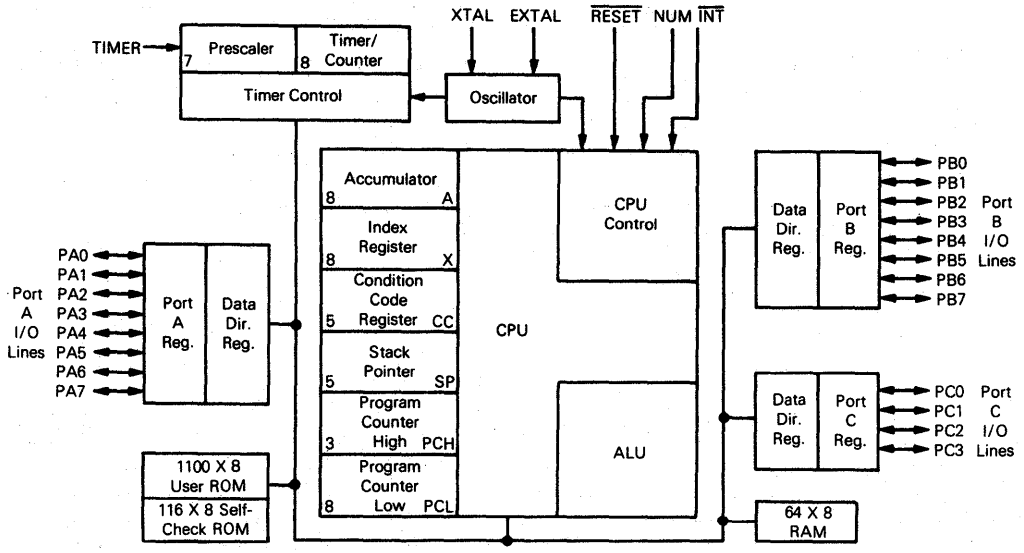


Figure 1-1. MC6805P2 Block Diagram

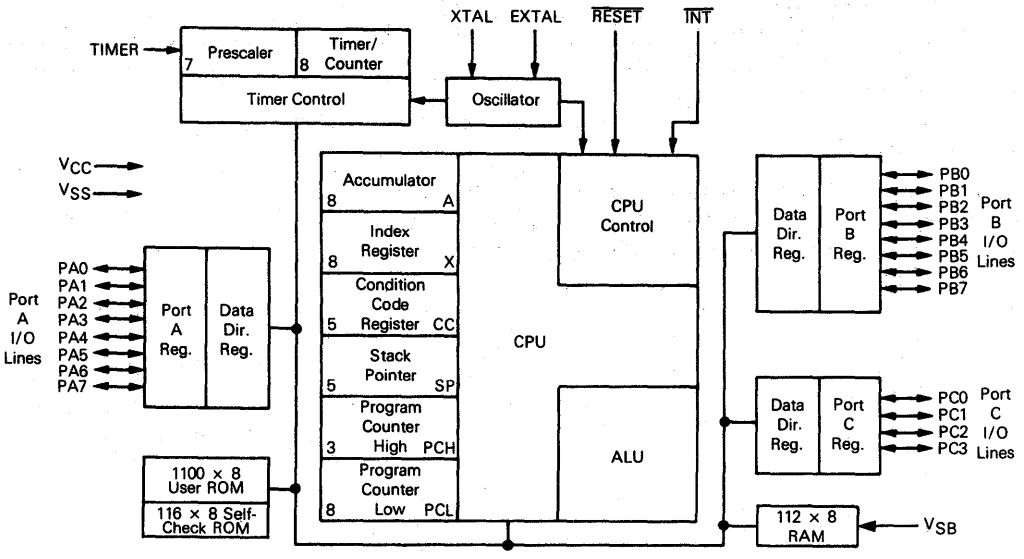


Figure 1-2. MC6805P4 Block Diagram

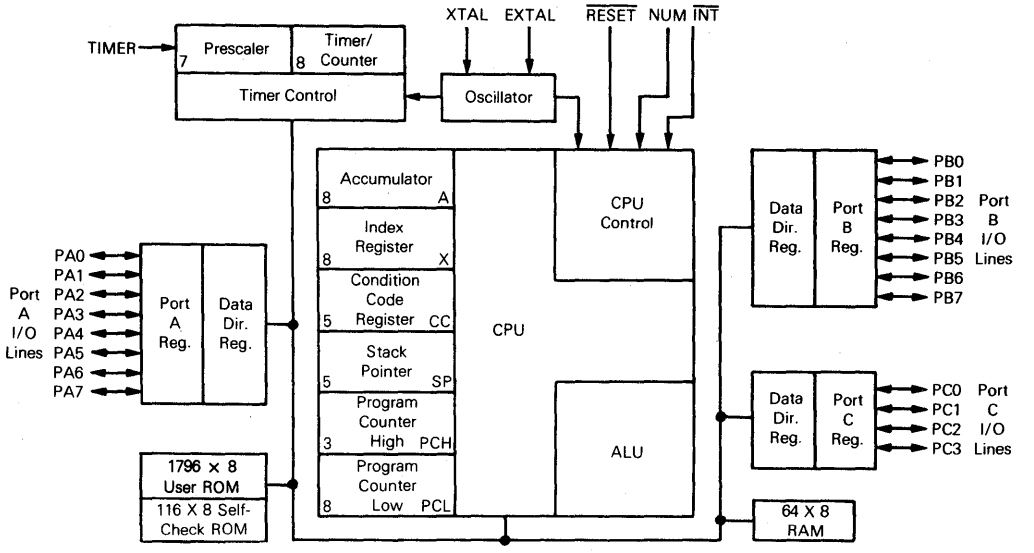


Figure 1-3. MC6805P6 Block Diagram

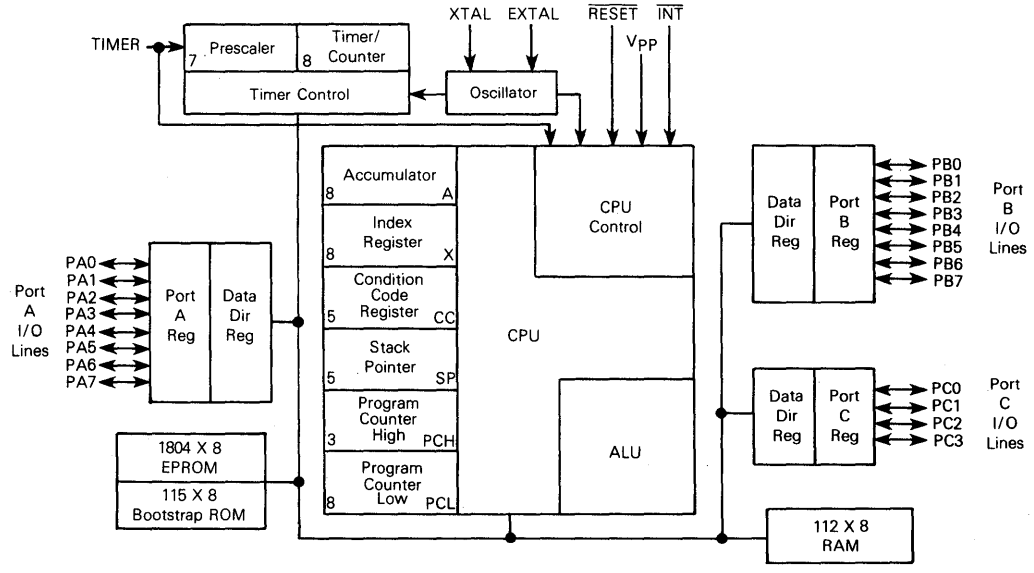


Figure 1-4. MC68705P3 Block Diagram

SECTION 2
SIGNAL DESCRIPTION

Brief descriptions of the input and output signals follow. Where applicable, reference has been made to other sections that contain more detail about the function being performed.

2.1 V_{CC} AND V_{SS}

Power is supplied to the microcomputers using these two pins. V_{CC} is power and V_{SS} is the ground connection.

2.2 V_{SB}

This pin supplies the standby RAM voltage. In order to allow orderly transition to the standby mode, the turn-off rate of V_{CC} must not exceed 1 volt per 100 μs.

2.3 V_{PP}

This pin is used when programming the EPROM. By applying the programming voltage to this pin, one of the requirements is met for programming the EPROM. In normal operation, this pin is connected to V_{CC}. Refer to **SECTION 9 (MASK OPTIONS AND PROGRAMMING)** for more detailed information.

2.4 $\overline{INT}$

This pin provides the capability for asynchronously applying an external interrupt to the microcomputer. Refer to **SECTION 7 (RESET, CLOCK, AND INTERRUPT STRUCTURE)** for additional information regarding the interrupt operation.

2.5 EXTAL AND XTAL

These pins provide control input for the on-chip clock oscillator circuit. A crystal, a resistor, or an external signal (depending upon the user selectable manufacturing mask option) can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized. Refer to **SECTION 7 (RESET, CLOCK, AND INTERRUPT STRUCTURE)** for the recommendations about these inputs.

2.6 TIMER

This pin is used as an external input to control the internal timer/counter circuitry. On the MC68705P3 version, this pin also detects a higher voltage level used to initiate the bootstrap program for loading the internal EPROM [see **SECTION 10 (SOFTWARE)**].

2.7 $\overline{\text{RESET}}$

This pin has a Schmitt trigger input and an on-chip pullup. The microcomputer can be reset by pulling RESET low. Refer to **SECTION 7 (RESET, CLOCK, AND INTERRUPT STRUCTURE)** for additional information.

2.8 NUM (NON-USER MODE)

Pin 6 of the MC6805P2 and MC6805P6 is identified as NUM (non-user mode). This pin is not for user applications and must be connected to V_{SS}.

2.9 INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC3)

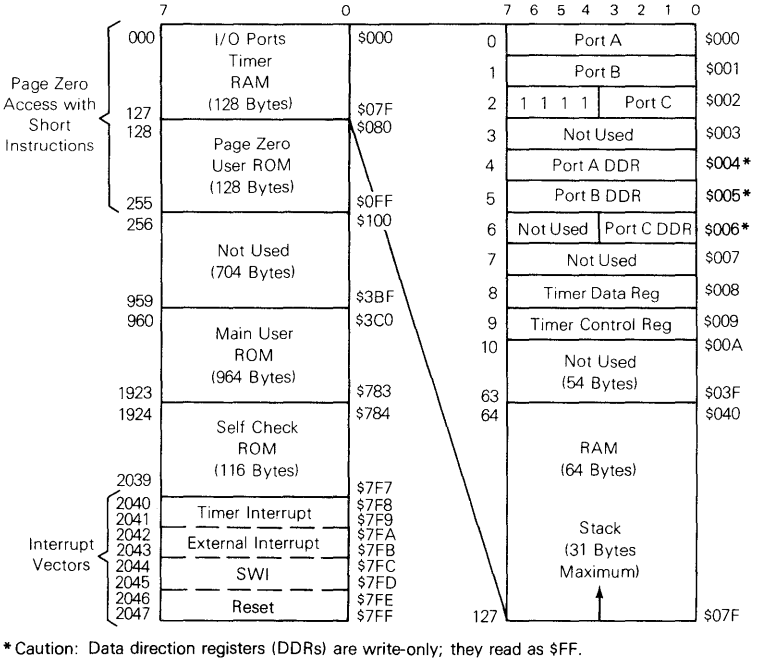
These 20 lines are arranged into two 8-bit ports (A and B) and one 4-bit port (C). All lines are programmable as either inputs or outputs under software control of the data direction registers. Refer to **SECTION 7 (RESET, CLOCK, AND INTERRUPT STRUCTURE)** and **SECTION 8 (INPUT/OUTPUT CIRCUITRY)** for additional information.

SECTION 3
MEMORY CONFIGURATIONS

Each member of the MC68(7)05P series of microcomputers is capable of addressing 2048 bytes of memory and I/O registers. The memory maps for the four versions of the M6805 Family described in this document are shown in Figures 3-1 through 3-4. The amount of ROM, EPROM, and RAM for each device is detailed in **SECTION 1.1 (DEVICE FEATURES).**

3.1 MC6805P2 MEMORY MAP

The memory map for MC6805P2 is shown in Figure 3-1. This device has implemented 1288 of the 2048 possible bytes of memory and I/O registers. The interrupt and $\overline{\text{RESET}}$ vectors are from $7F8 to $7FF. The self-check ROM occupies 116 bytes from $784 to $7F7. The 1100 bytes of user ROM is divided into two portions located from $080 to $0FF and from $3C0 to $783. This division allows 128 bytes of ROM to be addressed with direct instructions. The RAM area of 64 bytes occupies from $000 to $07F. There are 6 bytes of port I/O and 2 timer registers.



*Caution: Data direction registers (DDRs) are write-only; they read as $FF.

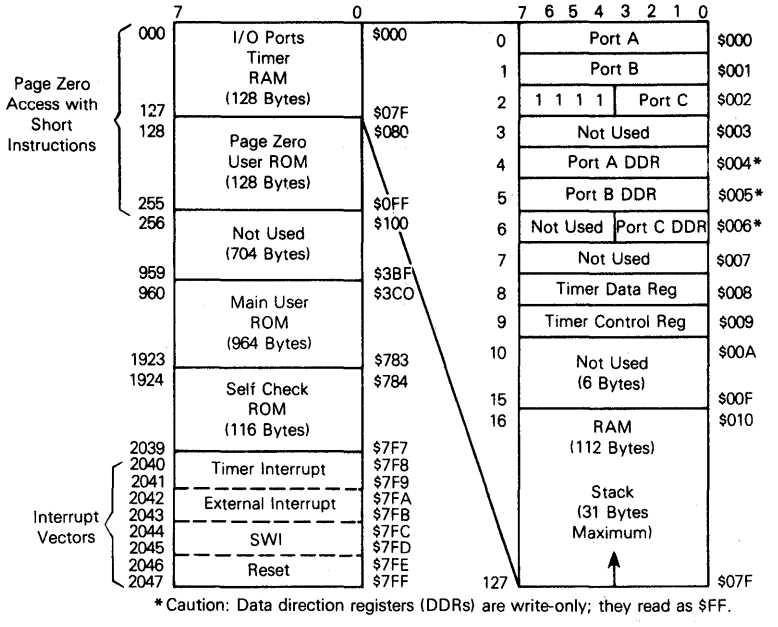
Figure 3-1. MC6805P2 Memory Map

3.2 MC6805P4 MEMORY MAP

The memory map for MC6805P4 is shown in Figure 3-2 and is identical to the MC6805P2 except that it has 112 bytes of RAM ($010 to $07F).

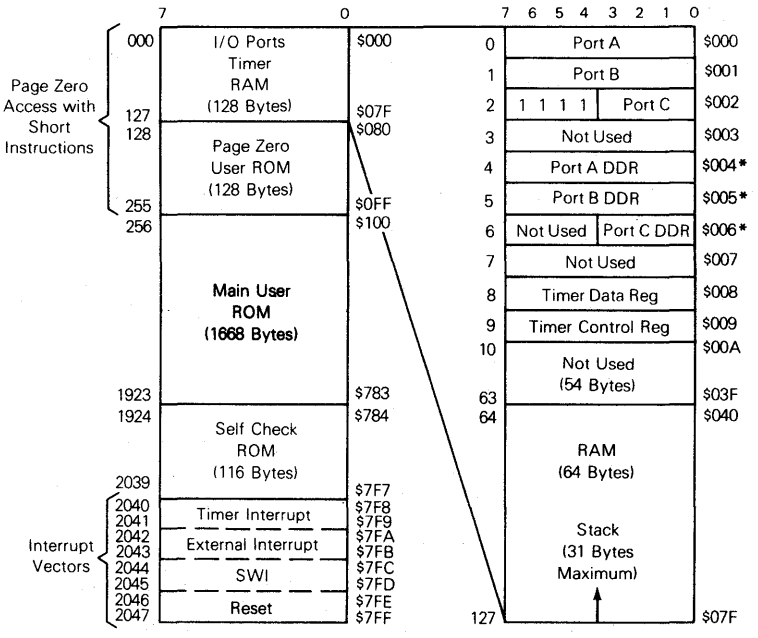
3.3 MC6805P6 MEMORY MAP

The memory map for MC6805P6 is shown in Figure 3-3 and is identical to the MC6805P2 except that it has 1668 bytes of main user ROM ($3C0 to $783).



*Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-2. MC6805P4 Memory Map



*Caution: Data direction registers (DDRs) are write-only; they read as $FF.

Figure 3-3. MC6805P6 Memory Map

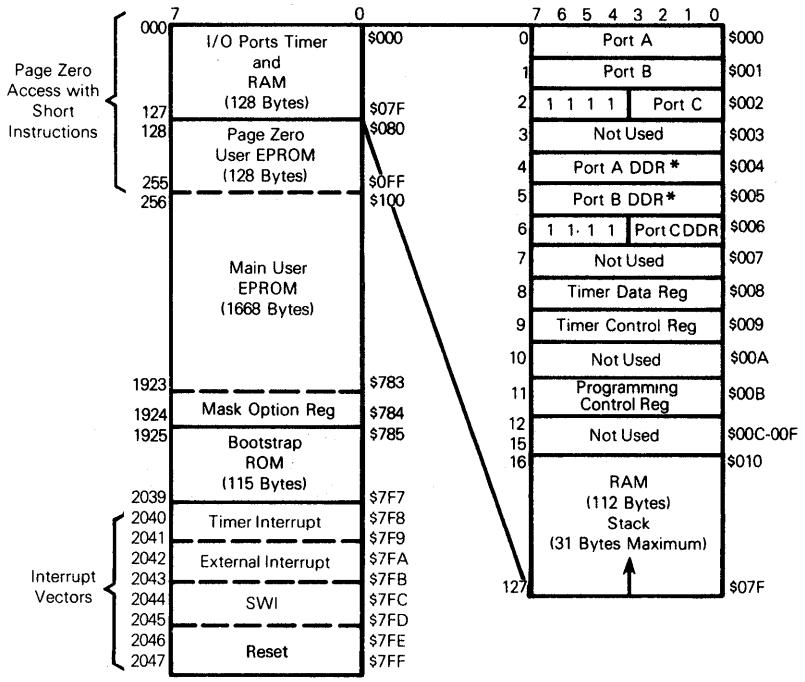
3.4 MC68705P3 MEMORY MAP

The memory map for MC68705P3 is shown in Figure 3-4. This MCU is capable of addressing 2048 bytes of memory and I/O registers with its program counter.

The MCU has implemented 2041 bytes of these locations. This consists of 1804 bytes of user EPROM ($080 to $783), 115 bytes of bootstrap ROM ($785 to $7F7), 112 bytes of user RAM ($010 to $07F), an EPROM mask option register (MOR), a program control register (PCR), and 8 bytes of I/O.

The bootstrap ROM allows the MC68705P3 to program its own EPROM. The bootstrap is a mask programmed ROM. The user EPROM is located in two areas. The main EPROM area is in memory locations $080 to $783. The second area is reserved for 8 interrupt/reset vector bytes at memory locations $7F8 to $7FF.

The MCU uses nine of the lowest 16 memory locations for program control and I/O features such as ports, the port DDRs, and the timer. The mask option register at memory location $784 completes the total. The 112 bytes of user RAM include up to 31 bytes for the stack.



Caution: Data Direction Registers (DDRs) are write-only; they read as $FF.

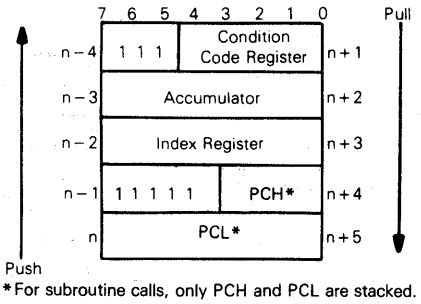
Figure 3-4. MC68705P3 Memory Map

3.5 SHARED STACK AREA

The shared stack area (RAM locations $061 to $07F) is used during the processing of an interrupt or subroutine call to save the contents of the central processing unit state. The register contents are pushed onto the stack in the order shown in Figure 3-5.

Since the stack pointer decrements during pushes, the low order byte of the program counter (PCL) is stacked first. Then the four high-order bits (PCH) are stacked. This ensures that the program counter is loaded correctly during pulls from the stack, since the stack pointer increments when it pulls data from the stack.

A subroutine call results in only the program counter (PCL and PCH) contents being pushed onto the stack. The remaining CPU registers are not pushed. The shared stack area must be used with care when it is used for data storage or temporary work locations to protect it from being overwritten, due to stacking from an interrupt or subroutine call.



*For subroutine calls, only PCH and PCL are stacked.

Figure 3-5. Interrupt Stacking Order

3.6 CENTRAL PROCESSING UNIT

The central processing unit for the M6805 Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal address, data, and control buses.

SECTION 4
PROGRAMMABLE REGISTERS

The M6805 Family CPU has five registers available to the programmer. They are shown in Figure 4-1 and are explained in the following paragraphs.

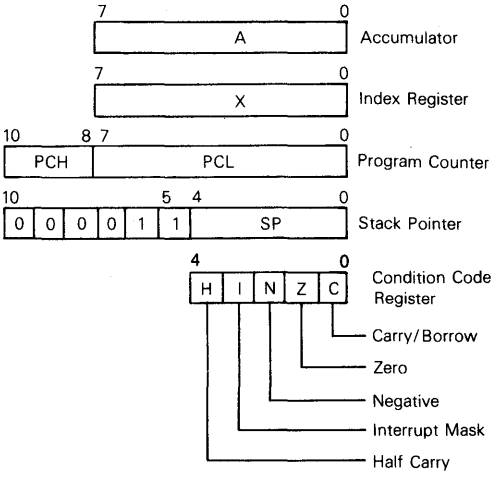


Figure 4-1. Programming Model

4.1 ACCUMULATOR (A)

The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

4.2 INDEX REGISTER (X)

The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit value that may be added to an 8- or 16-bit immediate value to create an effective address. The index register may also be used as a temporary storage area.

4.3 PROGRAM COUNTER (PC)

The program counter is an 11-bit register that contains the address of the next byte to be fetched.

4.4 STACK POINTER (SP)

The stack pointer is an 11-bit register that contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set at location $07F. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

The six most significant bits of the stack pointer are permanently set at 0000011. Subroutines and interrupts may be nested down to location $061 (31 bytes maximum), which allows the programmer to use up to 15 levels of subroutine calls (less if interrupts are allowed).

4.5 CONDITION CODE REGISTER (CC)

The condition code register is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific actions can be taken as a result of their state. Each bit is explained below.

4.5.1 Half Carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

4.5.2 Interrupt (I)

When this bit is set, the timer and external interrupt ($\overline{INT}$) is masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and is processed as soon as the interrupt bit is cleared.

4.5.3 Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logic 1).

4.5.4 Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

4.5.5 Carry/Borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logical unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions, and during shifts and rotates.

SECTION 5
TIMER

The timer circuitries for the four versions of the M6805 Family covered in this document are described below. Note that while each timer consists of an 8-bit software programmable counter driven by a 7-bit prescaler, there are two distinctly different configurations. The MC6805P2/P4/P6 devices have one configuration (Figure 5-1) and the MC68705P3 has another configuration (Figure 5-2).

5.1 MC6805P2/P4/P6 TIMER CIRCUITRY

The timer circuitry for the MC6805P2, MC6805P4, and MC6805P6 microcomputers is shown in Figure 5-1. The 8-bit counter may be loaded under program control and is decremented toward zero by the clock input (or prescaler output). When the timer reaches zero, the timer interrupt request bit (bit 7) in the timer control register (TCR) is set.

The timer interrupt can be masked (disabled) by setting the timer interrupt mask bit (bit 6) in the TCR. The interrupt bit (1 bit) in the condition code register also prevents a timer interrupt from being processed. The MCU responds to this interrupt by saving the present CPU state on the stack, fetching the timer interrupt vector from locations $7F8 and $7F9, and then executing the interrupt routine (see **SECTION 7 RESET, CLOCK, AND INTERRUPT STRUCTURE**). The timer interrupt request bit must be cleared by software.

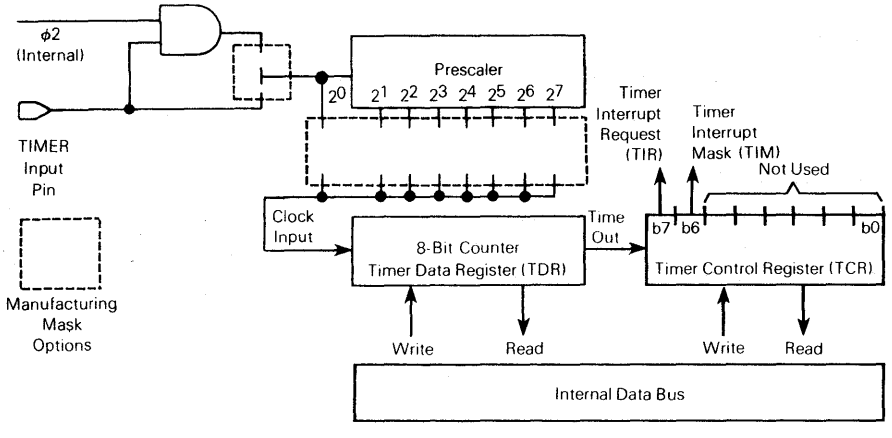


Figure 5-1. MC6805P2/P4/P6 Timer Block Diagram

The clock input to the timer can be from an external source (decrementing of the timer counter occurs on a positive transition of the external source) applied to the timer input pin or it can be from the internal phase two signal.

Three machine cycles are required for a change in state of the $\overline{\text{TIMER}}$ pin to decrement the timer prescaler. The maximum frequency of the signal that can be recognized by the timer pin logic is dependent on the parameter labeled t_{WL}, t_{WH}. The pin logic that recognizes the high state on the pin must also recognize the low state on the pin in order to "re-arm" the internal logic. Therefore the periods can be calculated as follows (assuming a 50/50 duty cycle for a given period):

$$t_{cyc} \times 2 + 250 \text{ ns} = \text{period} = 1/\text{freq}$$

The period is not simply $t_{WL} + t_{WH}$. This computation is allowable, but it does reduce the maximum allowable frequency by defining an unnecessarily longer period (250 nanoseconds times two).

When the phase two signal is used as the source, it can be gated by an input applied to the $\overline{\text{TIMER}}$ input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the mask options that is specified before manufacture of the MC6805P2/P4/P6 MCU parts.

NOTE

For ungated phase two clock input to the timer prescaler, the $\overline{\text{TIMER}}$ pin should be tied to V_{CC}.

A prescaler option (divide by 2^n) can be applied to the clock input. This option will extend the timing interval up to a maximum of 128 counts before decrementing the counter. This prescaling mask option must be specified before manufacture of the MCU. To avoid truncation errors, the prescaler is cleared when bit 3 of the timer control register is written to a logic one (this bit always needs a logic zero).

The timer continues to count past zero, falling from $00 through to $FF, and then continues the countdown. Thus, the counter can be read at any time by reading the timer data register (TDR). This allows a program to determine the length of time since a timer interrupt has occurred without disturbing the counting process.

At power up or reset, the prescaler and counter are initialized with all logic ones; the timer-interrupt-request-bit (bit 7) is cleared and the timer-interrupt-mask-bit (bit 6) is set.

5.2 MC68705P3 TIMER CIRCUITRY

The timer for the MC68705P3 microcomputer is shown in Figure 5-2. The timer contains an 8-bit software programmable counter that is driven by a 7-bit prescaler with one-of-eight selectable outputs. Various timer clock sources may be selected ahead of the prescaler and counter. The timer selections are made via the timer control register (TCR) and/or mask option register (MOR). The TCR also contains the interrupt control bits.

The 8-bit counter may be loaded under program control and decremented toward zero by the counter input frequency (f_{CIN}) input (the output of the prescaler selector). Once the 8-bit counter has decremented to zero, it sets the TIR (timer interrupt request) bit (b7 of TCR). The TIM (timer interrupt mask) bit (b6) can be software set to inhibit the interrupt request or software cleared to pass the interrupt request to the processor.

When the I bit in the condition code register is cleared, the processor receives the timer interrupt. The MCU responds to this interrupt by saving the present CPU state on the stack, fetching the timer interrupt vector from locations $7F8 and $7F9, and then executing the interrupt routine.

The processor is sensitive to the level of the timer interrupt request line. If the interrupt is masked, the TIR bit may be cleared by software (e.g., BCLR) without generating an interrupt. The TIR bit **must** be cleared by the timer interrupt service routine to clear the timer interrupt request.

The counter continues to count (decrement) by falling through to $FF from zero. Thus, the counter can be read at any time by the processor without disturbing the count. This allows a program to determine the length of time elapsed since the occurrence of a $\overline{\text{TIMER}}$ interrupt without disturbing the counting process.

The clock input to the timer can be from an external source (decrementing the counter occurs on a positive transition of the external source) applied to the timer input pin or from the internal phase two signal. The maximum frequency of a signal that can be recognized by the $\overline{\text{TIMER}}$ or $\overline{\text{INT}}$ pin logic is dependent on the parameter labeled t_{WL}, t_{WH}. The pin logic must recognize the high and low states on the pin in order to "re-arm" the internal logic. Therefore, the periods can be calculated as follows (assuming a 50/50 duty cycle for a given period):

$$t_{cyc} \times 2 + 250 \text{ ns} = \text{period} = 1/\text{freq}$$

The period is not simply $t_{WL} + t_{WH}$. This computation is allowable, but it does reduce the maximum allowable frequency by defining an unnecessarily longer period (250 nanoseconds times two).

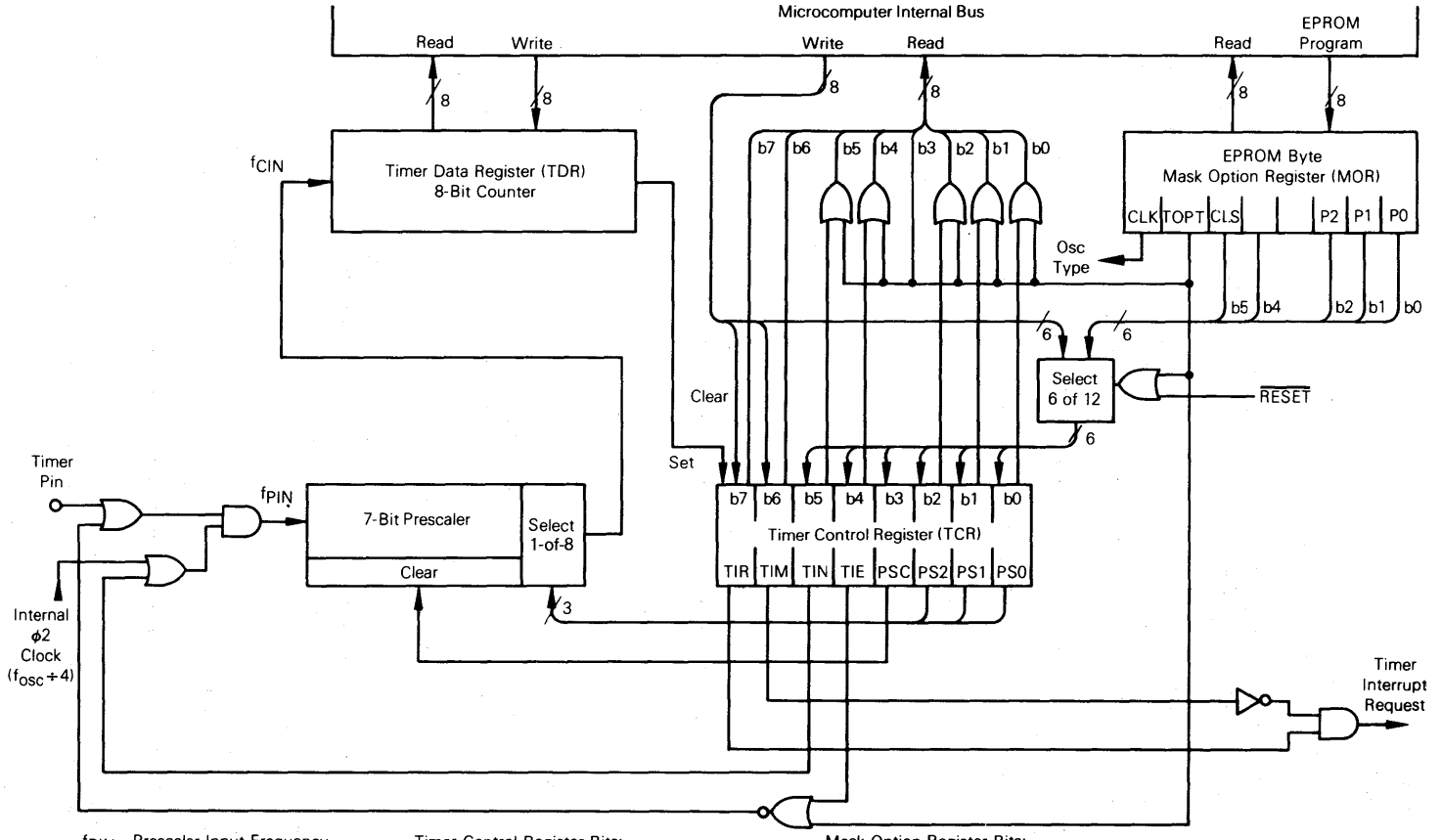
When the phase two ($\phi 2$) signal is used as the source, it can be gated by an input applied to the $\overline{\text{TIMER}}$ input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is selected via the TCR or the MOR as described later.

A prescaler option can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before decrementing the counter. The prescaling TCR or MOR option selects one of eight outputs on the 7-bit binary divider; one output bypasses prescaling. To avoid truncation errors, the prescaler is cleared when bit 3 (b3) of the TCR is written to a logic one; however, the TCR bit 3 always reads as a logic zero to ensure proper operation with read-modify-write instructions (bit set and clear for example).

At reset, the prescaler and counter are initialized to an "all ones" condition; the timer interrupt request bit (TCR, b7) is cleared and the timer interrupt request (TCR, b6) is set. TCR bits b0, b1, b2, b4, and b5 are initialized by the corresponding mask option register (MOR) bits at reset. They are then software selectable after reset if the TOPT bit (b6) in the MOR equals zero.

Note that the timer clock diagrams in Figures 5-2 and 5-3 reflect two separate timer control configurations: (a) software-controlled mode via the timer control register (TCR) and (b) MOR controlled mode to emulate a mask ROM version with the mask option register.

In the software-controlled mode, all TCR bits are read/write except for bit b3 which is write-only (always reads as a logic zero). In the MOR-controlled mode, all TCR bits b7 and b6 are read/write and bits b5, b4, b2, b1, and b0 have no effect on a write (always read as logic one). For the MC68705P3 bit b3 is write only (reads as logic zero).



f_{PIN} – Prescaler Input Frequency
f_{CIN} – Counter Input Frequency

Timer Control Register Bits:
- TIR – Timer Interrupt Request Status
- TIM – Timer Interrupt Mask
- TIN – Timer Input Select
- TIE – Timer External Input Enable
- PSC – Prescaler Clear
- PS2, PS1, PS0 – Prescaler Select

Mask Option Register Bits:
- CLK – Clock Oscillator Type
- TOPT – Timer Mask/Programmable Option
- CLS – Timer Clock Source
- P2, P1, P0 – Prescaler Option

NOTE: The TOPT bit in the Mask Option Register selects whether the timer is software programmable via the Timer Control Register or emulates the mask programmable parts via the MOR PROM byte.

Figure 5-2. MC68705P3 Timer Block Diagram

5.2.1 Software Controlled Mode

The TOPT (timer option) bit (b6) in the mask option register is EPROM programmed to a logic zero to select the software controlled mode. TCR bits b5, b4, b3, b2, b1, and b0 give the program direct control of the prescaler and input select options.

The timer prescaler input frequency (f_{PIN}) can be configured for three different operating modes plus a disable mode, depending upon the value written to TCR control bits b4 and b5 (TIE and TIN).

When the TIE and TIN bits are programmed to zero, the timer input is from the internal clock (phase two, $\phi 2$) and the timer input pin is disabled. The internal clock mode can be used for periodic interrupt generation as well as a reference for frequency and event measurement.

When TIE = 1 and TIN = 0, the internal clock and the timer input pin signals are ANDed to form the timer input. This mode can be used to measure external pulse widths. The external pulse simply gates in the internal clock for the duration of the pulse. The accuracy of the count in this mode is ± 1.

When TIE = 0 and TIN = 1, no prescaler input frequency is applied to the prescaler and the timer is disabled.

When TIE and TIN are both programmed to a one, the timer is from the external clock. The external clock can be used to count external events as well as to provide an external frequency for generating periodic interrupts.

Bits b0, b1, and b2 in the TCR are program controlled to choose the appropriate prescaler output. The prescaling divides the prescaler input frequency by 1, 2, 4, etc. (binary multiples to 128) to produce the counter input frequency to the counter. The processor cannot write into or read from the prescaler; however, the prescaler is set to all ones by a write operation to TCR, b3 (when bit 3 of the written data equals one) that allows for truncation-free counting.

5.2.2 MOR Controlled Mode

The MOR-controlled mode of the timer is selected when the TOPT (timer option) bit (b6) in the MOR is programmed to a logic one to emulate the MC6805P2/P4/P6 mask-programmable prescaler and timer clock source. The timer circuits are the same as described above; however, the timer control register (TCR) is configured differently as discussed below.

The logic level for the functions of bits b0, b1, b2, and b5 in the TCR are all determined at the time of EPROM programming. They are controlled by corresponding bits within the mask option register (MOR, $784). The value programmed into MOR bits b0, b1, b2, and b5 controls the prescaler division and the timer clock selection.

Bits b4 (TIE) and b3 (PSC) in the TCR are set to a logic one in the MOR-controlled mode (when read by software, these six TCR bits always read as logic ones). As in the software programmable configuration, the TIM (b6) and TIR (b7) bits of the TCR are controlled by the counter and software as described above and in **Section 5.2.3 Timer Control Register (TCR)** below.

The MOR-controlled mode is designed to exactly emulate the MC6805P2/P4/P6 that have only TIM and TIR in the TCR and have the prescaler options defined as manufacturing mask options.

5.2.3 Timer Control Register (TCR)

The configuration of the TCR is determined by the logic level of bit 6 (timer option TOPT) in the mask option register (MOR). Two configurations of the TCR are shown below, one for TOPT = 1 and the other for TOPT = 0. TOPT = 1 configures the TCR to emulate the MC6805P2/P4/P6. When TOPT = 1, the prescaler "mask" options are user programmable via the MOR. A description of each TCR bit is provided below (also see Figure 5-2).

b7	b6	b5	64	b3	b2	b1	b0	Timer Control
TIR	TIM	1	1	1	1	1	1	Register $009

TCR with MOR TOPT = 1 (MC6805P2/P4/P6 Emulation)

b7	b6	b5	64	b3	b2	b1	b0	Timer Control
TIR	TIM	TIN	TIE	PSC*	PS2	PS1	PS0	Register $009

TCR with MOR TOPT = 0 (Software Programmable Timer)

* = write only, reads as a zero

b7, TIR Timer Interrupt Request—The TIR initiates the timer interrupt or signals a timer data register underflow when at logic one.

Logic 1 is set when the timer data register changes to all zeros.
Logic 0 is cleared by external reset or under program control.

b6, TIM Timer Interrupt Mask—The TIM inhibits the timer interrupt to the processor when at logic one.

Logic 1 is set by an external reset or under program control.
Logic 0 is cleared under program control.

b5, TIN Timer Input Source—The TIN selects the input clock source that is either the external timer pin (7) or the internal $\phi 2$.

Logic 1 selects the external clock source.
Logic 0 selects the internal $\phi 2$ ($f_{OSC}/4$) clock source.

b4, TIE Timer Enable—TIE is used to enable the external timer pin (7) or to enable the internal clock (if TIN = 0) regardless of the external timer pin state (disables gated clock feature). When TOPT = 1, TIE is always a logic one.

Logic 1 enables the external timer pin.
Logic 0 disables the external timer pin.

Prescaler Select—These bits are decoded to select one of either outputs on the timer prescaler. The table below shows the prescaler division resulting from decoding these bits.

b3, PSC — Prescaler Clear—This is a write-only bit. It reads a logic zero (when TOPT equals 0) when the BSET and BCLR on the TCR function correctly. Writing a "1" into PSC generates a pulse which clears the prescaler. (When TOPT equals 1, this bit is always read as logic "1" and has no effect on the prescaler.)

b2, PS2
b1, PS1
b0, PS0 — Prescaler Select—These bits are decoded to select one of either outputs on the timer prescaler. The table below shows the prescaler division results from decoding these bits.

PS2	PS1	PS0	Prescaler Division
0	0	0	1 (Bypass Prescaler)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

NOTE

When changing the PS2-PS0 bits in software, the PSC bit should be written to a "1" in the same write cycle to clear the prescaler. Changing the PS bits without clearing the prescaler may cause an extraneous toggle of the timer data register.

SECTION 6
SELF-CHECK

6.1 ROM-BASED SELF-CHECK

The self-check capability of the MC6805P2/P4/P6 MCU provides an internal check to determine if the part is functional. Connect the MCU as shown in Figure 6-1 and monitor the output of port C bit 3 for an oscillation of approximately 7 Hz. A 9-volt level on the TIMER input pin 7 energizes the ROM-based self-check feature. The self-check program exercises the RAM, ROM, timer, interrupts, and I/O ports.

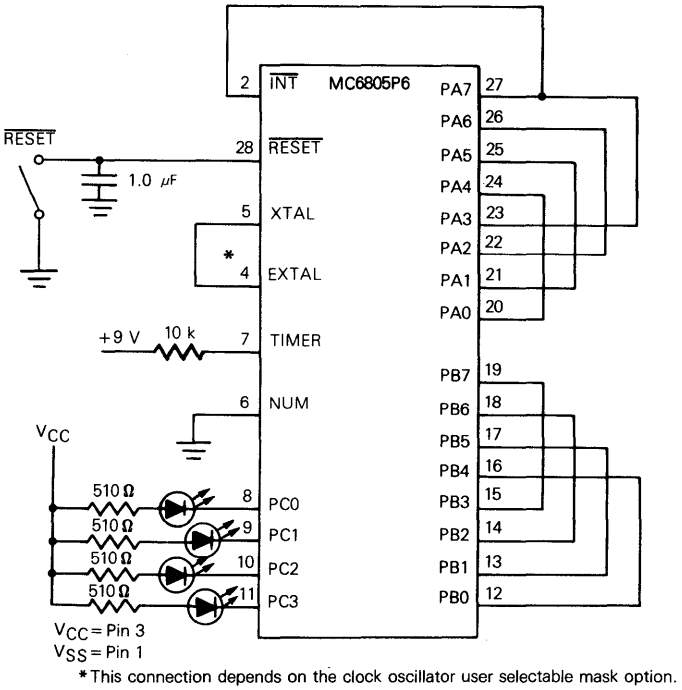


Figure 6-1. Self-Check Connections for MC6805P2/P4/P6

Table 6-1 shows the status of the LEDs as a result of a failure. Port C is tested only once (just after reset). If port C fails, no lights will appear.

Table 6-1. Self-Check Error Patterns

PC1	PC0	Problem
0	0	Interrupt Failure
0	1	Bad Port A or Port B
1	0	Bad RAM
1	1	Bad RAM
All 4 LEDs Flashing		Good Device

NOTE

When PC1 or PC0 is 0, the LED is on.

SECTION 7
RESET, CLOCK, AND INTERRUPT STRUCTURE

7.1 RESET

The MCU can be reset three ways: (1) by initial power-up, (2) by the external reset input ($\overline{\text{RESET}}$) and (3) by an optional, internal, low-voltage detect circuit (not available on the MC68705P3 EPROM version). The $\overline{\text{RESET}}$ input consists mainly of a Schmitt trigger that senses the $\overline{\text{RESET}}$ line logic level. A typical reset Schmitt trigger hysteresis curve is shown in Figure 7-1. The Schmitt trigger provides an internal reset voltage if it senses a logical zero on the $\overline{\text{RESET}}$ pin.

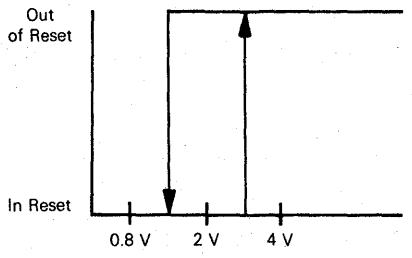


Figure 7-1. Typical Reset Schmitt Trigger Hysteresis

7.1.1 Power-On Reset (POR)

An internal reset is generated upon power-up that allows the internal clock generator to stabilize. A delay of t_{RHL} milliseconds is required before allowing the $\overline{\text{RESET}}$ input to go high. See the power and reset timing diagram (Figure 7-2). Connecting a capacitor to the $\overline{\text{RESET}}$ input (see Figure 7-3) typically provides sufficient delay. During power up, the Schmitt trigger switches on (removes reset) when $\overline{\text{RESET}}$ rises to V_{IRES+}.

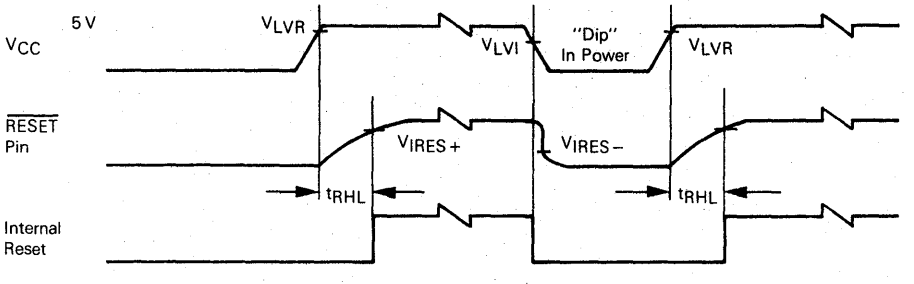


Figure 7-2. Power and Reset Timing

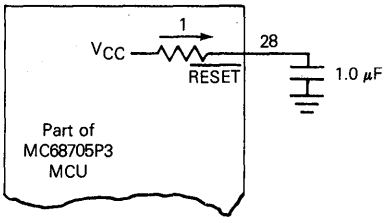


Figure 7-3. Power-Up $\overline{\text{RESET}}$ Delay Circuit

7.1.2 External Reset Input

The MCU is reset when a logic zero is applied to the $\overline{\text{RESET}}$ input for a period longer than one machine cycle (t_{CYC}). Under this type of reset, the Schmitt trigger switches off at V_{IRES-} to provide an internal reset voltage.

7.1.3 Low-Voltage Inhibit (LVI)

The optional low-voltage detection circuit (not available on the MC68705P3) causes a reset of the MCU if the power supply voltage falls below a certain level (V_{LVI}). The only requirement is that the V_{CC} must remain at or below the V_{LVI} threshold for one t_{CYC} minimum.

In typical applications, the V_{CC} bus filter capacitor will eliminate negative-going voltage glitches of less than one t_{CYC}. The output from the low-voltage detector is connected directly to the internal reset circuitry. It also forces the $\overline{\text{RESET}}$ pin low via a strong discharge device through a resistor. The internal reset is removed once the power supply voltage rises above a recovery level (V_{LVR}) at which time a normal power-on reset occurs.

7.2 INTERNAL CLOCK GENERATOR OPTIONS

The internal clock generator circuit is designed to require a minimum of external components. A crystal, a resistor, a jumper wire, or an external signal may be used to generate a system clock with various stability/cost tradeoffs.

For the MC68705P3 MCU, the EPROM mask option register is programmed to select crystal or resistor operation. For MC6805P2/P4/P6, a manufacturing mask option is used to select crystal or resistor operation.

The different connection methods are shown in Figure 7-4. Crystal specifications and suggested PC board layouts are given in Figure 7-5. A resistor selection graph is given in Figure 7-6.

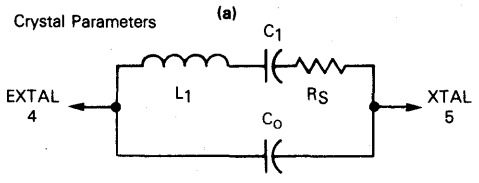
The crystal oscillator start-up time is a function of many variables: crystal parameters (especially R_S, oscillator load capacitances, IC parameters, ambient temperature, and supply voltage). To ensure rapid oscillator start-up, neither the crystal characteristics nor the load capacitances should exceed recommendations.

When utilizing the on-board oscillator, the MCU should remain in a reset condition ($\overline{\text{RESET}}$ pin voltage below V_{IRES+}) until the oscillator has stabilized at its operating frequency. Several factors are involved in calculating current specifications.

Once V_{CC} minimum is reached, the external $\overline{RESET}$ capacitor will begin to charge at a rate dependent on the capacitor value. The charging current is supplied from V_{CC} through a large resistor, so it functions almost like a constant current source until the reset voltages rises above V_{IRES+}. Therefore, the $\overline{RESET}$ pin will charge at approximately:

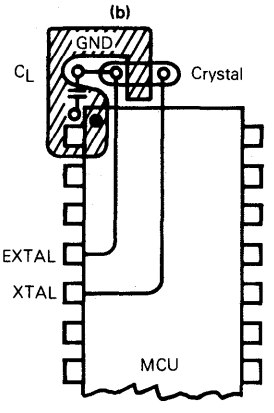
$$(V_{IRES+}) \cdot C_{ext} = I_{RES} \cdot t_{RHL}$$

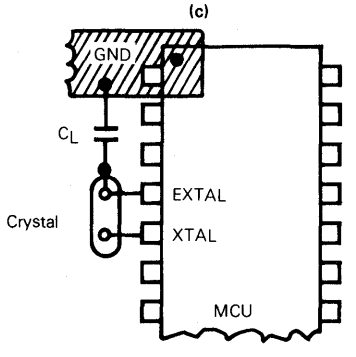
It is assumed that the external capacitor is initially discharged.



AT – Cut Parallel Resonance Crystal
$C_O = 7$ pF Max.
Freq = 4.0 MHz@$C_L = 24$ pF
$R_S = 50$ ohms Max.

Piezoelectric ceramic resonators which have the equivalent specifications may be used instead of crystal oscillators. Follow ceramic resonator manufacturer's suggestions for C_0, C_1, and R_S values.





NOTE: Keep crystal leads and circuit connections as short as possible.

Figure 7-4. Crystal Parameters and Suggested PC Board Layout

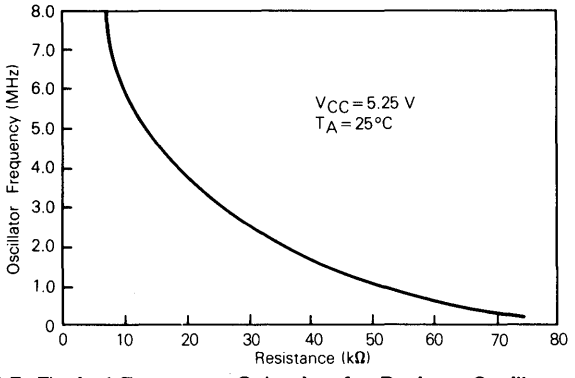


Figure 7-5. Typical Frequency Selection for Resistor Oscillator Option

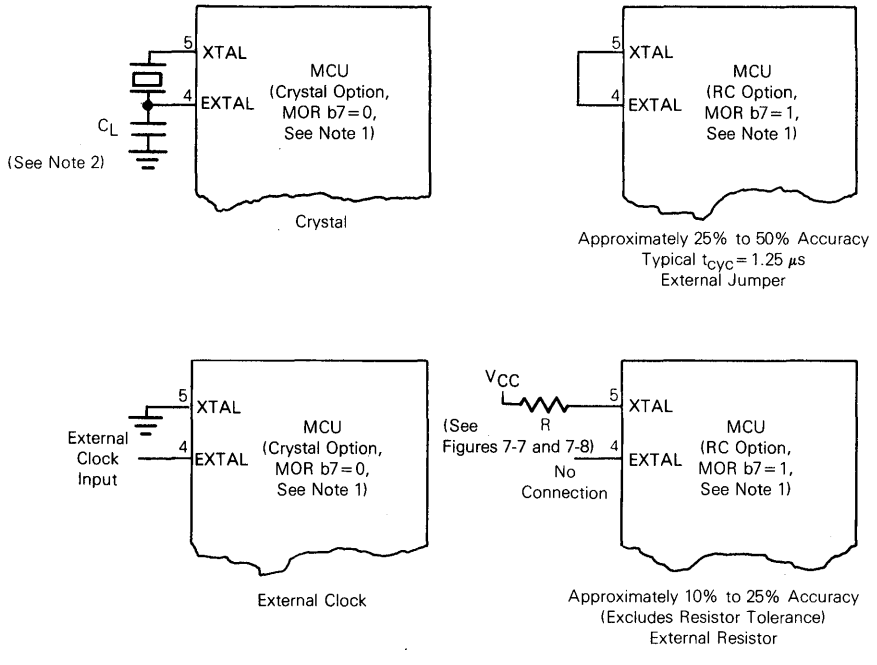


Figure 7-6. Clock Generator Options

NOTES:

1. For the MC68705P3, MOR b7 = 0 for the crystal option and MOR b7 = 1 for the RC option. When the TIMER input pin is in the V_{IHTP} range (in the bootstrap EPROM programming mode), the crystal option is forced. When the TIMER input is at or below V_{CC}, the clock generator option is determined by bit 7 of the mask option register (CLK).
2. The recommended C_L value with a 4.0 MHz crystal is 27 pF maximum including system distributed capacitance. There is an internal capacitance of approximately 25 pF on the XTAL pin. For crystal frequencies other than 4 MHz, the total capacitance on each pin should be scaled as the inverse of the frequence ratio. For example, with a 2 MHz crystal, use approximately 50 pF on EXTAL and approximately 25 pF on XTAL. The exact value depends on the motional-arm parameters of the crystal used.

7.3 INTERRUPTS

The MC68(7)05P series MCUs can be interrupted three different ways: (1) through the external interrupt ($\overline{INT}$) input pin, (2) with the internal timer interrupt request, or (3) using the software interrupt instruction (SWI).

When any interrupt occurs, processing is suspended, the present CPU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. Stacking the CPU registers, setting the I bit, and vector fetching requires a total of 11 t_{CYC} periods for completion.

Flowcharts of the interrupt sequence are shown in Figures 7-7 and 7-8. Figure 7-8 (for MC68705P3) has one more step than Figure 7-7 (for MC6805P2/P4/P6). The EPROM MCU allows options to be loaded from MOR ($784) into the control logic.

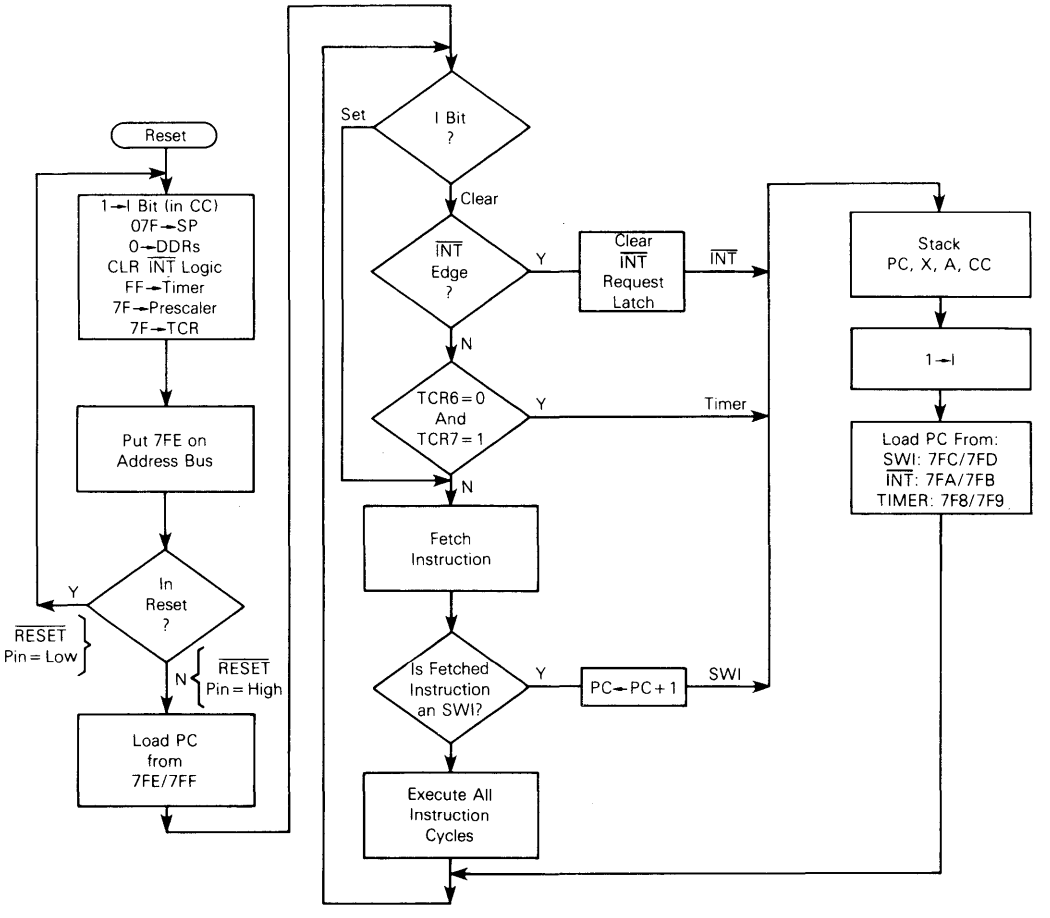


Figure 7-7. Reset and Interrupt Processing Flowchart for MC6805P2/P4/P6

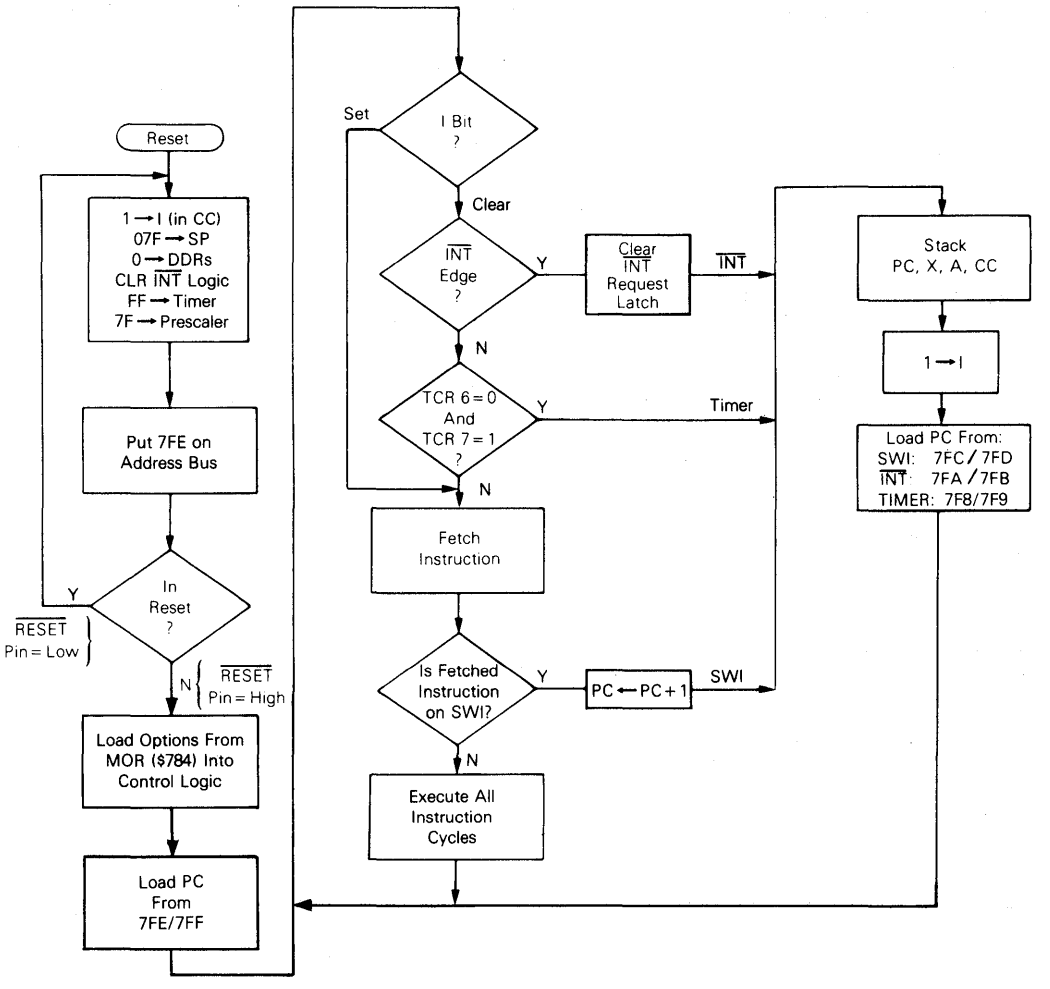


Figure 7-8. Reset and Interrupt Processing Flowchart for MC68705P3

The interrupt service routine must end with a return from the interrupt (RTI) instruction that allows the CPU to resume processing of the program prior to the interrupt (by unstacking the previous CPU state). Unlike reset, hardware interrupts do not cause the current instruction execution to be halted. The instruction is considered pending until the current instruction execution is complete.

When the current instruction is complete, the processor checks all pending hardware interrupts and, if unmasked, proceeds with interrupt processing; otherwise, the next instruction is fetched and executed. Note that masked interrupts are latched for later interrupt service.

If both an external interrupt and a timer interrupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed as any other instruction.

The external interrupt is internally synchronized and then latched on the falling edge of $\overline{INT}$. A sinusoidal input signal (f_{INT} maximum) can be used to generate an external interrupt (see Figure 7-9a) for use as a zero-crossing detector (for negative transitions of the ac sinusoid).

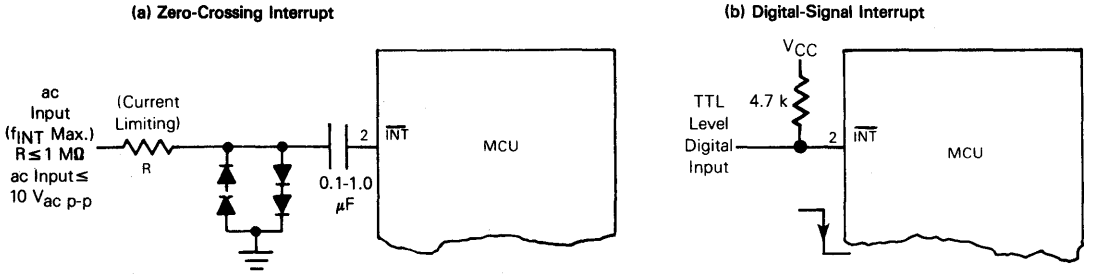


Figure 7-9. Typical Interrupt Circuits

This allows applications such as servicing time-of-day routines and engaging/disengaging ac power control devices. Off-chip, full-wave, rectification provides an interrupt at every zero crossing of the ac signal and thereby provides a 2f clock.

For digital applications, the $\overline{INT}$ pin can be driven by a digital signal. The maximum frequency of a signal that can be recognized by the TIMER or $\overline{INT}$ pin logic is dependent on the parameter labeled t_{WL}, t_{WH}.

The pin logic that recognizes the high (or low) state on the pin must also recognize the low (or high) state on the pin in order to "re-arm" the internal logic. Therefore, the period can be calculated as follows (assuming 50/50 duty cycle for a given period):

$$t_{cyc} \times 2 + 250 \text{ ns} = \text{period} = 1/\text{freq}$$

The period is not simply $t_{WL} = t_{WH}$. This computation is allowable, but it does reduce the maximum allowable frequency by defining an unnecessarily long period (250 ns twice). See Figure 7-9b.

A software interrupt (SWI) is an executable instruction that is executed regardless of the state of the I bit in the condition code register. If the I bit is zero, SWI executes after the other interrupts. SWIs are usually used as breakpoints for debugging or as system calls.

SECTION 8
INPUT/OUTPUT CIRCUITRY

8.1 INPUT/OUTPUT CIRCUITRY

There are 20 input/output pins. The $\overline{INT}$ pin may also be polled with branch instructions to provide an additional input pin. All pins (ports A, B, and C) are programmable as either inputs or outputs under software control of the corresponding write-only data direction register (DDR).

The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic 1 for output or a logic 0 for input. On reset, all the DDRs are initialized to a logic 0 state to put the ports in the input mode. To avoid undefined levels, the port output registers are not initialized on reset, but may be written to before setting the DDR bits.

When programmed as outputs, the latched output data is readable as input data regardless of the logic levels at the output pin due to output loading (see Figure 8-1). Port B has high output sink capability (see the electrical characteristics table in Sections 11.4 through 11.7).

All input/output lines are TTL compatible as both inputs and outputs. Ports B and C are CMOS compatible as inputs. With MC6805P2/P4/P6 MCUs, port A may be made CMOS compatible as outputs with a mask option. Port A of the MC68705P3 MCU is CMOS compatible as outputs.

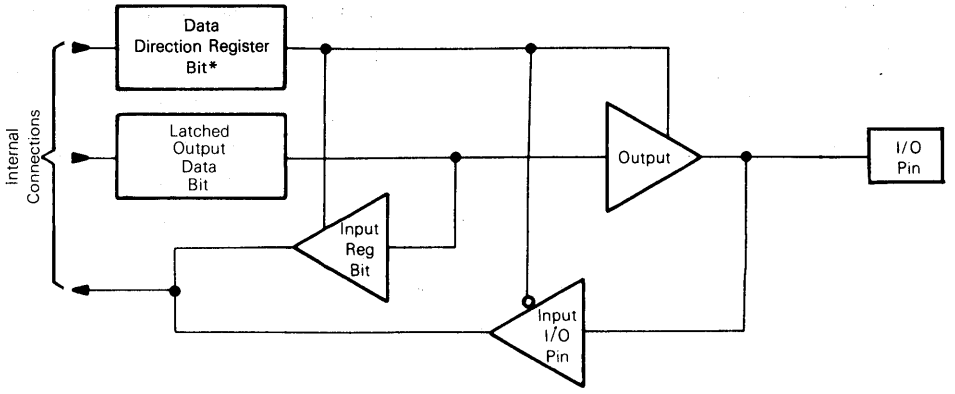
8.2 REGISTER CONFIGURATIONS

The memory maps (see Figures 3-1 — 3-4) give the address of data registers and DDRs. The register configurations shown in Figures 8-2 (for MC6805P2/P4/P6) and 8-3 (for MC68705P3) provide some samples of port connections.

CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, and $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write functions, they cannot be used to set or clear a DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be written using a single-store instruction.

The latched output data bit (see Figure 8-1) may always be written. Therefore, any write to a port writes all of its data bits, even though the port DDR is set to input. This may be used to initialize the data registers and avoid undefined outputs; however, care must be exercised when using read-modify-write instructions since the data read corresponds to the pin level if the DDR is an input (0) and corresponds to the latched output data when the DDR is an output (1).



Data Direction Register Bit	Output Data Bit	Output State	Input To MCU
1	0	0	0
1	1	1	1
0	X	Hi-Z**	Pin

*DDR is a write-only register and reads as all "1s".

**Ports A (with CMOS drive disabled), B, and C are three state ports. Port A has optional internal pullup devices to provide CMOS drive capability. See Electrical Characteristics tables for complete information.

Figure 8-1. Typical Port I/O Circuitry

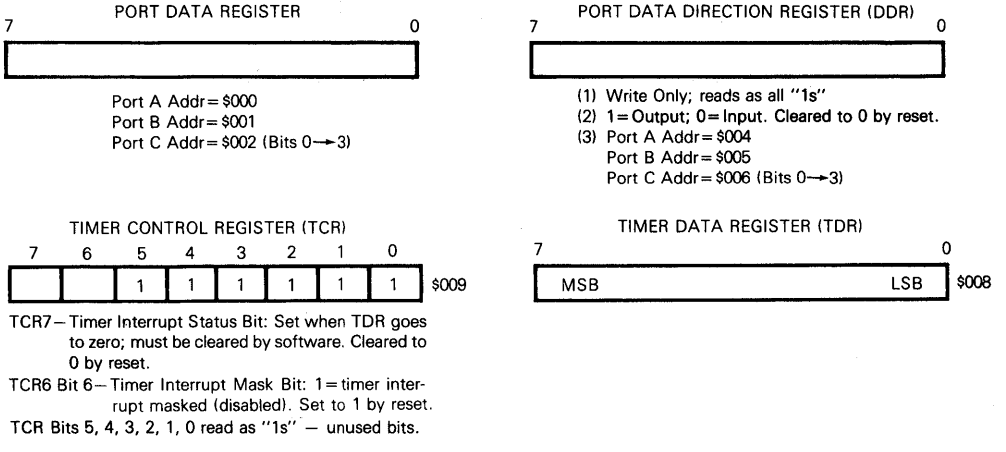


Figure 8-2. MCU Register Configuration for MC6805P2/P4/P6

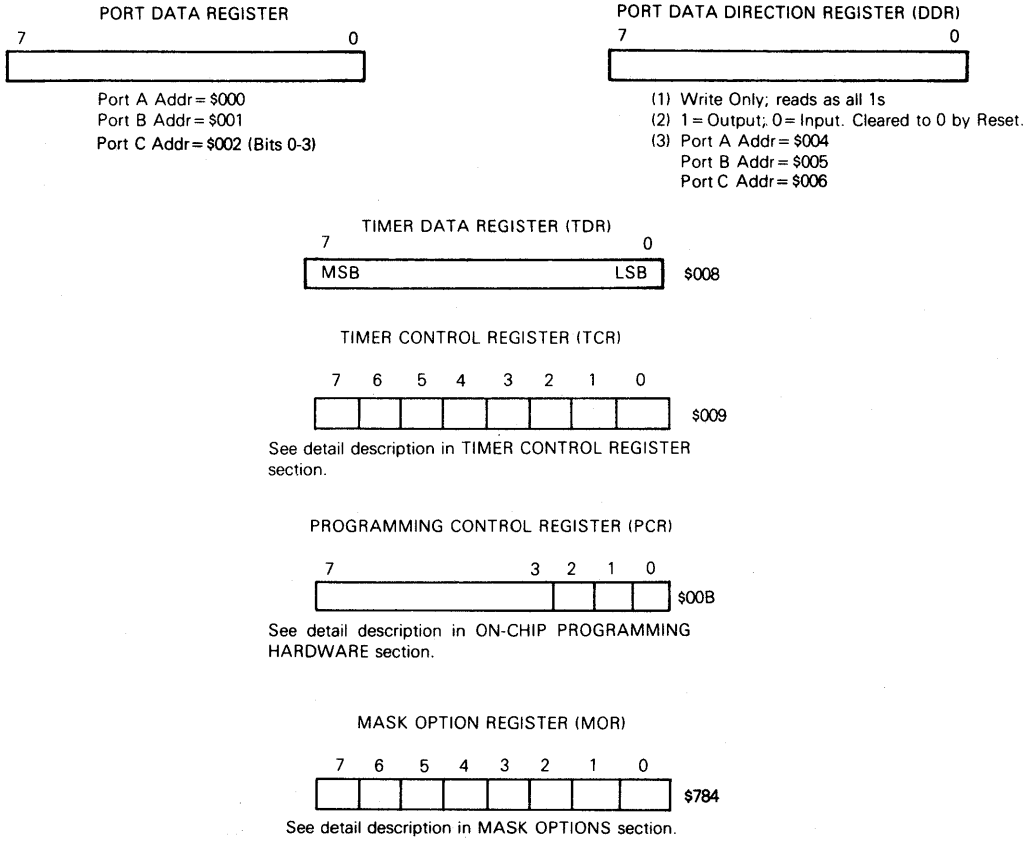
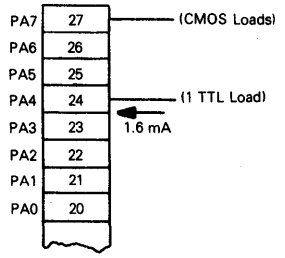
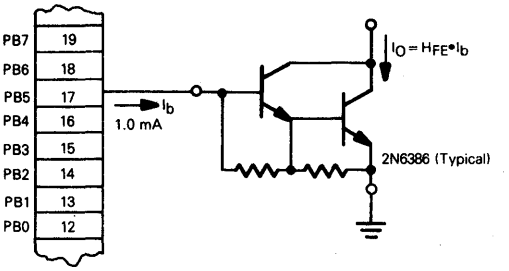


Figure 8-3. MCU Register Configuration for MC68705P3

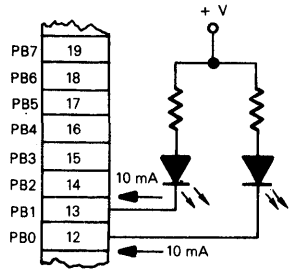
(a) Output Modes



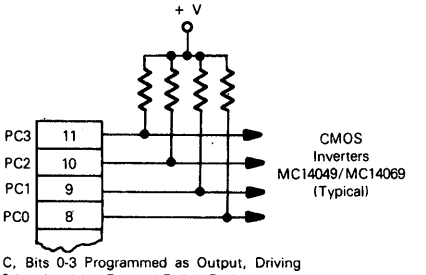
Port A, Bit 7 Programmed as Output, Driving CMOS Loads and Bit 4 Driving one TTL Load Directly (using CMOS output option).



Port B, Bit 5 Programmed as Output, Driving Darlington-Base Directly.

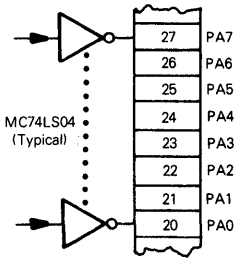


Port B, Bit 0 and Bit 1 Programmed as Output, Driving LEDs Directly.

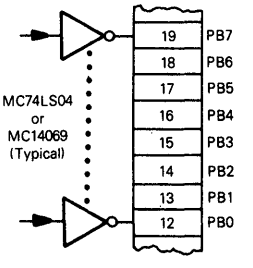


Port C, Bits 0-3 Programmed as Output, Driving CMOS Loads, Using External Pullup Resistors.

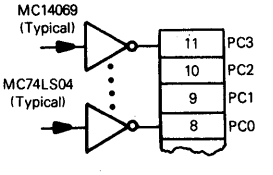
(b) Input Modes



TTL Driving Port A Directly.



CMOS or TTL Driving Port B Directly.



CMOS and TTL Driving Port C Directly.

Figure 8-4. Typical Port Connections

SECTION 9
MASK OPTIONS AND PROGRAMMING

The information in this section pertains only to the MC68705P3 EPROM microcomputer.

9.1 MASK OPTIONS

The MC68705P3 mask option register is implemented in EPROM. Like all other EPROM bytes, the MOR contains all zeros prior to programming (if erased).

When used to emulate the MC6805P2/P4/P6, five of the eight MOR bits are used in conjunction with the prescaler. Of the remaining bits, b7 is used to select the type of oscillator clock and b3 and b4 are not used. Bits b0, b1, and b2 determine the division of the timer prescaler. Bit b5 determines the timer clock source. The value of the TOPT bit (b6) is programmed to configure the TCR (logic 1) for MC6805P2/P4/P6 emulation.

If the MOR timer option (TOPT) bit is a 0, bits b5, b4, b2, b1, and b0 set the initial value of their respective TCR bits during reset. After initialization, the TCR is software controllable.

The MOR bits are described as follows:

b7	b6	b5	b4	b3	b2	b1	b0	Mask Option
CLK	TOPT	CLS	TIE	SNM	P2	P1	P0	Register $784

b7, CLK Clock (oscillator type)
Logic 1 = Resistor Capacitor (RC)
Logic 0 = Crystal

NOTE

V_{IHTP} on the timer pin (7) forces the crystal mode.

b6, TOPT Timer Option
Logic 1 = MC6805P2/P4/P6 type timer/prescaler. All bits except 6 and 7, of the timer control register (TCR) are invisible to the user. Bits 5, 2, 1, and 0 of the mask option register (MOR) determine the equivalent MC6805P2/P4/P6 mask options.
Logic 0 = All TCR bits are implemented as a software programmable timer. The state of MOR bits 5, 4, 2, 1, and 0 sets the initial values of their respective TCR bits (TCR is then software controlled after initialization).

b5, CLS Timer/Prescaler Clock Source
Logic 1 = External timer pin
Logic 0 = Internal $\phi 2$

b4, (TIE) Not used if MOR TOPT = 1 (MC6805P2/P4/P6 emulation). Sets the initial value of TCR TIE if MOR TOPT = 0.

b3 Not used.

b2, P2
b1, P1
b0, P0 Prescaler Option — The logical levels of these bits, when decoded, select one of eight outputs on the timer prescaler. Table 9-1 shows the division resulting from decoding combinations of these three bits.

Two examples for programming the MOR are discussed below.

Example 1 To emulate an MC6805P2 with an RC oscillator and an event count input for the timer with no prescaling, set the MOR at "11111000". To write the MOR, it is programmed the same way as any other EPROM byte.

Example 2 To use the MC68705P3 programmable prescaler functions so that the prescaler is set to be divided by 64, an internal clock source must be used. With the clock oscillator in the crystal mode, set the MOR at "00001110".

Table 9-1. Prescaler Division

P2	P1	P0	Prescaler Division
0	0	0	1 (Bypass Prescaler)
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

9.2 ON-CHIP PROGRAMMING HARDWARE

The programming control register (PCR) at locations $00B is an 8-bit register that utilizes the three LSBs (the five MSBs are set to logic 1). This register provides the necessary control bits for programming the MC68705P3 EPROM. The bootstrap program manipulates the PCR when programming so that users can forget about the PCR in most applications. The description of each bit follows.

b7	b6	b5	64	b3	b2	b1	b0	Program Control
1	1	1	1	1	VPON	PGE	PLE	Register $00B

b0, PLE Programming Latch Enable — When cleared, this bit allows the address and data to be latched into the EPROM. When this bit is set, data can be read from the EPROM. The PLE is set during a reset, but may be cleared anytime. However, its effect on the EPROM is inhibited if VPON is a logic 1.
Logic 1 = Set (read EPROM)
Logic 0 = Clear (latch address and data into EPROM, read disabled)

b1, PGE Program Enable—When cleared, PGE enables programming of the EPROM. PGE can only be cleared if PLE is cleared. PGE must be set when changing the address and data; i.e., when setting up the byte to be programmed. PGE is set during a reset; however, it has no effect on EPROM circuits if VPON is a logic 1.
Logic 1 = Set (inhibit EPROM programming)
Logic 0 = Clear (enable EPROM programming if PLE is low)

b2, VPON V_{PP} ON—This is a read-only bit. When at logic 0, VPON indicates that a "high voltage" is present at the V_{PP} pin. When at logic 1, the PGE and PLE are disconnected from the rest of the chip to prevent accidental clearing of these bits from affecting the normal operating mode.
Logic 1 = No high voltage on V_{PP} pin
Logic 0 = "High voltage" on V_{PP} pin

NOTE

A "0" on VPON does not indicate that the V_{PP} level is correct for programming. It is used as a safety interlock for the user in the normal operating mode.

The programming control register functions are shown in Table 9-2.

Table 9-2. Programming Control Register Functions

VPON	PGE	PLE	Programming Conditions
0	0	0	Programming Mode (Program EPROM Byte)
1	0	0	PGE and PLE Disabled from System
0	1	0	Programming Disabled (Latch Address and Data in EPROM)
1	1	0	PGE and PLE Disabled from System
0	0	1	Invalid State: PGE=0 iff PLE=0
1	0	1	Invalid State: PGE=0 iff PLE=0
0	1	1	"High Voltage" on V_{PP}
1	1	1	PGE and PLE Disabled from System (Operating Mode)

9.3 ERASING THE EPROM

The MC68705P3 EPROM can be erased by exposure to high-intensity ultraviolet (UV) light with a wavelength of 2537 Å. The recommended integrated dose (UV intensity × exposure time) is 25 Ws/cm^2. The lamps should be used without software filters and the MC68705P3 should be positioned about one inch from the UV tubes. Ultraviolet erasure clears all bits of the EPROM to the "0" state. Data can then be entered by programming "1s" into the desired bit locations.

CAUTION

Be sure that the EPROM window is shielded from light except when erasing. This protects both the EPROM and light-sensitive nodes.

9.4 PROGRAMMING FIRMWARE

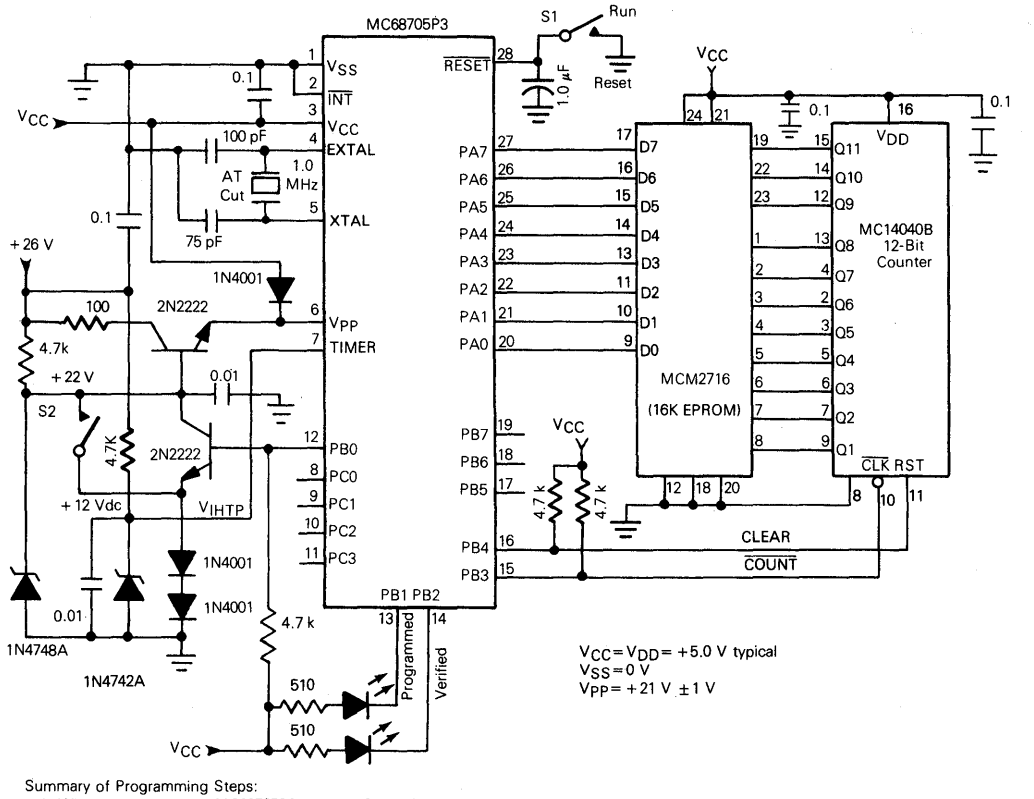
The MC68705P3 has 115 bytes of mask ROM containing a bootstrap program that can be used to program the MC68705P3 EPROM. The vector at address $7F6 and $7F7 is used to start executing the program. This vector is fetched when V_{IHTP} is applied to pin 7 (timer pin) of the MC68705P3 and the $\overline{\text{RESET}}$ pin is allowed to rise above V_{IRES+}. Figure 9-1 is a schematic diagram of a circuit and a summary of programming steps that can be used to program the EPROM in MC68705P3.

9.5 PROGRAMMING STEPS

The MCM2716 UV EPROM must first be programmed with the same information that is to be transferred to the MC68705P3/P5. Non-EPROM addresses are ignored by the bootstrap. Since the MC68705P3/P5 and the MCM2716 are to be inserted and removed from the circuit, they should be mounted in sockets. In addition, the precaution below must be observed (refer to Figure 9-1).

CAUTION

Be sure S1 and S2 are closed and V_{CC} and +26 V are not applied when inserting the MC68705P3 and MCM2716 into their respective sockets. This ensures that $\overline{RESET}$ is held low while inserting the devices.



Summary of Programming Steps:

1. When plugging in the MC68705P3 or the MCM2716, be sure that S1 and S2 are closed and that V_{CC} and +26 V are not applied.
2. To initiate programming, be sure S1 is closed; S2 is closed; and V_{CC} and +26 V are applied. Then open S2, followed by S1.
3. Before removing the MC68705P3, first close S2 and then close S1. Disconnect V_{CC} and +26 V; then remove the MC68705P3.

Figure 9-1. Programming Connections Schematics Diagram

When ready to program the MC68705P3, it is only necessary to (1) provide V_{CC} and +26 V, (2) open the switch S2 to apply V_{PP} and V_{IHTP}, and (3) open S1 to remove reset. Once the voltages are applied and both S2 and S1 are open, the CLEAR output control line (PB4) goes high and then low. The 11-bit counter (MC14040B) is then clocked by the PB3 output (COUNT).

The counter selects the MCM2716 EPROM byte that is to load the equivalent MC68705P3 EPROM byte selected by the bootstrap program. Once the EPROM location is loaded, COUNT clocks the counter to the next EPROM location. This continues until the MC68705P3 is completely programmed, at which time the PROGRAMMED indicator LED lights. The counter is cleared and the loop is repeated to verify the programmed data. The VERIFIED indicator LED lights if the programming is correct.

Once the MC68705P3 has been programmed and verified, close the switch S2 (to remove V_{PP} and V_{IHTP}) and close switch S1 (to reset). Disconnect +26 V and V_{CC} and then remove the MC68705P3 from its socket.

9.6 EMULATION

The MC68705P3 emulates the MC6805P2, P4, and P6 "exactly." The MC6805P2/P4/P6 mask features are implemented in the mask-option register (MOR) EPROM byte on the MC68705P3. There are a few minor exceptions to the exactness of emulation that are listed below.

1. The MC68705P2/P4/P6 "future ROM" area is implemented in the MC68705P3 and these 704 bytes must be left unprogrammed to accurately simulate the MC6805P2/P4/P6. The MC6805P2/P4/P6 read all "0s" from this area.

2. The reserved ROM areas in the MC6805P2/P4/P6 and the MC68705P3 have different data stored in them and this data is subject to change without notice. The MC6805P2/P4/P6 use the reserved ROM for the self-check feature and the MC68705P3 uses this area for the bootstrap program.

3. The MC6805P2/P4/P6 read all "1s" in its 48-byte "future RAM" area. This RAM is not implemented in the MC6805P2/P4/P6 mask ROM versions, but is implemented in the MC68705P3.

4. The V_{PP} line (pin 6) in the MC68705P3 must be tied to V_{CC} for normal operation. In the MC6805P2/P6, pin 6 is the NUM pin and is grounded in normal operation. The MC6805P4 uses pin 6 for V_{SB} that is normally tied to V_{CC} as with the MC68705P3.

5. The LVI feature is not available in the MC68705P3. Processing differences are not presently compatible with proper design of this feature in the EPROM version.

6. The function in the non-user mode is not identical to the MC6805P2/P4/P6 version. Therefore, the MC68705P3 will not function in the MEX6805 support system. In normal operation, all pin functions are the same as the MC6805P2/P4/P6 versions, except for pin 6 as previously noted.

7. The MC6805P4 provides a standby RAM feature that is not available on the MC68705P3.

The operation of all other circuitry has been exactly duplicated or designed to function identically in both devices including interrupts, timer, data ports, and data direction registers (DDRs). A design goal has been to provide the user with a safe, inexpensive way to verify a program and system design before committing to a factory programmed ROM.

SECTION 10
SOFTWARE

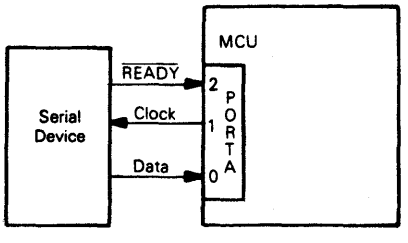
10.1 BIT MANIPULATION

The microcomputers have the ability to set or clear any single RAM or I/O bit (except the data direction registers) with a single instruction ($\overline{\text{BSET}}$, $\overline{\text{BCLR}}$, see **CAUTION** below). Any bit in page zero can be tested using the $\overline{\text{BRSET}}$ and $\overline{\text{BRCLR}}$ instructions and the program branches as a result of its state. The carry bit equals the value of the bit references by $\overline{\text{BRSET}}$ and $\overline{\text{BRCLR}}$. The capability of working with any bit in RAM, ROM, or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines.

CAUTION

The corresponding data direction registers for ports A, B, and C are write-only registers (locations $004, $005, and $006). A read operation on these registers is undefined. Since $\overline{\text{BSET}}$ and $\overline{\text{BCLR}}$ are read-modify-write functions, they cannot be used to set a data direction register bit (all "unaffected" bits would be set). It is recommended that all data direction register bits in a port be written using a single-store instruction.

The coding examples shown in Figure 10-1 illustrate the usefulness of the bit manipulation and test instruction. Assume that the microcomputer is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line to clock data one bit at a time (least significant bit out of the device first). The microcomputer waits until the data is ready, clocks the external device, picks up the data in the carry flag, clears the clock line, and finally accumulates the data bit in a random access memory location.




```
                .
                .
                .
SELF    BRSET   2,PORTA,SELF
                .
                .
                .
        BSET    1,PORTA
        BRCLR   0,PORTA,CONT
CONT    BCLR    1,PORTA
        ROR     RAMLOC
                .
                .
                .
```

Figure 10-1. Bit Manipulation Examples

10.2 ADDRESSING MODES

The microcomputers have ten addressing modes available to use by the programmer. They are explained briefly in the following paragraphs. For additional details and illustrations, refer to the *M6805 HMOS/M146805 CMOS Family Microcomputer/Microprocessor User's Manual.*

The term "effective address" (EA) is used in describing addressing modes. Effective address is defined as the address from which the argument for an instruction is fetched or stored.

10.2.1 Immediate

In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants that do not change during program execution (e.g., a constant used to initialize a loop counter).

10.2.2 Direct

In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single two-byte instruction.

10.2.3 Extended

In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single three-byte instruction. When using the Motorola assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction.

10.2.4 Relative

The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte (the offset) following the opcode is added to the PC if, and only if, the branch conditions are true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from − 126 to + 129 from the opcode address. The programmer need not worry about calculating the correct offset if he uses the Motorola assembler, since it calculates the proper offset and checks to see if it is within the span of the branch.

10.2.5 Indexed, No Offset

In the indexed, no offset, addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

10.2.6 Indexed, 8-Bit Offset

In the indexed, 8-bit offset, addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. The addressing mode is useful for selecting the Kth element in an n element table. With this 2-byte instruction, K would

typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510 ($1FE is the last location at which the instruction may begin).

10.2.7 Indexed, 16-Bit Offset

In the indexed, 16-bit offset, addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset except that this 3-byte instruction allows tables to be anywhere in memory. As with direct and extended, the Motorola assembler determines the shortest form of indexed addressing.

10.2.8 Bit Set/Clear

In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode and the byte following the opcode specifies the direct addressing of the byte, in which the specified bit is to be set or cleared. Thus, any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single 2-byte instruction.

CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, and $006). A read operation on these registers is undefined since $\overline{\text{BSET}}$ and $\overline{\text{BCLR}}$ are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be written using a single-store instruction.

10.2.9 Bit Test and Branch

The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit that is to be tested and its condition (set or clear) is included in the opcode. The address of the byte to be tested is in the single byte immediately following the opcode byte. The signed relative 8-bit offset in the third byte is added to the PC if the specified bit is set or cleared in the specified memory location.

This single 3-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from −125 to +130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code registers. See **CAUTION** in **Section 10.2.8.**

10.2.10 Inherent

In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator as well as the control instruction with no other arguments are included in this mode. These instructions are one byte long.

10.3 INSTRUCTION SET

The MCU has a set of 59 basic instructions which, when combined with the 10 addressing modes, produce 207 usable opcodes. They can be divided into five types: register/memory, read-modify-write, branch, bit manipulation, and control. Each type is explained in the following paragraphs. All the instructions within a given type are presented in individual tables.

10.3.1 Register/Memory Instructions

Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. See Table 10-1.

10.3.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify or test its contents, and then write the modified value back to memory or to the register (see **CAUTION** under **Section 10.2.8**). The test for negative or zero (TST) instructions is included in the read-modify-write instruction although, it does not perform the write. See Table 10-2.

10.3.3 Branch Instructions

The branch instructions cause a branch from the program, when a certain condition is met. Refer to Table 10-3.

10.3.4 Bit Manipulation Instructions

These instructions are used on any bit in the first 256 bytes of memory. See the **CAUTION** in **Section 10.2.8.** One group either sets or clears. The other group performs the bit test and branch operations. See Table 10-4.

10.3.5 Control Instructions

The control instructions control the MCU operations during program execution. See Table 10-6.

10.3.6 Alphabetical Listing

The complete instruction set is given in alphabetical order in Table 10-6.

10.3.7 Opcode Map Summary

Table 10-7 is an opcode map for the instructions used on the MCU.

Table 10-1. Register Memory Instructions

		Addressing Modes																	
		Immediate			Direct			Extended			Indexed (No Offset)			Indexed (8-Bit Offset)			Indexed (16-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Load A from Memory	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6
Load X from Memory	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6
Store A in Memory	STA	–	–	–	B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7
Store X in Memory	STX	–	–	–	BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7
Add Memory to A	ADD	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6
Add Memory and Carry to A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6
Subtract Memory	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6
AND Memory to A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6
OR Memory with A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6
Bit Test Memory with A (Logical Compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6
Jump Unconditional	JMP	–	–	–	BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5
Jump to Subroutine	JSR	–	–	–	BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9

Table 10-2. Read-Modify-Write-Instructions

		Addressing Modes														
		Inherent (A)			Inherent (X)			Direct			Indexed (No Offset)			Indexed (8-Bit Offset)		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
Negate (2's Complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

Table 10-3. Branch Instructions

		Relative Addressing Mode		
Function	Mnemonic	Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
(Branch IFF Higher or Same)	(BHS)	24	2	4
Branch IFF Carry Set	BCS	25	2	4
(Branch IFF Lower)	(BLO)	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF Interrupt Mask Bit is Clear	BMC	2C	2	4
Branch IFF Interrupt Mask Bit is Set	BMS	2D	2	4
Branch IFF Interrupt Line is Low	BIL	2E	2	4
Branch IFF Interrupt Line is High	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

Table 10-4. Bit Manipulation Instructions

		Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
Function	Mnemonic	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF Bit n is Set	BRSET n(n=0. . .7)	–	–	–	2•n	3	10
Branch IFF Bit n is Clear	BRCLR n(n=0. . .7)	–	–	–	01+2•n	3	10
Set Bit n	BSET n(n=0. . .7)	10+2•n	2	7	–	–	–
Clear Bit n	BCLR n(n=0. . .7)	11+2•n	2	7	–	–	–

Table 10-5. Control Instructions

Function	Mnemonic	Inherent		
		Op Code	# Bytes	# Cycles
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-Operation	NOP	9D	1	2

Table 10-6. Instruction Set (Sheet 1 of 2)

	Addressing Modes										Condition Code				
Mnem	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			^	•	^	^	^
ADD		X	X	X		X	X	X			^	•	^	^	^
AND		X	X	X		X	X	X			•	•	^	^	•
ASL	X		X			X	X				•	•	^	^	^
ASR	X		X			X	X				•	•	^	^	^
BCC					X						•	•	•	•	•
BCLR									X		•	•	•	•	•
BCS					X						•	•	•	•	•
BEQ					X						•	•	•	•	•
BHCC					X						•	•	•	•	•
BHCS					X						•	•	•	•	•
BHI					X						•	•	•	•	•
BHS					X						•	•	•	•	•
BIH					X						•	•	•	•	•
BIL					X						•	•	•	•	•
BIT		X	X	X		X	X	X			•	•	^	^	•
BLO					X						•	•	•	•	•
BLS					X						•	•	•	•	•

Condition Code Symbols:

- H Half Carry (From Bit 3)
- I Interrupt Mask
- N Negative (Sign Bit)
- Z Zero
- C Carry/Borrow
- ^ Test and Set if True, Cleared Otherwise
- • Not Affected

Table 10-6. Instruction Set (Sheet 2 of 2)

	Addressing Modes										Condition Code				
Mnem	Inherent	Immediate	Direct	Extended	Relative	Indexed (No Offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/ Clear	Bit Test & Branch	H	I	N	Z	C
BMC					X						•	•	•	•	•
BMI					X						•	•	•	•	•
BMS					X						•	•	•	•	•
BNE					X						•	•	•	•	•
BPL					X						•	•	•	•	•
BRA					X						•	•	•	•	•
BRN					X						•	•	•	•	•
BRCLR										X	•	•	•	•	^
BRSET										X	•	•	•	•	^
BSET									X		•	•	•	•	•
BSR					X						•	•	•	•	•
CLL	X										•	•	•	•	0
CLI	X										•	0	•	•	•
CLR	X		X			X	X				•	•	0	1	•
CMP		X	X	X		X	X	X			•	•	^	^	^
COM	X		X			X	X				•	•	^	^	1
CPX		X	X	X		X	X	X			•	•	^	^	^
DEC	X		X			X	X				•	•	^	^	•
EOR		X	X	X		X	X	X			•	•	^	^	•
INC	X		X			X	X				•	•	^	^	•
JMP			X	X		X	X	X			•	•	•	•	•
JSR			X	X		X	X	X			•	•	•	•	•
LDA		X	X	X		X	X	X			•	•	^	^	•
LDX		X	X	X		X	X	X			•	•	^	^	•
LSL	X		X			X	X				•	•	^	^	^
LSR	X		X			X	X				•	•	0	^	^
NEQ			X			X	X				•	•	^	^	^
NOP	X										•	•	•	•	•
ORA	X	X	X	X		X	X	X			•	•	^	^	•
ROL	X		X			X	X				•	•	^	^	^
RSP	X										•	•	•	•	•
RTI	X										?	?	?	?	?
RTS	X										•	•	•	•	•
SBC		X	X	X		X	X	X			•	•	^	^	^
SEC	X										•	•	•	•	1
SEI	X										•	1	•	•	•
STA			X	X		X	X	X			•	•	^	^	•
STX			X	X		X	X	X			•	•	^	^	•
SUB		X	X	X		X	X	X			•	•	^	^	^
SWI	X										•	1	•	•	•
TAX	X										•	•	•	•	•
TST	X		X			X	X				•	•	^	^	•
TXA	X										•	•	•	•	•

Condition Code Symbols:

- H Half Carry (From Bit 3)
- I Interrupt Mask
- N Negative (Sign Bit)
- Z Zero
- C Carry/Borrow
- ^ Test and Set if True, Cleared Otherwise
- • Not Affected
- ? Load CC Register From Stack

Table 10-7. M6805 HMOS Family Instruction Set Opcode Map (Sheet 1 of 2)

	Bit Manipulation		Branch	Read/Modify/Write				
	BTB	BSC	REL	DIR	A	X	IX1	IX
Hi / Low	0 0000	1 0001	2 0010	3 0011	4 0100	5 0101	6 0110	7 0111
0 0000	10 5 BRSET0 3 BTB	7 5 BSET0 2 BSC	4 3 BRA 2 REL	6 5 NEG 2 DIR	4 3 NEG 1 A	4 3 NEG 1 X	7 6 NEG 2 IX1	6 5 NEG 1 IX
1 0001	10 5 BRCLR0 3 BTB	7 5 BCLR0 2 BSC	4 3 BRN 2 REL					
2 0010	10 5 BRSET1 3 BTB	7 5 BSET1 2 BSC	4 3 BHI 2 REL					
3 0011	10 5 BRCLR1 3 BTB	7 5 BCLR1 2 BSC	4 3 BLS 2 REL	6 5 COM 2 DIR	4 3 COM 1 A	4 3 COM 1 X	7 6 COM 2 IX1	6 5 COM 1 IX
4 0100	10 5 BRSET2 3 BTB	7 5 BSET2 2 BSC	4 3 BCC 2 REL	6 5 LSR 2 DIR	4 3 LSR 1 A	4 3 LSR 1 X	7 6 LSR 2 IX1	6 5 LSR 1 IX
5 0101	10 5 BRCLR2 3 BTB	7 5 BCLR2 2 BSC	4 3 BCS 2 REL					
6 0110	10 5 BRSET3 3 BTB	7 5 BSET3 2 BSC	4 3 BNE 2 REL	6 5 ROR 2 DIR	4 3 ROR 1 A	4 3 ROR 1 X	7 6 ROR 2 IX1	6 5 ROR 1 IX
7 0111	10 5 BRCLR3 3 BTB	7 5 BCLR3 2 BSC	4 3 BEQ 2 REL	6 5 ASR 2 DIR	4 3 ASR 1 A	4 3 ASR 1 X	7 6 ASR 2 IX1	6 5 ASR 1 IX
8 1000	10 5 BRSET4 3 BTB	7 5 BSET4 2 BSC	4 3 BHCC 2 REL	6 5 LSL 2 DIR	4 3 LSL 1 A	4 3 LSL 1 X	7 6 LSL 2 IX1	6 5 LSL 1 IX
9 1001	10 5 BRCLR4 3 BTB	7 5 BCLR4 2 BSC	4 3 BHCS 2 REL	6 5 ROL 2 DIR	4 3 ROL 1 A	4 3 ROL 1 X	7 6 ROL 2 IX1	6 5 ROL 1 IX
A 1010	10 5 BRSET5 3 BTB	7 5 BSET5 2 BSC	4 3 BPL 2 REL	6 5 DEC 2 DIR	4 3 DEC 1 A	4 3 DEC 1 X	7 6 DEC 2 IX1	6 5 DEC 1 IX
B 1011	10 5 BRCLR5 3 BTB	7 5 BCLR5 2 BSC	4 3 BMI 2 REL					
C 1100	10 5 BRSET6 3 BTB	7 5 BSET6 2 BSC	4 3 BMC 2 REL	6 5 INC 2 DIR	4 3 INC 1 A	4 3 INC 1 X	7 6 INC 2 IX1	6 5 INC 1 IX
D 1101	10 5 BRCLR6 3 BTB	7 5 BCLR6 2 BSC	4 3 BMS 2 REL	6 4 TST 2 DIR	4 3 TST 1 A	4 3 TST 1 X	7 5 TST 2 IX1	6 4 TST 1 IX
E 1110	10 7 BRSET7 3 BTB	7 5 BSET7 2 BSC	4 3 BIL 2 REL					
F 1111	10 7 BRCLR7 3 BTB	7 5 BCLR7 2 BSC	4 3 BIH 2 REL	6 5 CLR 2 DIR	4 3 CLR 1 A	4 3 CLR 1 X	7 6 CLR 2 IX1	6 5 CLR 1 IX

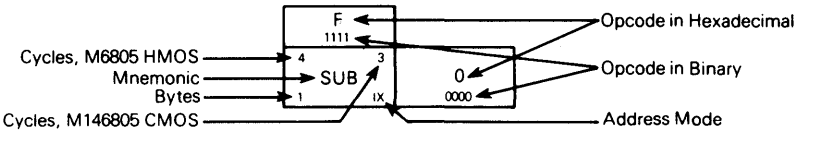
Abbreviations for Address Modes

INH	Inherent	EXT	Extended	IX	Indexed (No Offset)
A	Accumulator	REL	Relative	IX1	Indexed, 1 Byte (8-Bit) Offset
X	Index Register	BSC	Bit Set/Clear	IX2	Indexed, 2 Byte (16-Bit) Offset
IMM	Immediate	BTB	Bit Test and Branch	*	M146805 CMOS Family Only
DIR	Direct				

Table 10-7. M6805 HMOS Family Instruction Set Opcode Map (Sheet 2 of 2)

Control		Register/Memory						
INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
8 1000	9 1001	A 1010	B 1011	C 1100	D 1101	E 1110	F 1111	Hi / Low
9 9 RTI 1 INH		2 2 SUB 2 IMM	4 3 SUB 2 DIR	5 4 SUB 3 EXT	6 5 SUB 3 IX2	5 4 SUB 2 IX1	4 3 SUB 1 IX	0 0000
6 6 RTS 1 INH		2 2 CMP 2 IMM	4 3 CMP 2 DIR	5 4 CMP 3 EXT	6 5 CMP 3 IX2	5 4 CMP 2 IX1	4 3 CMP 1 IX	1 0001
		2 2 SBC 2 IMM	4 3 SBC 2 DIR	5 4 SBC 3 EXT	6 5 SBC 3 IX2	5 4 SBC 2 IX1	4 3 SBC 1 IX	2 0010
11 10 SWI 1 INH		2 2 CPX 2 IMM	4 3 CPX 2 DIR	5 4 CPX 3 EXT	6 5 CPX 3 IX2	5 4 CPX 2 IX1	4 3 CPX 1 IX	3 0011
		2 2 AND 2 IMM	4 3 AND 2 DIR	5 4 AND 3 EXT	6 5 AND 3 IX2	5 4 AND 2 IX1	4 3 AND 1 IX	4 0100
		2 2 BIT 2 IMM	4 3 BIT 2 DIR	5 4 BIT 3 EXT	6 5 BIT 3 IX2	5 4 BIT 2 IX1	4 3 BIT 1 IX	5 0101
		2 2 LDA 2 IMM	4 3 LDA 2 Dir	5 4 LDA 3 EXT	6 5 LDA 3 IX2	5 4 LDA 2 IX1	4 3 LDA 1 IX	6 0110
	2 2 TAX 1 INH		5 4 STA 2 DIR	6 5 STA 3 EXT	7 6 STA 3 IX2	6 5 STA 2 IX1	5 4 STA 1 IX	7 0111
	2 2 CLC 1 INH	2 2 EOR 2 IMM	4 3 EOR 2 DIR	5 4 EOR 3 EXT	6 5 EOR 3 IX2	5 4 EOR 2 IX1	4 3 EOR 1 IX	8 1000
	2 2 SEC 1 INH	2 2 ADC 2 IMM	4 3 ADC 2 DIR	5 4 ADC 3 EXT	6 5 ADC 3 IX2	5 4 ADC 2 IX1	4 3 ADC 1 IX	9 1001
	2 2 CLI 1 INH	2 2 ORA 2 IMM	4 3 ORA 2 DIR	5 4 ORA 3 EXT	6 5 ORA 3 IX2	5 4 ORA 2 IX1	4 3 ORA 1 IX	A 1010
	2 2 SEI 1 INH	2 2 ADD 2 IMM	4 3 ADD 2 DIR	5 4 ADD 3 EXT	6 5 ADD 3 IX2	5 4 ADD 2 IX1	4 3 ADD 1 IX	B 1011
	2 2 RSP 1 INH		3 2 JMP 2 DIR	4 3 JMP 3 EXT	5 4 JMP 3 IX2	4 3 JMP 2 IX1	3 2 JMP 1 IX	C 1100
	2 2 NOP 1 INH	8 6 BSR 2 REL	7 5 JSR 2 DIR	8 6 JSR 3 EXT	9 7 JSR 3 IX2	8 6 JSR 2 IX1	7 5 JSR 1 IX	D 1101
* 2 STOP 1 INH		2 2 LDX 2 IMM	4 3 LDX 2 DIR	5 4 LDX 3 EXT	6 5 LDX 3 IX2	5 4 LDX 2 IX1	4 3 LDX 1 IX	E 1110
* 2 WAIT 1 INH	2 2 TXA 1 INH		5 4 STX 2 DIR	6 5 STX 3 EXT	7 6 STX 3 IX2	6 5 STX 2 IX1	5 4 STX 1 IX	F 1111

LEGEND



SECTION 11
ELECTRICAL CHARACTERISTICS

11.1 MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage			
MC6805P2/P4/P6 (Except TIMER in Self-Check Mode)	V_{in}	−0.3 to +7.0	V
Self-Check Mode (TIMER Pin Only)	V_{in}	−0.3 to +15.0	V
MC68705P3			
EPROM Programming Voltage (V_{PP} Pin)	V_{PP}	−0.3 to +22.0	V
TIMER Pin (Normal Mode)	V_{in}	−0.3 to +7.0	V
TIMER Pin (Bootstrap Programming Mode)	V_{in}	−0.3 to +15.0	V
All Others	V_{in}	−0.3 to +7.0	V
Operating Temperature Range		T_L to T_H	
MC6805P2, P4, and P6, MC68705P3	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−55 to +150	V
Junction Temperature			
Plastic (MC6805P2, P4, and P6 Only)		150	
Ceramic	T_J	175	°C/W
Cerdip		175	

These devices contain circuitry to protect the inputs against damage due to high static voltages or electrical fields; however, normal precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ and $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs except EXTAL are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

11.2. THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance			
Ceramic — MC6805P2, MC6805P4, MC6805P6, MC68705P3		50	
Cerdip — MC6805P2, MC6805P4, MC6805P6, MC68705P3	ϕJA	60	°C/W
Plastic — MC6805P2, MC6805P4, MC6805P6		72	

11.3 POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

T_A ≡ Ambient Temperature, °C

θ_{JA} ≡ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

P_{PORT} ≡ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An appropriate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

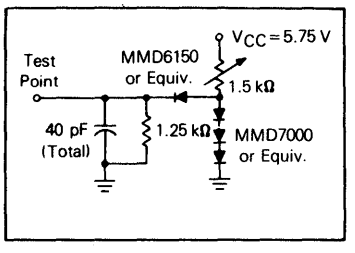


Figure 11-1. TTL Equivalent Test Load (Port B)

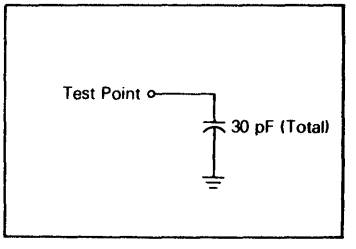


Figure 11-2. CMOS Equivalent Test Load (Port A)

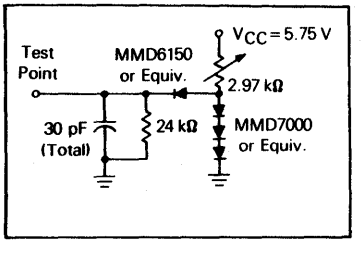


Figure 11-3. TTL Equivalent Test Load (Ports A and C)

11.4 MC6805P2 CHARACTERISTICS

11.4.1 Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage					
$\overline{RESET}$ (4.75 ≤ V_{CC} ≤ 5.75)	V_{IH}	4.0	–	V_{CC}	V
(V_{CC} < 4.75)		V_{CC} – 0.5	–	V_{CC}	
$\overline{INT}$ (4.75 ≤ V_{CC} ≤ 5.75)		4.0	*	V_{CC}	
(V_{CC} < 4.75)		V_{CC} – 0.5	*	V_{CC}	
All Other		2.0	–	V_{CC}	
Input High Voltage Timer					
Timer Mode	V_{IH}	2.0	–	V_{CC} + 1	V
Self-Check Mode		9.0	10.0	15.0	
Input Low Voltage					
$\overline{RESET}$	V_{IL}	V_{SS}	–	0.8	V
$\overline{INT}$		V_{SS}	*	1.5	
All Other		V_{SS}	–	0.8	
$\overline{RESET}$ Hysteresis Voltage (See Figures 10, 11, and 12)					
"Out of Reset"	V_{IRES+}	2.1	–	4.0	V
"Into Reset"	V_{IRES-}	0.8	–	2.0	
$\overline{INT}$ Zero Crossing Input Voltage, Through a Capacitor	V_{INT}	2.0	–	4.0	$V_{ac\ p-p}$
Internal Power Dissipation – No Port Loading V_{CC} = 5.75 V, T_A = 0°C	P_{INT}	–	400	690	mW
Input Capacitance					
XTAL	C_{in}	–	25	–	pF
All Other		–	10	–	
Low Voltage Recover	V_{LVR}	–	–	4.75	V
Low Voltage Inhibit 0°C to 70°C	V_{LVI}	2.75	3.5	–	V
–40°C to 85°C		3.1	3.5	–	
Input Current					
TIMER (V_{in} = 0.4 V)	I_{in}	–	–	20	μA
$\overline{INT}$ (V_{in} = 2.4 V to V_{CC})		–	20	50	
EXTAL (V_{in} = 2.4 V to V_{CC}, Crystal Option)		–	–	10	
(V_{in} = 0.4 V, Crystal Option)		–	–	–1600	
$\overline{RESET}$ (V_{in} = 0.8 V)		–4.0	–	–40	
(External Capacitor Charging Current)					

* Due to internal biasing, this input (when unused) floats to approximately 2.0 Vdc.

11.4.2 Port DC Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A with CMOS Drive Enabled					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = −100 μA	V_{OH}	2.4	–	–	V
Output High Voltage, I_{Load} = −10 μA	V_{OH}	V_{CC}−1	–	–	V
Input High Voltage, I_{Load} = −300 μA (max.)	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltate, I_{Load} = −500 μA (max.)	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 2.0 V to V_{CC})	I_{IH}	–	–	−300	μA
Hi-Z State Input Current (V_{in} = 0.4 V)	I_{IL}	–	–	−500	μA
Port B					
Output Low Voltage, I_{Load} = 3.2 mA	V_{OL}	–	–	0.4	V
Output Low Voltage, I_{Load} = 10 mA (sink)	V_{OL}	–	–	1.0	V
Output High Voltage, I_{Load} = −200 μA	V_{OH}	2.4	–	–	V
Darlington Current Drive (Source), V_O = 1.5 V	I_{OH}	−1.0	–	−10	mA
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	10	μA
Port C and Port A with CMOS Drive Disabled					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = −100 μA	V_{OH}	2.4	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	10	μA

11.4.3 Switching Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0°C to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Oscillator Frequency	MC6805P2	f_{osc}	0.4	–	4.2	MHz
	MC68A05P2		0.4	–	6.0	
	MC68B05P2		0.4	–	8.0	
Cycle Time (4/f_{osc})		t_{cyc}	0.95	–	10	μs
$\overline{INT}$ and TIMER Pulse Width (See Interrupt Section)		t_{WL}, t_{WH}	t_{cyc}+250	–	–	ns
$\overline{RESET}$ Pulse Width		t_{RWL}	t_{cyc}+250	–	–	ns
$\overline{RESET}$ Delay Time (External Capacitance = 1.0 μF)		t_{RHL}	–	100	–	ms
$\overline{INT}$ Zero Crossing Detection Input Frequency		f_{INT}	0.03	–	1.0	kHz
External Clock Input Duty Cycle (EXTAL)		–	40	50	60	%

11.5 MC6805P4 CHARACTERISTICS

11.5.1 Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage					
$\overline{RESET}$ (4.75≤V_{CC}≤5.75)	V_{IH}	4.0	–	V_{CC}	V
(V_{CC}<4.75)		V_{CC}−0.5	–	V_{CC}	
$\overline{INT}$ (4.75≤V_{CC}≤5.75)		4.0	*	V_{CC}	
(V_{CC}<4.75)		V_{CC}−0.5	*	V_{CC}	
All Other		2.0	–	V_{CC}	
Input High Voltage Timer					
Timer Mode	V_{IH}	2.0	–	V_{CC}+1	V
Self-Check Mode		9.0	10.0	15.0	
Input Low Voltage					
$\overline{RESET}$	V_{IL}	V_{SS}	–	0.8	V
$\overline{INT}$		V_{SS}	*	1.5	
All Other		V_{SS}	–	0.8	
$\overline{RESET}$ Hysteresis Voltage (See Figures 10, 11, and 12)					
"Out of Reset"	V_{IRES+}	2.1	–	4.0	V
"Into Reset"	V_{IRES-}	0.8	–	2.0	
$\overline{INT}$ Zero-Crossing Input Voltage, Through a Capacitor	V_{INT}	2.0	–	4.0	$V_{ac\ p-p}$
Internal Power Dissipation—No Port Loading V_{CC}=5.75 V, T_A=0°C	P_{INT}	–	400	TBD	mW
Input Capacitance					
XTAL	C_{in}	–	25	–	pF
All Other		–	10	–	
Low Voltage Recover	V_{LVR}	–	–	4.75	V
Low Voltage Inhibit 0°C to 70°C	V_{LVI}	2.75	3.5	–	V
−40°C to 80°C		3.1	3.5	–	
Input Current					
TIMER (V_{in}=0.4 V)	I_{in}	–	–	20	μA
$\overline{INT}$ (V_{in}=2.4 V to V_{CC})		–	20	50	
EXTAL (V_{in}=0.4 V, Crystal Option)		–	–	10	
_____ (V_{in}=0.4 V, Crystal Option)		–	–	−1600	
$\overline{RESET}$ (V_{in}=0.8 V)		−4.0	–	−40	
(External Capacitor Charging Current)					

* Due to internal biasing, this input (when unused) floats to approximately 2.0 Vdc.

11.5.2 Port DC Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A with CMOS Drive Enabled					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = −100 μA	V_{OH}	2.4	–	–	V
Output High Voltage, I_{Load} = −10 μA	V_{OH}	V_{CC}−1	–	–	V
Input High Voltage, I_{Load} = −300 μA (max)	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, I_{Load} = −500 μA (max)	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 2.0 V to V_{CC})	I_{IH}	–	–	−300	μA
Hi-Z State Input Current (V_{in} = 0.4 V)	I_{IL}	–	–	−500	μA
Port B					
Output Low Voltage, I_{Load} = 3.2 mA	V_{OL}	–	–	0.4	V
Output Low Voltage, I_{Load} = 10 mA (sink)	V_{OL}	–	–	1.0	V
Output High Voltage, I_{Load} = −200 μA	V_{OH}	2.4	–	–	V
Darlington Current Drive (Source), V_O = 1.5 V	I_{OH}	−1.0	–	−10	mA
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	10	μA
Port C and Port A with CMOS Drive Disabled					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = −100 μA	V_{OH}	2.4	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	10	μA
Port B and Port C with Open-Drain Option					
Output High Voltage	V_{OH}	2.4	–	13.0	V
Hi-Z State Input Current	I_{TSI}	–	–	20	μA

11.5.3 Switching Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency	f_{osc}	0.4	–	4.2	MHz
Cycle Time (4/f_{osc})	t_{cyc}	0.95	–	10	μs
$\overline{INT}$ and TIMER Pulse Width (See Interrupt Section)	t_{WL},t_{WH}	t_{cyc} + 250	–	–	ns
$\overline{RESET}$ Pulse Width	t_{RWL}	t_{cyc} + 250	–	–	ns
$\overline{RESET}$ Delay Time (External Capacitance = 1.0 μF)	t_{RHL}	–	100	–	ms
$\overline{INT}$ Zero Crossing Detection Input Frequency	f_{INT}	0.03	–	1.0	kHz
External Clock Input Duty Cycle (EXTAL)	–	40	50	60	%

11.5.4 Standby RAM Characteristics (T_A = 0° to 70°C)

Characteristic	Symbol	Min	Typ	Max	Unit
Standby Current					
8 Bytes	I_{SB}	–	1.0	TBD	mA
32 Bytes		–	2.2	TBD	
64 Bytes		–	3.4	TBD	
112 Bytes		–	5.2	TBD	
RAM Standby Voltage	V_{SB}	3.0	5.25	5.75	V
V_{CC} Turn-off Rate	V_{CCTO}	–	–	1/100	V/μs

11.6 MC6805P6 CHARACTERISTICS

11.6.1 Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage					
$\overline{RESET}$ (4.75≤V_{CC}≤5.75)	V_{IH}	4.0	–	V_{CC}	V
(V_{CC}<4.75)		V_{CC}−0.5	–	V_{CC}	
$\overline{INT}$ (4.75≤V_{CC}≤5.75)		4.0	*	V_{CC}	
(V_{CC}<4.75)		V_{CC}−0.5	*	V_{CC}	
All Other		2.0	–	V_{CC}	
Input High Voltage Timer					
Timer Mode	V_{IH}	2.0	–	V_{CC}+1	V
Self-Check Mode		9.0	10.0	15.0	
Input Low Voltage					
$\overline{INT}$	V_{IL}	V_{SS}	*	1.5	V
All Other		V_{SS}	–	0.8	
$\overline{RESET}$ Hysteresis Voltage (See Figures 10, 11, and 12)					
"Out of Reset"	V_{IRES+}	2.1	–	4.0	V
"Into Reset"	V_{IRES-}	0.8	–	2.0	
$\overline{INT}$ Zero Crossing Input Voltage, Through a Capacitor	V_{INT}	2.0	–	4.0	$V_{ac\ p\text{-}p}$
Internal Power Dissipation – No Port Loading V_{CC}=5.75 V, T_A=0°C	P_{INT}	–	400	690	mW
Input Capacitance					
XTAL	C_{in}	–	25	–	pF
All Other		–	10	–	
Low Voltage Recover	V_{LVR}	–	–	4.75	V
Low Voltage Inhibit 0°C to 70°C	V_{LVI}	2.75	3.5	–	V
−40°C to 85°C		3.1	3.5	–	
Input Current (External Capacitor Charging Current)					
TIMER (V_{in}=0.4 V)	I_{in}	–	–	20	μA
$\overline{INT}$ (V_{in}=2.4 V to V_{CC})		–	20	50	
EXTAL (V_{in}=2.4 V to V_{CC}, Crystal Option)		–	–	10	
(V_{in}=0.4 V, Crystal Option)		–	–	−1600	
$\overline{RESET}$ (V_{in}=0.8 V)		−4.0	–	−40	

*Due to internal biasing, this input (when unused) floats to approximately 2.0 Vdc.

11.6.2 Port DC Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A with CMOS Drive Enabled					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = – 100 μA	V_{OH}	2.4	–	–	V
Output High Voltage, I_{Load} = – 10 μA	V_{OH}	V_{CC} – 1	–	–	V
Input High Voltage, I_{Load} = – 300 μA (max.)	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage, I_{Load} = – 500 μA (max.)	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 2.0 V to V_{CC})	I_{IH}	–	–	– 300	μA
Hi-Z State Input Current (V_{in} = 0.4 V)	I_{IL}	–	–	– 500	μA
Port B					
Output Low Voltage, I_{Load} = 3.2 mA	V_{OL}	–	–	0.4	V
Output Low Voltage, I_{Load} = 10 mA (sink)	V_{OL}	–	–	1.0	V
Output High Voltage, I_{Load} = – 200 μA	V_{OH}	2.4	–	–	V
Darlington Current Drive (Source), V_O = 1.5 V	I_{OH}	– 1.0	–	– 10	mA
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	10	μA
Port C and Port A with CMOS Drive Disabled					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = – 100 μA	V_{OH}	2.4	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	10	μA
Port B with Open-Drain Option					
Output High Voltage	V_{OH}	2.4	–	13.0	V
Hi-Z State Input Current	I_{TSI}	–	2	20	μA

11.6.3 Switching Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency MC6805P6	f_{osc}	0.4	–	4.2	MHz
MC68A05P6		0.4	–	6.0	
MC68B05P6		0.4	–	8.0	
Cycle Time ($4/f_{osc}$)	t_{cyc}	0.95	–	10	μs
$\overline{INT}$ and TIMER Pulse Width (See INTERRUPTS)	t_{WL},t_{WH}	t_{cyc} + 250	–	–	ns
$\overline{RESET}$ Pulse Width	t_{RWL}	t_{cyc} + 250	–	–	ns
$\overline{RESET}$ Delay Time (External Capacitance = 1.0 μF)	t_{RHL}	–	100	–	ms
$\overline{INT}$ Zero Crossing Detection Input Frequency	f_{INT}	0.03	–	1.0	kHz
External Clock Input Duty Cycle (EXTAL)	–	40	50	60	%

11.7 MC68705P3 CHARACTERISTICS

11.7.1 Programming Operation Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 20° to 30°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage (V_{PP} Pin)	V_{PP}	20.0	21.0	22.0	V
V_{PP} Supply Current V_{PP} = 5.25 V V_{PP} = 21.0 V	I_{PP}	– –	– –	8 30	mA
Programming Oscillator Frequency	f_{oscp}	0.9	1.0	1.1	MHz
Bootstrap Programming Mode Voltage (TIMER Pin) I_{in} = 100 µA Max	V_{IHTP}	9.0	12.0	15.0	V

11.7.2 Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage $\overline{RESET}$ (4.75 ≤ V_{CC} ≤ 5.75) (V_{CC} < 4.75) $\overline{INT}$ (4.75 ≤ V_{CC} ≤ 5.75) (V_{CC} < 4.75) All Other	V_{IH}	4.0 V_{CC} – 0.5 4.0 V_{CC} – 0.5 2.0	– – ** ** –	V_{CC} V_{CC} V_{CC} V_{CC} V_{CC}	V
Input High Voltage (TIMER Pin) Timer Mode Bootstrap Programming Mode	V_{IH}	2.0 9.0	– 12.0	V_{CC} 15.0	V
Input Low Voltage $\overline{RESET}$ $\overline{INT}$ All Other	V_{IL}	–0.3 –0.3 –0.3	– ** –	0.8 1.5 0.8	V
Internal Power Dissipation (No Port Loading, V_{CC} = 5.25 V, T_A = 0°C)	P_{INT}	–	450	TBD	mW
Input Capacitance XTAL All Other	C_{in}	– –	25 10	– –	pF
$\overline{INT}$ Zero-Crossing Voltage, through a Capacitor	V_{INT}	2.0	–	4.0	V_{acp-p}
$\overline{RESET}$ Hysteresis Voltage (See Figure 11) Out of Reset Voltage Into Reset Voltage	V_{IRES+} V_{IRES-}	2.1 0.8	– –	4.0 2.0	V
Programming Voltage (V_{PP} Pin) Programming EPROM Operating Mode	V_{PP}*	20.0 4.0	21.0 V_{CC}	22.0 5.75	V
Input Current TIMER (V_{in} = 0.4 V) $\overline{INT}$ (V_{in} = 0.4 V) EXTAL (V_{in} = 2.4 V to V_{CC} Crystal Option) (V_{in} = 0.4 V Crystal Option) $\overline{RESET}$ (V_{in} = 0.8 V) (External Capacitor Changing Current)	I_{in}	– – – – –4.0	– 20 – – –	20 50 10 –1600 –40	µA

*V_{PP} is Pin 6 on the MC68705P3 and is connected to V_{CC} in the Normal Operating Mode. In the MC6805P2, Pin 6 is NUM and is connected to V_{SS} in the Normal Operating Mode. The user must allow for this difference when emulating the MC6805P2 ROM-based MCU.

**Due to internal biasing, this input (when not used) floats to approximately 2.0 V.

11.7.3 Port DC Electrical Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Port A					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = −100 μA	V_{OH}	2.4	–	–	V
Output High Voltage, I_{Load} = −10 μA	V_{OH}	V_{CC}−1.0	–	–	V
Input High Voltage, I_{Load} = −300 μA (Max)	V_{IH}	2.0	–	V_{CC}+0.7	V
Input Low Voltage, I_{Load} = −500 μA (Max)	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current (V_{in} = 2.0 V to V_{CC})	I_{IH}	–	–	−300	μA
Hi-Z State Input Current (V_{in} = 0.4 V)	I_{IL}	–	–	−500	μA
Port B					
Output Low Voltage, I_{Load} = 3.2 mA	V_{OL}	–	–	0.4	V
Output Low Voltage, I_{Load} = 10 mA (Sink)	V_{OL}	–	–	1.0	V
Output High Voltage, I_{Load} = −200 μA	V_{OH}	2.4	–	–	V
Darlington Current Drive (Source), V_O = 1.5 V	I_{OH}	−1.0	–	−10	mA
Input High Voltage	V_{IH}	2.0	–	V_{CC}+0.7	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	20	μA
Port C					
Output Low Voltage, I_{Load} = 1.6 mA	V_{OL}	–	–	0.4	V
Output High Voltage, I_{Load} = −100 μA	V_{OH}	2.4	–	–	V
Input High Voltage	V_{IH}	2.0	–	V_{CC}+0.7	V
Input Low Voltage	V_{IL}	V_{SS}	–	0.8	V
Hi-Z State Input Current	I_{TSI}	–	2	20	μA

11.7.4 Switching Characteristics

(V_{CC} = +5.25 ±0.5 Vdc, V_{SS} = 0 Vdc, T_A = 0° to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Oscillator Frequency Normal	f_{osc}	0.4	–	4.2	MHz
Instruction Cycle Time ($4/f_{osc}$)	t_{cyc}	0.950	–	10	μs
$\overline{INT}$ or Timer Pulse Width (See Interrupt Section)	t_{WL}, t_{WH}	t_{cyc}+250	–	–	ns
$\overline{RESET}$ Pulse Width	t_{RWL}	t_{cyc}+250	–	–	ns
$\overline{RESET}$ Delay Time (External Cap = 1.0 μF)	t_{RHL}	100	–	–	ms
$\overline{INT}$ Zero Crossing Detection Input Frequency	f_{INT}	0.03	–	1.0	kHz
External Clock Duty Cycle (EXTAL) (See Figure 12)	–	40	50	60	%

11.8 I/O CHARACTERISTICS

Figures 11-4 through 11-14 illustrate I/O characteristic data for HMOS M6805 Family devices. Simplified port logic diagrams are shown in Figures 11-15 and 11-16, typical input protection in Figure 11-17, and an I/O characteristic measurement circuit in Figure 11-18. The I/O characteristic curves and logic diagrams are intended to allow the system designer to interface the M6805 in a variety of applications where non-TTL loading conditions exist.

A minimum specification curve (included with V_{OH} vs I_{OH} charts only) is provided as a guaranteed limit of performance under the conditions shown. The expected minimum and maximum curves in each figure represent the anticipated performance window under normal manufacturing and operating conditions. A typical curve also is illustrated indicating performance under nominal conditions.

Figure 11-14 represents the variation of I_{DD} with temperature and V_{DD} for a typical M6805 Family device. As shown I_{DD} varies directly with V_{DD} and inversely with temperature.

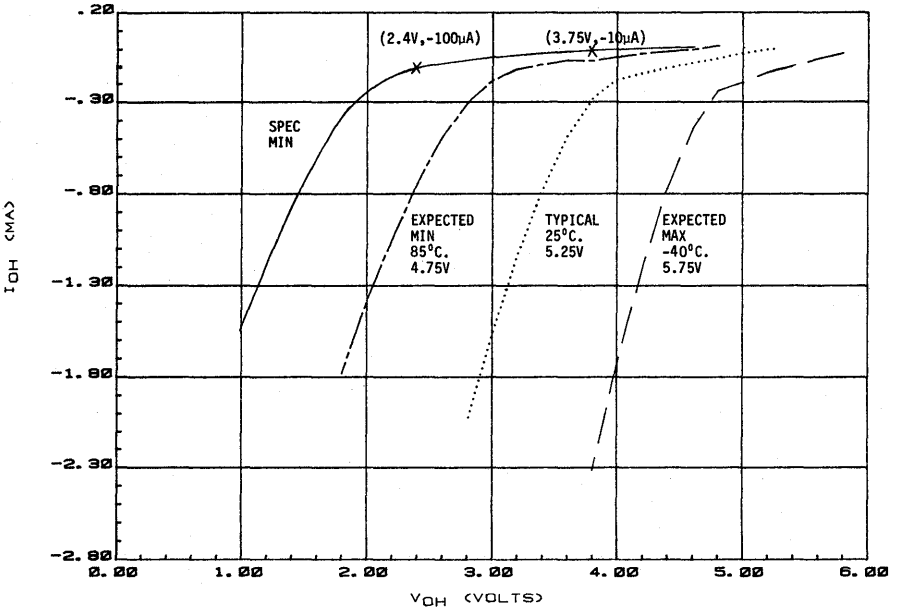


Figure 11-4. Port A V_{OH} vs I_{OH} (With CMOS Pull-Ups)

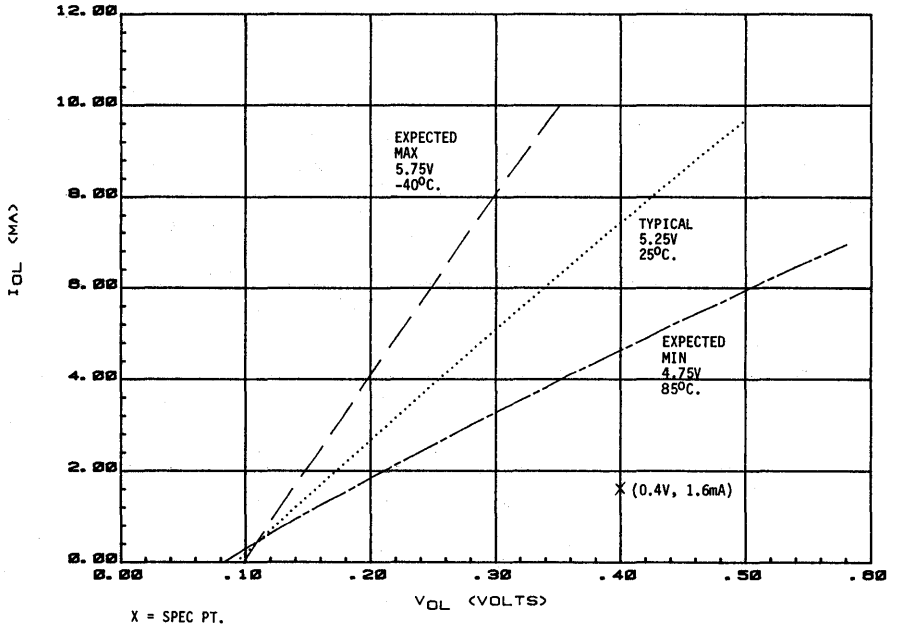


Figure 11-5. Port A V_{OL} vs I_{OL} (With CMOS Pull-Ups)

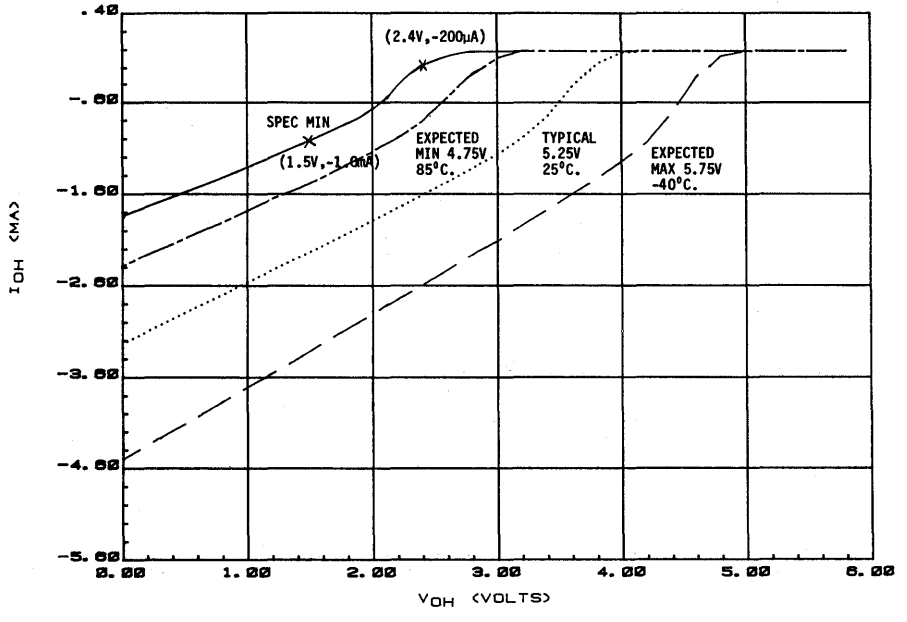


Figure 11-6. Port B V_{OH} vs I_{OH}

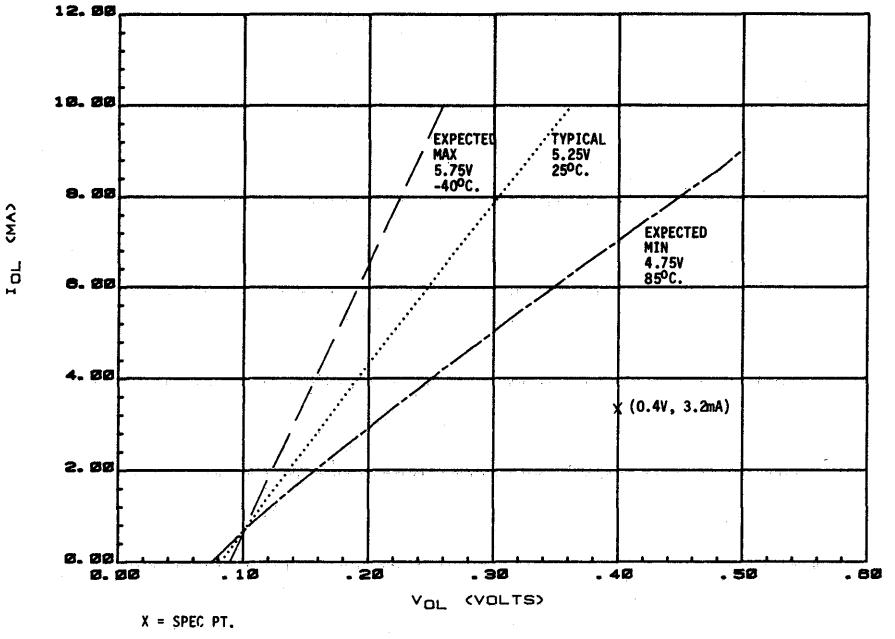


Figure 11-7. Port B V_{OL} vs I_{OL}

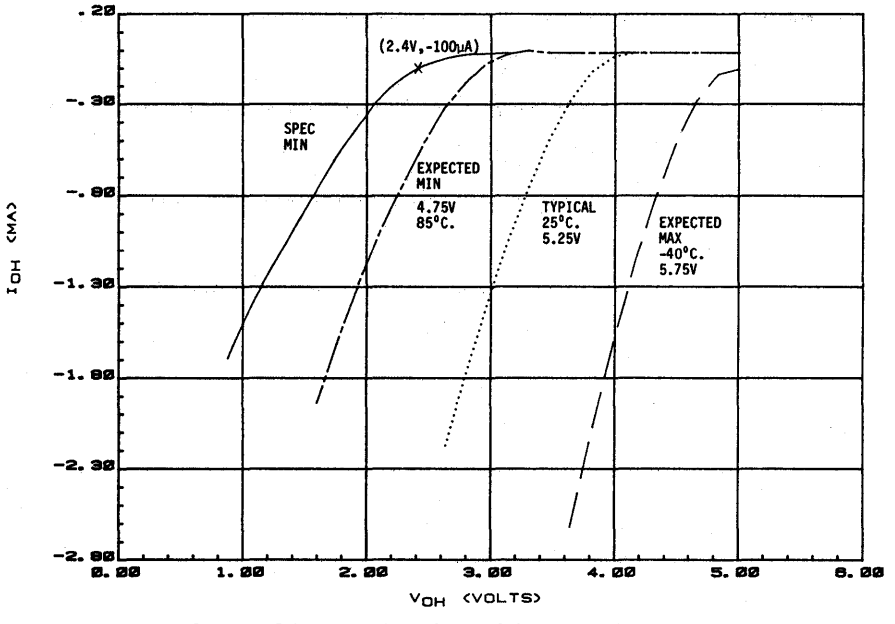


Figure 11-8. Port C V_{OH} vs I_{OH} (Port A Without CMOS Pull-Up)

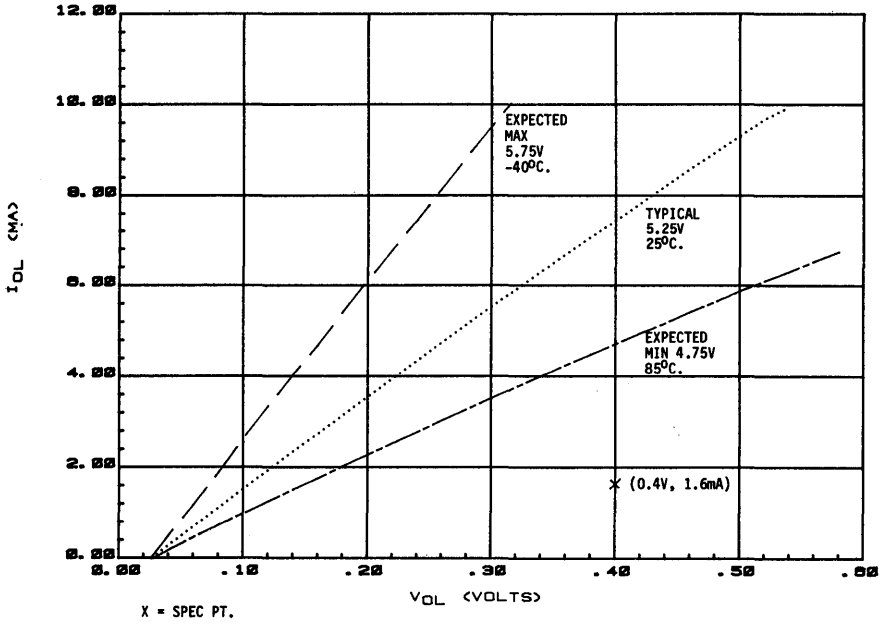


Figure 11-9. Port C V_{OL} vs I_{OL} (Port A Without CMOS Pull-Ups)

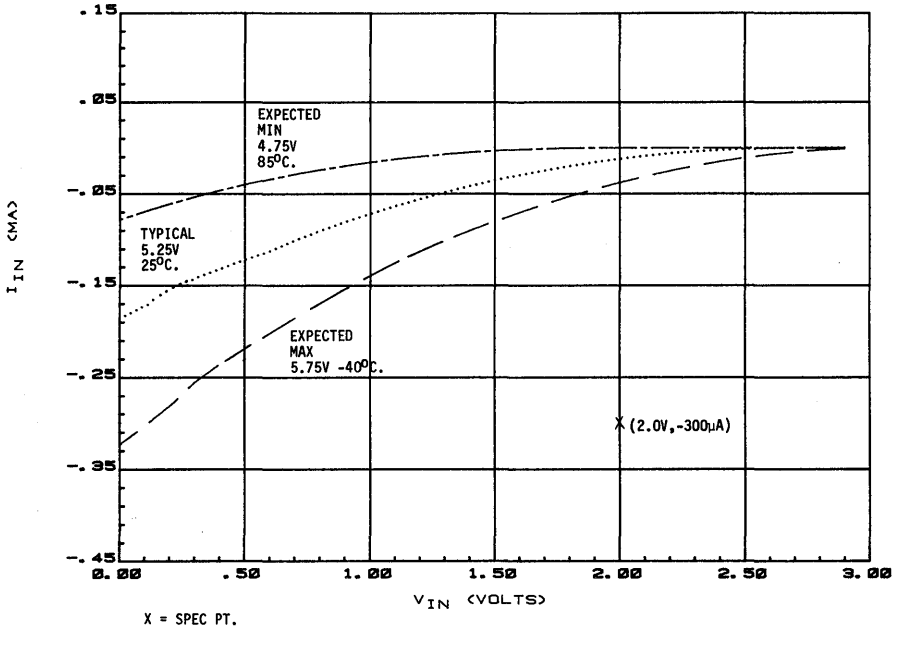


Figure 11-10. Port A V_{in} vs I_{in} (With CMOS Pull-Ups)

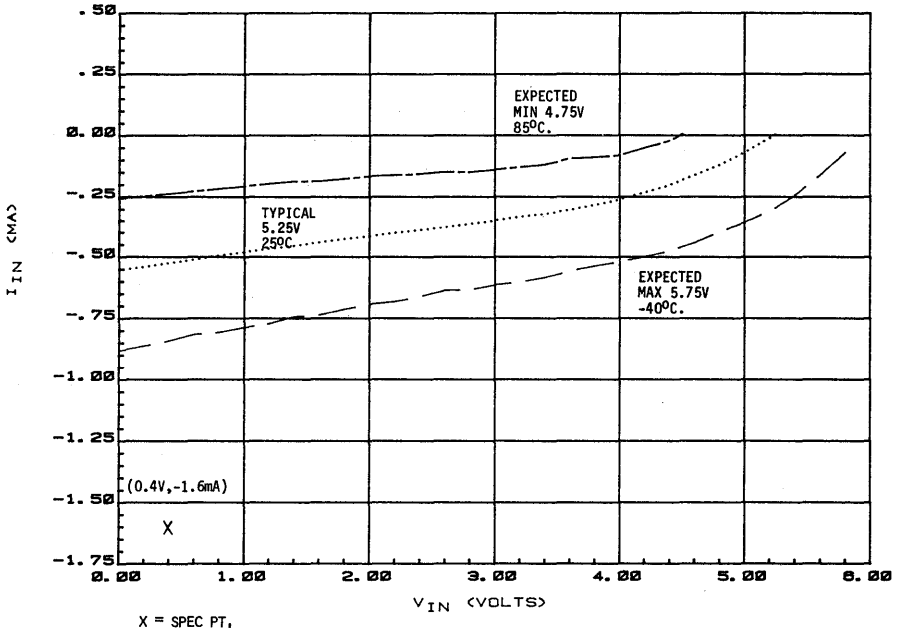


Figure 11-11. EXTAL V_{in} vs I_{in}

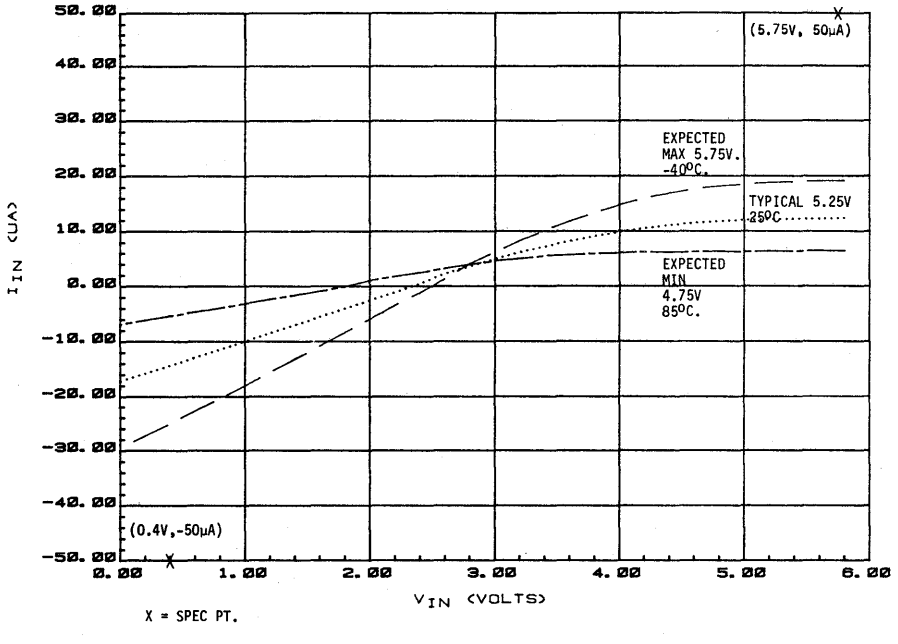


Figure 11-12. Interrupt V_{in} vs I_{in}

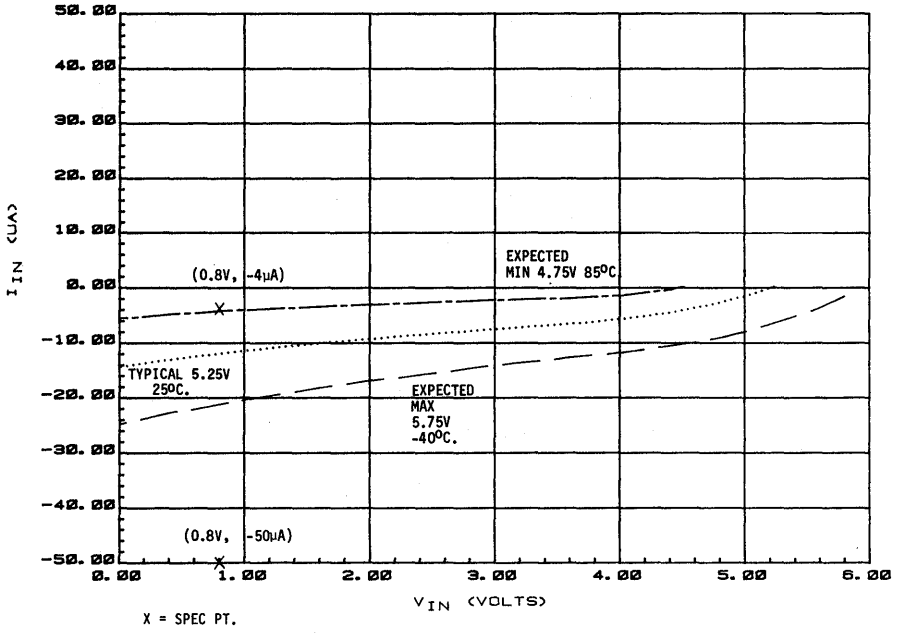


Figure 11-13. $\overline{\text{RESET}}$ V_{in} vs V_{in}

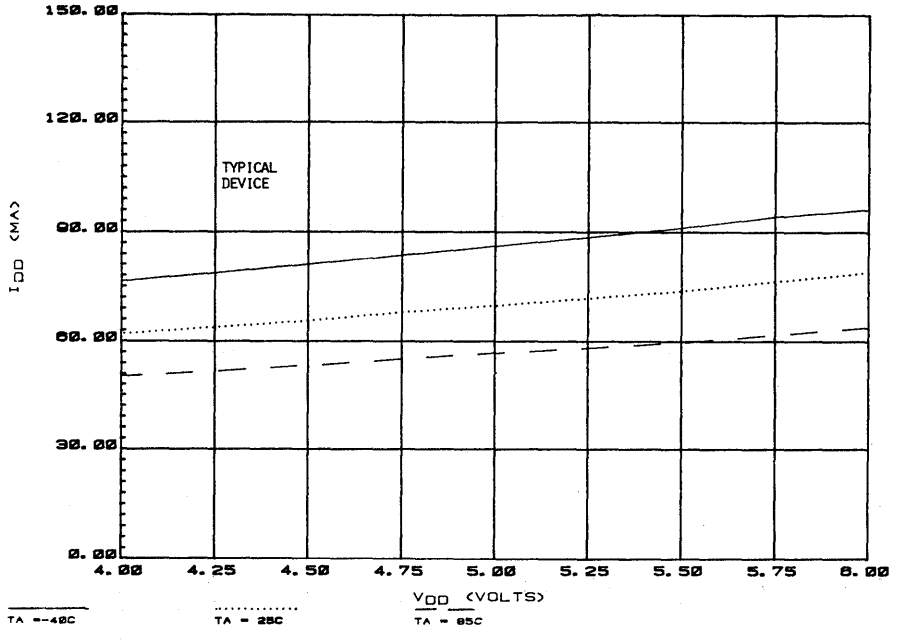


Figure 11-14. V_{DD} vs I_{DD} (Variation with Temperature)

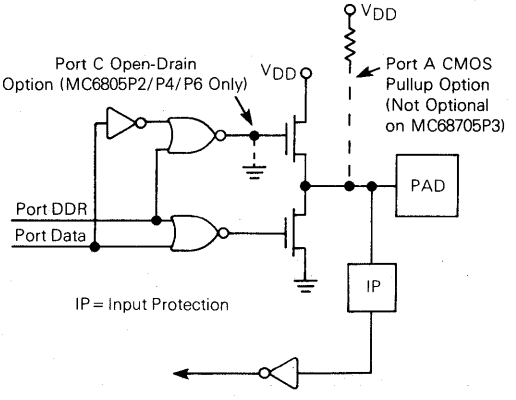


Figure 11-15. Ports A and C Logic Diagram

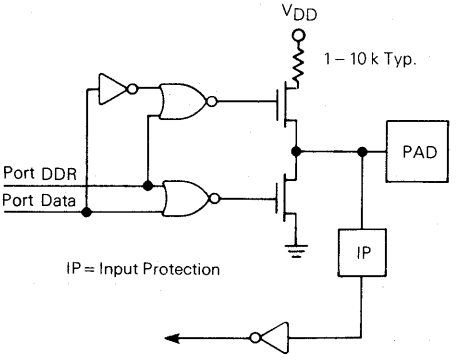


Figure 11-16. Port B Logic Diagram

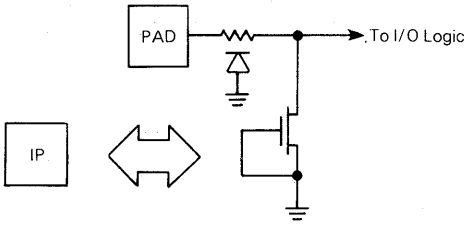


Figure 11-17. Typical Input Protection

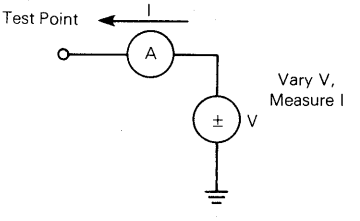


Figure 11-18. I/O Characteristic Measurement Circuit

SECTION 12
ORDERING INFORMATION

This section contains detailed information to be used as a guide when ordering an MC68(7)05P series device.

12.1 MC6805P2

Package Type	Internal Clock Frequency (MHz)	Temperature	Generic Number
Ceramic (L Suffix)	1.0	0° to 70°C	MC6805P2L
	1.5	0° to 70°C	MC68A05P2L
	2.0	0° to 70°C	MC68B05P2L
Plastic (P Suffix)	1.0	0° to 70°C	MC6805P2P
	1.5	0° to 70°C	MC68A05P2P
	2.0	0° to 70°C	MC68B05P2P
Cerdip (S Suffix)	1.0	0° to 70°C	MC6805P2S
	1.5	0° to 70°C	MC68A05P2S
	2.0	0° to 70°C	MC68B05P2S

12.2 MC6805P4

Package Type	Internal Clock Frequency (MHz)	Temperature	Generic Number
Ceramic (L Suffix)	1.0	0° to 70°C	MC6805P4L
Plastic (P Suffix)	1.0	0° to 70°C	MC6805P4P
Cerdip (S Suffix)	1.0	0° to 70°C	MC6805P4S

12.3 MC6805P6

Package Type	Internal Clock Frequency (MHz)	Temperature	Generic Number
Ceramic (L Suffix)	1.0	0° to 70°C	MC6805P6L
	1.5	0° to 70°C	MC68A05P6L
	2.0	0° to 70°C	MC68B05P6L
Plastic (P Suffix)	1.0	0° to 70°C	MC6805P6P
	1.5	0° to 70°C	MC68A05P6P
	2.0	0° to 70°C	MC68B05P6P
Cerdip (S Suffix)	1.0	0° to 70°C	MC6805P6S
	1.5	0° to 70°C	MC68A05P6S
	2.0	0° to 70°C	MC68B05P6S

12.4 MC68705P3

Package Type	Internal Clock Frequency (MHz)	Temperature	Generic Number
Ceramic (L Suffix)	1.0	0° to 70°C	MC68705P3L
Cerdip (S Suffix)	1.0	0° to 70°C	MC68705P3S

12.5 CUSTOM MCUs

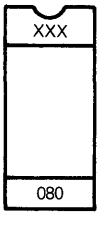
The information required when ordering a custom MCU is listed below. The ROM program may be transmitted to Motorola on EPROM(s) or an MDOS disk file.

To initiate a ROM pattern for the MCU, first contact your local Motorola representative or Motorola distributor.

12.5.1 EPROMs

The MC68705P3 EPROM MCUs programmed with the customer program may be used to submit the ROM pattern for the MC6805P2 and MC6805P6 devices. Note that the MC6805P2 has 1100 bytes of ROM, the MC6805P6 has 1796 bytes of ROM, while the MC68705P3 has 1804 bytes of EPROM.

The MCM2716 or MCM2532 type EPROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The EPROM must be clearly marked to indicate which EPROM corresponds to which address space. The recommended marking procedure is illustrated in Figure 12-1.



XXX = Customer ID

Figure 12-1. Recommended Marking Procedure

After the EPROM(s) are marked, they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

12.5.2 Verification Media

All original pattern media (EPROMs or floppy disks) are filed for contractural purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to Motorola.

The signed verification form constitutes the contractual agreement for creation of the customer mask. If desired, Motorola will program one blank EPROM from the data file used to create the custom mask to aid in the verification process.

12.5.3 ROM Verification Units (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units are made using the custom mask but are for the purpose of ROM verification only. For expediency, they are usually unmarked, packaged in ceramic, and tested only at room temperature and 5 volts. These RVUs are included in the mask charge and are not production parts. Therefore, the RVUs are not guaranteed by Motorola Quality Assurance and should be discarded after verification is complete.

12.5.4 Flexible Disk

The disk media submitted must be single-sided, single-density, 8-inch MDOS compatible floppies. The customer must write the binary file name and company name of the disk with a felt-tip pen. The minimum MDOS system files as well as the absolute binary object file (filename .LO type of file) from the M6805 cross assembly must be on the disk. An object file made from a memory dump using the ROLLOUT command is also acceptable.

Consider submitting a source listing as well as the following files: filename .LX (EXORciser loadable format) and filename .SA (ASCII source code). These files will of course be kept confidential and are used (1) to speed up the process in-house if any problems arise and (2) to speed up the user-to-factory interface if the user finds any software errors and needs assistance quickly from Motorola factory representative.

MDOS is Motorola's Disk Operating System available on the EXORciser development system.

MDOS is a trademark of Motorola Inc.
EXORciser is a registered trademark of Motorola Inc.

MC6805P2 MCU CUSTOM ORDERING INFORMATION

Date _____ Customer PO Number _____

Customer Company _____ Motorola Part Numbers

Address _____ MC _____

SC _____

City _____ State _____ Zip _____

Country _____

Phone _____ Extension _____

Customer Contact Person _____

Customer Part Number _____

OPTION LIST

Select the options for your MCU from the following list. A manufacturing mask will be generated from this information.

Timer Clock Source
- ☐ Internal $\phi 2$ clock
- ☐ TIMER input pin

Internal Oscillator Input
- ☐ Crystal
- ☐ Resistor

Timer Prescaler
- ☐ 2^0 (divide by 1)
- ☐ 2^1 (divide by 2)
- ☐ 2^2 (divide by 4)
- ☐ 2^3 (divide by 8)
- ☐ 2^4 (divide by 16)
- ☐ 2^5 (divide by 32)
- ☐ 2^6 (divide by 64)
- ☐ 2^7 (divide by 128)

Low Voltage Inhibit
- ☐ Disable
- ☐ Enable

Port A Output Drive
- ☐ CMOS and TTL
- ☐ TTL Only

Pattern Media (All other media requires prior factory approval.)
- ☐ EPROMs (MCM2716 or MCM2532)
- ☐ EPROM MCU (MC68705P3)
- ☐ Floppy Disk
- ☐ Other _____

Clock Freq. _____

Temp. Range _____ ☐ 0° to +70°C (Standard) ☐ −40° to +85°C

Marking Information (12 Characters Maximum)

Title _____

Signature _____

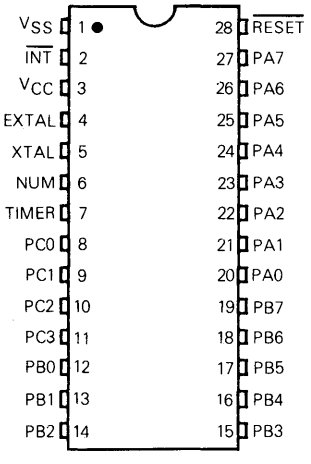
FIGURE 12-2. Sample Custom MCU Order Form

SECTION 13
MECHANICAL DATA

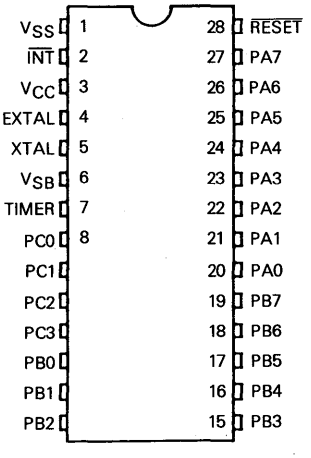
This section contains the pin assignments and package dimension for the MC68(7)05 series devices.

13.1 PIN ASSIGNMENT

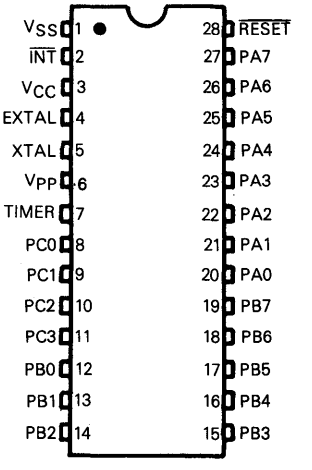
MC6805P2 and MC6805P6



MC6805P4

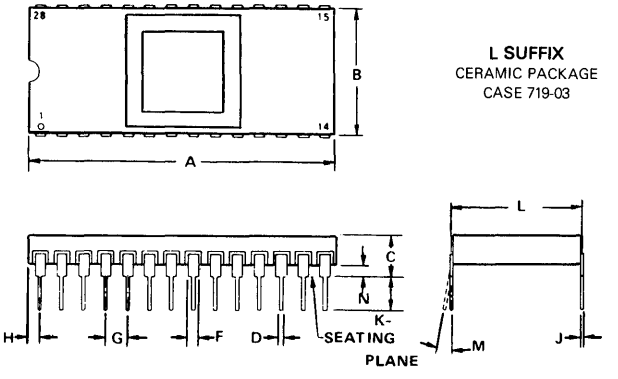


MC68705P3



13.2 PACKAGE DIMENSIONS

13.2.1 Ceramic — MC6805P2, MC6805P4, and MC6805P6

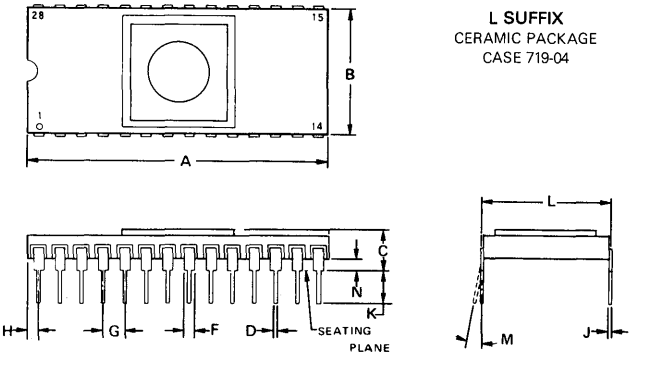


L SUFFIX
CERAMIC PACKAGE
CASE 719-03

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.94	15.34	0.588	0.604
C	3.05	4.19	0.120	0.165
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.19	0.100	0.165
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

13.2.2 Ceramic — MC68705P3

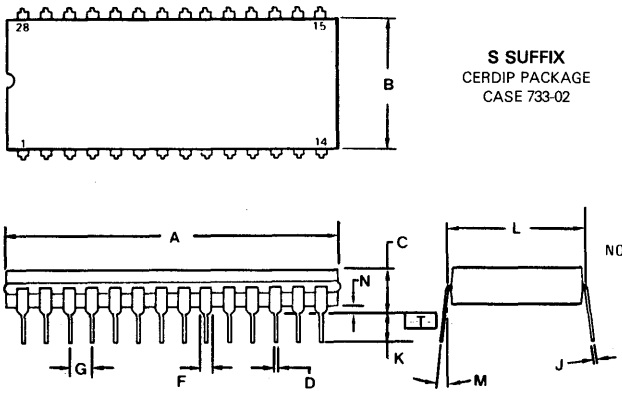


L SUFFIX
CERAMIC PACKAGE
CASE 719-04

DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	35.20	35.92	1.386	1.414
B	14.73	15.34	0.580	0.604
C	3.18	5.08	0.125	0.200
D	0.38	0.53	0.015	0.021
F	0.76	1.40	0.030	0.055
G	2.54 BSC		0.100 BSC	
H	0.76	1.78	0.030	0.070
J	0.20	0.30	0.008	0.012
K	2.54	4.57	0.100	0.180
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.52	0.020	0.060

NOTES:
1. LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIAMETER (AT SEATING PLANE) AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

13.2.3 Cerdip — MC6805P2, MC6805P4, and MC6805P6

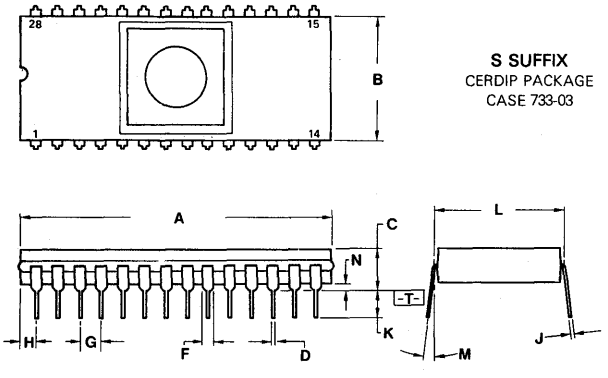


S SUFFIX
CERDIP PACKAGE
CASE 733-02

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.54	4.06	0.100	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

13.2.4 Cerdip — MC68705P3

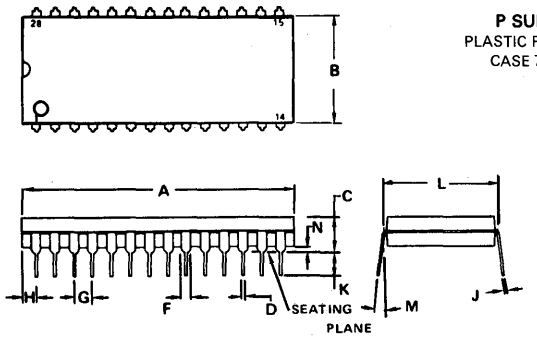


S SUFFIX
CERDIP PACKAGE
CASE 733-03

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	36.45	37.85	1.435	1.490
B	12.70	15.37	0.500	0.605
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOL FOR LEADS:
   ⌖ | Ø 0.25 (0.010) Ⓜ | T | A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM A AND B INCLUDES MENISCUS.
5. DIM -L- TO CENTER OF LEADS WHEN FORMED PARALLEL.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

13.2.5 Plastic — MC6805P2, MC6805P4, and MC6805P6



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	36.45	37.21	1.435	1.465
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0^0	15^0	0^0	15^0
N	0.51	1.02	0.020	0.040

NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

MOTOROLA *Semiconductor Products Inc.*

3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721 • A SUBSIDIARY OF MOTOROLA INC.

A17774 PRINTED IN USA 10-84 IMPERIAL LITHO C25888 18,000

ADI-1031