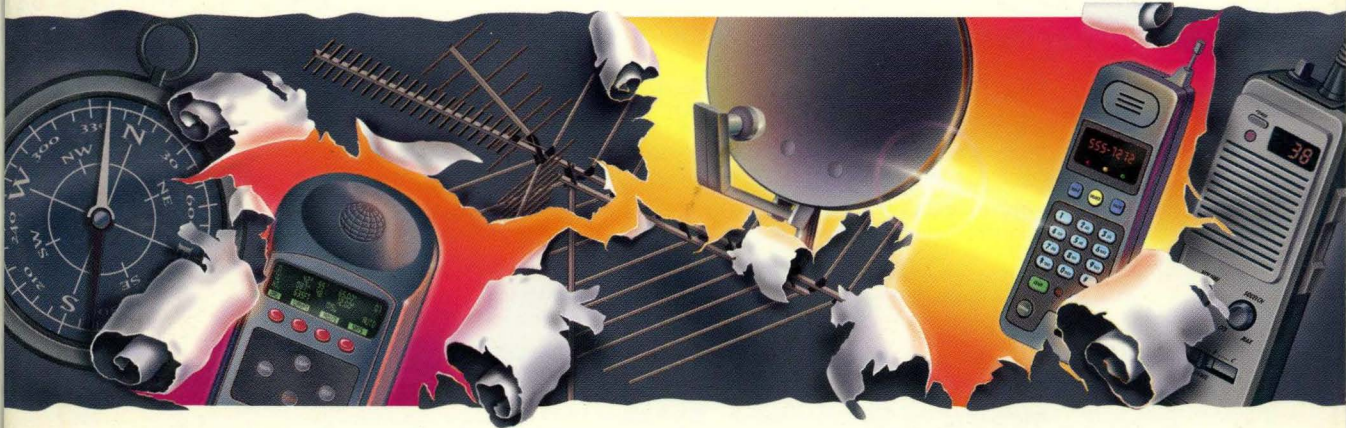


# HIPERCOMM

High Performance Frequency Control Products



FAMILIAR TERRAIN  BETTER TRAILS

*featuring*  
*1.1, 2.0 and 2.5GHz*  
*Single and Dual Synthesizers*

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# Hipercomm

## High Performance Frequency Control Products

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This book presents technical data on a broad line of integrated circuits useful in a wide variety of PLL (Phase-Locked Loop) applications. Complete specifications for individual circuits are provided in the form of data sheets. In addition, an introductory section is included to simplify selection of the proper component(s) for a given set of application requirements. The Hi-Performance and Communication Products family of Frequency Control PLL products is growing rapidly. For data sheets designated as "Product Preview" or "Advance Information," as well as new products, please contact your Motorola representative.

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# Numerical Device Listing

Device	Function	Pins	DIP	SM	Temperature Range
MC1648	Voltage Controlled Oscillator	14	P,L	D,FN	-30 to +85°C
MC1658	Voltage Controlled Multivibrator	16	P,L	D,FN	-30 to +85°C
MC12015	225MHz +32/33 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12016	225MHz +40/41 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12017	225MHz +64/65 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12018	520MHz +128/129 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12019	225MHz +20/21 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12022A	1.1GHz +64/65, +128/129 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12022B	1.1GHz +64/65, +128/129 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12022LVA	1.1GHz +64/65, +128/129 Low Voltage Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12022LVB	1.1GHz +64/65, +128/129 Low Voltage Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12022SLA	1.1GHz +64/65, +128/129 Low Power Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12022SLB	1.1GHz +64/65, +128/129 Low Power Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12022TSA	1.1GHz +64/65, +128/129 Low Power Dual Modulus Prescaler With On-Chip Output Termination	8	P	D	-40 to +85°C
MC12022TSB	1.1GHz +64/65, +128/129 Low Power Dual Modulus Prescaler With On-Chip Output Termination	8	P	D	-40 to +85°C
MC12022TVA	1.1GHz +64/65, +128/129 Low Voltage, Low Power Dual Modulus Prescaler With On-Chip Output Termination	8	P	D	-40 to +85°C
MC12022TVB	1.1GHz +64/65, +128/129 Low Voltage, Low Power Dual Modulus Prescaler With On-Chip Output Termination	8	P	D	-40 to +85°C
MC12023	225MHz +64 Prescaler	8	P	D	0 to +70°C
MC12025	520MHz +64/65 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12026A	1.1GHz +8/9, +16/17 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12026B	1.1GHz +8/9, +16/17 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12028A	1.1GHz +32/33, +64/65 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12028B	1.1GHz +32/33, +64/65 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12031A	2.0GHz +64/65, +128/129 Low Voltage Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12031B	2.0GHz +64/65, +128/129 Low Voltage Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12032A	2.0GHz +64/65, +128/129 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12032B	2.0GHz +64/65, +128/129 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12033A	2.0GHz +32/33, +64/65 Low Voltage Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12033B	2.0GHz +32/33, +64/65 Low Voltage Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12034A	2.0GHz +32/33, +64/65 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12034B	2.0GHz +32/33, +64/65 Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12036A	1.1GHz +64/65, +128/129 Dual Modulus Prescaler With Stand-By Mode	8	P	D	-40 to +85°C
MC12036B	1.1GHz +64/65, +128/129 Dual Modulus Prescaler With Stand-By Mode	8	P	D	-40 to +85°C
MC12038A	1.1GHz +64/65, +127/128, +255/256 Low Power Dual Modulus Prescaler	8	P	D	-40 to +85°C
MC12040	Phase-Frequency Detector	14,20	P,L	FN	0 to +75°C

## Numerical Device Listing (continued)

Device	Function	Pins	DIP	SM	Temperature Range
MC12052A	1.1GHz +64/65, +128/129 Super Low Power Dual Modulus Prescaler	8	–	D, SD	–40 to +85°C
MC12053A	1.1GHz +64/65, +128/129 Super Low Power Dual Modulus Prescaler With Stand-By Mode	8	–	D, SD	–40 to +85°C
MC12054A	2.0GHz +64/65, +128/129 Super Low Power Dual Modulus Prescaler	8	–	D, SD	–40 to +85°C
MC12058	1.1GHz +126/128, +254/256 Low Power Dual Modulus Prescaler	8	–	D, SD	–40 to +85°C
MC12073	1.1GHz +64 Prescaler	8	P	D	0 to +70°C
MC12074	1.1GHz +256 Low-Power Prescaler	8	P	D	0 to +70°C
MC12075	1.3GHz +64 Prescaler	8	P	D	0 to +85°C
MC12076	1.3GHz +256 Prescaler	8	P	D	0 to +85°C
MC12078	1.3GHz +256 Prescaler	8	P	D	0 to +85°C
MC12079	2.8GHz +64/128/256 Prescaler	8	P	D	–40 to +85°C
MC12080	1.1GHz +10/20/40/80 Prescaler	8	P	D	–40 to +85°C
MC12083	1.1GHz +2 Low Power Prescaler With Stand-By Mode	8	P	D	–40 to +85°C
MC12089	2.8GHz +64/128 Prescaler	8	P	D	–40 to +85°C
MC12090	750MHz +2 UHF Prescaler	16	P,L	–	0 to +75°C
MC12093	1.1GHz +2/4/8 Low Power Prescaler With Stand-By Mode	8	–	D, SD	–40 to +85°C
MC12095	2.5GHz +2/4 Low Power Prescaler With Stand-By Mode	8	–	D, SD	–40 to +85°C
MC12100	200MHz Voltage Controlled Multivibrator	20	P	DW, M, FN	0 to +75°C
MC12101	130MHz Voltage Controlled Multivibrator	20	P	DW, M, FN	0 to +75°C
MCH/K12140	Phase-Frequency Detector	8	–	D	–40 to +70°C
MC12148	Low Power Voltage Controlled Oscillator Buffer	8	–	D, SD	–40 to +85°C
MC12148	Low Power Voltage Controlled Oscillator	8	–	D, SD	–40 to +85°C
MC12149	Ultra Low Power Voltage Controlled Oscillator	8	–	D, SD	–40 to +85°C
MC12179	500–2800MHz Single Channel Frequency Synthesizer	8	–	D	–40 to +85°C
MC12202	1.1GHz Serial Input Synthesizer	16,20	–	D, DT	–40 to +85°C
MC12206	2.0GHz Serial Input Synthesizer	16,20	–	D, DT	–40 to +85°C
MC12210	2.5GHz Serial Input Synthesizer	16,20	–	D, DT	–40 to +85°C
MC12302	1.1GHz/500MHz Low Voltage Dual RF/IF PLL Frequency Synthesizer	20	–	DT	–40 to +85°C
MC12306	2.0GHz/500MHz Low Voltage Dual RF/IF PLL Frequency Synthesizer	20	–	DT	–40 to +85°C
MC12310	2.5GHz/500MHz Low Voltage Dual RF/IF PLL Frequency Synthesizer	20	–	DT	–40 to +85°C



# Prescalers

### Prescaler Selection Table

Device	Frequency (MHz)		Modulus	Prescaler Ratio(s)	Output Edge	Supply Voltage	Typical I <sub>CC</sub> (mA)	Sensitivity (mVpp)		Special Features
	Min	Max						Min	Max	
12015	35	225	Dual	32/33	A	4.5–9.0	6.0	200	800	TTL Output
12016	35	225	Dual	40/41	A	4.5–9.0	6.0	200	800	TTL Output
12017	35	225	Dual	64/65	A	4.5–9.0	6.0	200	800	TTL Output
12018	75	520	Dual	128/129	A	4.5–9.0	8.0	200	800	On-Chip Regulator for 5.5V to 9.5V Supply
12019	20	225	Dual	20/21	A	4.5–9.0	6.0	200	800	On-Chip Regulator for 5.5V to 9.5V Supply
12022	100	1100	Dual	64/65 or 128/129	A or B	4.5–5.5	7.5	100	1500	
12022LV	100	1100	Dual	64/65 or 128/129	A or B	2.7–5.0	4.0	100	1500	
12022SL	100	1100	Dual	64/65 or 128/129	A or B	4.5–5.5	4.0	100	1500	
12022TS	100	1100	Dual	64/65 or 128/129	A or B	4.5–5.5	4.0	100	1500	On-Chip Output Termination
12022TV	100	1100	Dual	64/65 or 128/129	A or B	2.7–5.0	4.0	100	1500	On-Chip Output Termination
12023	35	225	Single	64	–	3.2–5.5	6.0	200	800	TTL Output
12025	30	520	Dual	64/65	A	4.75–5.25	9.5	100	800	
12026	100	1100	Dual	8/9 or 16/17	A or B	4.5–5.5	4.0	100	1000	Short Setup Time on Modulus Control
12028	100	1100	Dual	32/33 or 64/65	A or B	4.5–5.5	4.0	100	1500	
12031	500	2000	Dual	64/65 or 128/129	A or B	2.7–5.0	10.0	100	1500	
12032	500	2000	Dual	64/65 or 128/129	A or B	4.5–5.5	8.5	100	1500	
12033	500	2000	Dual	32/33 or 64/65	A or B	2.7–5.0	10.0	100	1000	
12034	500	2000	Dual	32/33 or 64/65	A or B	4.5–5.5	8.5	100	1500	
12036	100	1100	Dual	64/65 or 128/129	A or B	4.5–5.5	4.0	100	1000	
12038	100	1100	Dual	127/128 or 255/256	A	4.5–5.5	4.0	100	1500	
12052	100	1100	Dual	64/65 or 128/129	A	4.5–5.5	1.0	100	1000	
12053	100	1100	Dual	64/65 or 128/129	A	4.5–5.5	1.6	100	1000	Standby/On-Chip Output Termination
12054	100	2000	Dual	64/65 or 128/129	A	2.7–5.5	2.0	100	1000	
12058	100	1100	Dual	126/128 or 254/256	A	2.7–5.5	1.1	100	1000	
12073	90	1100	Single	64	–	4.5–5.5	23.0	20*	200*	Differential PECL Outputs
12074	90	1100	Single	256	–	4.5–5.5	23.0	20*	200*	Differential PECL Outputs
12075	70	1300	Single	64	–	4.5–5.5	36.0	4*	400*	Differential PECL Outputs
12076	70	1300	Single	256	–	4.5–5.5	36.0	4*	400*	Differential PECL Outputs
12078	90	1300	Single	256	–	4.5–5.5	28.0	20*	400*	Differential PECL Outputs
12079	250	2800	Single	64/128/256	–	4.5–5.5	9.0	100	400	
12080	100	1100	Single	10/20/40/80	–	4.5–5.5	3.7	100	400	
12083	100	1100	Single	2	–	2.7–5.5	4.4	100	1100	
12089	250	2800	Single	64/128	–	4.5–5.5	10.2	100	1000	
12093	100	1000	Single	2/4/8	–	2.7–5.5	3.0	100	1000	Standby Power–Down
12095	100	2500	Single	2/4	–	2.7–5.5	10.0	100	1000	Standby Power–Down

\* Specified as RMS

## Dual Modulus Prescaler

The MC12015, MC12016 and MC12017 are dual modulus prescalers which will drive divide by 32 and 33, 40 and 41, and 64 and 65, respectively. An internal regulator is provided to allow these devices to be used over a wide range of power-supply voltages. The devices may be operated by applying a supply voltage of 5.0Vdc  $\pm$ 10% at Pin 7, or by applying an unregulated voltage source from 5.5Vdc to 9.5Vdc to Pin 8.

- 225MHz Toggle Frequency
- Low-Power 7.5mA Maximum at 6.8V
- Control Input and Output Are Compatible With Standard CMOS
- Connecting Pins 2 and 3 Allows Driving One TTL Load
- Supply Voltage 4.5V to 9.5V

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
V <sub>reg</sub>	Regulated Voltage, Pin 7	8.0	Vdc
V <sub>CC</sub>	Power Supply Voltage, Pin 8	10.0	Vdc
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +175	°C

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5.5 to 9.5V; V<sub>reg</sub> = 4.5 to 5.5V; T<sub>A</sub> = -40 to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
f <sub>max</sub> f <sub>min</sub>	Toggle Frequency (Sine Wave Input)	225		35	MHz
I <sub>CC</sub>	Supply Current		6.0	7.8	mA
V <sub>IH</sub>	Control Input HIGH (÷32, 40 or 64)	2.0			V
V <sub>IL</sub>	Control Input LOW (÷33, 41 or 65)			0.8	V
V <sub>OH</sub>	Output Voltage HIGH <sup>1</sup> (I <sub>source</sub> = 50μA)	2.5			V
V <sub>OL</sub>	Output Voltage LOW <sup>1</sup> (I <sub>sink</sub> = 2mA)			0.5	V
V <sub>in</sub>	Input Voltage Sensitivity 35MHz 50-225MHz	400 200		800 800	mVpp
t <sub>PLL</sub>	PLL Response Time (Notes 2 and 3)			t <sub>out</sub> -70	ns

1. Pin 2 connected to Pin 3
2. t<sub>PLL</sub> = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection
3. t<sub>out</sub> = period of output waveform

**MC12015**  
**MC12016**  
**MC12017**

### MECL PLL COMPONENTS

#### DUAL MODULUS PRESCALER

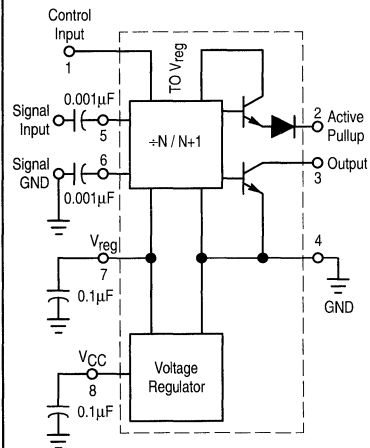


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### PRESCALER BLOCK DIAGRAM



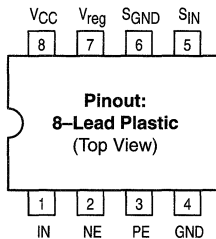
1. V<sub>reg</sub> at Pin 7 is not guaranteed to be between 4.5 and 5.5V when V<sub>CC</sub> is being applied to Pin 8
2. Pin 7 is not to be used as a source of regulated output voltage



## 520MHz Dual Modulus Prescaler

The MC12018 is a dual modulus prescaler which divides by 128 and 129. An internal regulator is provided to allow this device to be used over a wide range of power-supply voltages. The devices may be operated by applying a supply voltage of 5.0Vdc  $\pm 10\%$  at Pin 7, or by applying an unregulated voltage source from 5.5Vdc to 9.5Vdc to Pin 8.

- 520MHz Toggle Frequency
- Low-Power 8.0mA Typical
- Control Input Is Compatible With Standard CMOS and TTL
- Supply Voltage 4.5V to 9.5V
- On-Chip 10K $\Omega$  Resistor from Positive Edge to Ground



### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{reg}$	Regulated Voltage, Pin 7	8.0	Vdc
$V_{CC}$	Power Supply Voltage, Pin 8	10.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +175	$^{\circ}\text{C}$

### ELECTRICAL CHARACTERISTICS

( $V_{CC} = 5.5$  to  $9.5\text{V}$ ;  $V_{reg} = 4.5$  to  $5.5\text{V}$ ;  $T_A = -40$  to  $+85^{\circ}\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_{max}$ $f_{min}$	Toggle Frequency (Sine Wave Input)	520		75	MHz
$I_{CC}$	Supply Current		8.0	10.7	mA
$V_{IH}$	Control Input HIGH (+128)	2.0			V
$V_{IL}$	Control Input LOW (+129)			0.8	V
$V_{out}$	Differential Output Voltage ( $I_{sink} = 200\mu\text{A}$ )	0.8	1.0		V
$V_{in}$	Input Voltage Sensitivity 75MHz 125–520MHz	400 200		800 800	mVpp
$t_{PLL}$	PLL Response Time (Notes 1 and 2)			$t_{out} - 50$	ns

1.  $t_{PLL}$  = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection
2.  $t_{out}$  = period of output waveform

## MC12018

### MECL PLL COMPONENTS

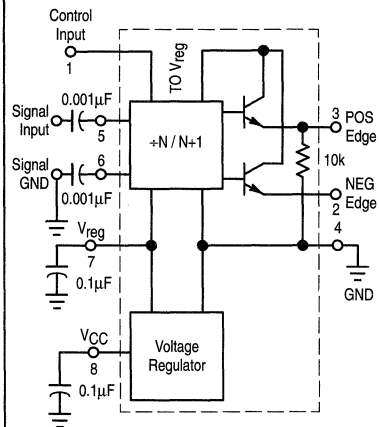
#### +128/129 DUAL MODULUS PRESCALER



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05

**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### PRESCALER BLOCK DIAGRAM



1.  $V_{reg}$  at Pin 7 is not guaranteed to be between 4.5 and 5.5V when  $V_{CC}$  is being applied to Pin 8
2. Pin 7 is not to be used as a source of regulated output voltage
3. 10K $\Omega$  pulldown recommended with negative edge output (Pin 2)

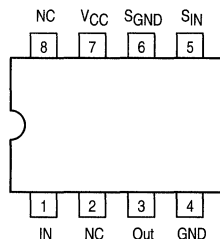


## Dual Modulus Prescaler

The MC12019 is a divide by 20 and 21 dual modulus prescaler. It will divide by 20 when the modulus control input is HIGH and divide by 21 when the modulus control input is LOW.

- 225MHz Toggle Frequency
- Low-Power 7.5mA Maximum at 5.5V
- Control Input Is Compatible With Standard Motorola CMOS Synthesizers
- Emitter Follower Outputs

Pinout: 8-Lead Plastic (Top View)



### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 7	8.0	Vdc
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +175	°C

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 4.5 to 5.5V; T<sub>A</sub> = -40 to +85°C)

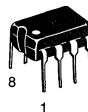
Symbol	Characteristic	Min	Typ	Max	Unit
f <sub>max</sub> f <sub>min</sub>	Toggle Frequency (Sine Wave Input)	225		20	MHz
I <sub>CC</sub>	Supply Current			7.5	mA
V <sub>IH</sub>	Control Input HIGH (÷20)	2.0			V
V <sub>IL</sub>	Control Input LOW (÷21)			0.8	V
V <sub>out</sub>	Output Swing Voltage	600		1200	mV <sub>pp</sub>
V <sub>in</sub>	Input Voltage Sensitivity 20-225MHz	200		800	mV <sub>pp</sub>
t <sub>PLL</sub>	PLL Response Time (Notes 1 and 2)			t <sub>out</sub> -70	ns

1. t<sub>PLL</sub> = the period of time the PLL has from the prescaler rising output transition (50%) to the modulus control input edge transition (50%) to ensure proper modulus selection
2. t<sub>out</sub> = period of output waveform

## MC12019

### MECL PLL COMPONENTS

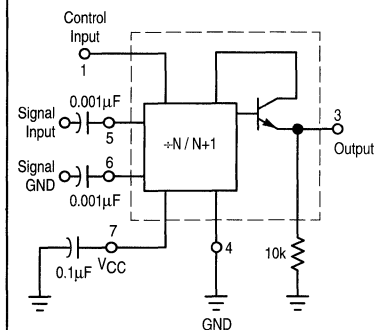
#### ÷20/21 DUAL MODULUS PRESCALER



P SUFFIX  
PLASTIC PACKAGE  
CASE 626-05

D SUFFIX  
PLASTIC SOIC PACKAGE 8  
CASE 751-05

### PRESCALER BLOCK DIAGRAM



# 1.1GHz Dual Modulus Prescaler

The MC12022A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

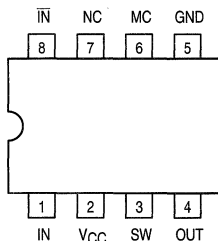
The MC12022B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5V
- Low-Power 7.5mA Typical
- Operating Temperature Range of -40 to +85°C
- Short Setup Time ( $t_{set}$ ) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL. Maximum Input Voltage Should Be Limited to 6.5Vdc

Pinout: 8-Lead Plastic (Top View)



### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H =  $V_{CC}$ , L = Open  
MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V

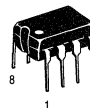
### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

**MC12022A**  
**MC12022B**

### MECL PLL COMPONENTS

**+64/65, +128/129**  
**DUAL MODULUS**  
**PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.6	1.1	GHz
$I_{CC}$	Supply Current Output Unloaded (Pin 2)		7.5	10	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input Low (MC)			0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
$V_{out}$	Output Voltage Swing ( $C_L = 12pF$ ; $R_L = 2.2k\Omega$ )	1.0	1.6		$V_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out		11	16	ns
$V_{in}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400		1500 1500	mVpp
$I_O$	Output Current ( $C_L = 12pF$ ; $R_L = 2.2k\Omega$ )		1.5	4.0	mA

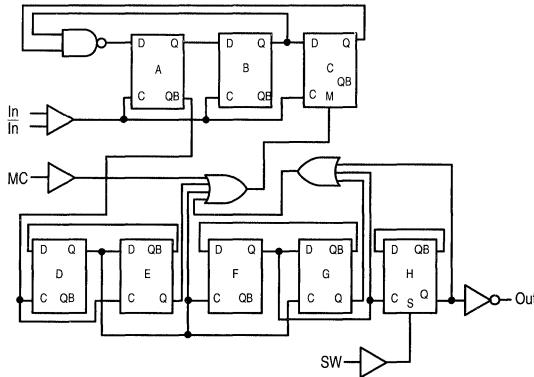
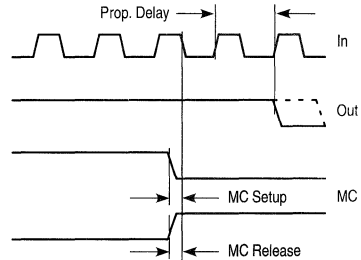
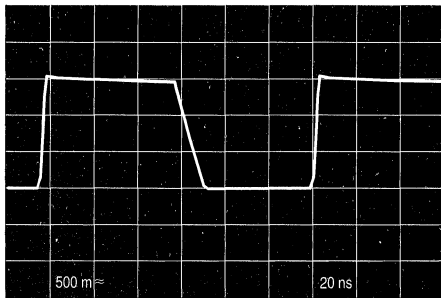


Figure 1. Logic Diagram (MC12022A)

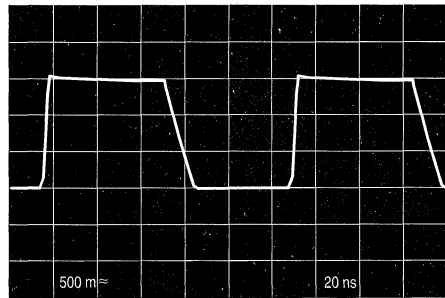


Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time



(+64, 500MHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)

Figure 3. Typical Output Waveforms

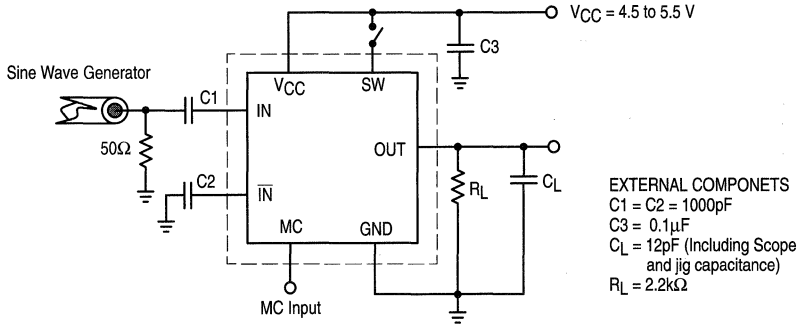


Figure 4. AC Test Circuit

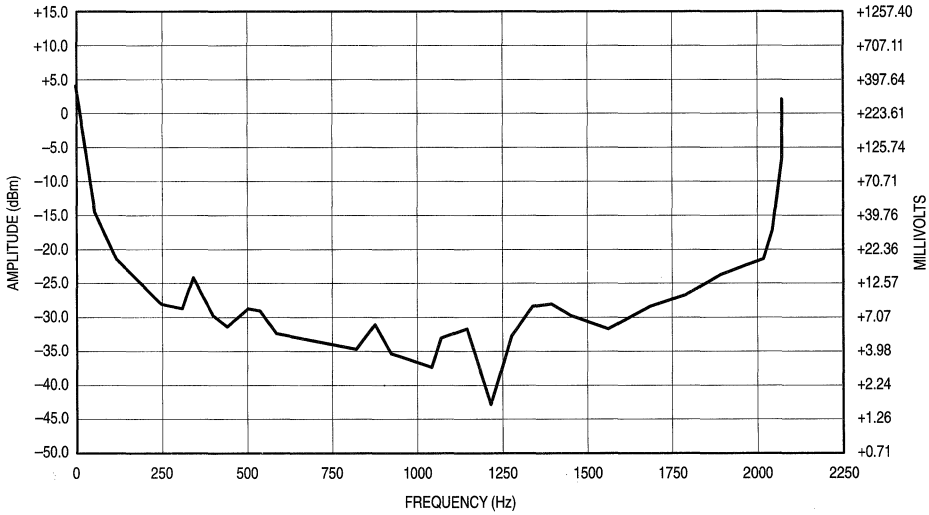


Figure 5. Input Signal Amplitude versus Input Frequency  
 Divide Ratio = 8; VCC = 5.0V; TA = 25°C

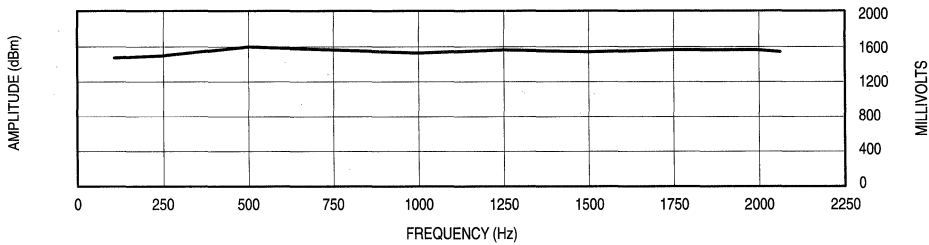


Figure 6. Output Amplitude versus Input Frequency



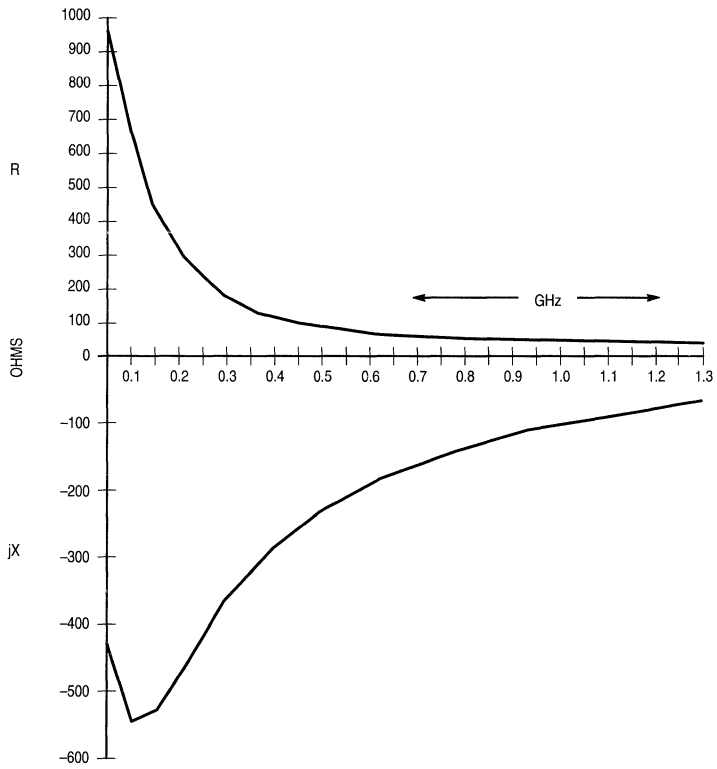


Figure 7. Typical Input Impedance versus Input Frequency

# 1.1GHz Low-Voltage Dual Modulus Prescaler

The MC12022LVA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

The MC12022LVB can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.0V
- Low-Power 4.0mA Typical at  $V_{CC} = 2.7V$
- Operating Temperature Range of  $-40$  to  $+85^{\circ}C$
- Short Setup Time ( $t_{set}$ ) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

## FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H =  $V_{CC}$ , L = Open  
MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V

## DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\* Equivalent to a two-input NAND gate

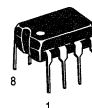
## MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to + 7.0	Vdc
$T_A$	Operating Temperature Range	-40 to + 85	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to + 150	$^{\circ}C$
MC	Modulus Control Input, Pin 6	-0.5 to + 6.5	Vdc

# MC12022LVA MC12022LVB

## MECL PLL COMPONENTS

### $\div 64/65$ , $\div 128/129$ DUAL MODULUS PRESCALER

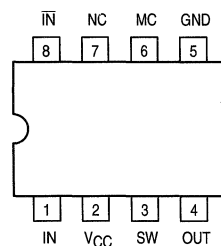


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

## Pinout: 8-Lead Plastic (Top View)



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.0V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CCL}$	Supply Current Output Unloaded (Pin 2) at 2.7Vdc		4.7	6.5	mA
$I_{CCH}$	Supply Current Output Unloaded (Pin 2) at 5.0Vdc		5.8	8.0	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input Low (MC)			0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
$V_{out}$	Output Voltage Swing $C_L = 12pF$ ; $R_L = 1.1k\Omega$ at 2.7Vdc	0.8	1.0		$V_{p-p}$
$V_{out}$	Output Voltage Swing $C_L = 12pF$ ; $R_L = 2.2k\Omega$ at 5.0Vdc	1.0	1.6		$V_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out		11	16	ns
$V_{in(min)}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400		1500 1500	mVpp
$I_O$	Output Current $C_L = 12pF$ ; $R_L = 1.1k\Omega$ at 2.7Vdc $C_L = 12pF$ ; $R_L = 2.2k\Omega$ at 5.0Vdc		1.2 1.2	4.0 4.0	mA

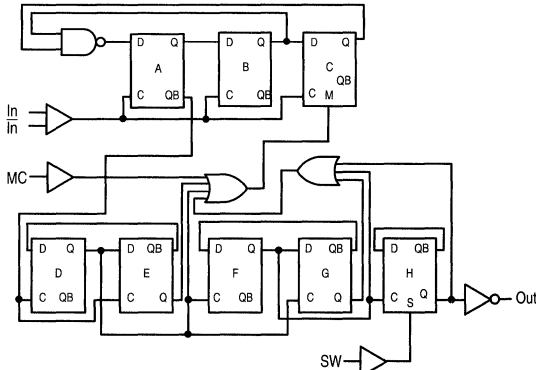
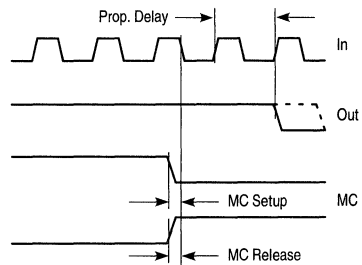
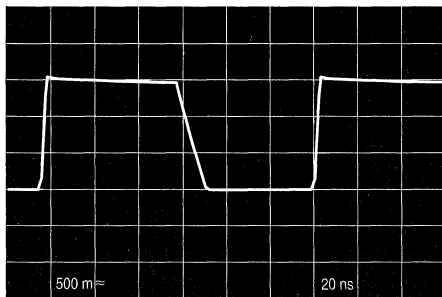


Figure 1. Logic Diagram (MC12022LVA)

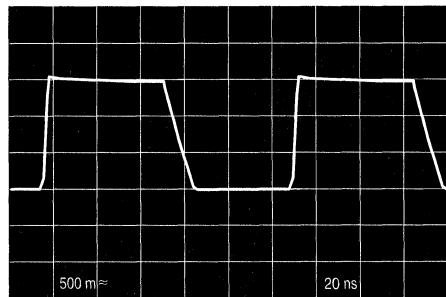


Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time



(+64, 500MHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)

Figure 3. Typical Output Waveforms

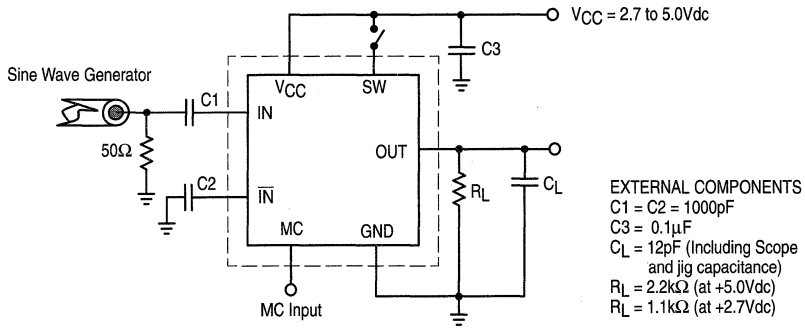


Figure 4. AC Test Circuit

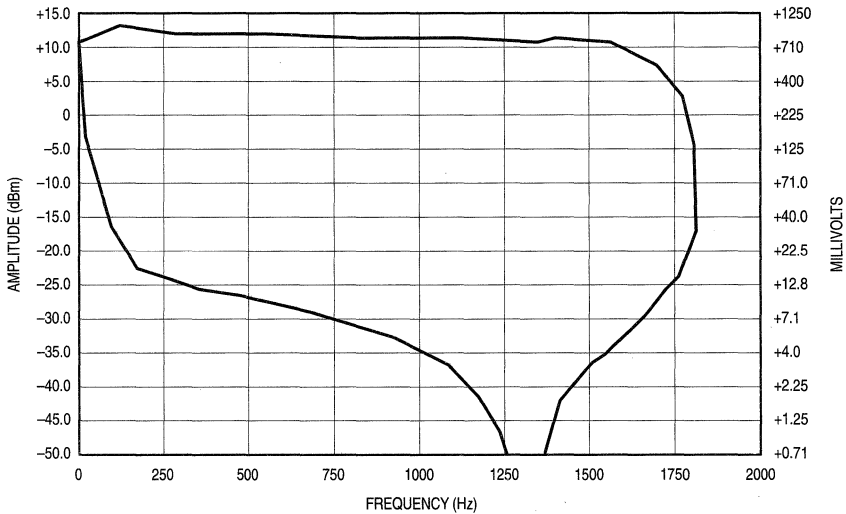


Figure 5. Input Signal Amplitude versus Input Frequency  
 Divide Ratio = 128; VCC = 5.0V; TA = 25°C

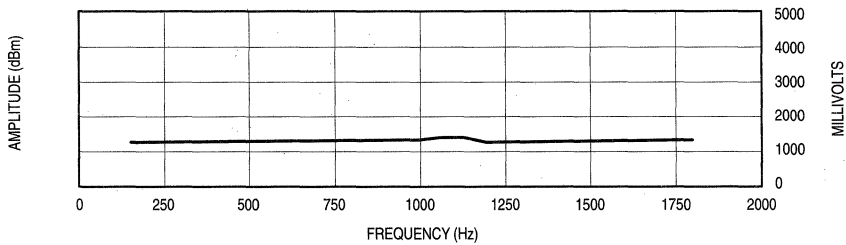


Figure 6. Output Amplitude versus Input Frequency

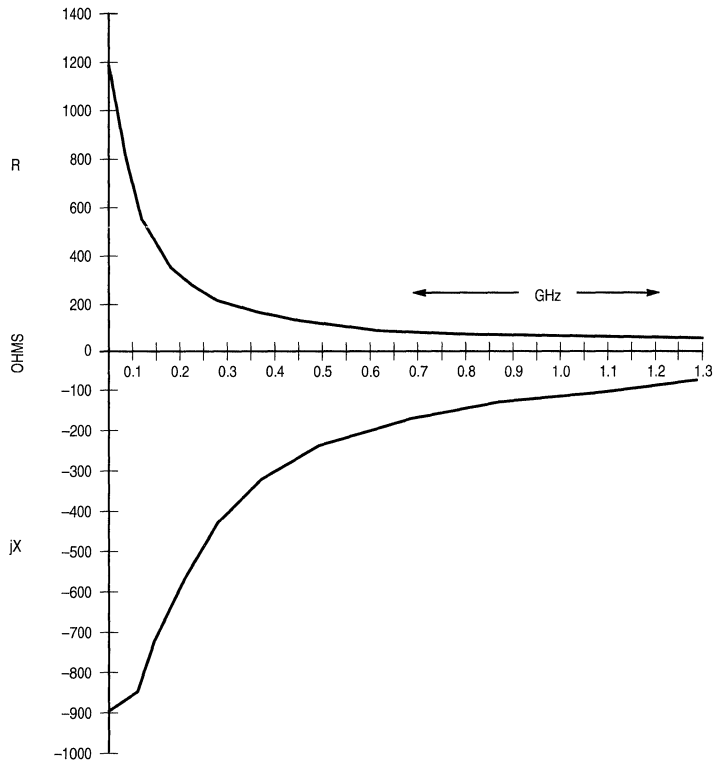


Figure 7. Typical Input Impedance versus Input Frequency

# 1.1GHz Low Power Dual Modulus Prescaler

The MC12022SLA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps. This device is a reduced current version of the MC12022A/B.

The MC12022SLB can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5V
- Low-Power 4.0mA Typical
- Operating Temperature Range of -40 to +85°C
- Short Setup Time ( $t_{set}$ ) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

## FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V<sub>CC</sub>, L = Open  
MC: H = 2.0 V to V<sub>CC</sub>, L = GND to 0.8 V

## DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\* Equivalent to a two-input NAND gate

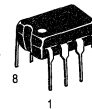
## MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 2	-0.5 to +7.0	V <sub>dc</sub>
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	V <sub>dc</sub>

**MC12022SLA**  
**MC12022SLB**

## MECL PLL COMPONENTS

**+64/65, +128/129**  
**DUAL MODULUS**  
**PRESCALER**

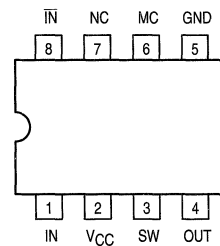


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

**Pinout: 8-Lead Plastic (Top View)**



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current Output Unloaded (Pin 2) at 5.0Vdc		3.8	6.5	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input Low (MC)			0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
$V_{out}$	Output Voltage Swing ( $C_L = 8pF$ ; $R_L = 4.4k\Omega$ )	1.0	1.6		$V_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out		11	16	ns
$V_{in(min)}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400		1500 1500	mVpp
$I_O$	Output Current ( $C_L = 8pF$ ; $R_L = 4.4k\Omega$ , $V_{CC} = 5.0V$ )		0.75	4.0	mA

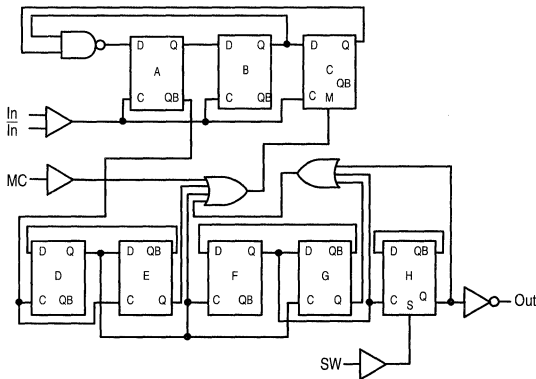


Figure 1. Logic Diagram (MC12022SLA)

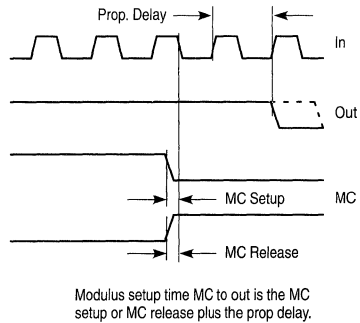
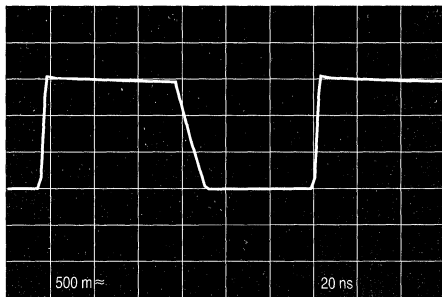
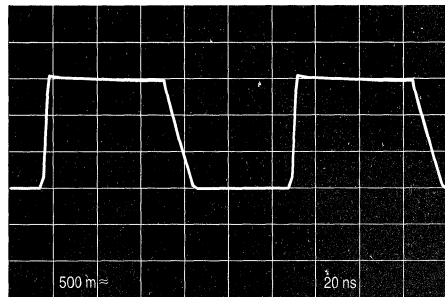


Figure 2. Modulus Setup Time



(+64, 500MHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)

Figure 3. Typical Output Waveforms

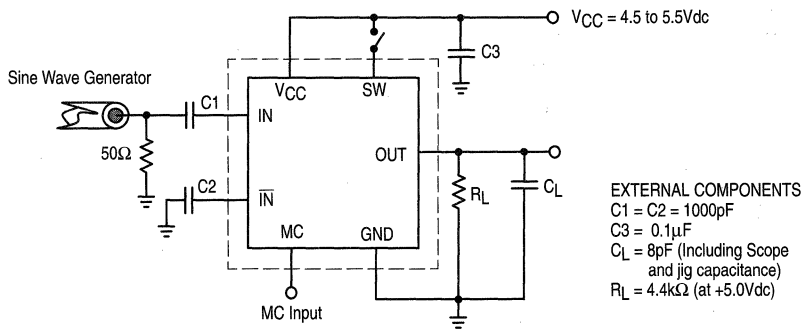


Figure 4. AC Test Circuit

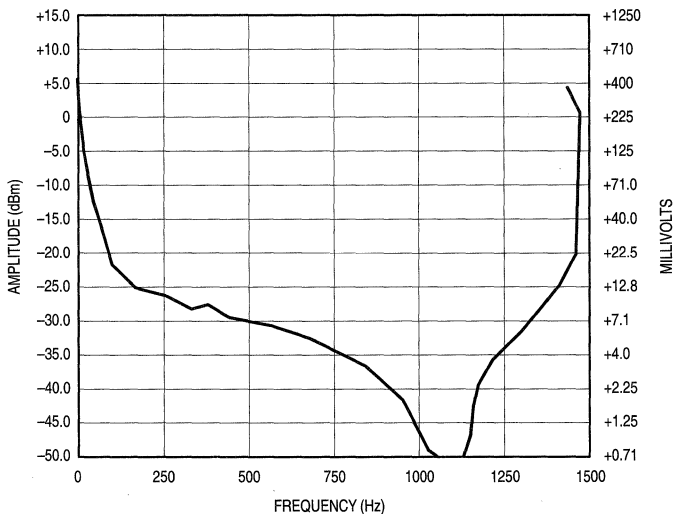


Figure 5. Input Signal Amplitude versus Input Frequency  
 Divide Ratio = 128; V<sub>CC</sub> = 5.0V; T<sub>A</sub> = 25°C

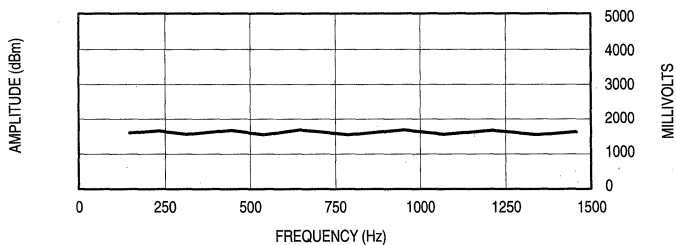


Figure 6. Output Amplitude versus Input Frequency



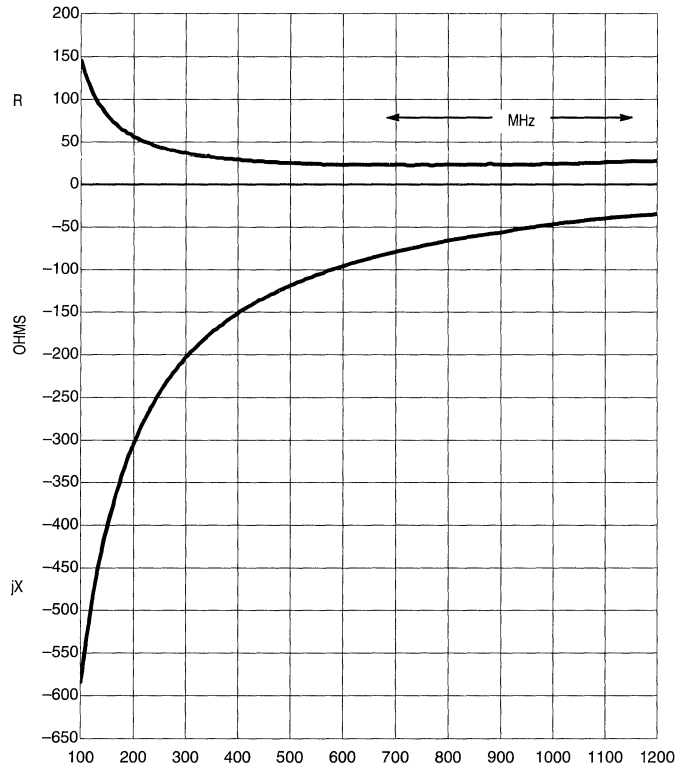


Figure 7. Typical Input Impedance versus Input Frequency

# 1.1GHz Low Power Dual Modulus Prescaler With On-Chip Output Termination

The MC12022TSA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps. This device is a reduced current drain version of the MC12022A/B with the addition of on-chip output termination.

The MC12022TSB can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5V
- Low-Power 4.0mA Typical
- Operating Temperature Range of -40 to +85°C
- Short Setup Time ( $t_{set}$ ) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Output Load Resistor on Die

### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H =  $V_{CC}$ , L = Open  
MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V

### DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\* Equivalent to a two-input NAND gate

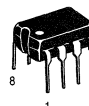
### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C

## MC12022TSA MC12022TSB

### MECL PLL COMPONENTS

÷64/65, ÷128/129  
DUAL MODULUS  
PRESCALER

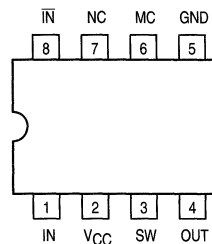


P SUFFIX  
PLASTIC PACKAGE  
CASE 626-05



D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-05

Pinout: 8-Lead Plastic (Top View)



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current (Pin 2)		4.6	6.5	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input Low (MC)			0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
$V_{out}$	Output Voltage Swing ( $C_L = 8pF$ )	1.0	1.4		$V_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out		11	16	ns
$V_{in}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400		1500 1500	mVpp

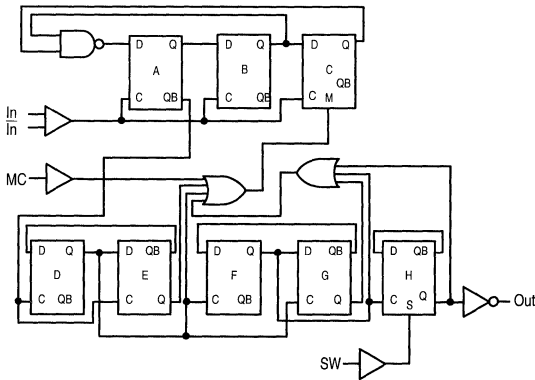


Figure 1. Logic Diagram (MC12022TSA)

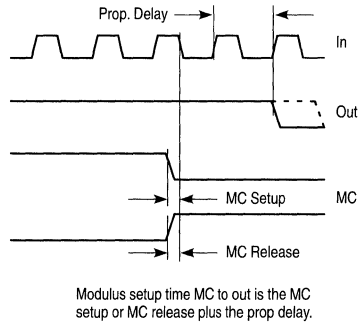
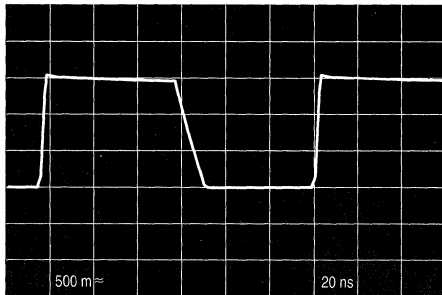
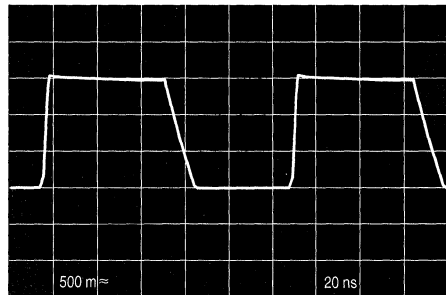


Figure 2. Modulus Setup Time



(+64, 500MHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)

Figure 3. Typical Output Waveforms

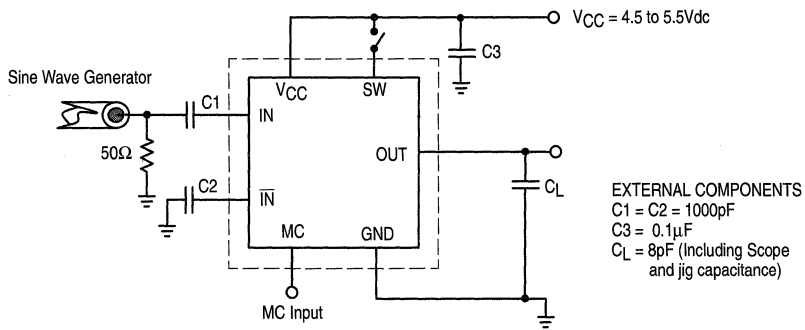


Figure 4. AC Test Circuit

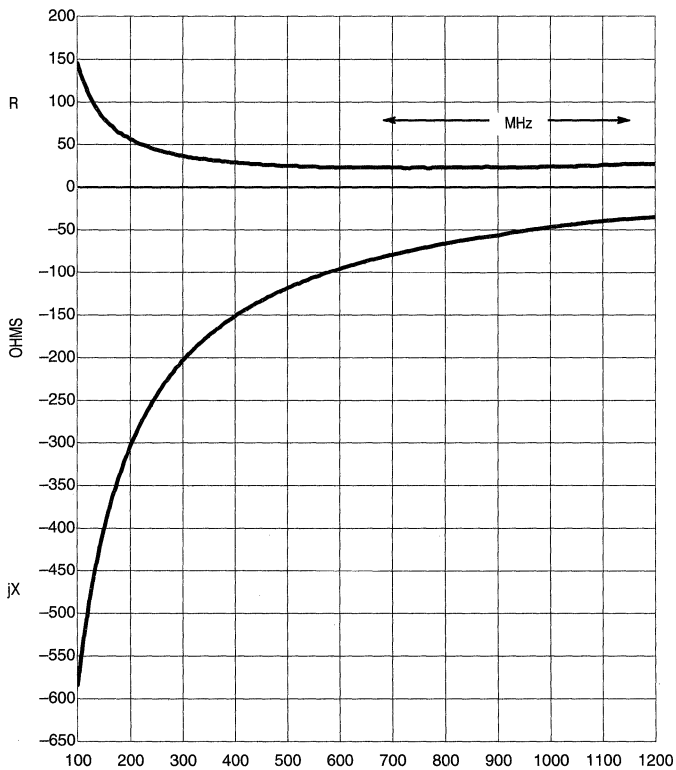


Figure 5. Typical Input Impedance versus Input Frequency

## 1.1GHz Low Voltage, Low Power Dual Modulus Prescaler With On-Chip Output Termination

The MC12022TVA can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX. This device is a low voltage version of the MC12022A/B with the addition of on-chip output termination.

The MC12022TVB can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.0V
- Low-Power 4.0mA Typical @  $V_{CC} = 2.7V$
- Short Setup Time ( $t_{set}$ ) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Output Load Resistor on Die

### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H =  $V_{CC}$ , L = Open

MC: H = 2.0 V to  $V_{CC}$ , L = Gnd to 0.8 V

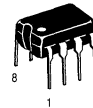
### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 8	-0.5 to + 7.0	Vdc
$T_A$	Operating Temperature Range	-40 to + 85	°C
$T_{stg}$	Storage Temperature Range	-65 to + 150	°C
MC	Modulus Control Input, Pin 6	-0.5 to + 6.5	Vdc

**MC12022TVA**  
**MC12022TVB**

### MECL PLL COMPONENTS

**±64/65, ±128/129**  
**LOW VOLTAGE**  
**DUAL MODULUS PRESCALER**

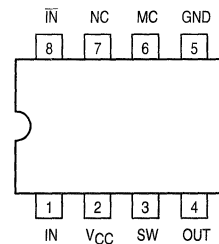


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### Pinout: 8-Lead Plastic (Top View)



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.0$  Vdc,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CCL}$	Supply Current (Pin 2 at 2.7 Vdc)	–	5.2	6.5	mA
$I_{CCH}$	Supply Current (Pin 2 at 5.0 Vdc)	–	5.8	8.0	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0	–	$V_{CC} + 0.5\text{V}$	V
$V_{IL1}$	Modulus Control Input Low (MC)	–	–	0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5\text{V}$	$V_{CC}$	$V_{CC} + 0.5\text{V}$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	–
$V_{out(L)}$	Output Voltage Swing @ 2.7V, $C_L = 8\text{pF}$	0.8	1.0	–	$V_{p-p}$
$V_{out(H)}$	Output Voltage Swing @ 5.0V, $C_L = 8\text{pF}$	1.0	1.4	–	$V_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out	–	11	16	ns
$V_{in}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400	– –	1500 1500	mVpp

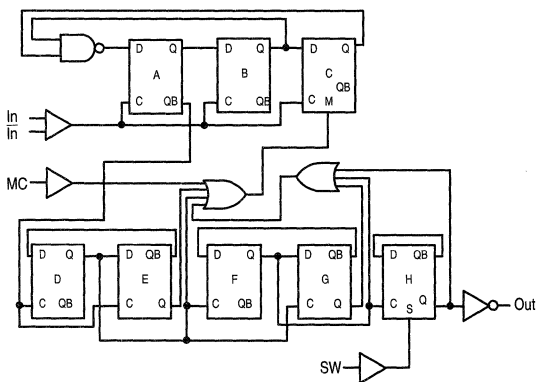
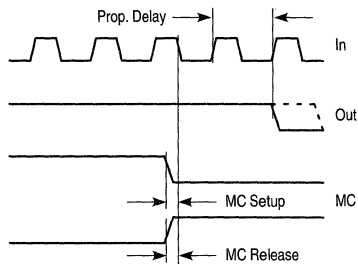
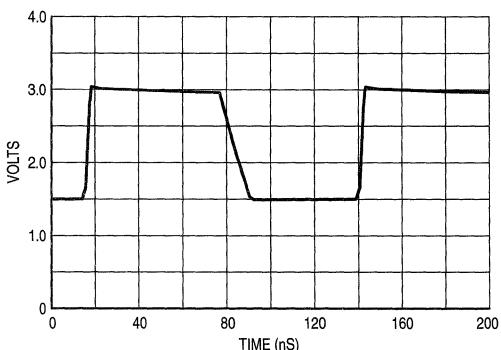


Figure 1. Logic Diagram (MC12022TVA)

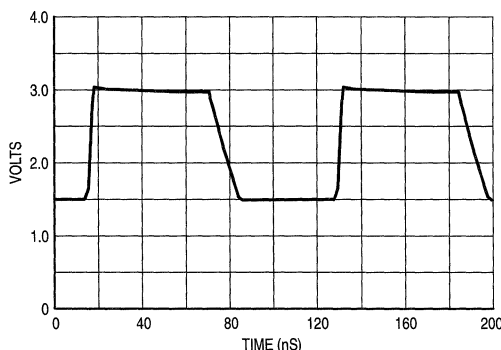


Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time



(+64, 500MHz Input Frequency,  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ , Output Loaded)



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ , Output Loaded)

Figure 3. Typical Output Waveform

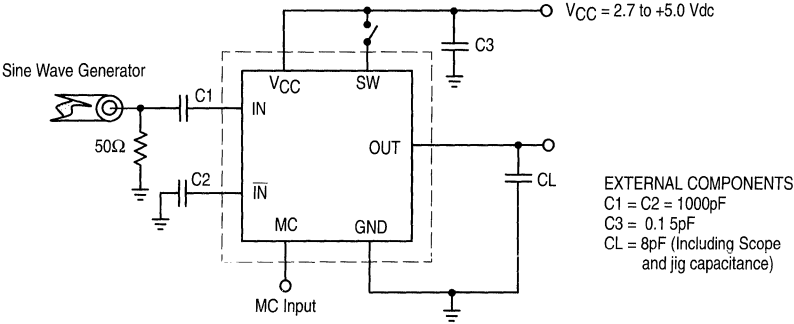


Figure 4. AC Test Circuit

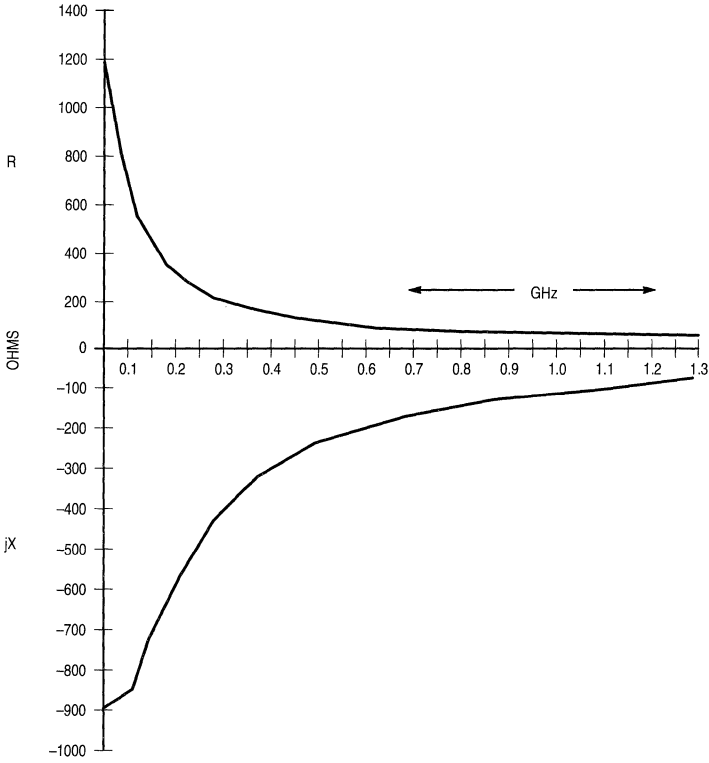


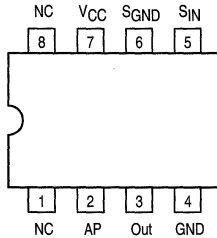
Figure 5. Typical Input Impedance versus Input Frequency

## 225MHz Prescaler

The MC12023 is a prescaler which will divide by 64. This device may be operated over a supply voltage range of 3.2 to 5.5V.

- 225MHz Toggle Frequency
- Low-Power 4.8mA Maximum at 5.5V
- Operating Supply Voltage of 3.2 to 5.5V
- Connecting Pins 2 and 3 Allows Driving One TTL Load

Pinout: 8-Lead Plastic (Top View)



### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
V <sub>CC</sub>	Power Supply Voltage	0 to +8.0	Vdc
T <sub>A</sub>	Operating Temperature Range	0 to +70	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +175	°C

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 3.2 to 5.5V; T<sub>A</sub> = 0 to +70°C)

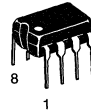
Symbol	Characteristic	Min	Typ	Max	Unit
f <sub>max</sub> f <sub>min</sub>	Toggle Frequency (Sine Wave Input)	225		35	MHz
I <sub>CC</sub>	Supply Current at 5.5V		3.5 <sup>3</sup>	4.8	mA
V <sub>OH</sub>	Output Voltage HIGH <sup>1</sup> (V <sub>CC</sub> = 3.2V) <sup>2</sup>	1.2	1.4		V
V <sub>OH</sub>	Output Voltage HIGH <sup>1</sup> (V <sub>CC</sub> = 5.0V) <sup>2</sup>	2.5			V
V <sub>OL</sub>	Output Voltage LOW <sup>1</sup> (I <sub>sink</sub> = 2.0mA)			0.5	V
V <sub>in</sub>	Input Voltage Sensitivity 35MHz 50-225MHz	400 200		800 800	mV <sub>pp</sub>

1. Pin 2 connected to Pin 3
2. I<sub>source</sub> = 50μA
3. V<sub>CC</sub> = 4.5V

## MC12023

### MECL PLL COMPONENTS

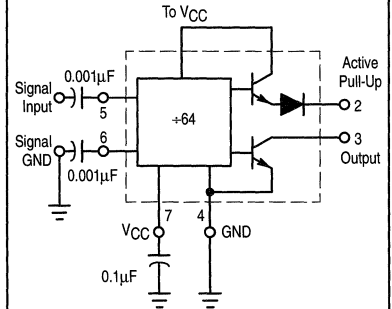
÷64  
PRESCALER



P SUFFIX  
PLASTIC PACKAGE  
CASE 628-05

D SUFFIX  
PLASTIC SOIC PACKAGE 8  
CASE 751-05

### PRESCALER BLOCK DIAGRAM





## 520MHz Dual Modulus Prescaler

The MC12025 is a dual modulus prescaler which divides by 64 and 65. Supply voltages of 4.75 to 5.25V may be connected to Pin 8.

- 520MHz Toggle Frequency
- Low-Power 9.5mA Typical
- Control Input Is Compatible With Standard CMOS and TTL
- Operating Supply Voltage of 5.0V  $\pm$ 0.25V
- Propagation Delay 30ns Typical

### MAXIMUM RATINGS

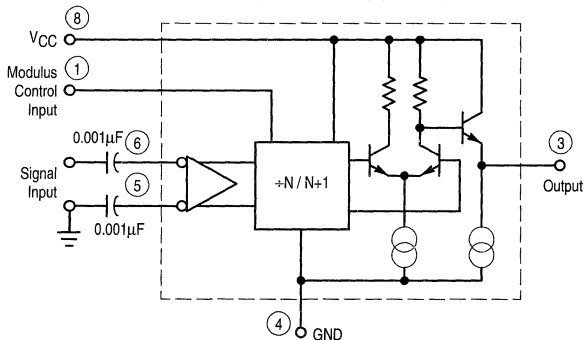
Symbol	Characteristic	Range	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 8	-0.5 to 7.0	Vdc
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +175	°C

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 4.75 to 5.25V; T<sub>A</sub> = -40 to +85°C)

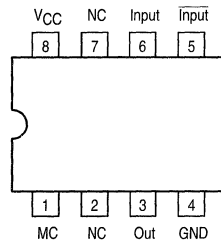
Symbol	Characteristic	Min	Typ	Max	Unit
f <sub>max</sub> f <sub>min</sub>	Toggle Frequency (Sine Wave Input)	520		30	MHz
I <sub>CC</sub>	Supply Current		9.5	11.5	mA
V <sub>IH</sub>	Control Input HIGH (+64)	2.0			V
V <sub>IL</sub>	Control Input LOW (+65)			0.8	V
V <sub>out</sub>	Output Voltage	0.8	1.2		V <sub>pp</sub>
V <sub>in</sub>	Input Voltage Sensitivity 30MHz 100-520MHz	400 100		800 800	mV <sub>pp</sub>
t <sub>PLL</sub>	PLL Response Time <sup>1</sup>			t <sub>out</sub> -42 <sup>2</sup>	ns

1. t<sub>PLL</sub> = The period of time the PLL has from the rising output transition to the Modulus Control input edge transition to ensure proper modulus selection
2. t<sub>out</sub> = Period of output waveform

### PRESCALER BLOCK DIAGRAM



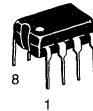
### Pinout: 8-Lead Plastic (Top View)



# MC12025

## MECL PLL COMPONENTS

**÷64/65**  
**DUAL MODULUS**  
**PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



## 1.1GHz Dual Modulus Prescaler

The MC12026 is a high frequency, low voltage dual modulus prescaler used in phase-locked loop (PLL) applications.

The MC12026A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

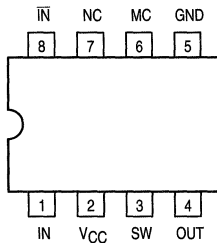
The MC12026B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of an 8/9 or 16/17 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1GHz Toggle Frequency
- Supply Voltage 4.5V to 5.5V
- Low Power 4.0mA Typical
- Operating Temperature Range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- The MC12026 is Pin Compatible With the MC12022
- Short Setup Time ( $t_{\text{set}}$ ) 6ns Typical @ 1.1GHz
- Modulus Control Input Level is Compatible With Standard CMOS and TTL

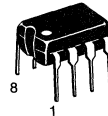
Pinout: 8-Lead Plastic (Top View)



**MC12026A**  
**MC12026B**

**MECL PLL COMPONENTS**

**$\div 8/9, \div 16/17$**   
**DUAL MODULUS PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

**FUNCTION TABLE**

SW	MC	Divide Ratio
H	H	8
H	L	9
L	H	16
L	L	17

Note: SW: H =  $V_{CC}$ , L = OPEN  
MC: H = 2.0V to  $V_{CC}$ ; L = GND to 0.8V

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	$-0.5$ to $+7.0$	Vdc
$T_A$	Operating Temperature Range	$-40$ to $+85$	$^{\circ}\text{C}$
$T_{\text{stg}}$	Storage Temperature Range	$-65$ to $+150$	$^{\circ}\text{C}$
MC	Modulus Control Input, Pin 6	$-0.5$ to $+6.5$	Vdc
$I_O$	Maximum Output Current, Pin 4	10.0	mA





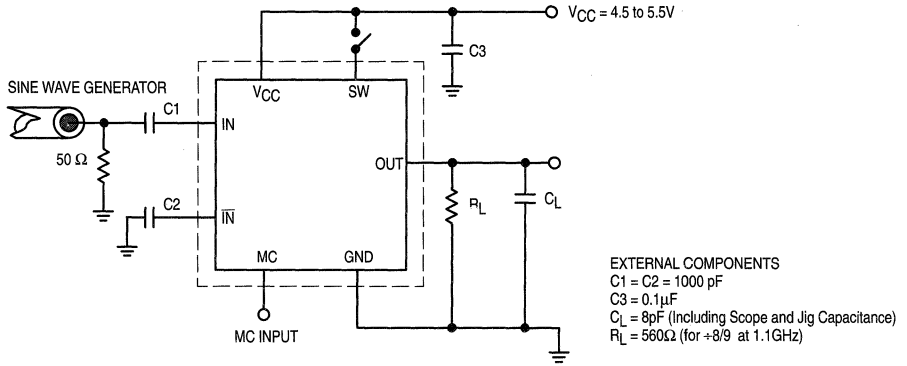


Figure 3. AC Test Circuit

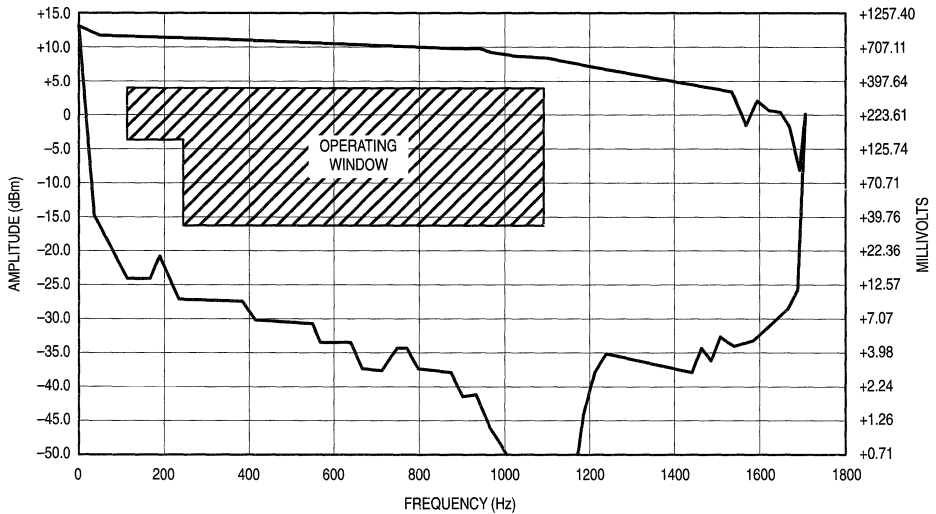


Figure 4. Input Signal Amplitude versus Input Frequency  
 Divide Ratio = 8; V<sub>CC</sub> = 5.0V; T<sub>A</sub> = 25°C

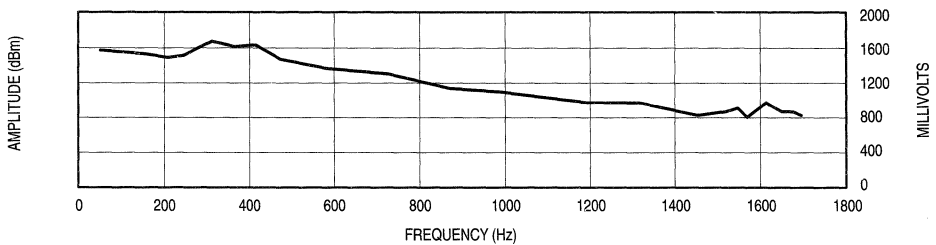
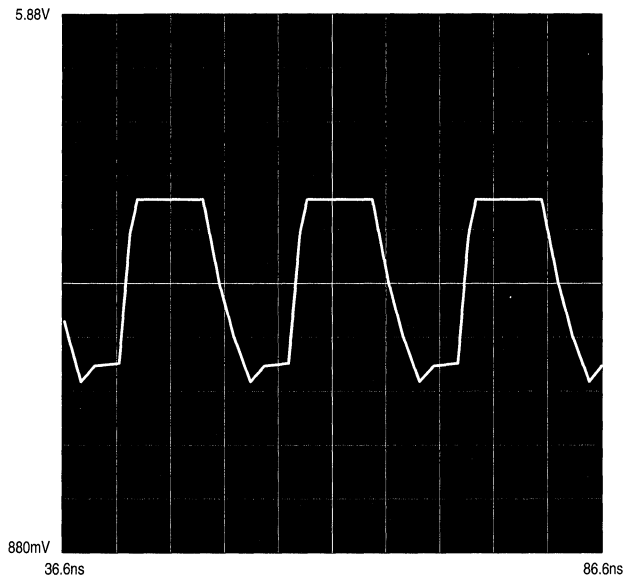


Figure 5. Output Amplitude versus Input Frequency



**Figure 6. Typical Output Waveform**  
(+8, 1.1GHz Input Frequency,  $V_{CC} = 5.0$ ,  $T_A = 25^\circ\text{C}$ , Output Loaded With 8pF)

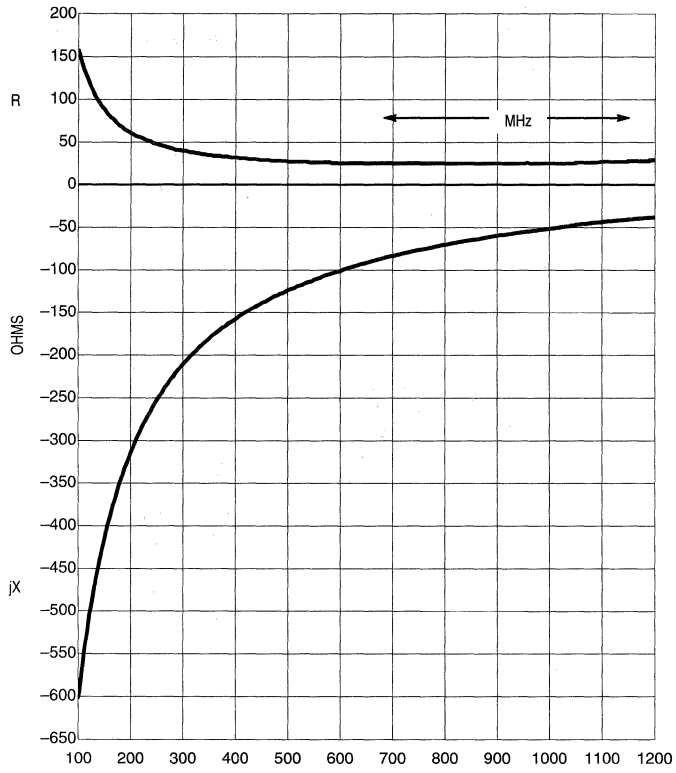


Figure 7. Typical Input Impedance versus Input Frequency

## 1.1GHz Dual Modulus Prescaler

The MC12028A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

The MC12028B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- MC12028A for Positive Edge Triggered Synthesizers
- MC12028B for Negative Edge Triggered Synthesizers
- 6.5mA Maximum,  $-40^{\circ}$  to  $+85^{\circ}$ C,  $V_{CC} = 5.5$ Vdc
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Low-Power 4.0mA Typical

### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

Note: SW: H =  $V_{CC}$ , L = Open

MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V

### DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\* Equivalent to a two-input NAND gate

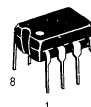
### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	$^{\circ}$ C
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}$ C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

**MC12028A**  
**MC12028B**

### MECL PLL COMPONENTS

**$\div 32/33, \div 64/65$**   
**DUAL MODULUS**  
**PRESCALER**

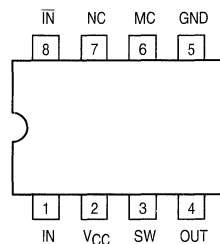


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### Pinout: 8-Lead Plastic (Top View)



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current Output Unloaded (Pin 2)		4.0	6.5	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input Low (MC)			0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
$V_{out}$	Output Voltage Swing ( $C_L = 12pF$ ; $R_L = 2.2k\Omega$ )	1.0	1.6		$V_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out		11	16	ns
$V_{in}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400		1500 1500	mVpp
$I_O$	Output Current ( $C_L = 12pF$ ; $R_L = 2.2k\Omega$ )		1.5	4.0	mA

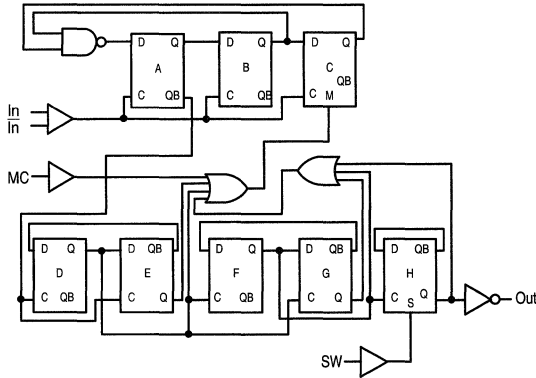
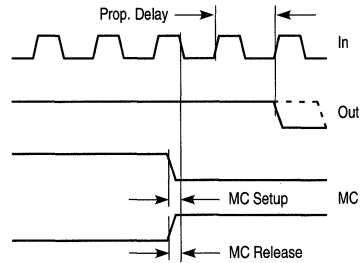


Figure 1. Logic Diagram (MC12028A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

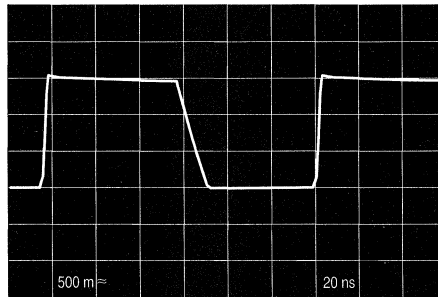


Figure 3. Typical Output Waveform



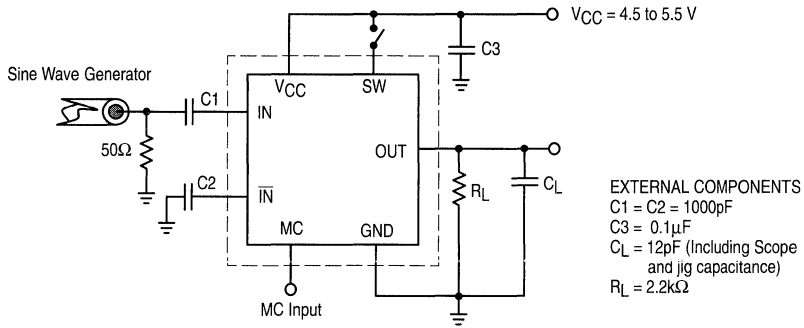


Figure 4. AC Test Circuit

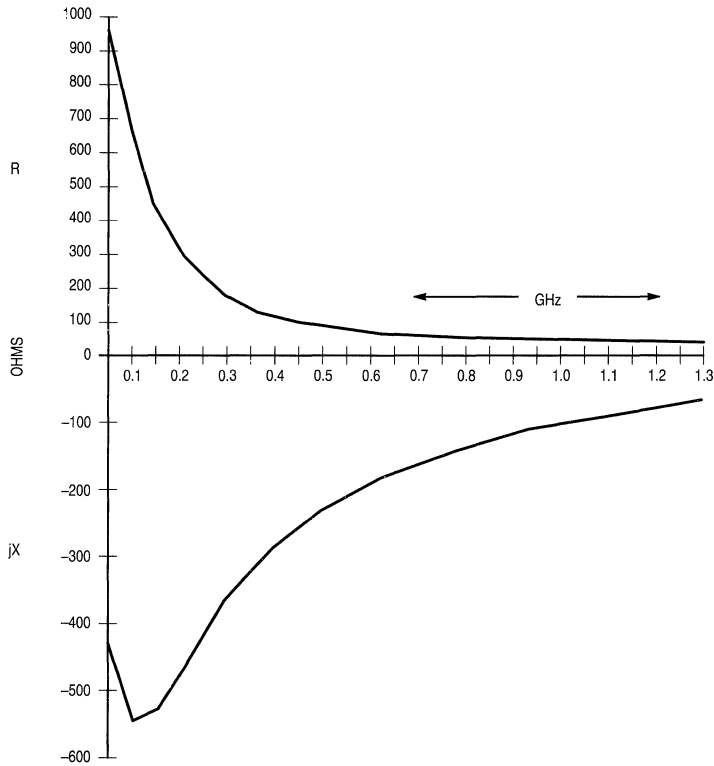
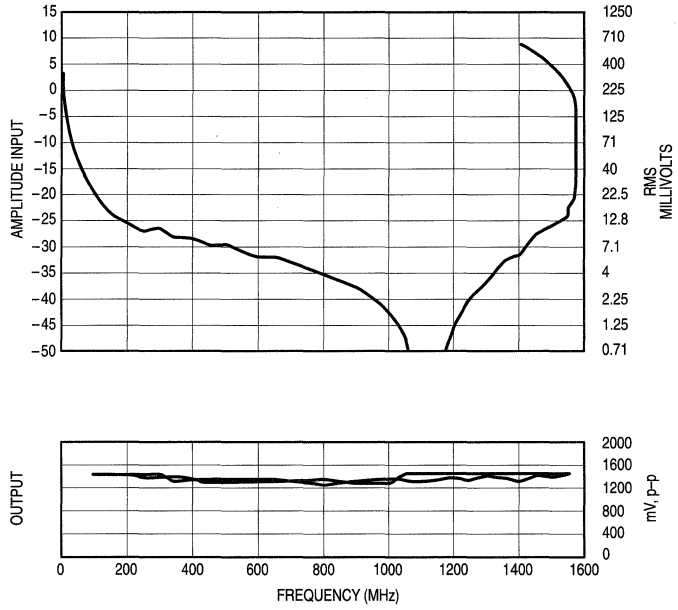


Figure 5. Typical Input Impedance versus Input Frequency



**Figure 6. Input Signal Amplitude versus Input Frequency**  
Divide Ratio = 32

## 2.0GHz Low Voltage Dual Modulus Prescaler

The MC12031 is a high frequency low voltage dual modulus prescaler used in phase-locked loop (PLL) applications. A high frequency input signal up to 2.0GHz is provided for cordless and cellular communication services such as DECT, PHS, and PCS. The MC12031 can be operated down to a minimum supply voltage of 2.7V required for battery operated portable systems.

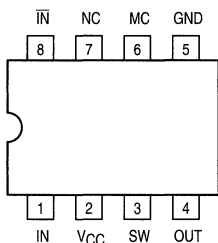
The MC12031A can be used with CMOS synthesizer requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signal up to 2.0GHz in programmable frequency steps. The MC12031B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0GHz Toggle Frequency
- Supply Voltage 2.7V to 5.0Vdc
- Low Power 10.0mA Typical at  $V_{CC} = 2.7V$
- Operating Temperature Range of  $-40$  to  $+85^{\circ}C$
- The MC12031 is Pin and Functionally Compatible With the MC12022
- Short Setup Time ( $t_{set}$ ) 8ns Typical at 2.0GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

**Pinout: 8-Lead Plastic (Top View)**

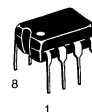


For positive edge triggered synthesizers, order the MC12031A  
For negative edge triggered synthesizers, order the MC12031B

### MC12031A MC12031B

#### MECL PLL COMPONENTS

**-64/65, +128/129  
LOW VOLTAGE  
DUAL MODULUS PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

#### FUNCTION TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H =  $V_{CC}$ , L = OPEN  
MC: H = 2.0V to  $V_{CC}$ ; L = GND to 0.8V

#### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	$-0.5$ to $+7.0$	Vdc
$T_A$	Operating Temperature Range	$-40$ to $+85$	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	$-65$ to $+150$	$^{\circ}C$
MC	Modulus Control Input, Pin 6	$-0.5$ to $+6.5$	Vdc
$I_O$	Maximum Output Current, Pin 4	10.0	mA



# MC12031A MC12031B

## ELECTRICAL CHARACTERISTICS ( $V_{CC} = 2.7$ to $5.0V$ ; $T_A = -40$ to $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave)	0.5	2.4	2.0	GHz
$I_{CC}$	Supply Current Output (Pin 2) $V_{CC} = 2.7V$ $V_{CC} = 5.0V$		10.0 13.0	12.5 16.0	mA
$V_{IH1}$	Modulus Control Input HIGH (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input LOW (MC)	GND		0.8	V
$V_{IH2}$	Divide Ratio Control Input HIGH (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	V
$V_{IL2}$	Divide Ratio Control Input LOW (SW)	OPEN	OPEN	OPEN	—
$V_{OUT}$	Output Voltage Swing (Note 1) $C_L = 8pF$ ; $R_L = 1.2k\Omega$	0.8	1.2		$V_{PP}$
$t_{set}$	Modulus Setup Time MC to OUT @ 2000MHz		8	10	ns
$V_{IN}$	Input Voltage Sensitivity 500–2000MHz	100		1000	mV <sub>PP</sub>
$I_O$	Output Current (Note 2) $V_{CC} = 2.7V$ , $C_L = 8pF$ , $R_L = 1.2k\Omega$ $V_{CC} = 5.0V$ , $C_L = 8pF$ , $R_L = 3.0k\Omega$		1.2 1.2	4.0 4.0	mA

- Valid over voltage range 2.7 to 5.0V;  $R_L = 1.2k\Omega$  @  $V_{CC} = 2.7V$ ;  $R_L = 3.0k\Omega$  @  $V_{CC} = 5.0V$
- Divide ratio of +64/65 @ 2.0GHz

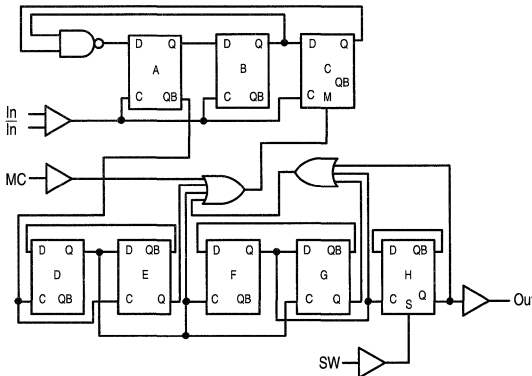


Figure 1. Logic Diagram (MC12031A)

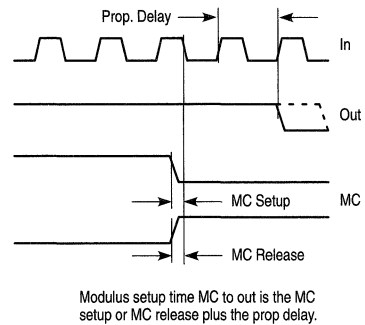
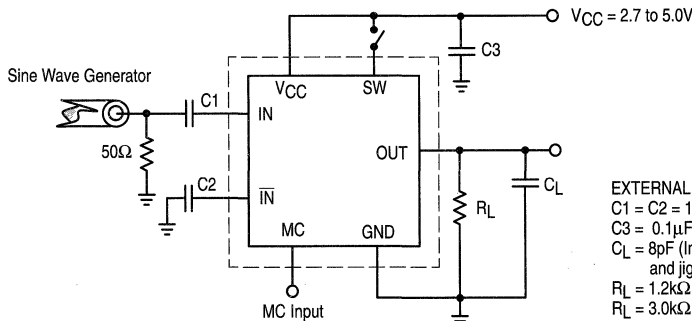
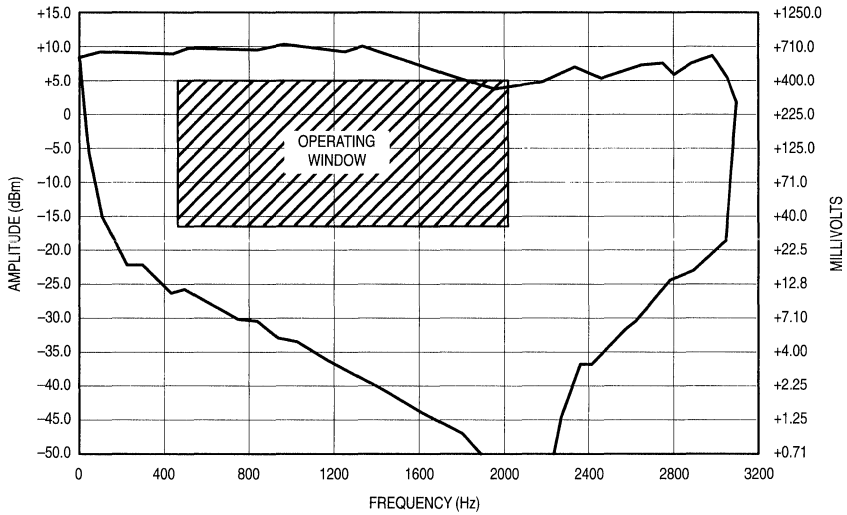


Figure 2. Modulus Setup Time

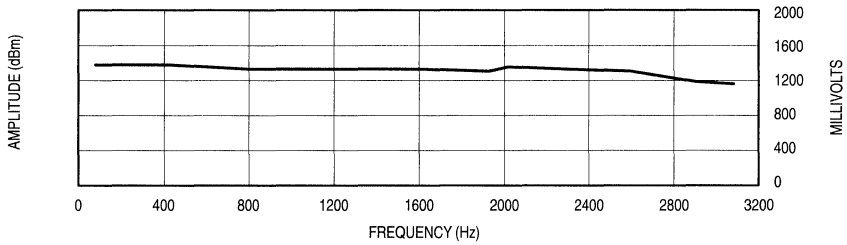


EXTERNAL COMPONENTS  
 $C1 = C2 = 1000pF$   
 $C3 = 0.1\mu F$   
 $C_L = 8pF$  (Including Scope and jig capacitance)  
 $R_L = 1.2k\Omega$  @  $V_{CC} = 2.7V$   
 $R_L = 3.0k\Omega$  @  $V_{CC} = 5.0V$

Figure 3. AC Test Circuit



**Figure 4. Input Signal Amplitude versus Input Frequency**  
 Divide Ratio = 64;  $V_{CC} = 5.0V$ ;  $T_A = 25^{\circ}C$



**Figure 5. Output Amplitude versus Input Frequency**

## 2.0GHz Dual Modulus Prescaler

The MC12032A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0GHz in programmable frequency steps.

The MC12032B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0 GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5V
- MC12032A for Positive Edge Triggered Synthesizers
- MC12032B for Negative Edge Triggered Synthesizers
- 12mA Maximum,  $-40^{\circ}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.5\text{Vdc}$
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- Low-Power 8.5mA Typical

### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H =  $V_{CC}$ , L = Open  
MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V

### DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\* Equivalent to a two-input NAND gate

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

**MC12032A**  
**MC12032B**

### MECL PLL COMPONENTS

**$\div 64/65, \div 128/129$**   
**DUAL MODULUS**  
**PRESCALER**

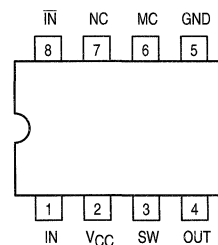


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

Pinout: 8-Lead Plastic (Top View)



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.5	2.4	2.0	GHz
$I_{CC}$	Supply Current Output Unloaded (Pin 2)		8.5	12	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input Low (MC)			0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
$V_{Out}$	Output Voltage Swing ( $C_L = 12pF$ ; $R_L = 2.2k\Omega$ )	1.0	1.6		$\hat{V}_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out		8.0	10	ns
$V_{in(min)}$	Input Voltage Sensitivity 500–2000 MHz	100		1500	mVpp
$I_O$	Output Current ( $C_L = 12pF$ ; $R_L = 2.2k\Omega$ )		1.5	4.0	mA

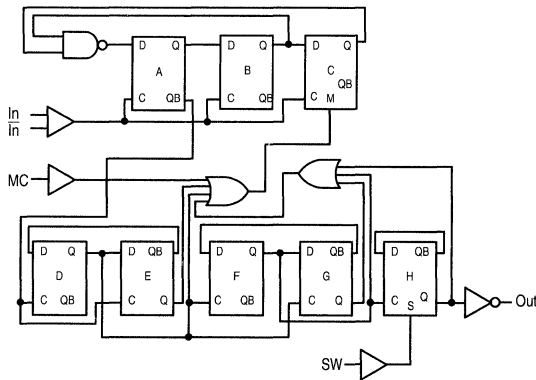


Figure 1. Logic Diagram (MC12032A)

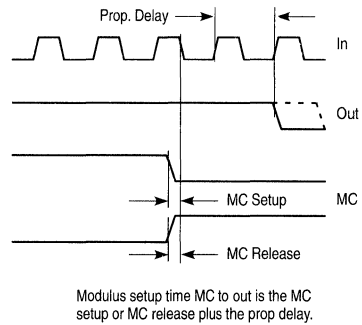
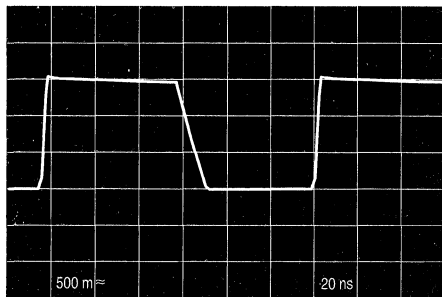
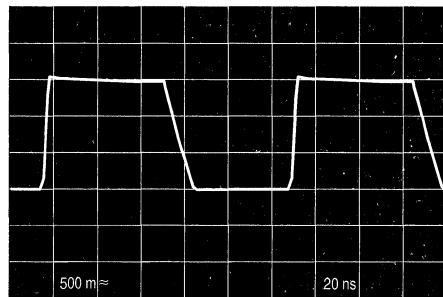


Figure 2. Modulus Setup Time



(+64, 500MHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)

Figure 3. Typical Output Waveforms

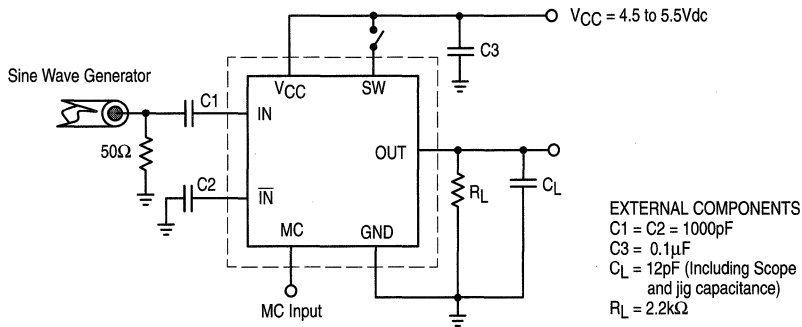


Figure 4. AC Test Circuit

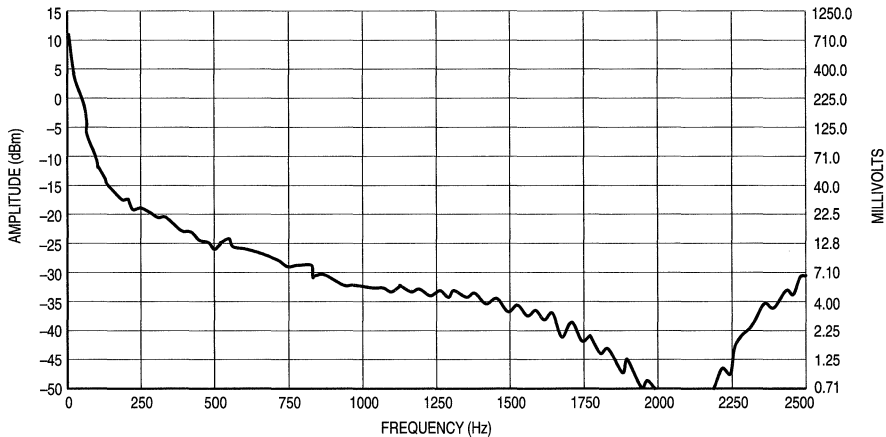


Figure 5. Input Signal Amplitude versus Input Frequency  
 Divide Ratio = 128

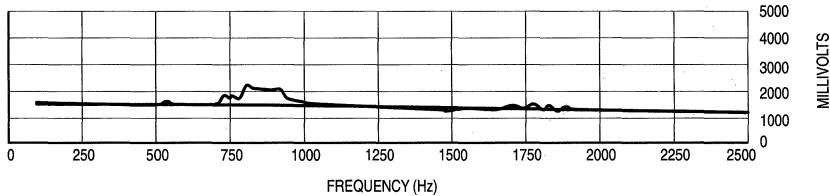


Figure 6. Output Amplitude versus Input Frequency



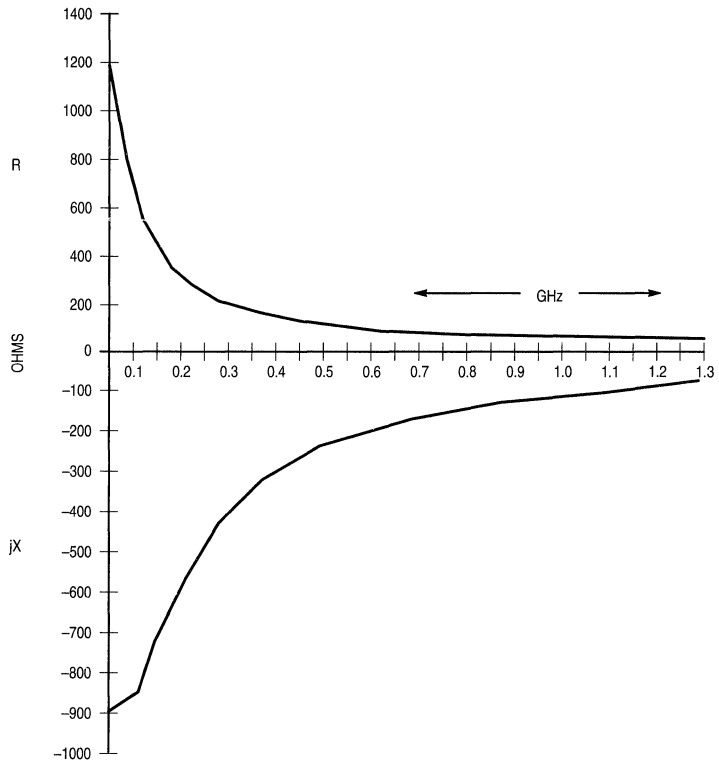


Figure 7. Typical Input Impedance versus Input Frequency

## 2.0GHz Low Voltage Dual Modulus Prescaler

The MC12033 is a high frequency low voltage dual modulus prescaler used in phase-locked loop (PLL) applications. A high frequency input signal up to 2.0GHz is provided for cordless and cellular communication services such as DECT, PHS, and PCS. The MC12033 can be operated down to a minimum supply voltage of 2.7V required for battery operated portable systems.

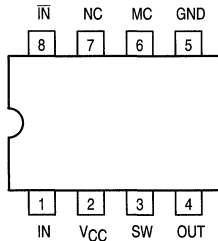
The MC12033A can be used with CMOS synthesizer requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signal up to 2.0GHz in programmable frequency steps. The MC12033B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0GHz Toggle Frequency
- Supply Voltage 2.7V to 5.0Vdc
- Low Power 10.0mA Typical at  $V_{CC} = 2.7V$
- Operating Temperature Range of  $-40$  to  $+85^{\circ}C$
- The MC12033 is Pin Compatible With the MC12022
- Short Setup Time ( $t_{set}$ ) 8ns Typical at 2.0GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

**Pinout: 8-Lead Plastic (Top View)**

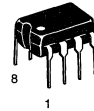


For positive edge triggered synthesizers, order the MC12033A  
For negative edge triggered synthesizers, order the MC12033B

### MC12033A MC12033B

#### MECL PLL COMPONENTS

**+32/33, +64/65  
LOW VOLTAGE  
DUAL MODULUS PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

#### FUNCTION TABLE

SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

Note: SW: H =  $V_{CC}$ , L = OPEN  
MC: H = 2.0V to  $V_{CC}$ ; L = GND to 0.8V

#### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc
$I_O$	Maximum Output Current, Pin 4	10.0	mA



**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.0V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave)	0.5	2.4	2.0	GHz
$I_{CC}$	Supply Current Output (Pin 2) $V_{CC} = 2.7V$ $V_{CC} = 5.0V$		10.0 13.0	12.5 16.0	mA
$V_{IH1}$	Modulus Control Input HIGH (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input LOW (MC)	GND		0.8	V
$V_{IH2}$	Divide Ratio Control Input HIGH (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	V
$V_{IL2}$	Divide Ratio Control Input LOW (SW)	OPEN	OPEN	OPEN	—
$V_{OUT}$	Output Voltage Swing (Note 1) $C_L = 8pF$ ; $R_L = 600\Omega$	0.8	1.2		$V_{PP}$
$t_{set}$	Modulus Setup Time MC to OUT @ 2000MHz		8	10	ns
$V_{IN}$	Input Voltage Sensitivity 500–2000MHz	100		1000	$mV_{PP}$
$I_O$	Output Current (Note 2) $V_{CC} = 2.7V$ , $C_L = 8pF$ , $R_L = 600\Omega$ $V_{CC} = 5.0V$ , $C_L = 8pF$ , $R_L = 1.5k\Omega$		2.4 2.4	4.0 4.0	mA

- Valid over voltage range 2.7 to 5.0V;  $R_L = 600\Omega$  @  $V_{CC} = 2.7V$ ;  $R_L = 1.5k\Omega$  @  $V_{CC} = 5.0V$
- Divide ratio of  $+32/33$  @ 2.0GHz

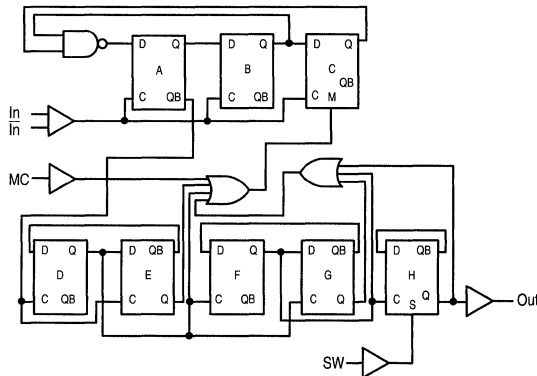
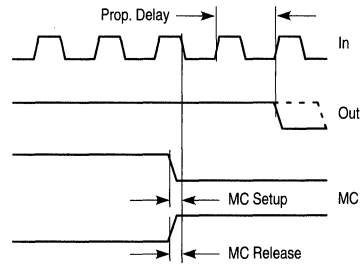


Figure 1. Logic Diagram (MC12033A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time

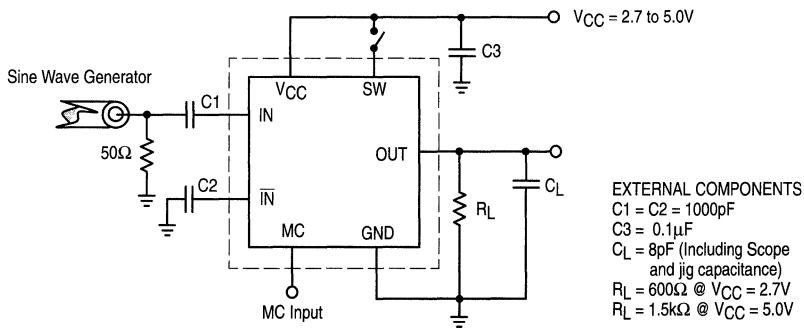
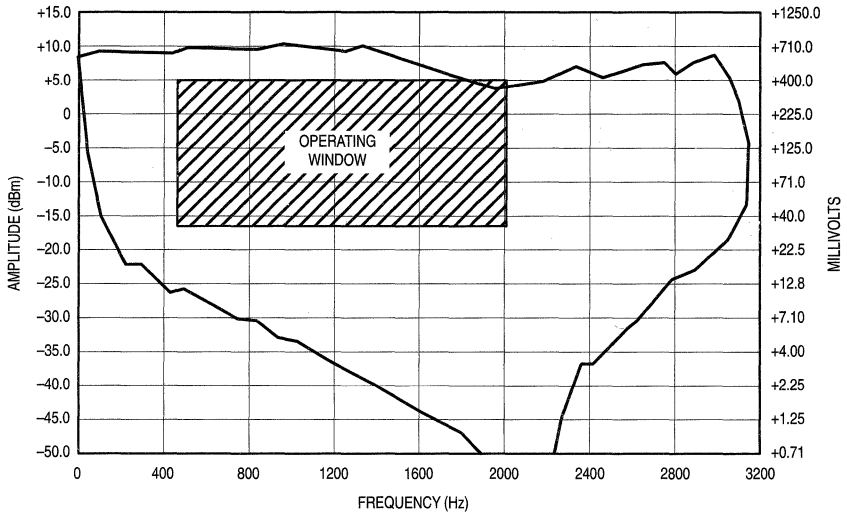
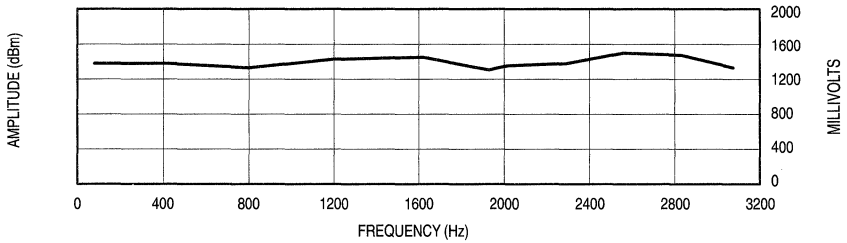


Figure 3. AC Test Circuit



**Figure 4. Input Signal Amplitude versus Input Frequency**  
Divide Ratio = 64;  $V_{CC} = 5.0V$ ;  $T_A = 25^\circ C$



**Figure 5. Output Amplitude versus Input Frequency**

## 2.0GHz Dual Modulus Prescaler

The MC12034A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 2.0GHz in programmable frequency steps.

The MC12034B can be used with CMOS synthesizers requiring negative edges to trigger internal counters such as Fujitsu's MB87001.

A Divide Ratio Control (SW) permits selection of a 32/33 or 64/65 divide ratio as desired.

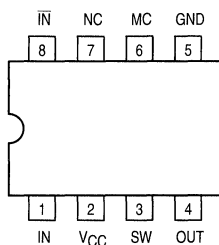
The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0GHz Toggle Frequency
- Supply Voltage 4.5 to 5.5V
- MC12034A for Positive Edge Triggered Synthesizers
- MC12034B for Negative Edge Triggered Synthesizers
- 12mA Maximum,  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5.5\text{Vdc}$
- Modulus Control Input is Compatible with Standard CMOS and TTL
- Low-Power 8.5mA Typical

Design Criteria	Value	Unit
Internal Gate Count *	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\*Equivalent to a two-input NAND gate.

Pinout: 8-Lead Plastic (Top View)



### MAXIMUM RATINGS

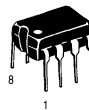
Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

## MC12034A MC12034B

### MECL PLL COMPONENTS

### $\div 32/33$ , $\div 64/65$ DUAL MODULUS PRESCALER



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### FUNCTION TABLE

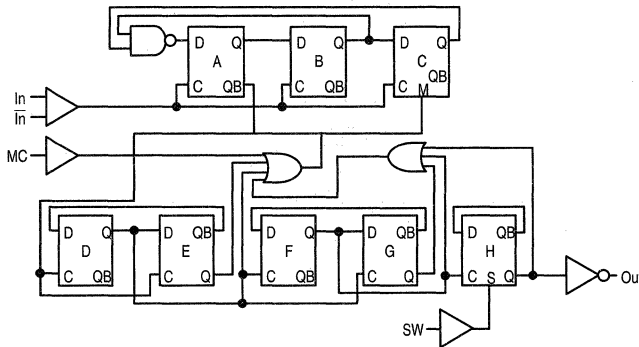
SW	MC	Divide Ratio
H	H	32
H	L	33
L	H	64
L	L	65

Note: SW: H =  $V_{CC}$ , L = OPEN  
MC: H = 2.0V to  $V_{CC}$ , L = GND to 0.8V

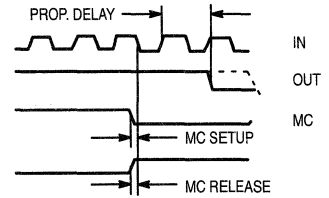


**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5$  Vdc,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave)	0.5	2.4	2.0	GHz
$I_{CC}$	Supply Current Output Unloaded (Pin 2)	—	8.5	12	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0	—	$V_{CC} + 0.5\text{V}$	V
$V_{IL1}$	Modulus Control Input Low (MC)	—	—	0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5\text{V}$	$V_{CC}$	$V_{CC} + 0.5\text{V}$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	OPEN	OPEN	OPEN	—
$V_{out}$	Output Voltage Swing ( $C_L = 12$ pF, $R_L = 1.1$ k $\Omega$ )	1.0	1.6	—	V <sub>p-p</sub>
$t_{SET}$	Modulus Setup Time MC to Out	—	8.0	10.0	ns
$V_{in}$	Input Voltage Sensitivity 500–2000 MHz	100	—	1500	mVpp
$I_O$	Output Current ( $C_L = 12$ pF, $R_L = 1.1$ k $\Omega$ )	—	—	3.5	mA

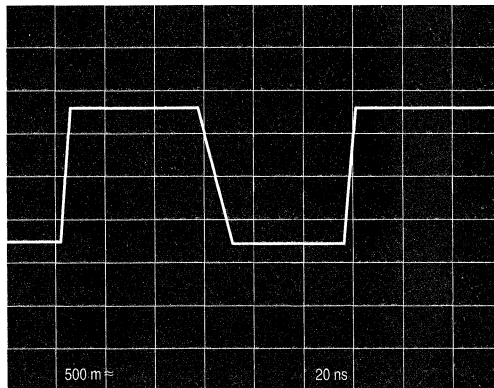


**LOGIC DIAGRAM (MC12034A)**



Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

**Figure 1. Modulus Setup Time**



**Figure 2. Typical Output Waveform**

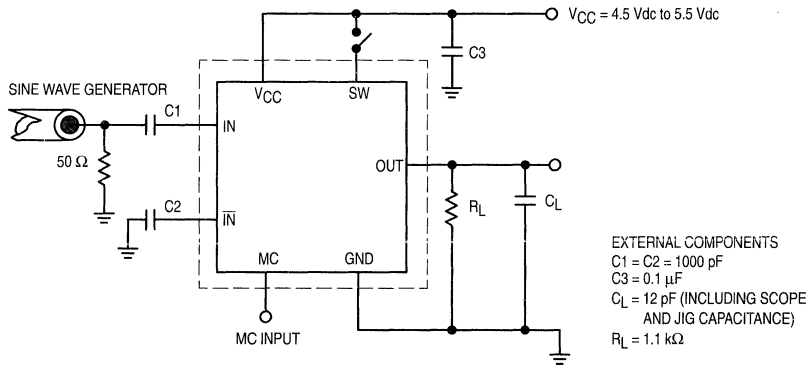


Figure 3. AC Test Circuit

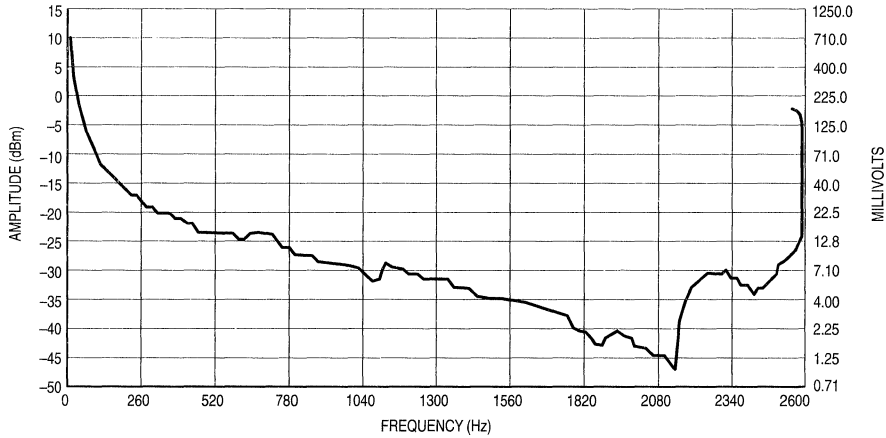


Figure 4. Input Signal Amplitude versus Input Frequency  
 Divide Ratio = 65

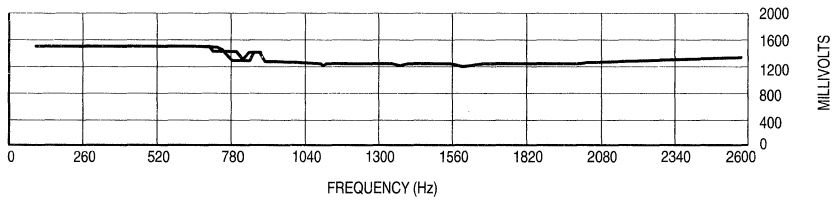


Figure 5. Output Amplitude versus Input Frequency

## 1.1GHz Dual Modulus Prescaler With Stand-By Mode

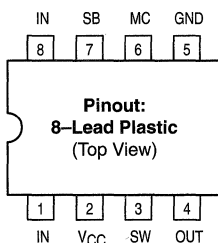
The MC12036 is a 1.1GHz +64/65, +128/129 dual modulus prescaler used in phase-locked loop (PLL) applications. Stand-By mode is featured to reduce current drain to 0.5mA typical when the standby pin (SB) is switched LOW, disabling the prescaler. On-chip output termination provides sufficient output current to drive a 12pF (typical) high impedance load.

The MC12036A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145xxx series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps. The MC12036B can be used with CMOS synthesizers requiring negative edges to trigger internal counters.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1GHz Toggle Frequency
- Low Power 4.0mA Typical
- Stand-By Mode
- On-Chip Output Termination
- Supply Voltage 4.5V to 5.5V
- Operating Temperature Range of -40°C to +85°C
- Short Setup Time ( $t_{set}$ ) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level is Compatible With Standard CMOS and TTL



Design Criteria	Value	Unit
Internal Gate Count *	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\*Equivalent to a two-input NAND gate.

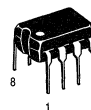
### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

**MC12036A**  
**MC12036B**

### MECL PLL COMPONENTS

**+64/65, +128/129**  
**DUAL MODULUS PRESCALER**  
**WITH STAND-BY MODE**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### FUNCTION TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

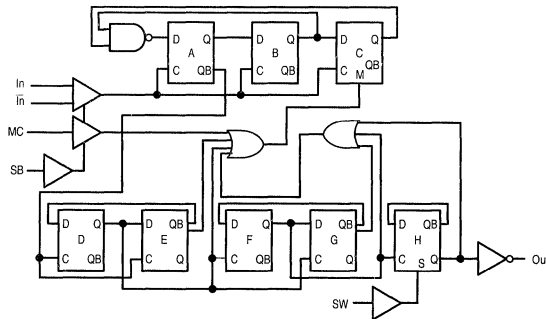
Note: SW: H =  $V_{CC}$ , L = OPEN  
MC: H = 2.0V to  $V_{CC}$ , L = GND to 0.8V



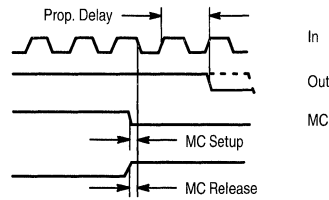


**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5$  Vdc,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current (Pin 2)	—	4.0	6.5	mA
$V_{IH1}$	Modulus Control & Standby Input High (MC & SB)	2.0	—	$V_{CC} + 0.5\text{V}$	V
$V_{IL1}$	Modulus Control & Standby Input Low (MC & SB)	—	—	0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5\text{V}$	$V_{CC}$	$V_{CC} + 0.5\text{V}$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	OPEN	OPEN	OPEN	—
$V_{out}$	Output Voltage Swing, $C_L = 8\text{pF}$	1.0	1.4	—	$V_{p-p}$
$t_{SET}$	Modulus Setup Time MC to Out	—	11	16	ns
$V_{in}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400	— —	1000 1000	mVpp
ISB	Standby Current	—	0.5	—	mA

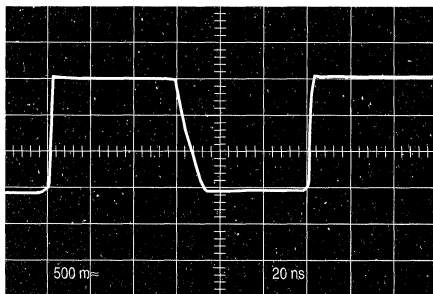


**LOGIC DIAGRAM (MC12036A)**

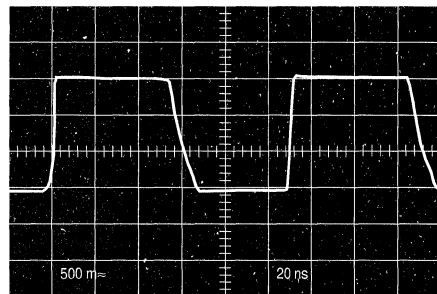


Modulus setup time MC to out is the MC setup or MC release plus the prop. delay.

**Figure 1. Modulus Setup Time**



(+64, 500MHz Input: Frequency,  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ , Output Loaded)



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ , Output Loaded)

**Figure 2. Typical Output Waveform**

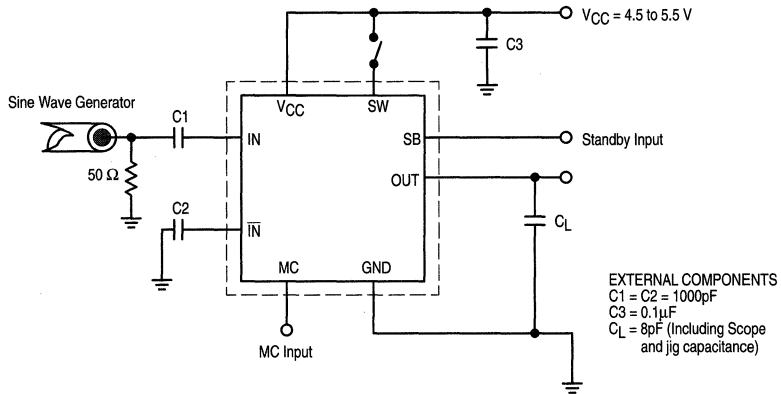


Figure 3. AC Test Circuit

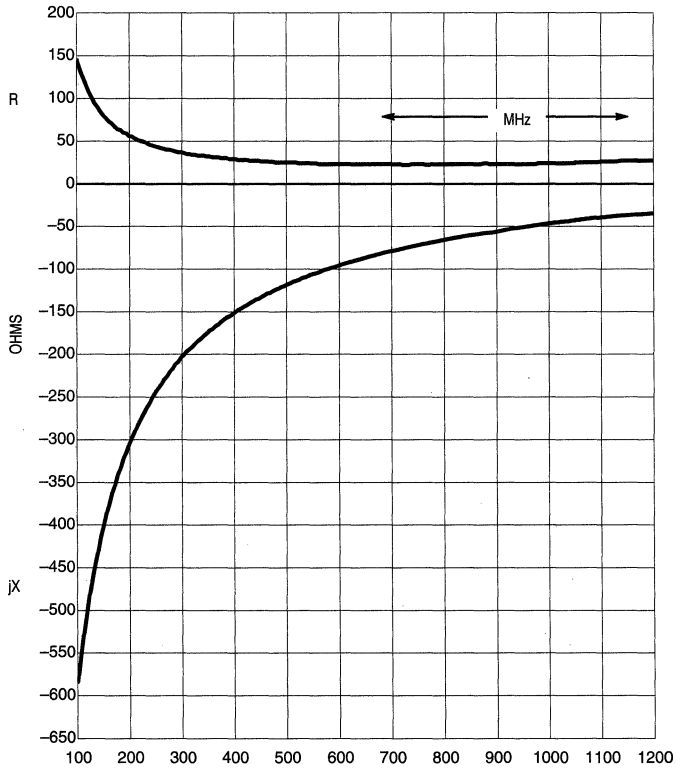


Figure 4. Typical Input Impedance versus Input Frequency

# 1.1GHz Low Power Dual Modulus Prescaler

The MC12038A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 127/128 or 255/256 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1 GHz Toggle Frequency
- Supply Voltage of 4.5 to 5.5V
- Low-Power 4.8mA Typical
- Operating Temperature Range of -40 to +85°C
- Short Setup Time ( $t_{set}$ ) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL
- On-Chip Output Termination

## FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	127
H	L	128
L	H	255
L	L	256

Note: SW: H =  $V_{CC}$ , L = Open

MC: H = 2.0 V to  $V_{CC}$ , L = GND to 0.8 V

## DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	67	ea
Internal Gate Propagation Delay	200	ps
Internal Gate Power Dissipation	0.75	mW
Speed Power Product	0.15	pJ

\* Equivalent to a two-input NAND gate

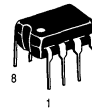
## MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

# MC12038A

## MECL PLL COMPONENTS

$\div 127/128, \div 255/256$   
**DUAL MODULUS  
PRESCALER**

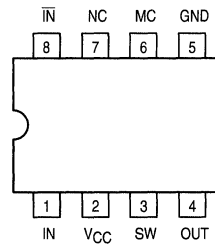


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

## Pinout: 8-Lead Plastic (Top View)



# MC12038A

## ELECTRICAL CHARACTERISTICS ( $V_{CC} = 4.5$ to $5.5V$ ; $T_A = -40^{\circ}C$ to $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current Output Unloaded (Pin 2) at 5.0Vdc		4.8	6.5	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0		$V_{CC} + 0.5V$	V
$V_{IL1}$	Modulus Control Input Low (MC)			0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5V$	$V_{CC}$	$V_{CC} + 0.5V$	Vdc
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
$V_{out}$	Output Voltage Swing ( $C_L = 8pF$ )	1.0	1.6		$V_{p-p}$
$t_{set}$	Modulus Setup Time MC to Out		11	16	ns
$V_{in(min)}$	Input Voltage Sensitivity 250–1100 MHz 100–250 MHz	100 400		1500 1500	mVpp

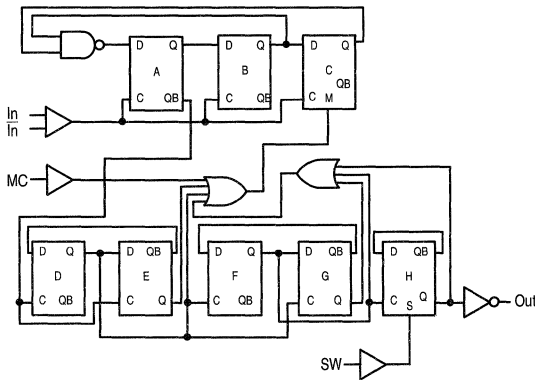


Figure 1. Logic Diagram (MC12038A)

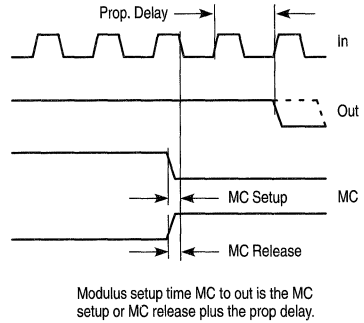
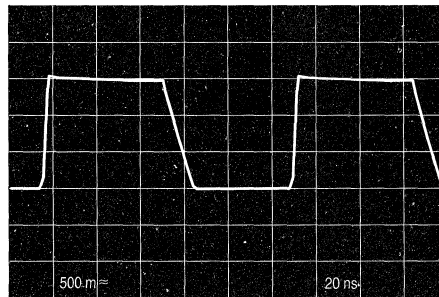


Figure 2. Modulus Setup Time



(+128, 1.1GHz Input Frequency,  $V_{CC} = 5.0V$ ,  $T_A = 25^{\circ}C$ , Output Loaded)

Figure 3. Typical Output Waveforms

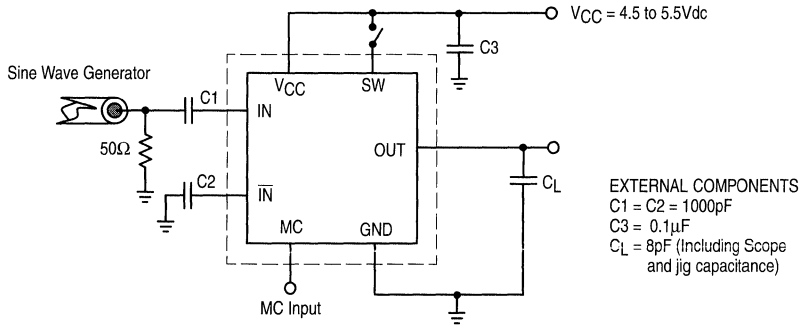


Figure 4. AC Test Circuit

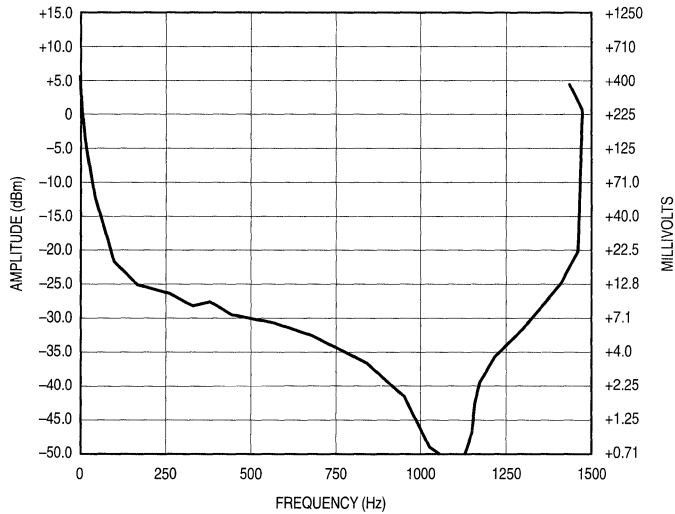


Figure 5. Input Signal Amplitude versus Input Frequency  
 Divide Ratio = 128; VCC = 5.0V; TA = 25°C

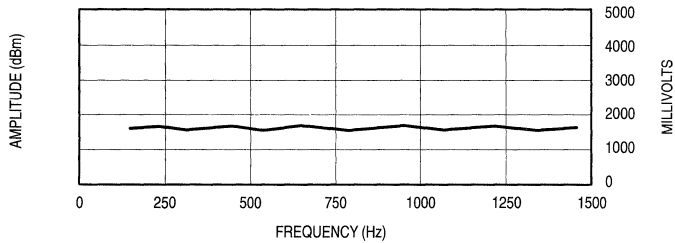


Figure 6. Output Amplitude versus Input Frequency

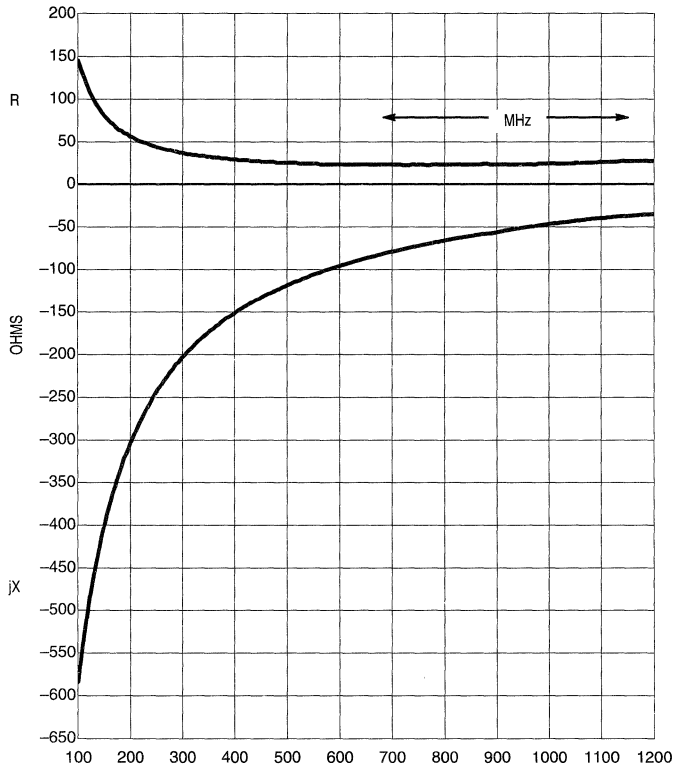


Figure 7. Typical Input Impedance versus Input Frequency

# 1.1GHz Super Low Power Dual Modulus Prescaler

The MC12052A is a super low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 2.7mW at a minimum supply voltage of 2.7V.

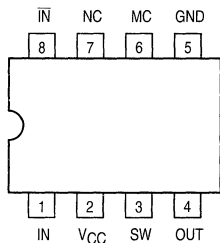
The MC12052A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 1.1GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1GHz Toggle Frequency
- The MC12052 is Pin and Functionally Compatible with the MC12022
- Low Power 1.0mA Typical
- 2.0mA Maximum, -40°C to +85°C, V<sub>CC</sub> = 2.7-5.5 Vdc
- Short Setup Time (t<sub>set</sub>) 16ns Maximum @ 1.1GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5Vdc

**Pinout: 8-Lead Plastic (Top View)**



## MC12052A

### MECL PLL COMPONENTS

÷64/65, ÷128/129  
**LOW POWER  
DUAL MODULUS PRESCALER**



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-02

### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H = V<sub>CC</sub>, L = Open  
MC: H = 2.0V to V<sub>CC</sub>, L = GND to 0.8V

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	Vdc

MOSAIC V is a trademark of Motorola



# MC12052A

## ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 2.7 to 5.5 VDC, T<sub>A</sub> = -40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
f <sub>t</sub>	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
I <sub>CC</sub>	Supply Current (Pin 2)	-	1.0	2.0	mA
V <sub>IH1</sub>	Modulus Control Input High (MC)	2.0	-	V <sub>CC</sub> + 0.5V	V
V <sub>IL1</sub>	Modulus Control Input Low (MC)	GND	-	0.8	V
V <sub>IH2</sub>	Divide Ratio Control Input High (SW)	V <sub>CC</sub> - 0.5V	V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	VDC
V <sub>IL2</sub>	Divide Ratio Control Input Low (SW)	Open	Open	Open	-
V <sub>out</sub>	Output Voltage Swing <sup>2</sup> (C <sub>L</sub> = 8pF, R <sub>L</sub> = 3.3kΩ)	0.8	1.1	-	V <sub>PP</sub>
t <sub>set</sub>	Modulus Setup Time MC to Out @ 1100MHz	-	11	16	ns
V <sub>in</sub>	Input Voltage Sensitivity 250-1100MHz 100-250MHz	100 400	- -	1000 1000	mV <sub>PP</sub>
I <sub>O</sub>	Output Current <sup>1</sup> V <sub>CC</sub> = 2.7V, C <sub>L</sub> = 8pF, R <sub>L</sub> = 3.3kΩ V <sub>CC</sub> = 5.0V, C <sub>L</sub> = 8pF, R <sub>L</sub> = 7.2kΩ	- -	0.5 0.5	3.0 3.0	mA

1. Divide ratio of +64/65 @ 1.1GHz

2. Valid over voltage range 2.7-5.5V; R<sub>L</sub> = 3.3kΩ @ V<sub>CC</sub> = 2.7V; R<sub>L</sub> = 7.2kΩ @ V<sub>CC</sub> = 5.0V

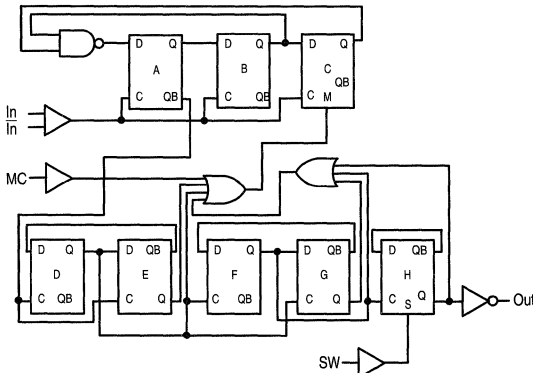
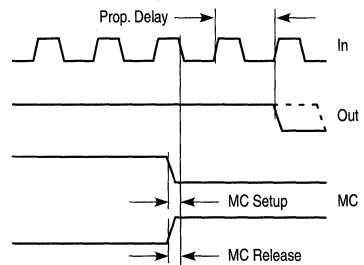
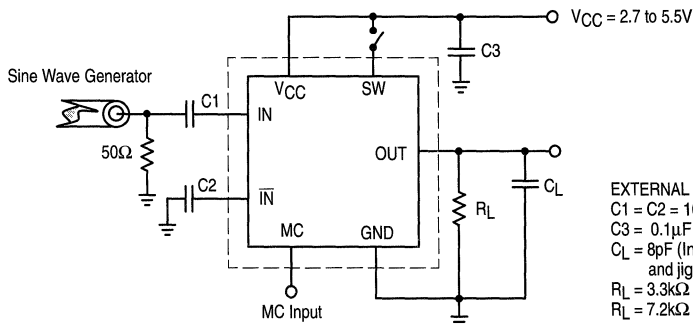


Figure 1. Logic Diagram (MC12052A)



Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

Figure 2. Modulus Setup Time



EXTERNAL COMPONENTS  
 C1 = C2 = 1000pF  
 C3 = 0.1μF  
 C<sub>L</sub> = 8pF (Including Scope  
 and jig capacitance)  
 R<sub>L</sub> = 3.3kΩ @ V<sub>CC</sub> = 2.7V  
 R<sub>L</sub> = 7.2kΩ @ V<sub>CC</sub> = 5.0V

Figure 3. AC Test Circuit



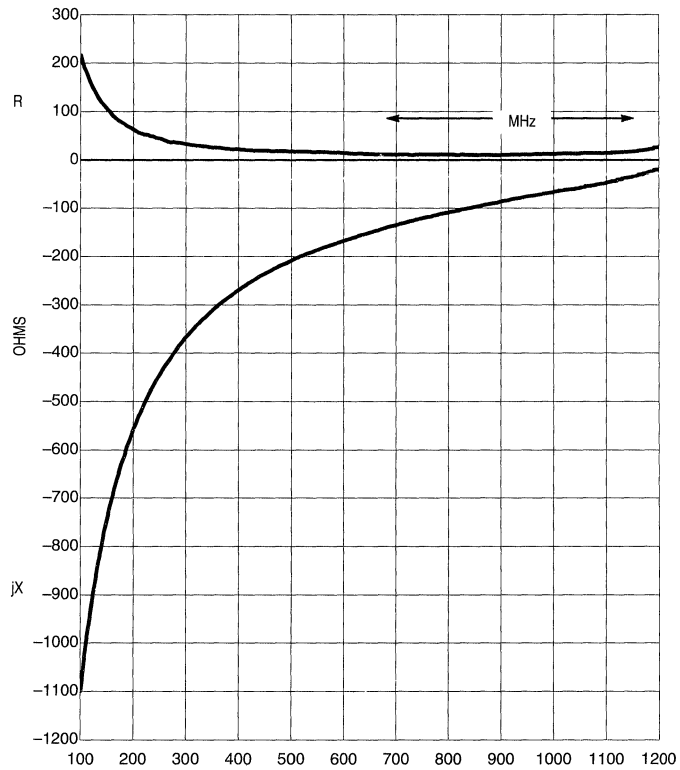


Figure 4. Typical Input Impedance versus Input Frequency

# 1.1GHz Super Low Power Dual Modulus Prescaler With Stand-By Mode

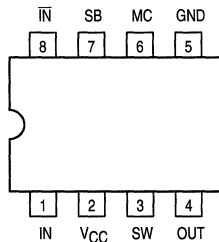
The MC12053A is a super low power +64/65, +128/129 dual modulus prescaler. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 4.3mW at a minimum supply voltage of 2.7V.

The Divide Ratio Control input, SW, permits selection of divide ratio as desired. A HIGH on SW selects +64/65; an OPEN on SW selects +128/129. The Modulus Control input, MC, selects the proper divide number after SW has been biased to select the desired divide ratio.

Stand-by mode is featured to reduce current drain to 50µA typical at 2.7V when the stand-by pin, SB, is switched LOW, disabling the prescaler. On-chip output termination provides 500µA (typical) output current, which is sufficient to drive a CMOS synthesizer input high impedance load (8pF typical).

- 1.1GHz Toggle Frequency
- Supply Voltage of 2.7 to 5.5V
- Low Power 1.5mA Typical at  $V_{CC} = 2.7V$
- Operating Temperature Range of  $-40^{\circ}C$  to  $+85^{\circ}C$
- On-Chip Output Termination
- The MC12053A Is Pin and Functionally Compatible With the MC12036
- Modulus Control Input Level Is Compatible With Standard CMOS and TTL

Pinout: 8-Lead Plastic (Top View)



## MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	Vdc
$T_A$	Operating Temperature Range	-40 to +85	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +150	$^{\circ}C$
MC	Modulus Control Input, Pin 6	-0.5 to + $V_{CC}$	Vdc
$I_O$	Maximum Output Current, Pin 4	4.0	mA

MOSAIC V is a trademark of Motorola

## MC12053A

### MECL PLL COMPONENTS

**+64/65, +128/129  
LOW POWER  
DUAL MODULUS PRESCALER  
WITH STAND-BY MODE**



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-03



**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-02

## FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

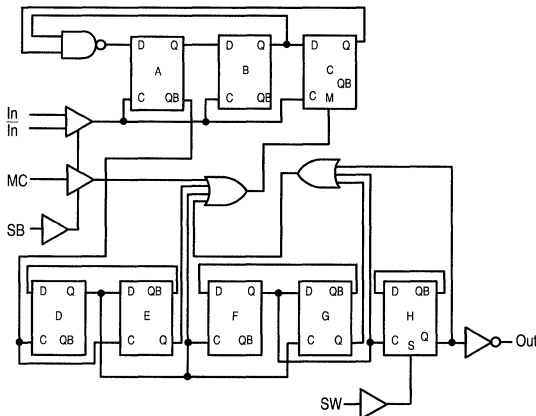
Note: SW: H =  $V_{CC} - 0.5$  to  $V_{CC}$ , L = Open  
MC & SB: H = 2.0 V to  $V_{CC}$ , L = Gnd to 0.8 V



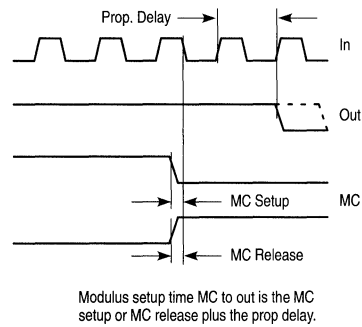
**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7V$  to  $5.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current Output (Pin 2) $V_{CC} = 2.7V$ $V_{CC} = 5.0V$		1.60 1.75	2.5 2.5	mA
$I_{SB}$	Stand-By Current $V_{CC} = 2.7V$ $V_{CC} = 5.0V$		50 100	250 250	$\mu A$
$V_{IH1}$	Modulus Control & Stand-By Input HIGH (MC & SB)	2.0		$V_{CC} + 0.5$	V
$V_{IL1}$	Modulus Control & Stand-By Input LOW (MC & SB)	GND		0.8	V
$V_{IH2}$	Divide Ratio Control Input HIGH (SW)	$V_{CC} - 0.5$	$V_{CC}$	$V_{CC} + 0.5$	V
$V_{IL2}$	Divide Ratio Control Input LOW (SW)	Open	Open	Open	
$V_{out}$	Output Voltage Swing <sup>1</sup>	0.8	1.1	Open	$V_{PP}$
$t_{set}$	Modulus Setup Time MC to OUT at 1100MHz		11	16	ns
$V_{in}$	Input Voltage Sensitivity 250–1100MHz 100–250MHz	100 400		1000 1000	mV <sub>PP</sub>

1. Assumes 8pF high impedance load.

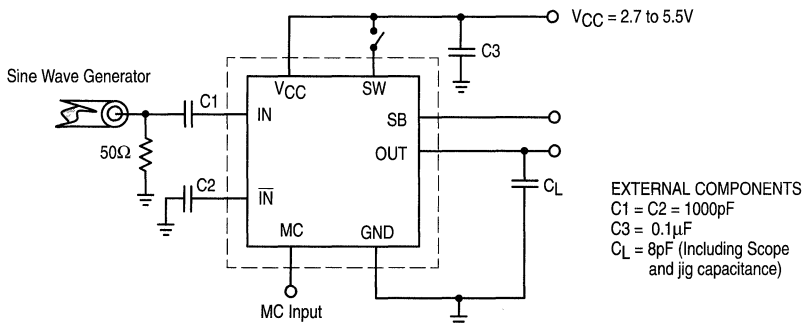


**Figure 1. Logic Diagram (MC12053A)**



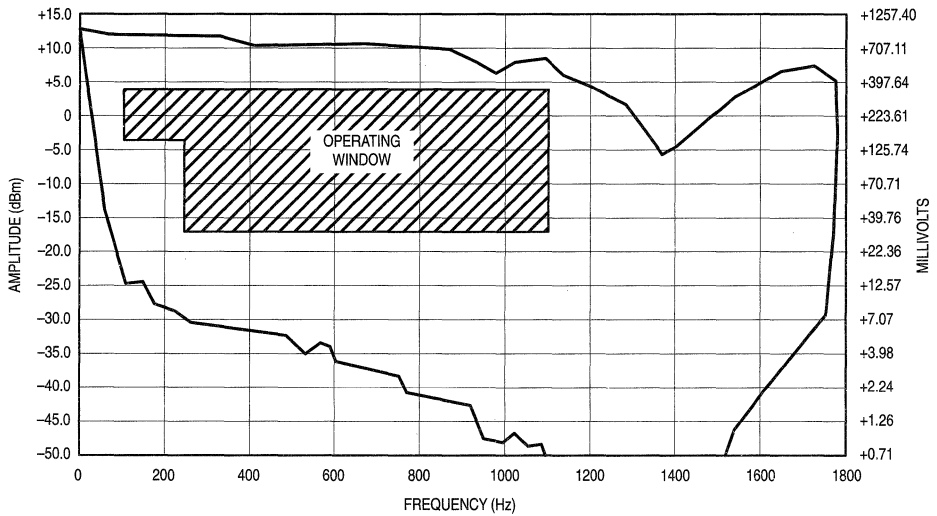
Modulus setup time MC to out is the MC setup or MC release plus the prop delay.

**Figure 2. Modulus Setup Time**

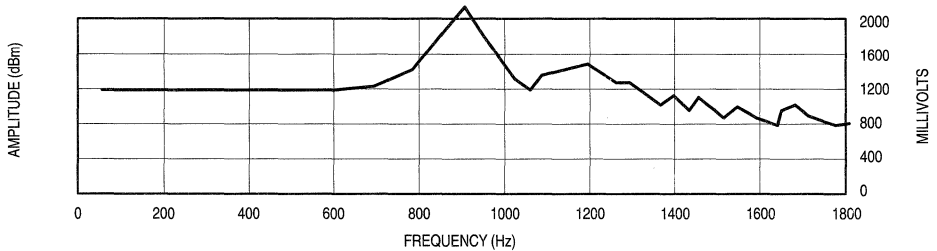


**EXTERNAL COMPONENTS**  
 $C1 = C2 = 1000pF$   
 $C3 = 0.1\mu F$   
 $C_L = 8pF$  (Including Scope and jig capacitance)

**Figure 3. AC Test Circuit**



**Figure 4. Input Signal Amplitude versus Input Frequency**  
 Divide Ratio = 64;  $V_{CC} = 2.7V$ ;  $T_A = 25^{\circ}C$



**Figure 5. Output Amplitude versus Input Frequency**

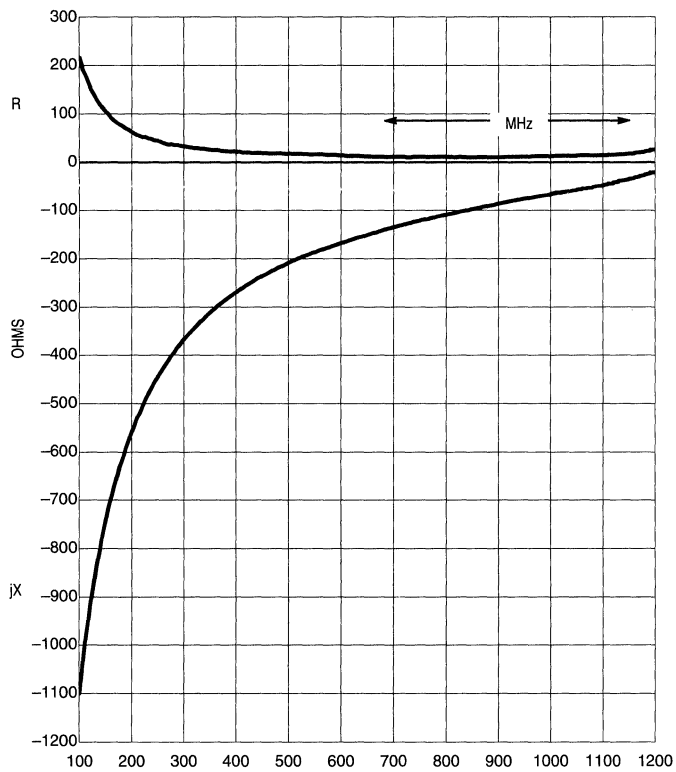


Figure 6. Typical Input Impedance versus Input Frequency

## 2.0GHz Super Low Power Dual Modulus Prescaler

The MC12054A is a super low power dual modulus prescaler used in phase-locked loop applications. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 5.4mW at a minimum supply voltage of 2.7V.

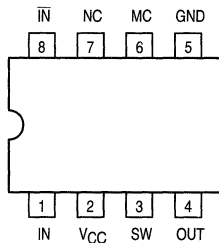
The MC12054A can be used with CMOS synthesizers requiring positive edges to trigger internal counters such as Motorola's MC145XXX series in a PLL to provide tuning signals up to 2.0GHz in programmable frequency steps.

A Divide Ratio Control (SW) permits selection of a 64/65 or 128/129 divide ratio as desired.

The Modulus Control (MC) selects the proper divide number after SW has been biased to select the desired divide ratio.

- 2.0GHz Toggle Frequency
- The MC12054 is Pin and Functionally Compatible with the MC12031
- Low Power 2.0mA Typical
- 2.6mA Maximum, -40°C to +85°C,  $V_{CC} = 2.7-5.5Vdc$
- Short Setup Time ( $t_{set}$ ) 10ns Maximum @ 2.0GHz
- Modulus Control Input Level is Compatible with Standard CMOS and TTL
- Maximum Input Voltage Should Be Limited to 6.5Vdc

**Pinout: 8-Lead Plastic (Top View)**



# MC12054A

## MECL PLL COMPONENTS +64/65, +128/129 LOW POWER DUAL MODULUS PRESCALER



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-02

**FUNCTIONAL TABLE**

SW	MC	Divide Ratio
H	H	64
H	L	65
L	H	128
L	L	129

Note: SW: H =  $V_{CC}$ , L = Open  
MC: H = 2.0V to  $V_{CC}$ , L = GND to 0.8V

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to +7.0	VDC
$T_A$	Operating Temperature Range	-40 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +150	°C
MC	Modulus Control Input, Pin 6	-0.5 to +6.5	VDC

MOSAIC V is a trademark of Motorola

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5$  VDC,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	2.5	2.0	GHz
$I_{CC}$	Supply Current (Pin 2)	–	2.0	2.6	mA
$V_{IH1}$	Modulus Control Input High (MC)	2.0	–	$V_{CC} + 0.5\text{V}$	V
$V_{IL1}$	Modulus Control Input Low (MC)	GND	–	0.8	V
$V_{IH2}$	Divide Ratio Control Input High (SW)	$V_{CC} - 0.5\text{V}$	$V_{CC}$	$V_{CC} + 0.5\text{V}$	VDC
$V_{IL2}$	Divide Ratio Control Input Low (SW)	Open	Open	Open	–
$V_{out}$	Output Voltage Swing <sup>2</sup> ( $C_L = 8\text{pF}$ , $R_L = 1.65\text{k}\Omega$ )	0.8	1.1	–	V <sub>pp</sub>
$t_{set}$	Modulus Setup Time MC to Out @ 2000MHz	–	8	10	ns
$V_{in}$	Input Voltage Sensitivity 250–2000MHz 100–250MHz	100 400	– –	1000 1000	mV <sub>pp</sub>
$I_O$	Output Current <sup>1</sup> $V_{CC} = 2.7\text{V}$ , $C_L = 8\text{pF}$ , $R_L = 1.65\text{k}\Omega$ $V_{CC} = 5.0\text{V}$ , $C_L = 8\text{pF}$ , $R_L = 3.6\text{k}\Omega$	– –	1.0 1.0	4.0 4.0	mA

1. Divide ratio of +64/65 @ 2.0GHz
2. Valid over voltage range 2.7–5.5V;  $R_L = 1.65\text{k}\Omega$  @  $V_{CC} = 2.7\text{V}$ ;  $R_L = 3.6\text{k}\Omega$  @  $V_{CC} = 5.0\text{V}$

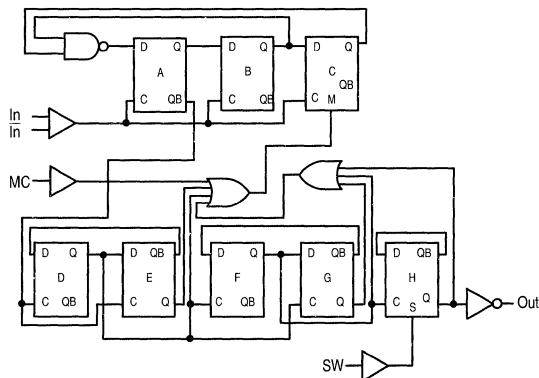


Figure 1. Logic Diagram (MC12054A)

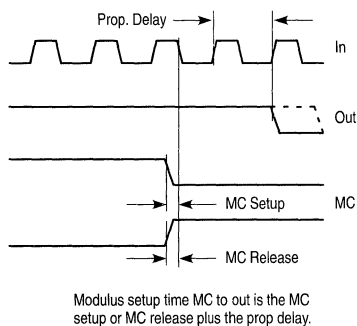


Figure 2. Modulus Setup Time

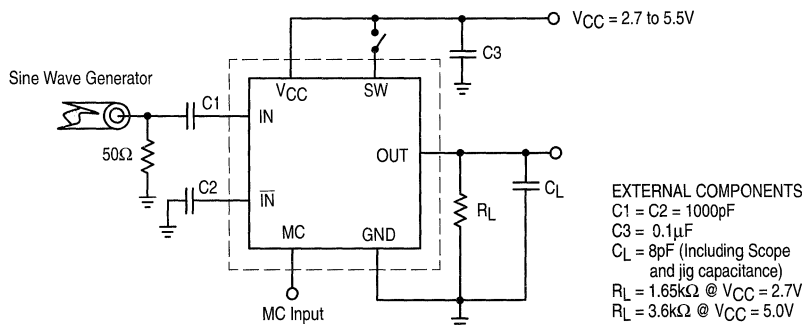


Figure 3. AC Test Circuit

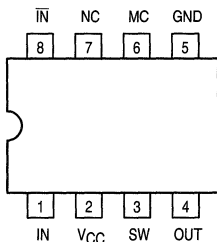
# 1.1GHz Low Power Dual Modulus Prescaler

The MC12058 is a low power +126/128, +254/256 dual modulus prescaler. Motorola's advanced Bipolar MOSAIC™ V technology is utilized to achieve low power dissipation of 3.0mW at a minimum supply voltage of 2.7V. The MC12058 can be operated down to a minimum supply voltage of 2.7V required for battery operated portable systems.

On-chip output termination provides 250µA (typical) output current to drive a 8pF (typical) high impedance load. The Divide Ratio Control input, SW, permits selection of divide ratio as desired. A HIGH on SW selects +126/128; an OPEN on SW selects +254/256. The Modulus Control input, MC, selects the proper divide number after SW has been biased to select the desired divide ratio.

- 1.1GHz Toggle Frequency
- Supply Voltage 2.7V to 5.5V
- Low Power 1.1mA Typical at  $V_{CC} = 3.0V$
- Operating Temperature Range of  $-40^{\circ}C$  to  $+85^{\circ}C$
- On-Chip Output Termination

**Pinout: 8-Lead Plastic (Top View)**



## MC12058

### MECL PLL COMPONENTS ÷126/128, ÷254/256 LOW POWER DUAL MODULUS PRESCALER



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-02

### FUNCTIONAL TABLE

SW	MC	Divide Ratio
H	H	126
H	L	128
L	H	254
L	L	256

Note: SW: H =  $V_{CC}$ , L = Open  
MC: H = 2.0 V to  $V_{CC}$ , L = Gnd to 0.8 V

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	-0.5 to + 7.0	Vdc
$T_A$	Operating Temperature Range	-40 to + 85	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to + 150	$^{\circ}C$
MC	Modulus Control Input, Pin 6	-0.5 to + $V_{CC}$	Vdc
$I_O$	Maximum Output Current, Pin 4	4.0	mA

MOSAIC V is a trademarks of Motorola.





**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7V$  to  $5.5V$ ;  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave Input)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current Output (Pin 2)		1.1	2.0	mA
$V_{IH1}$	Modulus Control Input HIGH (MC)	2.0		$V_{CC} + 0.5$	V
$V_{IL1}$	Modulus Control Input LOW (MC)	GND		0.8	V
$V_{IH2}$	Divide Ratio Control Input HIGH (SW)	$V_{CC} - 0.5$	$V_{CC}$	$V_{CC} + 0.5$	V
$V_{IL2}$	Divide Ratio Control Input LOW (SW)	Open	Open	Open	
$V_{out}$	Output Voltage Swing <sup>1</sup>	0.8	1.1		$V_{PP}$
$t_{set}$	Modulus Setup Time MC to OUT at 1100MHz		11	16	ns
$V_{in}$	Input Voltage Sensitivity	250-1100MHz 100-250MHz	100	1000 1000	mV <sub>PP</sub>

1. Assumes 8pF high impedance load.

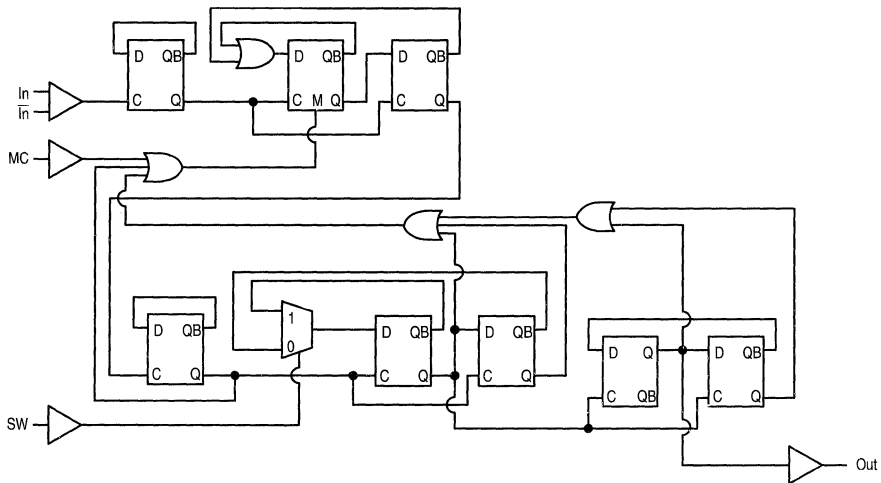
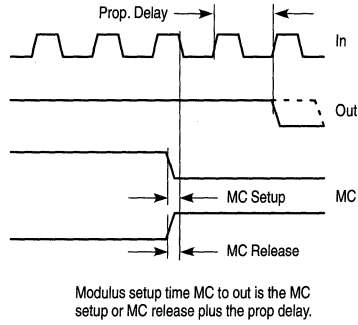
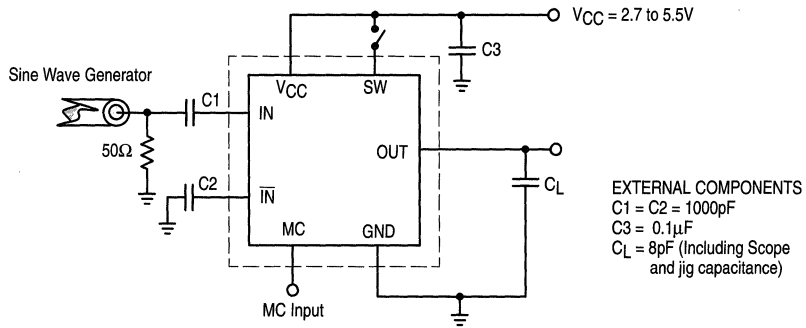


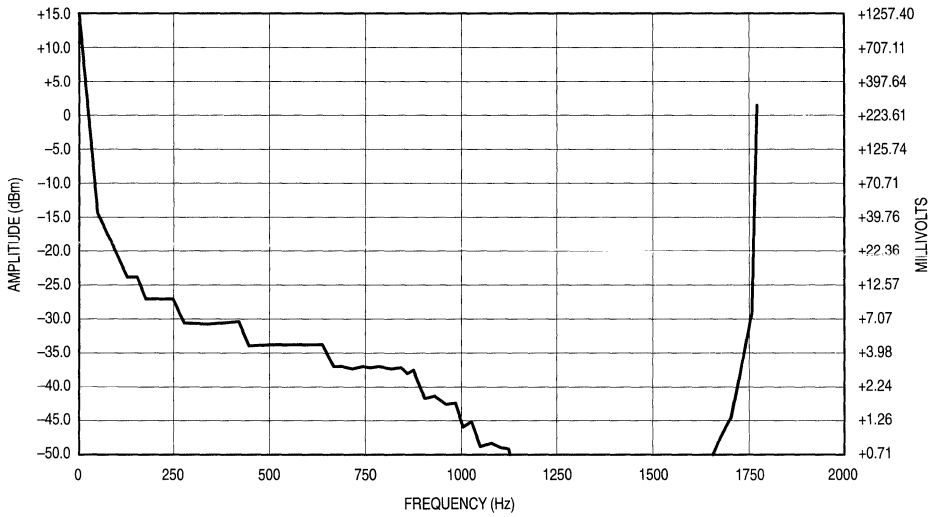
Figure 1. Logic Diagram (MC12058)



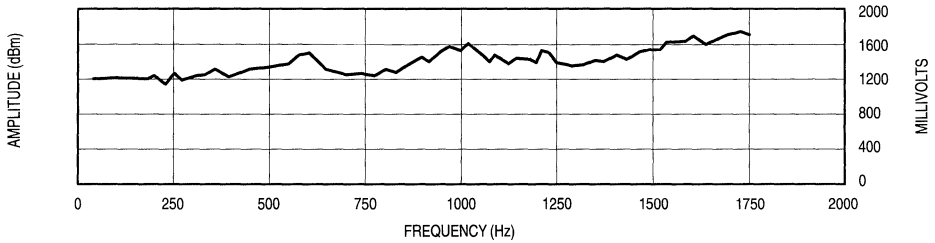
**Figure 2. Modulus Setup Time**



**Figure 3. AC Test Circuit**



**Figure 4. Input Signal Amplitude versus Input Frequency**  
 Divide Ratio = 126; V<sub>CC</sub> = 5.5V; T<sub>A</sub> = 25°C



**Figure 5. Output Amplitude versus Input Frequency**

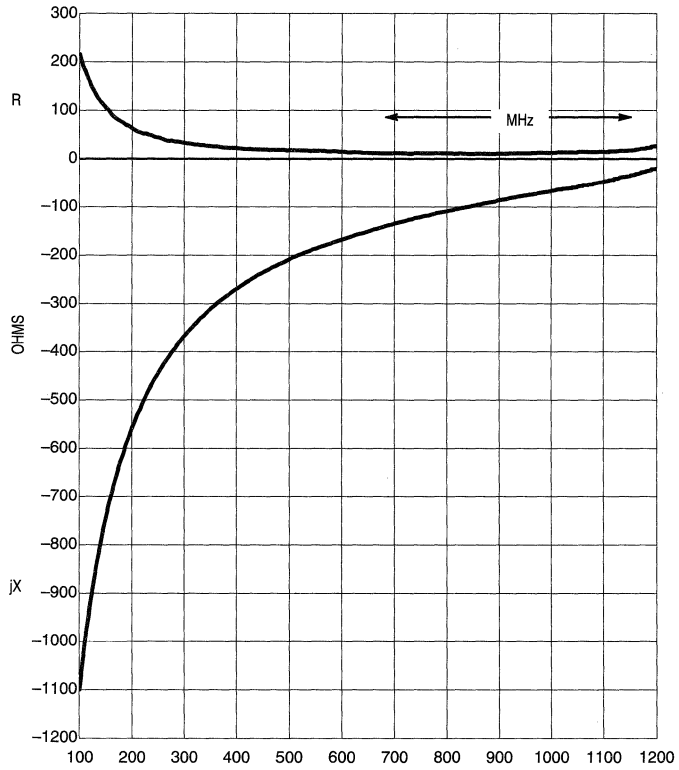


Figure 6. Typical Input Impedance versus Input Frequency

## 1.1GHz Prescaler

The MC12073 is a divide by 64 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential PECL outputs are provided.

- 1.1GHz Toggle Frequency
- Operating Supply Voltage of 4.5 to 5.5V
- Low-Power 23mA Typical at  $V_{CC} = 5.0V$
- High Input Sensitivity,  $20mV_{RMS}$  at  $V_{CC} = 5.0 \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$
- 800mV Minimum Peak-to-Peak Output Swing
- Differential PECL Outputs

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage	7.0	Vdc
$T_A$	Operating Temperature Range	0 to +70	$^\circ C$
$T_{stg}$	Storage Temperature Range	-65 to +175	$^\circ C$

### ELECTRICAL CHARACTERISTICS ( $V_{CC} = 4.5$ to $5.5V$ ; $T_A = 0$ to $+70^\circ C$ )

Symbol	Characteristic	Min	Typ*	Max	Unit
$f_{max}$ $f_{min}$	Toggle Frequency (Sine Wave Input)	1.1	1.3	90	GHz MHz
$I_{CC}$	Supply Current at 5.5V		23	30	mA
$V_{out}$	Output Voltage (Load = 10pF)	0.8	1.2		$V_{PP}$
$V_{in min}$	Input Voltage Sensitivity 150-1100MHz 90MHz		10	20 30	$mV_{RMS}$
$V_{in max}$	Input Overload	200	400		$mV_{RMS}$

\* Typical measured at  $+25^\circ C$ , 5.0V

1. See Figure 1

## MC12073

### MECL PLL COMPONENTS

**-64  
PRESCALER**



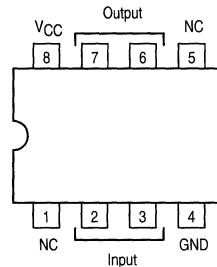
**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05

1

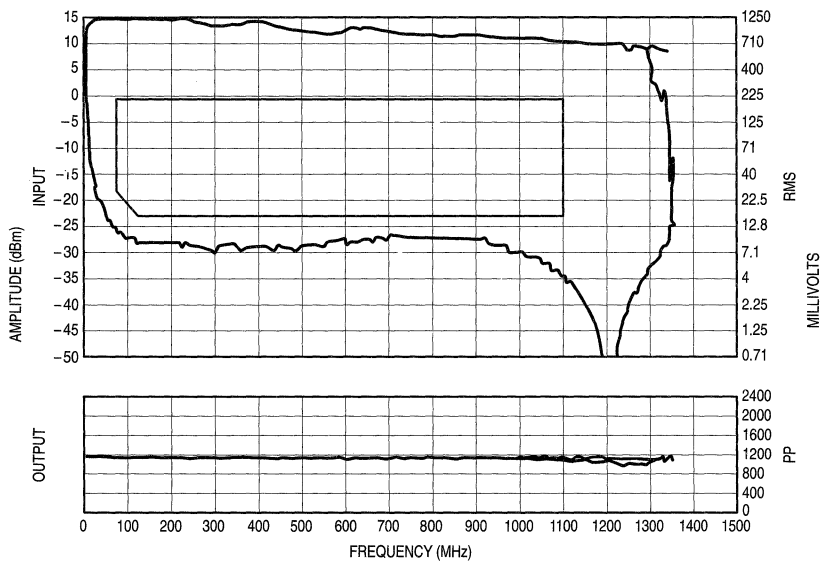
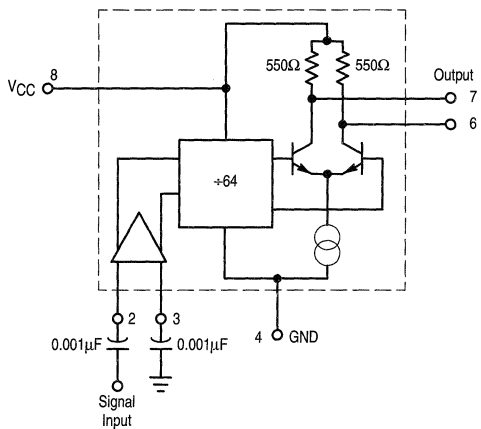
**D SUFFIX**  
PLASTIC SOIC PACKAGE 8  
CASE 751-05



### Pinout: 8-Lead Plastic (Top View)



**PRESCALER BLOCK DIAGRAM**



**Figure 1. Divide Ratio = 64**  
 (Maximum Toggle Frequency: Min = 1348, Mean = 1348, Max = 1348  
 Temp = 25°C, V<sub>CC</sub> = 5.0V, Number of Devices = 1, I<sub>CC</sub> (mA) = 22.51)

## 1.1GHz Prescaler

The MC12074 is a divide by 256 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential PECL outputs are provided.

- 1.1GHz Toggle Frequency
- Operating Supply Voltage of 4.5 to 5.5V
- Low-Power 23mA Typical at  $V_{CC} = 5.0V$
- High Input Sensitivity,  $20mV_{rms}$  at  $V_{CC} = 5.0 \pm 10\%$ ,  $T_A = 0^\circ C$  to  $+70^\circ C$
- 800mV Minimum Peak-to-Peak Output Swing
- Differential PECL Outputs

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage	7.0	Vdc
$T_A$	Operating Temperature Range	0 to +70	$^\circ C$
$T_{stg}$	Storage Temperature Range	-65 to +175	$^\circ C$

### ELECTRICAL CHARACTERISTICS ( $V_{CC} = 4.5$ to $5.5V$ ; $T_A = 0$ to $+70^\circ C$ )

Symbol	Characteristic	Min	Typ*	Max	Unit
$f_{max}$ $f_{min}$	Toggle Frequency (Sine Wave Input)	1.1	1.3	90	GHz MHz
$I_{CC}$	Supply Current at 5.5V		23	30	mA
$V_{out}$	Output Voltage (Load = 10pF)	0.8	1.2		$V_{PP}$
$V_{in min}$	Input Voltage Sensitivity 150-1100MHz 90MHz		10	20 30	$mV_{rms}$
$V_{in max}$	Input Overload	200	400		$mV_{rms}$

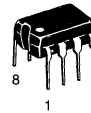
\* Typical measured at  $+25^\circ C$ , 5.0V

1. See Figure 1

## MC12074

### MECL PLL COMPONENTS

$\div 256$   
**PRESCALER**

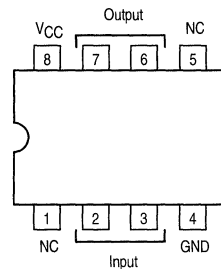


**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 626-05

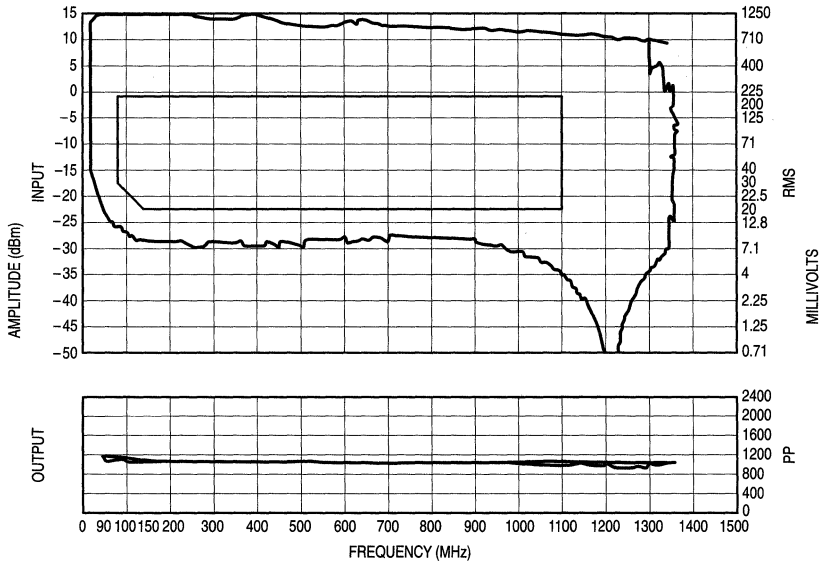
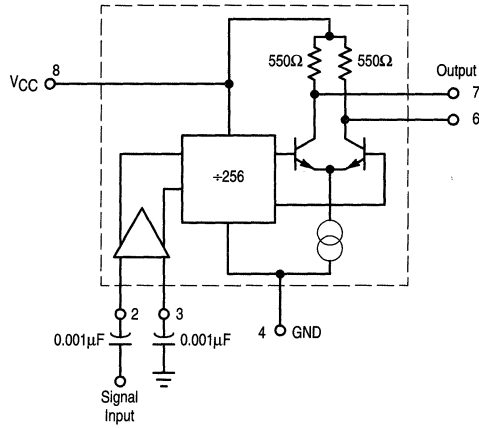


**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751-04

### Pinout: 8-Lead Plastic (Top View)



PRESCALER BLOCK DIAGRAM



**Figure 1. Divide Ratio = 256**  
 (Maximum Toggle Frequency: Min = 1357, Mean = 1357, Max = 1357  
 Temp = 25°C, V<sub>CC</sub> = 5.0V, Number of Devices = 1)



## 1.3GHz Prescaler

The MC12075 is a divide by 64 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential PECL outputs are provided.

The MC12075 is pin and functionally compatible with the Plessey SP4633.

- 1.3GHz Toggle Frequency
- Operating Supply Voltage of 4.5 to 5.5V
- Low-Power 36mA Typical at  $V_{CC} = 5.0V$
- Operating Temperature Range of  $0^{\circ}C$  to  $+85^{\circ}C$
- High Input Sensitivity
- 800mV Minimum Peak-to-Peak Output Swing
- Differential PECL Outputs

### DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	62	ea
Internal Gate Propagation Delay	250	ps
Internal Gate Power Dissipation	10	mW
Speed Power Product	2.5	pJ

\* Equivalent to a two-input NAND gate

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage	7.0	Vdc
$T_A$	Operating Temperature Range	0 to +85	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	-65 to +175	$^{\circ}C$

### ELECTRICAL CHARACTERISTICS ( $V_{CC} = 4.5$ to $5.5V$ ; $T_A = 0$ to $+85^{\circ}C$ )

Symbol	Characteristic	Min	Typ*	Max	Unit
$f_{max}^1$ $f_{min}$	Toggle Frequency (Sine Wave Input)	1.3	1.6	70	GHz MHz
$I_{CC}$	Supply Current at 5.5V		36	50	mA
$V_{out}$	Output Voltage (Load = 10pF)	0.8	1.2		$V_{pp}$
$V_{in min}$	Input Voltage Sensitivity		10 1.0 1.5 3.0	20 4.0 15 20	$mV_{rms}$
$V_{in max}$	Input Overload	400			$mV_{rms}$

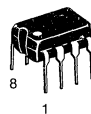
\* Typical measured at  $+25^{\circ}C$ , 5.0V

1. See Figure 1

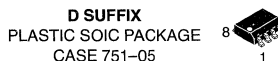
## MC12075

### MECL PLL COMPONENTS

**-64  
PRESCALER**

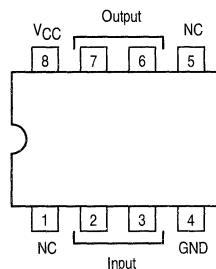


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05

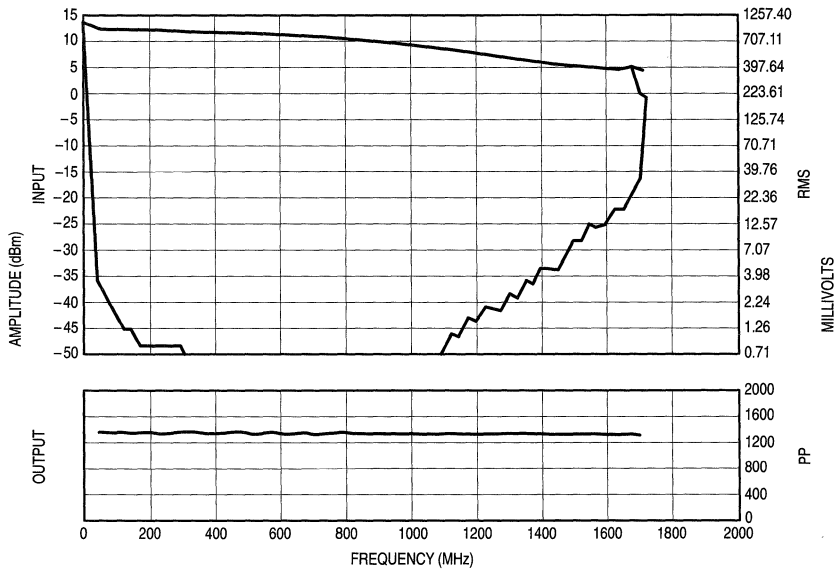
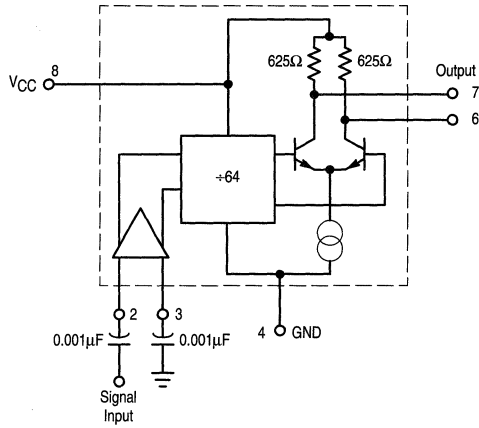


**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### Pinout: 8-Lead Plastic (Top View)



**PRESCALER BLOCK DIAGRAM**



**Figure 1. Typical MC12075 Input Signal Amplitude versus Input Frequency**

## 1.3GHz Prescaler

The MC12076 is a divide by 256 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential PECL outputs are provided.

- 1.3GHz Toggle Frequency
- Operating Supply Voltage of 4.5 to 5.5V
- Low-Power 36mA Typical at  $V_{CC} = 5.0V$
- Operating Temperature Range of 0°C to +85°C
- High Input Sensitivity
- 800mV Minimum Peak-to-Peak Output Swing
- Differential PECL Outputs

### DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	62	ea
Internal Gate Propagation Delay	250	ps
Internal Gate Power Dissipation	10	mW
Speed Power Product	2.5	pJ

\* Equivalent to a two-input NAND gate

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage	7.0	Vdc
$T_A$	Operating Temperature Range	0 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +175	°C

### ELECTRICAL CHARACTERISTICS ( $V_{CC} = 4.5$ to $5.5V$ ; $T_A = 0$ to $+85^\circ C$ )

Symbol	Characteristic	Min	Typ*	Max	Unit
$f_{max}$ <sup>1</sup> $f_{min}$	Toggle Frequency (Sine Wave Input)	1.3	1.6	70	GHz MHz
$I_{CC}$	Supply Current at 5.5V		36	50	mA
$V_{out}$	Output Voltage (Load = 10pF)	0.8	1.2		$V_{PP}$
$V_{in min}$	Input Voltage Sensitivity		10 1.0 1.5 3.0	20 4.0 15 20	mV <sub>rms</sub>
$V_{in max}$	Input Overload	400			mV <sub>rms</sub>

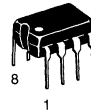
\* Typical measured at +25°C, 5.0V

1. See Figure 1

## MC12076

### MECL PLL COMPONENTS

#### ÷256 PRESCALER

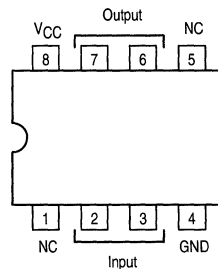


**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05

**D SUFFIX**  
PLASTIC SOIC PACKAGE CASE 751-04



### Pinout: 8-Lead Plastic (Top View)



PRESCALER BLOCK DIAGRAM

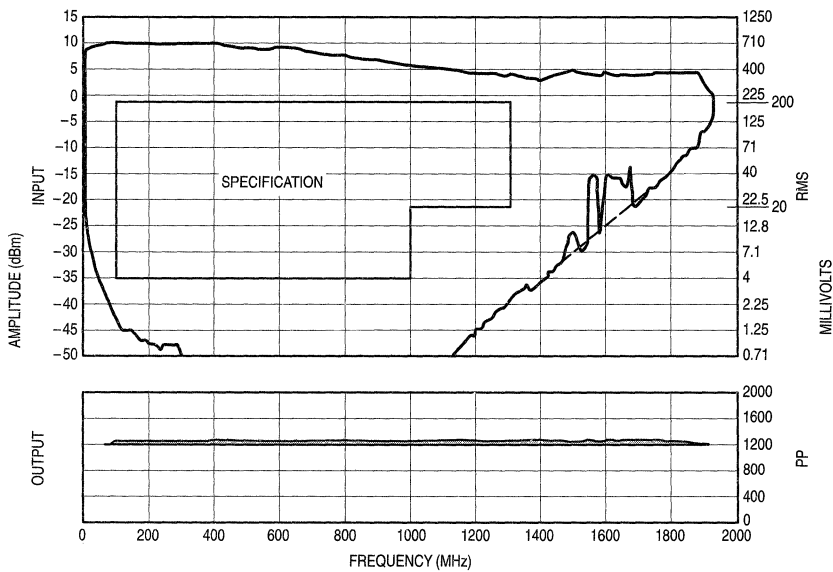
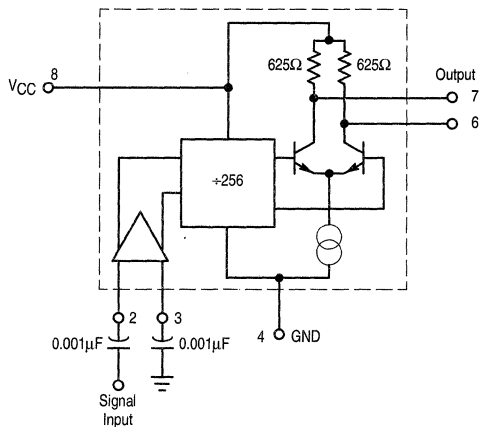


Figure 1. MC12076 Input Signal Amplitude versus Input Frequency

## 1.3GHz Prescaler

The MC12078 is a divide by 256 prescaler. Typical frequency synthesis applications include electronically tuned TV/CATV and communication systems as well as instrumentation.

An internal preamplifier is included which isolates the differential inputs and provides gain for the input signal. Differential PECL outputs are provided.

- 1.3GHz Toggle Frequency
- Operating Supply Voltage of 4.5 to 5.5V
- Low-Power 28mA Typical at  $V_{CC} = 5.0V$
- Operating Temperature Range of 0°C to +85°C
- High Input Sensitivity
- 800mV Minimum Peak-to-Peak Output Swing
- Differential PECL Outputs

### DESIGN GUIDE

Criteria	Value	Unit
Internal Gate Count*	62	ea
Internal Gate Propagation Delay	250	ps
Internal Gate Power Dissipation	10	mW
Speed Power Product	2.5	pJ

\* Equivalent to a two-input NAND gate

### MAXIMUM RATINGS

Symbol	Characteristic	Range	Unit
$V_{CC}$	Power Supply Voltage	7.0	Vdc
$T_A$	Operating Temperature Range	0 to +85	°C
$T_{stg}$	Storage Temperature Range	-65 to +175	°C

### ELECTRICAL CHARACTERISTICS ( $V_{CC} = 4.5$ to $5.5V$ ; $T_A = 0$ to $+85^\circ C$ )

Symbol	Characteristic	Min	Typ*	Max	Unit
$f_{max}$ <sup>1</sup>	Toggle Frequency (Sine Wave Input)	1.3	1.6	90	GHz
$f_{min}$					
$I_{CC}$	Supply Current at 5.5V		28	35	mA
$V_{out}$	Output Voltage (Load = 10pF)	0.8	1.2		$V_{pp}$
$V_{in min}$	Input Voltage		10	20	mV <sub>rms</sub>
	90MHz Sensitivity		4.0	10	
	150-1100MHz 1.3GHz		7.0	20	
$V_{in max}$	Input	400			mV <sub>rms</sub>
	90-500MHz Overload 500-1300MHz				

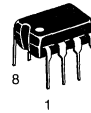
\* Typical measured at +25°C, 5.0V

1. See Figure 1

## MC12078

### MECL PLL COMPONENTS

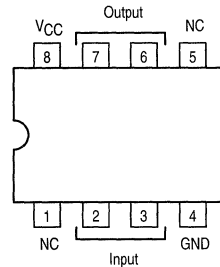
÷256  
**PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05

**D SUFFIX**  
PLASTIC SOIC PACKAGE 8 1  
CASE 751-04

### Pinout: 8-Lead Plastic (Top View)



PRESCALER BLOCK DIAGRAM

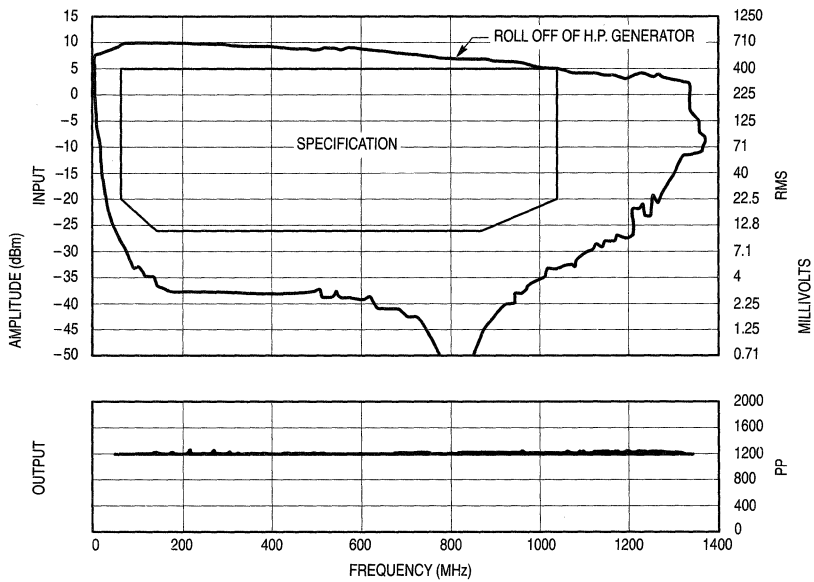
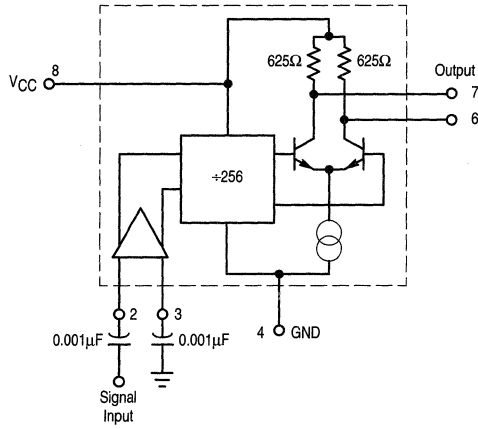


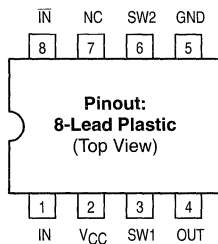
Figure 1. MC12078 Input Signal Amplitude versus Input Frequency

## 2.8GHz Prescaler

The MC12079 is a single modulus divide by 64, 128, 256 prescaler for low power frequency division of a 2.8GHz (typical) high frequency input signal. Divide ratio control inputs SW1 and SW2 select the required divide ratio of +64, +128, or +256.

An external load resistor is required to terminate the output. A 1.2kΩ resistor is recommended to achieve a 1.6V<sub>pp</sub> output swing, when dividing a 1.1GHz input signal by the minimum divide ratio of 64, assuming a 12pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V<sub>out</sub> specification for various divide ratios at 2.8GHz input frequency.

- 2.8GHz Toggle Frequency
- Supply Voltage 4.5V to 5.5V
- Low Power 9mA Typical at V<sub>CC</sub> = 5.0V
- Operating Temperature Range of -40°C to +85°C



### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 2	-0.5 to +7.0	VDC
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
I <sub>O</sub>	Maximum Output Current, Pin 4	4	mA

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 4.5 to 5.5V; T<sub>A</sub> = -40 to +85°C)

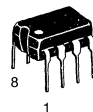
Symbol	Parameter	Min	Typ	Max	Unit
f <sub>t</sub>	Toggle Frequency (Sine Wave)	0.25	3.4	2.8	GHz
I <sub>CC</sub>	Supply Current Output (Pin 2)	—	9.0	11.5	mA
V <sub>in</sub>	Input Voltage Sensitivity	250–500MHz 400	—	1000	mV <sub>pp</sub>
		500–2800MHz 100	—	1000	
V <sub>IH</sub>	Divide Ratio Control Input High (SW)	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
V <sub>out</sub>	Output Voltage Swing (C <sub>L</sub> = 12pF; R <sub>L</sub> = 1.2kΩ; I <sub>O</sub> = 2.7mA) <sup>1</sup> (C <sub>L</sub> = 12pF; R <sub>L</sub> = 2.2kΩ; I <sub>O</sub> = 1.5mA) <sup>2</sup> (C <sub>L</sub> = 12pF; R <sub>L</sub> = 3.9kΩ; I <sub>O</sub> = 0.85mA) <sup>3</sup>	1.0	1.6	—	V <sub>pp</sub>

1. Divide ratio of +64 at 2.8GHz.
2. Divide ratio of +128 at 2.8GHz.
3. Divide ratio of +256 at 2.8GHz.

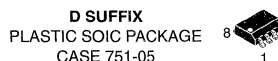
**MC12079**

**MECL PLL COMPONENTS**

**+64/128/256  
PRESCALER**



**P SUFFIX  
PLASTIC PACKAGE  
CASE 626-05**

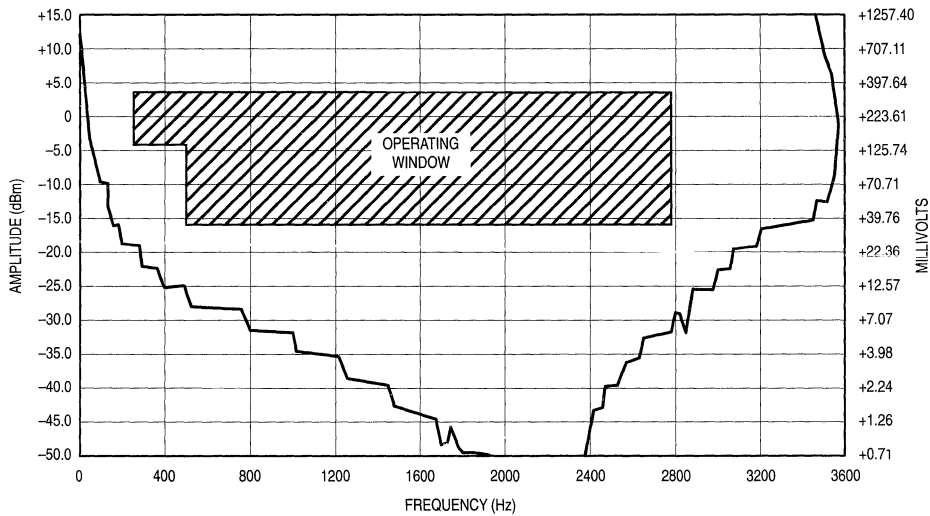


**D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-05**

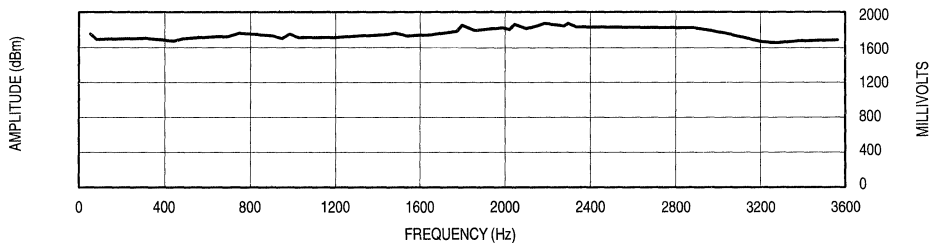








**Figure 3. Input Signal Amplitude versus Input Frequency**  
 Divide Ratio = 64;  $V_{CC} = 5.0V$ ;  $T_A = 25^{\circ}C$



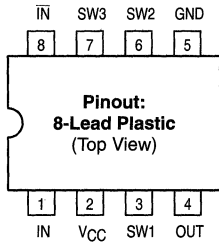
**Figure 4. Output Amplitude versus Input Frequency**

## 1.1GHz Prescaler

The MC12080 is a single modulus divide by 10, 20, 40, 80 prescaler for low power frequency division of a 1.1GHz high frequency input signal. Divide ratio control inputs SW1, SW2 and SW3 select the required divide ratio of +10, +20, +40, or +80.

An external load resistor is required to terminate the output. A 820Ω resistor is recommended to achieve a 1.2V<sub>pp</sub> output swing, when dividing a 1.1GHz input signal by the minimum divide by ratio of 10, assuming a 8pF load. Output current can be minimized dependent on conditions such as output frequency, capacitive load being driven, and output voltage swing required. Typical values for load resistors are included in the V<sub>out</sub> specification for various divide ratios at 1.1GHz input frequency.

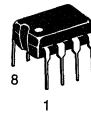
- 1.1GHz Toggle Frequency
- Supply Voltage 4.5V to 5.5V
- Low Power 3.7mA Typical at V<sub>CC</sub> = 5.0V
- Operating Temperature Range of -40°C to +85°C



**MC12080**

**MECL PLL COMPONENTS**

**+10/20/40/80  
PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05

**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 2	-0.5 to +7.0	VDC
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
I <sub>O</sub>	Maximum Output Current, Pin 4	10	mA

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 4.5 to 5.5V; T<sub>A</sub> = -40 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>t</sub>	Toggle Frequency (Sine Wave)	0.1	1.4	1.1	GHz
I <sub>CC</sub>	Supply Current Output (Pin 2)	—	3.7	5.0	mA
V <sub>in</sub>	Input Voltage Sensitivity	100–250MHz 250–1100MHz	400 100	— 1000	mV <sub>pp</sub>
V <sub>IH</sub>	Divide Ratio Control Input High (SW1, SW2, SW3)	V <sub>CC</sub> - 0.5V	V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	V
V <sub>IL</sub>	Divide Ratio Control Input Low (SW1, SW2, SW3)	Open	Open	Open	—
V <sub>out</sub>	Output Voltage Swing <sup>1</sup>	0.8	1.2	—	V <sub>pp</sub>

1. Assumes 8pF load and 1.1GHz input frequency (typical), I<sub>O</sub> at V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C



FUNCTION TABLE

SW1	SW2	SW3	Divide Ratio
L	L	L	80
L	L	H	40
L	H	L	40
L	H	H	20
H	L	L	40
H	L	H	20
H	H	L	20
H	H	H	10

NOTE: For SW1, SW2 and SW3: H = V<sub>CC</sub>; L = Open

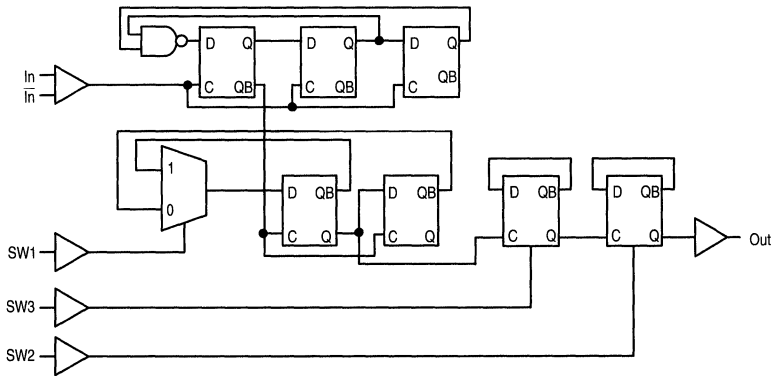


Figure 1. Logic Diagram (MC12080)

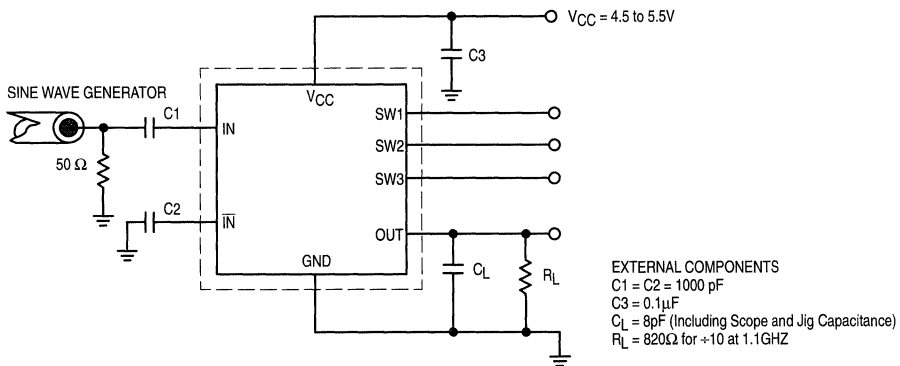
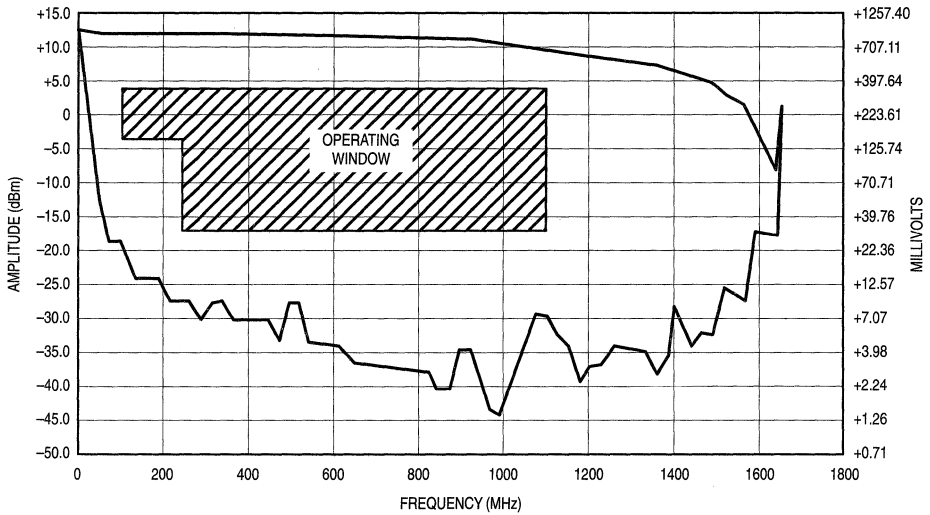
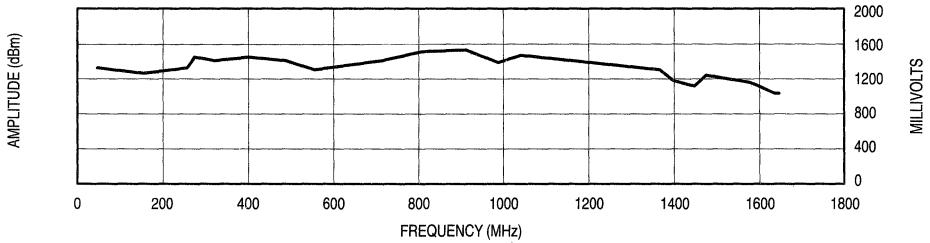


Figure 2. AC Test Circuit



**Figure 3. Input Signal Amplitude versus Input Frequency**  
 Divide Ratio = 10;  $V_{CC} = 5.0V$ ;  $T_A = 25^{\circ}C$



**Figure 4. Output Amplitude versus Input Frequency**

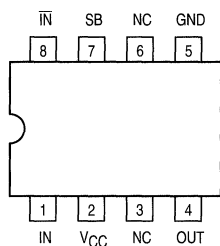
## 1.1GHz Prescaler With Stand-By Mode

The MC12083 is a  $\pm 2$  prescaler for low power frequency division of a 1.1GHz high frequency input signal. On-chip output termination provides output current to drive a 2pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added parallel from the OUT Pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Stand-By mode is featured to reduce current drain to 250 $\mu$ A typical when the stand-by pin SB is switched LOW disabling the prescaler.

- 1.1GHz Toggle Frequency
- Supply Voltage 2.7V to 5.5V
- Low Power 4.5mA Typical at  $V_{CC} = 2.7V$
- Operating Temperature  $-40$  to  $+85^{\circ}C$
- On-Chip Termination

Pinout: 8-Lead Plastic (Top View)

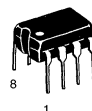


A LOW on the Stand-By Pin 7 disables the device.

**MC12083**

**MECL PLL COMPONENTS**

$\pm 2$   
**PRESCALER  
WITH STAND-BY MODE**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### MAXIMUM RATINGS

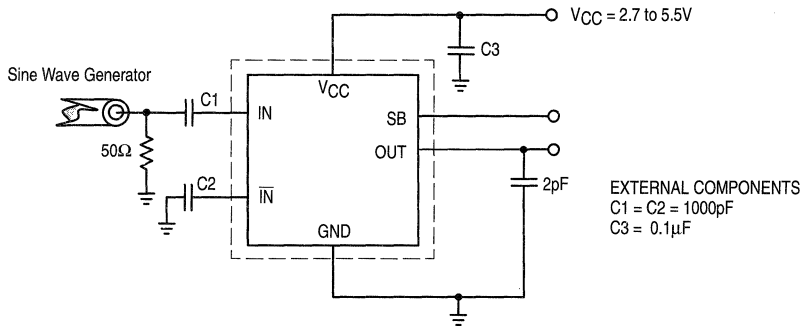
Symbol	Parameter	Value	Unit
$V_{CC}$	Power Supply Voltage, Pin 2	$-0.5$ to $+7.0$	VDC
$T_A$	Operating Temperature Range	$-40$ to $+85$	$^{\circ}C$
$T_{stg}$	Storage Temperature Range	$-65$ to $+150$	$^{\circ}C$
$I_O$	Maximum Output Current, Pin 4	10.0	mA



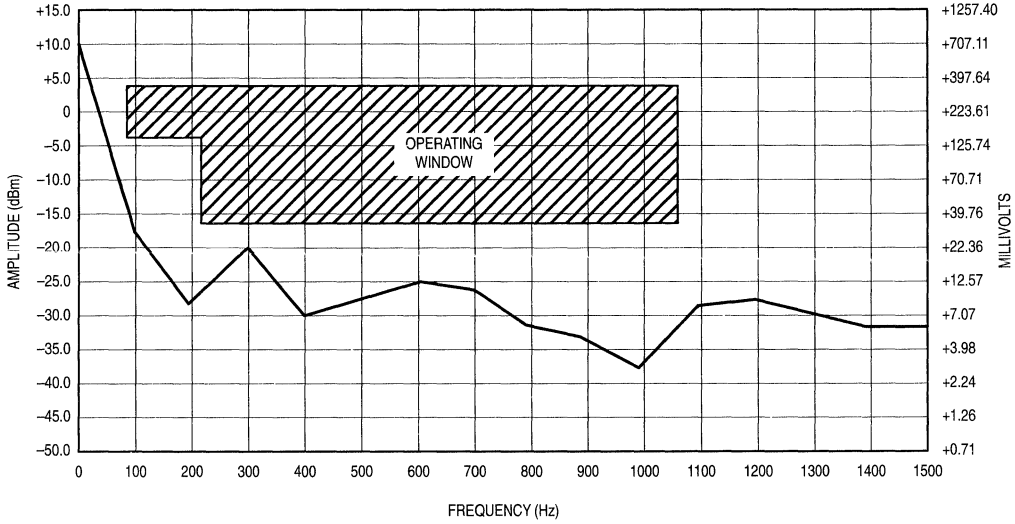
**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$f_t$	Toggle Frequency (Sine Wave)	0.1	1.4	1.1	GHz
$I_{CC}$	Supply Current Output (Pin 2) $V_{CC} = 3.0V$ $V_{CC} = 5.5V$		4.4 4.8	6.5 6.5	mA
$I_{SB}$	Standby Current $V_{CC} = 3.0V$ $V_{CC} = 5.5V$		250 500	350 600	$\mu A$
$V_{IH}$	Standby Input HIGH (SB)	2.0		$V_{CC}$	V
$V_{IL}$	Standby Input LOW (SB)	GND		0.8	V
$V_{OUT}$	Output Voltage Swing (Note 1) 2pF Load @ 500MHz Input 2pF Load @ 750MHz Input 2pF Load @ 1100MHz Input	700 600 400	800 700 450		mV <sub>PP</sub>
$V_{IN}$	Input Voltage Sensitivity 100–250MHz 250–400MHz 400–1100MHz	400 200 100		1000 1000 1000	mV <sub>PP</sub>

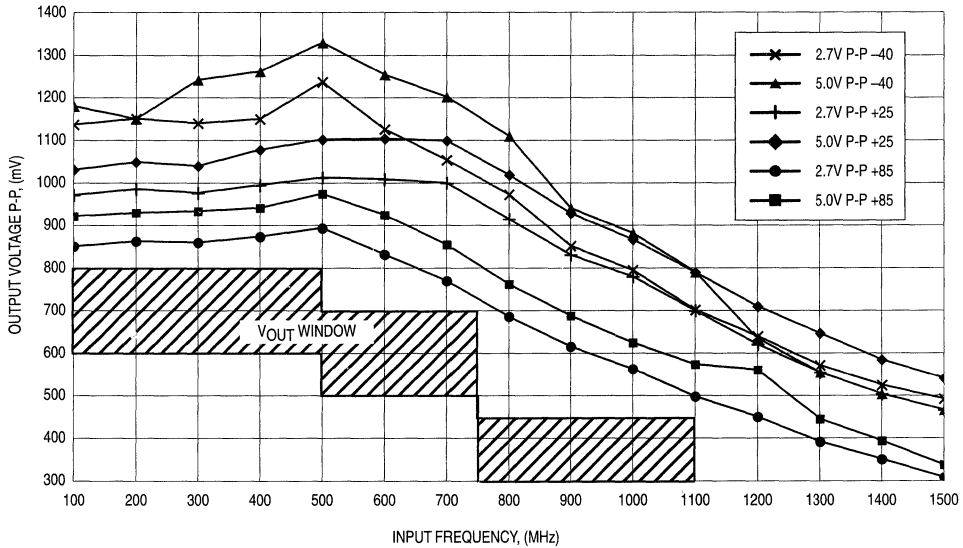
1. Assume 2pF load,  $V_{CC} = 2.7V$ ,  $V_{IN}$  = minimum specification for each frequency band,  $T_A = 85^\circ C$



**Figure 1. AC Test Circuit**



**Figure 2. Input Signal Amplitude versus Input Frequency**  
 Divide Ratio = 2;  $V_{CC} = 2.7V$ ;  $T_A = 25^\circ C$ ; Output Loaded With 2pF



**Figure 3. 12083 Output Peak-to-Peak at 2pF Load**

## 2.8GHz Prescaler

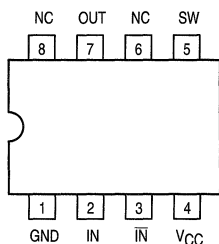
The MC12089 is a single modulus divide by 64 and 128 prescaler for low power frequency division of a 2.8GHz high frequency input signal. The low power (10.2mA typical at 5.0V) and high operating frequency features make this prescaler ideal in satellite TV receiver applications.

Divide ratio control input SW selects the required divide ratio of +64 or +128.

On-chip output termination provides 2.5mA of output current to drive a 12pF (typical) high impedance load. The output voltage swing under typical supply voltage and temperature conditions is 1.2V. If additional drive is required for the prescaler output, an external resistor can be added in parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

- 2.8GHz Toggle Frequency
- Supply Voltage 4.5V to 5.5V
- Low Power Dissipation 51mW Typical
- Operating Temperature Range of -40°C to +85°C

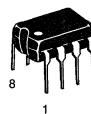
Pinout: 8-Lead Plastic (Top View)



## MC12089

### MECL PLL COMPONENTS

#### -64/128 PRESCALER



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 626-05



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 4	-0.5 to +7.0	VDC
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
I <sub>O</sub>	Maximum Output Current, Pin 7	4	mA

### ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 4.5 to 5.5V; T<sub>A</sub> = -40 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>t</sub>	Toggle Frequency (Sine Wave)	0.25	3.4	2.8	GHz
I <sub>CC</sub>	Supply Current Output (Pin 2)	—	10.2	14.5	mA
V <sub>in</sub>	Input Voltage Sensitivity	250–500MHz 500–2800MHz	400 100	— 1000 1000	mV <sub>pp</sub>
V <sub>IH</sub>	Divide Ratio Control Input High (SW)	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Divide Ratio Control Input Low (SW)	Open	Open	Open	—
V <sub>out</sub>	Output Voltage Swing <sup>1</sup>	0.8	1.2	—	V <sub>pp</sub>

<sup>1</sup> Assumes C<sub>L</sub> = 12pF





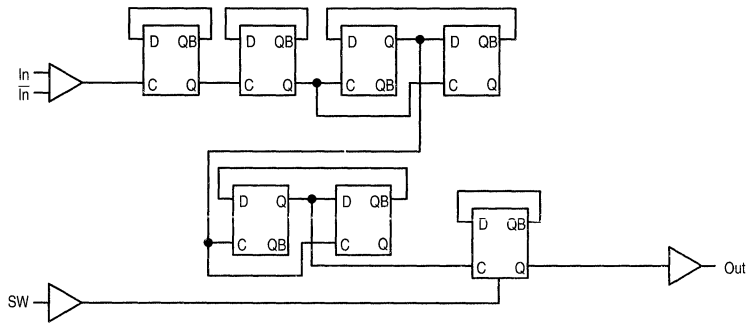


Figure 1. Logic Diagram (MC12089)

FUNCTION TABLE

SW	Divide Ratio
H	64
L	128

Note: H = V<sub>CC</sub>; L = Open

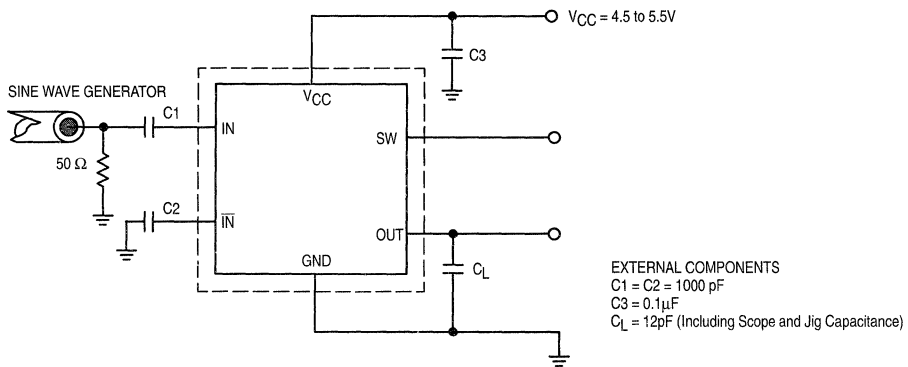
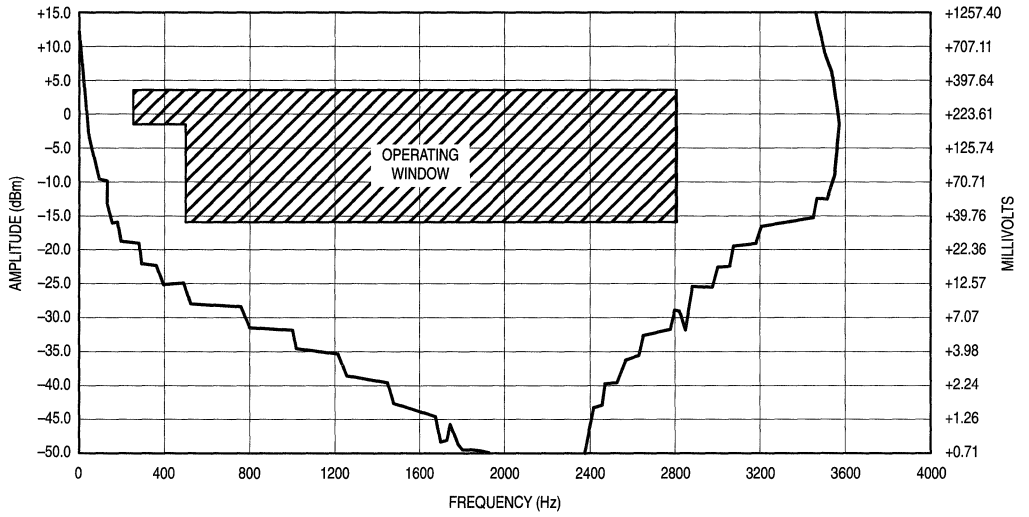


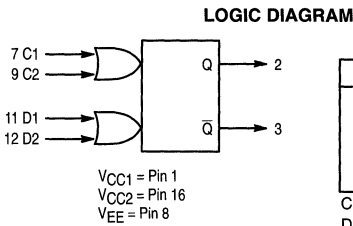
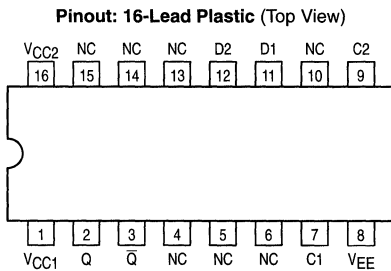
Figure 2. AC Test Circuit



**Figure 3. Input Signal Amplitude versus Input Frequency**  
 Divide Ratio = 64;  $V_{CC} = 5.0V$ ;  $T_A = 25^\circ C$

*Not Recommended for New Designs*  
*Consider MC12083 or MC10EL32*  
**UHF Prescaler**

The MC12090 is a high-speed D master-slave flip-flop capable of toggle rates of over 700MHz. It was designed primarily for high-speed prescaling applications in communications and instrumentation. This device employs two data inputs, two clock inputs as well as complementary Q and  $\bar{Q}$  outputs. There are no SET or RESET inputs.



**TRUTH TABLE**

C	D	Q <sub>n</sub> + 1
L	X	Q <sub>n</sub>
H	X	Q <sub>n</sub>
	L	L
	H	H

C = C1 + C2, X = Don't Care  
D = D1 + D2

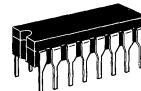
**MC12090**

**MECL PLL COMPONENTS**

**HIGH-SPEED  
PRESCALER**



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10

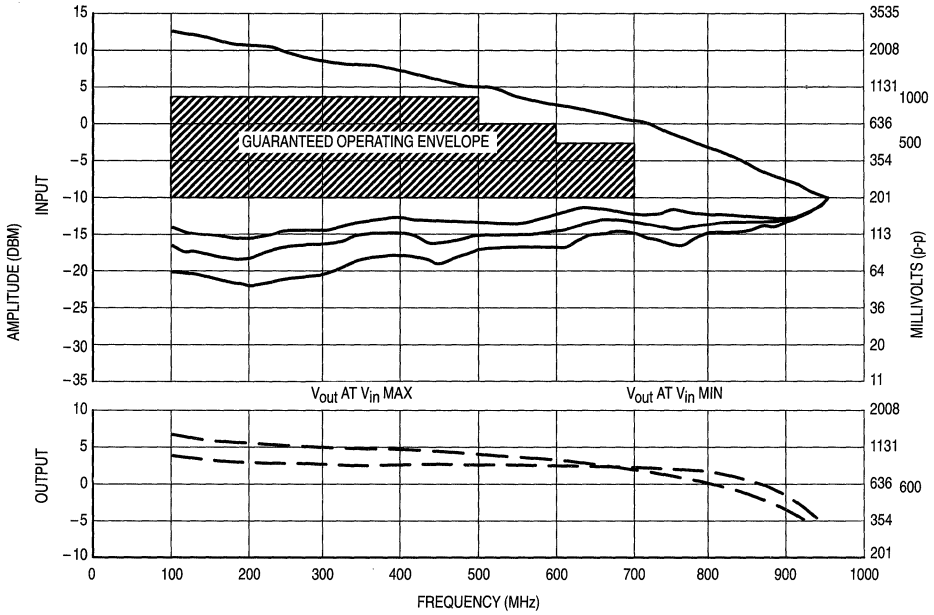
**ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	0°C		25°C		75°C		Unit
		Min	Max	Min	Max	Min	Max	
I <sub>E</sub>	Power Supply Current		65		59		65	mA
I <sub>inH</sub>	Input Current HIGH		400 435		260 280		260 280	μA
I <sub>inL</sub>	Input Current LOW	0.5		0.5		0.3		μA
V <sub>OH</sub>	Output Voltage HIGH	-1.02	-0.84	-0.98	-0.81	-0.92	-0.735	Vdc
V <sub>OL</sub>	Output Voltage LOW	-1.95	-1.63	-1.95	-1.63	-1.95	-1.60	Vdc
V <sub>IH</sub>	Input Voltage HIGH	-1.17	-0.84	-1.13	-0.81	-1.70	-0.735	Vdc
V <sub>IL</sub>	Input Voltage LOW	-1.87	-1.495	-1.85	-1.48	-1.83	-1.45	Vdc

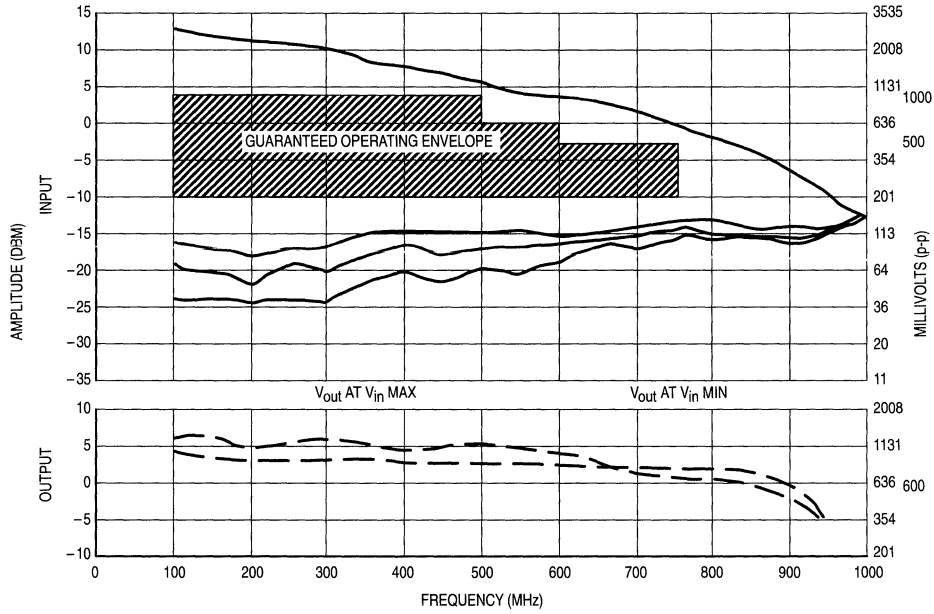


**ELECTRICAL CHARACTERISTICS**

Symbol	Characteristic	-30°C		0°C		25°C		75°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
$f_{tog}$	Toggle Frequency	500		700		750		700		500		MHz
<b>Typical (25°C)</b>												
$t_{pd}$	Propagation Delay (Clock to Output Pins 7,9,12)	1.3										ns
$t_s$	Setup Time	$t_{setup H}$				0.3						ns
		$t_{setup L}$				0.3						
$t_h$	Hold Time	$t_{hold H}$				0.3						ns
		$t_{hold L}$				0.3						
$t_r$	Rise Time	0.9										ns
$t_f$	Fall Time	0.9										ns



**Figure 1. Guaranteed Range of Operation**  
 (Temp = 75°C, 5 Devices,  $V_{CC} = 2.0V$ ,  $V_{EE} = -3.2V$ ,  $V_{Bias} = 0.710V$ )



**Figure 2. Guaranteed Range of Operation**  
 (Temp = 25°C, 5 Devices, V<sub>CC</sub> = 2.0V, V<sub>EE</sub> = -3.2V, V<sub>Bias</sub> = 0.710V)

## ÷2, ÷4, ÷8 1.1GHz Low Power Prescaler with Stand-By Mode

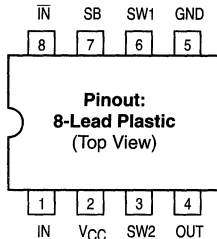
The MC12093 is a single modulus prescaler for low power frequency division of a 1.1GHz high frequency input signal. Motorola's advanced MOSAIC™ V technology is utilized to achieve low power dissipation of 6.75mW at a minimum supply voltage of 2.7V.

On-chip output termination provides output current to drive a 2pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Divide ratio control inputs SW1 and SW2 select the required divide ratio of ÷2, ÷4, or ÷8.

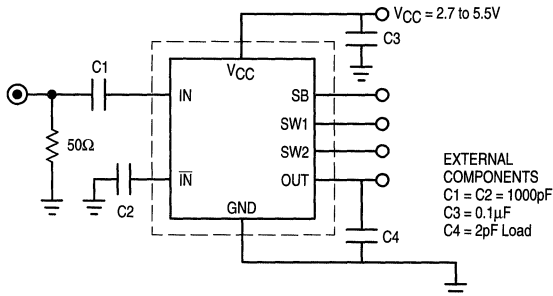
Stand-By mode is featured to reduce current drain to 50µA typical when the standby pin SB is switched LOW disabling the prescaler.

- 1.1GHz Toggle Frequency
- Supply Voltage 2.7V to 5.5VDC
- Low Power 3.0mA Typical
- Operating Temperature -40°C to +85°C
- Divide by 2, 4 or 8 Selected by SW1 and SW2 Pins
- On-Chip Termination



A LOW on the Stand-By Pin 7 disables the device.

### AC TEST CIRCUIT



## MC12093

### MECL PLL COMPONENTS

÷2, ÷4, ÷8  
**LOW POWER PRESCALER**  
**WITH STAND-BY MODE**



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



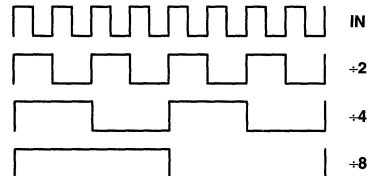
**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-02

### FUNCTION TABLE

SW1	SW2	Divide Ratio
L	L	8
H	L	4
L	H	4
H	H	2

Note: SW1 & SW2: H = ( $V_{CC}-0.5V$ ) to  $V_{CC}$ ;  
L = OPEN  
SB: H = 2.0V to  $V_{CC}$ ; L = GND to 0.8V

### FUNCTION CHART



**MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 2	-0.5 to +6.0	VDC
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
I <sub>O</sub>	Maximum Output Current, Pin 4	4.0	mA

**ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 2.7 to 5.5V; T<sub>A</sub> = -40 to +85°C)

Symbol	Parameter	Min	Typ	Max	Unit
f <sub>t</sub>	Toggle Frequency (Sine Wave)	0.1	1.4	1.1	GHz
I <sub>CC</sub>	Supply Current		3.0	4.5	mA
I <sub>SB</sub>	Stand-By Current		120	200	μA
V <sub>IH1</sub>	Stand-By Input HIGH (SB)	2.0		V <sub>CC</sub>	V
V <sub>IL1</sub>	Stand-By Input LOW (SB)	GND		0.8	V
V <sub>IH2</sub>	Divide Ratio Control Input HIGH (SW1 & SW2)	V <sub>CC</sub> - 0.5	V <sub>CC</sub>	V <sub>CC</sub> + 0.5	V
V <sub>IL2</sub>	Divide Ratio Control Input LOW (SW1 & SW2)	OPEN	OPEN	OPEN	
V <sub>OUT</sub>	Output Voltage Swing (2pF Load)				V <sub>PP</sub>
	Output Frequency 12.5–350MHz <sup>1</sup>	0.6	0.80		
	Output Frequency 350–400MHz <sup>2</sup>	0.5	0.70		
	Output Frequency 400–450MHz <sup>3</sup>	0.4	0.55		
	Output Frequency 450–550MHz <sup>4</sup>	0.3	0.45		
V <sub>IN</sub>	Input Voltage Sensitivity				mV <sub>PP</sub>
	250–1100MHz	100		1000	
	100–250MHz	400		1000	

1. Input frequency 1.1GHz, +8, minimum output frequency of 12.5MHz.
2. Input frequency 700–800MHz, +2.
3. Input frequency 800–900MHz, +2.
4. Input frequency 900–1100MHz, +2.

## 2.5GHz Low Power Prescaler With Stand-By Mode

The MC12095 is a single modulus prescaler for low power frequency division of a 2.5GHz high frequency input signal. Motorola's advanced MOSAIC™ V technology is utilized to achieve low power dissipation of 24mW at a minimum supply voltage of 2.7V.

On-chip output termination provides output current to drive a 2pF (typical) high impedance load. If additional drive is required for the prescaler output, an external resistor can be added in parallel from the OUT pin to GND to increase the output power. Care must be taken not to exceed the maximum allowable current through the output.

Divide ratio control input (SW) selects the required divide ratio of +2 or +4. Stand-By mode is available to reduce current drain to 100µA typical when the standby pin SB is switched LOW disabling the prescaler.

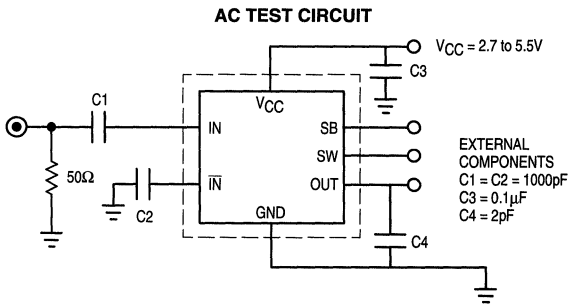
- 2.5GHz Toggle Frequency
- Supply Voltage 2.7V to 5.5VDC
- Low Power 8.7mA Typical
- Operating Temperature -40°C to +85°C
- Divide by 2 or 4 Selected by the SW Pin

**NOTE:** For applications up to 1.1GHz, please consult the MC12083 or MC12093 datasheets.

### FUNCTIONAL TABLE

SW	Divide Ratio
H	2
L	4

Note: SW: H = (V<sub>CC</sub> - 0.4V) to V<sub>CC</sub>; L = OPEN  
SB: H = 2.0V to V<sub>CC</sub>; L = GND to 0.8V



MOSAIC V is a trademark of Motorola.

## MC12095

### MECL PLL COMPONENTS

#### +2, +4 LOW POWER PRESCALER WITH STAND-BY MODE

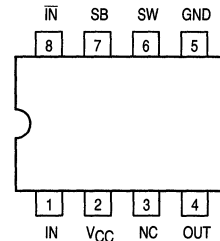


**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-02

### Pinout: 8-Lead Plastic SOIC (Top View)



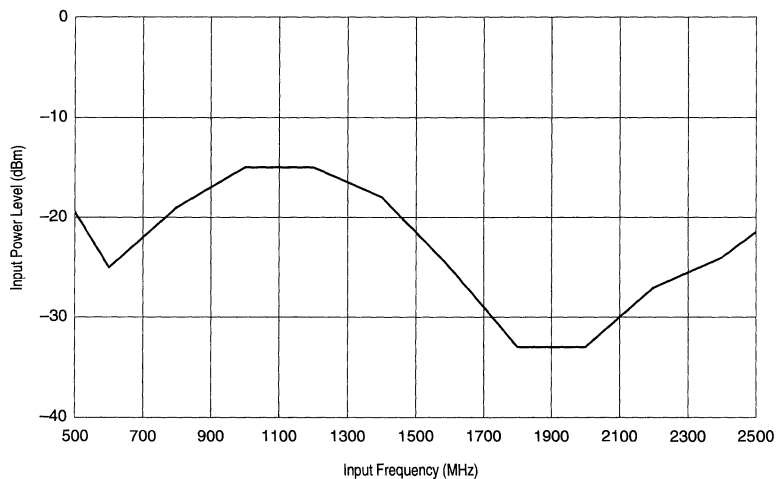


**MAXIMUM RATINGS**

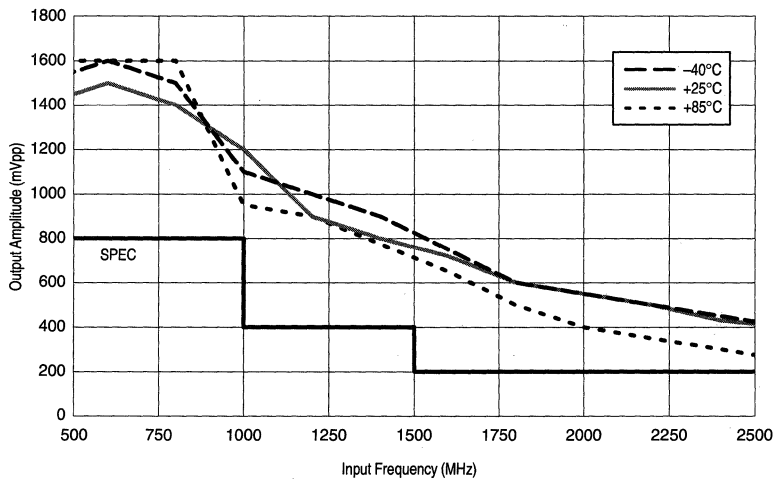
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 2	-0.5 to +6.0	VDC
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
I <sub>O</sub>	Maximum Output Current, Pin 4	8.0	mA

**ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 2.7 to 5.5V; T<sub>A</sub> = -40 to +85°C)

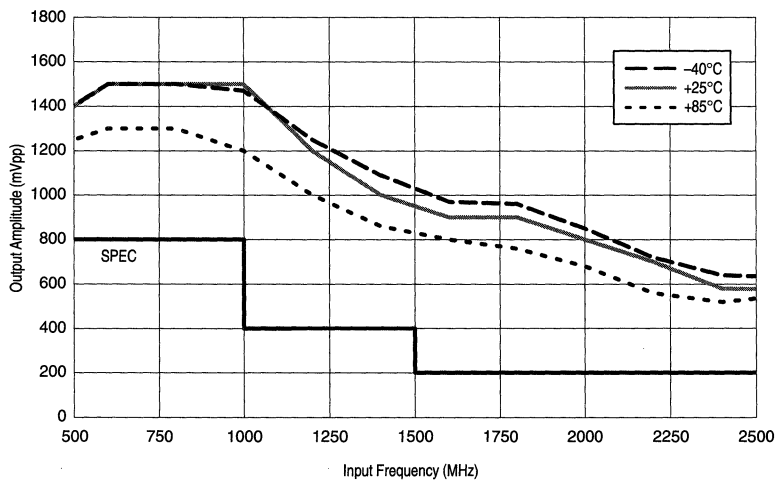
Symbol	Parameter	Min	Typ	Max	Unit
f <sub>t</sub>	Toggle Frequency (Sine Wave)	500	3.0	2.5	GHz
I <sub>CC</sub>	Supply Current		8.7	14	mA
I <sub>SB</sub>	Stand-By Current		100	200	μA
V <sub>IH1</sub>	Stand-By Input HIGH (SB)	2.0		V <sub>CC</sub> + 0.5V	V
V <sub>IL1</sub>	Stand-By Input LOW (SB)	GND		0.8	V
V <sub>IH2</sub>	Divide Ratio Control Input HIGH (SW)	V <sub>CC</sub> - 0.4	V <sub>CC</sub>	V <sub>CC</sub> + 0.5V	V
V <sub>IL2</sub>	Divide Ratio Control Input LOW (SW)	OPEN	OPEN	OPEN	
V <sub>OUT</sub>	Output Voltage Swing (2pF Load)	500–1000MHz Input 1000–1500MHz Input 1500–2500MHz Input	800 400 200	450 250	mV <sub>PP</sub>
V <sub>IN</sub>	Input Voltage Sensitivity	200		1000	mV <sub>PP</sub>



**Figure 1. Typical Minimum Input Sensitivity versus Input Frequency**  
(Divide By 2 Mode, T = 25°C, V<sub>CC</sub> = 2.7V)



**Figure 2. Typical Output Amplitude versus Frequency over Temperature**  
(Divide By 2 Mode,  $V_{CC} = 2.7V$ )



**Figure 3. Typical Output Amplitude versus Frequency over Temperature**  
(Divide By 4 Mode,  $V_{CC} = 2.7V$ )

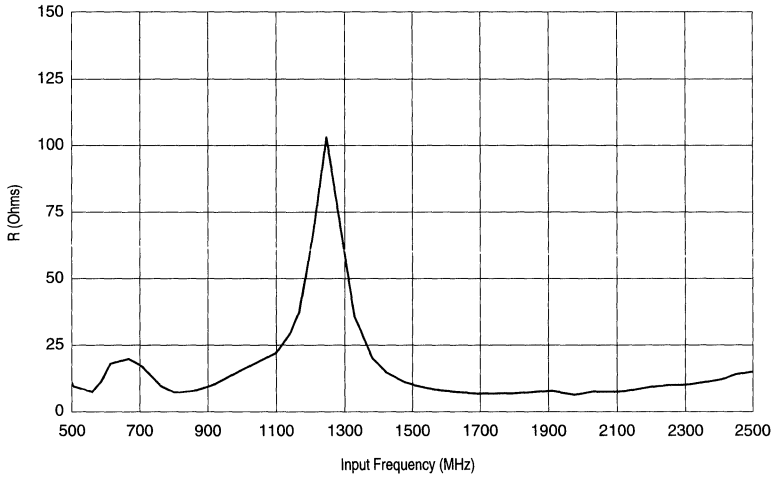


Figure 4. Input Impedance versus Frequency

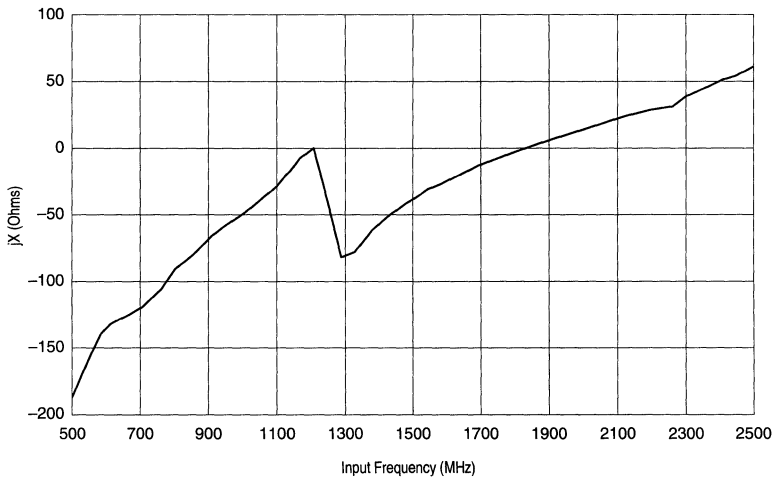


Figure 5. Input Impedance versus Frequency



# VCM/VCOs

# Voltage Controlled Oscillator

## Consider MC12148 for New Designs

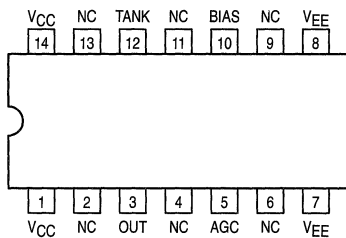
The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). For Maximum Performance  $Q_L \geq 100$  at Frequency of Operation.

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2)

The MC1648 may be operated from a +5.0Vdc supply or a -5.2Vdc supply, depending upon system requirements.

**NOTE:** The MC1648 is NOT useable as a crystal oscillator.

**Pinout: 14-Lead Package (Top View)**



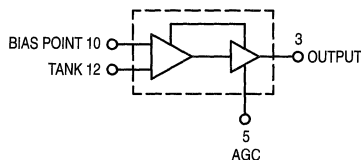
Supply Voltage	GND Pins	Supply Pins
+5.0Vdc	7,8	1,14
-5.2Vdc	1,14	7,8

**MC1648 NON-STANDARD PIN CONVERSION DATA**

Package	TANK	VCC	VCC	OUT	AGC	VEE	VEE	BIAS
8 D	1	2	3	4	5	6	7	8
14 L,P	12	14	1	3	5	7	8	10
20FN	18	20	2	4	8	10	12	14

\*NOTE - All unused pins are not connected.

### LOGIC DIAGRAM

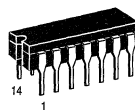


- Input Capacitance = 6.0pF (TYP)
- Maximum Series Resistance for L (External Inductance) = 50Ω (TYP)
- Power Dissipation = 150mW (TYP)/Pkg (+5.0Vdc Supply)
- Maximum Output Frequency = 225MHz (TYP)

VCC1 = Pin 1  
VCC2 = Pin 14  
VEE = Pin 7

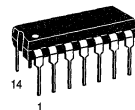
## MC1648

### VOLTAGE CONTROLLED OSCILLATOR



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 632-08

*Not Recommended for New Designs*



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



**FN SUFFIX**  
PLCC PACKAGE  
CASE 775-02



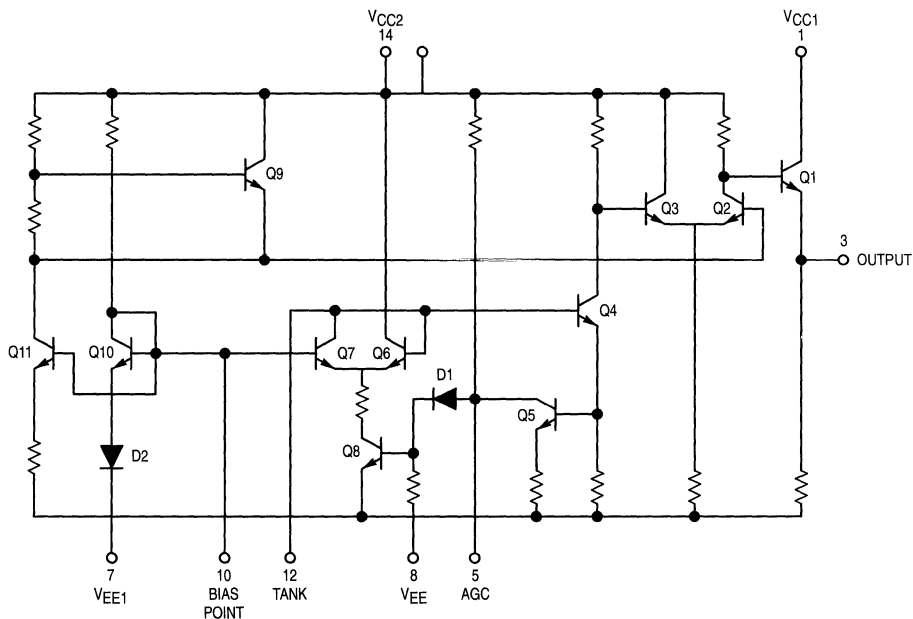


Figure 1. Circuit Schematic

## TEST VOLTAGE/CURRENT VALUES

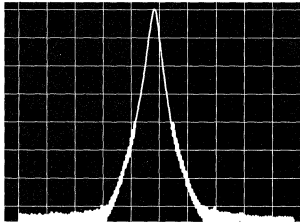
© Test Temperature	(Volts)			mAdc
	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>CC</sub>	I <sub>L</sub>
<b>MC1648</b>				
-30°C	+2.0	+1.5	5.0	-5.0
+25°C	+1.85	+1.35	5.0	-5.0
+85°C	+1.7	+1.2	5.0	-5.0

Note: SOIC "D" package guaranteed -30°C to +70°C only

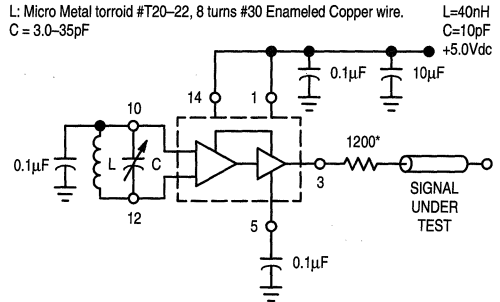
## ELECTRICAL CHARACTERISTICS (Supply Voltage = +5.0V)

Symbol	Characteristic	-30°C		+25°C		+85°C		Unit	Condition			
		Min	Max	Min	Max	Min	Max					
I <sub>E</sub>	Power Supply Drain Current	-	-	-	41	-	-	mAdc	Inputs and outputs open			
V <sub>OH</sub>	Logic "1" Output Voltage	3.955	4.185	4.04	4.25	4.11	4.36	Vdc	V <sub>ILmin</sub> to Pin 12, I <sub>L</sub> @ Pin 3			
V <sub>OL</sub>	Logic "0" Output Voltage	3.16	3.4	3.2	3.43	3.22	3.475	Vdc	V <sub>IHmax</sub> to Pin 12, I <sub>L</sub> @ Pin 3			
V <sub>BIAS</sub> <sup>1</sup>	Bias Voltage	1.6	1.9	1.45	1.75	1.3	1.6	Vdc	V <sub>ILmin</sub> to Pin 12			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V <sub>P-P</sub>	Peak-to-Peak Tank Voltage	-	-	-	-	400	-	-	-	-	mV	See Figure 3
V <sub>dc</sub>	Output Duty Cycle	-	-	-	-	50	-	-	-	-	%	
f <sub>max</sub> <sup>2</sup>	Oscillation Frequency	-	225	-	200	225	-	-	225	-	MHz	

1. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.
2. Frequency variation over temperature is a direct function of the  $\Delta C/\Delta$  Temperature and  $\Delta L/\Delta$  Temperature.



B.W. = 10 kHz  
 Center Frequency = 100 MHz  
 Scan Width = 50 kHz/div  
 Vertical Scale = 10 dB/div



\* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-075-50 or equivalent.

Figure 2. Spectral Purity of Signal Output for 200MHz Testing

TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	(Volts)			(mAdc)
	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>CC</sub>	I <sub>L</sub>
<b>MC1648</b>				
-30°C	-3.2	-3.7	-5.2	-5.0
+25°C	-3.35	-3.85	-5.2	-5.0
+85°C	-3.5	-4.0	-5.2	-5.0

Note: SOIC "D" package guaranteed -30°C to +70°C only

ELECTRICAL CHARACTERISTICS (Supply Voltage = -5.2V)

Symbol	Characteristic	-30°C		+25°C		+85°C		Unit	Condition			
		Min	Max	Min	Max	Min	Max					
I <sub>E</sub>	Power Supply Drain Current	-	-	-	41	-	-	mAdc	Inputs and outputs open			
V <sub>OH</sub>	Logic "1" Output Voltage	-1.045	-0.815	-0.96	-0.75	-0.89	-0.64	Vdc	V <sub>ILmin</sub> to Pin 12, I <sub>L</sub> @ Pin 3			
V <sub>OL</sub>	Logic "0" Output Voltage	-1.89	-1.65	-1.85	-1.62	-1.83	-1.575	Vdc	V <sub>IHmax</sub> to Pin 12, I <sub>L</sub> @ Pin 3			
V <sub>BIAS</sub> <sup>1</sup>	Bias Voltage	-3.6	-3.3	-3.75	-3.45	-3.9	-3.6	Vdc	V <sub>ILmin</sub> to Pin 12			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	Condition
V <sub>p-p</sub>	Peak-to-Peak Tank Voltage	-	-	-	-	400	-	-	-	-	mV	See Figure 3
V <sub>dc</sub>	Output Duty Cycle	-	-	-	-	50	-	-	-	-	%	
f <sub>max</sub> <sup>2</sup>	Oscillation Frequency	-	225	-	200	225	-	-	225	-	MHz	

1. This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor tuning diode at this point.  
 2. Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.



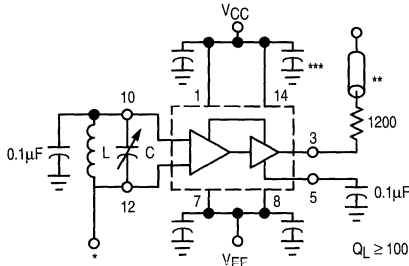


Figure 3. Test Circuit and Waveforms

- \* Use high impedance probe (>1.0 Megohm must be used).
- \*\* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent.
- \*\*\* Bypass only that supply opposite ground.

**OPERATING CHARACTERISTICS**

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q6 to the collector of Q7. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q6) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that the cathode of the varactor diode (D) should be biased at least "2" V<sub>BE</sub> above

V<sub>EE</sub> (≈1.4V for positive supply operation).

When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

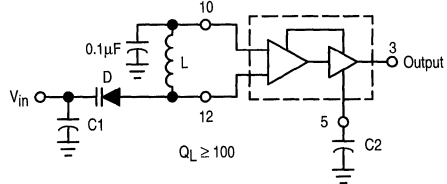
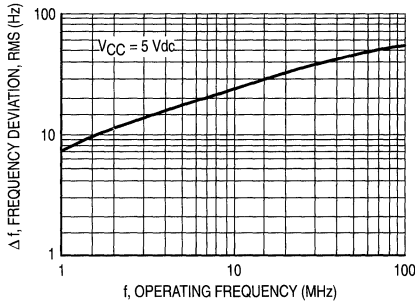


Figure 4. The MC1648 Operating in the Voltage Controlled Mode



Oscillator Tank Components (Circuit of Figure 4)

f MHz	D	L µH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15

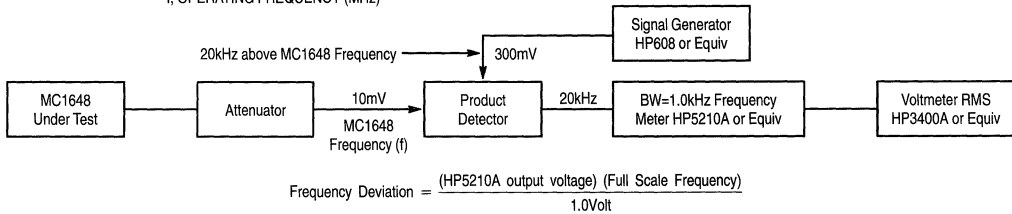


Figure 5. Noise Deviation Test Circuit and Waveform

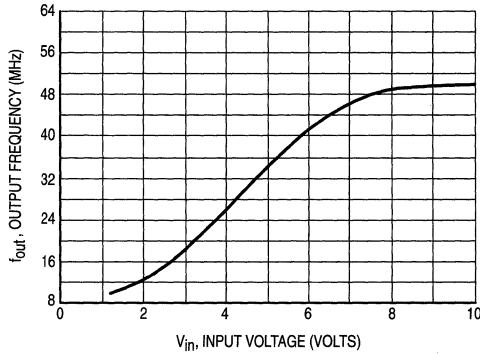
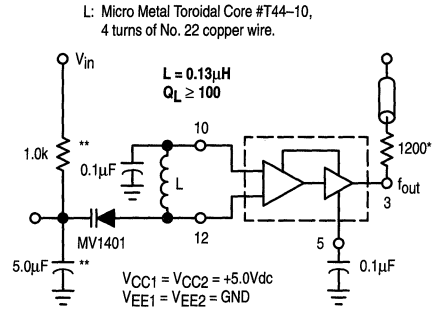


Figure 6



- \* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent. NOT used in normal operation.
- \*\* Input resistor and cap are for test only. They are NOT necessary for normal operation.

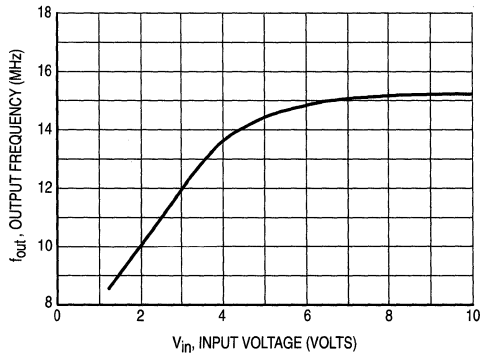
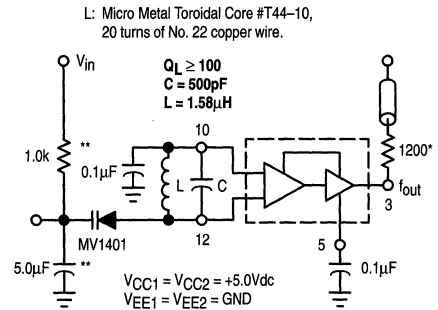


Figure 7



- \* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent. NOT used in normal operation.
- \*\* Input resistor and cap are for test only. They are NOT necessary for normal operation.

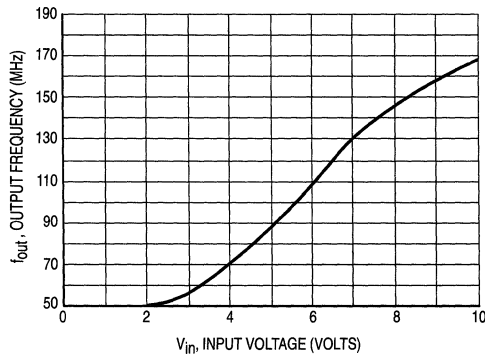
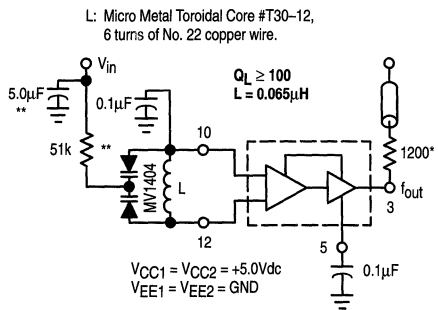


Figure 8



- \* The 1200 ohm resistor and the scope termination impedance constitute a 25:1 attenuator probe. Coax shall be CT-070-50 or equivalent. NOT used in normal operation.
- \*\* Input resistor and cap are for test only. They are NOT necessary for normal operation.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figure 6, Figure 7 and Figure 8. Figure 6 and Figure 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6.0pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1.0k $\Omega$  resistor in Figure 6 and Figure 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51k $\Omega$ ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{\max}}{f_{\min}} = \frac{\sqrt{C_D(\max) + C_S}}{\sqrt{C_D(\min) + C_S}}$$

$$\text{where } f_{\min} = \frac{1}{2\pi \sqrt{L(C_D(\max) + C_S)}}$$

CS = shunt capacitance (input plus external capacitance)

CD = varactor capacitance as a function of bias voltage

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1.0MHz and 50MHz a 0.1 $\mu$ F capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1.0k $\Omega$  minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

## APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter;  $f_{\text{out}} = Nf_{\text{ref}}$ . The channel spacing is equal to frequency ( $f_{\text{ref}}$ ).

For additional information on applications and designs for phase locked-loops and digital frequency synthesizers, see

Motorola Brochure BR504/D, Electronic Tuning Address Systems, (ETAS).

Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to VEE.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0Vdc supply. To extend the useful range of the device (maintain a square wave output above 175Mhz), a resistor is added to the AGC circuit at pin 5 (1.0 kohm minimum).

Figure 12 shows the MC1648 operating from +5.0Vdc and +9.0Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figure 13 and Figure 14 for 100MHz and 10MHz operation. The total collector load includes R in parallel with  $R_p$  of L1 and C1 at resonance. The optimum value for R at 100MHz is approximately 850 ohms.

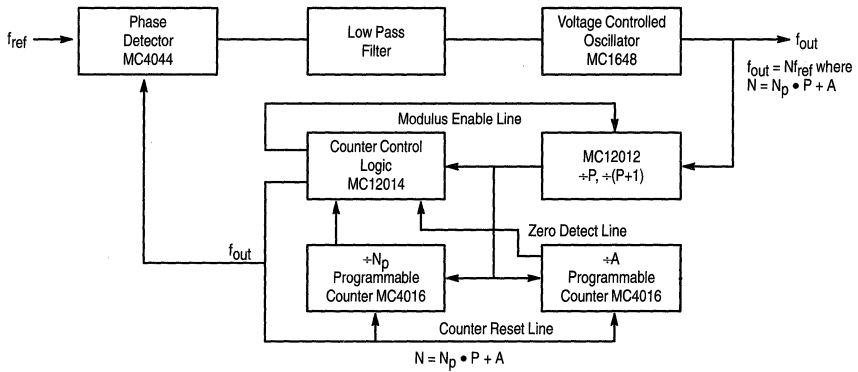


Figure 9. Typical Frequency Synthesizer Application

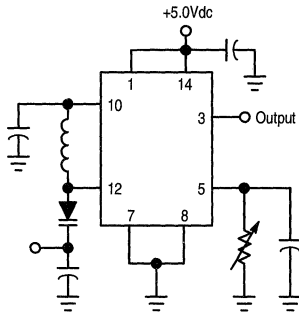


Figure 10. Method of Obtaining a Sine-Wave Output

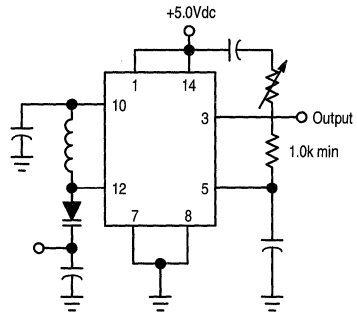


Figure 11. Method of Extending the Useful Range of the MC1648 (Square Wave Output)

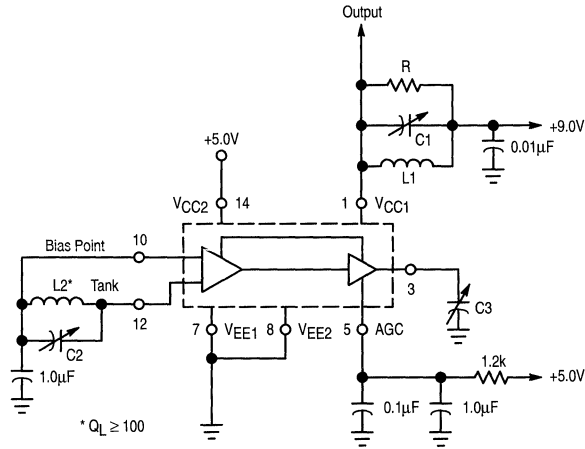
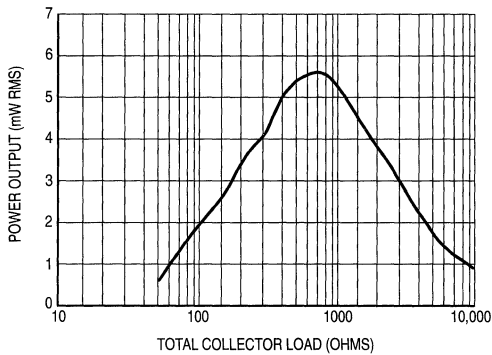
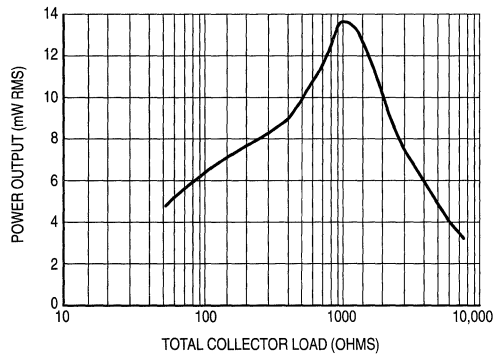


Figure 12. Circuit Used for Collector Output Operation



See test circuit, Figure 12,  $f = 100\text{MHz}$   
 $C3 = 3.0\text{--}35\text{pF}$   
 Collector Tank  
 $L1 = 0.22\mu\text{H}$        $C1 = 1.0\text{--}7.0\text{pF}$   
 $R = 50\Omega\text{--}10\text{k}\Omega$   
 $R_p$  of  $L1$  and  $C1 = 11\text{k}\Omega$  @  $100\text{MHz}$  Resonance  
 Oscillator Tank  
 $L2 = 4$  turns #20 AWG 3/16" ID  
 $C2 = 1.0\text{--}7.0\text{pF}$

Figure 13. Power Output versus Collector Load



See test circuit, Figure 12,  $f = 10\text{MHz}$   
 $C3 = 470\text{pF}$   
 Collector Tank  
 $L1 = 2.7\mu\text{H}$        $C1 = 24\text{--}200\text{pF}$   
 $R = 50\Omega\text{--}10\text{k}\Omega$   
 $R_p$  of  $L1$  and  $C1 = 6.8\text{k}\Omega$  @  $10\text{MHz}$  Resonance  
 Oscillator Tank  
 $L2 = 2.7\mu\text{H}$   
 $C2 = 16\text{--}150\text{pF}$

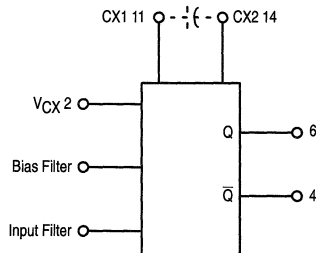
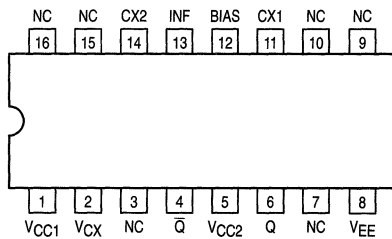
Figure 14. Power Output versus Collector Load

## Voltage Controlled Multivibrator

The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

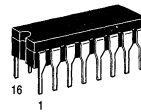
Pinout: 16-Lead Package (Top View)



VCC = Pin 1  
VCC2 = Pin 5  
VEE = Pin 8

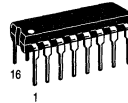
**MC1658**

**VOLTAGE  
CONTROLLED  
MULTIVIBRATOR**

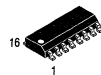


**L SUFFIX**  
CERAMIC PACKAGE  
CASE 620-10

*Not Recommended for New Designs*



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 648-08



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B-05



**FN SUFFIX**  
PLCC PACKAGE  
CASE 775-02



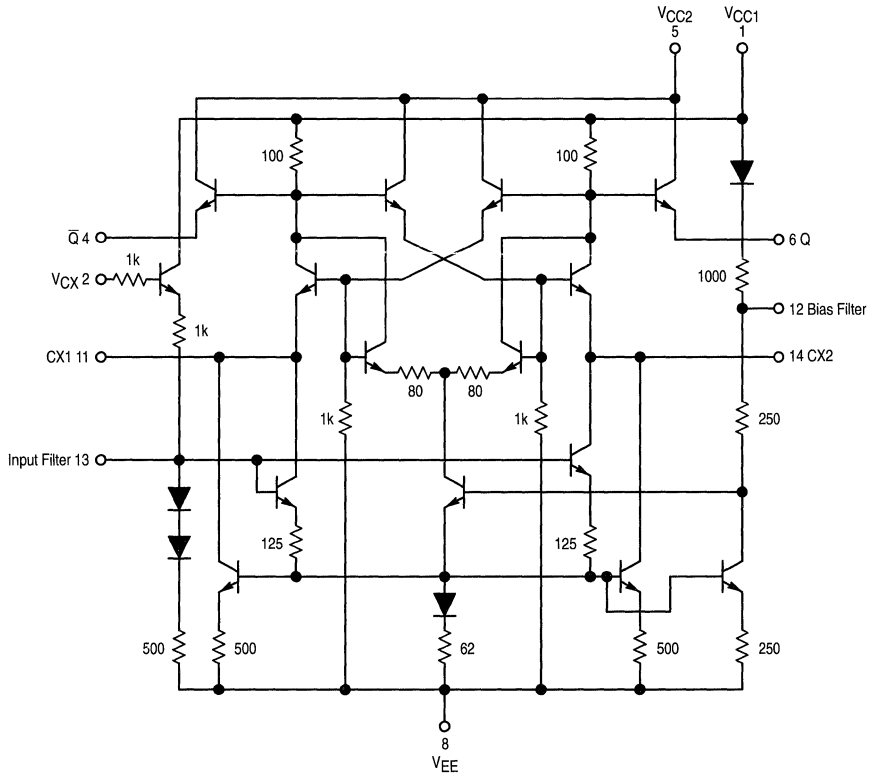


Figure 1. Circuit Schematic

TEST VOLTAGE VALUES

④ Test Temperature	Vdc ±1%			
	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>3</sub>	I <sub>IHA</sub>
-30°C	0	-2.0	-1.0	+2.0
+25°C	0	-2.0	-1.0	+2.0
+85°C	0	-2.0	-1.0	+2.0

Note: SOIC "D" package guaranteed -30°C to +70°C only

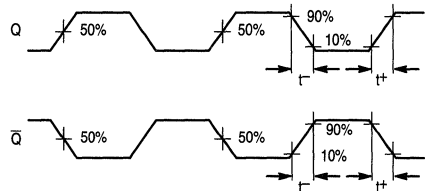
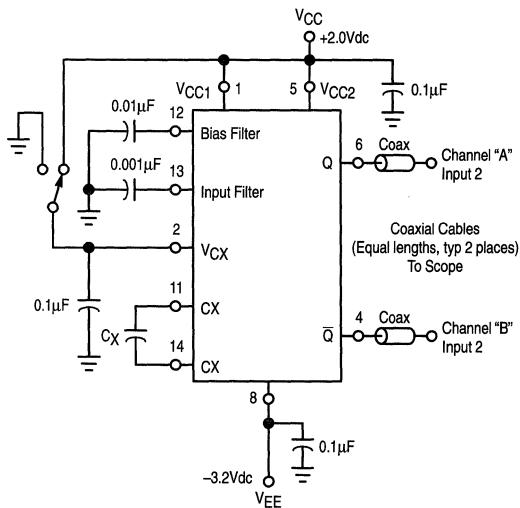
**ELECTRICAL CHARACTERISTICS** ( $V_{EE} = -5.2V$ ,  $V_{CC} = 0V$  [GND])

Symbol	Characteristic	-30°C		+25°C		+85°C		Unit	Condition
		Min	Max	Min	Max	Min	Max		
$I_E$	Power Supply Drain Current	-	-	-	32	-	-	mAdc	$V_{IH}$ to $V_{CX}$ Limit Applies for 1 or 2
$I_{inH}$	Input Current	-	-	-	350	-	-	$\mu$ Adc	$V_{IH}$ to $V_{CX}^1$
$V_{OH}$	Output Voltage "Q" HIGH	-1.045	-0.875	-0.96	-0.81	-0.89	-0.7	Vdc	$V_3$ to $V_{CX}$ . Limits Apply for 1 or 2
$V_{OL}$	Output Voltage "Q" LOW	-1.89	-1.65	-1.85	-1.62	-1.83	-1.575	Vdc	

**AC CHARACTERISTICS** ( $V_{EE} = -3.2V$ ,  $V_{CC} = +2.0V$ )

Symbol	Characteristic	-30°C		+25°C			+85°C		Unit	Condition (See Figure 2)
		Min	Max	Min	Typ	Max	Min	Max		
$t^+$	Rise Time (10% to 90%)	-	2.7	-	1.6	2.7	-	3.0	ns	$V_{IH}$ to $V_{CX}$ , CX1 <sup>4</sup> from Pin 11 to Pin 14
$t^-$	Fall Time (10% to 90%)	-	2.7	-	1.4	2.7	-	3.0	ns	
$f_{osc1}$	Oscillator Frequency	130	-	130	155	175	110	-	MHz	$V_{IH}$ to $V_{CX}$ , CX2 <sup>5</sup> from Pin 11 to Pin 14
$f_{osc2}$		-	-	78	100	120	-	-		
TR <sup>3</sup>	Tuning Ratio Test	-	-	3.1	4.5	-	-	-	-	CX2 <sup>5</sup> from Pin 11 to Pin 14

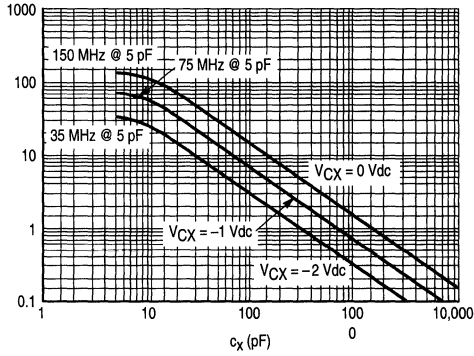
- 1 Germanium diode (0.4 drop) forward biased from 11 to 14 (11→14).
- 2 Germanium diode (0.4 drop) forward biased from 14 to 11 (11←14).
- 3  $TR = \frac{\text{Output frequency at } V_{CX} = \text{GND}}{\text{Output frequency at } V_{CX} = -2.0V}$
- 4 CX1 = 5.0pF connected from pin 11 to pin 14.
- 5 CX2 = 10pF connected from pin 11 to pin 14.



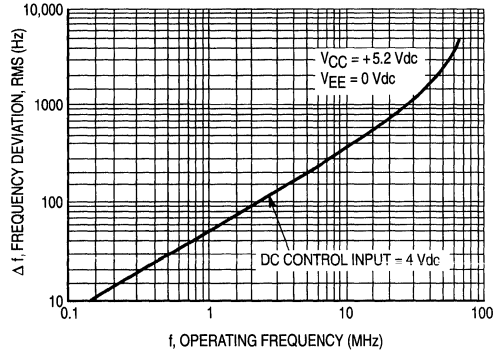
50 ohm termination to ground located in each scope channel input.  
 All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < 1/4 inch from  $TP_{in}$  to input pin and  $TP_{out}$  to output pin.  
 Note: All power supply and logic levels are shown shifted 2.0V positive.

**Figure 2. AC Test Circuit and Waveforms**

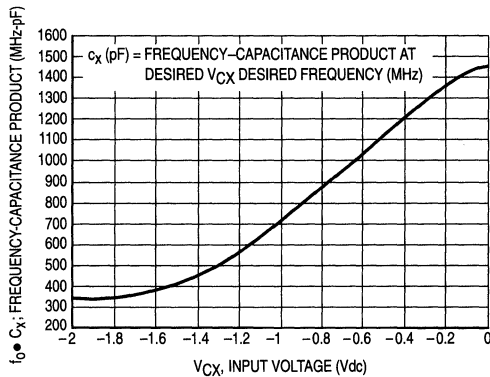




**Figure 3. Output Frequency versus Capacitance for Various Values of Input Voltage**



**Figure 4. RMS Noise Deviation versus Operating Frequency**

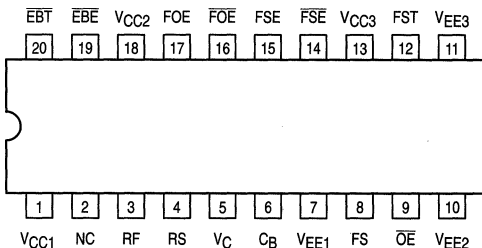


**Figure 5. Frequency Capacitance Product versus Control Voltage ( $V_{CX}$ )**

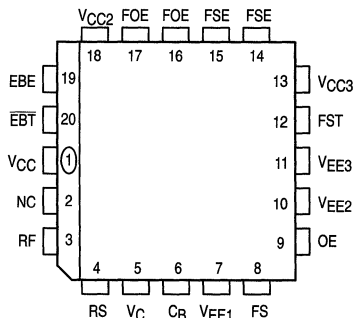
# 200MHz Voltage Controlled Multivibrator

- High Frequency VCM Ideal for PLL Applications
- Single External Resistor Determines Center Frequency; Additional Resistor Determines  $f/V$  Sensitivity
- Internal Ripple Counter (1/2, 1/4, 1/8) For Low Frequency Applications – TTL/ECL Outputs
- VCO Output Enable Pins (TTL/ECL Level)
- +5.0V Single Supply Voltage
- Packages: DIP, PLCC

**Pinout: 20-Lead Plastic Package (Top View)**

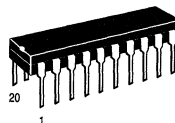


**Pinout: 20-Lead PLCC Package (Top View)**



**MC12100**

**200MHz VOLTAGE  
CONTROLLED  
MULTIVIBRATOR**



**P SUFFIX**  
PLASTIC DIP PACKAGE  
CASE 738-03



**FN SUFFIX**  
PLCC PACKAGE  
CASE 775-02

**PIN NAMES**

Pin	Function
RF, RS	Center Frequency Inputs
VC	Frequency Control Input
CB	Bias Filter Input
FS	Frequency Select Input
OE	TTL Output Enable
FST	TTL +2, +4, +8 Output
FSE, <del>FSE</del>	Diff ECL +2, +4, +8 Outputs
FOE, <del>FOE</del>	Diff ECL +1 Outputs
EBE	VCO Disable, ECL Level Input
EBT	VCO Disable, TTL Level Input



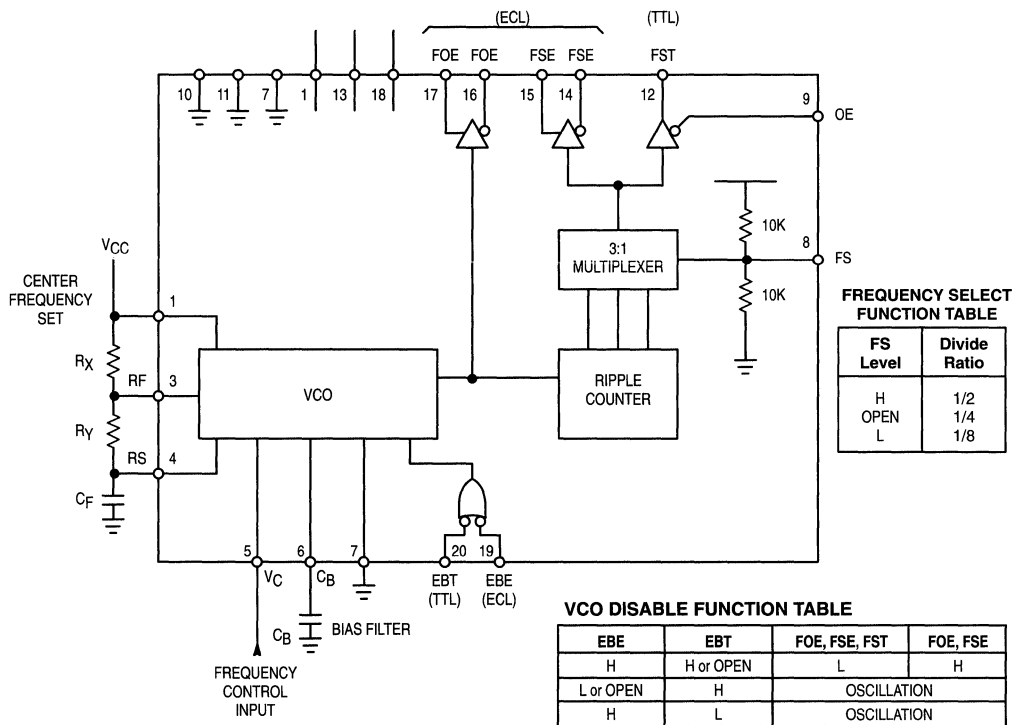


Figure 1. Block Diagram

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC1</sub> V <sub>CC2</sub> V <sub>CC3</sub>	Power Supply Voltage	-0.5 to +8.0	V
V <sub>IN</sub> (TTL)	Input Voltage	-0.5 to V <sub>CC</sub>	V
V <sub>IN</sub> (ECL)	Input Voltage	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub> (ECL)	Output Source Current - Surge	100	mA
	Output Source Current - Continuous	50	mA
T <sub>J</sub>	Junction Operating Temperature	+140	°C
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C

**OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Temperature	0 to +75	°C
V <sub>CC</sub>	Supply Voltage	+4.75 to +5.25	V
I <sub>OH</sub> (TTL)	TTL High Output Current	-1.0	mA
I <sub>OL</sub> (TTL)	TTL Low Output Current	20	mA

MC12100

**DC CHARACTERISTICS** ( $V_{CC} = 5.0V \pm 5\%$ ;  $R_X = 2.4k\Omega$ ;  $R_Y = 1.5k\Omega$ ;  $C_B = 0.001\mu F$ )

Symbol	Characteristic	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
I <sub>CC</sub>	Supply Current	75	120	65	90	110	80	135	mA	$\overline{EBT} = \overline{EBE} = V_{CC}$ (ECL, TTL)
V <sub>OLT</sub>	Output Low Voltage, TTL					0.5			V	$F_S = GND$
V <sub>OHT</sub>	Output High Voltage, TTL			2.4					V	$F_S = GND$
V <sub>OLE</sub>	Output Low Voltage, ECL			3.0		3.4			V	$V_{CC} = 5.0V, R_L = 50\Omega,$ $V_T = 3.0V$
V <sub>OHE</sub>	Output High Voltage, ECL			3.9		4.19			V	$V_{CC} = 5.0V, R_L = 50\Omega,$ $V_T = 3.0V$
I <sub>ILT</sub>	$\overline{EBT}$ Input Low Current					400			$\mu A$	$V_{IN} = 0.4V$
I <sub>IHT</sub>	$\overline{EBT}$ Input High Current					20			$\mu A$	$V_{IN} = 2.7V$
						100			$\mu A$	$V_{IN} = 7.0V$
I <sub>INHE</sub>	EBE Input High Current					250			$\mu A$	$V_{IN} = 4.19V$
I <sub>INLE</sub>	EBE Input Low Current			1.0					$\mu A$	$V_{IN} = 3.05V$
V <sub>ILS</sub>	FS Input, Max "L" Level					1.2			V	$V_{CC} = 5.0V$
V <sub>IMS</sub>	FS Input, "Medium" Level			2.0		3.0			V	$V_{CC} = 5.0V$
V <sub>IHS</sub>	FS Input, Min "H" Level			3.8					V	$V_{CC} = 5.0V$
V <sub>ILT</sub>	$\overline{EBT}$ Input Low Voltage		0.8			0.8	0.8		V	
V <sub>IHT</sub>	$\overline{EBT}$ Input High Voltage	2.0		2.0			2.0		V	
V <sub>IHE</sub>	EBE Input High Voltage			3.87		4.19			V	$V_{CC} = 5.0V$
V <sub>ILE</sub>	EBE Input Low Voltage			3.05		3.52			V	$V_{CC} = 5.0V$
V <sub>LM</sub>	V <sub>C</sub> Input Voltage, $V_C = V_{CC} \div 2$			$\pm 1.1$	$\pm 1.3$	$\pm 1.5$			V	$V_{CC} = 5.0V$
V <sub>CB</sub>	C <sub>B</sub> Output Voltage			2.35	2.50	2.65			V	$V_{CC} = 5.0V$

**AC CHARACTERISTICS** ( $V_{CC} = 5.0V$ ;  $R_X = 2.4k\Omega$ ;  $R_Y = 1.5k\Omega$ ;  $C_B = 0.001\mu F$ ;  $V_T = 3.0V$ )

Symbol	Characteristic	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
FO	Center Frequency ( $V_{VC} - V_{CB} = 0V$ )			180	200	220			MHz	$V_{CC} = +2.0V$ $V_{EE} = -3.0V$
F <sub>MAX</sub> - F <sub>MIN</sub>	Frequency Range ( $V_C = 1/2 V_{CC} \pm 1.5V, V_{CC} = 5.0V$ )			85	100	115			MHz	
t <sub>rE</sub>	FOE/ $\overline{FOE}$ /FSE/ $\overline{FSE}$ Rise Time			0.5		2.4			ns	
t <sub>fE</sub>	FOE/ $\overline{FOE}$ /FSE/ $\overline{FSE}$ Fall Time			0.5		2.4			ns	
TTT	Reset Time					35			ns	$\overline{EBT} \sim FST$
TTO	Reset Time					25			ns	$\overline{EBT} \sim FOE/\overline{FOE}$
TTS	Reset Time					30			ns	$\overline{EBT} \sim FSE/\overline{FSE}$
TET	Reset Time					37			ns	$\overline{EBE} \sim FST$
TEO	Reset Time					12			ns	$\overline{EBE} \sim FOE/\overline{FOE}$
TES	Reset Time					25			ns	$\overline{EBE} \sim FSE/\overline{FSE}$

Loading: ECL = 50Ω to V<sub>T</sub>; TTL = 500Ω, 50pF

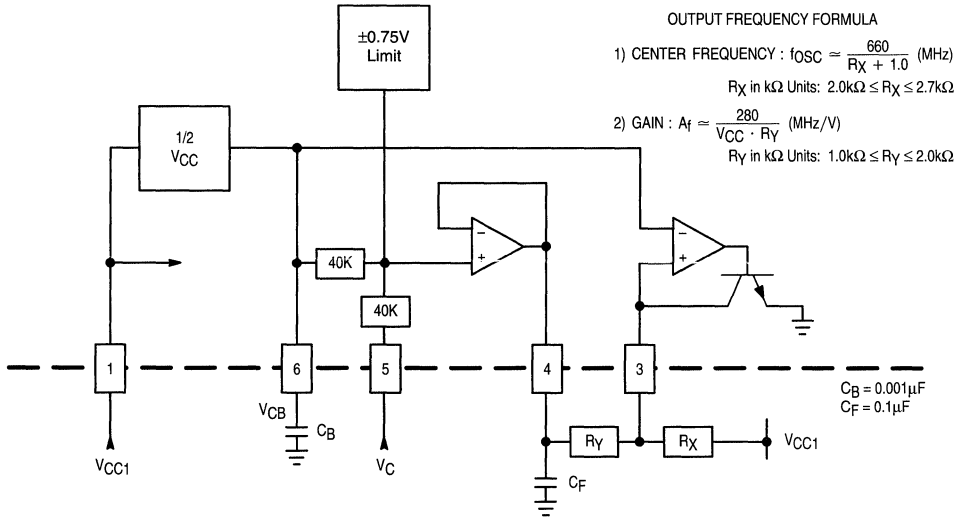


Figure 2. VCO Detail

**Notes:**

- For optimum VCO linearity (MHz/V), the following resistor ranges are recommended:  
 $2.0k\Omega \leq R_X \leq 2.7k\Omega$  ( $R_Y = 1.5k\Omega$ )  
 $1.0k\Omega \leq R_Y \leq 2.0k\Omega$  ( $R_X = 2.4k\Omega$ )
- TTL output maximum frequency = 50MHz
- Simultaneous use of both ECL and TTL outputs are not recommended due to excessive power consumption for the EIAJ Type II SO package

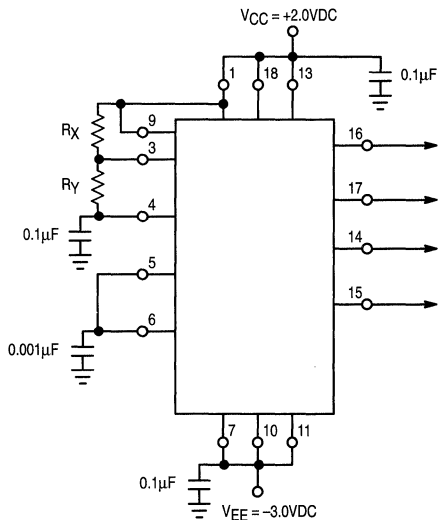


Figure 3. AC Test Circuit (FO/ $t_{RE}$ / $t_{FE}$  Measurement)

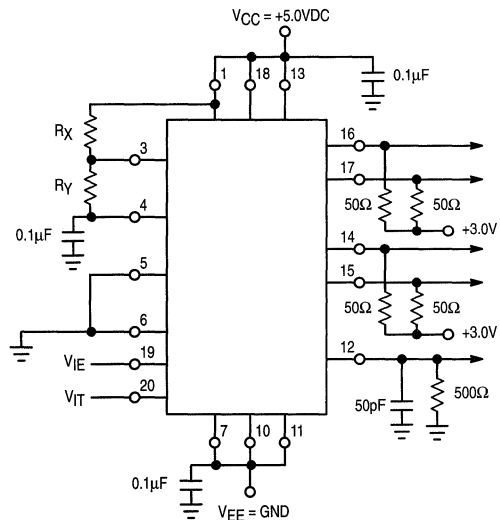
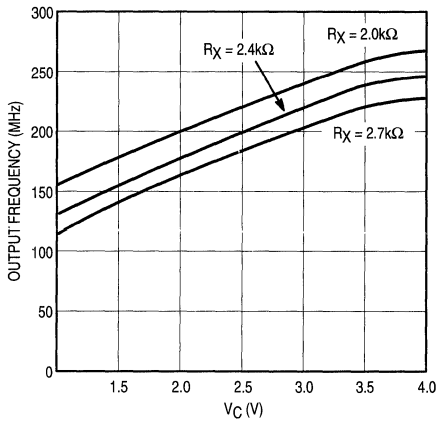
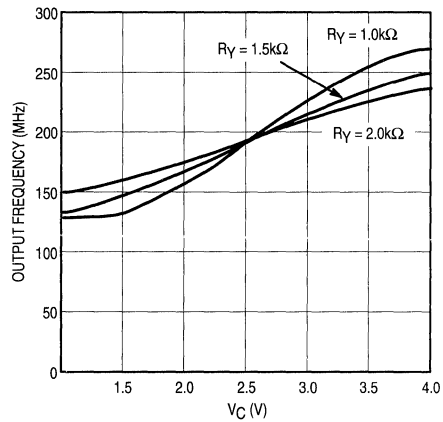


Figure 4. AC Test Circuit (Other Measurements)

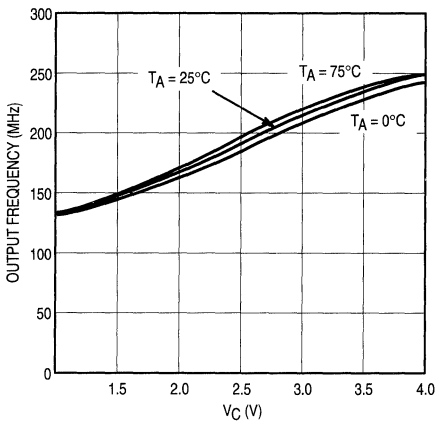




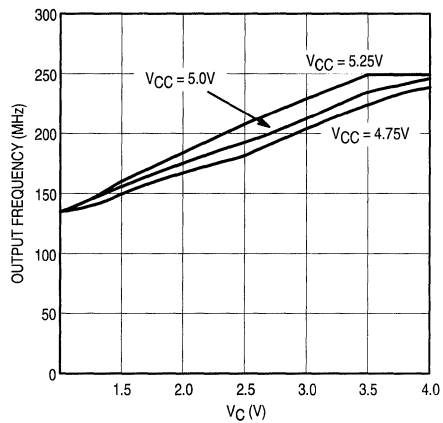
**Figure 6.  $V_C$  versus Output Frequency**  
 Varying  $R_X$  @  $V_{CC} = 5.0V$ ;  $T_A = 25^\circ C$ ;  $R_Y = 1.5k\Omega$



**Figure 7.  $V_C$  versus Output Frequency**  
 Varying  $R_Y$  @  $V_{CC} = 5.0V$ ;  $T_A = 25^\circ C$ ;  $R_X = 2.4k\Omega$



**Figure 8.  $V_C$  versus Output Frequency**  
 Varying  $T_A$  @  $V_{CC} = 5.0V$ ;  $R_X = 2.4k\Omega$ ;  $R_Y = 1.5k\Omega$

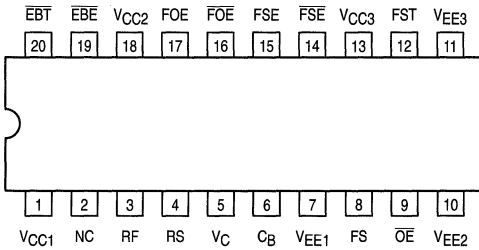


**Figure 9.  $V_C$  versus Output Frequency**  
 Varying  $V_{CC}$  @  $R_X = 2.4k\Omega$ ;  $R_Y = 1.5k\Omega$ ;  $T_A = 25^\circ C$

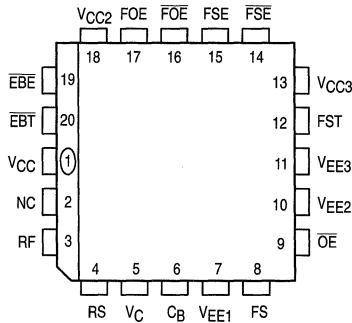
# 130MHz Voltage Controlled Multivibrator

- High Frequency VCM Ideal for PLL Applications
- Single External Resistor Determines Center Frequency; Additional Resistor Determines f/V Sensitivity
- Internal Ripple Counter (1/2, 1/4, 1/8) for Low Frequency Applications, TTL/ECL Outputs
- VCO Output Enable Pins (TTL/ECL Level)
- +5.0V Single Supply Voltage
- Packages: DIP, PLCC

**Pinout: 20-Lead Plastic Package (Top View)**

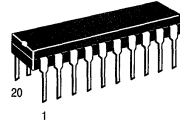


**Pinout: 20-Lead PLCC Package (Top View)**



**MC12101**

**130MHz VOLTAGE  
CONTROLLED  
MULTIVIBRATOR**



**P SUFFIX**  
PLASTIC DIP PACKAGE  
CASE 738-03



**FN SUFFIX**  
PLCC PACKAGE  
CASE 775-02

**PIN NAMES**

Pin	Function
RF, RS	Center Frequency Inputs
VC	Frequency Control Input
CB	Bias Filter Input
FS	Frequency Select Input
OE	TTL Output Enable
FST	TTL +2, +4, +8 Output
FSE, FSE	Diff ECL +2, +4, +8 Outputs
FOE, FOE	Diff ECL +1 Outputs
EBE	VCO Disable, ECL Level Input
EBT	VCO Disable, TTL Level Input





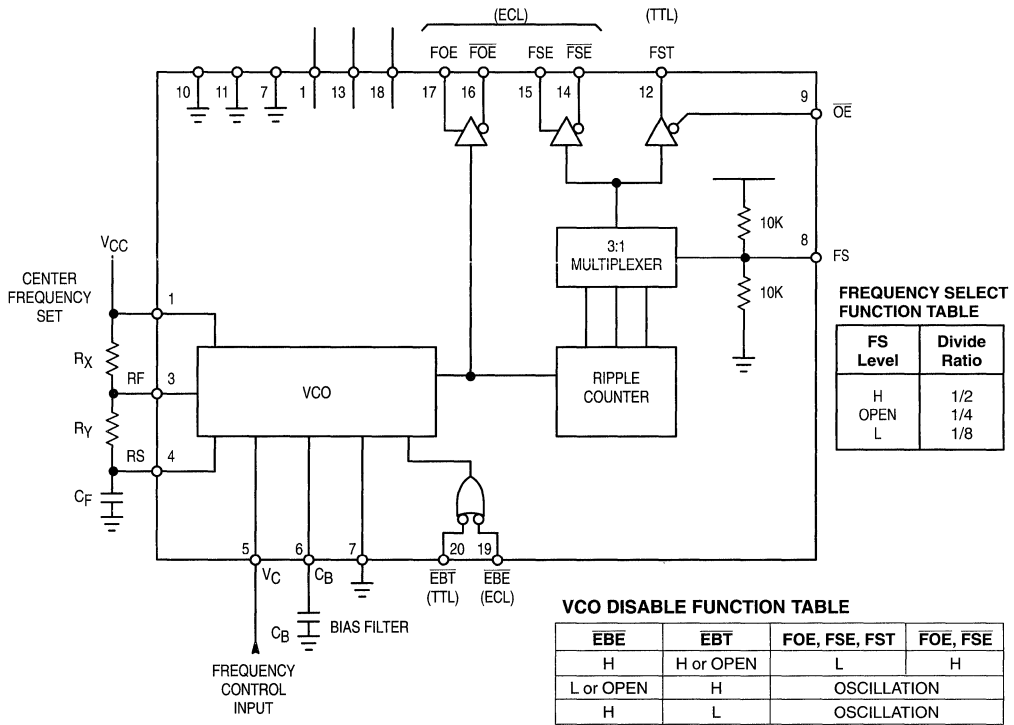


Figure 1. Block Diagram

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>CC1</sub> V <sub>CC2</sub> V <sub>CC3</sub>	Power Supply Voltage	-0.5 to +8.0	V
V <sub>IN</sub> (TTL)	Input Voltage	-0.5 to V <sub>CC</sub>	V
V <sub>IN</sub> (ECL)	Input Voltage	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub> (ECL)	Output Source Current – Surge	100	mA
	Output Source Current – Continuous	50	mA
T <sub>J</sub>	Junction Operating Temperature	+140	°C
T <sub>STG</sub>	Storage Temperature	-55 to +150	°C

**OPERATING CONDITIONS**

Symbol	Parameter	Value	Unit
T <sub>A</sub>	Ambient Temperature	0 to +75	°C
V <sub>CC</sub>	Supply Voltage	+4.75 to +5.25	V
I <sub>OH</sub> (TTL)	TTL High Output Current	-1.0	mA
I <sub>OL</sub> (TTL)	TTL Low Output Current	20	mA

# MC12101

## DC CHARACTERISTICS ( $V_{CC} = 5.0V \pm 5\%$ ; $R_X = 2.4k\Omega$ ; $R_Y = 1.5k\Omega$ ; $C_B = 0.001\mu F$ )

Symbol	Characteristic	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
I <sub>CC</sub>	Supply Current	80	135	70	100	120	85	150	mA	EBT = EBE = V <sub>CC</sub> (ECL, TTL)
V <sub>OLT</sub>	Output Low Voltage, TTL					0.5			V	F <sub>S</sub> = GND
V <sub>OHT</sub>	Output High Voltage, TTL			2.4					V	F <sub>S</sub> = GND
V <sub>OLE</sub>	Output Low Voltage, ECL			3.0		3.4			V	V <sub>CC</sub> = 5.0V, R <sub>L</sub> = 50Ω, V <sub>T</sub> = 3.0V
V <sub>OHE</sub>	Output High Voltage, ECL			3.9		4.19			V	V <sub>CC</sub> = 5.0V, R <sub>L</sub> = 50Ω, V <sub>T</sub> = 3.0V
I <sub>ILT</sub>	$\overline{EBT}$ Input Low Current					400			μA	V <sub>IN</sub> = 0.4V
I <sub>IHT</sub>	$\overline{EBT}$ Input High Current					20			μA	V <sub>IN</sub> = 2.7V
						100			μA	V <sub>IN</sub> = 7.0V
I <sub>INHE</sub>	$\overline{EBE}$ Input High Current					250			μA	V <sub>IN</sub> = 4.19V
I <sub>INLE</sub>	$\overline{EBE}$ Input Low Current			1.0					μA	V <sub>IN</sub> = 3.05V
V <sub>ILS</sub>	FS Input, Max "L" Level					1.2			V	V <sub>CC</sub> = 5.0V
V <sub>IMS</sub>	FS Input, "Medium" Level			2.0		3.0			V	V <sub>CC</sub> = 5.0V
V <sub>IHS</sub>	FS Input, Min "H" Level			3.8					V	V <sub>CC</sub> = 5.0V
V <sub>ILT</sub>	$\overline{EBT}$ Input Low Voltage		0.8					0.8	V	
V <sub>IHT</sub>	$\overline{EBT}$ Input High Voltage	2.0		2.0			2.0		V	
V <sub>IHE</sub>	$\overline{EBE}$ Input High Voltage			3.87		4.19			V	V <sub>CC</sub> = 5.0V
V <sub>ILE</sub>	$\overline{EBE}$ Input Low Voltage			3.05		3.52			V	V <sub>CC</sub> = 5.0V
V <sub>LM</sub>	V <sub>C</sub> Input Voltage, V <sub>C</sub> = V <sub>CC</sub> + 2			±1.1	±1.3	±1.5			V	V <sub>CC</sub> = 5.0V
V <sub>CB</sub>	C <sub>B</sub> Output Voltage			2.35	2.50	2.65			V	V <sub>CC</sub> = 5.0V

## AC CHARACTERISTICS ( $V_{CC} = 5.0V$ ; $R_X = 2.4k\Omega$ ; $R_Y = 1.5k\Omega$ ; $C_B = 0.001\mu F$ ; $V_T = 3.0V$ )

Symbol	Characteristic	0°C		25°C			75°C		Unit	Condition
		Min	Max	Min	Typ	Max	Min	Max		
FO	Center Frequency (V <sub>C</sub> - V <sub>CB</sub> = 0V)			117	130	143			MHz	V <sub>CC</sub> = +2.0V V <sub>EE</sub> = -3.0V
F <sub>MAX</sub> - F <sub>MIN</sub>	Frequency Range (V <sub>C</sub> = 1/2 V <sub>CC</sub> ± 1.5V, V <sub>CC</sub> = 5.0V)			68	80	92			MHz	
t <sub>rE</sub>	FOE/ $\overline{FOE}$ /FSE/FSE Rise Time			0.5		2.4			ns	
t <sub>fE</sub>	FOE/ $\overline{FOE}$ /FSE/FSE Fall Time			0.5		2.4			ns	
TTT	Reset Time					40			ns	$\overline{EBT}$ ~ FST
TTO	Reset Time					25			ns	$\overline{EBT}$ ~ FOE/ $\overline{FOE}$
TTS	Reset Time					35			ns	$\overline{EBT}$ ~ FSE/FSE
TET	Reset Time					32			ns	$\overline{EBE}$ ~ FST
TEO	Reset Time					12			ns	$\overline{EBE}$ ~ FOE/ $\overline{FOE}$
TES	Reset Time					30			ns	$\overline{EBE}$ ~ FSE/FSE

Loading: ECL = 50Ω to V<sub>T</sub>; TTL = 500Ω, 50pF

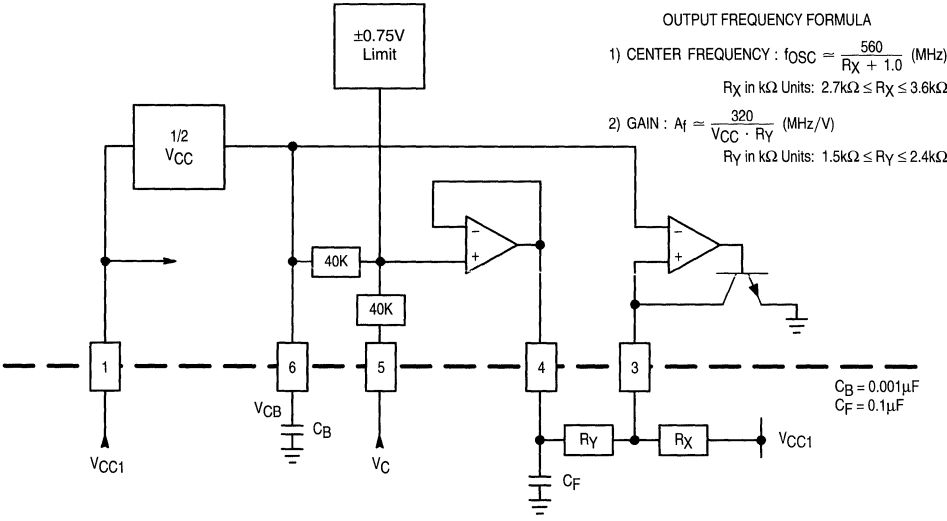


Figure 2. VCO Detail

**Notes:**

- For optimum VCO linearity (MHz/V), the following resistor ranges are recommended:  
 $3.6k\Omega \leq R_X \leq 4.6k\Omega$  ( $R_Y = 2.0k\Omega$ )  
 $1.5k\Omega \leq R_Y \leq 2.4k\Omega$  ( $R_X = 3.3k\Omega$ )
- TTL output maximum frequency = 50MHz
- Simultaneous use of both ECL and TTL outputs are not recommended due to excessive power consumption for the EIAJ Type II SO package

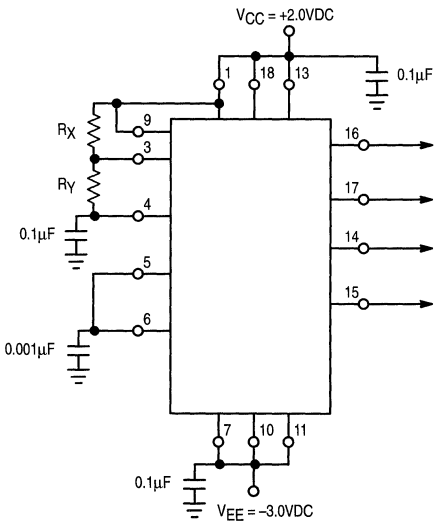


Figure 3. AC Test Circuit (FO/t<sub>rE</sub>/t<sub>fE</sub> Measurement)

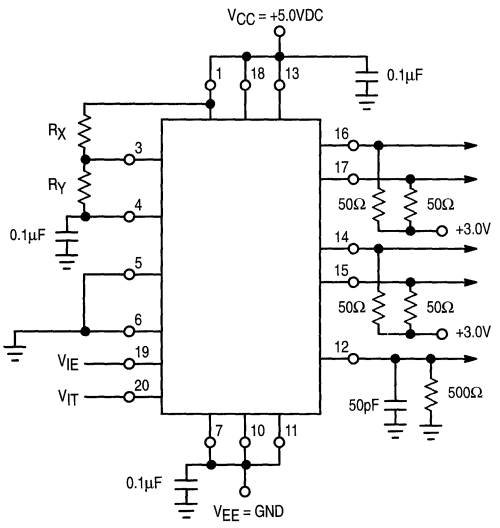


Figure 4. AC Test Circuit (Other Measurements)

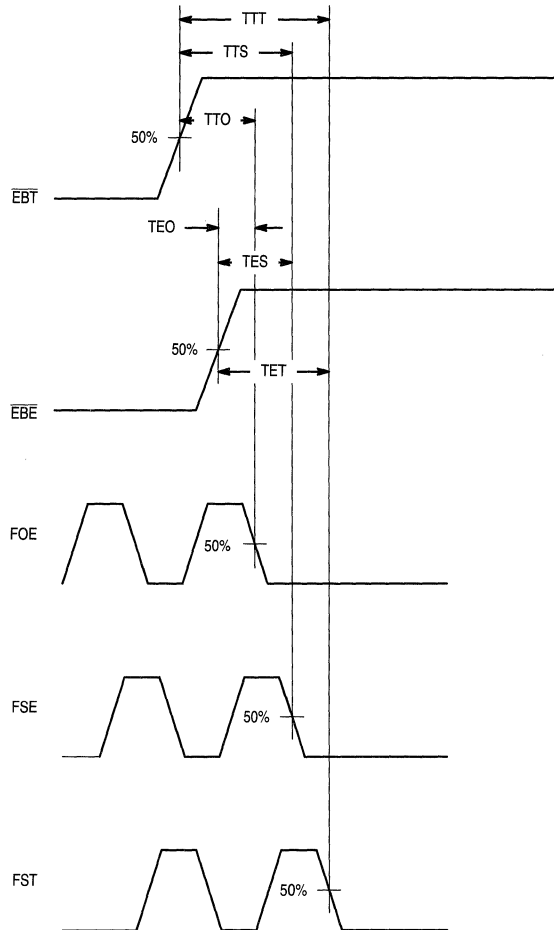
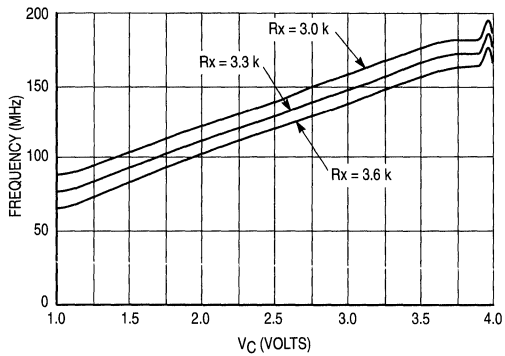


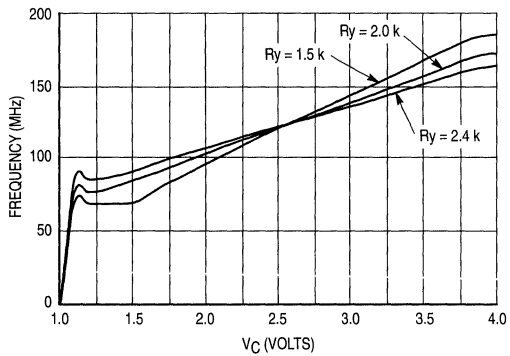
Figure 5. Switching Waveforms

VCO DISABLE FUNCTION TABLE

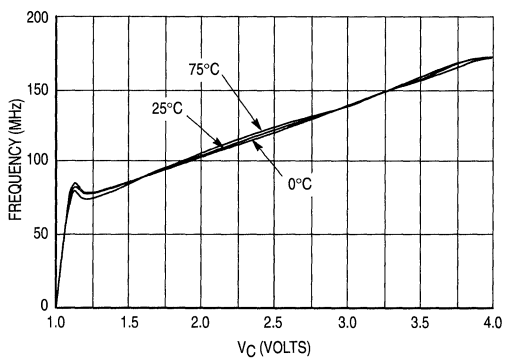
EBE	EBT	FOE, FSE, FST	FOE, FSE
H	H or OPEN	L	H
L or OPEN	H	OSCILLATION	
H	L	OSCILLATION	



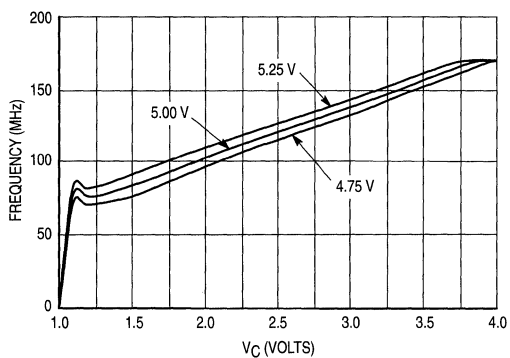
**Figure 6. V<sub>C</sub> versus Output Frequency**  
 Varying R<sub>x</sub> @ V<sub>CC</sub> = 5.0 V; T<sub>A</sub> = 25°C; R<sub>y</sub> = 2.0 kΩ



**Figure 7. V<sub>C</sub> versus Output Frequency**  
 Varying R<sub>y</sub> @ V<sub>CC</sub> = 5.0 V; T<sub>A</sub> = 25°C; R<sub>x</sub> = 3.3 kΩ



**Figure 8. V<sub>C</sub> versus Output Frequency**  
 Varying T<sub>A</sub> @ V<sub>CC</sub> = 5.0 V; R<sub>x</sub> = 3.3 kΩ; R<sub>y</sub> = 2.0 kΩ



**Figure 9. V<sub>C</sub> versus Output Frequency**  
 Varying V<sub>CC</sub> @ R<sub>x</sub> = 3.3 kΩ; R<sub>y</sub> = 2.0 kΩ; T<sub>A</sub> = 25°C

## Low Power Voltage Controlled Oscillator Buffer

The MC12147 is intended for applications requiring high frequency signal generation up to 1300MHz. An external tank circuit is used to determine the desired frequency of operation. The VCO is realized using an emitter-coupled pair topology. The MC12147 can be used with an integrated PLL IC such as the MC12202 1.1GHz Frequency Synthesizer to realize a complete PLL sub-system. The device is specified to operate over a voltage supply range of 2.7V to 5.5V. It has a typical current consumption of 13mA at 3V which makes it attractive for battery operated handheld systems.

**NOTE:** The MC12147 is NOT suitable as a crystal oscillator.

- Operates Up to 1.3GHz
- Space-Efficient 8-Pin SOIC or SSOP Package
- Low Power 13mA Typical @ 3.0V Operation
- Supply Voltage of 2.7 to 5.5V
- Typical 900MHz Performance
  - Phase Noise  $-105\text{dBc/Hz}$  @ 100KHz Offset
  - Tuning Voltage Sensitivity of 20MHz/V
- Output Amplitude Adjustment Capability
- Two High Drive Outputs With a Typical Range from  $-8\text{dBm}$  to  $-2\text{dBm}$

The device has two high frequency outputs which make it attractive for transceiver applications which require both a transmit and receive local oscillator (LO) signal. The outputs Q and QB are available for servicing the receiver IF and transmitter up-converter single-ended. In receiver applications, the outputs can be used together if it is necessary to generate a differential signal for the receiver IF. Because the Q and QB outputs are open collector, terminations to the  $V_{CC}$  supply are required for proper operation. Since the outputs are complementary, BOTH outputs must be terminated even if only one is needed. The Q and QB outputs have a nominal drive level of  $-8\text{dBm}$  to conserve power. If addition signal amplitude is needed, a level adjustment pin (CNTL) is available, which when tied to ground, boosts the nominal output levels to  $-2\text{dBm}$ .

External components required for the MC12147 are: (1) tank circuit (LC network); (2) Inductor/capacitor to provide the termination for the open collector outputs; and (3) adequate supply voltage bypassing. The tank circuit consists of a high-Q inductor and varactor components. The preferred tank configuration allows the user to tune the VCO across the full supply range. VCO performance such as center frequency, tuning voltage sensitivity, and noise characteristics are dependent on the particular components and configuration of the VCO tank circuit.

**MC12147**

**LOW POWER VOLTAGE  
CONTROLLED OSCILLATOR  
BUFFER**



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-03

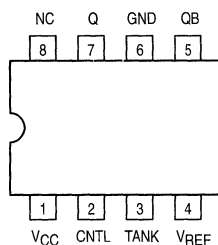


**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-03



## PIN NAMES

Pin	Function
V <sub>CC</sub>	Power Supply
CNTL	Amplitude Control for Q, QB Output Pair
TANK	Tank Circuit Input
V <sub>REF</sub>	Bias Voltage Output
QB	Open Collector Output
GND	Ground
Q	Open Collector Output



Pinout: 8-Lead Plastic Package (Top View)

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 1	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
I <sub>O</sub>	Maximum Output Current, Pin 5,7	12	mA

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 2.7 to 5.5 VDC, T<sub>A</sub> = -40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I <sub>CC</sub>	Supply Current (CNTL=GND) V <sub>CC</sub> = 3.3V V <sub>CC</sub> = 5.5V		14.0 23.5	18 28	mA
I <sub>CC</sub>	Supply Current (CNTL=OPEN) V <sub>CC</sub> = 3.3V V <sub>CC</sub> = 5.5V		8 13	13.0 22.5	mA
V <sub>OH</sub> , V <sub>OL</sub>	Output Amplitude (Pin 5 & 7) V <sub>CC</sub> = 2.7V 50Ω to V <sub>CC</sub> V <sub>CC</sub> = 2.7V	2.6 2.1	2.7 2.3	2.4	V
V <sub>OH</sub> , V <sub>OL</sub>	Output Amplitude (Pin 5 & 7) V <sub>CC</sub> = 5.5V 50Ω to V <sub>CC</sub> V <sub>CC</sub> = 5.5V	5.4 4.8	5.5 5.0	5.1	V
T <sub>stg</sub>	Tuning Voltage Sensitivity <sup>2,3</sup>		20		MHz/V
F <sub>C</sub>	Frequency of Operation	100		1300	MHz
L(f)	CSR at 10KHz Offset, 1Hz BW <sup>2,3</sup>		-85		dBc/Hz
L(f)	CSR at 100KHz Offset, 1Hz BW <sup>2,3</sup>		-105		dBc/Hz
F <sub>sts</sub> , f <sub>stt</sub>	Frequency Stability <sup>3,4</sup> Supply Drift Thermal Drift		0.8 50		MHz/V KHz/°C

1. CNTL pin tied to ground.
2. Actual performance depends on tank components selected.
3. See Figure 12, 750MHz tank.
4. T = 25°C, V<sub>CC</sub> = 5V ±10%

## OPERATIONAL CHARACTERISTICS

A simplified schematic of the MC12147 is found in Figure 1. The oscillator incorporates positive feedback by coupling the base of transistor Q2 to the collector of transistor Q1. In order to minimize interaction between the VCO outputs and the oscillator tank transistor pair, a buffer is incorporated into the circuit. This differential buffer is realized by the Q3 and Q4 transistor pair. The differential buffer drives the gate which contains the primary open collector outputs, Q and QB. The output is actually a current which has been set by an internal bias driver to a nominal current of 4mA. Additional circuitry is incorporated into the tail of the current source which allows the current source to be increased to approximately 10mA. This is accommodated by the addition of a resistor which is brought out to the CNTL pin. When this pin is tied to ground, the additional current is sourced through the current source thus increasing the output amplitude of the Q/QB output pair. If less than 10mA of current is needed, a resistor can be added to ground which reduces the amount of current.

### APPLICATION INFORMATION

Figure 2 illustrates the external components necessary for the proper operation of the VCO buffer. The tank circuit configuration in this figure allows the VCO to be tuned across the full operating voltage of the power supply. This is very important in 3V applications where it is desirable to utilize as much of the operating supply range as possible so as to minimize the VCO sensitivity (MHz/V). In most situations, it is desirable to keep the sensitivity low so the circuit will be less susceptible to external noise influences. An additional benefit to this configuration is that additional regulation/ filtering can

be incorporated into the VCC line without compromising the tuning range of the VCO. With the AC-coupled tank configuration, the V<sub>tune</sub> voltage can be greater than the VCC voltage supplied to the device.

There are four main areas that the user directly influences the performance of the VCO. These include Tank Design, Output Termination Selection, Power Supply Decoupling, and Circuit Board Layout/Grounding.

The design of the tank circuit is critical to the proper operation of the VCO. This tank circuit directly impacts the main VCO operating characteristics:

- 1) Frequency of Operation
- 2) Tuning Sensitivity
- 3) Voltage Supply Pushing
- 4) Phase Noise Performance

The tank circuit, in its simplest form, is realized as an LC circuit which determines the VCO operating frequency. This is described in Equation 1.

$$f_o = \frac{1}{2\pi \sqrt{LC}} \quad \text{Equation 1}$$

In the practical case, the capacitor is replaced with a varactor diode whose capacitance changes with the voltage applied, thus changing the resonant frequency at which the VCO tank operates. The capacitive component in Equation 1 also needs to include the input capacitance of the device and other circuit and parasitic elements. Typically, the inductor is realized as a surface mount chip or a wound-coil. In addition, the lead inductance and board inductance and capacitance also have an impact on the final operating point.

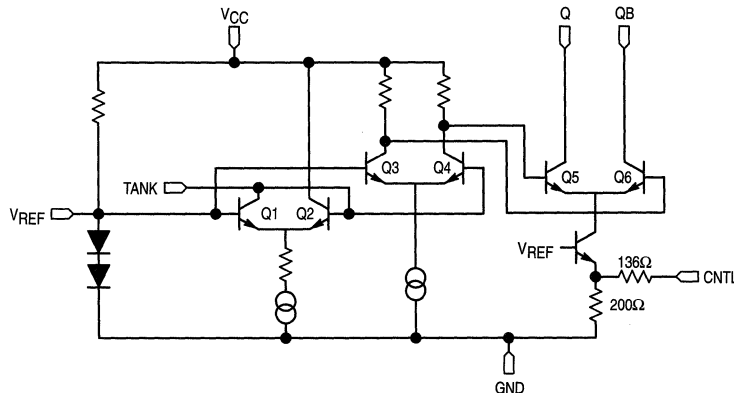
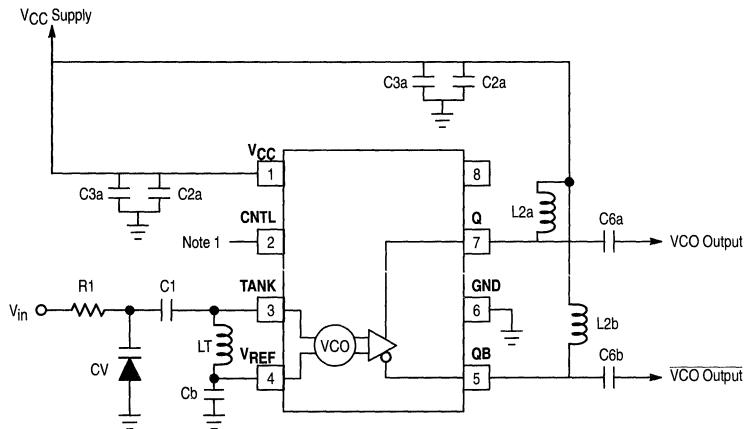


Figure 1. Simplified Schematic





1. This input can be left open, tied to ground, or tied with a resistor to ground, depending on the desired output amplitude needed at the Q and QB output pair.
2. Typical values for R1 range from 5k $\Omega$  to 10k $\Omega$ .

**Figure 2. MC12147 Typical External Component Connections**

A simplified linear approximation of the device, package, and typical board parasitics has been developed to aid the designer in selecting the proper tank circuit values. All the parasitic contributions have been lumped into a parasitic capacitive component and a parasitic inductive component. While this is not entirely accurate, it gives the designer a solid starting point for selecting the tank components.

Below are the parameters used in the model.

Cp	Parasitic Capacitance
Lp	Parasitic Inductance
LT	Inductance of Coil
C1	Coupling Capacitor Value
Cb	Capacitor for decoupling the Bias Pin
CV	Varactor Diode Capacitance (Variable)

The values for these components are substituted into the following equations:

$$C_i = \frac{C_1 \times CV}{C_1 + CV} + C_p \quad \text{Equation 2}$$

$$C = \frac{C_i \times C_b}{C_i + C_b} \quad \text{Equation 3}$$

$$L = L_p + LT \quad \text{Equation 4}$$

From Figure 2, it can be seen that the varactor capacitance (CV) is in series with the coupling capacitor (C1). This is calculated in Equation 2. For analysis purposes, the parasitic capacitances (CP) are treated as a lumped element and placed in parallel with the series combination of C1 and CV. This compound capacitance (Ci) is in series with the bias capacitor (Cb) which is calculated in Equation 3. The influences of the various capacitances; C1, CP, and Cb,

impact the design by reducing the variable capacitance effects of the varactor which controls the tank resonant frequency and tuning range.

Now the results calculated from Equation 2, Equation 3 and Equation 4 can be substituted into Equation 1 to calculate the actual frequency of the tank.

To aid in analysis, it is recommended that the designer use a simple spreadsheet based on Equation 1 through Equation 4 to calculate the frequency of operation for various varactor/inductor selections before determining the initial starting condition for the tank.

The two main components at the heart of the tank are the inductor (LT) and the varactor diode (CV). The capacitance of a varactor diode junction changes with the amount of reverse bias voltage applied across the two terminals. This is the element which actually "tunes" the VCO. One characteristic of the varactor is the tuning ratio which is the ratio of the capacitance at specified minimum and maximum voltage points. For characterizing the MC12147, a Matsushita (Panasonic) varactor – MA393 was selected. This device has a typical capacitance of 11 pF at 1V and 3.7 pF at 4V and the C–V characteristic is fairly linear over that range. Similar performance was also achieved with Loral varactors. A multi-layer chip inductor was used to realize the LT component. These inductors had typical Q values in the 35–50 range for frequencies between 500 and 1000MHz.

**Note:** There are many suppliers of high performance varactors and inductors a Motorola can not recommend one vendor over another.

The Q (quality factor) of the components in the tank circuit has a direct impact on the resulting phase noise of the oscillator. In general, the higher the Q, the lower the phase noise of the resulting oscillator. In addition to the LT and CV

components, only high quality surface-mount RF chip capacitors should be used in the tank circuit. These capacitors should have very low dielectric loss (high-Q). At a minimum, the capacitors selected should be operating 100 MHz below their series resonance point. As the desired frequency of operation increases, the values of the C1 and Cb capacitors will decrease since the series resonance point is a function of the capacitance value. To simplify the selection of C1 and Cb, a table has been constructed based on the intended operating frequency to provide recommended starting points. These may need to be altered depending on the value of the varactor selected.

Frequency	C1	Cb
200 – 500 MHz	47 pF	47 pF
500 – 900 MHz	5.1 pF	15 pF
900 – 1200 MHz	2.7 pF	15 pF

The value of the Cb capacitor influences the VCO supply pushing. To minimize pushing, the Cb capacitor should be kept small. Since C1 is in series with the varactor, there is a strong relationship between these two components which influences the VCO sensitivity. Increasing the value of C1 tends to increase the sensitivity of the VCO.

The parasitic contributions Lp and Cp are related to the MC12147 as well as parasitics associated with the layout, tank components, and board material selected. The input capacitance of the device, bond pad, the wire bond, package/lead capacitance, wire bond inductance, lead inductance, printed circuit board layout, board dielectric, and proximity to the ground plane all have an impact on these parasitics. For example, if the ground plane is located directly below the tank components, a parasitic capacitor will be formed consisting of the solder pad, metal traces, board dielectric material, and the ground plane. The test fixture used for characterizing the device consisted of a two sided copper clad board with ground plane on the back. Nominal values were determined by selecting a varactor and characterizing the device with a number of different tank/frequency combinations and then performing a curve fit with the data to determine values for Lp and Cp. The nominal values for the parasitic effects are seen below:

Parasitic Capacitance	Cp	4.2 pF
Parasitic Inductance	Lp	2.2 nH

These values will vary based on the users unique circuit board configuration.

#### Basic Guidelines:

1. Select a varactor with high Q and a reasonable capacitance versus voltage slope for the desired frequency range.
2. Select the value of Cb and C1 from the table above .
3. Calculate a value of inductance (L) which will result in achieving the desired center frequency. Note that L includes both LT and Lp.
4. Adjust the value of C1 to achieve the proper VCO sensitivity.
5. Re-adjust value of L to center VCO.
6. Prototype VCO design using selected components. It is important to use similar construction techniques and materials, board thickness, layout, ground plane spacing as intended for the final product.
7. Characterize tuning curve over the voltage operation conditions.
8. Adjust, as necessary, component values – L, C1, and Cb to compensate for parasitic board effects.
9. Evaluate over temperature and voltage limits.
10. Perform worst case analysis of tank component variation to insure proper VCO operation over full temperature and voltage range and make any adjustments as needed.

Outputs Q and QB are open collector outputs and need a inductor to VCC to provide the voltage bias to the output transistor. In most applications, DC-blocking capacitors are placed in series with the output to remove the DC component before interfacing to other circuitry. These outputs are complementary and should have identical inductor values for each output. This will minimize switching noise on the VCC supply caused by the outputs switching. It is important that both outputs be terminated, even if only one of the outputs is used in the application.

Referring to Figure 2, the recommended value for L2a and L2b should be 47 nH and the inductor components resonance should be at least 300 MHz greater than the maximum operating frequency. For operation above 1100 MHz, it may be necessary to reduce that inductor value to 33 nH. The recommended value for the coupling capacitors C6a, C6b, and C7 is 47 pF. Figure 2 also includes decoupling capacitors for the supply line as well as decoupling for the output inductors. Good RF decoupling practices should be used with a series of capacitors starting with high quality 100 pF chip capacitors close to the device. A typical layout is shown below in Figure 3.

The output amplitude of the Q and QB can be adjusted using the CNTL pin. Referring to Figure 1, if the CNTL pin is connected to ground, additional current will flow through the current source. When the pin is left open, the nominal current flowing through the outputs is 4 mA. When the pin is grounded, the current increases to a nominal value of 10 mA. So if a 50 ohm resistor was connected between the outputs and VCC, the output amplitude would change from 200 mV pp to 500 mV pp with an additional current drain for the device of 6 mA. To select a value between 4 and 10 mA, an external resistor can be added to ground. The equation below is used to calculate the current.

$$I_{out(nom)} = \frac{(200 + 136 + R_{ext}) \times 0.8V}{200 \times (136 + R_{ext})}$$

Figure 4 through Figure 13 illustrate typical performance achieved with the MC12147. The curves illustrate the tuning curve, supply pushing characteristics, output power, current

drain, output spectrum, and phase noise performance. In most cases, data is present for both a 750 MHz and 1200 MHz tank design. The table below illustrates the component values used in the designs.

Component	750MHz Tank	1200MHz Tank	Units
R1	5000	5000	Ω
C1	5.1	2.7	pF
LT	4.7	1.8	nH
CV	3.7@1V 11@4V	3.7@1V 11@4V	pF
Cb	100*	15	pF
C6, C7	47	33	pF
L2	47	47	nH

\* The value of Cb should be reduced to minimize pushing.

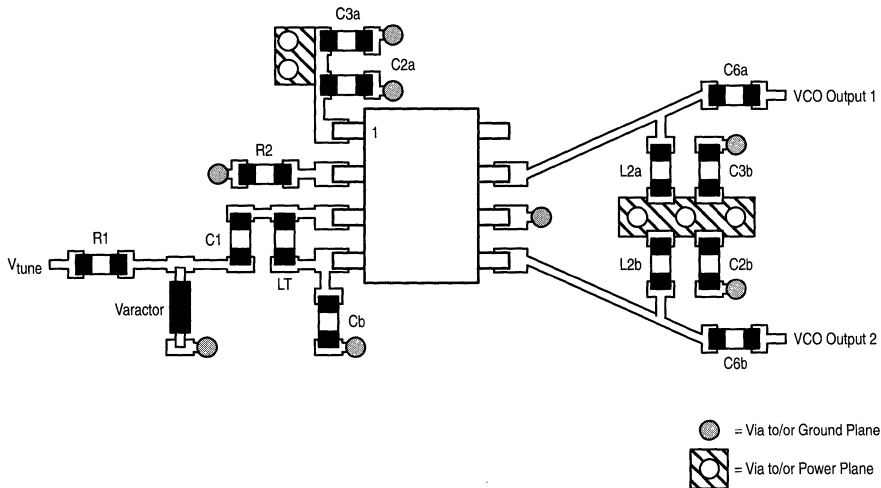


Figure 3. MC12147 Typical Layout (Not to Scale)

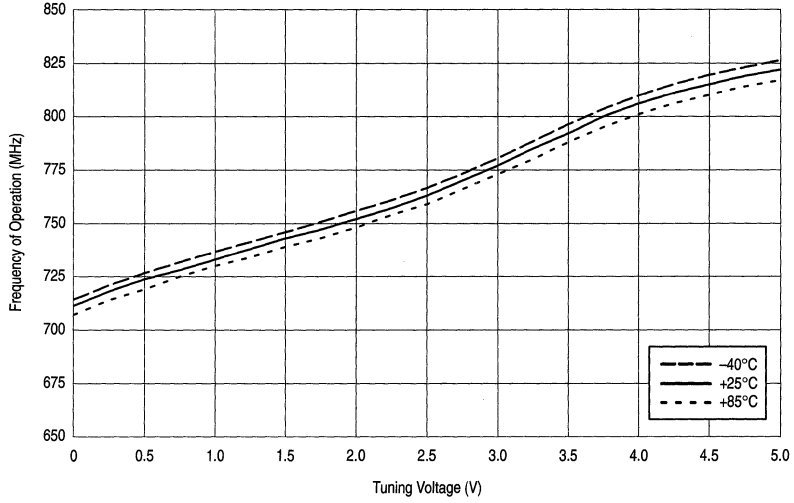


Figure 4. Typical VCO Tuning Curve, 750MHz Tank

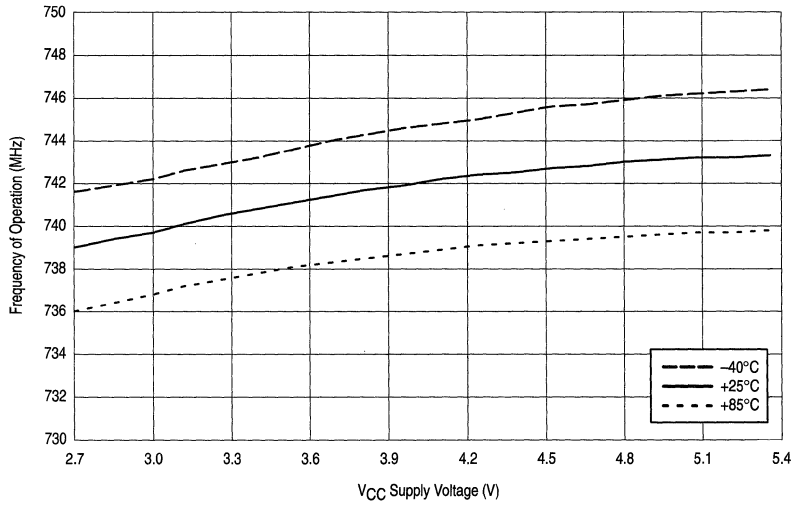


Figure 5. Typical Supply Pushing, 750MHz Tank

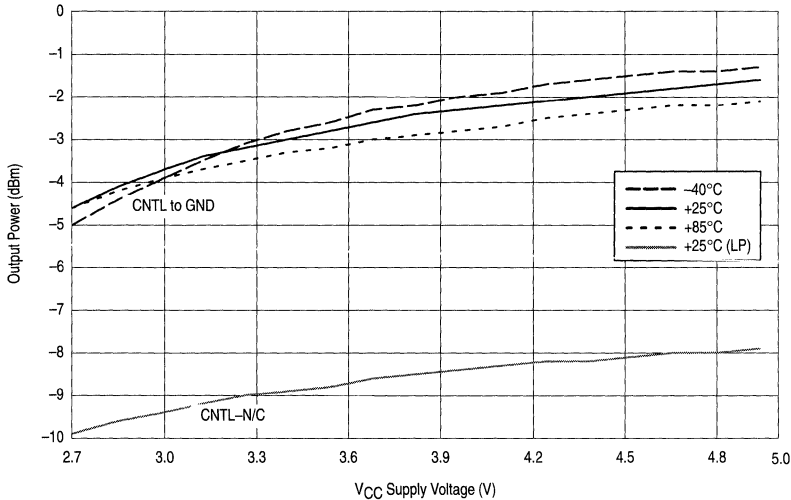


Figure 6. Typical Q/QB Output Power versus Supply, 750MHz Tank

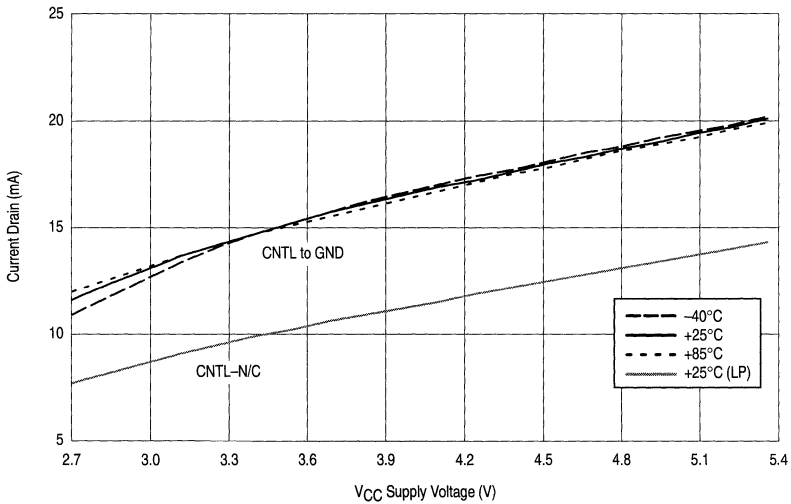


Figure 7. Typical Current Drain versus Supply, 750MHz Tank

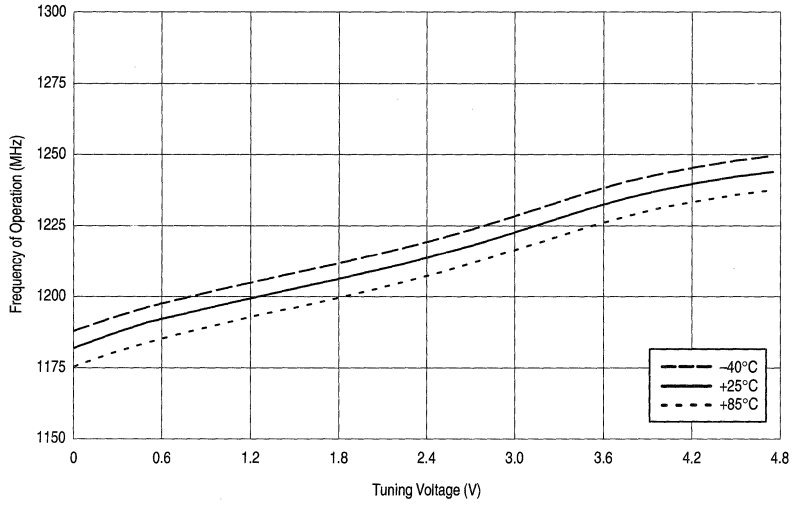


Figure 8. Typical VCO Tuning Curve, 1200MHz Tank ( $V_{CC} = 5.0V$ )

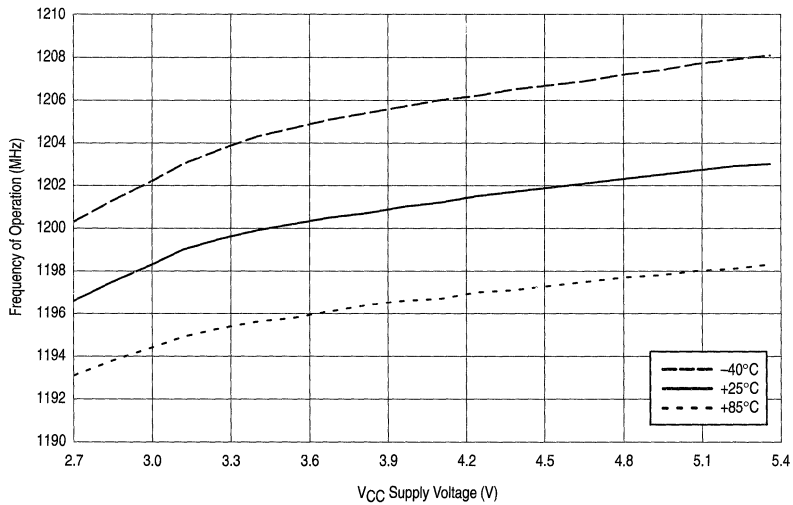


Figure 9. Typical Supply Pushing, 1200MHz Tank

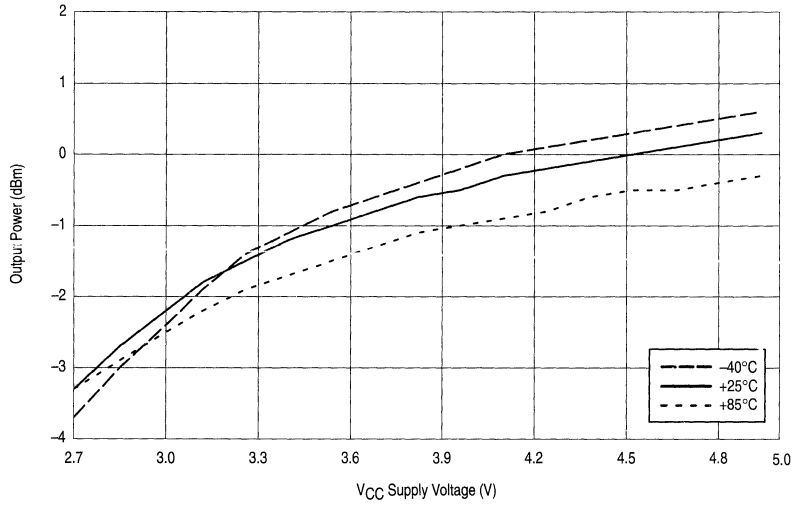


Figure 10. Q/QB Output Power versus Supply, 1200MHz Tank

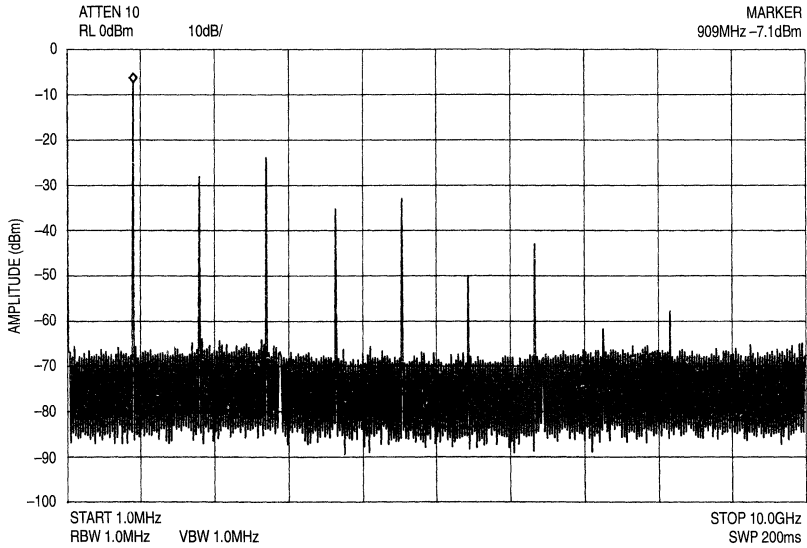


Figure 11. Typical VCO Output Spectrum

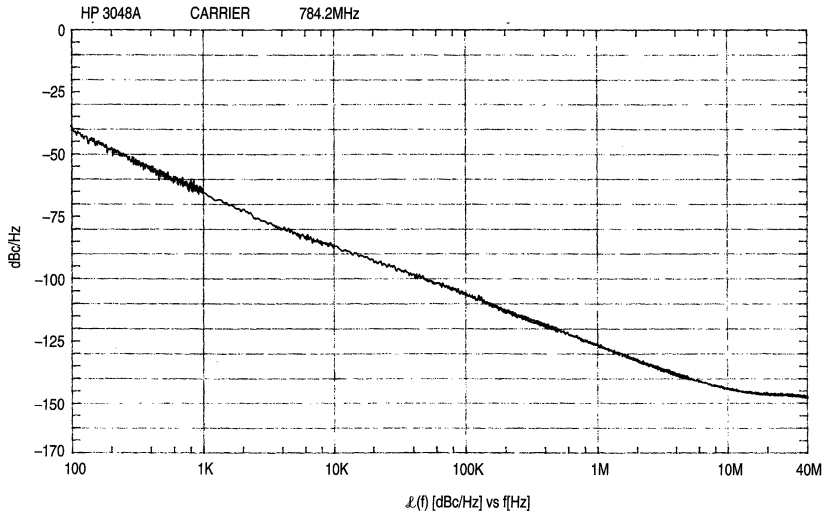


Figure 12. Typical Phase Noise Plot, 750MHz Tank

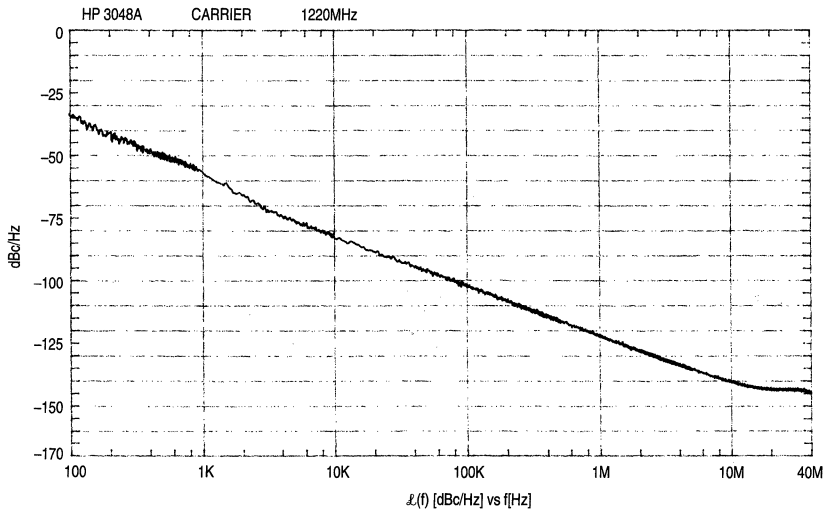


Figure 13. Typical Phase Noise Plot, 1200MHz Tank



# Low-Power Voltage Controlled Oscillator

The MC12148 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C). A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). This device may also be used in many other applications requiring a fixed frequency clock.

The MC12148 is ideal in applications requiring a local oscillator. Systems include electronic test equipment and digital high-speed telecommunications.

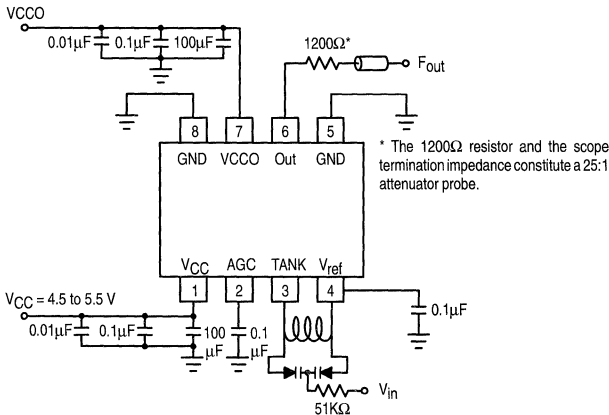
The MC12148 is based on the VCO circuit topology of the MC1648. The MC12148 has been realized utilizing Motorola's MOSAIC III advanced bipolar process technology which results in a design which can operate at a much higher frequency than the MC1648 while utilizing half the current. Please consult with the MC1648 data sheet for additional background information.

The ECL output circuitry of the MC12148 is not a traditional open emitter output structure and instead has an on-chip termination resistor with a nominal value of 500 ohms. This facilitates direct AC-coupling of the output signal into a transmission line. Because of this output configuration, an external pull-down resistor is not required to provide the output with a DC current path. This output is intended to drive one ECL load. If the user needs to fanout the signal, an ECL buffer such as the MC10EL16 Line Receiver/Driver should be used.

**NOTE: The MC12148 is NOT useable as a crystal oscillator.**

- Typical Operating Frequency Up to 1100MHz
- Low-Power 20mA at 5.0Vdc Power Supply
- 8-Pin SOIC Package
- Phase Noise -90dBc/Hz at 25KHz Typical

### BLOCK DIAGRAM (Typical Test Circuit)



## MC12148

### LOW-POWER VOLTAGE CONTROLLED OSCILLATOR

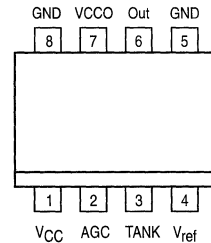


**D SUFFIX**  
SOIC PACKAGE  
CASE 751-05



**SD SUFFIX**  
SSOP PACKAGE  
CASE 940-02

### Pinout: 8-Lead SOIC (Top View)

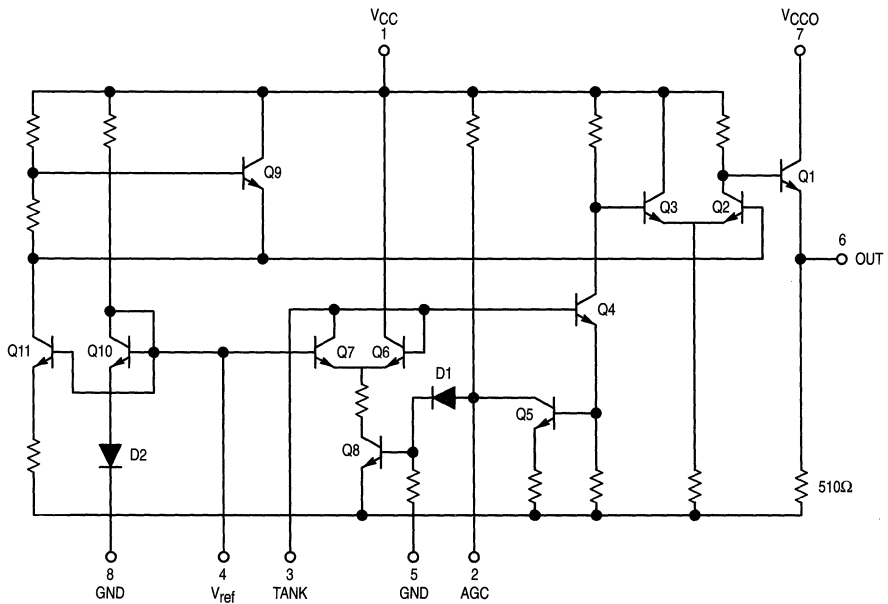


**MAXIMUM RATINGS**

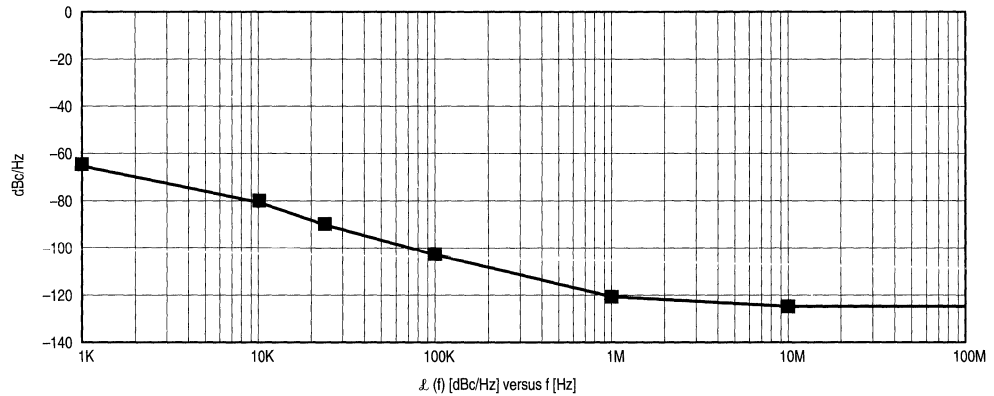
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 1	-0.5 to +7.0	Vdc
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

**ELECTRICAL CHARACTERISTICS** (V<sub>CC</sub> = 5.0V; T<sub>A</sub> = -40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I <sub>CC</sub>	Supply Current		19	25	mA
V <sub>OH</sub>	Output Level HIGH (1MΩ Impedance)	3.95	4.17	4.61	V
V <sub>OL</sub>	Output Level LOW (1MΩ Impedance)	3.04	3.41	3.60	V
ℒ(f)	CSR @ 25KHz Offset, 1Hz BW		-90		dBc/Hz
ℒ(f)	CSR @ 1MHz Offset, 1Hz BW		-120		dBc/Hz
SNR	SNR (Signal to Noise Ratio from Carrier)		40		dB
F <sub>sts</sub>	Frequency Stability	Supply Drift	3.6		KHz/mV
F <sub>st</sub>		Thermal Drift	0.1		KHz/°C
H2	Second Harmonic (from Carrier)		-25		dBc



**Figure 1. Circuit Schematic**



**Figure 2. Typical Evaluation Results**  
(CSR MC12148 5.0Vdc;  $V_{CC}$  @ 25°C; 930MHz CW)

### Tank Component Suppliers

Below are suppliers who manufacture tuning varactors and inductors which can be used to build an external tank circuit. Motorola has used these varactors and inductors for evaluation purposes, however, there are other vendors who manufacture similar products.

Coilcraft Inductors A01T thru A05T  
Coilcraft-Coilcraft, Inc.  
1102 Silver Lake Rd.  
Gary, Illinois 60013  
708-639-6400

Alpha Tuning Diodes DVH6730 Series  
Alpha Semiconductor Devices Division  
20 Sylvan Road  
Woburn, MA 01801  
617-935-5150

Loral Tuning Varactors GC1500 Series  
Loral  
16 Maple Road  
Chelmsford, Massachusetts 01824  
508-256-8101 or 508-256-4113

\* At 1.1GHz, use a Coilcraft A01T Springair coil at 2.5nH and a Loral Varactor 3–8pF at  $V_{IN} = 1$  to 5V.

## Low Power Voltage Controlled Oscillator Buffer

The MC12149 is intended for applications requiring high frequency signal generation up to 1300MHz. An external tank circuit is used to determine the desired frequency of operation. The VCO is realized using an emitter-coupled pair topology. The MC12149 can be used with an integrated PLL IC such as the MC12202 1.1GHz Frequency Synthesizer to realize a complete PLL sub-system. The device is specified to operate over a voltage supply range of 2.7V to 5.5V. It has a typical current consumption of 15mA at 3V which makes it attractive for battery operated handheld systems.

**NOTE:** The MC12149 is NOT suitable as a crystal oscillator.

- Operates Up to 1.3GHz
- Space-Efficient 8-Pin SOIC or SSOP Package
- Low Power 15mA Typical @ 3.0V Operation
- Supply Voltage of 2.7 to 5.5V
- Typical 900MHz Performance
  - Phase Noise  $-105\text{dBc/Hz}$  @ 100KHz Offset
  - Tuning Voltage Sensitivity of 20MHz/V
- Output Amplitude Adjustment Capability
- Two High Drive Outputs With a Typical Range from  $-8\text{dBm}$  to  $-2\text{dBm}$
- One Low-Drive Output for Interfacing to a Prescaler

The device has three high frequency outputs which make it attractive for transceiver applications which require both a transmit and receive local oscillator (LO) signal as well as a lower amplitude signal to drive the prescaler input of the frequency synthesizer. The outputs Q and QB are available for servicing the receiver IF and transmitter up-converter single-ended. In receiver applications, the outputs can be used together if it is necessary to generate a differential signal for the receiver IF. Because the Q and QB outputs are open collector, terminations to the VCC supply are required for proper operation. Since the outputs are complementary, BOTH outputs must be terminated even if only one is needed. The Q and QB outputs have a nominal drive level of  $-8\text{dBm}$  to conserve power. If addition signal amplitude is needed, a level adjustment pin (CNTL) is available, which when tied to ground, boosts the nominal output levels to  $-2\text{dBm}$ . A low power VCO output (Q2) is also provided to drive the prescaler input of the PLL. The amplitude of this signal is nominally 500mV which is suitable for most prescalers.

External components required for the MC12149 are: (1) tank circuit (LC network); (2) Inductor/capacitor to provide the termination for the open collector outputs; and (3) adequate supply voltage bypassing. The tank circuit consists of a high-Q inductor and varactor components. The preferred tank configuration allows the user to tune the VCO across the full supply range. VCO performance such as center frequency, tuning voltage sensitivity, and noise characteristics are dependent on the particular components and configuration of the VCO tank circuit.

**MC12149**

**LOW POWER VOLTAGE  
CONTROLLED OSCILLATOR  
BUFFER**



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-03

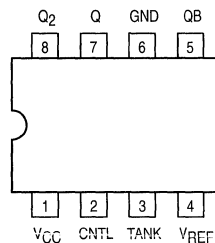


**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940-03



## PIN NAMES

Pin	Function
V <sub>CC</sub>	Power Supply
CNTL	Amplitude Control for Q, QB Output Pair
TANK	Tank Circuit Input
V <sub>REF</sub>	Bias Voltage Output
QB	Open Collector Output
GND	Ground
Q	Open Collector Output
Q <sub>2</sub>	Low Power Output



Pinout: 8-Lead Plastic Package (Top View)

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 1	-0.5 to +7.0	V
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C
I <sub>O</sub>	Maximum Output Current, Pin 8	7.5	mA
I <sub>O</sub>	Maximum Output Current, Pin 5,7	12	mA

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 2.7 to 5.5 VDC, T<sub>A</sub> = -40°C to +85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I <sub>CC</sub>	Supply Current (CNTL=GND)V <sub>CC</sub> = 3.3V V <sub>CC</sub> = 5.5V		16 23.5	20 30	mA
I <sub>CC</sub>	Supply Current (CNTL=OPEN)V <sub>CC</sub> = 3.3V V <sub>CC</sub> = 5.5V		10 15	15.0 24.5	mA
V <sub>OH</sub> , V <sub>OL</sub>	Output Amplitude (Pin 8)V <sub>CC</sub> = 2.7V High Impedance LoadV <sub>CC</sub> = 2.7V	1.75 1.20	1.85 1.35	1.95 1.50	V
V <sub>OH</sub> , V <sub>OL</sub>	Output Amplitude (Pin 8)V <sub>CC</sub> = 5.5V High Impedance LoadV <sub>CC</sub> = 5.5V	4.50 3.85	4.6 4.0	4.70 4.15	V
V <sub>OH</sub> , V <sub>OL</sub>	Output Amplitude (Pin 5 & 7) <sup>1</sup> V <sub>CC</sub> = 2.7V 50Ω to V <sub>CC</sub> V <sub>CC</sub> = 2.7V	2.6 2.1	2.7 2.3	2.4	V
V <sub>OH</sub> , V <sub>OL</sub>	Output Amplitude (Pin 5 & 7) <sup>1</sup> V <sub>CC</sub> = 5.5V 50Ω to V <sub>CC</sub> V <sub>CC</sub> = 5.5V	5.4 4.8	5.5 5.0	5.1	V
T <sub>stg</sub>	Tuning Voltage Sensitivity <sup>2,3</sup>		20		MHz/V
F <sub>C</sub>	Frequency of Operation	100		1300	MHz
ℒ(f)	CSR at 10KHz Offset, 1Hz BW <sup>2,3</sup>		-85		dBc/Hz
ℒ(f)	CSR at 100KHz Offset, 1Hz BW <sup>2,3</sup>		-105		dBc/Hz
F <sub>sts</sub> , f <sub>stt</sub>	Frequency Stability <sup>3,4</sup> Supply Drift Thermal Drift		0.8 50		MHz/V KHz/°C

1. CNTL pin tied to ground.
2. Actual performance depends on tank components selected.
3. See Figure 12, 750MHz tank.
4. T = 25°C, V<sub>CC</sub> = 5V ±10%

## OPERATIONAL CHARACTERISTICS

A simplified schematic of the MC12149 is found in Figure 1. The oscillator incorporates positive feedback by coupling the base of transistor Q2 to the collector of transistor Q1. In order to minimize interaction between the VCO outputs and the oscillator tank transistor pair, a buffer is incorporated into the circuit. This differential buffer is realized by the Q3 and Q4 transistor pair. The differential buffer drives the gate which contains the primary open collector outputs, Q and QB. The output is actually a current which has been set by an internal bias driver to a nominal current of 4mA. Additional circuitry is incorporated into the tail of the current source which allows the current source to be increased to approximately 10mA. This is accommodated by the addition of a resistor which is brought out to the CNTL pin. When this pin is tied to ground, the additional current is sourced through the current source thus increasing the output amplitude of the Q/QB output pair. If less than 10mA of current is needed, a resistor can be added to ground which reduces the amount of current.

The Q/QB outputs drive an additional differential buffer which generate the Q2 output signal. To minimize current, the circuit is realized as an emitter-follower buffer with an on chip pull down resistor. This output is intended to drive the prescaler input of the PLL synthesizer block.

### APPLICATION INFORMATION

Figure 2 illustrates the external components necessary for the proper operation of the VCO buffer. The tank circuit configuration in this figure allows the VCO to be tuned across the full operating voltage of the power supply. This is very important in 3V applications where it is desirable to utilize as much of the operating supply range as possible so as to minimize the VCO sensitivity (MHz/V). In most situations, it is desirable to keep the sensitivity low so the circuit will be less

susceptible to external noise influences. An additional benefit to this configuration is that additional regulation/ filtering can be incorporated into the VCC line without compromising the tuning range of the VCO. With the AC-coupled tank configuration, the V<sub>TUNE</sub> voltage can be greater than the VCC voltage supplied to the device.

There are four main areas that the user directly influences the performance of the VCO. These include Tank Design, Output Termination Selection, Power Supply Decoupling, and Circuit Board Layout/Grounding.

The design of the tank circuit is critical to the proper operation of the VCO. This tank circuit directly impacts the main VCO operating characteristics:

- 1) Frequency of Operation
- 2) Tuning Sensitivity
- 3) Voltage Supply Pushing
- 4) Phase Noise Performance

The tank circuit, in its simplest form, is realized as an LC circuit which determines the VCO operating frequency. This is described in Equation 1.

$$f_0 = \frac{1}{2\pi \sqrt{LC}} \quad \text{Equation 1}$$

In the practical case, the capacitor is replaced with a varactor diode whose capacitance changes with the voltage applied, thus changing the resonant frequency at which the VCO tank operates. The capacitive component in Equation 1 also needs to include the input capacitance of the device and other circuit and parasitic elements. Typically, the inductor is realized as a surface mount chip or a wound-coil. In addition, the lead inductance and board inductance and capacitance also have an impact on the final operating point.

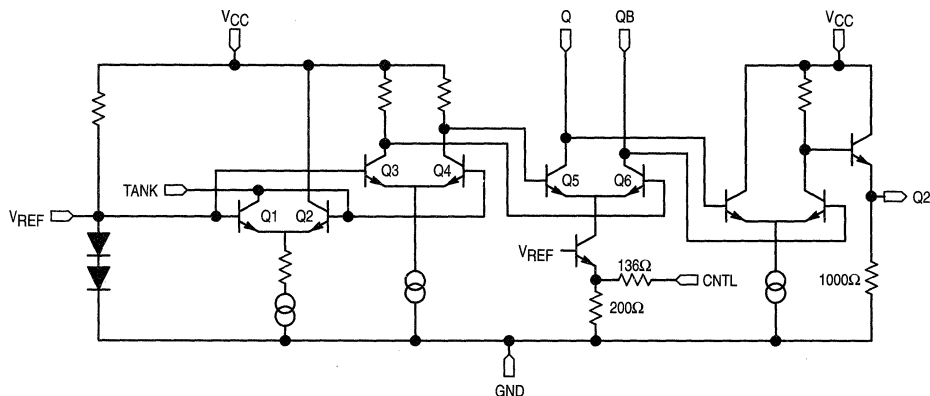
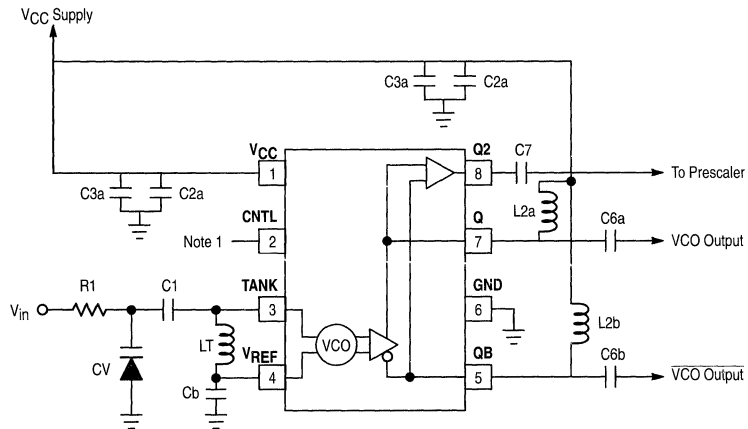


Figure 1. Simplified Schematic



1. This input can be left open, tied to ground, or tied with a resistor to ground, depending on the desired output amplitude needed at the Q and QB output pair.
2. Typical values for R1 range from 5k $\Omega$  to 10k $\Omega$ .

**Figure 2. MC12149 Typical External Component Connections**

A simplified linear approximation of the device, package, and typical board parasitics has been developed to aid the designer in selecting the proper tank circuit values. All the parasitic contributions have been lumped into a parasitic capacitive component and a parasitic inductive component. While this is not entirely accurate, it gives the designer a solid starting point for selecting the tank components.

Below are the parameters used in the model.

Cp	Parasitic Capacitance
Lp	Parasitic Inductance
LT	Inductance of Coil
C1	Coupling Capacitor Value
Cb	Capacitor for decoupling the Bias Pin
CV	Varactor Diode Capacitance (Variable)

The values for these components are substituted into the following equations:

$$C_i = \frac{C_1 \times CV}{C_1 + CV} + C_p \quad \text{Equation 2}$$

$$C = \frac{C_i \times C_b}{C_i + C_b} \quad \text{Equation 3}$$

$$L = L_p + LT \quad \text{Equation 4}$$

From Figure 2, it can be seen that the varactor capacitance (CV) is in series with the coupling capacitor (C1). This is calculated in Equation 2. For analysis purposes, the parasitic capacitances (CP) are treated as a lumped element and placed in parallel with the series combination of C1 and CV. This compound capacitance (Ci) is in series with the bias capacitor (Cb) which is calculated in Equation 3. The influences of the various capacitances; C1, CP, and Cb,

impact the design by reducing the variable capacitance effects of the varactor which controls the tank resonant frequency and tuning range.

Now the results calculated from Equation 2, Equation 3 and Equation 4 can be substituted into Equation 1 to calculate the actual frequency of the tank.

To aid in analysis, it is recommended that the designer use a simple spreadsheet based on Equation 1 through Equation 4 to calculate the frequency of operation for various varactor/inductor selections before determining the initial starting condition for the tank.

The two main components at the heart of the tank are the inductor (LT) and the varactor diode (CV). The capacitance of a varactor diode junction changes with the amount of reverse bias voltage applied across the two terminals. This is the element which actually "tunes" the VCO. One characteristic of the varactor is the tuning ratio which is the ratio of the capacitance at specified minimum and maximum voltage points. For characterizing the MC12149, a Matsushita (Panasonic) varactor – MA393 was selected. This device has a typical capacitance of 11 pF at 1V and 3.7 pF at 4V and the C–V characteristic is fairly linear over that range. Similar performance was also achieved with Loral varactors. A multi-layer chip inductor was used to realize the LT component. These inductors had typical Q values in the 35–50 range for frequencies between 500 and 1000MHz.

**Note:** There are many suppliers of high performance varactors and inductors and Motorola can not recommend one vendor over another.

The Q (quality factor) of the components in the tank circuit has a direct impact on the resulting phase noise of the oscillator. In general, the higher the Q, the lower the phase noise of the resulting oscillator. In addition to the LT and CV

components, only high quality surface-mount RF chip capacitors should be used in the tank circuit. These capacitors should have very low dielectric loss (high-Q). At a minimum, the capacitors selected should be operating 100 MHz below their series resonance point. As the desired frequency of operation increases, the values of the C1 and Cb capacitors will decrease since the series resonance point is a function of the capacitance value. To simplify the selection of C1 and Cb, a table has been constructed based on the intended operating frequency to provide recommended starting points. These may need to be altered depending on the value of the varactor selected.

Frequency	C1	Cb
200 – 500 MHz	47 pF	47 pF
500 – 900 MHz	5.1 pF	15 pF
900 – 1200 MHz	2.7 pF	15 pF

The value of the Cb capacitor influences the VCO supply pushing. To minimize pushing, the Cb capacitor should be kept small. Since C1 is in series with the varactor, there is a strong relationship between these two components which influences the VCO sensitivity. Increasing the value of C1 tends to increase the sensitivity of the VCO.

The parasitic contributions Lp and Cp are related to the MC12149 as well as parasitics associated with the layout, tank components, and board material selected. The input capacitance of the device, bond pad, the wire bond, package/lead capacitance, wire bond inductance, lead inductance, printed circuit board layout, board dielectric, and proximity to the ground plane all have an impact on these parasitics. For example, if the ground plane is located directly below the tank components, a parasitic capacitor will be formed consisting of the solder pad, metal traces, board dielectric material, and the ground plane. The test fixture used for characterizing the device consisted of a two sided copper clad board with ground plane on the back. Nominal values were determined by selecting a varactor and characterizing the device with a number of different tank/frequency combinations and then performing a curve fit with the data to determine values for Lp and Cp. The nominal values for the parasitic effects are seen below:

Parasitic Capacitance	Cp	4.2 pF
Parasitic Inductance	Lp	2.2 nH

These values will vary based on the users unique circuit board configuration.

#### Basic Guidelines:

11. Select a varactor with high Q and a reasonable capacitance versus voltage slope for the desired frequency range.
12. Select the value of Cb and C1 from the table above .
13. Calculate a value of inductance (L) which will result in achieving the desired center frequency. Note that L includes both LT and Lp.
14. Adjust the value of C1 to achieve the proper VCO sensitivity.
15. Re-adjust value of L to center VCO.
16. Prototype VCO design using selected components. It is important to use similar construction techniques and materials, board thickness, layout, ground plane spacing as intended for the final product.
17. Characterize tuning curve over the voltage operation conditions.
18. Adjust, as necessary, component values – L,C1, and Cb to compensate for parasitic board effects.
19. Evaluate over temperature and voltage limits.
20. Perform worst case analysis of tank component variation to insure proper VCO operation over full temperature and voltage range and make any adjustments as needed.

Outputs Q and QB are open collector outputs and need a inductor to VCC to provide the voltage bias to the output transistor. In most applications, DC-blocking capacitors are placed in series with the output to remove the DC component before interfacing to other circuitry. These outputs are complementary and should have identical inductor values for each output. This will minimize switching noise on the VCC supply caused by the outputs switching. It is important that both outputs be terminated, even if only one of the outputs is used in the application.

Referring to Figure 2, the recommended value for L2a and L2b should be 47 nH and the inductor components resonance should be at least 300 MHz greater than the maximum operating frequency. For operation above 1100 MHz, it may be necessary to reduce that inductor value to 33 nH. The recommended value for the coupling capacitors C6a, C6b, and C7 is 47 pF. Figure 2 also includes decoupling capacitors for the supply line as well as decoupling for the output inductors. Good RF decoupling practices should be used with a series of capacitors starting with high quality 100 pF chip capacitors close to the device. A typical layout is shown below in Figure 3.



The output amplitude of the Q and QB can be adjusted using the CNTL pin. Referring to Figure 1, if the CNTL pin is connected to ground, additional current will flow through the current source. When the pin is left open, the nominal current flowing through the outputs is 4 mA. When the pin is grounded, the current increases to a nominal value of 10 mA. So if a 50 ohm resistor was connected between the outputs and VCC, the output amplitude would change from 200 mV pp to 500 mV pp with an additional current drain for the device of 6 mA. To select a value between 4 and 10 mA, an external resistor can be added to ground. The equation below is used to calculate the current.

$$I_{out(nom)} = \frac{(200 + 136 + R_{ext}) \times 0.8V}{200 \times (136 + R_{ext})}$$

Figure 4 through Figure 13 illustrate typical performance achieved with the MC12149. The curves illustrate the tuning curve, supply pushing characteristics, output power, current

drain, output spectrum, and phase noise performance. In most cases, data is present for both a 750 MHz and 1200 MHz tank design. The table below illustrates the component values used in the designs.

Component	750MHz Tank	1200MHz Tank	Units
R1	5000	5000	Ω
C1	5.1	2.7	pF
LT	4.7	1.8	nH
CV	3.7@1V 11@4V	3.7@1V 11@4V	pF
Cb	100*	15	pF
C6, C7	47	33	pF
L2	47	47	nH

\* The value of Cb should be reduced to minimize pushing.

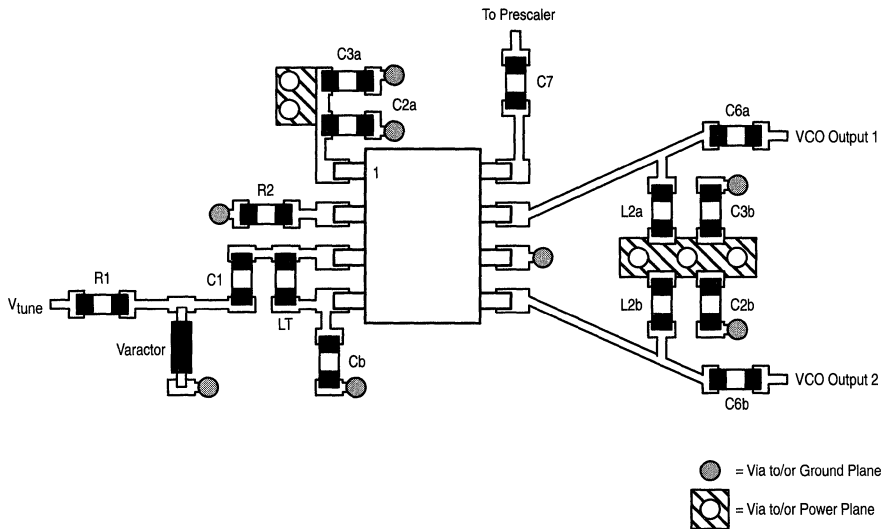


Figure 3. MC12149 Typical Layout (Not to Scale)

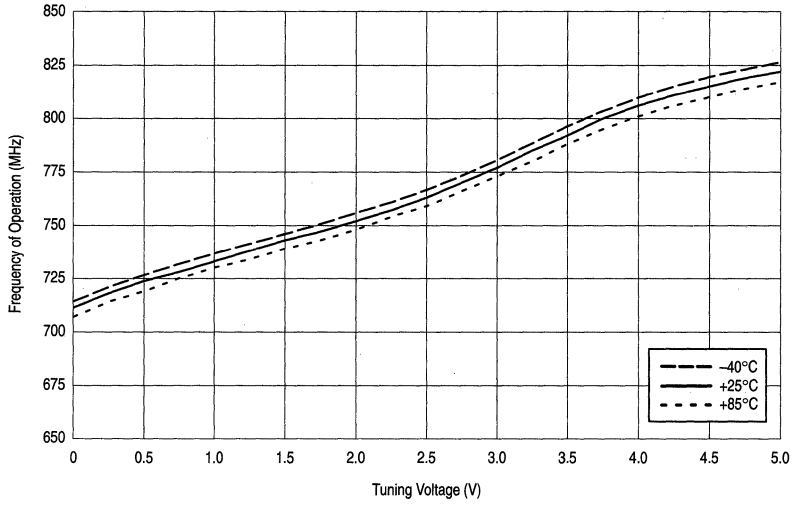


Figure 4. Typical VCO Tuning Curve, 750MHz Tank

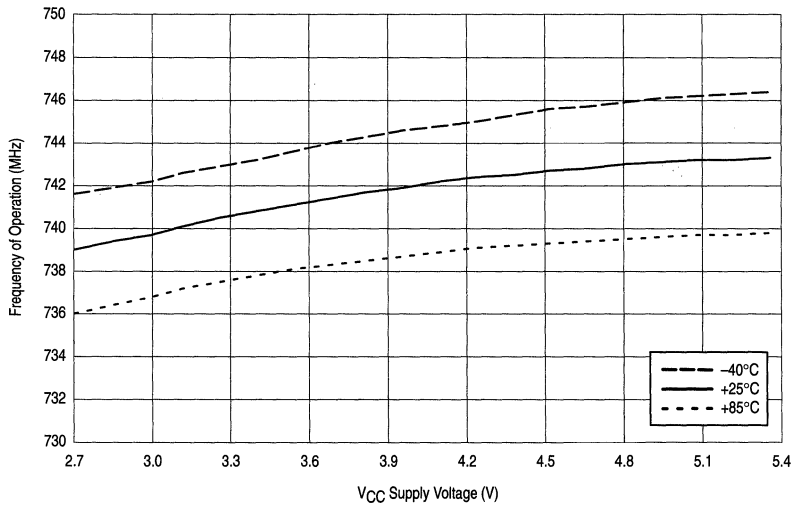


Figure 5. Typical Supply Pushing, 750MHz Tank

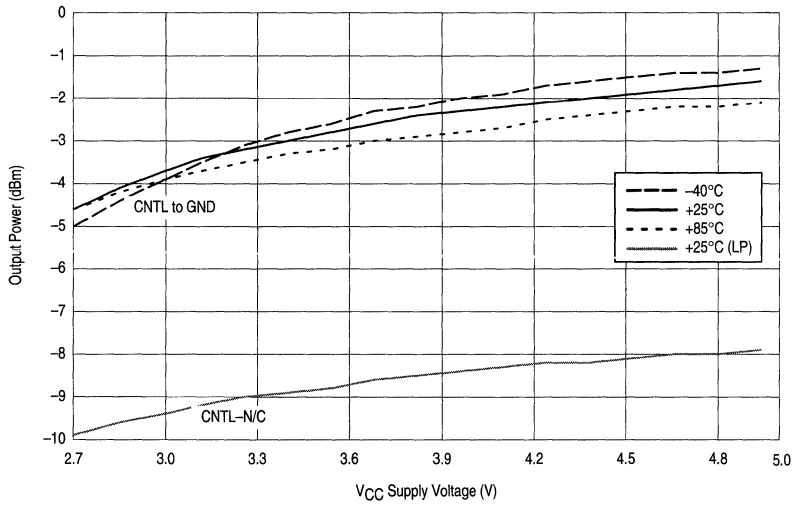


Figure 6. Typical Q/QB Output Power versus Supply, 750MHz Tank

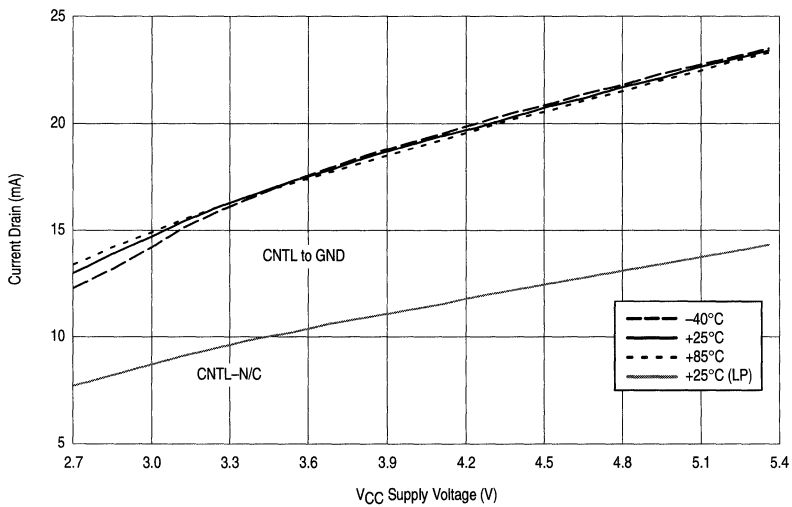


Figure 7. Typical Current Drain versus Supply, 750MHz Tank

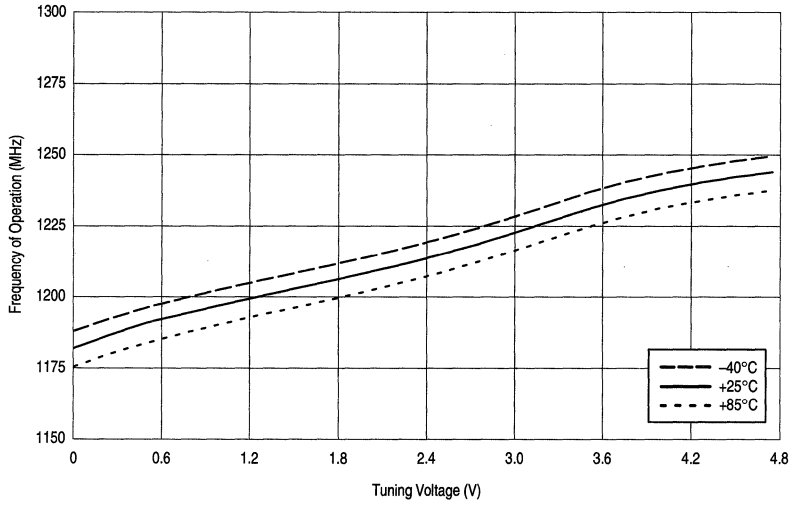


Figure 8. Typical VCO Tuning Curve, 1200MHz Tank ( $V_{CC} = 5.0V$ )

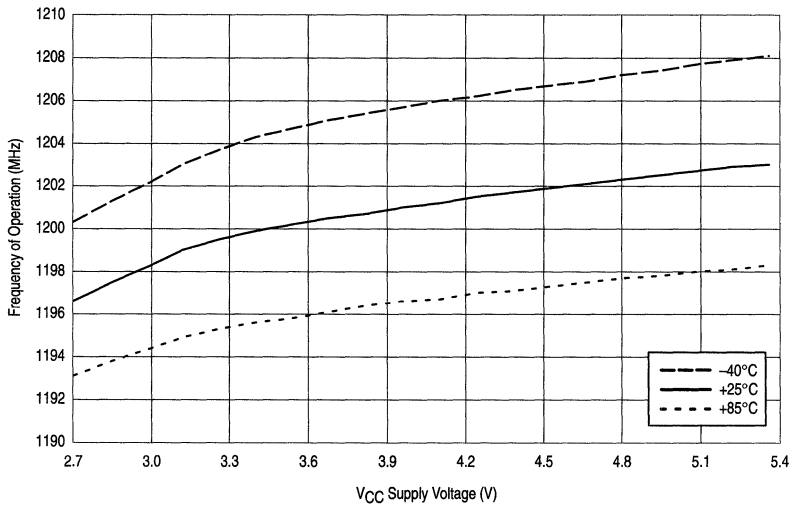


Figure 9. Typical Supply Pushing, 1200MHz Tank

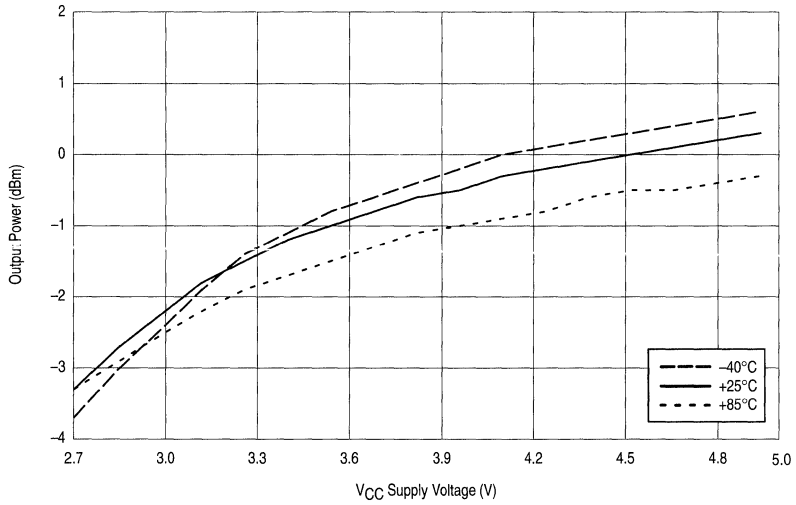


Figure 10. Q/QB Output Power versus Supply, 1200MHz Tank

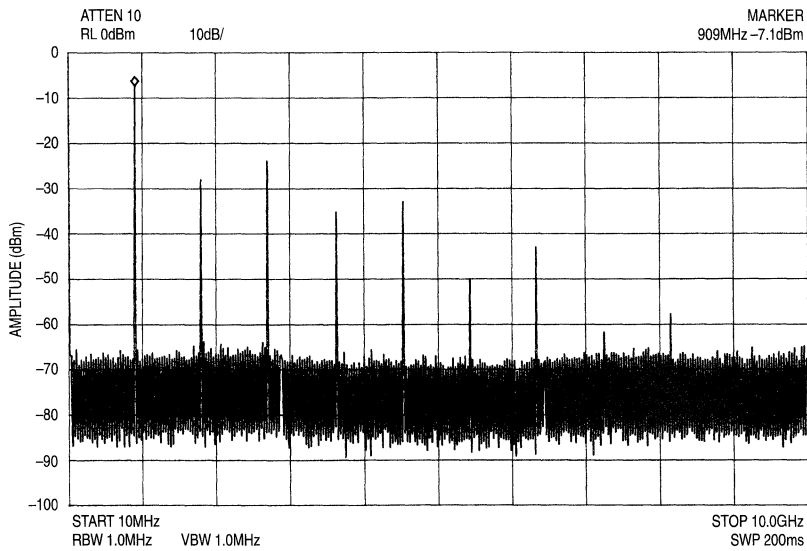


Figure 11. Typical VCO Output Spectrum

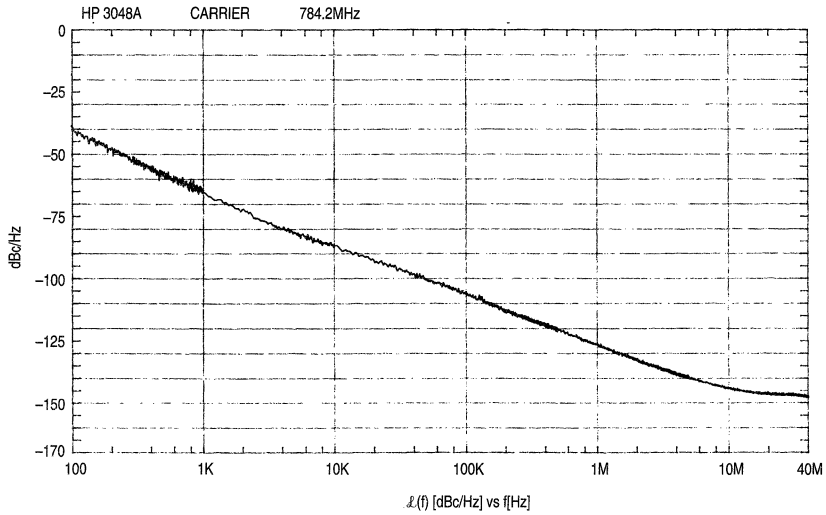


Figure 12. Typical Phase Noise Plot, 750MHz Tank

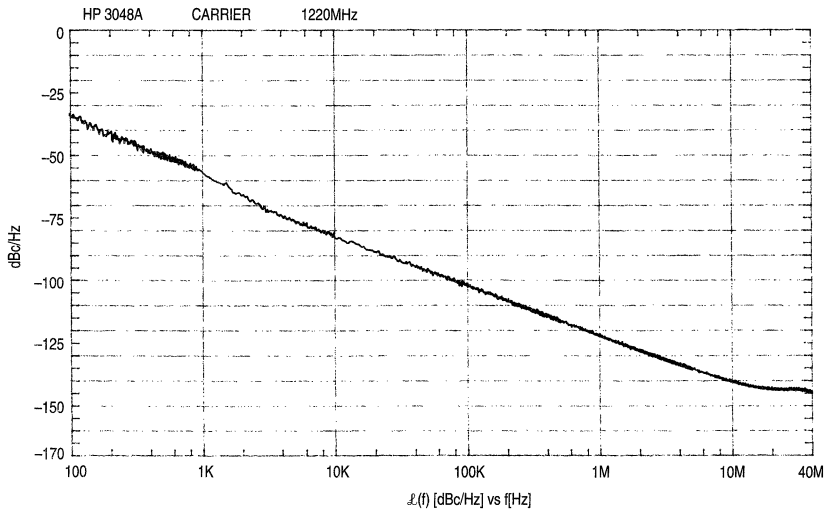


Figure 13. Typical Phase Noise Plot, 1200MHz Tank

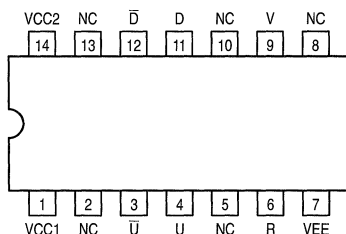
# Phase-Frequency Detectors

## Phase-Frequency Detector

The MC12040 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648, MC12147, MC12148 or MC12149), it is useful in a broad range of phase-locked loop applications. Operation of this device is identical to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

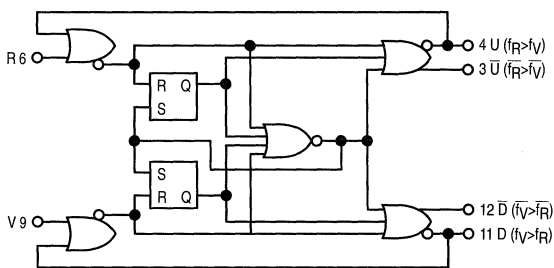
- Operating Frequency = 80MHz Typical

Pinout: 14-Lead Package (Top View)



NC = No Connect

LOGIC DIAGRAM



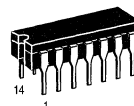
VCC1 = Pin 1  
VCC2 = Pin 14  
VEE = Pin 7

### TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

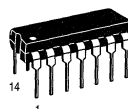
## MC12040

### PHASE-FREQUENCY DETECTOR



**L SUFFIX**  
CERAMIC PACKAGE  
CASE 632-08

*Not Recommended for New Designs*



**P SUFFIX**  
PLASTIC PACKAGE  
CASE 646-06



**FN SUFFIX**  
PLCC PACKAGE  
CASE 775-02

Inputs		Outputs			
R	V	U	D	$\bar{U}$	$\bar{D}$
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	0	1	1
0	1	0	1	1	0
1	1	0	0	1	1

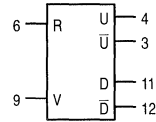
X = Don't Care





**ELECTRICAL CHARACTERISTICS**

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0V for +5.0V tests and through a 50 ohm resistor to -2.0V for -5.2V tests.



**NOTE:** For more information on using an ECL device in a +5V system, refer to Motorola Application Note AN1406/D, "Designing with PECL (ECL at +5.0V)"

Supply Voltage = -5.2V

Symbol	Characteristics	Pin Under Test	MC12040								TEST VOLTAGE APPLIED TO PINS BELOW					(V <sub>CC</sub> ) Gnd	
			0°C		25°C		75°C		Unit	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>			
			Min	Max	Min	Max	Min	Max									
I <sub>E</sub>	Power Supply Drain	7			-120	-60									7	1,14	
I <sub>NH</sub>	Input Current	6 9				350 350					μAdc	6 9				7 7	1,14 1,14
V <sub>OH</sub> <sup>1</sup>	Logic "1" Output Voltage	3 4 11 12	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720			Vdc					7	1,14
V <sub>OL</sub> <sup>1</sup>	Logic "0" Output Voltage	3 4 11 12	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595			Vdc					7	1,14
V <sub>OHA</sub> <sup>2</sup>	Logic "1" Input Voltage	3 4 11 12	-1.020		-0.980		-0.920				Vdc			6.9		7	1,14
V <sub>OLA</sub> <sup>2</sup>	Logic "0" Input Voltage	3 4 11 12		-1.615		-1.600		-1.575			Vdc			9 6 9 6 6	6 9 6 9	7	1,14

TEST VOLTAGE VALUES					
(Volts)					
Test Temperature	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Supply Voltage = +5.0V

Symbol	Characteristics	Pin Under Test	MC12040								TEST VOLTAGE APPLIED TO PINS BELOW					(V <sub>CC</sub> ) Gnd	
			0°C		25°C		75°C		Unit	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>			
			Min	Max	Min	Max	Min	Max									
I <sub>E</sub>	Power Supply Drain	7			-115	-60									1,14	7	
I <sub>NH</sub>	Input Current	6 9				350 350					μAdc	6 9				1,14 1,14	7 7
V <sub>OH</sub> <sup>1</sup>	Logic "1" Output Voltage	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280			Vdc					1,14	7
V <sub>OL</sub> <sup>1</sup>	Logic "0" Output Voltage	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470			Vdc					1,14	7
V <sub>OHA</sub> <sup>2</sup>	Logic "1" Input Voltage	3 4 11 12	3.980		4.020		4.080				Vdc			6.9		1,14	7
V <sub>OLA</sub> <sup>2</sup>	Logic "0" Input Voltage	3 4 11 12		3.450		3.460		3.490			Vdc			9 6 9 6 6	6 9 6 9	1,14	7

TEST VOLTAGE VALUES					
(Volts)					
Test Temperature	V <sub>IHmax</sub>	V <sub>ILmin</sub>	V <sub>IHAmin</sub>	V <sub>ILAmax</sub>	V <sub>EE</sub>
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

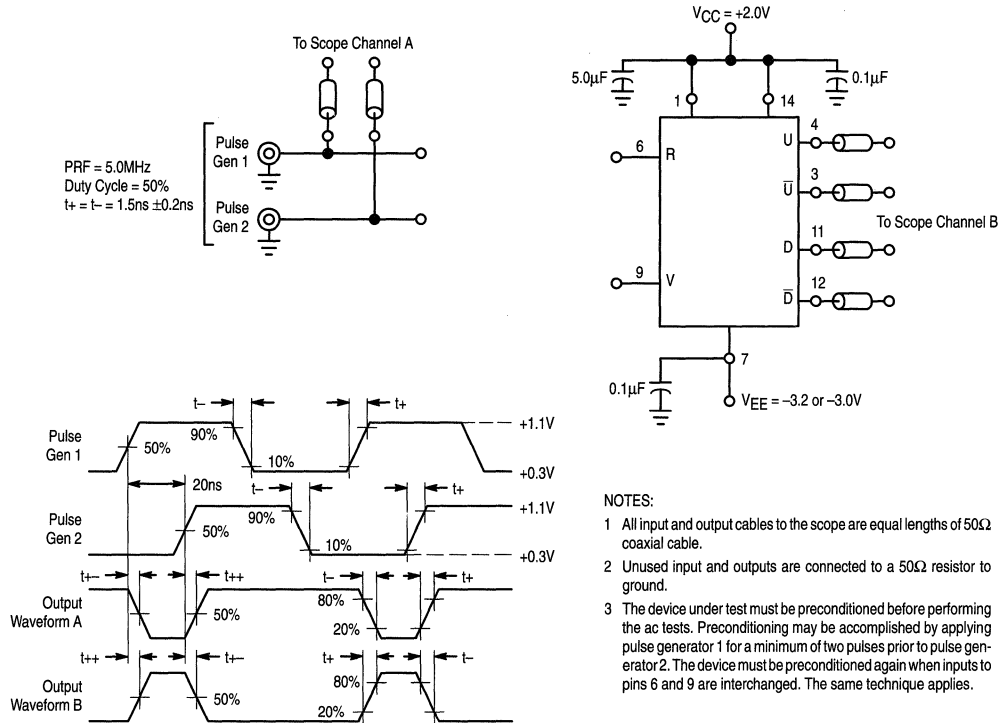


Figure 1. AC Tests

Symbol	Characteristic	Pin Under Test	Output Waveform	MC12040			Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED			
				0°C	25°C	85°C		Pulse Gen 1	Pulse Gen 2	V <sub>EE</sub> -3.0 or -3.2V	V <sub>CC</sub> +2.0V
				Max	Max	Max					
$t_{6+4+}$ $t_{6+12+}$ $t_{6+3-}$ $t_{6+11-}$ $t_{9+11+}$ $t_{9+3+}$ $t_{9+12-}$ $t_{9+4-}$	Propagation Delay	6,4 6,12 6,3 6,11 9,11 9,3 9,12 9,4	B A A B B A A B	4.6 6.0 4.5 6.4 4.6 6.0 4.5 6.4	4.6 6.0 4.5 6.4 4.6 6.0 4.5 6.4	5.0 6.6 4.9 7.0 5.0 6.6 4.9 7.0	ns	6 9 6 9 9 6 9 6	9 6 9 6 6 9 6 9	7	1,14
$t_{3+}$ $t_{4+}$ $t_{11+}$ $t_{14+}$	Output Rise Time	3 4 11 14	A B B A	3.4 3.4	3.4 3.4	3.8	ns	6 6 9 9	9 9 6 6	7	1,14
$t_{3-}$ $t_{4-}$ $t_{11-}$ $t_{14-}$	Output Fall Time	3 4 11 14	A B B A	3.4 3.4	3.4 3.4	3.8	ns	6 6 9 9	9 9 6 6	7	1,14

## APPLICATIONS INFORMATION

The MC12040 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 2), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 2), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle—that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage controlled oscillator can be developed. A circuit useful for this function is shown in Figure 3.

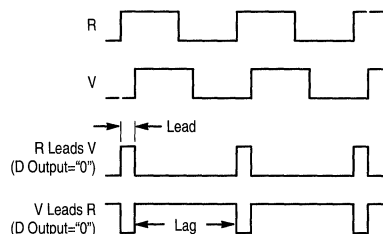


Figure 2. Timing Diagram

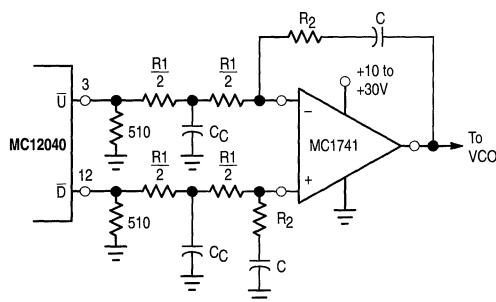


Figure 3. Typical Filter and Summing Network

## Phase-Frequency Detector

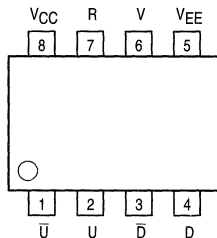
The MCH/K12140 is a phase frequency-detector intended for phase-locked loop applications which require a minimum amount of phase and frequency difference at lock. When used in conjunction with the MC12147, MC12148 or MC12149 VCO, a high bandwidth PLL can be realized. The device is functionally compatible with the MC12040 phase-frequency detector, however the MOSAIC™ III process is used to push the maximum frequency to 800MHz and significantly reduce the dead zone of the detector. When the Reference (R) and VCO (V) inputs are unequal in frequency and/or phase, the differential UP (U) and DOWN (D) outputs will provide pulse streams which when subtracted and integrated provide an error voltage for control of a VCO.

The device is packaged in a small outline, surface mount 8-lead SOIC package. There are two versions of the device to provide I/O compatibility to the two existing ECL standards. The MCH12140 is compatible with MECL10H™ logic levels while the MCK12140 is compatible to 100K ECL logic levels. This device can also be used in +5V systems. Please refer to Motorola Application Note AN1406/D, "Designing with PECL (ECL at +5.0V)" for more information.

- 800MHz Typical Bandwidth
- Small Outline 8-Lead SOIC Package
- 75kΩ Internal Input Pulldown Resistors
- >1000V ESD Protection

For proper operation, the input edge rate of the R and V inputs should be less than 5ns.

Pinout: 8-Lead SOIC (Top View)



TRUTH TABLE\*

Input		Output				Input		Output			
R	V	U	D	$\bar{U}$	$\bar{D}$	R	V	U	D	$\bar{U}$	$\bar{D}$
0	0	X	X	X	X	1	1	0	0	1	1
0	1	X	X	X	X	1	0	0	0	1	1
1	1	X	X	X	X	1	1	0	1	1	0
0	1	X	X	X	X	1	0	0	1	1	0
1	1	1	0	0	1	1	1	0	1	1	0
0	1	1	0	0	1	0	1	0	1	1	0
1	1	1	0	0	1	1	1	0	0	1	1

\* This is not strictly a functional table; i.e., it does not cover all possible modes of operation. However, it gives a sufficient number of tests to ensure that the device will function properly.

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**MCH12140**  
**MCK12140**

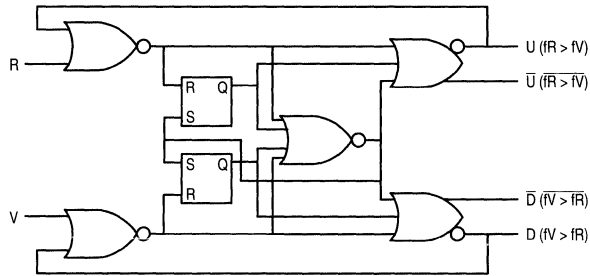
**PHASE-FREQUENCY**  
**DETECTOR**



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05



## LOGIC DIAGRAM

**H-SERIES DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min}) - V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}^1$ )

Symbol	Characteristic	-40°C		0°C		25°C		70°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
$V_{OH}$	Output HIGH Voltage	-1080	-890	-1020	-840	-980	-810	-910	-720	mV
$V_{OL}$	Output LOW Voltage	-1950	-1650	-1950	-1630	-1950	-1630	-1950	-1595	mV
$V_{IH}$	Input HIGH Voltage	-1230	-890	-1170	-840	-1130	-810	-1060	-720	mV
$V_{IL}$	Input LOW Voltage	-1950	-1500	-1950	-1480	-1950	-1480	-1950	-1445	mV
$I_{IL}$	Input LOW Current	0.5	—	0.5	—	0.5	—	0.3	—	$\mu\text{A}$

1. 10H circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50 $\Omega$  resistor to -2.0V except where otherwise specified on the individual data sheets.

**K-SERIES DC CHARACTERISTICS** ( $V_{EE} = V_{EE}(\text{min}) - V_{EE}(\text{max})$ ;  $V_{CC} = \text{GND}^1$ )

Symbol	Characteristic	-40°C			0°C to 70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max		
$V_{OH}$	Output HIGH Voltage	-1085	-1005	-880	-1025	-955	-880	mV	$V_{IN} = V_{IH}(\text{max})$
$V_{OL}$	Output LOW Voltage	-1830	-1695	-1555	-1810	-1705	-1620	mV	or $V_{IL}(\text{min})$
$V_{OHA}$	Output HIGH Voltage	-1095	—	—	-1035	—	—	mV	$V_{IN} = V_{IH}(\text{min})$
$V_{OLA}$	Output LOW Voltage	—	—	-1555	—	—	-1610	mV	or $V_{IL}(\text{max})$
$V_{IH}$	Input HIGH Voltage	-1165	—	-880	-1165	—	-880	mV	
$V_{IL}$	Input LOW Voltage	-1810	—	-1475	-1810	—	-1475	mV	
$I_{IL}$	Input LOW Current	0.5	—	—	0.5	—	—	$\mu\text{A}$	$V_{IN} = V_{IL}(\text{max})$

1. This table replaces the three tables traditionally seen in ECL 100K data books. The same DC parameter values at  $V_{EE} = -4.5\text{V}$  now apply across the full  $V_{EE}$  range of -4.2V to -5.5V. Outputs are terminated through a 50 $\Omega$  resistor to -2.0V except where otherwise specified on the individual data sheets.

**ABSOLUTE MAXIMUM RATINGS<sup>1</sup>**

Characteristic	Symbol	Rating	Unit
Power Supply ( $V_{CC} = 0\text{V}$ )	$V_{EE}$	-8.0 to 0	VDC
Input Voltage ( $V_{CC} = 0\text{V}$ )	$V_I$	0 to -6.0	VDC
Output Current	$I_{out}$	50 100	mA
Operating Temperature Range	$T_A$	-40 to +70	°C
Operating Range <sup>1,2</sup>	$V_{EE}$	-5.7 to -4.2	V

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.

2. Parametric values specified at:  
 H-Series: -4.20V to -5.50V  
 K-Series: -4.94V to -5.50V

**DC CHARACTERISTICS** ( $V_{EE} = V_{EE(min)} - V_{EE(max)}$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			70°C			Unit	
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
$I_{EE}$	Power Supply Current	H K	45 45		38 38	45 45	52 52	38 38	45 45	52 52	38 42	45 50	52 58	mA	
$V_{EE}$	Power Supply Voltage	H K	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	-4.75 -4.20	-5.2 -4.5	-5.5 -5.5	V
$I_{IH}$	Input HIGH Current			150			150			150			150	$\mu$ A	

**AC CHARACTERISTICS** ( $V_{EE} = V_{EE(min)} - V_{EE(max)}$ ;  $V_{CC} = GND$ )

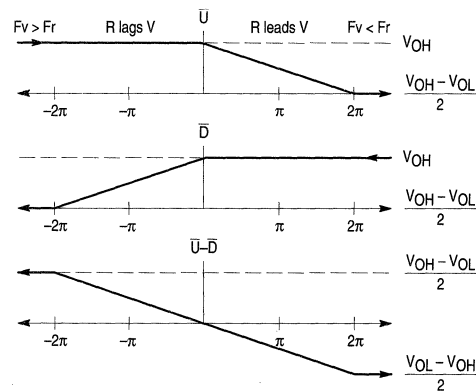
Symbol	Characteristic	-40°C			0°C			25°C			70°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$F_{MAX}$	Maximum Toggle Frequency		800		650	800		650	800		650	800		
$t_{PLH}$ $t_{PHL}$	Propagation Delay R to D to Output R to U V to D V to U		440 330 330 440		320 210 210 320	440 330 330 440	580 470 470 580	320 210 210 320	440 330 330 440	580 470 470 580	360 240 240 360	480 360 360 480	620 500 500 620	ps
$t_r$ $t_f$	Output Rise/Fall Times Q (20 to 80%)		225		100	225	350	100	225	350	100	225	350	ps

**APPLICATIONS INFORMATION**

The 12140 is a high speed digital circuit used as a phase comparator in an analog phase-locked loop. The device determines the "lead" or "lag" phase relationship and time difference between the leading edges of a VCO (V) signal and a Reference (R) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

The operation of the 12140 can best be described using the plots of Figure 1. Figure 1 plots the average value of  $\bar{U}$ ,  $\bar{D}$  and the difference between  $\bar{U}$  and  $\bar{D}$  versus the phase difference between the V and R inputs.

There are four potential relationships between V and R: R lags or leads V and the frequency of R is less than or greater than the frequency of V. Under these four conditions the 12140 will function as follows:



**Figure 1. Average Output Voltage versus Phase Difference**

**R lags V in phase**

When the R and V inputs are equal in frequency and the phase of R lags that of V the  $\bar{U}$  output will stay HIGH while the  $\bar{D}$  output will pulse from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on  $\bar{D}$  indicates to the VCO to decrease in frequency to bring the loop into lock.

**V frequency > R frequency**

When the frequency of V is greater than that of R the 12140 behaves in a similar fashion as above. Again the signal on  $\bar{D}$  indicates that the VCO frequency must be decreased to bring the loop into lock.

**R leads V in phase**

When the R and V inputs are equal in frequency and the phase of R leads that of V the  $\bar{D}$  output will stay HIGH while the  $\bar{U}$  output pulses from HIGH to LOW. The magnitude of the pulse will be proportional to the phase difference between the V and R inputs reaching a minimum 50% duty cycle under a 180° out of phase condition. The signal on  $\bar{U}$  indicates to the VCO to increase in frequency to bring the loop into lock.

**V frequency < R frequency**

When the frequency of V is less than that of R the 12140 behaves in a similar fashion as above. Again the signal on  $\bar{U}$  indicates that the VCO frequency must be decreased to bring the loop into lock.

From Figure 1 when V and R are at the same frequency and in phase the value of  $\bar{U} - \bar{D}$  is zero thus providing a zero error voltage to the VCO. This situation indicates the loop is in lock and the 12140 action will maintain the loop in its locked state.

# Frequency Synthesizers

## Serial Input PLL Frequency Synthesizer

The MC12202 is a 1.1GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse-swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over 2.7 to 5.5V supply range for input frequencies up to 1.1GHz with a typical current drain of 6.5mA. The low power consumption makes the MC12202 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 64/65 or 128/129 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 5.8mA Typical for I<sub>CC</sub> and 0.7mA Typical for I<sub>p</sub>
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 64/65 or 128/129
- On-Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14–Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7–Bit Swallow Counter and an 11–Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of –40°C to +85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages
- The MC12202 Is Pin Compatible With the Fujitsu MB1502 or MB1511

**MC12202**

### MECL PLL COMPONENTS

#### Serial Input PLL Frequency Synthesizer



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B–05



**M SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 966–01



**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 948E–02

#### MAXIMUM RATINGS\*

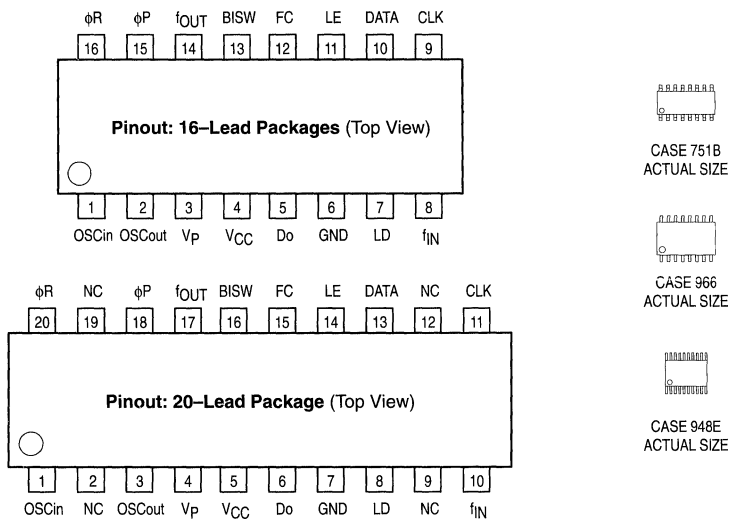
Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 4 (Pin 5 in 20–lead package)	–0.5 to +6.0	VDC
V <sub>p</sub>	Power Supply Voltage, Pin 3 (Pin 4 in 20–lead package)	V <sub>CC</sub> to +6.0	VDC
T <sub>stg</sub>	Storage Temperature Range	–65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

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## PIN NAMES

Pin	I/O	Function	16-Lead Pkg Pin No.	20-Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal is connected between OSCin and OSCout. An external source can be AC coupled into this input	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V <sub>p</sub>	—	Power supply for charge pumps (V <sub>p</sub> should be greater than or equal to V <sub>CC</sub> ) V <sub>p</sub> provides power to the Do, BISW and φP outputs	3	4
V <sub>CC</sub>	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f <sub>IN</sub>	I	Prescaler input. The VCO signal is AC-coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects fp or fr on the f <sub>OUT</sub> pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN ("analog switch is ON") the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f <sub>OUT</sub>	O	Phase comparator input signal. When FC is HIGH, f <sub>OUT</sub> =fr, programmable reference divider output; when FC is LOW, f <sub>OUT</sub> =fp, programmable divider output	14	17
φP	O	Output for external charge pump. Standard CMOS output level	15	18
φR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

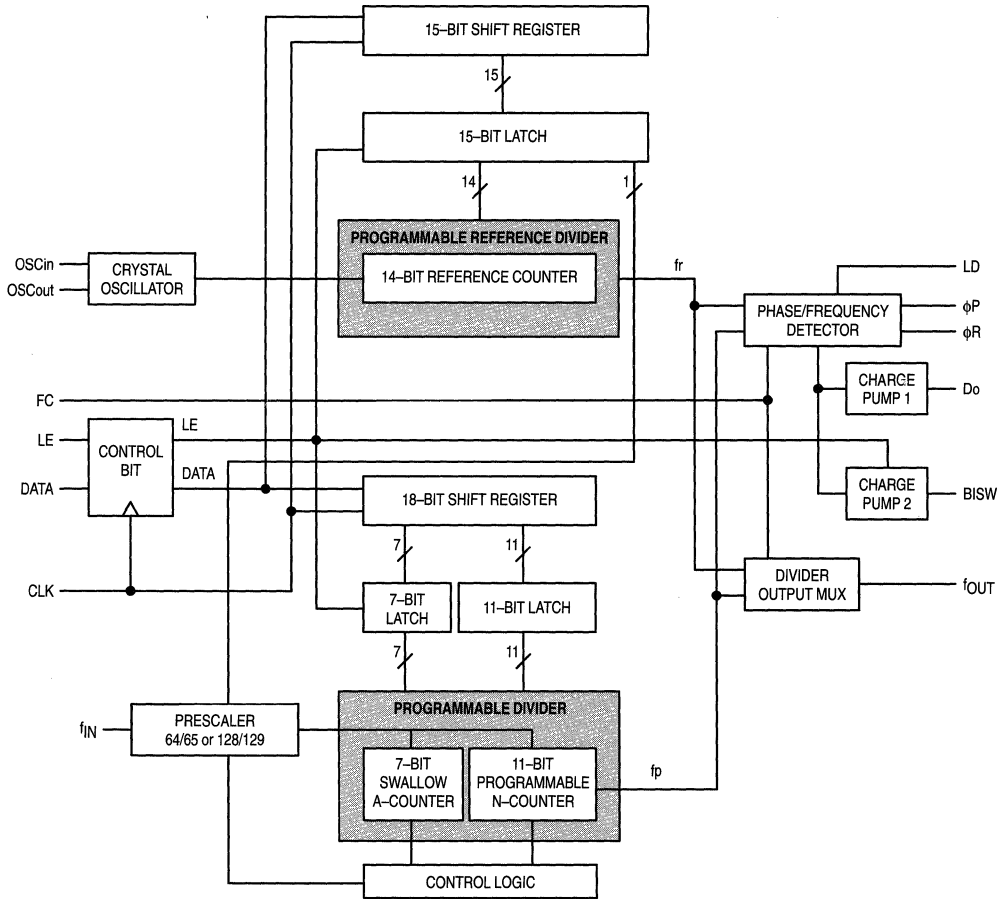


Figure 1. MC12202 Block Diagram

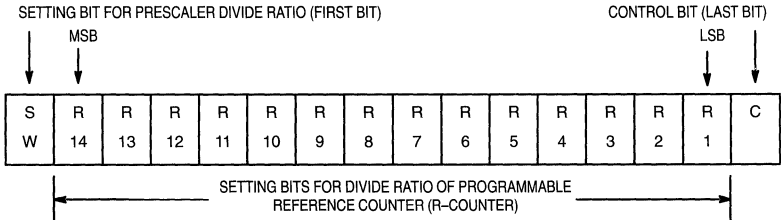
**DATA ENTRY FORMAT**

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14-bit programmable reference divider plus the prescaler setting bit, and the 18-bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

Control bit: "H" = data is transferred into 15-bit latch of programmable reference divider  
 "L" = data is transferred into 18-bit latch of programmable divider

**PROGRAMMABLE REFERENCE DIVIDER**

16-bit serial data format for the programmable reference counter, "R-counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15-bit shift register into the 15-bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for +128/129, SW=1 for +64/65). An R divide ratio less than 8 is prohibited. For Control bit (C) = HIGH:



**DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER**

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

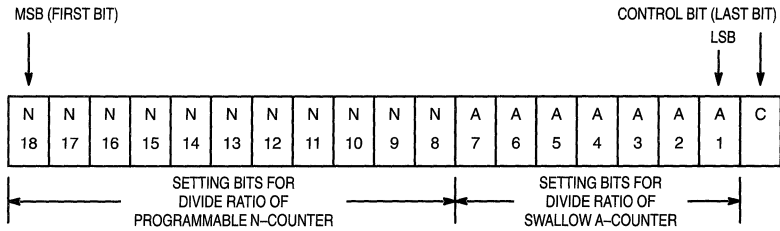
**PRESCALER SELECT BIT**

Prescaler Divide Ratio P	SW
128/129	0
64/65	1

**PROGRAMMABLE DIVIDER**

19-bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18-bit shift register into the 18-bit latch which specifies the swallow A-counter divide ratio (0 to 127) and the programmable N-counter divide ratio (16 to 2047). An N-counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



**DIVIDE RATIO OF PROGRAMMABLE N-COUNTER**

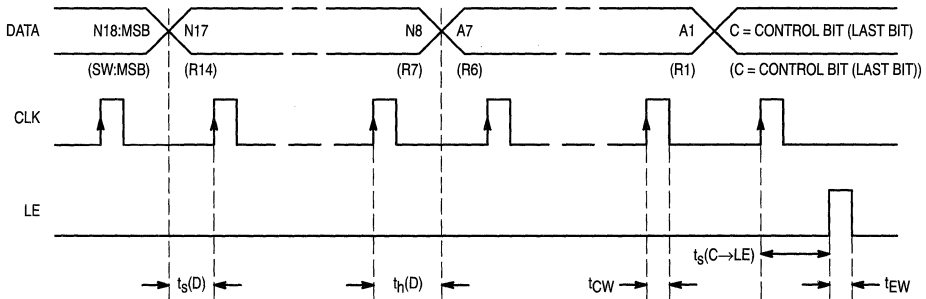
**DIVIDE RATIO OF SWALLOW A-COUNTER**

Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	127	1	1	1	1	1	1	1

**DIVIDE RATIO SETTING**

$$f_{vco} = [(P \cdot N) + A] \cdot f_{osc} \div R \text{ with } A < N$$

- f<sub>vco</sub>: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7-bit swallow counter (0 to 127, A < N)
- f<sub>osc</sub>: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (64 or 128)



NOTES: Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

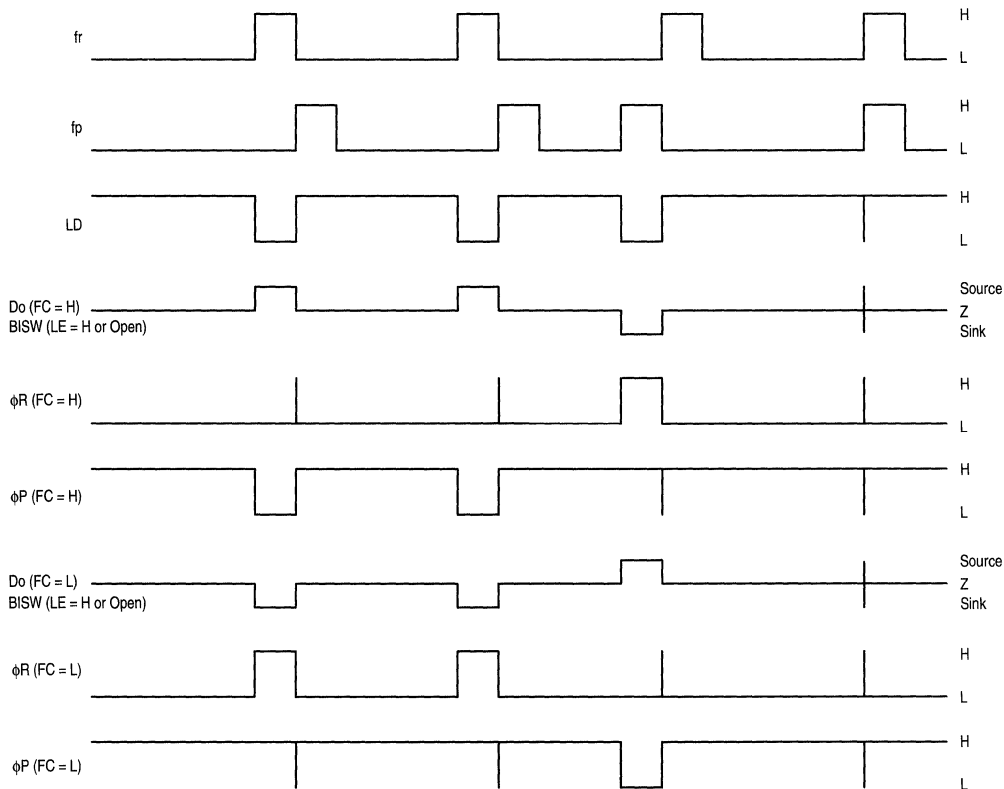
- t<sub>S</sub>(D) = Setup Time DATA to CLK      t<sub>S</sub>(D) ≥ 10ns
- t<sub>H</sub>(D) = Hold Time DATA to CLK      t<sub>H</sub>(D) ≥ 20ns
- t<sub>CW</sub> = CLK Pulse Width      t<sub>CW</sub> ≥ 30ns
- t<sub>EW</sub> = LE Pulse Width      t<sub>EW</sub> ≥ 20ns
- t<sub>S</sub>(C->LE) = Setup Time CLK to LE      t<sub>S</sub>(C->LE) ≥ 30ns

**Figure 2. Serial Data Input Timing**

### PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12202 is a high speed digital phase frequency detector circuit. The circuit determines the “lead” or “lag” phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians. The phase comparator outputs are standard CMOS rail-to-rail levels ( $V_P$  to GND for  $\phi_P$  and  $V_{CC}$  to GND for  $\phi_R$ ), designed for up to 20MHz operation into a 15pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures 3 and 5. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs,  $\phi_R$  and  $\phi_P$ , as well as the charge pump output Do can be reversed by switching the FC pin.



NOTES: Do and BISW are current outputs.  
 Phase difference detection range:  $-2\pi$  to  $+2\pi$   
 Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.  
 When  $f_r > f_p$  or  $f_r < f_p$ , spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{\text{source}} + I_{\text{sink}}}{4\pi} \right| = \frac{4\text{mA}}{4\pi}$$

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms

**For FC = HIGH:**

**fr lags fp in phase OR fp > fr in frequency**

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the φP output will remain in a HIGH state while the φR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φR indicates to the VCO to decrease in frequency to bring the loop into lock.

**fr leads fp in phase OR fp < fr in frequency**

When the phase of fr leads that of fp or the frequency of fp is less than fr, the φR output will remain in a LOW state while the φP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φP indicates to the VCO to increase in frequency to bring the loop to lock.

**fr = fp in phase and frequency**

When the phase and frequency of fr and fp are equal, the output φP will remain in a HIGH state and φR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

**For FC = LOW:**

**fr lags fp in phase OR fp > fr in frequency**

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the φR output will remain in a LOW state while the φP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φP indicates to the VCO to increase in frequency to bring the loop into lock.

**fr leads fp in phase OR fp < fr in frequency**

When the phase of fr leads that of fp or the frequency of fp is less than fr, the φP output will remain in a HIGH state while the φR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φR indicates to the VCO to decrease in frequency to bring the loop to lock.

**fr = fp in phase and frequency**

When the phase and frequency of fr and fp are equal, the output φP will remain in a HIGH state and φR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the fOUT test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the fOUT output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, fOUT = fr, the programmable reference divider output. When FC is LOW, fOUT = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. fOUT = fr

If VCO characteristics are like (2), FC should be set LOW. fOUT = fp

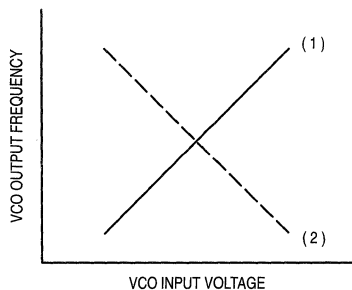


Figure 4. VCO Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	φR	φP	fOUT	Do	φR	φP	fOUT
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTE: Z = High impedance  
When LE is HIGH or Open, BISW has the same characteristics as Do.

Figure 5. Phase Comparator, Internal Charge Pump, and fOUT Characteristics

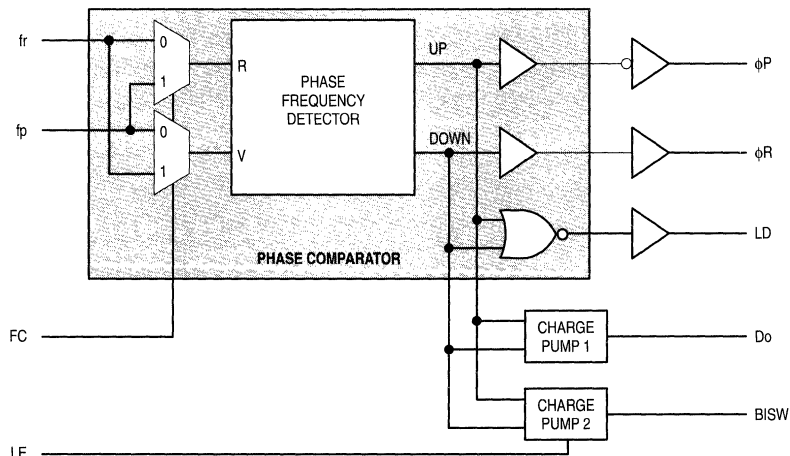


Figure 6. Detailed Phase Comparator Block Diagram

### LOCK DETECT

The Lock Detect (LD) output pin provides a LOW pulse when  $f_r$  and  $f_p$  are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See Figure 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See Figure 9.

### OSCILLATOR INPUT

The device incorporates an on-chip reference oscillator/buffer so that an external parallel-resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure 10 are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance).

If an external reference oscillator is available, the signal should be AC-coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC-coupled signal must be between 500 and 2200 mV peak-to-peak.

### DUAL INTERNAL CHARGE PUMPS ("ANALOG SWITCH")

Due to the pure Bipolar nature of the MC12202 design, the "analog switch" function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure 7 below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN ("analog switch is ON"), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

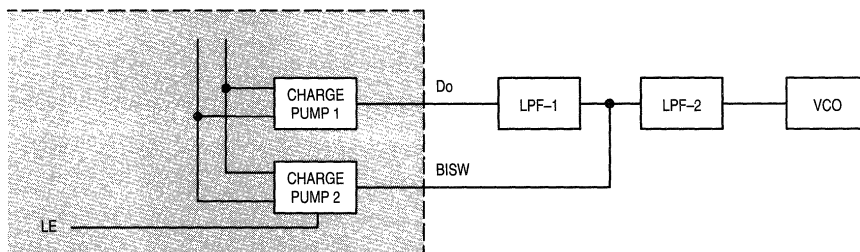


Figure 7. "Analog Switch" Block Diagram

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I <sub>CC</sub>	Supply Current for V <sub>CC</sub>		5.8	9.0	mA	Note 1
			7.2	10.5		Note 2
I <sub>P</sub>	Supply Current for V <sub>p</sub>		0.7	1.1	mA	Note 3
			0.8	1.3		Note 4
F <sub>IN</sub>	Operating Frequency	f <sub>IN</sub> max f <sub>IN</sub> min	1100	100	MHz	Note 5
F <sub>OSC</sub>	Operating Frequency (OSCin)		12	20	MHz	Crystal Mode
				40	MHz	External Reference Mode
V <sub>IN</sub>	Input Sensitivity	f <sub>IN</sub>	200	1000	mV <sub>p-p</sub>	
V <sub>OSC</sub>		OSCin	500	2200	mV <sub>p-p</sub>	
V <sub>IH</sub>	Input HIGH Voltage	CLK, DATA, LE, FC	0.7V <sub>CC</sub>		V	
V <sub>IL</sub>	Input LOW Voltage	CLK, DATA, LE, FC		0.3V <sub>CC</sub>	V	V <sub>CC</sub> = 5.5V
I <sub>IH</sub>	Input HIGH Current (DATA and CLK)		1.0	2.0	μA	V <sub>CC</sub> = 5.5V
I <sub>IL</sub>	Input LOW Current (DATA and CLK)		-10	-5.0	μA	V <sub>CC</sub> = 5.5V
I <sub>OSC</sub>	Input Current (OSCin)		130 -310		μA	OSCin = V <sub>CC</sub> OSCin = V <sub>CC</sub> - 2.2V
I <sub>IH</sub>	Input HIGH Current (LE and FC)		1.0	2.0	μA	
I <sub>IL</sub>	Input LOW Current (LE and FC)		-75	-60	μA	
I <sub>Source</sub> <sup>6</sup>	Charge Pump Output Current		-2.6	-2.0	mA	V <sub>DO</sub> = V <sub>p</sub> /2; V <sub>p</sub> = 2.7V V <sub>BISW</sub> = V <sub>p</sub> /2; V <sub>p</sub> = 2.7V
I <sub>Sink</sub> <sup>6</sup>	Do and BISW		+1.4	+2.0		
I <sub>HI-Z</sub>			-15	+15	nA	0.5 < V <sub>DO</sub> < V <sub>p</sub> -0.5 0.5 < V <sub>BISW</sub> < V <sub>p</sub> -0.5
V <sub>OH</sub>	Output HIGH Voltage (LD, φR, φP, f <sub>OUT</sub> )		4.4		V	V <sub>CC</sub> = 5.0V
			2.4		V	V <sub>CC</sub> = 3.0V
V <sub>OL</sub>	Output LOW Voltage (LD, φR, φP, f <sub>OUT</sub> )			0.4	V	V <sub>CC</sub> = 5.0V
				0.4	V	V <sub>CC</sub> = 3.0V
I <sub>OH</sub>	Output HIGH Current (LD, φR, φP, f <sub>OUT</sub> )		-1.0		mA	
I <sub>OL</sub>	Output LOW Current (LD, φR, φP, f <sub>OUT</sub> )		1.0		mA	

1. V<sub>CC</sub> = 3.3V, all outputs open.
2. V<sub>CC</sub> = 5.5V, all outputs open.
3. V<sub>p</sub> = 3.3V, all outputs open.

4. V<sub>p</sub> = 6.0V, all outputs open.
5. AC coupling, F<sub>IN</sub> measured with a 1000pF capacitor.
6. Source current flows out of the pin and sink current flows into the pin.

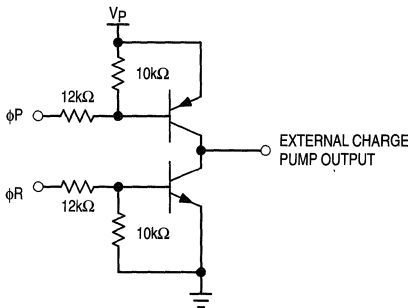


Figure 8. Typical External Charge Pump Circuit

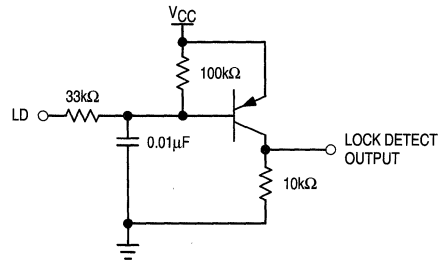
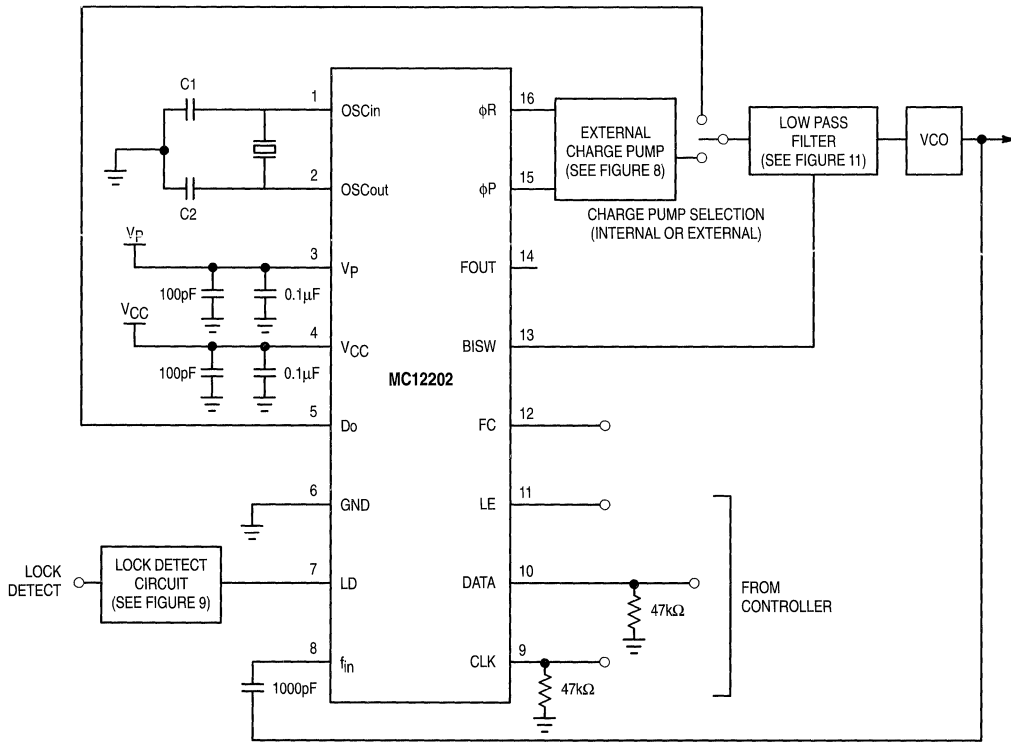


Figure 9. Typical Lock Detect Circuit





C1, C2: Dependent on Crystal Oscillator

Figure 10. Typical Applications Example (16-Pin Package)

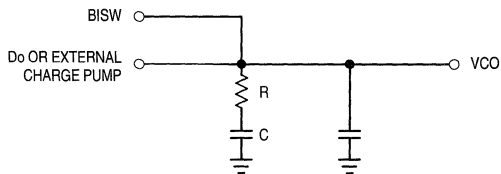


Figure 11. Typical Loop Filter

# Serial Input PLL Frequency Synthesizer

The MC12206 is a 2.0GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse-swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over 2.7 to 5.5V supply range for input frequencies up to 2.0GHz with a typical current drain of 7.4mA. The low power consumption makes the MC12206 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 64/65 or 128/129 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 6.7mA Typical for I<sub>CC</sub> and 0.7mA Typical for I<sub>p</sub>
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 64/65 or 128/129
- On-Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14-Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7-Bit Swallow Counter and an 11-Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of -40°C to +85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages

**MC12206**

**MECL PLL COMPONENTS**

**Serial Input PLL  
 Frequency Synthesizer**



**D SUFFIX**  
 PLASTIC SOIC PACKAGE  
 CASE 751B-05



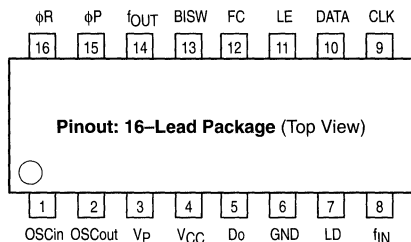
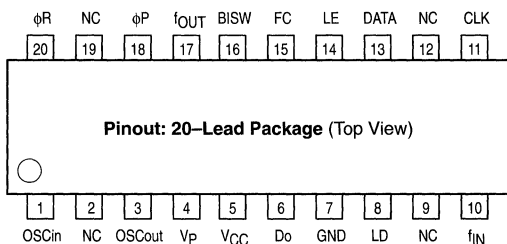
**DT SUFFIX**  
 PLASTIC TSSOP PACKAGE  
 CASE 948E-03

**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 4 (Pin 5 in 20-lead package)	-0.5 to +6.0	VDC
V <sub>P</sub>	Power Supply Voltage, Pin 3 (Pin 4 in 20-lead package)	V <sub>CC</sub> to +6.0	VDC
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MOSAIC V and *InterActiveApNote* are trademarks of Motorola, Inc.

CASE 751B  
ACTUAL SIZECASE 948E  
ACTUAL SIZE**PIN NAMES**

Pin	I/O	Function	16-Lead Pkg Pin No.	20-Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal is connected between OSCin and OSCout. An external source can be AC coupled into this input	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V <sub>P</sub>	—	Power supply for charge pumps (V <sub>P</sub> should be greater than or equal to V <sub>CC</sub> ) V <sub>P</sub> provides power to the Do, BISW and phiP outputs	3	4
V <sub>CC</sub>	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f <sub>IN</sub>	I	Prescaler input. The VCO signal is AC-coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects f <sub>p</sub> or f <sub>r</sub> on the f <sub>OUT</sub> pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN ("analog switch is ON") the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f <sub>OUT</sub>	O	Phase comparator input signal. When FC is HIGH, f <sub>OUT</sub> =f <sub>r</sub> , programmable reference divider output; when FC is LOW, f <sub>OUT</sub> =f <sub>p</sub> , programmable divider output	14	17
phiP	O	Output for external charge pump. Standard CMOS output level	15	18
phiR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

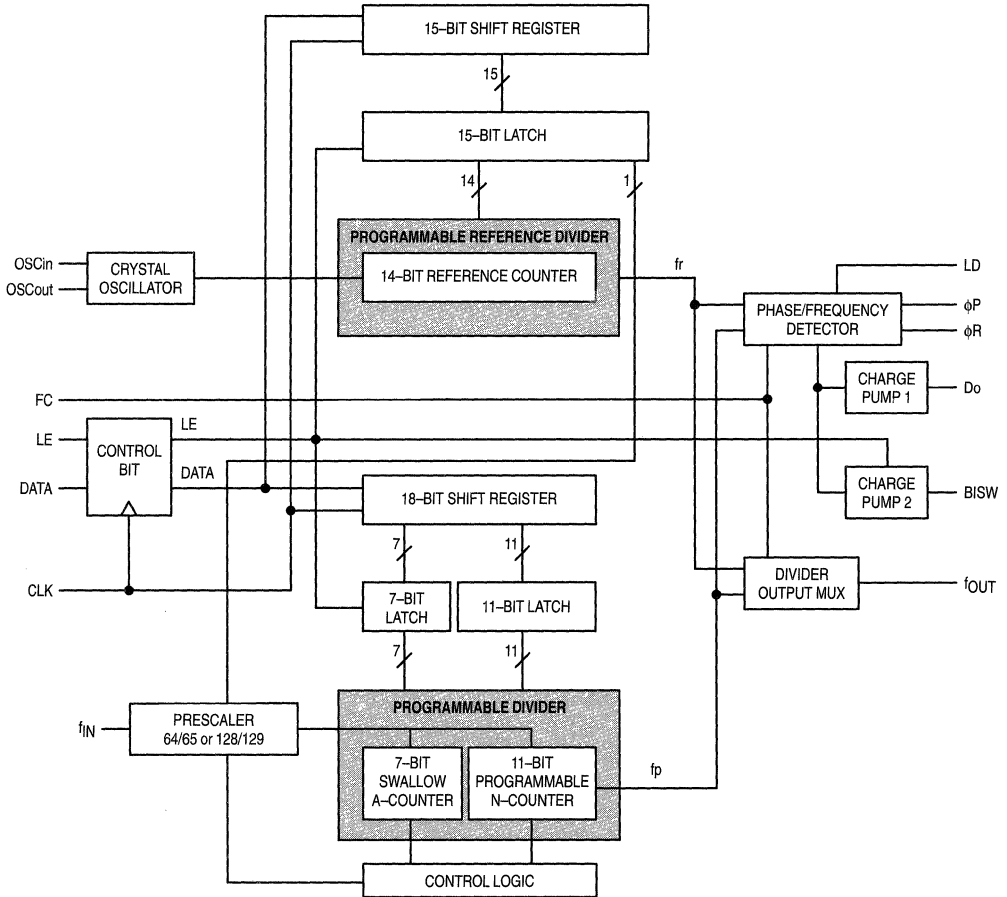


Figure 1. MC12206 Block Diagram

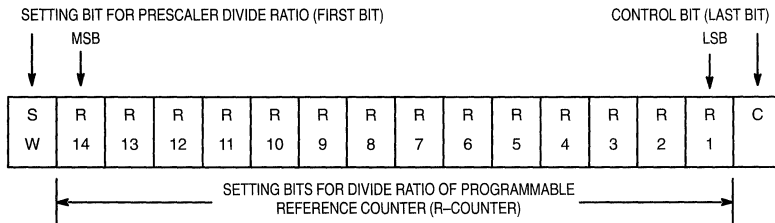
**DATA ENTRY FORMAT**

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14-bit programmable reference divider plus the prescaler setting bit, and the 18-bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

Control bit: "H" = data is transferred into 15-bit latch of programmable reference divider  
 "L" = data is transferred into 18-bit latch of programmable divider

**PROGRAMMABLE REFERENCE DIVIDER**

16-bit serial data format for the programmable reference counter, "R-counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15-bit shift register into the 15-bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for +128/129, SW=1 for +64/65). An R divide ratio less than 8 is prohibited. For Control bit (C) = HIGH:



**DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER**

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

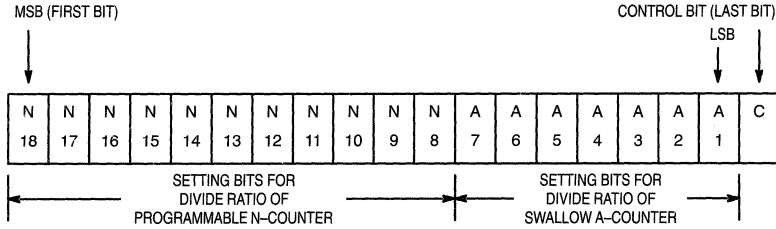
**PRESCALER SELECT BIT**

Prescaler Divide Ratio P	SW
128/129	0
64/65	1

**PROGRAMMABLE DIVIDER**

19-bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18-bit shift register into the 18-bit latch which specifies the swallow A-counter divide ratio (0 to 127) and the programmable N-counter divide ratio (16 to 2047). An N-counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



**DIVIDE RATIO OF PROGRAMMABLE N-COUNTER**

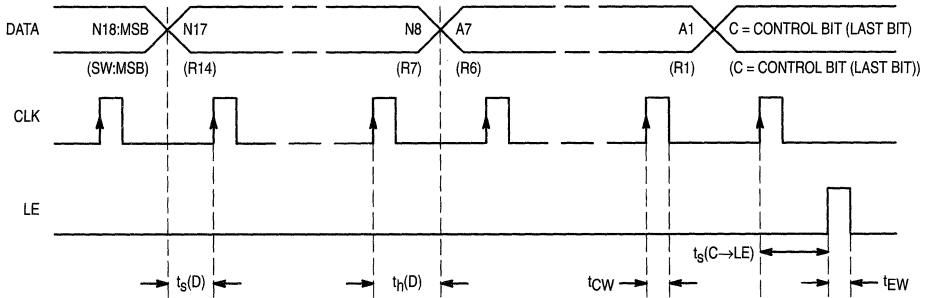
**DIVIDE RATIO OF SWALLOW A-COUNTER**

Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	127	1	1	1	1	1	1	1

**DIVIDE RATIO SETTING**

$$f_{vco} = [(P \cdot N) + A] \cdot f_{osc} \div R \text{ with } A < N$$

- f<sub>vco</sub>: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7-bit swallow counter (0 to 127, A < N)
- f<sub>osc</sub>: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (64 or 128)



NOTES: Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

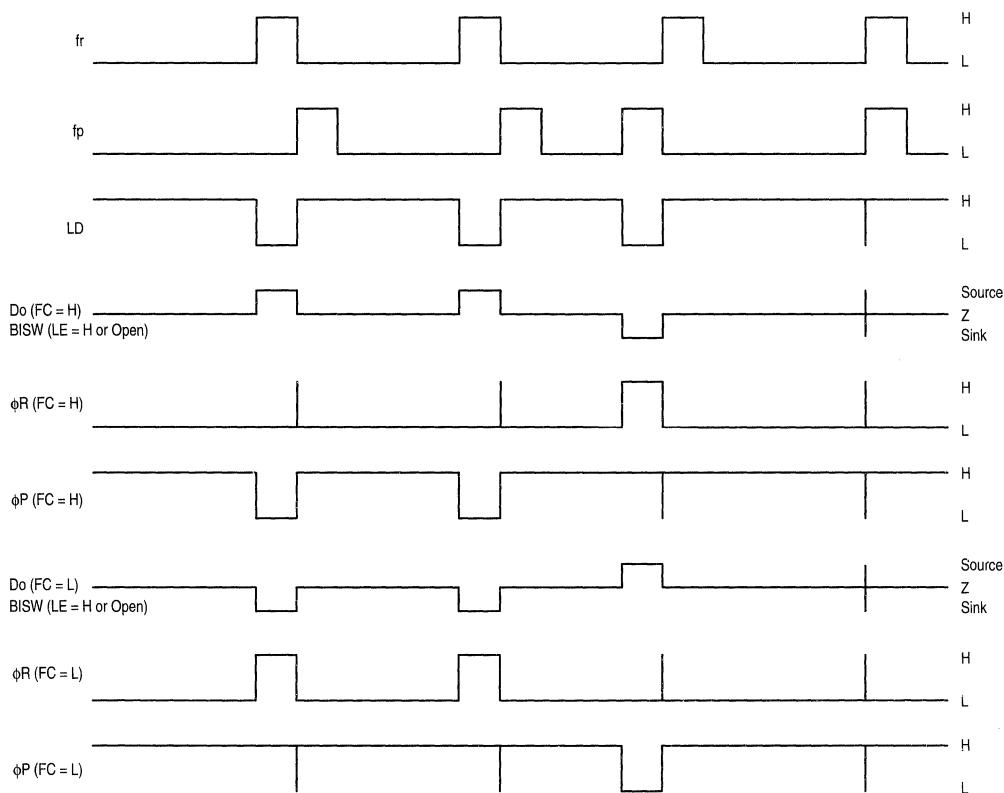
- t<sub>s</sub>(D) = Setup Time DATA to CLK      t<sub>s</sub>(D) ≥ 10ns
- t<sub>h</sub>(D) = Hold Time DATA to CLK      t<sub>h</sub>(D) ≥ 20ns
- t<sub>CW</sub> = CLK Pulse Width      t<sub>CW</sub> ≥ 30ns
- t<sub>EW</sub> = LE Pulse Width      t<sub>EW</sub> ≥ 20ns
- t<sub>s</sub>(C->LE) = Setup Time CLK to LE      t<sub>s</sub>(C->LE) ≥ 30ns

**Figure 2. Serial Data Input Timing**

## PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12206 is a high speed digital phase frequency detector circuit. The circuit determines the “lead” or “lag” phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians. The phase comparator outputs are standard CMOS rail-to-rail levels ( $V_P$  to GND for  $\phi_P$  and  $V_{CC}$  to GND for  $\phi_R$ ), designed for up to 20MHz operation into a 15pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures 3 and 5. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs,  $\phi_R$  and  $\phi_P$ , as well as the charge pump output Do can be reversed by switching the FC pin.



NOTES: Do and BISW are current outputs.  
 Phase difference detection range:  $-2\pi$  to  $+2\pi$   
 Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.  
 When  $f_r > f_p$  or  $f_r < f_p$ , spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{\text{source}} + I_{\text{sink}}}{4\pi} \right| = \frac{4\text{mA}}{4\pi}$$

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms

**For FC = HIGH:**

**fr lags fp in phase OR fp > fr in frequency**

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the φP output will remain in a HIGH state while the φR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φR indicates to the VCO to decrease in frequency to bring the loop into lock.

**fr leads fp in phase OR fp < fr in frequency**

When the phase of fr leads that of fp or the frequency of fp is less than fr, the φR output will remain in a LOW state while the φP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φP indicates to the VCO to increase in frequency to bring the loop to lock.

**fr = fp in phase and frequency**

When the phase and frequency of fr and fp are equal, the output φP will remain in a HIGH state and φR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

**For FC = LOW:**

**fr lags fp in phase OR fp > fr in frequency**

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the φR output will remain in a LOW state while the φP output will pulse from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φP indicates to the VCO to increase in frequency to bring the loop into lock.

**fr leads fp in phase OR fp < fr in frequency**

When the phase of fr leads that of fp or the frequency of fp is less than fr, the φP output will remain in a HIGH state while the φR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φR indicates to the VCO to decrease in frequency to bring the loop to lock.

**fr = fp in phase and frequency**

When the phase and frequency of fr and fp are equal, the output φP will remain in a HIGH state and φR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the f<sub>OUT</sub> test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the f<sub>OUT</sub> output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, f<sub>OUT</sub> = fr, the programmable reference divider output. When FC is LOW, f<sub>OUT</sub> = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. f<sub>OUT</sub> = fr

If VCO characteristics are like (2), FC should be set LOW. f<sub>OUT</sub> = fp

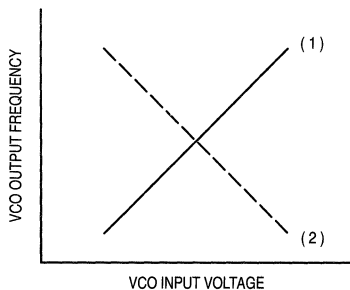


Figure 4. VCO Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	φR	φP	f <sub>OUT</sub>	Do	φR	φP	f <sub>OUT</sub>
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTES: Z = High impedance  
When LE is High or Open, BISW has the same characteristics as Do.

Figure 5. Phase Comparator, Internal Charge Pump, and f<sub>OUT</sub> Characteristics



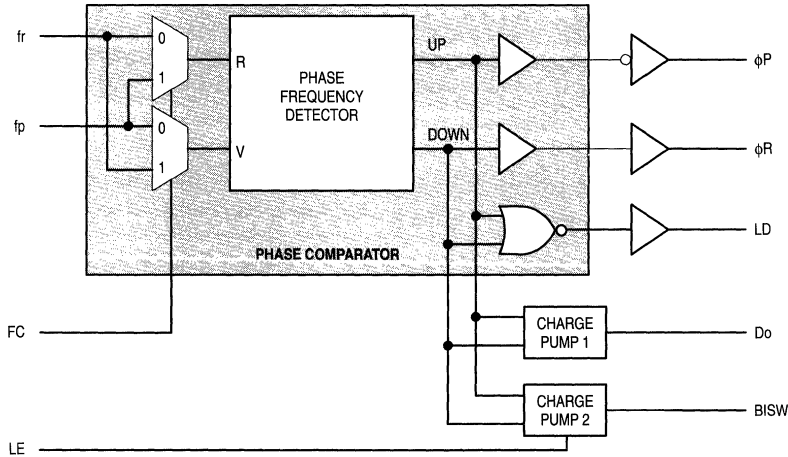


Figure 6. Detailed Phase Comparator Block Diagram

**LOCK DETECT**

The Lock Detect (LD) output pin provides a LOW pulse when fr and fp are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector’s outputs UP and DOWN. See Figure 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See Figure 9.

**OSCILLATOR INPUT**

The device incorporates an on–chip reference oscillator/buffer so that an external parallel–resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure 10 are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance).

If an external reference oscillator is available, the signal should be AC–coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC–coupled signal must be between 500 and 2200 mV peak–to–peak.

**DUAL INTERNAL CHARGE PUMPS (“ANALOG SWITCH”)**

Due to the pure Bipolar nature of the MC12206 design, the “analog switch” function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure 7 below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN (“analog switch is ON”), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

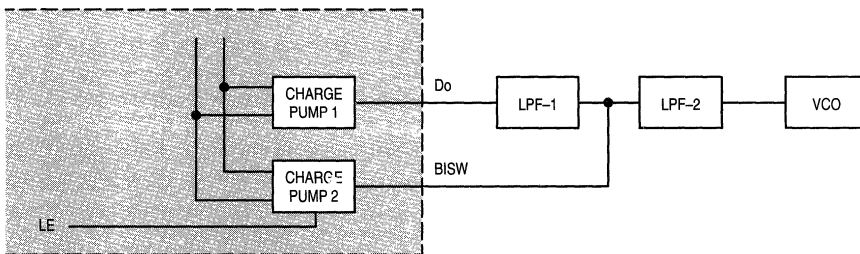


Figure 7. “Analog Switch” Block Diagram

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$I_{CC}$	Supply Current for $V_{CC}$		6.7	10.5	mA	Note 1
			8.1	12.5		Note 2
$I_P$	Supply Current for $V_P$		0.7	1.1	mA	Note 3
			0.8	1.3		Note 4
$F_{IN}$	Operating Frequency $f_{INmax}$ $f_{INmin}$	2000		500	MHz	Note 5
$F_{OSC}$	Operating Frequency (OSCin)		12	20	MHz	Crystal Mode
				40	MHz	External Reference Mode
$V_{IN}$	Input Sensitivity $f_{IN}$	200		1000	mV <sub>p-p</sub>	
$V_{OSC}$	OSCin	500		2200	mV <sub>p-p</sub>	
$V_{IH}$	Input HIGH Voltage CLK, DATA, LE, FC	$0.7V_{CC}$			V	
$V_{IL}$	Input LOW Voltage CLK, DATA, LE, FC			$0.3V_{CC}$	V	$V_{CC} = 5.5V$
$I_{IH}$	Input HIGH Current (DATA and CLK)		1.0	2.0	$\mu A$	$V_{CC} = 5.5V$
$I_{IL}$	Input LOW Current (DATA and CLK)	-10	-5.0		$\mu A$	$V_{CC} = 5.5V$
$I_{OSC}$	Input Current (OSCin)		130 -310		$\mu A$	OSCin = $V_{CC}$ OSCin = $V_{CC} - 2.2V$
$I_{IH}$	Input HIGH Current (LE and FC)		1.0	2.0	$\mu A$	
$I_{IL}$	Input LOW Current (LE and FC)	-75	-60		$\mu A$	
$I_{Source}^6$	Charge Pump Output Current	-2.6	-2.0	-1.4	mA	$V_{DO} = V_P/2$ ; $V_P = 2.7V$
$I_{Sink}^6$	Do and BISW	+1.4	+2.0	+2.6		$V_{BISW} = V_P/2$ ; $V_P = 2.7V$
$I_{HI-Z}$		-15		+15	nA	$0.5 < V_{DO} < V_P - 0.5$ $0.5 < V_{BISW} < V_P - 0.5$
$V_{OH}$	Output HIGH Voltage (LD, $\phi R$ , $\phi P$ , $f_{OUT}$ )		4.4		V	$V_{CC} = 5.0V$
			2.4		V	$V_{CC} = 3.0V$
$V_{OL}$	Output LOW Voltage (LD, $\phi R$ , $\phi P$ , $f_{OUT}$ )			0.4	V	$V_{CC} = 5.0V$
				0.4	V	$V_{CC} = 3.0V$
$I_{OH}$	Output HIGH Current (LD, $\phi R$ , $\phi P$ , $f_{OUT}$ )	-1.0			mA	
$I_{OL}$	Output LOW Current (LD, $\phi R$ , $\phi P$ , $f_{OUT}$ )	1.0			mA	

1.  $V_{CC} = 3.3V$ , all outputs open.

2.  $V_{CC} = 5.5V$ , all outputs open.

3.  $V_P = 3.3V$ , all outputs open.

4.  $V_P = 6.0V$ , all outputs open.

5. AC coupling,  $F_{IN}$  measured with a 1000pF capacitor.

6. Source current flows out of the pin and sink current flows into the pin.

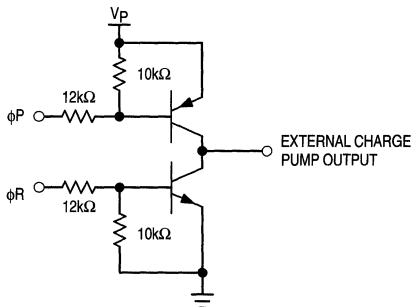


Figure 8. Typical External Charge Pump Circuit

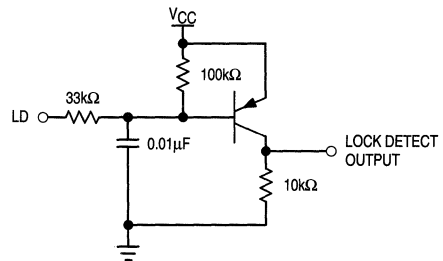
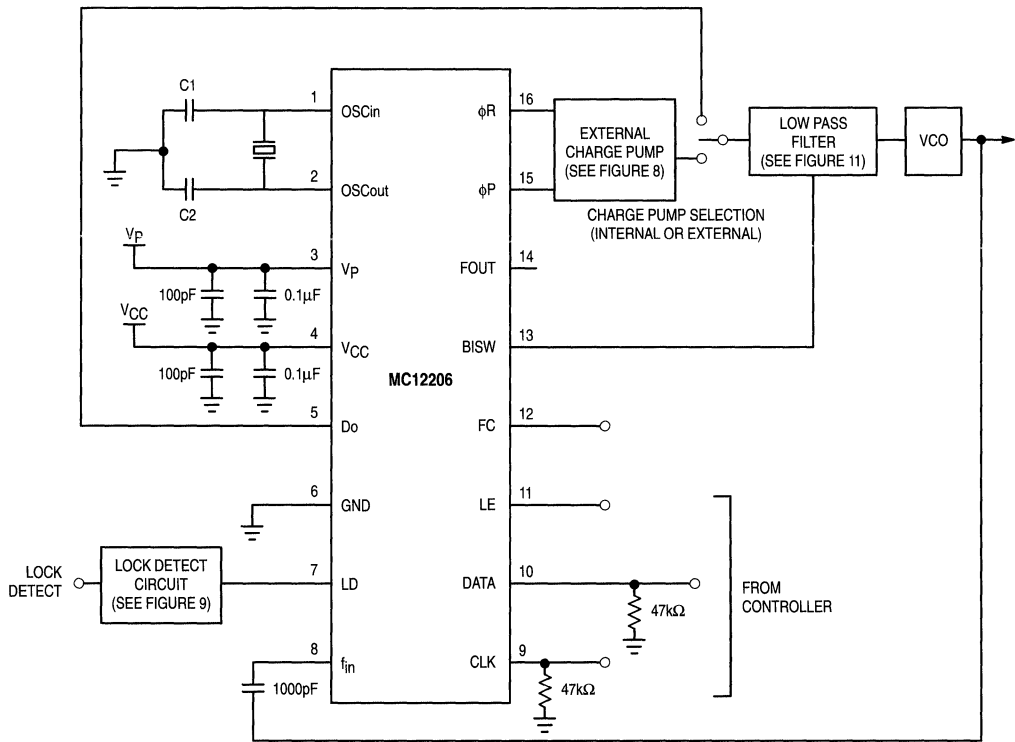


Figure 9. Typical Lock Detect Circuit



C1, C2: Dependent on Crystal Oscillator

Figure 10. Typical Applications Example (16-Pin Package)

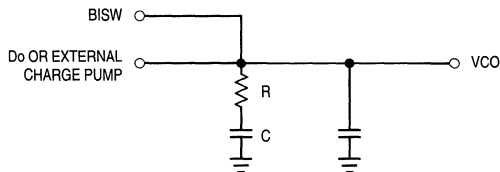


Figure 11. Typical Loop Filter

## Serial Input PLL Frequency Synthesizer

The MC12210 is a 2.5GHz Bipolar monolithic serial input phase locked loop (PLL) synthesizer with pulse-swallow function. It is designed to provide the high frequency local oscillator signal of an RF transceiver in handheld communication applications.

Motorola's advanced Bipolar MOSAIC™ V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over 2.7 to 5.5V supply range for input frequencies up to 2.5GHz with a typical current drain of 9.5mA. The low power consumption makes the MC12210 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication services. A dual modulus prescaler is integrated to provide either a 32/33 or 64/65 divide ratio.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 8.8mA Typical for I<sub>CC</sub> and 0.7mA Typical for I<sub>p</sub>
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 32/33 or 64/65
- On-Chip Reference Oscillator/Buffer
- Programmable Reference Divider Consisting of a Binary 14-Bit Programmable Reference Counter
- Programmable Divider Consisting of a Binary 7-Bit Swallow Counter and an 11-Bit Programmable Counter
- Phase/Frequency Detector With Phase Conversion Function
- Balanced Charge Pump Outputs
- Dual Internal Charge Pumps for Bypassing the First Stage of the Loop Filter to Decrease Lock Time
- Outputs for External Charge Pump
- Operating Temperature Range of -40°C to +85°C
- Space Efficient Plastic Surface Mount SOIC or TSSOP Packages

**MC12210**

### MECL PLL COMPONENTS

#### Serial Input PLL Frequency Synthesizer



**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751B-05



**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 948E-02

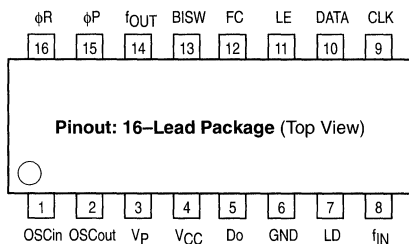
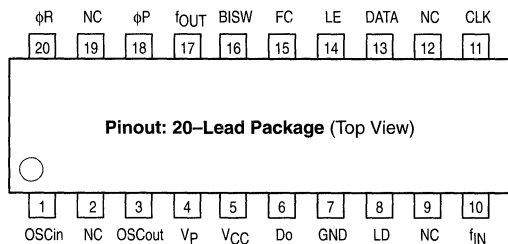
### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 4 (Pin 5 in 20-lead package)	-0.5 to +6.0	VDC
V <sub>p</sub>	Power Supply Voltage, Pin 3 (Pin 4 in 20-lead package)	V <sub>CC</sub> to +6.0	VDC
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

MOSAIC V and *InterActiveApNote* are trademarks of Motorola, Inc.



CASE 751B  
ACTUAL SIZECASE 948E  
ACTUAL SIZE**PIN NAMES**

Pin	I/O	Function	16-Lead Pkg Pin No.	20-Lead Pkg Pin No.
OSCin	I	Oscillator input. A crystal is connected between OSCin and OSCout. An external source can be AC coupled into this input	1	1
OSCout	O	Oscillator output. Pin should be left open if external source is used	2	3
V <sub>p</sub>	—	Power supply for charge pumps (V <sub>p</sub> should be greater than or equal to V <sub>CC</sub> ) V <sub>p</sub> provides power to the Do, BISW and φP outputs	3	4
V <sub>CC</sub>	—	Power supply voltage input. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	4	5
Do	O	Internal charge pump output. Do remains on at all times	5	6
GND	—	Ground	6	7
LD	O	Lock detect, phase comparator output	7	8
f <sub>IN</sub>	I	Prescaler input. The VCO signal is AC-coupled into this pin	8	10
CLK	I	Clock input. Rising edge of the clock shifts data into the shift registers	9	11
DATA	I	Binary serial data input	10	13
LE	I	Load enable input (with internal pull up resistor). When LE is HIGH or OPEN, data stored in the shift register is transferred into the appropriate latch (depending on the level of control bit). Also, when LE is HIGH or OPEN, the output of the second internal charge pump is connected to the BISW pin	11	14
FC	I	Phase control select (with internal pull up resistor). When FC is LOW, the characteristics of the phase comparator and charge pump are reversed. FC also selects f <sub>p</sub> or f <sub>r</sub> on the f <sub>OUT</sub> pin	12	15
BISW	O	Analog switch output. When LE is HIGH or OPEN ("analog switch is ON") the output of the second charge pump is connected to the BISW pin. When LE is LOW, BISW is high impedance	13	16
f <sub>OUT</sub>	O	Phase comparator input signal. When FC is HIGH, f <sub>OUT</sub> =f <sub>r</sub> , programmable reference divider output; when FC is LOW, f <sub>OUT</sub> =f <sub>p</sub> , programmable divider output	14	17
φP	O	Output for external charge pump. Standard CMOS output level	15	18
φR	O	Output for external charge pump. Standard CMOS output level	16	20
NC	—	No connect	—	2, 9, 12, 19

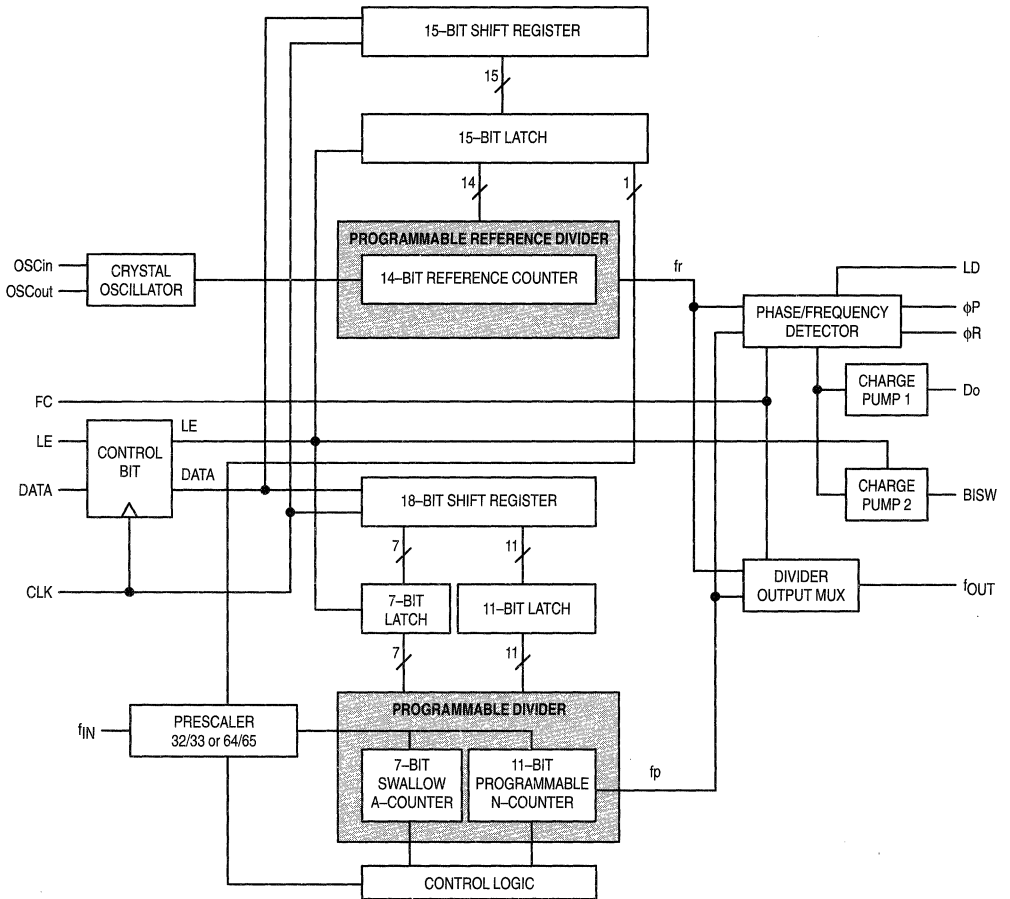


Figure 1. MC12210 Block Diagram

**DATA ENTRY FORMAT**

The three wire interface of DATA pin, CLK (clock) pin and LE (load enable) pin controls the serial data input of the 14-bit programmable reference divider plus the prescaler setting bit, and the 18-bit programmable divider. A rising edge of the clock shifts one bit of serial data into the internal shift registers. Depending upon the level of the control bit, stored data is transferred into the latch when load enable pin is HIGH or OPEN.

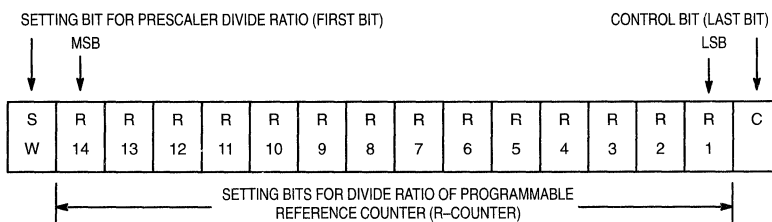
Control bit: "H" = data is transferred into 15-bit latch of programmable reference divider

"L" = data is transferred into 18-bit latch of programmable divider

**PROGRAMMABLE REFERENCE DIVIDER**

16-bit serial data format for the programmable reference counter, "R-counter", and prescaler select bit (SW) is shown below. If the control bit is HIGH, data is transferred from the 15-bit shift register into the 15-bit latch which specifies the R divide ratio (8 to 16383) and the prescaler divide ratio (SW=0 for +64/65, SW=1 for +32/33). An R divide ratio less than 8 is prohibited.

For Control bit (C) = HIGH:



**DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER**

Divide Ratio R	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

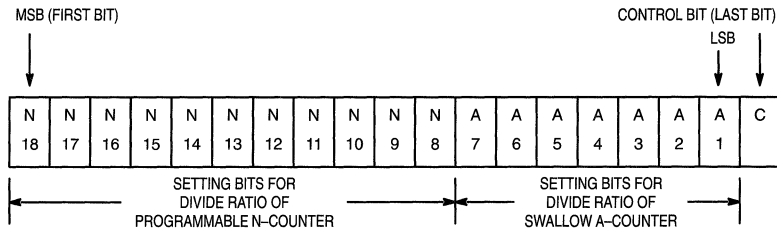
**PRESCALER SELECT BIT**

Prescaler Divide Ratio P	SW
64/65	0
32/33	1

**PROGRAMMABLE DIVIDER**

19-bit serial data format for the programmable divider is shown below. If the control bit is LOW, data is transferred from the 18-bit shift register into the 18-bit latch which specifies the swallow A-counter divide ratio (0 to 127) and the programmable N-counter divide ratio (16 to 2047). An N-counter divide ratio less than 16 is prohibited.

For Control bit (C) = LOW:



**DIVIDE RATIO OF PROGRAMMABLE N-COUNTER**

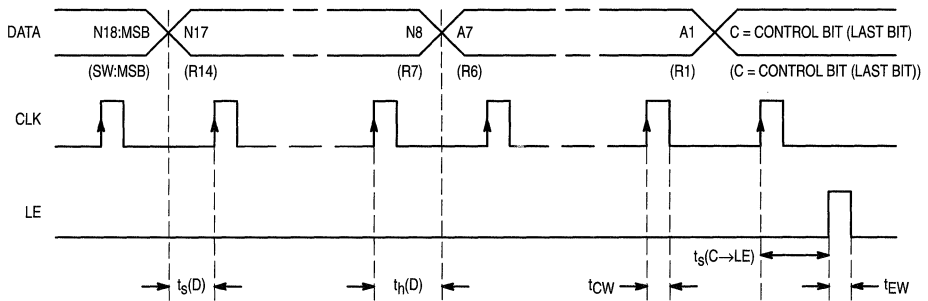
**DIVIDE RATIO OF SWALLOW A-COUNTER**

Divide Ratio N	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8	Divide Ratio A	A 7	A 6	A 5	A 4	A 3	A 2	A 1
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	127	1	1	1	1	1	1	1

**DIVIDE RATIO SETTING**

$$f_{vco} = [(P \cdot N) + A] \cdot f_{osc} \div R \text{ with } A < N$$

- f<sub>vco</sub>: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 7-bit swallow counter (0 to 127, A < N)
- f<sub>osc</sub>: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (32 or 64)



NOTES: Programmable reference divider data shown in parenthesis. Data shifted into register on rising edge of CLK.

$t_s(D)$ = Setup Time DATA to CLK	$t_s(D) \geq 10\text{ns}$
$t_h(D)$ = Hold Time DATA to CLK	$t_h(D) \geq 20\text{ns}$
$t_{CW}$ = CLK Pulse Width	$t_{CW} \geq 30\text{ns}$
$t_{EW}$ = LE Pulse Width	$t_{EW} \geq 20\text{ns}$
$t_s(C \rightarrow LE)$ = Setup Time CLK to LE	$t_s(C \rightarrow LE) \geq 30\text{ns}$

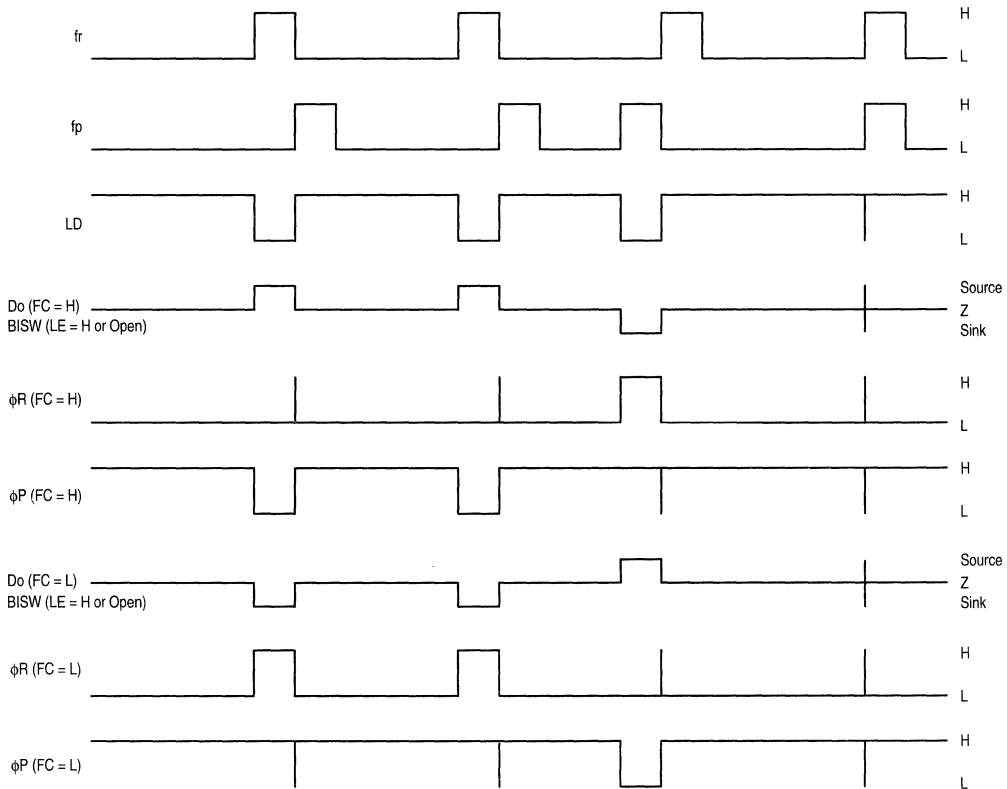
**Figure 2. Serial Data Input Timing**



### PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12210 is a high speed digital phase frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fp) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians. The phase comparator outputs are standard CMOS rail-to-rail levels ( $V_P$  to GND for  $\phi_P$  and  $V_{CC}$  to GND for  $\phi_R$ ), designed for up to 20MHz operation into a 15pF load. These phase comparator outputs can be used along with an external charge pump to enhance the PLL characteristics.

The operation of the phase comparator is shown in Figures 3 and 5. The phase characteristics of the phase comparator are controlled by the FC pin. The polarity of the phase comparator outputs,  $\phi_R$  and  $\phi_P$ , as well as the charge pump output Do can be reversed by switching the FC pin.



NOTES: Do and BISW are current outputs.  
 Phase difference detection range:  $-2\pi$  to  $+2\pi$   
 Spike difference depends on charge pump characteristics. Also, the spike is output in order to diminish dead band.  
 When  $fr > fp$  or  $fr < fp$ , spike might not appear depending upon charge pump characteristics.

$$\text{Internal Charge Pump Gain} \approx \left| \frac{I_{\text{source}} + I_{\text{sink}}}{4\pi} \right| = \frac{4\text{mA}}{4\pi}$$

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms

**For FC = HIGH:**

**fr lags fp in phase OR fp>fr in frequency**

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the φP output will remain in a HIGH state while the φR output will pulse from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φR indicates to the VCO to decrease in frequency to bring the loop into lock.

**fr leads fp in phase OR fp<fr in frequency**

When the phase of fr leads that of fp or the frequency of fp is less than fr, the φR output will remain in a LOW state while the φP output pulses from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φP indicates to the VCO to increase in frequency to bring the loop to lock.

**fr = fp in phase and frequency**

When the phase and frequency of fr and fp are equal, the output φP will remain in a HIGH state and φR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

When FC = LOW, the operation of the phase comparator is reversed from the above explanation.

**For FC = LOW:**

**fr lags fp in phase OR fp>fr in frequency**

When the phase of fr lags that of fp or the frequency of fp is greater than fr, the φR output will remain in a LOW state while the φP output will pulse from HIGH to LOW. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φP indicates to the VCO to increase in frequency to bring the loop into lock.

**fr leads fp in phase OR fp<fr in frequency**

When the phase of fr leads that of fp or the frequency of fp is less than fr, the φP output will remain in a HIGH state while the φR output pulses from LOW to HIGH. The output pulse will reach a minimum 50% duty cycle under a 180° out of phase condition. The signal on φR indicates to the VCO to decrease in frequency to bring the loop to lock.

**fr = fp in phase and frequency**

When the phase and frequency of fr and fp are equal, the output φP will remain in a HIGH state and φR will remain in a LOW state except for voltage spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

The FC pin controls not only the phase characteristics, but also controls the fOUT test pin. The FC pin permits the user to monitor either of the phase comparator input signals, fr or fp, at the fOUT output providing a test mode where the programming of the dividers and the output of the counters can be checked. When FC is HIGH, fOUT = fr, the programmable reference divider output. When FC is LOW, fOUT = fp, the programmable divider output.

Hence,

If VCO characteristics are like (1), FC should be set HIGH or OPEN. fOUT = fr

If VCO characteristics are like (2), FC should be set LOW. fOUT = fp

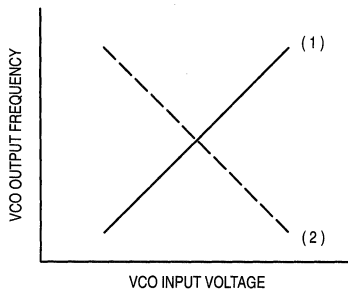


Figure 4. VCO Characteristics

	FC = HIGH or OPEN				FC = LOW			
	Do	φR	φP	fOUT	Do	φR	φP	fOUT
fp < fr	H	L	L	fr	L	H	H	fp
fp > fr	L	H	H	fr	H	L	L	fp
fp = fr	Z	L	H	fr	Z	L	H	fp

NOTES: Z = High impedance  
When LE is HIGH or Open, B1SW has the same characteristics as Do.

Figure 5. Phase Comparator, Internal Charge Pump, and fOUT Characteristics

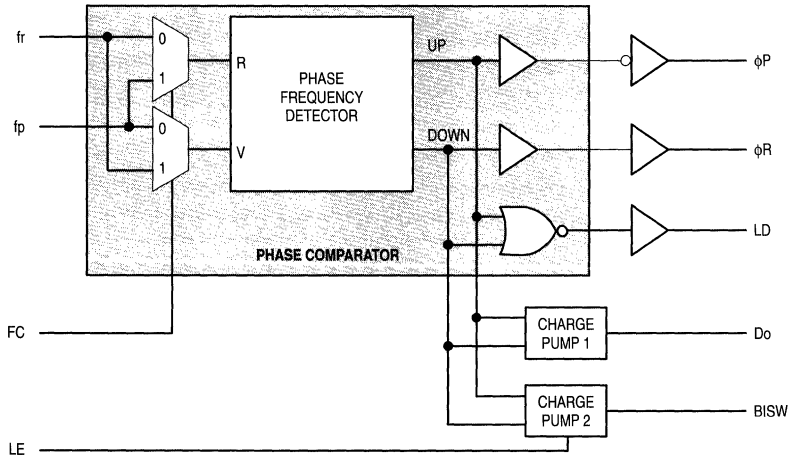


Figure 6. Detailed Phase Comparator Block Diagram

### LOCK DETECT

The Lock Detect (LD) output pin provides a LOW pulse when  $f_r$  and  $f_p$  are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See Figure 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See Figure 9.

### OSCILLATOR INPUT

The device incorporates an on-chip reference oscillator/buffer so that an external parallel-resonant fundamental crystal can be connected between OSCin and OSCout. External capacitor C1 and C2 as shown in Figure 10 are required to set the proper crystal load capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen (up to a maximum of 30 pF each including parasitic and stray capacitance).

If an external reference oscillator is available, the signal should be AC-coupled to the OSCin pin through a coupling capacitor. In this case, no connection to OSCout is required. The magnitude of the AC-coupled signal must be between 500 and 2200 mV peak-to-peak.

### DUAL INTERNAL CHARGE PUMPS ("ANALOG SWITCH")

Due to the pure Bipolar nature of the MC12210 design, the "analog switch" function is implemented with dual internal charge pumps. The loop filter time constant can be decreased by bypassing the first stage of the loop filter with the charge pump output BISW as shown in Figure 7 below. This enables the VCO to lock in a shorter amount of time.

When LE is HIGH or OPEN ("analog switch is ON"), the output of the second internal charge pump is connected to the BISW pin, and the Do output is ON. The charge pump 2 output on BISW is essentially equal to the charge pump 1 output on Do. When LE is LOW, BISW is in a high impedance state and Do output is active.

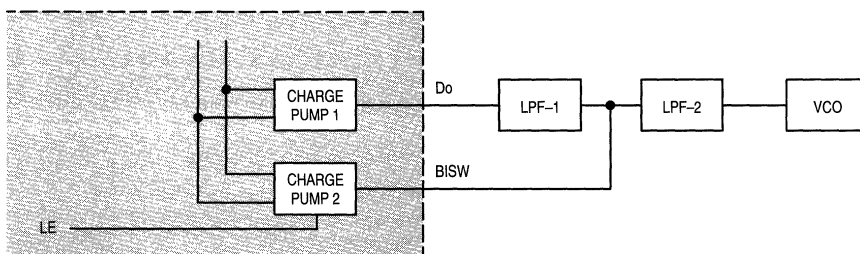


Figure 7. "Analog Switch" Block Diagram

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5V$ ;  $T_A = -40$  to  $+85^{\circ}C$ )

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I <sub>CC</sub>	Supply Current for V <sub>CC</sub>		8.8	13.0	mA	Note 1
			10.2	16.0		Note 2
I <sub>P</sub>	Supply Current for V <sub>P</sub>		0.7	1.1	mA	Note 3
			0.8	1.3		Note 4
F <sub>IN</sub>	Operating Frequency f <sub>INmax</sub> f <sub>INmin</sub>	2500		500	MHz	Note 5
F <sub>OSC</sub>	Operating Frequency (OSCin)		12	20	MHz	Crystal Mode
				40	MHz	External Reference Mode
V <sub>IN</sub>	Input Sensitivity f <sub>IN</sub>	200		1000	mV <sub>P-P</sub>	
V <sub>OSC</sub>	OSCin	500		2200	mV <sub>P-P</sub>	
V <sub>IH</sub>	Input HIGH Voltage CLK, DATA, LE, FC	0.7V <sub>CC</sub>			V	
V <sub>IL</sub>	Input LOW Voltage CLK, DATA, LE, FC			0.3V <sub>CC</sub>	V	V <sub>CC</sub> = 5.5V
I <sub>IH</sub>	Input HIGH Current (DATA and CLK)		1.0	2.0	μA	V <sub>CC</sub> = 5.5V
I <sub>IL</sub>	Input LOW Current (DATA and CLK)	-10	-5.0		μA	V <sub>CC</sub> = 5.5V
I <sub>OSC</sub>	Input Current (OSCin)		130 -310		μA	OSCin = V <sub>CC</sub> OSCin = V <sub>CC</sub> - 2.2V
I <sub>IH</sub>	Input HIGH Current (LE and FC)		1.0	2.0	μA	
I <sub>IL</sub>	Input LOW Current (LE and FC)	-75	-60		μA	
I <sub>Source</sub> <sup>6</sup>	Charge Pump Output Current	-2.6	-2.0	-1.4	mA	V <sub>DO</sub> = V <sub>P</sub> /2; V <sub>P</sub> = 2.7V
I <sub>Sink</sub> <sup>6</sup>	Do and BISW	+1.4	+2.0	+2.6		V <sub>BISW</sub> = V <sub>P</sub> /2; V <sub>P</sub> = 2.7V
I <sub>Hi-Z</sub>		-15		+15	nA	0.5 < V <sub>DO</sub> < V <sub>P</sub> - 0.5 0.5 < V <sub>BISW</sub> < V <sub>P</sub> - 0.5
V <sub>OH</sub>	Output HIGH Voltage (LD, φR, φP, f <sub>OUT</sub> )		4.4		V	V <sub>CC</sub> = 5.0V
			2.4		V	V <sub>CC</sub> = 3.0V
V <sub>OL</sub>	Output LOW Voltage (LD, φR, φP, f <sub>OUT</sub> )			0.4	V	V <sub>CC</sub> = 5.0V
				0.4	V	V <sub>CC</sub> = 3.0V
I <sub>OH</sub>	Output HIGH Current (LD, φR, φP, f <sub>OUT</sub> )	-1.0			mA	
I <sub>OL</sub>	Output LOW Current (LD, φR, φP, f <sub>OUT</sub> )	1.0			mA	

- V<sub>CC</sub> = 3.3V, all outputs open.
- V<sub>CC</sub> = 5.5V, all outputs open.
- V<sub>P</sub> = 3.3V, all outputs open.

- V<sub>P</sub> = 6.0V, all outputs open.
- AC coupling, F<sub>IN</sub> measured with a 1000pF capacitor.
- Source current flows out of the pin and sink current flows into the pin.

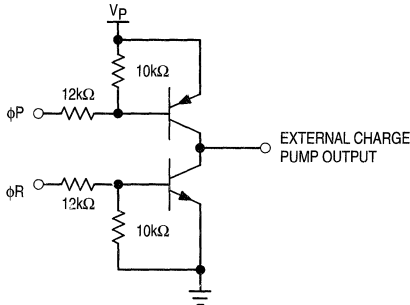


Figure 8. Typical External Charge Pump Circuit

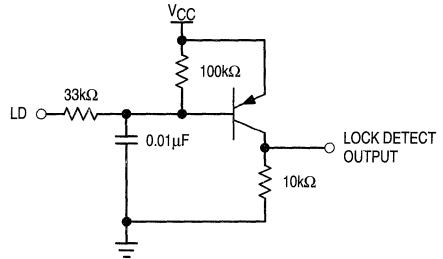
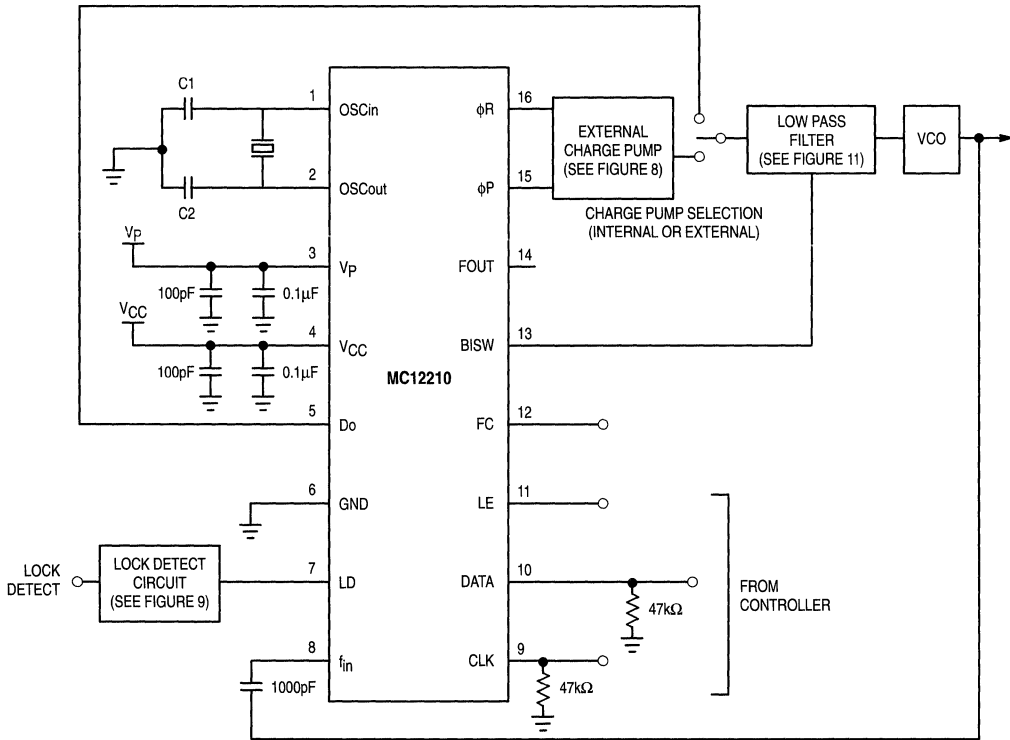


Figure 9. Typical Lock Detect Circuit



C1, C2: Dependent on Crystal Oscillator

Figure 10. Typical Applications Example (16-Pin Package)

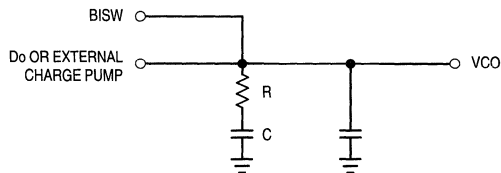


Figure 11. Typical Loop Filter

## 500-2800MHz Single Channel Frequency Synthesizer

The MC12179 is a monolithic Bipolar synthesizer integrating the high frequency prescaler, phase/frequency detector, charge pump, and reference oscillator/buffer functions. When combined with an external loop filter and VCO, the MC12179 serves as a complete PLL subsystem. Motorola's advanced MOSAIC™ V technology is utilized for low power operation at a 5V supply voltage. The device is designed for operation up to 2.8GHz for high frequency applications such as CATV down converters and satellite receiver tuners.

- 2.8GHz Maximum Operating Frequency
- Low Power Supply Current of 3.5mA Typical, Including I<sub>CC</sub> and I<sub>p</sub> Currents
- Supply Voltage of 5.0V Typical
- Integrated Divide by 256 Prescaler
- On-Chip Reference Oscillator/Buffer
  - 2–11MHz Operation When Driven From Reference Source
  - 5–11MHz Operation When Used With a Crystal
- Digital Phase/Frequency Detector with Linear Transfer Function
- Balanced Charge Pump Output
- Space Efficient 8-Lead SOIC
- Operating Temperature Range of –40°C to +85°C

For additional information on calculating the loop filter components, an *InterActiveApNote*™ document containing software (based on a Microsoft Excel spreadsheet) and an Application Note is available. Please order DK306/D from the Motorola Literature Distribution Center.

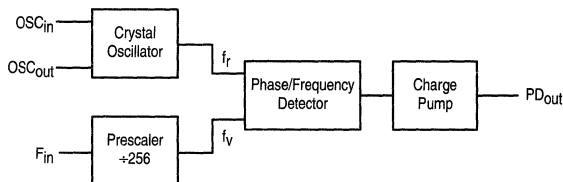
**MC12179**

**500–2800MHz  
SINGLE CHANNEL  
FREQUENCY SYNTHESIZER**

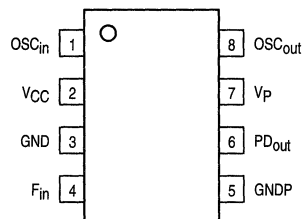


**D SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751-05

**BLOCK DIAGRAM**



**Pinout: 8-Lead SOIC (Top View)**



**MAXIMUM RATINGS\***

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pin 2	–0.5 to +6.0	VDC
V <sub>P</sub>	Power Supply Voltage, Pin 7	V <sub>CC</sub> to +6.0	VDC
T <sub>stg</sub>	Storage Temperature Range	–65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions as identified in the Electrical Characteristics table.

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**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 4.5$  to  $5.5V$ ;  $V_P = V_{CC}$  to  $5.5V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
$I_{CC}$	Supply Current for $V_{CC}$		3.1	5.6	mA	Note 1
$I_P$	Supply Current for $V_P$		0.4	1.3	mA	Note 1
$F_{IN}$	Operating Frequency $f_{INmax}$ $f_{INmin}$	2800		500	MHz	Note 2
$F_{OSC}$	Operating Frequency Crystal Mode External Oscillator $OSC_{in}$	5 2		11 11	MHz	Note 3 Note 4
$V_{IN}$	Input Sensitivity $F_{in}$	200		1000	mV <sub>P-P</sub>	Note 2
$V_{OSC}$	Input Sensitivity External Oscillator $OSC_{in}$	500		2200	mV <sub>P-P</sub>	Note 4
$I_{OH}$	Output Source Current <sup>5</sup> ( $PD_{out}$ )	-2.8	-2.2	-1.6	mA	$V_P = 4.5V$ , $V_{PDout} = V_P/2$
$I_{OL}$	Output Sink Current <sup>5</sup> ( $PD_{out}$ )	1.6	2.2	2.8	mA	$V_P = 4.5V$ , $V_{PDout} = V_P/2$
$I_{OZ}$	Output Leakage Current ( $PD_{out}$ )		0.5	15	nA	$V_P = 5.0V$ , $V_{PDout} = V_P/2$

- $V_{CC}$  and  $V_P = 5.5V$ ;  $F_{IN} = 2.56GHz$ ;  $F_{OSC} = 10MHz$  crystal;  $PD_{out}$  open.
- AC coupling,  $F_{IN}$  measured with a 1000pF capacitor.
- Assumes  $C_1$  and  $C_2$  (Figure 1) limited to  $\leq 30pF$  each including stray and parasitic capacitances.
- AC coupling to  $OSC_{in}$ .
- Refer to Figure 15 and Figure 16 for typical performance curves over temperature and power supply voltage.

**PIN NAMES**

Pin	I/O	Function	Pin No.
$OSC_{in}$	I	Oscillator Input — An external parallel-resonant, fundamental crystal is connected between $OSC_{in}$ and $OSC_{out}$ to form an internal reference oscillator (crystal mode). External capacitors $C_1$ and $C_2$ , as shown in Figure 1, are required to set the proper crystal load capacitance and oscillator frequency. For an external reference oscillator, an external signal is AC-coupled to the $OSC_{in}$ pin with a 1000pF coupling capacitor, with no connection to $OSC_{out}$ . In either mode, a resistor with a nominal value of 50k $\Omega$ MUST be placed across the $OSC_{in}$ and $OSC_{out}$ pins for proper operation.	1
$V_{CC}$	—	Positive Power Supply. Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.	2
GND	—	Ground.	3
$F_{in}$	I	Prescaler Input — The VCO signal is AC coupled into the $F_{in}$ pin.	4
GNDP	—	Ground — For charge pump circuitry.	5
$PD_{out}$	O	Single ended phase/frequency detector output (charge pump output). Three-state current sink/source output for use as a loop error signal when combined with an external low pass filter. The phase/frequency detector is characterized by a linear transfer function.	6
$V_P$	—	Positive power supply for charge pump. $V_P$ MUST be equal or greater than $V_{CC}$ . Bypass capacitors should be placed as close as possible to the pin and be connected directly to the ground plane.	7
$OSC_{out}$	O	Oscillator output, for use with an external crystal as shown in Figure 1.	8

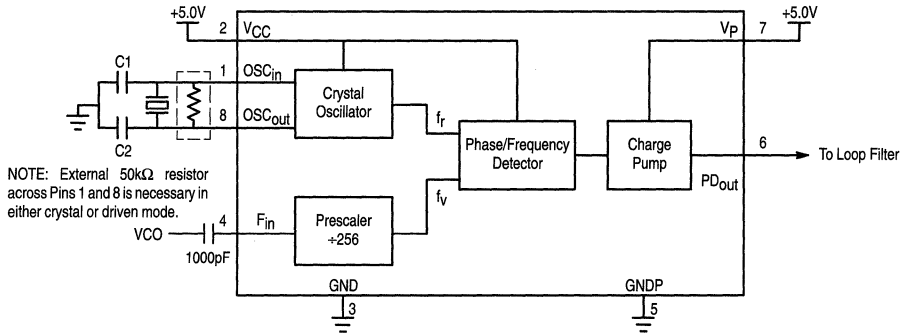


Figure 1. MC12179 Expanded Block Diagram

**PHASE CHARACTERISTICS**

The phase comparator in the MC12179 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fv) signal and the reference (fr) input. The detector can cover a range of ±2π radian of fv/fr phase difference. The operation of the charge pump output is shown in Figure 2.

**fr lags fv in phase OR fv > fr in frequency**

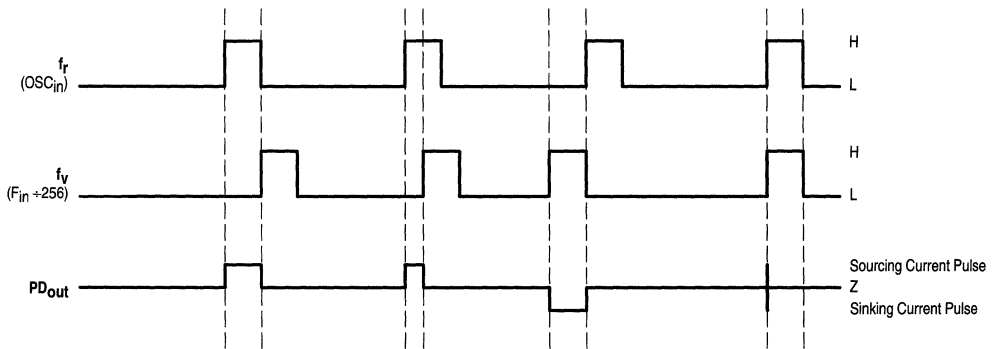
When the phase of fr lags that of fv or the frequency of fv is greater than fr, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

**fr leads fv in phase OR fv < fr in frequency**

When the phase of fr leads that of fv or the frequency of fv is less than fr, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

**fr = fv in phase and frequency**

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.



H = High voltage level; L = Low voltage level; Z = High impedance  
 NOTES: Phase difference detection range: --2π to 2π

$$K_p \text{ -- Charge Pump Gain} \approx \frac{||\text{source}|| + ||\text{sink}||}{4\pi} = \frac{|2.2| + |-2.2|}{4\pi} = \frac{1.1\text{mA}}{\pi\text{radian}}$$

Figure 2. Phase/Frequency Detector and Charge Pump Waveforms



## Applications Information

The MC12179 is intended for applications where a fixed local oscillator is required to be synthesized. The prescaler on the MC12179 operates up to 2.8GHz which makes the part ideal for many satellite receiver applications as well as applications in the 2nd ISM (Industrial, Scientific, and Medical) band which covers the frequency range of 2400MHz to 2483MHz. The part is also intended for MMDS (Multi-channel Multi-point Distribution System) block downconverter applications. Below is a typical block diagram of the complete PLL.

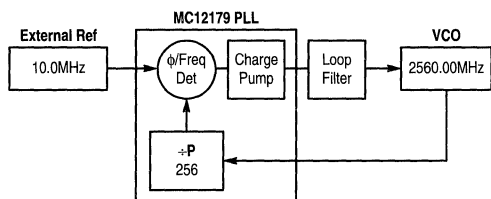


Figure 3. Typical Block Diagram of Complete PLL

As can be seen from the block diagram, with the addition of a VCO, a loop filter, and either an external oscillator or crystal, a complete PLL sub-system can be realized. Since most of the PLL function is integrated into the MC12179, the user's primary focus is on the loop filter design and the crystal reference circuit. Figure 13 and Figure 14 illustrate typical VCO spectrum and phase noise characteristics. Figure 17 and Figure 18 illustrate the typical input impedance versus frequency for the prescaler input.

### Crystal Oscillator Design

The MC12179 is used as a multiply-by-256 PLL circuit which transfers the high stability characteristic of a low frequency reference source to the high frequency VCO in the PLL loop. To facilitate this, the device contains an input circuit which can be configured as a crystal oscillator or a buffer for accepting an external signal source.

In the external reference mode, the reference source is AC-coupled into the  $OSC_{in}$  input pin. The input level signal should be between 500–2200mVp-p. When configured with an external reference, the device can operate with input frequencies down to 2MHz, thus allowing the circuit to control the VCO down to 512MHz. To optimize the phase noise of the PLL when used in this mode, the input signal amplitude should be closer to the upper specification limit. This maximizes the slew rate of the input signal as it switches against the internal voltage reference.

In the crystal mode, an external parallel-resonant fundamental mode crystal is connected between the  $OSC_{in}$  and  $OSC_{out}$  pins. This crystal must be between 5MHz and 11MHz. External capacitors, C1 and C2 as shown in Figure 1, are required to set the proper crystal load

capacitance and oscillator frequency. The values of the capacitors are dependent on the crystal chosen and the input capacitance of the device and any stray board capacitance.

In either mode, a 50k $\Omega$  resistor must be connected between the  $OSC_{in}$  and the  $OSC_{out}$  pins for proper device operation. The value of this resistor is not critical so a 47k $\Omega$  or 51k $\Omega$   $\pm$ 10% resistor is acceptable.

Since the MC12179 is realized with an all-bipolar ECL style design, the internal oscillator circuitry is different from more traditional CMOS oscillator designs which realize the crystal oscillator with a modified inverter topology. These CMOS designs typically excite the crystal with a rail-to-rail signal which may overdrive the crystal resulting in damage or unstable operation. The MC12179 design does not exhibit these phenomena because the swing out of the  $OSC_{out}$  pin is less than 600mV. This has the added advantage of minimizing EMI and switching noise which can be generated by rail-to-rail CMOS outputs. The  $OSC_{out}$  output should not be used to drive other circuitry.

The oscillator buffer in the MC12179 is a single stage, high speed, differential input/output amplifier; it may be considered to be a form of the Pierce oscillator. A simplified circuit diagram is seen in Figure 4.

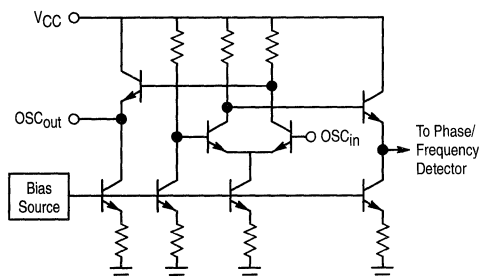


Figure 4. Simplified Crystal Oscillator/Buffer Circuit

$OSC_{in}$  drives the base of one input of an NPN transistor differential pair. The non-inverting input of the differential pair is internally biased.  $OSC_{out}$  is the inverted input signal and is buffered by an emitter follower with a 70 $\mu$ A pull-down current and has a voltage swing of about 600mVp-p. Open loop output impedance is about 425 $\Omega$ . The opposite side of the differential amplifier output is used internally to drive another buffer stage which drives the phase/frequency detector. With the 50k $\Omega$  feedback resistor in place,  $OSC_{in}$  and  $OSC_{out}$  are biased to approximately 1.1V below  $V_{CC}$ . The amplifier has a voltage gain of about 15dB and a bandwidth in excess of 150MHz. Adherence to good PCB design and layout techniques, including power supply pin decoupling, is strongly recommended.

A typical crystal oscillator application is shown in Figure 1. The crystal and the feedback resistor are connected directly between  $OSC_{in}$  and  $OSC_{out}$ , while the loading capacitors, C1

and C<sub>2</sub>, are connected between OSC<sub>in</sub> and ground, and OSC<sub>out</sub> and ground respectively. It is important to understand that as far as the crystal is concerned, the two loading capacitors are in series (albeit through ground). So when the crystal specification defines a specific loading capacitance, this refers to the total external (to the crystal) capacitance seen across its two pins.

This capacitance consists of the capacitance contributed by the amplifier (IC and packaging), layout capacitance, and the series combination of the two loading capacitors. This is illustrated in the equation below:

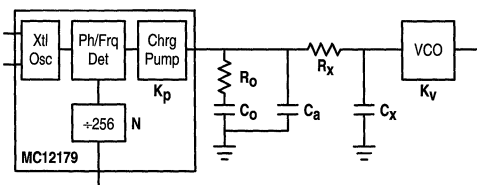
$$C_l = C_{AMP} + C_{STRAY} + \frac{C_1 \times C_2}{C_1 + C_2}$$

Provided the crystal and associated components are located immediately next to the IC, thus minimizing the stray capacitance, the combined value of C<sub>AMP</sub> and C<sub>STRAY</sub> is approximately 5pF. Note that the location of the OSC<sub>in</sub> and OSC<sub>out</sub> pins at the end of the package, facilitates placing the crystal, resistor and the C<sub>1</sub> and C<sub>2</sub> capacitors very close to the device. Usually, one of the capacitors is in parallel with an adjustable capacitor used to trim the frequency of oscillation. It is important that the total external (to the IC) capacitance seen by either OSC<sub>in</sub> or OSC<sub>out</sub>, be no greater than 30pF.

In operation, the crystal oscillator will start up with the application of power. If the crystal is in a can that is not grounded it is often possible to monitor the frequency of oscillation by connecting an oscilloscope probe to the can; this technique minimizes any disturbance to the circuit. If a malfunction is indicated, a high impedance, low capacitance, FET probe may be connected to either OSC<sub>in</sub> or OSC<sub>out</sub>. Signals typically seen at those points will be very nearly sinusoidal with amplitudes of roughly 300–600mVp–p. Some distortion is inevitable and has little bearing on the accuracy of the signal going to the phase detector.

**Loop Filter Design**

Because the device is designed for a non–frequency agile synthesizer (i.e., how fast it tunes is not critical) the loop filter design is very straight forward. The current output of the charge pump allows the loop filter to be realized without the need of any active components. The preferred topology for the filter is illustrated below in Figure 5.



**Figure 5. Loop Filter**

The R<sub>0</sub>/C<sub>0</sub> components realize the primary loop filter. C<sub>a</sub> is added to the loop filter to provide for reference sideband suppression. If additional suppression is needed, the R<sub>x</sub>/C<sub>x</sub>

realizes an additional filter. In most applications, this will not be necessary. If all components are used, this results in a 4th order PLL, which makes analysis difficult. To simplify this, the loop design will be treated as a 2nd order loop (R<sub>0</sub>/C<sub>0</sub>) and additional guidelines are provided to minimize the influence of the other components. If more rigorous analysis is needed, mathematical/system simulation tools can be used.

Component	Guideline
C <sub>a</sub>	<0.1 × C <sub>0</sub>
R <sub>x</sub>	>10 × R <sub>0</sub>
C <sub>x</sub>	<0.1 × C <sub>0</sub>

The focus of the design effort is to determine what the loop’s natural frequency, ω<sub>0</sub>, should be. This is determined by R<sub>0</sub>, C<sub>0</sub>, K<sub>p</sub>, K<sub>v</sub>, and N. Because K<sub>p</sub>, K<sub>v</sub>, and N are given, it is only necessary to calculate values for R<sub>0</sub> and C<sub>0</sub>. There are 3 considerations in selecting the loop bandwidth:

- 1) Maximum loop bandwidth for minimum tuning speed
- 2) Optimum loop bandwidth for best phase noise performance
- 3) Minimum loop bandwidth for greatest reference sideband suppression

Usually a compromise is struck between these 3 cases, however, for the fixed frequency application, minimizing the tuning speed is not a critical parameter.

To specify the loop bandwidth for optimal phase noise performance, an understanding of the sources of phase noise in the system and the effect of the loop filter on them is required. There are 3 major sources of phase noise in the phase–locked loop – the crystal reference, the VCO, and the loop contribution. The loop filter acts as a low–pass filter to the crystal reference and the loop contribution equal to the total divide–by–N ratio. This is mathematically described in Figure 10. The loop filter acts as a high–pass filter to the VCO with an in–band gain equal to unity. This is described in Figure 11. The loop contribution includes the PLL IC, as well as noise in the system; supply noise, switching noise, etc. For this example, a loop contribution of 15dB has been selected, which corresponds to data in Figure 14.

The crystal reference and the VCO are characterized as high–order 1/f noise sources. Graphical analysis is used to determine the optimum loop bandwidth. It is necessary to have noise plots from the manufacturer. This method provides a straightforward approximation suitable for quickly estimating the optimal bandwidth. The loop contribution is characterized as white–noise or low–order 1/f noise given in the form of a noise factor which combines all the noise effects into a single value. The phase noise of the Crystal Reference is increased by the noise factor of the PLL IC and related circuitry. It is further increased by the total divide–by–N ratio of the loop. This is illustrated in Figure 6.

The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. In the example of Figure 6, the optimum bandwidth is approximately 15KHz.

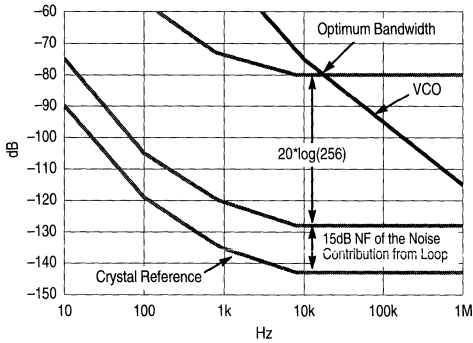


Figure 6. Graphical Analysis of Optimum Bandwidth

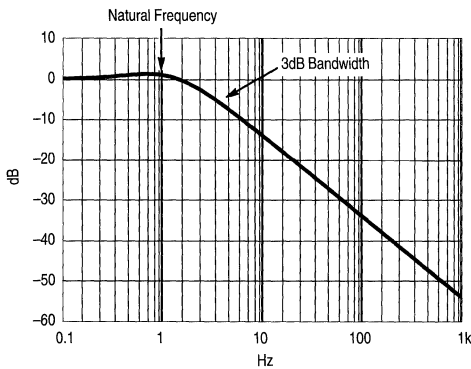


Figure 7. Closed Loop Frequency Response for  $\zeta = 1$

To simplify analysis further a damping factor of 1 will be selected. The normalized closed loop response is illustrated in Figure 7 where the loop bandwidth is 2.5 times the loop natural frequency (the loop natural frequency is the frequency at which the loop would oscillate if it were unstable). Therefore the optimum loop bandwidth is

$$\text{Let: } \frac{NC_0}{K_p K_v} = \frac{1}{\omega_0^2}, \quad R_0 C_0 = \frac{2\zeta}{\omega_0}$$

$$\text{Let: } C_a = aC_0, \quad C_x = bC_0, \quad A = 1 + a, \quad \text{and } B = 1 + a + b$$

$$\text{Let: } R_0 C_0 = \frac{1}{\omega_3}, \quad R_x C_x = \frac{1}{\omega_4}, \quad R_0(C_a + C_x) = \frac{1}{\omega_5}$$

$$\text{Let: } K_3 \omega_3 = \omega_0, \quad K_4 \omega_4 = \omega_0, \quad K_5 \omega_5 = \omega_0$$

Figure 9. Loop Parameter Relations

15kHz/2.5 or 6kHz (37.7krads) with a damping coefficient,  $\zeta = 1$ .  $T(s)$  is the transfer function of the loop filter.

$$T(s) = \frac{R_0 C_0 s + 1}{\left(\frac{NC_0}{K_p K_v}\right) s^2 + R_0 C_0 s + 1} = \frac{\left(\frac{2\zeta}{\omega_0}\right) s + 1}{\left(\frac{1}{\omega_0^2}\right) s^2 + \left(\frac{2\zeta}{\omega_0}\right) s + 1}$$

$$\left(\frac{NC_0}{K_p K_v}\right) = \left(\frac{1}{\omega_0^2}\right) \rightarrow \omega_0 = \sqrt{\frac{K_p K_v}{NC_0}} \rightarrow C_0 \approx \left(\frac{K_p K_v}{N \omega_0^2}\right)$$

$$R_0 C_0 = \left(\frac{2\zeta}{\omega_0}\right) \rightarrow \zeta = \left(\frac{\omega_0 R_0 C_0}{2}\right) \rightarrow R_0 = \left(\frac{2\zeta}{\omega_0 C_0}\right)$$

Figure 8. Design Equations for the 2nd Order System

In summary, follow the steps given below:

- Step 1: Plot the phase noise of crystal reference and the VCO on the same graph.
- Step 2: Increase the phase noise of the crystal reference by the noise contribution of the loop.
- Step 3: Convert the divide-by-N to dB (20log 256 – 48dB) and increase the phase noise of the crystal reference by that amount.
- Step 4: The point at which the VCO phase noise crosses the amplified phase noise of the Crystal Reference is the point of the optimum loop bandwidth. This is approximately 15kHz in Figure 6.
- Step 5: Correlate this loop bandwidth to the loop natural frequency and select components per Figure 8. In this case the 3dB bandwidth for a damping coefficient of 1 is 2.5 times the loop's natural frequency. The relationship between the 3dB loop bandwidth and the loop's "natural" frequency will vary for different values of  $\zeta$ . Making use of the equations defined above in a math tool or spreadsheet is useful. To aid in the use of such a tool the equations are summarized in Figure 9 through Figure 11.

$$T(j\omega) = N \cdot \frac{1 + j \left( 2\zeta \frac{\omega}{\omega_0} \right)}{\left( 1 + K_3 K_4 \frac{\omega^4}{\omega_0^4} - B \frac{\omega^2}{\omega_0^2} \right) + j \left( 2\zeta \frac{\omega}{\omega_0} - (AK_4 + K_5) \frac{\omega^3}{\omega_0^3} \right)}$$

Figure 10. Transfer Function for the Crystal Noise in the Frequency Plane

$$T(j\omega) = \frac{\left( K_3 K_4 \frac{\omega^4}{\omega_0^4} - B \frac{\omega^2}{\omega_0^2} \right) - j \left( (AK_4 + K_5) \frac{\omega^3}{\omega_0^3} \right)}{\left( 1 + K_3 K_4 \frac{\omega^4}{\omega_0^4} - B \frac{\omega^2}{\omega_0^2} \right) + j \left( 2\zeta \frac{\omega}{\omega_0} - (AK_4 + K_5) \frac{\omega^3}{\omega_0^3} \right)}$$

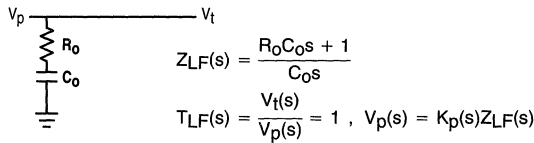
Figure 11. Transfer Function for the VCO Noise in the Frequency Plane

**Appendix: Derivation of Loop Filter Transfer Function**

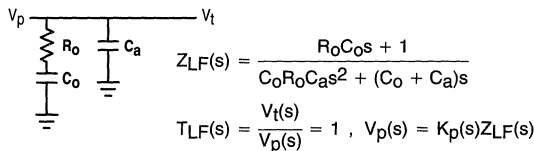
The purpose of the loop filter is to convert the current from the phase detector to a tuning voltage for the VCO. The total transfer function is derived in two steps. Step 1 is to find the voltage generated by the impedance of the loop filter. Step 2 is to find the transfer function from the input of the loop filter to its output. The “voltage” times the “transfer function” is the

overall transfer function of the loop filter. To use these equations in determining the overall transfer function of a PLL multiply the filter’s impedance by the gain constant of the phase detector then multiply that by the filter’s transfer function (which is unity in the 2nd and 3rd order cases below).

For the 2nd Order PLL:



For the 3rd Order PLL:



For the 4th Order PLL:

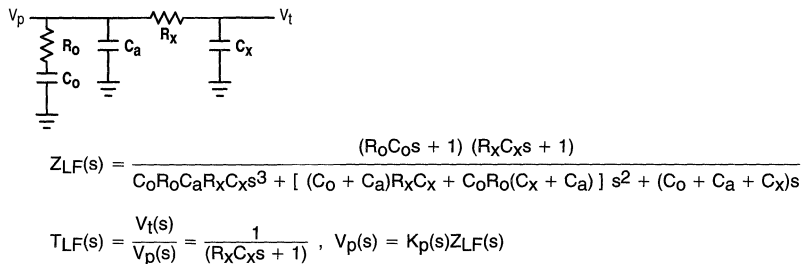


Figure 12. Overall Transfer Function of the PLL

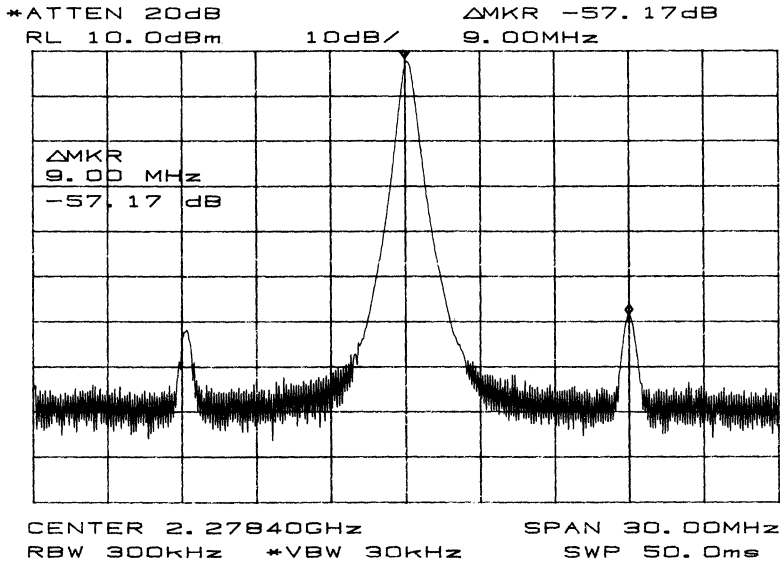


Figure 13. VCO Output Spectrum with MC12179,  $V_{CC} = 5.0V$   
(ECLIPTEK 8.9MHz Crystal and ZCOM 2500 VCO)

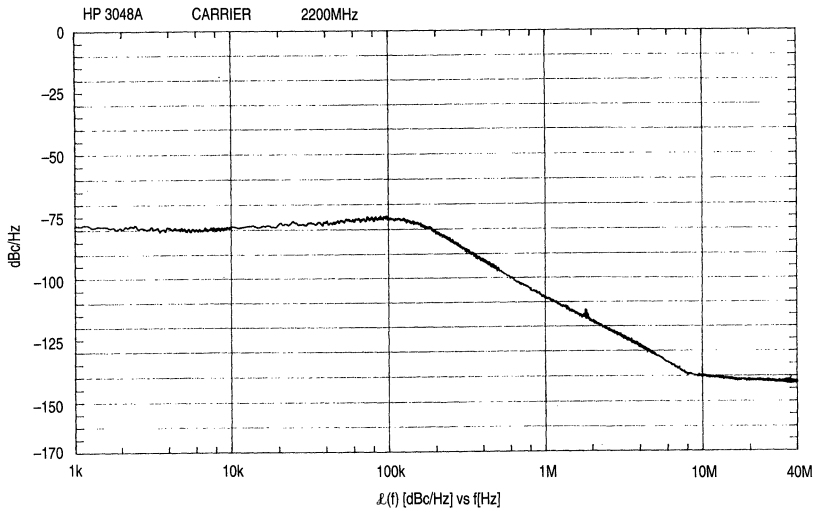
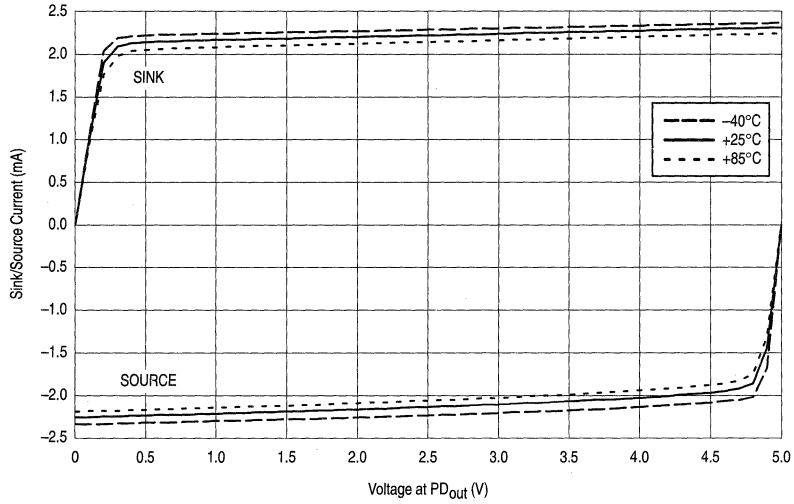
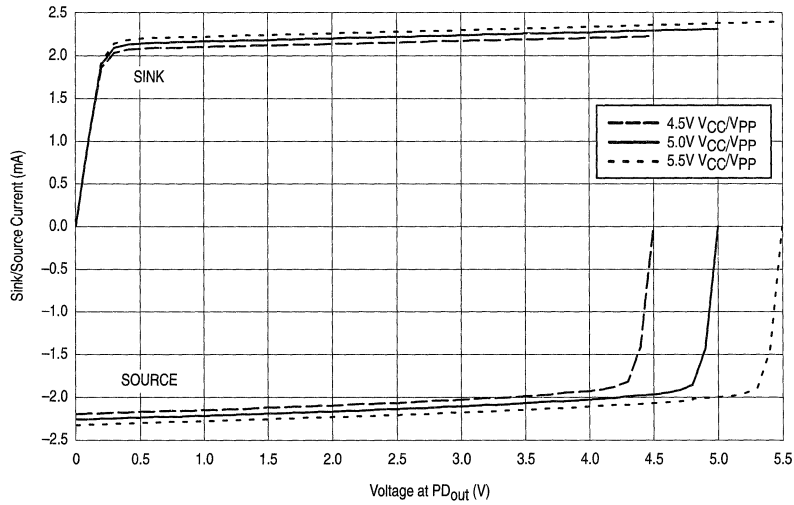


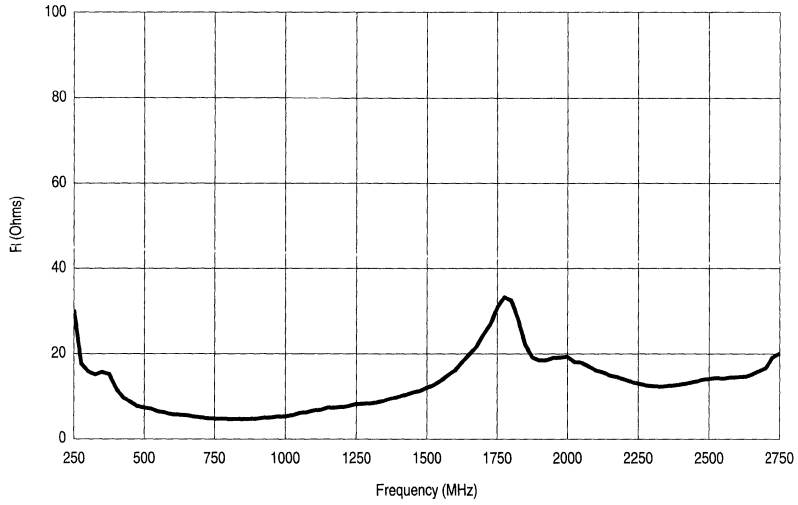
Figure 14. Typical Phase Noise Plot, 2200MHz VCO  
(With the MC12179 in a Closed Loop)



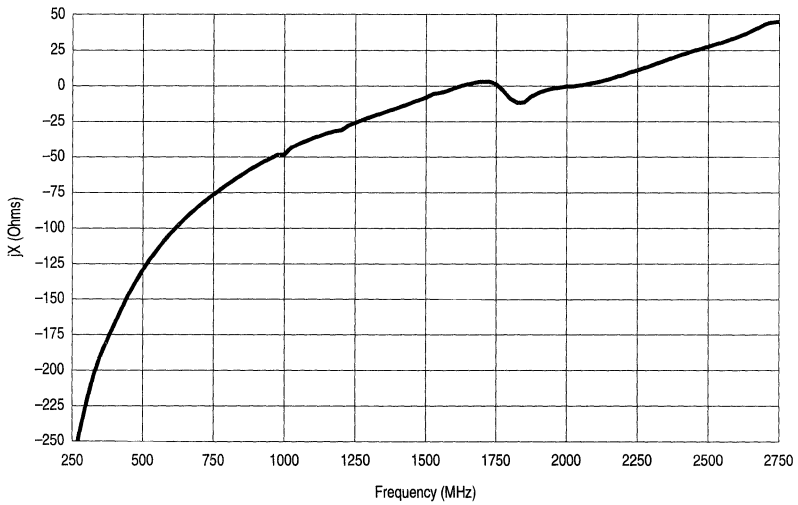
**Figure 15. Typical Charge Pump Current versus Temperature**  
( $V_{CC} = V_{PP} = 5V$ )



**Figure 16. Typical Charge Pump Current versus Voltage**  
( $T = 25^{\circ}C$ )



**Figure 17. Typical Real Input Impedance versus Input Frequency**  
(For the  $F_{IN}$  Input)



**Figure 18. Typical Imaginary Input Impedance versus Input Frequency**  
(For the  $F_{IN}$  Input)

*Product Preview*  
**Low Voltage Dual RF/IF PLL  
Frequency Synthesizer**

The MC12302 is a 1.1GHz (RF)/500MHz (IF) monolithic serial input dual phase locked loop (PLL) synthesizer. The device contains a complete RF prescaler/PLL synthesizer and an IF prescaler/PLL synthesizer. It is designed to provide the high frequency RF local oscillator control and IF oscillator control for dual conversion receivers or transceivers. The two synthesizers share a common serial programming port as well as the reference oscillator input. Each side contains separate reference counters for independent programming of the comparison frequency. The device is intended for RF personal communication applications where small size and low power are critical.

Motorola's advanced Bipolar MOSAIC V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over a 2.7 to 5.5V supply range for input frequencies up to 1.1GHz/500 MHz with a typical current drain of 9.0mA. The low power consumption makes the MC12302 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or personal communication devices. Dual modulus prescalers are integrated to provide either a 32/33 or 64/65 divide ratio for the RF synthesizer and a 8/9 or 16/17 divide ratio for the IF synthesizer.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 8.5 mA Typical for  $I_{CC}$  and 0.5mA Typical for  $I_p$
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 32/33 or 64/65 for the RF Synthesizer and 8/9 or 16/17 for the IF Synthesizer
- On-Chip Reference Frequency Buffer
- Two Programmable Reference Dividers Consisting of a Binary 14-Bit Reference Counter ( $R = 8$  to 16383)
- Two Programmable Dividers Consisting of a Binary 6-Bit (4 Bit for IF) Swallow Counter and an 11-Bit Counter
- Integrated Digital Phase/Frequency Detectors
- Balanced Charge Pump Outputs Which Can Be Disabled Individually Under Software Control
- Multi-function Test Pin for Observing RF or IF Lock Detect Output or Any One of Four Comparison Signals
- Test Pin Can Be Disabled Under Software Control to Reduce Current Drain
- Operating Temperature Range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Space Efficient Plastic Surface Mount TSSOP Package

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This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

**MC12302**

**1.1GHz/500MHz  
LOW VOLTAGE DUAL PLL  
FREQUENCY SYNTHESIZER**



**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 948E-02







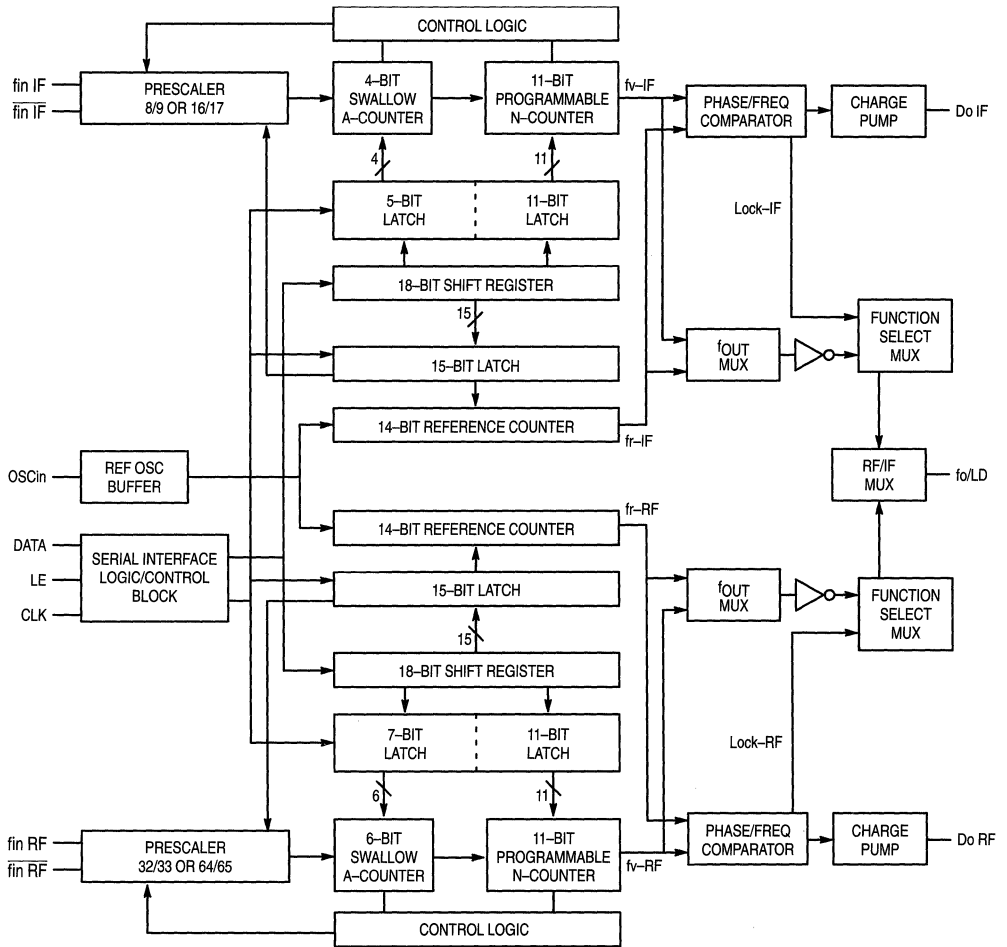


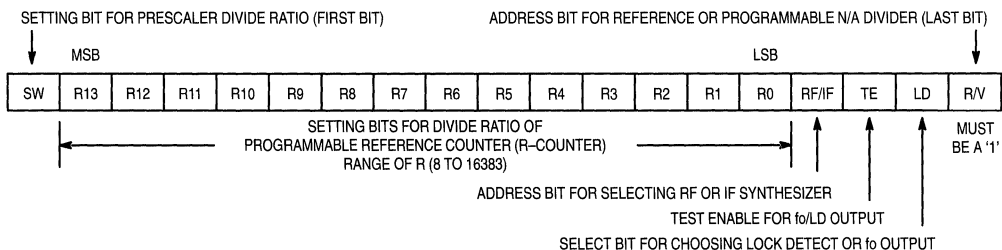
Figure 1. MC12302 Functional Block Diagram

**SERIAL PROGRAMMING INTERFACE**

A simple 3-line uni-directional serial interface is used to program the synthesizer. The interface consists of DATA, CLK (clock), and LE (load enable) inputs. While the LE input is LOW, a rising edge of the clock shifts one bit of serial data into the internal shift registers. The most significant bit (MSB) is shifted in first (SW). The last bit is a control bit which steers the data stream to either the Reference Divider (19 bits) or Programmable N/A Divider (22 bits) Latch. When the LE input pulses HIGH, the contents shifted in will be latched into the device. Only the last 19 bits (or 22-bits) serially clocked into the device are retained. Additional leading bits are ignored. This is useful in those cases where the programmer prefers to deal with bit streams which are multiples of a byte in length.

**PROGRAMMABLE REFERENCE DIVIDER**

A 19-bit serial data format is used to access the programmable reference counter and prescaler select bit. There are 3 separate fields in this data format which are illustrated below. The first field is 1-bit wide (SW) and selects one of the two modulus prescalers. A HIGH selects the lower modulus prescaler pair while LOW selects the higher modulus prescaler pair. The next field is 14-bits wide and contains the value of the reference counter divide ratio. The final field is 4-bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi-function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit, Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set high (1=R/V) to address the data stream to the Reference Divider.



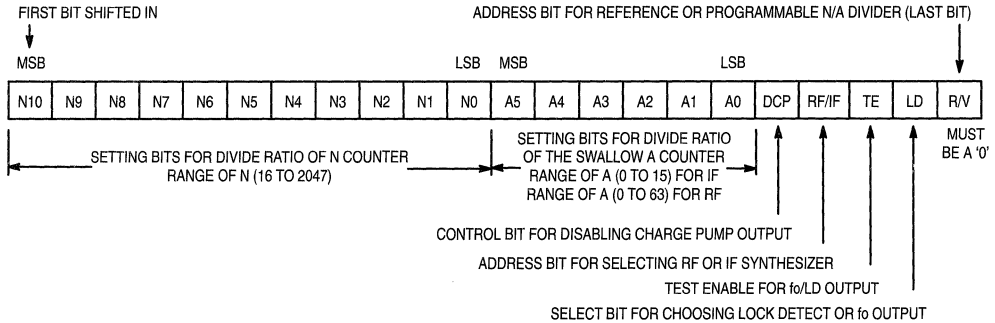
**DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER**

Divide Ratio R	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1	R 0
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PRESCALER SELECT BIT			SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT	
Synthesizer	Prescaler Divide Ratio	SW	Synthesizer	RF/IF	Status of fo/LD	TE	Signal From fo/LD	LD
RF	64/65	0	IF	0	Powered Down	0	fout	0
RF	32/33	1						
IF	16/17	0	RF	1	Active	1	Lock Detect	1
IF	8/9	1						

**PROGRAMMABLE N/A DIVIDER**

A 22-bit serial data format is used to access the N Divider, A Divider, and some test control functions. There are 4 separate fields in this data format which are illustrated below. The first field is 11-bits wide and is used to program the N-counter. The next field is 6-bits wide and is used to program the A-counter. The next field (DCP) is 1-bit wide and it is used to enable and disable the charge pump output. If the field is set (1=DCP), the addressed charge pump is placed in a high-impedance state. In normal operation, the charge pump is enabled (0=DCP). The final field is 4-bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi-function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set low (0=R/V) to address the data stream to the Programmable N/A Divider.



NOTE: When programming the A-counter for the IF loop, A4 and A5 should be set to '0'.

**DIVIDE RATIO OF PROGRAMMABLE N-COUNTER**

Divide Ratio N	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1	N 0
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

**DIVIDE RATIO OF SWALLOW A-COUNTER**

Divide Ratio A	A 5	A 4	A 3	A 2	A 1	A 0
0	0	0	0	0	0	0
1	1	0	0	0	0	0
•	•	•	•	•	•	•
63	1	1	1	1	1	1

SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT		CHARGE PUMP CONTROL BIT	
Synthesizer	RF/IF	Status of fo/LD	TE	Signal from fo/LD	LD	Do Output Status	DCP
IF	0	Powered Down	0	f <sub>OUT</sub>	0	Normal Operation	0
RF	1	Active	1	Lock Detect	1	Disabled	1

**PROGRAMMING ORDER**

There is no specific order by which the data words must be programmed for normal operation. In most applications, the RF and IF Programmable Reference Divider words are programmed first and the Programmable N/A Divider words are programmed last. The Programmable N/A Divider words are then changed as the synthesizer is tuned to different channels. It is important to note that the status of the TE and LD fields of the last word programmed determines the state of the fo/LD output.

**PROGRAMMING THE STATE OF THE fo/LD OUTPUT**

The multi-function test pin output can be used to observe any one of six internal signals: fr-RF, fr-IF, fv-RF, fv-IF, Lock-RF, and Lock-IF. In addition this output pin can be disabled to reduce current consumption of the part and minimize switching noise. All these functions are under software control. To fully configure the synthesizer, four data words must be programmed into the device to load all the latches. As previously stated, programming order is not important for normal operation. This is not the case though when the user would like to observe a test point. Under this condition, the last word loaded determines what test point will be observed. The table below illustrates which register needs to be programmed last and the state of the control bits to access each test point.

fo/LD Output	Register	R/V	RF/IF	TE	LD
fr IF	Reference Divider	1	0	1	0
fv IF	N/A Divider	0	0	1	0
Lock IF	Either	X	0	1	1
fr RF	Reference Divider	1	1	1	0
fv RF	N/A Divider	0	1	1	0
Lock RF	Either	X	1	1	1
Disabled	Either	X	X	0	X

X = Don't Care

**DIVIDE RATIO SETTING**

$$f_{vco} = [(P \cdot N) + A] \cdot f_{osc} \div R \text{ with } A \leq N \text{ (for continuous frequency steps } P \cdot N + A \geq P(P-1))$$

f<sub>vco</sub>: Output frequency of external voltage controlled oscillator (VCO)

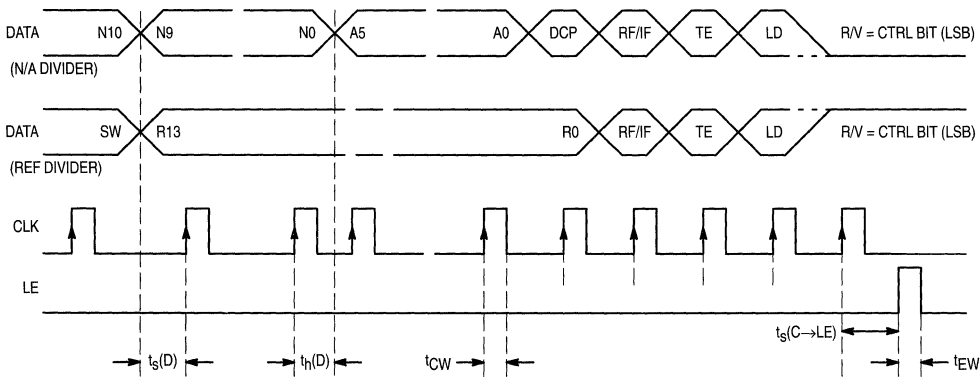
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 4-bit or 6-bit swallow counter (0 to 63, A ≤ N, for RF synthesizer; 0 to 15, A ≤ N, for IF synthesizer)

f<sub>osc</sub>: Output frequency of the external frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

P: Preset mode of dual modulus prescaler (32 or 64 for RF synthesizer; 8 or 16 for IF synthesizer)



NOTE: Data shifted into register on rising edge of CLK.

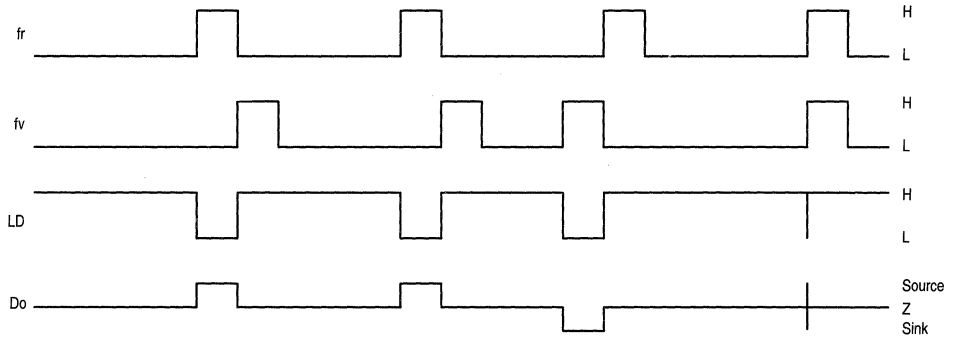
- $t_s(D)$  = Setup Time DATA to CLK
- $t_h(D)$  = Hold Time DATA to CLK
- $t_{CW}$  = CLK Pulse Width
- $t_{EW}$  = LE Pulse Width
- $t_s(C \rightarrow LE)$  = Setup Time CLK to LE
- $t_s(D) \geq 10\text{ns}$
- $t_h(D) \geq 20\text{ns}$
- $t_{CW} \geq 30\text{ns}$
- $t_{EW} \geq 20\text{ns}$
- $t_s(C \rightarrow LE) \geq 30\text{ns}$

**Figure 2. Serial Data Input Timing**

### PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12302 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fv) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

The operation of the phase comparator is shown in 3.



NOTES: Do is a current output.  
Phase difference detection range:  $-2\pi$  to  $+2\pi$   
The spike is output in order to diminish dead band.

$$\text{Internal Charge Pump Gain} \approx \frac{|I_{\text{source}}| + |I_{\text{sink}}|}{4\pi} = \frac{4\text{mA}}{4\pi}$$

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms

#### fr lags fv in phase OR fv > fr in frequency

When the phase of fr lags that of fv or the frequency of fv is greater than fr, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

#### fr leads fv in phase OR fv < fr in frequency

When the phase of fr leads that of fv or the frequency of fv is less than fr, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

#### fr = fv in phase and frequency

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

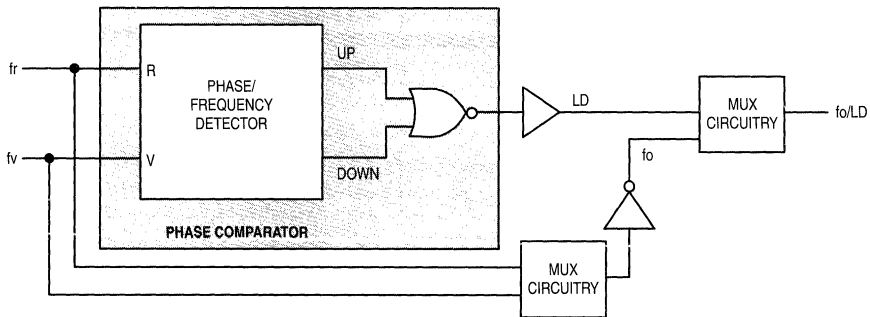


Figure 4. Detailed Phase/Frequency Comparator Block Diagram

### LOCK DETECT

When the lock detector signal (Lock-IF or Lock-RF) is selected to be routed to the fo/LD output pin, the lock detector circuit provides a LOW pulse when fr and fv are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See 9.

### fo

When selected, the output frequency pin (fo/LD) provides a LOW going pulse at the fr or fv rate. The pulse width is determined by the frequency in the respective counter. This output is for test purposes only and may not swing all the way down to ground. The scope probe capacitive load should be less than 5pF.

### OSCILLATOR INPUT

The device incorporates an on-chip reference buffer so that an external reference oscillator signal can be ac-coupled to the OSCin pin through a coupling capacitor. The magnitude of the ac-coupled signal must be between 500 and 2200 mV peak-to-peak.

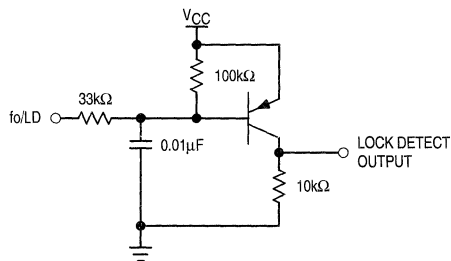


Figure 5. Typical Lock Detect Circuit

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5V$ ;  $V_P = V_{CC}$  to  $6.0V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I <sub>CC</sub>	Supply Current for V <sub>CC</sub>		8.5		mA	Note 1
			9.5		mA	Note 2
I <sub>P</sub>	Supply Current for V <sub>P</sub>		0.5		mA	Note 3
			0.7		mA	Note 4
F <sub>IN-RF</sub>	Operating Frequency f <sub>INmax</sub> f <sub>INmin</sub>	1100		100	MHz	Note 5
F <sub>IN-IF</sub>	Operating Frequency f <sub>INmax</sub> f <sub>INmin</sub>	500		40	MHz	Note 5
F <sub>OSC</sub>	Operating Frequency (OSCin)	TBD	12	40	MHz	Note 5
V <sub>IN</sub>	Input Sensitivity f <sub>IN-RF</sub> (100–500MHz) f <sub>IN-IF</sub> (40–100MHz) f <sub>IN-IF</sub>	200		1000	mV <sub>P-P</sub>	
		200 600		1000 2000		
V <sub>OSC</sub>	OSCin	500		2200	mV <sub>P-P</sub>	
V <sub>IH</sub>	Input HIGH Voltage CLK, DATA, LE	0.7V <sub>CC</sub>			V	
V <sub>IL</sub>	Input LOW Voltage CLK, DATA, LE			0.3V <sub>CC</sub>	V	
I <sub>IH</sub>	Input HIGH Current (DATA, CLK and LE)		0.1	2.0	μA	V <sub>CC</sub> = 5.5V
I <sub>IL</sub>	Input LOW Current (DATA, CLK and LE)	-2.0	-0.1		μA	V <sub>CC</sub> = 5.5V
I <sub>OSC</sub>	Input Current (OSCin)		TBD		μA	
I <sub>Source</sub>	Charge Pump Output Current		-2.0		mA	V <sub>Do</sub> = V <sub>P</sub> /2; V <sub>P</sub> = 2.7V
I <sub>Sink</sub>	Do		+2.0			V <sub>CC</sub> = 2.7V; Note 6
I <sub>Hi-Z</sub>	Output Disabled	-15		+15	nA	0.5V < V <sub>Do</sub> < V <sub>P</sub> - 0.5V
V <sub>OH</sub>	Output HIGH Voltage (fo/LD)	4.4			V	V <sub>CC</sub> = 5.0V
		2.4			V	V <sub>CC</sub> = 3.0V
V <sub>OL</sub>	Output LOW Voltage (fo/LD)			0.4	V	V <sub>CC</sub> = 5.0V
				0.4	V	V <sub>CC</sub> = 3.0V
I <sub>OH</sub>	Output HIGH Current (fo/LD)			-1.0	mA	
I <sub>OL</sub>	Output LOW Current (fo/LD)	1.0			mA	

1. V<sub>CC</sub> = 3.3V, all outputs open.

2. V<sub>CC</sub> = 5.5V, all outputs open.

3. V<sub>P</sub> = 3.3V, all outputs open.

4. V<sub>P</sub> = 6.0V, all outputs open.

5. AC coupling, F<sub>IN</sub> measured with a 1000pF capacitor.

6. Source current flows out of the pin and sink current flows into the pin, typical charge pump sink and source curves are found in Figure 9.



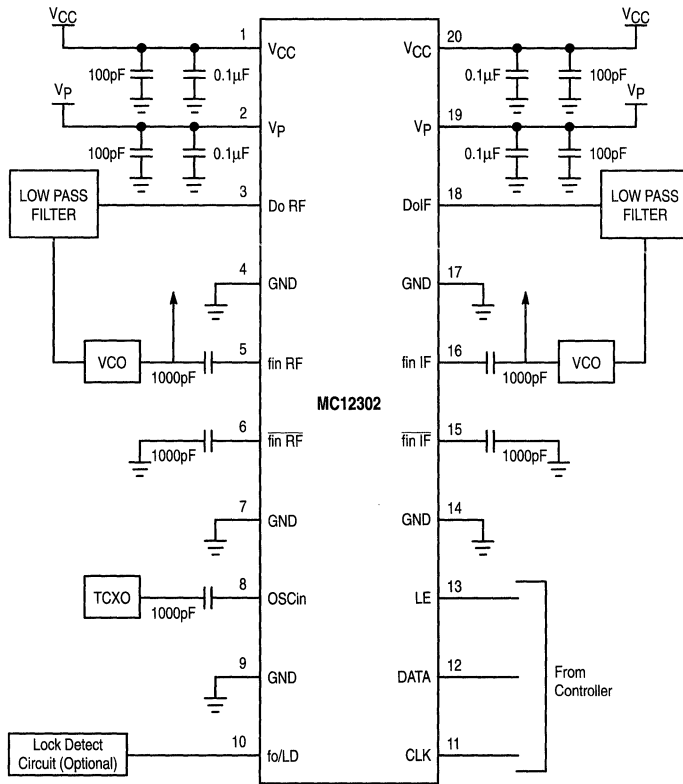


Figure 6. Typical Applications Example

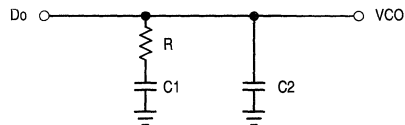


Figure 7. Typical Loop Filter

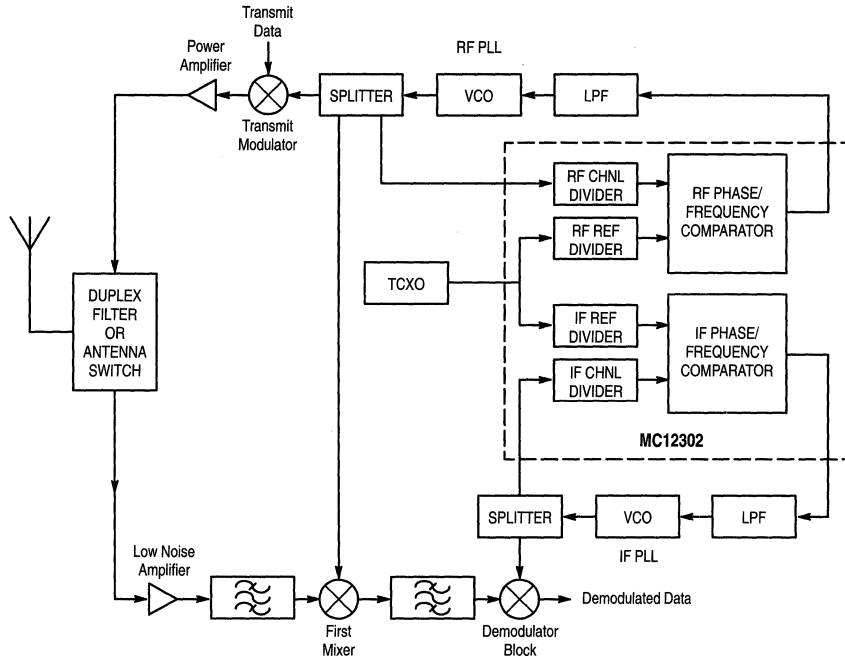


Figure 8. Typical Sub-System Block Diagram

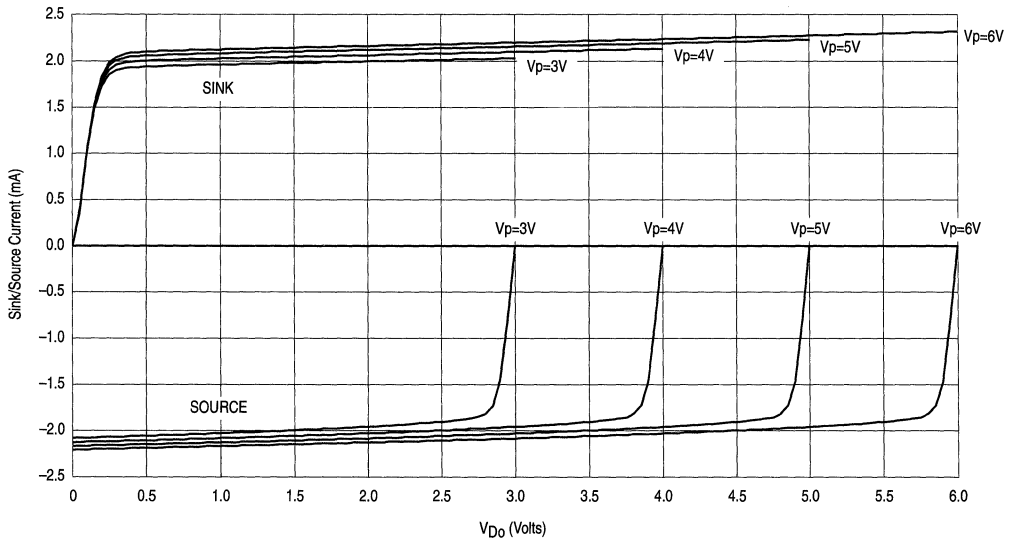


Figure 9. Typical MC12302 Charge Pump Sink and Source Current versus  $V_{DO}$   
 ( $V_{CC} = 2.7V$ ,  $T_A = 25^\circ C$ )

*Product Preview*  
**Low Voltage Dual RF/IF PLL  
Frequency Synthesizer**

The MC12306 is a 2.0GHz (RF)/500MHz (IF) monolithic serial input dual phase locked loop (PLL) synthesizer. The device contains a complete RF prescaler/PLL synthesizer and an IF prescaler/PLL synthesizer. It is designed to provide the high frequency RF local oscillator control and IF oscillator control for dual conversion receivers or transceivers. The two synthesizers share a common serial programming port as well as the reference oscillator input. Each side contains separate reference counters for independent programming of the comparison frequency. The device is intended for RF personal communication applications where small size and low power are critical.

Motorola's advanced Bipolar MOSAIC V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over a 2.7 to 5.5V supply range for input frequencies up to 2.0GHz/500 MHz with a typical current drain of 10.5mA. The low power consumption makes the MC12306 ideal for handheld battery operated applications such as cellular or cordless telephones, wireless LAN or GPS receivers. Dual modulus prescalers are integrated to provide either a 32/33 or 64/65 divide ratio for the RF synthesizer and a 8/9 or 16/17 divide ratio for the IF synthesizer.

For additional applications information, two *InterActiveApNote*<sup>TM</sup> documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 10mA Typical for I<sub>CC</sub> and 0.5mA Typical for I<sub>p</sub>
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 32/33 or 64/65 for the RF Synthesizer and 8/9 or 16/17 for the IF Synthesizer
- On-Chip Reference Frequency Buffer
- Two Programmable Reference Dividers Consisting of a Binary 14-Bit Reference Counter (R = 8 to 16383)
- Two Programmable Dividers Consisting of a Binary 6-Bit (4 Bit for IF) Swallow Counter and an 11-Bit Counter
- Integrated Digital Phase/Frequency Detectors
- Balanced Charge Pump Outputs Which Can Be Disabled Individually Under Software Control
- Multi-function Test Pin for Observing RF or IF Lock Detect Output or Any One of Four Comparison Signals
- Test Pin Can Be Disabled Under Software Control to Reduce Current Drain
- Operating Temperature Range of -40°C to +85°C
- Space Efficient Plastic Surface Mount TSSOP Package

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**MC12306**

**2.0GHz/500MHz  
LOW VOLTAGE DUAL PLL  
FREQUENCY SYNTHESIZER**



**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 948E-02

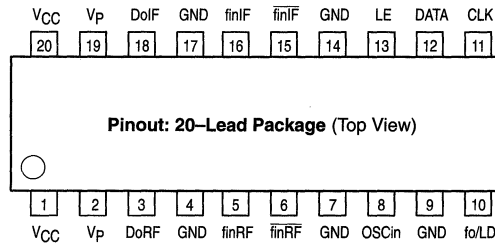


# MC12306

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pins 1 and 20	-0.5 to +6.0	VDC
V <sub>p</sub>	Power Supply Voltage, Pins 2 and 19	V <sub>CC</sub> to +6.0	VDC
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.



## PIN NAMES

Name	I/O	Function
OSCin	I	Reference oscillator input. An external oscillator source must be ac coupled in to this pin
V <sub>p</sub>	-	Power supply for charge pumps. V <sub>p</sub> should be greater than or equal to V <sub>CC</sub> . Separate pins (Pin 2 for RF/Pin 19 for IF) supply the charge pump circuitry
V <sub>CC</sub>	-	Power supply voltage input. Bypass capacitors should be placed close to this pin and connected directly to the ground plane. Separate pins (Pin 1 for RF/Pin 20 for IF) supply the internal circuitry. Both V <sub>CC</sub> voltages must be equal
Do RF	O	Internal charge pump output for RF synthesizer, can be disabled under SW control
Do IF	O	Internal charge pump output for IF synthesizer, can be disabled under SW control
GND	-	Ground
fo/LD	O	Multi-function digital output. This output is selectable as fr-RF, fr-IF, fv-RF, fv-IF, Lock-RF or Lock-IF under software control
fin RF	I	Prescaler input for the RF synthesizer. The high-frequency VCO output signal is ac-coupled into this pin
fin RF	I	Complementary prescaler input for the RF synthesizer. This pin is ac-bypassed to ground
fin IF	I	Prescaler input for the IF synthesizer. The low frequency VCO output signal is ac-coupled into this pin
fin IF	I	Complementary prescaler input for the IF synthesizer. This pin is ac-bypassed to ground
CLK	I	Clock input. Rising edge of clock shifts data into the shift registers
DATA	I	Binary serial input data
LE	I	Load Enable input. When LE pulses high, data stored in the shift registers is transferred into the appropriate latch (depending on the status of the control bits). In addition, while LE is high, the CLK input is disabled

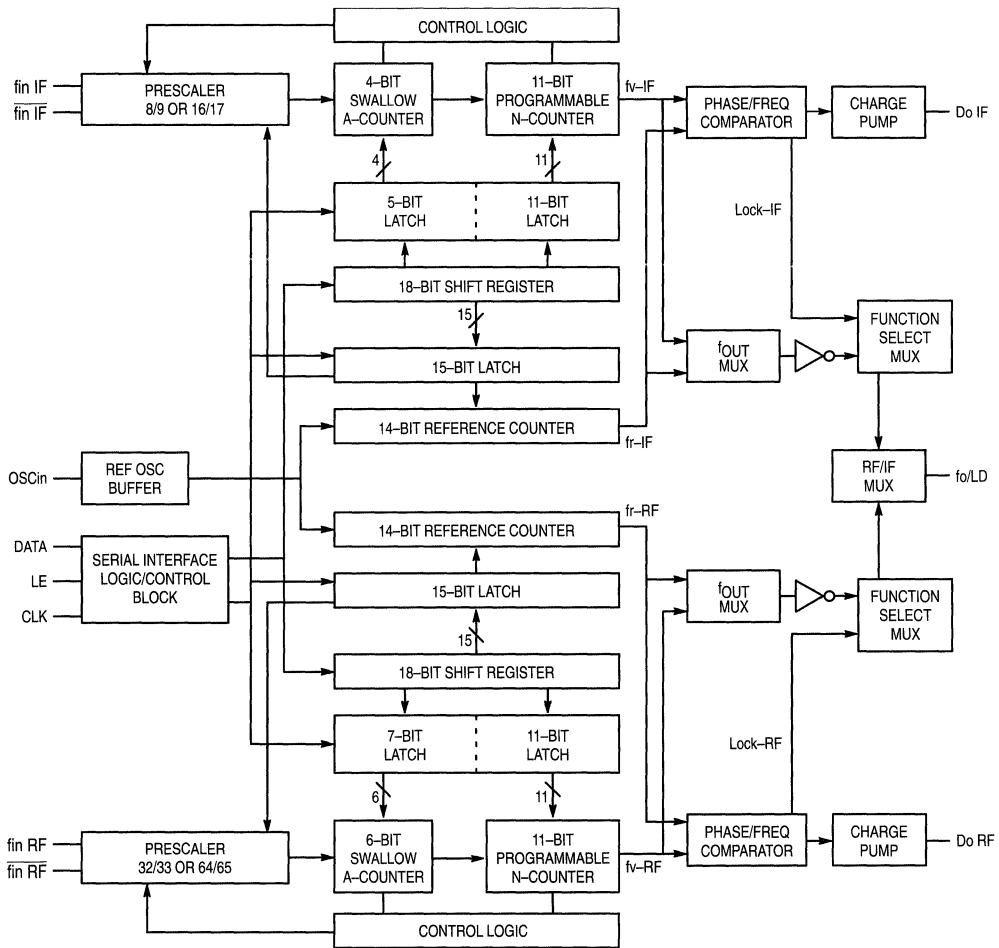


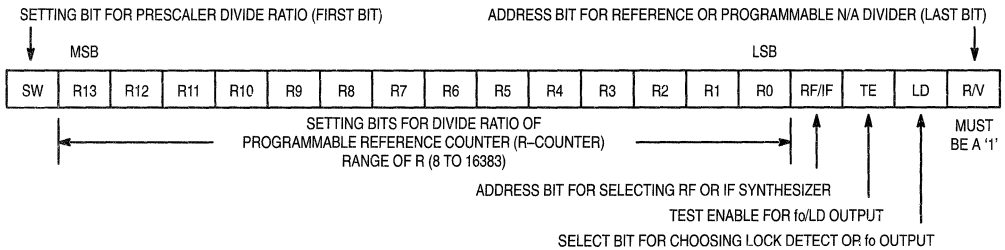
Figure 1. MC12306 Functional Block Diagram

**SERIAL PROGRAMMING INTERFACE**

A simple 3-line uni-directional serial interface is used to program the synthesizer. The interface consists of DATA, CLK (clock), and LE (load enable) inputs. While the LE input is LOW, a rising edge of the clock shifts one bit of serial data into the internal shift registers. The most significant bit (MSB) is shifted in first (SW). The last bit is a control bit which steers the data stream to either the Reference Divider (19 bits) or Programmable N/A Divider (22 bits) Latch. When the LE input pulses HIGH, the contents shifted in will be latched into the device. Only the last 19 bits (or 22-bits) serially clocked into the device are retained. Additional leading bits are ignored. This is useful in those cases where the programmer prefers to deal with bit streams which are multiples of a byte in length.

**PROGRAMMABLE REFERENCE DIVIDER**

A 19-bit serial data format is used to access the programmable reference counter and prescaler select bit. There are 3 separate fields in this data format which are illustrated below. The first field is 1-bit wide (SW) and selects one of the two modulus prescalers. A HIGH selects the lower modulus prescaler pair while LOW selects the higher modulus prescaler pair. The next field is 14-bits wide and contains the value of the reference counter divide ratio. The final field is 4-bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi-function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit, Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set high (1=R/V) to address the data stream to the Reference Divider.



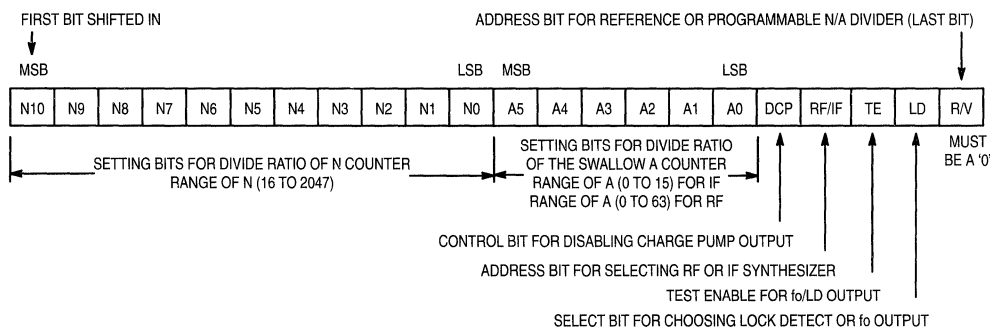
**DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER**

Divide Ratio R	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1	R 0
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PRESCALER SELECT BIT			SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT	
Synthesizer	Prescaler Divide Ratio	SW	Synthesizer	RF/IF	Status of fo/LD	TE	Signal From fo/LD	LD
RF RF	64/65 32/33	0 1	IF	0	Powered Down	0	f <sub>OUT</sub>	0
IF IF	16/17 8/9	0 1	RF	1	Active	1	Lock Detect	1

## PROGRAMMABLE N/A DIVIDER

A 22-bit serial data format is used to access the N Divider, A Divider, and some test control functions. There are 4 separate fields in this data format which are illustrated below. The first field is 11-bits wide and is used to program the N-counter. The next field is 6-bits wide and is used to program the A-counter. The next field (DCP) is 1-bit wide and it is used to enable and disable the charge pump output. If the field is set (1=DCP), the addressed charge pump is placed in a high-impedance state. In normal operation, the charge pump is enabled (0=DCP). The final field is 4-bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi-function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set low (0=R/V) to address the data stream to the Programmable N/A Divider.



NOTE: When programming the A-counter for the IF loop, A4 and A5 should be set to '0'.

### DIVIDE RATIO OF PROGRAMMABLE N-COUNTER

Divide Ratio N	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1	N 0	Divide Ratio A	A 5	A 4	A 3	A 2	A 1	A 0
16	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1	63	1	1	1	1	1	1

### DIVIDE RATIO OF SWALLOW A-COUNTER

SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT		CHARGE PUMP CONTROL BIT	
Synthesizer	RF/IF	Status of fo/LD	TE	Signal from fo/LD	LD	Do Output Status	DCP
IF	0	Powered Down	0	f <sub>OUT</sub>	0	Normal Operation	0
RF	1	Active	1	Lock Detect	1	Disabled	1

## PROGRAMMING ORDER

There is no specific order by which the data words must be programmed for normal operation. In most applications, the RF and IF Programmable Reference Divider words are programmed first and the Programmable N/A Divider words are programmed last. The Programmable N/A Divider words are then changed as the synthesizer is tuned to different channels. It is important to note that the status of the TE and LD fields of the last word programmed determines the state of the fo/LD output.

**PROGRAMMING THE STATE OF THE fo/LD OUTPUT**

The multi-function test pin output can be used to observe any one of six internal signals: fr-RF, fr-IF, fv-RF, fv-IF, Lock-RF, and Lock-IF. In addition this output pin can be disabled to reduce current consumption of the part and minimize switching noise. All these functions are under software control. To fully configure the synthesizer, four data words must be programmed into the device to load all the latches. As previously stated, programming order is not important for normal operation. This is not the case though when the user would like to observe a test point. Under this condition, the last word loaded determines what test point will be observed. The table below illustrates which register needs to be programmed last and the state of the control bits to access each test point.

fo/LD Output	Register	R/V	RF/IF	TE	LD
fr IF	Reference Divider	1	0	1	0
fv IF	N/A Divider	0	0	1	0
Lock IF	Either	X	0	1	1
fr RF	Reference Divider	1	1	1	0
fv RF	N/A Divider	0	1	1	0
Lock RF	Either	X	1	1	1
Disabled	Either	X	X	0	X

X = Don't Care

**DIVIDE RATIO SETTING**

$$f_{vco} = [(P \cdot N) + A] \cdot f_{osc} \div R \text{ with } A \leq N \text{ (for continuous frequency steps } P \cdot N + A \geq P(P-1))$$

f<sub>vco</sub>: Output frequency of external voltage controlled oscillator (VCO)

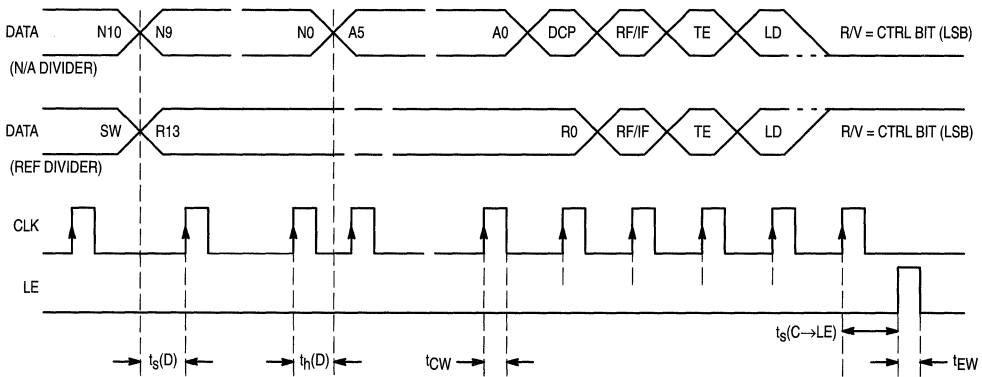
N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)

A: Preset divide ratio of binary 4-bit or 6-bit swallow counter (0 to 63, A ≤ N, for RF synthesizer; 0 to 15, A ≤ N, for IF synthesizer)

f<sub>osc</sub>: Output frequency of the external frequency oscillator

R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)

P: Preset mode of dual modulus prescaler (32 or 64 for RF synthesizer; 8 or 16 for IF synthesizer)



NOTE: Data shifted into register on rising edge of CLK.

- ts(D) = Setup Time DATA to CLK
- th(D) = Hold Time DATA to CLK
- tcw = CLK Pulse Width
- tEW = LE Pulse Width
- ts(C->LE) = Setup Time CLK to LE
- ts(D) ≥ 10ns
- th(D) ≥ 20ns
- tcw ≥ 30ns
- tEW ≥ 20ns
- ts(C->LE) ≥ 30ns

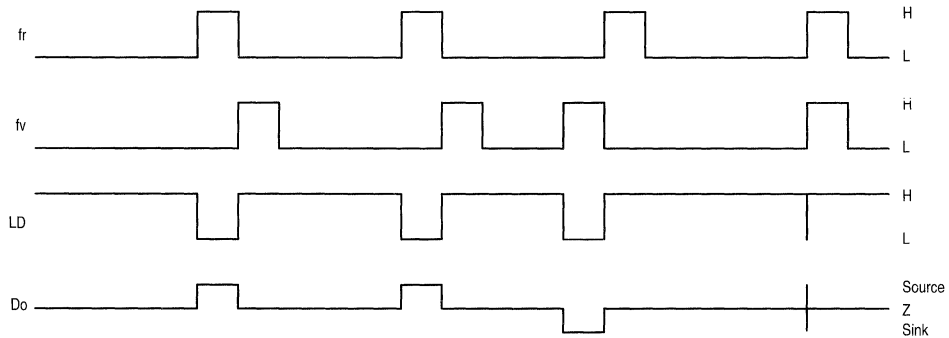
**Figure 2. Serial Data Input Timing**



### PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12306 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fv) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

The operation of the phase comparator is shown in 3.



NOTES: Do is a current output.  
Phase difference detection range:  $-2\pi$  to  $+2\pi$   
The spike is output in order to diminish dead band.

$$\text{Internal Charge Pump Gain} \approx \frac{|I_{\text{source}}| + |I_{\text{sink}}|}{4\pi} = \frac{4\text{mA}}{4\pi}$$

Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms

#### fr lags fv in phase OR fv > fr in frequency

When the phase of fr lags that of fv or the frequency of fv is greater than fr, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

#### fr leads fv in phase OR fv < fr in frequency

When the phase of fr leads that of fv or the frequency of fv is less than fr, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

#### fr = fv in phase and frequency

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

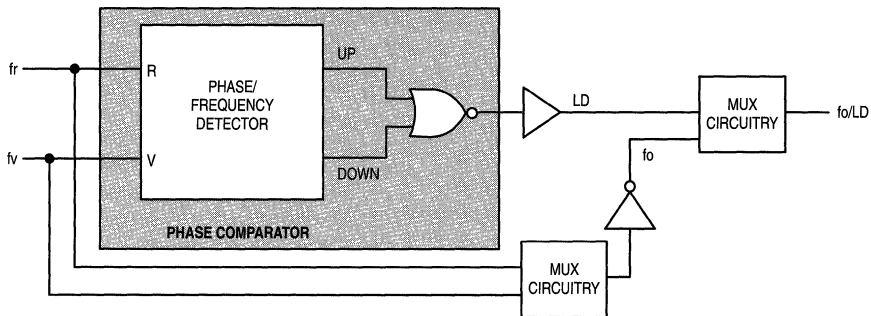


Figure 4. Detailed Phase/Frequency Comparator Block Diagram

**LOCK DETECT**

When the lock detector signal (Lock-IF or Lock-RF) is selected to be routed to the fo/LD output pin, the lock detector circuit provides a LOW pulse when fr and fv are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See 9.

**fo**

When selected, the output frequency pin (fo/LD) provides a LOW going pulse at the fr or fv rate. The pulse width is determined by the frequency in the respective counter. This output is for test purposes only and may not swing all the way down to ground. The scope probe capacitive load should be less than 5pF.

**OSCILLATOR INPUT**

The device incorporates an on-chip reference buffer so that an external reference oscillator signal can be ac-coupled to the OSCin pin through a coupling capacitor. The magnitude of the ac-coupled signal must be between 500 and 2200 mV peak-to-peak.

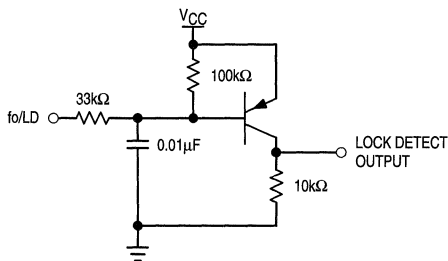


Figure 5. Typical Lock Detect Circuit

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5V$ ;  $V_P = V_{CC}$  to  $6.0V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit	Condition
I <sub>CC</sub>	Supply Current for V <sub>CC</sub>		10.0		mA	Note 1
			11.0		mA	Note 2
I <sub>P</sub>	Supply Current for V <sub>P</sub>		0.5		mA	Note 3
			0.7		mA	Note 4
F <sub>IN-RF</sub>	Operating Frequency f <sub>INmax</sub> f <sub>INmin</sub>	2000		500	MHz	Note 5
F <sub>IN-IF</sub>	Operating Frequency f <sub>INmax</sub> f <sub>INmin</sub>	500		40	MHz	Note 5
F <sub>OSC</sub>	Operating Frequency (OSCin)	TBD	12	40	MHz	Note 5
V <sub>IN</sub>	Input Sensitivity f <sub>IN-RF</sub> (100–500MHz) f <sub>IN-IF</sub> (40–100MHz) f <sub>IN-IF</sub>	200		1000	mV <sub>P-P</sub>	
		200 600		1000 2000		
V <sub>OSC</sub>	OSCin	500		2200	mV <sub>P-P</sub>	
V <sub>IH</sub>	Input HIGH Voltage CLK, DATA, LE	0.7V <sub>CC</sub>			V	
V <sub>IL</sub>	Input LOW Voltage CLK, DATA, LE			0.3V <sub>CC</sub>	V	
I <sub>IH</sub>	Input HIGH Current (DATA, CLK and LE)		0.1	2.0	μA	V <sub>CC</sub> = 5.5V
I <sub>IL</sub>	Input LOW Current (DATA, CLK and LE)	-2.0	-0.1		μA	V <sub>CC</sub> = 5.5V
I <sub>OSC</sub>	Input Current (OSCin)		TBD		μA	
I <sub>Source</sub>	Charge Pump Output Current Do		-2.0		mA	V <sub>Do</sub> = V <sub>P</sub> /2; V <sub>P</sub> = 2.7V V <sub>CC</sub> = 2.7V; Note 6
I <sub>Sink</sub>			+2.0			
I <sub>Hi-Z</sub>	Output Disabled	-15		+15	nA	0.5V < V <sub>Do</sub> < V <sub>P</sub> - 0.5V
V <sub>OH</sub>	Output HIGH Voltage (fo/LD)	4.4			V	V <sub>CC</sub> = 5.0V
		2.4			V	V <sub>CC</sub> = 3.0V
V <sub>OL</sub>	Output LOW Voltage (fo/LD)			0.4	V	V <sub>CC</sub> = 5.0V
				0.4	V	V <sub>CC</sub> = 3.0V
I <sub>OH</sub>	Output HIGH Current (fo/LD)			-1.0	mA	
I <sub>OL</sub>	Output LOW Current (fo/LD)	1.0			mA	

1. V<sub>CC</sub> = 3.3V, all outputs open.

2. V<sub>CC</sub> = 5.5V, all outputs open.

3. V<sub>P</sub> = 3.3V, all outputs open.

4. V<sub>P</sub> = 6.0V, all outputs open.

5. AC coupling, F<sub>IN</sub> measured with a 1000pF capacitor.

6. Source current flows out of the pin and sink current flows into the pin, typical charge pump sink and source curves are found in Figure 9.

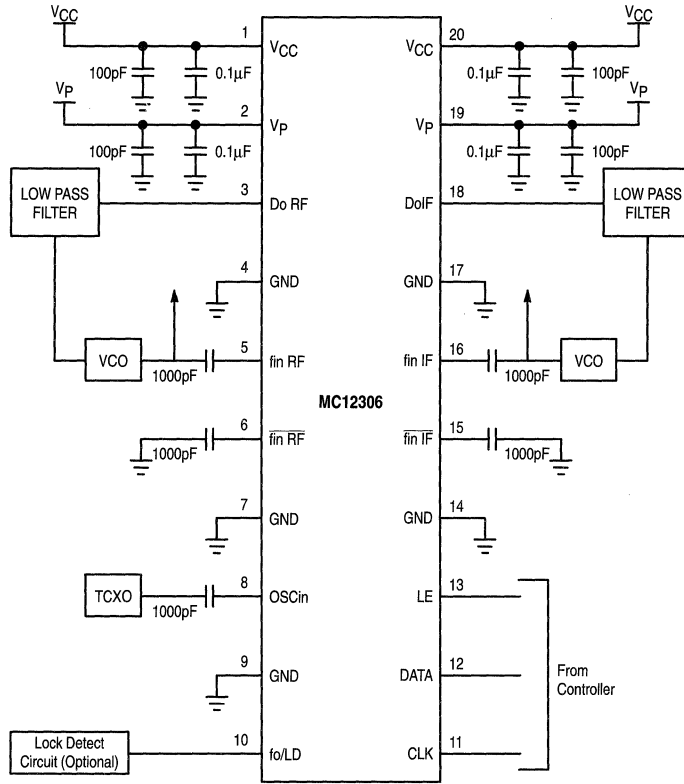


Figure 6. Typical Applications Example

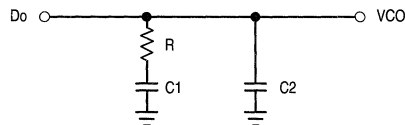


Figure 7. Typical Loop Filter

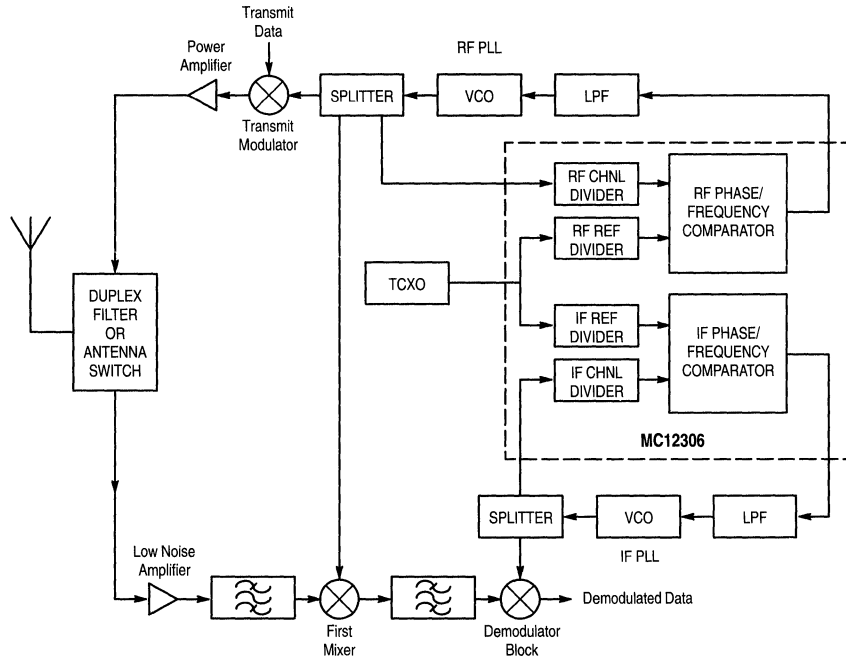


Figure 8. Typical Sub-System Block Diagram

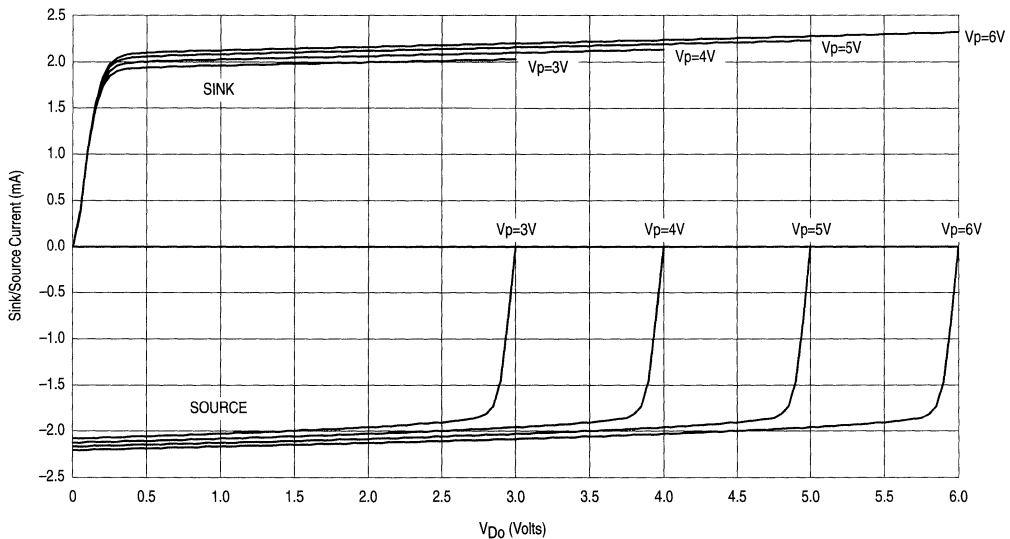


Figure 9. Typical MC12306 Charge Pump Sink and Source Current versus  $V_{DO}$   
 ( $V_{CC} = 2.7V$ ,  $T_A = 25^\circ C$ )

*Product Preview*

**Low Voltage Dual RF/IF PLL  
Frequency Synthesizer**

The MC12310 is a 2.5GHz (RF)/500MHz (IF) monolithic serial input dual phase locked loop (PLL) synthesizer. The device contains a complete RF prescaler/PLL synthesizer and an IF prescaler/PLL synthesizer. It is designed to provide the high frequency RF local oscillator control and IF oscillator control for dual conversion receivers or transceivers. The two synthesizers share a common serial programming port as well as the reference oscillator input. Each side contains separate reference counters for independent programming of the comparison frequency. The device is intended for RF personal communication applications where small size and low power are critical.

Motorola's advanced Bipolar MOSAIC V technology is utilized for low power operation at a minimum supply voltage of 2.7V. The device is designed for operation over a 2.7 to 5.5V supply range for input frequencies up to 2.5GHz/500 MHz with a typical current drain of 12.0mA. The low power consumption makes the MC12310 ideal for handheld battery operated applications such as cordless telephones or wireless LAN cards. Dual modulus prescalers are integrated to provide either a 32/33 or 64/65 divide ratio for the RF synthesizer and a 8/9 or 16/17 divide ratio for the IF synthesizer.

For additional applications information, two *InterActiveApNote*™ documents containing software (based on a Microsoft Excel spreadsheet) and an Application Note are available. Please order DK305/D and DK306/D from the Motorola Literature Distribution Center.

- Low Power Supply Current of 11.5mA Typical for I<sub>CC</sub> and 0.5mA Typical for I<sub>p</sub>
- Supply Voltage of 2.7 to 5.5V
- Dual Modulus Prescaler With Selectable Divide Ratios of 32/33 or 64/65 for the RF Synthesizer and 8/9 or 16/17 for the IF Synthesizer
- On-Chip Reference Frequency Buffer
- Two Programmable Reference Dividers Consisting of a Binary 14-Bit Reference Counter (R = 8 to 16383)
- Two Programmable Dividers Consisting of a Binary 6-Bit (4 Bit for IF) Swallow Counter and an 11-Bit Counter
- Integrated Digital Phase/Frequency Detectors
- Balanced Charge Pump Outputs Which Can Be Disabled Individually Under Software Control
- Multi-function Test Pin for Observing RF or IF Lock Detect Output or Any One of Four Comparison Signals
- Test Pin Can Be Disabled Under Software Control to Reduce Current Drain
- Operating Temperature Range of -40°C to +85°C
- Space Efficient Plastic Surface Mount TSSOP Package

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**MC12310**

**2.5GHz/500MHz  
LOW VOLTAGE DUAL PLL  
FREQUENCY SYNTHESIZER**



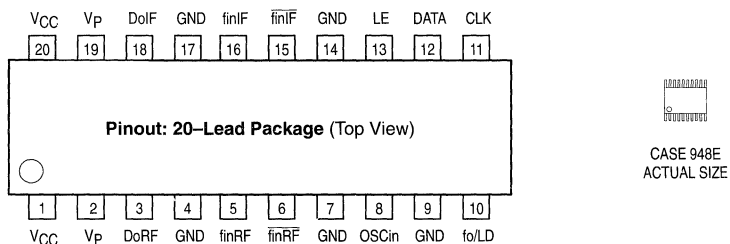
**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 948E-02



## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply Voltage, Pins 1 and 20	-0.5 to +6.0	VDC
V <sub>p</sub>	Power Supply Voltage, Pins 2 and 19	V <sub>CC</sub> to +6.0	VDC
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C

\* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.



## PIN NAMES

Name	I/O	Function
OSCin	I	Reference oscillator input. An external oscillator source must be ac coupled in to this pin
V <sub>p</sub>	-	Power supply for charge pumps. V <sub>p</sub> should be greater than or equal to V <sub>CC</sub> . Separate pins (Pin 2 for RF/Pin 19 for IF) supply the charge pump circuitry
V <sub>CC</sub>	-	Power supply voltage input. Bypass capacitors should be placed close to this pin and connected directly to the ground plane. Separate pins (Pin 1 for RF/Pin 20 for IF) supply the internal circuitry. Both V <sub>CC</sub> voltages must be equal
Do RF	O	Internal charge pump output for RF synthesizer, can be disabled under SW control
Do IF	O	Internal charge pump output for IF synthesizer, can be disabled under SW control
GND	-	Ground
fo/LD	O	Multi-function digital output. This output is selectable as fr-RF, fr-IF, fv-RF, fv-IF, Lock-RF or Lock-IF under software control
fin RF	I	Prescaler input for the RF synthesizer. The high-frequency VCO output signal is ac-coupled into this pin
fin RF	I	Complementary prescaler input for the RF synthesizer. This pin is ac-bypassed to ground
fin IF	I	Prescaler input for the IF synthesizer. The low frequency VCO output signal is ac-coupled into this pin
fin IF	I	Complementary prescaler input for the IF synthesizer. This pin is ac-bypassed to ground
CLK	I	Clock input. Rising edge of clock shifts data into the shift registers
DATA	I	Binary serial input data
LE	I	Load Enable input. When LE pulses high, data stored in the shift registers is transferred into the appropriate latch (depending on the status of the control bits). In addition, while LE is high, the CLK input is disabled

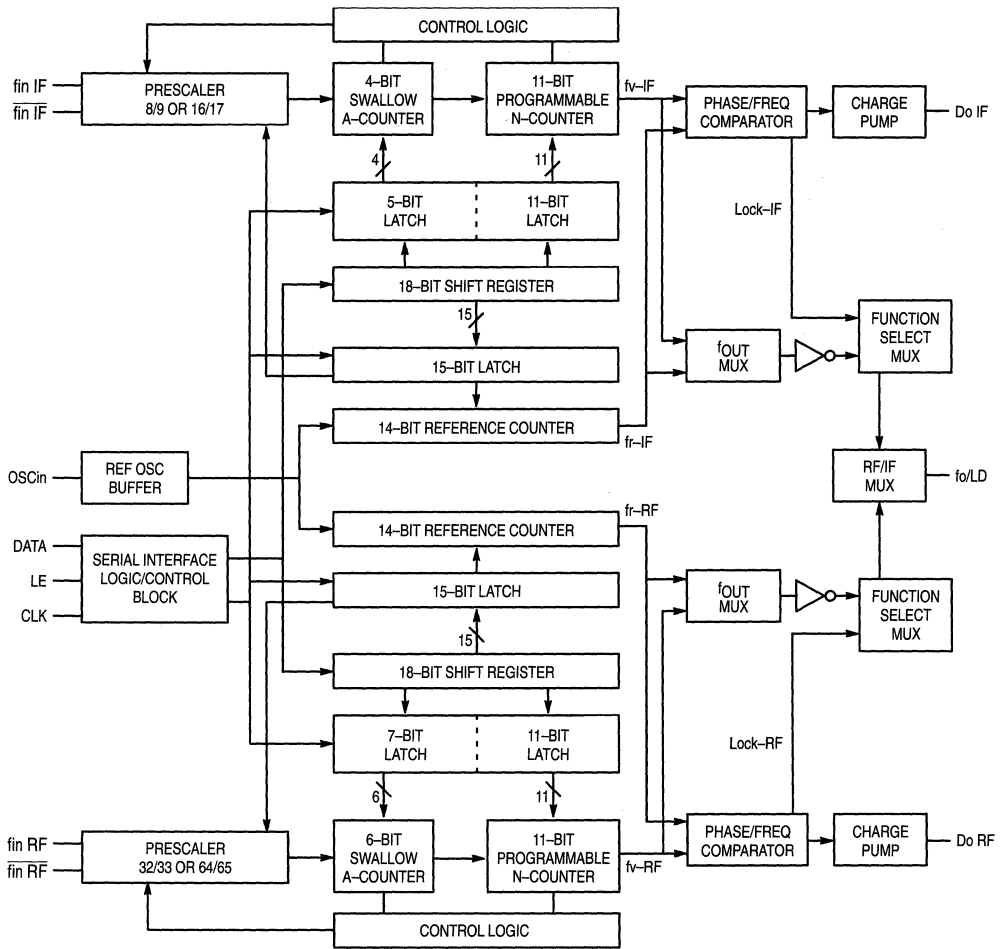


Figure 1. MC12310 Functional Block Diagram

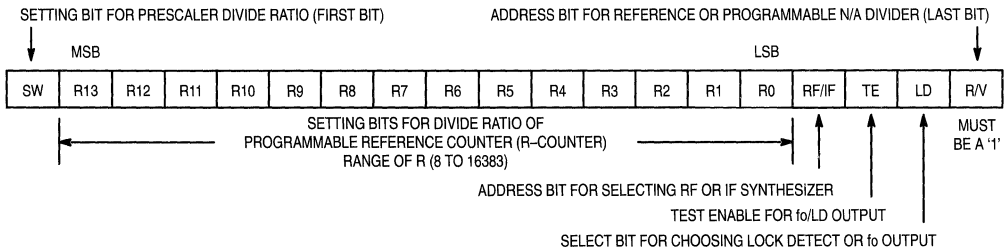


**SERIAL PROGRAMMING INTERFACE**

A simple 3–line uni–directional serial interface is used to program the synthesizer. The interface consists of DATA , CLK (clock), and LE (load enable) inputs. While the LE input is LOW, a rising edge of the clock shifts one bit of serial data into the internal shift registers. The most significant bit (MSB) is shifted in first (SW). The last bit is a control bit which steers the data stream to either the Reference Divider (19 bits) or Programmable N/A Divider (22 bits) Latch. When the LE input pulses HIGH, the contents shifted in will be latched into the device. Only the last 19 bits (or 22–bits) serially clocked into the device are retained. Additional leading bits are ignored. This is useful in those cases where the programmer prefers to deal with bit streams which are multiples of a byte in length.

**PROGRAMMABLE REFERENCE DIVIDER**

A 19–bit serial data format is used to access the programmable reference counter and prescaler select bit. There are 3 separate fields in this data format which are illustrated below. The first field is 1–bit wide (SW) and selects one of the two modulus prescalers. A HIGH selects the lower modulus prescaler pair while LOW selects the higher modulus prescaler pair. The next field is 14–bits wide and contains the value of the reference counter divide ratio. The final field is 4–bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi–function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit, Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set high (1=R/V) to address the data stream to the Reference Divider.



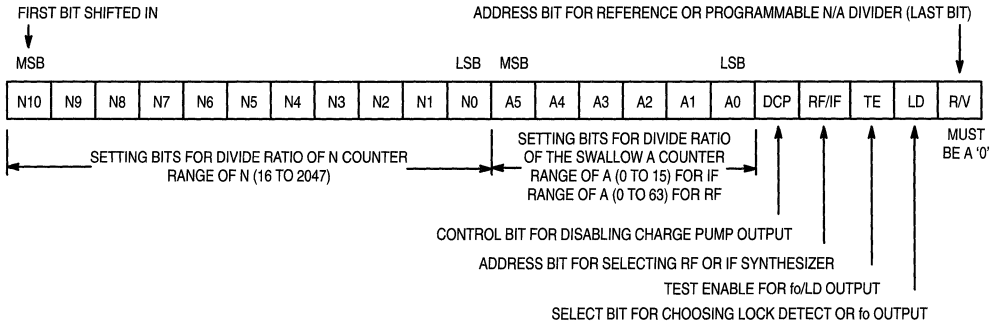
**DIVIDE RATIO OF PROGRAMMABLE REFERENCE (R) COUNTER**

Divide Ratio R	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1	R 0
8	0	0	0	0	0	0	0	0	0	0	1	0	0	0
9	0	0	0	0	0	0	0	0	0	0	1	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

PRESCALER SELECT BIT			SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT	
Synthesizer	Prescaler Divide Ratio	SW	Synthesizer	RF/IF	Status of fo/LD	TE	Signal From fo/LD	LD
RF	64/65	0	IF	0	Powered Down	0	fOUT	0
RF	32/33	1						
IF	16/17	0	RF	1	Active	1	Lock Detect	1
IF	8/9	1						

**PROGRAMMABLE N/A DIVIDER**

A 22-bit serial data format is used to access the N Divider, A Divider, and some test control functions. There are 4 separate fields in this data format which are illustrated below. The first field is 11-bits wide and is used to program the N-counter. The next field is 6-bits wide and is used to program the A-counter. The next field (DCP) is 1-bit wide and it is used to enable and disable the charge pump output. If the field is set (1=DCP), the addressed charge pump is placed in a high-impedance state. In normal operation, the charge pump is enabled (0=DCP). The final field is 4-bits wide and is used for addressing and control. The first bit in this field is RF/IF, which selects whether the data is going to be latched into the RF section (1=RF) or the IF section (0=IF). The next bit, Test Enable (TE) controls the multi-function fo/LD output (1=Active). When this bit is disabled (0=TE), the output circuitry is shut off to conserve power. The next bit Lock Detect (LD) controls whether the lock detector signal (1=Lock) or the fout (0=fout) is routed to the fo/LD output. The final bit is a control bit R/V which must be set low (0=R/V) to address the data stream to the Programmable N/A Divider.



NOTE: When programming the A-counter for the IF loop, A4 and A5 should be set to '0'.

**DIVIDE RATIO OF PROGRAMMABLE N-COUNTER**

Divide Ratio N	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1	N 0
16	0	0	0	0	0	0	1	0	0	0	0
17	0	0	0	0	0	0	1	0	0	0	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

**DIVIDE RATIO OF SWALLOW A-COUNTER**

Divide Ratio A	A 5	A 4	A 3	A 2	A 1	A 0
0	0	0	0	0	0	0
1	1	0	0	0	0	0
•	•	•	•	•	•	•
63	1	1	1	1	1	1

SYNTHESIZER SELECT BIT		TEST ENABLE BIT		LD SELECT BIT		CHARGE PUMP CONTROL BIT	
Synthesizer	RF/IF	Status of fo/LD	TE	Signal from fo/LD	LD	Do Output Status	DCP
IF	0	Powered Down	0	f <sub>OUT</sub>	0	Normal Operation	0
RF	1	Active	1	Lock Detect	1	Disabled	1

**PROGRAMMING ORDER**

There is no specific order by which the data words must be programmed for normal operation. In most applications, the RF and IF Programmable Reference Divider words are programmed first and the Programmable N/A Divider words are programmed last. The Programmable N/A Divider words are then changed as the synthesizer is tuned to different channels. It is important to note that the status of the TE and LD fields of the last word programmed determines the state of the fo/LD output.

**PROGRAMMING THE STATE OF THE fo/LD OUTPUT**

The multi-function test pin output can be used to observe any one of six internal signals: fr–RF, fr–IF, fv–RF, fv–IF, Lock–RF, and Lock–IF. In addition this output pin can be disabled to reduce current consumption of the part and minimize switching noise. All these functions are under software control. To fully configure the synthesizer, four data words must be programmed into the device to load all the latches. As previously stated, programming order is not important for normal operation. This is not the case though when the user would like to observe a test point. Under this condition, the last word loaded determines what test point will be observed. The table below illustrates which register needs to be programmed last and the state of the control bits to access each test point.

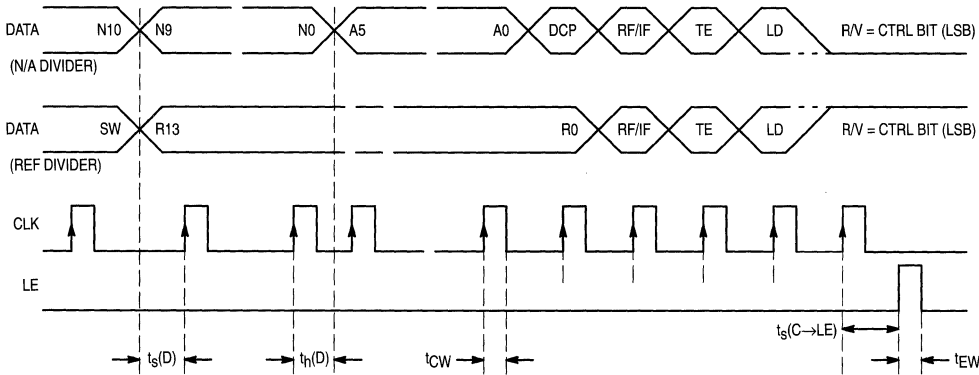
fo/LD Output	Register	R/V	RF/IF	TE	LD
fr IF	Reference Divider	1	0	1	0
fv IF	N/A Divider	0	0	1	0
Lock IF	Either	X	0	1	1
fr RF	Reference Divider	1	1	1	0
fv RF	N/A Divider	0	1	1	0
Lock RF	Either	X	1	1	1
Disabled	Either	X	X	0	X

X = Don't Care

**DIVIDE RATIO SETTING**

$$f_{vco} = [(P \cdot N) + A] \cdot f_{osc} + R \text{ with } A \leq N \text{ (for continuous frequency steps } P \cdot N + A \geq P(P-1))$$

- fvco: Output frequency of external voltage controlled oscillator (VCO)
- N: Preset divide ratio of binary 11-bit programmable counter (16 to 2047)
- A: Preset divide ratio of binary 4-bit or 6-bit swallow counter (0 to 63, A ≤ N, for RF synthesizer; 0 to 15, A ≤ N, for IF synthesizer)
- fosc: Output frequency of the external frequency oscillator
- R: Preset divide ratio of binary 14-bit programmable reference counter (8 to 16383)
- P: Preset mode of dual modulus prescaler (32 or 64 for RF synthesizer; 8 or 16 for IF synthesizer)



NOTE: Data shifted into register on rising edge of CLK.

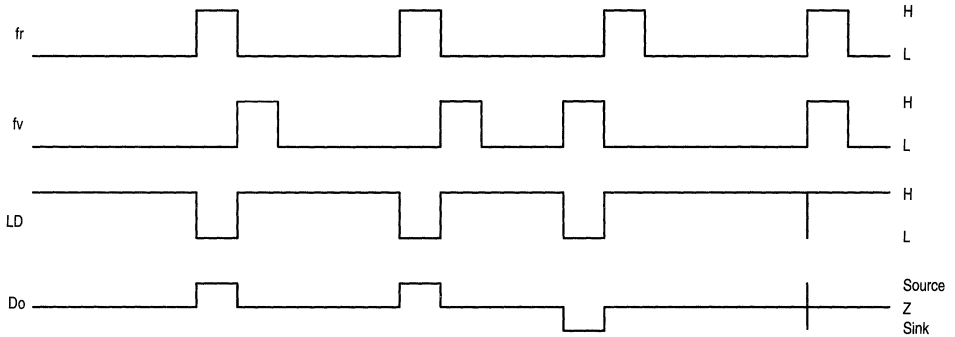
$t_s(D)$ = Setup Time DATA to CLK	$t_s(D) \geq 10\text{ns}$
$t_h(D)$ = Hold Time DATA to CLK	$t_h(D) \geq 20\text{ns}$
$t_{CW}$ = CLK Pulse Width	$t_{CW} \geq 30\text{ns}$
$t_{EW}$ = LE Pulse Width	$t_{EW} \geq 20\text{ns}$
$t_s(C \rightarrow LE)$ = Setup Time CLK to LE	$t_s(C \rightarrow LE) \geq 30\text{ns}$

**Figure 2. Serial Data Input Timing**

### PHASE CHARACTERISTICS/VCO CHARACTERISTICS

The phase comparator in the MC12310 is a high speed digital phase/frequency detector circuit. The circuit determines the "lead" or "lag" phase relationship and time difference between the leading edges of the VCO (fv) signal and the reference (fr) input. Since these edges occur only once per cycle, the detector has a range of  $\pm 2\pi$  radians.

The operation of the phase comparator is shown in 3.



NOTES: Do is a current output.  
Phase difference detection range:  $-2\pi$  to  $+2\pi$   
The spike is output in order to diminish dead band.

$$\text{Internal Charge Pump Gain} \approx \frac{|I_{\text{source}}| + |I_{\text{sink}}|}{4\pi} = \frac{4\text{mA}}{4\pi}$$

**Figure 3. Phase/Frequency Detector, Internal Charge Pump and Lock Detect Waveforms**

#### **fr lags fv in phase OR fv > fr in frequency**

When the phase of fr lags that of fv or the frequency of fv is greater than fr, the Do output will sink current. The pulse width will be determined by the time difference between the two rising edges.

#### **fr leads fv in phase OR fv < fr in frequency**

When the phase of fr leads that of fv or the frequency of fv is less than fr, the Do output will source current. The pulse width will be determined by the time difference between the two rising edges.

#### **fr = fv in phase and frequency**

When the phase and frequency of fr and fv are equal, the charge pump will be in a quiet state, except for current spikes when signals are in phase. This situation indicates that the loop is in lock and the phase comparator will maintain the loop in its locked state.

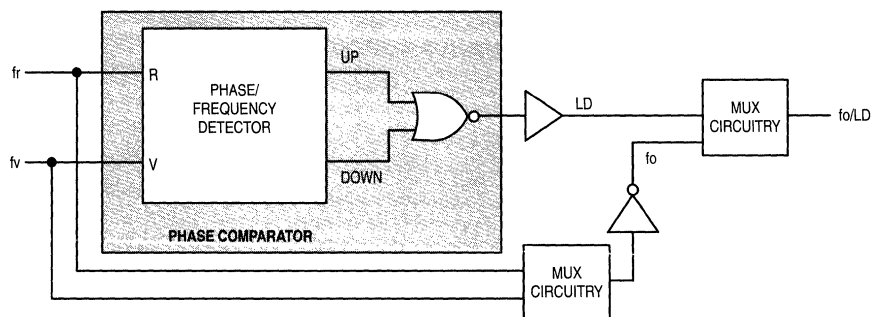


Figure 4. Detailed Phase/Frequency Comparator Block Diagram

### LOCK DETECT

When the lock detector signal (Lock-IF or Lock-RF) is selected to be routed to the fo/LD output pin, the lock detector circuit provides a LOW pulse when fr and fv are not equal in phase or frequency. The output is normally HIGH. LD is designed to be the logical NORing of the phase frequency detector's outputs UP and DOWN. See 6. In typical applications the output signal drives external circuitry which provides a steady LOW signal when the loop is locked. See 9.

### fo

When selected, the output frequency pin (fo/LD) provides a LOW going pulse at the fr or fv rate. The pulse width is determined by the frequency in the respective counter. This output is for test purposes only and may not swing all the way down to ground. The scope probe capacitive load should be less than 5pF.

### OSCILLATOR INPUT

The device incorporates an on-chip reference buffer so that an external reference oscillator signal can be ac-coupled to the OSCin pin through a coupling capacitor. The magnitude of the ac-coupled signal must be between 500 and 2200 mV peak-to-peak.

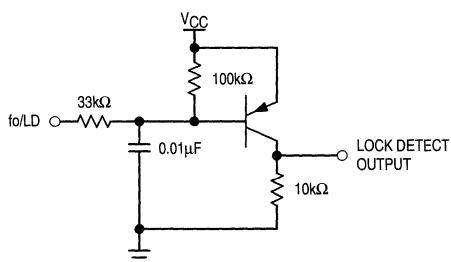


Figure 5. Typical Lock Detect Circuit

**ELECTRICAL CHARACTERISTICS** ( $V_{CC} = 2.7$  to  $5.5V$ ;  $V_P = V_{CC}$  to  $6.0V$ ;  $T_A = -40$  to  $+85^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit	Condition
$I_{CC}$	Supply Current for $V_{CC}$		11.5		mA	Note 1
			12.5		mA	Note 2
$I_P$	Supply Current for $V_P$		0.5		mA	Note 3
			0.7		mA	Note 4
$F_{IN-RF}$	Operating Frequency $f_{INmax}$ $f_{INmin}$	2500		500	MHz	Note 5
$F_{IN-IF}$	Operating Frequency $f_{INmax}$ $f_{INmin}$	500		40	MHz	Note 5
$F_{OSC}$	Operating Frequency (OSCin)	TBD	12	40	MHz	Note 5
$V_{IN}$	Input Sensitivity $f_{IN-RF}$ (100–500MHz) $f_{IN-IF}$ (40–100MHz) $f_{IN-IF}$	200		1000	mV <sub>p-p</sub>	
		200		1000		
		600		2000		
$V_{OSC}$	OSCin	500		2200	mV <sub>p-p</sub>	
$V_{IH}$	Input HIGH Voltage CLK, DATA, LE	$0.7V_{CC}$			V	
$V_{IL}$	Input LOW Voltage CLK, DATA, LE			$0.3V_{CC}$	V	
$I_{IH}$	Input HIGH Current (DATA, CLK and LE)		0.1	2.0	$\mu A$	$V_{CC} = 5.5V$
$I_{IL}$	Input LOW Current (DATA, CLK and LE)	-2.0	-0.1		$\mu A$	$V_{CC} = 5.5V$
$I_{OSC}$	Input Current (OSCin)		TBD		$\mu A$	
$I_{Source}$	Charge Pump Output Current		-2.0		mA	$V_{Do} = V_P/2$ ; $V_P = 2.7V$
$I_{Sink}$	Do		+2.0		mA	$V_{CC} = 2.7V$ ; Note 6
$I_{Hi-Z}$	Output Disabled	-15		+15	nA	$0.5V < V_{Do} < V_P - 0.5V$
$V_{OH}$	Output HIGH Voltage (fo/LD)	4.4			V	$V_{CC} = 5.0V$
		2.4			V	$V_{CC} = 3.0V$
$V_{OL}$	Output LOW Voltage (fo/LD)			0.4	V	$V_{CC} = 5.0V$
				0.4	V	$V_{CC} = 3.0V$
$I_{OH}$	Output HIGH Current (fo/LD)			-1.0	mA	
$I_{OL}$	Output LOW Current (fo/LD)	1.0			mA	

1.  $V_{CC} = 3.3V$ , all outputs open.

2.  $V_{CC} = 5.5V$ , all outputs open.

3.  $V_P = 3.3V$ , all outputs open.

4.  $V_P = 6.0V$ , all outputs open.

5. AC coupling,  $F_{IN}$  measured with a 1000pF capacitor.

6. Source current flows out of the pin and sink current flows into the pin, typical charge pump sink and source curves are found in Figure 9.

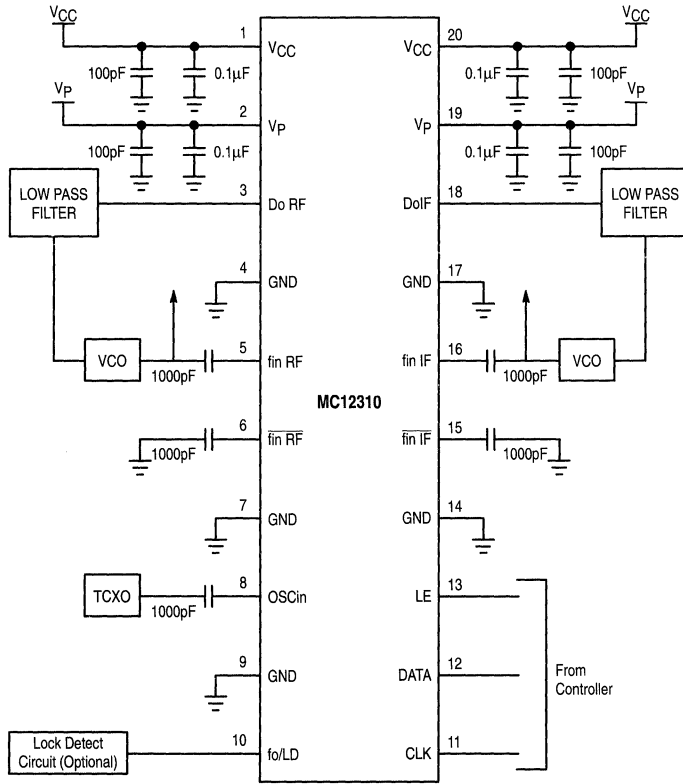


Figure 6. Typical Applications Example

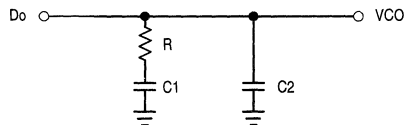


Figure 7. Typical Loop Filter

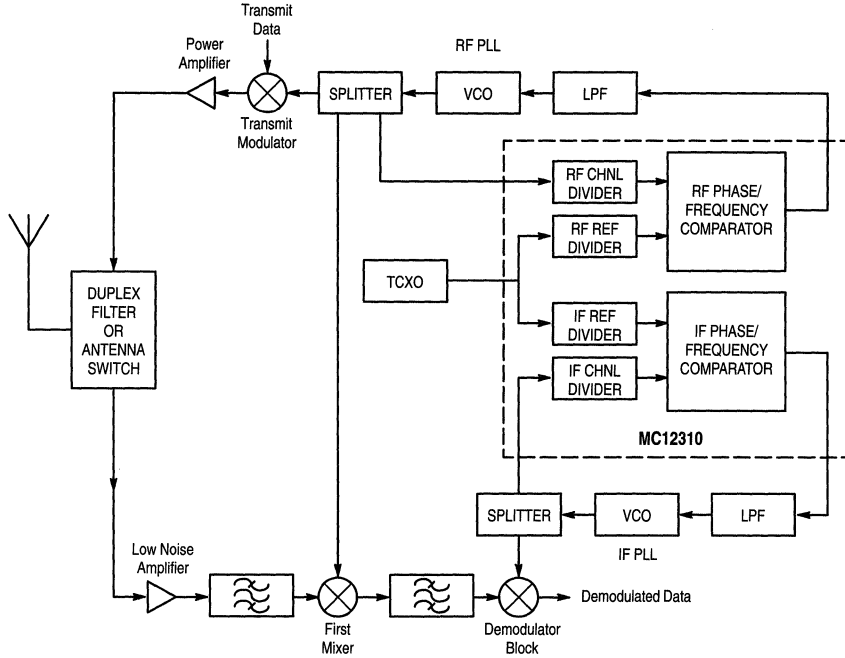


Figure 8. Typical Sub-System Block Diagram

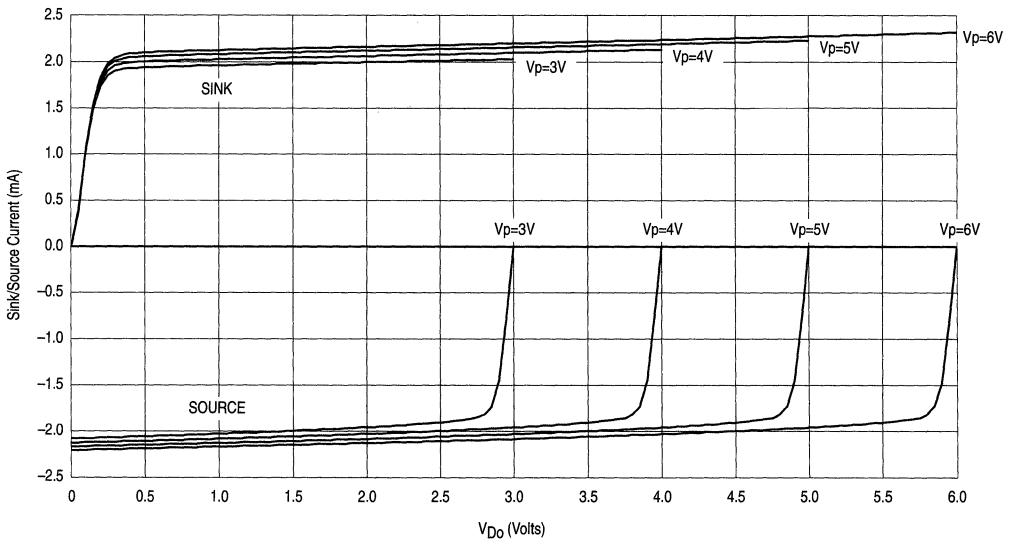


Figure 9. Typical MC12310 Charge Pump Sink and Source Current versus  $V_{Do}$   
 ( $V_{CC} = 2.7V, T_A = 25^\circ C$ )



# Applications Information

# Phase-Locked Loop Design Fundamentals

*Prepared by*  
**Garth Nash**  
Applications Engineering

*The fundamental design concepts for phase-locked loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example.*



# Phase-Locked Loop Design Fundamentals

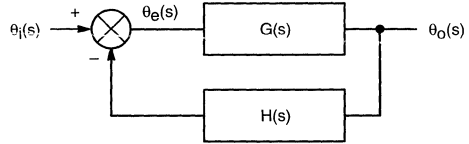
## Introduction

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase-Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace Transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted, hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

## Parameter Definition

The Laplace Transform permits the representation of the time response  $f(t)$  of a system in the complex domain  $F(s)$ . This response is twofold in nature in that it contains both transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.<sup>1</sup>

The parameters in Figure 1 are defined and will be used throughout the text.



- $\theta_i(s)$  Phase Input
- $\theta_e(s)$  Phase Error
- $\theta_o(s)$  Output Phase
- $G(s)$  Product of the Individual Feed Forward Transfer Functions
- $H(s)$  Product of the Individual Feedback Transfer Functions

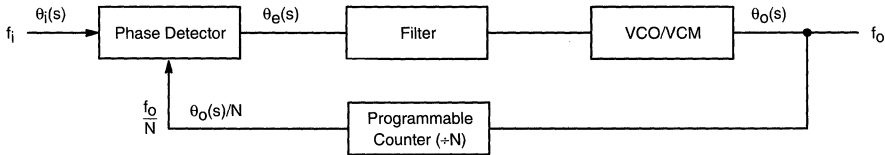
**Figure 1. Feedback System**

Using servo theory, the following relationships can be obtained.<sup>2</sup>

$$\theta_e(s) = \frac{1}{1 + G(s) H(s)} \theta_i(s) \quad (5)$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s) H(s)} \theta_i(s) \quad (6)$$

These parameters relate to the functions of a PLL as shown in Figure 2.



**Figure 2. Phase Locked Loop**

The phase detector produces a voltage proportional to the phase difference between the signals  $\theta_i$  and  $\theta_o/N$ . This voltage upon filtering is used as the control signal for the VCO/VCM (VCM – Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N f_i \quad (7)$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path ( $N = 1$ ). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

### Type — Order

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The **type** of a system refers to the number of poles of the loop transfer function  $G(s)H(s)$  located at the origin. Example:

$$\text{let } G(s)H(s) = \frac{10}{s(s+10)} \quad (8)$$

This is a *type one* system since there is only one pole at the origin.

The **order** of a system refers to the highest degree of the polynomial expression

$$1 + G(s)H(s) = 0 \triangleq \text{C.E.} \quad (9)$$

which is termed the **Characteristic Equation** (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.

Example:

$$G(s)H(s) = \frac{10}{s(s+10)} \quad (10)$$

then

$$1 + G(s)H(s) = 1 + \frac{10}{s(s+10)} = 0 \quad (11)$$

therefore

$$\text{C.E.} = s(s+10) + 10 \quad (12)$$

$$\text{C.E.} = s^2 + 10s + 10 \quad (13)$$

which is a *second order* polynomial. Thus, for the given  $G(s)H(s)$ , we obtain a type 1 second order system.

### Error Constants

Various inputs can be applied to a system. Typically, these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$  represents the phase error that exists in the phase detector between the incoming reference signal  $\theta_i(s)$  and the feedback  $\theta_o(s)/N$ . In evaluating a system,  $\theta_e(s)$  must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error  $\theta_e(s)$  resulting from the input  $\theta_i(s)$  without transforming back to the time domain.<sup>3</sup>

Simply stated

$$\lim_{t \rightarrow \infty} [\theta(t)] = \lim_{s \rightarrow 0} [s\theta_e(s)] \quad (14)$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)H(s)} \theta_i(s) \quad (15)$$

The input signal  $\theta_i(s)$  is characterized as follows:

$$\text{Step position: } \theta_i(t) = C_p t \geq 0 \quad (16)$$

$$\text{Or, in Laplace notation: } \theta_i(s) = \frac{C_p}{s} \quad (17)$$

where  $C_p$  is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by  $C_p$  radians:

$$\text{Step velocity: } \theta_i(t) = C_v t \geq 0 \quad (18)$$

$$\text{Or, in Laplace notation: } \theta_i(s) = \frac{C_v}{s^2} \quad (19)$$

where  $C_v$  is the magnitude of the rate of change of phase in radians per second. This corresponds to inputting a frequency that is different than the feedback portion of the VCO frequency. Thus,  $C_v$  is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration: } \theta_i(t) = C_a t^2 \geq 0 \quad (20)$$

$$\text{Or, in Laplace notation: } \theta_i(s) = \frac{2 C_a}{s^3} \quad (21)$$

$C_a$  is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop  $G(s)H(s)$  transfer functions for types 1, 2, and 3 are:

$$\text{Type 1 } G(s)H(s) = \frac{K}{s(s+a)} \quad (22)$$

$$\text{Type 2} \quad G(s) H(s) = \frac{K(s+a)}{s^2} \quad (23)$$

$$\text{Type 3} \quad G(s) H(s) = \frac{K(s+a)(s+b)}{s^3} \quad (24)$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\begin{aligned} \theta_e(s) &= \left( \frac{1}{1 + \frac{K}{s(s+a)}} \right) \left( \frac{C_p}{s} \right) \\ &= \frac{(s+a)C_p}{(s^2 + as + K)} \end{aligned} \quad (25)$$

$$\theta_e(t = \infty) = \lim_{s \rightarrow 0} \left[ s \left( \frac{s+a}{s^2 + as + K} \right) C_p \right] = 0 \quad (26)$$

Thus, the final value of the phase error is zero when a step position (phase) is applied.

Similarly, applying the three inputs into type 1, 2, and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

**Table 1. Steady State Phase Errors for Various System Types**

	Type 1	Type 2	Type 3
Step Position	Zero	Zero	Zero
Step Velocity	Constant	Zero	Zero
Step Acceleration	Continually Increasing	Constant	Zero

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table 1, the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

### Stability

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the

characteristic equation) vary with loop gain. For stability, all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.<sup>2</sup>

Rule 1 – The root locus begins at the poles of  $G(s) H(s)$  ( $K = 0$ ) and ends at the zeroes of  $G(s) H(s)$  ( $K = \infty$ ), where  $K$  is loop gain.

Rule 2 – The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of  $G(s) H(s)$ .

Rule 3 – The root locus contour is bounded by asymptotes whose angular position is given by:

$$\frac{(2n+1)}{\#P - \#Z} \pi; \quad n = 0, 1, 2, \dots \quad (27)$$

Where  $\#P$  ( $\#Z$ ) is the number of poles (zeroes).

Rule 4 – The intersection of the asymptotes is positioned at the center of gravity C.G.:

$$\text{C.G.} = \frac{\sum P - \sum Z}{\#P - \#Z} \quad (28)$$

Where  $\sum P$  ( $\sum Z$ ) denotes the summation of the poles (zeroes).

Rule 5 – On a given section of the real axis, root loci may be found in the section only if the  $\#P + \#Z$  to the right is odd.

Rule 6 – Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \quad (29)$$

Again, where  $K$  is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s) H(s) = \frac{K}{s(s+4)} \quad (30)$$

The root locus has two branches (Rule 2) which begin at  $s = 0$  and  $s = -4$  and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes, the equation becomes:

$$\frac{2n+1}{2} \pi = \begin{cases} \frac{\pi}{2} & \text{for } n = 0 \\ \frac{3\pi}{2} & \text{for } n = 1 \end{cases} \quad (31)$$

The position of the intersection according to the Rule 4 is:

$$s = \frac{\sum P - \sum Z}{\#P - \#Z} = \frac{(-4 - 0) - (0)}{2 - 0}$$

$$s = -2 \quad (32)$$

The breakaway point, as defined by Rule 6, can be found by first writing the characteristic equation.

$$C.E. = 1 + G(s) H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \quad (33)$$

Now solving for K yields

$$K = -s^2 - 4s \quad (34)$$

Taking the derivative with respect to s and setting it equal to zero, then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \quad (35)$$

$$\frac{dK}{ds} = -2s - 4 = 0 \quad (36)$$

or

$$s = -2 \quad (37)$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

The second order characteristic equation, given by Equation 29, has been normalized to a standard form<sup>2</sup>

$$s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (38)$$

where the damping ratio  $\xi = \cos \phi$  ( $0^\circ \leq \phi \leq 90^\circ$ ) and  $\omega_n$  is the natural frequency as shown in Figure 3.

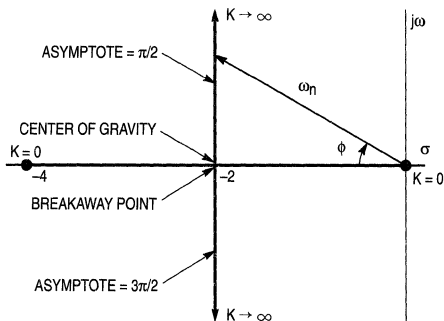


Figure 3. Type 1 Second Order Root Locus Contour

The response of this type 1, second order system to a step input, is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

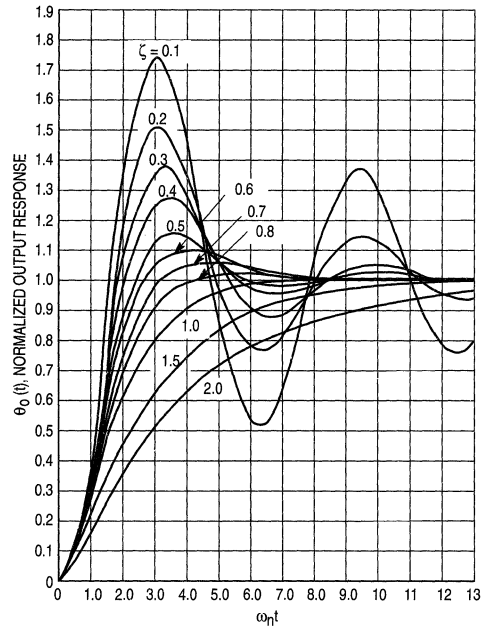


Figure 4. Type 1 Second Order Step Response

The overshoot and stability as a function of the damping ratio  $\xi$  is illustrated by the various plots. Each response is plotted as a function of the normalized time  $\omega_n t$ . For a given  $\xi$  and a lock-up time  $t$ , the  $\omega_n$  required to achieve the desired results can then be determined. Example:

Assume  $\xi = 0.5$   
error < 10%  
for  $t > 1$  ms

From  $\xi = 0.5$  curve error is less than 10% of final value for all time greater than  $\omega_n t = 4.5$ . The required  $\omega_n$  can then be found by:

$$\omega_n t = 4.5 \quad (39)$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{ krad/s} \quad (40)$$

$\xi$  is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.

Example:

Another common loop transfer function takes the form:

$$G(s) H(s) = \frac{(s + a)k}{s^2} \quad (41)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero, the poles would move along the  $j\omega$  axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is  $s = a$ ; however, with only one asymptote, there is no intersection at this point. The root locus lies on a circle centered at  $s = -a$  and continues on all portions of the negative real axis to left of the zero. The breakaway point is  $s = -2a$ .

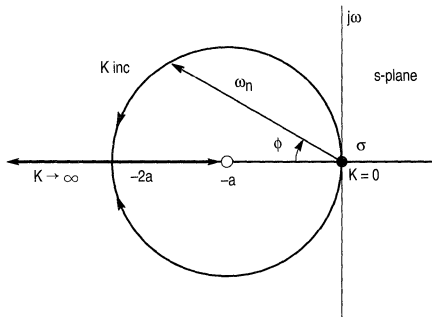


Figure 5. Type 2 Second Order Root Locus Contour

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example, the required  $\omega_n$  can be determined by the use of the graph when  $\xi$  and the lock-up time are given.

### Bandwidth

The -3dB bandwidth of the PLL is given by:

$$\omega_{-3dB} = \omega_n \left( 1 - 2\xi^2 + \sqrt{2 - 4\xi^2 + 4\xi^4} \right)^{1/2} \quad (42)$$

for a type 1 second order<sup>4</sup> system, and by:

$$\omega_{-3dB} = \omega_n \left( 1 + 2\xi^2 + \sqrt{2 + 4\xi^2 + 4\xi^4} \right)^{1/2} \quad (43)$$

for a type 2 second order<sup>1</sup> system.

### Phase-Locked Loop Design Example

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach to

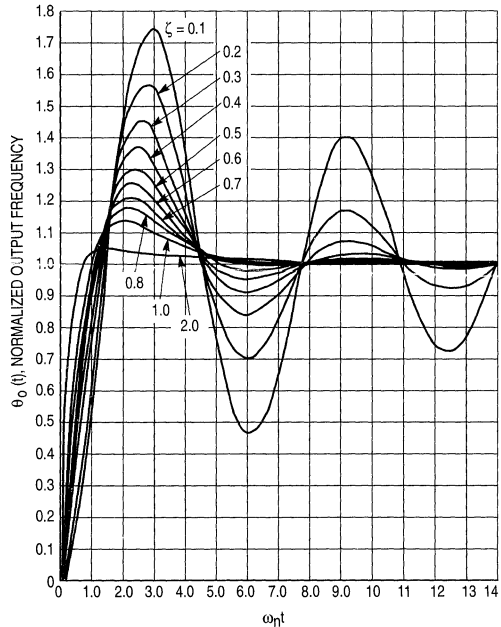


Figure 6. Type 2 Second Order Step Response

these design constraints is now illustrated. It is desired for the system to have the following specifications:

Output Frequency	2.0MHz to 3.0MHz
Frequency Steps	100KHz
Phase Coherent Frequency Output	—
Lock-Up Time Between Channels	1ms
Overshoot	<20%

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer

From the given specifications, the circuit parameters shown in Figure 7 can now be determined.

The devices used to configure the PLL are:

Frequency-Phase Detector	MC4044/4344
Voltage Controlled Multivibrator (VCM)	MC4024/4324
Programmable Counter	MC4016/4316

The forward and feedback transfer functions are given by:

$$G(s) = K_p K_f K_o \quad H(s) = K_n \quad (44)$$

where  $K_n = 1/N$  (45)

The programmable counter divide ratio  $K_n$  can be found from Equation 3.

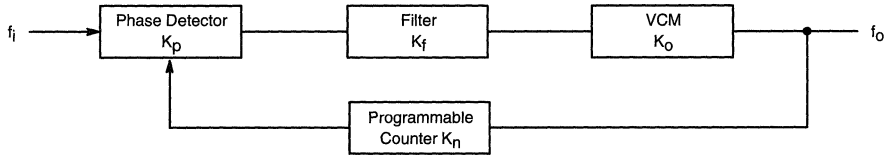


Figure 7. Phase-Locked Loop Circuit Parameters

$$N_{\min} = \frac{f_o \min}{f_i} = \frac{f_o \min}{f_{\text{step}}} = \frac{2\text{MHz}}{100\text{KHz}} = 20 \quad (46)$$

$$N_{\max} = \frac{f_o \max}{f_{\text{step}}} = \frac{3\text{MHz}}{100\text{KHz}} = 30 \quad (47)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \quad (48)$$

A type 2 system is required to produce a phase coherent output relative to the input (See Table 1). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2MHz to 3MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields  $C = 100\text{pF}$ . The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

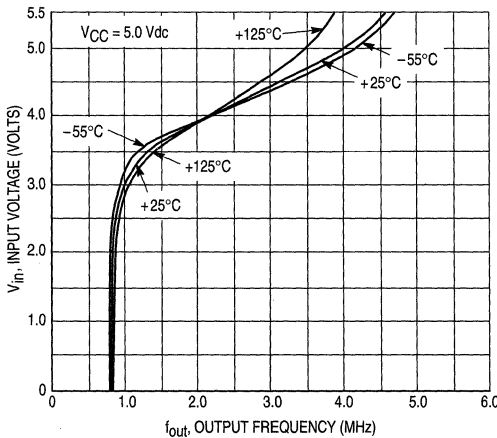


Figure 8. MC4324 Input Voltage versus Output Frequency (100pF Feedback Capacitor)

The transfer function of the VCM is given by:

$$K_o = \frac{K_v}{s} \quad (49)$$

Where  $K_v$  is the sensitivity in radians per second per volt. From the curve in Figure 8,  $K_v$  is found by taking the reciprocal of the slope.

$$K_v = \frac{4\text{MHz} - 1.5\text{MHz}}{5\text{V} - 3.6\text{V}} = 2\pi \text{ rad/s/V}$$

$$K_v = 11.2 \times 10^6 \text{ rad/s/V} \quad (50)$$

Thus

$$K_o = \frac{11.2 \times 10^6}{s} \text{ rad/s/V} \quad (51)$$

The  $s$  in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by<sup>5</sup>

$$K_p = \frac{DF_{\text{High}} - UF_{\text{Low}}}{2(2\pi)} = \frac{2.3\text{V} - 0.9\text{V}}{4\pi} = 0.111\text{V/rad} \quad (52)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 23. The parameters thus far determined include  $K_p, K_o, K_n$  leaving only  $K_f$  as the variable for design. Writing the loop transfer function and relating it to Equation 23

$$G(s)H(s) = \frac{K_p K_v K_n K_f}{s} = \frac{K(s+a)}{s^2} \quad (53)$$

Thus,  $K_f$  must take the form

$$K_f = \frac{s+a}{s} \quad (54)$$

in order to provide all of the necessary poles and zeroes for the required  $G(s)H(s)$ . The circuit shown in Figure 9 yields the desired results.

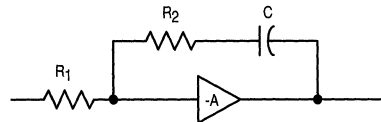


Figure 9. Active Filter Design



$K_f$  is expressed by

$$K_f = \frac{R_2 C s + 1}{R_1 C s} \text{ for large } A \quad (55)$$

where  $A$  is voltage gain of the amplifier.

$R_1$ ,  $R_2$ , and  $C$  are then the variables used to establish the overall loop characteristics.

The MC4044/4344 provides the active circuitry required to configure the filter  $K_f$ . An additional low current high  $\beta$  buffering device or FET can be used to boost the input impedance, thus minimizing the leakage current from the capacitor  $C$  between sample updates. As a result, longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor  $K_C$  must be applied to  $K_f$  in order to properly characterize the function.  $K_C$  is found experimentally to be  $K_C = 0.5$ .

$$K_{fc} = K_f K_C = 0.5 \left( \frac{R_2 C s + 1}{R_1 C s} \right) \quad (56)$$

(For large gain, Equation 55 applies.)

The PLL circuit diagram is shown in Figure 11 and its Laplace representation in Figure 10.

The loop transfer function is

$$G(s) H(s) = K_p K_{fc} K_o K_n \quad (57)$$

$$G(s)H(s) = K_p(0.5) \left( \frac{R_2 C s + 1}{R_1 C s} \right) \left( \frac{K_v}{s} \right) \left( \frac{1}{N} \right) \quad (58)$$

The characteristic equation takes the form

$$\begin{aligned} \text{C.E.} &= 1 + G(s) H(s) = 0 \\ &= s^2 + \frac{0.5 K_p K_v R_2}{R_1 N} s + \frac{0.5 K_p K_v}{R_1 C N} \end{aligned} \quad (59)$$

Relating Equation 59 to the standard form given by Equation 38

$$\begin{aligned} s^2 + \frac{0.5 K_p K_v R_2}{R_1 N} s + \frac{0.5 K_p K_v}{R_1 C N} \\ = s^2 + 2\zeta\omega_n s + \omega_n^2 \end{aligned} \quad (60)$$

Equating like coefficients yields

$$\frac{0.5 K_p K_v}{R_1 C N} = \omega_n^2 \quad (61)$$

$$\text{and } \frac{0.5 K_p K_v R_2}{R_1 N} = 2\zeta\omega_n \quad (62)$$

With the use of an active filter whose open loop gain ( $A$ ) is large ( $K_C = 1$ ), Equations 61 and 62 become

$$\frac{K_p K_v}{R_1 C N} = \omega_n^2 \quad (63)$$

$$\frac{K_p K_v R_2}{R_1 N} = 2\zeta\omega_n \quad (64)$$

The percent overshoot and settling time are now used to determine  $\omega_n$ . From Figure 6, it is seen that a damping ratio  $\zeta = 0.8$  will produce a peak overshoot less than 20% and will settle within 5% at  $\omega_n t = 4.5$ . The required lock-up time is 1ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5 \text{krad/s} \quad (65)$$

Rewriting Equation 61

$$R_1 C = \frac{0.5 K_p K_v}{\omega_n^2 N} \quad (66)$$

$$= \frac{(0.5) (0.111) (11.2 \times 10^6)}{(4500)^2} (30)$$

$$R_1 C = 0.00102$$

(Maximum overshoot occurs at  $N_{\max}$  which is minimum loop gain)

$$\text{Let } C = 0.5\mu\text{F}$$

$$\text{Then } R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04\text{k}\Omega$$

$$\text{Use } R_1 = 2\text{k}\Omega$$

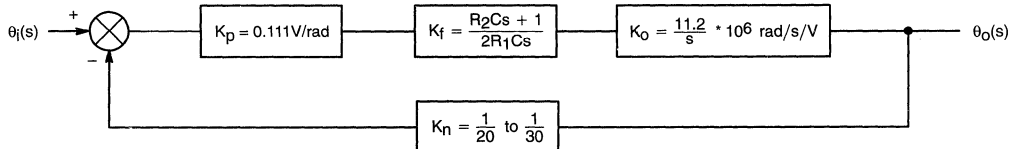


Figure 10. Laplace Representation of Diagram in Figure 11

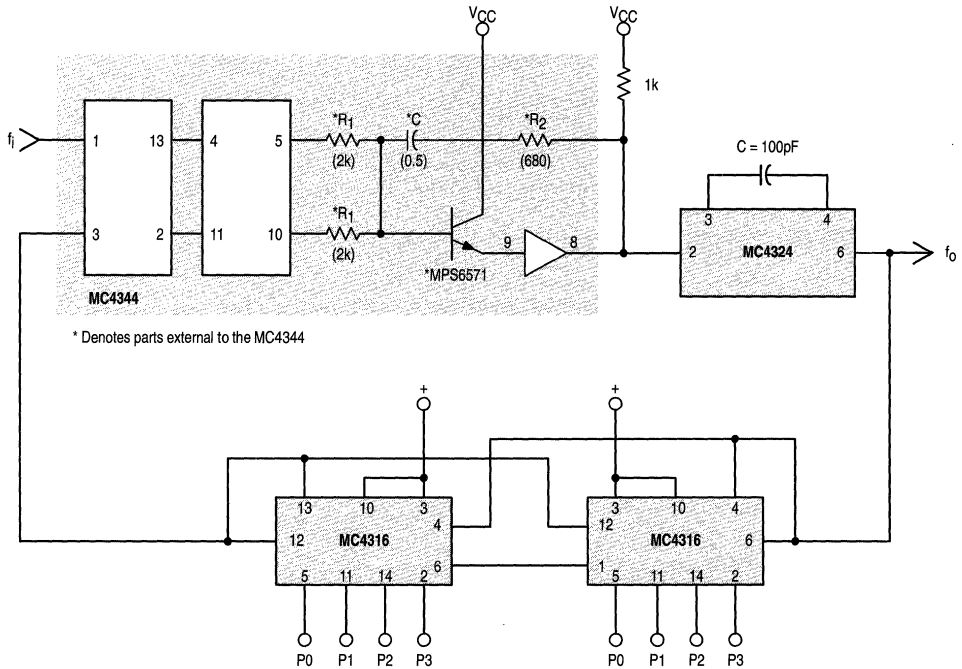


Figure 11. Circuit Diagram of Type 2 Phase-Locked Loop

R<sub>1</sub> is typically selected greater than 1kΩ.

Solving for R<sub>2</sub> in Equation 62

$$R_2 = \frac{2\zeta \omega_n R_1 N}{K_p K_v (0.5)} = \frac{2\zeta}{C \omega_n} \quad (67)$$

$$= \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5k)}$$

$$= 711\Omega$$

Use R<sub>2</sub> = 680Ω

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio K<sub>N</sub>, the closed loop poles will vary its position as K<sub>N</sub> varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

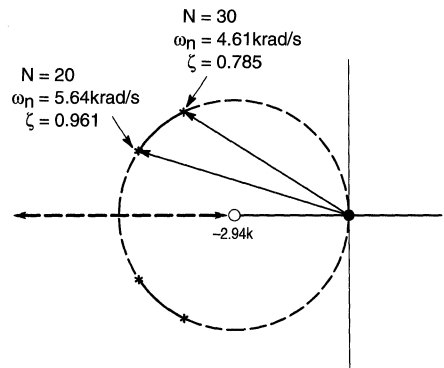


Figure 12. Root Locus Variation

NOTE: The type 2 second order loop was illustrated as a design sample because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency, a type 2 loop still offers an optimum design.

## Experimental Results

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve  $N = 30$  illustrates the frequency response when the programmable counter is stepped from 29 to 30, thus producing a change in the output frequency from 2.9MHz to 3.0MHz. An overshoot of 18% is obtained and the output frequency is within 5kHz of the final value one millisecond after the applied step. The curve  $N = 20$  illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate, but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30, the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrated that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than  $2\pi$ , i.e. there is no cycle slippage at the phase detector.

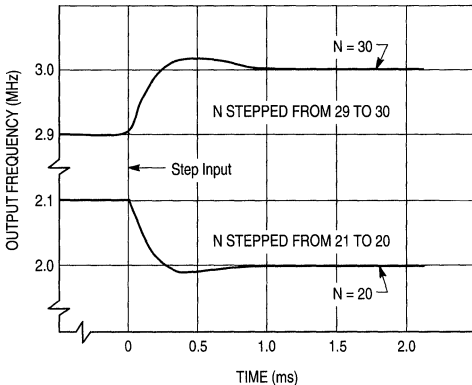


Figure 13. Frequency-Time Response

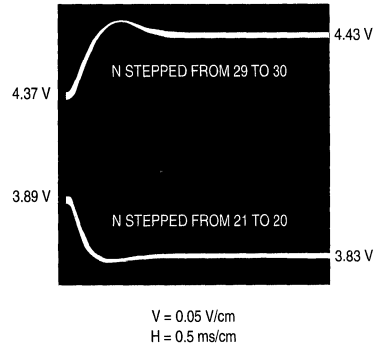


Figure 14. VCM Control Voltage (Frequency) Transient

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 62 and 63 (type 2) as the input variables and is valid for all damping ratios of  $\zeta \leq 1.0$ . The program prints or plots control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one, the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between experimental and analytical results.

## Summary

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

\*THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT

PHASE DETECTOR GAIN CONSTANT	P1 = 0.111 VOLTS PER RADIAN
VCM GAIN CONSTANT	V1 = 1.12 E+7 RAD PER VOLT
FILTER INPUT RESISTOR	R1 = 3900 OHMS (R1C = 2k)
FILTER FEEDBACK RESISTOR	R2 = 680 OHMS
FILTER CAPACITOR	C1 = 0.5 MICROFARADS
DIVIDER VALUE	N1-N2 = 29 - 30
REFERENCE FREQUENCY	F1 = 100000 CPS
OUTPUT FREQUENCY CHANGE	F5 = 100000 CPS

P2 = 0.111	C2 = 0.5
V2 = 1.12 E+7	N3-N4 = 21 - 20
R3 = 3900 (R1C = 2k)	F2 (F6) = 100000 (100000)
R4 = 680	

PLOT OF FUNCTIONS

(NOTE: Y(T) IS '+', Z(T) IS '\*', AND '0' IS COMMON)

FOR T:	TOP = 0	BOTTOM = 0.0015	INCREMENT = 0.0005
FOR FCTS:	LEFT = 0	RIGHT = 0.12	INCREMENT = 0.002

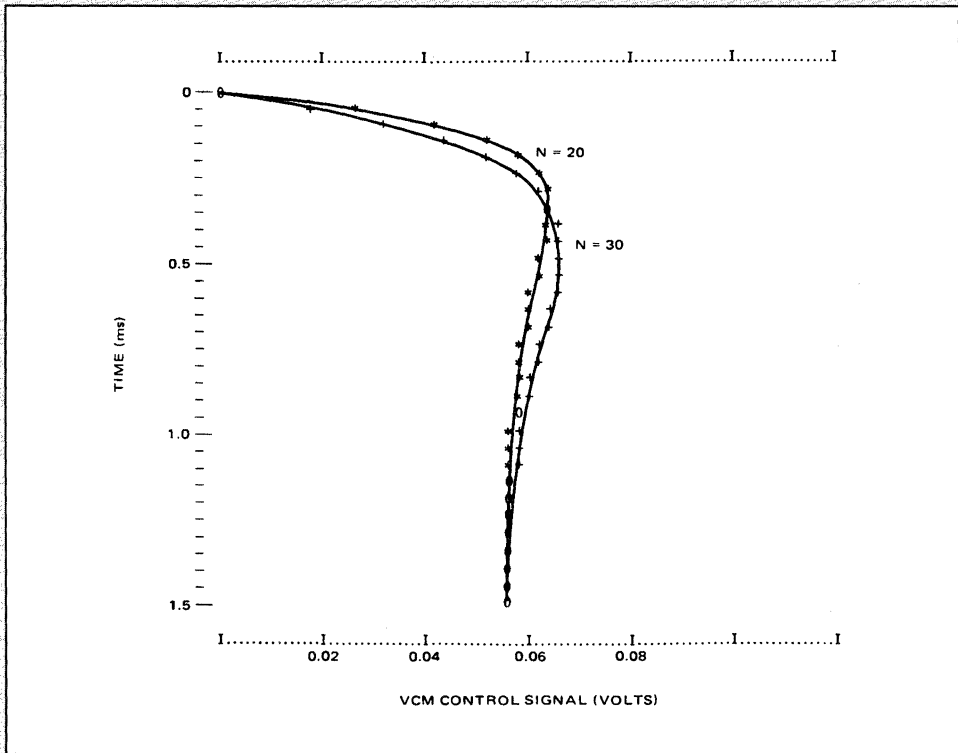


Figure 15. VCM Control Signal Transient

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## **Phase-Locked Loop Design Articles**

- "Analyze, Don't Estimate, Phase-Locked Loop Performance"
- "Optimize Phase-Lock Loops to Meet Your Needs — Or Determine Why You Can't"
- "Suppress Phase-Lock-Loop Sidebands Without Introducing Instability"
- "Programmable Calculator Computes PLL Noise, Stability"



# Analyze, don't estimate, phase-lock-loop performance of type-2, third-order systems. You can do the job with a programmable-calculator in 48 steps, or less.

Phase-lock loops certainly have many uses, especially in frequency synthesizers, but exact mathematical calculation of their transfer functions is difficult. This is particularly true for type-2, third-order systems (Figure 1), which don't produce steady-state phase errors for step-position or velocity signal inputs. However, a small programmable calculator, the HP-25, easily — and exactly — determines the complete loop transfer function in 48 steps. In addition, the program data reveals the noise reduction you can expect for the loop's voltage-controlled oscillator (VCO), as well as the loop's stability.

Most other design approaches must resort to second-order loop approximations to simplify calculations; a more exact method manually would take too long.

Unlike a type-1 loop, a type-2 loop has two *true* integrators within the loop — a VCO and an integrator/filter after the phase detector. Replacing the integrator/filter with a passive-RC, low-pass filter results in the more common type-1 response, which doesn't have the phase coherence for step and velocity inputs between the two signal inputs to the phase comparator that the type-2 has.

Moreover, a third-order loop — the order is usually determined by the transfer function of the integrator/filter ( $F_S$ ) — can reduce VCO noise substantially, without increasing reference-frequency sidebands in the output signal. These sidebands hamper simpler loop-circuit performance.

The transfer function of a generalized phase-lock loop can be represented as follows (Figure 2):

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)H(s)} \quad (1)$$

where, from Figure

$$G(s) = (K_p) (F(s)) (K_v/s) \quad (2)$$

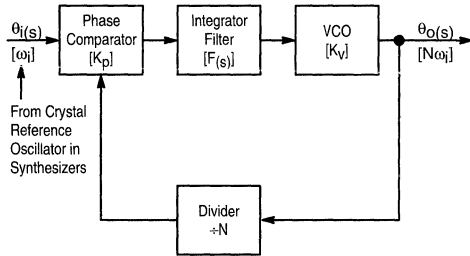
$$\text{and } H(s) = 1/N \quad (3)$$

The phase comparator transfer function is  $K_p$  and  $N$  is a digital counter/divider factor.

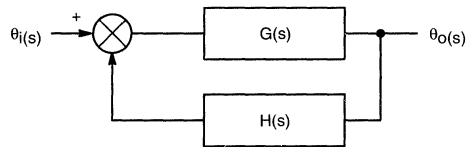
A typical integrator/filter built around an op amp (Figure 3) has a transfer function determined by the amplifier-circuit's closed-loop gain,

$$A_{CL} = -\frac{Z_f}{Z_i}$$

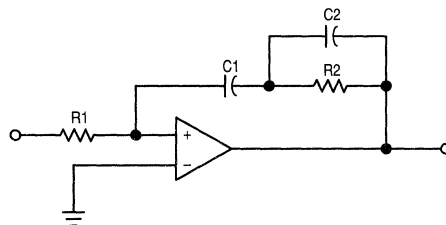
**Andrzej B. Przedpelski**, Vice President of Development, A.R.F. Products Inc., 2559 75th St., Boulder, CO 80301.



**Figure 1. A type-2 phase-lock loop** has two true integrators — the integrator/filter ( $F_S$ ) and the VCO ( $K_V$ ). Replacing the integrator/filter with a passive-RC network converts the circuit to a type-1 system.



**Figure 2. The phase-lock loop's generalized open-loop transfer function,  $G(s)H(s)$ , has a third-order denominator** — from which the circuit's name is derived.



**Figure 3. An integrator/filter circuit** can be built with a wideband op amp and RC feedback network.

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**Table 1. Third order type-2 PLL**

Display		Key Entry	Remarks	Registers
Line	Code			
00				R <sub>0</sub>
01	1573	(g)π		
02	61	x		
03	02	2		R <sub>1</sub> T <sub>1</sub>
04	61	x		
05	2307	STO7		
06	2403	RCL3		R <sub>2</sub> T <sub>2</sub>
07	61	x		
08	01	1		
09	1509	(g)→P		R <sub>3</sub> T <sub>3</sub>
10	2304	STO4		
11	22	R↓		
12	2402	RCL2		R <sub>4</sub>
13	2407	RCL7		
14	61	x		
15	32	CHS		R <sub>5</sub> $\frac{K_p K_v}{N}$
16	01	1		
17	32	CHS		
18	1509	(g)→P		R <sub>6</sub>
19	2404	RCL4		
20	71	+		
21	2405	RCL5		R <sub>7</sub>
22	61	x		
23	2401	RCL1		
24	71	+		
25	2407	RCL7		
26	1502	(g) x <sup>2</sup>		
27	71	+		
28	2304	STO4		
29	1408	(f) log		
30	02	2		
31	00	0		
32	61	x	G <sub>jω</sub> H <sub>jω</sub>	
33	74	R/S		
34	22	R↓		
35	21	x ≙ y		
36	41	—	∠θ	
37	74	R/S		
38	2404	RCL4		
39	1409	(f)→R		
40	01	1		
41	51	+		
42	1509	(g)→P		
43	1522	(g) 1/x		
44	1408	(f) log		
45	02	2		
46	00	0	e/en	
47	61	x		
48	1300	GTO 00		
49				

where  $Z_1 = R_1$  (4)  
 $Z_f$  = impedance of feedback network

The transform of the feedback network is

$$Z_f(s) = \frac{s(C_1 + C_2) + \frac{1}{R_2}}{sC_1(sC_2 + \frac{1}{R_2})}, \quad (5)$$

and the integrator/filter transfer function is then

$$F(s) = - \frac{s(C_1 + C_2) + \frac{1}{R_2}}{C_1 R_1 (sC_2 + \frac{1}{R_2})}, \quad (6)$$

Multiply Equation 6 by  $R_2/R_2$ , then

$$F(s) = - \frac{s(C_1 R_2 + C_2 R_2) + 1}{s C_1 R_1 (s C_2 R_2 + 1)}, \quad (7)$$

or

$$F(s) = - \frac{s T_2 + 1}{s T_1 (s T_3 + 1)}, \quad (8)$$

where  $T_1 = R_1 C_1$   
 $T_2 = R_2 (C_1 + C_2)$   
 $T_3 = R_2 C_2$

The open-loop transfer function of Figure 2 is  $G(s) H(s)$ ; therefore, from Equations 2, 3 and 8

$$G(s)H(s) = \frac{s(T_2)(K_v K_p) + K_v K_p}{s^3 N T_1 T_3 + s^2 N T_1} \quad (9)$$

Note the third-order denominator, from which the circuits name — third-order-loop — is derived. Note also the deletion of the minus sign: the circuit configuration (a phase inverter) provides the negative feedback. Both  $K_p$  and  $K_v$  are positive.

If you substitute  $j\omega$  for  $s$  in Equation 9, you can get the equation for plotting the magnitude and phase of the circuit's open-loop gain as a function of frequency:

$$G(j\omega)H(j\omega) = \frac{j\omega(T_2)(K_v K_p) + K_v K_p}{j\omega^3 N T_1 T_3 + \omega^2 N T_1} \quad (10)$$

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	T <sub>1</sub>	R <sub>1</sub> ENTER	G <sub>Jω</sub> H <sub>Jω</sub> ∠θ (e/en)
			C <sub>1</sub> X STO 1	
	T <sub>2</sub>	C <sub>1</sub> ENTER		
		C <sub>2</sub> +		
		R <sub>2</sub> X STO 2		
	T <sub>3</sub>	R <sub>2</sub> ENTER		
		C <sub>2</sub> X STO 3		
	(K <sub>p</sub> K <sub>v</sub> )/N	K <sub>p</sub> ENTER		
		K <sub>v</sub> X		
		N = STO 5		
3	Calculate	F	(f) PRGM R/S	
			R/S	
			R/S	
4	Repeat step 3 for other values of frequency, F			





# Optimize phase-lock loops to meet your needs — or determine why you can't

The time constants of a PLL's integrator/filter are the keys to controlling a loop's performance. In the integrator/filter, you can trade off circuit parameters most easily to meet your needs. The other loop components (Figure 1) have simple, real-valued transfer functions ( $K_V$ ,  $K_P$ ,  $N$ ) that can't be changed as easily. But the integrator/filter's transfer function ( $F_S$ ), detailed in Figure 1c is the source of the high-order complex function in the following equation for open-loop gain:

$$G(j\omega)H(j\omega) = \frac{K_V K_P}{N T_1 \omega^2} \left[ \frac{-j\omega T_2 - 1}{j\omega T_3 + 1} \right] \quad (1)$$

where

$T_1, T_2, T_3$  = time constants defined in Figure 1c, seconds

$K_P$  = phase-detector gain constant, volts/radian

$K_V$  = voltage-controlled-oscillator (VCO) sensitivity, radians/second/volt

$N$  = frequency divisor

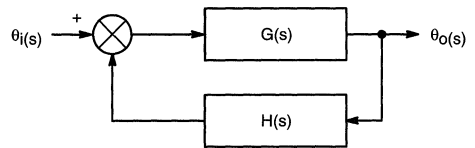
$\omega$  =  $(2\pi f)$  frequency, radians

Usually,  $K_P$ ,  $K_V$  and  $N$  are given, but you can choose  $T_1$ ,  $T_2$  and  $T_3$  to give you the loop performance you want. Generally, of course, you want the loop to be stable, to attenuate the reference frequency and to reduce VCO noise. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

A damping factor to control stability as in simpler second-order loops can't be readily defined in the third-order loop of Figure 1. Instead, the phase margin — the difference between  $180^\circ$  and the phase of the open-loop transfer function, where the gain is one — becomes the criterion for stability. Figure 2 is a typical open-loop response curve showing both amplitude and phase response, and the phase margin.

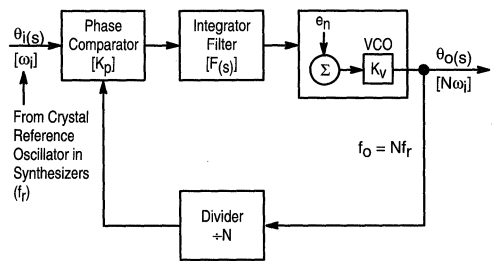
*In ED No. 10, May 10, 1978, p. 120, A. B. Przedpelski advised: "Analyze, don't estimate, phase-lock-loop performance." He showed how to calculate the performance of a given type-2, third-order PLL system with a 48-step program for an HP-25 programmable calculator. This article will show you how to optimize such a PLL to your requirements. But you will discover that you may not be able to get all requirements simultaneously. Compromises may be necessary.*

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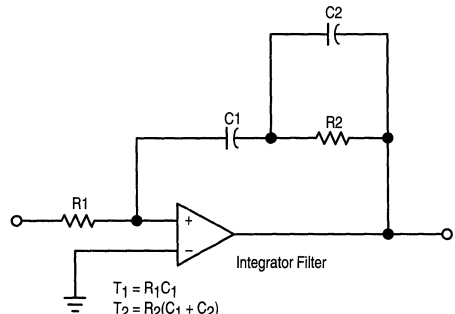


$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{G(s)}{1 + G(s)H(s)}$$

(A)



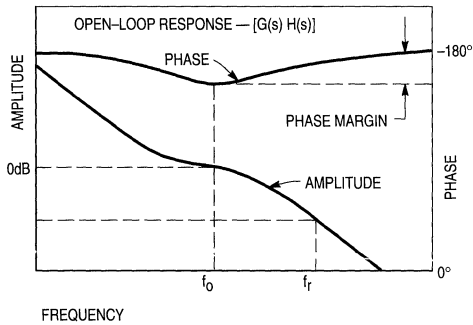
(B)



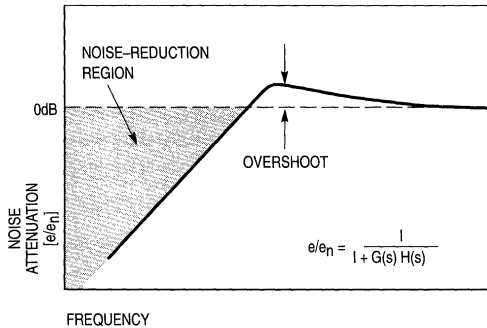
$$\begin{aligned} T_1 &= R_1 C_1 \\ T_2 &= R_2 (C_1 + C_2) \\ T_3 &= R_2 C_2 \end{aligned}$$

(C)

**Figure 1. A phase-lock loop (a) with two integrators (b) is classified type 2. And the order — third, in this case — is established by the characteristics of the integrator/filter (c). Time constants  $T_1$ ,  $T_2$ , and  $T_3$  determine the integrator/filter's detailed performance.**



**Figure 2.** This open-loop gain/phase plot shows a typical phase displacement from  $-180^\circ$ . When the frequency,  $f_0$ , which corresponds to 0dB gain, is made to align with the maximum phase displacement, calculating  $T_1$ ,  $T_2$  and  $T_3$  is simplified.



**Figure 3.** Increase  $f_0$  and you increase the noise-reduction region — the shaded area bounded by the 0dB line and the noise-attenuation curve.

The asymptotic slope of the amplitude curve is fixed at 40dB per octave by the loop's integrator/filter and VCO. The phase delay would be constant at  $-180^\circ$ , except for the phase lead introduced at the middle frequencies by the transfer function  $F(s)$ . This phase lead provides the phase margin that ensures loop stability.

#### 45° — a good compromise

The phase margin should be between  $30^\circ$  and  $70^\circ$  for most applications. The larger the phase margin, the more stable the loop. But a large phase margin not only slows the response, it also increases output sidebands and reduces the loop's VCO-noise suppression capability. Thus, a phase margin of about  $45^\circ$  is a good compromise between desired stability and the other generally undesired effects.

Ideally, a phase comparator provides an error signal that is proportional to the phase difference between its two inputs, and nothing else. But in practice, some of the reference frequency,  $f_r$ , always leak through the comparator, which frequency modulates the output signal to produce undesirable sideband frequencies. Shifting the open-loop gain-amplitude curve of  $G(j\omega) H(j\omega)$  Figure 2 to the left would attenuate  $f_r$  and the sidebands. But such a shift also would weaken the circuit's VCO-noise suppression capability.

A typical VCO noise-reduction plot is shown in Figure 3. Noise attenuates in the region that lies to the left of the curve and below the 0dB line (shown cross-hatched). The unity-gain frequency,  $f_0$ , defines the noise reduction: It's directly proportional to  $f_0$ . Clearly, then, shifting the  $G(j\omega) H(j\omega)$  curve to the right by increasing  $f_0$  will also increase the VCO noise-reduction region — which is opposite the requirement for reducing the sidebands. Thus, as so often happens, you must compromise. Locate the point of minimum phase shift (inflection point of the phase response, Figure 2) exactly at  $f_0$ , the unity-gain value.

#### The inflection point is strategic

Locating  $f_0$  at the phase inflection point is strategically valuable, because it will help solve for the value of  $T_1$ . But first you must determine  $T_3$ . Accordingly, from Equation 1 the phase margin,  $\phi$ , is

$$\phi = \tan^{-1} \omega T_2 - \tan^{-1} \omega T_3 + 180^\circ. \quad (2)$$

Differentiate  $\phi$  with respect to  $\omega$  and set the result equal to zero to locate  $\omega_0$ , and the result is

$$\frac{d\phi}{d\omega} = \frac{T_2}{1 + (\omega T_2)^2} - \frac{T_3}{1 + (\omega T_3)^2} = 0 \quad (3)$$

Solving Equation 3 then gives you

$$\omega_0 = \frac{1}{\sqrt{T_2 T_3}}. \quad (4)$$

And substituting Equation 4 into Equation 2 gives you

$$\tan \phi = \frac{T_2 - T_3}{2\sqrt{T_2 T_3}}. \quad (5)$$

Finally, plug Equation 4 into Equation 5 and re-arrange to get

$$T_3 = \frac{\sec \phi - \tan \phi}{\omega_0}. \quad (6)$$

Then re-arrange Equation 5 to get

$$T_2 = \frac{1}{\omega_0^2 T_3}. \quad (7)$$

Since you want the gain to be one at the phase-inflection point, solve for  $T_1$  in Equation 1 with  $G(j\omega) H(j\omega) = 1$ ; as a result,

$$T_1 = \frac{K_p K_v}{N \omega^2} \left[ \frac{j\omega T_2 - 1}{j\omega T_3 + 1} \right] \quad (8)$$

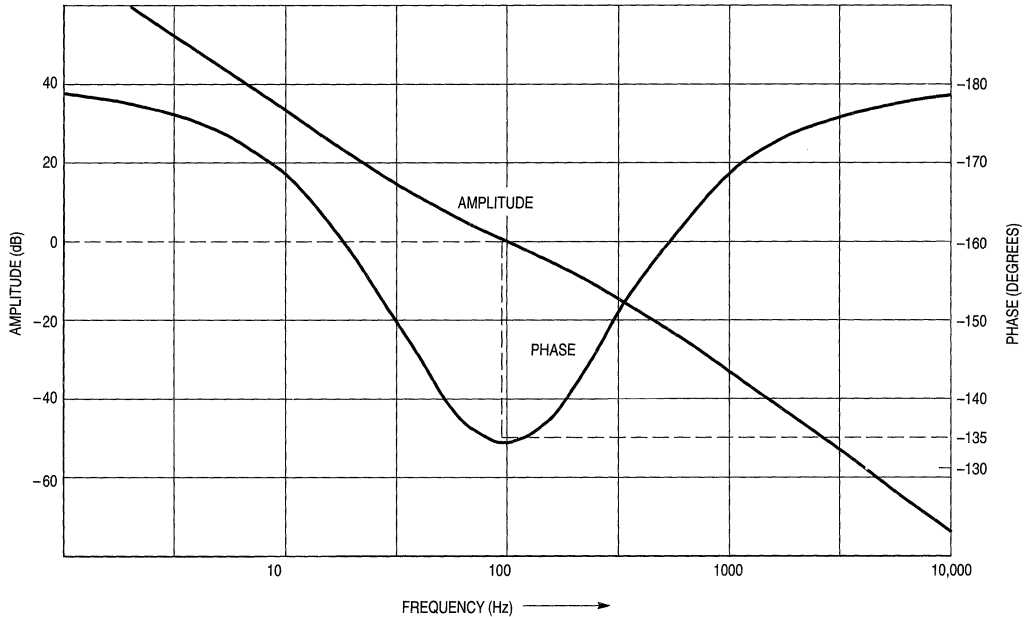


Figure 4. This plot of a PLL's open-loop transfer function confirms the design-parameter choices — a 45° phase margin at an  $f_0$  of 100Hz and unity gain. The loop is stable, but some adjustments may be desirable.

#### The 41 steps

The program in the table solves Equations 6, 7 and 8 in 41 steps with an HP-25 programmable calculator. Of course, the program can be adapted to other programmable calculators.

To illustrate the program's procedure, consider a PLL that must produce an output of 16.95MHz from a 5kHz reference,  $f_r$ . The phase comparator, VCO and divider transfer functions are as follows:

$$\begin{aligned} K_D &= 0.19\text{V/rad} \\ K_V &= 10.6 \times 10^6 \text{ rad/s/V} \\ N &= 3390 \end{aligned}$$

For stability, start with a phase margin of 45° and an  $f_0$  of about 1/50 of  $f_r$ . Thus, with

$$\phi = 45^\circ$$

and

$$\begin{aligned} f_0 &= 5000/50 \\ &= 100\text{Hz}, \end{aligned}$$

calculate  $T_1$ ,  $T_2$  and  $T_3$  with the program: You get

$$\begin{aligned} T_1 &= 3.63 \times 10^{-3}\text{s} \\ T_2 &= 3.84 \times 10^{-3}\text{s} \\ T_3 &= 6.59 \times 10^{-4}\text{s} \end{aligned}$$

But with those time constants you would need components with nonstandard values. However, if you select standard capacitors and resistors as follows:

$$\begin{aligned} C_1 &= 0.33\mu\text{F}, & R_1 &= 12\text{k}\Omega \\ C_2 &= 0.068\mu\text{F}, & R_2 &= 10\text{k}\Omega \end{aligned}$$

you get the following time constants:

$$\begin{aligned} T_1 &= 3.96 \times 10^{-3}\text{s} \\ T_2 &= 3.98 \times 10^{-3}\text{s} \\ T_3 &= 6.8 \times 10^{-4}\text{s} \end{aligned}$$

which are close enough for a first try.

#### Verifying the results

To verify the results, the open-loop transfer function,  $G(j\omega)$ ,  $H(j\omega)$ , and noise response,  $e/e_n$ , were calculated with the program provided in the previous article and plotted in Figure 4 and Figure 5. The curves confirm that the design is stable with a maximum phase margin of 45° at a frequency

Display		Key Entry	Remarks	Registers
Line	Code			
00				R <sub>0</sub>
01	2407	RCL7		
02	1406	(f) tan		
03	32	CHS		R <sub>1</sub>
04	2407	RCL7		
05	1405	(f) cos		
06	1522	(g) 1/x		R <sub>2</sub>
07	51	+		
08	2406	RCL6		R <sub>3</sub>
09	1573	(g) π		
10	61	x		
11	02	2		R <sub>4</sub>
12	61	x		
13	2304	STO4		
14	71	+		
15	2303	STO3	3	R <sub>5</sub> $\frac{K_p K_v}{N}$
16	74	R/S		
17	2404	RCL4		R <sub>6</sub> f <sub>0</sub>
18	1502	(g) x <sup>2</sup>		
19	61	x		
20	1522	(g) 1/x		
21	2302	STO2	T <sub>2</sub>	R <sub>7</sub> φ
22	74	R/S		
23	2404	RCL4		
24	61	x		
25	01	1		
26	1509	(g) → P		
27	2403	RCL3		
28	2404	RCL4		
29	61	x		
30	01	1		
31	1509	(g) → P		
32	21	x ≙ y		
33	22	R↓		
34	71	+		
35	2404	RCL4		
36	1502	(g) x <sup>2</sup>		
37	71	+		
38	2405	RCL5		
39	61	x		
40	2301	STO1	T <sub>1</sub>	
41	1300	GTO 00		

Step	Instructions	Input Data/Units	Keys			Output Data/Units
1	Enter program					
2	Store	f <sub>0</sub>	STO	6		
		φ	STO	7		
		K <sub>p</sub>	ENTER			
		K <sub>v</sub>	X			
		N	:	STO	5	
3	Calculate		(f)	PRGM	R/S	T <sub>3</sub>
			R/S			T <sub>2</sub>
			R/S			T <sub>1</sub>
3	Recall (if desired)		RCL	1		T <sub>1</sub>
			RCL	2		T <sub>2</sub>
			RCL	3		T <sub>3</sub>
			RCL	4		o

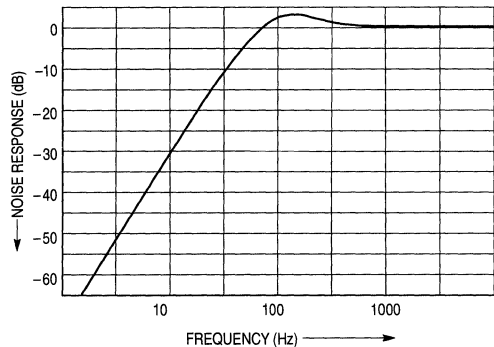


Figure 5. The noise response calculation corresponding to Figure 4 shows that VCO noise is attenuated below about 70Hz.

where the open-loop gain is about unity. And the VCO noise-reduction curve shows a moderate 3.2dB overshoot with noise frequencies below about 70Hz in the attenuation region.

Still, adjustments may be desired. For instance, if you want more reference-frequency ( $f_r$ ) attenuation, the  $G(j\omega) H(j\omega)$  curve can be shifted to the left. Move  $f_0$  one decade (to about 10Hz) and you'll increase the  $f_r$  attenuation by 40dB. Or, if noise frequencies above 70Hz are bothersome, you can shift the  $G(j\omega) H(j\omega)$  curve to the right by increasing  $f_0$ .

If you still aren't satisfied, you can change the phase margin.

Reduce the margin and you improve both  $f_r$  and VCO-noise attenuation — but then you loose some stability. ■■

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# Suppress phase-lock-loop sidebands without introducing instability

## Phase-lock-loops: Part Three

The first two parts of this series showed how to analyze and then optimize type-2, third-order PLL systems and provided simple calculator programs for an HP-25 to do the otherwise tedious computations.<sup>1,2</sup> This article takes you a step further and shows how to suppress sidebands, especially undesired when the PLL is used in frequency-synthesis systems.

Frequency synthesis, a major application of the phase-lock loop (PLL), always involves PLL-performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and voltage-controlled oscillator noise, and at the same time suppressing reference-frequency sidebands that can pass through wide bandwidths (Figure 1).

Fortunately, reference frequency is considerably above the required loop bandwidth in most cases, which alleviates the sideband problem to some extent. But for heavy suppression of undesired sidebands, extra filtering is necessary. However, it must be done carefully so as not to introduce loop instability. Three filtering circuits, none of which reduce bandwidth or VCO-noise attenuation can help solve the problem. In fact, an active LP-filtering technique, the most versatile and efficient of the three, is programmed on an HP-25 to speed the design.

All methods assume the the PLL, a type-2 third-order loop,<sup>1</sup> meets all requirements<sup>2</sup> except adequate reference-frequency sideband suppression. The three approaches include RC, active-notch and active-LP filtering. The PLL's phase margin serves as a measure of loop stability, since the damping-factor concept isn't applicable to third-order loops:<sup>2</sup> phase margins between 30° and 45° are minimum criteria for stable operation. And the filter's action in reducing the feedforward gain,  $G(j\omega)$ , at the sideband frequencies is the criterion for the suppression effectiveness.

Since  $H(j\omega)$  is equal to  $1/N$ , a constant, then the open-loop gain,  $G(j\omega)H(j\omega)$  in Equation 1, can be used as a measure of this sideband-suppression effectiveness:

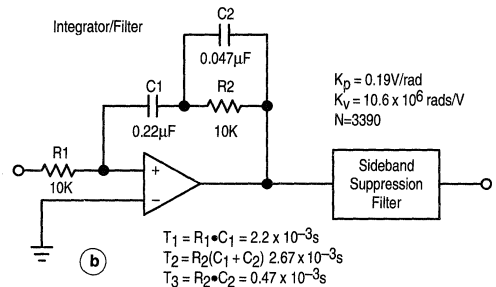
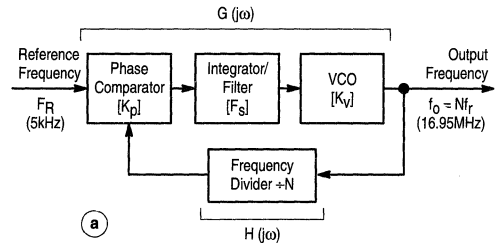
$$G(j\omega)H(j\omega) = \frac{K_V K_P}{N T_1 \omega^2} \frac{[-j\omega T_2 - 1]}{[j\omega T_3 + 1]}, \quad (1)$$

$K_P$  = gain constant of the phase detector,

$K_V$  = VCO sensitivity,

$N$  = counter divide ratio,

$T_1, T_2, T_3$  = integrator/filter time constants.



NOTE: Similar to example in Phase-lock Loops: Part Two (ED 19, Sept. 13, 1978, p1 134) only time constants  $T_1, T_2$  and  $T_3$  have been changed, to improve margin and over-all performance.

**Figure 1. A phase-lock loop frequency synthesizer** (a) generates 16.95MHz from a crystal-oscillator reference frequency of 5kHz. To help suppress sidebands, a sideband-suppression filter is added in tandem with the output of the loop's original integrator/filter circuit (b).

**Table 1. Filter suppression/phase margin tradeoffs**

Circuit	Phase Margin	Phase Margin Deterioration	First Sideband Reduction	Second Sideband Reduction
Original	44°	—	—	—
RC low-pass RC = 3 x 10 <sup>-4</sup>	32	12°	20dB	26dB
Notch filter Q = 10 Q = 1 Q = 0.1	44	0	∞*	0
	43	1	∞*	1.5
	31	13	∞*	16.5
Second-order active d = 0.707 d = 0.1	34	10	28	40
	42	2	28	40

\*Theoretical — actual value about 40dB

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**Table 2. Third order type-2 PLL with two-pole low-pass filter**

Display		Key Entry	Remarks	Registers
Line	Code			
00				R <sub>0</sub> ω <sub>0</sub>
01	2400	RCL0		
02	1502	(g) x <sup>2</sup>		
03	2407	RCL7		R <sub>1</sub> T <sub>1</sub>
04	1502	(g) x <sup>2</sup>		
05	41	—		
06	2304	STO4		R <sub>2</sub> T <sub>2</sub>
07	2403	RCL3		
08	61	x		
09	2406	RCL6		R <sub>3</sub> T <sub>3</sub>
10	2400	RCL0		
11	61	x		
12	51	+		R <sub>4</sub>
13	2407	RCL7		
14	61	x		
15	2404	RCL4		R <sub>5</sub> K <sub>p</sub> K <sub>v</sub>
16	2406	RCL6		N
17	2403	RCL3		
18	61	x		
19	2400	RCL0		R <sub>6</sub> 2d
20	61	x		
21	2407	RCL7		R <sub>7</sub> ω
22	1502	(g) x <sup>2</sup>		
23	61	x		
24	41	—		
25	32	CHS		
26	1509	(g) → P		
27	21	x↑y		
28	2407	RCL7		
29	2402	RCL2		
30	61	x		
31	32	CHS		
32	01	1	∠° Phase-margin	
33	32	CHS		
34	1500	(g) → P		
35	22	R↓		
36	51	+		
37	74	R/S		
38	22	R↓		
39	71	+		
40	2405	RCL5		
41	61	x		
42	2401	RCL1		
43	71	+		
44	2407	RCL7		
45	1502	(g) x <sup>2</sup>		
46	71	+		
47	2400	RCL0		
48	1502	(g) x <sup>2</sup>		
49	61	x	G <sub>S</sub> H <sub>S</sub>	

**Simple but limited**

The simplest approach adds in series with the Integrator/Filter an RC low-pass section (Figure 2a), whose cutoff frequency is larger than the upper end of the loop's bandwidth. For illustration, let the value of RC be 3 x 10<sup>-4</sup>s for the frequency-synthesizer example outlined in Figure 1. (A larger value would reduce the sidebands more, but would also decrease the phase margin too much.) With a value of 3 x 10<sup>-4</sup>s, the phase margin remains within a "safe" 30°-to-45°.

Step	Instructions	Input Data/Units	Keys		Output Data/Units
1	Enter program				
2	Store	ω <sub>0</sub>	STO	0	
		T <sub>1</sub>	STO	1	
		T <sub>2</sub>	STO	2	
		T <sub>3</sub>	STO	3	
		K <sub>v</sub>	ENTER		
		K <sub>p</sub>	x		
		N	+ STO	5	
		d	ENTER	2	x
			STO	6	
3	Enter		STO	7	
4	Calculate		(f)	PRGM	R/S ∠°Phase margin
5	Repeat step 3 for other values of frequency, F		R/S		G(s)H(s)

The open-loop transfer function then becomes:

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2} \left[ \frac{-j\omega T_2 - 1}{j\omega(T_3 + T_4) + 1 + \omega^2 T_3 T_4} \right], \quad (2)$$

where T<sub>4</sub> is the additional RC time constant.

Solving Equation 1 at frequencies of 5 and 10kHz shows that the first sideband (at 5kHz) is reduced a respectable 20dB and the second sideband (at 10kHz) even more to 26dB. But the phase margin is also reduced to a marginal 32° (Table 1).

However, an active RC notch filter<sup>3</sup> (Figure 2) gives much more attenuation at the first sideband (5kHz) and is more flexible in some applications. Its gain is

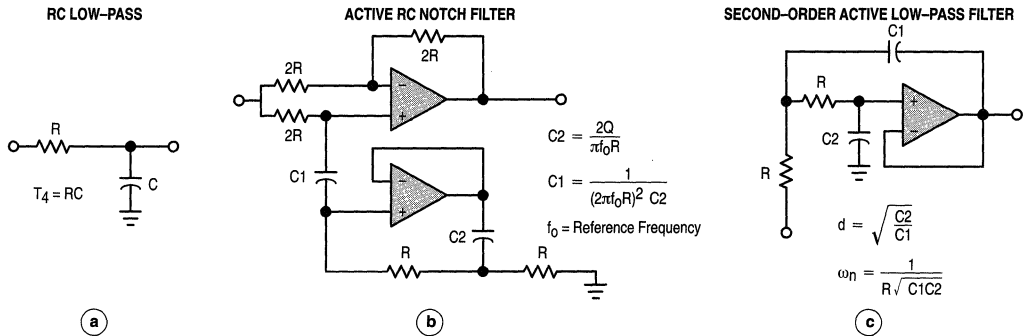
$$A(j\omega) = \frac{1}{j\omega \left[ \frac{\omega_0}{Q(\omega^2 - \omega_0^2)} \right] + 1}, \quad (3)$$

where ω<sub>0</sub> = the notch frequency (2πf<sub>0</sub>),  
Q = the circuit Q.

The open-loop transfer function, the product of Equations 1 and 3, is

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1\omega^2} \times \left[ \frac{-j\omega T_2 - 1}{j\omega \left( T_3 - \frac{\omega_0}{Q(\omega^2 - \omega_0^2)} \right) + \omega^2 T_3 \left( \frac{\omega_0}{Q(\omega^2 - \omega_0^2)} \right) + 1} \right], \quad (4)$$

Although the notch frequency ω<sub>0</sub> must be fixed at the reference frequency, the value of Q can vary. Theoretically, the reference frequency receives infinite attenuation. Actually, only about 40dB can be realized, even under ideal conditions.



**Figure 2.** Many filter configurations can be used to suppress sidebands. The simplest is a low-pass RC circuit (a). Somewhat more flexible is an active RC notch filter (b). But of all filters, a second-order active low-pass filter (c) is most versatile, since two of its parameters are independently adjustable.

Evaluation of Equation 4 for Q's of 10, 1 and 0.1 shows that high Q values produce negligible phase-margin deterioration, but attenuation of the second harmonic of the reference frequency is small or zero (Table 1). At a Q of 0.1, however, the second harmonic is reduced 16.5dB, but then the phase margin suffers.

Most versatile, however, is a second-order, active, low-pass filter with variable damping (Figure 2c). Its gain (with "s" functions of its more familiar form replaced by  $j\omega$ ) is:<sup>3</sup>

$$A(j\omega) = \frac{\omega_n^2}{-\omega^2 + 2dj\omega\omega_n + \omega_n^2}, \quad (5)$$

where  $\omega_n$  = the filter's natural pole frequency,  
 $d$  = the filter's damping factor.

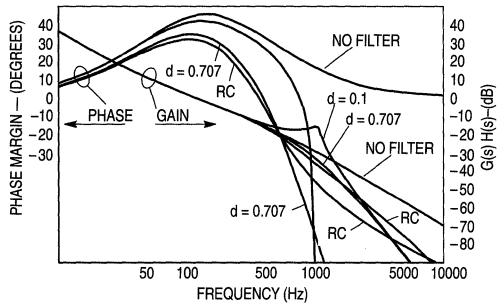
This time, multiplying Equations 1 and 5, the overall open-loop transfer function becomes

$$G(j\omega)H(j\omega) = \frac{K_v K_p}{NT_1 \omega^2} \times \left[ \frac{-j\omega T_2 - 1}{j\omega[2d\omega_n + T_3(\omega_n^2 - \omega)] + [\omega_n^2 - \omega^2 - 2dT_3\omega_n\omega^2]} \right], \quad (6)$$

If  $\omega_n$  is chosen to be 6283 ( $2\pi \times 1000$ ) at damping factors of 0.707 (Butterworth response) and 0.1 (16dB peak Chebyshev), Equation 6 gives the same sideband attenuation for both damping factors, but the high-ripple Chebyshev deteriorates the phase margin least (Table 1 and Figure 3).

Since both the pole frequency and the damping factor can be varied in Equation 5, the circuit it represents is most versatile. Therefore, Equation 6 is programmed for easy solution on an HP-25 (Table 2) in 49 steps. However, for easier stability evaluation, the program solves directly for the phase margin — the difference between 180° and the open-loop transfer-function angle — rather than the phase

angle itself.



**Figure 3.** A plot of open-loop gain and phase response of the system in Figure 1 compares sideband suppression at 5 and 10kHz without and with a filter with that of a simple RC and an active, second-order filter.

Clearly, the simple RC circuit is least efficient. It gives the least sideband attenuation and the largest phase-margin deterioration. The notch filter, although theoretically capable of very high attenuation of the sidebands only with very small phase-margin deterioration, generally requires component tolerances too critical for other than some special applications. The more complex, active, second-order low-pass filter, however, can be tailored to most applications — illustrating an often observed design phenomenon: the more complex the circuit the better the performance. Of course, then, more complex filter circuits than those used in the examples may offer even better solutions to sideband reduction. ■ ■

**References**

- 1 Przedpelski, A. B., "Analyze, Don't Estimate, Phase-lock-loop Performance of Type-2, Third-order Systems," *Electronic Design*, May 10, 1978, p. 120.
- 2 Przedpelski, A. B., "Optimize Phase-lock Loops to Meet Your Needs," *Electronic Design*, Sept. 13, 1978, p. 134.
- 3 Stout, D. P., and Kaufman, M., *Operational Amplifier Circuit Design*, McGraw-Hill, NY, 1976.



Calculate the noise spectral density and short-term frequency stability in a PLL with a programmable calculator, and vary the parameters to trade off the noise/functional performance requirements.

## Programmable calculator computes PLL noise, stability

This article is the fourth by the author on phase locked loops, starting with "Analyze, Don't Estimate, Phase-Lock-Loop Performance" (May 10, 1978, p. 120); then "Optimize Phase-Lock-Loops to Meet Your Needs" (Sept. 13, 1978, p. 134); followed by "Suppress Phase-Lock-Loop Sidebands without Introducing Instability" (Sept. 13, 1979, p. 142).

The circuit constants of a phase-lock loop can be optimized not only for performance requirements (acquisition time, sideband levels, step response, and stability, among others), but also for noise output and the resulting short-term (or "instantaneous") frequency stability. Because most other frequency generation methods lack this versatile performance and noise and stability control, phase-lock loops (PLLs) are preferable for frequency synthesis. Moreover, a programmable HP-19C (or 21C) calculator with the proper program makes the design tradeoffs between noise effects and functional performance requirements relatively easy to determine.

A properly designed frequency synthesizer derived from a PLL (Figure 1, top) will offer a high degree of flexibility and long-term frequency stability. In a PLL, the frequency of the stable reference oscillator (say, a quartz-crystal circuit) can be multiplied by a precisely controlled factor over a very wide range. Although the PLL may seem more complicated than the conventional so-called frequency-multiplier circuit (Figure 1, bottom), in practice, the PLL is more efficient, more compact, and considerably wider in bandwidth. All the advantages increase as the multiplication factor increases.

In most PLL frequency synthesizers, the primary concern is the functional performance—a problem that has been treated extensively.<sup>1</sup> Even the theoretical aspects of phase noise in low-noise signal sources have been extensively covered.<sup>2,3,4</sup> However, specific methods for calculating the noise and short term frequency stability and details of the tradeoffs are generally not available, except for some recent work by the National Bureau of Standards on low noise signal sources.<sup>5,6,7</sup>

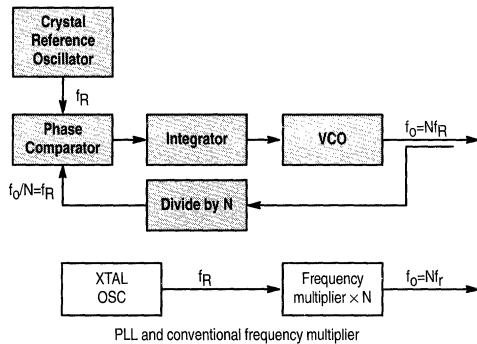


Figure 1. Although the PLL frequency multiplier (top) looks more complex than the conventional multiplier (bottom), it is in fact more compact and more flexible, and can handle a much wider frequency range.

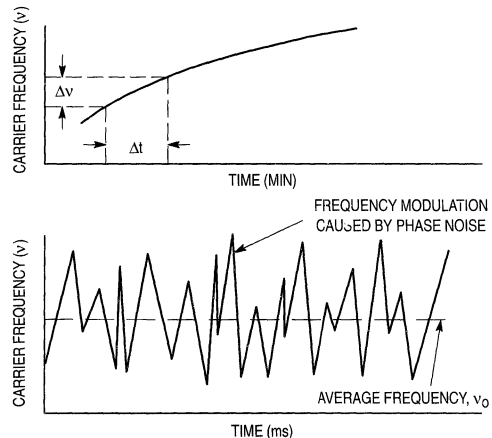


Figure 2. Short-term frequency stability can be far worse (bottom) than the long-term average of a PLL system (top).

Andrzej B. Przedpelski, Vice President of Development, A.R.F. Products Inc., 2559 75th St., Boulder, CO 80301.

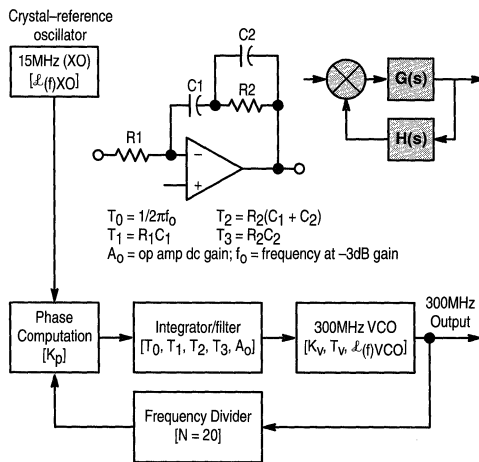
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Short-term (or “instantaneously” sampled) frequency stability, in the millisecond range, is particularly important for accuracy in position-finding applications, as in LORAN navigation and various radar and sonar Doppler systems. Even though frequency drift over a short time generally is less than the average long-term frequency drift, instantaneously measured samples show much wider variations in the frequency swings caused by phase noise in the signal source (Figure 2).

The overall phase-noise, or spectral-density output,  $S_{\phi(\omega)0}$ , of a PLL<sup>8</sup> is found by

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO} \left| \frac{1}{1 + G(\omega)H(\omega)} \right|^2 + S_{\phi(\omega)REF} \left| \frac{G(\omega)}{1 + G(\omega)H(\omega)} \right|^2,$$

where  $S_{\phi(\omega)VCO}$  is the open-loop spectral density of phase fluctuations in the PLL's voltage-controlled oscillator (VCO) and  $S_{\phi(\omega)REF}$  is the equivalent spectral density of fluctuations in the reference oscillator. These phase fluctuations are measured in rad<sup>2</sup>/Hz, but generally plotted in dBc, which is 10 log<sub>10</sub> S<sub>φ(ω)</sub>. More commonly, however, vendor-supplied phase-noise data, designated  $\mathcal{L}(\omega)$ , and also measured in dBc, are for single-sideband noise. (The dBc designation is defined as 10 log<sub>10</sub> of the ratio between the output from a spectrum analyzer with a 1-Hz bandwidth and the signal's carrier level.)



**Figure 3.** For a fifth-order PLL, four of the time constants are determined by the integrator/filter circuit, and the fifth is determined by the VCO.

Accordingly,

$$\mathcal{L}(\omega) = 10 \log_{10} (1/2)S_{\phi(\omega)} \text{ (per rad}^2\text{)},$$

assuming that

$$\mathcal{L}(-\omega) = \mathcal{L}(\omega).$$

Therefore, to convert  $\mathcal{L}(\omega)$  data to “straight”  $S_{\phi(\omega)}$  data, add 3dB to the  $\mathcal{L}(\omega)$  data and take the antilog.

An HP-19C program (see “Noise in a 5th-order PLL”) calculates this single-sideband noise, where  $G(\omega)H(\omega)$  is the open-loop gain of the PLL<sup>1</sup>. The feedback path,  $H(\omega)$ , is simply 1/N; and  $G(\omega)$  equals

$$\frac{(K_p K_v / \omega T_1) (j\omega T_2 + 1)}{j \left[ \omega^2 (\omega^2 \frac{T_0}{A_0} T_V T_3 - T_3 - T_V) + \frac{1}{A_0 T_1} \right] + \omega (\omega^2 T_V T_3 - 1)}$$

Optimized for functional performance, the following circuit constants are used for a typical PLL (Figure 3):

- $A_0 = 320,000$
- $T_0 = 7.96 \times 10^{-4} \text{ s}$
- $T_V = 1.59 \times 10^{-7} \text{ s}$
- $T_1 = 2.408 \times 10^{-5} \text{ s}$
- $T_2 = 2.491 \times 10^{-6} \text{ s}$
- $T_3 = 4.700 \times 10^{-7} \text{ s}$
- $K_p = 314 \times 10^6 \text{ V/rad}$
- $K_v = 0.16 \text{ rad/V}$
- $N = 20$

The single-sideband phase noise, when calculated by the program for a range of so-called Fourier frequencies (offsets from a carrier,  $f = \omega/2\pi$ ), can be plotted as in Figure 4 (dotted line). Although this output phase noise can be reduced by varying circuit constants to increase the loop's bandwidth, proceed with caution, because other desirable operating characteristics (such as circuit stability or speed of response) could be compromised. The program, however, offers an easy way to determine how systematic changes in the parameters affect noise.

#### Oscillator noise should be low

In addition to the calculated PLL noise, Figure 4 shows a plot of the SSB-noise characteristics of the circuit's VCO and crystal-reference oscillator. The oscillators are the main source of phase noise in a PLL. The information for plotting their noise can be obtained from the manufacturers of the oscillators, or from measurements made by the user.

Where noise reduction is of prime importance select oscillators that generate minimum noise and have noise spectral densities that complement each other (as in Figure 5). The point at which the two curves cross is called the crossover frequency ( $f_c$ ). This frequency is an important parameter for optimizing a PLL's noise characteristics.

In Figure 5, the VCO noise-distribution plot is divided into three characteristic regions. High-quality oscillators generally exhibit this spectral-density relationship. In region I,  $S_{\phi(f)}$  is typically proportional to  $1/f^3$ , so-called flicker-frequency noise; in region II,  $S_{\phi(f)}$  is proportional to  $1/f^2$ , so-called white-frequency noise; and in region III,  $S_{\phi(f)}$  is constant, so-called white-phase noise. Beyond region III, the bandwidth limitation of the circuit attenuates the noise to negligible levels.

Noise in 5th order PLL

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	T <sub>0</sub> T <sub>1</sub> T <sub>2</sub> T <sub>3</sub> T <sub>v</sub> K <sub>p</sub> K <sub>vo</sub> N A <sub>o</sub> 180 10	STO 0 STO 1 STO 2 STO 3 STO 4 STO 5 STO 6 STO 7 STO 8 STO 9 STO .5	
3	Calculate	f	GSB 0	
4	Repeat step 3 for other Fourier frequencies	S <sub>href</sub> S <sub>vto</sub>	R/S R/S	S <sub>po</sub>

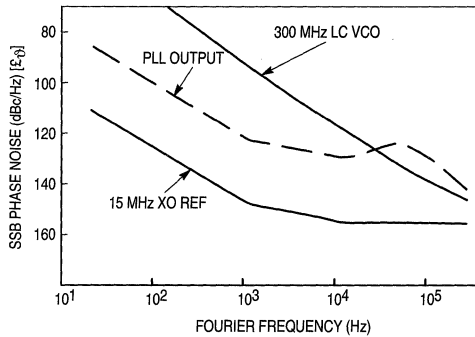
NOTE: Enter S<sub>href</sub> and S<sub>vto</sub> in dB. S<sub>po</sub> answer is in dB.



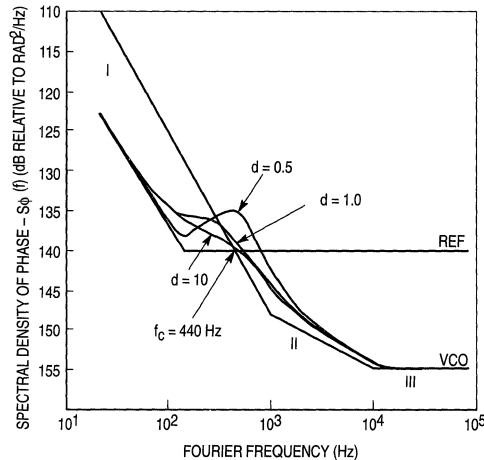
Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	050	RCL 9	55 09
002	PRx	65	051	—	31
003	(g) DEG	25 24	052	STO .1	45 .1
004	(g) π	25 63	053	R↓	12
005	x	51	054	+	61
006	2	02	055	RCL 5	55 05
007	x	51	056	x	51
008	STO .0	45 .0	057	RCL 6	55 06
009	(g) x <sup>2</sup>	25 53	058	x	51
010	RCL 0	55 00	059	RCL 7	55 07
011	x	51	060	+	61
012	RCL 8	55 08	061	RCL 1	55 01
013	+	61	062	+	61
014	RCL 4	55 04	063	RCL .0	55 .0
015	x	51	064	+	61
016	RCL 3	55 03	065	STO .2	45 .2
017	x	51	066	RCL .1	55 .1
018	RCL 3	55 03	067	x ↔ y	11
019	—	31	068	(f) → R	16 34
020	RCL 4	55 04	069	1	01
021	—	31	070	+	41
022	RCL .0	55 .0	071	(g) → P	25 34
023	(g) x <sup>2</sup>	25 53	072	(g) 1/x	25 64
024	x	51	073	STO .3	45 .3
025	RCL 8	55 08	074	RCL .2	55 .2
026	RCL 1	55 01	075	RCL 7	55 07
027	x	51	076	x	51
028	(g) 1/x	25 64	077	x	51
029	+	41	078	STO .4	45 .4
030	RCL .0	55 .0	079	(g) x <sup>2</sup>	25 53
031	(g) x <sup>2</sup>	25 53	080	R/S	64
032	RCL 3	55 03	081	RCL .5	55 .5
033	x	51	082	+	61
034	RCL 4	55 04	083	(g) 10 <sup>x</sup>	25 33
035	x	51	084	x	51
036	1	01	085	RCL .3	55 .3
037	—	31	086	(g) x <sup>2</sup>	25 53
038	RCL .0	55 .0	087	R/S	64
039	x	51	088	RCL .5	55 .5
040	CHS	22	089	+	61
041	(g) → P	25 34	090	(g) 10 <sup>x</sup>	25 33
042	x ↔ y	11	091	x	51
043	RCL .2	55 02	092	+	41
044	RCL .0	55 .0	093	(f) log	16 33
045	x	51	094	RCL .5	55 .5
046	1	01	095	x	51
047	(g) → P	25 34	096	PRx	65
048	R↓	12	097	(g) SPC	25 65
049	+	41	098	(g) RTN	25 13

REGISTERS

0	T <sub>0</sub>	1	T <sub>1</sub>	2	T <sub>2</sub>	3	T <sub>3</sub>	4	T <sub>v</sub>	5	K <sub>p</sub>	6	K <sub>vo</sub>	7	N	8	A <sub>o</sub>	9	180
S0	S1	S2	S3	S4	S5	S6	S7	S8	S9										



**Figure 4. A PLL is optimized** for performance characteristics, such as stability, response time, and sideband levels; but the noise characteristics generally fall where they may, as exemplified in this plot of a fifth-order PLL.



**Figure 5. The "optimum" PLL output-noise characteristic** is the one that coincides with the PLL's intersecting reference crystal oscillator and VCO-oscillator noise characteristics (heavy lines). A high damping-factor value (such as  $d=10$ ) makes the best correspondence with this criterion.

Region I noise stems from fluctuations in oscillator-circuit frequency-control components; region II, from thermal noise in the oscillator's gain element; and region III, from additive thermal noise from other elements of the circuit (including the gain element).

A plot of the optimum phase-noise characteristic of a PLL would coincide with the lower parts of the two oscillator curves (heavy lines in Figure 5).

The type-2, second-order PLL circuit in Figure 6 helps to illustrate how closely this condition can be approached. This circuit can be generalized by relating the integrator's time

constants ( $T_1$  and  $T_2$ ) and the VCO's and phase comparator's transfer coefficients ( $K_V$  and  $K_P$ ) with a damping factor ( $d$ ), and with the reference and VCO crossover frequency ( $f_c = \omega_c/2\pi$ ), as follows:

$$\begin{aligned} d &= (T/2) \sqrt{K_P K_V / T_1}; \quad d \gg 1 \\ T_2 &= 4d^2 / \omega_c \\ T_1 &= T_2 K_P K_V / \omega_c. \end{aligned}$$

When these circuit parameters are considered together with the circuit's open-loop gain (note:  $H(\omega) = 1$ ),

$$G(j\omega)H(j\omega) = \frac{K_V K_P}{T_1 \omega^2} (-j\omega T_2 - 1),$$

and substituted in the phase-noise equation for  $S_{\phi(\omega)}$  the PLL's spectral density becomes

$$S_{\phi(\omega)} = S_{\phi(\omega)} \text{VCO} \left[ \frac{1}{\left(1 - \frac{\omega_c^2}{4d^2\omega^2}\right) + \left(\frac{\omega_c}{\omega}\right)^2} \right] + S_{\phi(\omega)} \text{REF} \left[ \frac{\left(\frac{1}{2d}\right)^2 \left(\frac{\omega_c}{\omega}\right)^2 + \left(\frac{\omega_c}{\omega}\right)^2}{\left(1 - \frac{\omega_c^2}{4d^2\omega^2}\right) + \left(\frac{\omega_c}{\omega}\right)^2} \right]$$

The "Optimizing PLL Phase Noise" program, with its subroutine 0, solves this equation for any Fourier frequency ( $f = \omega/2\pi$ ). In Figure 5, solutions are shown for damping-factor values ( $d$ ) of 0.5, 1.0, and 10.

The largest damping factor ( $d = 10$ ) causes the noise curve to approach the "optimum" noise characteristic most closely—when it lies completely between the VCO/reference-oscillator lines and as closely as possible to the lower lines. To satisfy this criterion, the curve generally passes through the frequency crossover point previously mentioned. Larger damping values than 10 will provide little further improvement. In fact, a larger damping value would slow response more than it would lower the noise output. Special cases may require low damping factors — a value of 1 or even 0.5 — to get a faster response or the special noise-distribution shapes that these lower damping factors produce.

After the phase-noise characteristics (based on the  $f_c$  of the oscillators and a selected damping factor) have been calculated, a second part of the optimizing program (subroutine 1) can then be used to calculate the time constants  $T_1$  and  $T_2$  for the given  $K_P$  and  $K_V$  of a type-2 second-order PLL.

Determining a PLL's short-term frequency stability requires integration of the spectral density of the phase fluctuations to obtain the so-called Allan variance (a dimensionless measure of stability, where  $\sigma_y^2 = \Delta f/f$  in a short sample period). Thus

$$\sigma_y^2(\tau, f_h) = \frac{2}{(\tau\pi)^2} \int_0^{\tau} S_{\phi}(f) \sin^4(\pi f \tau) df,$$

Optimizing PLL phase noise

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	$f_c$ $d$ $K_p$ $K_v$	STO 2 STO 3 STO 7 STO 8	
3	Calculate phase noise	$f$ $S_{\phi_{VCO}}$ $S_{\phi_{ref}}$	GSB 0 R/S R/S	$S_{\phi_0}$
4	Repeat step 3 for other values of Fourier frequency			
5	Calculate time constants		GSB 1	T1 T2

NOTE:  $S_{\phi_{VCO}}$ ,  $S_{\phi_{ref}}$  and  $S_{\phi_0}$  in dB. Subroutine 0 must be performed before the time constants can be calculated with subroutine 1

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	038	(g) $x^2$	25 53
002	PRx	65	039	RCL 4	55 04
003	(g) $\pi$	25 63	040	+	41
004	$\times$	51	041	RCL 5	55 05
005	2	02	042	+	61
006	$\times$	51	043	R/S	64
007	(g) 1/x	25 64	044	0	01
008	RCL 2	55 02	045		00
009	(g) $\pi$	25 63	046	+	61
010	$\times$	51	047	(g) $10^x$	25 33
011	2	02	048	$\times$	51
012	$\times$	51	049	+	41
013	STO 1	45 01	050	(f) log	16 33
014	$\times$	51	051	+	01
015	(g) $x^2$	25 53	052	0	00
016	STO 4	45 04	053	$\times$	51
017	RCL 3	55 03	054	PRx	65
018	(g) $x^2$	25 53	055	(g) SPC	25 65
019	+	61	056	(g) RTN	25 13
020	4	04	057	(g) LBL 1	25 14 01
021	+	61	058	RCL 3	55 03
022	STO 6	45 06	059	(g) $x^2$	25 53
023	CHS	22	060	4	04
024	1	01	061	$\times$	51
025	+	41	062	RCL 1	55 01
026	(g) $x^2$	25 53	063	+	61
027	RCL 4	55 04	064	PRx	65
028	+	41	065	RCL 7	55 07
029	STO 5	45 05	066	$\times$	51
030	(g) 1/x	25 64	067	RCL 8	55 08
031	R/S	64	068	$\times$	51
032	1	01	069	RCL 1	55 01
033	0	00	070	+	61
034	+	61	071	PRx	65
035	(g) $10^x$	25 33	072	(g) SPC	25 65
036	$\times$	51	073	(g) RTN	25 13
037	RCL 6	55 06			

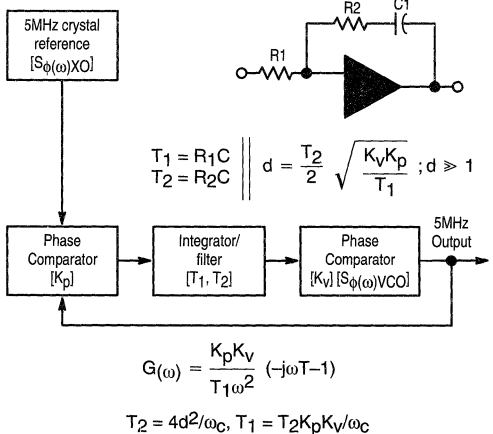
REGISTERS

0	1	2 $f_c$	3 $d$	4	5	6	7 $K_p$	8 $K_v$	9
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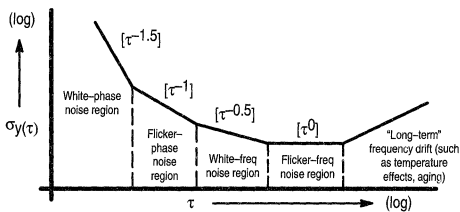
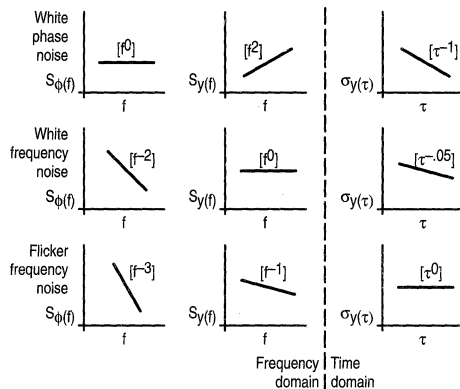
where  $\tau$  is the sampling time (in seconds),  $\nu$  is the long-term average frequency (in Hz), and  $f_h$  is the bandwidth, or maximum excursion of the offset from the carrier (the maximum Fourier frequency).

Figure 7 (top) shows the relationship between frequency or phase and the resultant short-term frequency stabilities, for several distinct types of phase or frequency noise. A typical complex signal source such as a PLL could have a combined short-term frequency stability as in Figure 7 (bottom). But such noise types generally do not obey simple integer-power curves and, therefore, pose a problem: The Allan equation does not have a closed-form solution for fractional powers, so it cannot be used directly. Nevertheless, very accurate answers can be obtained with Simpson's Rule and a programmable calculator.

Although the Allan equation requires integration over the Fourier frequency range of 0 to  $f_h$ , the low-frequency limit of 0 Hz cannot be used in a log-log Simpson's Rule integration. Fortunately, frequencies below  $(2\pi\tau f_h)^{-1}$ , where  $\tau f_h$  is the longest sampling time, do not contribute appreciably to the value of the Allan variance. The longest sampling time for short-term effects is generally 1s; therefore, for a measuring-system bandwidth of 1000Hz, just the Fourier frequencies between about 0.16 and an  $f_h$  of 1000Hz need be considered. (Since the manufacturer did not supply data below 2Hz for the reference oscillator and VCO used in Figure 5; a new oscillator with data to 0.1Hz was substituted in Figure 8, top.)



**Figure 6.** The phase-output noise in this type-2 second-order PLL can be optimized by adjusting the damping factor ( $d$ ) in relation to the oscillator-noise crossover frequency ( $f_c$ ).



**Figure 7.** The distribution of the different types of frequency and phase noise can be expressed as line segments that represent powers of frequency or time (top), and the overall distribution of a system can be shown by combining appropriate segments (bottom).

As shown in Figure 7 (bottom) and Figure 8, (top), the phase-noise curves can be approximated with straight-line segments. The segments are plotted on semilog paper with  $S_{\phi}(f)$  measured in dBc on the vertical axis. Therefore, the segments,

$$y = ax^b,$$

can be established from the end points on their phasenoise curves — where  $S_{\phi}(f_1)$  and  $S_{\phi}(f_2)$  correspond to the low-frequency ( $f_1$ ) and the high-frequency ( $f_2$ ) end points, as follows:

$$b = \frac{S_{\phi}(f_1) - S_{\phi}(f_2)}{10(\log f_1 - \log f_2)}$$

and

$$\left( \frac{S_{\phi}(f_1) - 10 \text{ b log } f_1}{10} \right).$$

$$a = 10$$

Allan variance calculations

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Key in the program			
2	Store	b α v τ	STO 7 STO .1 STO .0 STO 8	
3	Enter and start program	f <sub>1</sub> f <sub>2</sub> n	ENT ↑ ENT ↑ GSB .3	σ <sup>2</sup> y

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 7	25 14 07	044	RCL 4	55 04
002	RCL 4	55 04	045	STO + 5	45 41 05
003	x	51	046	RCL 5	55 05
004	x ↔ y	11	047	GSB 0	13 00
005	+	61	048	GSB 6	13 08
006	GTO 2	14 02	049	(g) RTN	25 13
007	(g) LBL 6	25 14 06	050	(g) LBL 5	25 14 05
008	ENT ↑	21	051	3	03
009	+	41	052	RCL 0	55 00
010	STO + 0	45 41 00	053	GTO 7	14 07
011	(g) RTN	25 13	054	(g) LBL 0	25 14 00
012	(g) LBL 3	25 14 03	055	(g) RAD	25 23
013	STO 3	45 03	056	STO 8	45 06
014	R ↓	12	057	(g) π	25 63
015	STO 2	45 02	058	x	51
016	R ↓	12	059	RCL 8	55 08
017	STO 1	45 01	060	x	51
018	GSB 0	13 00	061	(f) sin	16 42
019	STO 0	45 00	062	(g) x <sup>2</sup>	25 53
020	RCL 2	55 02	063	(g) x <sup>2</sup>	25 53
021	GSB 0	13 00	064	RCL 6	55 06
022	STO + 0	45 41 00	065	RCL 7	55 07
023	RCL 2	55 02	066	(f) y <sup>x</sup>	16 54
024	RCL 1	55 01	067	x	51
025	STO 5	45 05	068	(g) DEG	25 24
026	—	31	069	(g) RTN	25 13
027	RCL 3	55 03	070	(g) LBL 2	25 14 02
028	+	61	071	(g) π	25 63
029	STO 4	45 04	072	RCL 8	55 08
030	0	00	073	x	51
031	STO 9	45 09	074	RCL 0	55 00
032	(g) LBL 8	25 14 08	075	x	51
033	GSB 4	13 04	076	(g) x <sup>2</sup>	25 53
034	STO + 0	45 41 00	077	(g) 1/x	25 64
035	2	02	078	x	51
036	STO + 9	45 41 09	079	2	02
037	RCL 3	55 03	080	x	51
038	RCL 9	55 09	081	RCL .1	55 .1
039	(f) x = y	16 61	082	x	51
040	GTO 5	14 05	083	PRx	65
041	GSB 4	13 04	084	(g) SPC	25 65
042	GTO 8	14 08	085	(g) RTN	25 13
043	(g) LBL 4	25 14 04			

REGISTERS

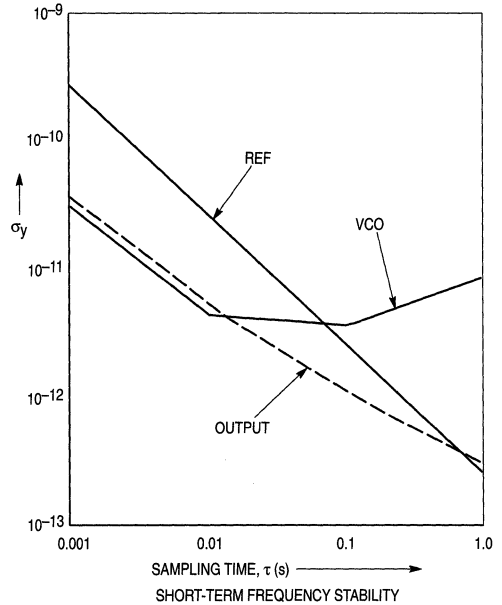
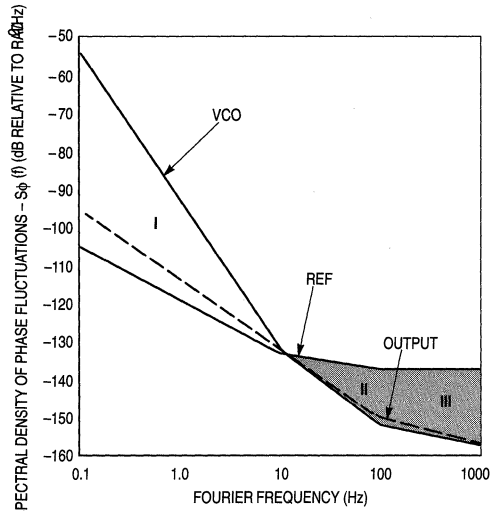
0	1	2	3	4	5	6	7	8	9
.0 v	.1 α	.2	.3	.4	.5	S6	S7 b	S8 τ	S9

With coefficients a and b established for each line segment the contributions of each segment to the overall Allan variance  $\sigma_y^2$  can be calculated with the approximate Allan equation,

$$\sigma_y^2(\tau, f) = \frac{2a}{(\tau\nu\pi)^2} \int_{f_1}^{f_2} f^b \sin^4(\pi f\tau) df,$$

by a modified Simpson's Rule program supplied by Hewlett-Packard (HP-19C/29C *Applications' Book*, 1977). The Simpson's Rule is incorporated into the complete program for an HP-19C calculator — "Allan Variance Calculations." With a, b, v, and  $\tau$  established, the only decision

Calculated short-term stability					
<b>Device</b>	<b>Segment I</b>				
Reference oscillator	$f_1 = 0.1\text{Hz}, f_2 = 10\text{Hz}$ $a = 1.26 \times 10^{-12}, b = -1.40$				
	T/n	0.001/10	0.01/10	0.1/20	1/100
	$\sigma_y^2$	$1.10 \times 10^{-27}$	$1.05 \times 10^{-25}$	$4.80 \times 10^{-25}$	$1.76 \times 10^{-26}$
Voltage-controlled oscillator	$f_1 = 0.1\text{Hz}, f_2 = 10\text{Hz}$ $a = 5.01 \times 10^{-10}, b = -3.90$				
	T/n	0.001/10	0.01/10	0.1/20	1/100
	$\sigma_y^2$	$4.49 \times 10^{-27}$	$4.39 \times 10^{-25}$	$1.34 \times 10^{-23}$	$8.10 \times 10^{-23}$
PLL output	$f_1 = 0.1\text{Hz}, f_2 = 100\text{Hz}$ $a = 4.64 \times 10^{-12}, b = -1.83$				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	$\sigma_y^2$	$2.43 \times 10^{-24}$	$1.46 \times 10^{-24}$	$1.19 \times 10^{-24}$	$8.21 \times 10^{-26}$
<b>Device</b>	<b>Segment II</b>				
Reference oscillator	$f_1 = 10\text{Hz}, f_2 = 100\text{Hz}$ $a = 1.26 \times 10^{-13}, b = -0.40$				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	$\sigma_y^2$	$3.27 \times 10^{-23}$	$8.22 \times 10^{-23}$	$7.56 \times 10^{-25}$	$7.56 \times 10^{-27}$
Voltage-controlled oscillator	$f_1 = 10\text{Hz}, f_2 = 100\text{Hz}$ $a = 6.31 \times 10^{-12}, b = -2.00$				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	$\sigma_y^2$	$1.59 \times 10^{-24}$	$1.06 \times 10^{-23}$	$1.63 \times 10^{-25}$	$1.27 \times 10^{-27}$
PLL output	$f_1 = 100\text{Hz}, f_2 = 1000\text{Hz}$ $a = 2.51 \times 10^{-14}, b = -0.70$				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	$\sigma_y^2$	$1.04 \times 10^{-21}$	$1.00 \times 10^{-23}$	$1.01 \times 10^{-25}$	$1.01 \times 10^{-27}$
<b>Device</b>	<b>Segment III</b>				
Reference oscillator	$f_1 = 100\text{Hz}, f_2 = 1000\text{Hz}$ $a = 2.00 \times 10^{-14}, b = -0.00$				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	$\sigma_y^2$	$6.08 \times 10^{-20}$	$5.47 \times 10^{-22}$	$5.47 \times 10^{-24}$	$5.47 \times 10^{-26}$
Voltage-controlled oscillator	$f_1 = 100\text{Hz}, f_2 = 1000\text{Hz}$ $a = 6.31 \times 10^{-15}, b = -0.50$				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	$\sigma_y^2$	$8.88 \times 10^{-27}$	$8.27 \times 10^{-24}$	$8.28 \times 10^{-26}$	—



**Figure 8.** The phase-noise characteristics of the reference oscillator and the VCO can be expressed with three straight-line segments (I, II, and III); and the PLL output by two (top). The short-term stability in terms of the Allan variance can then be calculated by keying the required coefficients as determined from the coordinates of these line-segment ends into the calculator (see Table) and plotting the results (bottom).



remaining, is the number of intervals,  $n$ , into which the segments must be divided. The more intervals chosen, the more accurate the calculation, but the longer the calculation takes. A good choice for a minimum  $n$  value (which must be an even number) is

$$n \geq 10 [\tau(f_2 - f_1)].$$

The calculation time, then, is  $0.056n + 0.15$  min.

To illustrate an application of the Allan variance calculations, the (a and b) program coefficients for the straight-line segments making up the VCO, reference oscillator, and overall output noise were determined from Figure 8 (top). The coefficients are listed in the "Calculated Short-term Stability" table. Sample times of 1, 10, 100, and 1000ms and end frequencies of 0.1, 10, and 1000Hz were employed.

With these inputs,  $\sigma_y^2$  was determined with the Allan variance program. The frequency stability

$$\sigma_y(\tau) = \sqrt{\sum \sigma_y^2(\tau, f_h)},$$

was calculated, after summing the individual  $\sigma_y^2$  contributions of each segment. A plot of  $\sigma_y$  vs sampling time for the VCO, reference, and output is shown in Figure 8 (bottom). ■ ■

#### Acknowledgements

The author wishes to thank Dr. D. Halford and Dr. Fred L. Walls of the National Bureau of Standards, whose constructive discussions contributed to a more insightful understanding of the problems involved in working with PLL noise and short-term frequency stability.

#### References

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- 2 Halford, D., et al., "Spectral Density Analysis: Frequency Domain Specification and Measurement of Signal Stability," *Proceedings of the 27th Annual Symposium on Frequency Control*, U.S. Army Electronics Command, Fort Monmouth, NJ, June, 1973, p. 421.
- 3 Barnes, J.A., et al., "Characterization of Frequency Stability," *IEEE Transactions of Instruments and Measurements*, 1971, p. 105.
- 4 Lance, A.L., et al., "Phase Noise Characteristics of Frequency Standards," *Ninth Annual Precise Time and Time Interval Applications and Planning Meeting*, NASA-GSFC, Greenbelt, MD, 1977.
- 5 Walls, F.L., and Stein, S.R., "A Frequency-Lock System for Improved Quartz Crystal Oscillator Performance," *IEEE Transactions of Instruments and Measurements*, 1978, p. 249.
- 6 Stein, S.R., et al., "A Systems Approach to High-Performance Oscillators," *NBS Technical Note*, Boulder, CO.
- 7 Stein, S.R., and Walls, F.L., "Composite Oscillator Systems for Meeting User Needs for Time and Frequency," *NBS Technical Note*, Boulder, CO.
- 8 Culter, L.S., and Searle, C.L., "Some Aspects of the Theory and Measurement of Frequency Fluctuations in Frequency Standards," *Proceedings of the IEEE*, February, 1966, p. 136.

# Case Outlines

**L SUFFIX  
CERAMIC PACKAGE  
CASE 620-10  
ISSUE V**

**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC			
F	0.055	0.065	1.40	1.65
G	0.100 BSC			
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC			
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**P SUFFIX  
PLASTIC PACKAGE  
CASE 626-05  
ISSUE K**

**NOTE 2:**

**NOTES:**

- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC			
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC			
M	—	10°	—	10°
N	0.76	1.01	0.030	0.040

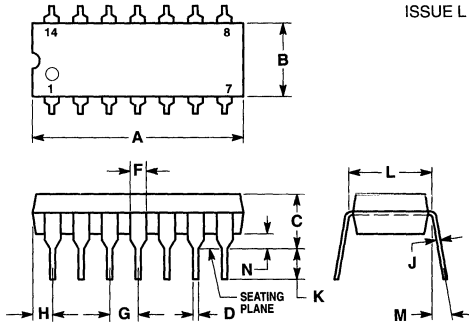
**L SUFFIX  
CERAMIC PACKAGE  
CASE 632-08  
ISSUE Y**

**NOTES:**

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.94
B	0.245	0.280	6.23	7.11
C	0.155	0.200	3.94	5.08
D	0.015	0.020	0.39	0.50
F	0.055	0.065	1.40	1.65
G	0.100 BSC			
J	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC			
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

**P SUFFIX  
PLASTIC PACKAGE  
CASE 646-06  
ISSUE L**

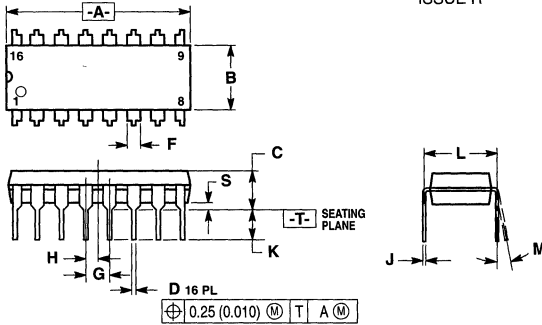


NOTES:

- LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

**P SUFFIX  
PLASTIC PACKAGE  
CASE 648-08  
ISSUE R**

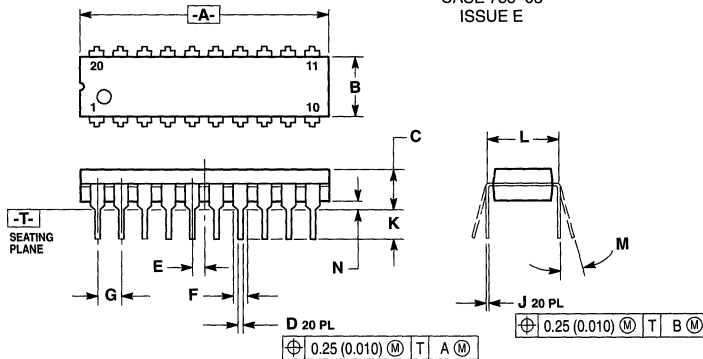


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.070	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

**P SUFFIX  
PLASTIC PACKAGE  
CASE 738-03  
ISSUE E**

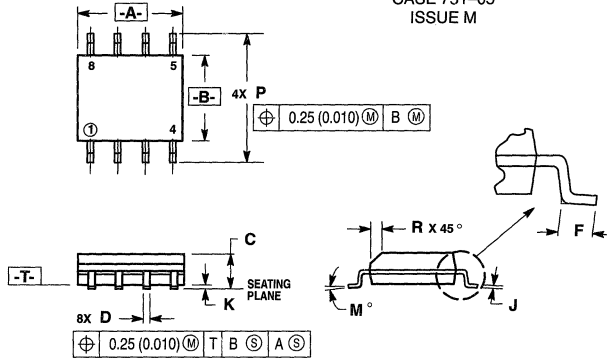


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIMENSION B DOES NOT INCLUDE MOLD FLASH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

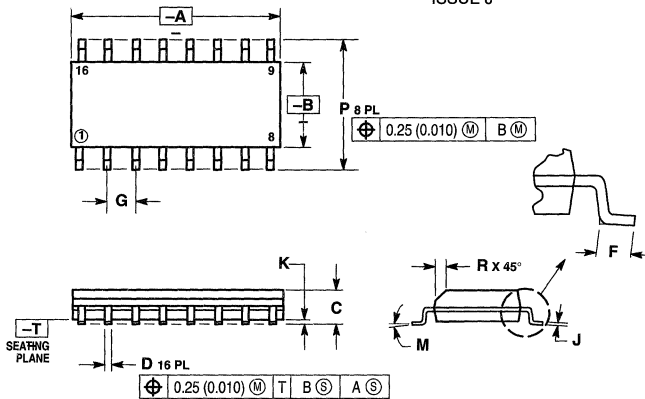
**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 751-05**  
**ISSUE M**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

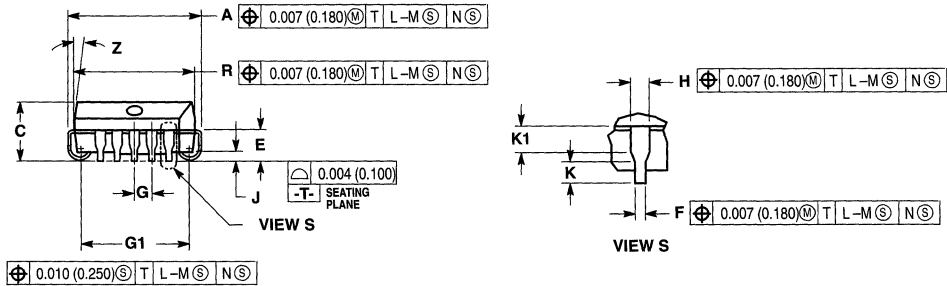
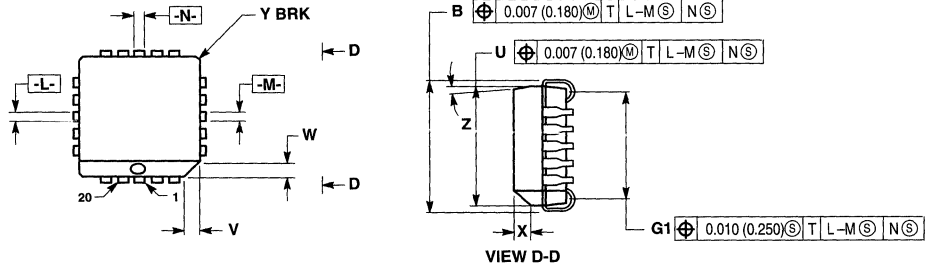
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**PLASTIC SOIC PACKAGE**  
**CASE 751B-05**  
**ISSUE J**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

MILLIMETERS		INCHES		
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

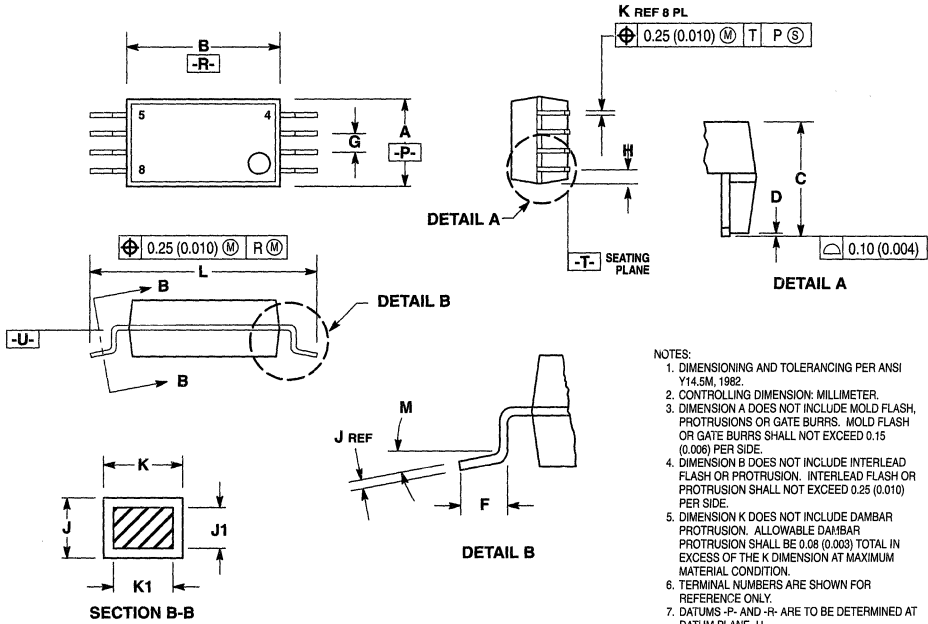
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**PLASTIC PLCC PACKAGE**  
**CASE 775-02**  
**ISSUE C**



- NOTES:**
- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
  - DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
  - DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
  - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH
  - THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
  - DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.385	0.395	9.78	10.03
B	0.385	0.395	9.78	10.03
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.350	0.356	8.89	9.04
U	0.350	0.356	8.89	9.04
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°	10°	2°	10°
G1	0.310	0.330	7.88	8.38
K1	0.040	—	1.02	—

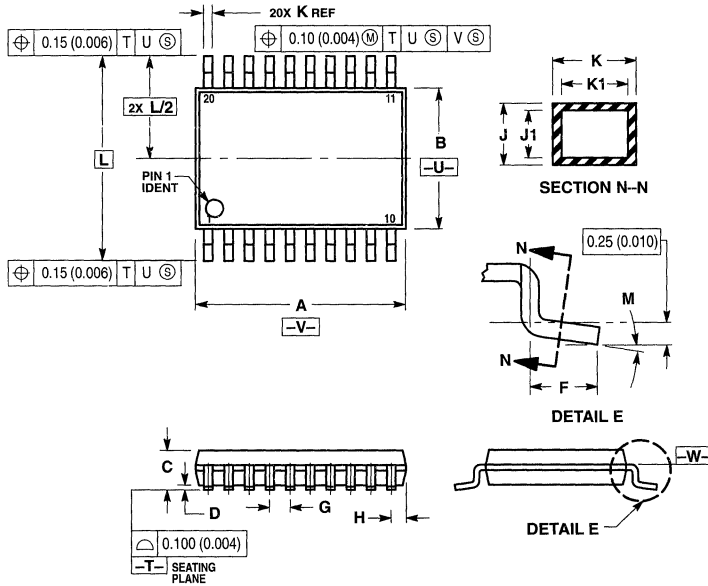
**SD SUFFIX  
PLASTIC SSOP PACKAGE  
CASE 940-02  
ISSUE A**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.008) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DATUMS -P- AND -R- ARE TO BE DETERMINED AT DATUM PLANE -U-.
  8. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -J-.
  9. CROSS SECTION B-B TO BE DETERMINED AT 0.10 (0.004) TO 0.25 (0.010) FROM THE LEAD TIP.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.87	3.13	0.113	0.123
B	5.20	5.38	0.205	0.212
C	1.73	1.99	0.068	0.078
D	0.05	0.21	0.002	0.008
F	0.53	0.95	0.022	0.037
G	0.65	BSC	0.026	BSC
H	0.50	—	0.020	—
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.22	0.38	0.009	0.015
K1	0.22	0.33	0.009	0.013
L	7.65	7.90	0.301	0.311
M	0°	8°	0°	8°

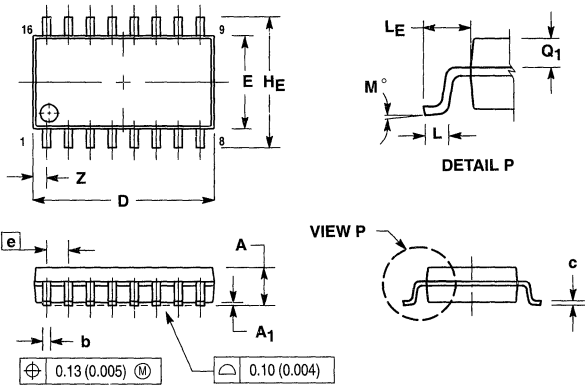
**DT SUFFIX**  
**PLASTIC TSSOP PACKAGE**  
**CASE 948E-02**  
**ISSUE A**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	+3.0	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.95	BSC	0.026	BSC
N	0.27	0.37	0.011	0.015
J	0.05	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252	BSC
M	0°	8°	0°	8°

**M SUFFIX**  
**PLASTIC SOIC PACKAGE**  
**CASE 966-01**  
**ISSUE O**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	—	2.05	—	0.081
A1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27	BSC	0.050	BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q1	0.70	0.90	0.028	0.035
Z	—	0.78	—	0.031

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