Designing with the LMC835 Digital-Controlled Graphic Equalizer

National Semiconductor
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INTRODUCTION

Because of the increasing use of digital techniques in consumer audio equipment, National has developed a digitally controlled graphic equalizer—the LMC835. This chip replaces the potentiometers used in a conventional graphic equalizer with digitally controlled step-variable resistors, thereby allowing computer manipulation of an analog signal path. The LMC835 is configured such that a high degree of flexibility remains in the overall equalizer design, without compromising the quality of the analog signal path.

Graphic equalizers are used to control the frequency response of an audio system. An equalizer contains a number of fixed-frequency bandpass/notch filters with a gain control for each filter. Resonances and nulls in the frequency response of an audio system are easily compensated with proper adjustment of the equalizer.

A single LMC835 contains enough step-variable resistors for a stereo, 7 band equalizer with 1 dB steps covering a ±12 dB range. Up to 14 monaural bands can be accommodated by paralleling the two halves of the chip. Because the internal step-variable resistors are implemented with inherently well-matched SiChrome resistors, accurate 1 dB control steps are possible. The LMC835 is available in a plastic 28-pin dual-in-line package.

The digital sections of a finished equalizing instrument will include a microprocessor, pushbutton controls, a large, multisegment display and any necessary circuitry to drive the display. The analog sections will contain the LMC835 and a number of associated operational amplifiers. Care has been taken in the design of the LMC835 to isolate sensitive analog circuitry from contamination by the digital sections. The analog sections of the equalizer will be considered first.

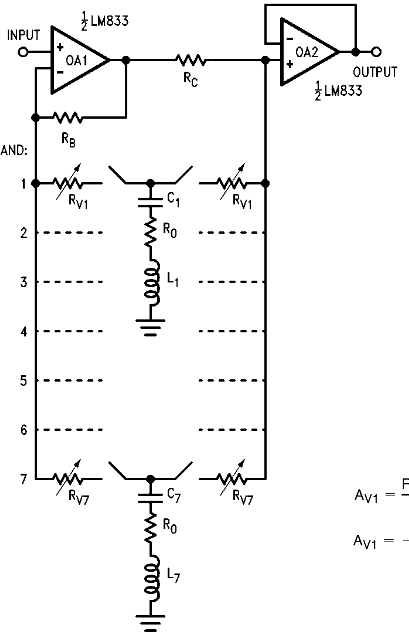
BASIC EQUALIZER TOPOLOGY

Many diverse equalizer circuit topologies have been commercially produced. A topology that works well within the constraints of step-variable resistors and uses a minimum of signal-path gain stages has been chosen for the LMC835.

The basic equalizer circuit shown in *Figure 1* uses two operational amplifiers in the signal path. This circuit represents ½ of an LMC835. R_B, R_C, R_{V1} through R_{V7}, and the selector switches are included on-chip. The first amplifier provides the boost (bandpass) function, while the second amplifier buffers the cut (notch) function. For any one frequency band both boost and cut functions are possible, but they are never selected simultaneously. Redundant external analog circuitry is therefore eliminated by exclusively switching each tuned circuit to either boost or cut.

The amount of boost or cut is controlled by on-chip variable resistors R_{V1} through R_{V7}. These are designed to ratio with R_B and R_C for perfect 1 dB steps. An optional 6 dB control range with 0.5 dB steps is discussed later in this application note.

Step-variable resistors were chosen for the LMC835 since they lend themselves well to digital control. Each variable



$$A_{V1} = \frac{R_{V1} + R_O + R_B}{R_{V1} + R_O} \text{ (Boost)}$$

$$A_{V1} = -\frac{R_{V1} + R_O}{R_{V1} + R_O + R_C} \text{ (Cut)}$$

$$F_1 = \frac{1}{2\pi\sqrt{L_1 C_1}}$$

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FIGURE 1. Basic Equalizer Topology

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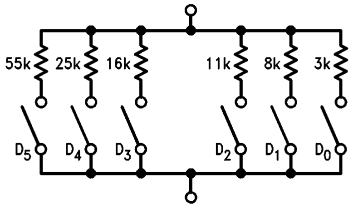
resistor shown in *Figure 1* is actually 6 fixed-value SiChrome resistors connected in parallel through CMOS FET switches. This is detailed in *Figure 2*. By selecting appropriate combinations of these 6 fixed resistors, better than 0.1 dB accuracy for each of 12 steps is obtained. The coding sequence is discussed in the programming section later.



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LEVEL	D_5	D_4	D_3	D_2	D_1	D_0
FLAT	0	0	0	0	0	0
1 dB	1	0	0	0	0	0
2	0	1	0	0	0	0
3	0	0	1	0	0	0
4	0	0	0	1	0	0
5	0	0	0	0	1	0
6	0	1	0	0	1	0
7	1	0	1	0	1	0
8	0	1	0	1	1	0
9	0	0	0	0	0	1
10	1	0	1	0	0	1
11	1	0	1	1	0	1
12	1	0	1	1	1	1

FIGURE 2. Digitally Controlled Variable Resistor

The frequency and bandwidth characteristics of each band are set by the L/C networks (*Figure 1*) and the value of each associated variable resistor. At resonance, the L/C network reduces to zero impedance. In the boost mode this leaves amplifier I with a gain set by the ratio of R_B and $R_O + R_V$. Conversely, attenuation is obtained in the cut mode with amplifier II buffering the circuit composed of R_C, R_O and R_V. Off resonance, the series tuned L/C network presents a high impedance and the gain (or attenuation) reduces to 1. Since the characteristics of the equalizer are determined by external L/C networks, the designer can tailor the equalizer circuit to suit his own needs.

Although it may seem that by relocating the switches of *Figure 1* a single bank of resistors could be used for boost and cut, this has not been done. Unlike mechanical switches, CMOS switches exhibit a finite ON resistance of several hundred ohms which unfortunately is not constant when large signal voltage swings occur across the switch. For a signal source with a nominal 1 Vrms level, with 12 dB of boost selected the signal swing would produce unacceptable distortion. By locating the switches between the resistor banks and the resonant circuit the actual peak signal swing across the switch is reduced to well within a linear operating region of the switches. The complete circuit with a 1 kHz, 1 Vrms signal input exhibits less than 0.003% distortion even with 12 dB boost.

BAND FREQUENCY SELECTION

Two basic equalizer types are in common use: one type has fixed band frequencies, the second type has variable band frequencies that can be tuned to allow control at specific points. The first type (graphic equalizer) is by far the most common, and the second type (parametric equalizer) finds limited popularity owing its cost and difficulty of use. The LMC835 circuit topology described here is intended for fixed band frequency applications.

The selection of band frequencies is entirely independent of the LMC835 as the chip has no frequency-sensitive or frequency-determining characteristics. There are two basic methods for selecting frequencies: 1) spread the bands out evenly over some desired frequency range, or 2) space the bands closely over the range where more control is desired, and space them more widely elsewhere. An example of this second technique is ***modified*** spacing where bands are tightly spaced at the low frequencies to allow control where it is most useful. The few remaining bands are spaced more widely at the higher frequencies ($>$500 Hz). Once the band frequencies have been selected, circuit Q, and the values for the series tuned circuits may be calculated. The following formulae find general use in equalizer design.

Band spacing is often measured in units of octaves. An octave covers a frequency ratio of 2:1, e.g. the frequencies between 1000 and 2000 Hz constitute an octave as do the frequencies between 200 Hz and 400 Hz. The number of octaves contained between any two frequencies is given by the equation

$$\# \text{ of octaves} = \mathrm{LOG}(F_2/F_1)/\mathrm{LOG}(2) \qquad (1)$$

where $F2 > F1$. Another formula used in conjunction with equalizer design is that which finds the musical center between two frequencies:

$$\text{center frequency} = \sqrt{F_2 F_1} \qquad (2)$$

As an example consider 2 frequencies, 220 Hz and 440 Hz. These are at an interval of 1 octave. At first glance it might appear that 330 Hz is halfway between these two, but as far as the ear can discern, 311 Hz is equidistant from 220 Hz and 440 Hz. This is because the ear hears logarithmic changes in pitch equally.

BAND SELECTION

In most consumer equalizers the band frequencies are equally spaced and centered around 1 kHz. The bands are related to each other by some factor. For example, 7-band equalizers with a 1 kHz center frequency use a factor of 2.5. If 1 kHz is repetitively multiplied and divided by 2.5 the other band frequencies will be found: multiplying (and rounding) we find 2.5 kHz, 6.3 kHz and 16 kHz, and dividing yields 400 Hz, 160 Hz and 63 Hz.

If the desired control range is defined, the center frequency can be found with the formula

$$\text{center band} = \sqrt{F_{MAX}F_{MIN}} \tag{3}$$

and the factor

$$\text{factor} = (F_{MAX}/F_{MIN})^{(1/d)} \tag{4}$$

F_{MIN} represents the lower −3 dB point of the "bottom" band when it is in full boost and all other bands are flat. F_{MAX} is the analogous higher −3 dB point of the "top" band. "d" is the number of bands. These formulae can be combined as

$$F_n = \left(F_{MAX}{}^{\frac{2n-1}{2d}}\right)\left(F_{MIN}{}^{\frac{2(d-n)+1}{2d}}\right) \tag{5}$$

where "n" is the band number (from 1 to d).

A common misconception about equalizers is that the band frequencies relate to the frequency response of the instrument. This is not true at all—the flat frequency response of the equalizer is completely independent of the band frequencies. Even so, many equalizer designs have bands extending beyond the normal range of hearing while compromising control at low frequencies.

There is no magic in spacing band frequencies. While equal spacing can offer control over a wide frequency range, it is possible to enhance control over a limited range by closely spacing the bands in one area while spreading out the remaining bands elsewhere. This technique (modified spacing) is especially useful at frequencies below 500 Hz where speakers and listening environments have pronounced resonances and antiresonances.

SELECTION OF MAXIMUM Q

The maximum desired Q of each band occurs at full boost or full cut and is set by the values of $R_O + R_V$, L_O and C_O. Mathematically Q_{MAX} is a function of the adjacent band frequencies:

$$Q_{MAX} = \frac{\sqrt{F_2}}{\sqrt{F_3} - \sqrt{F_1}} \tag{6}$$

where Q_{MAX} is the maximum Q of F_2 during full cut or boost, and F_3 and F_1 are the adjacent band frequencies. The highest and lowest bands on an equalizer have only one adjacent band. In this case:

$$Q_{MAX} = \text{ABS}\left(\frac{\sqrt{F_1F_2}}{F_2 - F_1}\right) \tag{7}$$

where F_1 is the adjacent band. In terms of a factor:

$$Q_{MAX} = \frac{\sqrt{\text{factor}}}{\text{factor} - 1} \tag{8}$$

In terms of F_{MIN} and F_{MAX}:

$$Q_{MAX} = \frac{\sqrt[2d]{F_{MAX}/F_{MIN}}}{\sqrt[d]{F_{MAX}/F_{MIN}} - 1} \tag{9}$$

The formulae for Q_{MAX} cause the −3 dB points of any two bands to occur at approximately the same frequency. If this is not desired, the maximum Q may be set to any value by appropriately designing the resonant networks. Higher values of Q give greater definition between bands while lower values of Q gives less ripple response between adjacent bands.

Once the maximum Q has been determined, L and C (from *Figure 1*) may be calculated:

$$L_n = 2270\, Q_{MAX}/\omega_n \tag{10}$$

$$C_n = 1/(\omega_n{}^2 L_n) \tag{11}$$

Note that 2270Ω is the minimum resistance including the 680Ω resistor (R_O), switch resistance and SiChrome resistance (R_V) as shown in *Figure 1*.

Using the typical 7-band consumer center frequencies (factor = 2.5) and a Q_{MAX} = 1.05 (from equation 8), the following values are calculated:

Band	Frequency (Hz)	L_O (mH)	C_O (nF)
1	63	6040	1060
2	160	2380	416
3	400	952	166
4	1000	381	66.5
5	2500	152	26.6
6	6300	60.4	10.6
7	16000	23.8	4.16

The inductances required at low frequencies would seem prohibitive, but there is an easy solution. The LMC835 is designed for use with series resonant networks. Since the inductances required are quite large and discrete realizations would be expensive, a simulated inductor, also called a gyrator, may be used.

GYRATOR DESIGN

The properties of an inductor may be simulated by a simple op amp circuit (often called gyrator) as shown in *Figure 3*. The impedance seen at the input terminal is $j\omega R_LR_OC_L$ and the inductance is given by the product $R_LR_OC_L$. As shown, R_O represents a loss resistance in series with the inductor. The internal SiChrome resistors are designed to accommodate an R_O of 680Ω.

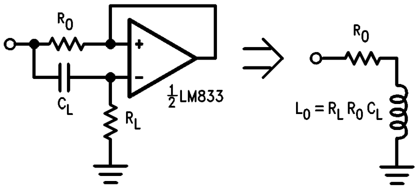

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FIGURE 3. Simulated Inductor

At high frequencies the impedance of the gyrator should approach infinity, but several effects limit the maximum impedance. The result is an increase in high frequency gain as contributed by the boost section, and a decrease in high frequency gain as contributed by the cut section.

Gyrator impedance is ultimately limited by the loading effects of R_L, especially for smaller inductances since R_L necessarily becomes small. To reduce loading effects keep $R_L > 47\ k\Omega$. In extreme cases C_L and R_L can be buffered by a second op amp as shown in *Figure 4*.

The voltage divider action caused by stray capacitance at the junction of C_L and R_L also reduces gyrator impedance. This effect is minimized by keeping $C_L > 470$ pF. Bootstrapping (*Figure 5*) is a viable alternative for reducing the effects of stray capacitance.

An important gyrator performance factor is the gain and phase of the op amp at high frequencies. An op-amp unity-gain bandwidth of at least 10 MHz is recommended since poor frequency response will reduce the gyrator impedance at high frequencies. Phase shift through the op amp causes the gyrator to become capacitive. The LM833 is an excellent choice for a gyrator as its bandwidth is well over 10 MHz, and it is unity gain stable.

Signal path stability and high frequency gain accuracy are affected by the feedback loop around the first amplifier of *Figure 6*. Most op amps cannot tolerate stray capacitance on their inverting input since it reduces the phase margin. This leads to increased gain at high frequency, if not instability. A 100 pF feedback capacitor compensates most op amps with little effect on the audio performance of the equalizer.

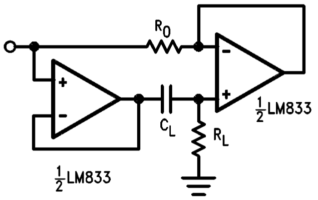

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FIGURE 4. Buffered Gyrator

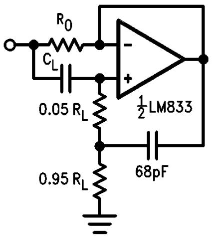

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FIGURE 5. Bootstrapped Gyrator

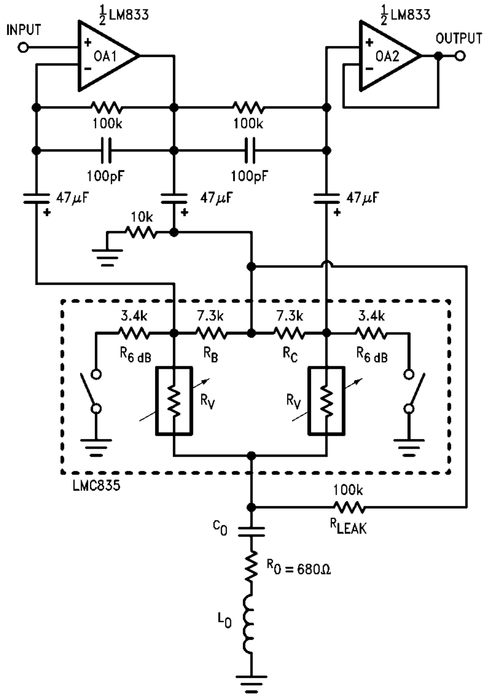

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FIGURE 6. AC Coupled Signal Path

SWITCH LEAKAGE

When the CMOS switches are OFF, a small leakage current of typically 1 nA can flow either into or out of any of the gyrator connections. This current charges C_O until a state of equilibrium is reached. If one of the switches is now closed, the charge stored on C_O will be injected into the signal path possibly causing an audible "pop" in the output. A 100 kΩ resistor is all that is necessary (as shown in *Figure 6*) to bleed this charge away and prevent pops. This results in a gain error or less than 0.2 dB at maximum boost or cut.

Provision is made to convert the equalizer to a +/−6 dB control range. The 3.4 kΩ resistors shown in *Figure 6*, when selected, drop the control range to +/−6 dB with approximately 0.5 dB steps. When the 3.4 kΩ resistors are selected, the resultant changes in the signal path DC gain can produce pops. Op amp input offset voltage and bias current are the root cause; the solution is to AC couple the signal path to the LMC835. In addition to the three 47 μF coupling capacitors of *Figure 6*, two 100 kΩ resistors are also necessary to provide a DC path around the op amps. Since the majority of applications require a "popless" configuration, the internal 7.3 kΩ resistors have been adjusted to accommodate the effects of the external 100 kΩ resistors. If DC coupling is not used, the 100 kΩ signal path resistors should be included to insure gain accuracy.

A complete seven-band graphic equalizer circuit is shown in *Figure 7*. 470Ω resistors are used in series with the output amplifiers to isolate capacitive loads that could cause instability. To increase signal handling capability the input is attenuated 6 dB by two 27 kΩ resistors and then equally amplified in the output buffer. With this configuration the maximum signal level at the input (with flat equalization) is about 9 Vrms yet the LMC835 sees only one-half of this—less than its +/−7.5V supply limitation. Clipping is still possible if, for instance, a 9 Vrms input is boosted 12 dB. There is sufficient headroom to handle full boost on a 2 Vrms input signal. Gyrator component values are shown in *Figure 8*.

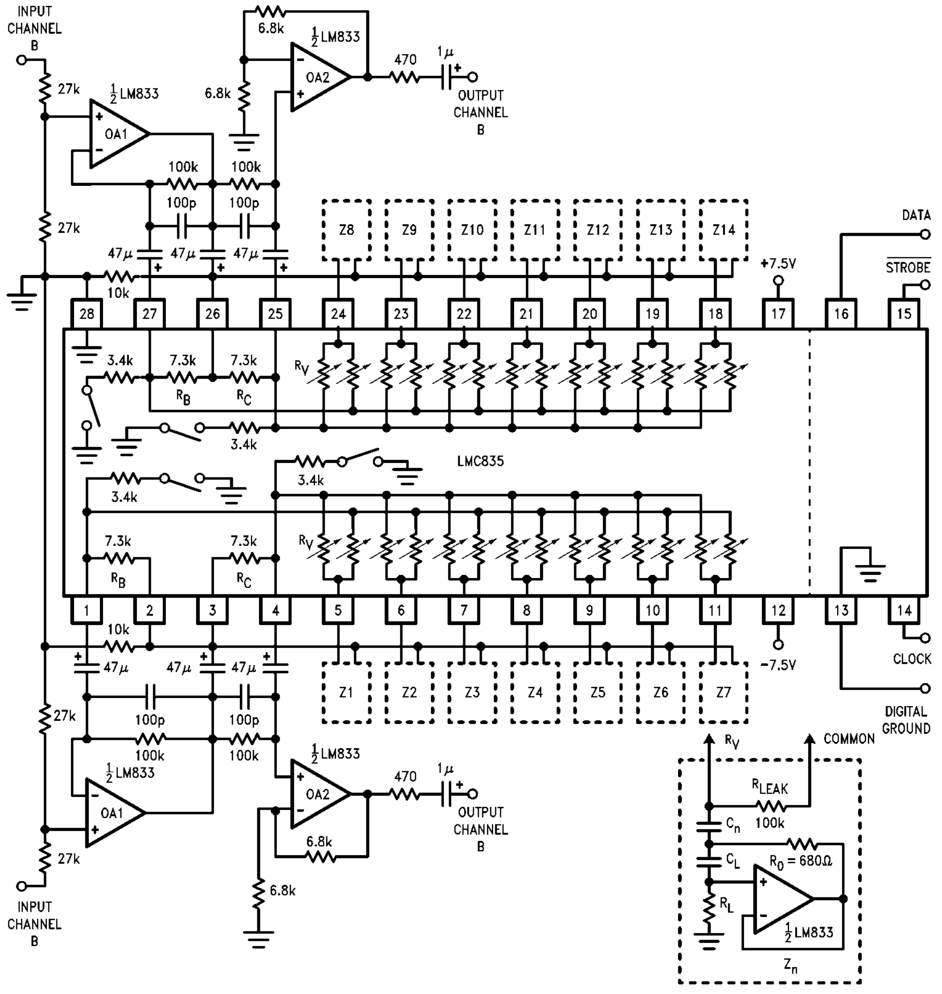

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FIGURE 7. Complete 7-Band Graphic Equalizer

Z_n	f_O(Hz)	C_O(F)	C_L(F)	R_L(Ω)	R_O(Ω)
Z1, 8	63	1µ	100n	100k	680
Z2, 9	160	470n	33n	100k	680
Z3, 10	400	150n	15n	100k	680
Z4, 11	1k	68n	6.8n	82k	680
Z5, 12	2.5k	22n	3.3n	82k	680
Z6, 13	6.3k	10n	1.5n	62k	680
Z7, 14	16k	4.7n	680p	47k	680

FIGURE 8. Gyrator Component Values

PARALLELING FOR MORE BANDS

The two halves of an LMC835 can be paralleled to provide up to 14 monaural bands. Paralleling (*Figure 9*) is accomplished by connecting pin 1 to pin 27 and pin 4 to pin 25. Pins 2 and 3 are left open, and any unused gyrator pins are simply tied off to ground. The ±6 dB range is selected by activating only one set of ±6 dB resistors, and either set will do.

In applications requiring 15 to 28 bands a second LMC 835 can be cascaded as shown in *Figure 10.* Note that the output buffer of the first LMC835 is made redundant by the input amplifier of the second LMC835. Therefore only 3 signal path op amps are required instead of 4.

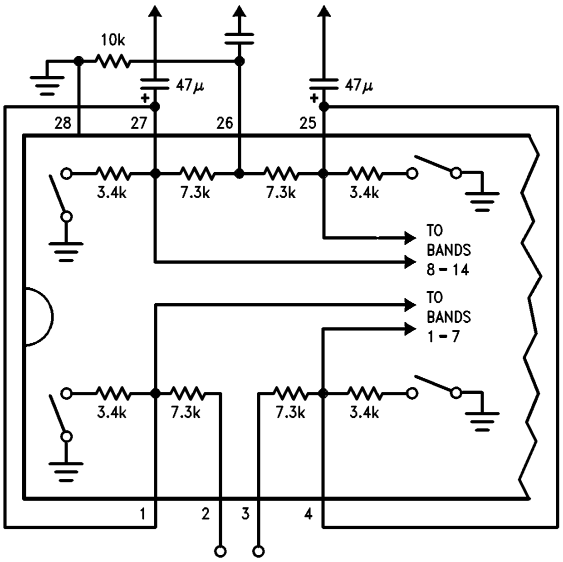

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FIGURE 9. Paralleling for 8 to 14 Bands on One Chip

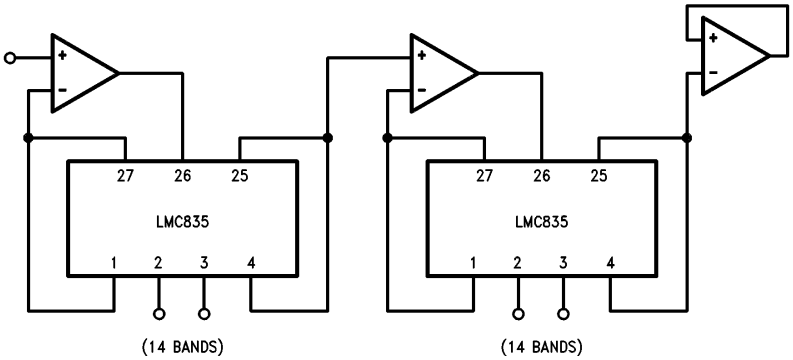

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FIGURE 10

PROGRAMMING

A three wire interface consisting of a DATA, CLOCK and STROBE line (*Figure 7*) is provided for programming the LMC835. DATA bits are shifted in to an internal serial register on positive CLOCK edges. This data is then latched (and executed) by a low-going pulse on the STROBE pin. A separate digital ground pin is provided to prevent contamination of the sensitive analog signal path.

Programming is accomplished with two 8-bit words. The first word selects a band for adjustment and selects either of ±6 or ±12 dB control range. The second 8-bit word selects boost or cut and the desired level for the band previously addressed. A timing diagram is shown in *Figure 11*. Note that bit D0 is shifted in first, D7 last. *Figure 12* shows the coding used for band and gain selection. With the maximum clock rate of 500 kHz, the entire equalizer can be programmed in less than 500 μs.

Parallel entry of data is possible using a simple word generator circuit as shown in *Figure 13*. A clock signal is applied continuously, and D0 through D7 are loaded and shifted into the LMC835 commencing with the positive edge of a start pulse. CLOCK, DATA and STROBE signals are all automatically generated and sequenced. D0 through D7 could be supplied by a parallel data bus or even toggle switches.

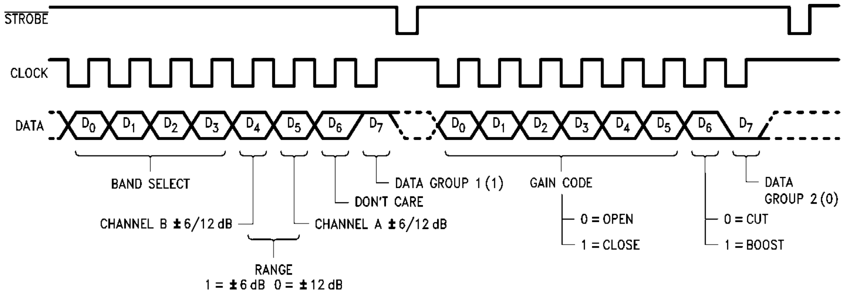

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FIGURE 11. Timing Diagram

DATA I (BAND SELECTION)

D7	D6	D5	D4	D3	D2	D1	D0	(CH A: BAND 1~7, CH B: BAND 8~14)
H	X	L	L	L	L	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, NO BAND SELECTION
H	X	L	L	L	L	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 1
H	X	L	L	L	L	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 2
H	X	L	L	L	L	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 3
H	X	L	L	L	H	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 4
H	X	L	L	L	H	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 5
H	X	L	L	L	H	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 6
H	X	L	L	L	H	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 7
H	X	L	L	H	L	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 8
H	X	L	L	H	L	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 9
H	X	L	L	H	L	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 10
H	X	L	L	H	L	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 11
H	X	L	L	H	H	L	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 12
H	X	L	L	H	H	L	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 13
H	X	L	L	H	H	H	L	CH A ±12 dB RANGE, CH B ±12 dB RANGE, BAND 14
H	X	L	L	H	H	H	H	CH A ±12 dB RANGE, CH B ±12 dB RANGE, NO BAND SELECTION
H	X	L	H	VALID BINARY INPUT				CH A ±12 dB RANGE, CH B ± 6 dB RANGE, BAND 1~14
H	X	H	L	VALID BINARY INPUT				CH A ± 6 dB RANGE, CH B ±12 dB RANGE, BAND 1~14
H	X	H	H	VALID BINARY INPUT				CH A ± 6 dB RANGE, CH B ± 6 dB RANGE, BAND 1~14

BAND CODE

CH B ±6 dB/ 12 dB RANGE

CH A ±6 dB/ 12 dB RANGE

DON'T CARE

DATA I

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DATA II (BAND SELECTION)

	D7	D6	D5	D4	D3	D2	D1	D0
FLAT	L	X	L	L	L	L	L	L
1 dB BOOST	L	H	H	L	L	L	L	L
2 dB BOOST	L	H	L	H	L	L	L	L
3 dB BOOST	L	H	L	L	H	L	L	L
4 dB BOOST	L	H	L	L	L	H	L	L
5 dB BOOST	L	H	L	L	L	L	H	L
6 dB BOOST	L	H	L	H	L	L	H	L
7 dB BOOST	L	H	H	L	H	L	H	L
8 dB BOOST	L	H	L	H	L	H	H	L
9 dB BOOST	L	H	L	L	L	L	L	H
10 dB BOOST	L	H	H	L	H	L	L	H
11 dB BOOST	L	H	H	L	H	H	L	H
12 dB BOOST	L	H	H	L	H	H	H	H
1 dB~12 dB CUT	L	L	VALID ABOVE INPUT					

This is the gain if the ±12 dB range is selected by DATA I. If the ±6 dB range is selected, then the values shown must be approximately halved.

GAIN CODE

BOOST/CUT

DATA II

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FIGURE 12. Coding Information

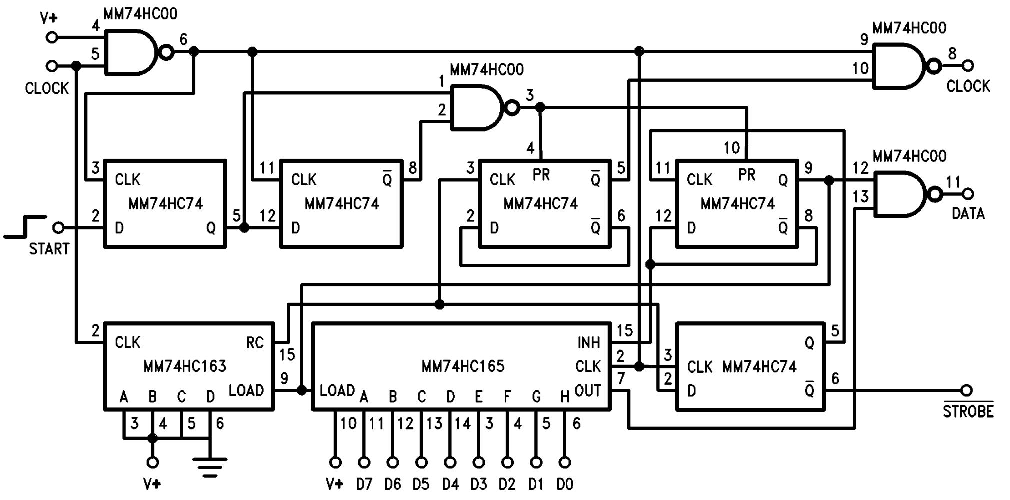

FIGURE 12. Test Word Generator

APPLICATIONS

Several distinct advantages are associated with computer controlled equalizers. Remote control is possible unlike conventional mechanically controlled equalizers. Since the LMC835 is programmed by a simple 3-wire interface, hardwired control from a remote location is also possible. This is useful on stage or in the studio where the equalizer must be located near the source and the amplifiers and/or speakers, but the control point is behind the audience or in a control room. The 3-wire digital interface is easier to connect than attempting to route low-level analog signal lines over long distances between signal source and control point.

Microprocessor storage of various equalization settings is possible. Specific settings for different instruments, diverse program material, or perhaps multiple speaker or listening environments can be accessed as easily as recalling a pocket calculator memory. If a real time analyzer (RTA) is included in the equalizer, automatic equalization is possible. In this application pink noise is played through the amplifier/speaker system, and a calibrated microphone feeds the resultant spectrum back to the RTA. One band at a time, the controlling microprocessor adjusts the LMC835 equalizer for flat response. Two or three iterations are required since the adjustments are interactive.

By using analog circuit techniques, the LMC835 is able to achieve 0.0015% distortion, 114 dB signal to noise ratio and 20 dB headroom relative to a 1 Vrms input signal. This performance is suitable for use with conventional analog audio sources as well as digital audio formats.

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