Differentiating FDDI Concentrators

National Semiconductor
Application Note 741
David Brief, Bob Hanrahan
February 1991

INTRODUCTION

The FDDI Standard offers a broad based set of capabilities that will allow it to become the standard high performance network of choice for the '90s. The FDDI Concentrator plays a central role in providing the necessary flexibility, reliability and manageability in order for FDDI to enjoy widespread deployment. A single Concentrator design is unlikely to meet the wide range of cost and performance objectives for all installations and environments. As the FDDI marketplace develops, many different types of concentrators will be required that are differentiated on the basis of their total cost combined with their expandability, functionality, reliability and the management features they provide. This market differentiation of concentrators is just beginning.

After a short overview of the place of concentrators within FDDI, issues relating to requirements of concentrators and how to differentiate them in the marketplace are discussed. Finally, two example designs that make full use of the National Semiconductor DP83200 chipset are presented. The example designs include a single board single processor design and a multiboard multi-processor design. These examples can be used as a basis and starting point for a whole spectrum of solutions.

1.0 CONCENTRATOR OVERVIEW

1.1 FDDI Topology Considerations

The FDDI Standard defines two classes of stations: a dual attach station (DAS) which connects to both rings either directly or through a concentrator and a single attach station (SAS) which connects to one of the rings through a concentrator. A concentrator, which can be either a single attach or dual attach node, provides ports to individual nodes, thereby including them in one of the rings. Further flexibility is provided by allowing a concentrator to connect into another concentrator and create a tree structure.

The FDDI topology is defined as a dual ring of trees where any subset is a legal topology. This permits many possible physical topologies:

1) single concentrator with a limited number of SASs
2) a ''tree'' of concentrators with several levels of concentrators with SASs at the lowest level
3) a dual counter rotating ring with multiple dual attach stations
4) a dual ring of concentrator trees

The concentrator plays a key role in many of the permitted and preferred physical topologies, providing the required flexibility to accommodate the common building cabling practices.

The FDDI physical topology is composed of point to point full duplex links. These links are arranged in a combination of tree (star) and ring topologies. These links are then formed into a logical ring topology using a signaling technique on each duplex link. When fully functional, the logical topology consists of dual counter-rotating rings, independent of the physical topology.

The counter-rotating rings allow a network to continue working in the presence of a single failed link or node. Such a failure causes the network to go into ''wrap'', wherein the station directly upstream of a failure re-routes its output to the secondary ring while the station immediately downstream of the failure accepts input from the secondary ring. This then bypasses the fault and creates a single logical ring.

A concentrator has the added benefit of isolating a faulty link or node in one of the ports that it is controlling. It does not need to wrap the ring and instead it can electronically bypass whatever is connected to that port to effectively heal the ring with minimal disruption.

1.2 Benefits of Using Concentrators

Employing concentrators as part of a physical topology plant provides many advantages as detailed below.

1.2.1 Simplicity of Wiring

Connectivity between a concentrator and SAS attachments matches normal wiring topologies. Most facility planners wire buildings in star or star-of-star fashion rather than in rings. Concentrators require installation of one fiber pair between offices and wiring closets instead of 2 fiber pairs required by a DAS attachment.

1.2.2 Reduce Overall Cost

Manufacturers constantly sustain pressure to reduce the footprint of their desktop workstations. Concentrators, by providing connectivity to SAS nodes, reduce the logic and power requirements of these nodes, which in turn reduces the footprint. This is then reflected in the cost of the node (workstation). In addition, there is reduced fiber and connector cost compared with not using a concentrator.

The additional cost of the concentrator may initially offset the reduced price of the workstation. This does not account for the long term network facility costs in which ease of maintenance, manageability and reliability are crucial.

1.2.3 Improved Network Reliability

If a network contains only DAS nodes connected on the dual ring, single failures will normally cause the ring to wrap, and subsequent failures will segment the ring into one or more disjoint rings. Since a concentrator can bypass any number of the nodes connected to its ports, it makes the ring tolerant to a larger number of failures. This higher reliability makes very large FDDI networks more practical.

For additional reliability, it is also possible to connect the ports of Dual Attach Stations to different concentrators. This increases the network reliability in terms of survivability in the presence of faults (at the cost of increasing the number of physical connections (links) in the network).

1.3 What Is in a Concentrator

The FDDI concentrator provides ports for connecting the concentrator into one of the rings and for connecting nodes into one of the rings. FDDI defines 4 types of ports, the A Port, the B Port, the S Port and the M Port.

RRD-B30M75/Printed in U. S. A.

The A and B ports are typically found in the dual ring of trees (sometimes called the trunk ring). An A–B connection is called a Peer Connection. The M (Master) and S (Slave) ports are typically found in the concentrator trees. The M–S connection is a Tree connection. The M port is provided by the concentrator to connect Slaves into the ring via their S ports. As defined currently by SMT, a concentrator may have from 1 to 255 M ports. A concentrator also provides a connection to the rest of the network. To connect a dual attach ring, an A port and B port are provided. To connect to another concentrator in a tree, an S port is provided. In a complete tree physical topology, the concentrator at the top of the tree would not have any A, B or S ports.

For each port in a concentrator there is one PHY (physical) layer entity. The PHYs perform the PHY layer services including re-timing the input data stream, performing the 4B/5B encode/decode function, monitoring the link error rate on the incoming link and providing the facilities to perform the link and connection establishment. Second generation FDDI chipsets such as National Semiconductor's DP83200 chipset, provide a large level of support for these functions, but so far none alleviate the need for some external processor support for performing CMT and LEM.

Aside from the number of M Ports a concentrator provides and the way it attaches to the rest of the network, concentrators are also differentiated on the basis of the number of internal paths they provide. The paths within a station are used to connect the stations attached to the concentrator M ports to the primary or secondary ring. Some concentrators may only be able to connect M ports onto the primary ring while others may be able to connect these ports onto the secondary ring as well. A configuration switch is required with each PHY entity in order to attach the associated M Port into either the primary or secondary ring.

To take full advantage of the management capabilities afforded by a concentrator, a MAC level entity is required in a concentrator. A concentrator may include up to one MAC per path. At the simplest level, the MAC provides a frame level interface. This makes possible communication with all of the other stations in the ring. This allows the concentrator to participate in all of the management protocols such as the parameter management and status reporting protocols.

The concentrator also provides an obvious place to perform network management functions such as gathering relevant statistics for all stations, detecting degrading links, isolating faulty stations, managing legal configurations, and detecting illegal topologies. The concentrator may also serve as an interface between higher level management services such as the Simple Network Management Protocol (SNMP) and the local FDDI station management.

1.4 Station Management in Concentrators

The FDDI concentrator is an active station in an FDDI LAN unlike hubs in IEEE 802.3 and passive wiring centers in IEEE 802.5. As an active station it is responsible for monitoring and maintaining all of its connections to other stations in the network and for performing and providing the services required by the FDDI Station Management (SMT). The SMT for Concentrators is a superset of the SMT for Stations. For example the path management requirements for a station are less complicated than the path management issues for a concentrator.

SMT can be viewed as an entity that manages several objects and their interactions within a Station or Concentrator. Information related to each manageable object is maintained as described in the FDDI SMT Management Information Base (MIB). Currently, the MIB defines four object types: MAC, PATH, PORT and ATTACHMENT. Each object may have multiple instances within a node. For example, a typical concentrator might have two MAC objects, two PATH objects and ten PORT and ATTACHMENT objects.

It is convenient to view SMT as a distributed database where each station keeps track of its own information. SMT defines the information in the MIB, how to access it, and how it changes. All SMT processes are involved with manipulating the MIB.

The SMT frame based processes typically convert information from the MIB into frames. SMT frames are defined to help build ring maps and detect duplicates (Neighbor Notification frames), provide station information, provide access to parameters (Parameter Management frames), and announce interesting conditions (Status Reporting frames). These processes are typically implemented for each MAC object.

An instance of the SMT Ring Management (RMT) process is present for each MAC object. RMT is responsible for providing information to keep the ring operational. This includes detecting Stuck Beacon conditions, detection of duplicate addresses that keep the ring from becoming operational, and notification of MAC Availability. RMT also provides recovery mechanisms for the stuck beacon condition and duplicate address conditions that prevent the ring from becoming operational. The current state of RMT is kept in the MIB. The DP83261 BMAC™ device supports efficient implementations of RMT by reporting all of the necessary events and conditions.

In addition, for each MAC frame level statistics are maintained. These include the number of frames transmitted, received, copied and not copied in addition to the frame error and lost frame counts. The measured Ring Latency and Token Count are also maintained. The DP83261 BMAC device provides extensive support for all of these statistics.

An instance of the Physical Connection Management (PCM) process is present for each PORT object. This process is responsible for the initialization of physical connections. This includes support for connection policies such as the withholding of undesirable and illegal connections, signaling of physical topology information and notification of availability for a PORT connection. PCM also includes support for the fault tracing function and testing of link confidence. The DP83251/55 PLAYER™ device supports efficient implementations of PCM with no external logic, and minimal constraints on the processor.

In addition, for each PORT continuous monitoring of the estimated Link Error Rate is also accomplished. Should this link error estimate fall below a MIB defined alarm threshold, the event is announced through Status Reporting Frames. Similarly if the link error estimate falls below a MIB defined cutoff threshold, the link is broken and an attempt is made to reconfigure the network around the physical layer fault. The DP83251/55 PLAYER device supports efficient software implementations of the Link Error Monitor with no additional components.

One instance of the Entity Coordination Management (ECM) process is present in a Node and controls all of the Attachment objects. This process is responsible for controlling the optional bypass switches and signaling PCM when the media is available. Actions that must be coordinated across several entities such as Path Testing and the Trace Function are handled in ECM.

The PATH Objects are handled slightly differently within SMT. Instances of Configuration Element Management (CEM) for each PORT are collectively responsible for managing all of the PATH objects. The DP83200 chipset and in particular the DP83255 PLAYER device supports CEM through its built in Configuration Switch.

In concentrators there are several special considerations for SMT. Handling of Dual Homing must be accounted for, as must the unique cases of propagating the Trace function. In addition, more complex configurations such as Trees must be described and managed. This includes detection of illegal topologies such as Master Slave Loops, and the notion of Root Concentrator MACs.

There is still a fair amount of confusion regarding Path Management issues in SMT, especially as they relate to a concentrator. As more experience is gained in building stations and concentrators, this process should converge to a ratified SMT Standard.

2.0 DIFFERENTIATING CONCENTRATORS

FDDI concentrators can be differentiated in many ways just as in any diversified product such as Adapter Cards, Bridges, Routers, etc.

The most obvious way in which concentrators are differentiated is in the number of each of the resources that are managed. Other ways concentrators are differentiated are in terms of the options they provide for expansion, the management features they offer, and the diagnostic capabilities they provide. The concentrator also is a logical place to implement Bridging and Routing Functions as well as Management Agent processes. Each of these ways for differentiating concentrators is discussed below.

2.1 Types of Concentrators

There are several concentrator configurations as shown in the table below:

TABLE I. Possible FDDI Concentrator Configurations

Name	Attach Count	Paths	MACs	M Ports
NAC	0	1–3	>1	>0
SAC	1	1–3	>1	>0
DAC	2	2–3	>1	>0

Naming Conventions

The concentrators are named according to the greatest number of attachments they can handle (Null, Single or Dual Attachment Concentrator NAC, SAC, DAC respectively). It is debatable whether this is the best way to name concentrators since the other parameters are more likely to vary.

Attach Count

This refers to the number of attachments that are available for use to either the trunk ring or to the concentrator tree. A concentrator with an attach count of 2 could default to a concentrator with an attach count of 0 or 1 if those attachments are not connected to anything else.

Paths

This refers to the number of token paths possible in a concentrator. These paths may then be used as part of the Primary, Secondary or Local Ring. There must be at least one path in single and null attach concentrators and at least two paths in a dual attach concentrator. These paths are used to connect ports into the appropriate path.

With only one path in a concentrator, attached stations can only be connected into the ring that the Attachment is connected into. In a tree, if the S Port of a SAC is connected into the Primary Ring then all of the stations attached to the M Ports of the concentrator can only be connected into the Primary Ring. Similarly, if the S port is connected into the Secondary Ring the stations attached to the M Ports can only be connected into the Secondary Ring.

With two paths in a Dual Attach Concentrator, Ports can be placed in both the primary and secondary rings. Currently it is difficult to reliably put a Port on the secondary ring. PCM does not offer the necessary set of hooks to request placement on the secondary ring. The default is that the station is placed in the primary path and can only be switched to the secondary using optional services (by using Parameter Management Frames to set the Requested Paths MIB parameter).

With two paths in a Single Attach Concentrator, Ports can be placed in either the Primary or Secondary Ring depending on the ring in which the Attachment is currently connected. The second path could then be used as a Local Path.

With three paths in a Single Attach Concentrator, Ports can be placed in both the Primary and Secondary Rings. The third path could then be used as a Local Path.

Use of a Local path within a concentrator is not well defined and there is not a clear consensus on the use of and the requirements for a Local Path in a concentrator. Functions that have been suggested for a Local Path usually assume that a MAC can be placed, at least temporarily onto the Local Path. This MAC is sometimes called a roving MAC or local MAC. Suggested uses of the Local Path include:

- setting of slave station's parameters
- testing of slave before insertion into ring
- determining the topology of a concentrator tree before insertion into the Primary or Secondary ring
- graceful insertion of slave stations or concentrator trees.

There are still several problems associated with each of these uses. There is no interoperable method for setting parameters in a slave station and no protocol defined for testing a slave before inserting it into a ring. Similarly it is not clear that a roving MAC could find out more about a slave station than a station self test could.

These same problems could be solved in the context of SMT without resort to a non-standard local path. A slave could do a self test before requesting insertion into the ring by causing remote loopback at the concentrator. The station could come into the ring with default parameters that could also be changed during normal operation. And to solve the ring mapping problems, an efficient protocol using well known SMT Group Addresses could be used. There is still a fair amount of work to be done in the area of inserting slave stations into a ring. Use of the local path does not solve these problems and the extra cost and complexity of adding an additional path is questionable in terms of the minimal payoff.

MACs

In order for a Concentrator to provide management services and act as a manageable entity in a network, it should contain at least one MAC. This gives the concentrator the ability to participate in the SMT frame based protocols and help isolate, announce and recover from all types of problems. By having MACs in concentrators, better logical and physical ring maps can be built.

To simplify the relationship between MACs and Paths, it is easiest to have one MAC per Path. Otherwise it is necessary to multiplex a MAC between the paths. It is difficult to manage inserted stations on a path that has no MAC.

The data throughput requirements for a MAC implementation are rather minimal, thus low cost management MACs can easily be added. The cost associated with MACs has been one of the main points of resistance to standardizing the presence of at least one MAC in a concentrator. The incremental cost of adding a MAC compared with the benefits of the added manageability makes it worthwhile, especially in configurations where it amounts to only two extra chips. (In these configurations all of the memory and processor support is already present.)

Master Ports

A concentrator will have several Master Ports, each of which can connect to a Slave or Peer Port. The number of ports is very implementation specific, and ranges from small departmental concentrators with 4 M Ports to large multiboard concentrators with up to over 250 ports.

2.2 Expandability/Configurability

Another way in which concentrators can be differentiated is by their packaging. In many instances a low cost fixed configuration makes sense. In other cases an expandable and configurable concentrator might be attractive.

An attractive fixed configuration might consist of 8 ports that could be used as an 8 port NAC, a 7 port SAC or a 6 port DAC.

An attractive flexible configuration might consist of Slave or Peer Attach boards and Master Port boards. On each Master Port Board there might be 4 or 8 Master Ports.

An example of both a fixed and flexible concentrator are outlined as examples in Section 4.

Another dimension in which concentrators can be configurable is in the PMD that is supported. FDDI already supports both a multi-mode and a single mode fiber optic PMD and it is very likely that additional lower cost PMDs such as Shielded Twisted Pair and shorter distance fiber optic connections will be supported. By isolating the PMD to a separate board the PMD could be a configurable option.

The Concentrator could also serve as a repeater between different media domains by using different PMDs in different ports.

2.3 Management Capabilities

Concentrators can also be differentiated by the management capabilities that they provide. The SMT Standard provides many implementation options does not specify how the services that it provides will be used. The Concentrator is a convenient location to run Network Management Applications such as a ring monitor, ring mapper, traffic analyzer, traffic generator, etc. It also is a logical location to run higher level management agents such as SNMP and/or CMIP. Management agents serve as proxy agents for management services between stations that do not implement the particular management protocol but do implement SMT and the actual management application.

2.4 Diagnostic Capabilities

Since a concentrator is one of the most complex nodes in the network, it should contain extensive diagnostic capabilities. Essential to this is the ability to perform sophisticated Path Testing and Resource testing of all resources within the concentrator. The National Semiconductor DP83200 FDDI chipset has numerous diagnostic capabilities built in to aid in isolating and resolving problems.

2.5 Bridging/Routing Capabilities

The concentrator is also a natural location to add in a MAC level bridging or routing function between similar or different media, networks, speeds, and protocols. Because of the concentrator position within an installation it may offer a natural point to segment the local traffic contained exclusively in the tree versus traffic that must go outside of the tree.

Such a concentrator would become a multi purpose network attachment that could be a repeater/bridge/router and manager where each function is added in as needed on a common backplane. You could think of it as a ring in a box.

3.0 USING THE NATIONAL DP83200 FDDI CHIPSET

The National Semiconductor DP83200 FDDI chip set was partitioned for use in all of the Standard FDDI configurations including Single and Dual Attach Stations with one or two MACs and in numerous Concentrator configurations.

The DP83251/55 Physical Layer Controller (PLAYER device) implements the Physical Layer (PHY) of FDDI and provides all of the support required by a processor running SMT. In addition to providing all of the functions required by an FDDI PHY, the PLAYER device includes support for the Link Error Monitor Function, the Noise Counter (TNE), Line State Detection and Generation, and Configuration Management. Two full duplex parallel ports are supported along with a built in Configuration Switch in order to provide the flexibility to support all of the station types (SAS, SM-DAS, DM-DAS) and configurations (THRU, WRAP, ISOLATE). Concentrator configurations with numerous M Ports and 2 internal paths can be created without any external logic. The low power dissipation and minimal real estate required by the PLAYER device makes these chips ideal for concentrator applications.

The DP83231 Clock Recovery Device (CRD™ device) provides a very high performance analog Phased Locked Loop with very high noise immunity. It can lock to the worst legal patterns in under 85 μs and provides a very high dynamic lock range.

The DP83261 Basic MAC Layer Controller (BMAC device) implements the Media Access Control Layer (MAC) of FDDI and provides the support required by a processor running SMT. In addition to providing all of the functions required by an FDDI MAC, the BMAC device includes support for RMT, all of the required and optional frame counters, measurements of the ring/path latency and many tunable parameters.

The DP83265 BMAC System Interface (BSI™ device) is also available for providing a straightforward system memory interface. The BSI device also provides several features that are useful for SMT such as independent channels for Management Data (SMT/MAC).

The DP83241 Clock Distribution Device (CDD™ device) generates all of the clocks required by the PLAYER, BMAC and BSI devices. The CDD device accepts either an external reference or a local crystal. In a concentrator the CDD device is particularly useful in that all of the clocks required by the PLAYER device can be generated locally and only slower speed 12.5 MHz clocks need be distributed. The CDD device also provides 10 different phased clock outputs.

The chipset also provides numerous diagnostic features. These include full duplex data paths to allow diagnostic transmission to self, multiple levels of loopback to isolate individual chip and interconnect errors and the ability to inject errors and make sure that proper recovery takes place. In addition, while operational, several levels of self checking are also employed. These include through parity support, full duplex data paths so that every frame transmitted can also be received and the FCS can be checked (the frames could also be copied), and a full implementation of the FDDI protocol which is self checking in itself.

The chipset also includes several programmable features that allow compatibility with the ongoing enhancements to the ANSI specification.

For more details see the appropriate device datasheets.

4.0 EXAMPLE DESIGNS

The following examples illustrate the simplicity of building concentrators with the National Semiconductor DP83200 FDDI chipset. Two example designs are shown representing two ends of the spectrum. First a Single Board, Single Processor Concentrator is shown, followed by a Multi-Board, Multi-Processor design.

4.1 A Single Board Single Processor Concentrator

A simple FDDI concentrator contains a single processor and is designed on a single card. The clear advantage of this type is reduced cost, though forfeiting flexibility and expandability.

Figure 4-1 shows a simple single processor dual attach dual path design. The diagram also suggests a physical layout of the devices. Even the pinout of the devices in the chipset were optimized for these applications.

The concentrator shown has an A Port, B Port, 4 or more M Ports and 2 MACs. It also has two complete physical paths, one of which can be used as the Primary Path, and the other as a Secondary Path or Local Path. The M Ports connect into the Primary or Secondary Path through the PLAYER device's configuration switch as shown in *Figure 4-2.*

Extensive Path testing can be accomplished as two complete rings can be made operational as shown in *Figure 4-3.* For the ring to be operational, all data paths have to be working properly. The MAC on each ring will go through the Claim Process and if it receives its own Claim frame successfully, a token will be issued which will continue to circulate. That MAC could then send frames to itself for even more robust path testing.

The port types are distinguishable by the fiber optic connector receptacle keying. During the connection establishment procedures of SMT (Physical Connection Management—PCM), the connected port types are checked for compatibility. Typically SMT will only allow A to B, B to A and M to S connections, but SMT can be configured to override this protection mechanism.

When there is no trunk ring or concentrator tree to connect into, SMT can be configured to allow slaves to attach to the A and B Ports (A to S and B to S connections). When there is a tree to connect into, the concentrator can be configured to allow M to A and/or M to B connections. In this way, this concentrator could be used as a Null Attach Concentrator with 10 leaf connections, a Single Attach Concentrator with 9 leaf connections or a Dual Attach Concentrator with 8 leaf connections.

With the two path design shown and correct programming of the configuration switches, the second path could be used as a local path while bypassing the ring's secondary path within the concentrator (see *Figure 4-4*). Note the subtle differences between *Figure 4-2* and *Figure 4-4.* Only the connection surrounding the Peer Ports is changed. Thus effectively, three paths are present within the concentrator, although not all of them can be active simultaneously. With additional external multiplexing, a dedicated third path could be added to the design. The third local path would then always be available for internal testing for use with a roving MAC. The benefits of a dedicated third path versus the additional cost are questionable.

The processor controls the BSI, BMAC and PLAYER devices through the common control interface. The control bus uses a simple asynchronous handshake. The processor can accomplish all of software oriented portions of SMT (CMT, RMT, monitoring functions) using this common interface. The SMT frames are typically generated and processed in a shared memory.

Moderate interrupt response time is required to assure compliance with the default requirements (3 ms) of the Physical Connection Management (T__REACT, PC__REACT, etc.). Depending on the interrupt latency of the processor, as additional M Ports are added, the processor will eventually reach its limit in terms of the number of ports that can be handled simultaneously. In concentrators with many M Ports, in order to guarantee the required response times, it may become necessary to partition tasks among multiple processors or switch to a processor with a better interrupt latency (provided that it is not saturated).

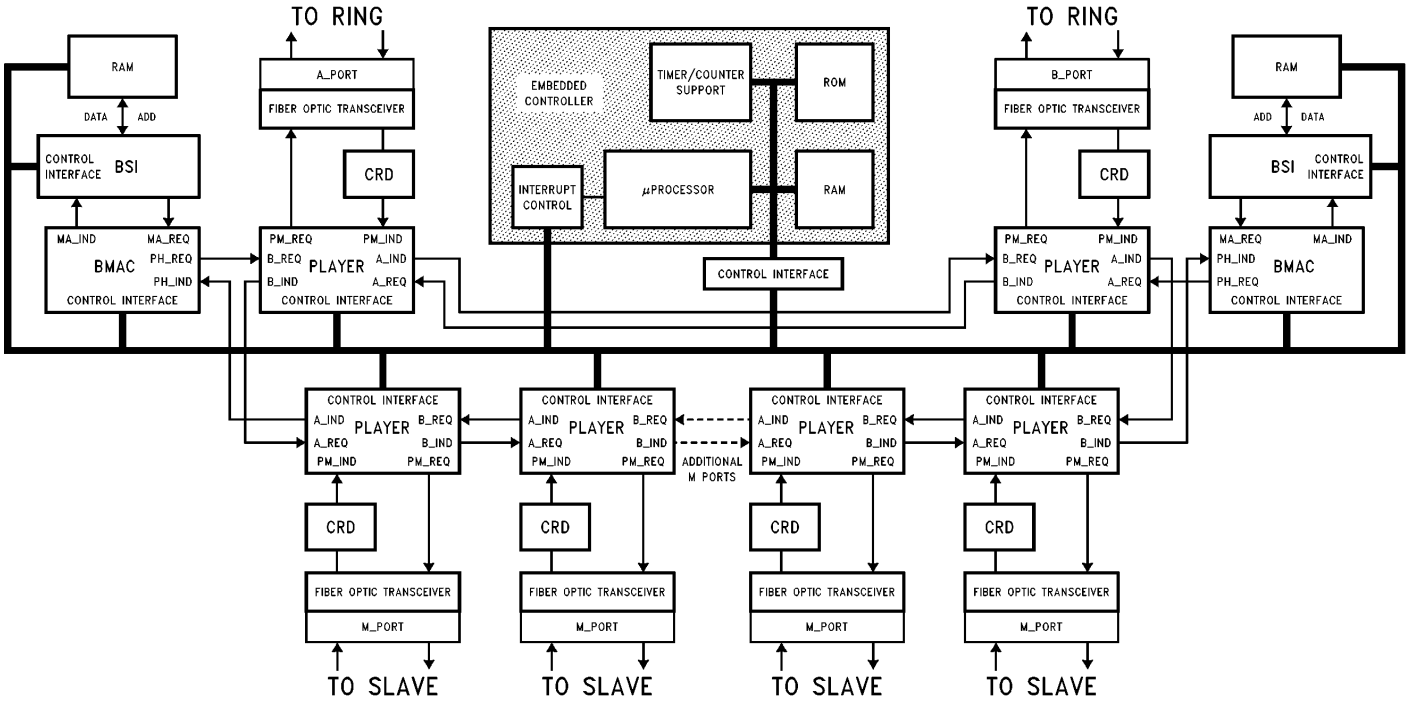
A concentrator requires a moderately high performance processor with support peripherals such as timers and interrupt control. In many designs it is preferable to use a processor that includes these support peripherals. National Semiconductor offers a full range of processors that are appropriate for this application from the HPC family of High Performance Controllers to the 32000 family of processors.

4.2 A Multi-Board Multi-Processor Concentrator

A multi-board concentrator will be used where flexibility and expandability is desired over lower cost. For an organization where adding functionality with time is attractive, the multi-board design is appropriate.

The design is partitioned into three basic cards and a backplane is defined (see *Figure 4-5*). The three cards include: a Master Port Card, a Slave Port Card, and a Peer Port Card.

A controller is present on each card to allow very large configurations beyond the constraints of a single processor. This also decreases the performance requirements of the main processor by reducing the response time requirements. Having a processor on each card coupled with a high enough performance serial bus between all cards also reduces the size and complexity of the backplane to less than 50 signal pins all at or below 12.5 MHz.



TL/F/11120–1

FIGURE 4-1. Single Board Concentrator

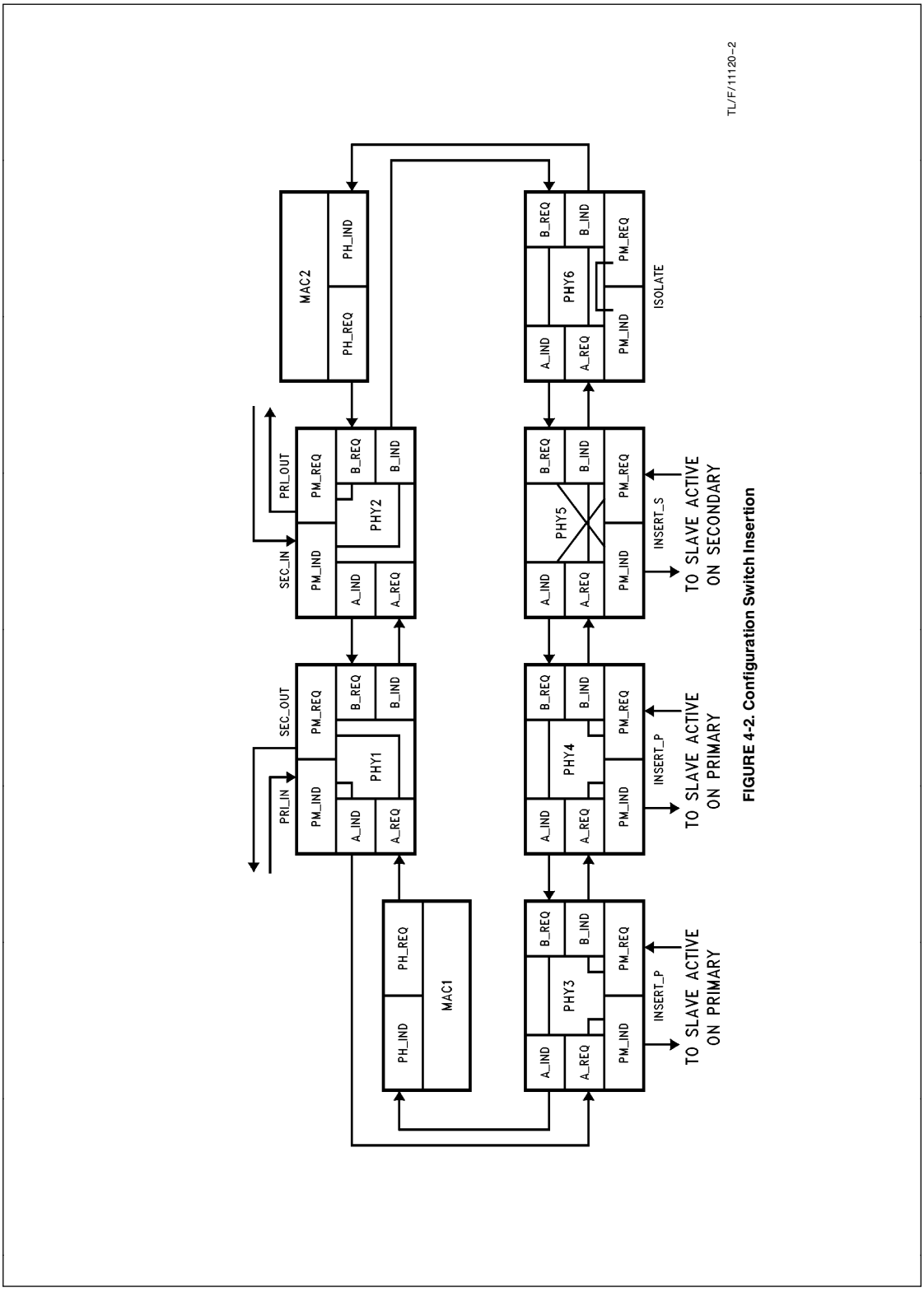


FIGURE 4-2. Configuration Switch Insertion

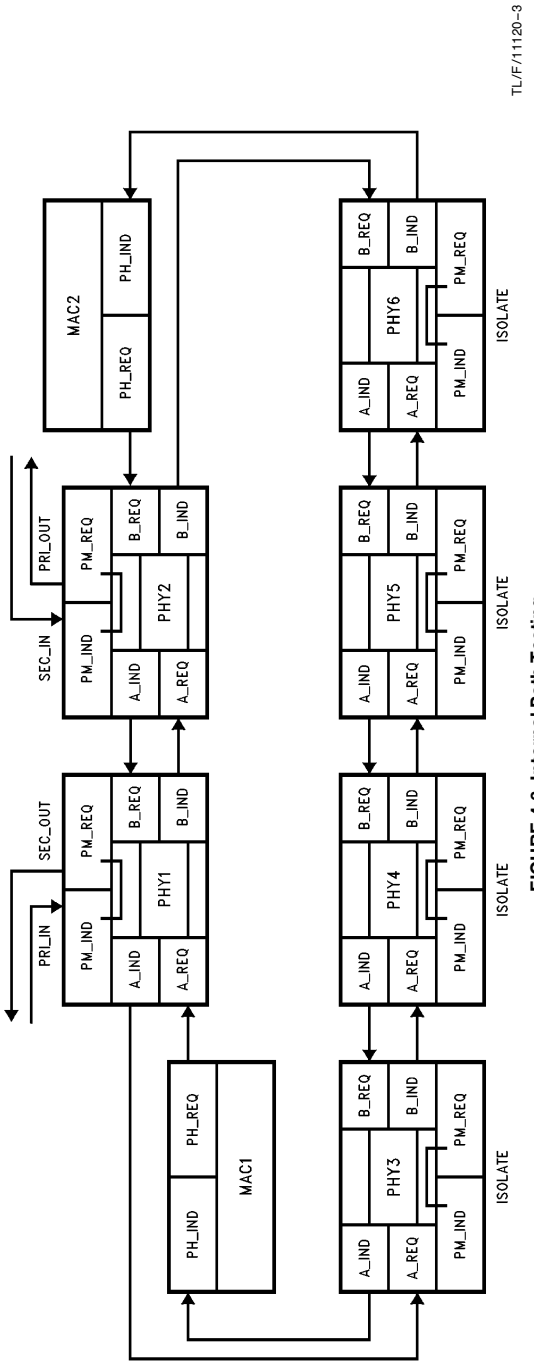


FIGURE 4-3. Internal Path Testing

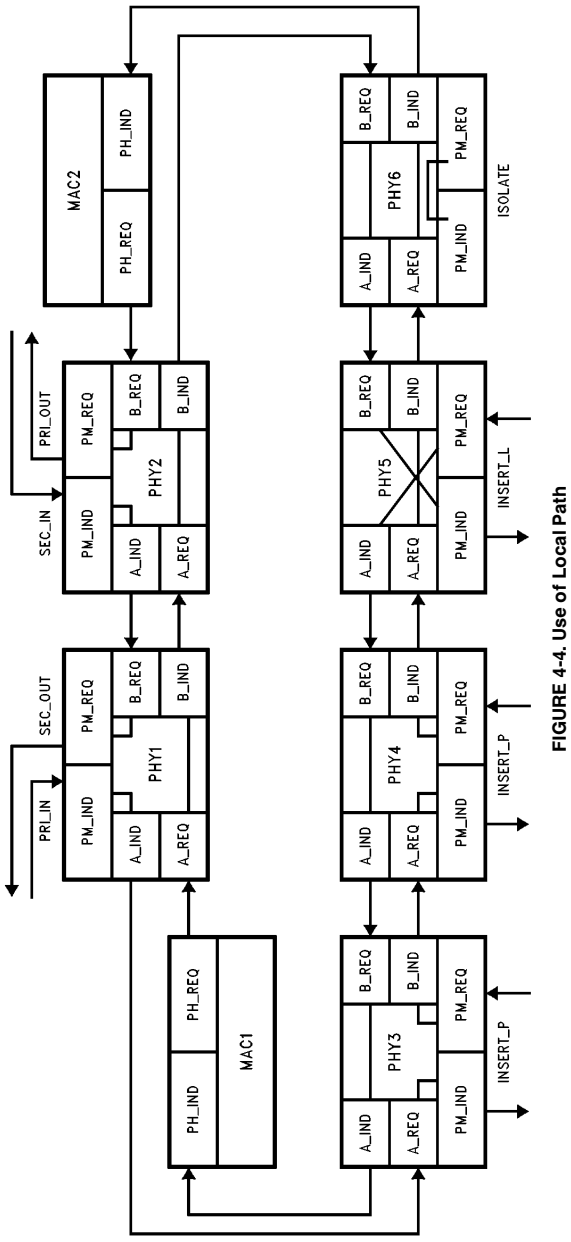
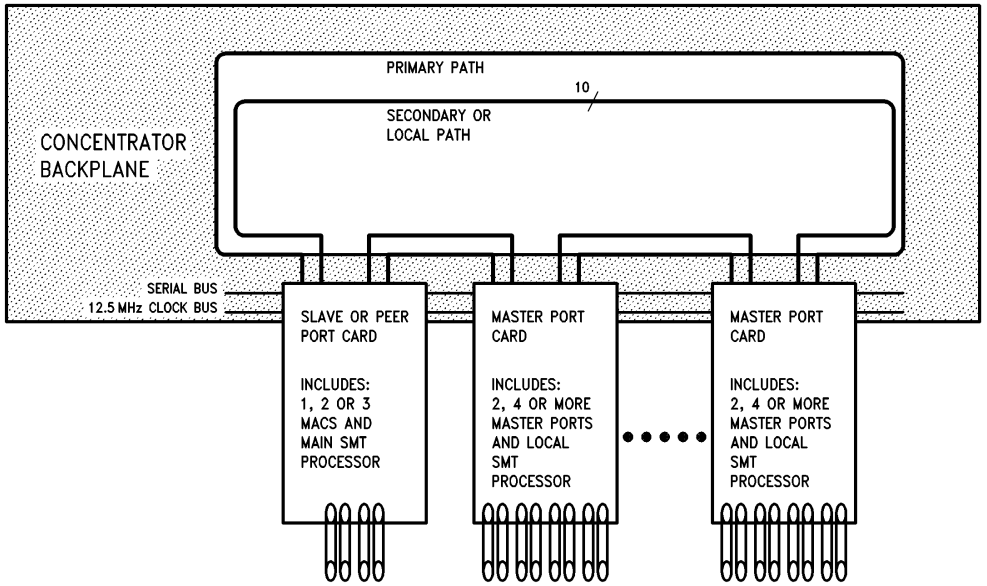


FIGURE 4-4. Use of Local Path



TL/F/11120–5

FIGURE 4-5. Concentrator Backplane

Master Port Card

The Master Port card provides several (2, 4, 8+) M Ports. The Card shown in *Figure 4-6* shows 4 M Ports. These M Ports are typically connected to the S Port of slave stations. The slave station could be a single attach workstation or single attach concentrator at the next lower (or same) level of the concentrator tree. The M Ports could also be used to connect Dual Attach Stations and Dual Attach Concentrators where Dual Homing is permitted. In these configurations, to maximize redundancy, the two attachments would be connected onto two different concentrators.

The M Port card can be designed with multiple PLAYER devices (PHY layers). The number of ports per card is restricted by the physical limitations of the card such as the space required by the connectors, optical components and PLAYER and CRD devices. The processor or microcontroller must service physical SMT tasks within the maximum times specified in the Standard (T_React, PC react, etc.). The increase in service latency that accumulates as additional PLAYER devices are connected to the control bus might also limit the number of Ports that can be supported on a card for a given processor configuration. SMT tasks are serviced locally by the processor and reported back to the main SMT processor located on the slave (or peer) card.

The National Semiconductor High Performance Microcontroller (HPC) is well suited for this local task. It provides low interrupt response time, fast 25 MHz operation, embedded timers for CMT and serial communications capabilities for implementing a serial bus.

Peer and Slave Port Cards

The Peer and Slave Port Cards provides ports for connection into the larger Ring. With the Peer Port Card, A and B Ports are provided for connection into either the trunk ring or a concentrator tree. With the Slave Port Card, an S Port is provided for connection into a concentrator tree.

Figure 4-7 shows a Peer Port Card design which includes the A and B Ports, two MACs and the main SMT processor. The Slave Port Card shown in *Figure 4-8* includes one S Port, one MAC and the main SMT processor. An advantage of placing the main SMT processor on the same card as the MAC implementations is to avoid providing support for a full databus on the backplane or on another potentially expensive special connector. With the DP83200 chipset including the DP83265 BSI, System Interface device, space efficient and cost-effective memory interfaces are possible.

The Clock Distribution Device provides all of the clocks required for the DP83200 chipset. Since there is typically only one Slave or Peer Port in a system, this card drives the 12.5 MHz reference clock onto the backplane. Each card has a local CDD device which uses the reference to generate the appropriate clocks for the card. Clock distribution in very large concentrators is discussed separately.

The SMT processor interfaces directly to the local PLAYER, BMAC and BSI devices across the 8-bit Control Bus. This bus is used for access to registers, parameters and counters (configuration switch, line state detector, statistic counters, etc.). The SMT processor also interfaces to the local memory used for frame transactions (PDUs). The SMT processor handles all lower level SMT tasks (PCM, CFM, etc.). This main SMT processor also uses a serial controller, to interface to the other processors in the concentrator across the serial bus.

National Semiconductor offers a variety of processors and controllers for this task. The NS32GX320 is a 15 MIP CISC machine with on-chip cache, timers, interrupt control and DMA support. The NS32CG160 is a lower performance and lower cost alternative and is suitable for the SMT function as is the HPC. The HPC also includes an on-chip 1 MHz serial interface and an on-chip UART that could be used for a local RS-232 connection. This connection can be used for diagnostic purposes, or for connection to a network analyzer console.

Backplane Design

The cards plug into a common backplane as shown in *Figure 4-4.* The backplane provides the interconnection between the various cards and provides a common clock reference and the serial bus. Less than 50 signal pins are necessary, all at or below 12.5 MHz so no sophisticated backplane design is required.

At each slot, two complete token paths are provided. The 10-bit internal National code is sent over the backplane. For each path, 10 input and 10 output signals are used. For each slot, 40 signals are present. The output of one slot is connected to the input of the next slot in order to create the token paths. The two physical paths are used by SMT as in the single board design.

A backplane design can use special shorting connectors on a terminator card which would keep the daisy chain paths connected when no board is plugged into a slot.

In a single processor design, the backplane must also provide a control path for inter-board communications. The control bus would have to be extended across the backplane in order to provide access to all of the devices. Depending on the capabilities of the main processor, the limitations of its response time, the desired extendability of the concentrator, this may or may not be warranted.

The requirements placed on the serial bus/ring are rather minimal if partitioning of the SMT functions is done well. Typically, all of PCM would be done locally on each M Port Card and the simple portions of CMT as well. One very simple protocol to run on a serial bus uses a two or three wire interface where a main processor polls the other processors in the system, one at a time. Small (size and cost) RS-485 transceivers such as National's DS75176B or DS3695 can be used for a simple interface to the backplane.

Concentrator Extensions

The backplane defined could be viewed as links between stations. The SMT standard only makes assumptions about the MAC at the exit ports and makes provisions for additional MACs within concentrators. This allows additional cards to be developed to provide a bridging function either to other rings, or even between paths.

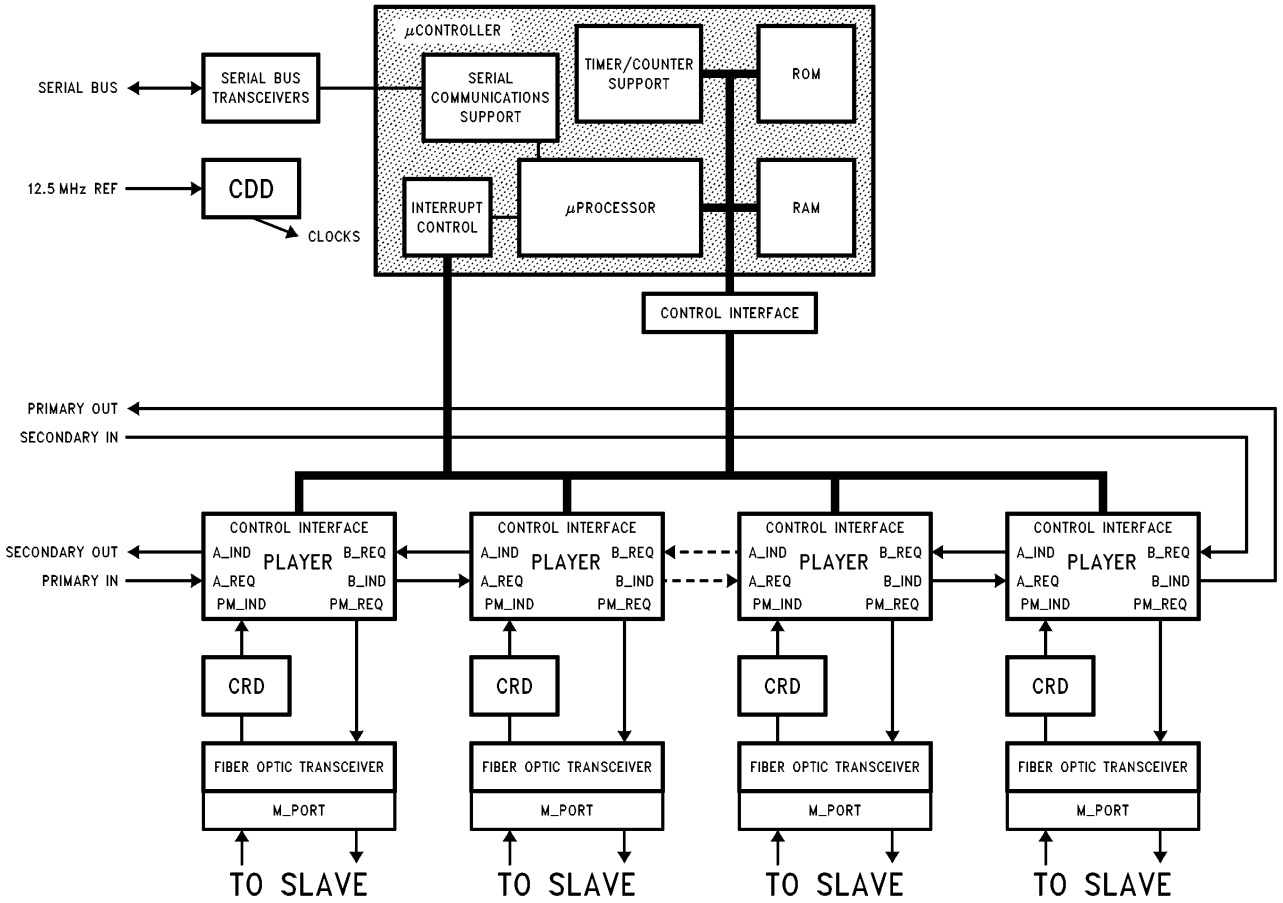
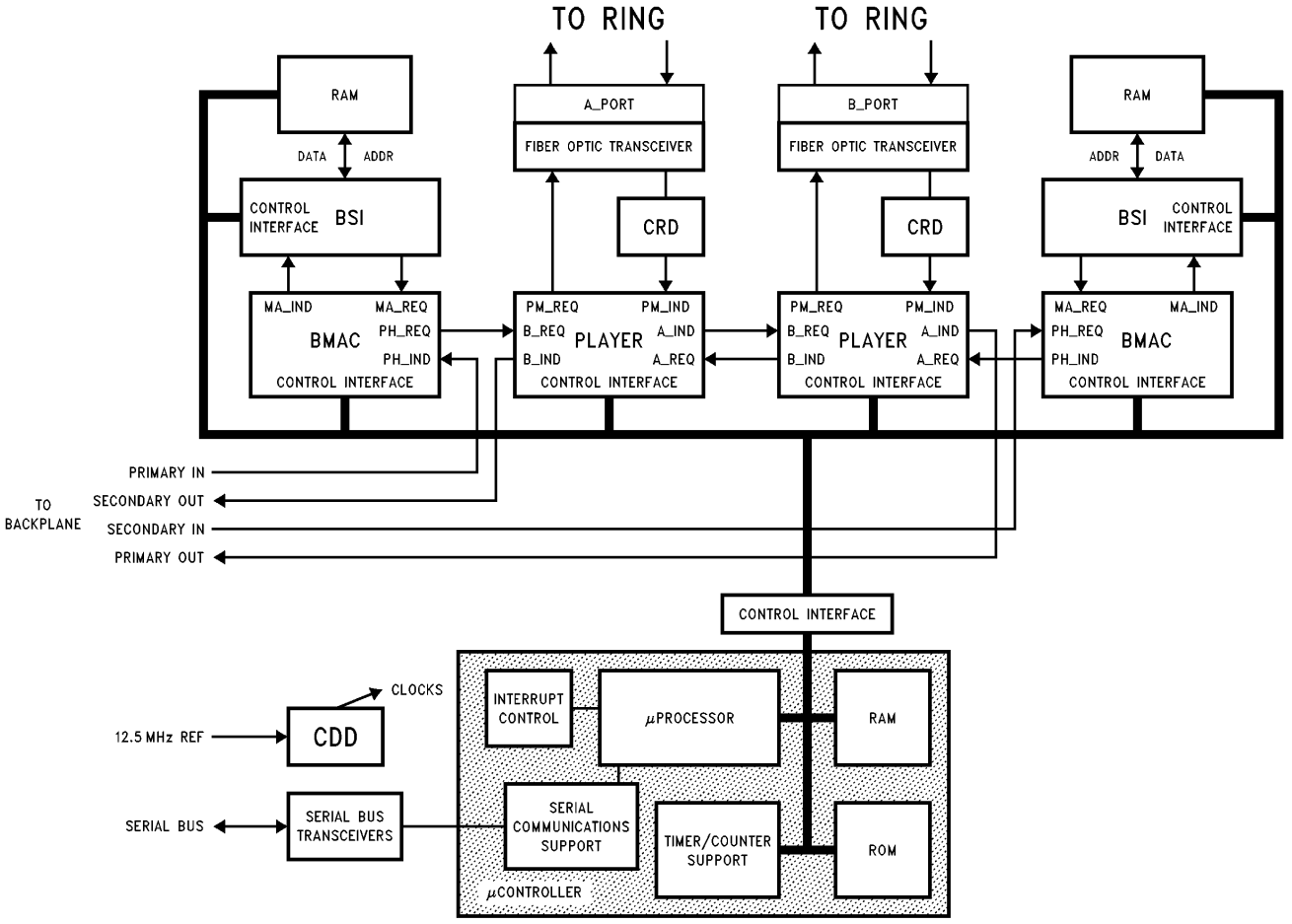
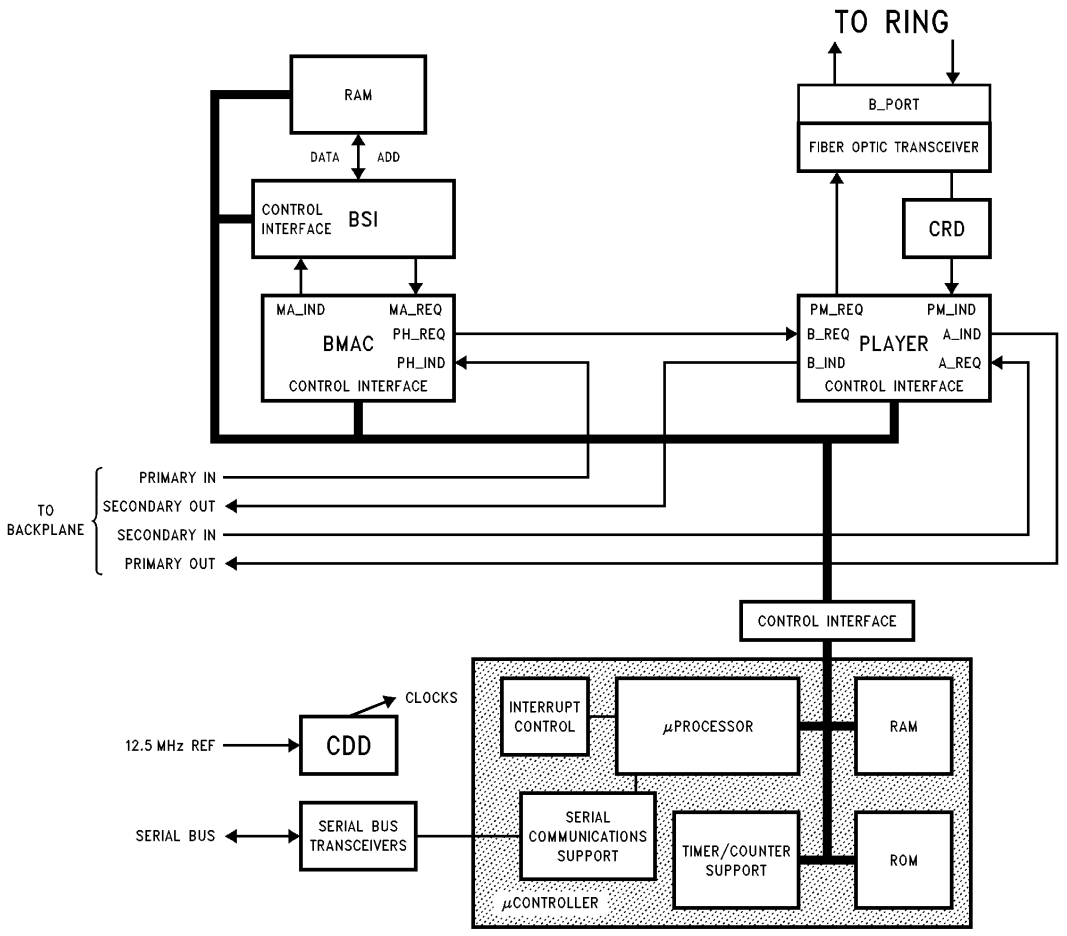


FIGURE 4-6. Master Port Card



TL/F/11120–7

FIGURE 4-7. Peer Port Card



TL/F/11120–8

FIGURE 4-8. Port Board

Another possibility for add in cards for a concentrator are special network monitoring cards and network testing cards.

Another extension is the ability to support live insertion of boards to avoid interruptions. This might even involve intelligent backplanes that could involve sophisticated multiplexing functions.

A standard for a concentrator backplane is a likely possibility at some point so that many different cards could be developed. This would allow customers to build concentrators with boards from many different vendors just as standard buses are used today to create customized computing environments.

This does cause one problem, when does a concentrator stop being a concentrator?

5.0 SMT NOTES

Several topics relating to implementations of Station Management for a Concentrator are worthy of discussion, many of these are covered below. Some of these topics relate to SMT implementations for stations as well.

5.1 Processor Performance Requirements

The most stringent requirement on an implementation of PCM using the PLAYER device is the Active to Break transition. The Standard requires that this transition takes place within 3 ms. This implies that within 3 ms after an interrupt is generated by the PLAYER device, a register is written to send out Quiet symbols and change the programming of the configuration switch. By using a low end processor to control several M Ports, the requirements on the main processor are reduced significantly. When bringing links up and going through the PCM signalling, the timing constraints are much less severe since there are no requirements for bringing up multiple links simultaneously. It is acceptable to distribute processing with several PLAYER devices controlled by a single processor.

5.2 Path Test

A complete path test in a concentrator is invaluable for isolating problems. Especially in large configurations, the ability to isolate errors, such as marginal connectors or connections, faulty components, etc., is extremely important.

The two complete token paths suggested in both example designs allows operational rings to be created within concentrators to check connectivity and components. The DP83200 chipset provides numerous features that aid in isolating problems down to the chip level. Modes such as 4 loopback paths, error insertion and statistic counters are just a few of the features included that give true network/system testing capability without complex external circuitry or equipment.

By having two complete paths, if a fault exists, the fault can be isolated precisely by careful programming of the configuration switch (see *Figure 4-3*). Once it is known which configurations are physically possible, it then becomes necessary to decide which paths should be connected and when this should be done. The current configuration must always be valid and up to date (there are still conflicting views on how this information should be kept in the MIB).

5.3 Moving MACs between Paths

In designs with fewer MACs than paths, it is necessary to move the MAC between paths. In many cases it is easier to just put a MAC on each path than to build all of the necessary software interlocks.

Before moving a MAC from one path to the other, it is necessary to remove all frames transmitted by this MAC in order not to create ownerless frames on the path that the MAC is leaving.

With the BMAC device, one way to accomplish this is to enable the Inhibit Token Capture option (Option.ITC) for at least one ring latency (after this station issues the token, if it is being held) before changing paths. Before leaving, it is also helpful to capture the token in order to avoid corrupting any frames. When placing the MAC on the new ring, it is necessary to insert while claiming. It is not possible to guarantee graceful entry if a token is not being held on that path.

When the situation exists for this station to scrub the ring of ownerless frames, several options are provided. The BMAC device provides a robust stripping mechanism that can be used without any destructive side effects, namely the STRIP option where stripping continues until a My__Void frame comes back around the ring, thus stripping all of the ownerless frames. This occurs automatically after this station wins Claim before the first token is issued. Similarly, the Inhibit Repeat option or the ability to block the MAC input from the PLAYER device for more than one ring latency also provide this function.

5.4 Graceful Insertion of Slaves

The graceful insertion (also known as smooth or bumpless insertion) of slave stations or slave concentrators into a ring allows stations to be placed into a ring without disrupting other stations in the ring. Unlike a ring consisting only of Dual Attach Stations where the ring must go through at least the Claim Process on each insertion/deinsertion and possibly cause frames to be corrupted, with concentrators it is possible to provide the capability to insert and deinsert stations gracefully without any data corruption.

Two methods of varying complexities are shown for graceful insertion.

With the first method to gracefully insert a slave the following must be accomplished:

1) make the slave ready to bring the ring operational on the next received token
2) capture a token on the path on which the slave will be inserted
3) while holding the token, modify configuration switch of the M Port to insert the slave
4) hold the token for at least actual ring latency of the new ring (the inserted slave concentrator might be bigger than the rest of the ring)
5) issue the token

Step 2 above requires a MAC on the path on which the slave will be inserted. The slave is inserted into the ring in step 3 above. The token must be held for a ring latency in order to guarantee that no frames are corrupted. This could occur if a slave connected to this concentrator transmitted a frame to an upstream slave connected to this concentrator. To avoid a TRT expiration in a downstream station while holding the token, a pool of synchronous bandwidth could be allocated and shared by all concentrators on the ring. This can be done using asynchronous transmission with THT disabled (one of the service classes provided by the BMAC device).

Depending on the assumptions you can rely on concerning a slave station after PCM, Step 1 may or may not require a MAC on a local path in a concentrator. If you can make the assumption that the slave will not enter claim because of TVX expirations and that its TREQ is set to TMAX, then a MAC would not be required. Otherwise a MAC would be required.

With this method, the theoretical possibility that a station will not accumulate lateness properly and will cause an unnecessary entry to Claim still exists. In the MAC, TRT is not cleared when a late token arrives, only late count is cleared. This means that if the ring is operating at heavy load, all stations in the ring will have some accumulated lateness. An inserted station cannot possibly know this and may hold the token longer than it would have if it had accumulated lateness. If it does, then a downstream station that had been accumulating lateness will consider the lack of a token arrival as a reason to enter Claim. Since this condition is very load and location dependent, and since Claiming is the only consequence (which it would be anyway if graceful entry was not attempted) it certainly doesn't hurt to try graceful entry. It is analogous to building a cache, if you can build one with a high hit rate (i.e., gracefully insert), do you? Implementors will need to decide if the payoff from graceful insertion is worth the additional complexities.

Another method to gracefully insert would be to capture a token on the path on which the slave will be inserted on and then always have the slave station go into the ring claiming or beaconing. This avoids the problems of accumulated lateness, at the expense of bringing the ring down for a potentially longer time, however no data is corrupted and only one MAC is required. Again this brings up questions regarding the assumptions that can be made about the default parameters of the slave station.

More work is necessary regarding the assumptions a concentrator can make about slaves upon insertion and how slaves should be inserted. Unfortunately, most proposals require services that are currently optional in SMT.

For example, a station could come into a ring and always default to a dual homing configuration. This would mean that A Ports are always attached to the primary ring, B Ports to the Secondary and S Ports to the primary. The Slave would be attached with default parameters and a default configuration. Once inserted into the ring the Slave would contact the Master in the concentrator using a well defined group address. In this way the Master MAC would determine its slaves quickly, and the slave would determine its Master. After this discovery process they could then use the standard parameter management frames to exchange configuration information. The Master would also have the ability to modify the Slave's default parameters.

This is currently unworkable because the ability to receive SMT group addresses is an optional facility as are the parameter management frames. In a future revision of SMT this may change.

6.0 CONCENTRATOR CLOCKING CONSIDERATIONS

Poor layout or clock distribution can forfeit the low error rate benefits of FDDI's fiber optic links. The greater number of PHY elements in concentrators exacerbates any problems in these areas. National Semiconductor designed the DP83241 to simplify the clock distribution.

Concentrators have more stringent packaging demands than most end attachments due to environmental, modularity and reliability considerations. They may range from a single board desktop implementation with a small number of master ports to large modular designs that support hot insertion and removal of master port cards. Though systems at these two extremes require different clocking structures, the DP83241 Clock Distribution Device provides reliable solutions.

The BSI, BMAC and PLAYER devices require 12.5 MHz TTL clocks for internal operation and communication between one another. The PLAYER device also requires a 12.5 MHz ECL clock to drive the parallel to serial conversion in the transmitter and a 125 MHz ECL clock to shift each bit out of the transmitter. The PLAYER device imposes specific timing relationships among these clocks, with relatively tight tolerances between the two ECL clocks and substantially relaxed tolerances between the two 12.5 MHz clocks. The CDD device guarantees the relationships of the ECL and TTL clocks that it generates to significantly tighter tolerances than the PLAYER device requires. A concentrator clocking structure must distribute and deliver these signals without introducing more skew than the PLAYER device can accept.

Appropriate layout and loading considerations must be followed in order to avoid unnecessary noise and skew. The PLAYER device at each port requires 12.5 MHz ECL and TTL clocks with a fixed relationship between them that must be preserved. In addition, the 125 MHz signals used for serial transmission have Standard defined jitter requirements.

In a single board concentrator, a single CDD device could be used to drive all devices on the board provided that the skews between the various clocks can be matched. Alternatively, one CDD device could be used for every two ports and a 12.5 MHz reference to be distributed around the card. This approach also minimizes the layout constraints as all clock lines can be kept as short as possible, with less variability. The layout recommendations for Dual Attach Stations can be applied.

In a multi-board design the above principle can be extended and on the backplane only the 12.5 MHz signal (from one of the Peer or Slave Port Cards) need be distributed to all boards in the concentrator. On each board the local CDD devices use it as a reference and generate all other clocks.

Flight Time Cancellation

Each board passes signals to the next downstream board and the propagation time between the adjacent boards is accounted for in the Set Up and Hold Times. Note that only one load is present for each board, not multiple loads, even in a fully loaded backplane. However at the endpoints of the backplane where the signals must be looped around, the margin of the setup and hold times may not be sufficient to accommodate the propagation time. In concentrators with less than 4 slots this may not pose a problem, but in concentrators with more than four slots, the backplane flight time, when added to the chip propagation delay from the local byte clock, would exceed the setup requirements at the next downstream port. This case therefore requires special attention.

The flight time that we are concerned about is the signal propagation time on the backplane of the return path. This propagation time needs to be measured once for each backplane. To compensate for this propagation delay, the CDD device provides ten different phases of the 12.5 MHz local byte clock. The appropriate phase of the CDD device could then be used to latch the data at the input to the next downstream card. The correct phase is chosen to match the set up and hold requirements of that latch such that the set and hold requirements of the next port on the PLAYER or BMAC devices are met. Five of the ten phases of the CDD device are selectable at either 8 ns or 16 ns increments to maximize the flexibility and range of its use in compensating for this design constraint.

In summary, for each path in a concentrator, an additional latch is used at the first input after the return path and is clocked by an appropriate phase of the 12.5 MHz LBC. For all other backplane connections, this additional latching is not required because the Setup and Hold times provide sufficient margin to account for clock skew and propagation time. (If this is not the case, additional latching may be required.)

Conclusion

The Concentrator creates additional degrees of configuration and greater reliability for FDDI networks. The National Semiconductor DP83200 FDDI chipset provides the basis for a variety of robust concentrator designs and offers many ways in which National's customers can differentiate their products.

Acknowledgements

Thanks to Gabriel Li, Dave Talaski, Nanette Talaski, Mehdi Salamat, Michael Yipp, and Simon Stanley of National Semiconductor, Bob Grow and Ron Perloff of XDI and Jim Hamstra of Stanatek for their assistance in this effort.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottinghill, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
Fax: (3) 558-9998