400085

National Semiconductor Corporation

Random Access Memory Databook

- *STATIC Rams*
- *TTL Rams*
- *TTL FIFOs*
- *ECL Rams*

1987 Random Access Memory Databook National Semiconductor

Random Access Memory
DATABOOK

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Random Access Memory Databook Introduction

The Random Access Memory databook contains comprehensive technical information on National's volatile memory product lines. National offers a breadth of static-RAM products from high-speed, low-power MOS SRAMs to ultra-high-performance ECL RAMs.

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Section 1

Static RAMs

Section 1 Contents

National Semiconductor Corporation

February 1987

NMC2147H 4096 x 1 Static RAM

General Description

The NMC2147H is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

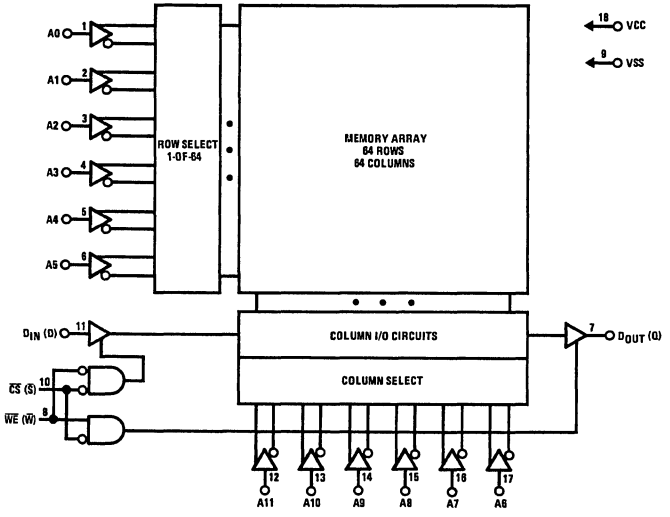
The separate chip select input automatically switches the part to its low power standby mode when it goes high.

The output is held in a high impedance state during write to simplify common I/O applications.

Features

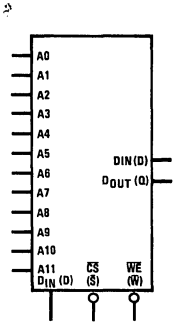
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 35 ns access time
- TRI-STATE® output for bus interface
- Separate Data In and Data Out pins
- Single +5V supply
- Standard 18-pin dual-in-line package
- Available in MIL-STD-883 class B screening

Block Diagram*



TL/D/5257–1

Logic Symbol*



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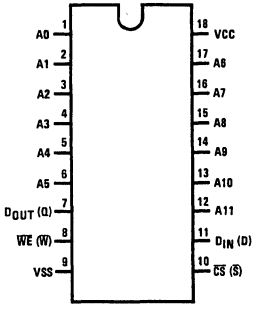
Connection Diagram*

Dual-In-Line Package



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Top View

Pin Names*

A0–A11	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
D_{IN} (D)	Data In
D_{OUT} (Q)	Data Out
V_{CC}	Power (5V)
V_{SS}	Ground

Order Number NMC2147HJ-1, NMC2147HJ-2, NMC2147HJ-3, or NMC2147HJ-3L
NS Package Number J18A
Order Number NMC2147HN-1, NMC2147HN-2, NMC2147HN-3 or NMC2147HN-3L
NS Package Number N18A

*The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin Relative to VSS	−3.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−65°C to +135°C
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table*

$\overline{CS}$ (S)	$\overline{WE}$ ($\overline{W}$)	DIN (D)	DOUT (Q)	Mode	Power
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2147H-3L		NMC2147H-1 NMC2147H-2 NMC2147H-3		NMC2147H		Units
			Min	Max	Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50		50	μA
VIL	Input Low Voltage		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180		160	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30		20	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
COUT	Output Capacitance	VOUT = 0V		6	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper orientation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Level (H-1)	1.5V
Output Timing Reference Level (H-2, H-3, H-3L)	0.8V and 2.0V
Output Load	See *Figure 1*

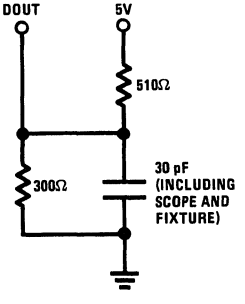

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FIGURE 1. Output Load

*Symbols in parentheses are proposed industry standard.

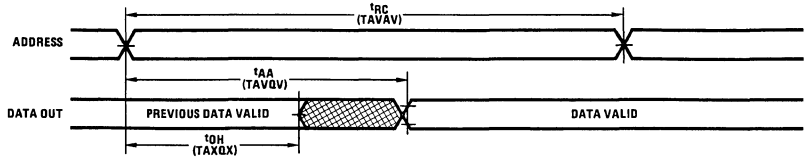
Read Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	35		45		55		70		ns
t_{AA}	TAVQV	Address Access Time		35		45		55		70	ns
t_{ACS}	TSLQV	Chip Select Access Time (Notes 4)		35		45		55		70	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	5		5		10		10		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	30	0	30	0	30	0	30	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		20		20		20		30	ns

Max Access/Current	NMC2147H-1	NMC2147H-2	NMC2147H-3	NMC2147H-3L	NMC2147H
Access (TAVQV—ns)	35	45	55	55	70
Active Current (ICC—mA)	180	180	180	125	160
Standby Current (ISB—mA)	30	30	30	20	20

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



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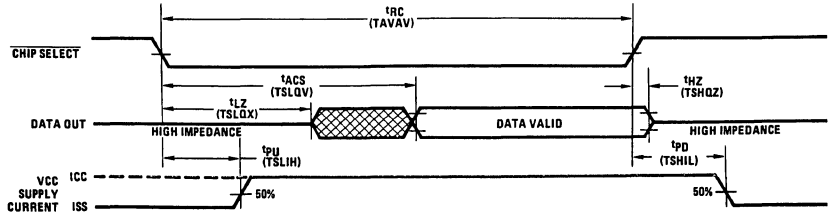
Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



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Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

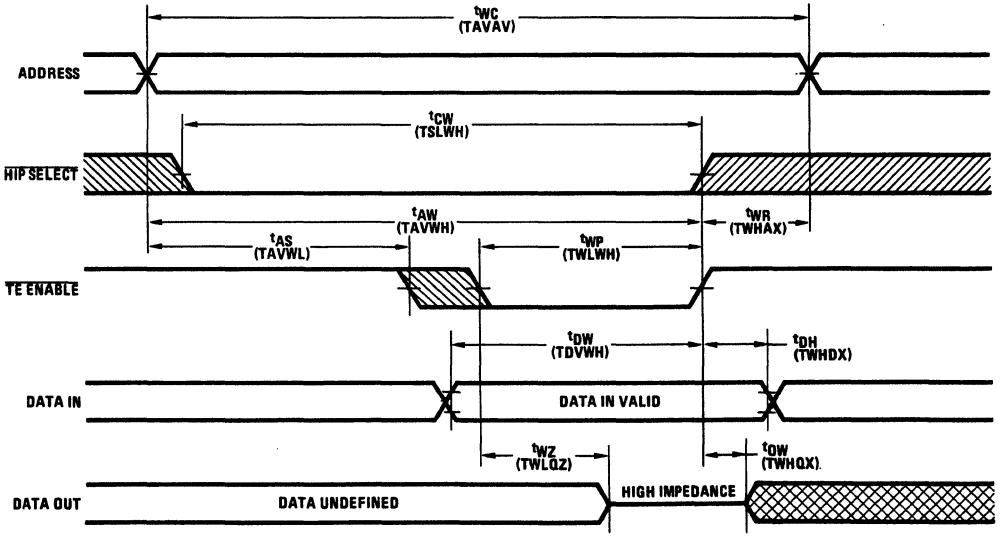
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	35		45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	35		45		45		55		ns
t_{AW}	TAVWH	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	20		25		25		40		ns
t_{WR}	TWHAX	Write Recovery Time	0		0		10		15		ns
t_{DW}	TDVWH	Data Set-Up Time	20		25		25		30		ns
t_{DH}	TWHDX	Data Hold Time	10		10		10		10		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	20	0	25	0	25	0	35	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 5)	0		0		0		0		ns

Write Cycle Waveforms* (Note 6)

Write Cycle 1 (Write Enable Limited)



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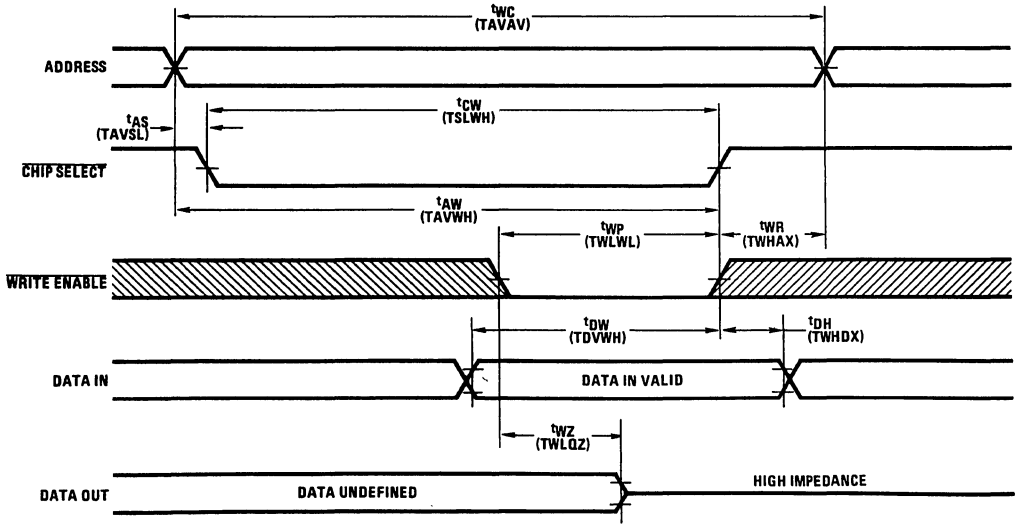
Write Cycle Waveforms* (Note 6)

Write Cycle 2 (Chip Select Limited)



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Note 6: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*The symbols in parentheses are proposed industry standard.

National Semiconductor Corporation

August 1986

NMC2148H 1024 x 4 Static RAM

General Description

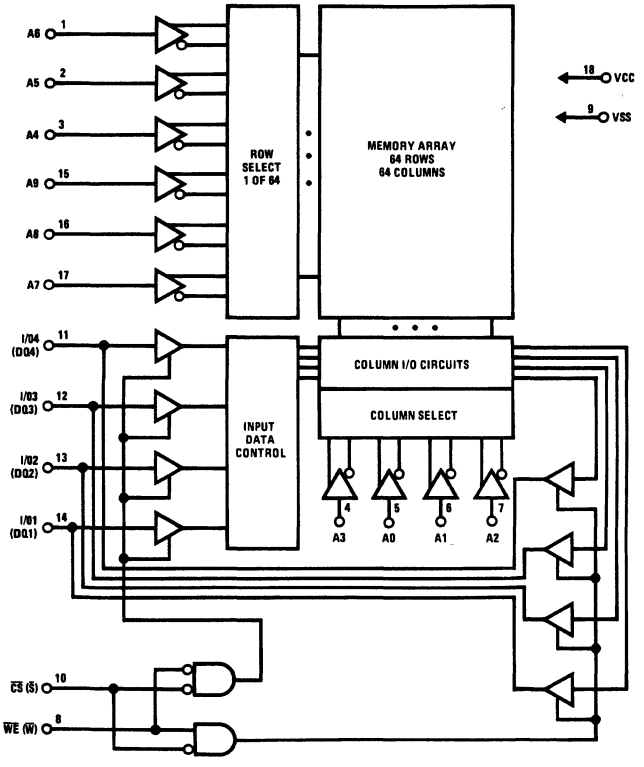
The NMC2148H is a 1024-word by 4-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high. Common input/output pins are provided.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High-speed—down to 45 ns access time
- TRI-STATE® output for bus interface
- Common data I/O pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Block Diagram*



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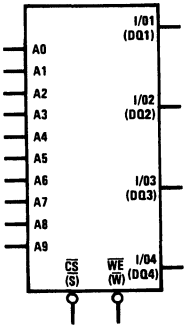
Logic Symbol*



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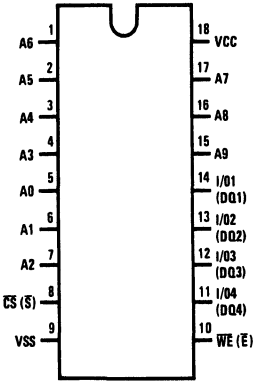
Connection Diagram*

Dual-In-Line Package



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Top View

Pin Names*

A0–A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
1/01–1/04 (DQ1–DQ4)	Data Input/Output
VCC	Power (5V)
VSS	Ground

Order Number NMC2148HJ-L, NMC2148HJ-3L, NMC2148HJ, NMC2148HJ-2 or NMC2148HJ-3
NS Package Number J18A

Order Number NMC2148HN-L, NMC2148HN-3L, NMC2148HN, NMC2148HN-2 or NMC2148HN-3
NS Package Number N18A

*Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage at Any Pin with Respect to VSS	−3.5V to +7V
Storate Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 sec.)	300°C

Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	Mode	Power
H	X	Hi-Z	Standby	Standby
L	L	H	Write 1	Active
L	L	L	Write 0	Active
L	H	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2148H-L NMC2148H-3L		NMC2148H NMC2148H-2 NMC2148H-3		Units
			Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50	μA
VIL	Input Low Voltage		−2.5	0.8	−2.5	0.8	V
VIH	Input High Voltage		2.1	6.0	2.1	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40	mA
|IOS|	Output Short Circuit Current	VOUT = GND to VCC		250		250	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
CI/O	Input/Output Capacitance	VI/O = 0V		7	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Levels	0.8V and 2.0V
Output Load	See *Figure 1*

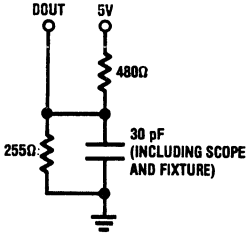

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FIGURE 1. Output Load

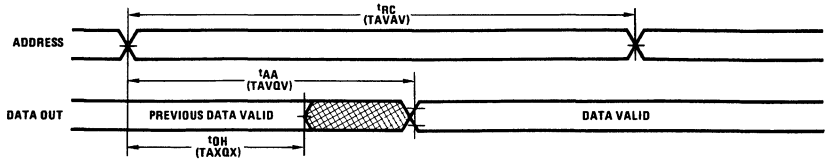
Read Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	45		55		70		ns
t_{AA}	TAVQV	Address Access Time		45		55		70	ns
t_{ACS1}	TSLQV1	Chip Select Access Time (Notes 4 and 5)		45		55		70	ns
t_{ACS2}	TLSQV2	Chip Select Access Time (Notes 4 and 6)		55		65		80	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 7)	20		20		20		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 7)	0	20	0	20	0	20	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		30		30		30	ns

Max Access/Current	NMC2148H-2	NMC2148H-3	NMC2148H	NMC2148H-3L	NMC2148H-L
Access (TAVQV—ns)	45	55	70	55	70
Active Current (ICC—mA)	180	180	180	125	125
Standby Current (ISB—mA)	30	30	30	20	20

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



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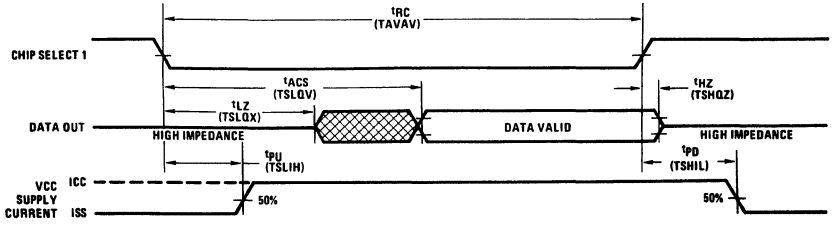
Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



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Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Chip deselected longer than 55 ns.

Note 6: Chip deselected less than 55 ns.

Note 7: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

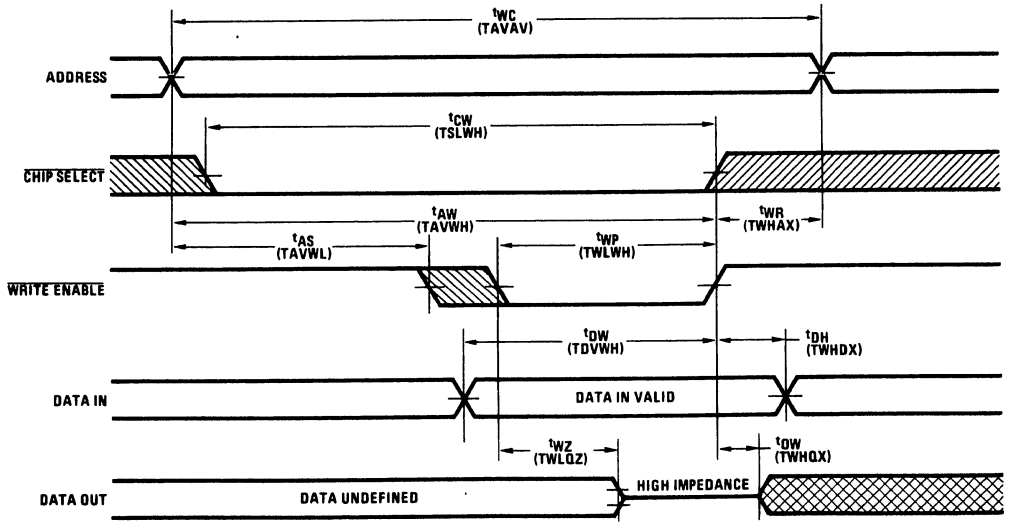
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ±10% (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	40		50		65		ns
t_{AW}	TAVWH	Address Valid to End of Write	40		50		65		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	35		40		50		ns
t_{WR}	TWHAX	Write Recovery Time	5		5		5		ns
t_{DW}	TDVWH	Data Set-Up Time	20		20		25		ns
t_{DH}	TWHDX	Data Hold Time	0		0		0		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 7)	0	15	0	20	0	25	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 7)	0		0		0		ns

Write Cycle Waveforms* (Note 8)

Write Cycle 1 (Write Enable Limited)



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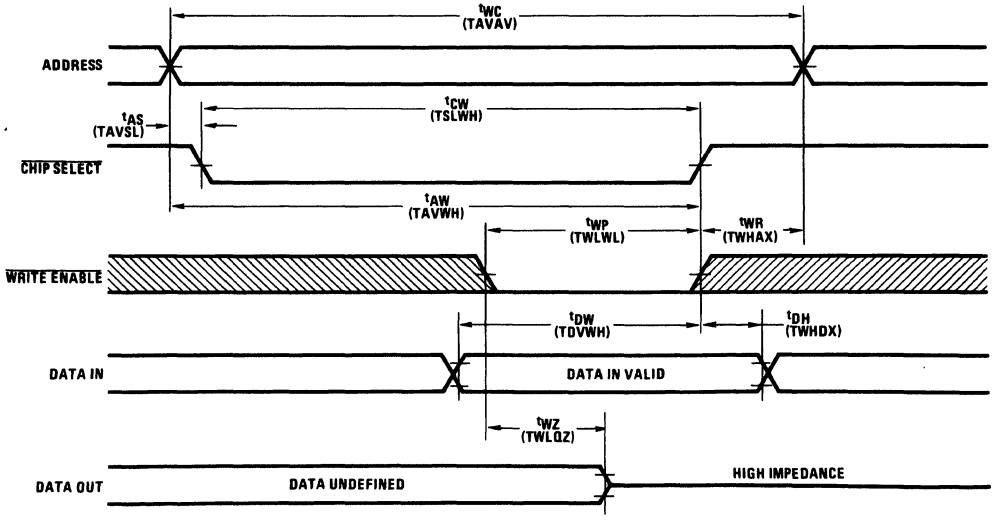
Write Cycle Waveforms* (Note 8) (Continued)

Write Cycle 2 (Chip Select Limited)



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Note 8: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simulataneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*Symbols in parentheses are proposed industry standard.

National Semiconductor Corporation

ADVANCED INFORMATION

microCMOS

NMC6164AN/6164AN-L 8192 x 8-Bit Static RAM

March 1987

General Description

The NMC6164A/6164AN-L is an 8192 by 8-bit, new generation, static RAM. It is fabricated with National's proprietary microCMOS double-polysilicon technology which combines high performance and high density with low power consumption and excellent reliability.

The NMC6164A/6164AN-L operates with a single 5V power supply with ±10% tolerance. Additional battery back-up operation is available (L version) for data retention down to 2V, with low standby current.

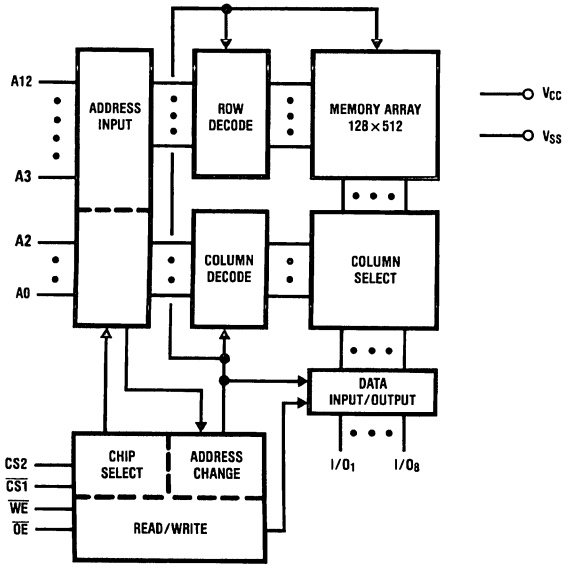
Packaging is available in standard 28-pin plastic DIP.

In addition to the inputs and outputs being TTL compatible, the outputs are also CMOS compatible, in that capacitive loads are driven to V_{CC} or V_{SS}.

Features

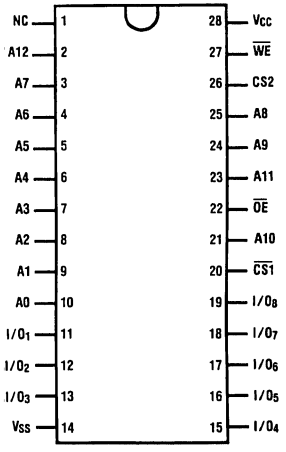
- Single power supply: 5V ±10%
- Fast access time 45 ns/55 ns/70 ns max
- Equal access and cycle times
- Completely static RAM: no clock or timing strobe required
- Low standby power and low power operation
  - Standby: 10 μW, typical
  - Operation: 10 mW/MHz, typical
- Battery back-up operation available (L version) with data retention supply voltage: 2V–5.5V
- Common data input and output, TRI-STATE® output
- TTL compatible: all inputs and outputs
- CMOS compatible: outputs drive capacitive loads to V_{CC} or V_{SS}
- Standard 28-pin package configuration

Block and Connection Diagrams



TL/D/8808–1

Dual-In-Line Package



Top View TL/D/8808–2

Order Number NMC6164AN or NMC6164AN-L
See NS Package Number N28B

Order Number / Parameter	NMC6164AN-45L	NMC6164AN-45	NMC6164AN-55L	NMC6164AN-55	NMC6164AN-70L	NMC6164AN-70
Access Time (ns)	45	45	55	55	70	70
I_{CC} Standby, CMOS	100 μA	2 mA	100 μA	2 mA	100 μA	2 mA

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin Relative to V_{SS}	−0.6V to +7V
Storage Temperature, T_{STG}	−55°C to +125°C
Temperature Under Bias, T_{BIAS}	−10°C to +85°C
Power Dissipation, P_D	1.0W
Current Through Any Pin	100 mA

ESD rating to be determined.

Recommended DC Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
V_{SS} Supply Voltage	0	0	V
V_{IH}, Input High Voltage (Logic 1)			
TTL	2.2	6.0	V
CMOS	V_{CC} − 0.2	V_{CC} + 0.2	V
V_{IL}, Input Low Voltage (Logic 0)			
TTL	−0.3	0.8	V
CMOS	−0.3	0.2	V
T_{OPR}, Operating Temp	0	70	°C

DC Electrical Characteristics at recommended operating conditions

Symbol		Parameter	Conditions	Min	Max	Units
I_{LI}		Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	−2	2	μA
I_{LO}		Output Leakage Current	$\overline{CS1} = V_{IH}$ or CS2 = V_{IL} or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	−2	2	μA
I_{CC}		Active Quiescent Current, TTL	All Inputs at TTL Levels		25	mA
I_{CC}	Std	Active Quiescent Current, CMOS	All Inputs at CMOS Levels		2	mA
	L				100	μA
I_{CC1}		Average Operating Current, TTL	$t_{RC} = t_{RC}$ Min $\overline{CS1} = V_{IL}$ TTL and CS2 = V_{IH} TTL $I_{I/O}$ = 0 mA All Inputs at TTL Levels		50	mA
		Average Operating Current, CMOS	$t_{RC} = t_{RC}$ Min $\overline{CS1} = V_{IL}$ CMOS and CS2 = V_{IH} CMOS $I_{I/O}$ = 0 mA All Inputs at CMOS Levels		30	mA
I_{SB}	Std	Standby Power Supply Current	$\overline{CS1} = V_{IH}$ TTL or CS2 = V_{IL} TTL		4	mA
	L				2	mA
I_{SB1}	Std	Standby Power Supply Current	$\overline{CS1} = V_{IH}$ CMOS or CS2 = V_{IL} CMOS		2	mA
	L				100	μA
V_{OL}		Output Low Voltage, TTL	I_{OL} = 8 mA		0.4	V
		Output Low Voltage, CMOS	I_{OL} = ±10 μA	−0.2	0.2	V
V_{OH}		Output High Voltage, TTL	I_{OH} = −4.0 mA	2.4		V
		Output High Voltage, CMOS	I_{OH} = ±10 μA	V_{CC} − 0.2	V_{CC} + 0.2	V

Capacitance

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V (Note 5)	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V (Note 5)	10	pF

Truth Table

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	Current
Not Selected (Power Down)	*	H	*	*	Hi-Z	I_{SB}, I_{SB1}
	*	*	L	*	Hi-Z	I_{SB}, I_{SB1}
Output Disabled	H	L	H	H	Hi-Z	I_{CC}, I_{CC1}
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}
Write	L	L	H	*	D_{IN}	I_{CC}, I_{CC1}

*Don't Care (H or L) H = Logic HIGH Level L = Logic LOW Level

AC Electrical Characteristics* (Note 1)

Symbol	Parameter	NMC6164AN/6164AN-L						Units
		-45		-55		-70		
		Min	Max	Min	Max	Min	Max	
READ CYCLE (Note 4)								
t_{RC}	Read Cycle Time	45		55		70		ns
t_{AA}	Address Access Time		45		55		70	ns
t_{CO1}	Chip Selection ($\overline{CS1}$) to Output Valid		45		55		70	ns
t_{CO2}	Chip Selection (CS2) to Output Valid		45		55		70	ns
t_{OE}	Output Enable ($\overline{OE}$) to Output Valid		20		25		30	ns
t_{LZ1}	Chip Selection ($\overline{CS1}$) to Output Active (Note 12)	15		15		15		ns
t_{LZ2}	Chip Selection (CS2) to Output Active (Note 12)	15		15		15		ns
t_{OLZ}	Output Enable ($\overline{OE}$) to Output Active (Note 12)	5		5		5		ns
t_{HZ1}	Chip Deselection ($\overline{CS1}$) to Output in Hi-Z (Notes 2 and 3)	0	20	0	25	0	30	ns
t_{HZ2}	Chip Deselection (CS2) to Output in Hi-Z (Notes 2 and 3)	0	20	0	25	0	30	ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z (Notes 2 and 3)	0	15	0	20	0	25	ns
t_{OHA}	Output Hold from Address Change	5		5		5		ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	45		55		70		ns
t_{CW1}	Chip Selection ($\overline{CS1}$) to End of Write (Note 10)	40		50		60		ns
t_{CW2}	Chip Selection ($\overline{CS2}$) to End of Write	40		50		60		ns
t_{AS}	Address Setup Time (Note 7)	0		0		0		ns
t_{AW}	Address Valid to End of Write	40		50		60		ns
t_{WP}	Write Pulse Width (Note 6)	35		40		50		ns
t_{WR1}	Write Recovery Time from $\overline{CS1}$ (Note 8)	0		0		0		ns
t_{WR2}	Write Recovery Time from CS2 (Note 8)	0		0		0		ns
t_{WHZ}	Beginning of Write to Output in Hi-Z (Note 9)	0	15	0	20	0	25	ns
t_{DW}	Data Valid to Write Time Overlap	20		25		35		ns
t_{DH}	Data Hold from End of Write	0		0		0		ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z	0	15	0	20	0	25	ns
t_{OW}	Output Active from End of Write	0		0		0		ns

*Applies to Standard and L Versions.

Note 1: AC test conditions T_A = 0°C to +70°C, V_{CC} = 5V ±10%.

Note 2: t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are determined as:
High to TRI-STATE, measured V_{OH} (DC) −0.10V
Low to TRI-STATE, measured V_{OL} (DC) +0.10V

Note 3: At any given temperature and voltage condition, $t_{HZ\ MAX}$ is less than $t_{LZ\ MIN}$, both for a given device and from device to device (guaranteed, not tested).

Note 4: $\overline{WE}$ is high for read cycle.

Note 5: T_A = 25°C, f = 1.0 MHz. This parameter is sampled and not 100% tested.

Note 6: A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$ and a high CS2 and a low $\overline{WE}$.

Note 7: t_{AS} is measured from the address changes to the beginning of the write.

Note 8: t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of the write cycle.

Note 9: If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. At this time, the data input signals of opposite phase to the outputs must not be applied.

Note 10: If the $\overline{CS1}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the outputs will remain in a Hi-Z state.

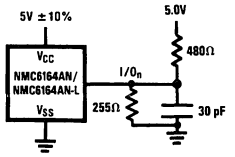
Note 11: CS2 controls the address buffers, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, D_{IN} buffer and $\overline{OE}$ buffer. When CS2 controls the data retention mode, all inputs (address, I/O, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$) can be in the high impedance state. When $\overline{CS1}$ controls the data retention mode, CS2 must be at V_{IH}, CMOS. All other input levels (address, $\overline{OE}$, $\overline{WE}$, I/O) can be in the high impedance state.

Note 12: Output active level is defined as steady state TRI-STATE level ±0.1V.

AC Test Conditions

Input pulse levels	V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall times	5 ns
All Input timing reference levels	1.5V
Output timing reference levels	V_{OH} = 2.0V, V_{OL} = 0.8V

AC Test Load

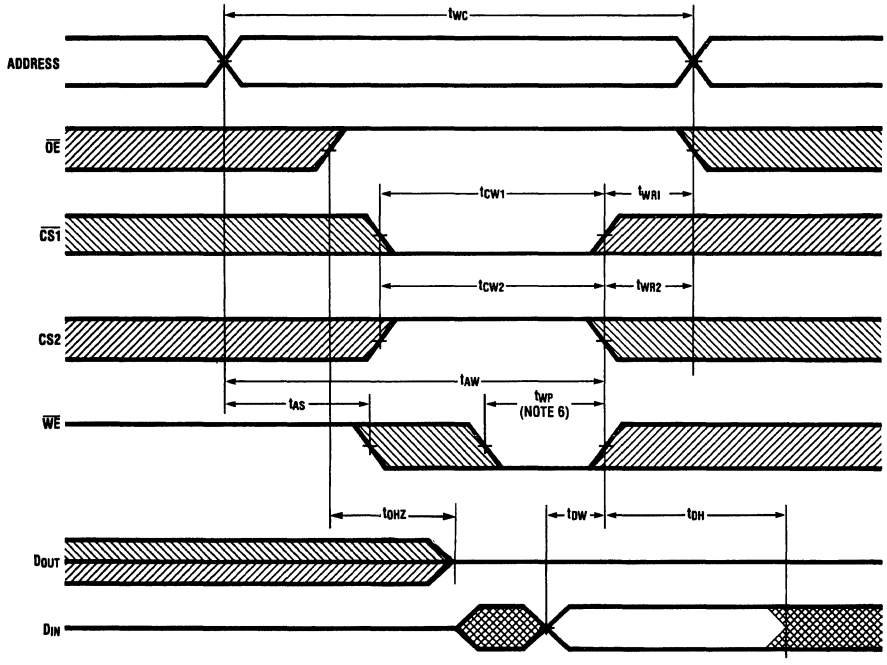


(Including Jig & Probe Capacitance)

TL/D/8808–3

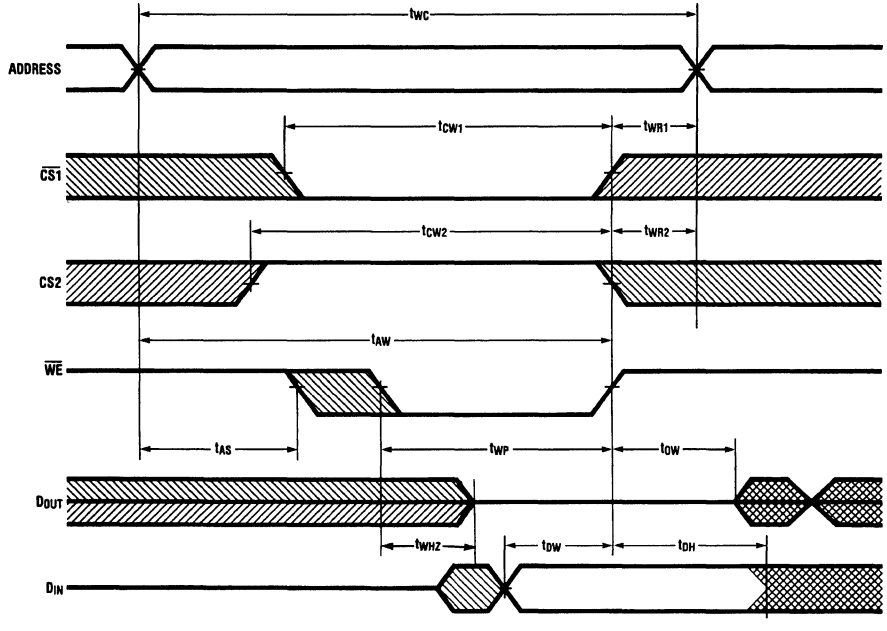
Timing Waveforms

Write Cycle 1 ($\overline{OE}$ Clocked)



TL/D/8808–4

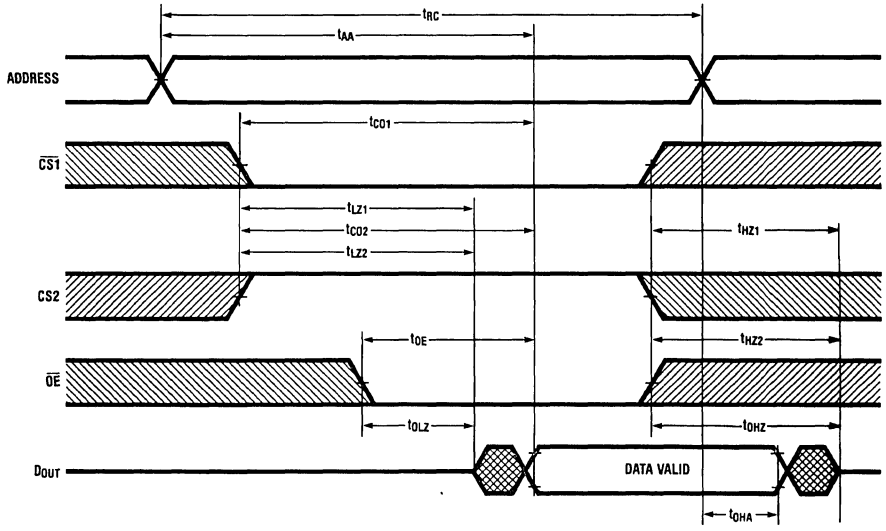
Write Cycle 2 ($\overline{OE}$ Low Fixed)



TL/D/8808–5

Timing Waveforms (Continued)

Read Cycle ($\overline{WE}$ = V_{IH})



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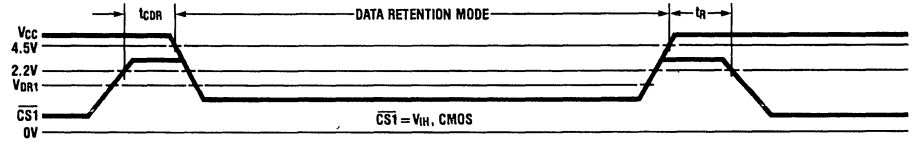
Low V_{CC} Data Retention (L Version)

Symbol	Parameter	Conditions	Min	Max	Units
V_{DR1}	V_{CC} for Data Retention	$\overline{CS1}$ > V_{IH}, CMOS (Note 11) CS2 > V_{IH}, CMOS	2.0	5.5	V
V_{DR2}	V_{CC} for Data Retention	CS2 < V_{IL}, CMOS (Note 11)	2.0	5.5	V
I_{CCDR1}	Data Retention Current	V_{CC} = 2V $\overline{CS1}$ > V_{IH}, CMOS CS2 > V_{IH}, CMOS		40	μA
I_{CCDR2}	Data Retention Current	V_{CC} = 2V CS2 < V_{IL}, CMOS		40	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operation Recovery Time	See Retention Waveform	t_{RC}		ns

Low V_{CC} Data Retention Waveforms

No. 1 ($\overline{CS1}$ Controlled)



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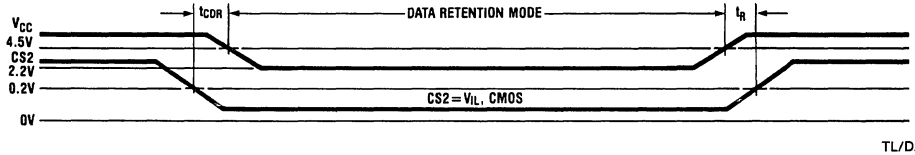
No. 2 (CS2 Controlled)



TL/D/8808–8

National Semiconductor Corporation

ADVANCED INFORMATION
April 1987

NMC61256N/NMC61256N-L 32,768 x 8-Bit Static RAM

General Description

The NMC61256N/NMC61256N-L is a 32,768 by 8-bit, new generation static RAM. It is fabricated with National's proprietary microCMOS double-polysilicon technology which combines high performance and high density with low power consumption and excellent reliability.

The NMC61256N/NMC61256N-L operates with a single 5V power supply with ±10% tolerance. Additional battery back-up operation is available (L version) for data retention down to 2V, with low standby current.

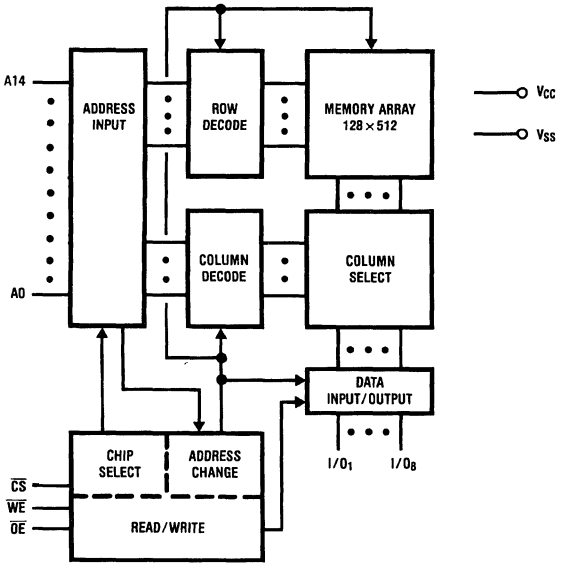
Packaging is in standard 28-pin plastic DIP.

In addition to the inputs and outputs being TTL compatible, the outputs are also CMOS compatible, in that capacitive loads are driven to V_{CC} or V_{SS}.

Features

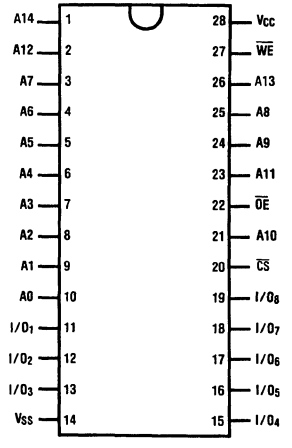
- Single power supply: 5V ±10%
- Fast access time 70 ns/100 ns/120 ns max
- Equal access and cycle times
- Completely static RAM: no clock or timing strobe required
- Low standby power and low power operation
  Standby: 50 μW, typical
  Operation: 10 mW/MHz, typical
- Battery back-up operation available (L version) with data retention supply voltage: 2V–5.5V
- Common data input and output, TRI-STATE® output
- TTL compatible: all inputs and outputs
- CMOS compatible: outputs drive capacitive loads to V_{CC} or V_{SS}
- Standard 28-pin package configuration

Block and Connection Diagrams



TL/D/8807–1

Dual-In-Line Package



TL/D/8807–2

Top View

Order Number NMC61256N or NMC61256N-L
See NS Package Number N28A

Order Number / Parameter	NMC61256N-70L	NMC61256N-70	NMC61256N-100L	NMC61256N-100	NMC61256N-120L	NMC61256N-120
Access Time (ns)	70	70	100	100	120	120
I_{CC} Standby, CMOS	500 μA	2 mA	500 μA	2 mA	500 μA	2 mA

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Voltage on Any Pin Relative to V_{SS}	−0.6V to +7V
Storage Temperature, T_{STG}	−55°C to +125°C
Temperature Under Bias, T_{BIAS}	−10°C to +85°C
Power Dissipation, P_D	1.0W
Current Through Any Pin	100 mA

ESD rating to be determined.

Recommended DC Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
V_{SS} Supply Voltage	0	0	V
V_{IH}, Input High Voltage (Logic 1)			
TTL	2.2	6.0	V
CMOS	V_{CC} − 0.2	V_{CC} + 0.2	V
V_{IL}, Input Low Voltage (Logic 0)			
TTL	−0.3	0.8	V
CMOS	−0.3	0.2	V
T_{OPR}, Operating Temp	0	70	°C

DC Electrical Characteristics at recommended operating conditions

Symbol		Parameter	Conditions	Min	Max	Units
I_{LI}		Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	−2	2	μA
I_{LO}		Output Leakage Current	$\overline{CS}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	−2	2	μA
I_{CC}		Active Quiescent Current, TTL	All Inputs at TTL Levels $\overline{CS} = V_{IL}$ TTL, $I_{I/O} = 0$ mA		25	mA
I_{CC}	Std.	Active Quiescent Current, CMOS	All Inputs at CMOS Levels $\overline{CS} = V_{IL}$ CMOS, $I_{I/O} = 0$ mA		2	mA
	L				500	μA
I_{CC1}		Average Operating Current, TTL	$T_{RC} = T_{RC}$ Min $\overline{CS} = V_{IL}$ TTL, $I_{I/O} = 0$ mA All Inputs at TTL Levels		50	mA
		Average Operating Current, CMOS	$T_{RC} = T_{RC}$ Min $\overline{CS} = V_{IL}$ TTL, $I_{I/O} = 0$ mA All Inputs at CMOS Levels		30	mA
I_{SB}	Std.	Standby Power Supply Current	$\overline{CS} = V_{IH}$ TTL $I_{I/O} = 0$ mA		4	mA
	L				2	mA
I_{SB1}	Std.	Standby Power Supply Current	$\overline{CS} = V_{IH}$ CMOS		2	mA
	L				500	μA
V_{OL}		Output Low Voltage, TTL	$I_{OL} = 8$ mA		0.4	V
		Output Low Voltage, CMOS	$I_{OL} = \pm 10$ μA	−0.2	0.2	V
V_{OH}		Output High Voltage, TTL	$I_{OH} = -4$ mA	2.4		V
		Output High Voltage, CMOS	$I_{OH} = \pm 10$ μA	V_{CC} − 0.2	V_{CC} + 0.2	V

Capacitance

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0$V (Note 5)	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O} = 0$V (Note 5)	10	pF

Truth Table

Mode	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Current
Not Selected (Power Down)	•	H	•	Hi-Z	I_{SB}, I_{SB1}
Output Disabled	H	L	H	Hi-Z	I_{CC}, I_{CC1}
Read	H	L	L	D_{OUT}	I_{CC}, I_{CC1}
Write	L	L	•	D_{IN}	I_{CC}, I_{CC1}

• = Don't care (H or L), H = Logic HIGH Level, L = Logic LOW Level

AC Electrical Characteristics* (Note 1)

Symbol	Parameter	NMC61256N/NMC61256N-L						Units
		-70		-100		-120		
		Min	Max	Min	Max	Min	Max	
READ CYCLE (Note 4)								
t_{RC}	Read Cycle Time	70		100		120		ns
t_{AA}	Address Access Time		70		100		120	ns
t_{CO}	Chip Selection ($\overline{CS}$) to Output Valid		70		100		120	ns
t_{OE}	Output Enable ($\overline{OE}$) to Output Valid		30		50		60	ns
t_{LZ}	Chip Selection ($\overline{CS}$) to Output Active (Note 11)	15		15		15		ns
t_{OLZ}	Output Enable ($\overline{OE}$) to Output Active (Note 11)	5		5		5		ns
t_{HZ}	Chip Deselection (CS) to Output in Hi-Z (Notes 2 and 3)	0	30	0	35	0	40	ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z (Notes 2 and 3)	0	25	0	35	0	40	ns
t_{OHA}	Output Hold from Address Change	5		10		10		ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	70		100		120		ns
t_{CW}	Chip Selection ($\overline{CS}$) to End of Write (Note 10)	60		80		85		ns
t_{AS}	Address Setup Time (Note 7)	0		0		0		ns
t_{AW}	Address Valid to End of Write	60		80		85		ns
t_{WP}	Write Pulse Width (Note 6)	40		60		70		ns
t_{WR}	Write Recovery Time from $\overline{CS}$ (Note 8)	0		0		0		ns
t_{WHZ}	Beginning of Write to Output in Hi-Z (Note 9)	0	25	0	35	0	40	ns
t_{DW}	Data Valid to Write Time Overlap	30		35		40		ns
t_{DH}	Data Hold from End of Write	0		0		0		ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z	0	25	0	35	0	40	ns
t_{OW}	Output Active from End of Write	0		0		0		ns

*Applies to Standard and L Versions.

Note 1: AC test conditions T_A = 0°C to +70°C, V_{CC} = 5V ±10%.

Note 2: t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are determined as:
High to TRI-STATE, measured V_{OH} (DC) − 0.10V
Low to TRI-STATE, measured V_{OL} (DC) + 0.10V

Note 3: At any given temperature and voltage condition, $t_{HZ\ MAX}$ is less than $t_{LZ\ MIN}$, both for a given device and from device to device (guaranteed not tested).

Note 4: $\overline{WE}$ is high for read cycle.

Note 5: T_A = 25°C, f = 1.0 MHz. This parameter is sampled and not 100% tested.

Note 6: A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.

Note 7: t_{AS} is measured from the address changes to the beginning of the write.

Note 8: t_{WR} is measured from the earliest of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.

Note 9: If $\overline{CS}$ is low during this period, I/O pins are in the output state. At this time, the data input signals of opposite phase to the outputs must not be applied.

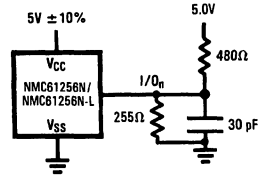
Note 10: If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the outputs will remain in a Hi-Z state.

Note 11: Output active level is defined as steady state TRI-STATE level ±0.1V.

AC Test Conditions

Input pulse levels:	V_{IH} = 3.0V, V_{IL} = 0.0V
Input rise and fall times:	5 ns
All input timing reference levels:	1.5V
Output timing reference levels:	V_{OH} = 2.0V, V_{OL} = 0.8V

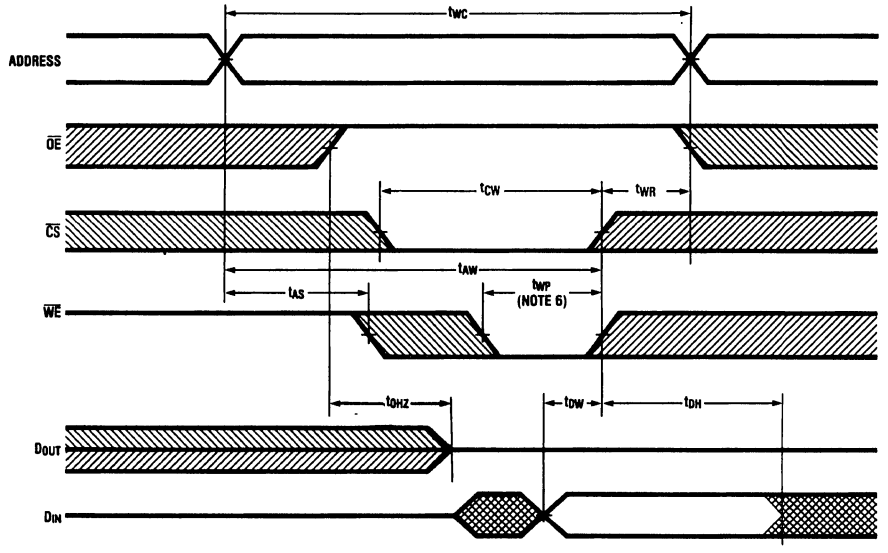
AC Test Load



TL/D/8807–3

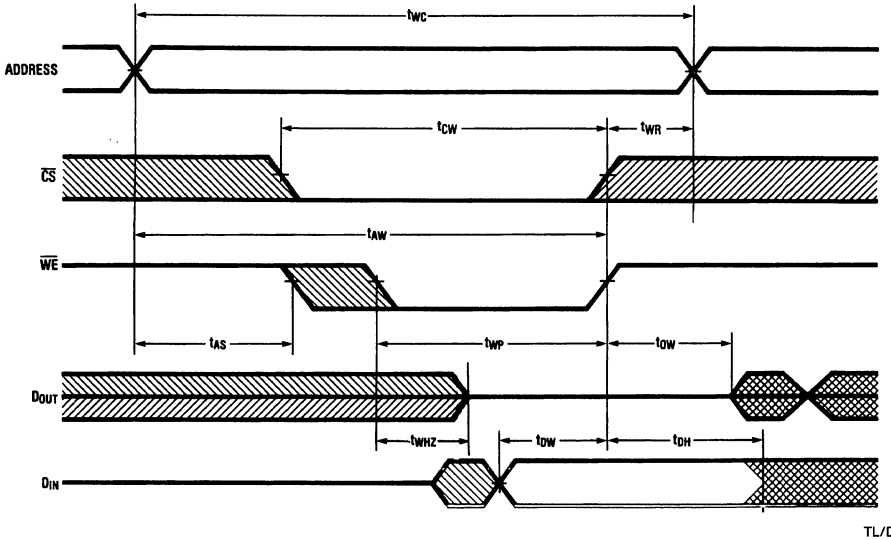
Timing Waveforms

Write Cycle 1 ($\overline{OE}$ Clocked)



TL/D/8807–4

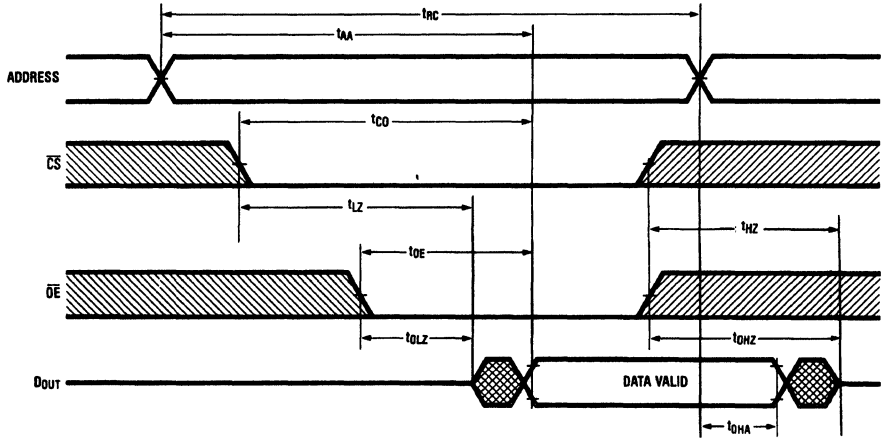
Write Cycle 2 ($\overline{OE}$ Low Fixed)



TL/D/8807–5

Timing Waveforms (Continued)

Read Cycle ($\overline{WE}$ = V_{IH})

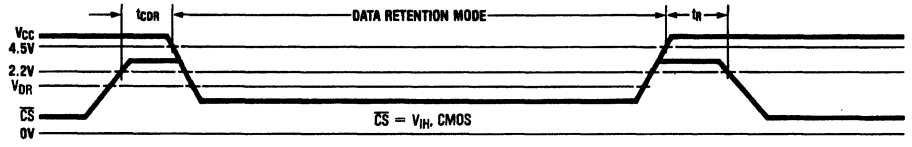


TL/D/8807–6

Low V_{CC} Data Retention (L Version)

Symbol	Parameter	Conditions	Min	Max	Units
V_{DR}	V_{CC} for Data Retention	$\overline{CS}$ > V_{IH}, CMOS	2.0	5.5	V
I_{CCDR}	Data Retention Current	V_{CC} = 2V $\overline{CS}$ > V_{IH}, CMOS		200	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operation Recovery Time	See Retention Waveform	t_{RC}		ns

Low V_{CC} Data Retention Waveform



TL/D/8807–7

Section 2

TTL RAMs

Section 2 Contents

TTL RAM Selection Guide

Size (Bits)	Organization	Outputs*	Pins (DIP)	P/N	T_{AA}	I_{CC}	Temp
INVERTING RAMS							
64	16 x 4	TS	16	DM54S189	50	110	−55°C to +125°C
	16 x 4	TS	16	DM74S189	35	110	0°C to +70°C
	16 x 4	TS	16	DM54S189A	30	100	−55°C to +125°C
	16 x 4	TS	16	DM74S189A	25	100	0°C to +70°C
	16 x 4	OC	16	DM74S289	35	110	0°C to +70°C
NON-INVERTING RAMS							
64	16 x 4	TS	16	DM75S07	50	100	−55°C to +125°C
	16 x 4	TS	16	DM85S07	35	100	0°C to +70°C
	16 x 4	TS	16	DM75S07A	30	100	−55°C to +125°C
	16 x 4	TS	16	DM85S07A	25	100	0°C to +70°C
	16 x 4	OC	16	DM85S06	35	100	0°C to +70°C
EDGE TRIGGERED REGISTERS							
64	16 x 4	TS	18	DM75S68	55	100	−55°C to +125°C
	16 x 4	TS	18	DM85S68	40	100	0°C to +70°C
	16 x 4	TS	18	DM75S68A	45	100	−55°C to +125°C
	16 x 4	TS	18	DM85S68A	24	100	0°C to +70°C

*TS = TRI-STATE® outputs

OC = Open Collector outputs

National Semiconductor Corporation

April 1987

DM54S189/DM74S189 64-Bit (16 x 4) TRI-STATE® RAM DM74S289 64-Bit Open-Collector RAM DM54S189A/DM74S189A High Speed 64-Bit TRI-STATE RAM

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM74S289.

Write Cycle: The complement of the information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM74S189 outputs are bus connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information (complement of information applied at the data inputs during the write cycle) is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

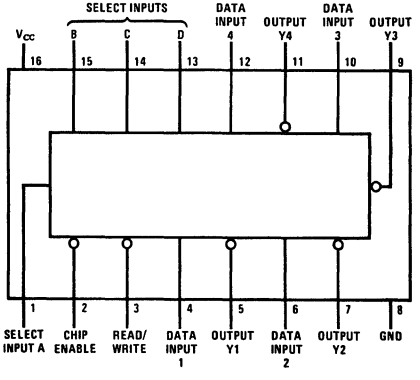
The fast access time of the DM74S189A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM74S189A outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

- Schottky-clamped for high speed applications (S189A)
  - Access from chip-enable input 17 ns max
  - Access from address inputs 25 ns max
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads (S189, S189A)
- DM74S289 are functionally equivalent and have open-collector outputs
- DM54SXXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



TL/L/9232-1

Top View

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write (Store Complement of Data)	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Order Number DM54S189J, DM54S189AJ, DM74S189J, DM74S189AJ, DM74S289J, DM74S189N, DM74S189AN or DM74S289N
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189	4.5	5.5	V
DM74S189, DM74S289	4.75	5.25	V
Temperature (T_A)			
DM54S189	−55	+125	°C
DM74S189, DM74S289	0	+70	°C

DM54S189, DM74S189, DM74S289 Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189	2.4	3.2		V
I_{CEX}	High Level Output Current Open Collector Only	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM54S189			0.5	V
			DM74S189, DM74S289			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.45V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V	DM54S189, DM74S189	−30		−100	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	110	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V	DM54S189, DM74S189			50	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.45V	DM54S189, DM74S189	−50			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM74S189 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189			DM74S189			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Times from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

DM74S289 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM74S289			Units
				Min	Typ (Note 2)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω *(Figure 4)*		25	35	ns
t_{CHL}	Enable Time from Chip-Enable				12	17	ns
t_{WHL}	Enable Time from Read/Write	Sense Recovery Time from Read/Write			12	25	ns
t_{CLH}	Disable Time from Chip-Enable				12	20	ns
t_{WLH}	Disable Time from Read/Write				13	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			ns
t_{ASW}	Set-Up Time *(Figure 2)*	Address to Read/Write		0			ns
t_{DSW}		Data to Read/Write		25			ns
t_{CSW}		Chip-Enable to Read/Write		0			ns
t_{AHW}	Hold Time *(Figure 2)*	Address from Read/Write		0			ns
t_{DHW}		Data from Read/Write		0			ns
t_{CHW}		Chip-Enable from Read/Write		0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189 and across the 0°C to +70°C range for the DM74S189/289. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM54S189(A)	4.5	5.5	V
DM74S189(A)/DM74S289	4.75	5.25	V
Temperature (T_A)			
DM54S189(A)	−55	+125	°C
DM74S189(A)/DM74S289	0	+70	°C

DM54S189A, DM74S189A Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM54S189A	2.4	3.4		V
			I_{OH} = −6.5 mA, DM74S189A	2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA			0.45	V
			I_{OL} = 20 mA			0.5	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V		−20		−90	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.4V		−40			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4.0		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz, Output "Off"			6.0		pF

DM54S189A, DM74S189A Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM54S189A			DM74S189A			Units
				Min	Typ (Note 2)	Max	Min	Typ (Note 2)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		20	30		20	25	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			11	25		11	17	ns
t_{CZL}	Output Enable Time to Low Level				11	25		11	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			20			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			20			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM54S189(A) and across the 0°C to +70°C range for the DM74S189(A). All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

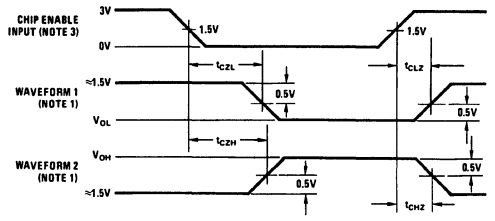
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

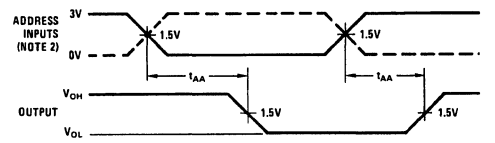
DM54S189(A), DM74S189(A) Switching Time Waveforms

Enable and Disable Time from Chip-Enable



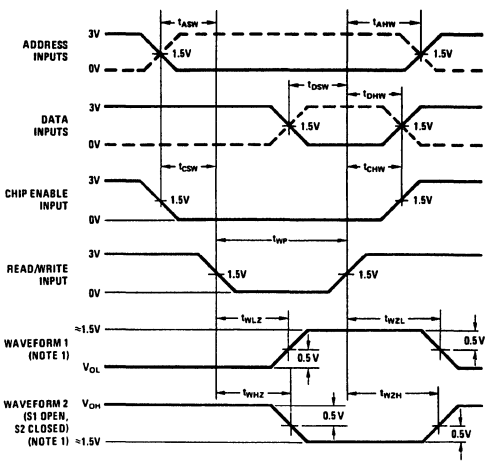
TL/L/9232-2

Access Time from Address Inputs



TL/L/9232-3

Write Cycle



TL/L/9232-4

FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

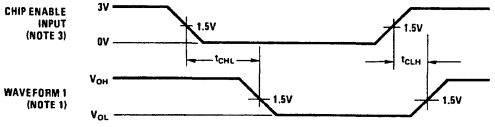
Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} = \approx 50\Omega$.

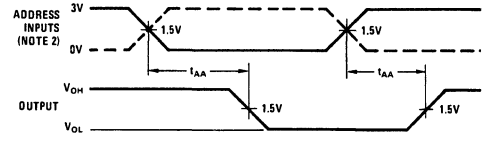
DM74S289 Switching Time Waveforms

Enable and Disable Time from Chip-Enable



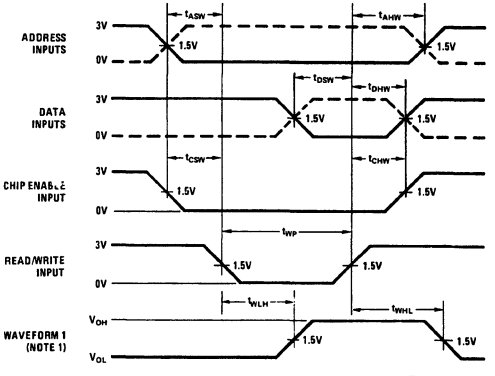
TL/L/9232-5

Access Time from Address Inputs



TL/L/9232-6

Write Cycle



TL/L/9232-7

FIGURE 2

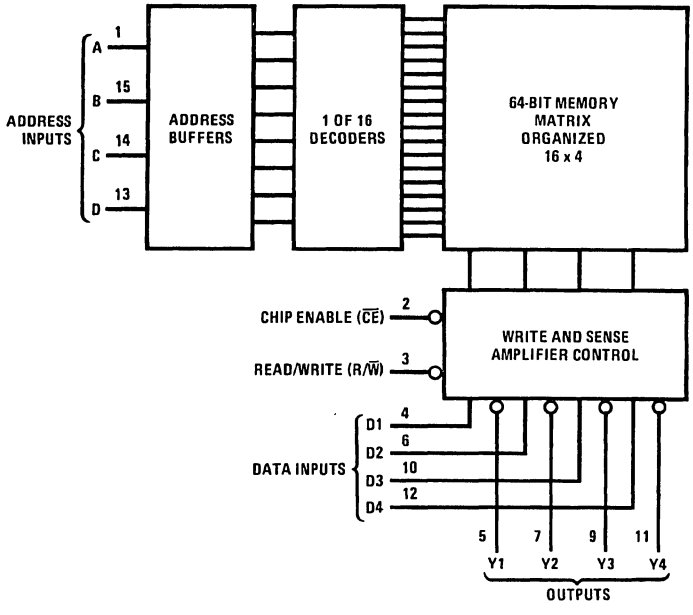
Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

Block Diagram

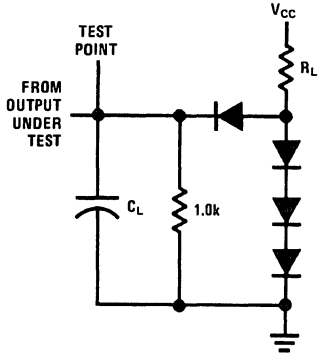


TL/L/9232–8

FIGURE 3

AC Test Circuits

DM54S189(A)/DM74S189(A)



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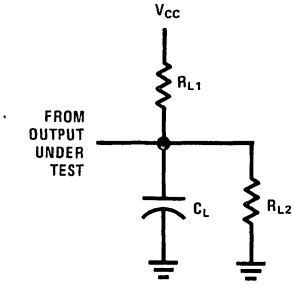
C_L includes probe and jig capacitance.

All diodes are 1N3064.

DM74S289



TL/L/9232–10

FIGURE 4

National Semiconductor Corporation

March 1987

DM85S06 Open-Collector DM75S07/DM85S07 TRI-STATE® DM75S07A/DM85S07A High Speed TRI-STATE Non-Inverting, 64-Bit (16 x 4) RAMs

General Description

These 64-bit active-element memories are monolithic Schottky-clamped transistor-transistor logic (TTL) arrays organized as 16 words of 4 bits each. They are fully decoded and feature a chip-enable input to simplify decoding required to achieve the desired system organization. The memories feature PNP input transistors that reduce the low level input current requirement to a maximum of −0.25 mA, only one-eighth that of a DM54S/DM74S standard load factor. The chip-enable circuitry is implemented with minimal delay times to compensate for added system decoding.

The TRI-STATE output combines the convenience of an open-collector with the speed of a totem-pole output; it can be bus-connected to other similar outputs; yet it retains the fast rise time characteristics of the TTL totem-pole output. Systems utilizing data bus lines with a defined pull-up impedance can employ the open-collector DM85S06.

Write Cycle: The information at the data input is written into the selected location when both the chip-enable input and the read/write input are low. While the read/write input is low, the outputs are in the high-impedance state. When a number of the DM85S07 outputs are bus-connected, this high-impedance state will neither load nor drive the bus line, but it will allow the bus line to be driven by another active output or a passive pull-up if desired.

Read Cycle: The stored information is available at the outputs when the read/write input is high and the chip-enable is low. When the chip-enable is high, the outputs will be in the high-impedance state.

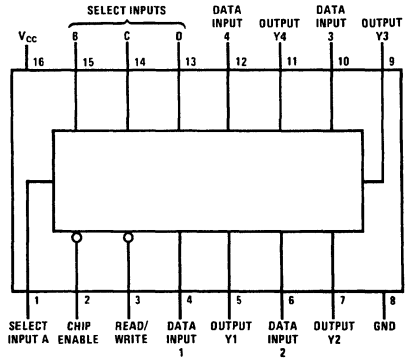
The fast access time of the DM75S07A makes it particularly attractive for implementing high-performance memory functions requiring access times less than 25 ns. The high capacitive drive capability of the outputs permits expansion without additional output buffering. The unique functional capability of the DM75S07 outputs being at a high-impedance during writing, combined with the data inputs being inhibited during reading, means that both data inputs and outputs can be connected to the data lines of a bus-organized system without the need for interface circuits.

Features

- Schottky-clamped for high speed applications (75S07A)
  - Access from chip-enable input 17 ns max
  - Access from address inputs 25 ns max
- TRI-STATE outputs drive bus-organized systems and/or high capacitive loads
- DM85S06 is functionally equivalent and has open-collector outputs
- DM75SXX is guaranteed for operation over the full military temperature range of −55°C to +125°C
- Compatible with most TTL logic circuits
- Chip-enable input simplifies system decoding

Connection Diagram

Dual-In-Line Package



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Top View

Truth Table

Function	Inputs		Output
	Chip-Enable	Read/Write	
Write	L	L	High-Impedance
Read	L	H	Stored Data
Inhibit	H	X	High-Impedance

H = High Level, L = Low Level, X = Don't Care

Order Number DM75S07J, DM75S07AJ, DM85S06J, DM85S07J, DM85S07AJ, DM85S06N, DM85S07N or DM85S07AN
See NS Package Number J16A or N16E

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
DM75S07(A)	4.5	5.5	V
DM85S06/DM85S07(A)	4.75	5.25	V
Temperature (T_A)			
DM75S07(A)	−55	+125	°C
DM85S06/DM85S07(A)	0	+70	°C

DM85S06, DM75S07/DM85S07, DM75S07A/DM85S07A Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S07(A)	2.4	3.4		V
			I_{OH} = −5.2 mA, DM85S07(A)	2.4	3.2		V
I_{CEX}	High Level Output Current Open-Collector Only	V_{CC} = Min	V_{OH} = 2.4V			40	μA
			V_{OH} = 5.5V			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min	I_{OL} = 16 mA			0.45	V
			I_{OL} = 20 mA			0.5	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V				−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_O = 0V DM75S07(A), DM85S07(A)		−30		−90	mA
I_{CC}	Supply Current (Note 5)	V_{CC} = Max			75	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	mA
I_{OZH}	TRI-STATE Output Current, High Level Voltage Applied	V_{CC} = Max, V_O = 2.4V DM75S07(A), DM85S07(A)				40	μA
I_{OZL}	TRI-STATE Output Current, Low Level Voltage Applied	V_{CC} = Max, V_O = 0.4V DM75S07(A), DM85S07(A)		−40			μA
C_{IN}	Input Capacitance	V_{CC} = 5V, V_{IN} = 2V, T_A = 25°C, 1 MHz			4		pF
C_O	Output Capacitance	V_{CC} = 5V, V_O = 2V, T_A = 25°C, 1 MHz Output "Off"			6		pF

DM75S07/DM85S07 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM75S07			DM85S07			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		25	50		25	35	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

DM75S07A/DM85S07A Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM75S07A			DM85S07A			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Access Time from Address		C_L = 30 pF, R_L = 280Ω *(Figure 4)*		20	30		20	25	ns
t_{CZH}	Output Enable Time to High Level	Access Times from Chip-Enable			12	25		12	17	ns
t_{CZL}	Output Enable Time to Low Level				12	25		12	17	ns
t_{WZH}	Output Enable Time to High Level	Sense Recovery Times from Read/Write			13	35		13	25	ns
t_{WZL}	Output Enable Time to Low Level				13	35		13	25	ns
t_{CHZ}	Output Disable Time from High Level	Disable Times from Chip-Enable	C_L = 5 pF, R_L = 280Ω *(Figure 4)*		12	25		12	17	ns
t_{CLZ}	Output Disable Time from Low Level				12	25		12	17	ns
t_{WHZ}	Output Disable Time from High Level	Disable Times from Read/Write			15	35		15	25	ns
t_{WLZ}	Output Disable Time from Low Level				15	35		15	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			20			ns
t_{ASW}	Set-Up Time *(Figure 1)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			20			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 1)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S07(A) and across the 0°C to +70°C range for the DM85S07(A). All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

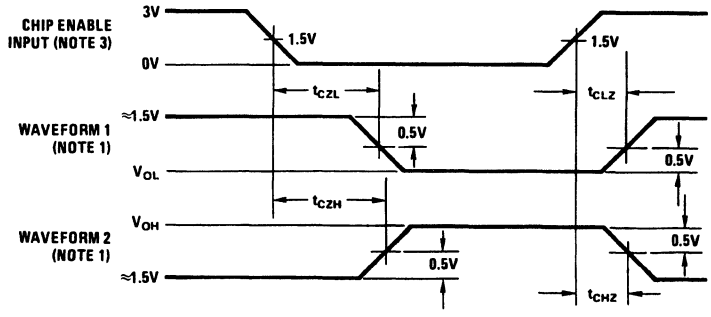
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

DM75S07(A)/DM85S07(A) Switching Time Waveforms

Enable and Disable Time from Chip-Enable



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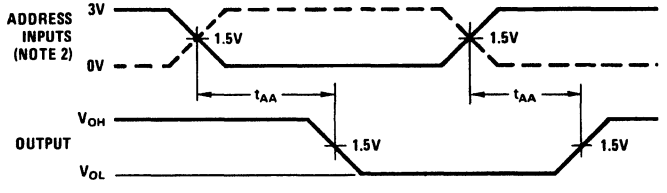
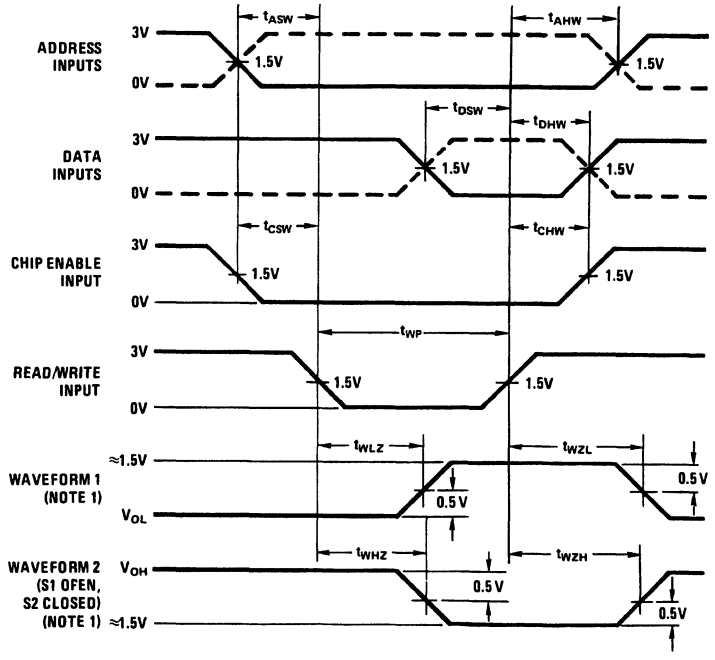
Access Time from Address Inputs



TL/L/9231–3

Write Cycle



TL/L/9231–4

FIGURE 1

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled. Waveform 2 is for the output with internal conditions such that the output is high except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} = \approx 50\Omega$.

DM75S06/DM85S06 Switching Characteristics

over recommended operating ranges of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		Conditions	DM75S06			DM85S06			Units
				Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{AA}	Access Times from Address		C_L = 30 pF, R_{L1} = 300Ω, R_{L2} = 600Ω *(Figure 4)*		25	50		25	35	ns
t_{CHL}	Enable Time from Chip-Enable				12	25		12	17	ns
t_{WHL}	Enable Time from Read/Write	Sense Recovery Time from Read/Write			13	35		13	25	ns
t_{CLH}	Disable Time from Chip-Enable				12	25		12	20	ns
t_{WLH}	Disable Time from Read/Write				13	35		13	25	ns
t_{WP}	Width of Write Enable Pulse (Read/Write Low)			25			25			ns
t_{ASW}	Set-Up Time *(Figure 2)*	Address to Read/Write		0			0			ns
t_{DSW}		Data to Read/Write		25			25			ns
t_{CSW}		Chip-Enable to Read/Write		0			0			ns
t_{AHW}	Hold Time *(Figure 2)*	Address from Read/Write		0			0			ns
t_{DHW}		Data from Read/Write		0			0			ns
t_{CHW}		Chip-Enable from Read/Write		0			0			ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S07(A) and across the 0°C to +70°C range for the DM85S07(A). All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

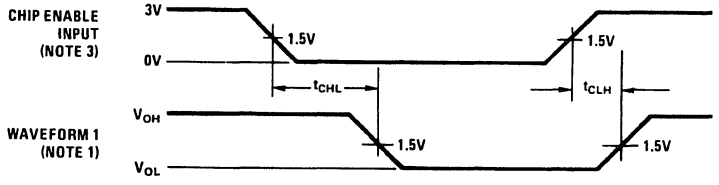
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Note 5: I_{CC} is measured with all inputs grounded; and the outputs open.

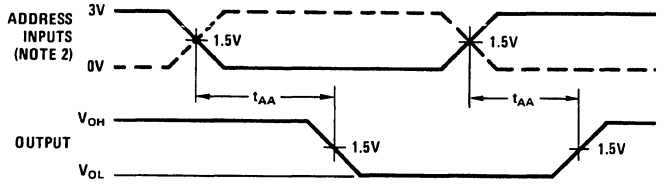
DM75S06/DM85S06 Switching Time Waveforms

Enable and Disable Time from Chip-Enable



TL/L/9231–5

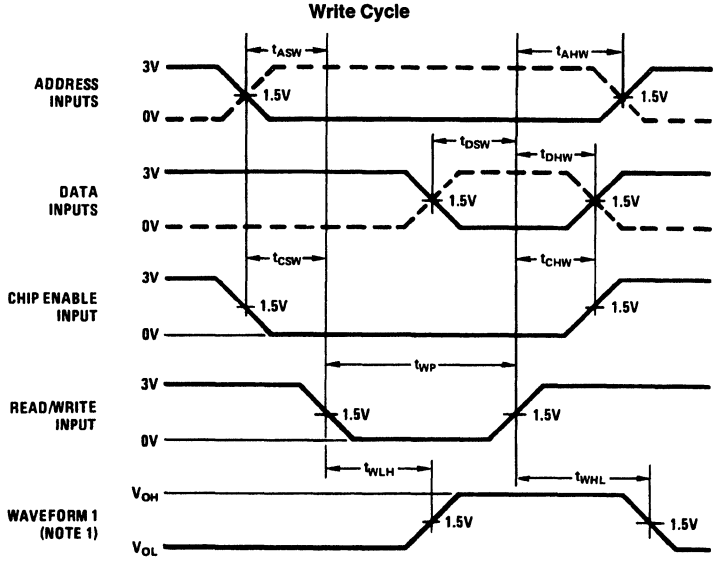
Access Time from Address Inputs



TL/L/9231–6

FIGURE 2

DM75S06/DM85S06 Switching Time Waveforms (Continued)



TL/L/9231–7

FIGURE 2 (Continued)

Note 1: Waveform 1 is for the output with internal conditions such that the output is low except when disabled.

Note 2: When measuring delay times from address inputs, the chip-enable input is low and the read/write input is high.

Note 3: When measuring delay times from chip-enable input, the address inputs are steady-state and the read/write input is high.

Note 4: Input waveforms are supplied by pulse generators having the following characteristics: $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns, PRR ≤ 1 MHz and $Z_{OUT} \approx 50\Omega$.

Block Diagram

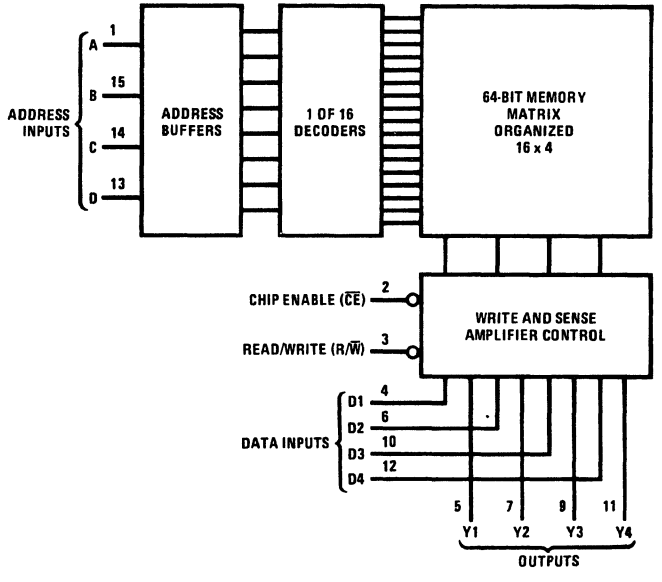


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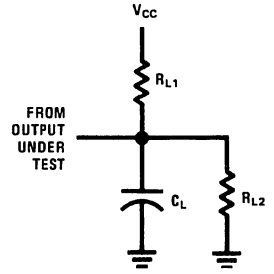
FIGURE 3

AC Test Circuits

DM75S06/DM85S06



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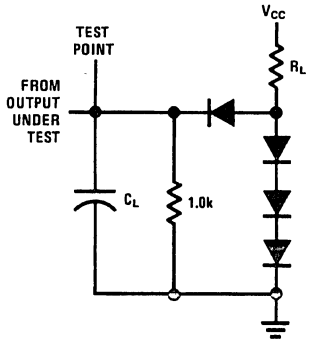
DM75S07(A)/DM85S07(A)



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C_L includes probe and jig capacitance.

All diodes are 1N3064.

FIGURE 4

National Semiconductor Corporation

March 1987

DM75S68/DM85S68/DM75S68A/DM85S68A 16 x 4 Edge Triggered Registers

General Description

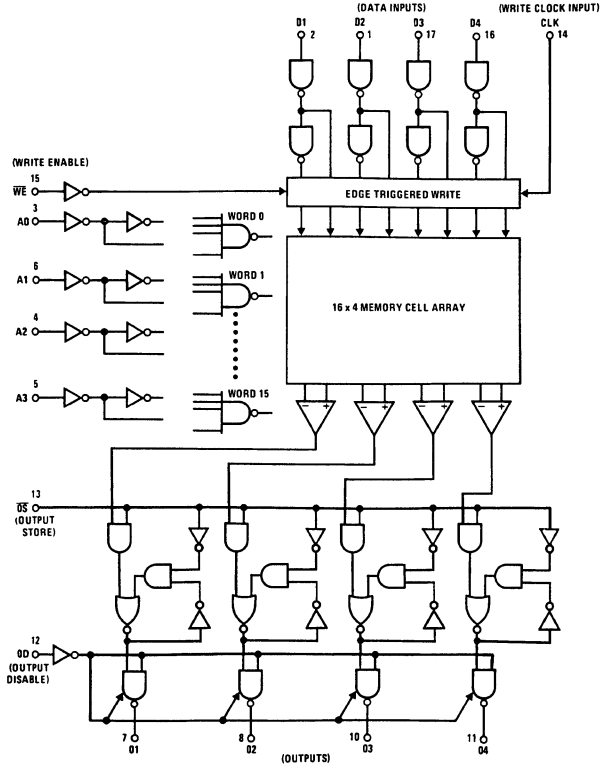
These Schottky memories are addressable "D" register files. Any of its 16 four-bit words may be asynchronously read or may be written into on the next clock transition. An input terminal is provided to enable or disable the synchronous writing of the input data into the location specified by the address terminals. An output disable terminal operates only as a TRI-STATE® output control terminal. The addressable register data may be latched at the outputs and retained as long as the output store terminal is held in a low state. This memory storage condition is independent of the state of the output disable terminal.

All input terminals are high impedance at all times, and all outputs have low impedance active drive logic states and the high impedance TRI-STATE condition.

Features

- On-chip output register
- PNP inputs reduce input loading
- Edge triggered write
- High speed—20 ns typ
- All parameters guaranteed over temperature
- TRI-STATE output
- Schottky-clamped for high speed
- Optimized for register stack applications
- Typical power dissipation—350 mW

Logic and Block Diagram



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Pin Names

A_0–A_3	Address Inputs
D_1–D_4	Data Inputs
0_1–0_4	Data Outputs
$\overline{WE}$	Write Enable
CLK	Write Clock Input
$\overline{OS}$	Output Store
OD	Output Disable

O_D	$\overline{W_E}$	CLK	$\overline{O_S}$	MODE	OUTPUTS
0	X	X	0	Output Store	Data From Last Addressed Location
X	0	⌐	X	Write Data	Dependent on State of OD and $\overline{OS}$
0	X	X	1	Read Data	Data Stored in Addressed Location
1	X	X	0	Output Store	High Impedance State
1	X	X	1	Output Disable	High Inpedance State

0 = Low Level
1 = High Level
X = Don't Care

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage	7.0V
Input Voltage	5.5V
Output Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}			
DM85S68/DM85S68A	4.75	5.25	V
DM75S68/DM75S68A	4.5	5.5	V
Temperature, T_A			
DM85S68/DM85S68A	0	70	°C
DM75S68/DM75S68A	−55	+125	°C

Electrical Characteristics

over recommended operating free-air temperature range unless otherwise noted (Notes 2 and 3)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IH}	High Level Input Voltage			2			V
V_{IL}	Low Level Input Voltage					0.8	V
V_{OH}	High Level Output Voltage	V_{CC} = Min	I_{OH} = −2.0 mA, DM75S68/DM75S68A	2.4			V
			I_{OH} = −5.2 mA, DM85S68/DM85S68A	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 16 mA	DM75S68/DM75S68A			0.5	V
			DM85S68/DM85S68A			0.45	V
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.4V				25	μA
I_I	High Level Input Current at Maximum Voltage	V_{CC} = Max, V_{IH} = 5.5V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.5V	Clock Input			−500	μA
			All Others			−250	μA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max, V_{OL} = 0V		−20		−55	mA
I_{CC}	Supply Current	V_{CC} = Max			70	100	mA
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_{IN} = −18 mA				−1.2	V
I_{OZ}	TRI-STATE Output Current	V_{CC}= Max	V_O = 2.4V			+40	μA
			V_O = 0.5V			−40	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2. Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DM75S68/DM75S68A and across the 0°C to +70°C range for the DM85S68/DM85S68A. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 4: Only one output at a time should be shorted.

Switching Characteristics over recommended operating range of T_A and V_{CC} unless otherwise noted

Symbol	Parameter		DM75S68		DM85S68		DM75S68A		DM85S68A		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ZH}	Output Enable to High Level			40		35		40		35	ns
t_{ZL}	Output Enable to Low Level			30		24		30		24	ns
t_{HZ}	Output Disable Time from High Level			35		15		35		15	ns
t_{LZ}	Output Disable Time from Low Level			35		18		35		18	ns
t_{AA}	Access Time	Address to Output		55		40		45		24	ns
t_{OSA}		Output Store to Output		35		30		35		20	ns
t_{CA}		Clock to Output		50		40		50		35	ns

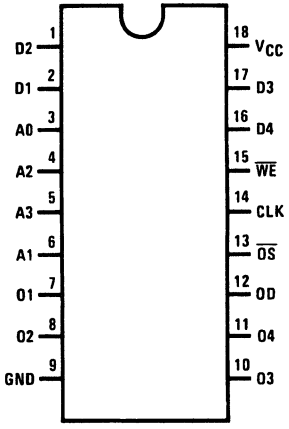
Switching Characteristics

over recommended operating range of T_A and V_{CC} unless otherwise noted (Continued)

Symbol	Parameter		DM75S68		DM85S68		DM75S68A		DM85S68A		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ASC}	Set-Up Time	Address to Clock	25		15		25		15		ns
t_{DSC}		Data to Clock	15		5		15		5		ns
t_{ASOS}		Address to Output Store	40		30		40		10		ns
t_{WESC}		Write Enable Set-Up Time	10		5		10		5		ns
t_{OSSC}		Store before Write	15		10		15		10		ns
t_{AHC}	Hold Time	Address from Clock	15		10		15		10		ns
t_{DHC}		Data from Clock	20		15		20		15		ns
t_{AHOS}		Address from Output Store	10		5		10		2		ns
t_{WEHC}		Write Enable Hold Time	20		15		20		10		ns

Connection Diagram

Dual-In-Line Package

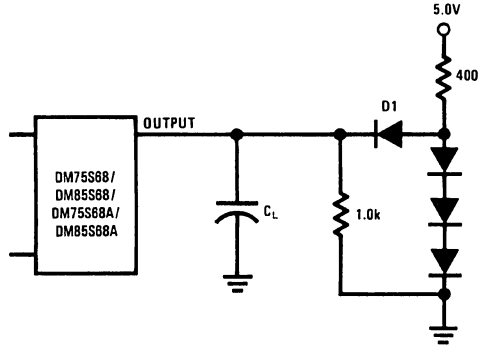


TL/F/9233–2

Top View

Order Number DM75S68J, DM85S68J, DM85S68N, DM75S68AJ, DM85S68AJ or DM85S68AN
See NS Package Number J18A or N18A

AC Test Circuit and Switching Time Waveforms

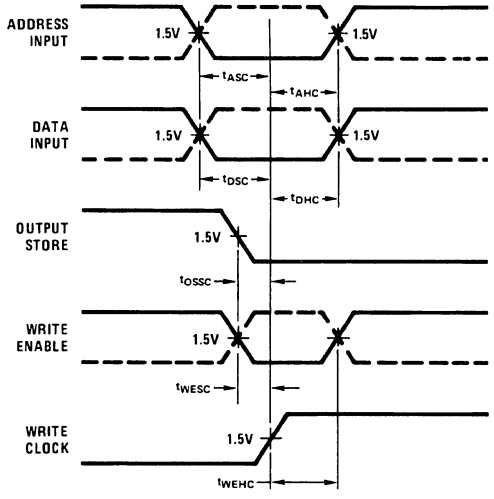


C_L = 5.0 pF for t_{HZ}, t_{LZ}
C_L = 30 pF for all others
C_L includes probe and jig capacitance
All diodes are 1N3064

TL/L/9233-3

Write Cycle

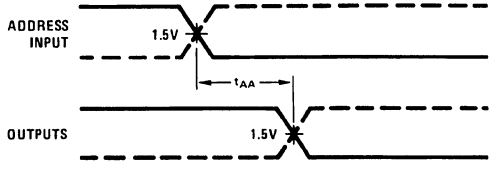
Clock Set-Up and Hold Time



TL/L/9233-4

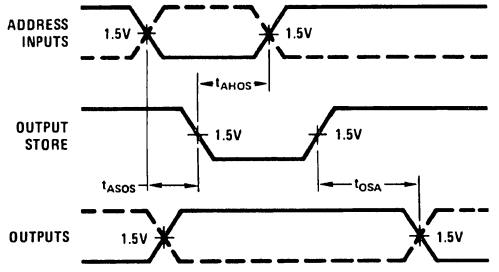
Read Cycle

Address to Output Access Time



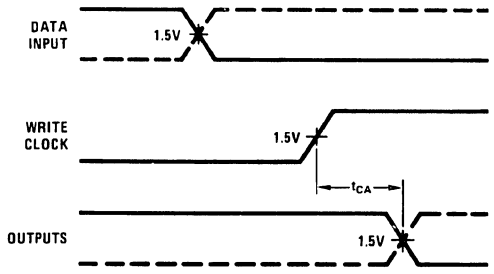
TL/L/9233-6

Output Store Access, Set-Up and Hold Time



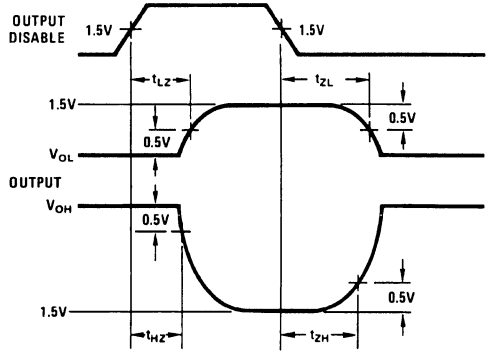
TL/L/9233-7

Clock to Output Access



TL/L/9233-5

Output Disable and Enable Time



TL/L/9233-8

Note: Input waveforms supplied by pulse generator having the following characteristics: V = 3.0V, $t_R \leq 2.5$ ns, PRR ≤ 1.0 MHz and Z_{OUT} = 50M.

National Semiconductor Corporation

March 1987

IDM29705/29705A 16-Word by 4-Bit Two-Port RAM/Register File

General Description

The IDM29705 and IDM29705A are 16-word by 4-bit RAM/Register File chips housed in a standard 28-pin dual-in-line package. The IDM29705 and the IDM29705A feature TRI-STATE® outputs. These RAMs, which are fabricated using SCL® (Schottky ECL Technology) feature two separate output ports that enable any two 4-bit words to be read from these outputs simultaneously. Each output port contains a four-bit latch. A common Latch Enable (LE) input is used to control all eight latches. The device, which has two Write Enable (WE) inputs, is designed so that either Write Enable (WE_1 or WE_2) and Latch Enable (LE) inputs can be wired together to make the operation of the RAM appear edge-triggered.

The device, which has fully decoded A-address and B-address fields, can address any of the 16 memory words for the A-output port and, simultaneously, select any of the 16 words for presentation at the B-output port. Incoming data is written into the four-bit RAM word selected by the B-address. The D inputs are used to load the new data into the device.

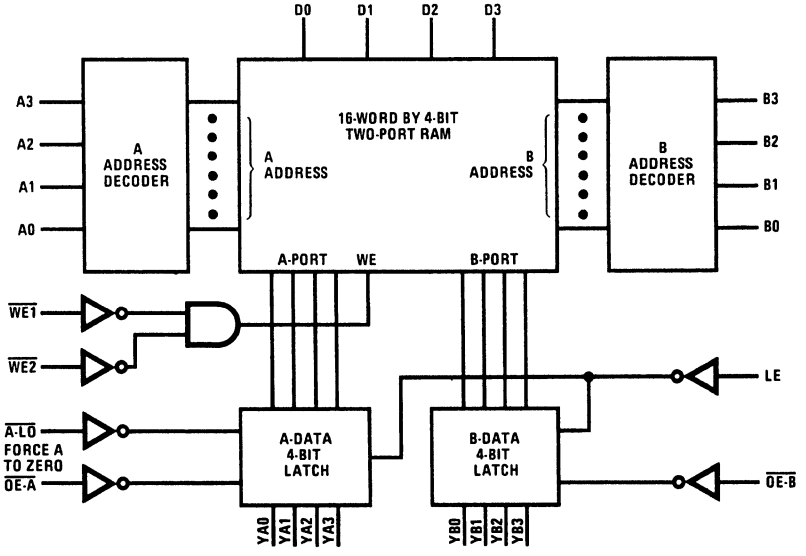
Several of these devices can be cascaded to increase the total number of memory words in the system. When $\overline{OE}$-A is high, the A-output port is in the high-impedance mode. $\overline{OE}$-B, when high, forces the B-output port to the high-impedance state.

The writing of new data into the RAM is controlled by the Write Enable inputs. With both Write Enable inputs low, data is written into the word selected by the B-address field. The memory outputs follow the data inputs during writing if the Latch Enable (LE) is high. With either Write Enable high, no data is written into the RAM.

Features and Benefits

- 16-word by 4-bit, 2-port RAM/Register Files
- Two output ports, each with separate output control
- 4-bit latches on each output port
- Non-inverted data output with respect to data input
- Output enable and write enable inputs provide ease in cascading
- SCL technology (Schottky ECL) provides ECL speeds while keeping low power Schottky input/output voltage and power consumption compatibility
- 100% reliability testing in compliance with MIL-STD-883

IDM29705/29705A Block Diagram



TL/L/9234–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for High Output State	−0.5V to +V_{CC}max
DC Input Voltage	−0.5V to +5.5V
DC Output Current, into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

Operating Range

P/N	Ambient Temperature	V_{CC}
IDM29705JC	0°C to +70°C	4.75V to 5.25V
IDM29705JM, JM/883	−55°C to +125°C	4.50V to 5.50V
IDM29705AJC, NC	0°C to +70°C	4.75V to 5.25V
IDM29705AJM, JM/883	−55°C to +125°C	4.50V to 5.50V

Standard Screening (conforms to MIL-STD-883 for Class C parts)

Step	MIL-STD-883 Method	Conditions	Level	
			DC, PC	DM, FM
Pre-Seal Visual Inspection	2010	B	100%	100%
Stabilization Bake	1008	C: 24-hour 150°C	100%	100%
Temperature Cycle	1010	C: −65°C to +150°C 10 cycles	100%	100%
Centrifuge	2001	B: 10,000 G	100%	100%
Fine Leak	1014	A: 5×10^{-8} atm-cc/cm^3	100%	100%
Gross Leak	1014	C2: Fluorocarbon	100%	100%
Electrical Test Subgroups 1 and 7 and 9	5004	See below for definitions of subgroups	100%	100%
Insert Additional Screening Here for Class B Parts				
Group A Sample Tests	5005	See below for definitions of subgroups		
Subgroup 1			LTPD = 5	LTPD = 5
Subgroup 2			LTPD = 7	LTPD = 7
Subgroup 3			LTPD = 7	LTPD = 7
Subgroup 7			LTPD = 7	LTPD = 5
Subgroup 8			LTPD = 7	LTPD = 7
Subgroup 9			LTPD = 7	LTPD = 5

Additional Screening for Class B Parts

Step	MIL-STD-883 Method	Conditions	Level
			DMB, FMB
Burn-In	1015	D: 125°C, 160 hours min	100%
Electrical Test	5004		
Subgroup 1			100%
Subgroup 2			100%
Subgroup 3			100%
Subgroup 7			100%
Subgroup 9			100%
Return to Group A Tests in Standard Screening			

Group A Subgroups (as defined in MIL-STD-883, method 5005)

Subgroup	Parameter	Temperature
1	DC	25°C
2	DC	Maximum rated temperature
3	DC	Minimum rated temperature
7	Function	25°C
8	Function	Maximum and minimum rated temperature
9	Switching	25°C
10	Switching	Maximum rated temperature
11	Switching	Minimum rated temperature

Electrical Characteristics (over operating temperature range, unless otherwise noted)

Symbol	Parameter	Test Conditions (Note 1)		Min.	Typ (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage (IDM29705 only)	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	Mil, I_{OH} = −2.0 mA	2.4			Volts
			Com'l, I_{OH} = −4.0 mA				
V_{OL}	Output LOW Voltage	V_{CC} = min, V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0 mA			0.4	Volts
			I_{OL} = 8.0 mA			0.45	
			I_{OL} = 12 mA			0.5	
			I_{OL} = 16 mA (Note 4)			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = min, I_{IN} = −18 mA				−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = max, V_{IN} = 0.4V	A_i, B_i			−0.25	mA
			Others			−0.36	
I_{IH}	Input HIGH Current	V_{CC} = max, V_{IN} = 2.7V				20	μA
I_I	Input HIGH Current	V_{CC} = max, V_{IN} = 5.5V				0.1	mA
I_{OZ}	Off state (High Impedance) Output Current	V_{CC} = max, V_{IN} = V_{IH} or V_{IL}	V_o = 2.7V			20	μA
			V_o = 0.4V			−20	
I_{SC}	Output Short Circuit Current (Note 3)	V_{CC} = max	29705A	−30		−85	mA
			29705	−25		−85	
I_{CC}	Power Supply Current	V_{CC} = max			120	175	mA
		AJC	V_{CC} = 5.25V, T = 70°C			155	mA
		AJM	V_{CC} = 5.5V, T = 125°C			145	mA

Note 1: For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.

Note 2: Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

Note 3: Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

Note 4: 29705A commercial temperature range only.

Switching Characteristics (Input Levels = 0V and 3.0V, Transitions measured at 1.5V)

Combinational Delays (in nanoseconds) (C_L = 50 pF)

Parameter	From	To	Conditions	Comm'l Max. (Note 1)		Mil Max. (Note 2)	
				705	705A	705	705A
Access Time	A Address Stable	YA Stable	LE = HIGH	40	30	55	35
	B Address Stable	YB Stable		40	30	55	35
	Both WE LOW	YA = D	LE = HIGH, A = B	45	45	48	45
		YB = D	LE = HIGH	45	45	48	45
Turn-On Time	OE-A or OE-B LOW			25	20	25	25
Turn-Off Time	OE-A or OE-B HIGH	YA or YB Off	C_L = 5 pF (Note 3)	20	20	20	20
Reset Time	A-LO LOW	YA LOW		20	20	30	25
Enable Time	LE HIGH	YA and YB Stable		25	20	25	25
	Data In	YA or YB = D	LE = HIGH, WE both LOW, A = B	45	45	45	45

Switching Characteristics (Continued)

Minimum Setup and Hold Times (in nanoseconds)

Parameter	From	To	Conditions	Comm'l Max. (Note 1)		Mil Max. (Note 2)	
				705	705A	705	705A
Data Setup Time	D Stable	Either WE HIGH		20	15	25	20
Data Hold Time	Either WE HIGH	D Changing		0	0	0	0
Address Setup Time	B Stable	Both WE LOW		3	0	5	3
Address Hold Time	Either WE HIGH	B Changing		0	0	0	0
Latch Close Before Write Begins	LE LOW	WE_1 LOW	WE_2 LOW	0	0	0	0
	LE LOW	WE_2 LOW	WE_1 LOW	0	0	0	0
Address Setup Before Latch Closes	A or B Stable	LE LOW		20	15	40	20
Minimum Pulse Widths (in nanoseconds)							
Write Pulse Width	WE_1	HIGH-LOW-HIGH	WE^2LOW	25	20	25	20
	WE_2	HIGH-LOW-HIGH	WE^1LOW	20	20	20	20
A Latch Reset Pulse	A-LO	HIGH-LOW-HIGH		20	15	20	15
Latch Data Capture	LE	LOW-HIGH-LOW	Address Stable	20	15	20	15

Note 1: T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%.

Note 2: −55°C to +125°C, V_{CC} = 5.0V ± 10%.

Note 3: Measured from 1.5V at the input to 0.5V change in the output level.

Function Tables

Write Control

$\overline{WE_1}$	$\overline{WE_2}$	Function	RAM Outputs at Latch Inputs	
			A-Port	B-Port
L	L	Write D into B	A data (A ≠ B)	D input data
X	H	No write	A data	B data
H	X	No write	A data	B data

YA Read

Inputs			YA Outputs	Function
$\overline{OE\text{-}A}$	$\overline{A\text{-}LO}$	LE		
H	X	X	Z	High impedance
L	L	X	L	Force YA LOW
L	H	H	A-Port RAM data	Latches transparent
L	H	L	NC	Latches retain data

Function Tables (Continued)

YB Read

Inputs		YB Output	Function
$\overline{OE\text{-}B}$	LE		
H	X	Z	High impedance
L	H	B-Port RAM data	Latches transparent
L	L	NC	Latches retain data

H = HIGH Z = High impedance
L = LOW NC = No change
X = Don't care

Pinout Descriptions of the IDM29705/29705A

D_3-D_0: Through these inputs new data can be written in the location specified by the B-address inputs.

A_3-A_0: The 4-bit address presented at the A inputs selects one of the 16 memory words for presentation at the A-data latch outputs.

B_3-B_0: The 4-bit address presented at the B inputs selects one of the 16 memory words for presentation at the B-data latch outputs. This address also selects the location into which data is written.

YA_3-YA_0: The four A-data latch outputs.

YB_3-YB_0: The four B-data latch outputs.

$\overline{WE}_1$, $\overline{WE}_2$: Write enable inputs. When both are low, enables data to be written into the RAM location selected by the B-address field. When either Write Enable input is high, no data can be written into memory.

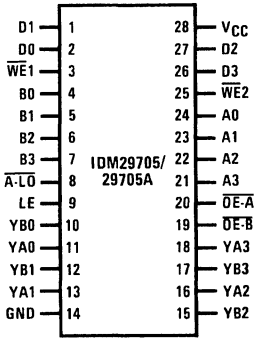
$\overline{OE\text{-}A}$: A-port output enable. When low, data in the A-data latch is present at the YA_i outputs. When high, the YA_i outputs are in the high-impedance mode.

$\overline{OE\text{-}B}$: B-port output enable. When low, data in the B-data latch is presented at the YB_i outputs. When high, the YB_i outputs are in the high-impedance mode.

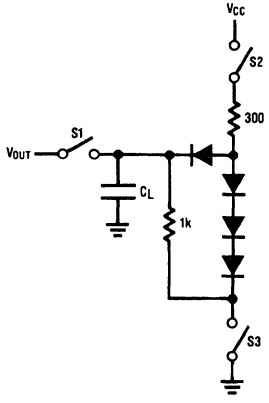
LE: Latch enable. The LE input acts as control for both the RAM-A and RAM-B output ports. When high the latches are transparent and data from the RAM, as selected by the A and B address inputs, is presented at the outputs. When low, the latches retain the last data read from the RAM regardless of the current A and B address inputs.

$\overline{A\text{-}LO}$: Force A to zero. This input operates to force the A-port latch outputs low independent of the LE input or A address inputs. The A-output bus can be forced low using this control input. With $\overline{A\text{-}LO}$ high, the A latches operate in their normal manner. Once forced low, the A latches remain low independent of the $\overline{A\text{-}LO}$ input if the Latch Enable (LE) is low.

IDM29705/29705A Connection Diagram and Test Load



TL/L/9234-2



TL/L/9234-3

Note 1: C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.

Note 2: S1, S2, S3 are closed during function tests and all AC tests except output enable tests.

Note 3: S1 and S3 are closed while S2 is open for t_{PZH} test. S1 and S2 are closed while S3 is open for t_{PZL} test.

Note 4: C_L = 5 pF for output disable tests.

Section 3

TTL FIFOs

Section 3 Contents

National Semiconductor Corporation

PRELIMINARY
March 1987

DM75/85X431 64 x 8 No-Fall-Through FIFO Memory

General Description

The device is a first-in-first-out (FIFO) sequential memory organized as 64 words by 8 bits. Data words written into the device are later read from a separate bus in the same order as entered but at an independent rate. Write and read operations may occur concurrently and at any time with respect to each other. The FIFO is a no-fall-through (NFT) type in which new input data becomes available for output in less time than the minimum write/read cycle period.

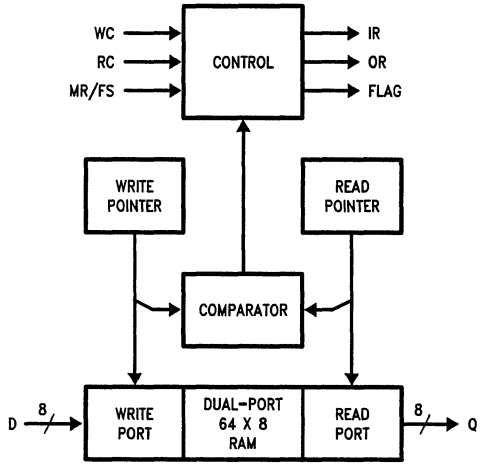
Features

- 64 x 8-bit FIFO memory
- No fall-through delay (first word propagates to output in less than one cycle period)
- 35 MHz write and read clock frequencies
- Totally independent asynchronous write and read clocks
- Cascadable to any depth and/or width (requiring no external hardware)
- Status outputs indicate full, empty and partially-filled conditions
- 24-pin 0.3″ wide DIP package
- TTL I/O signal levels
- Single +5V supply

Applications

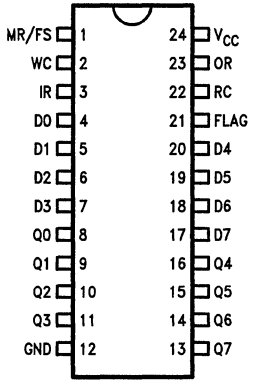
- Data rate translator for computer peripheral controller, eg. disc, tape, printer, graphic display, etc.
- Data rate translator for telecommunications or data communications controller (including local area network)
- ADC or DAC interface buffer for real-time DSP
- Real-time data acquisition buffer
- Variable length shift register for real-time signal delay
- Variable length pipeline register for multiprocessing, DSP, graphics, image analysis, etc.

Block and Connection Diagrams



TL/L/8676–2

Dual-In-Line Package



TL/L/8676–1

Top View

Order Numbers DM75/85X431J or DM85X431N
NS Package Numbers J24F or N24C

3

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 5)	To Be Determined

Electrical Characteristics Over Operating Conditions DM75/DM85X431

Symbol	Parameter	Conditions		Guaranteed Limits			Units
				Min	Typ	Max	
V_{IL}	Low-Level Input Voltage					0.8	V
V_{IH}	High-Level Input Voltage			2			V
V_{IC}	Input Clamp Voltage	V_{CC} = Min,	I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = Max,	V_I = 0.45V			−0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max,	V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max,	V_I = 5.5V			1.0	mA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 8 mA for Q Outputs I_{OL} = 4 mA for IR, OR and FLAG Outputs			0.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min V_{IL} = 0.8V V_{IH} = 2V	I_{OH} = −0.9 mA for Q Outputs I_{OH} = −0.6 mA for IR, OR and FLAG Outputs	2.4			V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max,	V_O = 0V	−30		−80	mA
I_{CC}	Supply Current	V_{CC} = Max Inputs Low, Outputs Open			200		mA

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Operating Conditions (Note 3)

Symbol	Parameter	DM75X431			DM85X431			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	−55		+125	0		+70	°C
t_{WWH}	WC Pulse Width High					12	15	ns
t_{WWL}	WC Pulse Width Low					7	10	ns
t_{SDW}	Input Data Setup					13	17	ns
t_{HDW}	Input Data Hold Time					0	5	ns
t_{WRH}	RC Pulse Width High					7	10	ns
t_{WRL}	RC Pulse Width Low					7	10	ns
t_{WM}	Master Reset Pulse Width (Note 4)					38	50	ns
t_{RMW}	Reset Recovery Time					38	50	ns

Note 2: Ambient Temperature.

Note 3: Since the FIFO is a very high speed device, care must be taken in the design of the hardware. Proper device grounding and supply decoupling are crucial to the correct operation of the FIFO.

Note 4: Minimum time between any two consecutive transitions on the MR/FS input.

Note 5: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Initial Conditions	DM75X431			DM85X431			Units
			Min	Typ	Max	Min	Typ	Max	
f_{WC}	Write Frequency						40	35	MHz
f_{RC}	Read Frequency						40	50	MHz
t_{PRQ}	RC to Data Output						20	27	ns
t_{PWOH}	WC to OR High	Empty, RC = H					15	20	ns
t_{PWIH}	WC Falling to IR High	< 63 Words					11	15	ns
t_{PWHIL}	WC Rising to IR Low	< 63 Words					11	15	ns
t_{PWLIL}	WC Falling to IR Low	63 Words, RC = H					11	15	ns
t_{PRIH}	RC to IR High	Full, WC = L					15	20	ns
t_{PROH}	RC to OR High	> 1 Word					13	18	ns
t_{PROL}	RC to OR Low						10	14	ns
t_{PRIL}	RC Falling to IR Low	63 Words, WC = H					13	18	ns
t_{PWFH}	WC to FLAG High						27	36	ns
t_{PRFL}	RC to FLAG Low						27	36	ns
t_{PDQ}	Transparent D to Q	Empty, WC = H					34	45	ns
t_{PWQ}	WC Rising to Q	Empty					34	45	ns
t_{PMIH}	MR to IR High	Full					28	38	ns
t_{PMOL}	MR to OR Low						15	20	ns
t_{PMFL}	MR to FLAG Low						28	38	ns

Pin Description

V_{CC} Supply voltage.

D0–D7 8-bit data input bus.

Q0–Q7 8-bit data output bus (non-inverted).

WC Write Clock input—latches in data word from D-bus on a high-to-low transition (except when FIFO is full). Data enters the memory while WC is high.

RC Read Clock input—presents next data word onto Q-bus on a low-to-high transition (except when FIFO is empty).

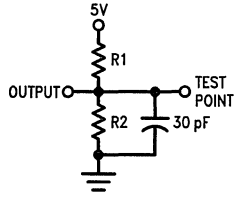
IR Input Ready status output—when high indicates FIFO is ready for another write cycle, ie., FIFO is not full. IR is forced low whenever WC is high (except during 64th write cycle) to accommodate cascading.

OR Output Ready status output—when high indicates FIFO is ready for another read cycle, ie., FIFO is not empty. OR is forced low whenever RC is low to accommodate cascading.

MR/FS Master Reset/FLAG Select input—resets the FIFO to the empty state (internal pointers reset to zero) on either a low-to-high or high-to-low transistion. The state of the MR/FS input during operation selects the waveform to be presented on the FLAG status output.

FLAG Intermediate status FLAG output—if MR/FS input is low, then a high output on FLAG indicates FIFO is at least one quarter filled (16 or more words remaining in memory). If MR/FS is high, then a high output on FLAG indicates FIFO is at least three quarters filled (48 or more words remaining).

Standard Test Load



TL/L/8676–10

I_{OL}	R1	R2
8 mA	560Ω	1100Ω
4 mA	1100Ω	2200Ω

Input Pulse Amplitude = 3V

Input Rise and Fall Time (10%–90%) = 2.5 ns

Measurements made at 1.5V

Functional Description

The NFT FIFO is implemented using a 64 x 8-bit RAM with separate write and read ports. The write port is addressed by the write pointer and the read port by the read pointer. While the WC input is high, a data word on the D inputs is written into the write port of the RAM. The write pointer (initially zero) is incremented on the falling edge of WC, thus concluding a write cycle. The RAM contents addressed by the read pointer (also initially zero) are always presented on the Q outputs. Thus the first word appears on the Q outputs as it is being written. The rising edge of RC increments the read pointer which then accesses the next data word from the RAM's read port.

When the value of the write pointer equals the read pointer, then the FIFO is empty, ie., any data words which had been written have also been read. When the value of the write pointer exceeds the read pointer by 64, then the FIFO is full, ie., the next RAM location into which data should be written contains the oldest word that has not yet been read.

The IR and OR status outputs indicate the full and empty conditions, respectively. When WC is brought low at the end of a write cycle, IR would go high if the FIFO is still not full. If the FIFO becomes full, IR would become low until a vacant

Functional Description (Continued)

RAM location is made available resulting from a read operation (or the Master Reset is activated). WC should remain low until IR goes high. If WC is brought high while IR is still low, then the entire write cycle would be ignored, the RAM contents and write pointer remaining unchanged.

IR is usually driven low whenever WC is high in order to accommodate cascading as described later. However, during the final write cycle (in which the last vacant location is being written) IR would remain high if and as long as RC is high. This is to provide sufficient cycle times to guarantee the proper transfer of data between cascaded devices while reading.

The OR output would go high after the rising edge of RC if the FIFO remains not empty. OR is initially low following a reset until the first word is written into the FIFO. RC should remain high until OR goes high. If RC is brought low before OR goes high, then the read cycle would be inhibited and the next rising edge of RC would not increment the read pointer.

The FIFO resets to the empty state (write and read pointers reset to zero) on either the rising or falling edge of the MR/FS input. Following a reset, IR will be high, provided WC is low, OR and FLAG will be low. WC and RC may be in either state when a reset occurs.

If WC is high following a reset, the first write cycle would not commence until after WC is returned low (a high output on IR must be observed before the FIFO performs any write cycle). Likewise, if RC is low following a reset, the first read cycle would not commence until RC is returned high and a high output is observed on OR (returning RC high does not advance the read pointer).

The FIFO may be operated while the MR/FS input is held either low or high. The state of the MR/FS input during operation selects one of two waveforms to appear on the FLAG status output.

If the FIFO is operated while the MR/FS input is held low, then the FLAG output would indicate when the FIFO is at least one quarter filled, i.e., when the write pointer value exceeds the read pointer by at least 16. If the FIFO is operated while MR/FS is high, then FLAG would indicate when the FIFO is at least three quarters filled, as shown in the following truth table:

# WORDS STORED	FLAG OUTPUT	
	MR/FS = L	MR/FS = H
0–15	L	L
16–47	H	L
48–64	H	H

The FLAG output remains stable throughout all write and read cycles which do not cross the above boundaries. Note that the FLAG waveform selection cannot be switched without resetting the FIFO.

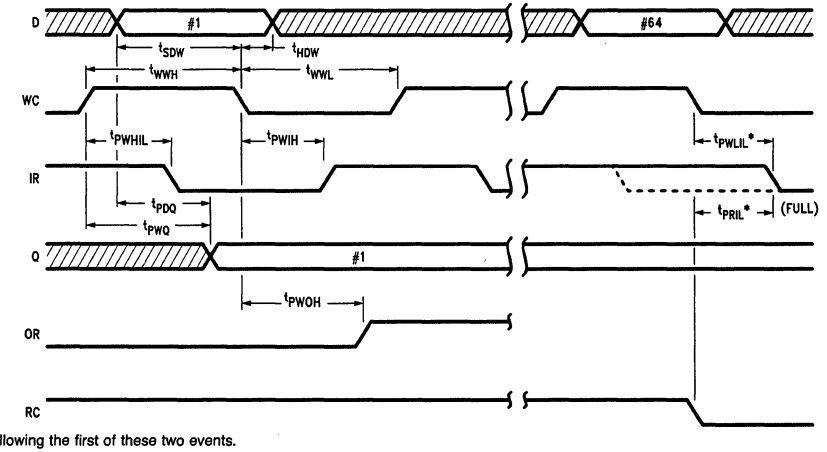
In a system, MR/FS may be connected to either a normally-low or normally-high system reset signal. Even though the FIFO responds to input transitions, conventional system reset pulses, including wakeup circuits, would produce desired results.

FIFO buffers wider than 8 bits can be implemented by connecting multiple chips in parallel. For 64 × 8n configurations, the IR, OR and FLAG status information can be taken from any one of the chips since there is no fall-through delay which may otherwise cause output skew between chips.

FIFO buffers deeper than 64 words can also be implemented by connecting multiple chips in series. To do this, the Q, OR and RC lines of one chip are connected to the D, WC and IR lines, respectively, of the next chip in the series (see "Cascading Devices" block diagram). When the first word is written into the first chip, the resulting rising edge of its OR initiates a write cycle into the second chip, which in turn produces a read cycle from the first chip. The handshaking signals passed over the OR/WC and RC/IR connections between each adjacent pair of chips causes the data word to be passed from one chip to the next until it settles onto the outputs of the last chip in the series. See "Cascaded Write Cycle Waveform" diagram.

As the buffer fills, each chip, beginning with the last, becomes full. A buffer consisting of n chips connected in series can store 63n + 1 words. This is because the last word written into each full chip (except the first chip) remains on the outputs of the previous chip. Each time a word is read from the last chip, one word is transferred down from each of the previous chips (or until an empty chip is encountered). See "Cascaded Read Cycle Waveform".

Write Cycle Timing Waveform



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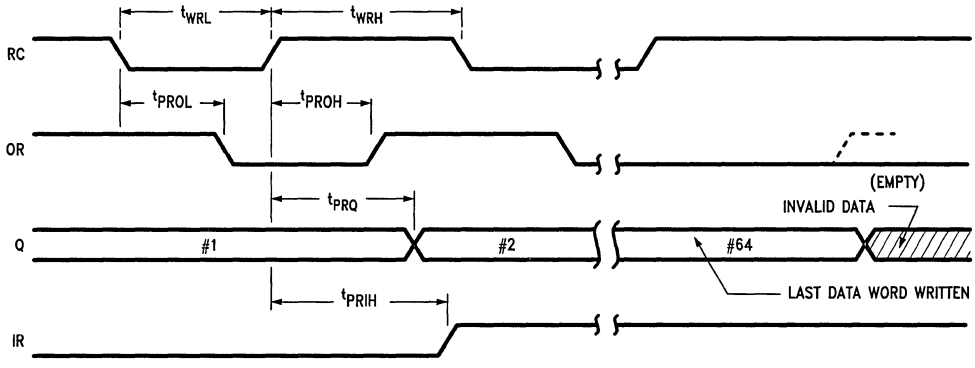
*IR goes low following the first of these two events.

Functional Description (Continued)

Since the control signals and data are passed from chip to chip in a serially cascaded buffer, some fall-through delay is introduced between the input of the first chip and the output of the last. The delay increases with the number of chips cascaded serially.

Chips can be cascaded both serially and in parallel to produce deeper and wider buffers (as shown in "Cascading Devices" block diagram). However, due to the resulting chip-level fall-through delays, it may be necessary to AND-gate the IR outputs of the first level of chips, as with the OR outputs of the last level.

Read Cycle Timing Waveform



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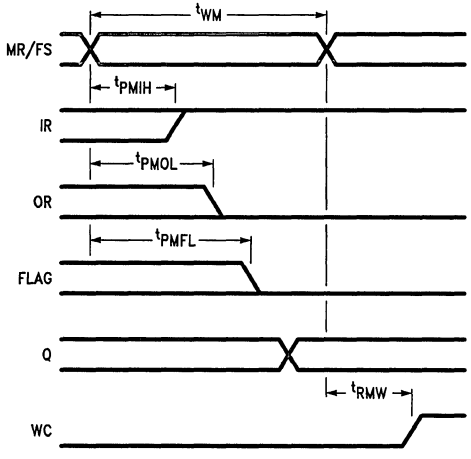
Master Reset Timing Waveform



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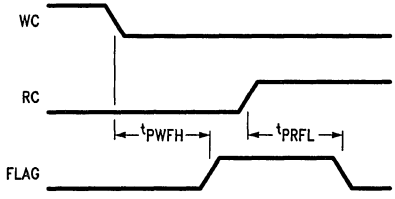
Flag Output Timing Waveform



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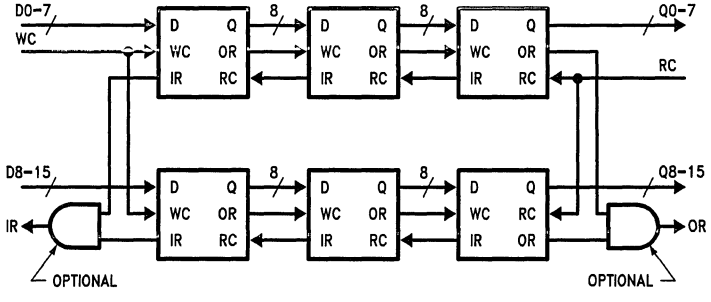
Cascading Devices
(190 × 16 Bit FIFO)



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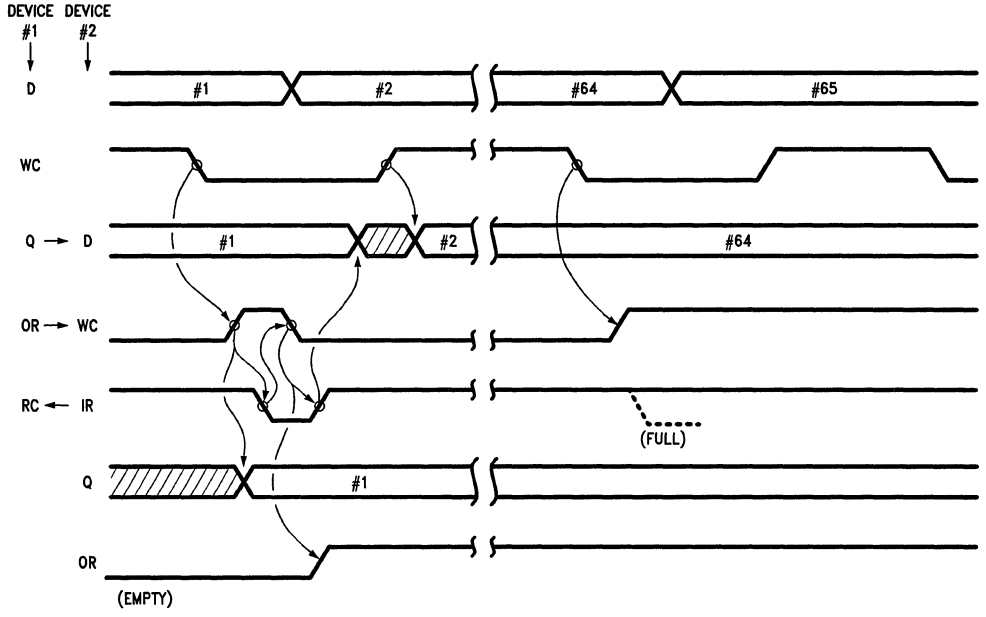
Functional Description (Continued)

Write Cycle Waveform For Two Devices Cascaded Serially



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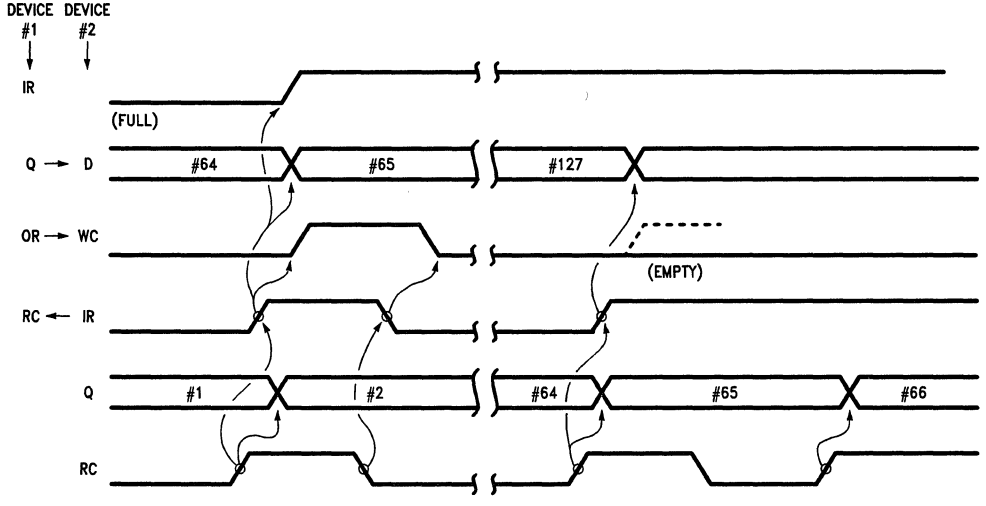
Read Cycle Waveform For Two Devices Cascaded Serially



TL/L/8676–9

National Semiconductor Corporation

PRELIMINARY
March 1987

DM75/85X432 128 x 4, DM75/85X433 128 x 5, No-Fall-Through FIFO Memories

General Description

The device is a first-in-first-out (FIFO) sequential memory organized as 128 words by either 4 or 5 bits. Data words written into the device are later read from a separate bus in the same order as entered but at an independent rate. Write and read operations may occur concurrently and at any time with respect to each other. The FIFO is a no-fall-through (NFT) type in which new input data becomes available for output in less time than the minimum write/read cycle period.

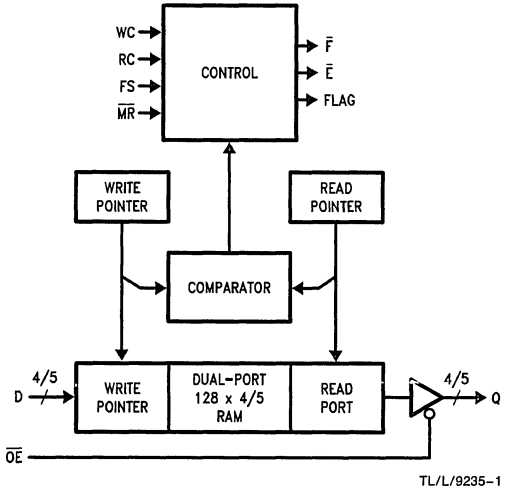
Features

- 128 x 4/5 bit FIFO memory
- No fall-through delay (first word propagates to output in less than one cycle period)
- 35 MHz write and read clock frequencies
- Totally independent asynchronous write and read clocks
- 16 mA TRI-STATE® data outputs for bus drive capability
- Status outputs indicate full, empty and partially-filled conditions
- 18/20 pin 0.3" wide DIP package
- TTL I/O signal levels
- Single +5V supply

Applications

- Data rate translator for computer peripheral controller, eg. disc, tape, printer, graphic display, etc.
- Data rate translator for telecommunications or data communications controller (including local area network)
- ADC or DAC interface buffer for real-time DSP
- Real-time data acquisition buffer
- Variable length shift register for real-time signal delay
- Variable length pipeline register for multiprocessing, DSP, graphics, image analysis, etc.

Block and Connection Diagrams



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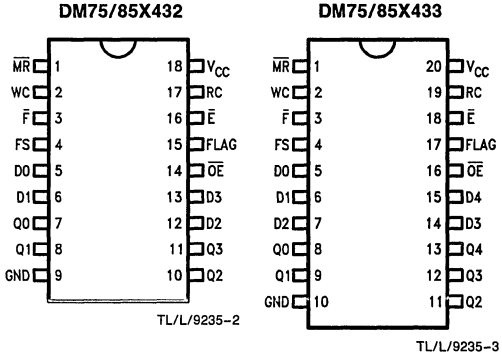
Dual-In-Line Package



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{CC}	7V
Input Voltage	7V
Off-State Output Voltage	5.5V
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 4)	To Be Determined

Electrical Characteristics Over Operating Conditions DM75/DM85X432/433

Symbol	Parameter	Conditions		Guaranteed Limits Min	Guaranteed Limits Max	Units
V_{IL}	Low-Level Input Voltage				0.8	V
V_{IH}	High-Level Input Voltage			2		V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.45V			−0.4	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.4V			50	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V			1.0	mA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OL} = 16 mA for Q Outputs I_{OL} = 4 mA for $\overline{F}$, $\overline{E}$ and FLAG Outputs		0.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, V_{IH} = 2V	I_{OH} = −2.6 mA for Q Outputs I_{OL} = −0.6 mA for $\overline{F}$, $\overline{E}$ and FLAG Outputs	2.4		V
I_{OS}	Output Short-Circuit Current (Note 1)	V_{CC} = Max, V_O = 0V		−30	−80	mA
I_{OZH}	High Voltage Off-State Output Current	V_{CC} = 5.5V, V_{OH} = 2.7V			20	μA
I_{OZL}	Low Voltage Off-State Output Current	V_{CC} = 5.5V, V_{OL} = 0.4V			−20	μA
I_{CC}	Supply Current	V_{CC} = Max, Inputs Low, Outputs Open			265	mA

Note 1: Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Operating Conditions (Note 3)

Symbol	Parameter	DM75X432/433 Min	DM75X432/433 Max	DM85X432/433 Min	DM85X432/433 Max	Units
V_{CC}	Supply Voltage	4.5	5.5	4.75	5.25	V
T_A	Operating Free-Air Temperature (Note 2)	−55	+125	0	+70	°C
t_{WWH}	WC Pulse Width High			10		ns
t_{WWL}	WC Pulse Width Low			15		ns
t_{SDW}	Input Data Setup			15		ns
t_{HDW}	Input Data Hold Time			0		ns
t_{WRH}	RC Pulse Width High			10		ns
t_{WRL}	RC Pulse Width Low			10		ns
t_{WM}	Master Reset Pulse Width					ns
t_{RMW}	Reset Recovery Time					ns

Note 2: Ambient Temperature.

Note 3: Since the FIFO is a very high speed device, care must be taken in the design of the hardware. Proper device grounding and supply decoupling are crucial to the correct operation of the FIFO.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Switching Characteristics Over Operating Conditions

Symbol	Parameter	Initial Conditions	DM75X432/433		DM85X432/433		Units
			Min	Max	Min	Max	
f_{WC}	Write Frequency					35	MHz
f_{RC}	Read Frequency					35	MHz
t_{PRQ}	RC to Data Output					20	ns
t_{PWF}	WC Rising to $\overline{F}$ Low	127 Words				15	ns
t_{PWE}	WC Rising to $\overline{E}$ High	Empty				15	ns
t_{PRE}	RC Rising to $\overline{E}$ Low	1 Word				15	ns
t_{PRF}	RC Rising to $\overline{F}$ High	Full				15	ns
t_{PWI}	WC Rising to FLAG High					20	ns
t_{PRI}	RC Rising to FLAG Low					20	ns
t_{SRW}	RC Rising Before WC	Full					ns
t_{SWR}	WC Rising Before RC	Empty					ns
t_{PDQ}	Transparent D to Q	Empty, WC = Low				30	ns
t_{PWQ}	WC Falling to Q	Empty				30	ns
t_{PMF}	MR to $\overline{F}$ High	Full				30	ns
t_{PME}	MR to $\overline{E}$ Low					30	ns
t_{PMI}	MR to FLAG Low					30	ns
t_{PZX}	Output Enable					20	ns
t_{PXZ}	Output Disable					20	ns

Pin Description

V_{CC} +5V supply.

D_0–$D_{3/4}$ 4/5-bit data input bus.

Q_0–$Q_{3/4}$ 4/5-bit data output bus (TRI-STATE non-inverted).

WC **Write Clock input**—latches in a data word from D-bus on a low-to-high transition (except when FIFO is full). Data enters the memory while WC is low.

RC **Read Clock input**—presents next data word onto Q-bus on a low-to-high transition (except when FIFO is empty).

$\overline{E}$ **Empty Status Output**—goes low when last word is read from FIFO (or when FIFO is reset); goes high when first word is written into an empty FIFO.

$\overline{F}$ **Full Status Output**—goes low when FIFO becomes full following a write; goes high when a read cycle creates a vacancy (or when FIFO is reset).

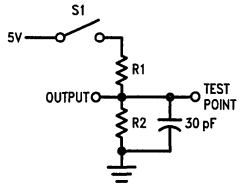
FLAG **Intermediate Status Flag Output**—high while FIFO is at least ¼ filled (32 or more words remaining in memory) if the FS input is low, or while FIFO is at least 3/4 filled (96 or more words) if FS is high; otherwise FLAG remains low.

FS **Flag Select Input**—selects FIFO word-count threshold for FLAG output (32 if low, 96 if high).

$\overline{MR}$ **Master Reset Input**—resets the FIFO to the empty state (internal pointers reset to zero) while low (level sensitive).

$\overline{OE}$ **Output Enable Input**—when low, enables output on the Q data bus; disables when high.

Standard Test Load



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I_{OL}	R1	R2
16 mA	300Ω	600Ω
4 mA	1100Ω	2200Ω

Input Pulse Amplitude = 3V

Input Rise and Fall Time (10%–90%) = 2.5 ns

t_{PHZ} measurement made at V_{OH} − 0.5V, t_{PLZ} measurement made at V_{OL} + 0.5V, all other measurements made at 1.5V.

Functional Description

The RAM contents addressed by the read pointer (also initially zero) are presented on the Q outputs whenever the $\overline{OE}$ input is low (Q bus outputs are disabled when $\overline{OE}$ is high). Thus the first word may appear on the Q outputs as it is being written. The rising edge of RC increments the read pointer which then accesses the next data word from the RAM's read port. (Each pointer automatically wraps around from the last to the first RAM location.)

When the value of the read pointer becomes equal to the write pointer due to a read cycle, then the FIFO is empty, ie. any data words which had been written have also been read. When the value of the write pointer exceeds the read pointer by 128 due to a write cycle, then the FIFO is full, ie. the next RAM location into which data should be written contains the oldest word that has not yet been read.

The $\overline{E}$ and $\overline{F}$ status outputs indicate the empty and full conditions, respectively. Initially (following a reset) $\overline{F}$ is high. When WC is brought high at the end of any write cycle, $\overline{F}$ would go low if the FIFO becomes full; otherwise it remains high (without glitches). When the FIFO is full, $\overline{F}$ remains low until a vacant RAM location is made available resulting from a read operation (or the Master Reset is activated). $\overline{F}$ goes high after the rising edge of RC which creates the first vacancy.

Writing is inhibited while $\overline{F}$ is low. If WC is brought low while $\overline{F}$ was still low, new data would not begin to be written into the RAM until after a read cycle causes $\overline{F}$ to go high (WC must then remain low long enough to complete the write cycle). Any low-to-high transitions on WC while $\overline{F}$ is low are ignored (write pointer not incremented).

Initially (followinig a reset) the $\overline{E}$ output is low. $\overline{E}$ remains low while the FIFO is empty until the first write cycle is completed. $\overline{E}$ goes high after the rising edge of WC concluding the first write cycle. When RC is brought high at the end of any read cycle, $\overline{E}$ would go low if the FIFO becomes emtpy; otherwise it remains high (without glitches).

Reading is inhibited while $\overline{E}$ is low. Any low-to-high transitions on RC while $\overline{E}$ is low are ignored (read pointer not incremented). While the FIFO is empty, the Q outputs (if enabled) would either be in an indetermined state if WC is high, or would reflect D input data as it is written into the memory if WC is low.

The FIFO is reset to the empty state (write and read pointers reset to zero) while the $\overline{MR}$ input is low. WC and RC inputs are ignored and may be in either state during a reset. If WC is low following a reset, it should remain low long enough to complete the write cycle.

The FS input selects the waveform to appear on the FLAG output. When FS is low, then the FLAG output indicates when the FIFO is at least one quarter filled (i.e., when the write pointer value exceeds the read pointer by at least 32). When FS is high, then FLAG indicates when the FIFO is at least three quarters filled (write pointer exceeds read pointer by at least 96). The FLAG output remains stable (without glitches) except following the write or read cycle which changes the FIFO's status with respect to the selected threshold.

It is recommended that the FS input be changed only while the FIFO is empty or full. If FS is changed while the FIFO contains between 32 and 96 words, the FLAG output may not change to reflect the accurate status until a threshold is crossed.

FLAG Output Truth Table:

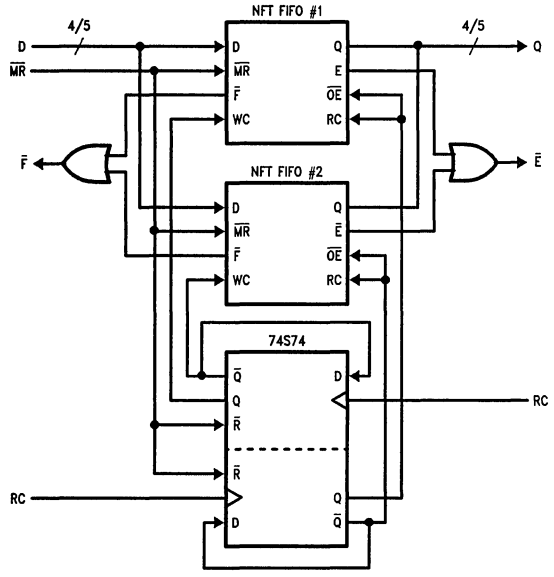
# Words Stored	FLAG Output	
	FS = L	FS = H
0–31	L	L
32–95	H	L
96–128	H	H

FIFO buffers wider than 4 or 5 bits can be implemented by connecting multiple chips in parallel. The $\overline{E}$, $\overline{F}$ and FLAG status information can be taken from any one of the chips since there is no fall-through delay which may otherwise cause output skew between chips.

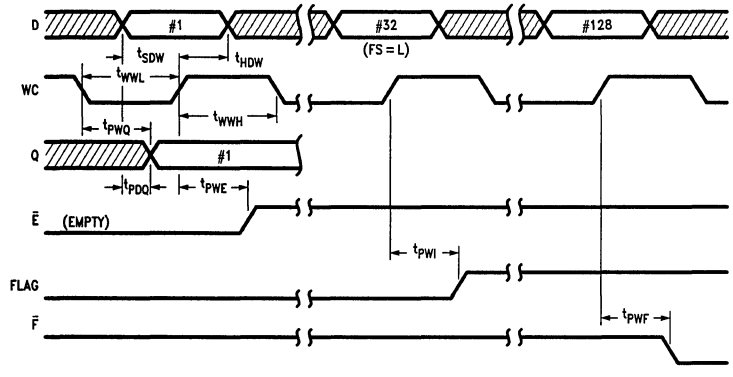
FIFO buffers deeper than 128 words could also be implemented by connecting the D and Q lines of multiple devices in parallel and alternating the WC and RC clocks between each of the devices in turn (the $\overline{OE}$ input of each device must then be connected to its own RC input). For example, a 256 x 4/5 FIFO buffer could be implemented using two FIFO chips plus a dual D-type flip-flop (eg. 74S74) as shown in the diagram, "External Cascading". Cascading more than two devices (depth greater than 256) requires more sophisticated logic to generate the alternating WC and RC clocks; registered programmable logic devices may be useful for this. Note that when cascading in this manner, there are no additional delays introduced. Also, the threshold boundaries for the FLAG output are proportional to the number of devices cascaded.

Functional Description (Continued)

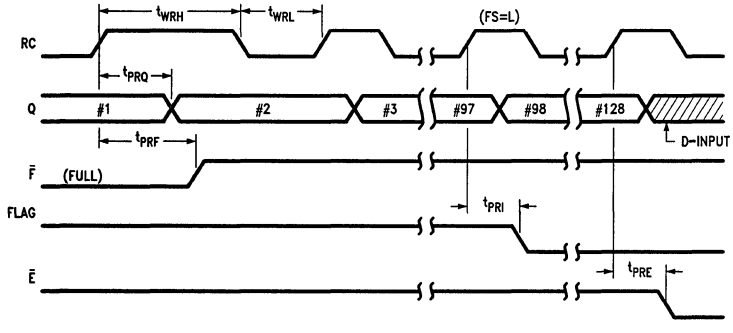
External Cascading (256 x 4/5 FIFO)



Write Cycle Timing

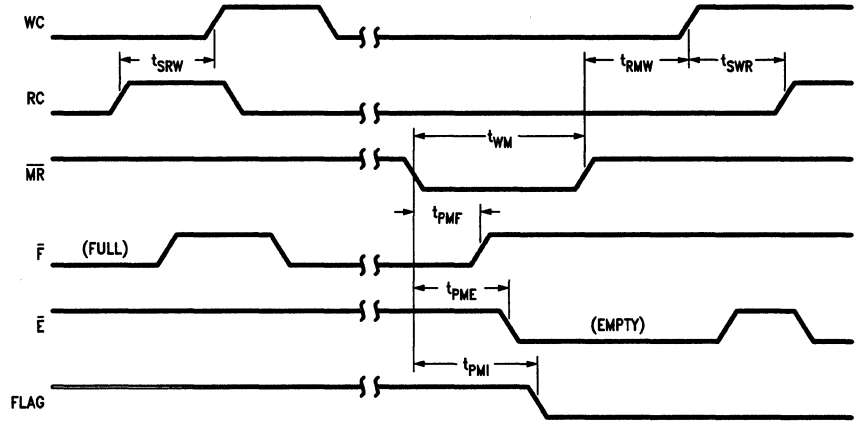


Read Cycle Timing



Functional Description (Continued)

Reset and Miscellaneous Timing



TL/L/9235–7

Section 4

ECL RAMs

Section 4 Contents

National Semiconductor Corporation

March 1987

DM10414/DM10414A
256 x 1 ECL Random Access Memory

General Description

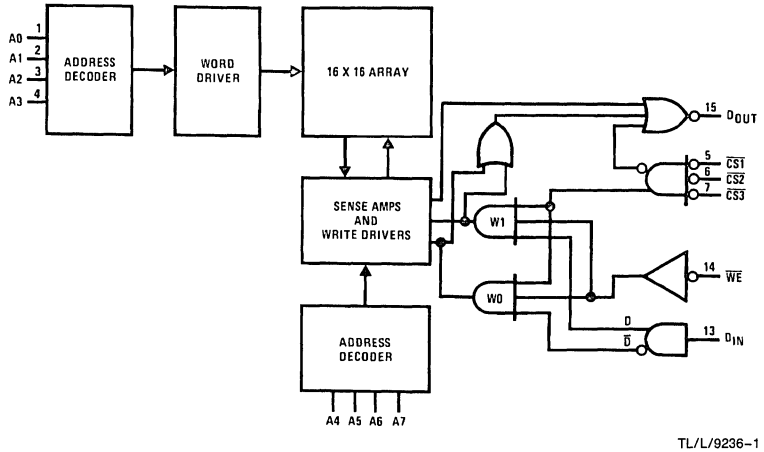
The DM10414, DM10414A is a 256-word by 1-bit ECL random access memory. The fully static memory is designed with active low chip selects and separate I/O pins. The 8 address bits (A0 through A7) are fully decoded on the chip. Applications such as scratch pad, cache, and buffer memories are ideal for this high speed RAM.

An unterminated emitter-follower output is provided to allow the outputs to be wire-ORed. Separate Data In and non-inverted Data Out pins are provided. These RAMs are compatible with compensated and uncompensated 10k ECL families.

Features

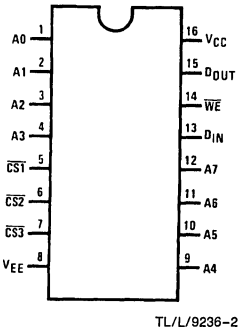
- Fully compatible with standard and voltage compensated 10k series ECL
- Temperature range 0°C to +75°C
- Unterminated emitter-follower output for wire-ORing
- Power dissipation decreases with increasing temperature
- Typical address access
  - DM10414 10 ns
  - DM10414A 7 ns
- Typical chip select access
  - DM10414 4 ns
  - DM10414A 3 ns

Block and Connection Diagrams



TL/L/9236-1

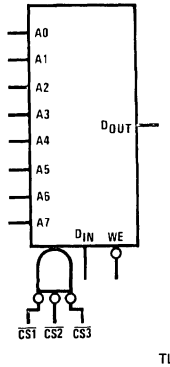
Dual-In-Line Package



TL/L/9236-2

Top View
Order Number DM10414J or DM10414AJ
See NS Package J16A

Logic Symbol



TL/L/9236-3

Pin Names

A0–A7	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$	Chip Select Inputs
$\overline{WE}$	Write Enable

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	L	Not Selected
L	L	H	L	Write 1
L	L	L	L	Write 0
L	H	X	D_{OUT}	Read

L = low (−1.7V nominal)
H = high (−0.9 nominal)
X = don't care

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias (ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to +75°C (Notes 1–3)

Symbol	Parameter	Conditions	T_A	Min Limit	Max Limit	Units
V_{OH}	Output Voltage High	V_{IN} = V_{IHMAX} or V_{ILMIN}	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	V_{IN} = V_{IHMAX} or V_{ILMIN}	0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	V_{IN} = V_{IHMIN} or V_{ILMAX} Performed on One Input at a Time	0°C +25°C +75°C	−1020 −980 −920		mV
V_{OLC}	Output Voltage Low	V_{IN} = V_{IHMIN} or V_{ILMAX} Performed on One Input at a Time	0°C +25°C +75°C		−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	V_{IN} = V_{IHMAX} Performed on One Input at a Time	0°C to +75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	V_{IN} = V_{ILMIN} Performed on One Input at a Time	0°C to +75°C	0.5 −50	170	μA
I_{EE}	Power Supply Current (Pin 8) (Note 4)	All Inputs and Outputs Open	0°C to +75°C	−150		mA

Note 1: Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Guaranteed with transverse air flow exceeding 500 linear F. P. M. and 2-minute warm-up period. Typical resistance values of the package are: θ_{JA}, (Junction to Ambient) = 90°C/W (still air); θ_{JA} (Junction to Ambient) = 50°C/W (at 500 F. P. M. air flow); θ_{JC} (Junction to Case) = 25°C/W.

Note 4: Typical values at V_{EE} = −5.2V: T_A = 0°C, I_{EE} = −105 mA; T_A = 75°C, I_{EE} = −90 mA.

Functional Description

Addressing the DM10414, DM10414A is achieved by means of the 8 address lines A0–A7. Each of the 2^8 one-zero combinations of the address lines corresponds to a bit location in the memory. The active low Chip Selects together with the unterminated emitter-follower output allows for wire-OR-ing. A 50Ω resistor to −2V (or an equivalent network) is required to provide a low at the output when the device is off. This termination is required for both single device or wire-ORed operation.

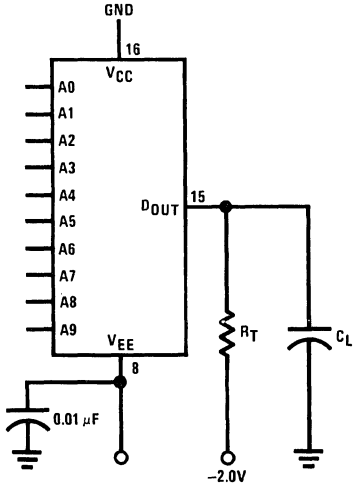
The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. The operating mode is controlled by the active low Write Enable ($\overline{WE}$). $\overline{WE}$ low causes the data at the Data Input (D_{IN}) to be stored at the selected address. $\overline{WE}$ low also causes the output to be disabled (low due to the 50Ω pull-down resistor). $\overline{WE}$ high causes the data stored at the selected address to be present at the Data Out (D_{OUT}) pin.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C, air flow exceeding 500 LFM

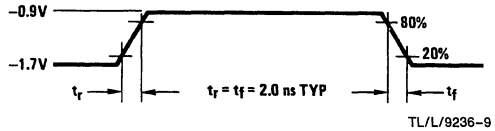
TEST CONDITIONS

Loading Conditions



TL/L/9236–8

Inputs Levels



TL/L/9236–9

All timing measurements referenced to 50% of input levels

C_L = 30 pF including jig and stray capacitance

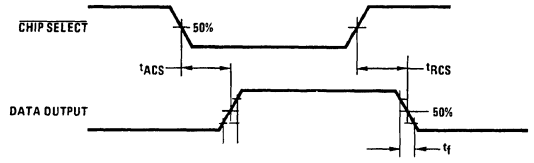
R_T = 50Ω

Symbol	Parameter	DM10414A		DM10414		Units
		Min	Max	Min	Max	
READ MODE						
t_{AA}	Address Access Time (Note 5)		10		15	ns
t_{ACS}	Chip Select Access Time		5		7	ns
t_{RCS}	Chip Select Recovery Time		5		7	ns

Note 5: The maximum address access time is guaranteed to be the worst-case bit in the memory using a pseudorandom testing pattern.

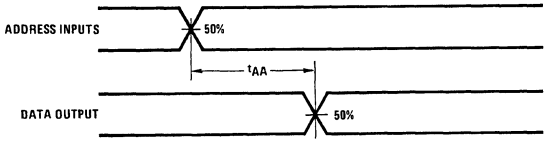
Switching Time Waveforms

Chip Select Access Time



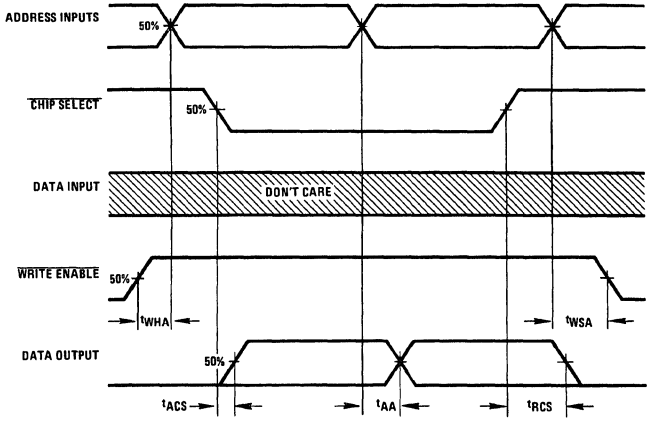
TL/L/9236-4

Address Access Time



TL/L/9236-5

Read Mode



TL/L/9236-6

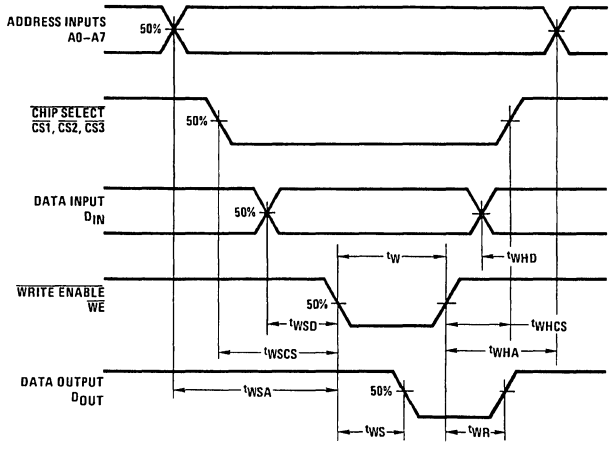
AC Electrical Characteristics (Continued)

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C, 500 LFM

Symbol	Parameter	DM10414A		DM10414		Units
		Min	Max	Min	Max	
WRITE MODE						
t_W	Write Pulse Width	6		8		ns
t_{WSD}	Data Set-Up Time Prior to Write	2		2		ns
t_{WHD}	Data Hold Time After Write	2		2		ns
t_{WSA}	Address Set-Up Time Prior to Write	3		4		ns
t_{WHA}	Address Hold Time After Write	2		3		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write	2		2		ns
t_{WHCS}	Chip Select Hold Time After Write	2		2		ns
t_{WS}	Write Disable Time		5		7	ns
t_{WR}	Write Recovery Time		5		7	ns

Switching Time Waveforms (Continued)

Write Mode



TL/L/9236–7

AC Electrical Characteristics (Continued)

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C, 500 LFM

Symbol	Parameter	DM10414A		DM10414		Units
		Min	Max	Min	Max	
RISE TIME AND FALL TIME						
t_r	Output Rise Time	1	3.5	1	3.5	ns
t_f	Output Fall Time	1	3.5	1	3.5	ns

Capacitance

Symbol	Parameter	Conditions	DM10414A			DM10414			Units
			Min	Typ (Note 5)	Max	Min	Typ (Note 5)	Max	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		4	5		4	5	pF
C_{OUT}	Output Pin Capacitance			7	8		7	8	pF

National Semiconductor Corporation

April 1987

DM10415/DM10415A
1024 x 1 ECL Random Access Memory

General Description

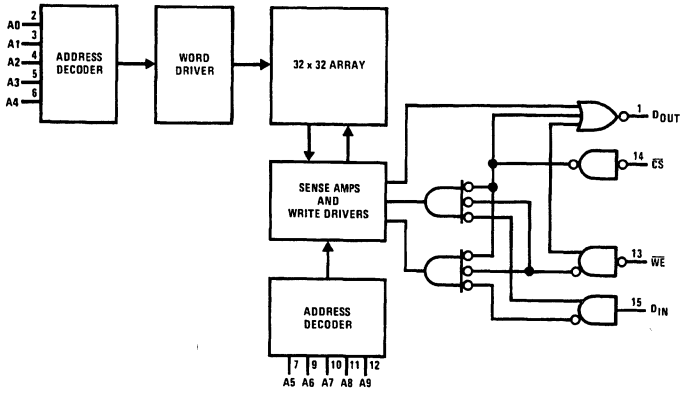
The DM10415, DM10415A is a 1024-word by 1-bit ECL random access memory. This fully static memory is designed with an active low chip select and separate I/O pins. The 10 address bits (A0 through A9) are fully decoded on the chip. Applications such as scratch pad, cache, and buffer memories are ideal for this high speed RAM.

An unterminated emitter-follower output is provided to allow the outputs to be wire-ORed. Separate Data In and non-inverted Data Out pins are provided. These RAMs are compatible with compensated and uncompensated 10k ECL families.

Features

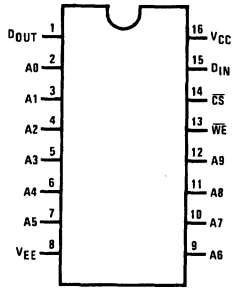
- Fully compatible with standard and voltage compensated 10k series ECL
- Temperature range 0°C to +75°C
- Unterminated emitter-follower output for wire-ORing
- Power dissipation decreases with increasing temperature
- Typical address access
  - DM10415 20 ns
  - DM10415A 12 ns
- Typical chip select access
  - DM10415 6 ns
  - DM10415A 4 ns

Block and Connection Diagrams



TL/L/9237–1

Dual-In-Line Package

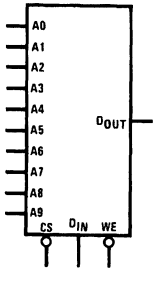


TL/L/9237–2

Top View

Order Number DM10415J or DM10415AJ
See NS Package J16A

Logic Symbol



TL/L/9237–3

Pin Names

A0–A9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable

Truth Table

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	X	X	L	Not Selected
L	L	H	L	Write 1
L	L	L	L	Write 0
L	H	X	D_{OUT}	Read

L = low (−1.7V nominal)
H = high (−0.9V nominal)
X = don't care

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V, Output Load = 50Ω and 30 pF to −2.0V, T_A = 0°C to +75°C (Notes 1–3)

Symbol	Parameter	Conditions	T_A	Min Limit	Max Limit	Units
V_{OH}	Output Voltage High	V_{IN} = V_{IHMAX} or V_{ILMIN}	0°C +25°C +75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	V_{IN} = V_{IHMAX} or V_{ILMIN}	0°C +25°C +75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	V_{IN} = V_{IHMIN} or V_{ILMAX}	0°C +25°C +75°C	−1020 −980 −920		mV
V_{OLC}	Output Voltage Low	V_{IN} = V_{IHMIN} or V_{ILMAX}	0°C +25°C +75°C		−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C +25°C +75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C +25°C +75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	V_{IN} = V_{IHMAX}	0°C to +75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	V_{IN} = V_{ILMIN}	0°C to +75°C	0.5 −50	170	μA
I_{EE}	Power Supply Current (Pin 8) (Note 4)	All Inputs and Outputs Open	0°C to +75°C	−150		mA

Note 1: Conditions for testing not shown in the tables are chosen to guarantee operation under "worst case" conditions.

Note 2: The specified limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.

Note 3: Guaranteed with transverse air flow exceeding 500 linear F. P. M. and 2-minute warm-up period. Typical resistance values of the package are: θ_{JA}, (Junction to Ambient) = 90°C/W (still air); θ_{JA} (Junction to Ambient) = 50°C/W (at 500 F. P. M. air flow); θ_{JC} (Junction to Case) = 25°C/W.

Note 4: Typical values at V_{EE} = −5.2V: T_A = 0°C, I_{EE} = −105 mA; T_A = 75°C, I_{EE} = −90 mA.

Functional Description

Addressing the DM10415/DM10415A is achieved by means of the 10 address lines A0–A9. Each of the 2^{10} one-zero combinations of the address lines corresponds to a bit location in the memory. The active low Chip Select ($\overline{CS}$) together with the unterminated emitter-follower output allows for memory array expansion to 2048 words without additional decoding. This emitter-follower output allows for wire-ORing. A 50Ω resistor to −2V (or an equivalent network) is required to provide a low at the output when the device is off. This termination is required for both single device or wire-ORed operation.

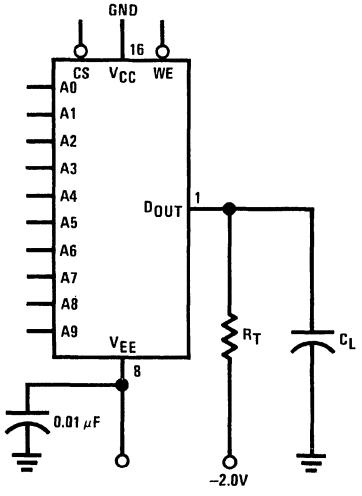
The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. The operating mode is controlled by the active low Write Enable ($\overline{WE}$). $\overline{WE}$ low causes the data at the Data Input (D_{IN}) to be stored at the selected address. $\overline{WE}$ low also causes the output to be disabled (low due to the 50Ω pull-down resistor). $\overline{WE}$ high causes the data stored at the selected address to be present at the Data Out (D_{OUT}) pin.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C, Airflow exceeding 500 LFM

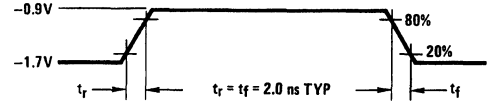
TEST CIRCUIT AND INPUT WAVEFORM

Loading Conditions



TL/L/9237–8

Input Levels



TL/L/9237–9

All timing measurements referenced to 50% of input levels

C_L = 30 pF including jig and stray capacitance

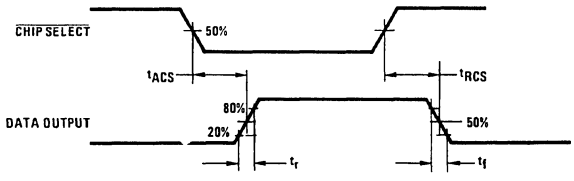
R_T = 50Ω

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C, Airflow exceeding 500 LFM (Continued)

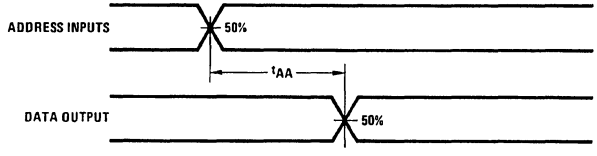
READ CYCLE TIMING DIAGRAMS

Select Access Time



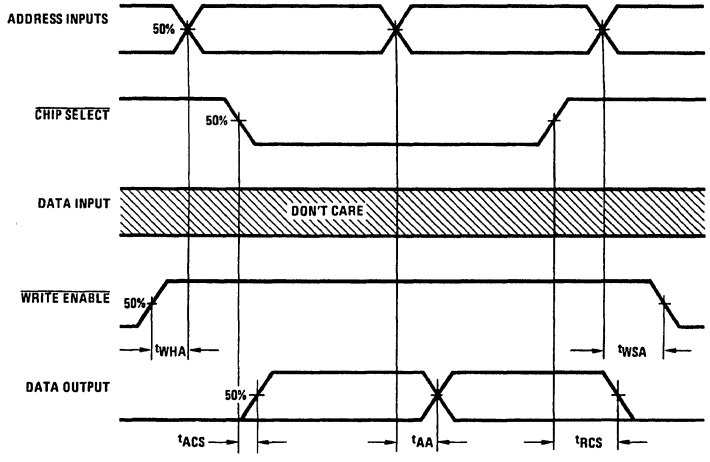
TL/L/9237–4

Address Access Time



TL/L/9237–5

Read Mode



TL/L/9237–6

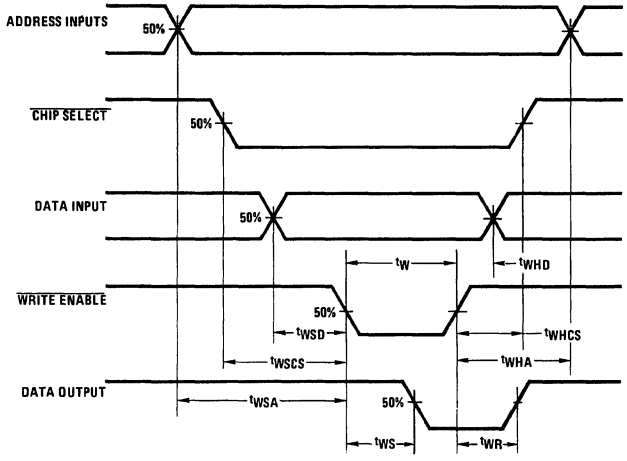
Symbol	Parameter	DM10415A		DM10415		Units
		Min	Max	Min	Max	
READ CYCLE						
t_{AA}	Address Access Time (Note 5)		20		35	ns
t_{ACS}	Chip Select Access Time		8		10	ns
t_{RCS}	Chip Select Recovery Time		8		10	ns

Note 5: The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, Output Load = 50Ω, 30 pF to −2.0V, T_A = 0°C to 75°C, Airflow exceeding 500 LFM (Continued)

WRITE CYCLE TIMING DIAGRAMS



TL/L/9237–7

Symbol	Parameter	DM10415A		DM10415		Units
		Min	Max	Min	Max	
WRITE CYCLE						
t_W	Write Pulse Width (to Guarantee Writing)	12		25		ns
t_{WSD}	Data Set-Up Time Prior to Write	4		5		ns
t_{WHD}	Data Hold Time After Write	4		5		ns
t_{WSA}	Address Set-Up Time Prior to Write	5		8		ns
t_{WHA}	Address Hold Time After Write	3		4		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write	4		5		ns
t_{WHCS}	Chip Select Hold Time After Write	4		5		ns
t_{WS}	Write Disable Time		10		10	ns
t_{WR}	Write Recovery Time		10		10	ns
RISE TIME AND FALL TIME						
t_r	Output Rise Time	1	3, 5	1	3, 5	ns
t_f	Output Fall Time	1	3, 5	1	3, 5	ns

Capacitance

Symbol	Parameter	DM10415A		DM10415		Units
		Min	Max	Min	Max	
C_{IN}	Input Pin Capacitance		5		5	pF
C_{OUT}	Output Pin Capacitance		8		8	pF

National Semiconductor Corporation

December 1986

DM10422/DM10422A/DM10422A-7 1024-Bit (256 x 4) ECL RAM

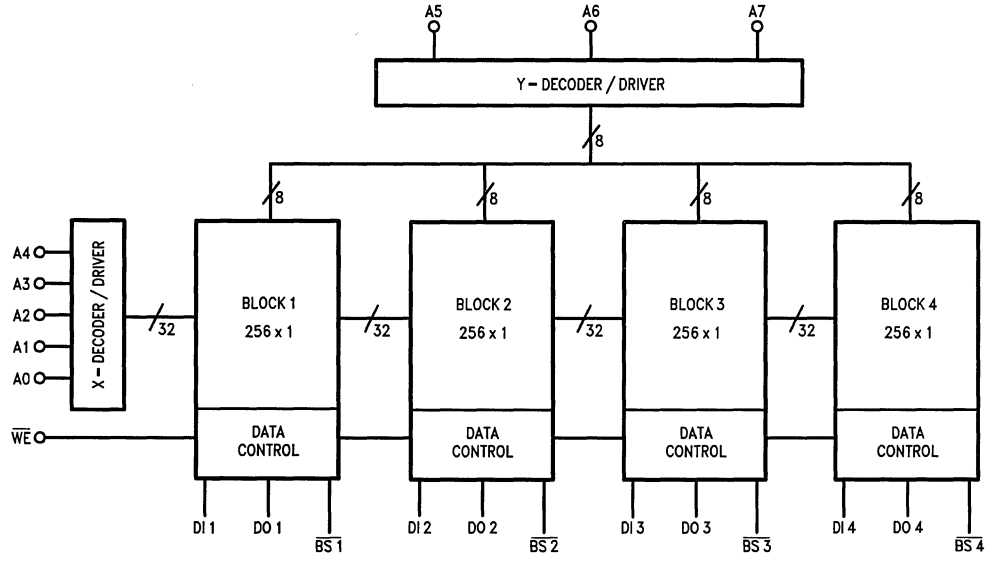
General Description

The DM10422/DM10422A/DM10422A-7 is a 1024-bit ECL random access memory organized as 4 blocks of 256 bits. Since each block has its own Select input, the memory can be configured for a maximum of 1024 by 1 bit through Wire-ORing of the outputs. The high-speed access time allows its use in scratch pad, buffer, and control storage applications. The device is voltage compensated and is compatible with all 10k ECL logic. Separate Data In and Data Out pins allow the set-up of data for a write cycle while performing a read.

Features

- 4 separate Block Select inputs for configurations from 256 x 4 to 1024 x 1
- Maximum address access time—DM10422 12 ns
  —DM10422A 10 ns
  —DM10422A-7 7 ns
- Maximum Block Select access time—DM10422 5 ns
  —DM10422A 5 ns
  —DM10422A-7 4 ns
- 10 kH logic compatible with on-chip voltage compensation
- Oxide isolation process
- Unterminated emitter-follower output for easy memory expansion
- Compatible with HM10422, MBM10422 and F10422

Block Diagram



TL/L/8693–10

Truth Table (Positive Logic)

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	DI		
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = High Voltage Level L = Low Voltage Level X = Don't Care

Pin Names

$\overline{BS1}$–$\overline{BS4}$	Block Selects
A0–A7	Address Inputs
$\overline{WE}$	Write Enable
DI1–DI4	Data Inputs
DO1–DO4	Data Outputs

4

Functional Description

Addressing the DM10422/DM10422A/DM10422A-7 is accomplished by means of the eight address lines (A0–A7). Each of the 256 possible combinations of address inputs corresponds to a unique four-bit word in the memory array. The availability of four active-low Block Select inputs ($\overline{BS1}$–$\overline{BS4}$) and the unterminated emitter-follower outputs allow the user to reconfigure the part into a 512 x 2 or 1024 x 1 architecture by wire-ORing the outputs and using the BS inputs as address lines.

The device is selected with $\overline{BS}$ low and deselected with $\overline{BS}$ high. A 50Ω resistor to −2V (or an equivalent network) is required to provide a logic low at the output when the device is turned off. This termination is required for both single device and wire-ORed operation. The $\overline{BS}$ inputs are internally pulled low so that in cases where no memory expansion is needed, no external connections are required.

The read and write operations are controlled by the active-low Write Enable input ($\overline{WE}$). With $\overline{WE}$ and $\overline{BS}$ held low, the data at the Data Inputs (DI1–DI4) is written into addressed location. $\overline{WE}$ low also causes the output to be disabled; the termination will then pull the output low. To read, $\overline{WE}$ is held high, while $\overline{BS}$ is held low. The rising edge of $\overline{WE}$ causes the data present at the selected address to be transferred to the Data Outputs (DO1–DO4). The data presented at the Data Outputs is non-inverted.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

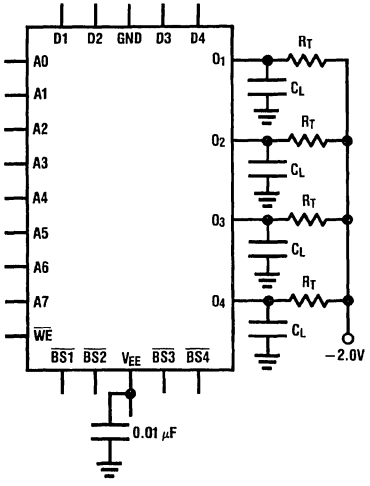
DC Electrical Characteristics V_{EE} = −5.2V, R_T = 50Ω to −2.0V, T_A = 0°C to +75°C, airflow ≥ 500 LFM

Symbol	Parameter	Conditions	T_A	Min	Max	Units
V_{OH}	Output Voltage High	V_{IN} = V_{IH} Max or V_{IL} Min	0°C 25°C 75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	V_{IN} = V_{IH} Max or V_{IL} Min	0°C 25°C 75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	V_{IN} = V_{IH} Min or V_{IL} Max	0°C 25°C 75°C	−1020 −980 −920	— — —	mV
V_{OLC}	Output Voltage Low	V_{IN} = V_{IH} Min or V_{IL} Max	0°C 25°C 75°C	— — —	−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C 25°C 75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C 25°C 75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	V_{IN} = V_{IH} Max	0°C to 75°C	—	220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	V_{IN} = V_{IL} Min	0°C to 75°C	0.5 −50	170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open	0°C to 75°C	−200	—	mA

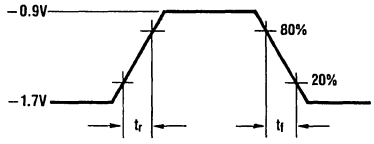
AC Electrical Characteristics

$V_{CC} = V_{CCA} = 0V$, $V_{EE} = -5.2V \pm 5\%$, $R_T = 50\Omega$ to $-2.0V$, $C_L = 30$ pF, $T_A = 0°C$ to $+75°C$, air flow exceeding 500 LFM

Test Circuit and Input Waveform



TL/L/8693–5



TL/L/8693–6

$t_r = t_f = 2.0$ ns $\pm 10\%$

$R_T = 50\Omega$

$C_L = 30$ pF

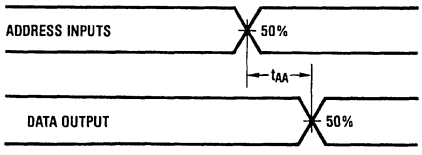
All timing measurements are referenced from 50% of input levels to 50% of input/output levels.

Read Cycle

Symbol	Parameter	DM10422		DM10422A		DM10422A-7		Units
		Min	Max	Min	Max	Min	Max	
t_{AA}	Address Access Time	—	12	—	10	—	7	ns
t_{ABS}	Block Select Access Time	—	5	—	5	—	4	ns
t_{RBS}	Block Select Recovery Time	—	5	—	5	—	4	ns

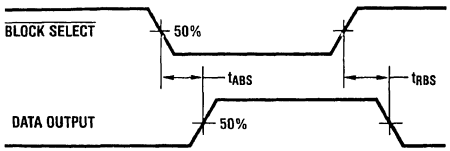
Read Cycle Timing Diagrams

Address Access Time



TL/L/8693–7

Block Select Access

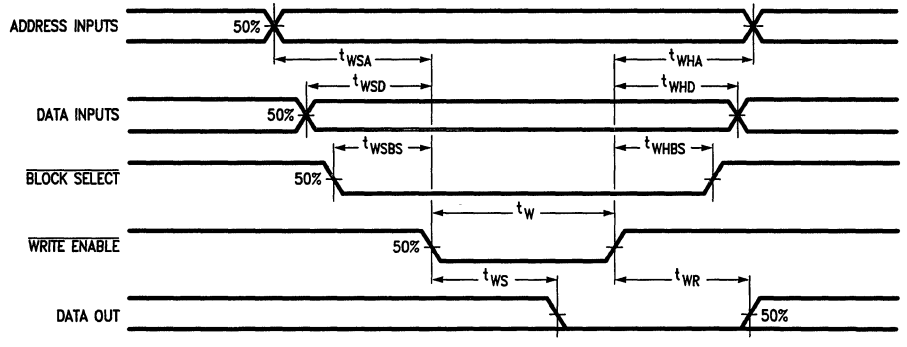


TL/L/8693–8

Write Cycle

Symbol	Parameter	DM10422		DM10422A		DM10422A-7		Units
		Min	Max	Min	Max	Min	Max	
t_W	Write Pulse Width	7	—	6	—	5	—	ns
t_{WSD}	Data Set-Up Time	2.0	—	2.0	—	1.0	—	ns
t_{WHD}	Data Hold Time	2.0	—	2.0	—	1.0	—	ns
t_{WSA}	Address Set-Up Time	3.0	—	2.0	—	1.0	—	ns
t_{WHA}	Address Hold Time	2.0	—	2.0	—	1.0	—	ns
t_{WSBS}	Block Select Set-Up Time	2.0	—	2.0	—	1.0	—	ns
t_{WHBS}	Block Select Hold Time	2.0	—	2.0	—	1.0	—	ns
t_{WS}	Write Disable Time		5	—	5	—	4	ns
t_{WR}	Write Recovery Time		7	—	7	—	7	ns

Write Cycle Timing Diagram



TL/L/8693–11

Rise Time and Fall Time

Symbol	Parameter	DM10422		DM10422A		DM10422A-7		Units
		Min	Max	Min	Max	Min	Max	
t_r	Output Rise Time	1	3.5	1	3.5	1	3.5	ns
t_f	Output Fall Time	1	3.5	1	3.5	1	3.5	ns

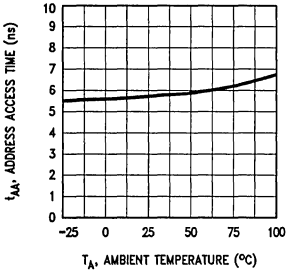
Capacitance

Symbol	Parameter	DM10422		DM10422A		DM10422A-7		Units
		Min	Max	Min	Max	Min	Max	
C_{IN}	Input Capacitance	—	5	—	5	—	5	pF
C_{OUT}	Output Capacitance	—	8	—	8	—	8	pF

Typical Performance Characteristics

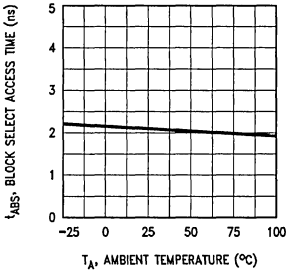
Address Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



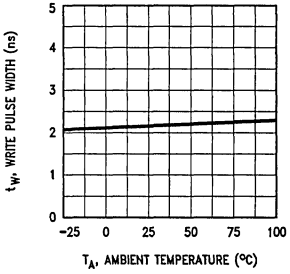
Block Select Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Write Pulse Width vs Ambient Temperature

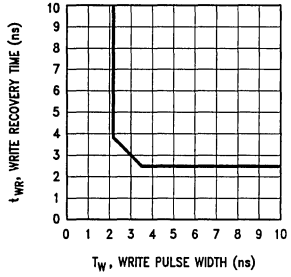
NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



TL/L/8693–12

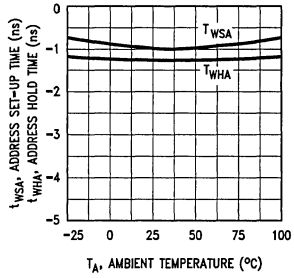
Write Recovery Time vs Write Pulse Width

25 °C, NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



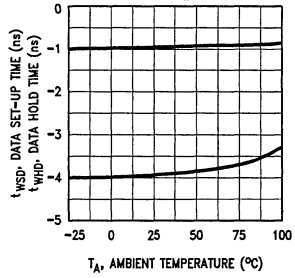
Address Setup and Hold Times vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW T_W = 19 ns



Data Setup and Hold Times vs Ambient Temperature

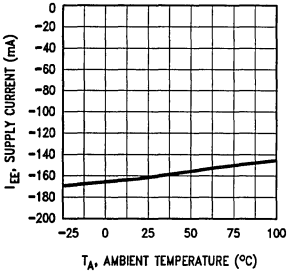
NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW T_W = 10 ns



TL/L/8693–13

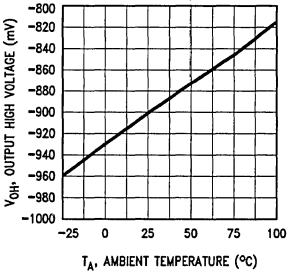
Supply Current (I_{EE}) vs Ambient Temperature

NOMINAL V_{EE}, INPUTS OPEN AND SPECIFIED AIRFLOW



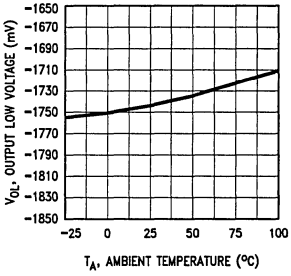
Output High Voltage (V_{OH}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Output Low Voltage (V_{OL}) vs Ambient Temperature

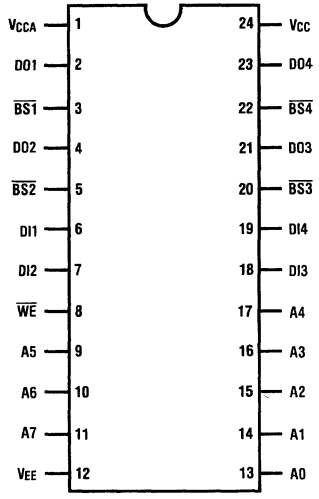
NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



TL/L/8693–14

Connection Diagrams

Dual-In-Line Package

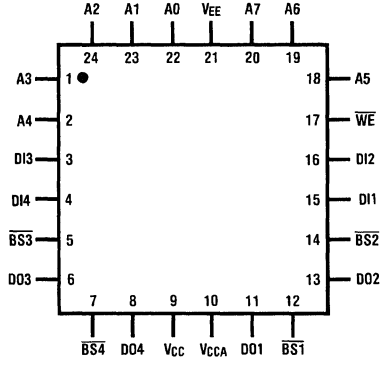


TL/L/8693–2

Top View

Order Number DM10422J, DM10422AJ or DM10422A-7J
See NS Package Number J24E

Quad Cerpack



TL/L/8693–4

Order Number DM10422W, DM10422AW or DM10422A-7W
See NS Package Number W24B

National Semiconductor Corporation

February 1987

DM10470/DM10470A 4096-Bit (4096 x 1) ECL RAMs

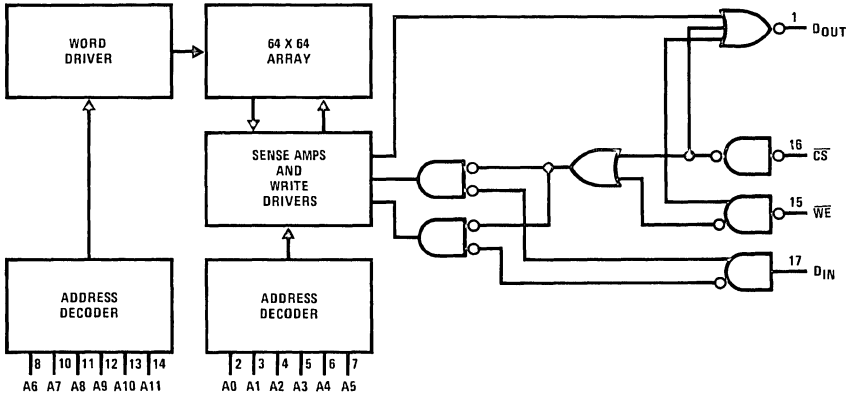
General Description

The DM10470/DM10470A is a fully decoded 4096-bit, 10K and 10 KH compatible, ECL read/write random access memory designed for high-speed scratch pad and buffer storage applications. This device is organized as 4096 words by 1 bit and has separate Data In and Data Out pins. On-chip voltage compensation is provided for improved noise margin. The active low Chip Select and unterminated emitter-follower outputs allow for easy expansion.

Features

- Two speed selected offerings for maximum cost-performance:
  - DM10470 — 25 ns/200 mA max
  - DM10470A — 15 ns/200 mA max
- 4096 x 1 bit organization
- 10K and 10 KH logic compatible
- On-chip voltage compensation for improved noise margin
- Oxide isolation process
- Unterminated emitter-follower outputs for easy memory expansion
- Compatible with HM10470, MBM10470 and F10470

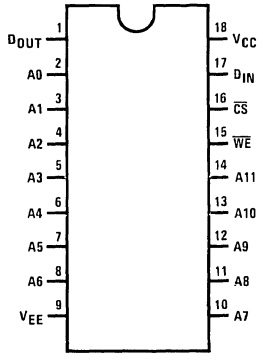
Logic Diagram



TL/L/7723-1

Connection Diagram

Dual-In-Line Package



TL/L/7723-2

Top View

Order Numbers DM10470J, DM10470AJ
See NS Package Number J18A

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Pin Names

$\overline{CS}$	Chip Select Input
A0–A11	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Functional Description

Addressing the DM10470/DM10470A is achieved by means of the twelve address lines (A0–A11). Each of the 2^{12} possible combinations of address inputs corresponds to a unique bit location in memory. The memory array can be expanded by wire-ORing the unterminated emitter-follower outputs of two or more devices and using the active-low Chip Select ($\overline{CS}$) inputs as address lines.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. A 50Ω resistor to −2V (or an equivalent network) is required to provide a logic low at the output when the device is turned off. This termination is required for both single device and wire-ORed operation. The $\overline{CS}$ input is internally pulled low so that in cases where no memory expansion is needed, no external connections are required.

The read and write operations are controlled by the state of the active-low Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held low, the data at the Data Input (D_{IN}) is written into the addressed location. $\overline{WE}$ low also disables the output; the termination will then pull the output low. To read, $\overline{WE}$ is held high while $\overline{CS}$ is held low. The rising edge of $\overline{WE}$ causes data at the addressed location to be transferred to the Data Output (D_{OUT}). The Data presented at D_{OUT} is non-inverted.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD Rating is to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics

V_{EE} = −5.2V, R_T = 50Ω to −2.0V, T_A = 0°C to +75°C, airflow exceeding 500 LFM

Symbol	Parameter	Conditions	T_A	Min	Max	Units
V_{OH}	Output Voltage High	V_{IN} = V_{IH} Max or V_{IL} Min	0°C 25°C 75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	V_{IN} = V_{IH} Max or V_{IL} Min	0°C 25°C 75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	V_{IN} = V_{IH} Min or V_{IL} Max	0°C 25°C 75°C	−1020 −980 −920		mV
V_{OLC}	Output Voltage Low	V_{IN} = V_{IH} Min or V_{IL} Max	0°C 25°C 75°C		−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C 25°C 75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C 25°C 75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	V_{IN} = V_{IH} Max	0°C to 75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	V_{IN} = V_{IL} Min	0°C to 75°C	0.5 −50	170	μA
I_{EE}	Power Supply Current Pin 9 (Note 1)	All Inputs & Outputs Open	0°C to 75°C	−200		mA

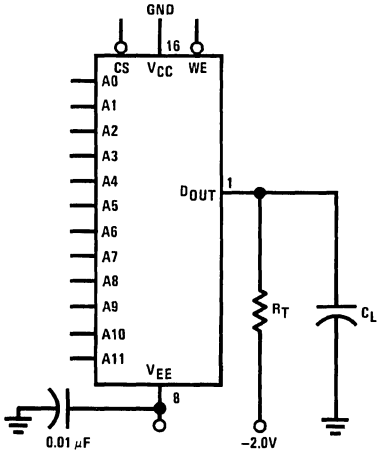
Note 1: Typical values at T_A = 0°C, I_{EE} = −160 mA; T_A = 25°C, I_{EE} = 155 mA, T_A = 75°C, I_{EE} = 140 mA, V_{EE} = −5.2V, output load = 50Ω and 30 pF to −2.0V.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, R_T = 50Ω to −2.0V, C_L = 30 pF, T_A = 0°C to +75°C, airflow exceeding 500 LFM

Test Circuit and Input Waveform

Loading Conditions



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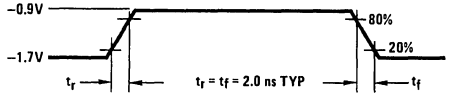
Input Levels



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All timing measurements referenced from 50% of input levels to 50% of input/output levels

C_L = 30 pF including jig and stray capacitance

R_T = 50Ω

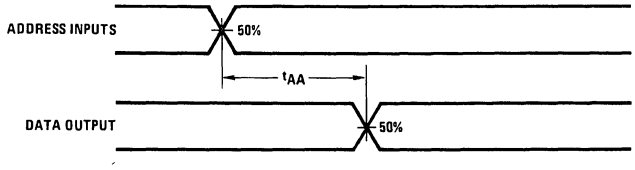
Read Cycle

Symbol	Parameter	Conditions	DM10470		DM10470A		Units
			Min	Max	Min	Max	
t_{AA}	Address Access Time	Measured at 50% of Input to 50% of Output (Note 2)		25		15	ns
t_{ACS}	Chip Select Access Time			10		8	ns
t_{RCS}	Chip Select Recovery Time			10		8	ns

Note 2: The maximum address access time is guaranteed to be the worst-case bit in the memory using a pseudorandom testing pattern.

Read Cycle Timing Diagrams

Address Access Time



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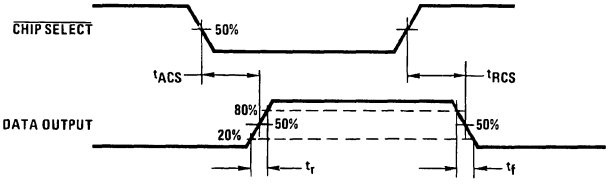
Chip Select Access Time



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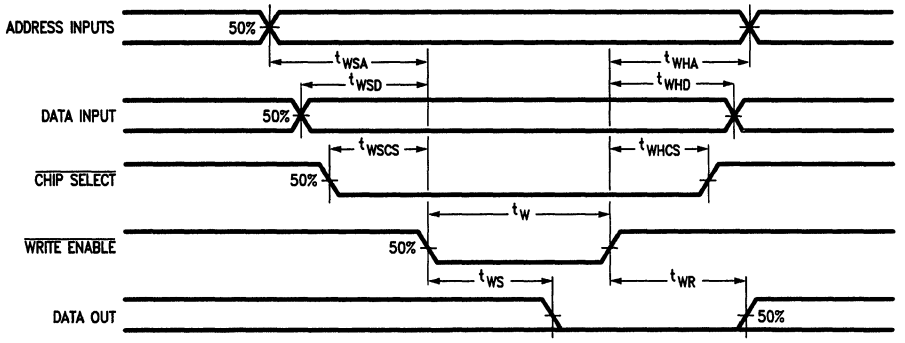
Write Cycle

Symbol	Parameter	DM10470		DM10470A		Units
		Min	Max	Min	Max	
t_W	Write Pulse Width (to Guarantee Writing)	15		10		ns
t_{WSD}	Data Set-Up Time Prior To Write	2		2		ns
t_{WHD}	Data Hold Time After Write	2		2		ns
t_{WSA}	Address Set-Up Time Prior to Write	3		3		ns
t_{WHA}	Address Hold Time After Write	2		2		ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write	2		2		ns
t_{WHCS}	Chip Select Hold Time After Write	2		2		ns
t_{WS}	Write Disable Time		8		8	ns
t_{WR}	Write Recovery Time		8		8	ns

Write Cycle Timing Diagram

Write Mode



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Rise Time and Fall Time

Symbol	Parameter	Conditions	DM10470		DM10470A		Units
			Min	Max	Min	Max	
t_r	Output Rise Time	Measured Between 20% and 80% Points	1	3.5	1	3.5	ns
t_f	Output Fall Time		1	3.5	1	3.5	ns

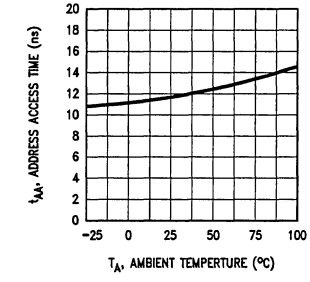
Capacitance

Symbol	Parameter	Conditions	DM10470		DM10470A		Units
			Min	Max	Min	Max	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		5		5	pF
C_{OUT}	Output Pin Capacitance			8		8	pF

Typical Performance Characteristics

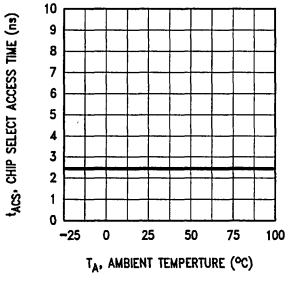
Address Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



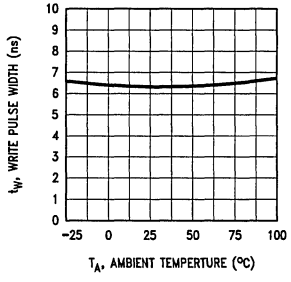
Chip Select Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Write Pulse Width vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



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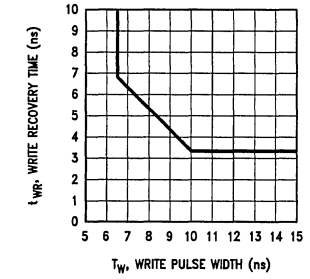
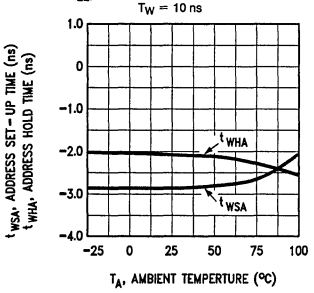
Write Recovery Time vs Write Pulse Width

25°C, NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



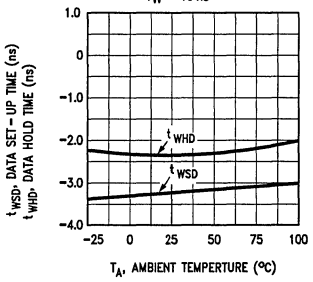
Address Set-Up and Hold Times vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



Data Set-Up and Hold Times vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



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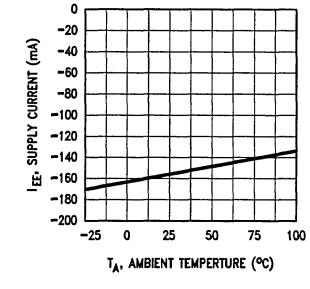
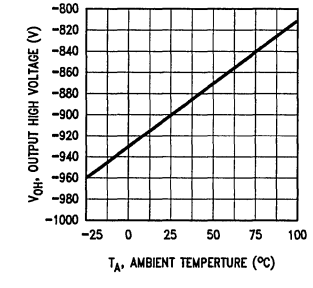
Supply Current (I_{EE}) vs Ambient Temperature

NOMINAL V_{EE}, INPUTS OPEN AND SPECIFIED AIRFLOW



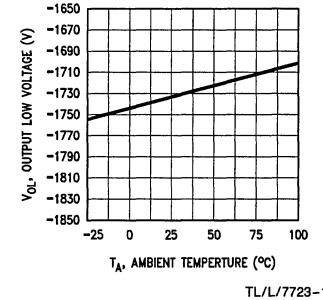
Output High Voltage (V_{OH}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Output Low Voltage (V_{OL}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



TL/L/7723–12

National Semiconductor Corporation

March 1987

DM10474A/DM10474A-10/DM10474A-8 4096-Bit (1024 x 4) ECL RAM

General Description

The DM10474A/DM10474A-10/DM10474A-8 is a fully decoded 4096-bit, 10KH compatible, ECL read/write random access memory designed for high-speed scratch pad and buffer storage applications. This device is organized as 1024 words by 4 bits and has separate Data In and Data Out pins. On-chip voltage compensation is provided for improved noise margin. The active-low Chip Select and unterminated emitter-follower outputs allow for easy expansion.

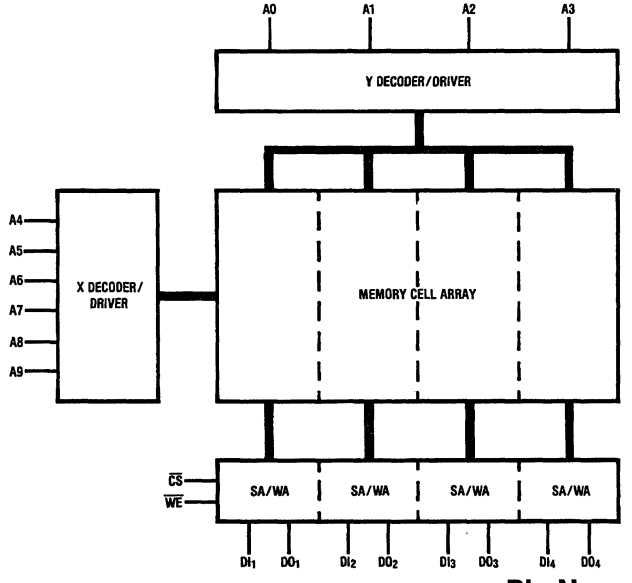
Features

- Three speed selected offerings for maximum cost-performance:

DM10474A	15 ns/−220 mA max
DM10474A-10	10 ns/−240 mA max
DM10474A-8	8 ns/−240 mA max

- 1024 words x 4 bit organization
- 10K and 10 KH logic compatible
- On-chip voltage compensation for improved noise margin
- Oxide isolation process
- Unterminated emitter-follower outputs for easy memory expansion
- Available in DIP and Flat Package
- Pin compatible with HM10474, MBM10474 and F10474

Block Diagram



TL/L/9229–1

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Pin Names

$\overline{CS}$	Chip Select Input
A0–A9	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

Functional Description

Addressing the DM10474A/DM10474A-10/DM10474A-8 is achieved by means of the ten address lines (A0–A9). Each of the 2^{10} possible combinations of address inputs corresponds to a unique word location in memory. The memory array can be expanded by wire-ORing the unterminated emitter-follower outputs of two or more devices and using the active-low Chip Select ($\overline{CS}$) inputs as address lines.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. A 50Ω resistor to −2V (or an equivalent network) is required to provide a logic low at the output when the device is turned off. This termination is required for both single device and wire-ORed operation. The $\overline{CS}$ input is internally pulled low so that in cases where no memory expansion is needed, no external connections are required.

The read and write operations are controlled by the state of the active-low Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held low, the data at the Data Inputs (DI1–DI4) is written into the addressed location. $\overline{WE}$ low also disables the output. The termination will then pull the output low. To read, $\overline{WE}$ is held high, while $\overline{CS}$ is held low. The rising edge of $\overline{WE}$ causes data at the addressed location to be transferred to the Data Outputs (DO1–DO4). The Data presented at Data Outputs is non-inverted.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−5.46	−4.94	V
Ambient Temperature (T_A)	0	+75	°C

DC Electrical Characteristics V_{EE} = −5.2V, R_T = 50Ω to −2.0V, T_A = 0°C to +75°C

Symbol	Parameter	Conditions	T_A	Min	Max	Units
V_{OH}	Output Voltage High	$V_{IN} = V_{IH}$ Max or V_{IL} Min	0°C 25°C 75°C	−1000 −960 −900	−840 −810 −720	mV
V_{OL}	Output Voltage Low	$V_{IN} = V_{IH}$ Max or V_{IL} Min	0°C 25°C 75°C	−1870 −1850 −1830	−1665 −1650 −1625	mV
V_{OHC}	Output Voltage High	$V_{IN} = V_{IH}$ Min or V_{IL} Max	0°C 25°C 75°C	−1020 −980 −920		mV
V_{OLC}	Output Voltage Low	$V_{IN} = V_{IH}$ Min or V_{IL} Max	0°C 25°C 75°C		−1645 −1630 −1605	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	0°C 25°C 75°C	−1145 −1105 −1045	−840 −810 −720	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	0°C 25°C 75°C	−1870 −1850 −1830	−1490 −1475 −1450	mV
I_{IH}	Input Current High	$V_{IN} = V_{IH}$ Max	0°C to 75°C		220	μA
I_{IL}	Input Current Low, $\overline{CS}$ All Others	$V_{IN} = V_{IL}$ Min	0°C to 75°C	0.5 −50	170	μA
I_{EE}	Power Supply Current Pin 9 (Note 1)	All Inputs & Outputs Open	0°C to 75°C	(10474-8) −240 (10474-10) −240 (10474-15) −220		mA

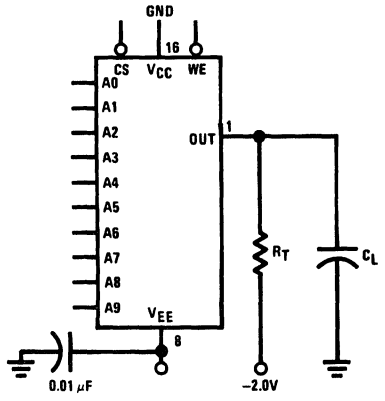
Note 1: Typical values at T_A = 0°C, I_{EE} = −200 mA; T_A = 25°C, I_{EE} = −190 mA, T_A = 75°C, I_{EE} = −175 mA, V_{EE} = −5.2V, output load = 50Ω and 30 pF to −2.0V.

AC Electrical Characteristics

V_{EE} = −5.2V ±5%, R_T = 50Ω to −2.0V, C_L = 30 pF, T_A = 0°C to +75°C

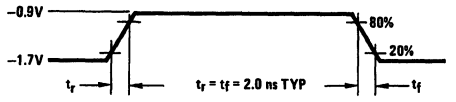
Test Circuit and Input Waveform

Loading Conditions



TL/L/9229–2

Input Levels



TL/L/9229–3

All timing measurements referenced from 50% of input levels to 50% of input/output levels

C_L = 30 pF including jig and stray capacitance

R_T = 50Ω

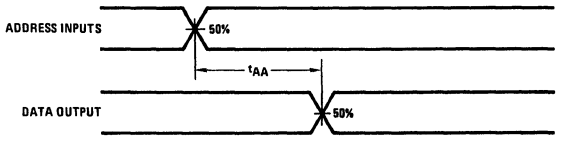
Read Cycle

Symbol	Parameter	Conditions	DM10474A		DM10474A-10		DM10474A-8		Units
			Min	Max	Min	Max	Min	Max	
t_{AA}	Address Access Time	Measured at 50% of Input to 50% of Output (Note 2)		15		10		8	ns
t_{ACS}	Chip Select Access Time			8		6		5	ns
t_{RCS}	Chip Select Recovery Time			8		6		5	ns

Note 2: The maximum address access time is guaranteed to be the worst-case bit in the memory using a pseudorandom testing pattern.

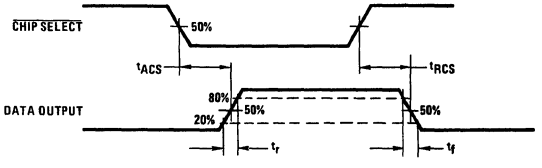
Read Cycle Timing Diagrams

Address Access Time



TL/L/9229–4

Chip Select Access Time



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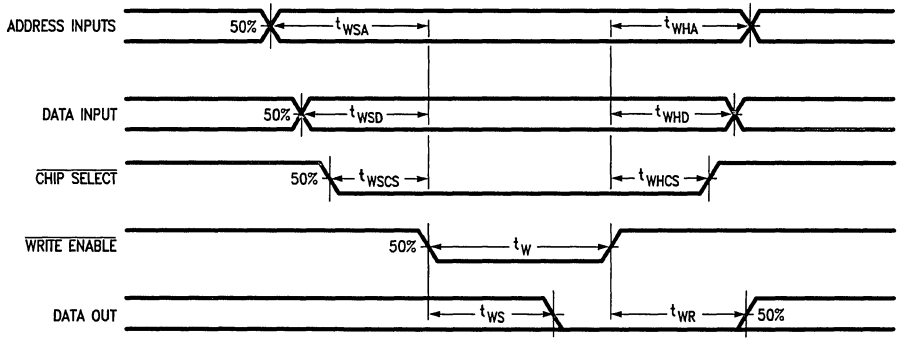
Write Cycle

Symbol	Parameter	DM10474A		DM10474A-10		DM10474A-8		Units
		Min	Max	Min	Max	Min	Max	
t_W	Write Pulse Width	15	—	10	—	6	—	ns
t_{WSD}	Data Set-Up Time Prior To Write	2	—	2	—	1	—	ns
t_{WHD}	Data Hold Time After Write	2	—	2	—	1	—	ns
t_{WSA}	Address Set-Up Time	3	—	3	—	1	—	ns
t_{WHA}	Address Hold Time	2	—	2	—	1	—	ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write	2	—	2	—	1	—	ns
t_{WHCS}	Chip Select Hold Time	2	—	2	—	1	—	ns
t_{WS}	Write Disable Time	—	8	—	8	—	5	ns
t_{WR}	Write Recovery Time	—	8	—	8	—	8	ns

Write Cycle Timing Diagram

Write Mode



TL/L/9229–06

Rise Time and Fall Time

Symbol	Parameter	Conditions	DM10474A/DM10474A-10/DM10474A-8		Units
			Min	Max	
t_r	Output Rise Time	Measured Between 20% and 80% Points	1	3.5	ns
t_f	Output Fall Time		1	3.5	ns

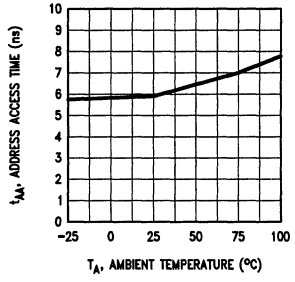
Capacitance

Symbol	Parameter	Conditions	DM10474A/DM10474A-10/DM10474A-8		Units
			Min	Max	
C_{IN}	Input Pin Capacitance	Measure With a Pulse Technique		5	pF
C_{OUT}	Output Pin Capacitance			8	pF

Typical Performance Characteristics

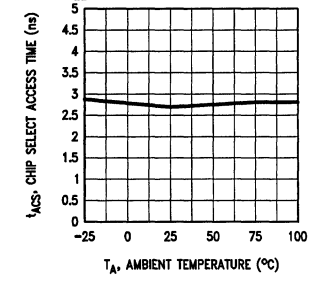
Address Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



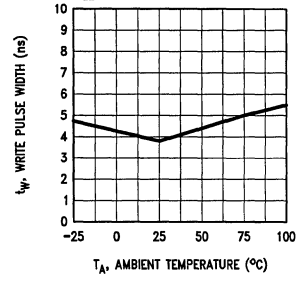
Chip Select Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Write Pulse Width vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



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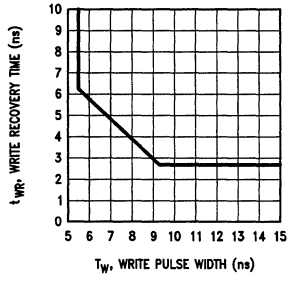
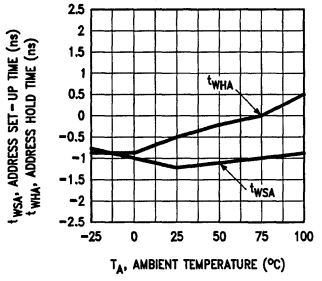
Write Recovery Time vs Write Pulse Width

25°C, NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



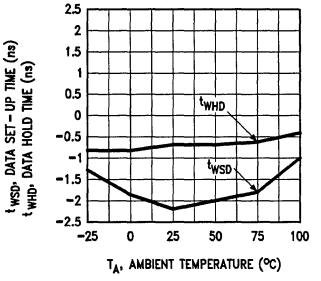
Address Set-Up and Hold Times vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



Data Set-Up and Hold Times vs Ambient Temperature

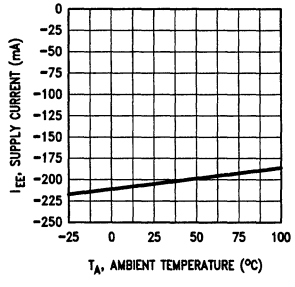
NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



TL/L/9229–8

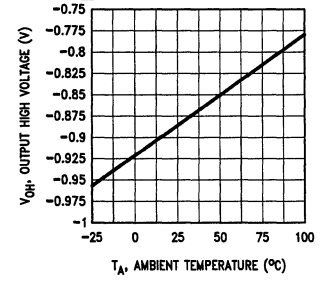
Supply Current (I_{EE}) vs Ambient Temperature

NOMINAL V_{EE}, INPUTS OPEN AND SPECIFIED AIRFLOW



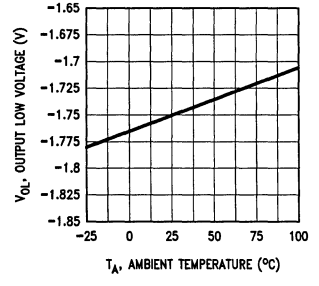
Output High Voltage (V_{OH}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Output Low Voltage (V_{OL}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



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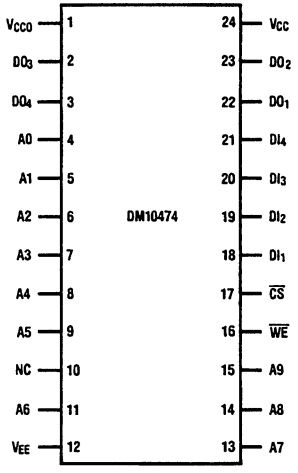
Connection Diagrams

Dual-In-Line Package

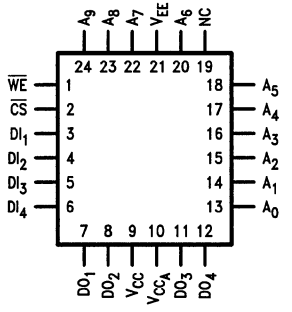


TOP VIEW

TL/L/9229–10

Order Number DM10474AJ, DM10474A-10J or DM10474-8J
See NS Package Number J24E

Flat Pack



TL/L/9229–11

Order Number DM10474AW, DM10474A-10W or DM10474A-8W
See NS Package Number W24B

4

National Semiconductor Corporation

March 1987

DM100422/DM100422A 1024-Bit (256 x 4) ECL RAM

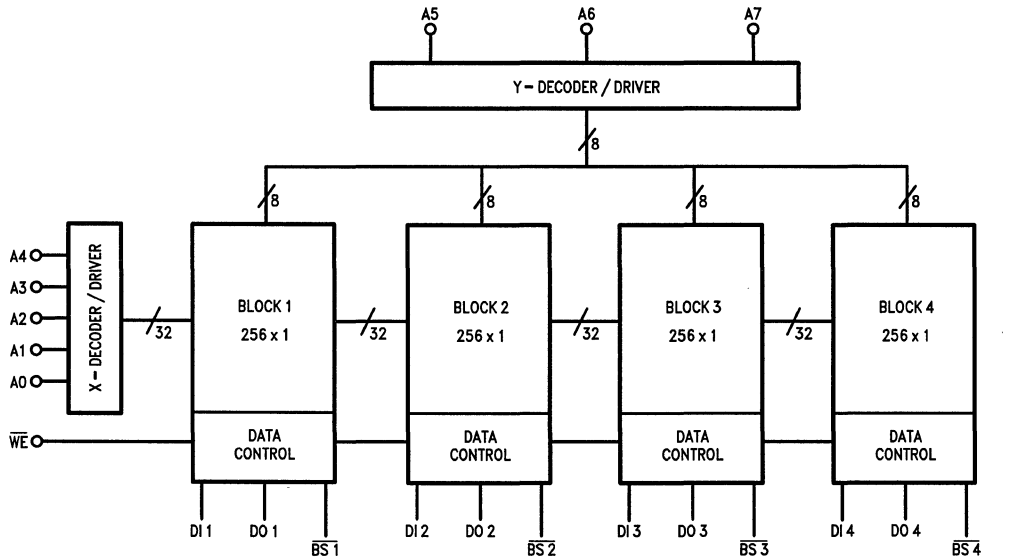
General Description

The DM100422/DM100422A is a 1024-bit ECL random access memory organized as 4 blocks of 256 bits. Since each block has its own Select input, the memory can be configured for a maximum of 1024 by 1 bit through Wire-ORing of the outputs. The high-speed access time allows its use in scratch pad, buffer, and control storage applications. The device is voltage and temperature compensated and is compatible with all 100k ECL logic. Separate Data In and Data Out pins allow the set-up of data for a write cycle while performing a read.

Features

- 4 separate Block Select inputs for configurations from 256 x 4 to 1024 x 1
- Maximum address access time—DM100422 12 ns
  —DM100422A 10 ns
- Maximum Block Select access time—DM100422 5 ns
  —DM100422A 5 ns
- 100k logic compatible with on-chip voltage and temperature compensation
- Oxide isolation process
- Unterminated emitter-follower output for easy memory expansion
- Compatible with HM100422, MBM100422 and F100422

Block Diagram



TL/L/6749–1

Truth Table (Positive Logic)

Input			Output	Mode
$\overline{BS}$	$\overline{WE}$	DI		
H	X	X	L	Disable
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Data	Read

H = High Voltage Level L = Low Voltage Level X = Don't Care

Pin Names

$\overline{BS1}$–$\overline{BS4}$	Block Selects
A0–A7	Address Inputs
$\overline{WE}$	Write Enable
DI1–DI4	Data Inputs
DO1–DO4	Data Outputs

Functional Description

Addressing the DM100422/DM100422A is accomplished by means of the eight address lines (A0–A7). Each of the 256 possible combinations of address inputs corresponds to a unique four-bit word in the memory array. The availability of four active-low Block Select inputs ($\overline{BS1}$–$\overline{BS4}$) and the unterminated emitter-follower outputs allow the user to reconfigure the part into a 512 x 2 or 1024 x 1 architecture by wire-ORing the outputs and using the BS inputs as address lines.

The device is selected with $\overline{BS}$ low and deselected with $\overline{BS}$ high. A 50Ω resistor to −2V (or an equivalent network) is required to provide a logic low at the output when the device is turned off. This termination is required for both single device and wire-ORed operation. The $\overline{BS}$ inputs are internally pulled low so that in cases where no memory expansion is needed, no external connections are required.

The read and write operations are controlled by the active-low Write Enable input ($\overline{WE}$). With $\overline{WE}$ and $\overline{BS}$ held low, the data at the Data Inputs (DI1–DI4) is written into addressed location. $\overline{WE}$ low also causes the output to be disabled; the termination will then pull the output low. To read, $\overline{WE}$ is held high, while $\overline{BS}$ is held low. The rising edge of $\overline{WE}$ causes the data present at the selected address to be transferred to the Data Outputs (DO1–DO4). The data presented at the Data Outputs is non-inverted.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Temperature Under Bias (Ambient)	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
V_{EE} Relative to V_{CC}	−7.0V to +0.5V
Any Input Relative to V_{CC}	V_{EE} to +0.5V
Output Current (Output High)	−30 mA to +0.1 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−4.73	−4.27	V
Ambient Temperature (T_A)	0	+85	°C

DC Electrical Characteristics

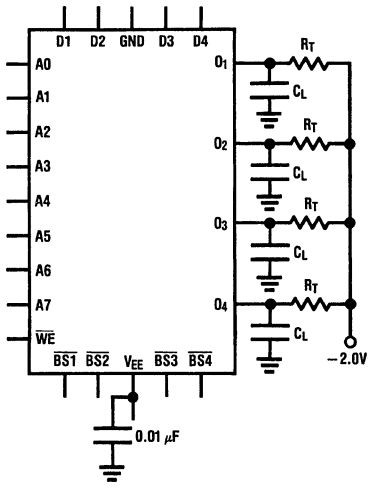
V_{EE} = −4.5V, R_T = 50Ω to −2.0V, T_A = 0°C to +85°C, airflow exceeding 500 LFM

Symbol	Parameter	Conditions	Min	Max	Units
V_{OH}	Output Voltage High	V_{IN} = V_{IH} Max or V_{IL} Min	−1025	−880	mV
V_{OL}	Output Voltage Low	V_{IN} = V_{IH} Max or V_{IL} Min	−1810	−1620	mV
V_{OHC}	Output Voltage High	V_{IN} = V_{IH} Min or V_{IL} Max	−1035	—	mV
V_{OLC}	Output Voltage Low	V_{IN} = V_{IH} Min or V_{IL} Max	—	−1610	mV
V_{IH}	Input Voltage High	Guaranteed Input Voltage High for All Inputs	−1165	−880	mV
V_{IL}	Input Voltage Low	Guaranteed Input Voltage Low for All Inputs	−1810	−1475	mV
I_{IH}	Input Current High	V_{IN} = V_{IH} Max	—	220	μA
I_{IL}	Input Current Low, $\overline{BS}$ All Others	V_{IN} = V_{IL} Min	0.5 −50	170	μA
I_{EE}	Power Supply Current	All Inputs and Outputs Open	−200	—	mA

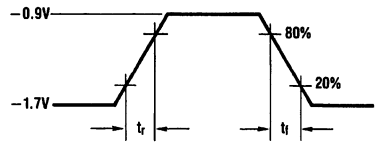
AC Electrical Characteristics

$V_{CC} = V_{CCA} = 0V$, $V_{EE} = -4.5V \pm 5\%$, $R_T = 50\Omega$ to $-2.0V$, $C_L = 30$ pF, $T_A = 0°C$ to $+85°C$, air flow exceeding 500 LFM

Test Circuit and Input Waveform



TL/L/6749–2



TL/L/6749–3

$t_r = t_f = 2.0$ ns $\pm 10\%$

$R_T = 50\Omega$

$C_L = 30$ pF

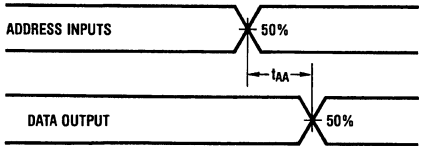
All timing measurements are referenced from 50% of input levels to 50% of input/output levels.

Read Cycle

Symbol	Parameter	DM100422		DM100422A		Units
		Min	Max	Min	Max	
t_{AA}	Address Access Time	—	12	—	10	ns
t_{ABS}	Block Select Access Time	—	5	—	5	ns
t_{RBS}	Block Select Recovery Time	—	5	—	5	ns

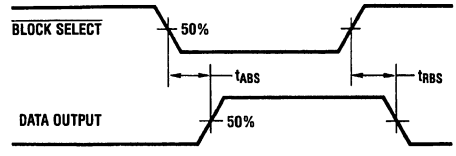
Read Cycle Timing Diagrams

Address Access Time



TL/L/6749–4

Block Select Access

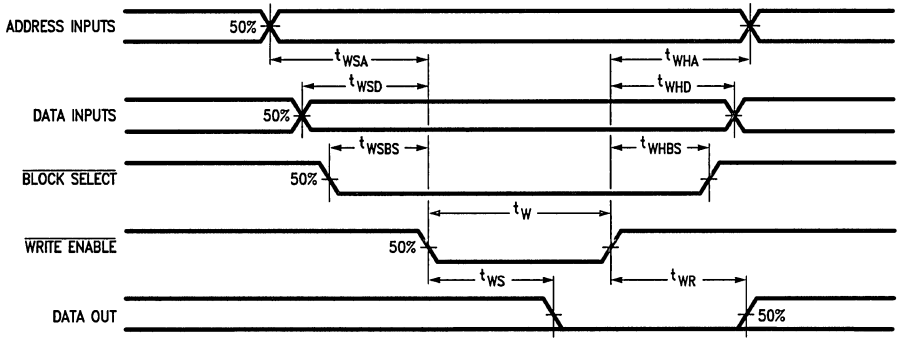


TL/L/6749–5

Write Cycle

Symbol	Parameter	DM100422		DM100422A		Units
		Min	Max	Min	Max	
t_W	Write Pulse Width	7	—	6	—	ns
t_{WSD}	Data Set-Up Time	2.0	—	2.0	—	ns
t_{WHD}	Data Hold Time	2.0	—	2.0	—	ns
t_{WSA}	Address Set-Up Time	3.0	—	2.0	—	ns
t_{WHA}	Address Hold Time	2.0	—	2.0	—	ns
t_{WSBS}	Block Select Set-Up Time	2.0	—	2.0	—	ns
t_{WHBS}	Block Select Hold Time	2.0	—	2.0	—	ns
t_{WS}	Write Disable Time		5	—	5	ns
t_{WR}	Write Recovery Time		7	—	7	ns

Write Cycle Timing Diagram



TL/L/6749–6

Rise Time and Fall Time

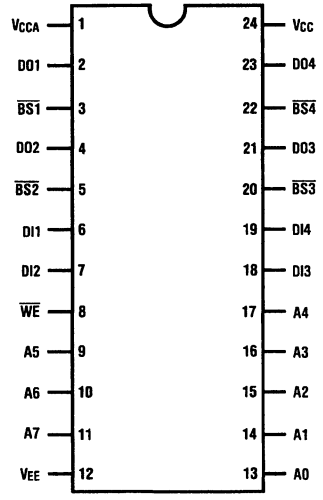
Symbol	Parameter	DM100422		DM100422A		Units
		Min	Max	Min	Max	
t_r	Output Rise Time	1	3.5	1	3.5	ns
t_f	Output Fall Time	1	3.5	1	3.5	ns

Capacitance

Symbol	Parameter	DM100422		DM100422A		Units
		Min	Max	Min	Max	
C_{IN}	Input Capacitance	—	5	—	5	pF
C_{OUT}	Output Capacitance	—	8	—	8	pF

Connection Diagram

Dual-In-Line Package

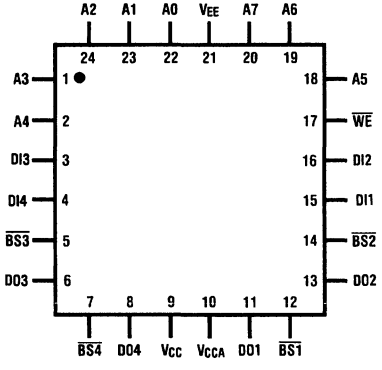


TL/L/6749–7

Top View

Order Number DM100422J or DM100422AJ
See NS Package Number J24E

Quad Cerpack



TL/L/6749–8

Order Number DM10422W, DM10422AW
or DM100422AJ
See NS Package Number W24B

National Semiconductor Corporation

December 1986

DM100470/DM100470A 4096-Bit (4096 x 1) ECL RAMs

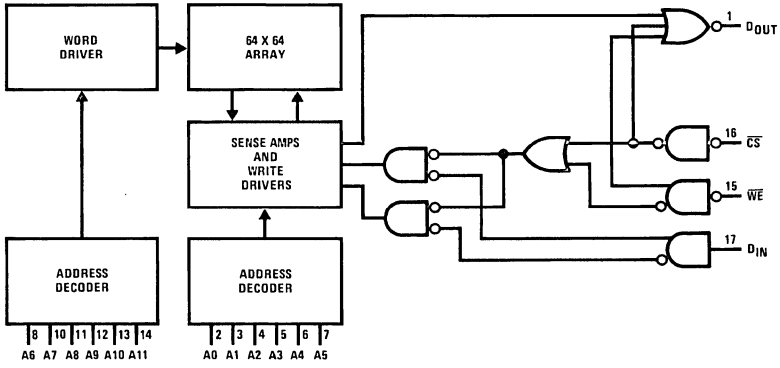
General Description

The DM100470/DM100470A is a fully decoded 4096-bit, 100K compatible, ECL read/write random access memory designed for high-speed scratch pad and buffer storage applications. This device is organized as 4096 words by 1 bit and has separate Data In and Data Out pins. On-chip voltage and temperature compensation is provided for improved noise margin. The active-low Chip Select $\overline{CS}$ and unterminated emitter-follower outputs allow for easy expansion.

Features

- Two speed-selected offerings for maximum cost-performance:
  - DM100470 — 25 ns/200 mA max
  - DM100470A — 15 ns/200 mA max
- 4096 x 1 bit organization
- 100K logic compatible
- On-chip voltage and temperature compensation for improved noise margin
- Oxide-isolation process
- Unterminated emitter-follower outputs for easy memory expansion
- Pin-compatible with HM100470 and F100470

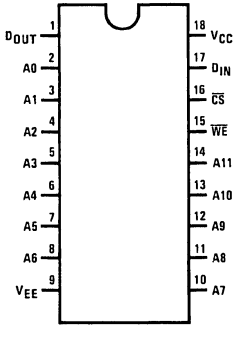
Logic Diagram



TL/L/8639–1

Connection Diagram

Dual-In-Line Package



TL/L/8639–2

Top View

Order Number DM100470J or DM100470AJ
See NS Package Number J18A

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

H = High Voltage Level L = Low Voltage Level X = Don't Care

Pin Names

$\overline{CS}$	Chip Select Input
A0–A11	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

4

Functional Description

Addressing the DM100470/DM100470A is achieved by means of the twelve address lines (A0–A11). Each of the 2^{12} possible combinations of address inputs corresponds to a unique bit location in memory. The memory array can be expanded by wire-ORing the unterminated emitter-follower outputs of two or more devices and using the active-low Chip Select ($\overline{CS}$) inputs as address lines.

The device is selected with $\overline{CS}$ low and deselected with $\overline{CS}$ high. A 50Ω resistor to −2V (or an equivalent network) is required to provide a logic low at the output when the device is turned off. This termination is required for both single device and wire-ORed operation. The $\overline{CS}$ input is internally pulled low so that in cases where no memory expansion is needed, no external connections is required.

The read and write operations are controlled by the state of the active-low Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held low, the data at the Data Input (D_{IN}) is written into the addressed location. $\overline{WE}$ low also disables the output. The termination will then pull the output low. To read, $\overline{WE}$ is held high while $\overline{CS}$ is held low. The rising edge of $\overline{WE}$ causes data at the addressed location to be transferred to the Data Output (D_{OUT}). The data presented at D_{OUT} is non-inverted.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage, V_{EE} to V_{CC}	+0.5V to −7.0V
Input Voltage, V_{IN}	+0.5V to V_{EE}
Output Current	−30 mA
Storage Temperature, T_{stg}	−65°C to +150°C
Storage Temperature Under Bias, T_{stg} (Bias)	−55°C to +125°C
Lead Temperature (Soldering, 10 sec.)	300°C

ESD Rating to be determined.

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{EE})	−4.73	−4.27	V
Ambient Temperature (T_A)	0	+85	°C

DC Electrical Characteristics

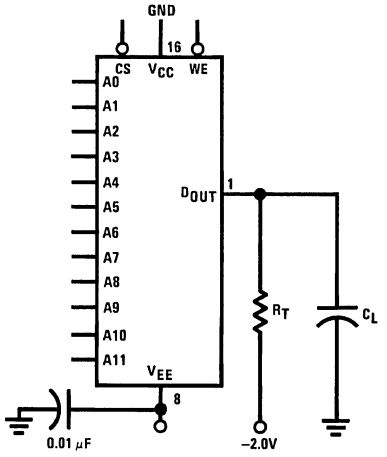
V_{CC} = 0V, V_{EE} = −4.5V, R_T = 50Ω to −2.0V, T_A = 0°C to +85°C, air flow exceeding 500 LFM

Symbol	Parameter	Min	Max	Units
V_{OH}	Output High Voltage (V_{IN} = V_{IHmax} or V_{ILmin})	−1025	−880	mV
V_{OL}	Output Low Voltage (V_{IN} = V_{IHmax} or V_{ILmin})	−1810	−1620	mV
V_{OHC}	Output High Voltage (V_{IN} = V_{IHmin} or V_{ILmax})	−1035	—	mV
V_{OLC}	Output Low Voltage (V_{IN} = V_{IHmin} or V_{ILmax})	—	−1610	mV
V_{IH}	Input High Voltage (Guaranteed Input Voltage High for All Inputs)	−1165	−880	mV
V_{IL}	Input High Voltage (Guaranteed Input Voltage Low for All Inputs)	−1810	−1475	mV
I_{IH}	Input High Current (V_{IN} = V_{IHmax})	—	220	μA
I_{IL}	Input Low Current (V_{IN} = V_{ILmin})	−50	—	μA
I_{IL}	$\overline{CS}$ Input Low Current (V_{IN} = V_{ILmin})	0.5	170	μA
I_{EE}	Power Supply Current (All Inputs and Outputs Open)	−200	—	mA

AC Electrical Characteristics

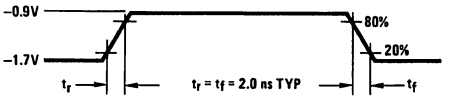
Test Circuit and Input Waveforms

Loading Conditions



TL/L/8639–8

Input Levels



TL/L/8639–9

All timing measurements referenced from 50% of input levels to 50% of input/output levels

C_L = 30 pF including jig and stray capacitance

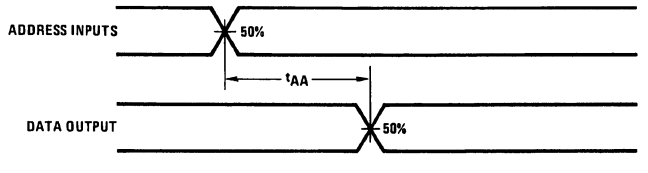
R_T = 50Ω

Read Cycle V_{EE} = −4.5V ±5%, R_T = 50Ω to −2.0V, C_L = 30 pF, T_A = 0°C to +85°C, airflow exceeding 500 LFM

Symbol	Parameter	Conditions	DM100470		DM100470A		Units
			Min	Max	Min	Max	
t_{ACS}	Chip Select Access		—	10	—	8	ns
t_{RCS}	Chip Select Recovery Time		—	10	—	8	ns
t_{AA}	Address Access Time		—	25	—	15	ns

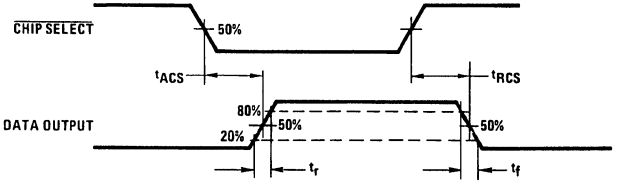
Read Cycle Timing Diagrams

Address Access Time



TL/L/8639–5

Chip Select Access Time

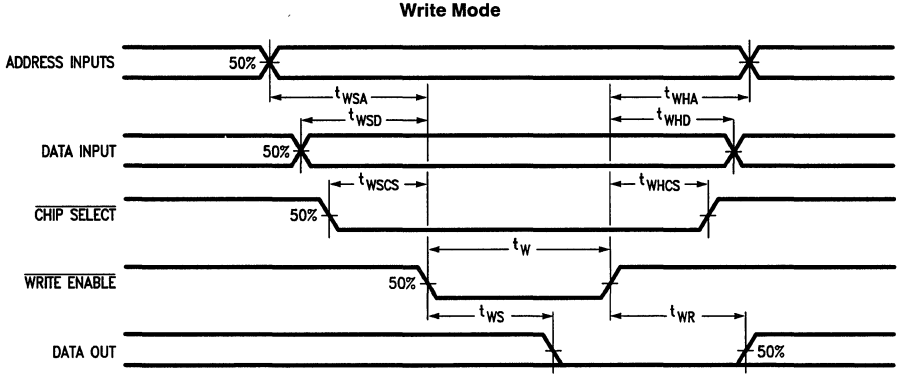


TL/L/8639–4

Write Cycle $V_{EE} = -4.5V \pm 5\%$, $R_T = 50\Omega$ to $-2.0V$, $C_L = 30$ pF, $T_A = 0°C$ to $+85°C$, airflow exceeding 500 LFM

Symbol	Parameter	DM100470		DM100470A		Units
		Min	Max	Min	Max	
t_W	Write Pulse Width	15	—	10	—	ns
t_{WSD}	Data Set-Up Time Prior to Write	2	—	2	—	ns
t_{WHD}	Data Hold Time After Write	2	—	2	—	ns
t_{WSA}	Address Set-Up Time Prior to Write	3	—	3	—	ns
t_{WHA}	Address Hold Time After Write	2	—	2	—	ns
t_{WSCS}	Chip Select Set-Up Time Prior to Write	2	—	2	—	ns
t_{WHCS}	Chip Select Hold Time After Write	2	—	2	—	ns
t_{WS}	Write Disable Time	—	8	—	8	ns
t_{WR}	Write Recovery Time	—	8	—	8	ns

Write Cycle Timing Diagram



TL/L/8639–7

Rise Time and Fall Time

Symbol	Parameter	Conditions	DM100470		DM100470A		Units
			Min	Max	Min	Max	
t_r	Output Rise Time	Measured Between 20% and 80% Points	1	3.5	1	3.5	ns
t_f	Output Fall Time		1	3.5	1	3.5	ns

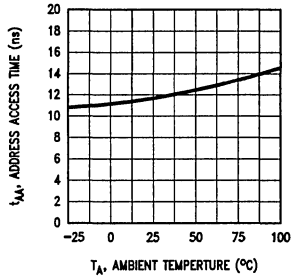
Capacitance

Symbol	Parameter	Conditions	DM100470		DM100470A		Units
			Min	Max	Min	Max	
C_{IN}	Input Pin Capacitance	Measure with a Pulse Technique	—	5	—	5	pF
C_{OUT}	Output Pin Capacitance		—	8	—	8	pF

Typical Performance Characteristics

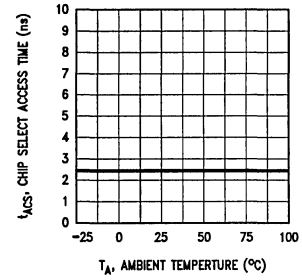
Address Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



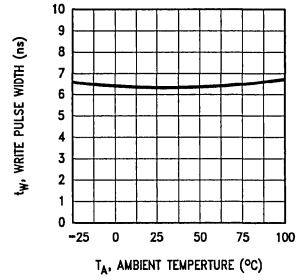
Chip Select Access Time vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Write Pulse Width vs Ambient Temperature

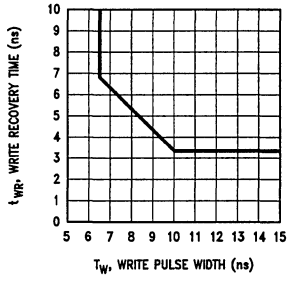
NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



TL/L/8639–10

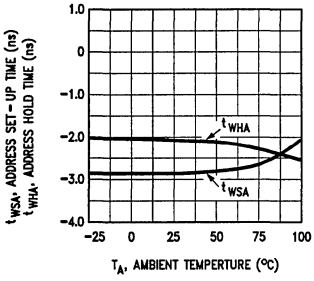
Write Recovery Time vs Write Pulse Width

25°C, NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



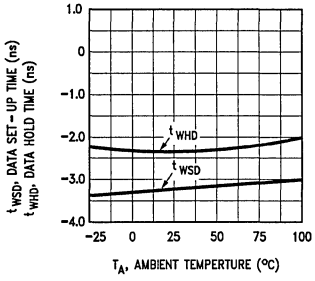
Address Set-Up and Hold Times vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



Data Set-Up and Hold Times vs Ambient Temperature

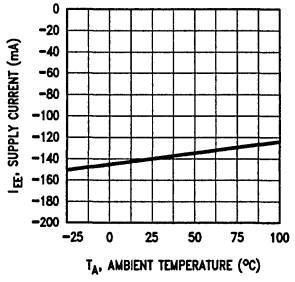
NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW
T_W = 10 ns



TL/L/8639–11

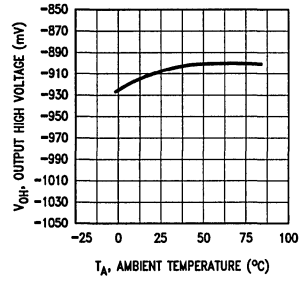
Supply Current (I_{EE}) vs Ambient Temperature

NOMINAL V_{EE}, INPUTS OPEN AND SPECIFIED AIRFLOW



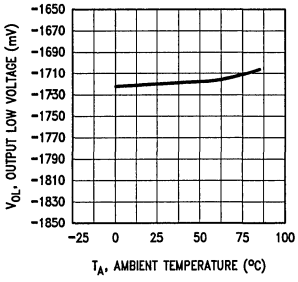
Output High Voltage (V_{OH}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



Output Low Voltage (V_{OL}) vs Ambient Temperature

NOMINAL V_{EE}, INPUT LEVELS AND SPECIFIED AIRFLOW



TL/L/8639–12

4

National Semiconductor Corporation

September 1985

DM100474/DM100474A (1024 x 4) 4096-Bit, 100k ECL RAM

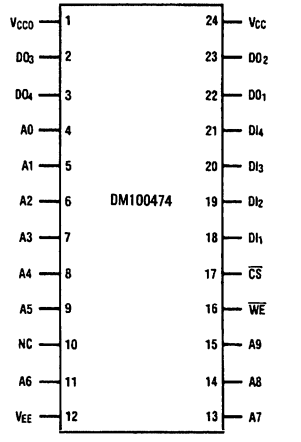
General Description

The DM100474 is a 4096-bit read/write random access memory, organized in the popular 1024 words by 4-bit configuration. It is designed for high-speed scratchpad, control and buffer storage applications. The device includes full on-chip address decoding, separate Data input and non-inverting Data output lines, as well as an active-low chip select line. The input and output levels are voltage compensated 100k ECL levels. The DM100474A has a maximum access time of 15 ns, and the DM100474 has a maximum access time of 25 ns.

Features

- 1024 words x 4-bit organization
- On chip voltage compensation for improved noise margin
- Fully compatible with industry standard 100k series ECL families
- Address access time: 25 ns max for standard part, 15 ns max for "A" part.
- Chip select access time: 10 ns max for standard part, 8 ns max for "A" part.
- Low power dissipation: −220 mA max for "A" part, −200 mA max for standard.
- Pin compatible with F100474 and MBM100474

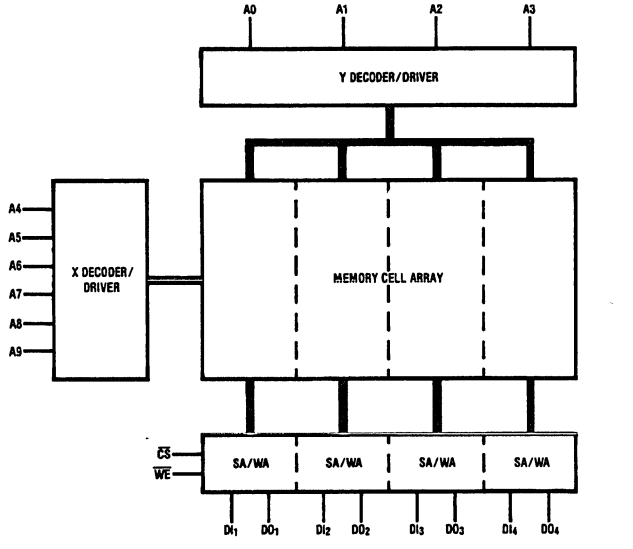
Connection and Block Diagrams



TL/L/6748–1

Top View

Order Number DM100474D or DM100474AD
See NS Package D24K



TL/L/6748–2

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Emitter	
H	X	X	L	Not Selected
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

H = high voltage level
L = low voltage level
X = don't care

Absolute Maximum Ratings

Supply Voltage, V_{EE} to V_{CC}	−7.0V to +0.5V	Storage Temperature, T_{STG}	−65°C to +150°C
Input Voltage, V_{IN}	V_{EE} to +0.5V	Storage Temperature Under Bias,	
Output Current	−30 mA to +0.1 mA	T_{STG} (Bias)	−55°C to +125°C

DC Electrical Characteristics

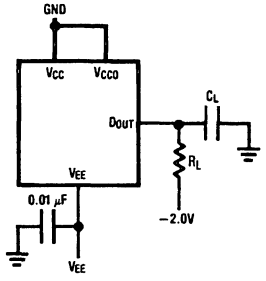
(V_{CC} = 0V, V_{EE} = − 4.5V, output load = 50Ω to −2.0V, T_A = 0°C to +85°C and airflow ≥ 500 LFM unless otherwise noted.)

Symbol	Parameter	Min	Typ	Max	Units
V_{OH}	Output High Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	−1025	−955	−880	mV
V_{OL}	Output Low Voltage (V_{IN} = $V_{IH\ max}$ or $V_{IL\ min}$)	−1810	−1715	−1620	mV
V_{OHC}	Output High Threshold Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)	−1035			mV
V_{OLC}	Output Low Threshold Voltage (V_{IN} = $V_{IH\ min}$ or $V_{IL\ max}$)			−1610	mV
V_{IH}	Input High Voltage (Guaranteed Input Voltage High for All Inputs)	−1165		−880	mV
V_{IL}	Input Low Voltage (Guaranteed Input Voltage Low for All Inputs)	−1810		−1475	mV
I_{IH}	Input High Current (V_{IN} = $V_{IH\ max}$)			220	μA
I_{IL}	Input Low Current (V_{IN} = $V_{IL\ min}$)	−50			μA
I_{IL}	$\overline{CS}$ Input Low Current (V_{IN} = $V_{IL\ min}$)	0.5		170	μA
I_{EE}	Power Supply Current (All Inputs and Outputs Open)	−200 −220*			mA

*For the DM100474A.

AC Test Circuit and Switching Time Waveform

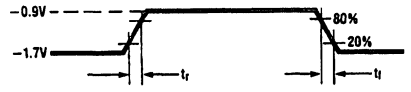
(Full guaranteed operating ranges, output load = 50Ω to −2.0V and 30 pF to GND and airflow > 500 LFM unless otherwise noted.)



TL/L/6748-3

Output Load: R_L = 50Ω
C_L = 30 pF
(including jig and stray capacitance)

Input Waveforms



TL/L/6748-4

t_r = t_f = 2.0 ns type

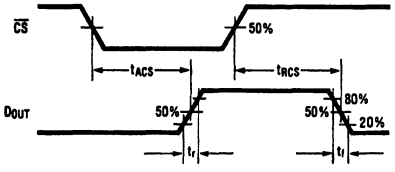
AC Electrical Characteristics

V_{EE} = −4.5V ±5%, output load = 50Ω to −2.0V, 30 pF to GND, T_A = 0°C to +85°C, air flow ≥ 500 LFM and 2 min warm up.

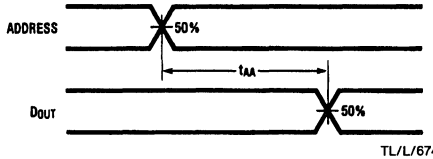
Read Cycle

Symbol	Parameter	DM100474		DM100474A		Units
		Typ	Max	Typ	Max	
t_{AA}	Address Access Time		25		15	ns
t_{ACS}	Chip Select Access Time		10		8	ns
t_{RCS}	Chip Select Recovery Time		10		8	ns

Read Cycle Timing Diagrams



TL/L/6748–5

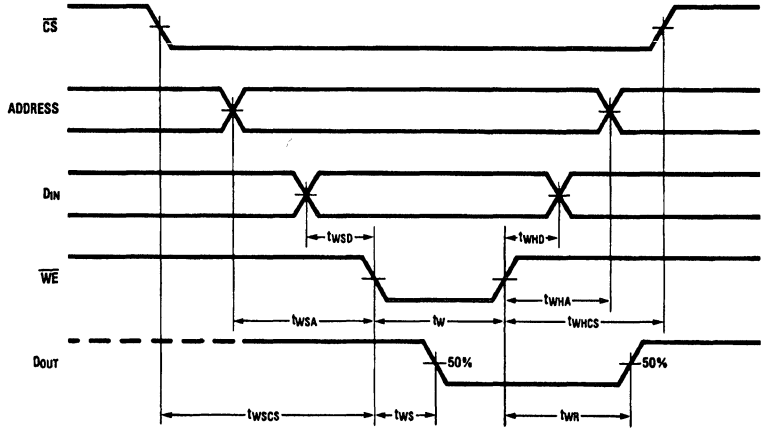


TL/L/6748–6

Write Cycle

Symbol	Parameter	DM100474			DM100474A			Units
		Min	Typ	Max	Min	Typ	Max	
t_W	Write Pulse Width	20			15			ns
t_{WS}	Write Disable Time			10			8	ns
t_{WR}	Write Recovery Time			10			8	ns
t_{WSA}	Address Set Up Time	2			2			ns
t_{WSCS}	Chip Select Set Up Time	2			2			ns
t_{WSD}	Data Set Up Time	2			2			ns
t_{WHA}	Address Hold Time	2			2			ns
t_{WHCS}	Chip Select Hold Time	2			2			ns
t_{WHD}	Data Hold Time	2			2			ns

Write Cycle Timing Diagrams



TL/L/6748–7

Note: All timing measurements referenced to 50% input levels.

Rise Time and Fall Time

Symbol	Parameter	DM100474/DM100474A			Units
		Min	Typ	Max	
t_r	Output Rise Time	—	2.5	—	ns
t_f	Output Fall Time	—	2.5	—	ns

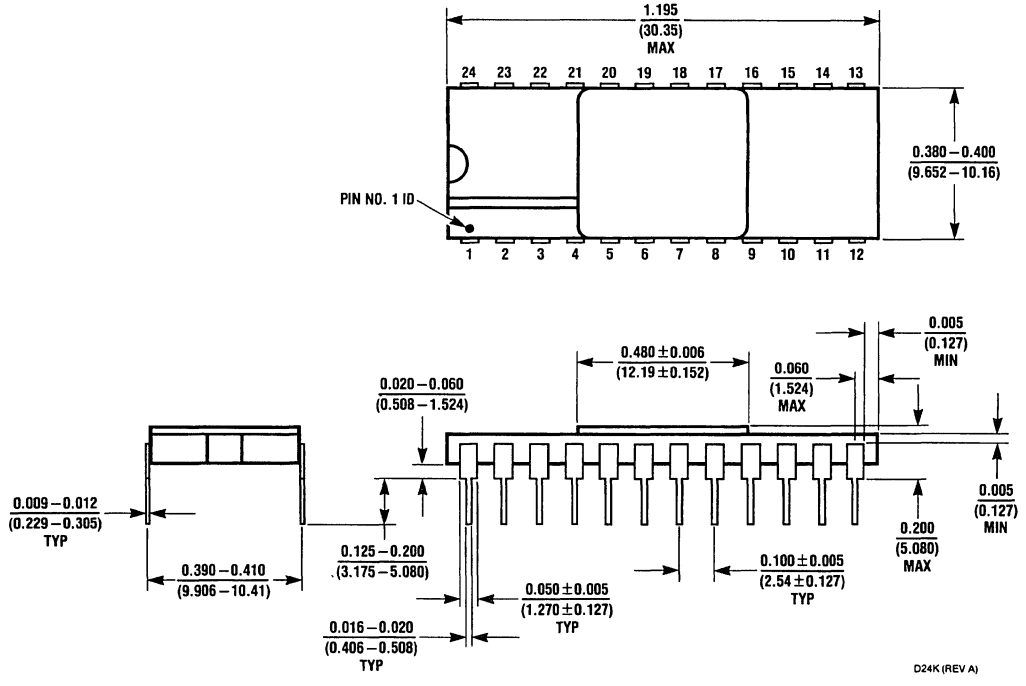
Section 5

Physical Dimensions

Section 5 Contents

National Semiconductor Corporation

All dimensions are in inches (millimeters)



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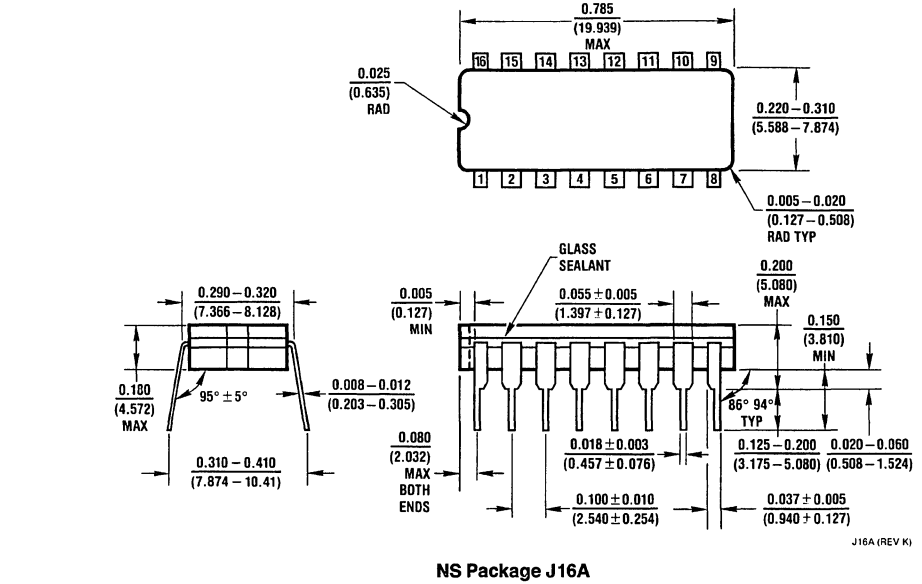

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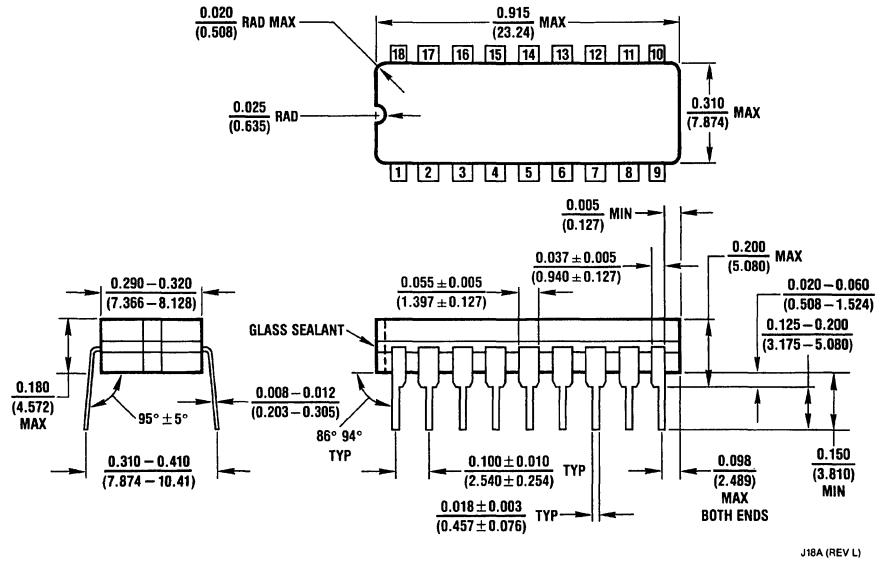

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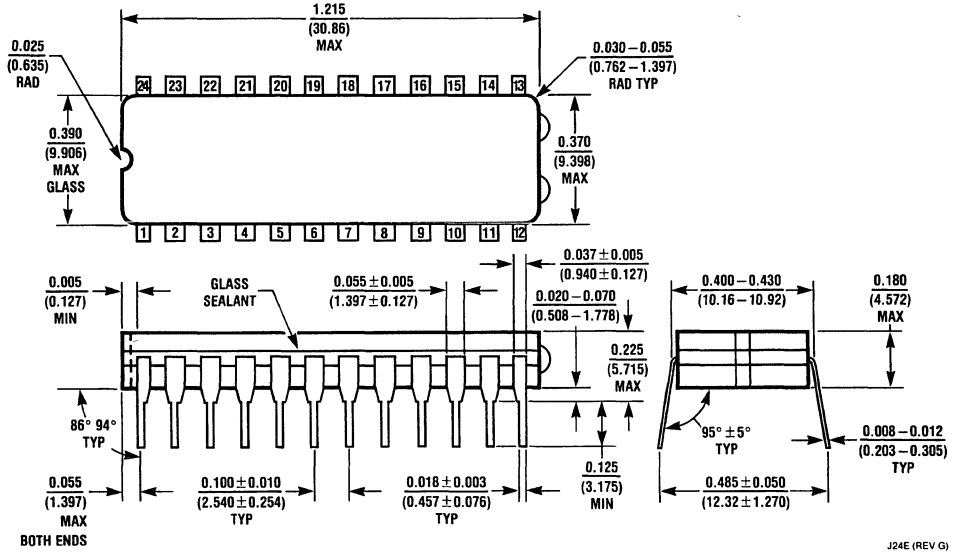

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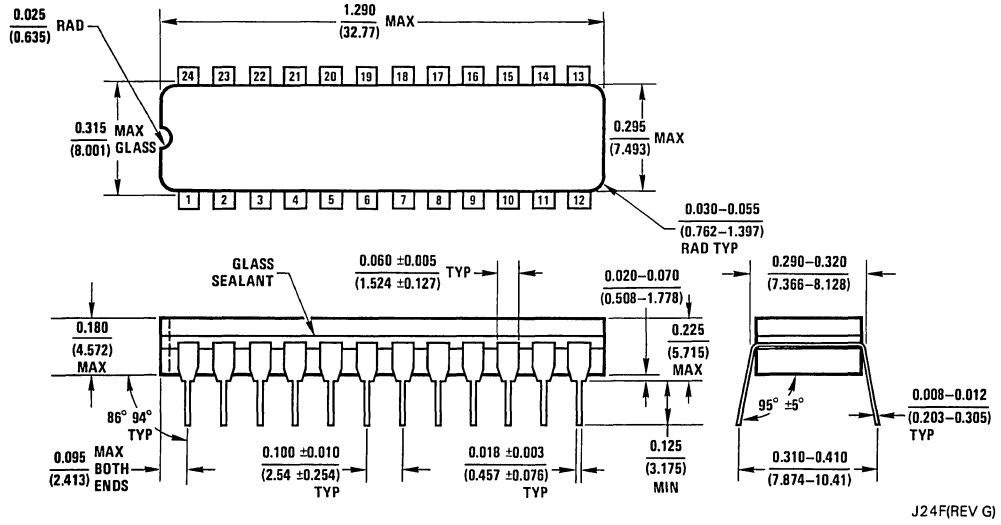

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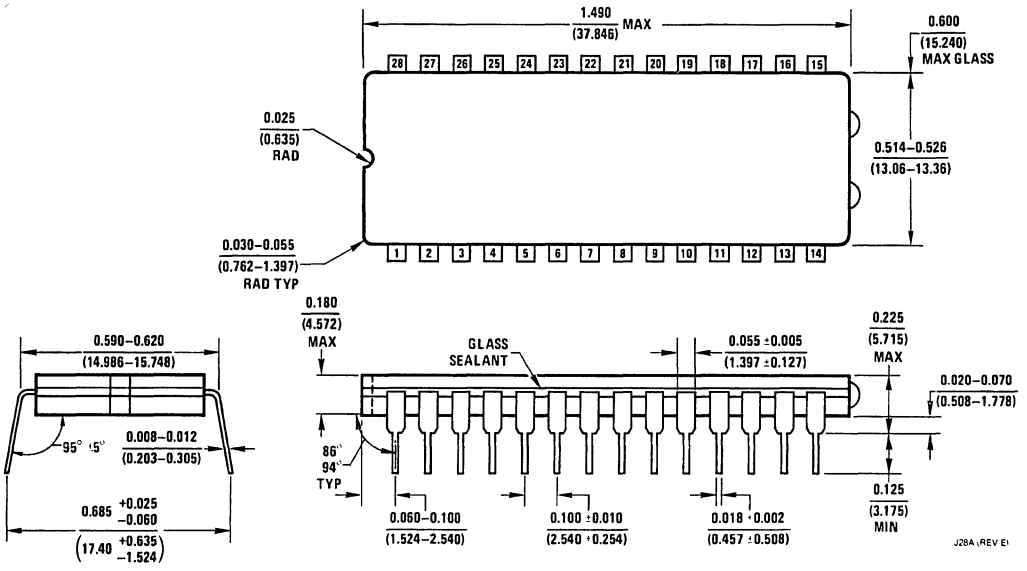

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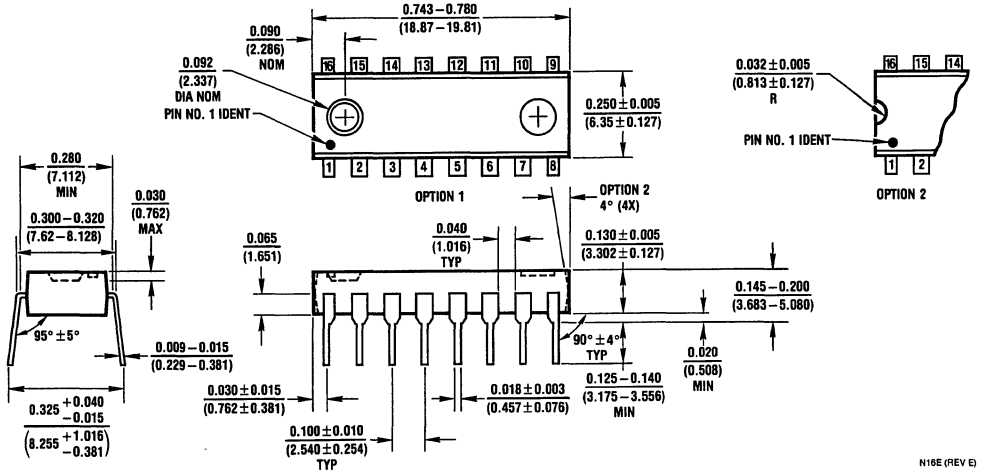

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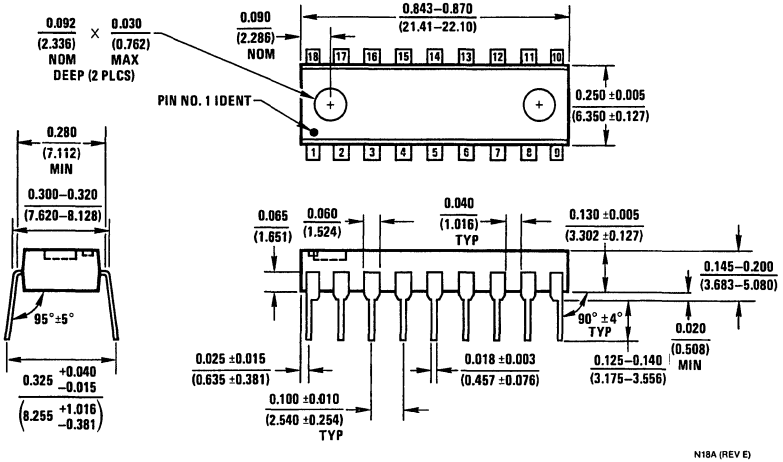

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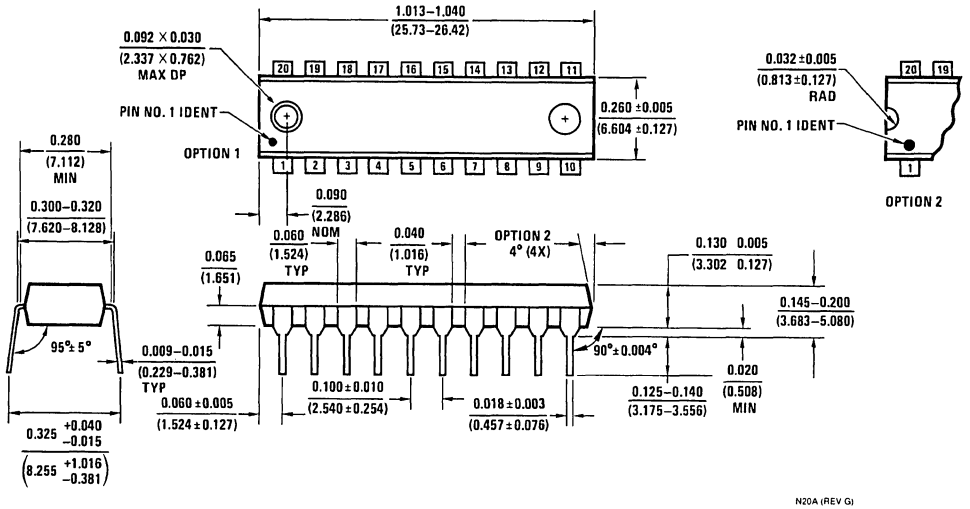

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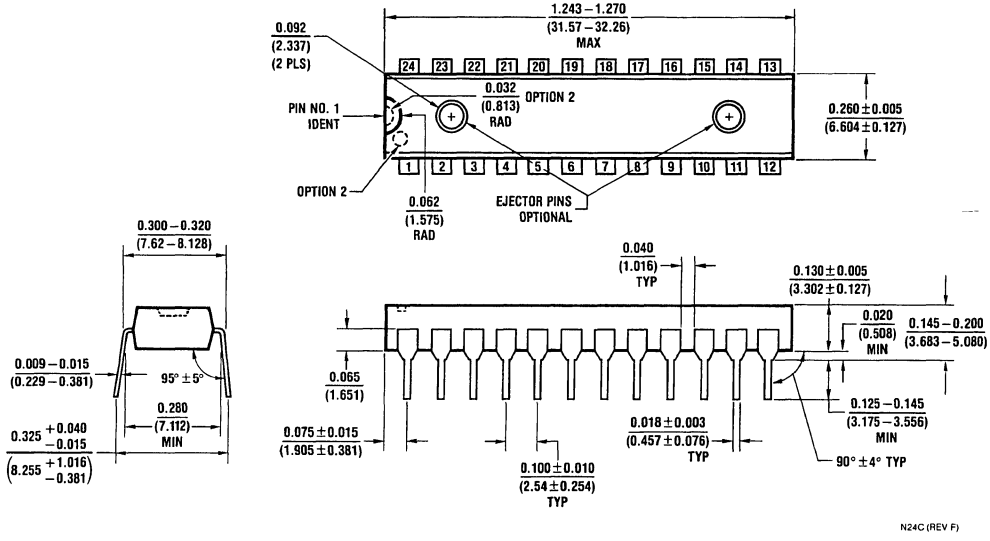

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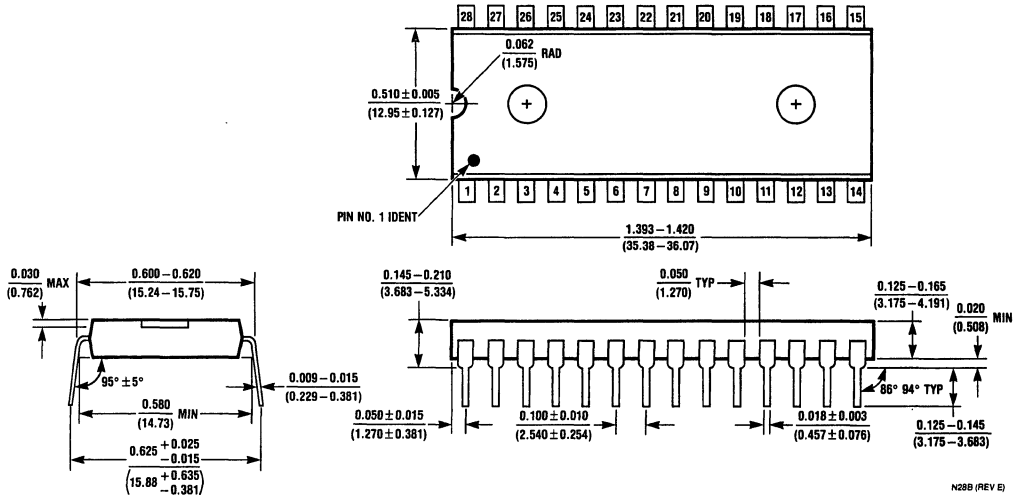

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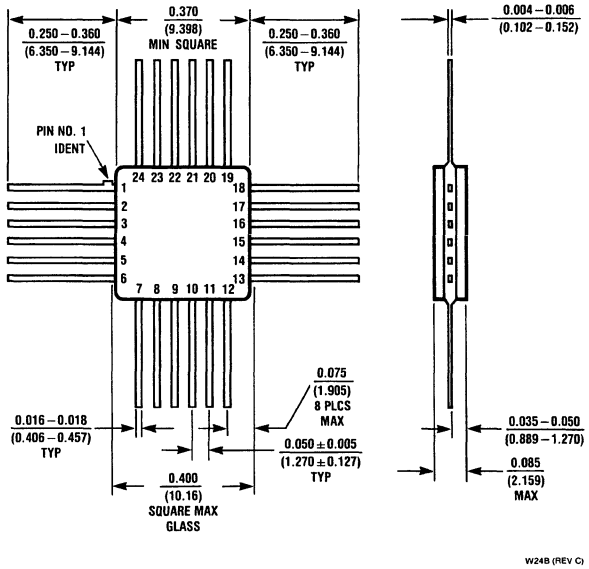

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