NEC

MOS INTEGRATED CIRCUIT

μPD70P3000

V851™
32-/16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD70P3000 is a one-time PROM version of the μPD703000. A program can be written only once to the PROM of the one-time PROM and this model is useful for small-scale production of a variety of application sets or early start of production.

Functions in detail are described in the following user's manuals. Be sure to read these manuals when you design your systems.

V851 User's Manual-Hardware : U10935E
V850 Family™ User's Manual-Architecture : U10243E

FEATURES

- Compatible with μPD703000
  - Can be replaced with mask ROM model, μPD703000, for mass production of application set
- Internal PROM: 32K bytes
  - Can be written only once
- PROM programming characteristics: μPD27C1001A compatible
- QTOP™ microcomputer compatible

Remark QTOP microcomputer is NEC's microcomputer with one-time PROM, with total support of writing service (from program writing, to marking, screening, and verifying).

ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency (MHz)
μPD70P3000GC-25-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	25
μPD70P3000GC-33-7EA	100-pin plastic QFP (fine pitch) (14 × 14 mm)	33

The one-time PROM model is referred to as "PROM" in this document.

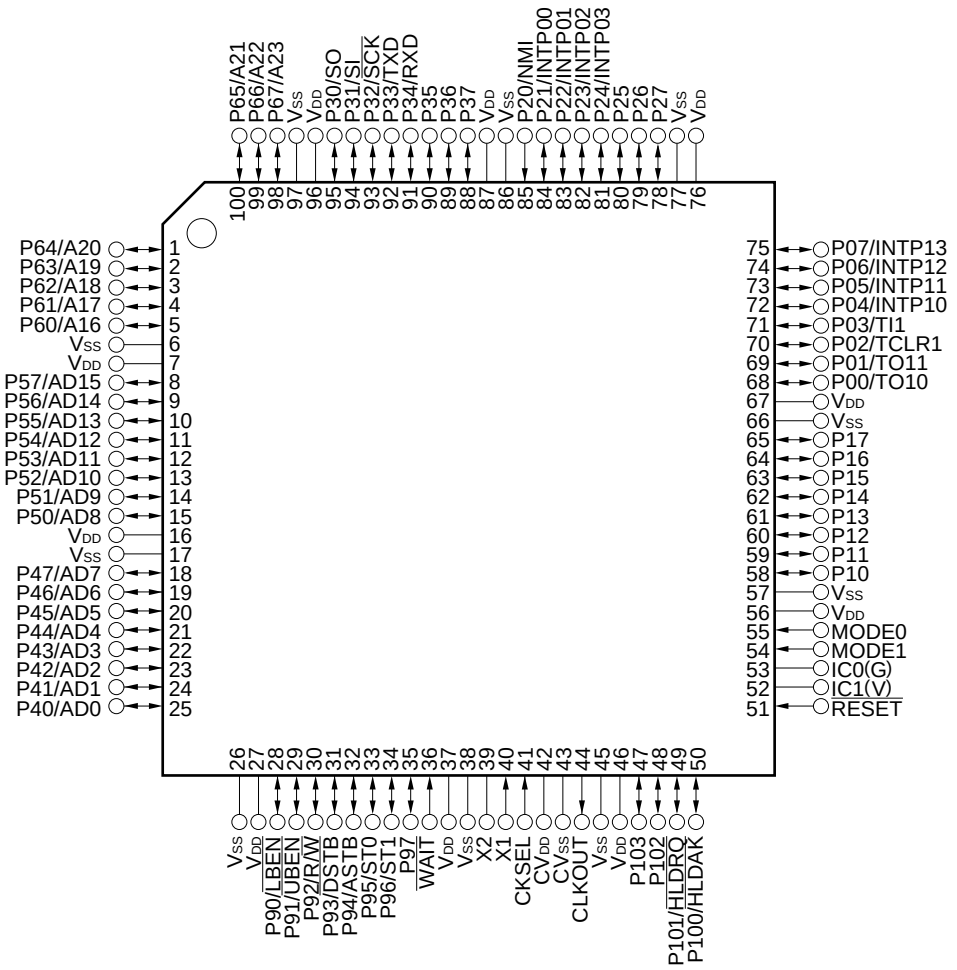
The information in this document is subject to change without notice.

Document No. U10988EJ3V0DS00 (3rd edition)
Date Published August 1997 N
Printed in Japan

The mark ★ shows major revised points.

PIN CONFIGURATION (Top View)

(1) Normal operation mode



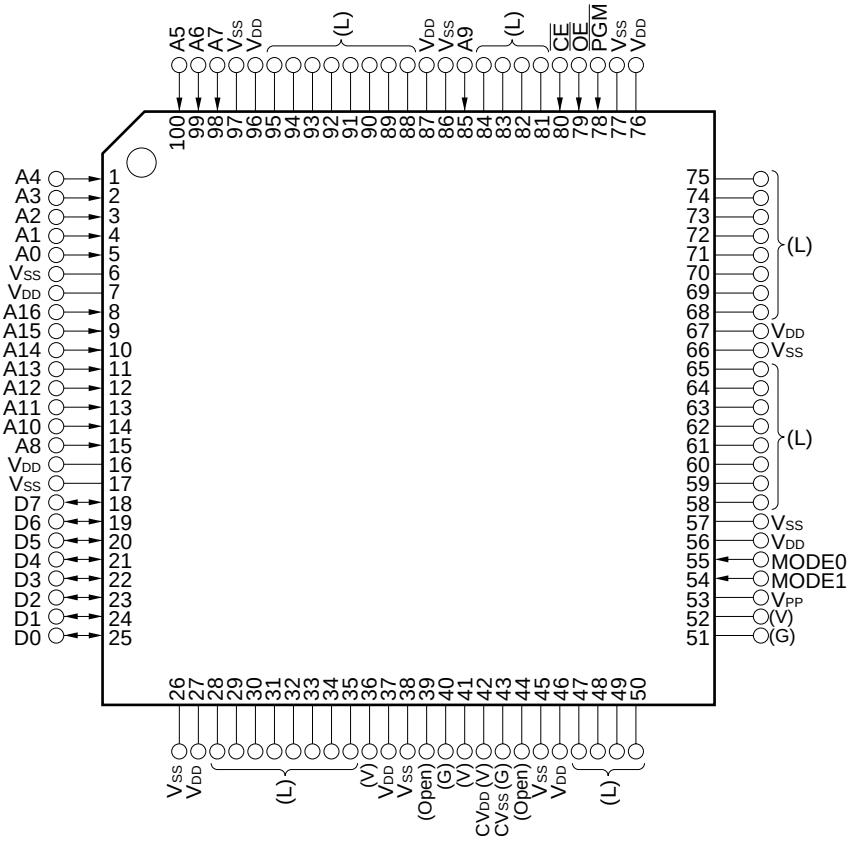
Caution The letters in brackets ( ) indicate the processing of the pins not used in the normal operation mode.

G: Directly connect this pin to V_{SS}.

V: Directly connect this pin to V_{DD}.

P00-P07	:	Port0
P10-P17	:	Port1
P20-P27	:	Port2
P30-P37	:	Port3
P40-P47	:	Port4
P50-P57	:	Port5
P60-P67	:	Port6
P90-P97	:	Port9
P100-P103	:	Port10
TO10, TO11	:	Timer Output
TCLR1	:	Timer Clear
TI1	:	Timer Input
INTP00-INTP03, INTP10-INTP13	:	Interrupt Request From Peripherals
NMI	:	Non-maskable Interrupt Request
SO	:	Serial Output
SI	:	Serial Input
$\overline{SCK}$	:	Serial Clock
TXD	:	Transmit Data
RXD	:	Receive Data
AD0-AD15	:	Address/Data Bus
A16-A23	:	Address Bus
$\overline{LBEN}$	:	Lower Byte Enable
$\overline{UBEN}$	:	Upper Byte Enable
R/$\overline{W}$	:	Read/Write Status
$\overline{DSTB}$	:	Data Strobe
ASTB	:	Address Strobe
ST0, ST1	:	Status
$\overline{HLDAK}$	:	Hold Acknowledge
$\overline{HLDRQ}$	:	Hold Request
CLKOUT	:	Clock Output
CKSEL	:	Clock Select
$\overline{WAIT}$	:	Wait
MODE0, MODE1	:	Mode
$\overline{RESET}$	:	Reset
X1, X2	:	Crystal
CV_{DD}	:	Clock Generator Power Supply
CV_{SS}	:	Clock Generator Ground
V_{DD}	:	Power Supply
V_{SS}	:	Ground
IC0, IC1	:	Internally Connected

(2) PROM programming mode



Caution The letters in brackets ( ) indicate the processing of the pins not used in the normal operation mode.

L : Individually connect to V_{SS} via resistor.

G : Directly connect this pin to V_{SS}.

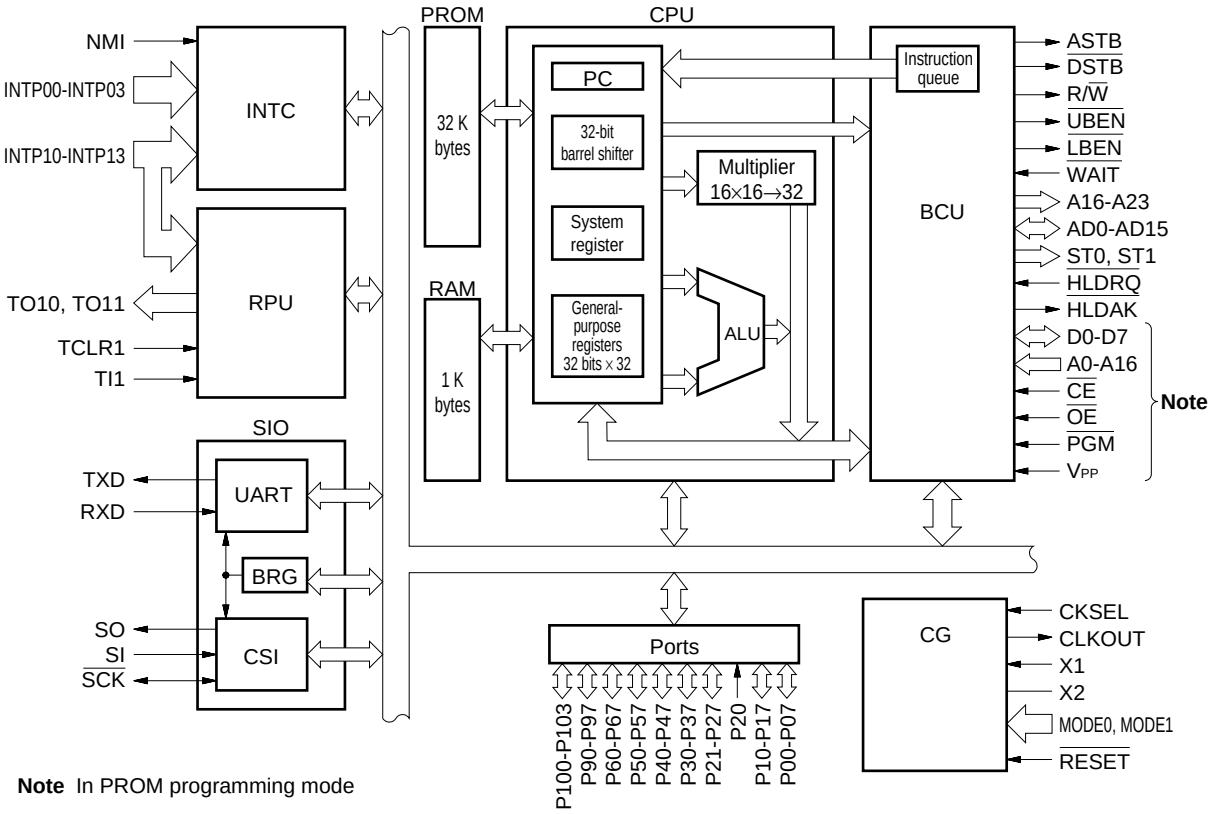
V : Directly connect this pin to V_{DD}.

Open : Connect nothing.

A0-A16	: Address Bus	MODE0, MODE1	: Programming Mode Set
D0-D7	: Data Bus	V_{DD}	: Power Supply
$\overline{CE}$	: Chip Enable	V_{SS}	: Ground
$\overline{OE}$	: Output Enable	V_{PP}	: Programming Power Supply
$\overline{PGM}$	: Programming Mode		

INTERNAL BLOCK DIAGRAM

★



Note In PROM programming mode

TABLE OF CONTENTS

1. DIFFERENCES BETWEEN μPD70P3000 and μPD703000

The μPD70P3000 is a PROM version of the μPD703000. Therefore, these two models are identical except for differences because of the ROM specifications (for example, specifications concerning writing and verifying). Table 1-1 shows the differences between the two.

Note that this document mainly describes the PROM specifications of the μPD70P3000. For the other functions, refer to the documents on the μPD703000.

Table 1-1. Differences between μPD70P3000 and μPD703000

Item \ Part Number	μPD70P3000	μPD70P3000
Internal program memory (electrical writing)	One-time PROM (can be written only once)	Mask ROM
PROM programming pin	Provided	None
Setting of MODE0 and MODE1 pins	• In normal operation mode MODE0, 1 = LH • In PROM programming mode MODE0, 1 = HH	• In normal operation mode MODE0, 1 = LH • In ROM-less mode MODE0, 1 = LL
Electrical specifications	Current consumption differs	
Others	Noise immunity and noise radiation differ because circuit scale and mask layout differ.	

Cautions 1. The PROM and mask ROM models differ from each other in terms of noise immunity and noise radiation. When replacing the PROM model with the mask ROM model in the course of experimental production to mass production, perform thorough evaluation with the CS model (not ES model) of the mask ROM model.

2. Directly connect the MODE0 and MODE1 pins to V_{DD} or V_{SS}.

★ **3. When replacing the PROM model with the mask ROM model, write the same code to the empty area of the on-chip ROM.**

Remark L : low level
H : high level

2. PIN FUNCTIONS

2.1 Normal Operation Mode (MODE0 = L, MODE1 = H)

2.1.1 Port pins

(1/2)

Pin Name	I/O	Function	Shared with:
P00	I/O	Port 0	TO10
P01		8-bit I/O port.	TO11
P02		Can be set in input or output mode in 1-bit units.	TCLR1
P03			TI1
P04			INTP10
P05			INTP11
P06			INTP12
P07			INTP13
P10-P17	I/O	Port 1 8-bit I/O port. Can be set in input or output mode in 1-bit units.	—
P20	Input	Port 2	NMI
P21	I/O	P20 is an input-only port.	INTP00
P22		Operates as an NMI input when valid edge is input.	INTP01
P23		Bit 0 of the P2 register indicates NMI input status.	INTP02
P24		P21 through P27 are 7-bit I/O ports.	INTP03
P25-P27		Can be set in input or output mode in 1-bit units.	—
P30	I/O	Port 3	SO
P31		8-bit I/O port.	SI
P32		Can be set in input or output mode in 1-bit units.	$\overline{\text{SCK}}$
P33			TXD
P34			RXD
P35-P37			—
P40-P47	I/O	Port 4 8-bit I/O port. Can be set in input or output mode in 1-bit units.	AD0-AD7
P50-P57	I/O	Port 5 8-bit I/O port. Can be set in input or output mode in 1-bit units.	AD8-AD15
P60-P67	I/O	Port 6 8-bit I/O port. Can be set in input or output mode in 1-bit units.	A16-A23

(2/2)

Pin Name	I/O	Function	Shared with:
P90	I/O	Port 9	$\overline{\text{LBEN}}$
P91		8-bit I/O port.	$\overline{\text{UBEN}}$
P92		Can be set in input or output mode in 1-bit units.	R/$\overline{\text{W}}$
P93			$\overline{\text{DSTB}}$
P94			ASTB
P95			ST0
P96			ST1
P97			—
P100	I/O	Port 10	$\overline{\text{HLDAK}}$
P101		4-bit I/O port.	$\overline{\text{HLDRQ}}$
P102		Can be set in input or output mode in 1-bit units.	—
P103			—

2.1.2 Pins other than port pins

(1/2)

Pin Name	I/O	Function	Shared with:
TO10	Output	Pulse signal output of timer 1	P00
TO11			P01
TCLR1	Input	External clear signal input of timer 1	P02
TI1		External count clock input of timer 1	P03
INTP10	Input	External maskable interrupt request input and external capture trigger	P04
INTP11		input of timer 1	P05
INTP12			P06
INTP13			P07
NMI	Input	Non-maskable interrupt request input	P20
INTP00	Input	External maskable interrupt request input	P21
INTP01			P22
INTP02			P23
INTP03			P24
SO	Output	Serial transmit data output of CSI	P30
SI	Input	Serial receive data input of CSI	P31
$\overline{\text{SCK}}$	I/O	Serial clock I/O of CSI	P32
TXD	Output	Serial transmit data output of UART	P33
RXD	Input	Serial receive data input of UART	P34
AD0-AD7	I/O	16-bit multiplexed address/data bus when external memory is connected	P40-P47
AD8-AD15			P50-P57
A16-A23	Output	High-order address bus when external memory is connected	P60-P67
$\overline{\text{LBEN}}$	Output	Low-order byte enable signal output of external data bus	P90
$\overline{\text{UBEN}}$		High-order byte enable signal output of external data bus	P91

(2/2)

Pin Name	I/O	Function	Shared with:
$\overline{R/W}$	Output	External read/write status output	P92
$\overline{DSTB}$		External data strobe signal output	P93
ASTB		External address strobe signal output	P94
ST0		External bus cycle status output	P95
ST1			P96
$\overline{HLDAK}$	Output	Bus hold acknowledge output	P100
$\overline{HLDRQ}$	Input	Bus hold request input	P101
CLKOUT	Output	System clock output	—
CKSEL	Input	Input specifying operation mode of clock generator	—
$\overline{WAIT}$	Input	Control signal input inserting wait state in bus cycle	—
MODE0, MODE1	Input	Operation mode specification	—
$\overline{RESET}$	Input	System reset input	—
X1	Input	System clock oscillator connection.	—
X2	—	Input external clock to X1 to supply external clock.	—
CV_{DD}	—	Positive power supply for internal clock generator	—
CV_{SS}	—	Ground potential for internal clock generator	—
V_{DD}	—	Positive power supply	—
V_{SS}	—	Ground potential	—
IC0, IC1	—	Internally connected	—

2.2 PROM Programming Mode (MODE0 = H, MODE1 = H)

Pin Name	Function	Corresponding Pin of μPD27C1001A
P60-P67	Low-order address (A0 through A7) input	A0-A7
P50, P20, P51-P57	High-order address (A8 through A16) input	A8, A9, A10-A16
P40-P47	Data I/O	D0-D7
P25	$\overline{CE}$ (chip enable) input	$\overline{CE}$
P26	$\overline{OE}$ (output enable) input	$\overline{OE}$
P27	$\overline{PGM}$ (program) input	$\overline{PGM}$
V_{PP}	Power for program writing	V_{PP}
MODE0, MODE1	Operation mode specification	—

2.3 I/O Circuits of Pins and Recommended Connections of Unused Pins

Table 2-1 shows the I/O circuit type of each pin in the normal operation mode, and the recommended connections of the unused pins. Figure 2-1 shows a partially simplified diagram of each circuit.

In the PROM programming mode, process the unused pins by referring to the diagram in PIN CONFIGURATION.

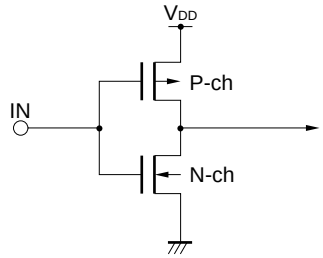
When connecting a pin to V_{DD} or V_{SS} via resistor, use of a resistor of 3 to 10 kΩ is recommended.

Table 2-1. I/O Circuit Types of Each Pin and Recommended Connections of Unused Pins

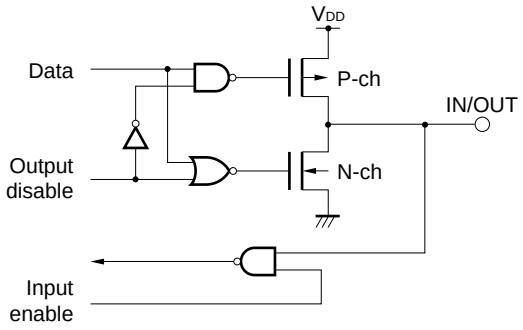
Pin	I/O Circuit Type	Recommended Connections
P00/TO10, P01/TO11	5	Input : Individually connect to V_{DD} or V_{SS} via resistor.
P02/TCLR1, P03/TI1	8	Output : Open
P04/INTP10-P07/INTP13		
P10-P17	5	
P20/NMI	2	Directly connect to V_{SS}.
P21/INTP00-P24/INTP03	8	Input : Individually connect to V_{DD} or V_{SS} via resistor.
P25	5	Output : Open
P26, P27	8	
P30/SO	5	
P31/SI, P32/$\overline{\text{SCK}}$	8	
P33/TXD, P34/RXD, P35	5	
P36, P37	8	
P40/AD0-P47/AD7	5	
P50/AD8-P57/AD15		
P60/A16-A67/A23		
P90/$\overline{\text{LBEN}}$		
P91/$\overline{\text{UBEN}}$		
P92/R/$\overline{\text{W}}$		
P93/$\overline{\text{DSTB}}$		
P94/ASTB		
P95/ST0, P96/ST1		
P97		
P100/$\overline{\text{HLDAK}}$		
P101/$\overline{\text{HLDRQ}}$		
P102		
P103		
CLKOUT	3	Open
CKSEL	2	—
$\overline{\text{WAIT}}$	1	Directly connect to V_{DD}.
MODE0, MODE1	2	—
$\overline{\text{RESET}}$		
IC0	—	Directly connect to V_{SS}.
IC1	—	Directly connect to V_{DD}.

Figure 2-1. I/O Circuits of Pins

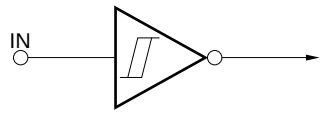
Type 1



Type 5

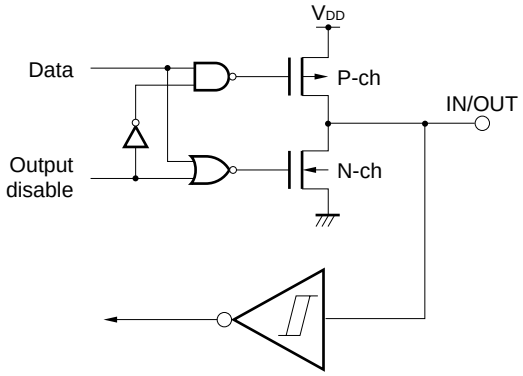


Type 2

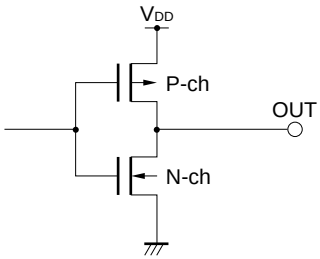


Schmitt trigger input with hysteresis characteristics

Type 8



Type 3



3. PROM PROGRAMMING

The μPD70P3000 has a 32K × 8 bit PROM that can be electrically written. To program this PROM, set the PROM programming mode by using the V_{PP}, MODE0, and MODE1 pins.

The programming characteristics are compatible with those of the μPD27C1001A.

Table 3-1. Pin Functions in PROM Programming Mode

Function	Normal Operation Mode	PROM Programming Mode
Address input	P60/A16-P67/A23, P50/AD8, P20/NMI, P51/AD9-P57/AD15	A0-A16
Data I/O	P40/AD0-P47/AD7	D0-D7
Program input	P27	$\overline{PGM}$
Chip enable input	P25	$\overline{CE}$
Output enable input	P26	$\overline{OE}$
Program voltage	V_{PP}	
Mode specification	MODE0, MODE1	

3.1 Operation Mode

To set the programming writing/verify mode, set as follows: V_{PP} = + 12.5 V, MODE0 = H, MODE1 = H

In this mode, the modes shown in Table 3-2 can be selected by using the $\overline{CE}$, $\overline{OE}$, and $\overline{PGM}$ pins.

To read the contents of the PROM, set the read mode.

Connect the unused pins by referring to the diagram in PIN CONFIGURATION.

Table 3-2. Operation Modes for PROM Programming

Operation Mode	MODE0	MODE1	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{DD}	D0-D7
Page data latch mode	H	H	H	L	H	+ 12.5 V	+ 6.5 V	Data input
Page write mode			H	H	L			High impedance
Byte write mode			L	H	L			Data input
Program verify mode			L	L	H			Data output
Program inhibit mode			x	L	L			High impedance[Note]
			x	H	H			
Read mode			L	L	H	+ 5.0 V	+ 5.0 V	Data output
Output disable mode			L	H	x			High impedance[Note]
Standby mode			H	x	x			High impedance[Note]

Note L or H can be input (address input is invalid).

Remark x: L or H

(1) Page data latch mode

The page data latch mode can be set by making the $\overline{CE}$ and $\overline{PGM}$ pins high and $\overline{OE}$ pin low at the beginning of the page write mode.

In the page data latch mode, 1 page or 4 bytes of data are latched to the internal address/data latch circuit.

(2) Page write mode

In this mode, page write is executed by applying a program pulse of 0.1 ms to the $\overline{PGM}$ pin when $\overline{CE}$ = H and $\overline{OE}$ = H after 1 page or 4 bytes of addresses and data have been latched in the page data latch mode. After that, the program is verified when $\overline{CE}$ = L and $\overline{OE}$ = L.

If the program cannot be written by applying the program pulse once, writing and verification are repeatedly executed X times (X ≤ 10).

(3) Byte write mode

Byte write is executed by applying a program pulse (active low) of 0.1 ms to the $\overline{PGM}$ pin when $\overline{CE}$ = L and $\overline{OE}$ = H. After that, the program is verified when $\overline{OE}$ = L.

If the program cannot be written by applying the program pulse once, writing and verification are repeatedly executed X times (X ≤ 10).

(4) Program verify mode

The program verify mode is set when $\overline{CE}$ = L, $\overline{OE}$ = L, and $\overline{PGM}$ = H.

Check to see if the program has been correctly written, in this mode.

(5) Program inhibit mode

The program inhibit mode is used to write a program to one of several μPD70P3000s whose $\overline{OE}$, V_{PP} and D0 through D7 pins are connected in parallel.

To write a program, either the page write mode or byte write mode above is used. At this time, the program is not written to any device whose $\overline{PGM}$ pin is made high.

(6) Read mode

The read mode is set when $\overline{CE}$ = L, $\overline{OE}$ = L, and $\overline{PGM}$ = H.

(7) Output disable mode

The data output goes into a high-impedance state and the output disable mode is set by making $\overline{CE}$ low and $\overline{OE}$ high.

When two or more μPD70P3000s are connected to the data bus, any one of the devices can be selected and data can be read by controlling the $\overline{OE}$ pin.

(8) Standby mode

The standby mode is set by making $\overline{CE}$ high.

In this mode, the data output goes into a high-impedance state regardless of the status of $\overline{OE}$.

3.2 PROM Writing Procedure

Figure 3-1. Flowchart in Page Program Mode

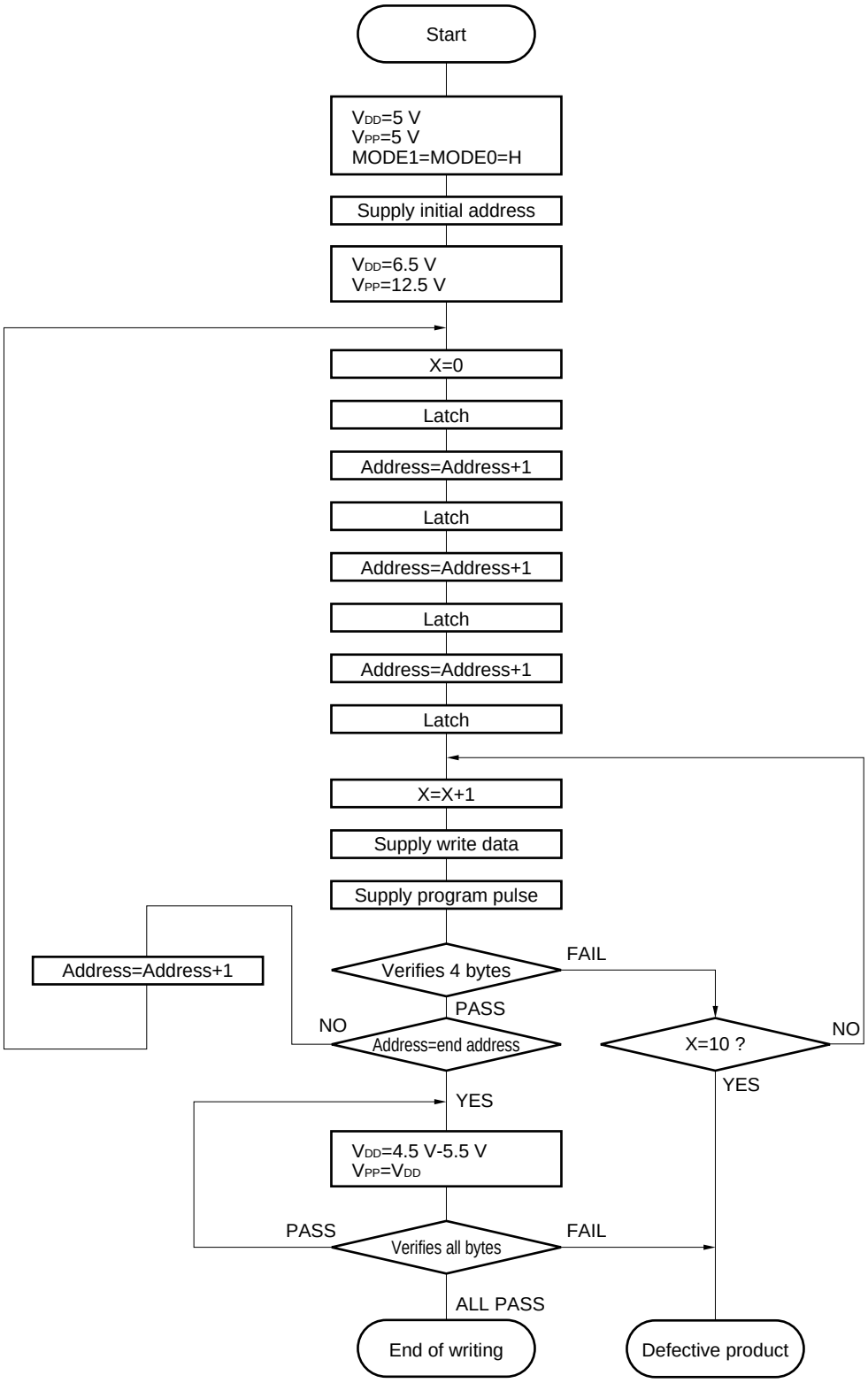
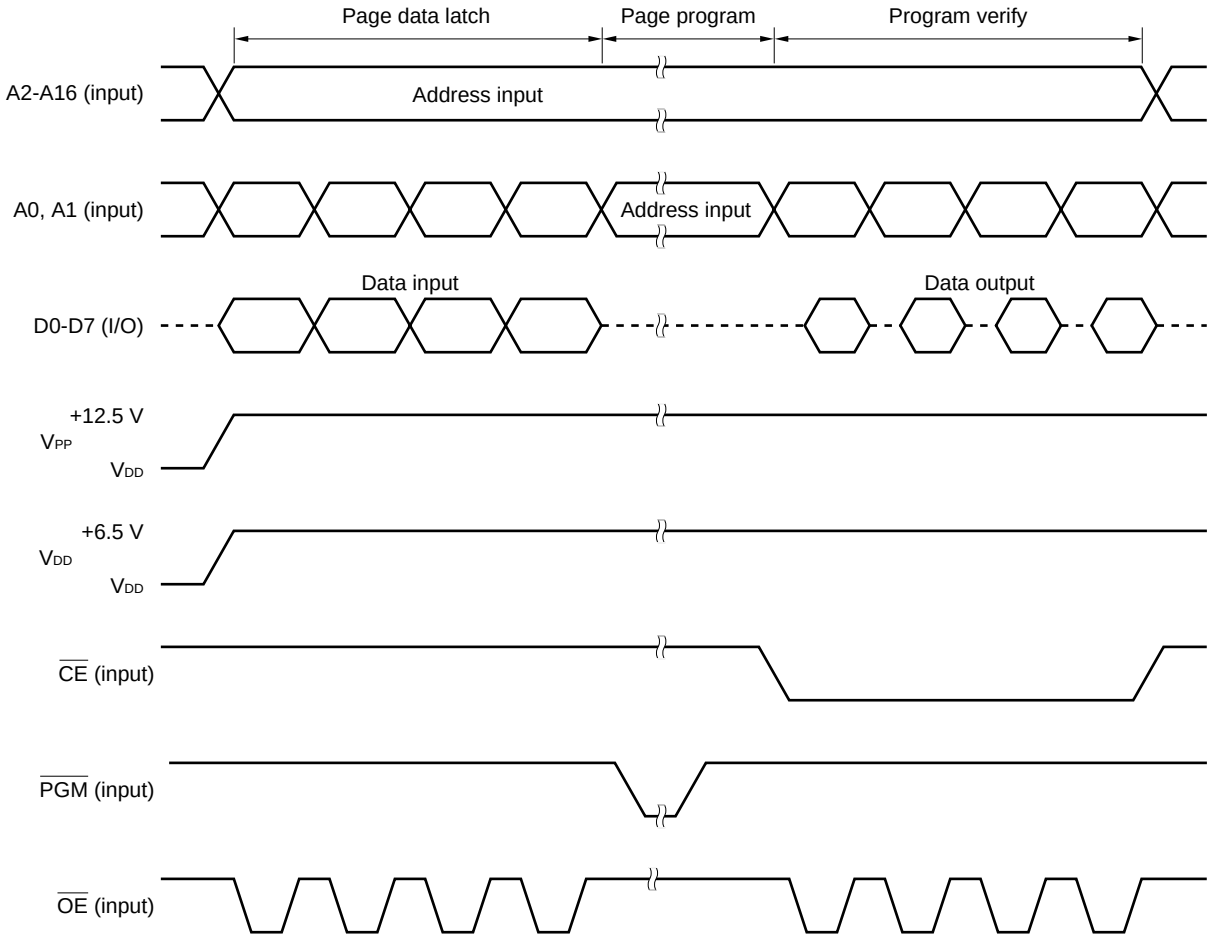


Figure 3-2. PROM Writing/Verify Timing (page program mode)



Remark The broken line indicates the high-impedance state.

Figure 3-3. Flowchart in Byte Program Mode

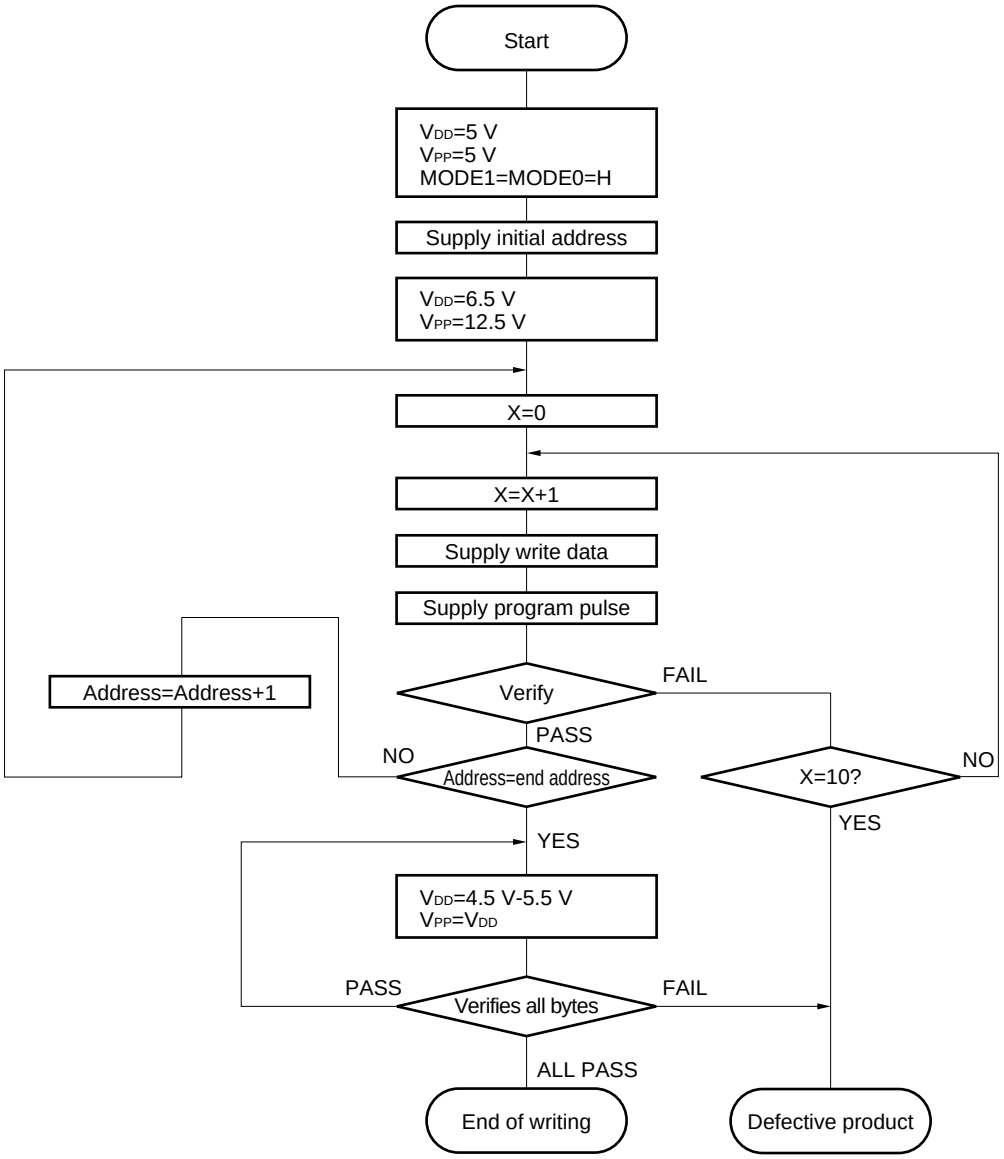
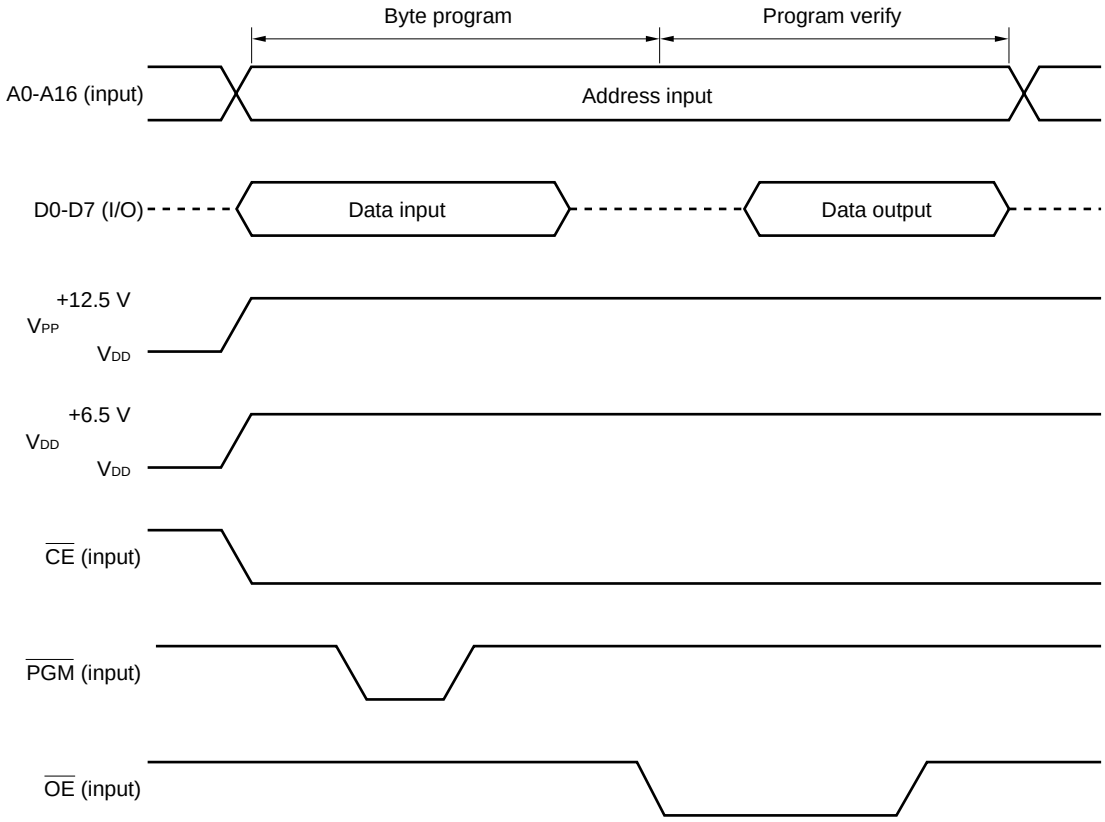


Figure 3-4. PROM Writing/Verifying Timing (byte program mode)



Remark The broken line indicates the high-impedance state.

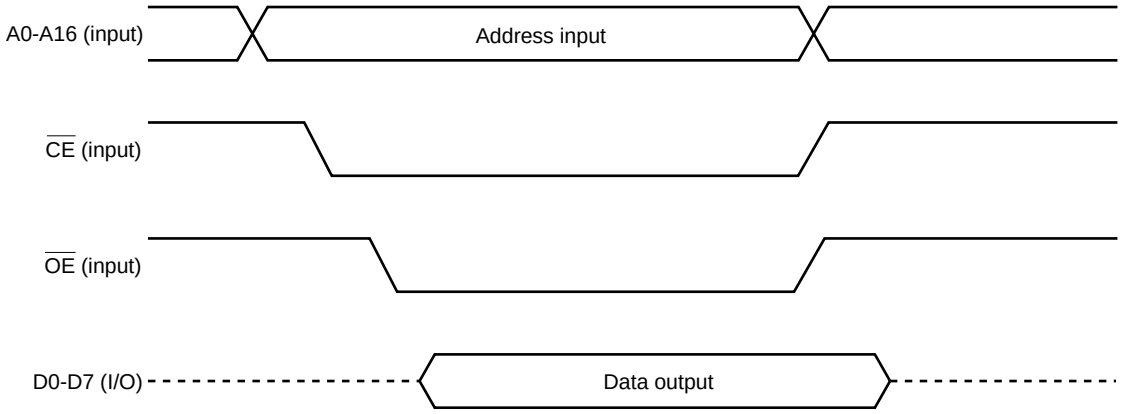
3.3 PROM Reading Procedure

The procedure to read the contents of the PROM to the external data bus (D0 through D7) is as follows:

(1) Fix the MODE0 and MODE1 pins to low level. Connect the unused pins by referring to the diagram in PIN CONFIGURATION.
(2) Supply + 5 V to the V_{DD} and V_{PP} pins.
(3) Input the address of the data to be read to the A0 through A16 pins.
(4) Set the read mode ($\overline{CE}$ = L, $\overline{OE}$ = L).
(5) Data are output to pins D0 through D7.

Figure 3-5 shows the timing of steps (2) through (5) above.

Figure 3-5. PROM Reading Timing



Remark The broken line indicates the high-impedance state.

4. SCREENING OF ONE-TIME PROM DEVICE

Because of its structure, the one-time PROM cannot be completely tested by NEC before shipment. It is recommended to perform screening to verify the PROM, after writing the necessary data to the PROM and storing the device under the following conditions:

Storage Temperature	Storage Time
125 °C	24 hours

NEC offers a service, at a charge, called QTOP microcontroller, for writing, marking, screening, and verifying one-time PROMs. For details, consult NEC.

5. NOTES ON RELEASING STOP MODE WHEN EXTERNAL CLOCK IS USED

When an external clock is used, the clock is supplied by an external system.

To release the STOP mode (by $\overline{\text{RESET}}$ or NMI input), therefore, resume clock supply at least 100 μs before inputting the $\overline{\text{RESET}}$ or NMI signal to make sure that a sufficiently long time elapses to allow the PROM to stabilize.

6. ELECTRICAL SPECIFICATIONS

6.1 Normal Operation Mode

Corresponding Electrical Specifications

Part Number	V_{DD} = 5.0 V ± 10 %	V_{DD} = 3.0 to 3.6 V
μPD70P3000GC-25-7EA	Electrical specifications specified	Outside guaranteed operating range
μPD70P3000GC-33-7EA	Electrical specifications specified	Electrical specifications specified

6.1.1 When V_{DD} = 5.0 V ± 10 %

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	–0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin	–0.5 to +7.0	V
	CV_{SS}	CV_{SS} pin	–0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 pin, V_{DD} = 5.0 V ± 10 %	–0.5 to V_{DD} + 0.3	V
	V_{I2}	V_{PP} pin in PROM programming mode, V_{DD} = 5.0 V ± 10 %	–0.5 to +13.5	V
Clock input voltage	V_X	X1 pin, V_{DD} = 5.0 V ± 10 %	–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	–4.0	mA
		Total of all pins	–100	mA
Output voltage	V_O	V_{DD} = 5.0 V ± 10 %	–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A	When operating at 25 MHz	–40 to +85	°C
		When operating at 33 MHz	–20 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to V_{DD}, V_{CC}, or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

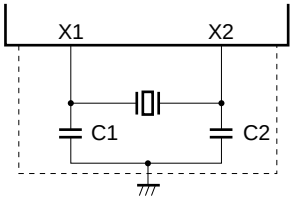
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz			15	pF
I/O capacitance	C_{IO}	Pins other than tested pin: 0 V			15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 25 MHz	–40 to +85 °C	5.0 V ± 10 %
	0 to 33 MHz	–20 to +70 °C	
PLL mode	Self oscillation frequency to 25 MHz	–40 to +85 °C	5.0 V ± 10 %
	Self oscillation frequency to 33 MHz	–20 to +70 °C	

Recommended Oscillation Circuit

(a) Ceramic resonator connection (TDK, Murata Mfg.: T_A = –40 to +85 °C, Kyocera: T_A = –20 to +80 °C)



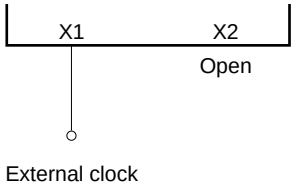
Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constants		Oscillation Voltage Renge		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK Corp.	FCR2.0MC3	2.0	Provided	Provided	4.5	5.5	0.26
	CCR3.2MC3	3.2	Provided	Provided	4.5	5.5	0.62
	FCR5.0MC5	5.0	Provided	Provided	4.5	5.5	0.30
	CCR5.0MC3	5.0	Provided	Provided	4.5	5.5	0.38
	CCR6.6MC3	6.6	Provided	Provided	4.5	5.5	0.32
Kyocera Corp.	KBR-2.0MS	2.0	82	82	4.5	5.5	1.2
	KBR-2.7MS	2.7	68	68	4.5	5.5	0.8
	KBR-3.2MS	3.2	47	47	4.5	5.5	0.3
	KBR-5.0MSA	5.0	33	33	4.5	5.5	0.4
	KBR-6.6MS	6.6	33	33	4.5	5.5	0.2
Murata Mfg. Co., Ltd.	CSA5.00MG	5.0	30	30	4.5	5.5	0.13
	CST5.00MGW	5.0	Provided	Provided	4.5	5.5	0.13
	CSA6.60MTZ	6.6	30	30	4.5	5.5	0.10
	CST6.60MTW	6.6	Provided	Provided	4.5	5.5	0.10

Cautions 1. Connect the oscillation circuit as closely to X2 pin as possible.

2. Do not route any other signal lines in the range indicated by the broken line in the above figure.

3. Thoroughly evaluate the matching between the μPD70P3000 and resonator.

(b) External clock input



Caution Input CMOS level voltage to the X1 pin.

DC Characteristics (T_A = –40 to +85 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-25
(T_A = –20 to +70 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-33

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	Except X1 and **Note 1**	2.2		V_{DD}	V
			Note 1	0.8 V_{DD}		V_{DD}	V
Input voltage, low		V_{IL}	Except X1 and **Note 1**	0		+0.8	V
			Note 1	0		0.2 V_{DD}	V
X1 clock input voltage, high		V_{XH}	Direct mode	0.8 V_{DD}		V_{DD}	V
			PLL mode	0.8 V_{DD}		V_{DD}	V
X1 clock input voltage, low		V_{XL}	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input threshold voltage		V_T^+	**Note 1**, rising		3.0		V
		V_T^-	**Note 1**, falling		2.0		V
Schmitt trigger input hysteresis width		$V_T^+ - V_T^-$	**Note 1**	0.5			V
Output voltage, high		V_{OH}	I_{OH} = –2.5 mA	0.7 V_{DD}			V
			I_{OH} = –100 μA	V_{DD} – 0.4			V
Output voltage, low		V_{OL}	I_{OC} = 2.5 mA			0.45	V
Input leakage current, high		I_{LIH}	$V_I = V_{DD}$			10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			–10	μA
Output leakage current, high		I_{LOH}	$V_O = V_{DD}$			10	μA
Output leakage current, low		I_{LOL}	V_O = 0 V			–10	μA
Supply current	Operating	I_{DD1}	Direct mode		$1.6 \times \phi + 14$	$2.5 \times \phi + 15$	mA
			PLL mode		$1.7 \times \phi + 16$	$2.7 \times \phi + 18$	mA
	In HALT mode	I_{DD2}	Direct mode		$0.5 \times \phi + 3$	$0.7 \times \phi + 10$	mA
			PLL mode		$0.6 \times \phi + 5$	$0.9 \times \phi + 13$	mA
	In IDLE mode	I_{DD3}	Direct mode		$8 \times \phi + 300$	$10 \times \phi + 500$	μA
			PLL mode		$0.1 \times \phi + 2$	$0.2 \times \phi + 3$	mA
	In STOP mode	I_{DD4}	**Note 2**		1	50	μA
			Note 3			200	μA

Notes 1. $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL

2. When operating at 25 MHz: –40 ˚C ≤ T_A ≤ +50 ˚C
When operating at 33 MHz: –20 ˚C ≤ T_A ≤ +50 ˚C

3. When operating at 25 MHz: 50 ˚C < T_A ≤ 85 ˚C
When operating at 33 MHz: 50 ˚C < T_A ≤ 70 ˚C

Remarks 1. TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 5.0 V.

2. ϕ : Internal operating clock frequency

Data Retention Characteristics (T_A = –40 to +85 °C): μPD70P3000GC-25
(T_A = –20 to +70 °C): μPD70P3000GC-33

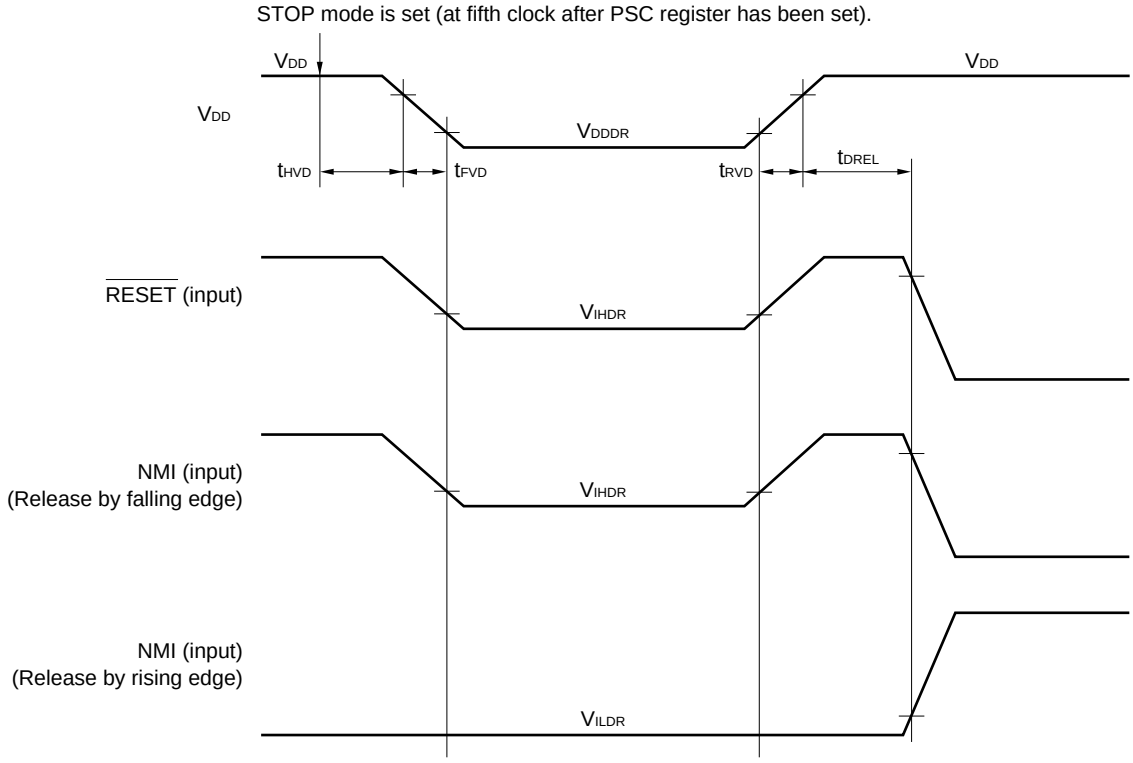
Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode		1.5		5.5	V
Data hold current	I_{DDDR}	V_{DD} = V_{DDDR}	**Note 1**		0.2 V_{DDDR}	50	μA
			Note 2		0.2 V_{DDDR}	200	μA
Supply voltage rise time	t_{RVD}			200			μs
Supply voltage fall time	t_{FVD}			200			μs
Supply voltage hold time (vs. STOP mode setting)	t_{HVD}			0			ms
STOP mode release signal input time	t_{DREL}			0			ns
Data hold input voltage, high	V_{IHDR}	**Note 3**		0.9 V_{DDDR}		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	**Note 3**		0		0.1 V_{DDDR}	V

Notes 1. When operating at 25 MHz: –40 °C ≤ T_A ≤ +50 °C
When operating at 33 MHz: –20 °C ≤ T_A ≤ +50 °C

2. When operating at 25 MHz: 50 °C < T_A ≤ 85 °C
When operating at 33 MHz: 50 °C < T_A ≤ 70 °C

3. $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INT03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1

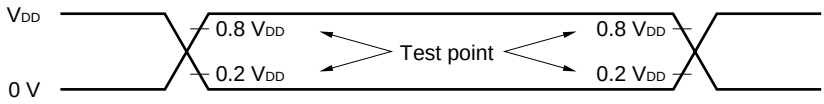
Remark TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 5.0 V.



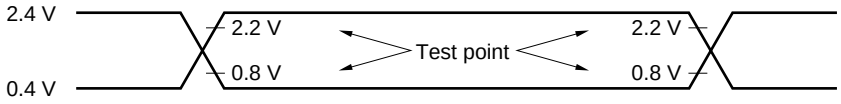
AC Characteristics (T_A = –40 to +85 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-25
(T_A = –20 to +70 °C, V_{DD} = 5.0 V ± 10 %, V_{SS} = 0 V): μPD70P3000GC-33

AC test input wave

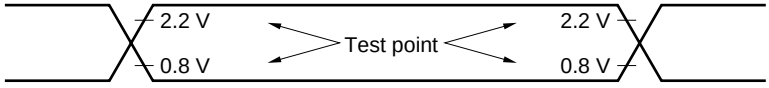
(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1



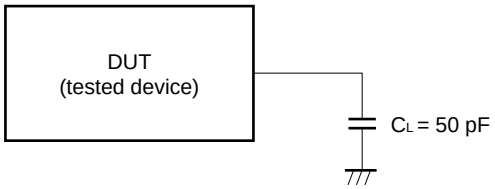
(b) Other than (a)



AC test output test point



Load condition



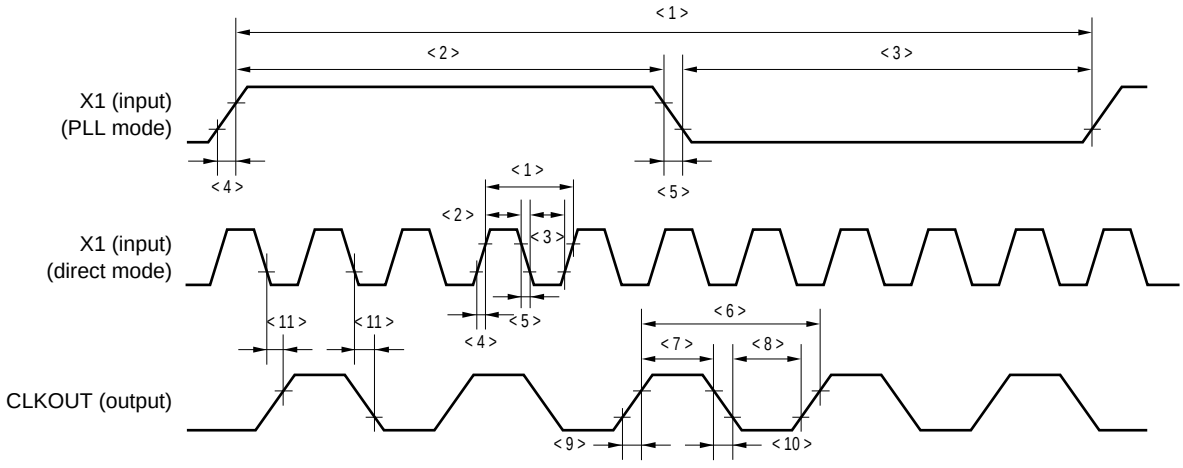
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, decrease the load capacitance of this device to less then 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
X1 input cycle	<1>	t_{CYX}	Direct mode	20	DC	15	DC	ns
			PLL mode	200	315	150	334	ns
X1 input width, high	<2>	t_{WXH}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input width, low	<3>	t_{WXL}	Direct mode	7		6		ns
			PLL mode	80		60		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7		7	ns
			PLL mode		15		10	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7		7	ns
			PLL mode		15		10	ns
CPU operating frequency	—	ϕ		0	25	0	33	MHz
CLKOUT output cycle	<6>	t_{CYK}		40	DC	30	DC	ns
CLKOUT width, high	<7>	t_{WKH}		0.5 T – 5		0.5 T – 5		ns
CLKOUT width, low	<8>	t_{WKL}		0.5 T – 5		0.5 T – 5		ns
CLKOUT rise time	<9>	t_{XR}			5		5	ns
CLKOUT fall time	<10>	t_{XF}			5		5	ns
X1 ↓→ CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	17	3	17	ns

Remark T = t_{CYK}

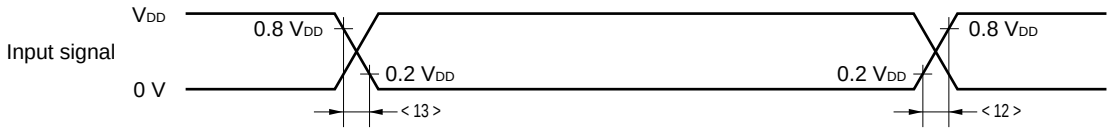
Parameter	Symbol		Condition	μPD70P3000-25	μPD70P3000-33	Unit
				TYP.	TYP.	
Self oscillation frequency	—	ϕ_P	PLL mode	2.8	2.8	MHz



(2) Input waveform

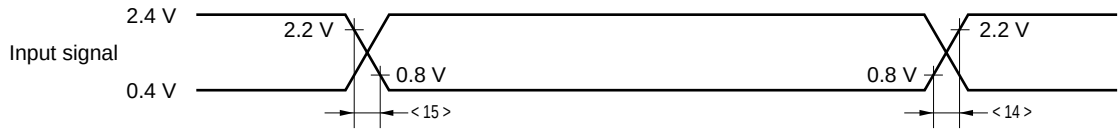
(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
Input rise time	<12>	t_{IR2}			20		20	ns
Input fall time	<13>	t_{IF2}			20		20	ns



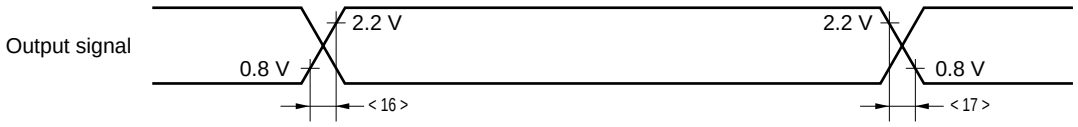
(b) Other than (a)

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
Input rise time	<14>	t_{IR1}			10		10	ns
Input fall time	<15>	t_{IF1}			10		10	ns



(3) Output waveform (other than CLKOUT)

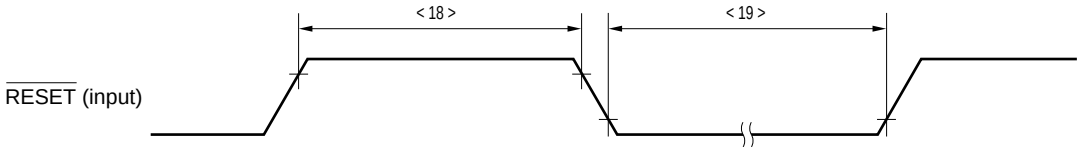
Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
Output rise time	<16>	t_{OR}			10		10	ns
Output fall time	<17>	t_{OF}			10		10	ns



(4) Reset timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{RESET}}$ width, high	<18>	t_{WRSH}		500		500		ns
$\overline{\text{RESET}}$ width, low	<19>	t_{WRSL}	On power application, or on releasing STOP mode	500 + T_{OST}		500 + T_{OST}		ns
			Except on power application, or except on releasing STOP mode	500		500		ns

Remark T_{OST}: oscillation stabilization time



(5) Read timing (1/2)

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	20	3	20	ns
CLKOUT ↑→ address float delay time	<21>	t_{FKA}		3	15	3	15	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	15	3	15	ns
CLKOUT ↓→ $\overline{\text{DSTB}}$ delay time	<23>	t_{DKD}		3	15	3	15	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	15	3	15	ns
Data input setup time (vs. CLKOUT ↑)	<25>	t_{SIDK}		5		5		ns
Data input hold time (vs. CLKOUT ↑)	<26>	t_{HKID}		5		5		ns
$\overline{\text{WAIT}}$ setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		5		5		ns
$\overline{\text{WAIT}}$ hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		5		5		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 10		0.5 T – 10		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 10		0.5 T – 10		ns
$\overline{\text{DSTB}}$ ↓→ address float delay time	<32>	t_{FDA}			0		0	ns
Data input setup time (vs. address)	<33>	t_{SAID}			(2 + n) T – 20		(2 + n) T – 20	ns
Data input setup time (vs. $\overline{\text{DSTB}}$ ↓)	<34>	t_{SDID}			(1 + n) T – 20		(1 + n) T – 20	ns
ASTB ↓→ $\overline{\text{DSTB}}$ ↓ delay time	<35>	t_{DSTD}		0.5 T – 10		0.5 T – 10		ns
Data input hold time (vs. $\overline{\text{DSTB}}$ ↑)	<36>	t_{HDID}		0		0		ns
$\overline{\text{DSTB}}$ ↑→ address output delay time	<37>	t_{DDA}		(1 + i) T		(1 + i) T		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 10		0.5 T – 10		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↓ delay time	<39>	t_{DDSTL}		(1.5 + i) T – 10		(1.5 + i) T – 10		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 10		0.5 T – 10		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 10		0.5 T – 10		ns
$\overline{\text{DSTB}}$ width, low	<42>	t_{WDL}		(1 + n) T – 10		(1 + n) T – 10		ns
ASTB width, high	<43>	t_{WSTH}		T – 10		T – 10		ns
$\overline{\text{WAIT}}$ setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 20		1.5 T – 20	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 20		(1.5 + n) T – 20	ns
$\overline{\text{WAIT}}$ hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		(1.5 + n) T		ns
$\overline{\text{WAIT}}$ setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 15		T – 15	ns
	<49>	t_{SSTWT2}			(1 + n) T – 15		(1 + n) T – 15	ns
$\overline{\text{WAIT}}$ hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		(1 + n) T		ns

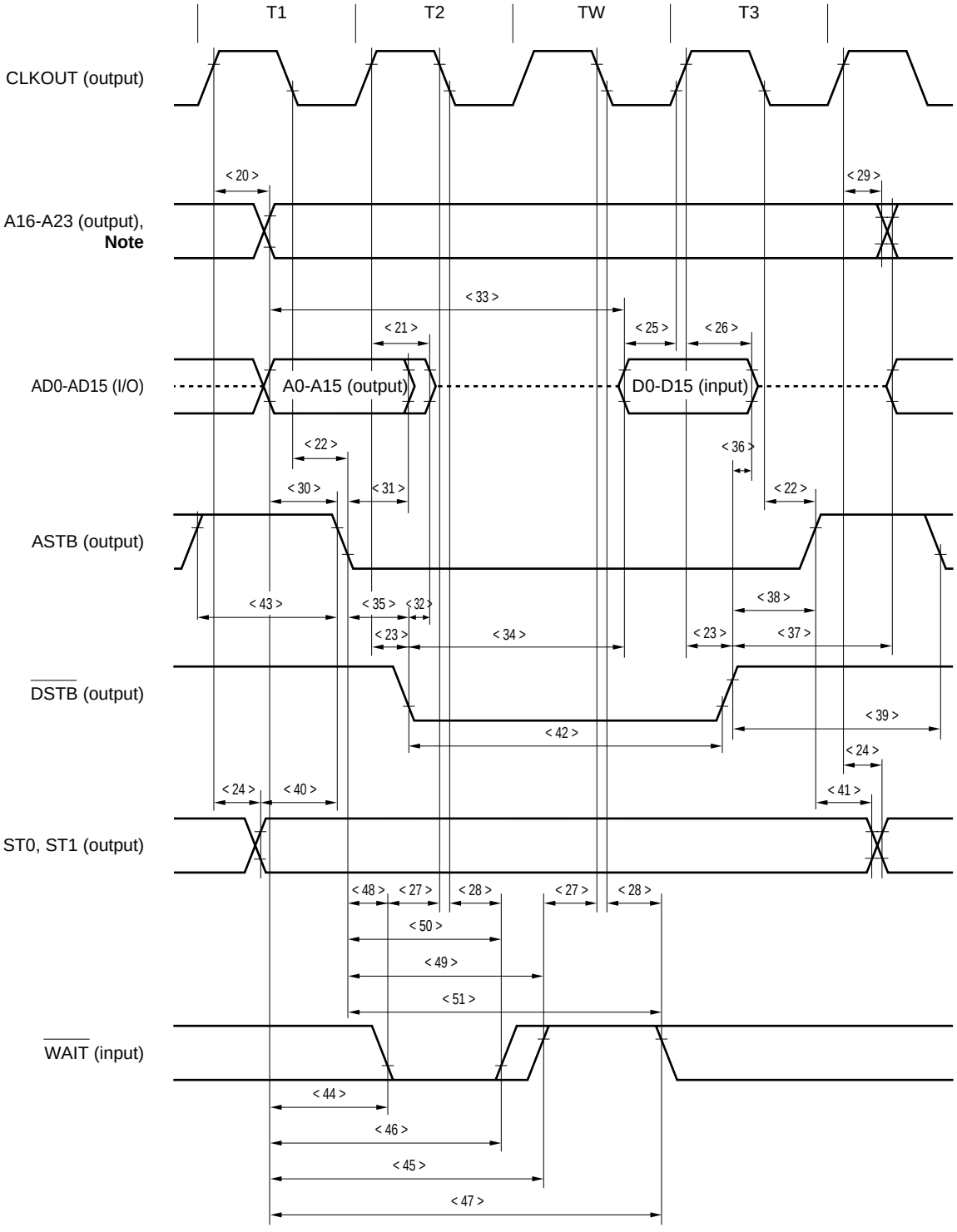
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

3. i indicates the number of idle states (0 or 1) t be inserted in the read cycle.

4. Be sure to observe at least one of data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read Timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

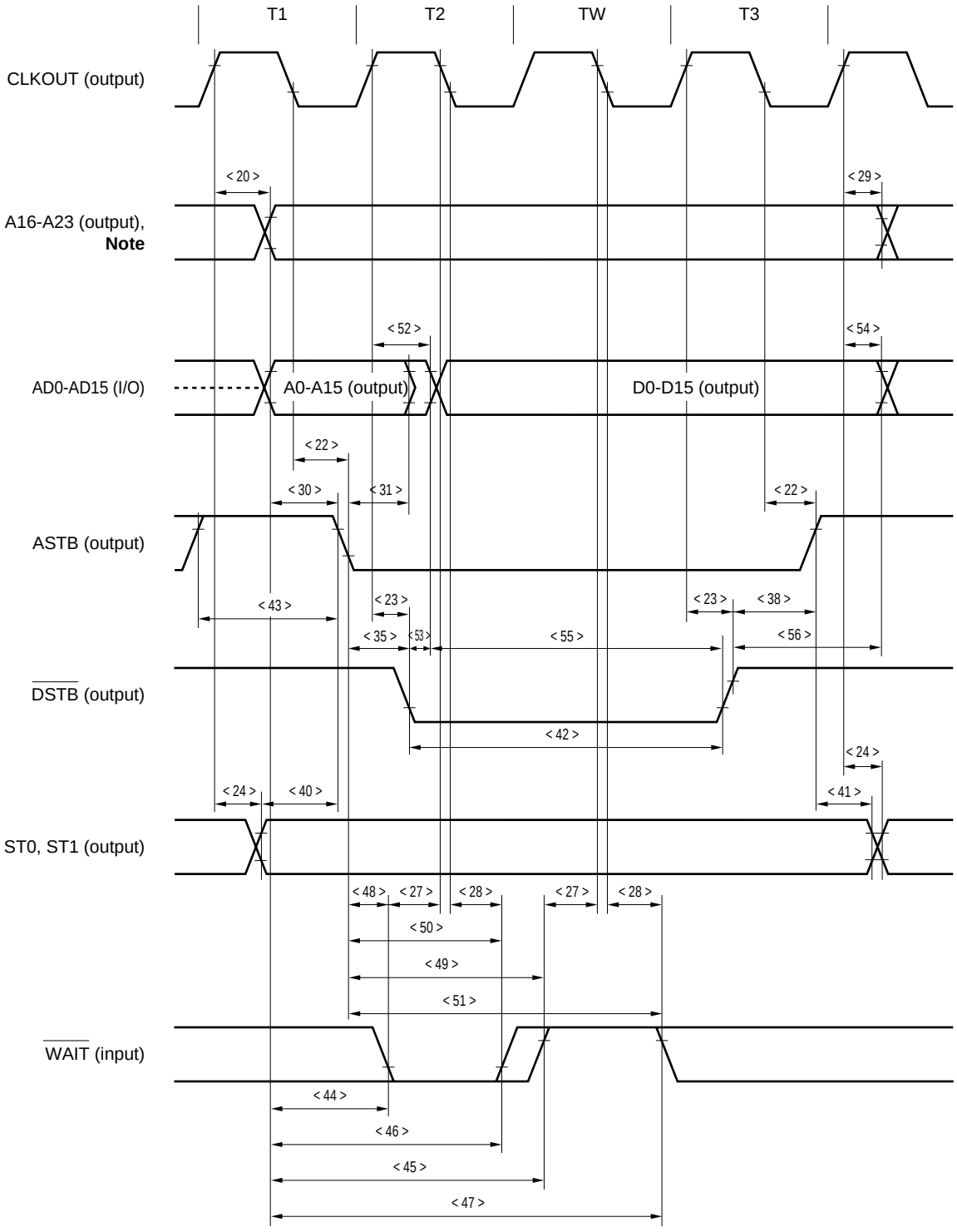
(6) Write timing (1/2)

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	20	3	20	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	15	3	15	ns
CLKOUT ↑→ $\overline{\text{DSTB}}$ delay time	<23>	t_{DKD}		3	15	3	15	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	15	3	15	ns
$\overline{\text{WAIT}}$ setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		5		5		ns
$\overline{\text{WAIT}}$ hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		5		5		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 10		0.5 T – 10		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 10		0.5 T – 10		ns
ASTB ↓→ $\overline{\text{DSTB}}$ ↓ delay time	<35>	t_{DSTD}		0.5 T – 10		0.5 T – 10		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 10		0.5 T – 10		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 10		0.5 T – 10		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 10		0.5 T – 10		ns
$\overline{\text{DSTB}}$ width, low	<42>	t_{WDL}		(1 + n) T – 10		(1 + n) T – 10		ns
ASTB width, high	<43>	t_{WSTH}		T – 10		T – 10		ns
$\overline{\text{WAIT}}$ setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 20		1.5 T – 20	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 20		(1.5 + n) T – 20	ns
$\overline{\text{WAIT}}$ hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		(1.5 + n) T		ns
$\overline{\text{WAIT}}$ setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 15		T – 15	ns
	<49>	t_{SSTWT2}			(1 + n) T – 15		(1 + n) T – 15	ns
$\overline{\text{WAIT}}$ hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		(1 + n) T		ns
CLKOUT ↑→ data output delay time	<52>	t_{DKOD}			20		20	ns
$\overline{\text{DSTB}}$ ↓→ data output delay time	<53>	t_{DDOD}			10		10	ns
Data output hold time (vs. CLKOUT ↑)	<54>	t_{HKOD}		0		0		ns
Data output setup time (vs. $\overline{\text{DSTB}}$ ↑)	<55>	t_{SODD}		(1 + n) T – 15		(1 + n) T – 15		ns
Data output hold time (vs. $\overline{\text{DSTB}}$ ↑)	<56>	t_{HDOD}		T – 10		T – 10		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

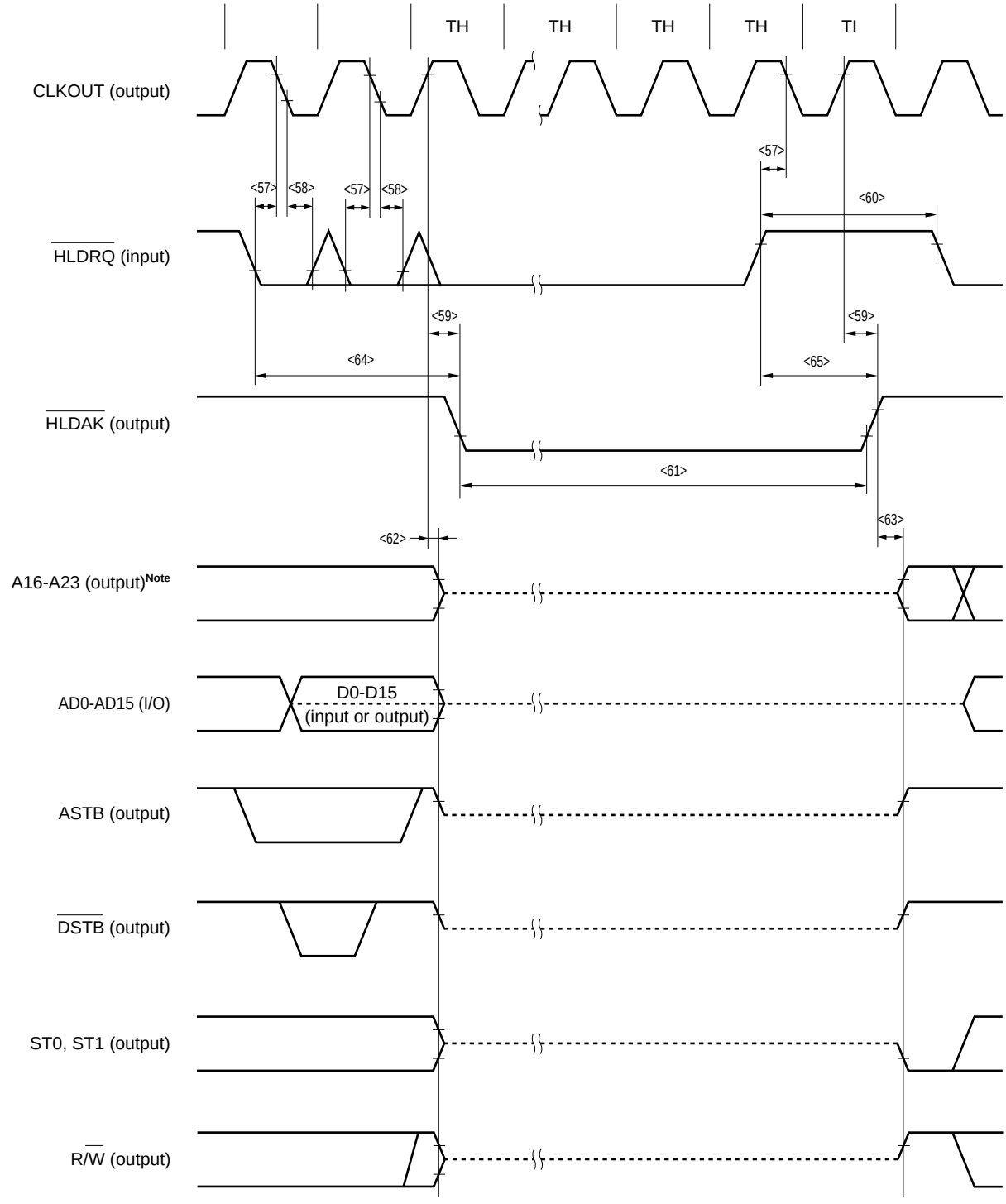
(7) Bus hold timing (1/2)

	Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
					MIN.	MAX.	MIN.	MAX.	
	$\overline{\text{HLDRQ}}$ setup time (vs. CLKOUT ↓)	<57>	t_{SHOK}		5		5		ns
	$\overline{\text{HLDRQ}}$ hold time (vs. CLKOUT ↓)	<58>	t_{HKHQ}		5		5		ns
	CLKOUT ↑→ $\overline{\text{HLDAK}}$ delay time	<59>	t_{DKHA}			20		20	ns
	$\overline{\text{HLDRQ}}$ width, high	<60>	t_{WHQH}		T + 10		T + 10		ns
	$\overline{\text{HLDAK}}$ width, low	<61>	t_{WHAL}		T – 10		T – 10		ns
★	CLKOUT ↑→ bus float delay time	<62>	t_{DKF}			20		20	ns
	$\overline{\text{HLDAK}}$ ↑→ bus output delay time	<63>	t_{DHAC}		–3		–3		ns
	$\overline{\text{HLDRQ}}$ ↓→ $\overline{\text{HLDAK}}$ ↓ delay time	<64>	t_{DHQHA1}			(2 n + 7.5) T + 20		(2 n + 7.5) T + 20	ns
	$\overline{\text{HLDRQ}}$ ↑→ $\overline{\text{HLDAK}}$ ↑ delay time	<65>	t_{DHQHA2}		0.5 T	1.5 T + 20	0.5 T	1.5 T + 20	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(7) Bus hold timing (2/2)



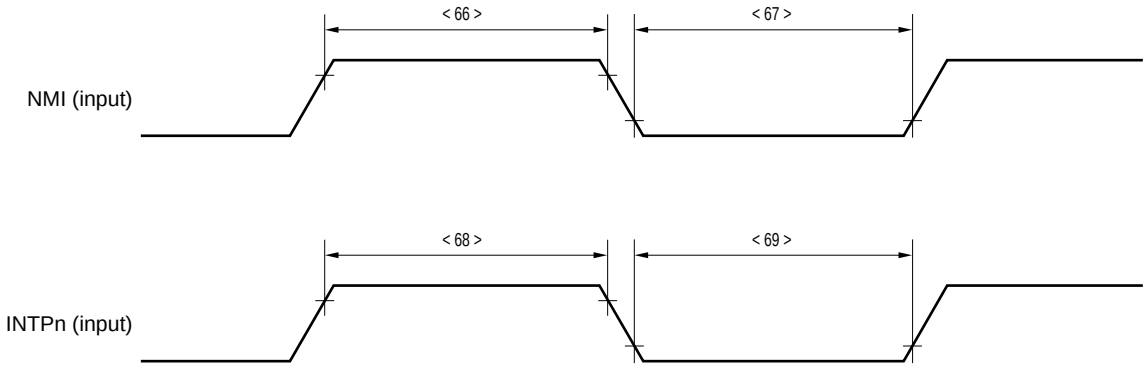
★ **Note** UBEN (output) and LBEN (output)

Remark The broken line indicates the high-impedance state.

(8) Interrupt timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
NMI width, high	<66>	t_{WNIH}		500		500		ns
NMI width, low	<67>	t_{WNIL}		500		500		ns
INTPn width, high	<68>	t_{WITH}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		3 T + 10		ns
INTPn width, low	<69>	t_{WITL}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		3 T + 10		ns

Remark T = t_{CYK}



Remark n = 00, 01, 02, 03, 10, 11, 12, 13

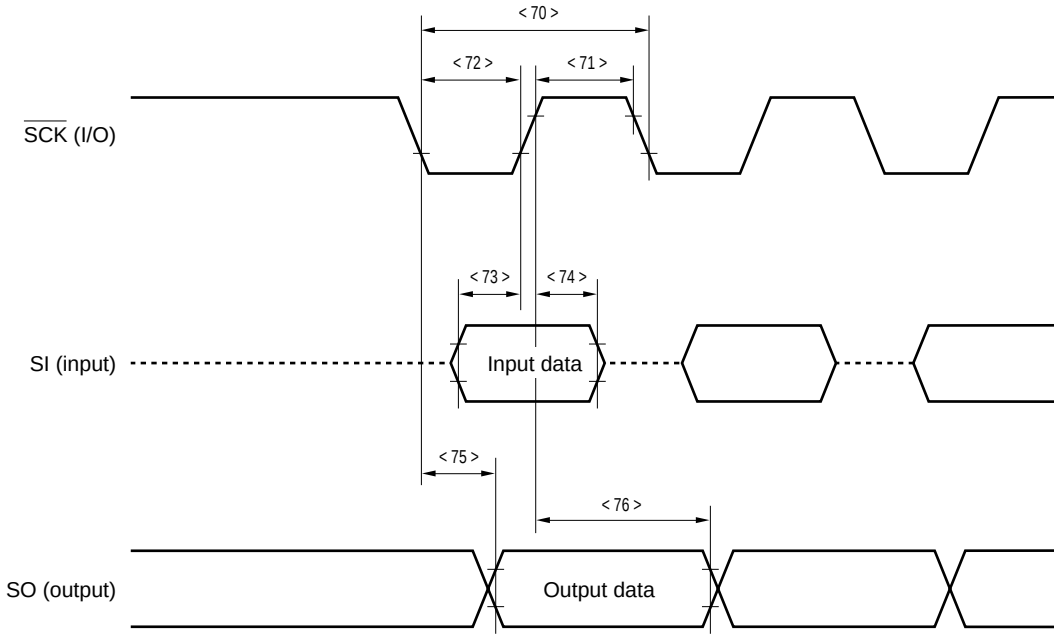
(9) CSI timing

(a) Master mode

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{SCK}$ cycle	<70>	t_{CYSK}	Output	160		120		ns
$\overline{SCK}$ width, high	<71>	t_{WSKH}	Output	0.5 t_{CYSK} – 20		0.5 t_{CYSK} – 20		ns
$\overline{SCK}$ width, low	<72>	t_{WSKL}	Output	0.5 t_{CYSK} – 20		0.5 t_{CYSK} – 20		ns
SI setup time (vs. $\overline{SCK}$ ↑)	<73>	t_{SSISK}		30		30		ns
SI hold time (vs. $\overline{SCK}$ ↑)	<74>	t_{HSKSI}		0		0		ns
SO output delay time (vs. $\overline{SCK}$ ↓)	<75>	t_{DSKSO}			18		18	ns
SO output hold time (vs. $\overline{SCK}$ ↑)	<76>	t_{HSKSO}		0.5 t_{CYSK} – 5		0.5 t_{CYSK} – 5		ns

(b) Slave mode

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
$\overline{SCK}$ cycle	<70>	t_{CYSK}	Input	160		120		ns
$\overline{SCK}$ width, high	<71>	t_{WSKH}	Input	50		30		ns
$\overline{SCK}$ width, low	<72>	t_{WSKL}	Input	50		30		ns
SI setup time (vs. $\overline{SCK}$ ↑)	<73>	t_{SSISK}		10		10		ns
SI hold time (vs. $\overline{SCK}$ ↑)	<74>	t_{HSKSI}		10		10		ns
SO output delay time (vs. $\overline{SCK}$ ↓)	<75>	t_{DSKSO}			30		30	ns
SO output hold time (vs. $\overline{SCK}$ ↑)	<76>	t_{HSKSO}		t_{WSKH}		t_{WSKH}		ns

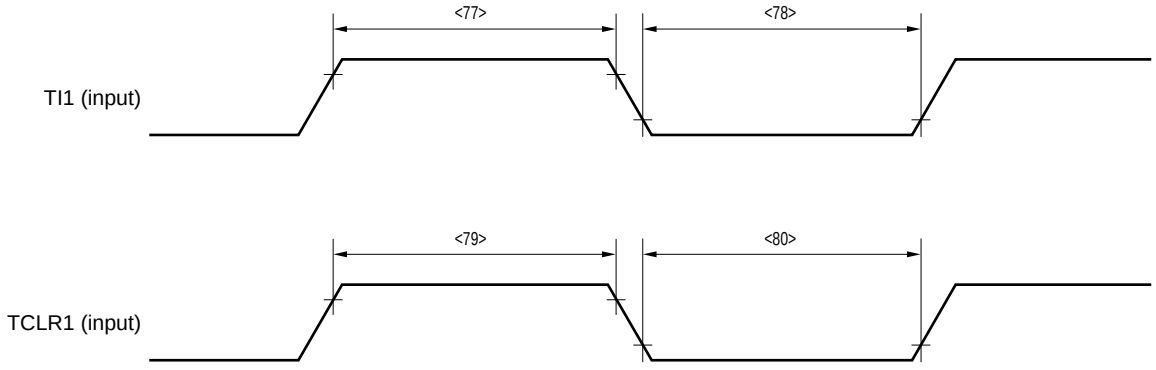


Remark The broken line indicates the high-impedance state.

(10) RPU timing

Parameter	Symbol		Condition	μPD70P3000-25		μPD70P3000-33		Unit
				MIN.	MAX.	MIN.	MAX.	
TI1 width, high	<77>	t_{WTIH}		3 T + 10		3 T + 10		ns
TI1 width, low	<78>	t_{WTIL}		3 T + 10		3 T + 10		ns
TCLR1 width, high	<79>	t_{WTCH}		3 T + 10		3 T + 10		ns
TCLR1 width, low	<80>	t_{WTCL}		3 T + 10		3 T + 10		ns

Remark T = t_{CYK}



6.1.2 When V_{DD} = 3.0 to 3.6 V

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	–0.5 to +7.0	V
	CV_{DD}	CV_{DD} pin	–0.5 to +7.0	V
	DV_{SS}	CV_{SS} pin	–0.5 to +0.5	V
Input voltage	V_{I1}	Except X1 pin, V_{DD} = 3.0 to 3.6 V	–0.5 to V_{DD} + 0.3	V
	V_{I2}	V_{PP} pin in PROM programming mode, V_{DD} = 3.0 to 3.6 V	–0.5 to +13.5	V
Clock input voltage	V_X	X1 pin, V_{DD} = 3.0 to 3.6 V	–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	–4.0	mA
		Total of all pins	–100	mA
Output voltage	V_O	V_{DD} = 3.0 to 3.6 V	–0.5 to V_{DD} + 0.3	V
Operating ambient temperature	T_A		–20 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to V_{DD}, V_{CC}, or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

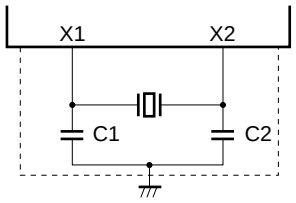
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz			15	pF
I/O capacitance	C_{IO}	Pins other than tested pin: 0 V			15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 12 MHz	–20 to +70 °C	3.0 to 3.6 V
PLL mode	Self oscillation frequency to 12 MHz	–20 to +70 °C	3.0 to 3.6 V

Recommended Oscillation Circuit

(a) Ceramic resonator connection (T_A = –40 to + 85 °C)



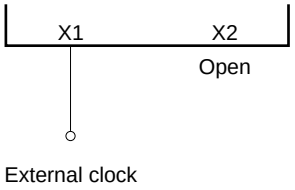
Manufacturer	Part Number	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constants		Oscillation Voltage Renge		Oscillation Stabilization Time (MAX.) T_{OST} (ms)
			C1 (pF)	C2 (pF)	MIN. (V)	MAX. (V)	
TDK Corp	FCR2.0MC3	2.0	Provided	Provided	3.0	3.6	0.26
	CCR3.2MC3	3.2	Provided	Provided	3.0	3.6	0.62
Murata Mfg. Co., Ltd.	CSA2.00MG	2.0	30	30	2.7	3.6	0.24
	CST2.00MG	2.0	Provided	Provided	2.7	3.6	0.24
	CSA2.70MG	2.7	30	30	2.7	3.6	0.16
	CST2.70MGW	2.7	Provided	Provided	2.7	3.6	0.16
	CSA3.20MG	3.2	30	30	2.7	3.6	0.13
	CST3.20MGW	3.2	Provided	Provided	2.7	3.6	0.13

Cautions 1. Connect the oscillation circuit as closely to X2 pin as possible.

2. Do not route any other signal lines in the range indicated by the broken line in the above figure.

3. Thoroughly evaluate the matching between the μPD70P3000 and resonator.

(b) External clock input



Caution Input CMOS level voltage to the X1 pin.

DC Characteristics (T_A = –20 to +70 °C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V)

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}	Except X1 and **Note**	0.7 V_{DD}		V_{DD}	V
			Note	0.8 V_{DD}		V_{DD}	V
Input voltage, low		V_{IL}	Except X1 and **Note**	0		0.2 V_{DD}	V
			Note	0		0.2 V_{DD}	V
X1 clock input voltage, high		V_{XH}	Direct mode	0.8 V_{DD}		V_{DD}	V
			PLL mode	0.8 V_{DD}		V_{DD}	V
X1 clock input voltage, low		V_{XL}	Direct mode	0		0.6	V
			PLL mode	0		0.6	V
Schmitt trigger input threshold voltage		V_T^+	**Note**, rising		3.0		V
		V_T^-	**Note**, falling		2.0		V
Schmitt trigger input hysteresis width		$V_T^+ - V_T^-$	**Note**	0.5			V
Output voltage, high		V_{OH}	I_{OH} = –2.5 mA	0.7 V_{DD}			V
			I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low		V_{OL}	I_{OC} = 2.5 mA			0.45	V
Input leakage current, high		I_{LIH}	$V_I = V_{DD}$			10	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			–10	μA
Output leakage current, high		I_{LOH}	$V_O = V_{DD}$			10	μA
Output leakage current, low		I_{LOL}	V_O = 0 V			–10	μA
Supply current	Operating	I_{DD1}	Direct mode		$1.0 \times \phi + 9.5$	$1.5 \times \phi + 10$	mA
			PLL mode		$1.1 \times \phi + 11$	$1.8 \times \phi + 12$	mA
	In HALT mode	I_{DD2}	Direct mode		$0.3 \times \phi + 2$	$0.5 \times \phi + 6.5$	mA
			PLL mode		$0.4 \times \phi + 3.5$	$0.6 \times \phi + 8.5$	mA
	In IDLE mode	I_{DD3}	Direct mode		$5.3 \times \phi + 200$	$6.5 \times \phi + 325$	μA
			PLL mode		$0.07 \times \phi + 1.5$	$0.15 \times \phi + 2$	mA
	In STOP mode	I_{DD4}	–20 °C ≤ T_A ≤ 50 °C		1	40	μA
			50 °C < T_A ≤ 70 °C			200	μA

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL

Remarks 1. TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 3.3 V.

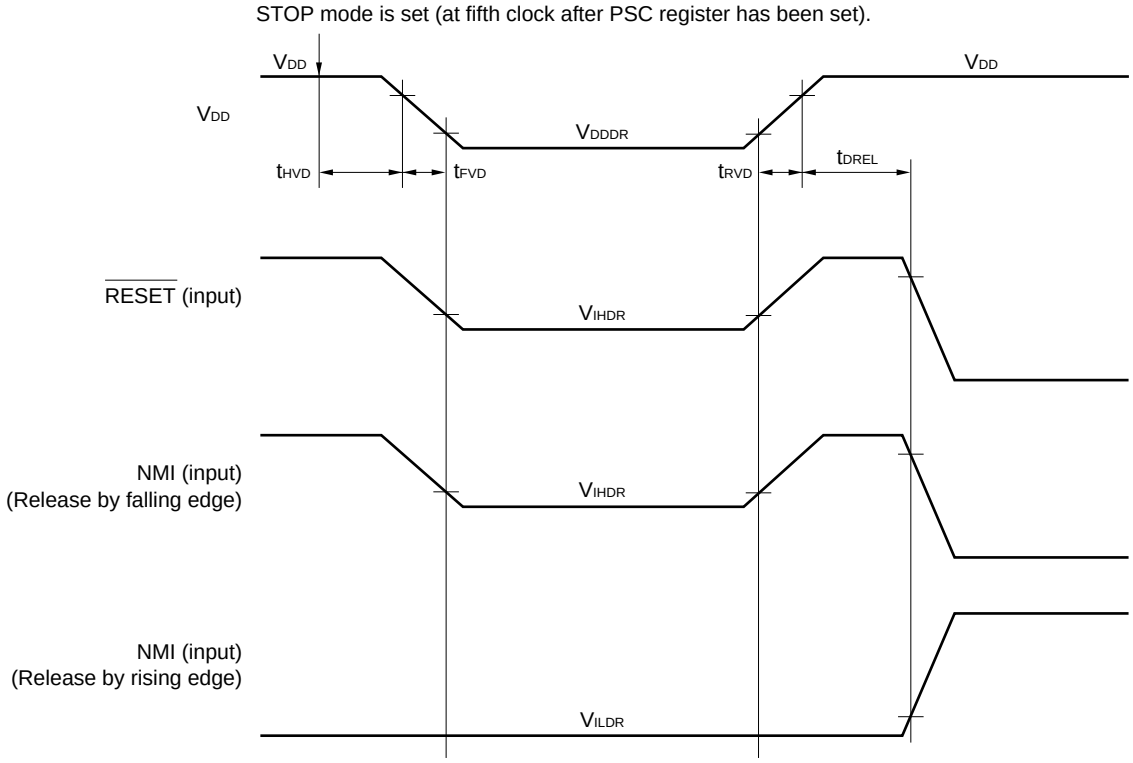
2. ϕ : Internal operating clock frequency

Data Retention Characteristics (T_A = –20 to +70 °C)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode		1.5		3.6	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$	–20 °C ≤ T_A ≤ +50 °C		0.2 V_{DDDR}	40	μA
			50 °C < T_A ≤ 70 °C		0.2 V_{DDDR}	200	μA
Supply voltage rise time	t_{RVD}			200			μs
Supply voltage fall time	t_{FVD}			200			μs
Supply voltage hold time (vs. STOP mode setting)	t_{HVD}			0			ms
STOP mode release signal input time	t_{DREL}			0			ns
Data hold input voltage, high	V_{IHDR}	**Note**		0.9 V_{DDDR}		V_{DDDR}	V
Data hold input voltage, low	V_{ILDR}	**Note**		0		0.1 V_{DDDR}	V

Note $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INT03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1

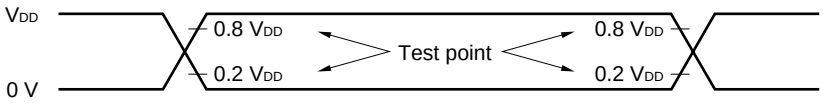
Remark TYP. value is a value for your reference at T_A = 25 °C and V_{DD} = 3.3 V.



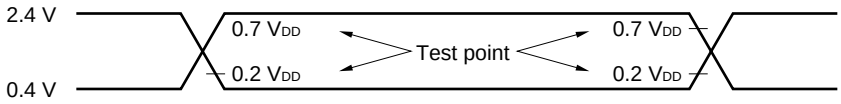
AC Characteristics (T_A = –20 to +70 °C, V_{DD} = 3.0 to 3.6 V, V_{SS} = 0 V)

AC test input wave

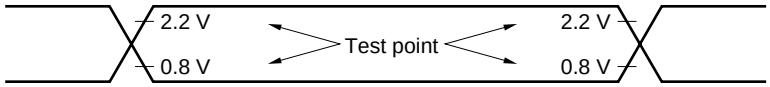
(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/$\overline{\text{SCK}}$, P36, P37, MODE0, MODE1, CKSEL, X1



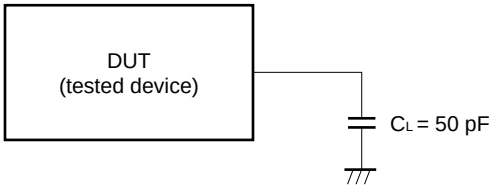
(b) Other than (a)



AC test output test point



Load condition



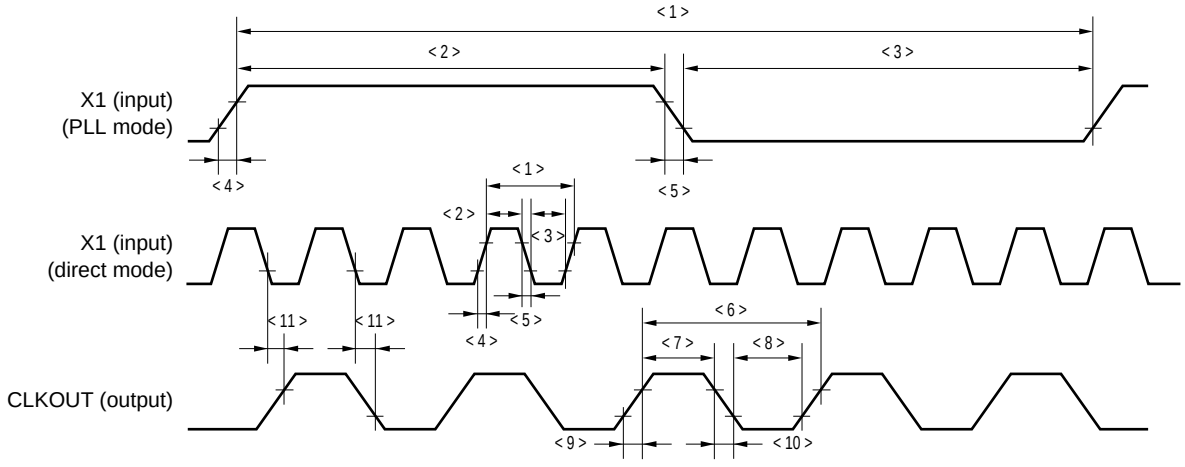
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, decrease the load capacitance of this device to less then 50 pF by using a buffer.

(1) Clock timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	41	DC	ns
			PLL mode	416	500	ns
X1 input width, high	<2>	t_{WXH}	Direct mode	7		ns
			PLL mode	170		ns
X1 input width, low	<3>	t_{WXL}	Direct mode	7		ns
			PLL mode	170		ns
X1 input rise time	<4>	t_{XR}	Direct mode		7	ns
			PLL mode		15	ns
X1 input fall time	<5>	t_{XF}	Direct mode		7	ns
			PLL mode		15	ns
CPU operating frequency	—	ϕ		0	12	MHz
CLKOUT output cycle	<6>	t_{CYK}		82	DC	ns
CLKOUT width, high	<7>	t_{WKH}		0.5 T – 15		ns
CLKOUT width, low	<8>	t_{WKL}		0.5 T – 15		ns
CLKOUT rise time	<9>	t_{XR}			15	ns
CLKOUT fall time	<10>	t_{XF}			15	ns
X1 ↓→ CLKOUT delay time	<11>	t_{DXK}	Direct mode	3	30	ns

Remark T = t_{CYK}

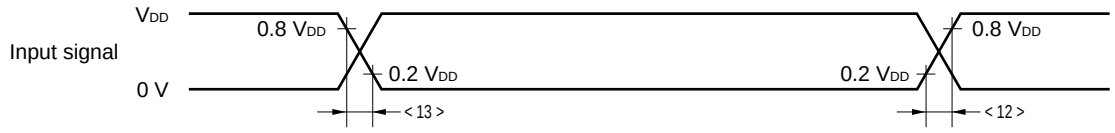
Parameter	Symbol		Condition	TYP.	Unit
Self-running oscillation frequency	—	ϕ_P	PLL mode	2.8	MHz



(2) Input waveform

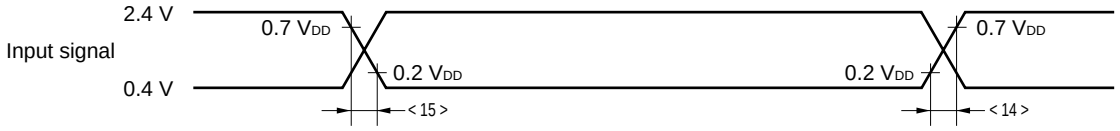
(a) $\overline{\text{RESET}}$, P02/TCLR1, P03/TI1, P04/INTP10 through P07/INTP13, P20/NMI, P21/INTP00 through P24/INTP03, P26, P27, P31/SI, P32/SCK, P36, P37, MODE0, MODE1, CKSEL, X1

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<12>	t_{IR2}			20	ns
Input fall time	<13>	t_{IF2}			20	ns



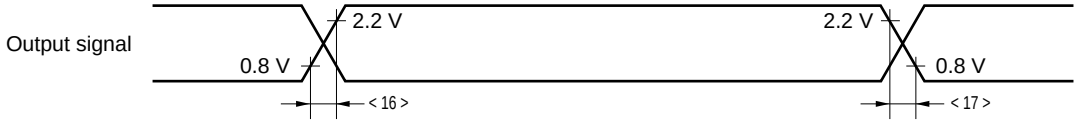
(b) Other than (a)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
Input rise time	<14>	t_{IR1}			10	ns
Input fall time	<15>	t_{IF1}			10	ns



(3) Output waveform (other than CLKOUT)

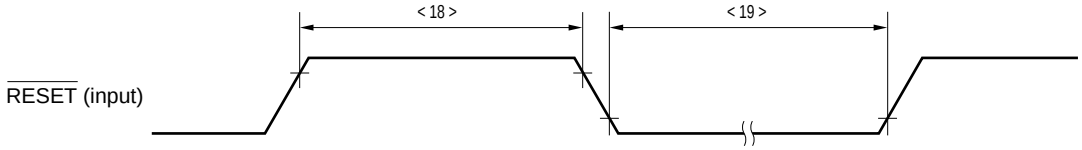
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<16>	t_{OR}			20	ns
Output fall time	<17>	t_{OF}			20	ns



(4) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ width, high	<18>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ width, low	<19>	t_{WRSL}	On power application, or on releasing STOP mode	500 + T_{OST}		ns
			Except on power application, or except on releasing STOP mode	500		ns

Remark T_{OST}: oscillation stabilization time



[MEMO]

(5) Read timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	32	ns
CLKOUT ↑→ address float delay time	<21>	t_{FKA}		3	32	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	32	ns
CLKOUT ↓→ $\overline{\text{DSTB}}$ delay time	<23>	t_{DKD}		3	32	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	32	ns
Data input setup time (vs. CLKOUT ↑)	<25>	t_{SIDK}		5		ns
Data input hold time (vs. CLKOUT ↑)	<26>	t_{HKID}		5		ns
$\overline{\text{WAIT}}$ setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		7		ns
$\overline{\text{WAIT}}$ hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		7		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 25		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 25		ns
$\overline{\text{DSTB}}$ ↓→ address float delay time	<32>	t_{FDA}			0	ns
Data input setup time (vs. address)	<33>	t_{SAID}			(2 + n) T – 45	ns
Data input setup time (vs. $\overline{\text{DSTB}}$ ↓)	<34>	t_{SDID}			(1 + n) T – 35	ns
ASTB ↓→ $\overline{\text{DSTB}}$ ↓ delay time	<35>	t_{DSTD}		0.5 T – 15		ns
Data input hold time (vs. $\overline{\text{DSTB}}$ ↑)	<36>	t_{HDID}		0		ns
$\overline{\text{DSTB}}$ ↑→ address output delay time	<37>	t_{DDA}		(1 + i) T		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 15		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↓ delay time	<39>	t_{DDSTL}		(1.5 + i) T – 15		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 15		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 20		ns
$\overline{\text{DSTB}}$ width, low	<42>	t_{WDL}		(1 + n) T – 15		ns
ASTB width, high	<43>	t_{WSTH}		T – 20		ns
$\overline{\text{WAIT}}$ setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 50	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 50	ns
$\overline{\text{WAIT}}$ hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		ns
$\overline{\text{WAIT}}$ setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 35	ns
	<49>	t_{SSTWT2}			(1 + n) T – 35	ns
$\overline{\text{WAIT}}$ hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		ns

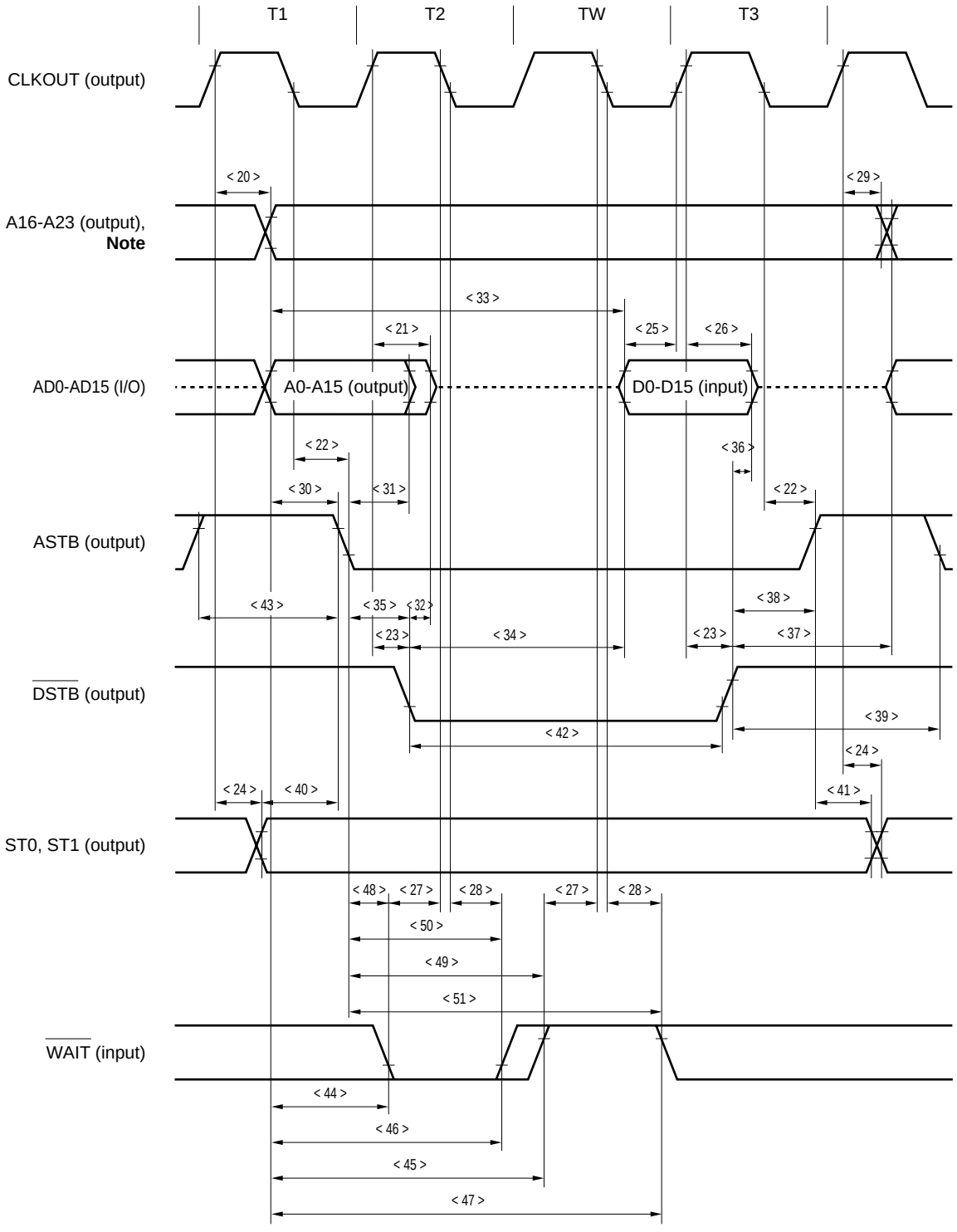
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

3. i indicates the number of idle states (0 or 1) t be inserted in the read cycle.

4. Be sure to observe at least one of data input hold times t_{HKID} (<26>) and t_{HDID} (<36>).

(5) Read Timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

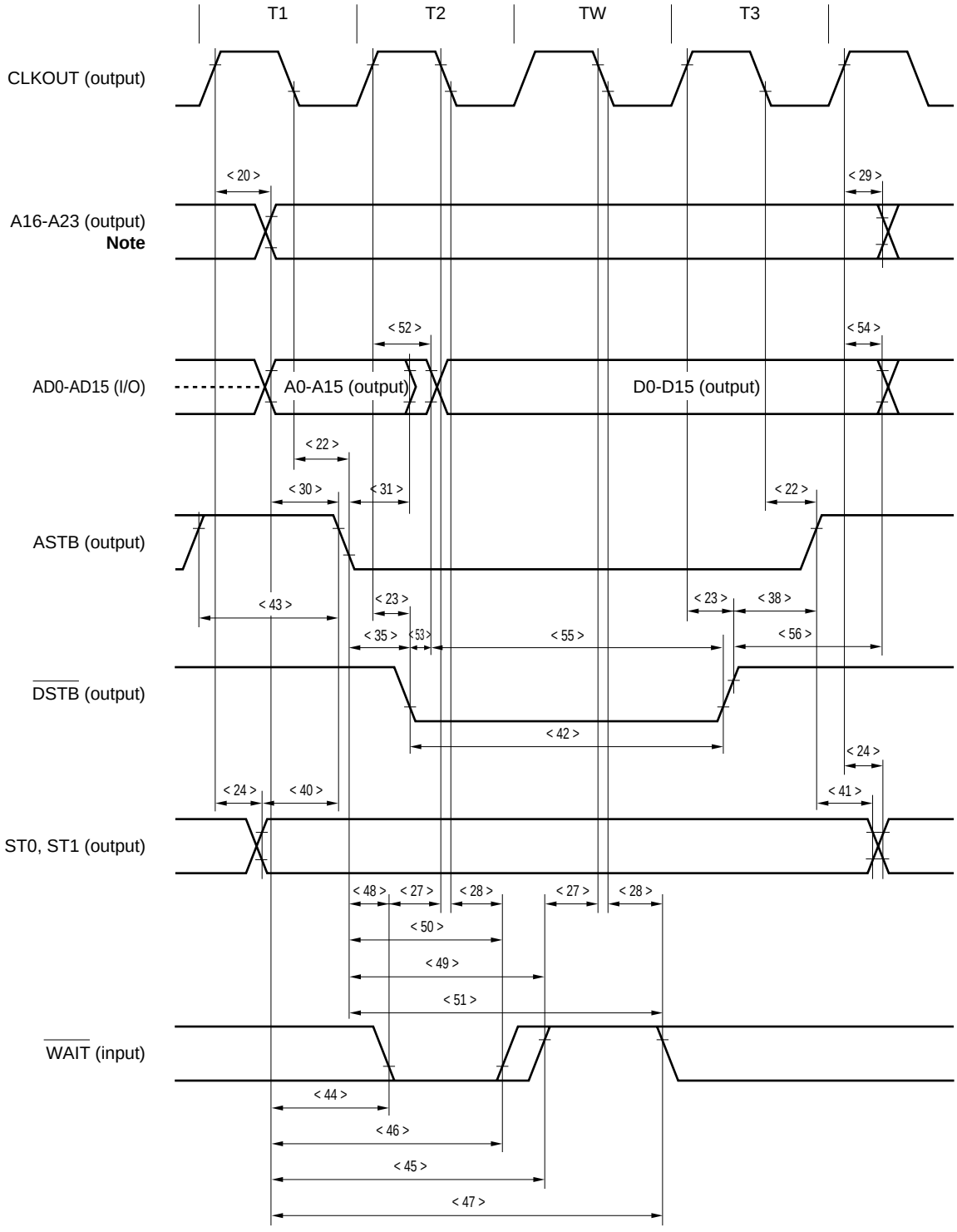
(6) Write timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<20>	t_{DKA}		3	32	ns
CLKOUT ↓→ ASTB delay time	<22>	t_{DKST}		3	32	ns
CLKOUT ↑→ $\overline{\text{DSTB}}$ delay time	<23>	t_{DKD}		3	32	ns
CLKOUT ↑→ status delay time	<24>	t_{DKS}		3	32	ns
$\overline{\text{WAIT}}$ setup time (vs. CLKOUT ↓)	<27>	t_{SWTK}		7		ns
$\overline{\text{WAIT}}$ hold time (vs. CLKOUT ↓)	<28>	t_{HKWT}		7		ns
Address hold time (vs. CLKOUT ↑)	<29>	t_{HKA}		0		ns
Address setup time (vs. ASTB ↓)	<30>	t_{SAST}		0.5 T – 25		ns
Address hold time (vs. ASTB ↓)	<31>	t_{HSTA}		0.5 T – 15		ns
ASTB ↓→ $\overline{\text{DSTB}}$ ↓ delay time	<35>	t_{DSTD}		0.5 T – 15		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↑ delay time	<38>	t_{DDSTH}		0.5 T – 15		ns
Status setup time (vs. ASTB ↓)	<40>	t_{SSST}		0.5 T – 15		ns
Status hold time (vs. ASTB ↑)	<41>	t_{HSTS}		0.5 T – 20		ns
$\overline{\text{DSTB}}$ width, low	<42>	t_{WDL}		(1 + n) T – 15		ns
ASTB width, high	<43>	t_{WSTH}		T – 20		ns
$\overline{\text{WAIT}}$ setup time (vs. address)	<44>	t_{SAWT1}	n ≥ 1		1.5 T – 50	ns
	<45>	t_{SAWT2}			(1.5 + n) T – 50	ns
$\overline{\text{WAIT}}$ hold time (vs. address)	<46>	t_{HAWT1}	n ≥ 1	(0.5 + n) T		ns
	<47>	t_{HAWT2}		(1.5 + n) T		ns
$\overline{\text{WAIT}}$ setup time (vs. ASTB ↓)	<48>	t_{SSTWT1}	n ≥ 1		T – 35	ns
	<49>	t_{SSTWT2}			(1 + n) T – 35	ns
$\overline{\text{WAIT}}$ hold time (vs. ASTB ↓)	<50>	t_{HSTWT1}	n ≥ 1	nT		ns
	<51>	t_{HSTWT2}		(1 + n) T		ns
CLKOUT ↑→ data output delay time	<52>	t_{DKOD}			32	ns
$\overline{\text{DSTB}}$ ↓→ data output delay time	<53>	t_{DDOD}			20	ns
Data output hold time (vs. CLKOUT ↑)	<54>	t_{HKOD}		0		ns
Data output setup time (vs. $\overline{\text{DSTB}}$ ↑)	<55>	t_{SODD}		(1 + n) T – 30		ns
Data output hold time (vs. $\overline{\text{DSTB}}$ ↑)	<56>	t_{HDOD}		T – 15		ns

Remarks 1. $T = t_{CYK}$

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Write timing (2/2): 1 wait



Note R/$\overline{W}$ (output), $\overline{UBEN}$ (output), $\overline{LBEN}$ (output)

Remark The broken line indicates the high-impedance state.

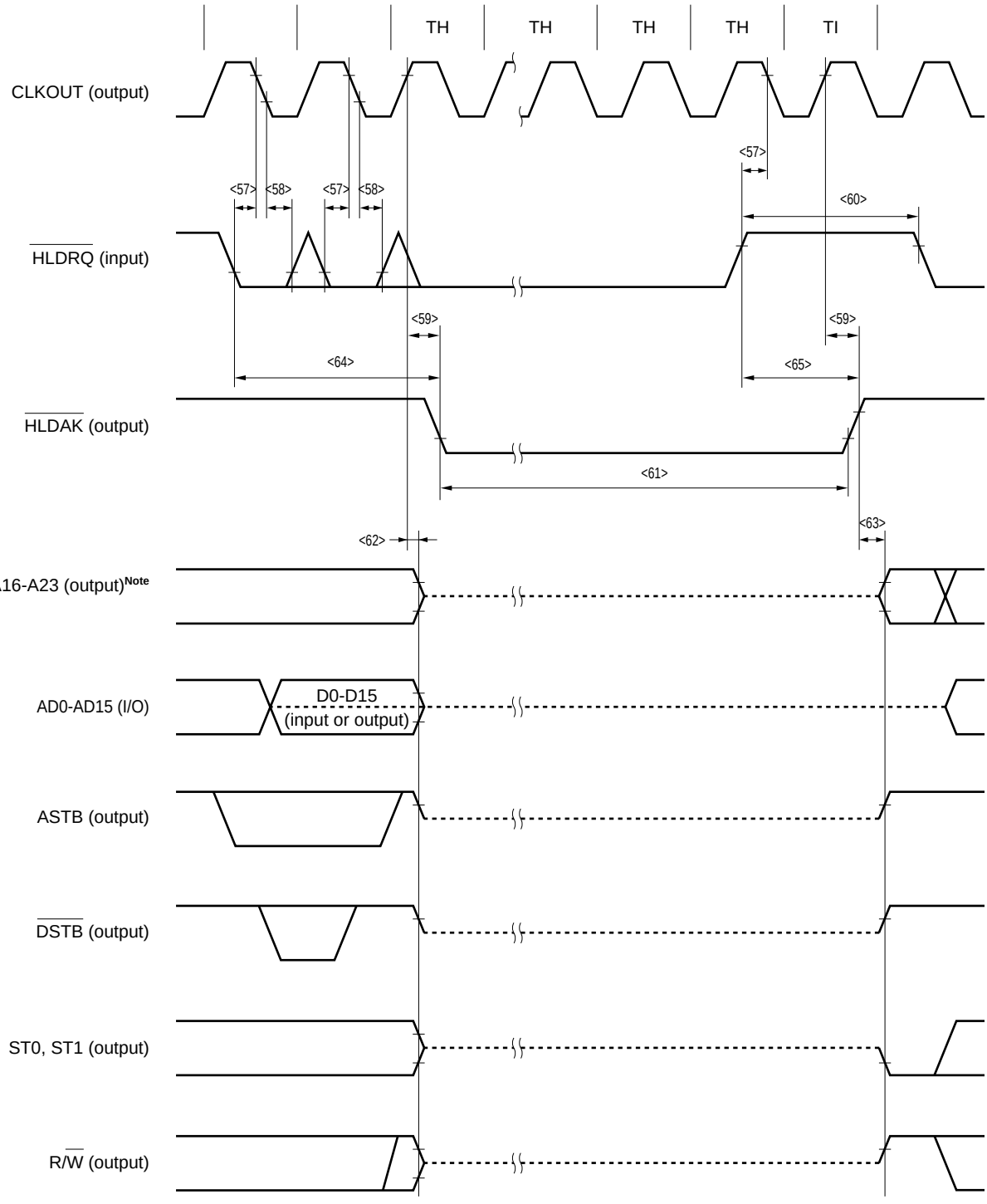
(7) Bus hold timing (1/2)

	Parameter	Symbol		Condition	MIN.	MAX.	Unit
	$\overline{\text{HLDRQ}}$ setup time (vs. CLKOUT ↓)	<57>	t_{SHOK}		7		ns
	$\overline{\text{HLDRQ}}$ hold time (vs. CLKOUT ↓)	<58>	t_{HKHQ}		7		ns
	CLKOUT ↑→ $\overline{\text{HLDAK}}$ delay time	<59>	t_{DKHA}			32	ns
	$\overline{\text{HLDRQ}}$ width, high	<60>	t_{WHQH}		T + 15		ns
	$\overline{\text{HLDAK}}$ width, low	<61>	t_{WHAL}		T – 15		ns
★	CLKOUT ↑→ bus float delay time	<62>	t_{DKF}			32	ns
	$\overline{\text{HLDAK}}$ ↑→ bus output delay time	<63>	t_{DHAC}		–5		ns
	$\overline{\text{HLDRQ}}$ ↓→ $\overline{\text{HLDAK}}$ ↓ delay time	<64>	t_{DHQHA1}			(2 n + 7.5) T + 40	ns
	$\overline{\text{HLDRQ}}$ ↑→ $\overline{\text{HLDAK}}$ ↑ delay time	<65>	t_{DHQHA2}		0.5 T	1.5 T + 40	ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(7) Bus hold timing (2/2)



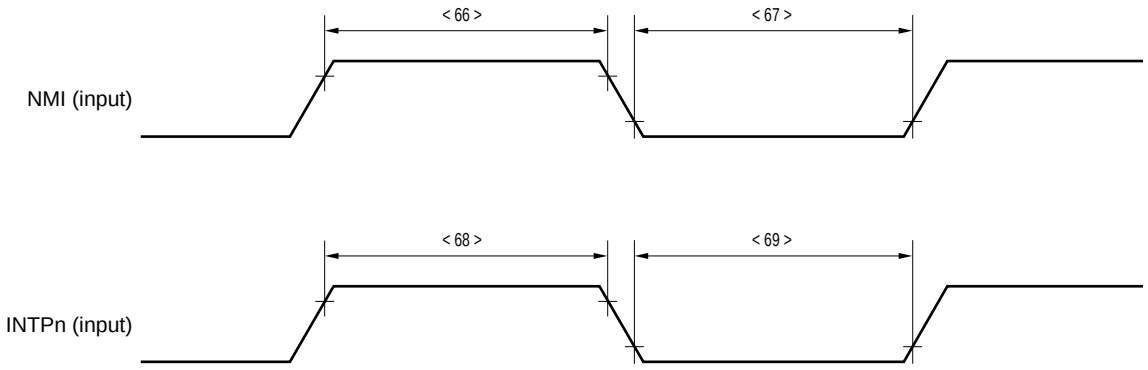
★ **Note** UBEN (output) and LBEN (output)

Remark The broken line indicates the high-impedance state.

(8) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI width, high	<66>	t_{WNIH}		500		ns
NMI width, low	<67>	t_{WNIL}		500		ns
INTPn width, high	<68>	t_{WITH}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		ns
INTPn width, low	<69>	t_{WITL}	n = 00, 01, 02, 03, 10, 11, 12, 13	3 T + 10		ns

Remark T = t_{CYK}



Remark n = 00, 01, 02, 03, 10, 11, 12, 13

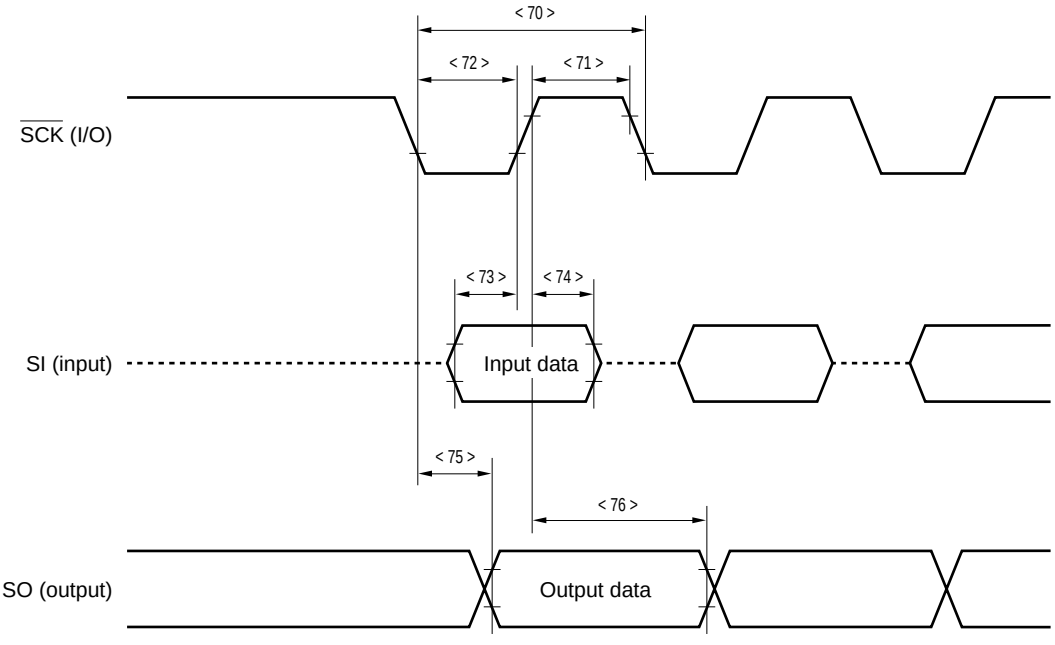
(9) CSI timing

(a) Master mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCK}$ cycle	<70>	t_{CYSK}	Output	330		ns
$\overline{SCK}$ width, high	<71>	t_{WSKH}	Output	0.5 t_{CYSK} – 40		ns
$\overline{SCK}$ width, low	<72>	t_{WSKL}	Output	0.5 t_{CYSK} – 40		ns
SI setup time (vs. $\overline{SCK}$ ↑)	<73>	t_{SSISK}		60		ns
SI hold time (vs. $\overline{SCK}$ ↑)	<74>	t_{HSKSI}		0		ns
SO output delay time (vs. $\overline{SCK}$ ↓)	<75>	t_{DSKSO}			40	ns
SO output hold time (vs. $\overline{SCK}$ ↑)	<76>	t_{HSKSO}		0.5 t_{CYSK} – 15		ns

(b) Slave mode

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCK}$ cycle	<70>	t_{CYSK}	Input	330		ns
$\overline{SCK}$ width, high	<71>	t_{WSKH}	Input	110		ns
$\overline{SCK}$ width, low	<72>	t_{WSKL}	Input	110		ns
SI setup time (vs. $\overline{SCK}$ ↑)	<73>	t_{SSISK}		20		ns
SI hold time (vs. $\overline{SCK}$ ↑)	<74>	t_{HSKSI}		20		ns
SO output delay time (vs. $\overline{SCK}$ ↓)	<75>	t_{DSKSO}			60	ns
SO output hold time (vs. $\overline{SCK}$ ↑)	<76>	t_{HSKSO}		t_{WSKH}		ns

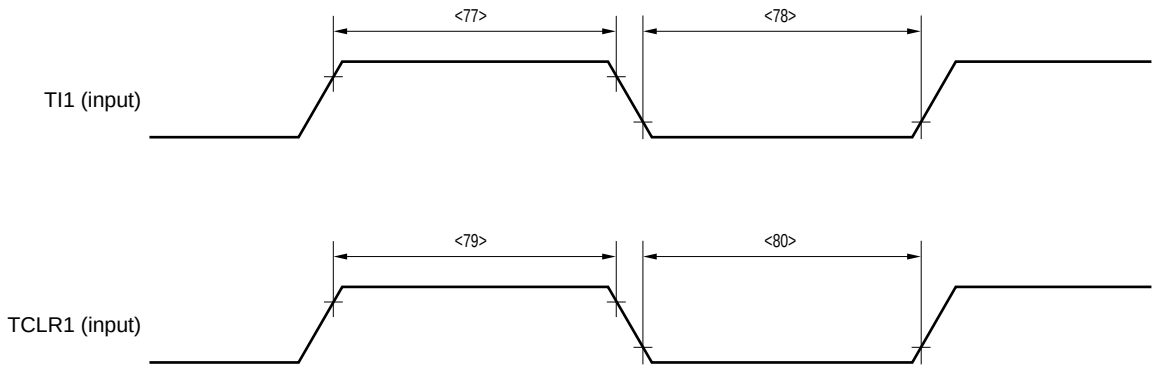


Remark The broken line indicates the high-impedance state.

(10) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TI1 width, high	<77>	t_{WTIH}		3 T + 10		ns
TI1 width, low	<78>	t_{WTIL}		3 T + 10		ns
TCLR1 width, high	<79>	t_{WTCH}		3 T + 10		ns
TCLR1 width, low	<80>	t_{WTCL}		3 T + 10		ns

Remark T = t_{CYK}



6.2 PROM Programming Mode

DC Programming Characteristics

PROM write mode (T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

Parameter	Symbol	Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage, high	V_{OH}	V_{OH}	I_{OH} = –1 mA	V_{DD} – 1.0			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		12.2	12.5	12.8	V
V_{DD} supply voltage	V_{DD}	V_{CC}		6.25	6.5	6.75	V
V_{PP} supply current	I_{PP}	I_{PP}	$\overline{PGM}$ = V_{IL}			50	mA
V_{DD} supply current	I_{DD}	I_{CC}				50	mA

Note Symbol of corresponding μPD27C1001A

PROM read mode (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD} ± 0.6 V)

Parameter	Symbol	Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}	V_{IH}		0.7 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL}	V_{IL}		0		0.3 V_{DD}	V
Output voltage, high	V_{OH1}	V_{OH1}	I_{OH} = –1 mA	V_{DD} – 1.0			V
	V_{OH2}	V_{OH2}	I_{OH} = –100 μA	V_{DD} – 0.5			V
Output voltage, low	V_{OL}	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Input leakage current	I_{LI}	I_{LI}	0 ≤ V_{IN} ≤ V_{DD}	–10		+10	μA
Output leakage current	I_{LO}	I_{LO}	0 ≤ V_{OUT} ≤ V_{DD}, $\overline{OE}$ = V_{IH}	–10		+10	μA
V_{PP} supply voltage	V_{PP}	V_{PP}		V_{DD} – 0.6	V_{DD}	V_{DD} + 0.6	V
V_{DD} supply voltage	V_{DD}	V_{CC}		4.5	5.0	5.5	V
V_{PP} supply current	I_{PP}	I_{PP}	V_{PP} = V_{DD}			100	μA
V_{DD} supply current	I_{DD}	I_{CCA1}	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH}			50	mA

Note Symbol of corresponding μPD27C1001A

AC Programming Characteristics

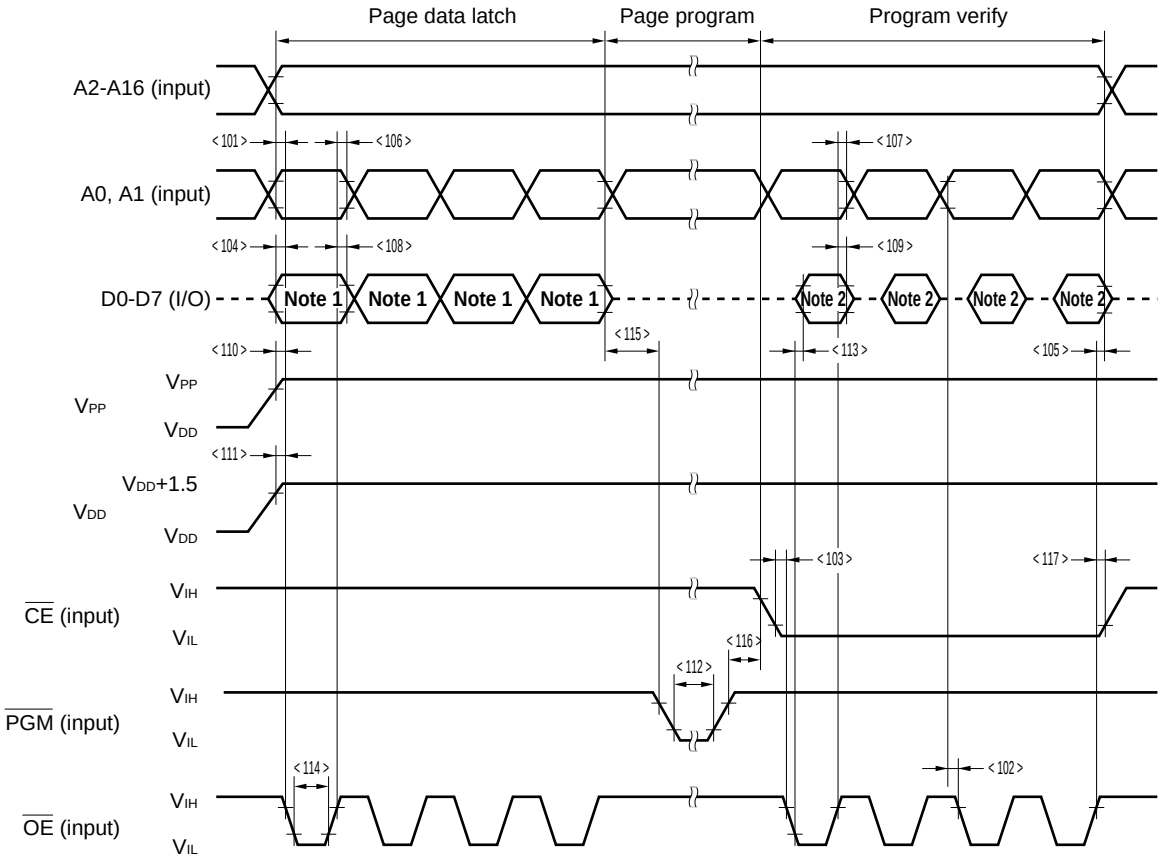
(1) PROM write mode timing (page program mode)

(T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V) (1/2)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (vs. $\overline{OE}$ ↓)	<101>	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	<102>	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (vs. $\overline{OE}$ ↓)	<103>	t_{CES}	t_{CES}		2			μs
Input data setup time (vs. $\overline{OE}$ ↓)	<104>	t_{DS}	t_{DS}		2			μs
Address hold time (vs. $\overline{OE}$ ↑)	<105>	t_{AH}	t_{AH}		2			μs
	<106>	t_{AHL}	t_{AHL}		2			μs
	<107>	t_{AHV}	t_{AHV}		0			μs
Input data hold time (vs. $\overline{OE}$ ↑)	<108>	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑→ data output float delay time	<109>	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (vs. $\overline{OE}$ ↓)	<110>	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (vs. $\overline{OE}$ ↓)	<111>	t_{VDS}	t_{VCS}		1.0			ms
Program pulse width	<112>	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓→ valid data delay time	<113>	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ pulse width in data latch	<114>	t_{LW}	t_{LW}		1			μs
$\overline{PGM}$ setup time	<115>	t_{PGMS}	t_{PGMS}		2			μs
$\overline{CE}$ hold time	<116>	t_{CEH}	t_{CEH}		2			μs
$\overline{OE}$ hold time	<117>	t_{OEH}	t_{OEH}		2			μs

Note Symbol of corresponding μPD27C1001A

(1) PROM write mode timing (page program mode) (2/2)



Notes 1. D0-D7 (input)

2. D0-D7 (output)

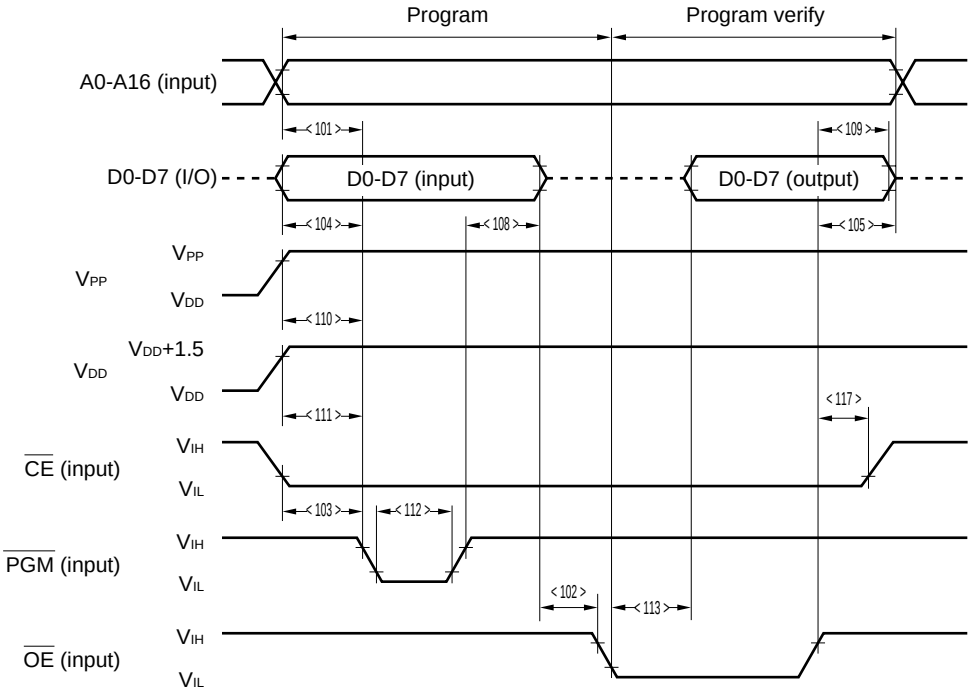
Remark The broken line indicates the high-impedance state.

(2) PROM write mode timing (byte program mode)

(T_A = 25 ± 5 °C, V_{DD} = 6.5 ± 0.25 V, V_{PP} = 12.5 ± 0.3 V)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address setup time (vs. $\overline{PGM}$ ↓)	<101>	t_{AS}	t_{AS}		2			μs
$\overline{OE}$ setup time	<102>	t_{OES}	t_{OES}		2			μs
$\overline{CE}$ setup time (vs. $\overline{PGM}$ ↓)	<103>	t_{CES}	t_{CES}		2			μs
Input data setup time (vs. $\overline{PGM}$ ↓)	<104>	t_{DS}	t_{DS}		2			μs
Address hold time (vs. $\overline{OE}$ ↑)	<105>	t_{AH}	t_{AH}		2			μs
Input data hold time (vs. $\overline{PGM}$ ↑)	<108>	t_{DH}	t_{DH}		2			μs
$\overline{OE}$ ↑→ data output float delay time	<109>	t_{DF}	t_{DF}		0		250	ns
V_{PP} setup time (vs. $\overline{PGM}$ ↓)	<110>	t_{VPS}	t_{VPS}		1.0			ms
V_{DD} setup time (vs. $\overline{PGM}$ ↓)	<111>	t_{VDS}	t_{VDS}		1.0			ms
Program pulse width	<112>	t_{PW}	t_{PW}		0.095	0.1	0.105	ms
$\overline{OE}$ ↓→ valid data delay time	<113>	t_{OE}	t_{OE}				1	μs
$\overline{OE}$ hold time	<117>	t_{OEH}	—		2			μs

Note Symbol of the corresponding μPD27C1001A



Cautions 1. Apply V_{DD} before V_{PP}, and turn off V_{DD} after V_{PP}.

2. Keep V_{PP} to less than +13.5 V including overshoot.

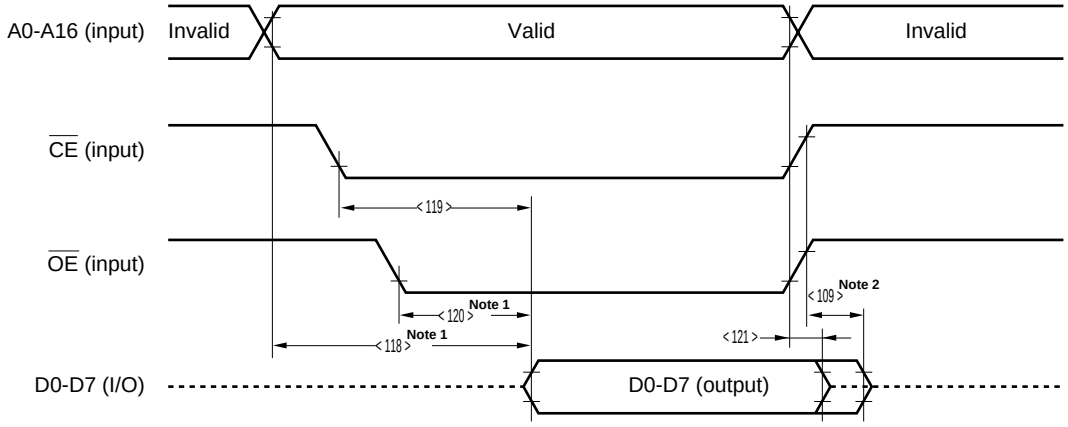
3. If the device is pulled out of the socket while +12.5 V is applied to V_{PP}, the reliability may be degraded.

Remark The broken line indicates the high-impedance state.

(3) PROM read mode timing (T_A = 25 ± 5 °C, V_{DD} = 5.0 ± 0.5 V, V_{PP} = V_{DD} ± 0.6 V)

Parameter	Symbol		Symbol[Note]	Condition	MIN.	TYP.	MAX.	Unit
Address → data output delay time	<118>	t_{ACC}	t_{ACC}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}			1	μs
$\overline{CE}$ ↓→ data output delay time	<119>	t_{CE}	t_{CE}	$\overline{OE}$ = V_{IL}			1	μs
$\overline{OE}$ ↓→ data output delay time	<120>	t_{OE}	t_{OE}	$\overline{CE}$ = V_{IL}			1	μs
$\overline{OE}$ ↑→ data output float delay time	<109>	t_{DF}	t_{DF}	$\overline{CE}$ = V_{IL}	0		60	ns
Address → data hold time	<121>	t_{OH}	t_{OH}	$\overline{CE}$ = $\overline{OE}$ = V_{IL}	0			ns

Note Symbol of the corresponding μPD27C1001A



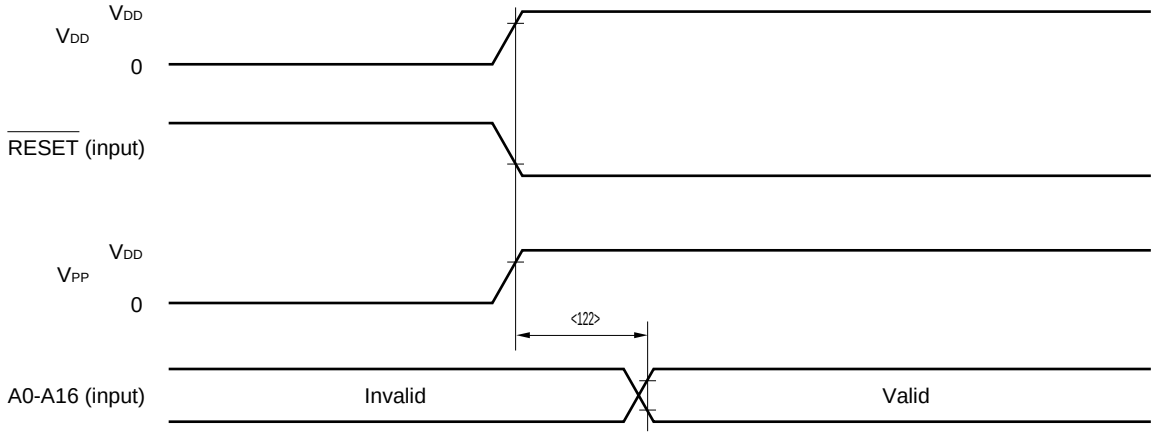
Notes 1. To read within the range of t_{ACC} (< 118 >), the delay time of $\overline{OE}$ input from the falling of $\overline{CE}$ must be t_{ACC}-t_{OE} (< 118 > - < 120 >) max.

2. t_{DF} (< 109 >) is the time after either $\overline{OE}$ or $\overline{CE}$ first reaches V_{IH}.

Remark The broken line indicates the high-impedance state.

(4) PROM programming mode setting timing (T_A = 25 °C, V_{SS} = 0 V)

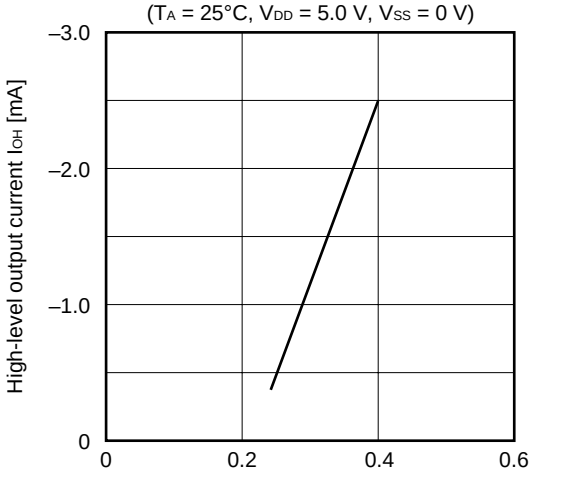
Parameter	Symbol		Condition	MIN.	TYP.	MAX.	Unit
PROM programming mode setup time	<122>	t_{SMA}		10			μs



7. CHARACTERISTICS CURVES (reference)

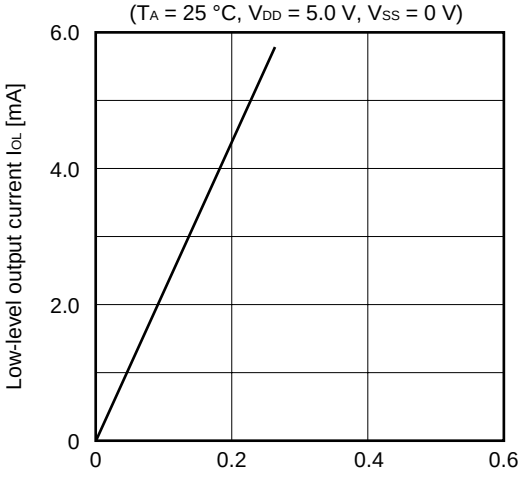
I_{OH} vs. (V_{DD} – V_{OH})

(T_A = 25°C, V_{DD} = 5.0 V, V_{SS} = 0 V)



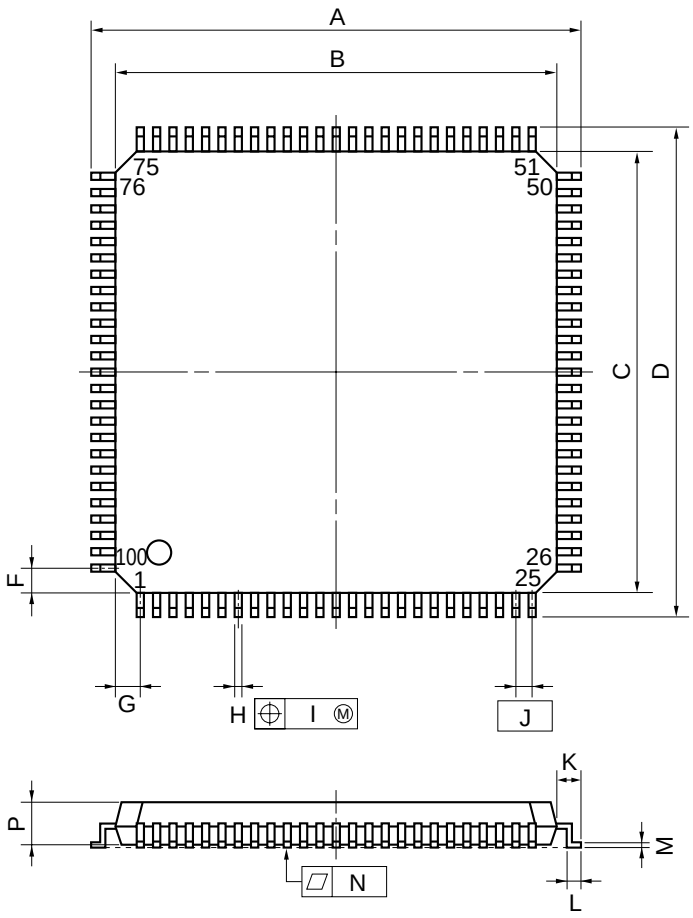
I_{OL} vs. V_{OL}

(T_A = 25 °C, V_{DD} = 5.0 V, V_{SS} = 0 V)

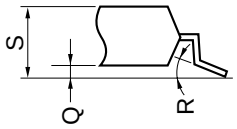


8. PACKAGE DRAWINGS

100 PIN PLASTIC QFP (FINE PITCH) (□14)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	16.0±0.2	0.630±0.008
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	16.0±0.2	0.630±0.008
F	1.0	0.039
G	1.0	0.039
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.17^{+0.03}_{-0.07}$	$0.007^{+0.001}_{-0.003}$
N	0.10	0.004
P	1.45	0.057
Q	0.125±0.075	0.005±0.003
R	5°±5°	5°±5°
S	1.7 MAX.	0.067 MAX.

P100GC-50-7EA-2

9. RECOMMENDED SOLDERING CONDITIONS

Solder this product under the folllowing recommended conditions.

For the details of the recommended soldering conditions, refer to Information Document **"Semiconductor Device Mounting Technology Manual" (C10535E)**.

For soldering methods and soldering conditions other than those recommended, consult NEC.

Table 9-1. Soldering Conditions of Surface Mount Type

Soldering Method	Soldering Condition	Symbol of Recommended Condition
Infrared reflow	Package peak temperature: 235 °C, Time: 30 seconds max. (210 °C min.), Number of times: 2 max., Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	IR35-107-2
VPS	Package peak temperature: 215 °C, Time: 40 seconds max. (200 °C min.), Number of times: 2 max., Number of days: 7[Note] (after that, prebaking is necessary at 125 °C for 10 hours) <Precaution> Products other than those supplied in thermal-resistant tray (magazine, taping, and non-thermal-resistant tray) cannot be baked in their packs.	VP15-107-2
Partial heating	Pin temperature: 300 °C max., Time: 3 seconds (per side of device)	–

Note The number of days during which the product can be stored at 25 °C, 65 % RH max. after the dry pack has been opened.

Caution Do not use two or more soldering methods in combination (except partial heating).

APPENDIX PROM WRITING TOOLS

(1) Hardware tools

Product	Product Name	Description
PROM programmer	PG-1500	NEC PROM programmer. The NEC PROM programmer can program PROM-contained single-chip microcontrollers in stand-alone mode or under control of a host machine when connected with an optional PROM programmer adapter. This programmer can also program representative PROMs from 256K-bit to 4M-bit models.
	UNISITE	Data I/O Japan Co., Ltd. PROM programmers
	2900	
	3900	
	MODEL1890A	Minato Electronics Inc. PROM programmers
★	AF-9705 Rev.01.37 or higher Algorithm Rev.02.40 or higher	Ando Electric Co., Ltd. PROM programmers
PROM programmer ★ adapter	PA-70P3000GC	PROM programmer adapter to write program to μPD70P3000 on general-purpose PROM programmer such as PG-1500

(2) Software tools

Product	Host Machine	OS	Supply Medium	Part Number	Description
PG-1500 controller	PC-9800 series	MS-DOS	3.5" FD	μS5A13PG1500	Controls PG-1500 on host machine by connecting PG-1500 and host machine with serial or parallel interface.
			5" FD	μS5A10PG1500	
	IBM PC/AT™ and compatible machines	PC DOS	3.5" FD	μS7B13PG1500	
			5" FD	μS7B10PG1500	

Remark The operations of the PG-1500 controller are guaranteed only on the above host machine and OS.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 800-366-9782
Fax: 800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.1.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
Eindhoven, The Netherlands
Tel: 040-2445845
Fax: 040-2444580

NEC Electronics (France) S.A.
Velizy-Villacoublay, France
Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

NEC Electronics (France) S.A.
Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 253-8311
Fax: 250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

NEC do Brasil S.A.
Sao Paulo-SP, Brasil
Tel: 011-889-1680
Fax: 011-889-1689

J96. 8

Related documents : μPD703000, 703001 Data Sheet (U10987E) V850 Family Instruction Table (U10229E)
V851 Register Table (U10662J) (Japanese version)

Some of the related documents are preliminary editions but are not so specified here.

V850 Family, V851, and QTOP are trademarks of NEC Corporation.
PC/AT is a trademark of IBM Corporation.

The export of this product from Japan is regulated by the Japanese government. To export this product may be prohibited without governmental license, the need for which must be judged by the customer. The export or re-export of this product from a country other than Japan may also be prohibited without a license from that country. Please call an NEC sales representative.

M4 96.5