NEC

MOS INTEGRATED CIRCUIT

μPD30111

VR4111™
64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30111 (VR4111) is one of NEC's VR Series RISC (Reduced Instruction Set Computer) microprocessors and is a high-performance 64-/32-bit microprocessor employing the MIPS™ RISC architecture.

The VR4111 uses the high-performance, super power-saving VR4110™ as the CPU core, and has many peripheral functions such as a DMA controller, software modem interface, serial interface, keyboard interface, IrDA interface, touch panel interface, real-time clock, A/D converter, and D/A converter. Configured with these functions, the VR4111 is suitable for high-speed battery-driven portable information systems. The external memory bus width can be selected from 32 bits and 16 bits, realizing high-speed data transfer.

Detailed function descriptions are provided in the following user's manual. Be sure to read it before designing.

- **VR4111 User's Manual (U13137E)**

FEATURES

- Employs 64-bit MIPS architecture
  - Conforms to MIPS III instruction set (deleting FPU, LL, LLD, SC, and SCD instructions)
  - Optimized 5-stage pipeline
- Supports MIPS16 instruction set
- Supports high-speed product-sum operation instructions
- Supports four types of operating modes, enabling more effective power-consumption management
- ★ Internal maximum operating frequency: 70 MHz
- On-chip clock generator
- Address space physical: 32 bits
  virtual: 40 bits
  Integrates 32 double entry TLBs
- High-capacity instruction/data separated cache memories
  Instruction: 16 Kbytes
  Data: 8 Kbytes
- DRAM interface and mask ROM interface to support flash memory
- Keyboard interface and touch panel interface
- 4-channel DMA controller
- Serial interface (NS16550 compatible)
- IrDA interface for infrared communication
- Software modem interface
- A/D and D/A converters to support digital voice I/O
- Supports ISA bus subset
- Power supply voltage: internal 2.3 to 2.7 V, external 3.0 to 3.6 V
- Package: 224-pin fine-pitch FBGA

APPLICATIONS

- Battery-driven portable information systems
- Embedded controllers, etc.

ORDERING INFORMATION

	Part Number	Package	Internal Maximum Operating Frequency
★	μPD30111S1-70-3C	224-pin fine-pitch BGA (16 × 16 mm)	70 MHz

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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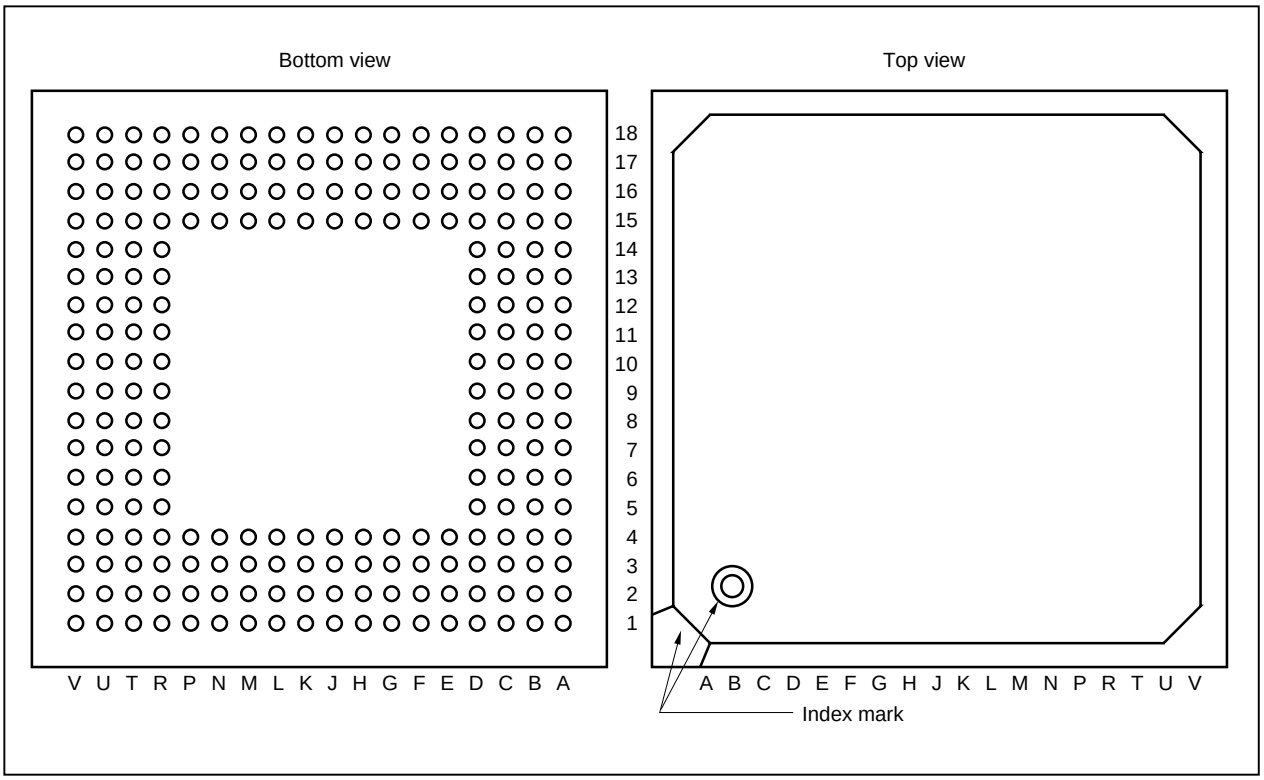
Printed in Japan

The mark ★ shows major revised points.

PIN CONFIGURATION

- 224-pin fine pitch BGA (16 × 16 mm)

★ μPD30111S1-70-3C



Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name
A1	3.3 V	$V_{DD}3$	C15	3.3 V	RTS#/CLKSEL1	H15	3.3 V	GND3
A2	3.3 V	SHB#	C16	3.3 V	GND3	H16	3.3 V	KPORT6
A3	3.3 V	BUSCLK	C17	3.3 V	ILCSENSE	H17	3.3 V	KPORT4
A4	3.3 V	HLDACK#	C18	3.3 V	AFERST#	H18	2.5 V	$V_{DD}2$
A5	3.3 V	IOCHRDY	D1	3.3 V	DATA5	J1	3.3 V	DATA20/GPIO20
A6	3.3 V	MEMW#	D2	3.3 V	DATA3	J2	3.3 V	DATA17/GPIO17
A7	3.3 V	ADD23	D3	3.3 V	DATA6	J3	3.3 V	DATA22/GPIO22
A8	3.3 V	$V_{DD}3$	D4	3.3 V	GND3	J4	3.3 V	DATA19/GPIO19
A9	3.3 V	ADD18	D5	3.3 V	MEMCS16#	J15	3.3 V	KSCAN9/GPIO41
A10	3.3 V	ADD15	D6	3.3 V	ADD25	J16	3.3 V	$V_{DD}3$
A11	3.3 V	ADD8	D7	3.3 V	GND3	J17	2.5 V	GND2
A12	3.3 V	ADD7	D8	3.3 V	ADD19	J18	3.3 V	KSCAN11/GPIO43
A13	2.5 V	$V_{DD}2$	D9	3.3 V	ADD16	K1	3.3 V	DATA23/GPIO23
A14	3.3 V	DCD#/GPIO15	D10	3.3 V	ADD14	K2	3.3 V	DATA26/GPIO26
A15	3.3 V	TXD/CLKSEL2	D11	3.3 V	$V_{DD}3$	K3	3.3 V	DATA25/GPIO25
A16	3.3 V	IRDOUT#	D12	3.3 V	GND3	K4	3.3 V	DATA21/GPIO21
A17	3.3 V	IRING	D13	3.3 V	ADD4	K15	3.3 V	KSCAN7/GPIO39
A18	3.3 V	$V_{DD}3$	D14	3.3 V	CTS#	K16	3.3 V	KSCAN10/GPIO42
B1	3.3 V	DATA1	D15	3.3 V	GND3	K17	3.3 V	KSCAN5/GPIO37
B2	3.3 V	IOR#	D16	3.3 V	GND3	K18	3.3 V	KSCAN8/GPIO40
B3	3.3 V	IOW#	D17	3.3 V	SDI	L1	3.3 V	DATA27/GPIO27
B4	3.3 V	LEDOUT#	D18	3.3 V	SDO	L2	3.3 V	DATA31/GPIO31
B5	3.3 V	FIRCLK	E1	3.3 V	DATA9	L3	3.3 V	DATA29/GPIO29
B6	3.3 V	HLDRQ#	E2	3.3 V	DATA4	L4	3.3 V	DATA24/GPIO24
B7	3.3 V	ZWS#	E3	3.3 V	DATA7	L15	3.3 V	KSCAN3/GPIO35
B8	3.3 V	ADD24	E4	3.3 V	DATA10	L16	3.3 V	KSCAN6/GPIO38
B9	3.3 V	ADD21	E15	3.3 V	OPD#	L17	3.3 V	KSCAN0/GPIO32
B10	3.3 V	ADD12	E16	3.3 V	HSPSCLK	L18	3.3 V	KSCAN4/GPIO36
B11	3.3 V	ADD6	E17	3.3 V	FS	M1	3.3 V	DATA30/GPIO30
B12	2.5 V	GND2	E18	3.3 V	HC0	M2	3.3 V	$V_{DD}3$
B13	3.3 V	DSR#	F1	3.3 V	DATA13	M3	3.3 V	GND3
B14	3.3 V	IRDIN	F2	3.3 V	DATA8	M4	3.3 V	DATA28/GPIO28
B15	3.3 V	FIRDIN#/SEL	F3	3.3 V	DATA11	M15	3.3 V	KSCAN2/GPIO34
B16	3.3 V	BATTINH/BATTINT#	F4	3.3 V	DATA14	M16	3.3 V	MIPS16EN
B17	3.3 V	OFFHOOK	F15	3.3 V	KPORT3	M17	3.3 V	GND3
B18	3.3 V	MUTE	F16	3.3 V	HSPMCLK	M18	3.3 V	KSCAN1/GPIO33
C1	3.3 V	DATA2	F17	3.3 V	TELCON	N1	2.5 V	$V_{DD}2$
C2	3.3 V	DATA0	F18	3.3 V	KPORT1	N2	3.3 V	ADD3
C3	3.3 V	GND3	G1	2.5 V	$V_{DD}2$	N3	3.3 V	ADD10
C4	3.3 V	GND3	G2	3.3 V	DATA12	N4	3.3 V	GND2
C5	3.3 V	GND3	G3	3.3 V	DATA15	N15	3.3 V	GND3
C6	3.3 V	IOCS16#	G4	3.3 V	GND3	N16	3.3 V	$V_{DD}3$
C7	3.3 V	MEMR#	G15	3.3 V	KPORT7	N17	2.5 V	$V_{DD}P$
C8	3.3 V	ADD22	G16	3.3 V	KPORT2	N18	3.3 V	GND3
C9	3.3 V	ADD20	G17	3.3 V	KPORT0	P1	3.3 V	ADD9
C10	3.3 V	ADD17	G18	3.3 V	KPORT5	P2	3.3 V	ADD0
C11	3.3 V	ADD13	H1	3.3 V	DATA16/GPIO16	P3	3.3 V	ADD2
C12	3.3 V	ADD5	H2	2.5 V	GND2	P4	3.3 V	ADD11
C13	3.3 V	R_XD	H3	3.3 V	DATA18/GPIO18	P15	2.5 V	$V_{DD}2$ ($V_{DD}PD$)
C14	3.3 V	DTR#/CLKSEL0	H4	3.3 V	$V_{DD}3$	P16	2.5 V	GNDP

Remark # indicates active low.

Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name	Pin No.	Power Supply	Pin Name
P17	3.3 V	CLKX2	T6	3.3 V	AV_{DD}	U13	3.3 V	GPIO9
P18	2.5 V	GND2 (GNDPD)	T7	3.3 V	LCAS#	U14	3.3 V	GPIO6
R1	3.3 V	ADD1	T8	3.3 V	ROMCS2#	U15	3.3 V	GPIO5
R2	3.3 V	POWER	T9	3.3 V	RD#	U16	3.3 V	GPIO1
R3	3.3 V	GND3	T10	3.3 V	WR#	U17	3.3 V	GPIO2
R4	3.3 V	GND3	T11	3.3 V	DBUS32/GPIO48	U18	3.3 V	CGND
R5	3.3 V	AUDIOIN	T12	3.3 V	DDOUT/GPIO44	V1	3.3 V	$V_{DD}3$
R6	3.3 V	DV_{DD}	T13	3.3 V	GPIO11	V2	3.3 V	PIUGND
R7	3.3 V	MRAS2#/ULCAS#	T14	3.3 V	GPIO8	V3	3.3 V	TPX0
R8	3.3 V	MRAS1#	T15	3.3 V	GND3	V4	3.3 V	TPY1
R9	3.3 V	ROMCS1#	T16	3.3 V	GND3	V5	3.3 V	ADIN2
R10	3.3 V	RSTOUT	T17	3.3 V	GPIO0	V6	3.3 V	AUDIOOUT
R11	3.3 V	GND3	T18	3.3 V	RTCX1	V7	3.3 V	MRAS3#/UUCAS#
R12	3.3 V	GPIO49	U1	3.3 V	MPOWER	V8	3.3 V	MRAS0#
R13	3.3 V	DDIN/GPIO45	U2	3.3 V	RTCRST#	V9	3.3 V	ROMCS0#
R14	3.3 V	GPIO12	U3	3.3 V	AGND	V10	3.3 V	$V_{DD}3$
R15	3.3 V	GND3	U4	3.3 V	TPX1	V11	3.3 V	LCDCS#
R16	3.3 V	CV_{DD}	U5	3.3 V	TPY0	V12	3.3 V	DCTS#/GPIO47
R17	3.3 V	RTCX2	U6	3.3 V	ADIN1	V13	3.3 V	GPIO14
R18	3.3 V	CLKX1	U7	3.3 V	DGND	V14	3.3 V	GPIO10
T1	3.3 V	POWERON	U8	3.3 V	UCAS#	V15	3.3 V	GPIO7
T2	3.3 V	RSTSW#	U9	3.3 V	ROMCS3#	V16	3.3 V	GPIO4
T3	3.3 V	GND3	U10	3.3 V	LDCRDY	V17	3.3 V	GPIO3
T4	3.3 V	$PIUV_{DD}$	U11	3.3 V	DRTS#/GPIO46	V18	3.3 V	$V_{DD}3$
T5	3.3 V	ADIN0	U12	3.3 V	GPIO13			

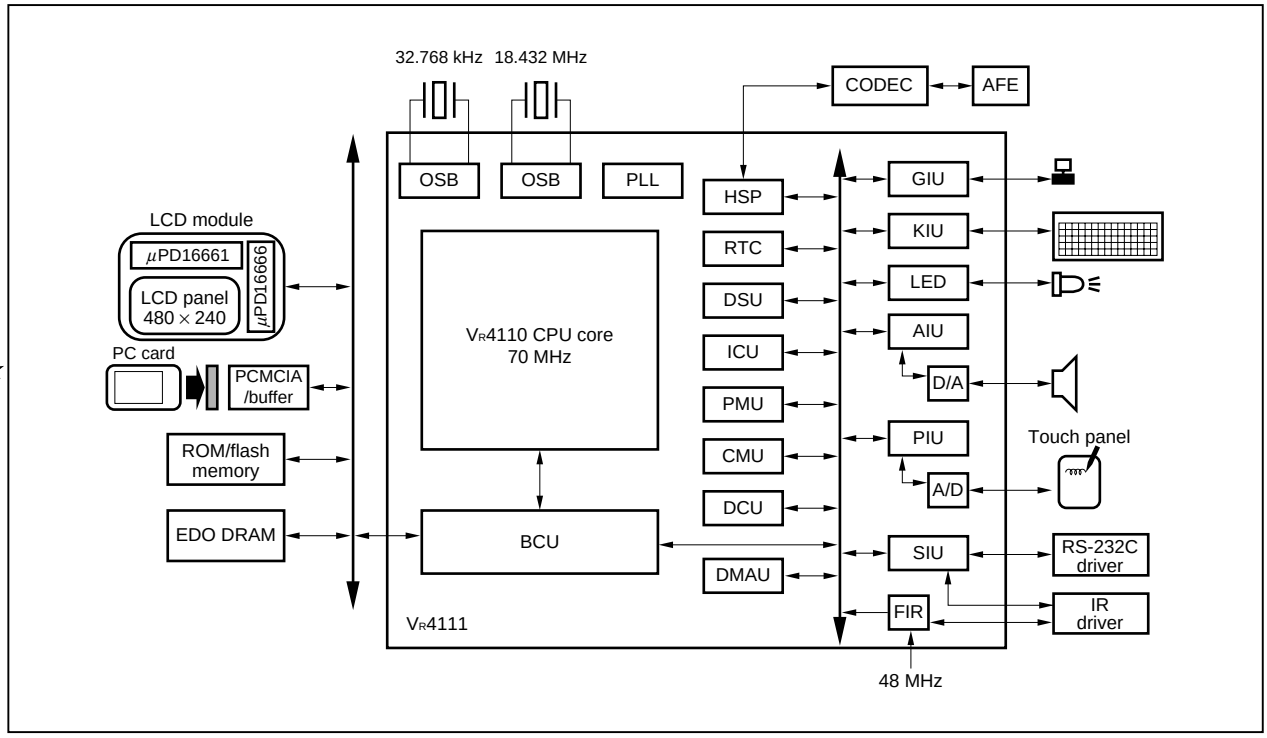
Remark # indicates active low.

PIN IDENTIFICATION

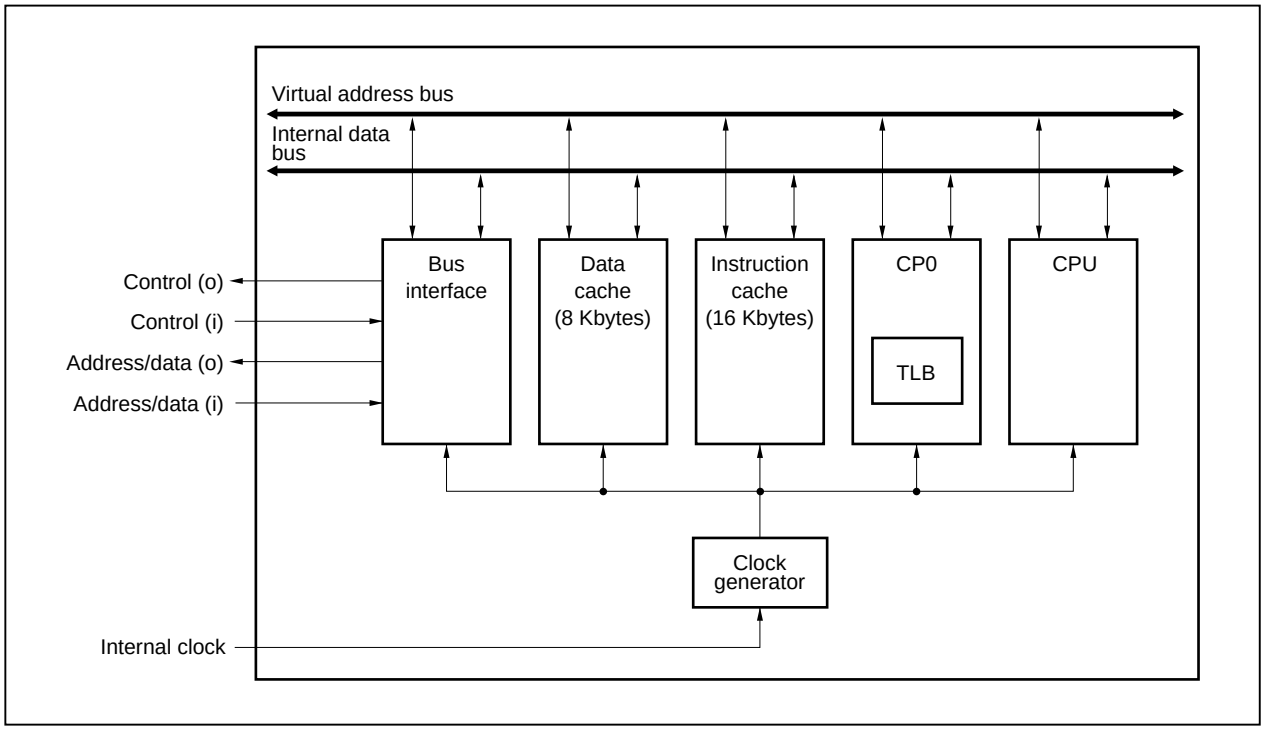
ADD (0:25):	Address Bus
ADIN (0:2):	General Purpose Input for A/D
AFERST#:	AFE Reset
AGND:	GND for A/D
AUDIOIN:	Audio Input
AUDIOOUT:	Audio Output
AV_{DD}:	V_{DD} for A/D
BATTINH:	Battery Inhibit
BATTINT:	Battery Interrupt Request
BUSCLK:	System Bus Clock
CGND:	GND for Oscillator
CLKSEL (0:2):	Clock Select
CLKX1:	Clock X1
CLKX2:	Clock X2
CTS#:	Clear to Send
CV_{DD}:	V_{DD} for Oscillator
DATA (0:31):	Data Bus
DBUS32:	Data Bus 32
DCD#:	Data Carrier Detect
DCTS#:	Debug Serial Clear to Send
DDIN:	Debug Serial Data Input
DDOUT:	Debug Serial Data Output
DGND:	GND for D/A
DRTS#:	Debug Serial Request to Send
DSR#:	Data Set Ready
DTR#:	Data Terminal Ready
DV_{DD}:	V_{DD} for D/A
FIRCLK:	FIR Clock
FIRDIN#:	FIR Data Input
FS:	Frame Synchronization
GND2, GND3:	Ground
GNDP, GNDPD:	Ground for PLL
GPIO (0:49):	General Purpose I/O
HC0:	Hardware Control 0
HLDACK#:	Hold Acknowledge
HLDRQ#:	Hold Request
HSPMCLK:	HSP Codec Master Clock
HSPSCLK:	HSP Codec Serial Clock
ILCSENSE:	Input Loop Current Sensing
IOCHRDY:	I/O Channel Ready
IOCS16#:	I/O Chip Select 16
IOR#:	I/O Read
IOW#:	I/O Write
IRDIN:	IrDA Data Input
IRDOUT#:	IrDA Data Output
IRING:	Input Ring
KPORT (0:7):	Key Code Data Input
KSCAN (0:11):	Key Scan Line
LCAS#:	Lower Column Address Strobe
LCDCS#:	LCD Chip Select
LCDRDY:	LCD Ready
LEDOUT#:	LED Output
MEMCS16#:	Memory Chip Select 16
MEMR#:	Memory Read
MEMW#:	Memory Write
MIPS16EN:	MIPS16 Enable
MPOWER:	Main Power
MRAS(0:3)#:	DRAM Row Address Strobe
MUTE:	Mute
OFFHOOK:	Off Hook
OPD#:	Output Power Down
PIUGND:	GND for Touch Panel Interface
$PIUV_{DD}$:	V_{DD} for Touch Panel Interface
POWER:	Power Switch
POWERON:	Power On State
RD#:	Read
ROMCS(0:3)#:	ROM Chip Select
RSTOUT:	System Bus Reset Output
RSTSW#:	Reset Switch
RTCRST#:	Real-time Clock Reset
RTCX1:	Real-time Clock X1
RTCX2:	Real-time Clock X2
RTS#:	Request to Send
RxD:	Receive Data
SDI:	HSP Serial Data Input
SDO:	HSP Serial Data Output
SEL:	IrDA Module Select
SHB#:	System Hi-Byte Enable
TELCON:	Telephone Control
TPX (0:1):	Touch Panel X I/O
TPY (0:1):	Touch Panel Y I/O
TxD:	Transmit Data
UCAS#:	Upper Column Address Strobe
ULCAS#:	Lower Byte of Upper Column Address Strobe
UUCAS#:	Upper Byte of Upper Column Address Strobe
$V_{DD}2$, $V_{DD}3$:	Power Supply Voltage
$V_{DD}P$, $V_{DD}PD$:	V_{DD} for PLL
WR#:	Write
ZWS#:	Zero Wait State

Remark # indicates active low.

INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 Pin Functions

(1) System bus interface signals

(1/2)

Signal Name	I/O	Function
ADD (0:25)	Output	This is a 26-bit address bus. Used to specify addresses of the VR4111, DRAM, ROM, LCD, and system bus (ISA).
DATA (0:15)	I/O	This is a 16-bit data bus. Used to transfer data from the VR4111 to DRAM, ROM, LCD, and system bus, and vice versa.
DATA (16:31)/ GPIO (16:31)	I/O	This function differs depending on how the DBUS32 pin is set. • When DBUS32 = 1 It is the higher 16 bits of the 32-bit data bus. This bus is used for transmitting and receiving data between the VR4111 and the DRAM and ROM. • When DBUS32 = 0 It is a general-purpose I/O (GPIO) port.
LCDCS#	Output	This is the LCD chip select signal. This signal is active when the VR4111 is performing LCD access using the ADD/DATA bus.
RD#	Output	Active when the VR4111 is reading data from the LCD, DRAM, or ROM.
WR#	Output	Active when the VR4111 is writing data to the LCD, DRAM, or ROM.
LCDRDY	Input	This is the LCD ready signal. Set this signal as active when the LCD controller is ready to be accessed from the VR4111.
ROMCS (2:3)#	Output	This function differs depending on how the DBUS32 pin is set. • When DBUS32 = 1 It is the chip select signal for expansion ROM/DRAM. • When DBUS32 = 0 It is a ROM chip select signal.
ROMCS (0:1)#	Output	This is the ROM chip select signal.
UUCAS#/ MRAS3#	Output	This function differs depending on how the DBUS32 pin is set. • When DBUS32 = 1 This signal is active when a valid column address is output via the ADD bus during access of DATA (24:31) in the 32-bit data bus. This signal also becomes active if the bus that accesses the LCD is 32 bits wide, and if a valid address is output to the ADD bus when DATA (24:31) is accessed. • When DBUS32 = 0 This is the DRAM's RAS signal. This signal is active when a valid row address is output via the ADD bus for the DRAM connected to the highest address.
ULCAS#/ MRAS2#	Output	This function differs depending on how the DBUS32 pin is set. • When DBUS32 = 1 This signal is active when a valid column address is output via the ADD bus during access of DATA (16:23) in the 32-bit data bus. This signal also becomes active if the bus that accesses the LCD is 32 bits wide, and if a valid address is output to the ADD bus when DATA (16:23) is accessed. • When DBUS32 = 0 This is the DRAM's RAS signal. This signal is active when a valid row address is output via the ADD bus for the DRAM connected to the next-highest address.

(2/2)

Signal Name	I/O	Function
MRAS (0:1)#	Output	This is the DRAM's RAS-only signal.
UCAS#	Output	This is the DRAM's CAS signal. This signal is active when a valid column address is output via the ADD bus during access of DATA (8:15) in the DRAM. This signal also becomes active if the bus that accesses the LCD is 32 bits wide, and if a valid address is output to the ADD bus when DATA (8:15) is accessed.
LCAS#	Output	This is the DRAM's CAS signal. This signal is active when a valid column address is output via the ADD bus during access of DATA (0:7) in the DRAM. This signal also becomes active if the bus that accesses the LCD is 32 bits wide, and if a valid address is output to the ADD bus when DATA (0:7) is accessed.
BUSCLK	Output	This is the system bus clock. It is used to output the clock that is supplied to the controller on the system bus. The frequency to be output is determined according to the state of pins CLKSEL2/TxD, CLKSEL1/RTS#, and CLKSEL0/DTR#. (See **(5) RS-232C interface signals**)
SHB#	Output	This is the system bus high-byte enable signal. During system bus access, this signal is active when the higher bytes are valid on the data bus.
IOR#	Output	This is the system bus I/O read signal. It is active when the VR4111 accesses the system bus to read data from an I/O port.
IOW#	Output	This is the system bus I/O write signal. It is active when the VR4111 accesses the system bus to write data to an I/O port.
MEMR#	Output	This is the system bus memory read signal. It is active when the VR4111 accesses the system bus to read data from memory.
MEMW#	Output	This is the system bus memory write signal. It is active when the VR4111 accesses the system bus to write data to memory.
ZWS#	Input	This is the system bus zero wait state signal. Set this signal as active to enable the controller on the system bus to be accessed by the VR4111 without a wait interval.
RSTOUT	Output	This is the system bus reset signal. It is active when the VR4111 resets the system bus controller.
MEMCS16#	Input	This is a dynamic bus sizing request signal. Set this signal as active when system bus memory accesses data in 16-bit width mode.
IOCS16#	Input	This is a dynamic bus sizing request signal. Set this signal as active when system bus I/O accesses data in 16-bit width mode.
IOCHRDY	Input	This is the system bus ready signal. Set this signal as active when the system bus controller is ready to be accessed by the VR4111.
HLDRQ#	Input	This is a hold request signal for the system bus and DRAM bus that is sent from an external bus master.
HLDACK#	Output	This is a hold acknowledge signal for the system bus and DRAM bus that is sent to an external bus master.

(2) Clock interface signals

Signal Name	I/O	Function
RTCX1	Input	This is the 32.768-kHz oscillator's input pin. It is connected to one side of a crystal resonator.
RTCX2	Output	This is the 32.768-kHz oscillator's output pin. It is connected to one side of a crystal resonator.
CLKX1	Input	This is the 18.432-MHz oscillator's input pin. It is connected to one side of a crystal resonator.
CLKX2	Output	This is the 18.432-MHz oscillator's output pin. It is connected to one side of a crystal resonator.
FIRCLK	Input	This is the 48-MHz clock input pin. Fix this at high level when FIR is not used.

(3) Battery monitor interface signals

Signal Name	I/O	Function
BATTINH/ BATTINT#	Input	This function differs depending on the state of the MPOWER pin. • When MPOWER = 0 BATTINH function Enables or disables starting of power application. 1: Enables starting 0: Disables starting • When MPOWER = 1 BATTINT# function This is an interrupt signal that is output when remaining battery power is low during normal operations. The external agent checks the remaining battery power and asserts the signal at this pin if voltage sufficient for operations cannot be supplied.

(4) Initialization interface signals

Signal Name	I/O	Function
MPOWER	Output	Indicates that the VR4111 is operating.
POWERON	Output	Signal indicating that VR4111 is to start activation. It is asserted active when start cause is detected, and deasserted inactive after BATTINH/BATTINT# signal check has been completed.
POWER	Input	Start signal of the VR4111.
RSTSW#	Input	Reset signal of the VR4111.
RTCRST#	Input	Signal resetting RTC. When power is supplied to system for the first time, the external circuit should assert this pin active for about 600 ms.

(5) RS-232C interface signals

Signal Name	I/O	Function
RxD	Input	This is a receive data signal. It is used when the RS-232C controller sends serial data to the VR4111.
CTS#	Input	This is the transmit enable (clear-to-send) signal. This signal is asserted when the RS-232C controller is ready to receive transmission of serial data.
DCD#/ GPIO15	Input	This is a carrier detection signal. Assert this signal active when valid serial data is being received. It is also used when detecting a power-on factor for the VR4111. When this is not used as the DCD# signal, this can be used as an interrupt detection I/O signal for the GIU unit.
DSR#	Input	This is the data set ready signal. Assert this signal active to set up transmission and reception of serial data between the RS-232C controller and the VR4111.
TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0	I/O	This function differs depending on the operating status. • During normal operation (output) These signals are used to perform serial communication. TxD: This is a transmit data signal. It is used when the VR4111 sends serial data to the RC-232C controller. RTS#: This is a transmit request signal. This signal is asserted when the VR4111 is ready to receive serial data from the RS-232C controller. DTR#: This is a terminal equipment ready signal. This signal is asserted when the VR4111 is ready to transmit or receive serial data. • At RTC reset (input) These signals (CLKSEL (0:2)) are used to set the operating frequency of the CPU core and the BUSCLK output frequency. These signals are sampled when the RTCRST# signal goes high.

CLKSEL (2:0)	CPU core operating frequency (MHz)	BUSCLK output frequency (MHz)
★ 1xx[Note]	RFU	RFU
011	69.3	5.77
010	65.4	5.45
001	62.0	5.17
★ 000	49.1	6.13

Note Do not set CLKSEL2 to 1.

Remark x: don't care

(6) IrDA interface signals

Signal Name	I/O	Function
IRDIN	Input	This is the IrDA serial data input signal. It is used when the IrDA controller sends the serial data to the VR4111. Both FIR and SIR can be used. However, if the IrDA controller used is made by HP, this signal should be used only for SIR.
FIRDIN#/SEL	I/O	This function differs according to the IrDA controller used. For details, see **15 SIU (SERIAL INTERFACE UNIT)**. • When an HP's controller is used FIRDIN#: FIR receive data input signal • When a TEMIC's controller is used SEL: FIR/SIR switch signal output signal • When a SHARP's controller is used Usage is prohibited.
IRDOUT#	Output	This is the IrDA serial data output signal. It is used when the VR4111 sends serial data to the IrDA controller.

(7) Debug serial interface signals

	Signal Name	I/O	Function
★	DDOUT/GPIO44	Output	This is the debug serial data output signal. It is used when the VR4111 sends serial data to an external debug serial controller. When this pin is not used as the DDOUT signal, it can be used as a general-purpose output port.
★	DDIN/GPIO45	I/O	This is the debug serial data input signal. It is used when an external debug serial controller sends serial data to the VR4111. When this pin is not used as the DDIN signal, it can be used as a general-purpose output port.
	DRTS#/GPIO46	Output	This is a transmission request signal. The VR4111 asserts this signal before sending serial data. When this pin is not used as the DRTS# signal, it can be used as a general-purpose output port.
	DCTS#/GPIO47	I/O	This is a transmit acknowledge signal. The VR4111 asserts this signal when it is ready to receive transmitted serial data. When this pin is not used as the DCTS# signal, it can be used as a general-purpose output port.

(8) Keyboard interface signals

Signal Name	I/O	Function
KPORT (0:7)	Input	This is a keyboard scan data input signal. It is used to scan for pressed keys on the keyboard.
KSCAN (0:11)/ GPIO (32:43)	Output	These signals are used as keyboard scan data output signals and a general-purpose output port. The scan line is set as active when scanning for pressed keys on the keyboard. Pins that are not used for the key scan operation can be used as a general-purpose output port.

(9) Audio interface signals

Signal Name	I/O	Function
AUDIOIN	Input	This is an audio input signal.
AUDIOOUT	Output	This is an audio output signal. Analog signals that have been converted via the on-chip 10-bit D/A converter are output.

(10) Touch panel/general-purpose A/D interface signals

Signal Name	I/O	Function
TPX (0:1)	I/O	These are I/O signals that are used for the touch panel. They use the voltage applied to the X coordinate and the voltage input to the Y coordinate to detect which coordinates on the touch panel are being pressed.
TPY (0:1)	I/O	These are I/O signals that are used for the touch panel. They use the voltage applied to the Y coordinate and the voltage input to the X coordinate to detect which coordinates on the touch panel are being pressed.
ADIN (0:2)	Input	This is a general-purpose A/D input signal.

(11) General-purpose I/O signals

Signal Name	I/O	Function
GPIO (0:3)	I/O	These are maskable activation factor input signals. After start-up, they are used as ordinary GPIO pins.
GPIO (4:8)	I/O	These are general-purpose I/O pins.
GPIO (9:12)	I/O	These are maskable activation factor input signals. After start-up, they are used as ordinary GPIO pins.
GPIO (13:14)	I/O	These are general-purpose I/O pins.
GPIO (16:31)/ DATA (16:31)	I/O	See **(1) System bus interface signals** in this section.
GPIO (32:43)/ KSCAN (0:11)	Output	See **(8) Keyboard interface signals** in this section.
GPIO44/DDOUT	Output	See **(7) Debug serial interface signals** in this section.
GPIO45/DDIN	I/O	See **(7) Debug serial interface signals** in this section.
GPIO46/DRTS#	Output	See **(7) Debug serial interface signals** in this section.
GPIO47/DCTS#	I/O	See **(7) Debug serial interface signals** in this section.
GPIO48/DBUS32	I/O	See **(14) Initialization signals** in this section.
GPIO49	Output	This function differs depending on the operating status. • During normal operation It can be used as a general-purpose output port. • At RTC reset This pin functions as an input pin. Input a low level to this pin. This signal is sampled when the RTCRST# signal goes high.

(12) HSP modem interface signals

Signal Name	I/O	Function
IRING	Input	This signal is asserted active when detecting the RING signal.
ILCSENSE	Input	Handset detect signal
OFFHOOK	Output	On-hook relay control signal
MUTE	Output	Modem speaker mute control signal
AFERST#	Output	CODEC reset signal
SDI	Input	Serial input signal from CODEC
FS	Input	Frame synchronization signal from CODEC
SDO	Output	Serial output signal to CODEC
HSPSCLK	Input	Operation clock input of modem interface block for CODEC
TELCON	Output	Handset relay control signal
HC0	Output	CODEC control signal
HSPMCLK	Output	Clock output to CODEC
OPD#	Output	This signal is asserted active when the power supply of CODEC or DAA is ON.

(13) LED interface signal

Signal Name	I/O	Function
LEDOUT#	Output	This is an output signal for lighting LEDs.

(14) Initialization signals

Signal Name	I/O	Function
DBUS32/ GPIO48	I/O	This function differs depending on the operating status. • During normal operation (output) This can be used as a general-purpose output port. • At RTC reset (input) This can be used as the data-bus width switch signal. This signal is sampled when the RTCRST# signal goes high. 1: Data bus is used in 32-bit width mode 0: Data bus is used in 16-bit width mode
MIPS16EN	Input	This signal enables or disables use of the MIPS16 instruction. This signal is sampled when the RTCRST# signal goes high. 1: Enable use of the MIPS16 instruction 0: Disables use of the MIPS16 instruction

(15) Dedicated V_{DD} and GND signals

Signal Name	Power Supply	Function
V_{DD}P	2.5 V	V_{DD} dedicated for the PLL analog block.
GNDP	2.5 V	GND dedicated for the PLL analog block.
V_{DD}PD	2.5 V	V_{DD} dedicated for the PLL digital block. The function is the same as V_{DD}2.
GNDPD	2.5 V	GND dedicated for the PLL digital block. The function is the same as GND2.
CV_{DD}	3.3 V	V_{DD} dedicated for the oscillator.
CGND	3.3 V	GND dedicated for the oscillator.
DV_{DD}	3.3 V	V_{DD} dedicated for the D/A converter. The voltage applied to this pin becomes the maximum value for AUDIOOUT's analog output.
DGND	3.3 V	GND dedicated for the D/A converter. The voltage applied to this pin becomes the minimum value for AUDIOOUT's analog output.
AV_{DD}	3.3 V	V_{DD} dedicated for the A/D converter. The voltage applied to this pin becomes the maximum voltage value for the AD interface signal.
AGND	3.3 V	GND dedicated for the A/D converter. The voltage applied to this pin becomes the minimum voltage value detectable by the AD interface signals.
$PIUV_{DD}$	3.3 V	V_{DD} dedicated for the touch panel interface.
PIUGND	3.3 V	GND dedicated for the touch panel interface.
V_{DD}2	2.5 V	Normally, V_{DD} of 2.5 V.
GND2	2.5 V	Normally, GND of 2.5 V.
V_{DD}3	3.3 V	Normally, V_{DD} of 3.3 V.
GND3	3.3 V	Normally, GND of 3.3 V.

Caution The V_R4111 has two types of power supplies. There are no restrictions as to the sequence in which these power supplies are applied. However, do not apply one type of power for more than one second while the other power supply is not applied.

1.2 Pin Status in Specific Status

(1/3)

Signal Name	After Reset by RTCRST	After Reset by Deadman's SW or RSTSW	In Suspend Mode	In Hibernate Mode or on Shutdown by HAL Timer	During Bus Hold
ADD (0:25)	0	0	**Note 1**	0	Hi-Z
DATA (0:15)	0	0	**Note 1**	0	Hi-Z
DATA (16:31)/ GPIO (16:31)	0/ Hi-Z	0/ Hi-Z	**Note 1**	0/ Hi-Z	Hi-Z/ **Note 1**
LCDCS#	Hi-Z	1	1	Hi-Z	1
RD#	Hi-Z	1	1	Hi-Z	Hi-Z
WR#	Hi-Z	1	1	Hi-Z	Hi-Z
LCDRDY	–	–	–	–	–
ROMCS (2:3)#	Hi-Z	**Note 2**	**Note 2**	**Note 2**	**Note 2**
ROMCS (0:1)#	Hi-Z	1	1	Hi-Z	1
UUCAS#/MRAS3#	**Note 3**	**Note 4**	0	0	Hi-Z
ULCAS#/MRAS2#	**Note 3**	**Note 4**	0	0	Hi-Z
MRAS (0:1)#	1	**Note 4**	0	0	Hi-Z
UCAS#	0	**Note 4**	0	0	Hi-Z
LCAS#	0	**Note 4**	0	0	Hi-Z
BUSCLK	0	0	**Note 1**	0	**Note 5**
SHB#	Hi-Z	1	1	Hi-Z	Hi-Z
IOR#	Hi-Z	1	1	Hi-Z	Hi-Z
IOW#	Hi-Z	1	1	Hi-Z	Hi-Z
MEMR#	Hi-Z	1	1	Hi-Z	Hi-Z
MEMW#	Hi-Z	1	1	Hi-Z	Hi-Z
ZWS#	–	–	–	–	–
RSTOUT	Hi-Z	1	0	Hi-Z	**Note 6**

Notes 1. The previous Fullspeed mode state is retained.

2. When these pins are used as chip select signals of ROM/expansion ROM, their function is the same as that of ROMCS (0:1)#. When they are used as RAS signals of the expansion DRAM, their function is the same as that of MRAS (0:1)#.

3. When DBUS32 = 1: Outputs low level.
When DBUS32 = 0: Outputs high level.

4. Reset by RSTSW# signal: This pin outputs low level (self-refresh function).
Reset by deadman's switch: This pin outputs high level.

5. Bus hold from suspend mode: The previous Fullspeed mode state is retained.
Bus hold from full speed mode or standby mode: Outputs clocks.

6. Normal operation is performed.

Remark 0: Low-level output, 1: High-level output, Hi-Z: High impedance

(2/3)

Signal Name	After Reset by RTCRST	After Reset by Deadman's SW or RSTSW	In Suspend Mode	In Hibernate Mode or on Shutdown by HAL Timer	During Bus Hold
IOCS16#	–	–	–	–	–
MEMCS16#	–	–	–	–	–
IOCHRDY	–	–	–	–	–
HLDRQ#	–	–	–	–	–
HLDACK#	Hi-Z	1	**Note 1**	Hi-Z	**Note 1**
RTCX1	–	–	–	–	–
RTCX2	–	–	–	–	–
CLKX1	–	–	–	–	–
CLKX2	–	–	–	–	–
FIRCLK	–	–	–	–	–
BATTINH/ BATTINT#	–	–	–	–	–
MPOWER	0	1	1	0	1
POWERON	0	0	0	0	0
POWER	–	–	–	–	–
RSTSW#	–	–	–	–	–
RTCRST#	–	–	–	–	–
RxD	–	–	–	–	–
TxD/CLKSEL2	Hi-Z	1	1	1	**Note 1**
RTS#/CLKSEL1	Hi-Z	1	1	1	**Note 1**
CTS#	–	–	–	–	–
DCD#/GPIO15	–	–	–	–	–
DTR#/CLKSEL0	Hi-Z	1	1	1	**Note 1**
DSR#	–	–	–	–	–
IRDIN	–	–	–	–	–
IRDOUT#	0	0	0	0	**Note 1**
FIRDIN#/SEL	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**
DDIN/ GPIO45 **Note 3**	–/ Hi-Z	–/ **Note 2**	–/ **Note 2**	–/ **Note 2**	–/ **Note 2**
DDOUT/ GPIO44 **Note 3**	1/ 1	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**
DRTS#/ GPIO46 **Note 3**	1/ 1	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**	1/ **Note 2**
DCTS#/ GPIO47 **Note 3**	–/ Hi-Z	–/ **Note 2**	–/ **Note 2**	–/ **Note 2**	–/ **Note 2**

Notes 1. Normal operation is performed.

2. The previous Fullspeed mode state is retained

3. Whether these pins are used as function pins or output port pins can be selected by software.

Remark 0: Low-level output, 1: High-level output, Hi-Z: High impedance

(3/3)

Signal Name	After Reset by RTCRST	After Reset by Deadman's SW or RSTSW	In Suspend Mode	In Hibernate Mode or on Shutdown by HAL Timer	During Bus Hold
KPORT (0:7)	–	–	–	–	–
KSCAN (0:11)/ GPIO (32:43)[Note 1]	Hi-Z/ Hi-Z	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**	Hi-Z/ **Note 2**	**Note 3**
AUDIOOUT	0	0	**Note 2**	0	**Note 3**
TPX (0:1)	1	1	**Note 2**	1	**Note 3**
TPY (0:1)	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 3**
ADIN (0:2)	–	–	–	–	–
AUDIOIN	–	–	–	–	–
GPIO (0:14)	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 3**
IRING	–	–	–	–	–
ILCSENSE	–	–	–	–	–
OFFHOOK[Note 4]	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**
MUTE[Note 4]	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**
AFERST#[Note 4]	0	0	**Note 2**	0	**Note 2**
SDI	–	–	–	–	–
FS	–	–	–	–	–
SDO	0	0	**Note 2**	0	**Note 2**
HSPSCLK	–	–	–	–	–
TELCON[Note 4]	Hi-Z	Hi-Z	**Note 2**	Hi-Z	**Note 2**
HC0[Note 4]	0	0	**Note 2**	0	**Note 2**
HSPMCLK[Note 4]	0	0	**Note 2**	0	**Note 2**
OPD#	0	0	**Note 2**	0	**Note 2**
LEDOUT#	1	**Note 3**	**Note 3**	**Note 3**	**Note 3**
DBUS32/ GPIO48[Note 5]	Hi-Z/ Hi-Z	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**	Hi-Z/ **Note 2**	**Note 2**/ **Note 2**
MIPS16EN	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
GPIO49[Note 5]	**Note 6**	**Note 2**	**Note 2**	**Note 2**	**Note 2**

Notes 1. Whether these pins are used as function pins or output port pins can be selected by software.

2. The previous Fullspeed mode state is retained.

3. Normal operation is performed.

4. Be sure to set the BSC bit of the HSPINT register (0x0C00 0020) to 1 at initialization.

5. This pin functions as an output port after RTC reset has been cleared.

6. This pin functions as an input pin. Input a low level to this pin.

Remark 0: Low-level output, 1: High-level output, Hi-Z: High impedance

1.3 Types of Pin I/O Circuits and Recommended Connection of Unused Pins

(1/3)

Signal Name	Internal Process	External Process	Drive Capacity	I/O Circuit Type
ADD (0:25)	Slew rate buffer	–	120 pF	A
DATA (0:15)	–	–	40 pF	A
DATA (16:31)/ GPIO (16:31)	–	**Note 1**	40 pF	A
LCDCS#	Slew rate buffer	–	40 pF	A
RD#	Slew rate buffer	**Note 2**	120 pF	A
WR#	Slew rate buffer	**Note 2**	120 pF	A
LCDRDY	–	**Note 3**	–	A
ROMCS (2:3)#	Slew rate buffer	**Note 4**	40 pF	A
ROMCS (0:1)#	Slew rate buffer	–	40 pF	A
UUCAS#/MRAS3#	Slew rate buffer	**Note 2**	120 PF	A
ULCAS#/MRAS2#	Slew rate buffer	**Note 2**	120 pF	A
MRAS (0:1)#	Slew rate buffer	**Note 2**	40 pF	A
UCAS#	Slew rate buffer	**Note 2**	120 pF	A
LCAS#	Slew rate buffer	**Note 2**	120 pF	A
BUSCLK	Slew rate buffer	–	40 pF	A
SHB#	Slew rate buffer	**Note 2**	40 pF	A
IOR#	Slew rate buffer	**Note 2**	40 pF	A
IOW#	Slew rate buffer	**Note 2**	40 pF	A
MEMR#	Slew rate buffer	**Note 2**	40 pF	A
MEMW#	Slew rate buffer	**Note 2**	40 pF	A
ZWS#	**Note 5**	**Note 3**	–	A
RSTOUT	Slew rate buffer	Pull-up	40 pF	A
IOCS16#	**Note 5**	**Note 3**	–	A
MEMCS16#	**Note 5**	**Note 3**	–	A
IOCHRDY	**Note 5**	**Note 3**	–	A

Notes 1. The DATA (16:31) pins of the VR4111 function as GPIO (16:31) when the width of the data bus is set to 16 bits. When using these pins as GPIO (16:31), pull them up/down so that an intermediate level is not input to them.

2. Externally pull up these pins when the bus hold function is used.

3. Do not input an intermediate level to these pins.

4. Externally pull up these pins when they are used as the RAS signals of the extension DRAM.

5. An intermediate level can be input to these pins while the MPOWER pin outputs a low level.

(2/3)

Signal Name	Internal Process	External Process	Drive Capacity	I/O Circuit Type
HLDRQ#	**Note 1**	**Note 2**	–	A
HLDACK#	Slew rate buffer	–	40 pF	A
RTCX1	–	Oscillator	–	–
RTCX2	–	Oscillator	–	–
CLKX1	–	Oscillator	–	–
CLKX2	–	Oscillator	–	–
FIRCLK	–	**Note 3**	–	A
BATTINH/ BATTINT#	Schmitt-triggered input	–	–	B
MPOWER	–	–	40 pF	A
POWERON	–	–	40pF	A
POWER	Schmitt-triggered input	–	–	B
RSTSW#	Schmitt-triggered input	–	–	B
RTCRST#	Schmitt-triggered input	–	–	B
RxD	–	–	–	A
TxD/CLKSEL2	–	Pull-up/pull-down	40 pF	A
RTS#/CLKSEL1	–	Pull-up/pull-down	40 pF	A
CTS#	–	–	–	A
DCD#/GPIO15	Schmitt-triggered input	Pull-up	–	B
DTR#/CLKSEL0	–	Pull-up/pull-down	40 pF	A
DSR#	–	–	–	A
IRDIN	–	Pull-up	–	A
IRDOUT#	–	–	40 pF	A
FIRDIN#/SEL	–	Pull-up/pull-down	40 pF	A
DDIN/GPIO45	–	–	40 pF	A
DDOUT/GPIO44	–	–	40 pF	A
DRTS#/GPIO46	–	–	40 pF	A
DCTS#/GPIO47	–	–	40 pF	A

Notes 1. An intermediate level can be input to these pins while the MPOWER pin outputs a low level.

2. When bus hold function is used: Pull up this pin.
When bus hold function is not used: Connect this pin to V_{DD}.

3. When FIR unit is used: Connect an oscillator to this pin.
When FIR unit is not used: Fix this pin to V_{DD}.

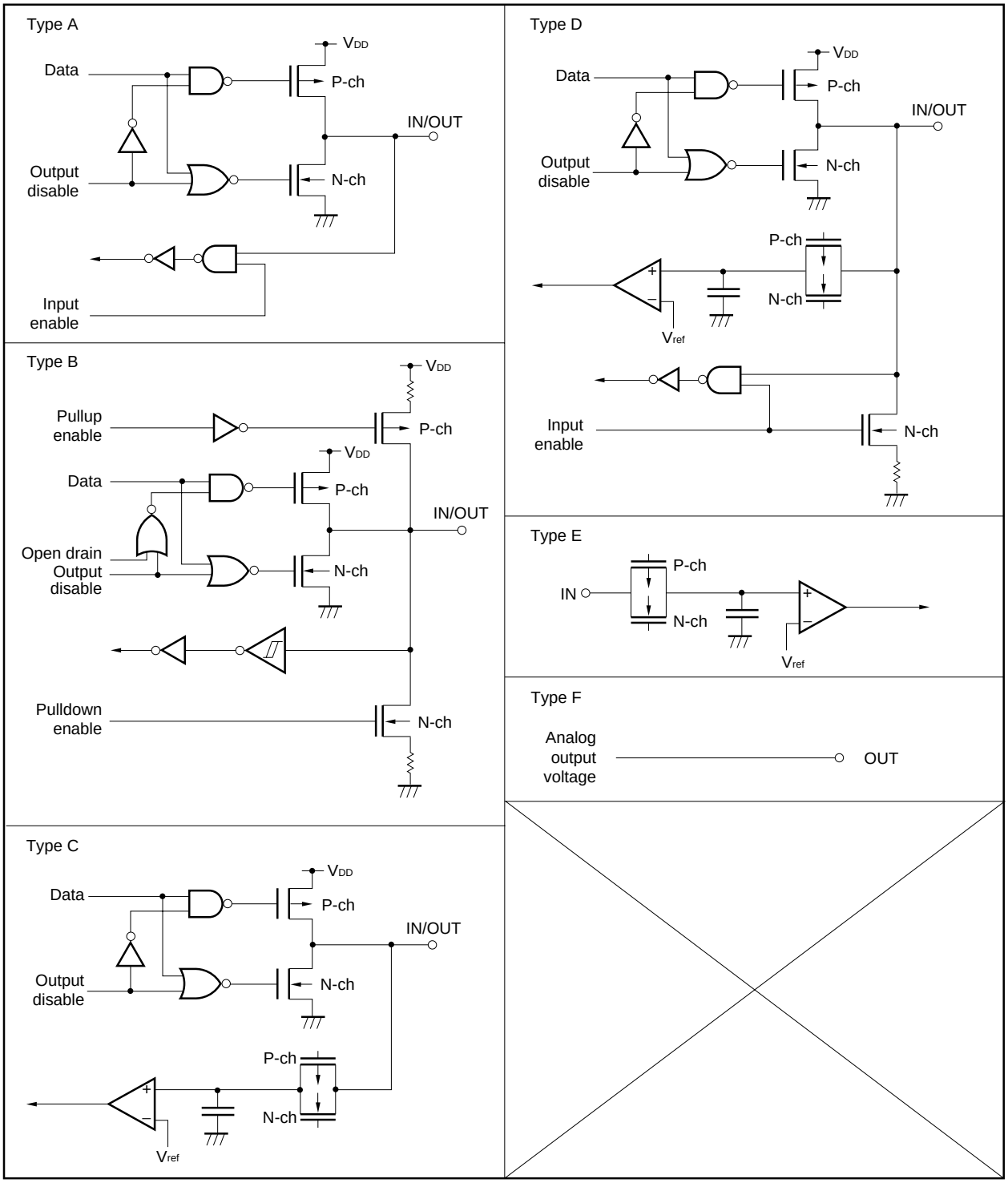
(3/3)

Signal Name	Internal Process	External Process	Drive Capacity	I/O Circuit Type
KPORT (0:7)	Schmitt-triggered input, pull-down	–	–	B
KSCAN (0:11)/ GPIO (32:43)	–	–	40 pF	A
AUDIOOUT	–	**Note 1**	–	F
TPX (0:1)	–	–	120 pF or higher	C
TPY1	–	–	120 pF or higher	D
TPY0	–	–	120 pF or higher	C
ADIN (0:2)	–	–	–	E
AUDIOIN	–	–	–	E
GPIO (0:14)	Schmitt-triggered input, **Note 2**	**Note 2**	40 pF	B
IRING	Schmitt-triggered input	Pull-down	–	B
ILCSENSE	–	Pull-down	–	A
OFFHOOK	–	–	40 pF	A
MUTE	–	–	40 pF	A
AFERST#	–	–	40 pF	A
SDI	–	Pull-up/pull-down	–	A
FS	–	Pull-up/pull-down	–	A
SDO	–	–	40 pF	A
HSPSCLK	–	–	–	A
TELCON	–	–	40 pF	A
HC0	–	–	40 pF	A
HSPMCLK	–	–	40 pF	A
OPD#	–	–	40 pF	A
LEDOUT#	–	–	40 pF	A
DBUS32/ GPIO48	–	Pull-up/pull-down	40 pF	A
MIPS16EN	–	Pull-up/pull-down	40 pF	A
GPIO49	–	Pull-down	–	A

Notes 1. The output level of the AUDIOOUT pin fluctuates with the external impedance. Connect an operational amplifier with input characteristics of high impedance to this pin.

2. Connecting an internal pull-up/pull-down resistor to the GPIO (0:14) pins can be selected by software. When the internal pull-up/pull-down resistor is not used, connect an external pull-up/pull-down resistor to these pins.

1.4 Pin I/O Circuits



2. INTERNAL BLOCKS

For the internal block configuration, see the figure on page 6.

2.1 VR4110 CPU Core

(1) CPU

The CPU processes integer instructions and consists of a 64-bit register file, a 64-bit integer data bus, and a sum-of-products operation unit.

(2) Coprocessor 0 (CP0)

The CP0 has a memory management unit (MMU) and an exception processing function. The MMU translates addresses and checks whether an access is made between different types (user, supervisor, or kernel) of memory segments. Translation of virtual addresses to physical addresses is performed by TLB (high-speed translation lookaside buffer).

(3) Instruction cache

The instruction cache has a 16-Kbyte capacity, consisting of direct mapping, virtual index, and physical tag type.

(4) Data cache

The data cache has an 8-Kbyte capacity, consisting of direct mapping, virtual index, physical tag, and write back type.

(5) CPU bus interface

The CPU bus interface controls data transfer between the VR4110 CPU core and BCU, which is one of the peripheral units. As the bus interface for the VR4110 CPU core, two 32-bit address/data multiplexed buses for input and output, clock signals, and interrupt control signals are used.

2.2 Clock Generator

The following clock inputs are oscillated to generate and supply clocks to internal units.

- 32.768-kHz clock for RTC. The 32.768-kHz clock generated by the crystal resonator is oscillated by the internal oscillator, and supplied to the RTC unit.
- 18.432-MHz clock for serial interface, touch panel interface, and reference operating clock of the VR4111. The 18.432-MHz clock generated by the crystal resonator is oscillated by the internal oscillator, multiplied by PLL (phase-locked loop), to generate the pipeline clock (PClock). The internal bus clock (TClock) is generated from PClock.

2.3 BCU (Bus Control Unit)

The BCU internally transfers data with the VR4110 CPU core via SysAD bus (internal). It also controls the LCD controller, DRAM, ROM (flash memory or mask ROM), and PCMCIA controller connected to the system bus, and transfers data with the above devices via ADD and DATA buses.

2.4 RTC (Real-Time Clock Unit)

The RTC has a precise counter that operates with a 32.768-kHz clock supplied from the clock generator. It also has several counters and compare registers for various interrupts.

2.5 DSU (Deadman's Switch Unit)

The DSU is used to check whether the processor is operating normally. If the software does not clear the register of this unit at specific intervals, the system is shut down.

2.6 ICU (Interrupt Control Unit)

The ICU controls interrupt requests generated from the external and internal sources of the VR4111, and reports an interrupt request, if any, to the VR4110 CPU core.

2.7 PMU (Power Management Unit)

The PMU outputs signals necessary for controlling the power of the entire system, including the VR4111. It also controls the PLL of the VR4110 CPU core and the internal clocks (PClock, TClock, and MasterOut) in the power-saving mode.

2.8 DMAAU (Direct Memory Access Address Unit)

The DMAAU controls three types of DMA transfer addresses.

2.9 DCU (Direct Memory Access Control Unit)

The DCU controls addresses of three types of DMA transfers.

2.10 CMU (Clock Mask Unit)

The CMU controls supply of the clocks (TClock or MasterOut) from the VR4110 CPU core to the internal peripheral units.

2.11 GIU (General Purpose I/O Unit)

GIU controls forty-nine GPIO pins.

2.12 AIU (Audio Interface Unit)

AIU performs microphone-input sampling and audio-signal output by controlling the internal A/D and D/A converters.

2.13 KIU (Keyboard Interface Unit)

The KIU has 8/10/12 scan lines and eight detection lines to detect input of 64/80/96 keys. It can also detect roll over of 2 or 3 keys by adding diodes.

2.14 PIU (Touch Panel Interface Unit)

PIU performs touch detection of the touch panel by controlling the internal A/D converter.

2.15 DSIU (Debug Serial Interface Unit)

The DSIU is a serial interface for debugging and supports a transfer rate of up to 115 kbps.

2.16 SIU (Serial Interface Unit)

★ The SIU is a serial interface that is compatible with NS16550 and conforms to the RS-232C Standards, and supports a transfer rate of up to 1.15 Mbps. In addition, an IrDA serial interface that supports a transfer rate of 4 Mbps using the FIR unit is also included, though this IrDA serial interface is exclusively used with the RS-232C interface.

2.17 FIR (Fast IrDA Interface Unit)

The FIR unit is a unit to perform IrDA communication of 0.576 Mbps to 4 Mbps. This unit operates with a dedicated 48-MHz clock input.

2.18 HSP (Host Signal Processing Unit)

★ The HSP unit is a unit for realizing a software modem. This unit controls interfacing between the CPU core and the CODEC devices.

2.19 LED (LED Unit)

The LED unit is a unit for controlling the lighting of external LEDs.

3. INTERNAL ARCHITECTURE

3.1 Pipeline

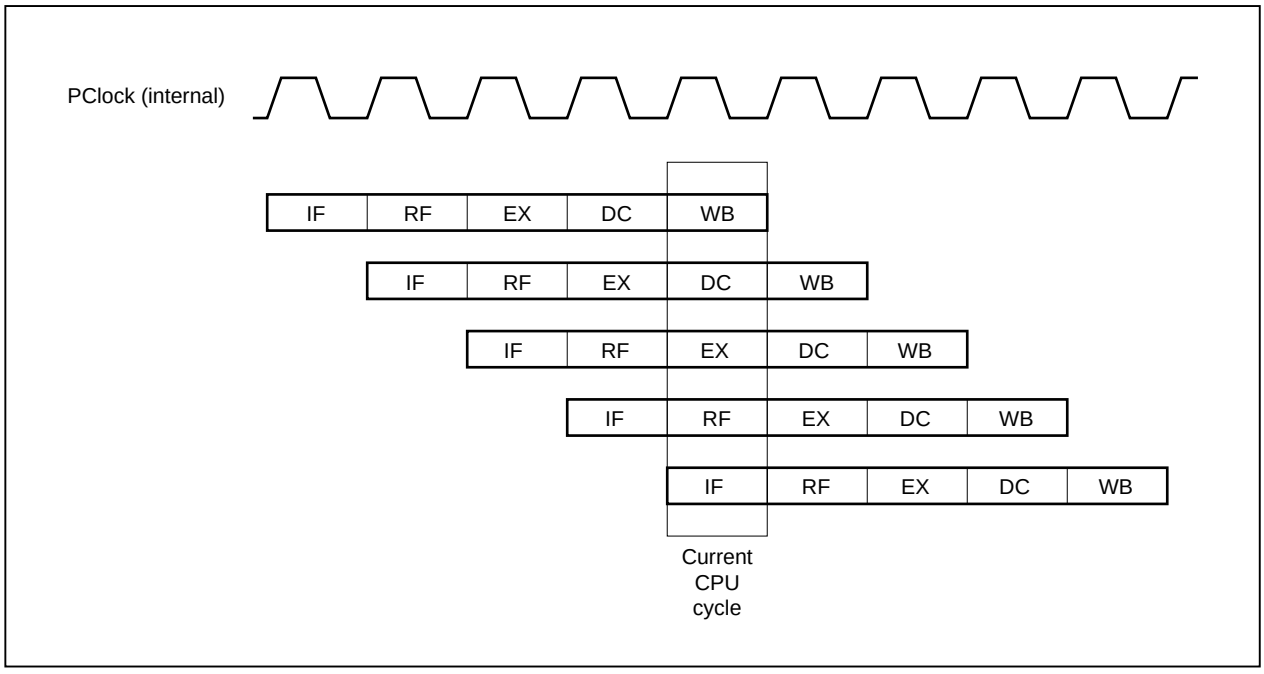
Each instruction is executed in the following five steps:

(1) IF Instruction fetch
(2) RF Register fetch
(3) EX Execution
(4) DC Data cache fetch
(5) WB Write back

The VR4111 has a five-stage pipeline. It takes five clocks to execute each instruction, but instructions can be executed in parallel. The pipeline clock, PClock, is determined by the setting of the CLKSEL (0:2) pins.

The following figure outlines the pipeline.

Figure 3-1. Pipeline of VR4111 (5-Stage)



3.2 CPU Registers

Figure 3-2 shows the CPU registers of the VR4111. The bit width of these registers is determined by the operation mode of the processor (32 bits in 32-bit mode or 64 bits in 64-bit mode).

Of the 32 general-purpose registers, the following two have a special function.

- Register r0: The contents of this register are always 0. To discard the result of an operation, describe this register as the target of an instruction. When the value 0 is necessary, this register can also be used as a source register.
- Register r31: This is a link register used by link instructions, such as the Jump and Link (JAL) instruction. r31 can be used by other instructions. However, be careful that use of the register by a link instruction will not coincide with use of the register for other operations.

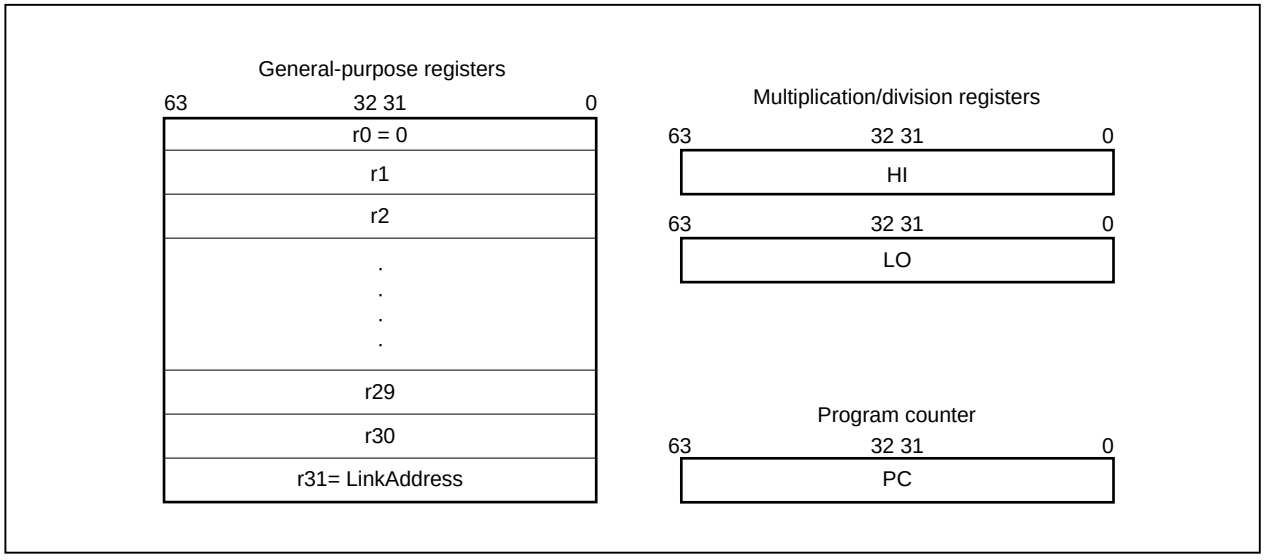
The two multiplication/division registers (HI and LO) store the result of a multiplication or sum-of-products operation, or the quotient (LO) and remainder (HI) resulting from division.

Because the VR4111 does not support floating-point instructions, it is not provided with the 32 floating-point general-purpose registers (FGR) found in the VR4300™ and VR4400™.

The VR4111 does not have a program status word (PSW). The function of PSW is substituted by the status registers and cause registers incorporated in the system control coprocessor (CP0).

Remark The load link bit (LL bit) used with synchronization instructions (LL and SC) for multiprocessor supported by the VR4300 and VR4400 is not provided in the VR4111 (refer to **3.3.1 (2) Deletion of multiprocessor instructions**).

Figure 3-2. CPU Registers



When the MIPS16 instruction set (refer to **3.3.2**) is used, eight of the above general registers can be used. The special instruction of MIPS16 implicitly uses some general-purpose registers and the special registers. The register set for the MIPS16 instruction set is shown below.

Table 3-1. Register Set When MIPS16 Instruction Set Is Used

(a) General registers

MIPS16 Instruction Register No.	32-Bit Instruction Register No.	Symbol	Description
0	16	s0	General-purpose register
1	17	s1	General-purpose register
2	2	v0	General-purpose register
3	3	v1	General-purpose register
4	4	a0	General-purpose register
5	5	a1	General-purpose register
6	6	a2	General-purpose register
7	7	a3	General-purpose register
–	24	t8	MIPS16 condition code register. BTEQZ, BTNEZ, CMP, CMPI, SLT, SLTU, SLTI, and SLTIU instructions are implicitly referenced.
–	29	sp	Stack pointer register
–	31	ra	Return address register

(b) Special registers

Symbol	Description
PC	Program counter. The PC-relative Add instruction and Load instruction can access this register.
HI	The higher word of the multiply or divide result is inserted.
LO	The lower word of the multiply or divide result is inserted.

Remark The symbols are the general assembler symbols.

3.3 Outline of Instruction Set

Basically, the instruction set of the VR4111 conforms to the MIPS I, II, and III instruction sets. In addition, the MIPS16 instruction set whose instruction code length is fixed to 16 bits is supported.

For details of each instruction set, refer to **VR4111 User's Manual**.

3.3.1 MIPS III instruction set

The MIPS III instruction set is different in the VR4111 compared to in other processors in the VR Series in the following four points. Note that the difference between the VR4100™ and VR4111 is that the VR4111 can manage operations including peripheral functions by using power mode instructions (refer to **(4)**).

(1) Deletion of floating-point (FPU) instructions

Because the VR4111 does not have a floating-point unit, it does not support FPU instructions. If an FPU instruction is encountered, therefore, a reserved instruction exception occurs. If it is necessary to use an FPU instruction, emulate the instruction in software in an exception handler.

(2) Deletion of multiprocessor instructions

The VR4111 does not support a multiprocessor operating environment. If a synchronization support instruction (LL or SC instruction) defined by MIPS II and III ISA is encountered, a reserved instruction exception occurs. In addition, the load link bit (LL bit) is also unavailable.

The VR4111 executes all load/store instructions in the programmed sequence. Therefore, the SYNC instruction is treated as a NOP instruction.

(3) Addition of sum-of-products instructions

The VR4111 has a dedicated sum-of-products operation core in the CPU and additional integer sum-of-products operation instructions, in order to execute sum-of-products operation at high speeds. Note that these instructions are not correctly executed with any other processors in the VR Series.

The operations by the sum-of-products instructions are as follows:

(a) MADD16 (Multiply and Add 16-bit Integer)

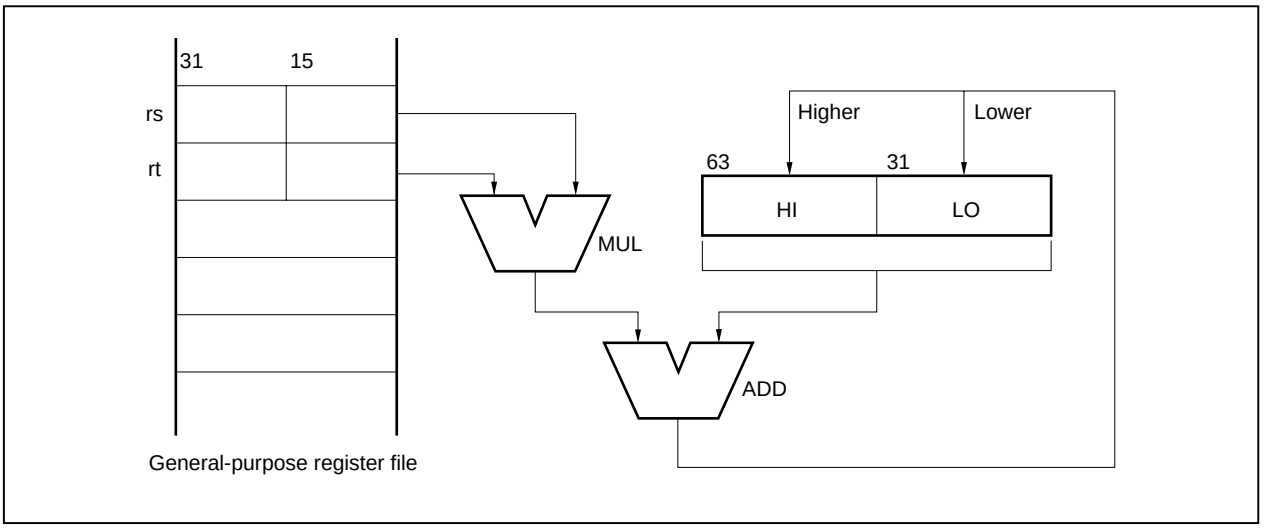
This instruction multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as signed 16-bit integers. Bits 62 through 15 of both the operands must be sign-extended.

The result of the multiplication is added to a 64-bit value combining special registers HI and LO. The lower word (64 bits) of the result is loaded to special register LO, and the higher word is loaded to HI.

An integer overflow exception does not occur.

Figure 3-3 outlines the operation of the MADD16 instruction.

Figure 3-3. Operation of MADD16 Instruction



(b) DMADD16 (Doubleword Multiply and Add 16-bit register)

This instruction multiplies the contents of general-purpose register rs by the contents of general-purpose register rt. Both the operands are treated as signed 16-bit integers. Bits 62 through 15 of both the operands must be sign-extended.

The result of the multiplication is added to the value of special register LO. The result of the addition is treated as a signed integer. The 64-bit result is loaded to special register LO.

An integer overflow exception does not occur.

This operation is defined in the 64-bit mode and 32-bit kernel mode. If this instruction is encountered in the 32-bit user/supervisor mode, a reserved instruction exception occurs.

(4) Addition of power mode instructions

The VR4111 supports three power modes to lower the power consumption, and therefore, has dedicated instructions that set these modes. Note that the power mode instructions are not correctly executed by any other processors in the VR Series.

The operations of the power mode instructions are as follows:

(a) Standby

This instruction places the processor in the Standby mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus (internal) has entered the idle status, the internal clock is fixed to high level, and the pipeline operation is stopped.

In the Standby mode, the PLL, clocks related to timers/interrupts, and interface clocks to the peripheral function blocks (TClock and MasterOut) operate normally.

When the processor is in the Standby mode it is returned to the Fullspeed mode by any interrupt including an internally generated timer interrupt.

(b) Suspend

This instruction places the processor in the Suspend mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus has entered the idle status, the internal clock and TClock are fixed to high level, and the pipeline operation and interfacing to the peripheral function blocks are stopped.

In the Suspend mode, the PLL, clocks related to timers/interrupts, and MasterOut operate normally.

The processor remains in the Suspend mode until it accepts an interrupt. When the processor accepts an interrupt, it returns to the Fullspeed mode.

(c) Hibernate

This instruction places the processor in the Hibernate mode from the Fullspeed mode.

When instruction execution has proceeded to the WB stage, and the SysAD bus has entered the idle status, all the clocks are fixed to high level, and the pipeline operation is stopped.

The processor remains in the Hibernate mode until either the POWER pin is asserted active or the WakeUp timer interrupt occurs. The processor returns to the Fullspeed mode when the POWER pin is asserted active, when the WakeUp Timer interrupt occurs, or when the DCD# pin is asserted active.

The CPU and peripheral units, including clock-related units, stop their operations in Hibernate mode.

3.3.2 MIPS16 instruction set

MIPS16 is an instruction set using 16-bit instructions. By using this instruction set, the memory capacity can be substantially reduced and the system cost can be lowered. MIPS16 is compatible with the MIPS I, II, and III instruction sets, and can be used with the existing instruction codes. Moreover, the instruction length can be changed between 32 bits and 16 bits.

Caution The 16-bit instruction codes can be executed only by a processor that supports the MIPS16 instruction set. At present, the MIPS16 instruction set is supported only by products employing the VR4110 core. Therefore, the VR4111 can execute a program using the existing 32-bit instructions without any modification, but the other processors (such as the VR4100 and VR4102™) cannot execute a VR4111 program including the 16-bit instructions.

3.4 System Control Coprocessor (CP0)

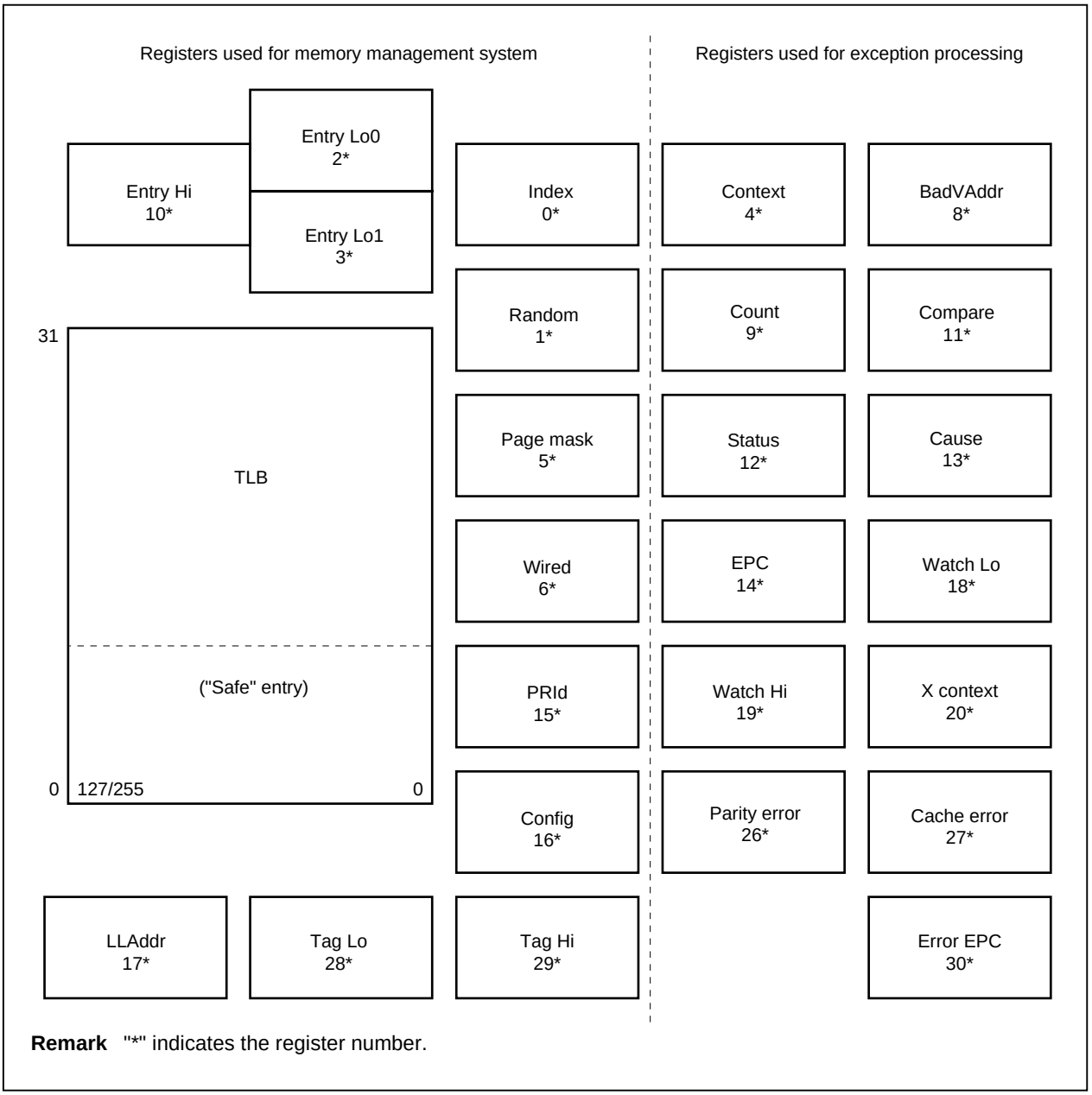
CP0 supports memory management, address translation, exception processing, and privilege operations. CP0 has the registers shown in Table 3-2, and a 32-entry TLB.

The basic configuration of the CP0 registers of the VR4111 is the same as that of the VR4300 and VR4400. However, because the number of entries of TLB, page size, cache size, physical address space, and system interface differ between the VR4111 and VR4300/VR4400, the bit configuration and settings differ. For details, refer to **VR4111 User's Manual**.

3.4.1 CP0 registers

All the CP0 registers that can be used with the VR4111 are shown below. Writing to or reading from an unused register (RFU) is undefined. In the 32-bit mode, the higher 32 bits of 64-bit registers are masked.

Figure 3-4. CP0 Registers and TLB



Remark "*" indicates the register number.

Table 3-2. CP0 Registers

No.	Register	Description
0	Index	Programmable pointer to TLB array
1	Random	Dummy random pointer to TLB array (read-only)
2	Entry Lo0	Latter half of TLB entry for even-number VPN
3	Entry Lo1	Latter half of TLB entry for odd-number VPN
4	Context	Pointer to virtual PTE table of kernel in 32-bit mode
5	Page mask	Specifies page size
6	Wired	Number of wired TLB entries
7	–	RFU (Reserved for Future Use)
8	BadVAddr	Indicates virtual address at which error occurs last
9	Count	Timer count
10	Entry Hi	First half of TLB entry (including ASID)
11	Compare	Timer compare value
12	Status	Sets operation status
13	Cause	Indicates cause of last exception
14	EPC	Exception program counter
15	PRId	Processor revision ID
16	Config	Sets memory system mode
17	LLAddr	RFU
18	Watch Lo	Lower bits of memory reference trap address
19	Watch Hi	Higher bits of memory reference trap address
20	X context	Pointer to virtual PTE table of kernel in 64-bit mode
21 to 25	–	RFU
26	Parity error[Note]	Parity bit of cache
27	Cache error[Note]	Error and status register of cache
28	Tag Lo	Cache tag register, low
29	Tag Hi	Cache tag register, high (reserved register)
30	Error EPC	Error exception program counter
31	–	RFU

Note These errors are defined to maintain compatibility between the VR4100 and VR4111, and are not used by the hardware of the VR4111.

3.5 Data Format and Addressing

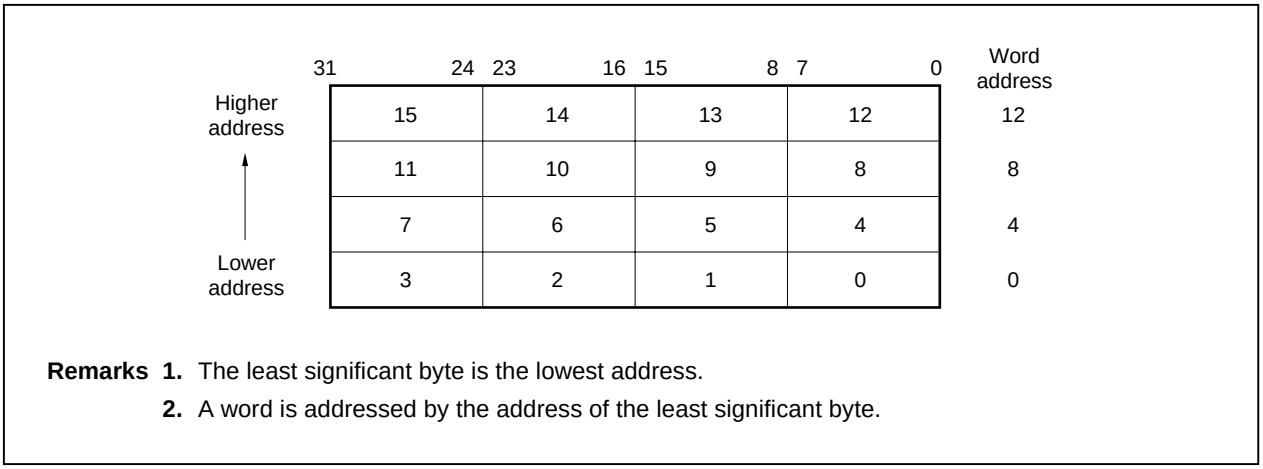
The VR4111 uses the following four data formats:

- Double word (64 bits)
- Word (32 bits)
- Half word (16 bits)
- Byte (8 bits)

The byte ordering is set by the BE bit of the config register. With the current VR4111, set little endian.

The byte ordering (endian) can be inverted during operation by setting the RE bit of the status register. However, be sure not to set this to 1 with the current VR4111.

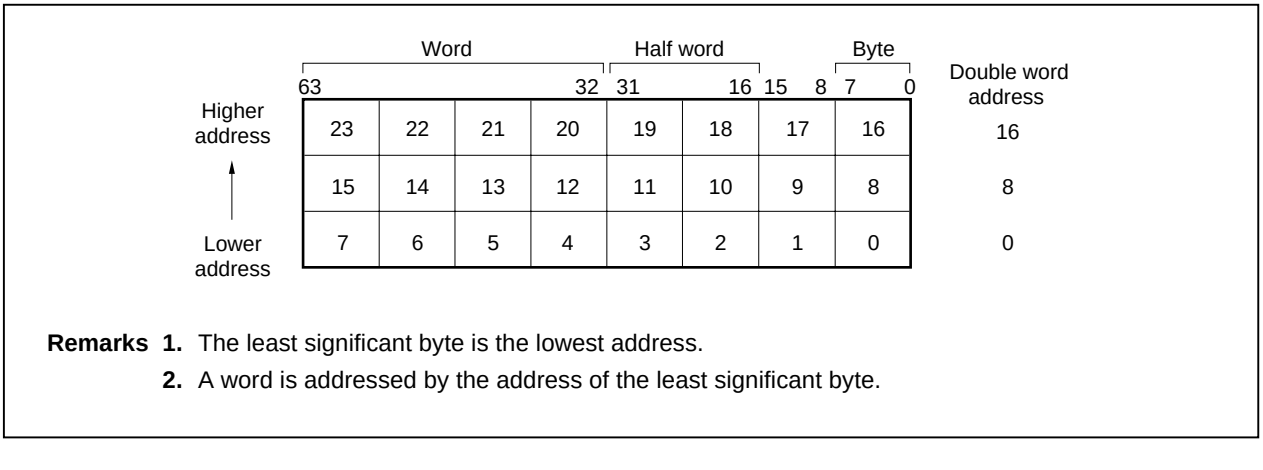
Figure 3-5. Byte Address in Word: Little Endian



Remarks 1. The least significant byte is the lowest address.

2. A word is addressed by the address of the least significant byte.

Figure 3-6. Byte Address in Double Word: Little Endian



Remarks 1. The least significant byte is the lowest address.

2. A word is addressed by the address of the least significant byte.

3.6 Virtual Storage

The VR4111 has a virtual storage management mechanism using TLB.

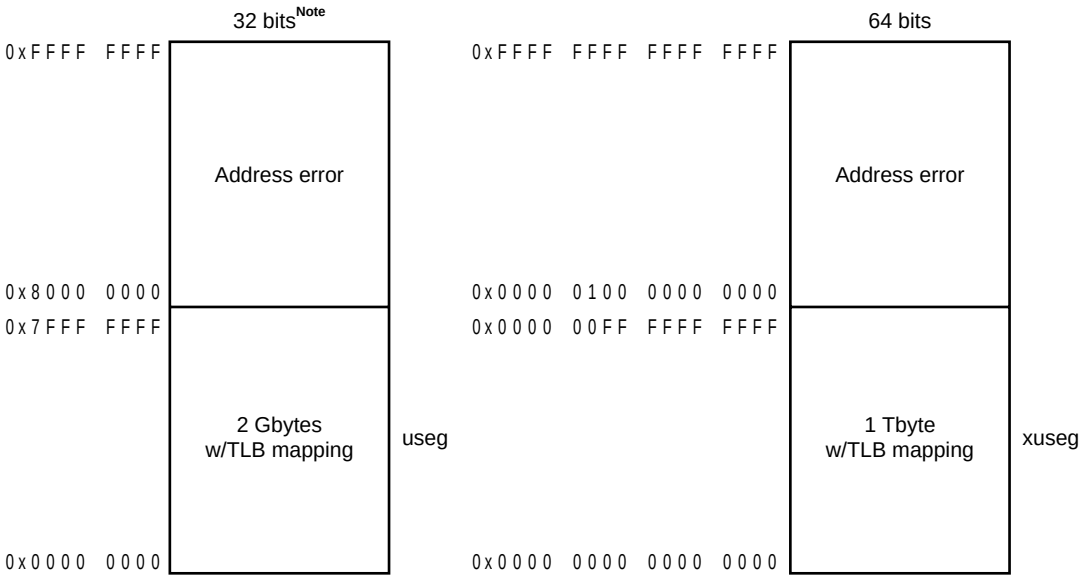
Virtual addresses are used for address management by software or address calculation of the pipeline. To access memories for program fetch and data access, and internal I/O and external I/O, physical addresses translated by TLB are used.

Note that part of the virtual address space is not translated by TLB, but is translated to physical addresses by merely changing specific addresses. If only this part of the address space is used, the VR4111 can be treated in the same manner as a CPU that operates with physical addresses.

3.6.1 Virtual address space

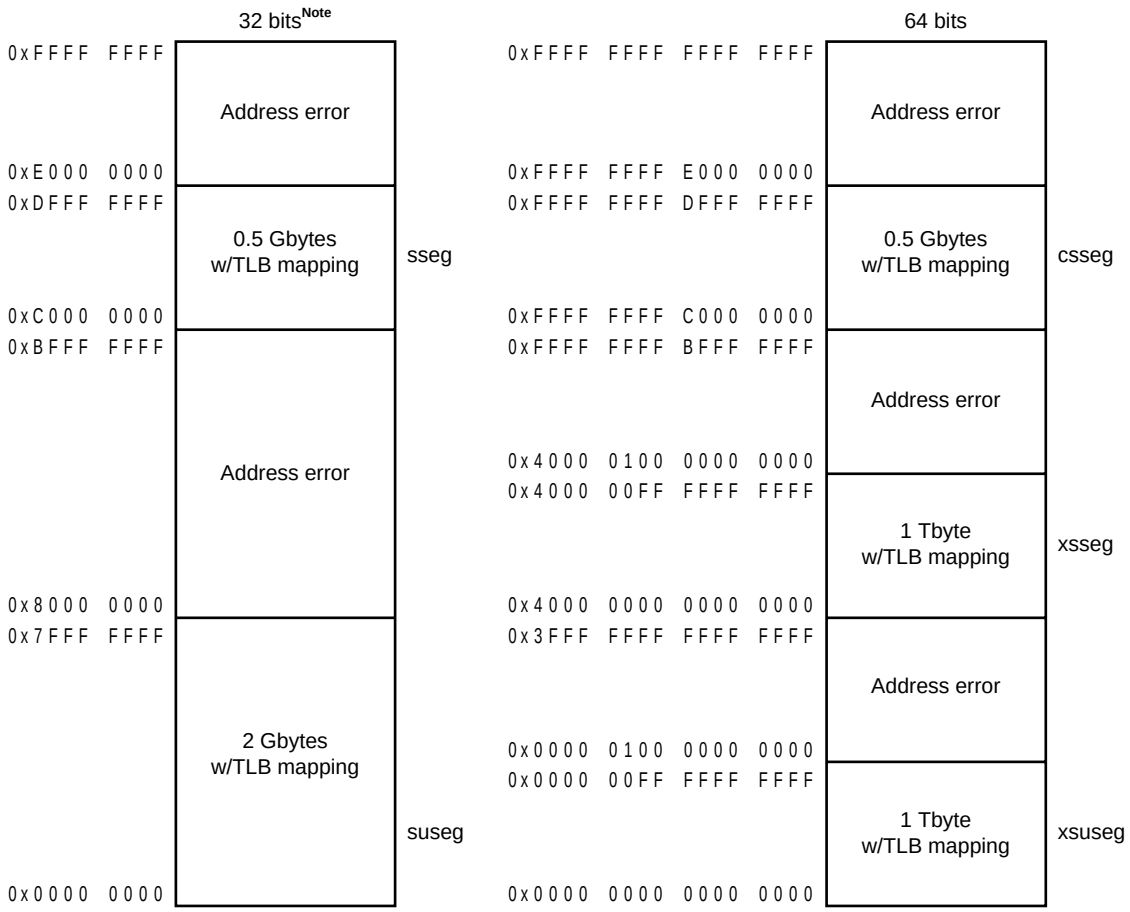
The VR4111 has two operation modes, 32-bit mode and 64-bit mode, and three types of operating modes: user mode, supervisor mode, and kernel mode. The virtual address space in each mode is shown below.

Figure 3-7. User Mode Address Space



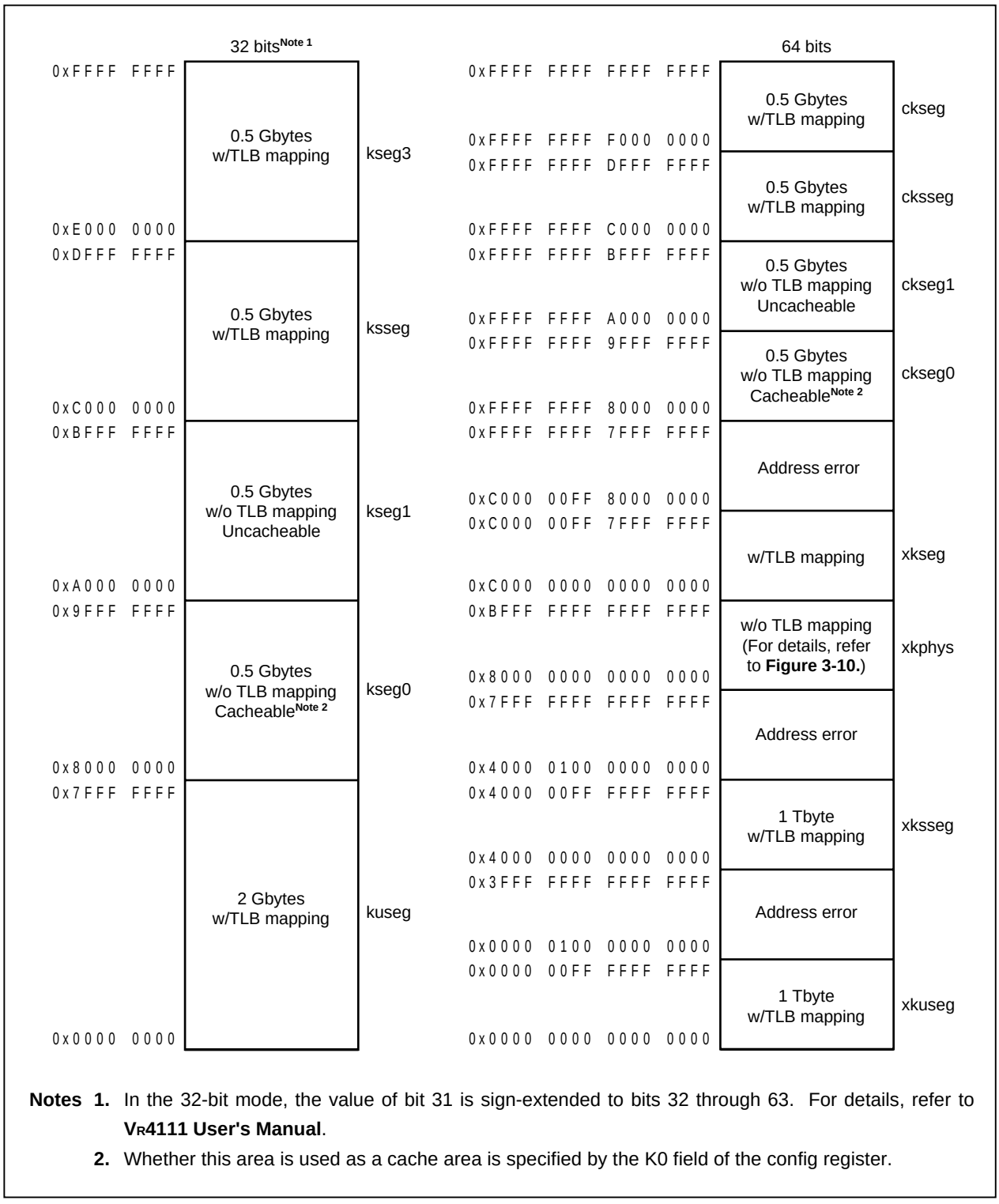
Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4111 User's Manual**.

Figure 3-8. Supervisor Mode Address Space



Note In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4111 User's Manual**.

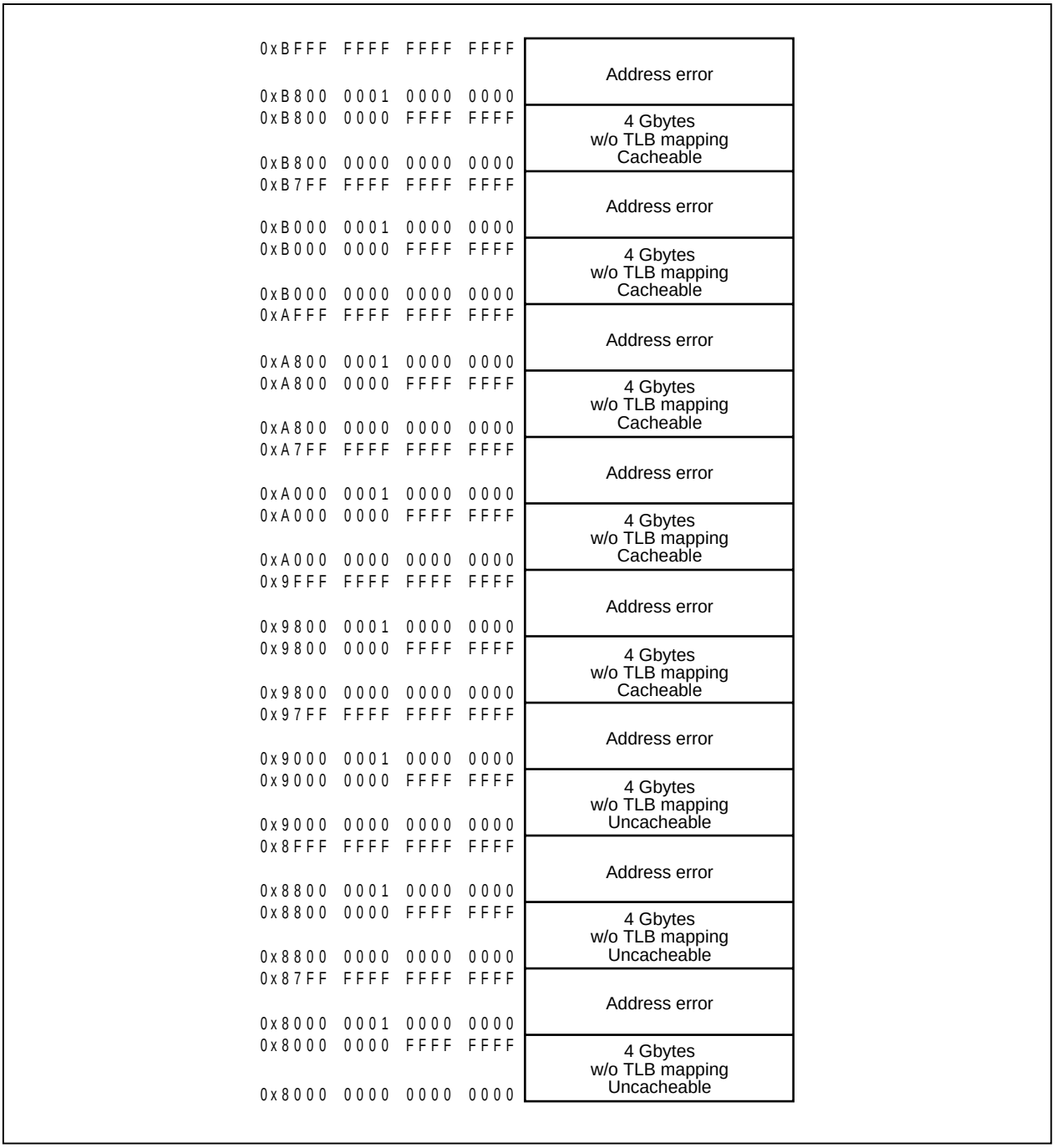
Figure 3-9. Kernel Mode Address Space



Notes 1. In the 32-bit mode, the value of bit 31 is sign-extended to bits 32 through 63. For details, refer to **VR4111 User's Manual**.

2. Whether this area is used as a cache area is specified by the K0 field of the config register.

Figure 3-10. Details of xkphys Area



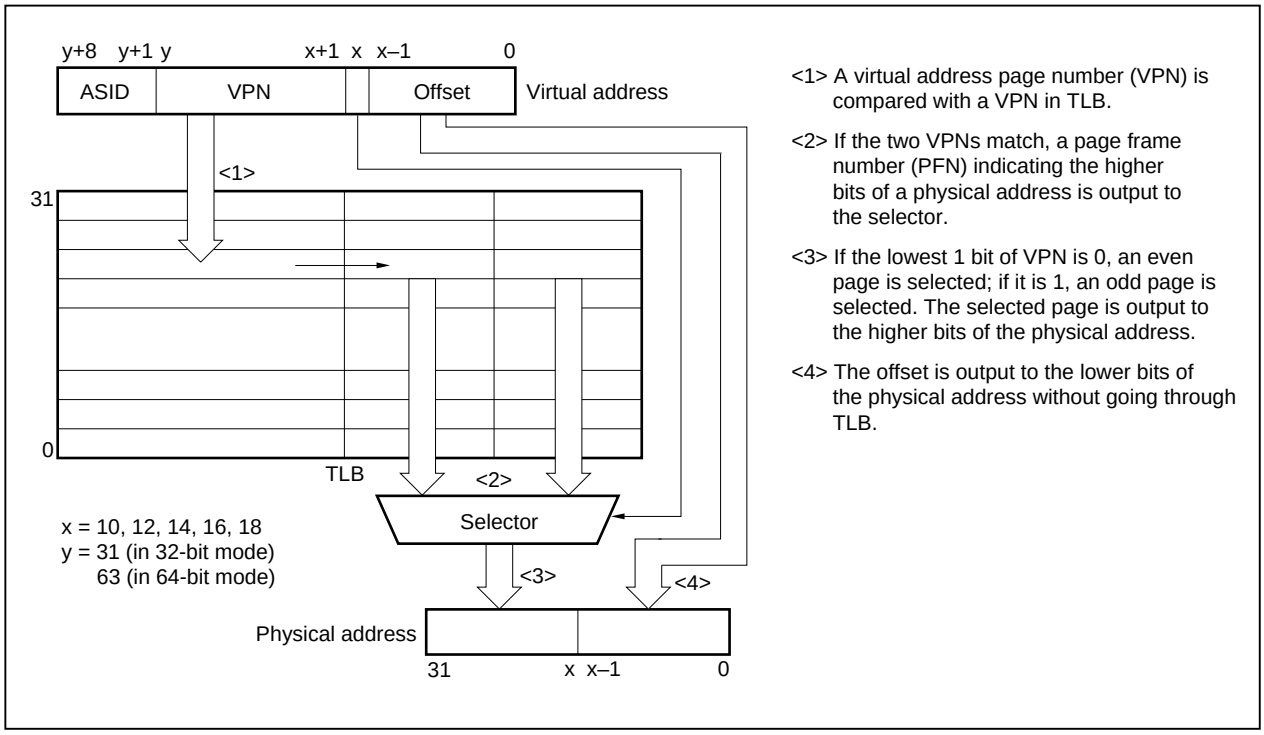
3.6.2 Address translation

Virtual addresses are translated into physical addresses by the internal TLB (Translation Lookaside Buffer) in page units. The TLB has a full-associative configuration and has 64 entries at the virtual address side and 32 entries at the physical address side. The page size is variable from 1 Kbyte to 256 Kbytes.

If a TLB entry is not found, a TLB refill exception occurs in the 32-bit mode, and an XTLB refill exception occurs in the 64-bit mode. Change the contents of the TLB in software.

The following figure outlines address translation.

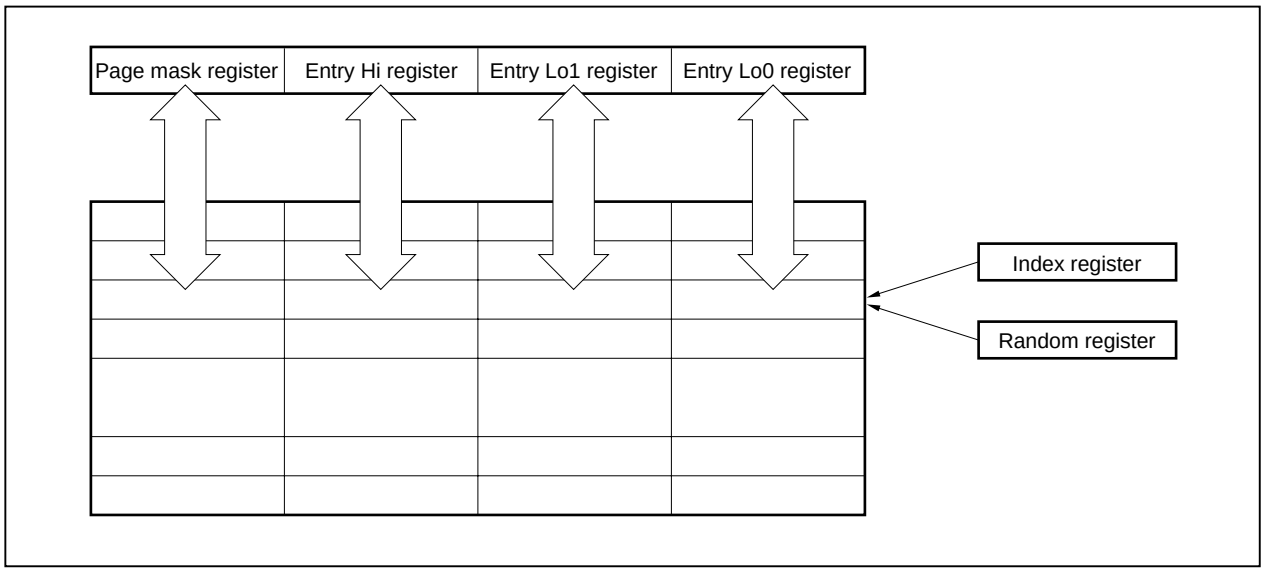
Figure 3-11. Outline of Address Translation



The TLB entry is read or written by loading/storing between the TLB entry indicated by the index register and the random register, entry Hi, entry Lo1, entry Lo0, and page mask registers.

How the TLB is manipulated is illustrated below.

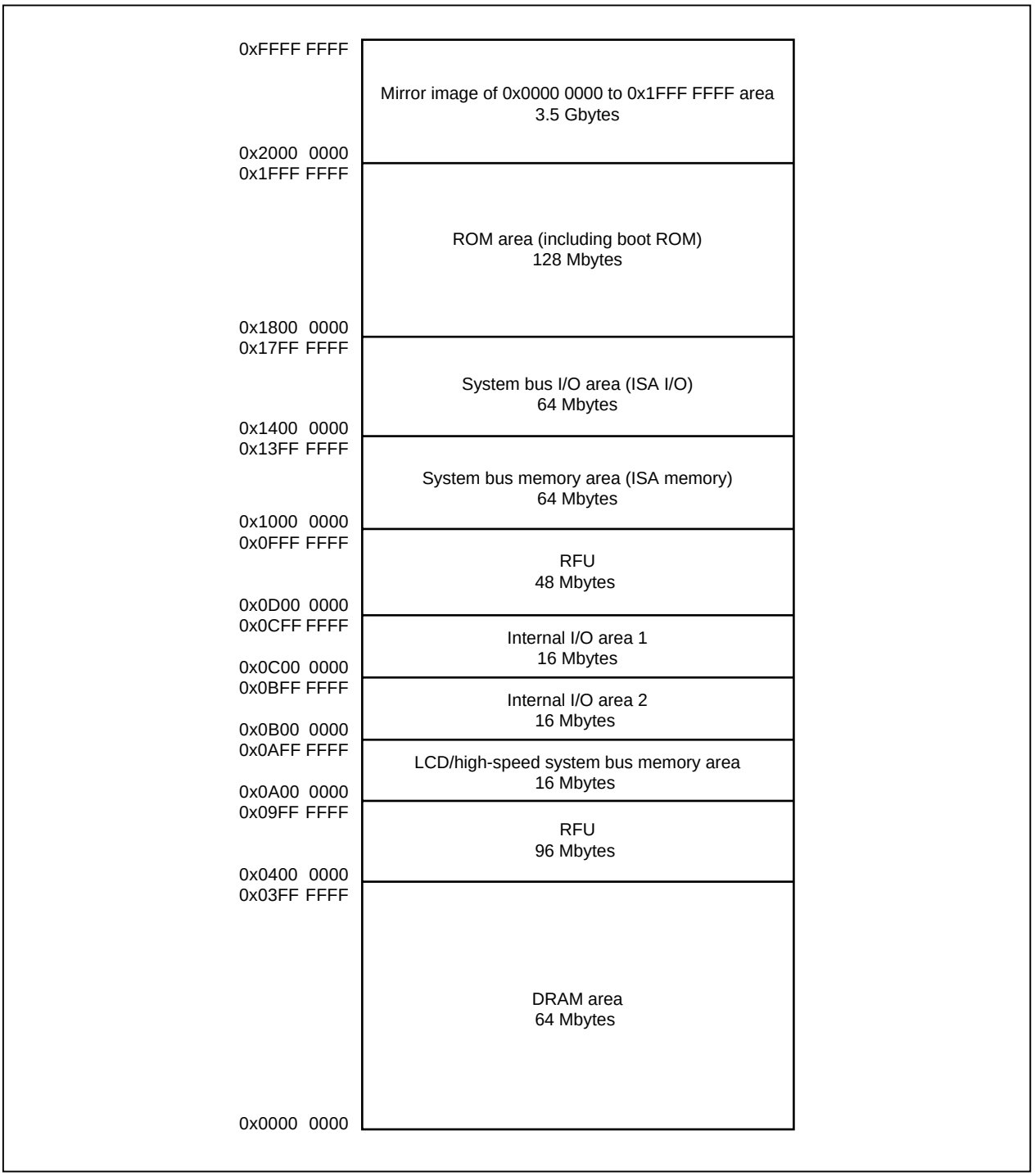
Figure 3-12. Outline of TLB Manipulation



3.7 Physical Address Space

Using a 32-bit address, the processor physical address space encompasses 4 Gbytes. The VR4111 uses this 4-Gbyte address space as shown in Figure 3-13.

Figure 3-13. VR4111 Physical Address Space



3.7.1 ROM address space

The ROM address space differs depending on the bit width of the memory data bus and the capacity of the ROM being used.

- The bit width of the memory data bus is specified by the setting of the DBUS32 pin.
- The ROM capacity is set via the ROM64 bit of the BCUCNTREG1 register or the EXT_ROM64 bit of the BCUCNTREG3 register.

The physical addresses of the ROM space are listed below.

Table 3-3. ROM Addresses (When Using 16-Bit Data Bus)

Physical Address	ADD (25:0)	When Using 32-Mbit ROM (DBUS32 = 0, ROM64 = 0)	When Using 64-Mbit ROM (DBUS32 = 0, ROM64 = 1)
0x1FFF FFFF to 0x1FC0 0000	0x3FF FFFF to 0x3C0 0000	BANK 3 (ROMCS3#)	BANK 3 (ROMCS3#)
0x1FBF FFFF to 0x1F80 0000	0x3BF FFFF to 0x380 0000	BANK 2 (ROMCS2#)	
0x1F7F FFFF to 0x1F40 0000	0x37F FFFF to 0x340 0000	BANK 1 (ROMCS1#)	BANK 2 (ROMCS2#)
0x1F3F FFFF to 0x1F00 0000	0x33F FFFF to 0x300 0000	BANK 0 (ROMCS0#)	
0x1EFF FFFF to 0x1E80 0000	0x2FF FFFF to 0x280 0000	RFU	BANK 1 (ROMCS1#)
0x1E7F FFFF to 0x1E00 0000	0x27F FFFF to 0x200 0000		BANK 0 (ROMCS0#)
0x1DFF FFFF to 0x1800 0000	0x1FF FFFF to 0x000 0000		RFU

Table 3-4. ROM Addresses (When Using 32-Bit Data Bus)

(a) When using 32-Mbit expansion ROM

Physical Address	ADD (25:0)	When Using 32-Mbit ROM (DBUS32 = 1, ROM64 = 0, EXT_ROM64 = 0)	When Using 64-Mbit ROM (DBUS32 = 1, ROM64 = 1, EXT_ROM64 = 0)
0x1FFF FFFF to 0x1F80 0000	0x3FF FFFF to 0x380 0000	BANK 1 (ROMCS1#)	BANK 1 (ROMCS1#)
0x1F7F FFFF to 0x1F00 0000	0x37F FFFF to 0x300 0000	BANK 0 (ROMCS0#)	
★ 0x1EFF FFFF to 0x1E80 0000	0x2FF FFFF to 0x280 0000	BANK 3 (ROMCS3#)Note	BANK 0 (ROMCS0#)
★ 0x1E7F FFFF to 0x1E00 0000	0x27F FFFF to 0x200 0000	BANK 2 (ROMCS2#)Note	
0x1DFF FFFF to 0x1D80 0000	0x1FF FFFF to 0x180 0000	RFU	BANK 3 (ROMCS3#)Note
0x1D7F FFFF to 0x1D00 0000	0x17F FFFF to 0x100 0000		BANK 2 (ROMCS2#)Note
0x1CFF FFFF to 0x1800 0000	0x0FF FFFF to 0x000 0000		RFU

(b) When using 64-Mbit expansion ROM

Physical Address	ADD (25:0)	When Using 32-Mbit ROM (DBUS32 = 1, ROM64 = 0, EXT_ROM64 = 1)	When Using 64-Mbit ROM (DBUS32 = 1, ROM64 = 1, EXT_ROM64 = 1)
0x1FFF FFFF to 0x1F80 0000	0x3FF FFFF to 0x380 0000	BANK 1 (ROMCS1#)	BANK 1 (ROMCS1#)
0x1F7F FFFF to 0x1F00 0000	0x37F FFFF to 0x300 0000	BANK 0 (ROMCS0#)	
★ 0x1EFF FFFF to 0x1E00 0000	0x2FF FFFF to 0x200 0000	BANK 3 (ROMCS3#)Note	BANK 0 (ROMCS0#)
★ 0x1DFF FFFF to 0x1D00 0000	0x1FF FFFF to 0x100 0000	BANK 2 (ROMCS2#)Note	BANK 3 (ROMCS3#)Note
0x1CFF FFFF to 0x1C00 0000	0x0FF FFFF to 0x000 0000	RFU	BANK 2 (ROMCS2#)Note
★ 0x1BFF FFFF to 0x1800 0000	–		RFU

Note Can be used exclusively from the expansion DRAM.

3.7.2 Internal I/O space

The VR4111 has two types of internal I/O spaces. Each of these spaces in the internal I/O space are described below.

Table 3-5. Internal I/O Space 1

Physical Address	Internal I/O
0x0BFF FFFF to 0x0C00 0080	RFU
0x0C00 007F to 0x0C00 0060	FIR2
0x0C0 005F to 0x0C00 0040	FIR
0x0C00 003F to 0x0C00 0020	HSP (software modem interface)
0x0C00 001F to 0x0C00 0000	SIU (16550)

Table 3-6. Internal I/O Space 2

Physical Address	Internal I/O
0x0BFF FFFF to 0x0B00 0300	RFU
0x0B00 02FF to 0x0B00 02E0	GIU2
0x0B00 02DF to 0x0B00 02C0	PMU2
0x0B00 02BF to 0x0B00 02A0	PIU2
0x0B00 029F to 0x0B00 0280	RFU
0x0B00 027F to 0x0B00 0260	A/D test
0x0B00 025F to 0x0B00 0240	LED
0x0B00 023F to 0x0B00 0220	RFU
0x0B00 021F to 0x0B00 0200	ICU2
0x0B00 01FF to 0x0B00 01E0	RFU
0x0B00 01DF to 0x0B00 01C0	RTC2
0x0B00 01BF to 0x0B00 01A0	DSIU
0x0B00 019F to 0x0B00 0180	KIU
0x0B00 017F to 0x0B00 0160	AIU
0x0B00 015F to 0x0B00 0140	RFU
0x0B00 013F to 0x0B00 0120	PIU1
0x0B00 011F to 0x0B00 0100	GIU1
0x0B00 00FF to 0x0B00 00E0	DSU
0x0B00 00DF to 0x0B00 00C0	RTC1
0x0B00 00BF to 0x0B00 00A0	PMU
0x0B00 009F to 0x0B00 0080	ICU1
0x0B00 007F to 0x0B00 0060	CMU
0x0B00 005F to 0x0B00 0040	DCU
0x0B00 003F to 0x0B00 0020	DMAAU
0x0B00 001F to 0x0B00 0000	BCU

3.7.3 DRAM address space

The DRAM address space differs depending on the bit width of the memory data bus and the capacity of the DRAM being used.

- The bit width of the memory data bus is specified by the setting of the DBUS32 pin.
- The DRAM capacity is set via the DRAM64 bit of BCUCNTREG1 register or EXT_DRAM64 bit of BCUCNTREG3 register.

The physical addresses of the DRAM space are listed in Tables 3-7 and 3-8.

Table 3-7. DRAM Addresses (When Using 16-Bit Data Bus)

Physical Address	When Using 16-Mbit DRAM (DBUS32 = 0, DRAM64 = 0)	When Using 64-Mbit DRAM (DBUS32 = 0, DRAM64 = 1)
0x03FF FFFF to 0x0200 0000	RFU	RFU
0x01FF FFFF to 0x0180 0000		BANK 3 (MRAS3#/UUCAS#)
0x017F FFFF to 0x0100 0000		BANK 2 (MRAS2#/ULCAS#)
0x00FF FFFF to 0x0080 0000		BANK 1 (MRAS1#)
0x007F FFFF to 0x0060 0000	BANK 3 (MRAS3#/UUCAS#)	BANK 0 (MRAS0#)
0x005F FFFF to 0x0040 0000	BANK 2 (MRAS2#/ULCAS#)	
0x003F FFFF to 0x0020 0000	BANK 1 (MRAS1#)	
0x001F FFFF to 0x0000 0000	BANK 0 (MRAS0#)	

Table 3-8. DRAM Addresses (When Using 32-Bit Data Bus)

(a) When using 16-Mbit expansion DRAM

	Physical Address	When Using 16-Mbit DRAM (DBUS32 = 1, DRAM64 = 0, EXT_DRAM64 = 0)	When Using 64-Mbit DRAM (DBUS32 = 1, DRAM64 = 1, EXT_DRAM64 = 0)
	0x03FF FFFF to 0x0280 0000	RFU	RFU
	0x027F FFFF to 0x0240 0000		BANK 3 (ROMCS3#)Note
	0x023F FFFF to 0x0200 0000		BANK 2 (ROMCS2#)Note
	0x01FF FFFF to 0x0180 0000		BANK 1 (MRAS1#)
	0x017F FFFF to 0x0100 0000		
★	0x00FF FFFF to 0x00E0 0000	BANK 3 (ROMCS3#)Note	BANK 0 (MRAS0#)
	0x00DF FFFF to 0100C0 0000		
★	0x00BF FFFF to 0x00A0 0000	BANK 2 (ROMCS2#)Note	
	0x009F FFFF to 0x0080 0000		
	0x007F FFFF to 0x0060 0000	BANK 1 (MRAS1#)	
	0x005F FFFF to 0x0040 0000		
	0x003F FFFF to 0x0020 0000	BANK 0 (MRAS0#)	
	0x001F FFFF to 0x0000 0000		

(b) When using 64-Mbit expansion DRAM

	Physical Address	When Using 16-Mbit DRAM (DBUS32 = 1, DRAM64 = 0, EXT_DRAM64 = 1)	When Using 64-Mbit DRAM (DBUS32 = 1, DRAM64 = 1, EXT_DRAM64 = 1)
	0x03FF FFFF to 0x0300 0000	RFU	BANK 3 (ROMCS3#)Note
	0x02FF FFFF to 0x0280 0000		BANK 2 (ROMCS2#)Note
★	0x027F FFFF to 0x0200 0000	BANK 3 (ROMCS3#)Note	
	0x01FF FFFF to 0x0180 0000		BANK 1 (MRAS1#)
★	0x017F FFFF to 0x0100 0000	BANK 2 (ROMCS2#)Note	
	0x00FF FFFF to 0x0080 0000		BANK 0 (MRAS0#)
	0x007F FFFF to 0x0060 0000	BANK 1 (MRAS1#)	
	0x005F FFFF to 0x0040 0000		
	0x003F FFFF to 0x0020 0000	BANK 0 (MRAS0#)	
	0x001F FFFF to 0x0000 0000		

Note Can be used exclusively from the expansion ROM.

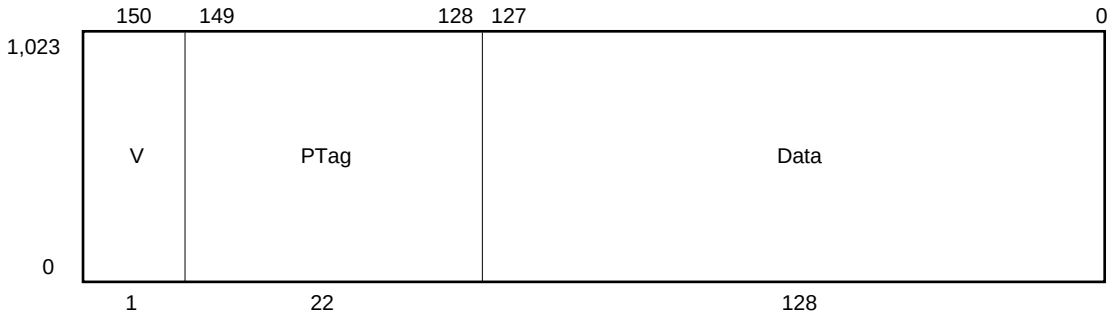
3.8 Cache

(1) Instruction cache

The instruction cache has the following features:

- On-chip cache memory
- Capacity: 16 Kbytes
- Direct mapping mode
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-14. Format of Instruction Cache



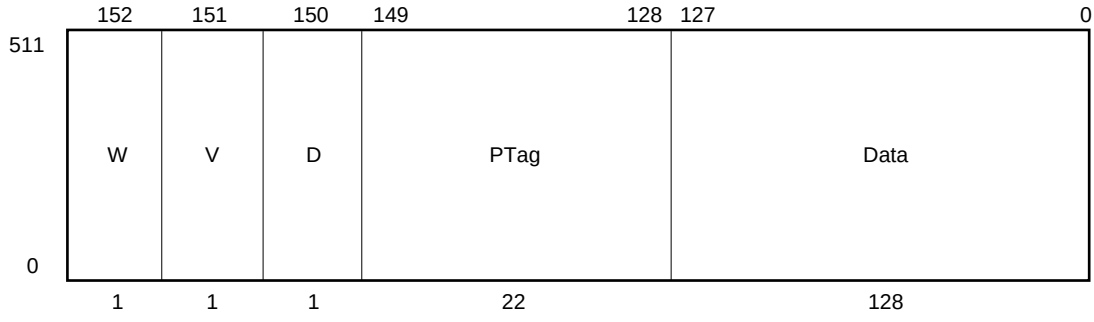
PTag: Physical tag (bits 31 to 10 of physical address)
V: Valid bit
Data: Cache data

(2) Data cache

The data cache has the following features:

- On-chip cache memory
- Capacity: 8 Kbytes
- Write back
- Direct mapping mode
- Virtual index address
- Physical tag check
- 4-word (16-byte) cache line

Figure 3-15. Format of Data Cache



W: Write back bit
V: Valid bit
D: Dirty bit
PTag: Physical tag (bits 31 to 10 of physical address)
Data: Cache data

3.9 Exception Processing

The VR4111 enters the kernel mode in which interrupts are disabled when an exception occurs, and executes an exception handler from a fixed exception vector address. To restore from the exception, the program counter, operating mode, and interrupt enable information must be restored to the original status. Save this information when the interrupt occurs.

When an interrupt occurs, the EPC register holds the address of the instruction that has caused the exception, or the address of the instruction immediately before if the exception has occurred in the branch delay slot. This means that the EPC register stores the address from which execution is to be started after the exception has been processed. After reset and on occurrence of NMI, the EPC register holds a restart address.

Table 3-9. Types of Exceptions

Exception	Symbol	Description
Cold reset	–	This exception occurs if the ColdReset# (internal) and Reset# (internal) signals are simultaneously asserted active (for details, refer to **Figures 4-1** through **4-5**). As a result, the instruction execution is stopped, and the handler on the reset vector is executed. The internal status, except some bits of the status registers, is undefined.
Soft reset	–	This exception occurs if the Reset# (internal) signal is asserted active. As a result, the instruction execution is stopped, and the handler on the reset vector is executed. The internal status before soft reset is retained. However, the current VR4111 does not support soft reset.
NIMI	–	This exception occurs if the NMI (internal) signal is asserted active.
TLB refill	TLBL/TLBS	This exception occurs if there is no TLB entry that matches an address to be referenced in the 32-bit mode.
Expanded addressing TLB non-coincidence	TLBL/TLBS	This exception occurs if there is no TLB entry that matches an address to be referenced in the 64-bit mode.
TLB invalid	TLBL/TLBS	This exception occurs if the TLB entry that matches the virtual address to be referenced is invalid (V bit = 0).
TLB modify	Mod	This exception occurs if the TLB entry that matches the virtual address to be referenced is valid but is disabled from being written (D bit = 0) when the store instruction is executed.
Bus error	IBE/DBE	This exception occurs when the external agent indicates an error of data on the SysCmd bus by using an external interrupt to the bus interface (bus time-out, bus parity error, or invalid physical memory address or access type).
Address error	AdEL/AdES	This exception occurs if an attempt is made to execute the LH, SH, LW, SW, LD, or SD instruction to the half word/word/double word not located at the half word/word/double word boundary, or if an attempt is made to reference a virtual address that cannot be accessed.
Integer overflow	Ov	This exception occurs if a 2's complement overflow occurs as a result of addition or subtraction.
Trap	Tr	This exception occurs if the condition is true as a result of executing the trap instruction.
System call	Sys	This exception occurs if the SYSCALL instruction is executed.
Breakpoint	Bp	This exception occurs if the BREAK instruction is executed.
Reserved instruction	RI	This exception occurs if an instruction with an undefined op code (bits 31 to 26) or SPECIAL instruction with an undefined op code (bits 5 to 0) is executed.
Coprocessor non-usable	CpU	This exception occurs if the coprocessor instruction is executed when the corresponding coprocessor enable bit is not set.
Interrupt	Int	This exception occurs if one of the eight interrupt sources becomes active.
Cache error	–	This exception occurs if a parity error is detected in the internal cache or system interface.
Watch	WATCH	This exception occurs if an attempt is made to reference a physical address set by the watch Lo/Hi register with the load/store instruction.

The exception vectors and their offset values in the 64-bit and 32-bit modes are shown below.

Table 3-10. Base Address of Exception Vector in 64-Bit Mode (Virtual Address)

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xFFFF FFFF BFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xFFFF FFFF A000 0000 (BEV = 0) 0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0100
TLB refill, EXL = 0	0xFFFF FFFF 8000 0000 (BEV = 0) 0xFFFF FFFF BFC0 0200 (BEV = 1)	0x0000
XTLB refill, EXL = 0		0x0080
Other than above		0x0180

Table 3-11. Base Address of Exception Vector in 32-Bit Mode (Virtual Address)

	Vector Base Address	Vector Offset
Cold reset, soft reset, NMI	0xBFC0 0000 (BEV bit is automatically set to 1.)	0x0000
Cache error	0xA000 0000 (BEV = 0) 0xBFC0 0200 (BEV = 1)	0x0100
TLB refill, EXL = 0	0x8000 0000 (BEV = 0) 0xBFC0 0200 (BEV = 1)	0x0000
XTLB refill, EXL = 0		0x0080
Other than above		0x0180

4. INITIALIZATION INTERFACE

Remark # in a signal name indicates active low.

4.1 Reset Function

The VR4111 can be reset in the following five ways. For details, refer to the **VR4111 User's Manual**.

4.1.1 RTC reset

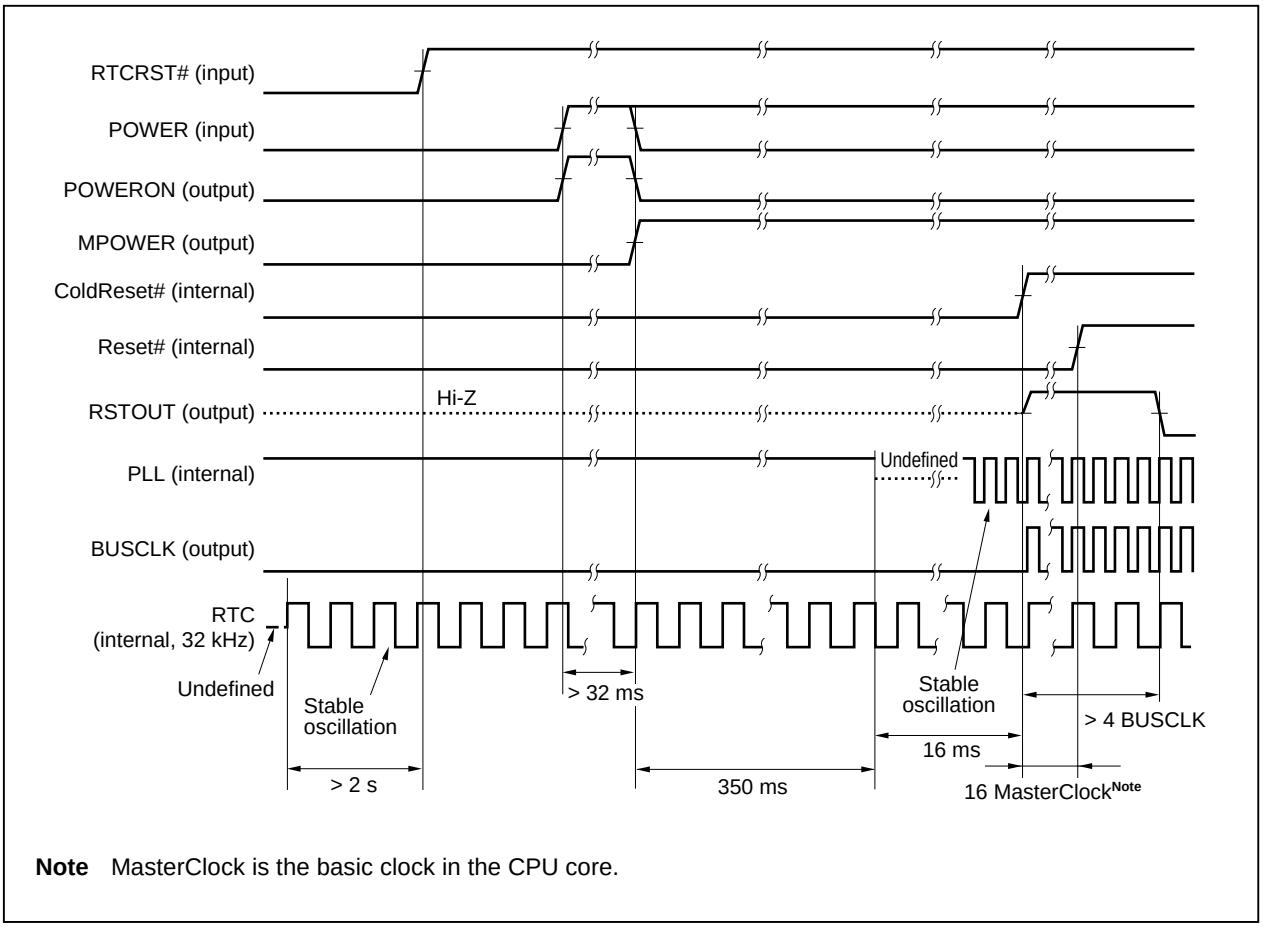
Assert the RTCRST# pin active on power application.

The status of each of the TxD/CLKSEL2, RTS#/CLKSEL1, DTR#/CLKSEL0, DBUS32/GPIO48, MIPS16EN, and GPIO49 pins is sampled at the rising edge of the RTCRST# signal, and is internally initialized by the VR4111.

RTC reset does not save the status information at all, and completely initializes the internal status of the processor. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after RTC reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4111 is reset, completely initialize the processor by software.

Figure 4-1. RTC Reset



Note MasterClock is the basic clock in the CPU core.

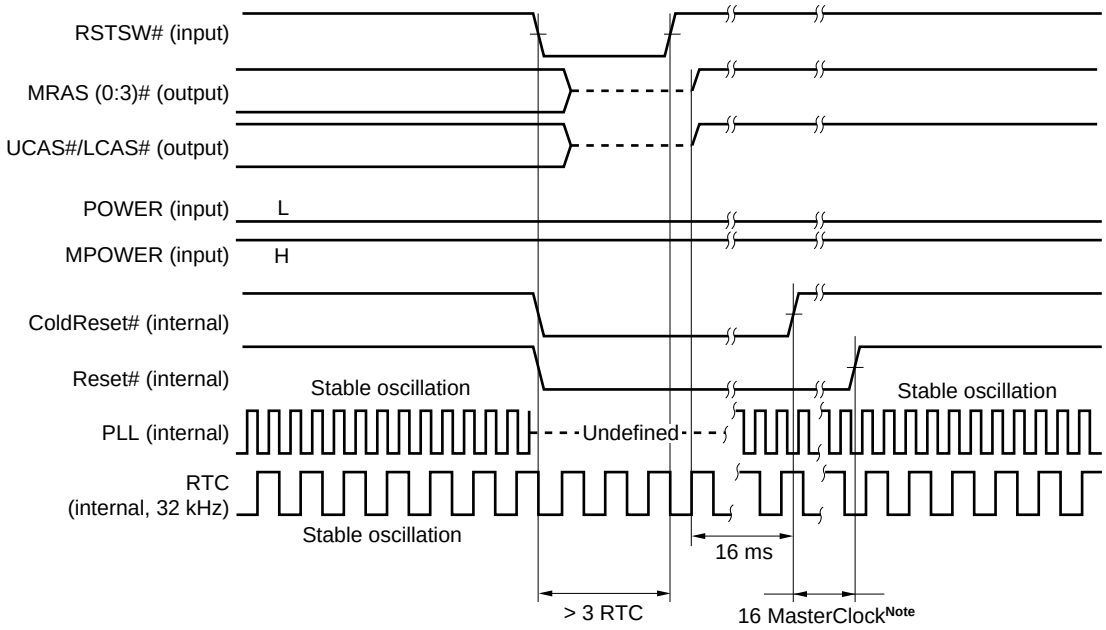
4.1.2 RSTSW

Assert the RSTSW# pin active.

Reset by RSTSW initializes all the internal statuses except the RTC timer and the PMU. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after RSTSW reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4111 is reset, completely initialize the processor by software.

Figure 4-2. RSTSW



Note MasterClock is the basic clock in the CPU core.

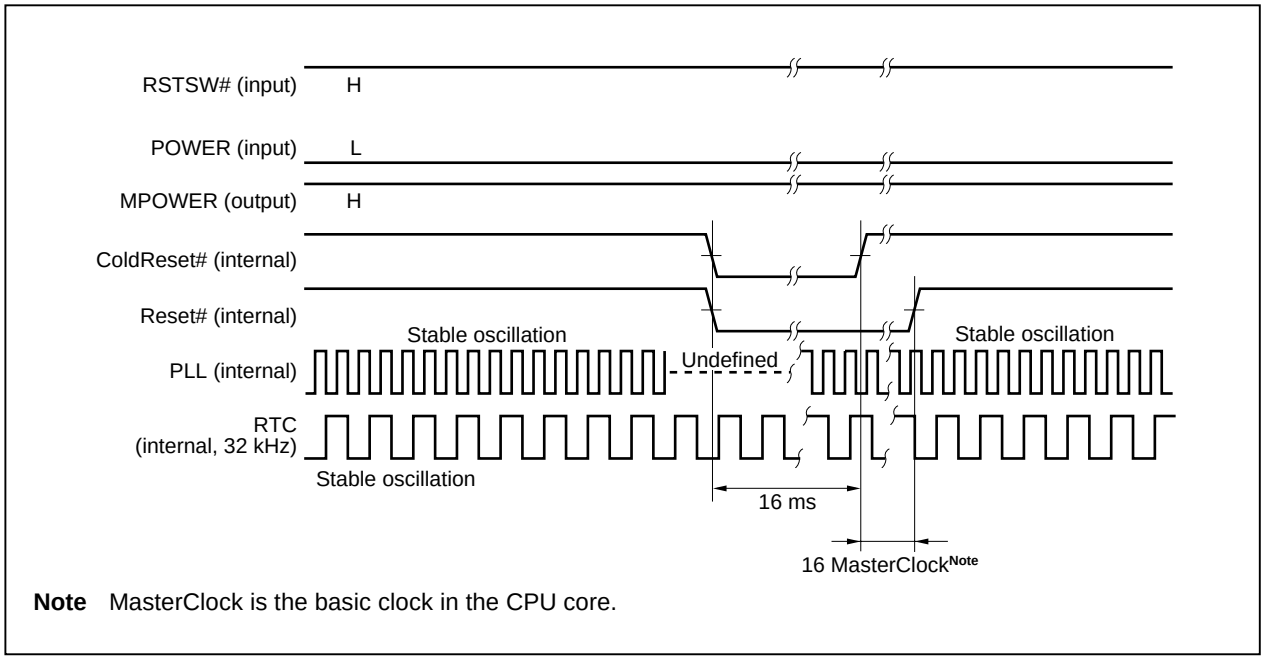
4.1.3 Deadman's SW

The VR4111 is reset if the Deadman's SW is not cleared within a specific time after the Deadman's SW was enabled. For the setting of the Deadman's SW, see **12. DSU (Deadman's SW Unit)**.

Reset by Deadman's SW initializes all the internal statuses except the RTC timer and PMU. Because the DRAM does not enter the self-refresh mode, the contents of the DRAM after Deadman's SW reset are not guaranteed.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4111 is reset, completely initialize the processor by software.

Figure 4-3. Deadman's SW



Note MasterClock is the basic clock in the CPU core.

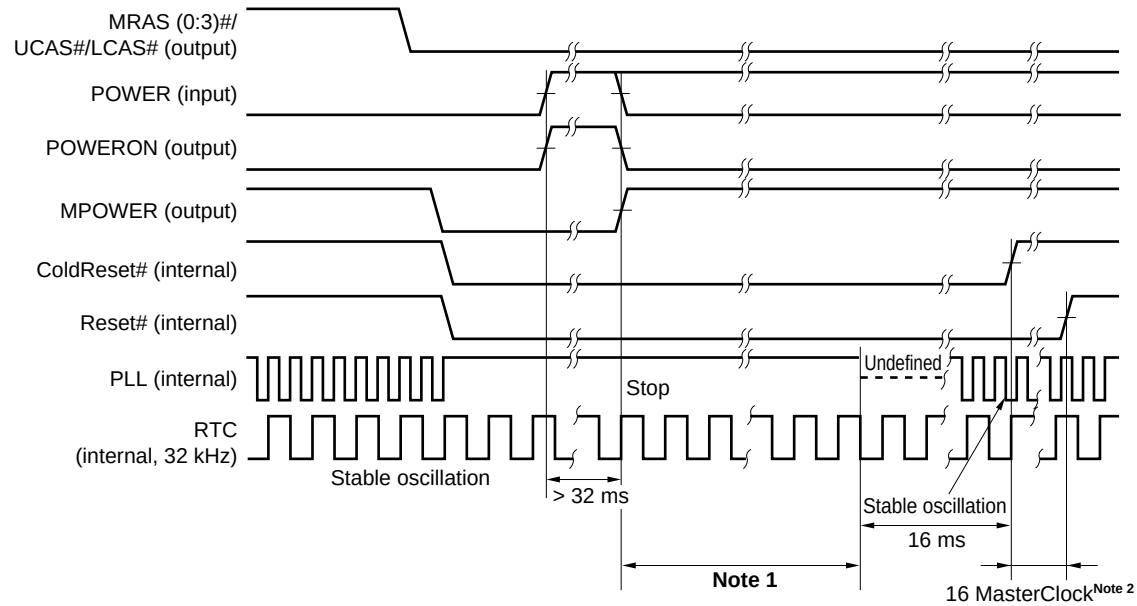
4.1.4 Software shutdown

When the software executes the HIBERNATE instruction, the VR4111 places the DRAM in the self-refresh mode, deasserts the MPOWER pin inactive, and enters the reset status.

Reset by software shutdown initializes all the internal statuses except the RTC timer and the PMU.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4111 is reset, completely initialize the processor by software.

Figure 4-4. Software Shutdown



Notes 1. Wait time until starting. This value can be changed by a setting of the PMUWAITREG register. For details, refer to **VR4111 User's Manual**.

2. MasterClock is the basic clock in the CPU core.

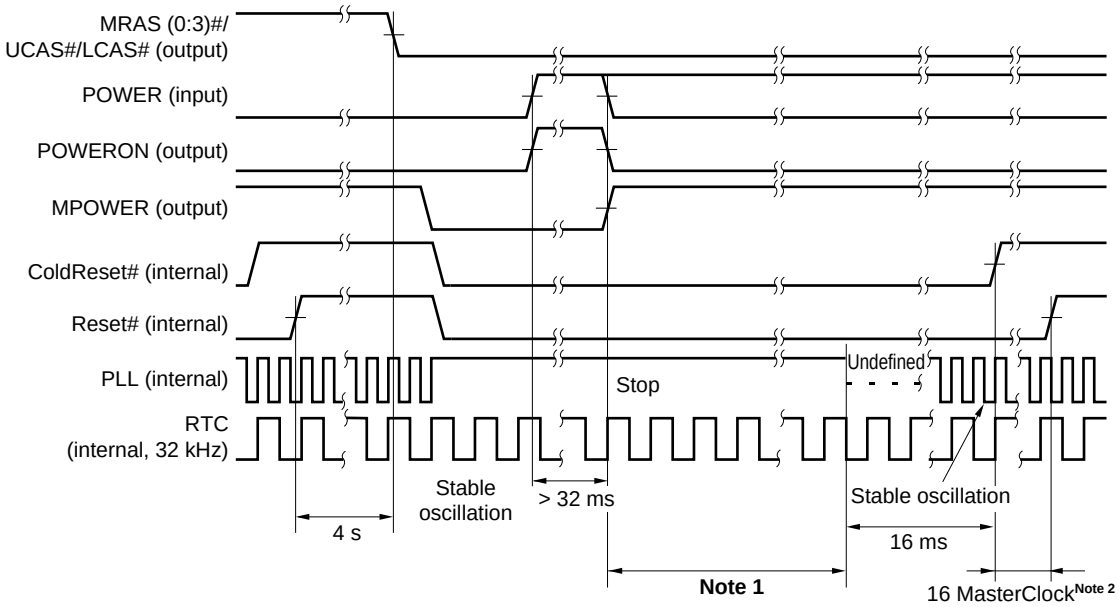
4.1.5 HALTimer shutdown

The VR4111 enters the reset status if the HALTimer is not cleared (the HALTIMERRST bit of the PMUCNTREG register is set to 1) by software within 4 seconds after RTC reset has been cleared.

Reset by HALTimer initializes all the internal statuses except the RTC timer and PMU.

After reset, the processor serves as the master of the system bus, the sequence of the cold reset exception is executed, and accessing the reset vector in the ROM space is started. Because only part of the internal status of the VR4111 is reset, completely initialize the processor by software.

Figure 4-5. HALTimer Shutdown



Notes 1. Wait time until starting. This value can be changed by a setting of the PMUWAITREG register. For details, refer to **VR4111 User's Manual**.

2. MasterClock is the basic clock in the CPU core.

4.2 CPU Core Registers after Reset

Each of the CPU core registers is reset as follows:

- The TS and SR bits of the status register are cleared to 0.
- The ERL and BEV bits of the status register are set to 1.
- The upper-limit value (31) is set to the random register.
- The wired register is initialized to 0.
- Bits 31 through 28 of the config register are cleared to 0, and bits 22 through 3 are set to 0x04800. The other bits are undefined.
- The values of the registers other than above are undefined.

4.3 Power-On Sequence

The causes that change the status of the VR4111 from the Hibernate mode or shutdown status to the Fullspeed mode are called power-on factors. The power-on factors include asserting the POWERON pin active, asserting the DCD# pin active, alarm from the WakeUp timer, and asserting the GPIO (0:3), GPIO (9:12) pins active. When a power-on factor occurs, the VR4111 asserts the POWERON pin active to inform the external circuit that power to the VR4111 is about to be turned ON. Three RTC clocks after the POWERON pin has been asserted active, the VR4111 checks the status of the BATTINH/BATTINT# pin. When the BATTINH/BATTINT# pin is low, the VR4111 deasserts the POWERON pin inactive one RTC clock after checking the BATTINH or GPIO9 pin status, and is not started. If the BATTINH/BATTINT# pin is high, the VR4111 deasserts the POWERON pin inactive three RTC clocks after the checking, asserts the MPOWER pin active, and is started.

Figure 4-6 shows the timing chart where the VR4111 is started. Figure 4-7 shows the timing chart where the VR4111 is not started because the BATTINH/BATTINT# pin is low.

Figure 4-6. Start Sequence of VR4111 (If Started)

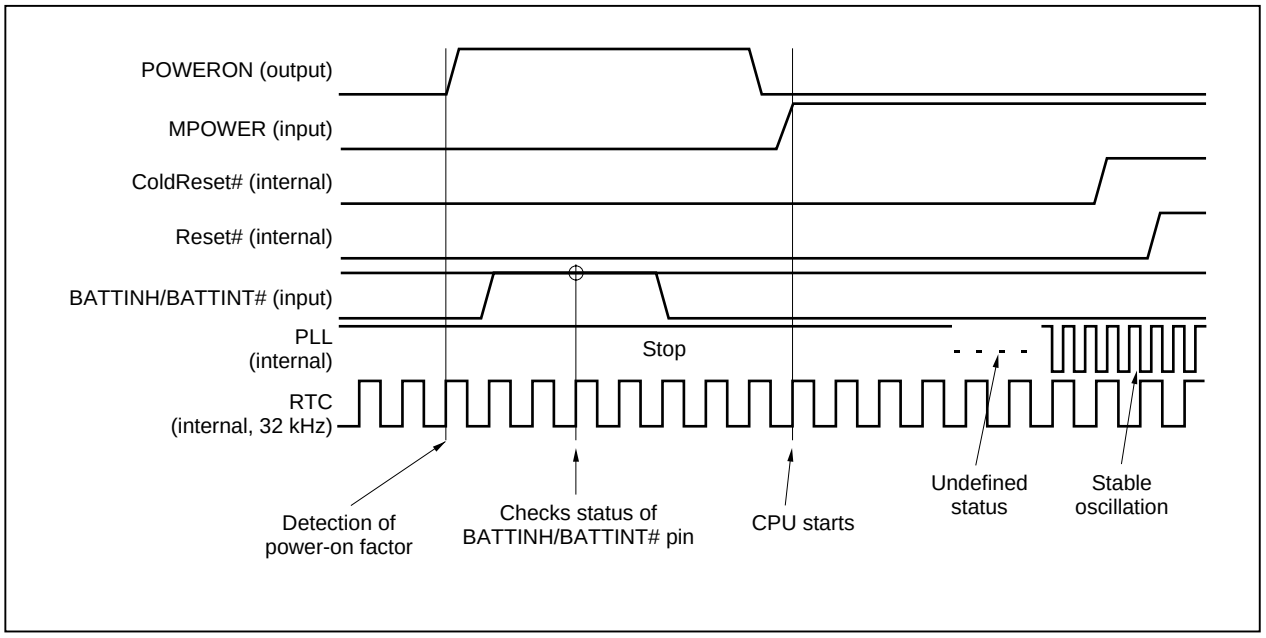
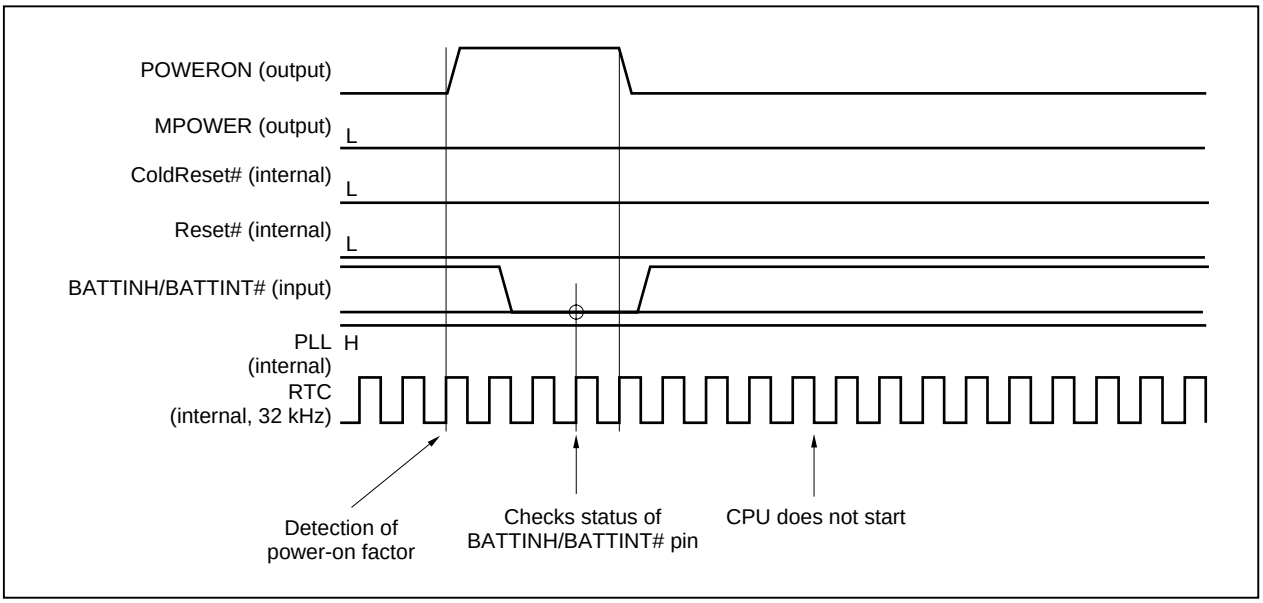


Figure 4-7. Start Sequence of VR4111 (If Not Started)



5. BCU (BUS CONTROL UNIT)

The BCU transfers data received via the VR4110 CPU core and SysAD bus (internal) inside the VR4111. It also controls an external LCD controller, DRAM, ROM (flash memory or mask ROM), and PCMCIA controller via a system bus, and transfers data received via these devices ADD bus and DATA bus.

For the charts of the timing between the VR4111 and each external device controlled by the BCU, see **23. ELECTRICAL SPECIFICATIONS**.

Table 5-1. BCU Registers

Physical Address	Symbol	Function
0x0B00 0000	BCUCNTREG1	BCU control register 1
0x0B00 0002	BCUCNTREG2	BCU control register 2
0x0B00 000A	BCUSPEEDREG	BCU access cycle change register
0x0B00 000C	BCUERRSTREG	BCU bus error status register
0x0B00 000E	BCURFCNTREG	BCU refresh control register
0x0B00 0010	REVIDREG	Peripheral unit revision ID register
0x0B00 0012	BCURFCOUNTREG	BCU refresh cycle count register
0x0B00 0014	CLKSPEEDREG	Clock specify register
0x0B00 0016	BCUCNTREG3	BCU control register 3

6. DMAAU (DMA ADDRESS UNIT)

The DMAAU controls the addresses for the DMA operations between AIU/IrDA 4-Mbps communication module (FIR) and memory.

The DMA start address of each DMA channel can be specified in the range of 0x0000 0000 to 0x01FF FFFE as a half-word address. The DMA space of each DMA channel is secured in a 2-Kbyte block that starts from the address generated by masking the lower ten bits of the DMA start address to zero.

The DMA operation is not guaranteed if the DMA space overlaps that of other peripheral units.

Table 6-1. DMAAU Registers

Physical Address	Symbol	Function
0x0B00 0020	AIUIBALREG	DMA base lower address register for AIU input
0x0B00 0022	AIUIBAHREG	DMA base higher address register for AIU input
0x0B00 0024	AIUIALREG	DMA lower address register for AIU input
0x0B00 0026	AIUIAHREG	DMA higher address register for AIU input
0x0B00 0028	AIUOBALREG	DMA base lower address register for AIU output
0x0B00 002A	AIUOBAHREG	DMA base higher address register for AIU output
0x0B00 002C	AIUOALREG	DMA lower address register for AIU output
0x0B00 002E	AIUOAHREG	DMA higher address register for AIU output
0x0B00 0030	FIRBALREG	DMA base lower address register for FIR
0x0B00 0032	FIRBAHREG	DMA base higher address register for FIR
0x0B00 0034	FIRALREG	DMA lower address register for FIR
0x0B00 0036	FIRAHREG	DMA higher address register for FIR

7. DCU (DMA CONTROL UNIT)

The DCU controls the DMA operation. It controls the DMA requests from the internal peripheral I/O units (AIU and FIR) and the acknowledge signal from the BCU that performs bus arbitration, and enables or disables the DMA operation.

Table 7-1. DCU Registers

Physical Address	Symbol	Function
0x0B00 0040	DMARSTREG	DMA reset register
0x0B00 0042	DMAIDLEREG	DMA sequencer status register
0x0B00 0044	DMASENREG	DMA sequencer enable register
0x0B00 0046	DMAMSKREG	DMA mask register
0x0B00 0048	DMAREQREG	DMA request register
0x0B00 004A	TDREG	Transfer direction set register

8. CMU (CLOCK MASK UNIT)

The CMU is used to specify whether the CPU core supplies the clock to each peripheral unit. By supplying the clock only to the necessary peripheral units, the power consumption can be reduced.

Table 8-1. CMU Register

Physical Address	Symbol	Function
0x0B00 0060	CMUCLKMSK	CMU clock mask register

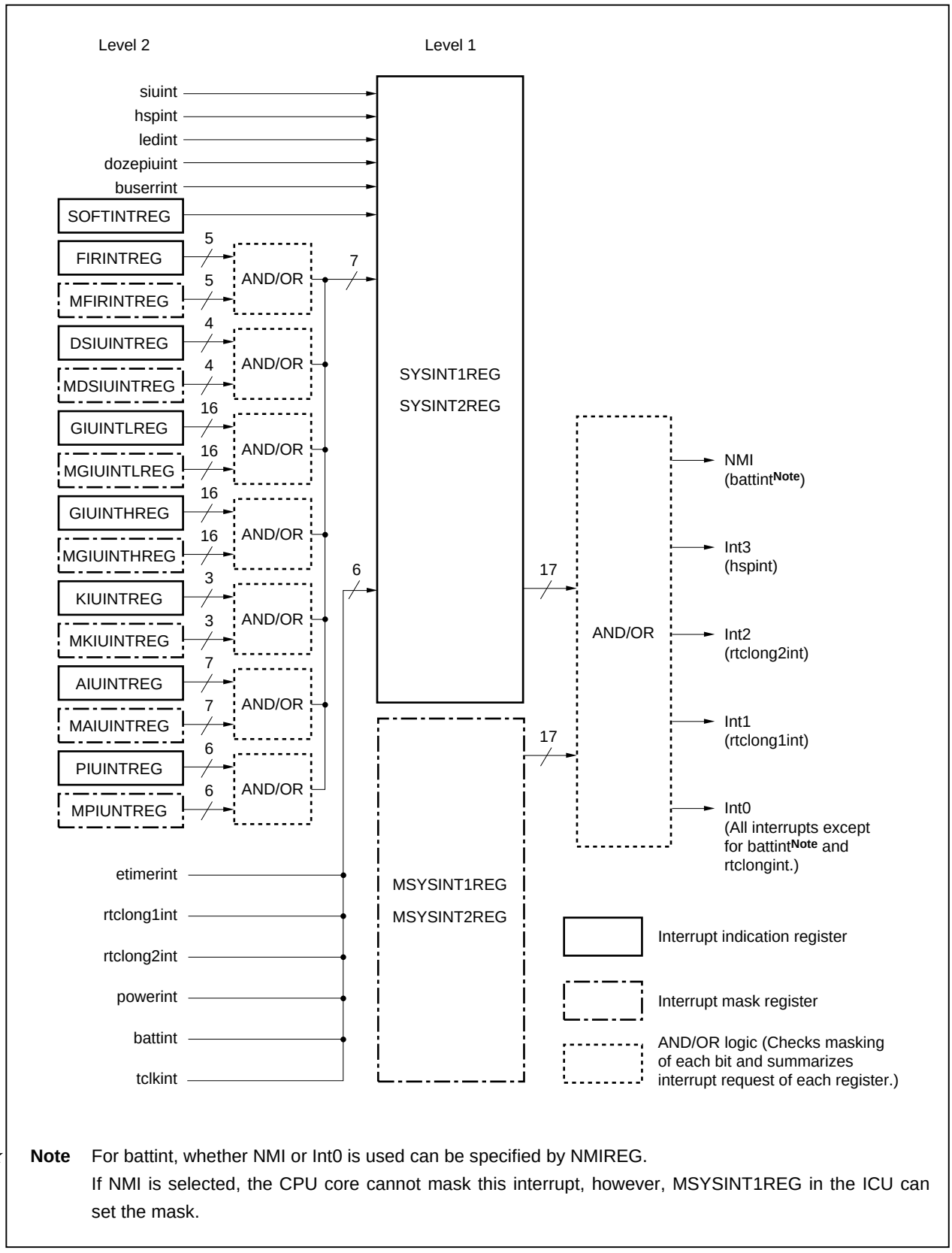
9. ICU (INTERRUPT CONTROL UNIT)

The ICU receives an interrupt request signal from each peripheral unit and generates an interrupt request signal (Int0, Int1, Int2, Int3, or NMI) to the CPU core.

Table 9-1. ICU Registers

Physical Address	Symbol	Function
0x0B00 0080	SYSINT1REG	System interrupt register 1 (level 1)
0x0B00 0082	PIUINTREG	PIU interrupt register (level 2)
0x0B00 0084	AIUINTREG	AIU interrupt register(level 2)
0x0B00 0086	KIUINTREG	KIU interrupt register (level 2)
0x0B00 0088	GIUINTLREG	GIU interrupt lower address register (level 2)
0x0B00 008A	DSIUINTREG	DSIU interrupt register (level 2)
0x0B00 008C	MSYSINT1REG	System interrupt mask register 1 (level 1)
0x0B00 008E	MPIUINTREG	PIU interrupt mask register (level 2)
0x0B00 0090	MAIUINTREG	AIU interrupt mask register (level 2)
0x0B00 0092	MKIUINTREG	KIU interrupt mask register (level 2)
0x0B00 0094	MGIUINTLREG	GIU interrupt mask lower address register (level 2)
0x0B00 0096	MDSIUINTREG	DSIU interrupt mask register (level 2)
0x0B00 0098	NMIREG	Battery interrupt select register
0x0B00 009A	SOFTINTREG	Software interrupt register
0x0B00 0200	SYSINT2REG	System interrupt register 2 (level 1)
0x0B00 0202	GIUINTHREG	GIU interrupt higher address register (level 2)
0x0B00 0204	FIRINTREG	FIR interrupt register (level 2)
0x0B00 0206	MSYSINT2REG	System interrupt mask register 2 (level 1)
0x0B00 0208	MGIUINTHREG	GIU interrupt mask higher address register (level 2)
0x0B00 020A	MFIRINTREG	FIR interrupt mask register (level 2)

Figure 9-1. ICU Configuration



★ **Note** For battint, whether NMI or Int0 is used can be specified by NMIREG.
If NMI is selected, the CPU core cannot mask this interrupt, however, MSYSINT1REG in the ICU can set the mask.

10. PMU (POWER MANAGEMENT UNIT)

The PMU manages and controls power to the internal and external circuits of the VR4111 as follows:

- Controls shutdown
- Controls reset
- Controls power-on
- Controls low-power consumption mode (power mode)

PMU also set the start cause via the GPIO (0:3), (9:12) pins and DCD# pin.

Table 10-1. PMU Registers

Physical Address	Symbol	Function
0x0B00 00A0	PMUINTREG	PMU interrupt/status register
0x0B00 00A2	PMUCNTREG	PMU control register
0x0B00 00A4	PMUINT2REG	PMU interrupt/status register 2
0x0B00 00A6	PMUCNT2REG	PMU control register 2
0x0B00 00A8	PMUWAITREG	PMU wait count register

10.1 Power Mode

The VR4111 supports the following four power modes:

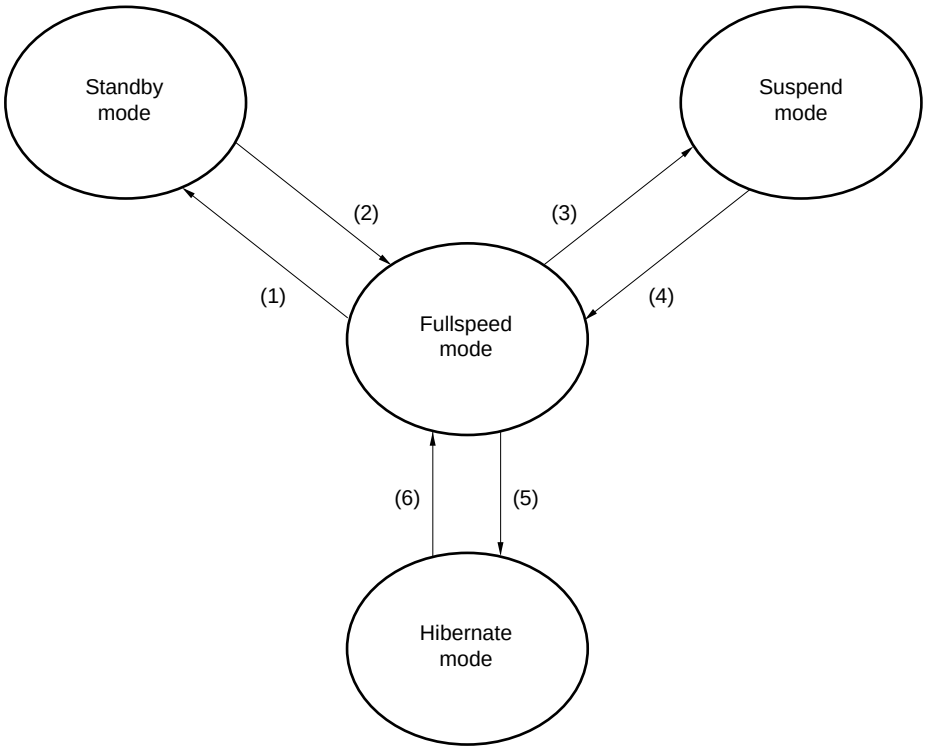
- Fullspeed mode
- Standby mode
- Suspend mode
- Hibernate mode

Figure 10-1 illustrates the transition of the power modes.

To change the mode from Fullspeed to Standby, Suspend, or Hibernate, execute the STANDBY, SUSPEND, or HIBERNATE instruction. To change the mode from Standby, Suspend, or Hibernate to Fullspeed, either generate an interrupt, or execute a reset operation.

Table 10-2 outlines each power mode.

Figure 10-1. Power Mode Transition



(1)	(2)	(3)	(4)	(5)	(6)
STANDBY instruction, pipeline flash, SysAD idle, PClock high level	All interrupts	SUSPEND instruction, pipeline flash, SysAD idle, PClock high level, TClock high level, DRAM self refresh start	POWER RSTSW Elapsed Time RTCLong1 RTCLong2 KeyTouch PenTouch GPIO (9:14) GPIO (0:3) DCD# (GPIO, SIU) BATTINTR	HIBERNATE instruction, pipeline flash, SysAD idle, PClock high level, TClock high level, MasterOut high level, DRAM self refresh start	POWER Elapsed Time DCD# GPIO (0:3) GPIO (9:12)

★ ★

Table 10-2. Outline of Power Mode

Mode	Internal Peripheral Unit				Pipe Line
	RTC	ICU	DCU	Others	
Fullspeed	On	On	On	Selectable[Note]	On
Standby	On	On	On	Selectable[Note]	Off
Suspend	On	On	Off	Off	Off
Hibernate	On	Off	Off	Off	Off
Off	Off	Off	Off	Off	Off

Note Refer to **8. CMU (CLOCK MASK UNIT)**.

11. RTC (REAL-TIME CLOCK UNIT)

The RTC unit consists of the following three types of timers.

- RTCLong timer (two timers)
  This is a 24-bit programmable down counter that counts down at a cycle of 32.768 kHz. It can generate an interrupt request at intervals of up to 512 seconds.
- ElapsedTime timer (one timer)
  This is a 48-bit up counter that counts up at a cycle of 32.768 kHz. When this counter counts up to about 272 years, it returns to 0. This counter consists of an 48-bit comparator (ECMPHREG, ECMPLREG, ECMPMREG) and a 48-bit alarm time register (ETIMELREG, ETIMEMREG, ETIMEHREG). By comparing these, an interrupt request can be generated at specific time.
- TClock count timer (one timer)
  This is a 25-bit programmable counter that counts down at each TClock cycle. Interrupt requests can be generated with a cycle of up to 2 seconds by setting the CLKSEL (0:2) pins.
  This timer is used for performance evaluation.

Table 11-1. RTC Registers

Physical Address	Symbol	Function
0x0B00 00C0	ETIMELREG	Elapsed Time timer lower register
0x0B00 00C2	ETIMEMREG	Elapsed Time timer middle register
0x0B00 00C4	ETIMEHREG	Elapsed Time timer higher register
0x0B00 00C8	ECMPLREG	Elapsed Time timer compare lower register
0x0B00 00CA	ECMPMREG	Elapsed Time timer compare middle register
0x0B00 00CC	ECMPHREG	Elapsed Time timer compare higher register
0x0B00 00D0	RTCL1LREG	RTCLong 1 timer lower register
0x0B00 00D2	RTCL1HREG	RTCLong 1 timer higher register
0x0B00 00D4	RTCL1CNTLREG	RTCLong 1 timer count lower register
0x0B00 00D6	RTCL1CNTHREG	RTCLong 1 timer count higher register
0x0B00 00D8	RTCL2LREG	RTCLong 2 timer lower register
0x0B00 00DA	RTCL2HREG	RTCLong 2 timer higher register
0x0B00 00DC	RTCL2CNTLREG	RTCLong 2 timer count lower register
0x0B00 00DE	RTCL2CNTHREG	RTCLong 2 timer count higher register
0x0B00 01C0	TCLKLREG	TClock counter lower register
0x0B00 01C2	TCLKHREG	TClock counter higher register
0x0B00 01C4	TCLKCNTLREG	TClock counter count lower register
0x0B00 01C6	TCLKCNTHREG	TClock counter count higher register
0x0B00 01CE	RTCINTREG	RTC interrupt register

12. DSU (DEADMAN'S SW UNIT)

The DSU automatically detects a runaway of the VR4111 and resets the VR4111. By stopping a runaway at the earliest stage by using the DSU, destruction of data can be minimized.

The DSU can be set for a cycle of up to 15 seconds in units of 1 second. Set the DSWCLR bit of the DSUCLRREG register to 1 within this time by means of software. If the bit is not set within this time, the VR4111 enters the reset status (refer to **4. INITIALIZATION INTERFACE**).

Table 12-1. DSU Registers

Physical Address	Symbol	Function
0x0B00 00E0	DSUCNTREG	DSU control register
0x0B00 00E2	DSUSETREG	DSU cycle set register
0x0B00 00E4	DSUCLRREG	DSU clear register
0x0B00 00E6	DSUTIMREG	DSU elapsed time register

13. GIU (GENERAL-PURPOSE I/O UNIT)

The GIU controls the GPIO and DCD# pins. The GPIO pins constitute a general-purpose I/O port. GIU can assign the interrupt request signal function for these pins. As a trigger, the edge of the input signal (rising or falling edge), high level, or low level can be selected. Use the PMUCNTREG register of PMU, however, to specify the power-on factor via the GPIO (0:3), GPIO (9:12), or DCD# pin.

Table 13-1. GIU Registers

Physical Address	Symbol	Function
0x0B00 0100	GIUIOSELL	GPIO input/output setting lower register
0x0B00 0102	GIUIOSELH	GPIO input/output setting higher register
0x0B00 0104	GIUPIODL	GPIO input/output data lower register
0x0B00 0106	GIUPIODH	GPIO input/output data higher register
0x0B00 0108	GIUINTSTATL	GPIO interrupt lower register
0x0B00 010A	GIUINTSTATH	GPIO interrupt higher register
0x0B00 010C	GIUINTENL	GPIO interrupt enable lower register
0x0B00 010E	GIUINTENH	GPIO interrupt enable higher register
0x0B00 0110	GIUINTTYPL	GPIO interrupt trigger setting lower register
0x0B00 0112	GIUINTTYPH	GPIO interrupt trigger setting higher register
0x0B00 0114	GIUINTALSELL	GPIO interrupt level setting lower register
0x0B00 0116	GIUINTALSELH	GPIO interrupt level setting higher register
0x0B00 0118	GIUINTHTSELL	GPIO interrupt hold setting lower register
0x0B00 011A	GIUINTHTSELH	GPIO interrupt hold setting higher register
0x0B00 011C	GIUPODATL	GPIO output data lower register
0x0B00 011E	GIUPODATH	GPIO output data higher register
0x0B00 02E0	GIUUSEUPDN	GPIO pull-up/pull-down enable register
0x0B00 02E2	GIUTERMUPDN	GPIO pull-up/pull-down setting register

Table 13-2. Outline of GPIO pins

Pin Name	Interrupt Request Detection Clock (Internal)	Input Buffer Type
GPIO (49:32)	–	–
GPIO (31:16)	TClock	Normal
GPIO15 (DCD#)	MasterOut	Normal
GPIO (14:9)	MasterOut	Normal
GPIO (8:4)	TClock	Schmitt
GPIO (3:0)	RTC	Schmitt

Caution Pin GPIO15 cannot be used as a general-purpose I/O pin because its function is fixed to DCD# signal input.

14. PIU (TOUCH PANEL UNIT)

The PIU uses an on-chip 10-bit A/D converter and detects the X and Y coordinates of pen contact locations on the touch panel, and scans the general-purpose A/D input port. Since the touch panel control circuit and the A/D converter (conversion precision: 10 bits) are both on-chip, the touch panel can be connected directly to the VR4111.

Figure 14-1. PIU Peripheral Block Diagram

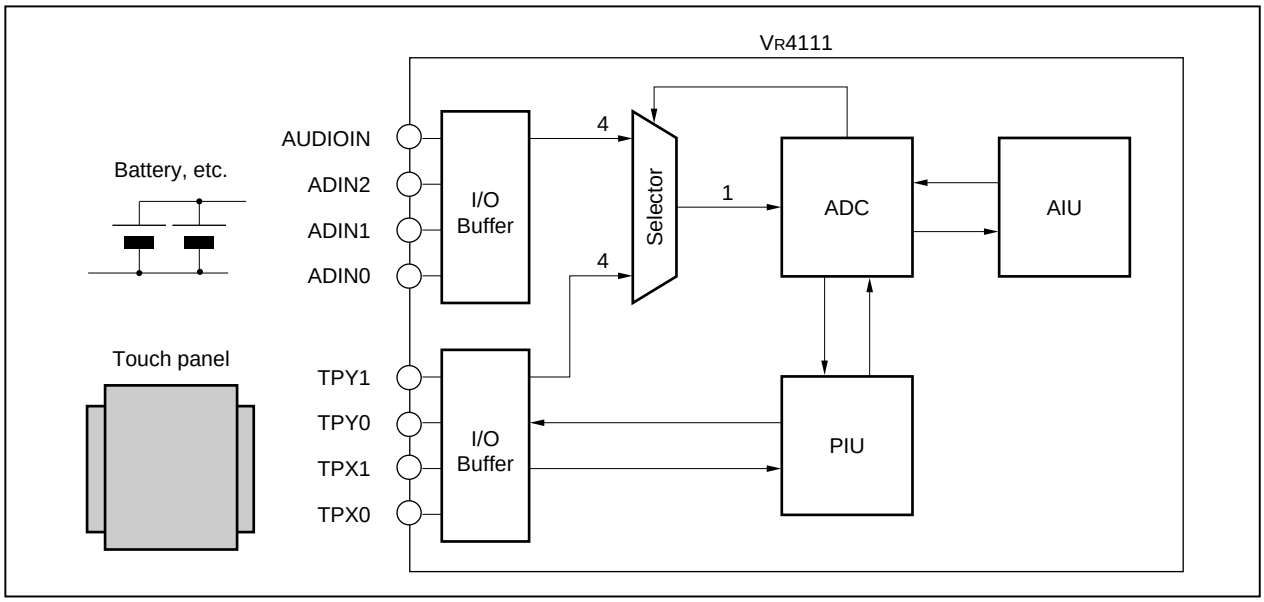


Table 14-1. PIU Registers

Physical Address	Symbol	Function
0x0B00 0122	PIUCNTREG	PIU control register
0x0B00 0124	PIUINTREG	PIU interrupt register
0x0B00 0126	PIUSIVLREG	PIU data sampling cycle set register
0x0B00 0128	PIUSTBLREG	PIU A/D converter wait time set register
0x0B00 012A	PIUCMDREG	PIU A/D command register
0x0B00 0130	PIUASCNREG	PIU A/D port scan register
0x0B00 0132	PIUAMSKREG	PIU A/D scan mask register
0x0B00 013E	PIUCIVLREG	PIU wait time count register
0x0B00 02A0	PIUPB00REG	PIU page 0 buffer 0 register
0x0B00 02A2	PIUPB01REG	PIU page 0 buffer 1 register
0x0B00 02A4	PIUPB02REG	PIU page 0 buffer 2 register
0x0B00 02A6	PIUPB03REG	PIU page 0 buffer 3 register
0x0B00 02A8	PIUPB10REG	PIU page 1 buffer 0 register
0x0B00 02AA	PIUPB11REG	PIU page 1 buffer 1 register
0x0B00 02AC	PIUPB12REG	PIU page 1 buffer 2 register
0x0B00 02AE	PIUPB13REG	PIU page 1 buffer 3 register
0x0B00 02B0	PIUAB0REG	PIU A/D scan buffer 0 register
0x0B00 02B2	PIUAB1REG	PIU A/D scan buffer 1 register
0x0B00 02B4	PIUAB2REG	PIU A/D scan buffer 2 register
0x0B00 02B6	PIUAB3REG	PIU A/D scan buffer 3 register
0x0B00 02BC	PIUPB04REG	PIU page 0 buffer 4 register
0x0B00 02BE	PIUPB14REG	PIU page 1 buffer 4 register

15. SIU (SERIAL INTERFACE UNIT)

The SIU is a serial interface that conforms to the RS-232C communication standard and is equipped with two one-channel interfaces, one for transmission and one for reception.

The SIU is functionally compatible with the NS16550, and supports a transfer rate up to 1.152 Mbps. This unit also has an infrared communication function that corresponds to SIR.

Table 15-1. SIU Registers

Physical Address	LCR7	R/W	Symbol	Function
0x0C00 0000	0	R	SIURB	Receive buffer register (Read)
		W	SIUTH	Transmission hold register (Write)
	1	R/W	SIUDLL	Division ratio lower byte register
0x0C00 0001	0	R/W	SIUIE	Interrupt enable register
	1	R/W	SIUDLM	Division ratio higher byte register
0x0C00 0002	–	R	SIUIID	Interrupt identification register (Read)
		W	SIUFC	FIFO control register (Write)
0x0C00 0003	–	R/W	SIULC	Line control register
0x0C00 0004	–	R/W	SIUMC	Modem control register
0x0C00 0005	–	R/W	SIULS	Line status register
0x0C00 0006	–	R/W	SIUMS	Modem status register
0x0C00 0007	–	R/W	SIUSC	Scratch register
0x0C00 0008	–	R/W	SIUIRSEL	Serial communication select register
0x0C00 0009	–	R/W	SIURESET	SIU reset register
0x0C00 000A	–	R/W	SIUCSEL	SIU echo-back control register

Remark LCR7 is bit 7 of the SIULC register.

Figure 15-1. SIU Peripheral Block Diagram

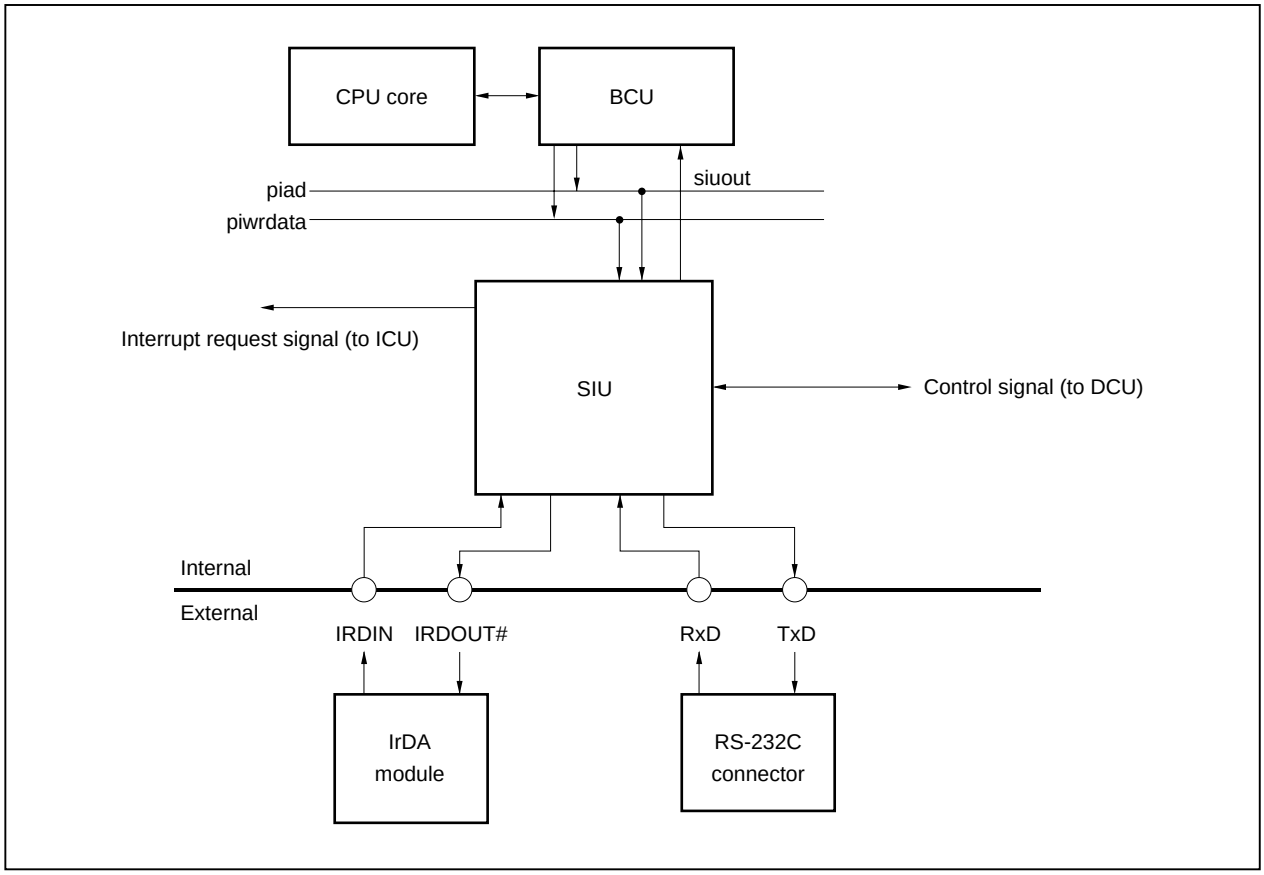
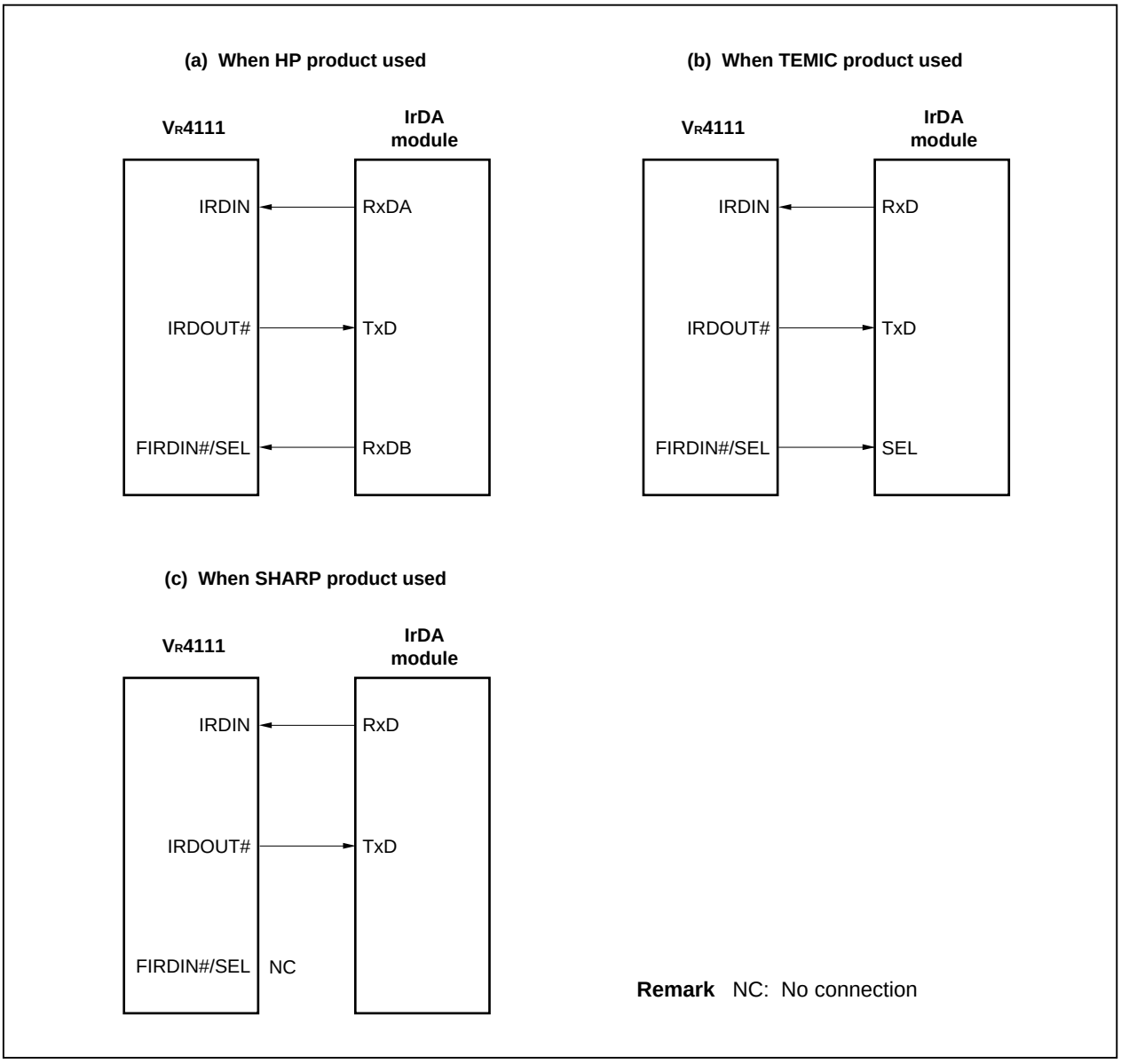


Figure 15-2. Example of Connection between VR4111 and IrDA Module



Remark NC: No connection

16. AIU (AUDIO INTERFACE UNIT)

The AIU supports speaker output and microphone input operations. It has 10-bit A/D and D/A converters, and functions as the digital voice I/O interface. DMA operation is supported for both input and output operations.

Table 16-1. AIU Registers

Physical Address	Symbol	Function
0x0B00 0160	MDMADATREG	Mic input DMA data register
0x0B00 0162	SDMADATREG	Speaker output DMA data register
0x0B00 0166	SODATREG	Speaker output data register
0x0B00 0168	SCNTREG	Speaker output control register
0x0B00 016A	SCNVRREG	D/A conversion rate setting register
0x0B00 0170	MIDATREG	Mic input data register
0x0B00 0172	MCNTREG	Mic input control register
0x0B00 0174	MCNVRREG	A/D conversion rate setting register
0x0B00 0178	DVALIDREG	Data valid indicate register
0x0B00 017A	SEQREG	Sequencer operation enable register
0x0B00 017C	INTREG	AIU interrupt register

17. KIU (KEYBOARD INTERFACE UNIT)

The KIU includes 12 scan lines and 8 detection lines to enable detection when 64, 80, or 96 keys are pressed. The number of scan lines can be selected from 8, 10, and 12.

The 12 scan lines can be used as a general-purpose output port by setting the following registers.

Table 17-1. KIU Registers

Physical Address	Symbol	Function
0x0B00 0180	KIUDAT0	KIU data 0 register
0x0B00 0182	KIUDAT1	KIU data 1 register
0x0B00 0184	KIUDAT2	KIU data 2 register
0x0B00 0186	KIUDAT3	KIU data 3 register
0x0B00 0188	KIUDAT4	KIU data 4 register
0x0B00 018A	KIUDAT5	KIU data 5 register
0x0B00 0190	KIUSCANREP	KIU key scan control register
0x0B00 0192	KIUSCANS	KIU sequencer status register
0x0B00 0194	KIUWKS	KIU key scan wait time setting register
0x0B00 0196	KIUWKI	KIU key scan interval setting register
0x0B00 0198	KIUINT	KIU interrupt register
0x0B00 019A	KIURST	KIU reset register
0x0B00 019C	KIUGPEN	KIU general-purpose output enable register
0x0B00 019E	SCANLINE	KIU scan line control register

18. DSIU (DEBUG SERIAL INTERFACE UNIT)

The DSIU is a dedicated serial interface unit that is used during debugging. It supports a data transfer rate of up to 115.2 kbps. In addition to the DDIN and DDOUT I/O pins, it supports the DCTS# and DRTS# pins that are used for hardware flow control. These pins can be used as a general-purpose output port when the DSIU is not used.

Table 18-1. DSIU Registers

Physical Address	Symbol	Function
0x0B00 01A0	PORTREG	General-purpose port switch register
0x0B00 01A2	MODEMREG	Modem control register
0x0B00 01A4	ASIM00REG	Asynchronous mode 0 register
0x0B00 01A6	ASIM01REG	Asynchronous mode 1 register
0x0B00 01A8	RXB0RREG	Extend receive buffer register
0x0B00 01AA	RXB0LREG	Receive buffer register
0x0B00 01AC	TXS0RREG	Extend transmit shift register
0x0B00 01AE	TXS0LREG	Transmit shift register
0x0B00 01B0	ASIS0REG	Communication state register
0x0B00 01B2	INTR0REG	DSIU interrupt register
0x0B00 01B6	BPRM0REG	Baud rate generator prescaler mode register
0x0B00 01B8	DSIURESETREG	DSIU reset register

19. LED (LED CONTROL UNIT)

LED switches LEDs on and off at a regular interval. This operation can be executed in Standby, Suspend, or Hibernate mode, and the interval time can be programmed.

Table 19-1. LED Registers

Physical Address	Symbol	Function
0x0B00 0240	LEDHTSREG	LED ON time setting register
0x0B00 0242	LEDLTSREG	LED OFF time setting register
0x0B00 0248	LEDCNTREG	LED control register
0x0B00 024A	LEDASTCREG	LED auto stop time setting register
0x0B00 024C	LEDINTREG	LED interrupt register

20. HSP (MODEM INTERFACE UNIT)

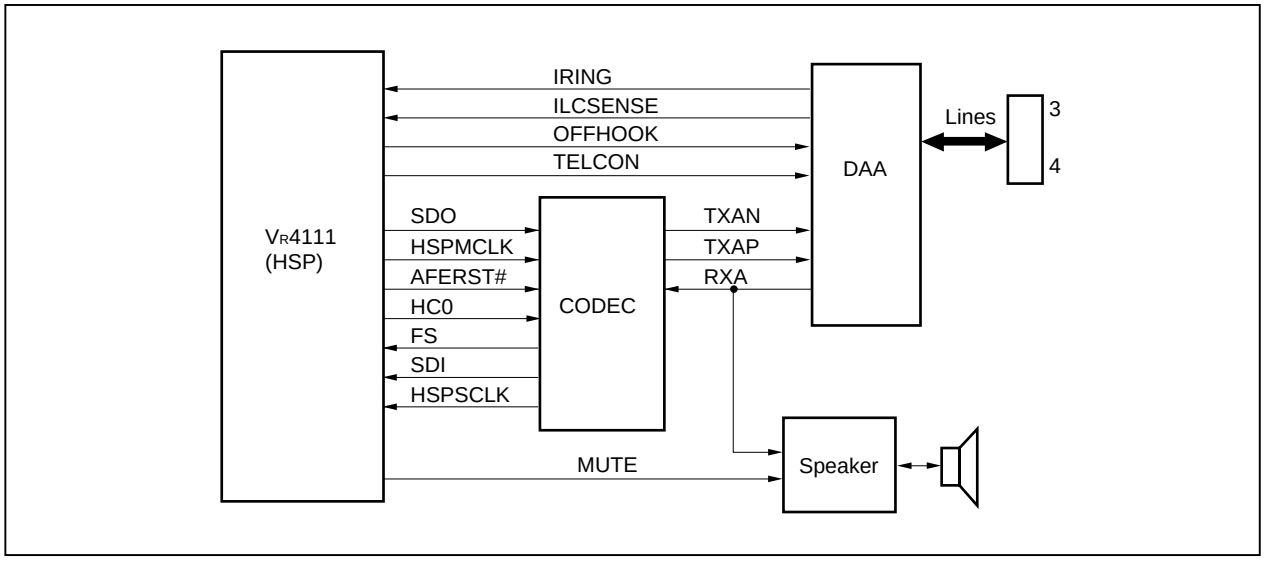
HSP interfaces between the modem software of the CPU core and the external circuits. This unit uses PC-TEL's NEC56K, and it has the following main functions.

- Controls CODEC devices and performs serial/parallel conversion of CODEC transmitted/received data
- Controls signal lines in the data access arrangement block (DAA), such as relay or hook

Table 20-1. HSP Registers

Physical Address	R/W	Symbol	Function
0x0C00 0020	R/W	HSPINIT	HSP initialization register
0x0C00 0022	R/W	HSPDATA (7:0)	HSP data register (lower)
0x0C00 0023	R/W	HSPDATA (15:8)	HSP data register (higher)
0x0C00 0024	W	HSPINDEX	HSP index register
0x0C00 0028	R	HSPID (7:0)	HSP ID register
0x0C00 0029	R	HSPPCS (7:0)	HSP I/O address program confirmation register
	W	HSPPCTEL (7:0)	HSP signature check port

Figure 20-1. Block Connection Example



21. FIR (FAST IrDA INTERFACE UNIT)

FIR supports the IrDA 1.1 high-speed infrared communication physical layer standard. For infrared communication corresponding to IrDA 1.0, use the SIU instead. However, the pins interfacing the IrDA module are common pins.

Table 21-1. FIR Registers

Physical Address	Symbol	Function
0x0C00 0040	FRSTR	FIR reset register
0x0C00 0042	DPINTR	DMA page interrupt register
0x0C00 0044	DPCNTR	DMA page control register
0x0C00 0050	TDR	Transmitted data register
0x0C00 0052	RDR	Received data register
0x0C00 0054	IMR	Interrupt mask register
0x0C00 0056	FSR	FIFO set-up register
0x0C00 0058	IRSR1	IR set-up register 1
0x0C00 005C	CRCSR	CRC set-up register
0x0C00 005E	FIRCR	FIR control register
0x0C00 0060	MIRCR	MIR control register
0x0C00 0062	DMACR	DMA control register
0x0C00 0064	DMAER	DMA enable register
0x0C00 0066	TXIR	Transmission indication register
0x0C00 0068	RXIR	Reception indication register
0x0C00 006A	IFR	Interrupt flag register
0x0C00 006C	RXSTS	Reception status register
0x0C00 006E	TXFL	Transmission frame length register
0x0C00 0070	MRXF	Maximum reception flame length register
0x0C00 0074	RXFL	Reception frame length register

22. INSTRUCTION SET

The VR4111 has two types of instructions: 32-bit instructions (MIPS III) and 16-bit instructions (MIPS16).

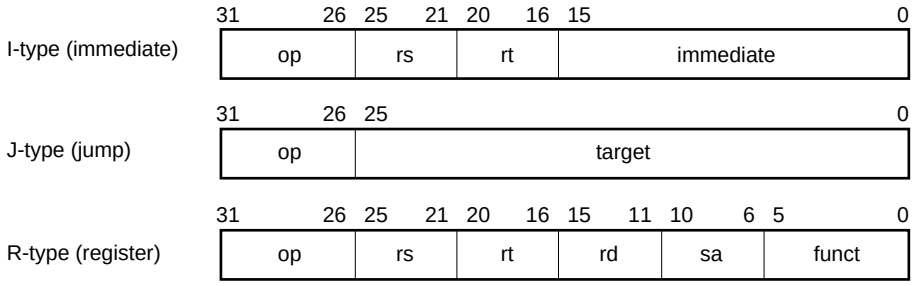
22.1 MIPS III Instruction

Each instruction of the MIPS III consists of 1 word (32 bits) located at a word boundary. Three instruction formats are available as shown in Figure 22-1. By employing the three simplified instruction formats, the decoding of instructions is simplified. Complicated operations and addressing modes that are not frequently used are realized by the compiler.

22.1.1 Instruction formats

The instruction formats of the MIPS III are shown below.

Figure 22-1. MIPS III CPU Instruction Format



op	6-bit instruction code
rs	5-bit source register number
rt	5-bit target (source/destination) register number, or branch condition
immediate	16-bit immediate value, branch displacement, or address displacement
target	26-bit unconditional branch target address
rd	5-bit destination register number
sa	5-bit shift
funct	6-bit function field

22.1.2 MIPS III instruction set list

All the MIPS III instructions of the VR4111 are classified into three sets: the instruction set common to all the VR Series processors (ISA: Instruction Set Architecture), the instruction set executed by the VR4000™ Series (extended ISA), and the system control coprocessor instruction set. Each instruction set is listed below.

Table 22-1. CPU Instruction Set: ISA (1/3)

Instruction	Description	Format
Load/store instruction	op | base | rt | offset	
LB	Load Byte	LB rt, offset (base)
LBU	Load Byte Unsigned	LBU rt, offset (base)
LH	Load Halfword	LH rt, offset (base)
LHU	Load Halfword Unsigned	LHU rt, offset (base)
LW	Load Word	LW rt, offset (base)
LWL	Load Word Left	LWL rt, offset (base)
LWR	Load Word Right	LWR rt, offset (base)
SB	Store Byte	SB rt, offset (base)
SH	Store Halfword	SH rt, offset (base)
SW	Store Word	SW rt, offset (base)
SWL	Store Word Left	SWL rt, offset (base)
SWR	Store Word Right	SWR rt, offset (base)
AIU immediate instruction	op | rs | rt | offset	
ADDI	Add Immediate	ADDI rt, rs, immediate
ADDIU	Add Immediate Unsigned	ADDIU rt, rs, immediate
SLTI	Set On Less Than Immediate	SLTI rt, rs, immediate
SLTIU	Set On Less Than Immediate Unsigned	SLTIU rt, rs, immediate
ANDI	And Immediate	ANDI rt, rs, immediate
ORI	Or Immediate	ORI rt, rs, immediate
XORI	Exclusive Or Immediate	XORI rt, rs, immediate
LUI	Load Upper Immediate	LUI rt, rs, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct	
ADD	Add	ADD rd, rs, rt
ADDU	Add Unsigned	ADDU rd, rs, rt
SUB	Subtract	SUB rd, rs, rt
SUBU	Subtract Unsigned	SUBU rd, rs, rt
SLT	Set On Less Than	SLT rd, rs, rt
SLTU	Set On Less Than Unsigned	SLTU rd, rs, rt
AND	And	AND rd, rs, rt
OR	Or	OR rd, rs, rt
XOR	Exclusive Or	XOR rd, rs, rt
NOR	Nor	NOR rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct	
SLL	Shift Left Logical	SLL rd, rt, sa
SRL	Shift Right Logical	SRL rd, rt, sa
SRA	Shift Right Arithmetic	SRA rd, rt, sa
SLLV	Shift Left Logical Variable	SLLV rd, rt, rs
SRLV	Shift Right Logical Variable	SRLV rd, rt, rs
SRAV	Shift Right Arithmetic Variable	SRAV rd, rt, rs

Table 22-1. CPU Instruction Set: ISA (2/3)

Instruction	Description	Format
Multiplication/division instruction	op | rs | rt | rd | sa | funct	
MULT	Multiply	MULT rs, rt
MULTU	Multiply Unsigned	MULTU rs, rt
DIV	Divide	DIV rs, rt
DIVU	Divide Unsigned	DIVU rs, rt
MFHI	Move From HI	MFHI rd
MFLO	Move From LO	MFLO rd
MTHI	Move To HI	MTHI rs
MTLO	Move To LO	MTLO rs
Jump instruction (1)	op | target	
J	Jump	J target
JAL	Jump And Link	JAL target
Jump instruction (2)	op | rs | rt | rd | sa | funct	
JR	Jump Register	JR rs
JALR	Jump And Link Register	JALR rs, rd
Branch instruction (1)	op | rs | rt | offset	
BEQ	Branch On Equal	BEQ rs, rt, offset
BNE	Branch On Not Equal	BNE rs, rt, offset
BLEZ	Branch On Less Than Or Equal To Zero	BLEZ rs, offset
BGTZ	Branch On Greater Than Zero	BGTZ rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset	
BLTZ	Branch On Less Than Zero	BLTZ rs, offset
BGEZ	Branch On Greater Than Or Equal To Zero	BGEZ rs, offset
BLTZAL	Branch On Less Than Zero And Link	BLTZAL rs, offset
BGEZAL	Branch On Greater Than Or Equal To Zero And Link	BGEZAL rs, offset
Special instruction	SPECIAL | rs | rt | rd | sa | funct	
SYNC	Synchronize	SYNC
SYSCALL	System Call	SYSCALL
BREAK	Breakpoint	BREAK
Coprocessor instruction (1)	op | rs | rt | rd | sa | funct	
LWCz	Load Word To Coprocessor z	LWCz rt, offset (base)
SWCz	Store Word From Coprocessor z	SWCz rt, offset (base)
Coprocessor instruction (2)	op | rs | rt | rd | sa | funct	
MTCz	Move To Coprocessor z	MTCz rt, rd
MFCz	Move From Coprocessor z	MFCz rt, rd
CTCz	Move Control To Coprocessor z	CTCz rt, rd
CFCz	Move Control From Coprocessor z	CFCz rt, rd

Table 22-1. CPU Instruction Set: ISA (3/3)

Instruction	Description	Format
Coprocessor instruction (3)	COPz | CO | cofun	
COPz	Coprocessor z Operation	COPz cofun
Coprocessor instruction (4)	COPz | BC | br | offset	
BCzT	Branch On Coprocessor z True	BCzT offset
BCzF	Branch On Coprocessor z False	BCzF offset

Table 22-2. CPU Instruction Set: Extended ISA (1/2)

Instruction	Description	Format
Load/store instruction	op | base | rt | offset	
LD	Load Doubleword	LD rt, offset (base)
LDL	Load Doubleword Left	LDL rt, offset (base)
LDR	Load Doubleword Right	LDR rt, offset (base)
LWU	Load Word Unsigned	LWU rt, offset (base)
SD	Store Doubleword	SD rt, offset (base)
SDL	Store Doubleword Left	SDL rt, offset (base)
SDR	Store Doubleword Right	SDR rt, offset (base)
AIU immediate instruction	op | rs | rt | immediate	
DADDI	Doubleword Add Immediate	DADDI rt, rs, immediate
DADDIU	Doubleword Add Immediate Unsigned	DADDIU rt, rs, immediate
3-operand type instruction	op | rs | rt | rd | sa | funct	
DADD	Doubleword Add	DADD rd, rs, rt
DADDU	Doubleword Add Unsigned	DADDU rd, rs, rt
DSUB	Doubleword Subtract	DSUB rd, rs, rt
DSUBU	Doubleword Subtract Unsigned	DSUBU rd, rs, rt
Shift instruction	op | rs | rt | rd | sa | funct	
DSLL	Doubleword Shift Left Logical	DSLL rd, rt, sa
DSRL	Doubleword Shift Right Logical	DSRL rd, rt, sa
DSRA	Doubleword Shift Right Arithmetic	DSRA rd, rt, sa
DSLLV	Doubleword Shift Left Logical Variable	DSLLV rd, rt, sa
DSRLV	Doubleword Shift Right Logical Variable	DSRLV rd, rt, sa
DSRAV	Doubleword Shift Right Arithmetic Variable	DSRAV rd, rt, sa
DSLL32	Doubleword Shift Left Logical+32	DSLL32 rd, rt, sa
DSRL32	Doubleword Shift Right Logical+32	DSRL32 rd, rt, sa
DSRA32	Doubleword Shift Right Arithmetic+32	DSRA32 rd, rt, sa
Multiplication/division instruction (1)	op | rs | rt | rd | sa | funct	
DMULT	Doubleword Multiply	DMULT rs, rt
DMULTU	Doubleword Multiply Unsigned	DMULTU rs, rt
DDIV	Doubleword Divide	DDIV rs, rt
DDIVU	Doubleword Divide Unsigned	DDIVU rs, rt

Table 22-2. CPU Instruction Set: Extended ISA (2/2)

Instruction	Description	Format
Multiplication/division instruction (2)	op | rs | rt | immediate	
MADD16 DMADD16	Multiply and Add 16-bit Integer Doubleword Multiply and Add 16-bit Integer	MADD16 rs, rt DMADD16 rs, rt
Jump instruction	op | target	
JALX	Jump And Link Exchange	JALX target
Branch instruction (1)	op | rs | rt | offset	
BEQL BNEL BLEZL BGTZL	Branch On Equal Likely Branch On Not Equal Likely Branch On Less Than Or Equal To Zero Likely Branch On Greater Than Zero Likely	BEQL rs, rt, offset BNEL rs, rt, offset BLEZL rs, offset BGTZL rs, offset
Branch instruction (2)	REGIMM | rs | sub | offset	
BLTZL BGEZL BLTZALL BGEZALL	Branch On Less Than Zero Likely Branch On Greater Than Or Equal To Zero Likely Branch On Less Than Zero And Link Likely Branch On Greater Than Or Equal To Zero And Link Likely	BLTZL rs, offset BGEZL rs, offset BLTZALL rs, offset BGEZALL rs, offset
Exception instruction	SPECIAL | rs | rt | rd | sa | funct	
TGE TGEU TLT TLTU TEQ TNE	Trap If Greater Than Or Equal Trap If Greater Than Or Equal Unsigned Trap If Less Than Trap If Less Than Unsigned Trap If Equal Trap If Not Equal	TGE rs, rt TGEU rs, rt TLT rs, rt TLTU rs, rt TEQ rs, rt TNE rs, rt
Exception immediate instruction	REGIMM | rs | sub | immediate	
TGEI TGEIU TLTI TLTIU TEQI TNEI	Trap If Greater Than Or Equal Immediate Trap If Greater Than Or Equal Immediate Unsigned Trap If Less Than Immediate Trap If Less Than Immediate Unsigned Trap If Equal Immediate Trap If Not Equal Immediate	TGEI rs, immediate TGEIU rs, immediate TLTI rs, immediate TLTIU rs, immediate TEQI rs, immediate TNEI rs, immediate

Table 22-3. System Control Coprocessor (CP0) Instruction Set

Instruction	Description	Format
System control coprocessor instruction (1)	COP0 | sub | rt | rd | 0	
MFC0 MTC0 DMFC0 DMTC0	Move From Coprocessor 0 Move To Coprocessor 0 Doubleword Move From Coprocessor 0 Doubleword Move To Coprocessor 0	MFC0 rt, rd MTC0 rt, rd DMFC0 rt, rd DMTC0 rt, rd
System control coprocessor instruction (2)	COP0 | CO | funct	
TLBR TLBWI TLBWR TLBP ERET	Read Indexed TLB Entry Write Indexed TLB Entry Write Random TLB Entry Probe TLB For Matching Entry Exception Return	TLBR TLBWI TLBWR TLBP ERET
System control coprocessor instruction (3)	COP0 | CO | funct	
STANDBY SUSPEND HIBERNATE	Standby Suspend Hibernate	STANDBY SUSPEND HIBERNATE
System control coprocessor instruction (4)	CACHE | base | sub | offset	
CACHE	Cache Operation	CACHE sub, offset (base)

22.1.3 Instruction execution time

In principle, the VR4111 executes one instruction in one cycle, but some instructions take two cycles or more.

(1) The data loaded by a load instruction cannot be used in the delay slot. If an instruction that uses load data is placed in the delay slot, the pipeline stalls.
A store instruction stalls by the delay slot if it is followed by a load instruction or MFC0.
If a branch instruction whose condition is satisfied or a jump instruction is executed, the instruction at the destination address is executed after the delay slot.

Table 22-4. Number of Delay Slot Cycles

Instruction Category	Necessary Number of Cycles (PCycle)
Load	1
Store	1
Jump	1
Branch	1

(2) The number of cycles indicated in the table below is necessary for executing an integer multiplication/division or sum-of-products operation instructions.
These instructions can be executed in parallel with other instructions, except those that access the HI/LO registers that store the result of an operation, and multiplication/division or sum-of-products operation instructions.

Table 22-5. Number of Execution Cycles of Integer Multiplication/Division Instructions

Instruction Category	Necessary Number of Cycles (PCycle)
MULT	1
MULTU	1
DIV	35
DIVU	35
DMULT	4
DMULTU	4
DDIV	67
DDIVU	67
MADD16	1
DMADD16	1

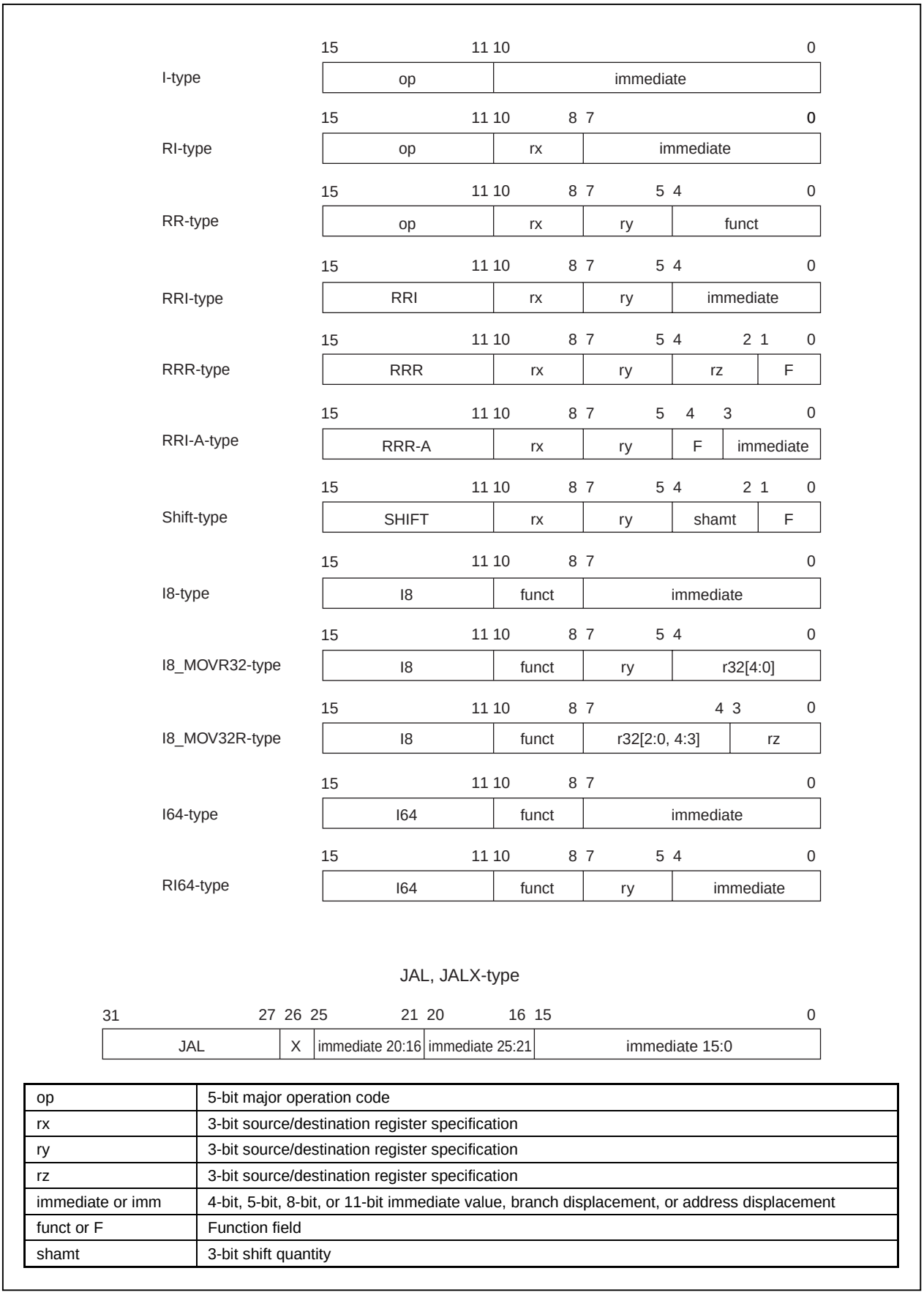
22.2 MIPS16 Instruction

MIPS16 instructions are 16 bits long and located at a half-word boundary. Therefore, instruction that is extended by the Extend instruction with immediate, and the JAL and JALX instructions are 32 bits long. There are 13 types of instruction formats available as shown in Figure 22-2.

Whether execution of the MIPS16 instructions is enabled or disabled is specified by the MIPS16EN pin on power application, and is indicated by config register CP0.

Figure 22-2 shows the formats of the MIPS16 instructions, and Table 22-6 lists the MIPS16 instruction set.

Figure 22-2. MIPS16 Instruction Format



op	5-bit major operation code
rx	3-bit source/destination register specification
ry	3-bit source/destination register specification
rz	3-bit source/destination register specification
immediate or imm	4-bit, 5-bit, 8-bit, or 11-bit immediate value, branch displacement, or address displacement
funct or F	Function field
shamt	3-bit shift quantity

Table 22-6. MIPS16 Instruction Set (1/2)

Instruction	Description	Format
Load/Store instructions		
LB	Load Bye	LB ry, offset (rx)
LBU	Load Byte Unsigned	LBU ry, offset (rx)
LH	Load Halfword	LH ry, offset (rx)
LHU	Load Halfword Unsigned	LHU ry, offset (rx)
LW	Load Word	LW ry, offset (rx)
		LW rx, offset (pc)
		LW rx, offset (sp)
LWU	Load Word Unsigned	LWU ry, offset (rx)
LD	Load Doubleword	LD ry, offset (rx)
		LD ry, offset (pc)
		LD ry, offset (sp)
SB	Store Byte	SB ry, offset (rx)
SH	Store Halfword	SH ry, offset (rx)
SW	Store Word	SW ry, offset (rx)
		SW rx, offset (sp)
		SW ra, offset (sp)
SD	Store Doubleword	SD ry, offset (rx)
		SD ry, offset (sp)
		SD ra, offset (sp)
ALU immediate instructions		
LI	Load Immediate	LI rx, immediate
ADDIU	Add Immediate Unsigned	ADDIU ry, rx, immediate
		ADDIU rx, immediate
		ADDIU sp, immediate
		ADDIU rx, pc, immediate
		ADDIU rx, sp, immediate
DADDIU	Doubleword Add Immediate Unsigned	DADDIU ry, rx, immediate
		DADDIU ry, immediate
		DADDIU ry, pc, immediate
		DADDIU ry, sp, immediate
		DADDIU sp, immediate
SLTI	Set on Less Than Immediate	SLTI rx, immediate
SLTIU	Set on Less Than Immediate Unsigned	SLTIU rx, immediate
CMPI	Compare Immediate	CMPI rx, immediate
2-/3-operand type instructions		
ADDU	Add Unsigned	ADDU rz, rx, ry
SUBU	Subtract Unsigned	SUBU rz, rx, ry
DADDU	Doubleword Add Unsigned	DADDU rz, rx, ry
DSUBU	Doubleword Subtract Unsigned	DSUBU rz, rx, ry
SLT	Set on Less Than	SLT rx, ry
SLTU	Set on Less Than Unsigned	SLTU rx, ry
CMP	Compare	CMP rx, ry
NEG	Negate	NEG rx, ry
AND	And	AND rx, ry
OR	Or	OR rx, ry
XOR	Exclusive Or	XOR rx, ry
NOT	Not	NOT rx, ry
MOVE	Move	MOVE ry, r32
		MOVE r32,rz

Table 22-6. MIPS16 Instruction Set (2/2)

Instruction	Description	Format
Special instructions		
EXTEND	Extend	EXTEND
BREAK	Breakpoint	BREAK immediate
Multiplication/division instructions		
MULT	Multiply	MULT rx, ry
MULTU	Multiply Unsigned	MULTU rx, ry
DIV	Divide	DIV rx, ry
DIVU	Divide Unsigned	DIVU rx, ry
MFHI	Move from HI	MFHI rx
MFLO	Move from LO	MFLO rx
DMULT	Doubleword Multiply	DMULT rx, ry
DMULTU	Doubleword Multiply Unsigned	DMULTU rx, ry
DDIV	Doubleword Divide	DDIV rx, ry
DDIVU	Doubleword Divide Unsigned	DDIVU rx, ry
Jump/branch instructions		
JAL	Jump and Link	JAL target
JALX	Jump and Link Exchange	JALX target
JR	Jump Register	JR rx
		JR ra
JALR	Jump and Link Register	JALR ra, rx
BEQZ	Branch on Equal to Zero	BEQZ rx, immediate
BNEZ	Branch on Not Equal to Zero	BNEZ rx, immediate
BTEQZ	Branch on T Equal To Zero	BTEQZ immediate
BTNEZ	Branch on T Not Equal To Zero	BTNEZ immediate
B	Branch Unconditional	B immediate
Shift instructions		
SLL	Shift Left Logical	SLL rx, ry, immediate
SRL	Shift Right Logical	SRL rx, ry, immediate
SRA	Shift Right Arithmetic	SRA rx, ry, immediate
SLLV	Shift Left Logical Variable	SLLV ry, rx
SRLV	Shift Right Logical Variable	SRLV ry, rx
SRAV	Shift Right Arithmetic Variable	SRAV ry, rx
DSLL	Doubleword Shift Left Logical	DSLL rx, ry, immediate
DSRL	Doubleword Shift Right Logical	DSRL ry, immediate
DSRA	Doubleword Shift Right Arithmetic	DSRA ry, immediate
DSLLV	Doubleword Shift Left Logical Variable	DSLLV ry, rx
DSRLV	Doubleword Shift Right Logical Variable	DSRLV ry, rx
DSRAV	Doubleword Shift Right Arithmetic Variable	DSRAV ry, rx

★23. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD2}	2.5 V (V_{DD}P, V_{DD}PD, V_{DD}2)	–0.5 to +3.6	V
	V_{DD3}	3.3 V (CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, V_{DD}3)	–0.5 to +4.0	V
Input voltage	V_I	$V_{DD3} \geq 3.7$ V	–0.5 to +4.0	V
		$V_{DD3} < 3.7$ V	–0.5 to V_{DD3} + 0.3	V
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

3. V_I can be –1.5 V if the input pulse is less than 10 ns.

Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{DD2}	2.5 V (V_{DD}P, V_{DD}PD, V_{DD}2)	2.3	2.7	V
	V_{DD3}	3.5 V (CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, V_{DD}3)	3.0	3.6	V
Ambient temperature	T_A		–10	+70	°C
Oscillation start voltage[Note 1]	V_{DDS}			3.0	V
Oscillation hold voltage[Note 2]	V_{DDH1}			2.5	V
Oscillation hold voltage[Note 3]	V_{DDH2}			3.0	V

Notes 1. This is a voltage at which oscillation is always started after power application, and is applied to oscillators of 32.768 kHz and 18.432 MHz.

2. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 32.768 kHz.

3. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 18.432 MHz.

Capacitance (T_A = 25°C, V_{DD} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		10	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.		10	pF

DC Characteristics (T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

(1/2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	I_{OH} = –2 mA	0.8V_{DD3}			V
Output voltage, high Note 1	V_{OH2}	I_{OH} = –12 mA	0.8V_{DD3}			V
Output voltage, low	V_{OL}	I_{OL} = 2 mA			0.4	V
		I_{OL} = 20 μA			0.1	
Output voltage, low Note 1	V_{OL2}	I_{OL} = 12 mA			0.4	V
		I_{OL} = 20 μA			0.1	
Input voltage, high Note 2	V_{IH1}		2.0		V_{DD3} + 0.3	V
Input voltage, low Note 2	V_{IL1}		–0.3		0.3V_{DD3}	V
		Pulse less than 10 ns	–1.5		0.3V_{DD3}	V
Input voltage, high Note 3	V_{IH2}		0.75V_{DD3}		V_{DD3} + 0.3	V
Input voltage, low Note 3	V_{IL2}		–0.3		0.6	V
		Pulse less than 10 ns	–1.5		0.6	V
Hysteresis voltage Note 4	V_H			0.17V_{DD3}		V
Input leakage current Note 5	I_{LI}	V_{DD3} = 3.6 V, V_I = V_{DD3}, 0 V			±5	μA
Input leakage current, high Note 6	I_{LIH}	V_{DD3} = 3.6 V, V_I = V_{DD3}			36	μA
Input leakage current, low Note 7	I_{LIL}	V_{DD3} = 3.6 V, V_I = 0 V			–36	μA
Output leakage current	I_{LO}	V_{DD3} = 3.6 V, V_I = V_{DD3}, 0 V			±5	μA

Notes 1. Applied to TPX (0:1), TPY (0:1). A panel resistance of 250 Ω is presumed.

2. Except RTCX1, CLKX1, FIRCLK, HSPSCLK, TPX (0:1), TPY (0:1), ADIN (0:2), AUDIOIN, POWER, RSTSW#, RTCRST#, DCD#/GPIO15, GPIO (0:14), BATTINH/BATTINT#, IRING, and KPORT (0:7) pins.

3. Applied to POWER, RSTSW#, RTCRST#, DCD#/GPIO15, GPIO (0:14), BATTINH/BATTINT#, IRING, and KPORT (0:7) pins.

4. Hysteresis voltage: Difference between the minimum voltage at which the high level of a Schmitt input signal is not recognized when the signal goes from low to high and the maximum voltage at which the low level is not recognized when the signal goes from high to low.

5. Except KPORT (0:7) (input pins with pull-down resistor).

6. Applied to KPORT (0:7) (input pins with pull-down resistor) and GPIO (0:14) when the internal pull-down resistor is used.

7. Applied to GPIO (0:14) when the internal pull-up resistor is used.

(2/2)

Parameter	Symbol	Condition	MIN.	TYP. Note 1	MAX.	Unit
Power supply current	I_{DD2} Note 2	In Fullspeed mode		60	140	mA
		In Standby mode		27	49	mA
		In Suspend mode		6	18	mA
		In Hibernate mode, V_{DD2} = 0.0 V, when LED unit is off.			0	μA
	I_{DD3} Note 3	In Fullspeed mode, ADD (0:25), RD#, WR#, TPX (0:1), TPY (0:1) = 120 pF, other pins = 40 pF		20	45	mA
		In Standby mode, external load 0 pF		6	12	mA
		In Suspend mode, external load 0 pF		0.5	2	mA
		In Hibernate mode, external load 0 pF, when LED unit is off.		5	50	μA
		In Hibernate mode, external load 0 pF, V_{DD3} = 2.5 V, when LED unit is off.		5	30	μA

Notes 1. Unless otherwise specified, these are reference values at T_A = 25°C, V_{DD2} = 2.5 V, V_{DD3} = 3.3 V.

2. Total current flowing to the V_{DD}P, V_{DD}PD, and V_{DD2} pins.

3. Total current flowing to the CV_{DD}, DV_{DD}, AV_{DD}, $PIUV_{DD}$, and V_{DD}3 pins.

Remark I_{DD2} and I_{DD3} do not reach the maximum value at the same time in the Fullspeed mode.

Data Retention Characteristics (T_A = 25°C)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data retention voltage Note 1	V_{DDDR3}	Hibernate mode, 3.3-V power supply	2.5	3.6	V
Data retention input voltage, high Note 2	V_{IHDR}		$0.9V_{DDDR3}$		V

Notes 1. The data retention voltage is the voltage at which the operation of the Elapsed Time timer and the data retention of the registers of the following peripheral units are guaranteed, and is not applied to the internal data of the CPU core.

BCU: BCURFCNTREG, BCUCNTREG3

PUM: PMUCNTREG (15:8), PMUCNT2REG, PMUWAITREG

RTC: ETIMELREG, ETIMEMREG, ETIMEHREG, ECMPLREG, ECMPMREG, ECMPHREG, RTCL1LREG, RTCL1HREG, RTCL1CNTLREG, RTCL1CNTHREG, RTCL2LREG, RTCL2HREG, RTCL2CNTLREG, RTCL2CNTHREG, RTCINTREG (2:0)

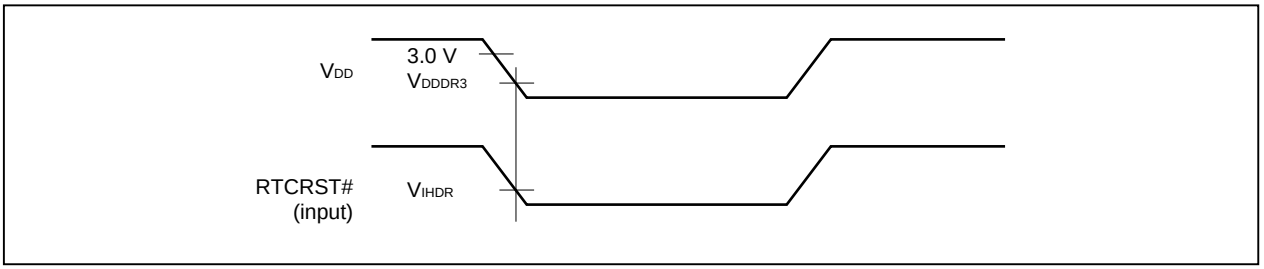
GIU: GIUPODATL, GIUPODATH, GIUUSEUPNL, GIUTERMUPNL

KIU: KIUGPEN, PORTREG

LED: LEDHTSREG, LEDLTSREG, LEDHLTCLREG, LEDHLTCHREG, LEDCNTREG

2. Applied to RTCRST# pin.

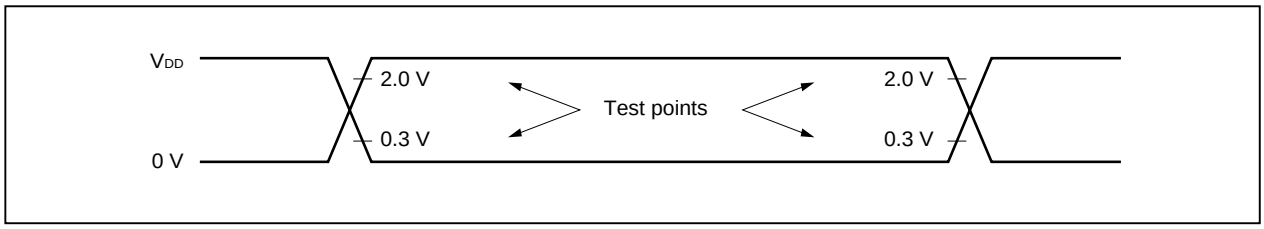
Remark The values in parentheses are the targeted values.



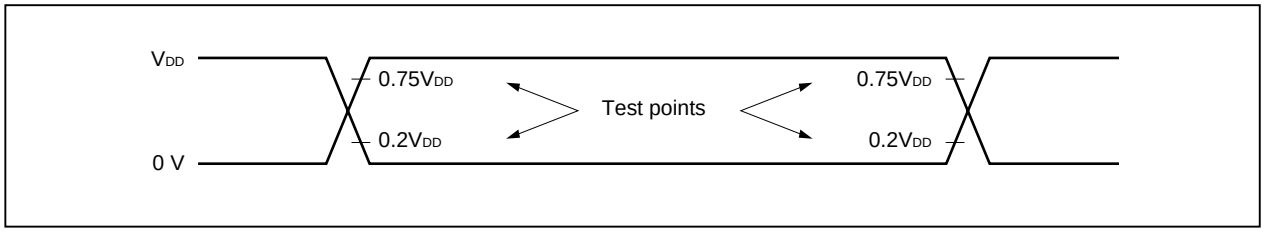
AC Characteristics (T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

AC test input waveform

(a) CTS#, DATA (0:15), DATA (16:31)/GPIO (16:31), DBUS32/GPIO48, DCTS#/GPIO47, DDIN/GPIO45, DSR#, DTR#/CLKSEL0, FS, FIRDIN#/SEL, GPIO49, HLDRQ#, ILCSENSE, IOCHRDY, IOCS16#, IRDIN, LCDRDY, MEMCS16#, RxD, RTS#/CLKSEL1, SDI, TxD/CLKSEL2, ZWS#

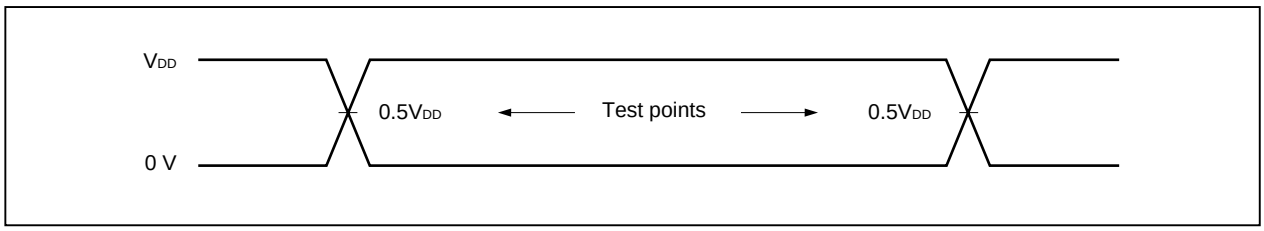


(b) BATTINH/BATTINT#, DCD#/GPIO15, GPIO (0:14), IRING, KPORT (0:7), POWER, RSTSW#, RTCRST#



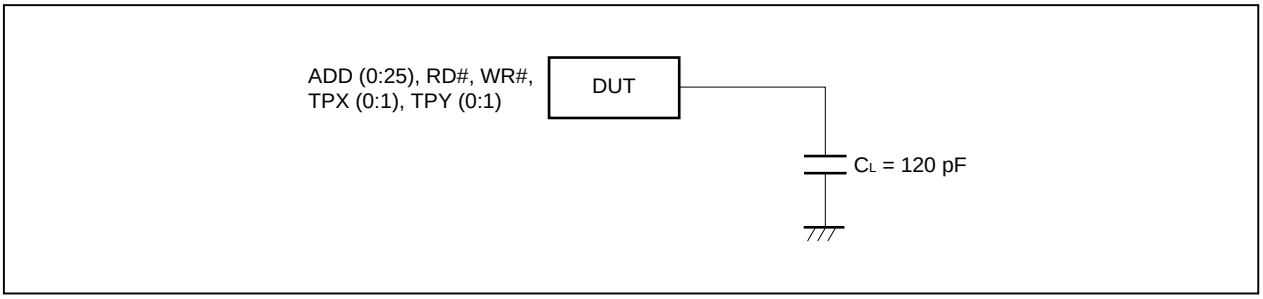
AC test output measuring points

(c) ADD (0:25), AFERST#, BUSCLK, GPIO49, DATA (0:15), DATA (16:31)/GPIO (16:31), DBUS32/GPIO48, DCTS#/GPIO47, DDIN/GPIO45, DDOUT/GPIO44, DRTS#/GPIO46, DTR#/CLKSEL0, FIRDIN#/SEL, GPIO (0:14), GPIO49, HC0, HLDACK#, HSPMCLK, IOR#, IOW#, IRDOUT#, KSCAN (0:11)/GPIO (32:43), LCAS#, LCDCS#, LEDOUT#, MEMR#, MEMW#, MPOWER, MRAS (0:1)#, MUTE, OFFHOOK, OPD#, POWERON, RD#, ROMCS (0:3)#, RSTOUT, RTS#/CLKSEL1, SDO, SHB#, TELCON, TPX (0:1), TPY (0:1), TxD/CLKSEL2, UCAS#, ULCAS#/MRAS2#, UUCAS#/MRAS3#, WR#

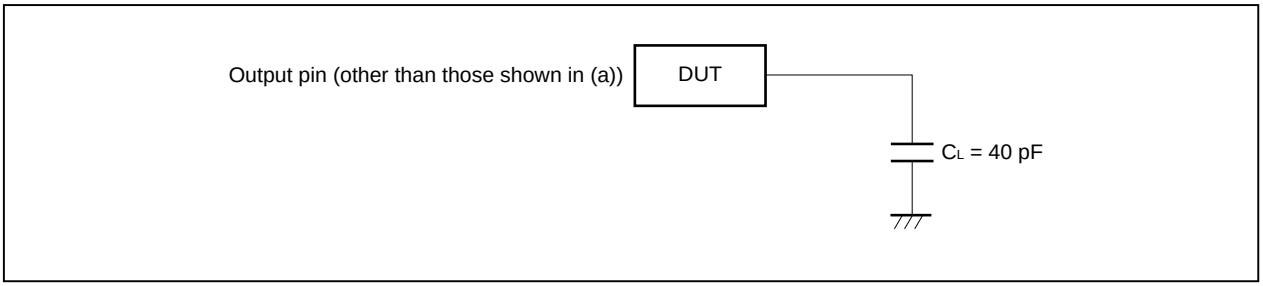


Load condition

(a) ADD (0:25), RD#, WR#, TPX (0:1), TPY (0:1)



(b) Other output pins



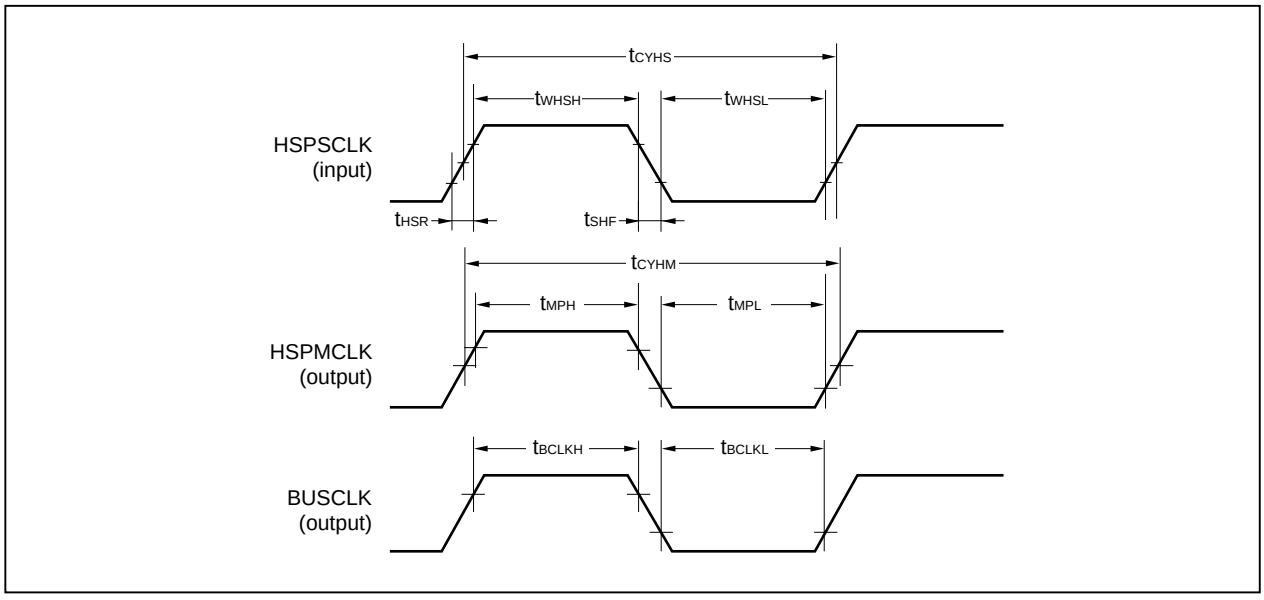
(1) Clock parameter

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
HSPSCLK high-level width	t_{WHSH}	When HSP unit is used	40			ns
HSPSCLK low-level width	t_{WHSL}	When HSP unit is used	40			ns
HSPSCLK clock frequency	t_{HSCYC}	When HSP unit is used			f_{CYC}	MHz
HSPSCLK clock cycle	t_{CYHS}	When HSP unit is used	108.5			ns
HSPSCLK clock rise time	t_{HSR}	When HSP unit is used			10	ns
HSPSCLK clock fall time	t_{SHF}	When HSP unit is used			10	ns
HSPMCLK high-level width	t_{MPH}	When HSP unit is used	$t_{CYHM} \times 0.45$		$t_{CYHM} \times 0.55$	ns
HSPMCLK low-level width	t_{MPL}	When HSP unit is used	$t_{CYHM} \times 0.45$		$t_{CYHM} \times 0.55$	ns
HSPMCLK clock frequency	t_{MCYC}	When HSP unit is used	0.585		18.432	MHz
HSPMCLK clock cycle	t_{CYHM}	When HSP unit is used	54.253		1790.365	ns
BUSCLK high-level width	t_{BCLKH}		45			ns
BUSCLK low-level width	t_{BCLKL}		45			ns
FIRCLK input frequency Note 1	$t_{FIRCYC1}$	In FIR 4 Mbps	47.996	48.000	48.005	MHz
	$t_{FIRCYC2}$	In FIR 1.152/0.576 Mbps	47.952	48.000	48.048	MHz
FIR clock duty Note 1	$t_{FIRDUTY}$		10		90	%
CPU core operating frequency	f_{PCYC}	CLKSEL (2:0) = 111 Note 2		RFU		MHz
		CLKSEL (2:0) = 110 Note 2		RFU		MHz
		CLKSEL (2:0) = 101 Note 2		RFU		MHz
		CLKSEL (2:0) = 100 Note 2		RFU		MHz
		CLKSEL (2:0) = 011		69.3		MHz
		CLKSEL (2:0) = 010		65.4		MHz
		CLKSEL (2:0) = 001		62.0		MHz
		CLKSEL (2:0) = 000		49.1		MHz

Notes 1. Applied to FIRCLK pin.

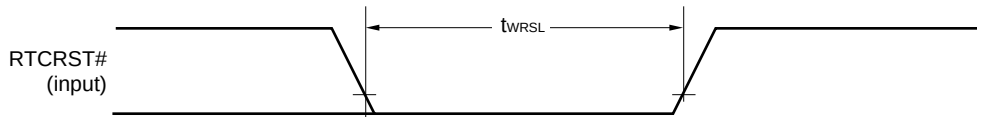
2. Do not set CLKSEL2 to 1.

Remark CLKSEL (2:0): Value set to the TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0 pins after reset.



(2) Reset parameter

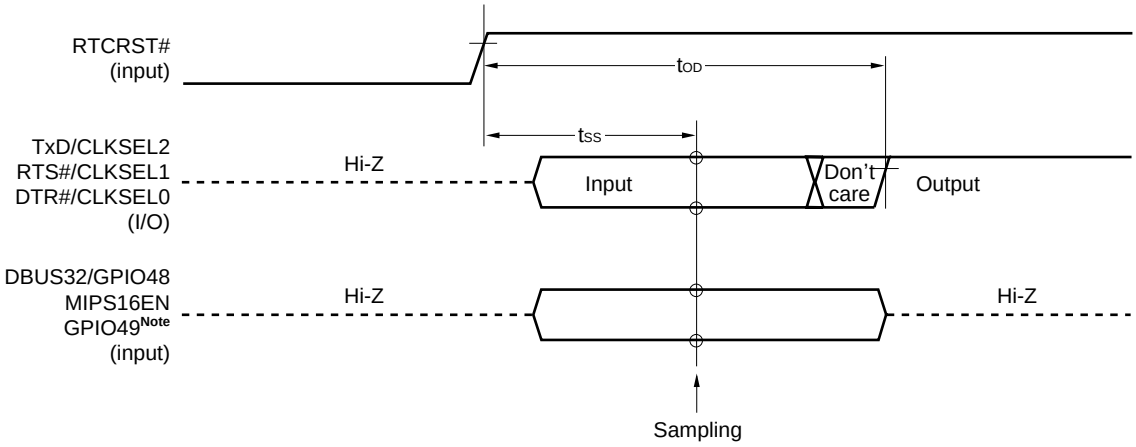
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RTCRST# pin	305		μs



Remark For the RTCRST# characteristics at power application, refer to **VR4111 User's Manual**.

(3) Initialization parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RTCRST# ↑)	t_{SS}			61.04	μs
Output delay time (from RTCRST# ↑)	t_{OD}		61.04		μs



Note Be sure to input a low level to GPIO49 in this timing.

Remark Set the input data level by using a pull-up or pull-down resistor with high resistance.

(4) GPIO interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{INP1}	**Note 1**	91.5		μs
	t_{INP2}	**Note 2**	361.5		ns
	t_{INP3}	**Note 3**	180.6		ns
GPIO input rise time	t_{GPINR1}	**Note 4**		200	ns
	t_{GPINR2}	**Note 5**		10	ns
GPIO input fall time	t_{GPINF1}	**Note 4**		200	ns
	t_{GPINF2}	**Note 5**		10	ns
Output level width	t_{OUTP}	**Note 6**	30		ns

Notes 1. Applied to GPIO (0:3) pins.

2. Applied to DCD#/GPIO15 and GPIO (9:14) pins.

3. Applied to DATA (16:31)/GPIO (16:31) and GPIO (4:8) pins.

4. Applied to GPIO (0:14) and DCD#/GPIO15 pins.

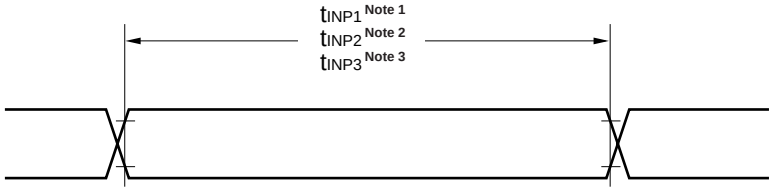
5. Applied to DATA (16:31)/GPIO (16:31) pins.

6. Applied to GPIO (0:14), DATA (16:31)/GPIO (16:31), KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, and GPIO49 pins.

Caution These parameters are applied when the DATA (16:31)/GPIO (16:31), DCD#/GPIO15, KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, or GPIO49 pin is used as the GPIO pin.

(4) GPIO interface parameter (2/2)

(a) Input level width

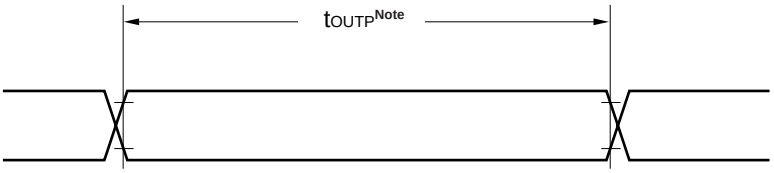


Notes 1. GPIO (0:3)
2. DCD#/GPIO15, GPIO (9:14)
3. DATA (16:31)/GPIO (16:31), GPIO (4:8)

(b) GPIO input rise/fall time

Notes 1. DCD#/GPIO15, GPIO (0:14)
2. DATA (16:31)/GPIO (16:31)

(c) Output level width



Note GPIO (0:14), DATA (16:31)/GPIO (16:31), KSCAN (0:11)/GPIO (32:43), DDOUT/GPIO44, DDIN/GPIO45, DRTS#/GPIO46, DCTS#/GPIO47, DBUS32/GPIO48, GPIO49

(5) EDO-type DRAM read parameter (1/2)

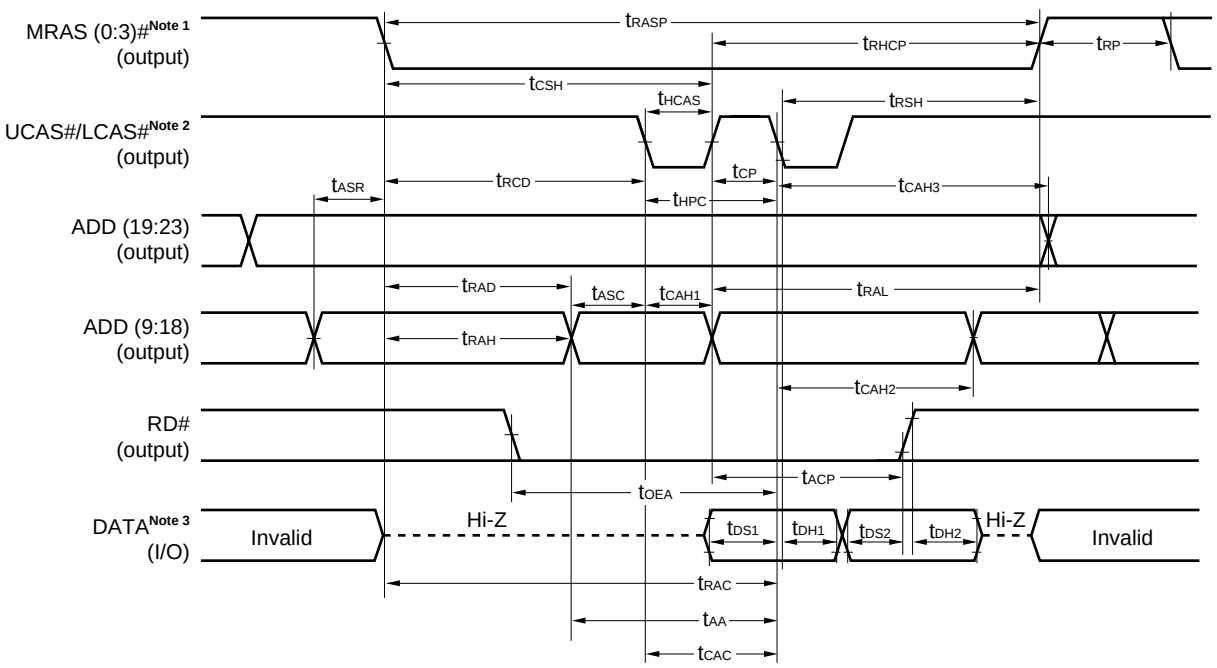
The target DRAM is the μPD42S16165L-A60, 42S16165L-A70, 42S18165L-A60, 42S18165L-A70, 42S64165G5-A50, 42S64165G5-A60, 42S65165G5-A50, or 42S65165G5-A60.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width	t_{RASP}		75		ns
MRAS (0:3)# hold time (from UCAS#/LCAS# precharge)	t_{RHCP}		45		ns
MRAS (0:3)# precharge time	t_{RP}		55		ns
UCAS#/LCAS# hold time (from MRAS (0:3)#)	t_{CSH}		55		ns
UCAS#/LCAS# pulse width	t_{HCAS}		12		ns
UCAS#/LCAS# precharge time	t_{CP}		10		ns
Read/write cycle time	t_{HPC}		31		ns
MRAS (0:3)# hold time (from UCAS#/LCAS#)	t_{RSH}		20		ns
Row address setup time (to MRAS (0:3)#)	t_{ASR}		0		ns
UCAS#/LCAS# ↓ delay time from MRAS (0:3)# ↓	t_{RCD}		19		ns
Column address delay time from MRAS (0:3)# ↓	t_{RAD}		17		ns
Column address setup time (to UCAS#/LCAS#)	t_{ASC}		0		ns
Column address read time (to MRAS (0:3)#↑)	t_{RAL}		40		ns
Row address hold time (from MRAS (0:3)# ↓)	t_{RAH}		15		ns
Column address hold time 1 (from UCAS#/LCAS# ↓)	t_{CAH1}		10		ns
Column address hold time 2 (from UCAS#/LCAS# ↓)	t_{CAH2}		10		ns
Column address hold time 3 (from UCAS#/LCAS# ↓)	t_{CAH3}		10		ns
Data access time (from UCAS#/LCAS# precharge)	t_{ACP}		45		ns
Data access time (from RD# ↓)	t_{OEA}		23		ns
Data input setup time 1 (to UCAS#/LCAS# ↓)	t_{DS1}		0		ns
Data input hold time 1 (from MRAS (0:3)#)	t_{DH1}		6		ns
Data input setup time 2 (to UCAS#/LCAS# ↓)	t_{DS2}		0		ns
Data input hold time 2 (from MRAS (0:3)#)	t_{DH2}		6		ns
Data access time (from MRAS (0:3)# ↓)	t_{RAC}		75		ns
Data access time (from column address)	t_{AA}		37		ns
Data access time (from UCAS#/LCAS# ↓)	t_{CAC}		23		ns

Caution These ratings are applied only when a device operates within the recommended operating condition range and the operating ambient temperature is kept constant.

If the power supply voltage or operating ambient temperature changes during DRAM access, the above ratings are not applied.

(5) EDO-type DRAM read parameter (2/2)



Notes 1. In 32-bit mode: Applied to MRAS (0:1)#
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)#

2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS#
In 16-bit mode: Applied to UCAS# and LCAS#

3. In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15)
In 16-bit mode: Applied to DATA (0:15)

Remark The broken lines indicate high impedance.

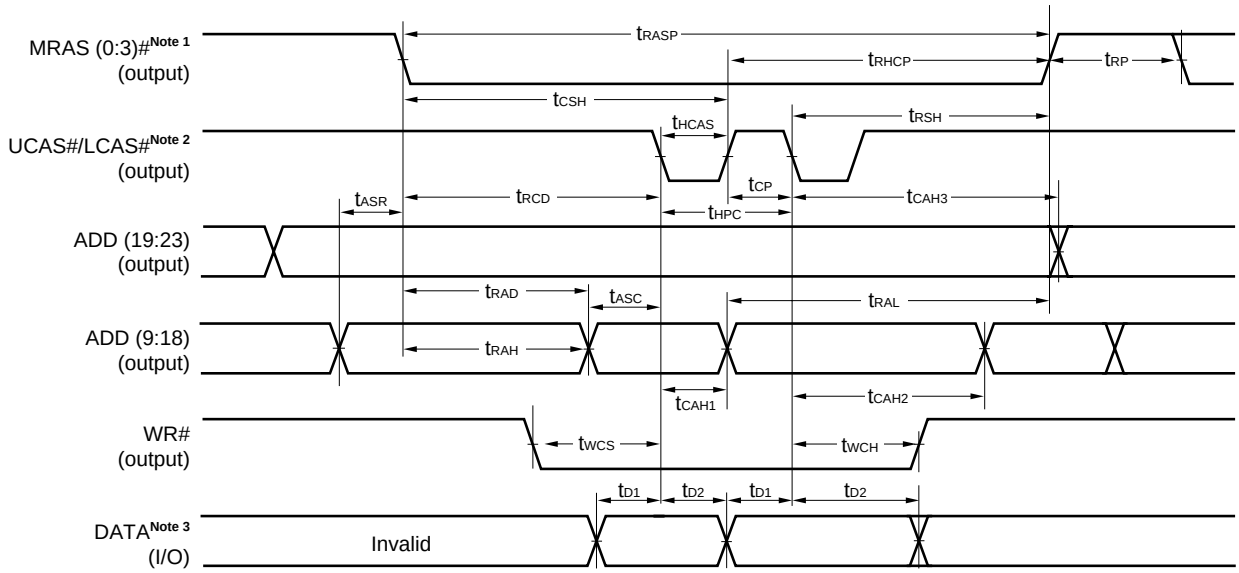
(6) EDO-type DRAM write parameter (1/2)

The target DRAM is the μPD42S16165L-A60, 42S16165L-A70, 42S18165L-A60, 42S18165L-A70, 42S64165G5-A50, 42S64165G5-A40, 42S65165G5-A50, or 42S65165G5-A60.

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width	t_{RASP}		75		ns
MRAS (0:3)# hold time (from UCAS#/LCAS# precharge)	t_{RHCP}		45		ns
MRAS (0:3)# precharge time	t_{RP}		55		ns
UCAS#/LCAS# hold time (from MRAS (0:3)# ↓)	t_{CSH}		55		ns
UCAS#/LCAS# pulse width	t_{HCAS}		12		ns
UCAS#/LCAS# precharge time	t_{CP}		10		ns
Read/write cycle time	t_{HPC}		31		ns
MRAS (0:3)# hold time (from UCAS#/LCAS#)	t_{RSH}		20		ns
Row address setup time (to MRAS (0:3)# ↓)	t_{ASR}		0		ns
UCAS#/LCAS# ↓ delay time from MRAS (0:3)# ↓	t_{RCD}		19		ns
Column address delay time from MRAS (0:3)# ↓	t_{RAD}		17		ns
Column address setup time (to UCAS#/LCAS# ↓)	t_{ASC}		0		ns
Column address read time (to MRAS (0:3)# ↑)	t_{RAL}		40		ns
Row address hold time (from MRAS (0:3)# ↓)	t_{RAH}		15		ns
Column address hold time 1 (from UCAS#/LCAS# ↓)	t_{CAH1}		10		ns
Column address hold time 2 (from UCAS#/LCAS# ↓)	t_{CAH2}		10		ns
Column address hold time 3 (from UCAS#/LCAS# ↓)	t_{CAH3}		10		ns
WR# setup time	t_{WCS}		0		ns
WR# hold time (from UCAS#/LCAS# ↓)	t_{WCH}		15		ns
Data output setup time	t_{D1}		0		ns
Data output hold time	t_{D2}		10		ns

Caution These ratings are applied only when a device operates within the recommended operating condition range and the operating ambient temperature is kept constant.
If the power supply voltage or operating ambient temperature changes during DRAM access, the above ratings are not applied.

(6) EDO-type DRAM write parameter (2/2)



Notes 1. In 32-bit mode: Applied to MRAS (0:1)#
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)#

2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS#
In 16-bit mode: Applied to UCAS# and LCAS#

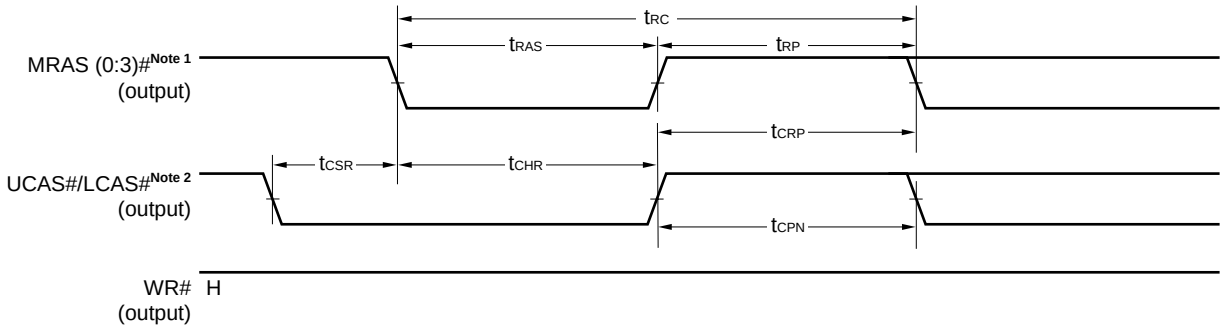
3. In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15)
In 16-bit mode: Applied to DATA (0:15)

(7) DRAM refresh parameter

The target DRAM is the μPD42S161615L-A60, 42S16165L-A70, 42S18165L-A60, 42S18165L-A70, 42S64165G5-A50, 42S64165G5-A60, 42S65165G5-A50, or 42S65165G5-A60.

(a) CAS-before-RAS refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Read/write cycle time	t_{RC}		124		ns
MRAS (0:3)# pulse width	t_{RAS}		70		ns
MRAS (0:3)# precharge time	t_{RP}		50		ns
UCAS#/LCAS# setup time (to MRAS (0:3)# ↓)	t_{CSR}		5		ns
UCAS#/LCAS# hold time (from MRAS (0:3)# ↓)	t_{CHR}		10		ns
MRAS (0:3)# precharge time from UCAS#/LCAS# ↑	t_{CRP}		5		ns
UCAS#/LCAS# precharge time	t_{CPN}		10		ns



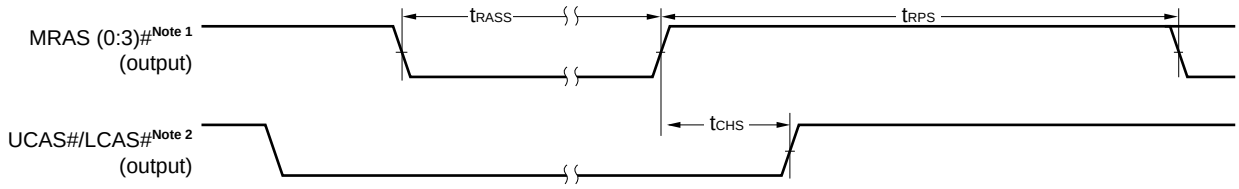
Notes 1. In 32-bit mode: Applied to MRAS (0:1)#
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)#

2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS#
In 16-bit mode: Applied to UCAS# and LCAS#

(b) CAS-before-RAS self-refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
MRAS (0:3)# pulse width[Note]	t_{RASS}		100		μs
MRAS (0:3)# precharge time	t_{RPS}		130		ns
UCAS#/LCAS# hold time	t_{CHS}		–50		ns

Note The CAS-before-RAS self-refresh parameter is valid when t_{RASS} exceeds 100 μs.



Notes 1. In 32-bit mode: Applied to MRAS (0:1)#
In 16-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#/MRAS2#, and MRAS (0:1)#

2. In 32-bit mode: Applied to UUCAS#/MRAS3#, ULCAS#MRAS2#, UCAS#, and LCAS#
In 16-bit mode: Applied to UCAS# and LCAS#

(8) Normal ROM parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}		T × N – 19		ns
Data access time (from ROMCS (0:3)# ↓)Note	t_{CE}		T × N – 19		ns
Data access time (from RD#↓)Note	t_{OE}		T × (N – 1) – 29		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		6		ns

Note The value of N is set by using the WROMA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

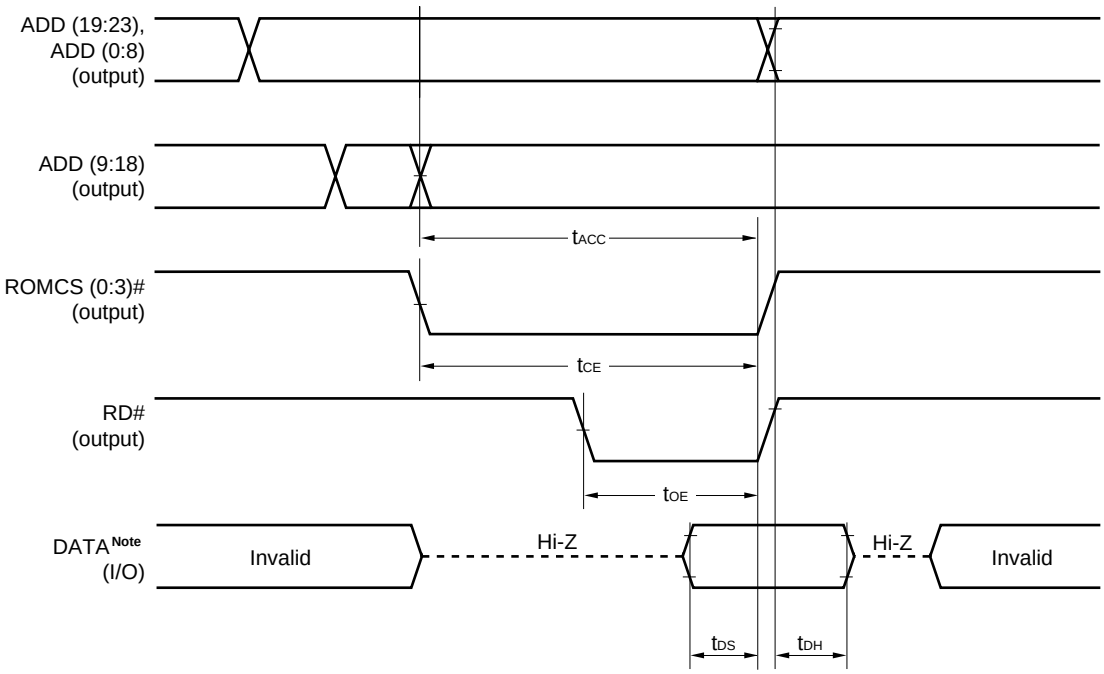
CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1Note	1Note	1Note	RFU
1Note	1Note	0Note	RFU
1Note	0Note	1Note	RFU
1Note	0Note	0Note	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

WROMA2	WROMA1	WROMA0	N
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2

Note Do not set CLKSEL2 to 1.

(8) Normal ROM parameter (2/2)

When WROMA (0:2) = 111



Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15)
In 16-bit mode: Applied to DATA (0:15)

Remark The broken lines indicate high impedance.

(9) Page ROM parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address) 1 Note	t_{ACC1}		T × N – 19		ns
Data access time (from address) 2 Note	t_{ACC2}		T × M – 12		ns
Data access time (from ROMCS (0:3)# ↓) Note	t_{CE}		T × N – 19		ns
Data access time (from RD#↓) Note	t_{OE}		T × (N – 1) – 29		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		6		ns

Note The value of N is set by using the WROMA (0:2) bits of the BCUSPEEDREG register.
The value of M is set by using the WPROM (0:1) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

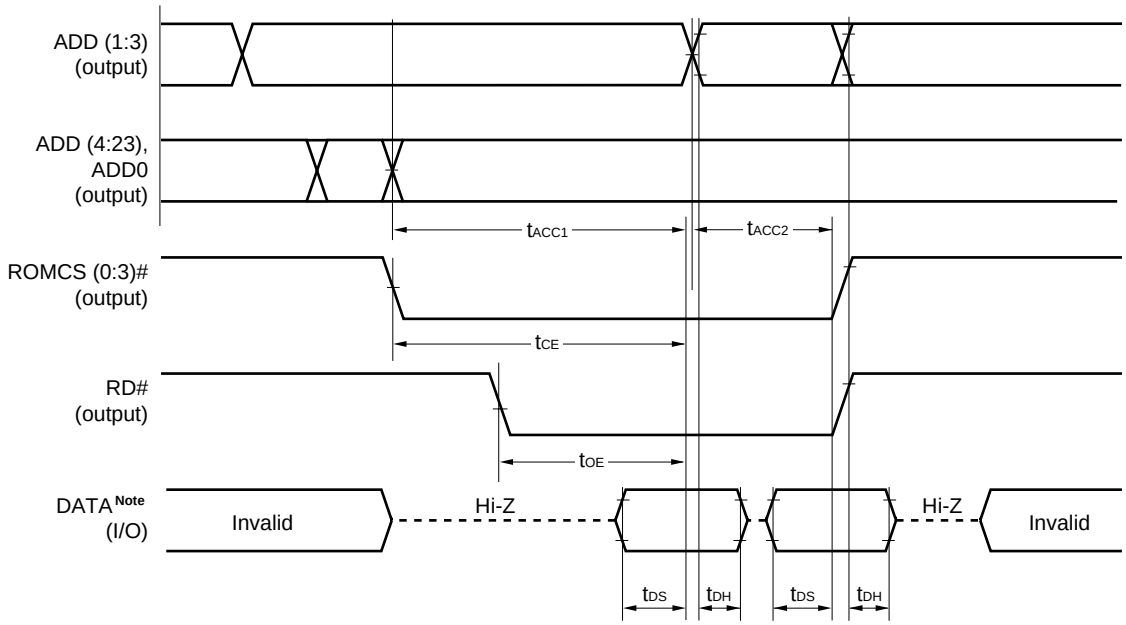
CLKSEL 2	CLKSEL 1	CLKSEL 0	T (ns)
1 Note	1 Note	1 Note	RFU
1 Note	1 Note	0 Note	RFU
1 Note	0 Note	1 Note	RFU
1 Note	0 Note	0 Note	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

WROMA 2	WROMA 1	WROMA 0	N (TClock)
0	0	0	9
0	0	1	8
0	1	0	7
0	1	1	6
1	0	0	5
1	0	1	4
1	1	0	3
1	1	1	2

WPROM 1	WPROM 0	M (TClock)
0	0	3
0	1	2
1	0	1
1	1	—

Note Do not set CLKSEL2 to 1.

(9) Page ROM parameter (2/2)

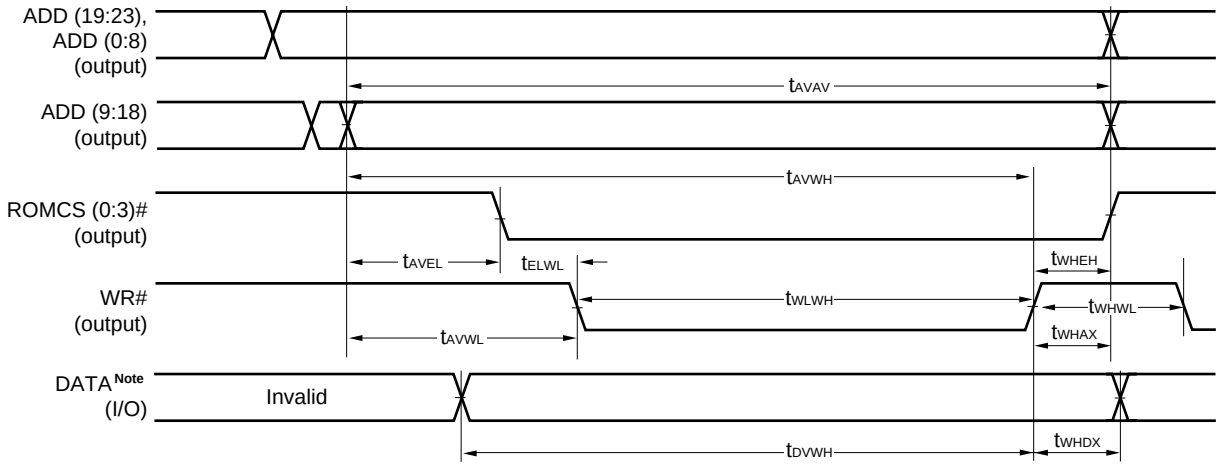


Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15)
In 16-bit mode: Applied to DATA (0:15)

Remark The broken lines indicate high impedance.

(10) Flash memory mode write parameter

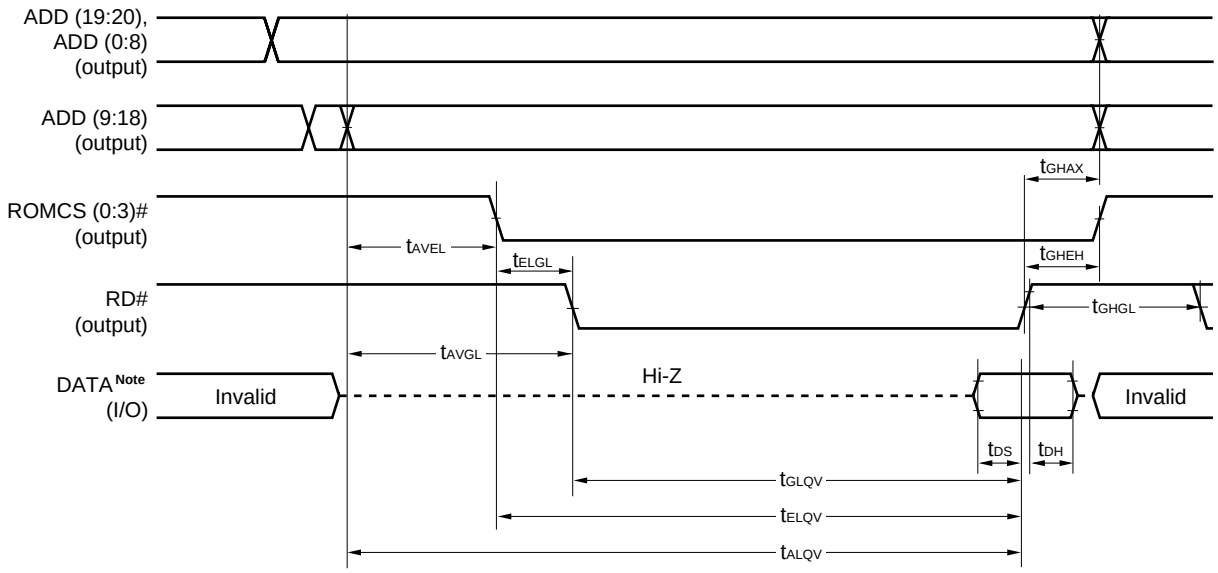
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Write cycle time	t_{AVAV}		150		ns
Address setup time (to WR# ↑)	t_{AVWH}		75		ns
Address setup time (to ROMCS (0:3)# ↓)	t_{AVEL}		0		ns
ROMCS (0:3)# setup time (to WR#↓)	t_{ELWL}		10		ns
WR# low-level width	t_{WLWH}		75		ns
ROMCS (0:3)# hold time (from WR# ↑)	t_{WHEH}		10		ns
Address hold time (from WR# ↑)	t_{WHAX}		10		ns
WR# high-level width	t_{WHWL}		75		ns
Address setup time (to WR# ↓)	t_{AVWL}		25		ns
Data output setup time (to WR# ↑)	t_{DVWH}		75		ns
Data output hold time (from WR# ↑)	t_{WHDX}		10		ns



Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15)
In 16-bit mode: Applied to DATA (0:15)

(11) Flash memory mode read parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data output delay time from address	t_{AVQV}		180		ns
Data output delay time from ROMCS (0:3)#	t_{ELQV}		180		ns
Address setup time (to ROMCS (0:3)# ↓)	t_{AVEL}		0		ns
Data output delay time from RD# ↓	t_{GLQV}		80		ns
Address setup time (to RD# ↓)	t_{AVGL}		0		ns
ROMCS (0:3)# hold time (from RD# ↑)	t_{GHEH}		10		ns
Address hold time (from RD# ↑)	t_{GHAX}		10		ns
RD# high-level width	t_{GHGL}		75		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		6		ns
ROMCS (0:3)# setup time (to RD# ↓)	t_{ELGL}		10		ns



Note In 32-bit mode: Applied to DATA (16:31)/GPIO (16:31) and DATA (0:15)
In 16-bit mode: Applied to DATA (0:15)

Remark The broken lines indicate high impedance.

(12) System bus parameter (IOCHRDY) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
BUSCLK low-level width	t_{BCLKL}		45		ns
BUSCLK high-level width	t_{BCLKH}		45		ns
Address setup time (to BUSCLK)	t_{AVCK}		15		ns
Address setup time (to command signal ↓) Notes 1, 2	t_{AVCL}		T × N – 29		ns
Command signal setup time (to BUSCLK) Note 1	t_{CLCK}		15		ns
Command signal low-level width Notes 1, 2	t_{CLCH}		2 × T × N – 29		ns
Address hold time (from command signal ↑) Note 1	t_{CHAV}		25		ns
Command signal recovery time Notes 1, 2	t_{CHCL}		T × (N + 1) – 29		ns
IOCHRDY sampling time Note 2	t_{CLR}		0	T × N – 44	ns
Command signal ↑ delay time from IOCHRDY ↑ Notes 1, 2	t_{RHCH}		T × N	2 × T × N + 29	ns
IOCHRDY hold time (from command signal ↑) Note 1	t_{CHRL}		0		ns
Data output setup time (to command signal ↓) Note 1	t_{DVCL}		0		ns
Data output hold time (from command signal ↑) Note 1	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start time Note 2	t_{AVSV1}		2 × T × N – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↓) Note 1	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		15		ns

Notes 1. With the V_R4111, the MEMW#, MEMR#, IOW#, and IOR# pins are called the command signals for the system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1 Note	1 Note	1 Note	RFU
1 Note	1 Note	0 Note	RFU
1 Note	0 Note	1 Note	RFU
1 Note	0 Note	0 Note	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

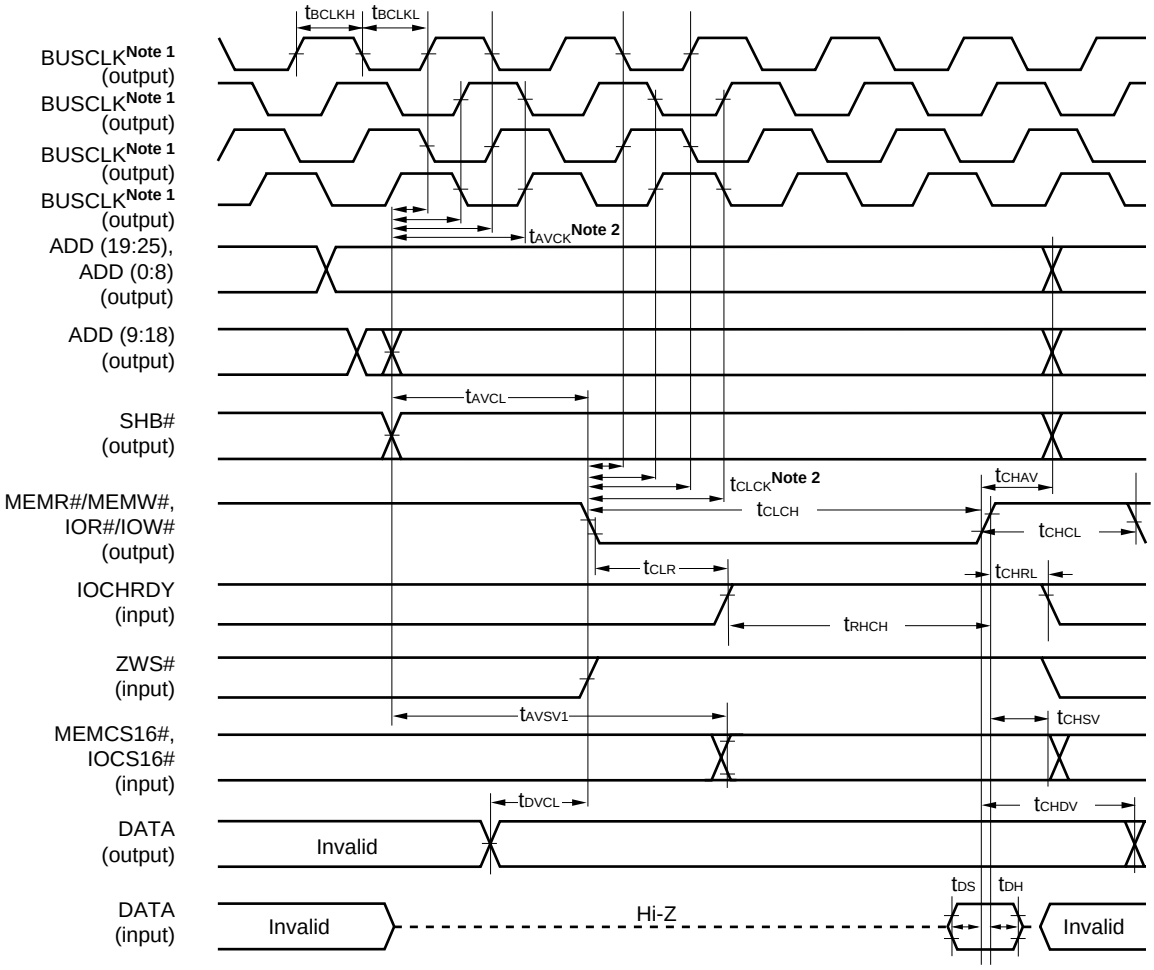
Note Do not set CLKSEL2 to 1.

WISAA2	WISAA1	WISAA0	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1 Note	0 Note	0 Note	4
1 Note	0 Note	1 Note	3
1	1	0	—
1	1	1	—

Note If the WISAA (0:2) bits are set to 100 or high, the AC characteristics of t_{AVCK} and t_{CLCK} are not guaranteed.

(12) System bus parameter (IOCHRDY) (2/2)

When WISAA (0:2) = 010



Notes 1. BUSCLK indicates that there are four possible relationships between BUSCLK and other system bus interface signals.

2. This indicates the minimum setup time to the BUSCLK rising or falling edge.

Remark The broken lines indicate high impedance.

(13) System bus parameter (ZWS#) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to BUSCLK)	t_{AVCK}		15		ns
Address setup time (to command signal ↓)Notes 1, 2	t_{AVCL}		T × N – 29		ns
Command signal setup time (to BUSCLK)Note 1	t_{CLCK}		15		ns
Command signal low-level widthNotes 1, 2	t_{CLCH}		T × N – 31		ns
Address hold time (from command signal ↑)Note 1	t_{CLAV}		25		ns
Command signal recovery timeNotes 1, 2	t_{CHCL}		T × (N + 1) – 29		ns
ZWS# ↓ delay time from command signal ↓Notes 1, 2	t_{CLZL}			T × (N – 1) – 20	ns
ZWS# hold time (from command signal ↑)Note 1	t_{CHZH}		0		ns
Data output setup time (to command signal ↓)Note 1	t_{DVCL}		0		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start timeNote 2	t_{AVSV2}		2 × T × (N – 1) – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↑)Note 1	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		15		ns

Notes 1. With the VR4111, the MEMW#, MEMR#, IOW#, and IOR# pins are called the command signals for the system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1Note	1Note	1Note	RFU
1Note	1Note	0Note	RFU
1Note	0Note	1Note	RFU
1Note	0Note	0Note	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

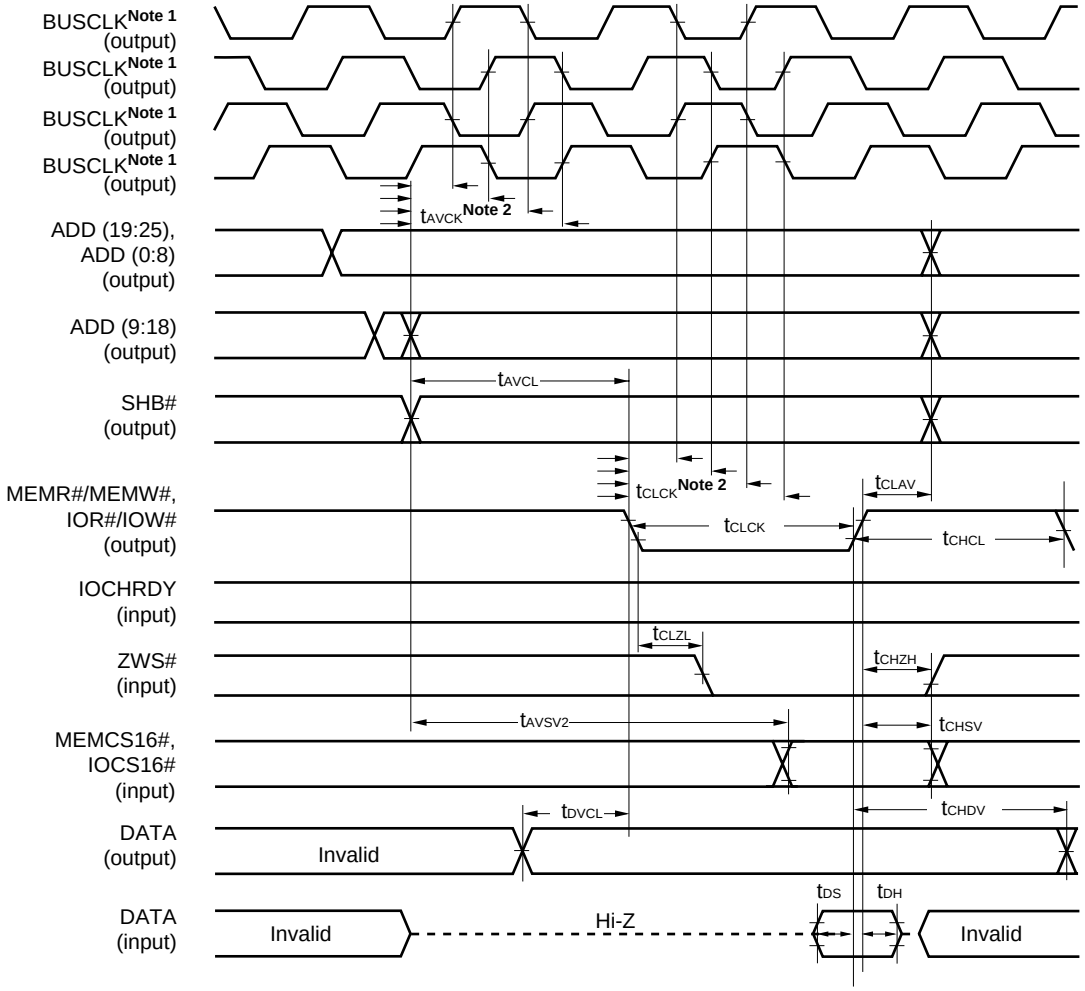
Note Do not set CLKSEL2 to 1.

WISAA2	WISAA1	WISAA0	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1Note	0Note	0Note	4
1Note	0Note	1Note	3
1	1	0	—
1	1	1	—

Note If the WISAA (0:2) bits are set to 100 or high, the AC characteristics of t_{CLCK} and t_{AVCK} are not guaranteed.

(13) System bus parameter (ZWS#) (2/2)

When WISAA (0:2) = 101



Notes 1. BUSCLK indicates that there are four possible relationships between BUSCLK and other system bus interface signals.

2. This indicates the minimum setup time to the BUSCLK rising or falling edge.

Remark The broken lines indicate high impedance.

(14) High-speed system bus parameter (IOCHRDY) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)Notes 1, 2	t_{AVCL}		T × N – 29		ns
Command signal low-level widthNotes 1, 2	t_{CLCH}		T × (N + M) – 29		ns
Address hold time (from command signal ↑)Note 1	t_{CHAV}		25		ns
Command signal recovery timeNotes 1, 2	t_{CHCL}		T × (N + 1) – 29		ns
IOCHRDY sampling start time	t_{CLR}		0		ns
Command signal ↑ delay time from IOCHRDY ↑Notes 1, 2	t_{RHCH}		T × M	T × (N + M) + 29	ns
IOCHRDY hold time (from command signal ↑)Note 1	t_{CHRL}		0		ns
Data output setup time (to command signal ↓)Note 1	t_{DVCL}		–15		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start timeNote 2	t_{AVSV1}		2 × T × N – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↑)Note 1	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		15		ns

Notes 1. With the VR4111, the MEMW# and MEMR# signals are called the command signals for the high-speed system bus interface.

2. The values of N and M are set by using the WLCD/M (0:2) bits of the BCUSPEEDREG register. The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

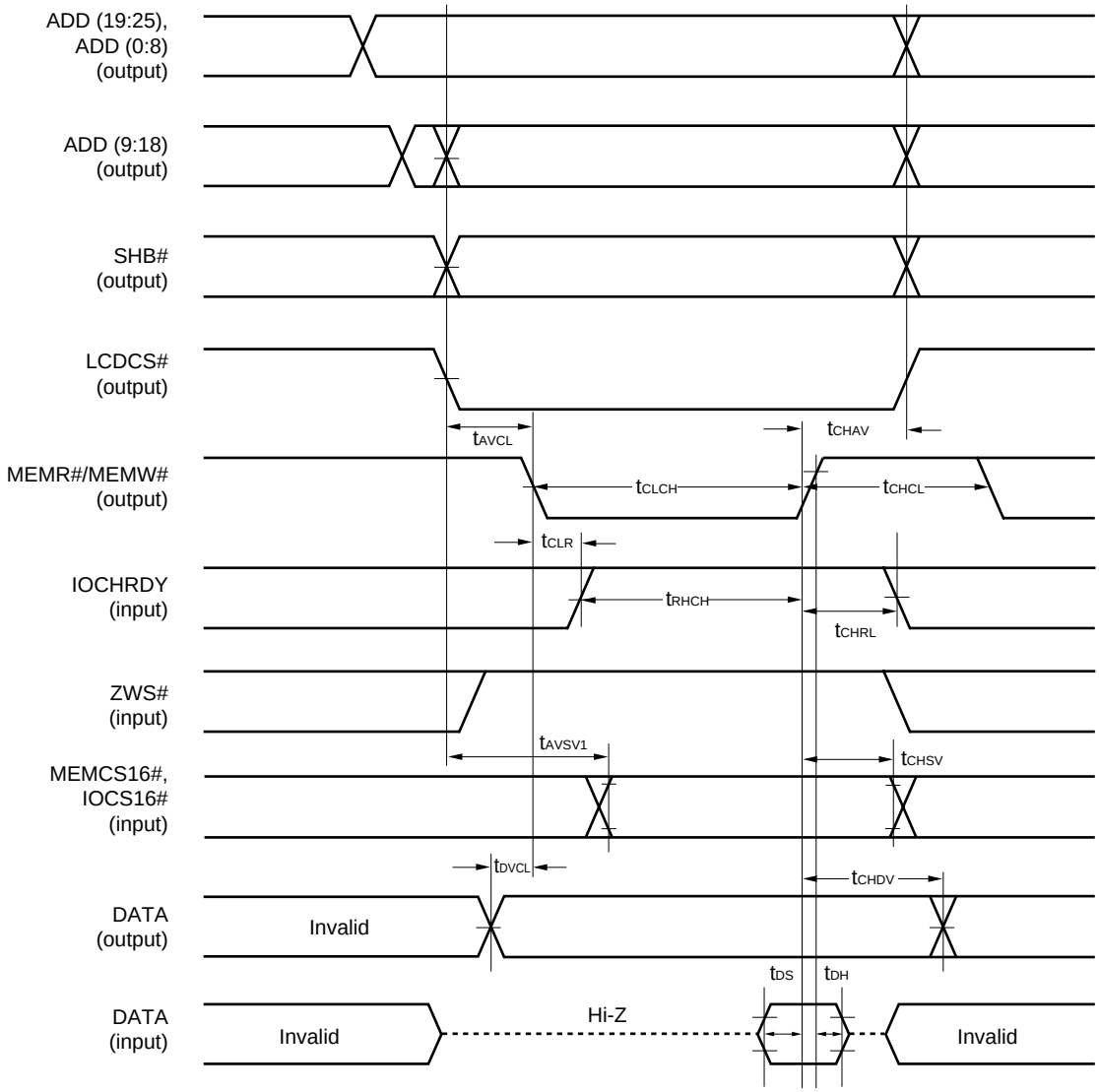
CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1Note	1Note	1Note	RFU
1Note	1Note	0Note	RFU
1Note	0Note	1Note	RFU
1Note	0Note	0Note	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

WLCD/M2	WLCD/M1	WLCD/M0	N (TClock)	M (TClock)
0	0	0	8	8
0	0	1	7	7
0	1	0	6	6
0	1	1	5	5
1	0	0	4	4
1	0	1	3	3
1	1	0	2	2
1	1	1	1	2

Note Do not set CLKSEL2 to 1.

(14) High-speed system bus parameter (IOCHRDY) (2/2)

When WISAA (2:0) = 111



Remark The broken lines indicate high impedance.

(15) High-speed system bus parameter (ZWS#) (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)Notes 1, 2	t_{AVCL}		T × N – 29		ns
Command signal low-level widthNotes 1, 2	t_{CLCH}		T × N – 31		ns
Address hold time (from command signal ↑)Note 1	t_{CHAV}		25		ns
Command signal recovery timeNotes 1, 2	t_{CHCL}		T × (N + 1) – 29		ns
ZWS# ↓ delay time from command signal ↓Notes 1, 2	t_{CLZL}			T × (N – 1) – 20	ns
ZWS# signal hold time (from command signal ↑)Note 1	t_{CHZH}		0		ns
Data output setup time (to command signal ↓)Note 1	t_{DVCL}		–15		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}		25		ns
MEMCS16#/IOCS16# sampling start timeNote 2	t_{AVSV2}		2 × T × (N – 1) – 44		ns
MEMCS16#/IOCS16# hold time (from command signal ↑)Note 1	t_{CHSV}		0		ns
Data input setup time	t_{DS}		0		ns
Data input hold time	t_{DH}		15		ns

Notes 1. With the VR4111, the MEMW# and MEMR# signals are called the command signals for the high-speed system bus interface.

2. The value of N is set by using the WISAA (0:2) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

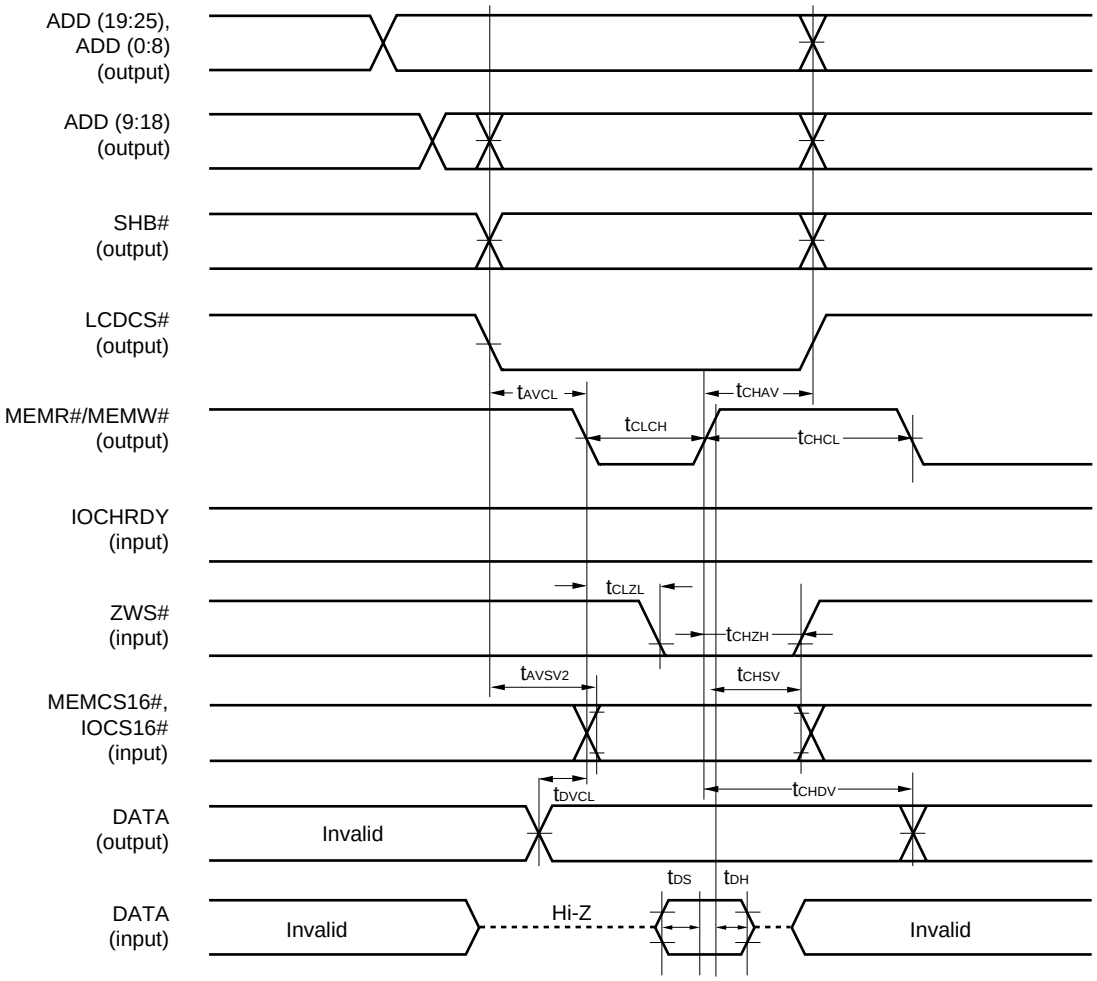
CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1Note	1Note	1Note	RFU
1Note	1Note	0Note	RFU
1Note	0Note	1Note	RFU
1Note	0Note	0Note	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

WISAA2	WISAA1	WISAA0	N (TClock)
0	0	0	8
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	2
1	1	1	1

Note Do not set CLKSEL2 to 1.

(15) High-speed system bus parameter (ZWS#) (2/2)

When WISAA (0:2) = 111



Remark The broken lines indicate high impedance.

(16) LCD interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address setup time (to command signal ↓)Note 1	t_{AS}		15		ns
Address hold time (from command signal ↑)Note 1	t_{AH}		0		ns
Command signal recovery timeNote 1	t_{RY}		30		ns
LCDRDY sampling start time	t_{CLR}		0		ns
Command signal delay time from LCDRDY ↑Notes 1, 2	t_{RHCH}		T × N	T × (N + 2) + 29	ns
LCDRDY hold time (from command signal ↑)Note 1	t_{RYZ}		0		ns
Data output setup time (to command signal ↑)Notes 1, 2	t_{DVCH}		T × (N + 2)		ns
Data output hold time (from command signal ↑)Note 1	t_{CHDV}		25		ns
Data input setup time (to command signal ↑)Note 1	t_{DS}		0		ns
Data input hold time (from command signal ↑)Note 1	t_{DH}		15		ns

Notes 1. With the VR4111, the RD# and WR# signals are called the command signals for the LCD interface.

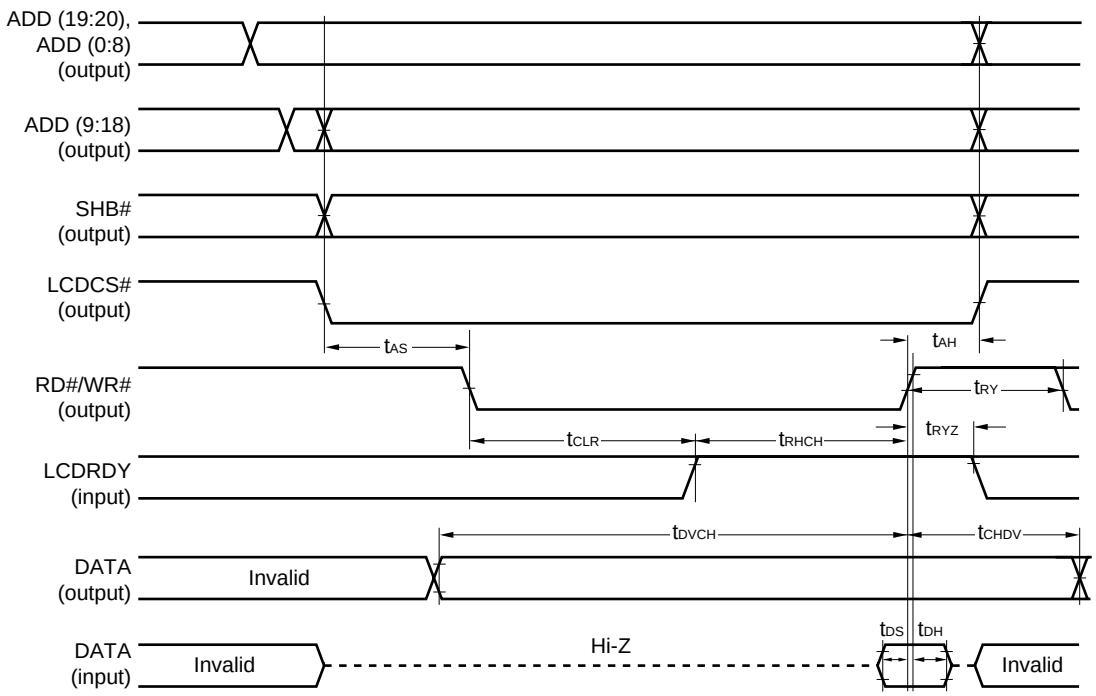
2. The values of N is set by using the WLCD/M (0:1) bits of the BCUSPEEDREG register.
The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1Note	1Note	1Note	RFU
1Note	1Note	0Note	RFU
1Note	0Note	1Note	RFU
1Note	0Note	0Note	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

WLCD/M1	WLCD/M0	N (TClock)
0	0	8
0	1	6
1	0	4
1	1	2

Note Do not set CLKSEL2 to 1.

(16) LCD interface parameter (2/2)



Remark The broken lines indicate high impedance.

(17) Bus hold parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
HLDRQ# input pulse width[Note]	t_{FHP}	In Full-speed/standby mode	5T		ns
Data floating delay time	t_{FOFF}	In Full-speed/standby mode	0		ns
Data valid delay time	t_{FON}	In Full-speed/standby mode	0		ns
HLDRQ# input pulse width[Note]	t_{SHP}	In Suspend mode	12T		ns
Data floating delay time	t_{SOFF}	In Suspend mode	0		ns
Data valid delay time	t_{SON}	In Suspend mode	0		ns
MRAS (0:3)# precharge time	t_{RPS}	In Suspend mode	110		ns
UCAS#/LCAS# setup time	t_{CSR}	In Suspend mode	5		ns

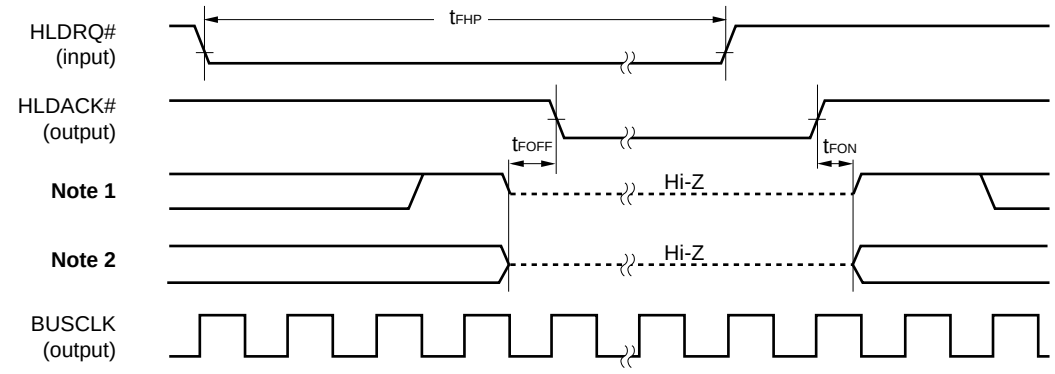
Note The value of T is set by using the CLKSEL (0:2) bits (TxD/CLKSEL2, RTS#/CLKSEL1, and DTR#/CLKSEL0).

CLKSEL2	CLKSEL1	CLKSEL0	T (ns)
1[Note]	1[Note]	1[Note]	RFU
1[Note]	1[Note]	0[Note]	RFU
1[Note]	0[Note]	1[Note]	RFU
1[Note]	0[Note]	0[Note]	RFU
0	1	1	43.3
0	1	0	45.9
0	0	1	48.4
0	0	0	40.7

Note Do not set CLKSEL2 to 1.

(17) Bus hold parameter (2/2)

(a) Bus hold in Fullspeed/Standby mode

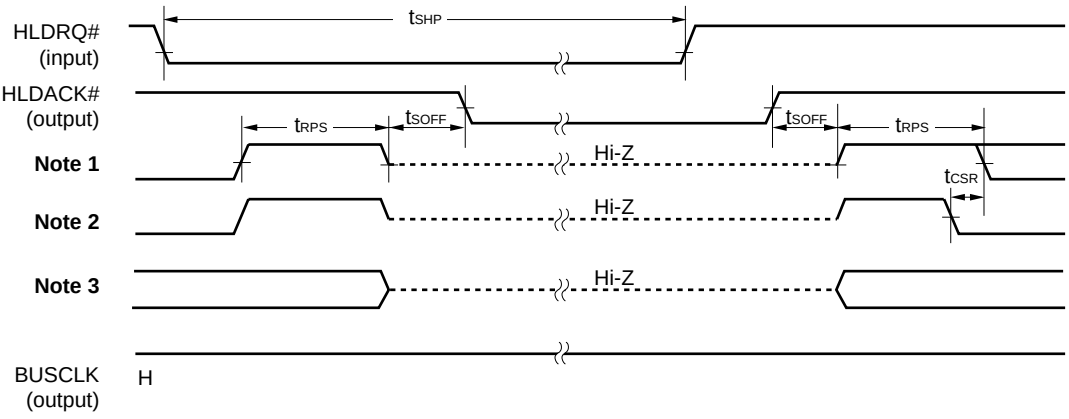


Notes 1. UUCAS#/MRAS3#, ULCAS#/MRAS#2, MRAS (0:1)#, UCAS#, LCAS#

2. SHB#, IOR#, IOW#, MEMR#, MEMW#, RD#, WR#, ADD (0:25), DATA (0:15), DATA (16:31)/GPIO (16:31) (In 32-bit data bus mode)

Remark The broken lines indicate high impedance.

(b) Bus hold in Suspend mode



Notes 1. In 32-bit mode: MRAS (0:1)#
In 16-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, MRAS (0:1)#

2. In 32-bit mode: UUCAS#/MRAS3#, ULCAS#/MRAS2#, UCAS#, LCAS#
In 16-bit mode: UCAS#, LCAS#

3. SHB#, IOR#, IOW#, MEMR#, MEMW#, RD#, WR#, ADD (0:25), DATA (0:15), DATA (16:31)/GPIO (16:31) (In 32-bit data bus mode)

Remark The broken lines indicate high impedance.

(18) Keyboard Interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
KSCAN (0:11) high-level width	t_{SCAN}		30 (K + 2) – 1	30.16 (K + 2) + 1	μs
Idle time (KSCAN (n+1) ↑ from KSCANn ↓)	t_{KWAIT}		30 (L + 1) – 1	30.16 (L + 1) + 1	μs
Key scan interval time	t_{KI}		30M – 1	30.16M + 1	μs
Key input setup time (to KSCANn ↑)	t_{KS}		30 (N + 1) – 1		μs
Key input hold time (from KSCANn ↑)	t_{KH}		0		μs

Notes 1. K: Sum of the values set to the T1CNT (0:4) bits and T2CNT (0:4) bits of the KIUWKS register

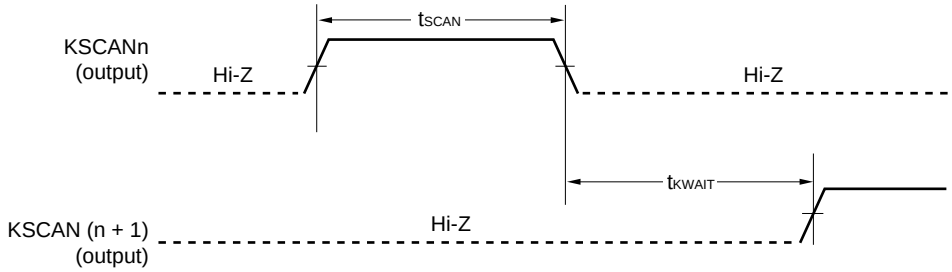
2. L: Value set to the T3CNT (0:4) bits of the KIUWKS register

3. M: Value set to KIUWKI register

4. N: Value set to the T1CNT (0:4) bits of the KIUWKS register

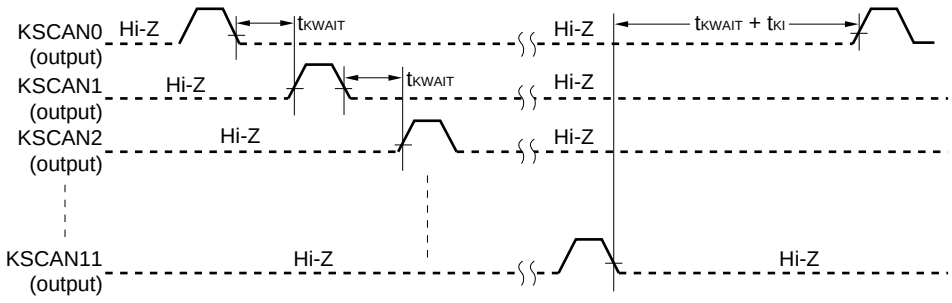
5. n = 0 to 11

(a) Keyboard scan parameter 1



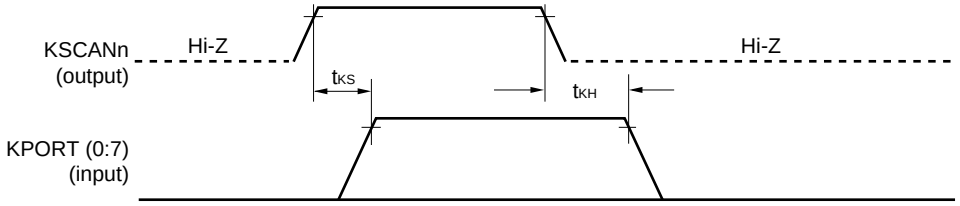
Remark n = 0 to 10

(b) Keyboard scan parameter 2



(18) Keyboard Interface parameter (2/2)

(c) Keyboard port parameter



Remark n = 0 to 11

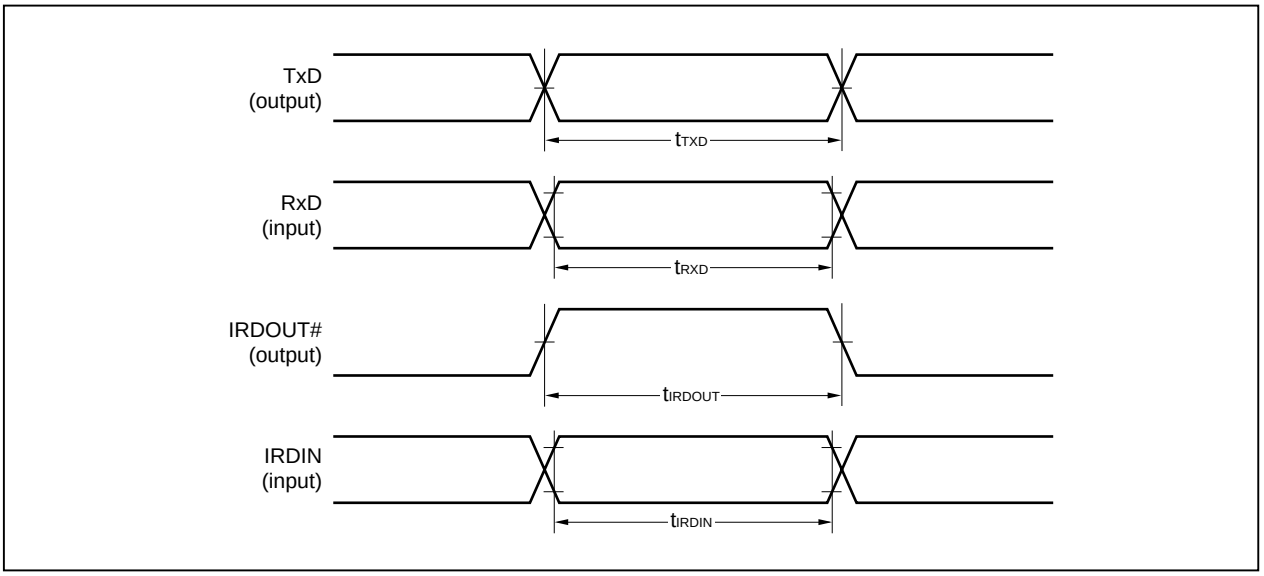
(19) Serial interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
TxD output pulse width[Note]	t_{TXD}		N – 1	N + 1	μs
RxD input pulse width[Note]	t_{RXD}		(9/16) × N		μs
IRDOUT# high-level output pulse width[Note]	t_{IRDOUT}		(3/16) × N – 1	(3/16) × N + 1	μs
IRDIN input pulse width	t_{IRDIN}		1		μs

Note N: Data transfer rate per bit, which is determined by the divisor of the baud-rate generator that is set with the SIUDLL and SIUDLM registers.

Baud Rate (bps)	SIUDLM, SIUDLL	N (μs)
50	23,040	20,000
75	15,360	13,333
110	10,473	9,091
134.5	8,565	7,435
150	7,680	6,667
300	3,840	3,333
600	1,920	1,667
1,200	920	833
1,800	640	556
2,000	573	500
2,400	480	417
3,600	320	278
4,800	240	208
7,200	160	139
9,600	120	104
19,200	60	52.1
38,400	30	26.0
56,000	21	17.9
128,000	9	7.81
144,000	8	6.94
192,000	6	5.21
230,400	5	4.34
288,000	4	3.47
384,000	3	2.60
576,000	2	1.74
1,152,000	1	0.868

(19) Serial interface parameter (2/2)

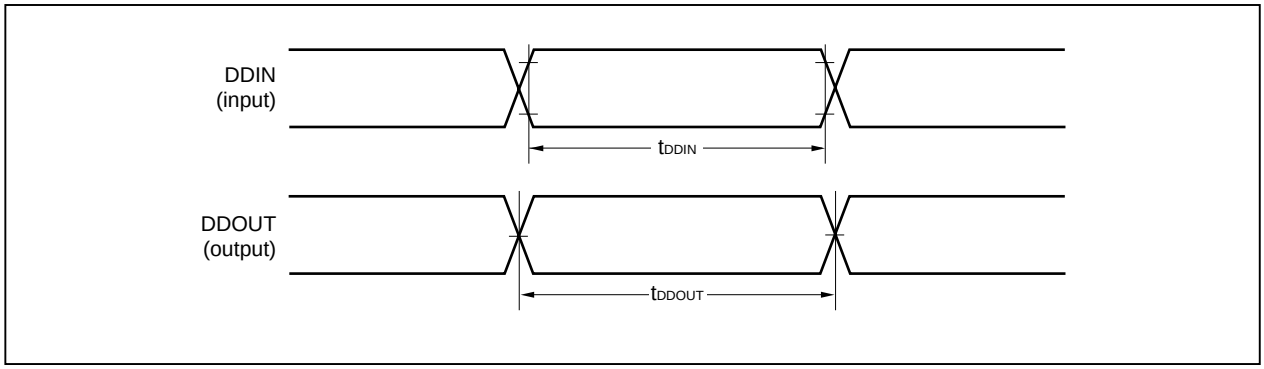


(20) Debug serial interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
DDOUT output pulse width[Note]	t_{DDOUT}		N – 1	N + 1	μs
DDIN input pulse width[Note]	t_{DDIN}		(9/16) × N		μs

Note N: Transfer rate of baud rate per bit set to the BPR0 bits of the BPRM0REG register.

BPR0 (2:0)	Baud Rate (bps)	N (μs)
111	115,200	8.68
110	57,600	17.36
101	38,400	26.04
100	19,200	52.03
011	9,600	104.16
010	4,800	208.33
001	2,400	416.66
000	1,200	833.33



(21) HSP interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SDO output delay time[Note 1]	t_{SDOD}			15	ns
SDI setup time[Note 2]	t_{SDIS}		25		ns
SDI hold time[Note 2]	t_{SDIH}		0		ns
FS setup time[Note 2]	t_{FSIS}		20		ns
FS hold time[Note 2]	t_{FSIH}		0		ns

Notes 1. The reference clock of this parameter is the rising edge of HSPSCLK.

2. The reference clock of this parameter is the falling edge of HSPSCLK.

A/D Converter Characteristics (T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Resolution			10		bit
Zero-scale error Notes 1, 2	ZSE		0	±4.0	LSB
Full-scale error Notes 1, 2	RSE		0	±5.0	LSB
Integral linearity error Notes 1, 2	INL		0	±3.0	LSB
Differential linearity error Notes 1, 2	DNL		0	±3.0	LSB
Analog input voltage Notes 1, 3	VIAN		–0.3	AV_{DD} + 0.3	V

Notes 1. Applied to TPX (0:1), TPY (0:1), ADIN (0:2), and AUDIOIN pins.

2. Quantization error is excluded.

3. AV_{DD} is a voltage on the AV_{DD} pin that is V_{DD} dedicated to the A/D converter.

D/A Converter Characteristics (T_A = –10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Resolution			10		bit
Integral linearity error Notes 1, 2	INL		0	±3.0	LSB
Differential linearity error Notes 1, 2	DNL		0	±3.0	LSB

Notes 1. Applied to AUDIOOUT pin.

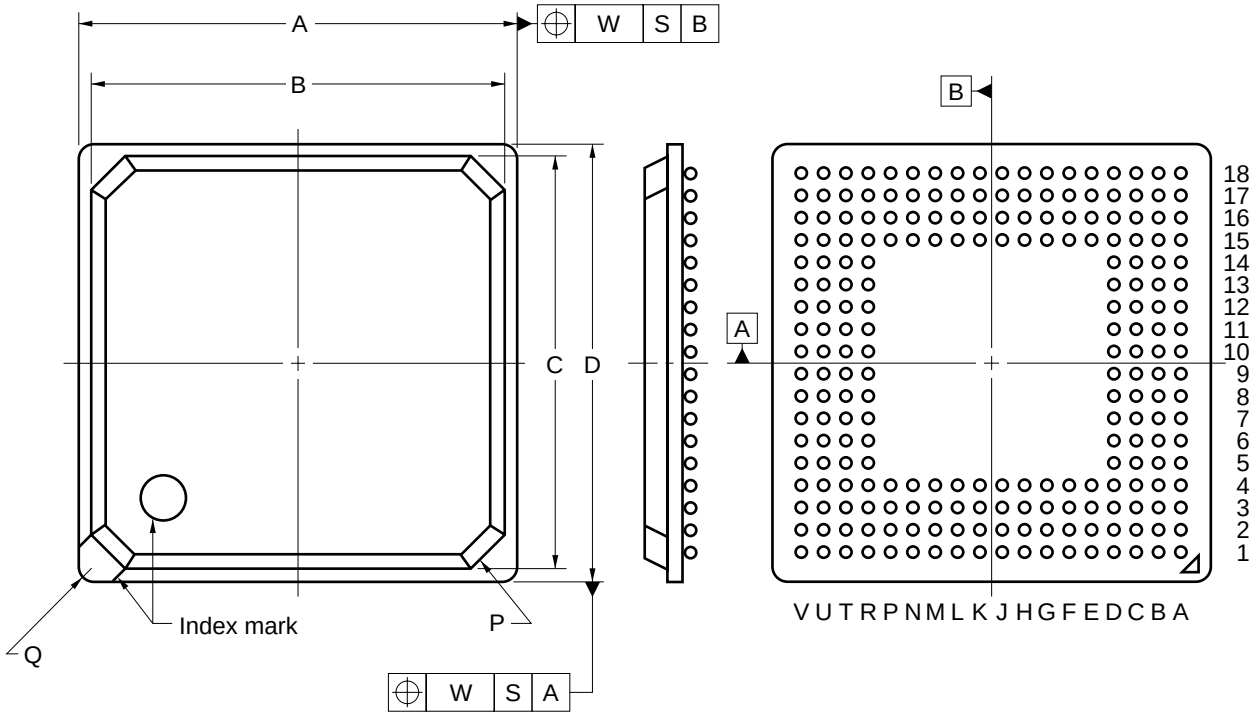
2. Quantization error is excluded.

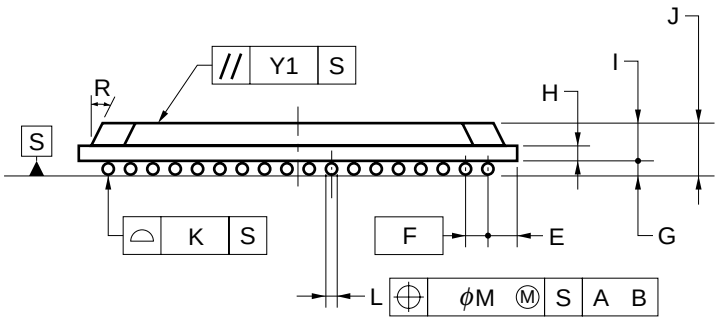
Load Coefficient (Delay Time per Load Capacitance)

Parameter	Symbol	Condition	Rating		Unit
			MIN.	MAX.	
Load coefficient	CLD			5	ns/20 pF

24. PACKAGE DRAWING

224-PIN FINE PITCH BGA (16x16)





ITEM	MILLIMETERS	INCHES
A	16.00±0.10	0.630±0.004
B	15.4	0.606
C	15.4	0.606
D	16.00±0.10	0.630±0.004
E	1.20	0.047
F	0.8 (T.P.)	0.031
G	0.35±0.1	$0.014^{+0.004}_{-0.005}$
H	0.36	0.014
I	0.96	0.038
J	1.31±0.15	$0.052^{+0.006}_{-0.007}$
K	0.10	0.004
L	$\phi 0.50^{+0.05}_{-0.10}$	$\phi 0.020^{+0.002}_{-0.005}$
M	0.08	0.003
P	C1.0	C0.039
Q	R0.3	R0.012
R	25°	25°
W	0.20	0.008
Y1	0.20	0.008

S224S1-3C-1

NOTES

1. Controlling dimension — millimeter.

2. Each ball centerline is located within ϕ0.08 mm of its true position (T.P.) at maximum material condition.

25. RECOMMENDED SOLERING CONDITIONS

The μPD30111 should be soldered and mounted under the following recommended conditions.

For details of recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact your NEC sales representative.

Table 25-1. Surface Mounting Type Soldering Conditions

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: 2 times max., Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours.)	IR30-103-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: 3 times max. , Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours.)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX DIFFERENCES BETWEEN VR4111 AND VR4102

Item		VR4111	VR4102
Cache memory	Size	Instruction: 16 Kbytes, data: 8 Kbytes	Instruction: 4 Kbytes, data: 1 Kbyte
	Parity check	None	Provided
Instruction set		MIPS III + high-speed sum-of-products operation + MIPS16	MIPS III + high-speed sum-of-products operation
LCD interface bus width		16 bits, 32 bits	16 bits
Memory controller	Maximum DRAM capacity (EDO type)	64 Mbytes	32 Mbytes
	Maximum ROM capacity	64 Mbytes	32 Mbytes
Power-on factor		4 types, 12 sources	4 types, 8 sources
Pull-up/pull-down of GPIO (0:14) pins		Internal. Can be independently set by means of software.	External processing
Modem interface		Transmit/receive FIFO: 96 bytes	Transmit/receive FIFO: 32 bytes
★ Internal maximum operating frequency		70 MHz	49 MHz
Supply voltage		Internal: 2.5 V External: 3.3 V	3.3 V
Package		224-pin FBGA	216-pin LQFP 224-pin FBGA

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Related documents VR4111 User's Manual (U13137E)
VR4102 User's Manual (U12739E)
μPD30102 (VR4102) Data Sheet (U12543E)

Reference document Electrical Characteristics for Microcomputer (IEI-601)[Note]

Note This document number is that of the Japanese version.

The documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

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