NEC

MOS INTEGRATED CIRCUIT

μPD30181

VR4181™
64-/32-BIT MICROPROCESSOR

DESCRIPTION

The μPD30181 (VR4181), which is a high-performance 64-/32-bit microprocessor employing the RISC (reduced instruction set computer) architecture developed by MIPS™, is one of the microprocessor VR-Series™ products manufactured by NEC.

The VR4181 consists of the ultra-low-power consumption VR4110™ CPU core with cache memory, high-speed product-sum operation unit, and address management unit. It also has interface units for peripheral circuits such as an LCD controller, CompactFlash controller, DMA, keyboard interface, serial interface, IrDA interface, touch panel interface, real-time clock, A/D converter and D/A converter required for the battery-driven portable information equipment.

The functions of the VR4181 are explained in detail in the following manual. Be sure to refer to this manual when designing your system.

VR4181 User's Manual Hardware (U14272E)
VR4100 Series™ User's Manual Architecture (U15509E)

FEATURES

- 64-bit RISC VR4110 CPU Core
- Pipeline clock up to 66 MHz
- Optimized 5-stage pipeline
- MIPS III instruction set (with the FPU, LL and SC instruction left out) and MIPS 16 instruction set supported
- MADD16 and DMADD16 instructions for executing a multiply-and-accumulate operation
  operation of 16-bit data × 16-bit data + 64-bit data within one clock cycle
- 4-KB instruction and 4-KB data cache
- Write-back cache for reducing store operations which use the system bus
- 32-bit physical and 40-bit virtual address space, and 32-double-entry TLB
- Effective power management features, which include the four operating modes; Fullspeed, Standby, Suspend and Hibernate modes
- PLL and clock generator
- DRAM interface supporting 16-bit width SDRAM and EDO DRAM
- ROM interface
- UMA based LCD controller
- DMA controller, Timer, Counter, and RTC unit
- UART-compatible serial interface (2 ch), and clocked serial interface
- IrDA (SIR) interface
- 8 × 8 keyboard scan interface and X-Y auto-scan touch panel interface
- CompactFlash interface
- A/D and D/A converters
- Supports subset of ISA bus
- Supply voltage: 2.5 V for core, 3.3 V for I/O
- Package: 160-pin plastic LQFP (fine pitch)

APPLICATIONS

- Palm-size PC
- Battery-driven portable information systems
- Embedded controllers, etc.

ORDERING INFORMATION

Part Number	Package	Internal Maximum Operating Frequency
μPD30181GM-66-8ED	160-pin plastic LQFP (fine pitch) (24 × 24)	66 MHz

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

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The mark ★ shows major revised points.

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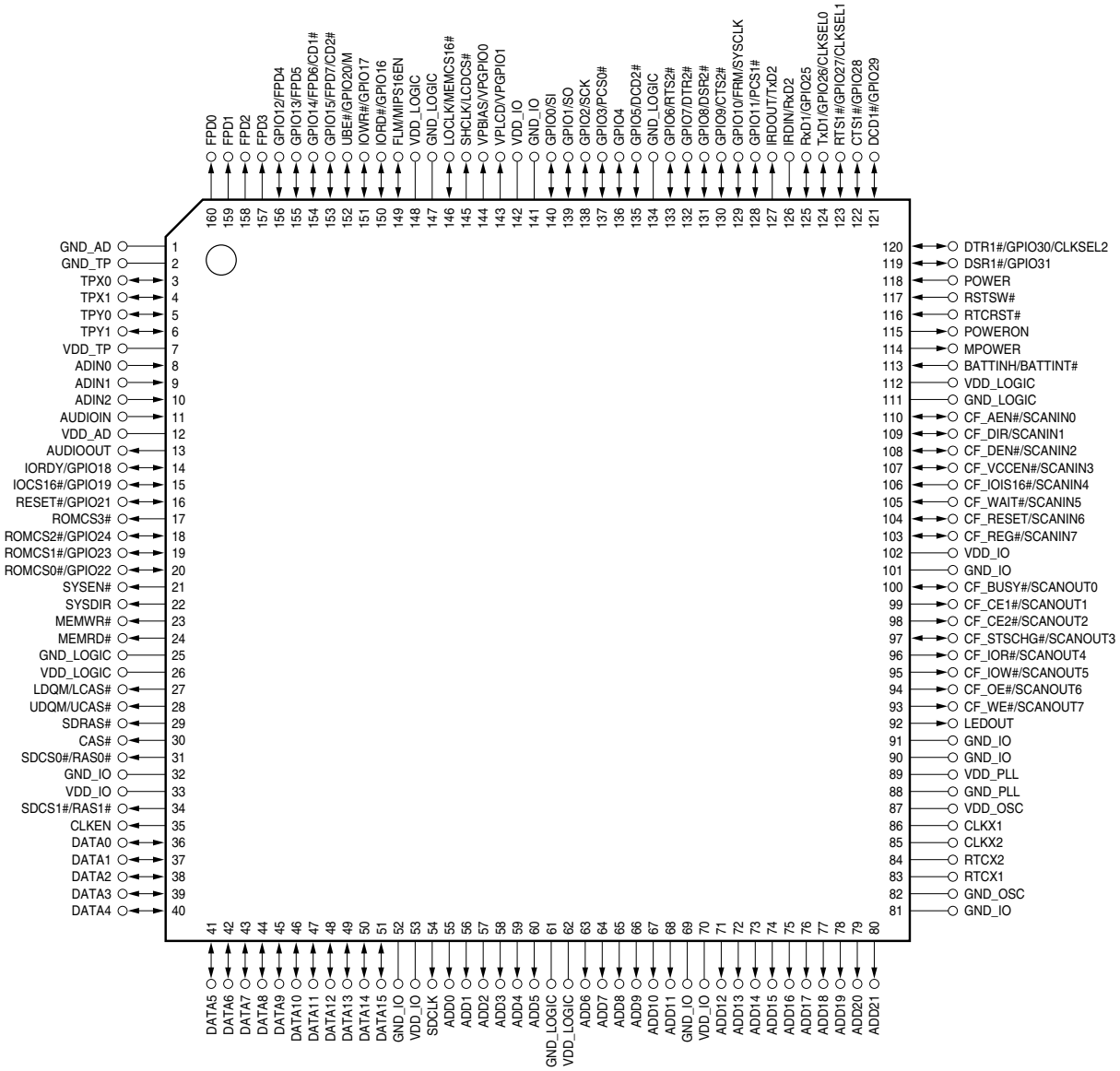
PIN CONFIGURATION

- 160-pin plastic LQFP (fine pitch) (24 × 24)



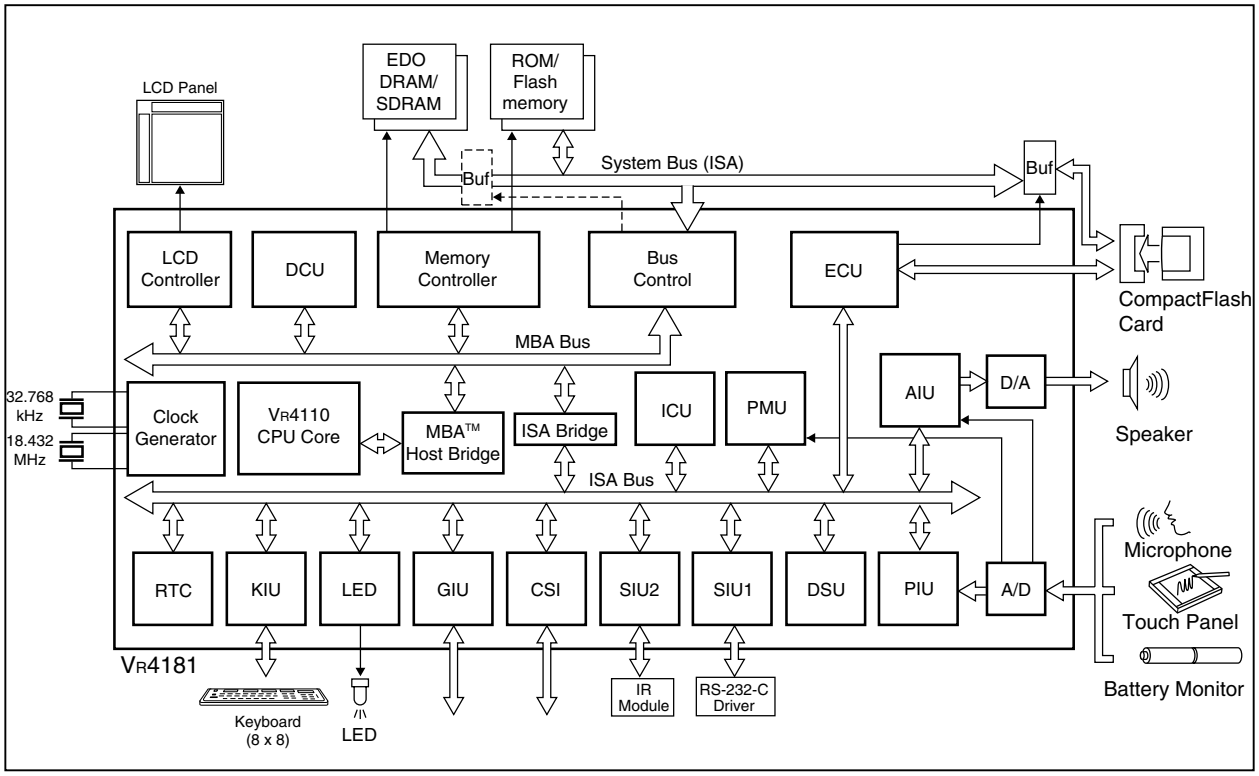
Remark # indicates active low.

Pin Identification

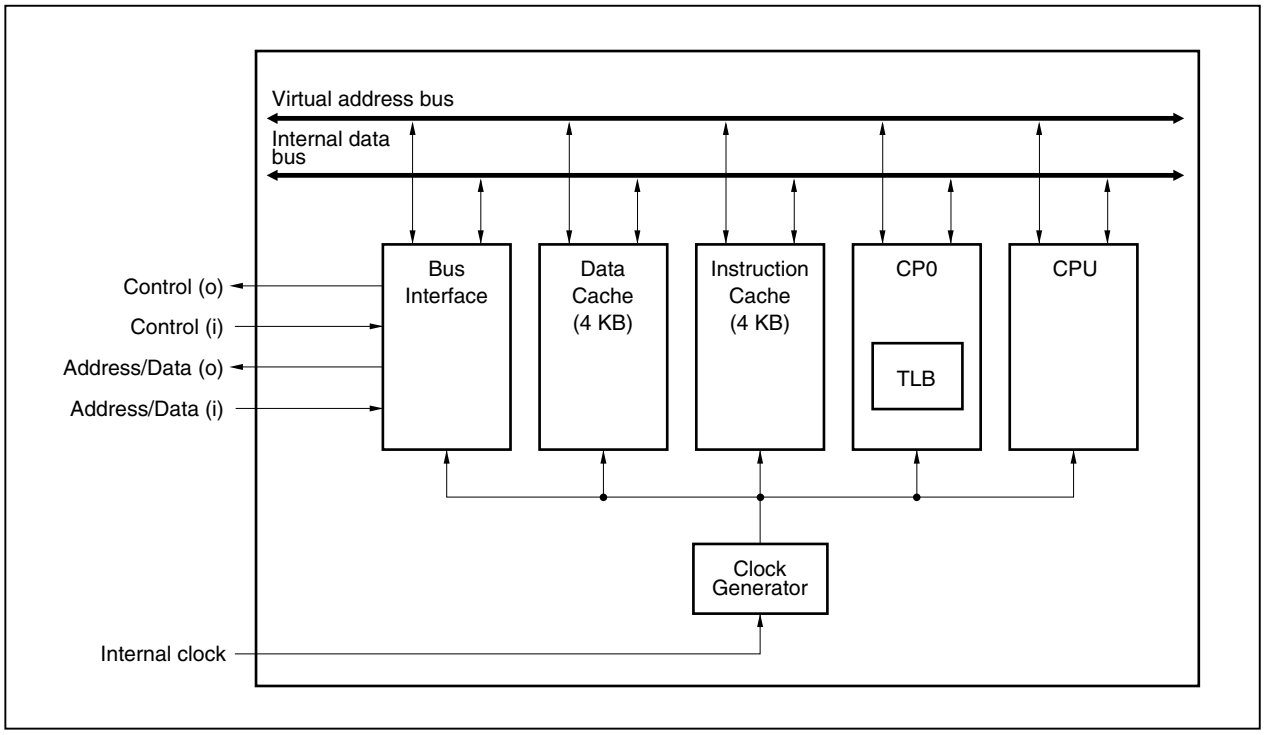
ADD(21:0) : Address Bus
ADIN(2:0) : Analog Data Input
AUDIOIN : Audio Input
AUDIOOUT : Audio Output
BATTINH : Battery Inhibit
BATTINT# : Battery Interrupt
CAS# : Column Address Strobe
CD1#, CD2# : Card Detect for CompactFlash
CF_AEN# : Address Enable for CompactFlash Buffer
CF_BUSY# : Ready/Busy/Interrupt Request for CompactFlash
CF_CE(2:1)# : Card Enable for CompactFlash
CF_DEN# : Data Enable for CompactFlash Buffer
CF_DIR : Data Direction for CompactFlash Buffer
CF_IOIS16# : I/O is 16 bits for CompactFlash
CF_IOR# : I/O Read Strobe for CompactFlash
CF_IOW# : I/O Write Strobe for CompactFlash
CF_OE# : Output Enable for CompactFlash
CF_REG# : Register Memory Access for CompactFlash
CF_RESET : Reset for CompactFlash
CF_STSCHG# : Status Change of CompactFlash
CF_VCCEN# : V_{CC} Enable for CompactFlash
CF_WAIT# : Wait Input for CompactFlash
CF_WE# : Write Enable for CompactFlash
CLKEN : Clock Enable for SDRAM
CLKSEL(2:0) : Clock Select
CLKX1, CLKX2 : Clock Input
CTS1#, CTS2# : Clear to Send
DATA(15:0) : Data Bus
DCD1#, DCD2# : Data Carrier Detect
DSR1#, DSR2# : Data Set Ready
DTR1#, DTR2# : Data Terminal Ready
FLM : First Line Clock for LCD
FPD(7:0) : Screen Data of LCD
FRM : Clocked Serial Frame
GND_AD : Ground for A/D and D/A Converter
GND_IO : Ground for I/O
GND_LOGIC : Ground for Logic
GND_OSC : Ground for Oscillator
GND_PLL : Ground for PLL
GND_TP : Ground for Touch Panel
GPIO(31:0) : General Purpose I/O
IOCS16# : I/O 16-bit Bus Sizing
IORD# : I/O Read
IORDY : I/O Ready
IOWR# : I/O Write
IRDIN : IrDA Data Input
IRDOUT : IrDA Data Output
LCAS# : Lower Column Address Strobe
LCDCS# : Chip Select for LCD
LDQM : Lower Byte Enable for SDRAM
LEDOUT : LED Output
LOCLK : Load Clock for LCD
M : LCD Modulation Clock
MEMCS16# : Memory 16-bit Bus Sizing
MEMRD# : Memory Read
MEMWR# : Memory Write
MIPS16EN : MIPS16 Enable
MPOWER : Main Power
PCS(1:0)# : Programmable Chip Select
POWER : Power Switch
POWERON : Power On State
RAS(1:0)# : Row Address Strobe for DRAM
RESET# : Reset Output
ROMCS(3:0)# : Chip Select for ROM
RSTSW# : Reset Switch
RTCRST# : Real-time Clock Reset
RTCX1, RTCX2 : Real-time Clock Input
RTS1#, RTS2# : Request to Send
RxD1,RxD2 : Receive Data
SCANIN(7:0) : Scan Data Input
SCANOUT(7:0) : Scan Data Output
SCK : CSI (Clocked Serial Interface) Clock
SDCLK : Operation Clock for SDRAM
SDCS(1:0)# : Chip Select for SDRAM
SDRAS# : Row Address Strobe for SDRAM
SHCLK : Shift Clock for LCD
SI : Clocked Serial Data Input
SO : Clocked Serial Data Output
SYSCLK : System Clock for System Bus
SYSDIR : System Data Direction
SYSEN# : System Data Enable
TPX(1:0) : Touch Panel Data of X
TPY(1:0) : Touch Panel Data of Y
TxD1, TxD2 : Transmit Data
UBE# : Upper Byte Enable for System Bus
UCAS# : Upper Column Address Strobe for DRAM
UDQM : Upper Byte Enable for SDRAM
VDD_AD : Power Supply for A/D and D/A Converter
VDD_IO : Power Supply for I/O
VDD_LOGIC : Power Supply for Logic
VDD_OSC : Power Supply for Oscillator
VDD_PLL : Power Supply for PLL
VDD_TP : Power Supply for Touch Panel
VPBIAS : Bias Power Control for LCD
VPGPIO(1:0) : General Purpose Output for LCD Panel Power Control
VPLCD : Logic Power Control for LCD

Remark # indicates active low.

★ INTERNAL BLOCK DIAGRAM AND EXAMPLE OF CONNECTION OF EXTERNAL BLOCKS



CPU CORE INTERNAL BLOCK DIAGRAM



CONTENTS

1. PIN FUNCTIONS

Remark # indicates active low.

1.1 Pin Functions

(1) System bus interface signals

(1/2)

Signal name	I/O	Description of function
ADD(21:0)[Note]	O	System address bus. Used to specify address for the DRAM, ROM, flash memory, or system bus (ISA).
DATA(15:0)	I/O	System data bus. Used to transmit and receive data between the VR4181 and DRAM, ROM, flash memory, or system bus.
IORD# / GPIO16	I/O	System bus I/O read signal output or general-purpose I/O. It is active when the VR4181 accesses the system bus to read data from an I/O port when configured as IORD#.
IOWR# / GPIO17	I/O	System bus I/O write signal output or general-purpose I/O. It is active when the VR4181 accesses the system bus to write data to an I/O port when configured as IOWR#.
IORDY / GPIO18	I/O	System bus I/O channel ready input or general-purpose I/O. Set this signal as active when system bus controller is ready to be accessed by the VR4181 when configured as IORDY.
IOCS16# / GPIO19	I/O	Bus sizing request input for system bus I/O or general-purpose I/O. Set this signal as active when system bus I/O accesses data in 16-bit width, if configured as IOCS16#.
UBE# / GPIO20/M	I/O	System bus upper byte enable output, general-purpose input, or LCD modulation output. During system bus accesses, this signal is active when the high-order byte is valid on the data bus.
RESET# / GPIO21	I/O	System bus reset output or general-purpose I/O. It is active when the VR4181 resets the system bus controller when configured as RESET#.

Note The VR4181 utilizes different addressings depending on the types of the external accesses.
During ROM accesses, bits 22 to 1 of the internal address lines are output to the ADD(21:0) pins (the minimum transfer data width is a half word (1 word = 32 bits)).
During accesses other than ROM accesses, bits 21 to 0 of the internal address lines are output to the ADD(21:0) pins (the minimum transfer data width is 1 byte).

(2/2)

Signal name	I/O	Description of function
★ SYSDIR[Note]	O	System data buffer direction control. This signal is valid only when ROM, ISA or CompactFlash accesses are enabled. This becomes low level during ROM, ISA or CompactFlash read cycle, or becomes high level during ROM, ISA or CompactFlash write cycle.
★ SYSEN#[Note]	O	System data buffer enable. This signal is valid only when ROM, ISA or CompactFlash accesses are enabled. This becomes active during ROM or ISA cycle.
SDCS(1:0)# / RAS(1:0)#	O	SDRAM chip select for bank 0 and bank 1 or EDO DRAM row address strobes.
CAS#	O	SDRAM column address strobe. Leave unconnected when using EDO DRAM.
SDRAS#	O	SDRAM row address strobe. Leave unconnected when using EDO DRAM.
UDQM / UCAS#	O	SDRAM upper byte enable or EDO DRAM upper byte column address strobe.
LDQM / LCAS#	O	SDRAM lower byte enable or EDO DRAM lower byte column address strobe.
SDCLK	O	SDRAM operating clock.
CLKEN	O	SDRAM clock enable output.
ROMCS3#	O	ROM chip select output for bank 3.
ROMCS2# / GPIO24	I/O	ROM chip select output for bank 2, or general-purpose I/O.
ROMCS1# / GPIO23	I/O	ROM chip select output for bank 1, or general-purpose I/O.
ROMCS0# / GPIO22	I/O	ROM chip select output for bank 0, or general-purpose I/O.
MEMRD#	O	Memory read signal for ROM and system bus.
MEMWR#	O	Memory write signal for ROM, DRAM and system bus.

Note The SYSEN# and SYSDIR signals control a buffer which is used to isolate SDRAM data bus from the bus of other low speed devices. By isolating the high-speed data bus of SDRAM, the load of the data bus ★ between the VR4181 and SDRAM is reduced. When the EXBUFFEN bit of the XISACTL register is cleared to 0, the SYSEN# and SYSDIR signals start their operation. These signals keep low level until EXBUFFEN bit is cleared to 0 after a reset. When an isolation buffer is used, SYSEN# and SYSDIR signals function as follows;

SYSEN#	SYSDIR	Bus operation
0	0	External ISA, CompactFlash, or ROM read cycle
0	1	External ISA, CompactFlash, or Flash Memory mode write cycle
1	Don't care	External Buffer Disable DRAM read/write cycle or Hibernate mode

(2) LCD interface signals

Signal name	I/O	Description of function
SHCLK / LCDCS#	O	LCD shift clock output or chip select for external LCD controller.
LOCLK / MEMCS16#	I/O	LCD load clock output or bus sizing request input for system bus memory access in 16-bit width.
FLM / MIPS16EN	I/O	This function differs depending on the operating status. <During RTC reset (input)> This signal enables use of MIPS16 instructions. 0: Disable use of MIPS16 instructions 1: Enable use of MIPS16 instructions <During normal operation (output)> LCD first line clock output.
FPD(7:4)[Note]	O	See **(11) General-purpose I/O signals** in this section.
FPD(3:0)[Note]	O	LCD screen data.
VPLCD / VPGPIO1	O	LCD logic power control. This signal may be defined as a general-purpose output when an external LCD controller is used.
VPBIAS / VPGPIO0	O	LCD bias power control. This signal may be defined as a general-purpose output when an external LCD controller is used.

Note Connection between FPD(7:0) of the VR4181 and LCD panel data lines differs depending on the panel data width as below.
For details, refer to VR4181 User's Manual.

VR4181	LCD Panel Data (4-bit width)	LCD Panel Data (8-bit width)
FPD0	Data Line 0	Data Line 4
FPD1	Data Line 1	Data Line 5
FPD2	Data Line 2	Data Line 6
FPD3	Data Line 3	Data Line 7
FPD4	–	Data Line 0
FPD5	–	Data Line 1
FPD6	–	Data Line 2
FPD7	–	Data Line 3

(3) Initialization interface signals

Signal name	I/O	Description of function
POWER	I	VR4181 activation signal.
RSTSW#	I	VR4181 reset signal.
RTCRST#	I	Reset signal for internal Real-time clock and all internal logic. When power is first supplied to the system, the external agent must activate this signal.
POWERON	O	This signal indicates that the VR4181 is ready to operate. It becomes active when a power-on factor is detected and becomes inactive when the BATTINH/BATTINT# signal check has been completed.
MPOWER	O	This signal indicates that the VR4181 is operating. This signal is inactive during Hibernate mode. During this signal being inactive, turn off the 2.5 V power supply.

(4) Battery monitor interface signals

Signal name	I/O	Description of function
BATTINH / BATTINT#	I	This function differs depending on the state of the MPOWER pin. <When MPOWER = 0> BATTINH function Enables or disables activation on power application. 1: Enable activation 0: Disable activation <When MPOWER = 1> BATTINT# function This is an interrupt signal that is output when remaining battery power is low during normal operations. The external agent checks the remaining battery power and activate this signal if voltage sufficient for operations cannot be supplied.

(5) Clock interface signals

Signal name	I/O	Description of function
RTCX(2:1)	–	Real-time clock (32.768 kHz) connections to crystal resonator.
CLKX(2:1)	–	Processor clock (18.432 MHz) connections to crystal resonator.

(6) Touch panel interface and audio interface signals

Signal name	I/O	Description of function
TPX(1:0)	I/O	Touch panel X coordinate data. They use the voltage applied to the X coordinate and the voltage input to the Y coordinate to detect which coordinates on the touch panel are being pressed.
TPY(1:0)	I/O	Touch panel Y coordinate data. They use the voltage applied to the Y coordinate and the voltage input to the X coordinate to detect which coordinates on the touch panel are being pressed.
ADIN(2:0)	I	General-purpose analog data inputs.
AUDIOIN	I	Analog audio input.
AUDIOOUT	O	Analog audio output.

(7) LED interface signals

Signal name	I/O	Description of function
LEDOUT	O	This is an output signal for lighting LEDs.

(8) CompactFlash interface and keyboard interface signals

Signal name	I/O	Description of function
CF_WE# / SCANOUT7	O	CompactFlash write enable output or keyboard scan data output.
CF_OE# / SCANOUT6	O	CompactFlash output enable or keyboard scan data output.
CF_IOW# / SCANOUT5	O	CompactFlash I/O write strobe output or keyboard scan data output.
CF_IOR# / SCANOUT4	O	CompactFlash I/O read strobe output or keyboard scan data output.
CF_STSCHG# / SCANOUT3	I/O	CompactFlash status changed input or keyboard scan data output.
CF_CE(2:1)# / SCANOUT(2:1)	O	CompactFlash card enable outputs or keyboard scan data outputs.
CF_BUSY# / SCANOUT0	I/O	CompactFlash ready/busy/interrupt request indication input or keyboard scan data output.
CF_REG# / SCANIN7	I/O	CompactFlash attribute memory chip access or keyboard scan data input.
CF_RESET / SCANIN6	I/O	CompactFlash reset output or keyboard scan data input.
CF_WAIT# / SCANIN5	I	CompactFlash wait input or keyboard scan data input.
CF_IOIS16# / SCANIN4	I	CompactFlash I/O 16-bit bus input or keyboard scan data input.
CF_VCCEN# / SCANIN3	I/O	CompactFlash V_{CC} enable output or keyboard scan data input.
CF_DEN# / SCANIN2	I/O	CompactFlash data buffer enable output or keyboard scan data input.
CF_DIR / SCANIN1	I/O	CompactFlash data direction output or keyboard scan data input.
CF_AEN# / SCANIN0	I/O	CompactFlash address buffer enable output or keyboard scan data input.

(9) Serial interface channel 1 signals

Signal name	I/O	Description of function
RxD1 / GPIO25	I/O	Serial channel 1 receive data input or general-purpose I/O.
TxD1 / GPIO26 / CLKSEL0	I/O	This function differs depending on the operating status. <During RTC reset (input)> This signal is used to set CPU core operation frequency clock[Note]. <During normal operation (input/output)> Serial channel 1 transmit data output or general-purpose I/O.
RTS1# / GPIO27 / CLKSEL1	I/O	This function differs depending on the operating status. <During RTC reset (input)> This signal is used to set CPU core operation frequency clock[Note]. <During normal operation (input/output)> Serial channel 1 request to send output or general-purpose I/O.
CTS1# / GPIO28	I/O	Serial channel 1 clear to send input or general-purpose I/O.
DCD1# / GPIO29	I/O	Serial channel 1 data carrier detect input or general-purpose I/O.
DTR1# / GPIO30 / CLKSEL2	I/O	This function differs depending on the operating status. <During RTC reset (input)> This signal is used to set CPU core operation frequency clock[Note]. <During normal operation (input/output)> Serial channel 1 data terminal ready output or general-purpose I/O.
DSR1# / GPIO31	I/O	Serial channel 1 data set ready input or general-purpose I/O.

Note CLKSEL(2:0) signals are used to set the frequency of the CPU core operation clock (PClock) and the internal MBA bus clock (TClock). These signals are sampled when the RTCRST# signal goes high.
The relationship between the CLKSEL(2:0) pin settings and clock frequency is shown below.

CLKSEL(2:0)	CPU core operation frequency (PClock)
111	Reserved (98.1 MHz)
110	Reserved (90.6 MHz)
101	Reserved (84.1 MHz
100	Reserved (78.5 MHz)
011	Reserved (69.3 MHz)
010	65.4 MHz
001	62.0 MHz
000	49.1 MHz

TClock is generated from PClock and its frequency is always 1/2 of the PClock frequency after RTC reset.

(10) IrDA interface signals

Signal name	I/O	Description of function
IRDIN / RxD2	I	IrDA receive data input or serial channel 2 receive data input. When connecting to an IrDA receive element, connect also to GND via resistor.
IRDOUT / TxD2	O	IrDA transmit data output or serial channel 2 transmit data output.

★

(11) General-purpose I/O signals

Signal name	I/O	Description of function
GPIO(31:25)	I/O	See **(9) Serial interface channel 1 signals** in this section
GPIO(24:16)	I/O	See **(1) System bus interface signals** in this section.
GPIO15 / FPD7 / CD2#	I/O	General-purpose I/O, LCD screen data output, or CompactFlash card detect 2 input.
GPIO14 / FPD6 / CD1#	I/O	General-purpose I/O, LCD screen data output, or CompactFlash card detect 1 input.
GPIO13 / FPD5	I/O	General-purpose I/O or LCD screen data output.
GPIO12 / FPD4	I/O	General-purpose I/O or LCD screen data output.
GPIO11 / PCS1#	I/O	General-purpose I/O or programmable chip select 1.
GPIO10 / FRM / SYSCLK	I/O	General-purpose I/O, clocked serial frame input for clocked serial interface, or ISA system clock output.
GPIO9 / CTS2#	I/O	General-purpose I/O or serial channel 2 clear to send output.
GPIO8 / DSR2#	I/O	General-purpose I/O or serial channel 2 data set ready input.
GPIO7 / DTR2#	I/O	General-purpose I/O or serial channel 2 data terminal ready input.
GPIO6 / RTS2#	I/O	General-purpose I/O or serial channel 2 request to send output.
GPIO5 / DCD2#	I/O	General-purpose I/O or serial channel 2 data carrier detect input.
GPIO4	I/O	General-purpose I/O.
GPIO3 / PCS0#	I/O	General-purpose I/O or programmable chip select 0.
GPIO2 / SCK	I/O	General-purpose I/O or serial clock signal for clocked serial interface.
GPIO1 / SO	I/O	General-purpose I/O or clocked serial data output signal for clocked serial interface.
GPIO0 / SI	I/O	General-purpose I/O or clocked serial data input signal for clocked serial interface.

(12) Dedicated V_{DD}/GND signals

Signal name	Power Supply	Description of function
VDD_PLL	2.5 V	Power supply dedicated for the PLL analog block.
GND_PLL	2.5 V	Ground dedicated for the PLL analog block.
VDD_TP	3.3 V	Power supply dedicated for the touch panel interface.
GND_TP	3.3 V	Ground dedicated for the touch panel interface.
VDD_AD	3.3 V	Power supply dedicated for the A/D and D/A converters. The voltage applied to this pin becomes the maximum value for the A/D and D/A interface signals.
GND_AD	3.3 V	Ground dedicated for the A/D and D/A converters. The voltage applied to this pin becomes the minimum value for the A/D and D/A interface signals.
VDD_OSC	3.3 V	Power supply dedicated for the oscillator.
GND_OSC	3.3 V	Ground dedicated for the oscillator.
VDD_LOGIC	2.5 V	Normally, power supply of 2.5 V
GND_LOGIC	2.5 V	Normally, ground of 2.5 V
VDD_IO	3.3 V	Normally, power supply of 3.3 V
GND_IO	3.3 V	Normally, ground of 3.3 V

Caution The V_R4181 has two types of power supplies. The 3.3 V power supply should be turned on at first. Turn on/off the 2.5 V power supply depending on the status of the MPOWER pin.

1.2 Pin Status in Specific Status

(1/3)

Signal Name	During RTCRST	After Reset by RTCRST	After Reset by Deadman's Switch or RSTSW	During Suspend mode	During Hibernate mode or Shut Down by HALTimer
ADD(21:0)	Hi-Z	0	0	**Note 1**	0
DATA(15:0)	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
MEMRD#	Hi-Z	1	1	1	Hi-Z
MEMWR#	Hi-Z	1	1	1	1
SDCS(1:0)# / RAS(1:0)#	Hi-Z	1	1	1 / 0 Note 2	1 / 0 Note 2
UDQM / UCAS#	Hi-Z	1	1	1 / 0 Note 2	1 / 0 Note 2
LDQM / LCAS#	Hi-Z	1	1	1 / 0 Note 2	1 / 0 Note 2
CAS#	Hi-Z	1	1	0	0
SDRAS#	Hi-Z	1	1	0	0
SDCLK	Hi-Z	Run	0	0	0
CLKEN	Hi-Z	1	1	1	0
SYSDIR	Hi-Z	0	0	0	0
SYSEN#	Hi-Z	0	0	0	0
IORD# / GPIO16	–	Hi-Z	Hi-Z	1 / **Note 1**	Hi-Z / **Note 3**
IOWR# / GPIO17	–	Hi-Z	Hi-Z	1 / **Note 1**	Hi-Z / **Note 3**
IORDY / GPIO18	–	Hi-Z	Hi-Z	**Note 1**	**Note 3**
IOCS16# / GPIO19	–	Hi-Z	Hi-Z	**Note 1**	**Note 3**
UBE# / GPIO20 / M	–	Hi-Z	Hi-Z	1 / **Note 1** / 0	Hi-Z / **Note 3** / 0
RESET# / GPIO21	–	Hi-Z	Hi-Z	**Note 1**	0 / **Note 3**
ROMCS(2:0)# / GPIO(24:22)	–	Hi-Z	Hi-Z	1 / **Note 1**	Hi-Z / **Note 3**
ROMCS3#	Hi-Z	Hi-Z	1	1	Hi-Z
SHCLK / LCDCS#	Hi-Z	0	0 / 1	0 / 1	0 / Hi-Z
LOCLK / MEMCS16#	Hi-Z	0	0 / –	0 / –	0 / –
FLM / MIPS16EN	**Note 4**	0	0	0	0
FPD(3:0)	Hi-Z	0	0	0	0
VPLCD / VPGPIO1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
VPBIAS / VPGPIO0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
POWER	–	–	–	–	–
RTCRST#	–	–	–	–	–
RSTSW#	–	–	–	–	–

Notes 1. Maintains the state of the previous Fullspeed mode.

2. The state depends on the MEMCFG_REG register setting.

3. The state depends on the GPHIBSTH/GPHIBSTL register setting.

4. The input level is sampled to determine the MIPS16 instruction mode.

Remark 0: low level, 1: high level, Hi-Z: high impedance

(2/3)

Signal Name	During RTCRST	After Reset by RTCRST	After Reset by Deadman's Switch or RSTSW	During Suspend mode	During Hibernate mode or Shut Down by HALTimer
POWERON	–	–	0	0	0
MPOWER	0	0	1	1	0
BATTINH / BATTINT#	–	–	–	–	–
RTCX2, RTCX1	–	–	–	–	–
CLKX2, CLKX1	–	–	–	–	–
TPX(1:0)	–	1	1	**Note 1**	1
TPY(1:0)	–	Hi-Z	Hi-Z	**Note 1**	Hi-Z
ADIN(2:0)	–	–	–	–	–
AUDIOIN	–	–	–	–	–
AUDIOOUT	–	0	0	**Note 1**	0
CF_WE# / SCANOUT7	Hi-Z	Hi-Z	Hi-Z	**Note 1**	**Note 2** / Hi-Z
CF_OE# / SCANOUT6	Hi-Z	Hi-Z	Hi-Z	**Note 1**	**Note 2** / Hi-Z
CF_IOW# / SCANOUT5	Hi-Z	Hi-Z	Hi-Z	**Note 1**	**Note 2** / Hi-Z
CF_IOR# / SCANOUT4	Hi-Z	Hi-Z	Hi-Z	**Note 1**	**Note 2** / Hi-Z
CF_STSCHG# / SCANOUT3	Hi-Z	Hi-Z	Hi-Z	**Note 1**	**Note 1** / Hi-Z
CF_CE(2:1)# / SCANOUT(2:1)	Hi-Z	Hi-Z	Hi-Z	**Note 1**	**Note 2** / Hi-Z
CF_BUSY# / SCANOUT0	Hi-Z	Hi-Z	Hi-Z	**Note 1**	**Note 1** / Hi-Z
CF_REG# / SCANIN7	Hi-Z	–	**Note 1**	**Note 1**	**Note 2** / **Note 1**
CF_RESET / SCANIN6	Hi-Z	–	**Note 1**	**Note 1**	**Note 3** / **Note 1**
CF_WAIT# / SCANIN5	–	–	**Note 1**	**Note 1**	–
CF_IOIS16# / SCANIN4	–	–	**Note 1**	**Note 1**	–
CF_VCCEN# / SCANIN3	Hi-Z	–	**Note 1**	**Note 1**	**Note 4** / **Note 1**
CF_DEN# / SCANIN2	Hi-Z	–	**Note 1**	**Note 1**	1 / **Note 1**
CF_DIR / SCANIN1	Hi-Z	–	**Note 1**	**Note 1**	1 / **Note 1**
CF_AEN# / SCANIN0	Hi-Z	–	**Note 1**	**Note 1**	1 / **Note 1**

Notes 1. Maintains the state of the previous Fullspeed mode.

2. When a wake-up by the CompactFlash interrupt request is enabled: Outputs high level.
When a wake-up by the CompactFlash interrupt request is disabled: Becomes high impedance.

3. When a wake-up by the CompactFlash interrupt request is enabled: Outputs low level.
When a wake-up by the CompactFlash interrupt request is disabled: Becomes high impedance.

4. When a wake-up by the CompactFlash interrupt request is enabled: Outputs low level.
When a wake-up by the CompactFlash interrupt request is disabled: Outputs high level.

Remark 0: low level, 1: high level, Hi-Z: high impedance

(3/3)

Signal Name	During RTCRST	After Reset by RTCRST	After Reset by Deadman's Switch or RSTSW	During Suspend mode	During Hibernate mode or Shut Down by HALTimer
RxD1 / GPIO25	–	Hi-Z	Hi-Z	**Note 1**	**Note 1** / **Note 2**
TxD1 / GPIO26 / CLKSEL0	**Note 3**	Hi-Z	Hi-Z	**Note 1**	**Note 1** / **Note 2**
RTS1# / GPIO27 / CLKSEL1	**Note 3**	Hi-Z	Hi-Z	**Note 1**	**Note 1** / **Note 2**
CTS1# / GPIO28	–	Hi-Z	Hi-Z	**Note 1**	**Note 1** / **Note 2**
DCD1# / GPIO29	–	Hi-Z	Hi-Z	**Note 1**	**Note 1** / **Note 2**
DTR1# / GPIO30 / CLKSEL2	**Note 3**	Hi-Z	Hi-Z	**Note 1**	**Note 1** / **Note 2**
DSR1# / GPIO31	–	Hi-Z	Hi-Z	**Note 1**	**Note 1** / **Note 2**
IRDIN / RxD2	–	–	–	–	–
IRDOUT / TxD2	Hi-Z	Hi-Z	1	**Note 1**	Hi-Z
GPIO(15:14) / FPD(7:6) / CD(2:1)#	–	Hi-Z	Hi-Z	**Note 1** / 0 / **Note 1**	**Note 2** / **Note 1**
GPIO(13:12) / FPD(5:4)	–	Hi-Z	Hi-Z	**Note 1** / 0	**Note 2** / **Note 1**
GPIO11 / PCS1#	– / Hi-Z	Hi-Z	Hi-Z / 1	**Note 1** / 1	**Note 2** / Hi-Z
GPIO10 / FRM / SYSCLK	– / Hi-Z	Hi-Z	Hi-Z	**Note 1** / 0	**Note 2** / **Note 1** / Hi-Z
GPIO9 / CTS2#	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
GPIO8 / DSR2#	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
GPIO7 / DTR2#	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
GPIO6/ RTS2#	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
GPIO5 / DCD2#	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
GPIO4	–	Hi-Z	Hi-Z	**Note 1**	**Note 2**
GPIO3 / PCS0#	– / Hi-Z	Hi-Z	Hi-Z / 1	**Note 1** / 1	**Note 2** / Hi-Z
GPIO2 / SCK	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
GPIO1 / SO	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
GPIO0 / SI	–	Hi-Z	Hi-Z	**Note 1**	**Note 2** / **Note 1**
LEDOUT	Hi-Z	1	**Note 1**	**Note 1**	**Note 1**

Notes 1. Maintains the state of previous Fullspeed mode.

2. The state depends on the GPHIBSTH/GPHIBSTL register setting.

3. The input level is sampled to determine the CPU core operation frequency.

Remark 0: low level, 1: high level, Hi-Z: high impedance

★ 1.3 Recommended Connection of Unused Pins and I/O Circuit Types

(1/3)

Pin Name	Recommended Connection When Not Used	I/O Circuit Type
ADD(21:0)	–	A
DATA(15:0)	–	A
MEMRD#	–	A
MEMWR#	–	A
SDCS(1:0)# / RAS(1:0)#	–	A
UDQM / UCAS#	–	A
LDQM / LCAS#	–	A
CAS#	Leave open	A
SDRAS#	Leave open	A
SDCLK	Leave open	A
CLKEN	Leave open	A
SYSDIR	Leave open	A
SYSEN#	Leave open	A
IORD# / GPIO16	Connect to VDD_IO or GND_IO via resistor	A
IOWR# / GPIO17	Connect to VDD_IO or GND_IO via resistor	A
IORDY / GPIO18	Connect to VDD_IO or GND_IO via resistor	A
IOCS16# / GPIO19	Connect to VDD_IO or GND_IO via resistor	A
UBE# / GPIO20 / M	Connect to VDD_IO or GND_IO via resistor	A
RESET# / GPIO21	Connect to VDD_IO or GND_IO via resistor	A
ROMCS(2:0)# / GPIO(24:22)	Connect to VDD_IO or GND_IO via resistor	A
ROMCS3#	–	A
SHCLK / LCDCS#	Leave open	A
LOCLK / MEMCS16#	Leave open	A
FLM / MIPS16EN	Connect to VDD_IO or GND_IO via resistor	A
FPD(3:0)	Leave open	A
VPLCD / VPGPIO1	Leave open	A
VPBIAS / VPGPIO0	Leave open	A
POWER	Connect to GND_IO via resistor	A
RTCRST#	–	A
RSTSW#	–	A
POWERON	Leave open	A
MPOWER	–	A
BATTINH / BATTINT#	–	A
TPX(1:0)	–	B
TPY(1:0)	–	C

Remark No specification (–) in the Recommended Connection When Not Used column indicates that the pin is always connected.

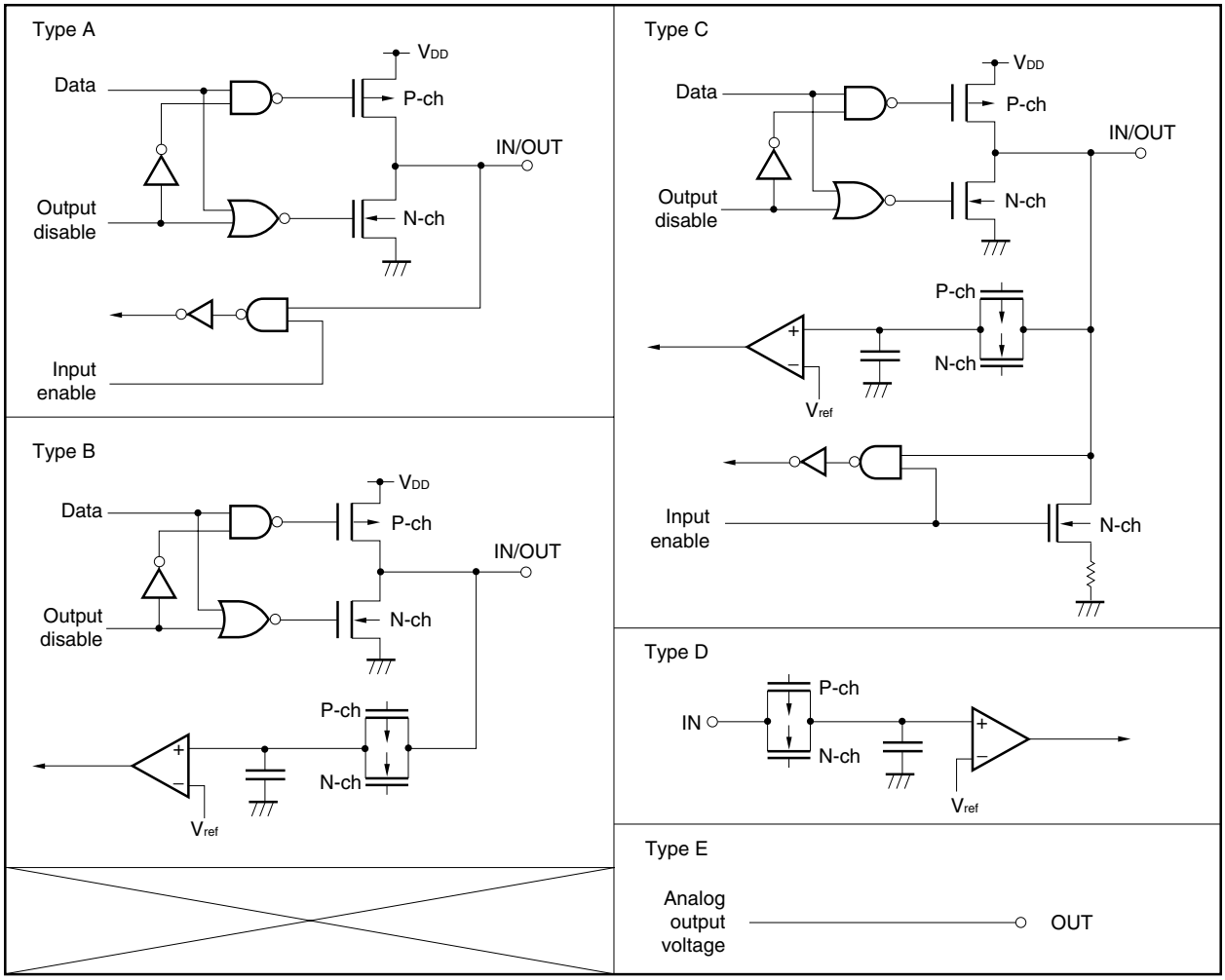
(2/3)

Pin Name	Recommended Connection When Not Used	I/O Circuit Type
ADIN(2:0)	Connect to GND_AD	D
AUDIOIN	Connect to GND_AD	D
AUDIOOUT	Leave open	E
CF_WE# / SCANOUT7	Leave open	A
CF_OE# / SCANOUT6	Leave open	A
CF_IOW# / SCANOUT5	Leave open	A
CF_IOR# / SCANOUT4	Leave open	A
CF_STSCHG# / SCANOUT3	Connect to VDD_IO via resistor	A
CF_CE(2:1)# / SCANOUT(2:1)	Leave open	A
CF_BUSY# / SCANOUT0	Connect to VDD_IO via resistor	A
CF_REG# / SCANIN7	Leave open	A
CF_RESET / SCANIN6	Leave open	A
CF_WAIT# / SCANIN5	Connect to VDD_IO via resistor	A
CF_IOIS16# / SCANIN4	Connect to VDD_IO via resistor	A
CF_VCCEN# / SCANIN3	Leave open	A
CF_DEN# / SCANIN2	Leave open	A
CF_DIR / SCANIN1	Leave open	A
CF_AEN# / SCANIN0	Leave open	A
RxD1 / GPIO25	Connect to VDD_IO or GND_IO via resistor	A
TxD1 / GPIO26 / CLKSEL0	Connect to VDD_IO or GND_IO via resistor	A
RTS1# / GPIO27 / CLKSEL1	Connect to VDD_IO or GND_IO via resistor	A
CTS1# / GPIO28	Connect to VDD_IO or GND_IO via resistor	A
DCD1# / GPIO29	Connect to VDD_IO or GND_IO via resistor	A
DTR1# / GPIO30 / CLKSEL2	Connect to VDD_IO or GND_IO via resistor	A
DSR1# / GPIO31	Connect to VDD_IO or GND_IO via resistor	A
IRDIN / RxD2	Connect to VDD_IO or GND_IO via resistor	A
IRDOUT / TxD2	Leave open	A
GPIO(15:14) / FPD(7:6) / CD(2:1)#	Connect to VDD_IO or GND_IO via resistor	A
GPIO(13:12) / FPD(5:4)	Connect to VDD_IO or GND_IO via resistor	A
GPIO11 / PCS1#	Connect to VDD_IO or GND_IO via resistor	A
GPIO10 / FRM / SYSCLK	Connect to VDD_IO or GND_IO via resistor	A
GPIO9 / CTS2#	Connect to VDD_IO or GND_IO via resistor	A
GPIO8 / DSR2#	Connect to VDD_IO or GND_IO via resistor	A
GPIO7 / DTR2#	Connect to VDD_IO or GND_IO via resistor	A
GPIO6 / RTS2#	Connect to VDD_IO or GND_IO via resistor	A
GPIO5 / DCD2#	Connect to VDD_IO or GND_IO via resistor	A
GPIO4	Connect to VDD_IO or GND_IO via resistor	A

(3/3)

Pin Name	Recommended Connection When Not Used	I/O Circuit Type
GPIO3 / PCS0#	Connect to VDD_IO or GND_IO via resistor	A
GPIO2 / SCK	Connect to VDD_IO or GND_IO via resistor	A
GPIO1 / SO	Connect to VDD_IO or GND_IO via resistor	A
GPIO0 / SI	Connect to VDD_IO or GND_IO via resistor	A
LEDOUT	Leave open	A

★ 1.4 Pin I/O Circuits



2. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD2}	2.5 V (VDD_LOGIC, VDD_PLL)	–0.5 to +3.6	V
	V_{DD3}	3.3 V (VDD_IO, VDD_TP, VDD_AD, VDD_OSC)	–0.5 to +4.0	V
Input voltage	V_I	$V_{DD3} \geq 3.7$ V	–0.5 to +4.0	V
		$V_{DD3} < 3.7$ V	–0.5 to V_{DD3} + 0.3	V
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not short-circuit two or more output pins simultaneously.

2. If even one of the above parameters exceeds the absolute maximum ratings even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding which the product may be physically damaged. Use the product well within these ratings.

The specifications and conditions shown in DC Characteristics and AC Characteristics are the ranges for normal operation and quality assurance of the product.

3. V_I can be –1.5 V if the input pulse is less than 10 ns.

Operating Conditions

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Supply voltage	V_{DD2}	2.5 V (VDD_LOGIC, VDD_PLL)	2.3	2.7	V
	V_{DD3}	3.3 V (VDD_IO, VDD_TP, VDD_AD, VDD_OSC)	3.0	3.6	V
Ambient temperature	T_A		–10	+70	°C
Oscillation start voltage Note 1	V_{DDS}			3.0	V
Oscillation hold voltage Note 2	V_{DDH1}			2.5	V
Oscillation hold voltage Note 3	V_{DDH2}			3.0	V

Notes 1. This is a voltage at which oscillation is always started after power application, and is applied to oscillators of 32.768 kHz and 18.432 MHz.

2. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 32.768 kHz.

3. This is a voltage at which oscillation can be guaranteed if the voltage is lowered from the normal operation level, and is applied to an oscillator of 18.432 MHz.

Remark The V_R4181 has two types of power supplies. The 3.3 V power supply should be turned on at first. Turn on/off the 2.5 V power supply depending on the status of the MPOWER pin.

Capacitance (T_A = 25°C, V_{DD3} = 0 V)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		10	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.		10	pF

DC Characteristics (T_A = −10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = −2 mA		2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA				0.4	V
High-level input voltage	V_{IH}			0.6V_{DD3}		V_{DD3} + 0.3	V
Low-level input voltage	V_{IL}			−0.3		0.8	V
Input leakage current	I_{LI}	V_{DD3} = 3.6 V, V_I = V_{DD3}, 0 V				±5	μA
Output leakage current	I_{LO}	V_{DD3} = 3.6 V, V_I = V_{DD3}, 0 V				±5	μA
Supply Current	I_{DD2} Note 1	In Fullspeed mode When using internal LCD controller	EDO		0.5fp	0.7fp	mA
			SDRAM		0.7fp	0.9fp	
		In Fullspeed mode When not using internal LCD controller	EDO		0.5fp−5	0.7fp−10	mA
			SDRAM		0.7fp−5	0.9fp−5	
		In Standby mode When using internal LCD controller			20	30	mA
		In Standby mode When not using internal LCD controller			15	25	mA
		In Suspend mode Note 2			10	20	mA
		In Hibernate mode VDD_LOGIC = 0 V			0	0	μA
	I_{DD3} Note 1	In Fullspeed mode When using internal LCD controller			10 (12)	15 (24)	mA
		In Fullspeed mode When not using internal LCD controller			8 (10)	13 (16)	mA
		In Standby mode When using internal LCD controller			7 (9)	12 (18)	mA
		In Standby mode When not using internal LCD controller			5 (7)	8 (14)	mA
		In Suspend mode Note 2			2 (4)	4 (8)	mA
		In Hibernate mode LED unit ON			2	4	mA
		In Hibernate mode LED unit OFF			25	50	μA

Notes 1. I_{DD2} is a total power supply current for the 2.5 V power supply. I_{DD2} is applied to the VDD_LOGIC and VDD_PLL pins.

I_{DD3} is a total power supply current for the 3.3 V power supply. I_{DD3} is applied to the VDD_OSC, VDD_IO, VDD_TP, and VDD_AD pins.

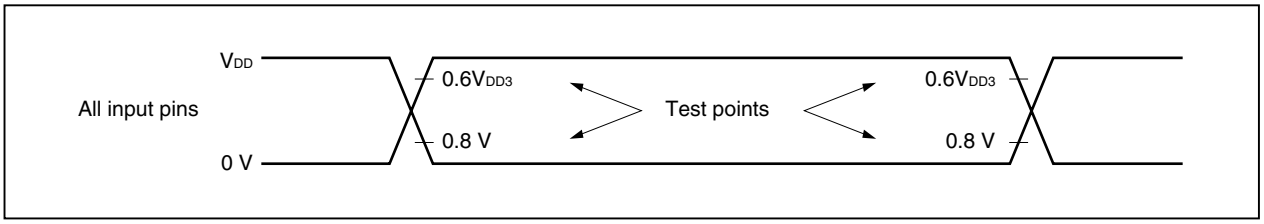
2. In Suspend mode, the internal LCD controller can not work because memory controller's clock and the LCD controller's clock are stopped.

Remarks 1. fp: Operation clock (PClock) frequency (MHz)

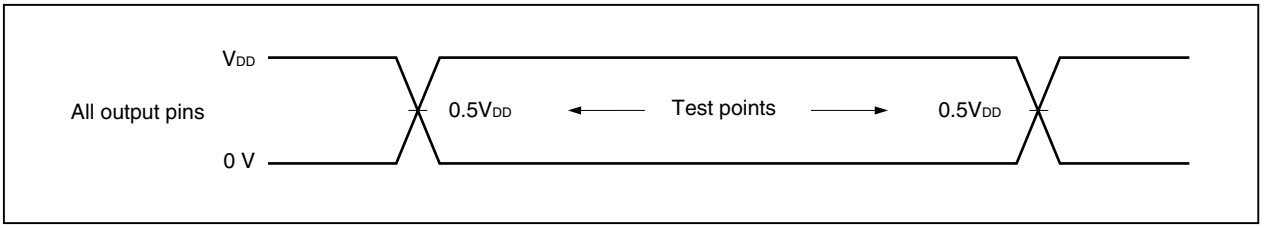
2. The values inside the parentheses are for those when using internal A/D converter.

AC Characteristics (T_A = −10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

AC test input waveform

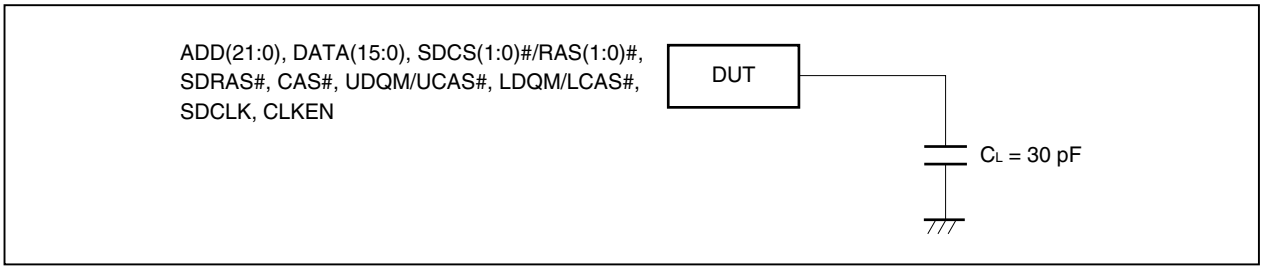


AC test output measuring points

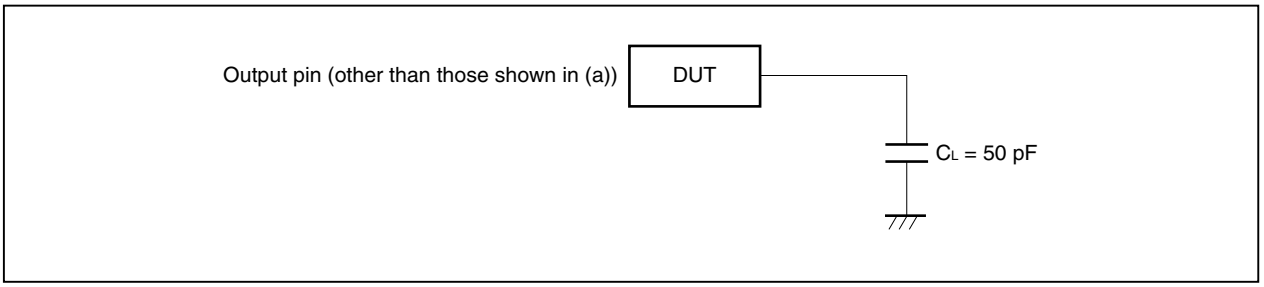


Load condition

(a) ADD(21:0), DATA(15:0), SDCS(1:0)#/RAS(1:0)#, SDRAS#, CAS#, UDQM/UCAS#, LDQM/LCAS#, SDCLK, CLKEN



(b) Other output pins



(1) Clock parameter

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU core operating frequency	f_{PCLOCK}	CLKSEL (2:0) = 111 Note 1		98.1		MHz
		CLKSEL (2:0) = 110 Note 1		90.6		MHz
		CLKSEL (2:0) = 101 Note 1		84.1		MHz
		CLKSEL (2:0) = 100 Note 1		78.5		MHz
		CLKSEL (2:0) = 011 Note 1		69.3		MHz
		CLKSEL (2:0) = 010		65.4		MHz
		CLKSEL (2:0) = 001		62.0		MHz
		CLKSEL (2:0) = 000		49.1		MHz
TClock, MBA clock, SDCLK frequency Note 2	f_{TCLOCK}	DIV(2:0) = 100 Note 1		$f_{PCLOCK}/4$	**Note 3**	MHz
		DIV(2:0) = 011		$f_{PCLOCK}/3$	**Note 3**	MHz
		DIV(2:0) = 010, 000		$f_{PCLOCK}/2$	**Note 3**	MHz
		DIV(2:0) = 001		f_{PCLOCK}	**Note 3**	MHz
SDCLK cycle time	t_{SDCLK}		15			ns
PCLK frequency Note 4	f_{PCK}	PCLKDIV(1:0) = 11		f_{TCLOCK}	**Note 5**	MHz
		PCLKDIV(1:0) = 10		$f_{TCLOCK}/2$	**Note 5**	MHz
		PCLKDIV(1:0) = 01		$f_{TCLOCK}/4$	**Note 5**	MHz
		PCLKDIV(1:0) = 00		$f_{TCLOCK}/8$	**Note 5**	MHz
SYSCLK frequency Note 6	f_{SYSCLK}	SCLKDIV(1:0) = 11		$f_{PCK}/8$	**Note 7**	MHz
		SCLKDIV(1:0) = 10		$f_{PCK}/6$	**Note 7**	MHz
		SCLKDIV(1:0) = 01		$f_{PCK}/3$	**Note 7**	MHz
		SCLKDIV(1:0) = 00		$f_{PCK}/2$	**Note 7**	MHz

Notes 1. Do not set these rates in the current VR4181.

2. TClock (internal), MBA clock (internal) and SDCLK frequency are programmable, however, the frequency immediately after RTC reset is fixed. To change these clock's frequency, set the DIV(2:0) bits of the PMUDIVREG register (0x0B00 00AC) in PMU and make the VR4181 into Hibernate mode. When the CPU wakes up from Hibernate mode next time, the frequency is changed.

3. The maximum value of f_{TCLOCK} is 66 MHz regardless of typical frequency.

4. PCLK (internal ISA peripheral clock) is generated by dividing TClock. Its division rate is defined by the PCLKDIV(1:0) bits of the ISABRGCTL register (0x0B00 02C0) in ISA Bridge.

5. The maximum value of f_{PCK} is 33 MHz regardless of typical frequency.

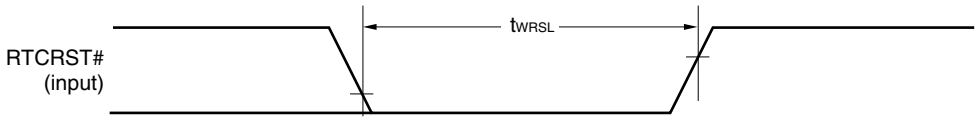
6. SYSCLK is generated by dividing PCLK. Its division rate is defined by the SCLKDIV(1:0) bits of the XISACTL register (0x0B00 02C4) in ISA Bridge.

7. The maximum value of f_{SYSCLK} is 16 MHz regardless of typical frequency.

Remark CPU core clock (Pipeline clock, PClock) frequency is defined by CLKSEL(2:0) pins just after RTC reset.

(2) Reset parameter

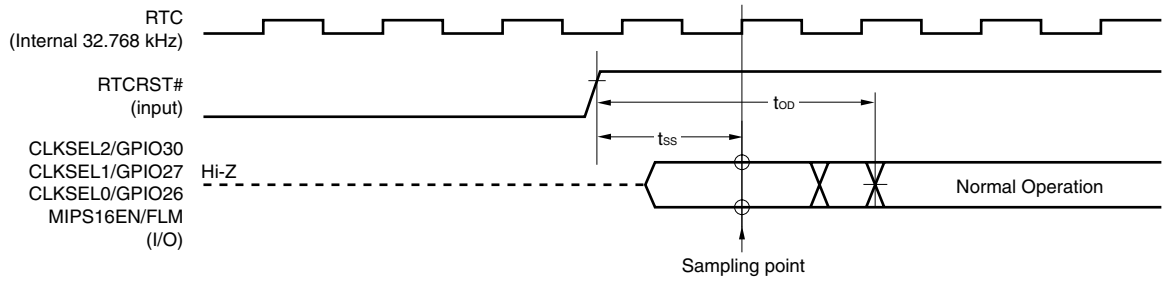
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RTCRST# pin	305		μs



Remark For the RTCRST# characteristics at power supply, refer to **VR4181 User's Manual**.

(3) Initialization parameter

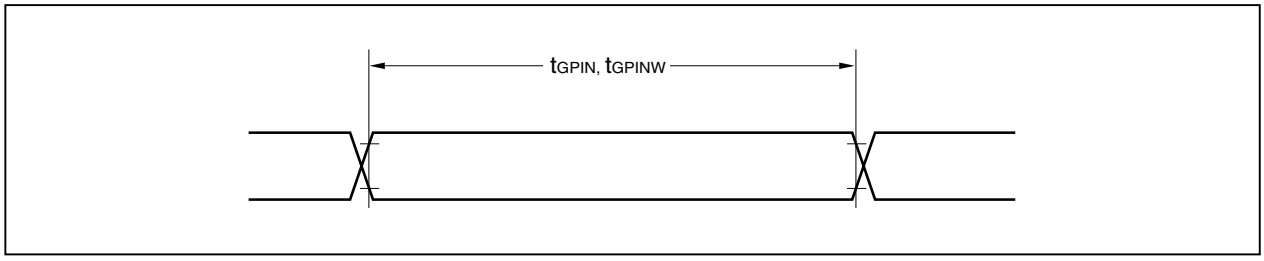
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RTCRST# ↑)	t_{SS}			61.04	μs
Output delay time (from RTCRST# ↑)	t_{OD}		61.04		μs



(4) GPIO interface parameter

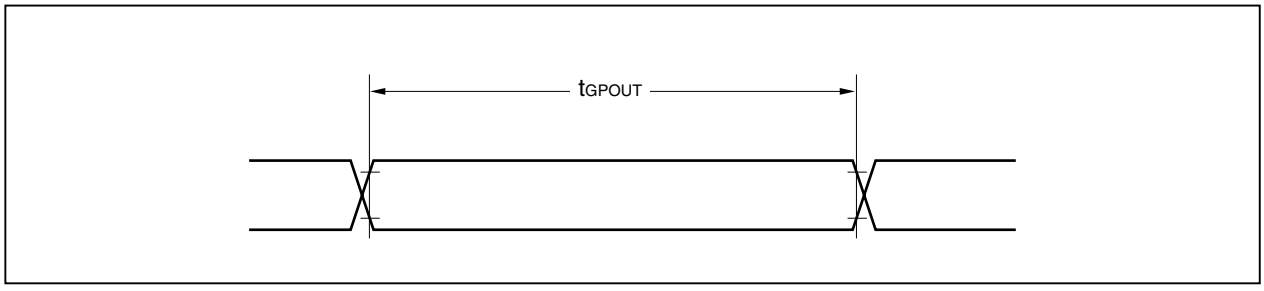
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input level width	t_{GPIN}	Normal operation	$16/f_{TCLOCK}$		μs
	t_{GPINW}	Wake-up Hibernate mode	100		μs
GPIO input rise time	t_{GPRISE}			200	ns
GPIO input fall time	t_{GPFALL}			200	ns
Output level width	t_{GPOUT}		$11/f_{PCK}$		ns

(a) Input level width



(b) Input rise/fall time

(c) Output level width



★ **(5) EDO type DRAM parameter**

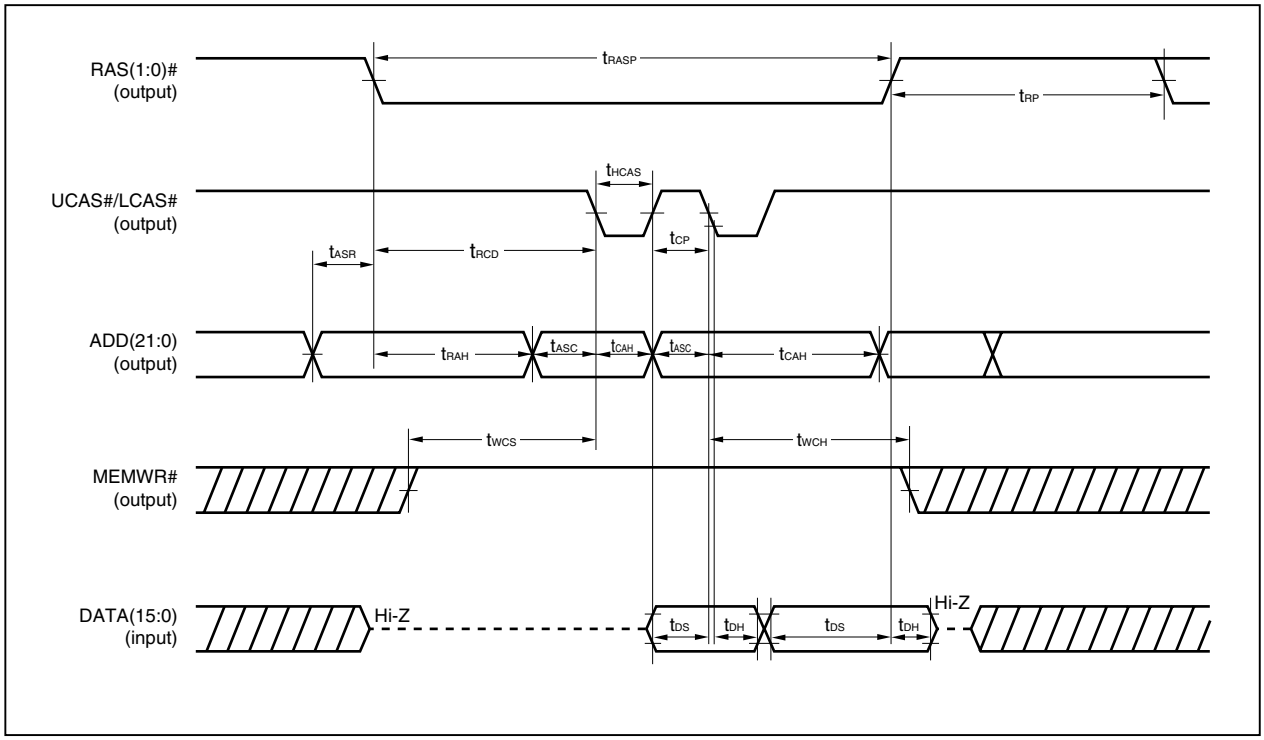
The target EDO-type DRAM organization is as follows.

- 16M-bit
  1M words × 16 bits (row × column = 10 × 10)
  1M words × 16 bits (row × column = 12 × 8)
- 64M-bit
  4M words × 16 bits (row × column = 13 × 9)

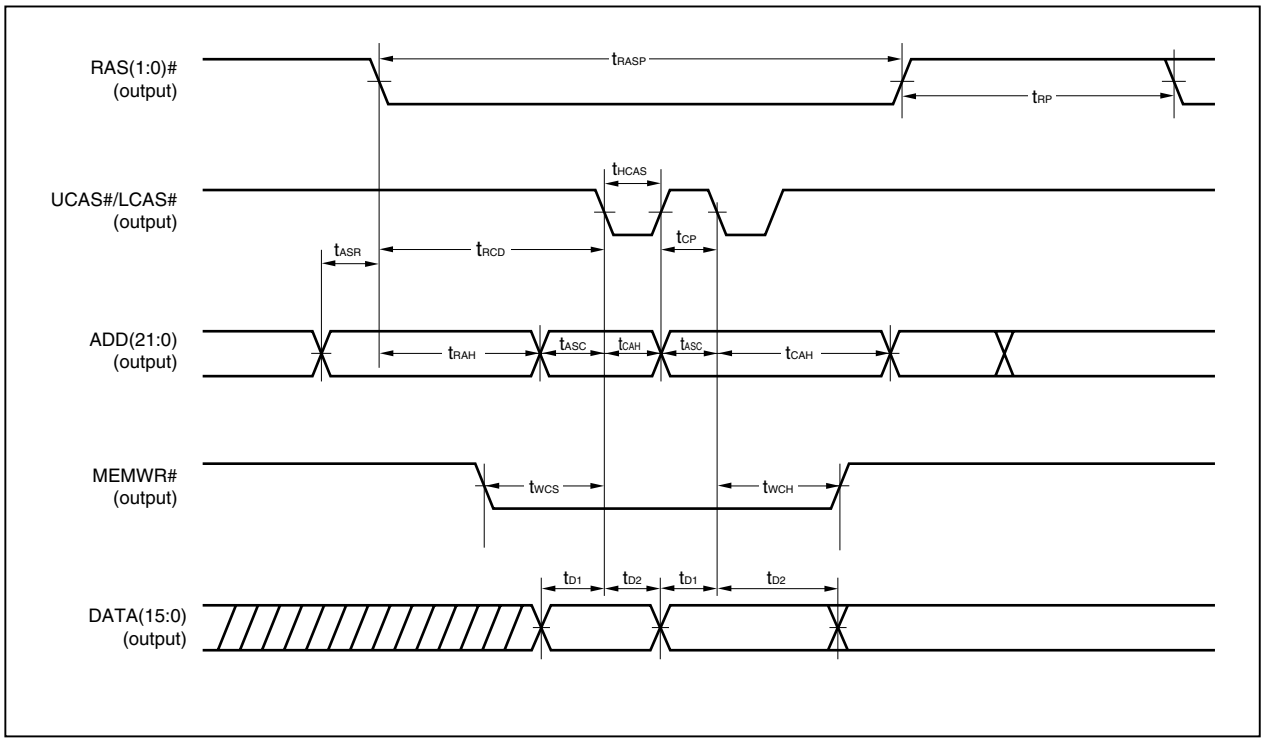
Parameter	Symbol	Condition	MIN.	MAX.	Unit
RAS(1:0)# pulse width	t_{RASP}		4000/f_{TCLOCK}		ns
RAS(1:0)# precharge time[Note]	t_{RP}		3000/f_{TCLOCK}		ns
UCAS#/LCAS# pulse width[Note]	t_{HCAS}		1000/f_{TCLOCK}		ns
UCAS#/LCAS# precharge time[Note]	t_{CP}		1000/f_{TCLOCK}		ns
Row address setup time (to RAS(1:0)#↓)	t_{ASR}		1000/f_{TCLOCK}		ns
UCAS#/LCAS# ↓ delay time from RAS(1:0)#[Note]	t_{RCD}		3000/f_{TCLOCK}		ns
Column address setup time (to UCAS#/LCAS#↓)	t_{ASC}		1000/f_{TCLOCK}		ns
Row address hold time (from RAS(1:0)# ↓)	t_{RAH}		1000/f_{TCLOCK}		ns
Column address hold time (UCAS#/LCAS#↓)	t_{CAH}		1000/f_{TCLOCK}		ns
Data input setup time	t_{DS}		1000/f_{TCLOCK}		ns
Data input hold time	t_{DH}		5		ns
MEMWR# setup time (to UCAS#/LCAS#↓)	t_{WCS}		2000/f_{TCLOCK}		ns
MEMWR# hold time (from UCAS#/LCAS#↓)	t_{WCH}		3000/f_{TCLOCK}		ns
Data output setup time (to UCAS#/LCAS#↓)	t_{D1}		1000/f_{TCLOCK}		ns
Data output hold time (from UCAS#/LCAS#↓)	t_{D2}		1000/f_{TCLOCK}		ns

Note t_{RP}, t_{CP}, t_{HCAS}, and t_{RCD} are programmable.

(a) Read parameter

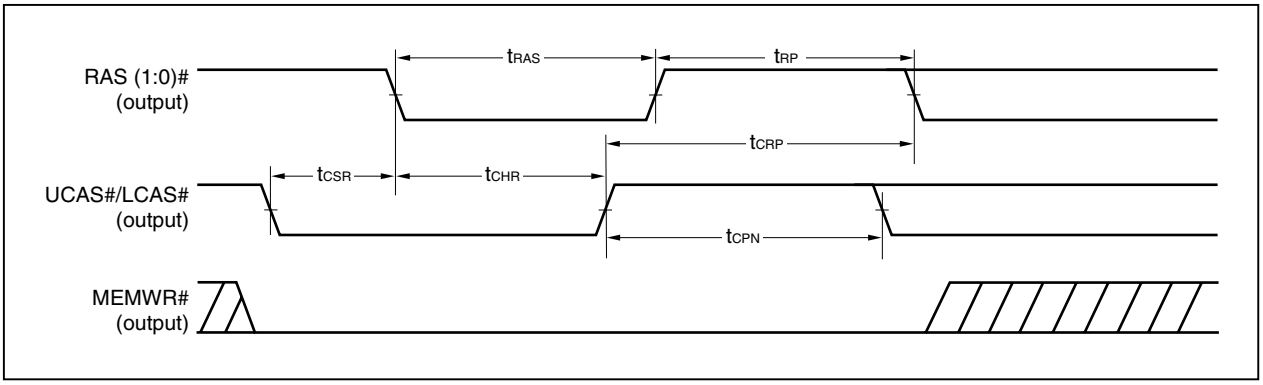


(b) Write parameter



★ **(6) EDO DRAM refresh parameter**

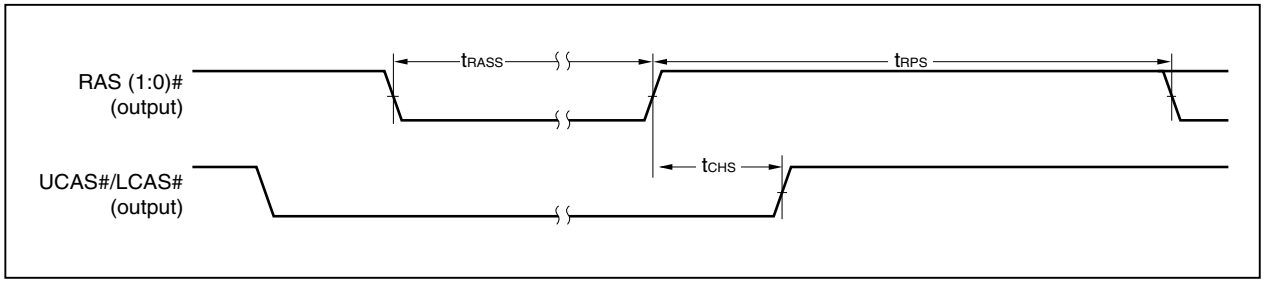
Parameter	Symbol	Condition	MIN.	MAX.	Unit
RAS (1:0)# pulse width	t_{RAS}		$4000/f_{TCLOCK}$		ns
RAS (1:0)# precharge time	t_{RP}		$3000/f_{TCLOCK}$		ns
UCAS#/LCAS# setup time (to RAS (1:0)# ↓)	t_{CSR}		$1000/f_{TCLOCK}$		ns
UCAS#/LCAS# hold time (from RAS (1:0)# ↓)	t_{CHR}		$4000/f_{TCLOCK}$		ns
RAS (1:0)# precharge time from UCAS#/LCAS# ↑	t_{CRP}		$2000/f_{TCLOCK}$		ns
UCAS#/LCAS# precharge time	t_{CPN}		$1000/f_{TCLOCK}$		ns



(7) EDO DRAM CAS-before-RAS self-refresh parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
RAS(1:0)# pulse width	t_{RASS}		100		μs
RAS(1:0)# precharge time[Note]	t_{RPS}		110		ns
UCAS#/LCAS# hold time	t_{CHS}		–50		ns

Note RAS(1:0)# precharge time in self-refresh mode is programmable.



(8) SDRAM parameter

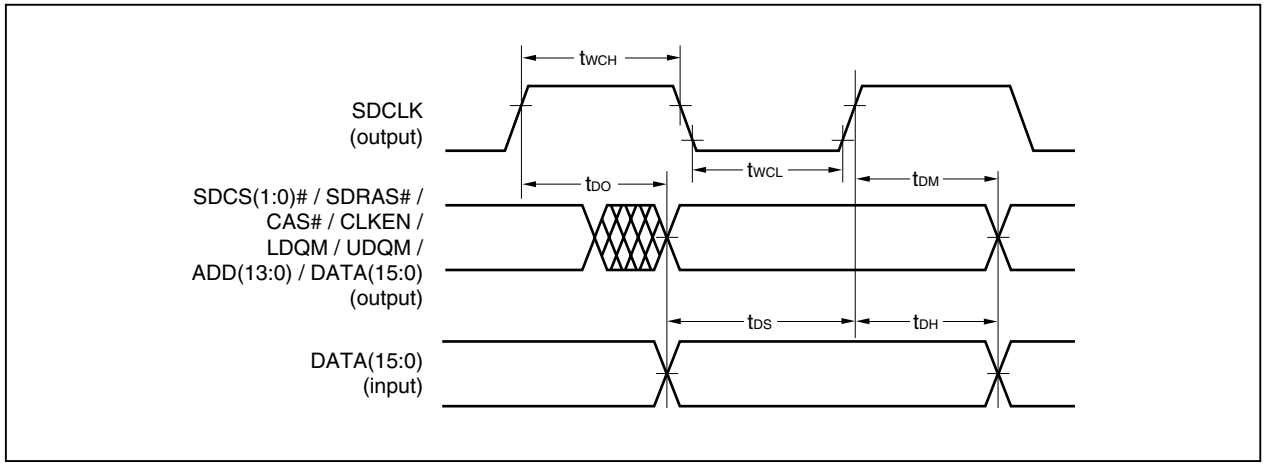
The target SDRAM organization is as follows.

- 16M-bit
  512K words × 16 bits × 2 banks
- 64M-bit
  2M words × 16 bits × 2 banks
  1M words × 16 bits × 4 banks

Parameter	Symbol	Condition	MIN.	MAX.	Unit
REF to REF/ACT Command signal period[Note]	t_{RC}		$7t_{SDCLK}$		ns
ACT to PRE Command signal[Note]	t_{RAS}		$5t_{SDCLK}$		ns
PRE to ACT Command signal[Note]	t_{RP}		$3t_{SDCLK}$		ns
UCAS#/LCAS# delay time from RAS(1:0)#	t_{RCD}		$3t_{SDCLK}$		ns
ACT to ACT Command signal[Note]	t_{RRD}		$14t_{SDCLK}$		ns
Data-in to PRE Command signal[Note]	t_{DPL}		$2t_{SDCLK}$		ns
Data-in to ACT Command signal[Note]	t_{DAL}		$12t_{SDCLK}$		ns
Mode register set cycle time	t_{RSC}		$4t_{SDCLK}$		ns
SDCLK high-level width	t_{WCH}		$0.3t_{SDCLK}$	$0.7t_{SDCLK}$	ns
SDCLK low-level width	t_{WCL}		$0.3t_{SDCLK}$	$0.7t_{SDCLK}$	ns
Data input setup time	t_{DS}		9		ns
Data input hold time	t_{DH}		0		ns
Command signal, ADD(13:0), DATA(15:0) output delay time[Note]	t_{DM}/t_{DO}		2	13	ns

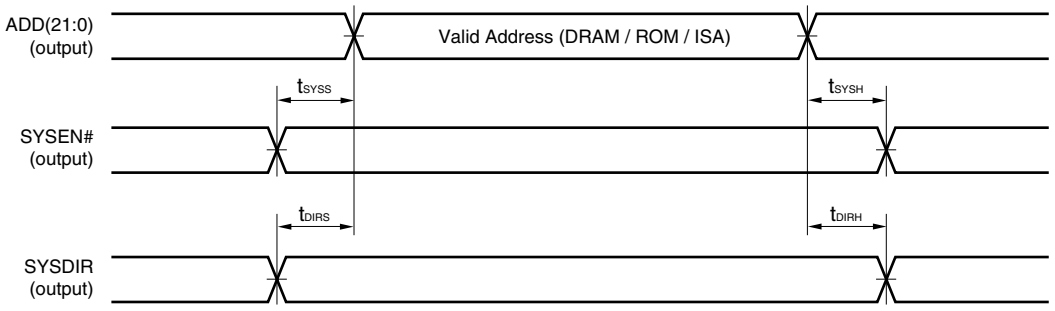
Note With the VR4181, the SDCS(1:0)#, SDRAS#, CAS#, CLKEN, LDQM, and UDQM are called the command signals for the SDRAM interface.

Remark t_{SDCLK}: SDCLK cycle time (see **(1) Clock parameter** in this section).



(9) System buffer control signal parameter

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SYSEN# setup time to Valid Address	t_{SYSS}		0	$1000/f_{TCLOCK}$		ns
SYSEN# hold time from Valid Address	t_{SYSH}		0			ns
SYSDIR setup time to Valid Address	t_{DIRS}		0	$1000/f_{TCLOCK}$		ns
SYSDIR hold time from Valid Address	t_{DIRH}		0			ns



★ **Remark**

SYSEN#	SYSDIR	Bus Cycle
High	Don't care	DRAM Read or Wtite Cycle
Low	Low	ROM / ISA / CompactFlash Read Cycle
Low	High	Flash Memory / ISA / CompactFlash Wtite Cycle

★ **(10) Ordinary ROM parameter**

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note]	t_{ACC}		N		ns
Data access time (from ROMCS (3:0)# ↓)[Note]	t_{CE}		N		ns
Data input setup time	t_{DS}		10		ns
Data input hold time	t_{DH}		6		ns

Note The value of N is set by using the WROMA (3:0) bits of the BCUSPEEDREG register.
The value of N can be obtained by calculating the following expression.

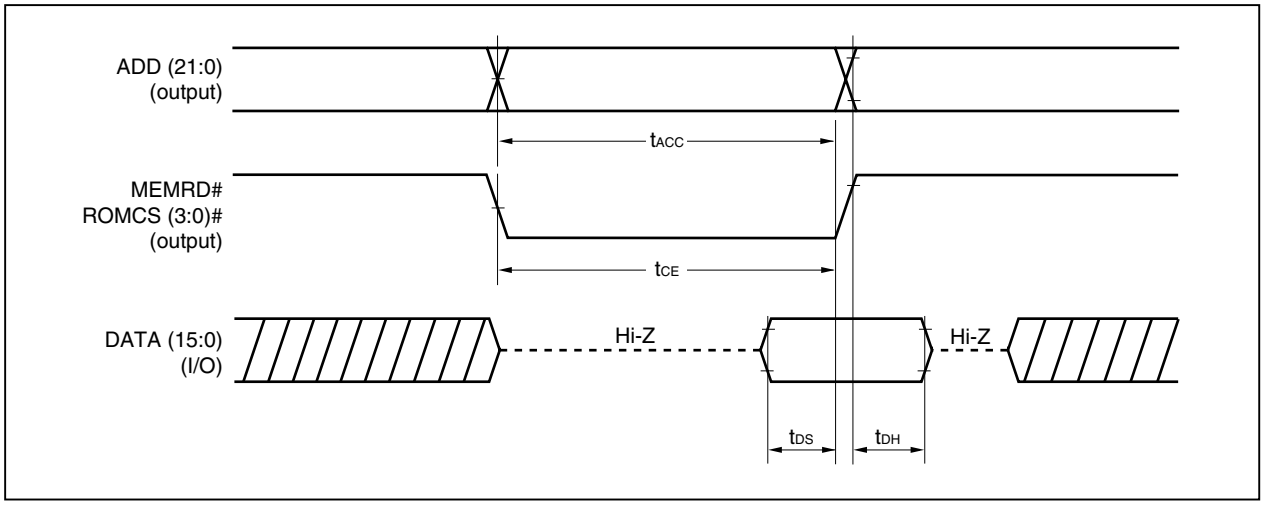
N = TClock cycle time × (WROMA (3:0) + 2)

WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
0	40	30
1	60	45
2	80	60
3	100	75
4	120	90
5	140	105
6	160	120
7	180	135

Note TClock frequency (example)

WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
8	200	150
9	220	165
10	240	180
11	260	195
12	280	210
13	300	225
14	320	240
15	340	255

Note TClock frequency (example)



★ **(11) Page ROM parameter (1/2)**

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address) 1[Note]	t_{ACC1}		N		ns
Data access time (from address) 2[Note]	t_{ACC2}		M		ns
Data access time (from ROMCS (3:0)# ↓)[Note]	t_{CE}		N		ns
Data input setup time	t_{DS}		10		ns
Data input hold time	t_{DH}		6		ns

Note The value of N is set by using the WROMA (3:0) bits of the BCUSPEEDREG register.
The value of M is set by using the WPROM (2:0) bits of the BCUSPEEDREG register.
The value of each variable can be obtained by calculating the following expression.

N = TClock cycle time × (WROMA (3:0) + 2)
M = TClock cycle time × (WPROM (2:0) + 2)

WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
0	40	30
1	60	45
2	80	60
3	100	75
4	120	90
5	140	105
6	160	120
7	180	135

Note TClock frequency (example)

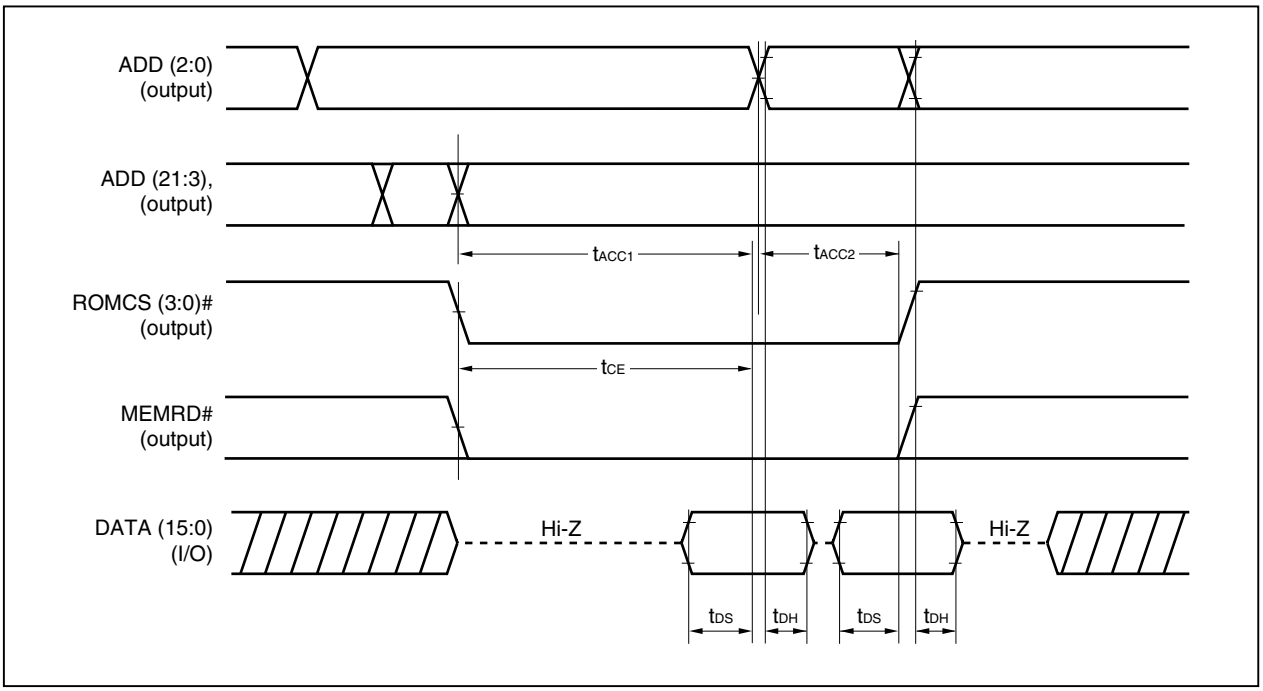
WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
8	200	150
9	220	165
10	240	180
11	260	195
12	280	210
13	300	225
14	320	240
15	340	255

Note TClock frequency (example)

WPROM(2:0)	M (ns)	
	50 MHz[Note]	66 MHz[Note]
0	40	30
1	60	45
2	80	60
3	100	75
4	120	90
5	140	105
6	160	120
7	180	135

Note TClock frequency (example)

(11) Page ROM parameter (2/2)



★ **(12) Flash memory mode write parameter**

Parameter	Symbol	Condition	50 MHz[Note 2]		66 MHz[Note 2]		Unit
			MIN.	MAX.	MIN.	MAX.	
Write cycle time[Note 1]	t_{AVAV}		N		N		ns
Address setup time (to MEMWR# ↑)[Note 1]	t_{AVWH}		N – 25		N – 20		ns
Address setup time (to ROMCS (3:0)# ↓)	t_{AVEL}		0		0		ns
ROMCS (3:0)# setup time (to MEMWR#↓)	t_{ELWL}		15		10		ns
MEMWR# low-level width[Note 1]	t_{WLWH}		N – 45		N – 35		ns
ROMCS (3:0)# hold time (from MEMWR# ↑)	t_{WHEH}		20		15		ns
Address hold time (from MEMWR# ↑)	t_{WHAX}		20		15		ns
MEMWR# high-level width	t_{WHWL}		170		130		ns
Address setup time (to MEMWR# ↓)	t_{AVWL}		15		10		ns
Data output setup time (to MEMWR# ↑)[Note 1]	t_{DVWH}		N – 45		N – 35		ns
Data output hold time (from MEMWR# ↑)	t_{WHDX}		15		10		ns

Notes 1. The value of N is set by using the WROMA(3:0) bits of the BCUSPEEDREG register.
The value of N can be obtained by calculating the following expression.

N = TClock cycle time × (WROMA (3:0) + 2)

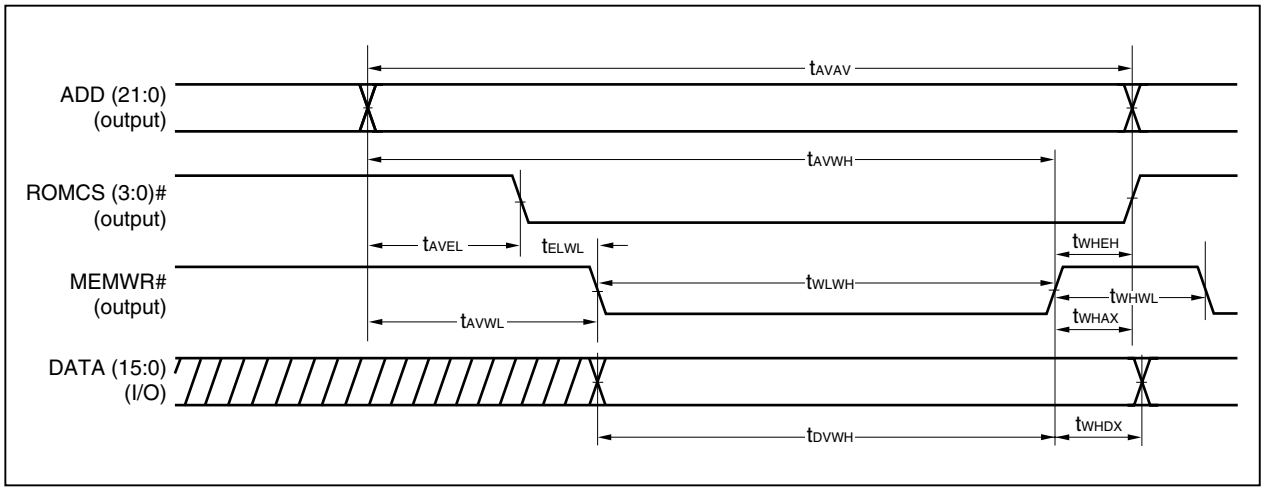
2. TClock frequency (example)

WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
0	60	45
1	80	60
2	100	75
3	120	90
4	140	105
5	160	120
6	180	135
7	200	150

Note TClock frequency (example)

WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
8	220	165
9	240	180
10	260	195
11	280	210
12	300	225
13	320	240
14	340	255
15	360	270

Note TClock frequency (example)



★ **(13) Flash memory mode read parameter**

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)[Note]	t_{ACC}		N		ns
Data access time (from ROMCS (3:0)# ↓)[Note]	t_{CE}		N		ns
Data input setup time	t_{DS}		10		ns
Data input hold time	t_{DH}		6		ns

Note The value of N is set by using the WROMA (3:0) bits of the BCUSPEEDREG register.
The value of N can be obtained by calculating the following expression.

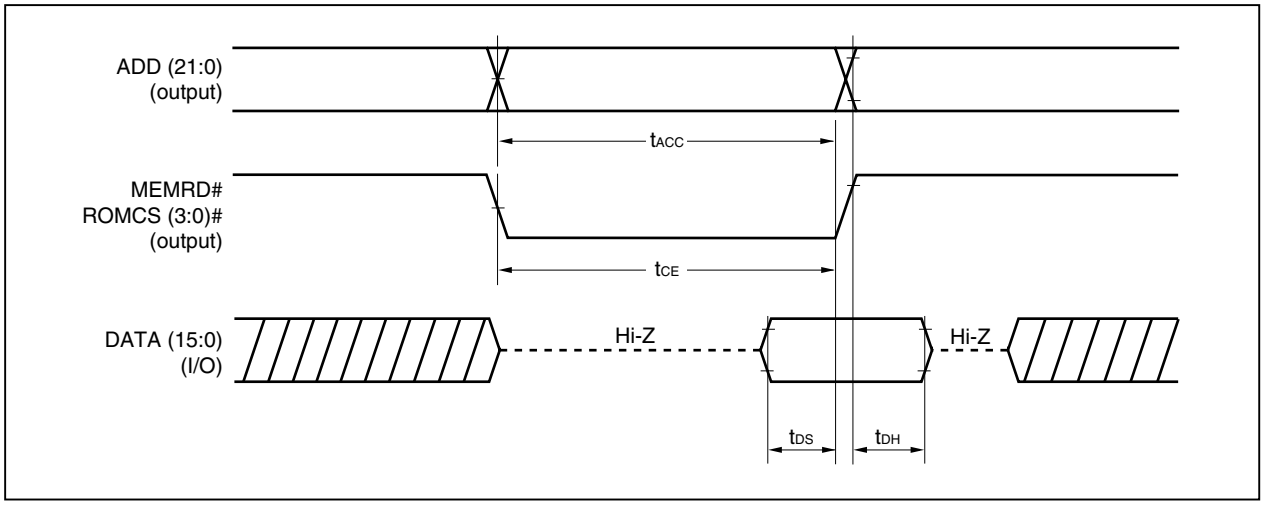
N = TClock cycle time × (WROMA (3:0) + 2)

WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
0	40	30
1	60	45
2	80	60
3	100	75
4	120	90
5	140	105
6	160	120
7	180	135

Note TClock frequency (example)

WROMA(3:0)	N (ns)	
	50 MHz[Note]	66 MHz[Note]
8	200	150
9	220	165
10	240	180
11	260	195
12	280	210
13	300	225
14	320	240
15	340	255

Note TClock frequency (example)



(14) External system bus parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Address, UBE# setup time (to command signal↓)[Note 1, 2]	t_{XAS}		S		ns
Command signal low-level width[Note 1, 2, 3]	t_{CMD}		S x W		ns
Address, UBE# hold time (from command signal↑)[Note 1, 2]	t_{XAH}		0.5S		ns
★ Command signal recovery time[Note 1]	t_{RCV}		30		ns
IORDY setup time (to SYSCLK↓)	t_{RDS}		10		ns
IORDY hold time (from command signal↑)[Note 1]	t_{RDH}		0		ns
Command signal low-level width from IORDY high level sampled[Note 1, 2]	t_{RHCH}		0.5S	1.5S	ns
Data output setup time (to command signal↓)[Note 1]	t_{WXDS}		0		ns
Data output hold time (from command signal↑)[Note 1]	t_{WXDH}		6		ns
MEMCS16#/IOCS16# setup time (to command signal↓)[Note 1]	t_{WSS}		10		ns
MEMCS16#/IOCS16# hold time (from command signal↑)[Note 1]	t_{WSH}		0		ns
Data input setup time (to command signal↑)[Note 1]	t_{RXDS}		40		ns
Data input hold time (from command signal↑)[Note 1]	t_{RXDH}		10		ns
LCDCS#, PCS(1:0)# delay time from ADD(21:0)	t_{CSD}			40	ns
LCDCS#, PCS(1:0)# setup time (to command signal↓)[Note 1]	t_{SU}		0		ns
LCDCS#, PCS(1:0)# hold time (from command signal↑)[Note 1]	t_{HD}		15		ns

Notes 1. With the V_R4181, the MEMRD#, MEMWR#, IORD#, and IOWR# are called the command signals for the External System Bus Interface.

2. S (ns) = 1000 / f_{SYSCLK}

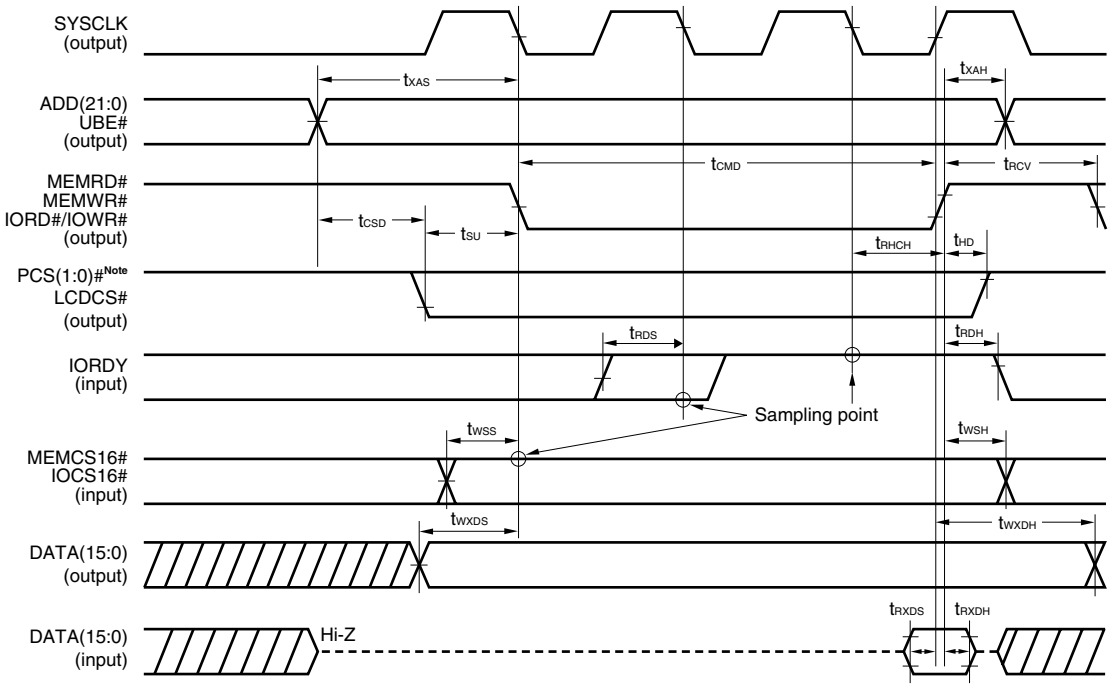
3. In External System I/O Bus Cycles, the value of W is set by using the IOWS(1:0) bits of the XISACTL register.

In External System Memory Bus Cycles, the value of W is set by using the MEMWS(1:0) bits of the XISACTL register.

★

IOWS(1:0) or MEMWS(1:0)	W
0	1.5
1	2.5
2	3.5
3	4.5

(14) External system bus parameter (2/2)



★ **Note** When PCS0MD(1:0) bits or PCS1MD(1:0) bits of the PCSMODE register are set to 01 or 10, PCS(1:0)# signals operate with the same parameters as those of MEMRD#, MEMWR#, IORD# and IOWR# signals.

(15) Keyboard interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SCANOUT(7:0) low-level width	t_{SCAN}		30.5 × K		μs
Voltage stabilization time (SCANOUTn↑→SCANOUT(n+1)↓)	t_{KWAIT}		30.5 × L		μs
Key scan interval time	t_{KI}		30.5 × (M–1)		μs
Key input delay time (from SCANOUTn↓)	t_{KS}		30.5 × (K–1)		μs
Key input hold time (from SCANOUTn↑)	t_{KH}		0		μs

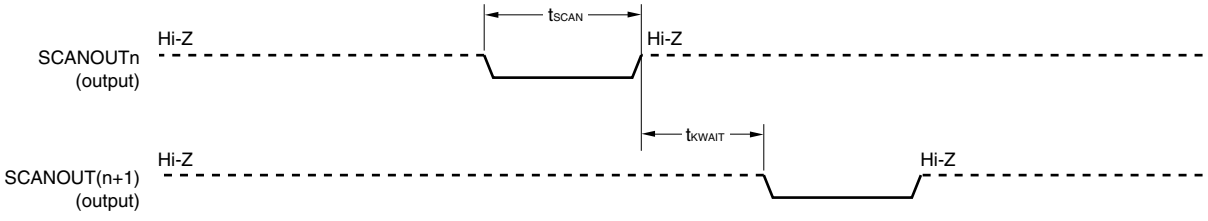
Remarks 1. K: Value set to the T1CNT(4:0) bits of the KIUWKS register

2. L: Value set to the T3CNT (4:0) bits of the KIUWKS register

3. M: Value set to the WINTVL(9:0) bits of the KIUWKI register

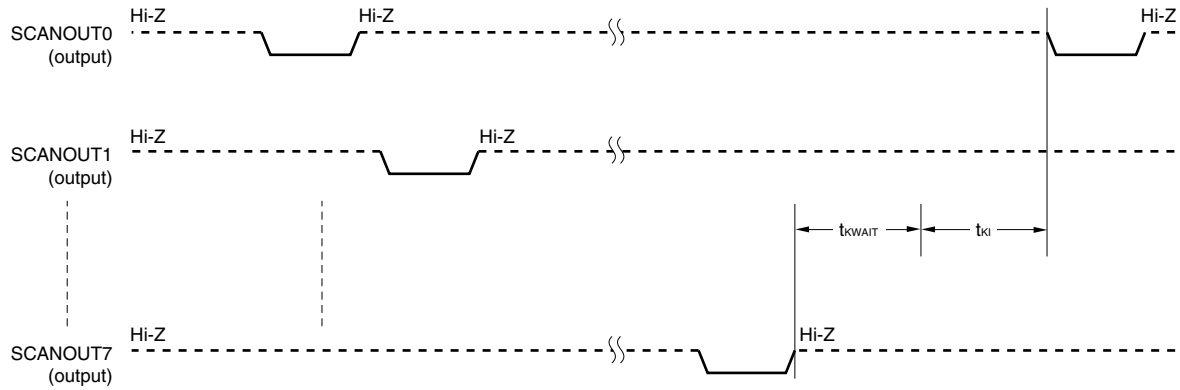
4. n = 0 to 7

(a) Keyboard scan parameter 1



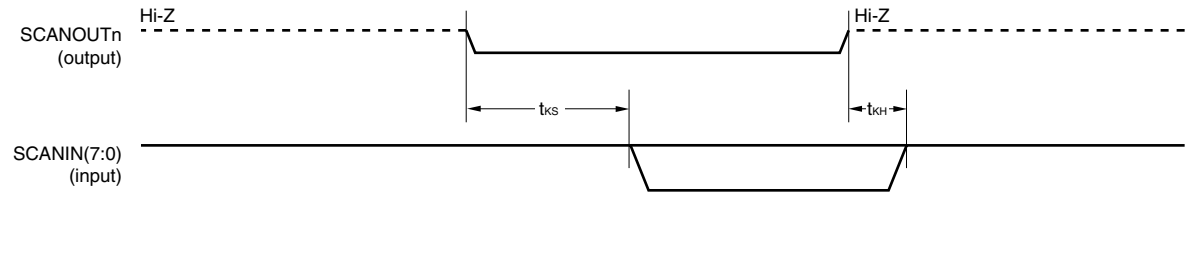
Remark n = 0 to 6

(b) Keyboard scan parameter 2



(15) Keyboard interface parameter (2/2)

(c) Keyboard port parameter



Remark n = 0 to 7

(16) Serial interface parameter (1/2)

	Parameter	Symbol	Condition	MIN.	MAX.	Unit
★	TxD1, TxD2 output pulse width[Note]	t_{TXD}		N – 0.1	N + 0.1	μs
	RxD1, RxD2 input pulse width[Note]	t_{RXD}		(9/16) × N		μs
★	IRDOUT high-level output pulse width[Note]	t_{IRDOUT}		(3/16) × N – 0.1	(3/16) × N + 0.1	μs
	IRDIN input pulse width	t_{IRDIN}		1		μs

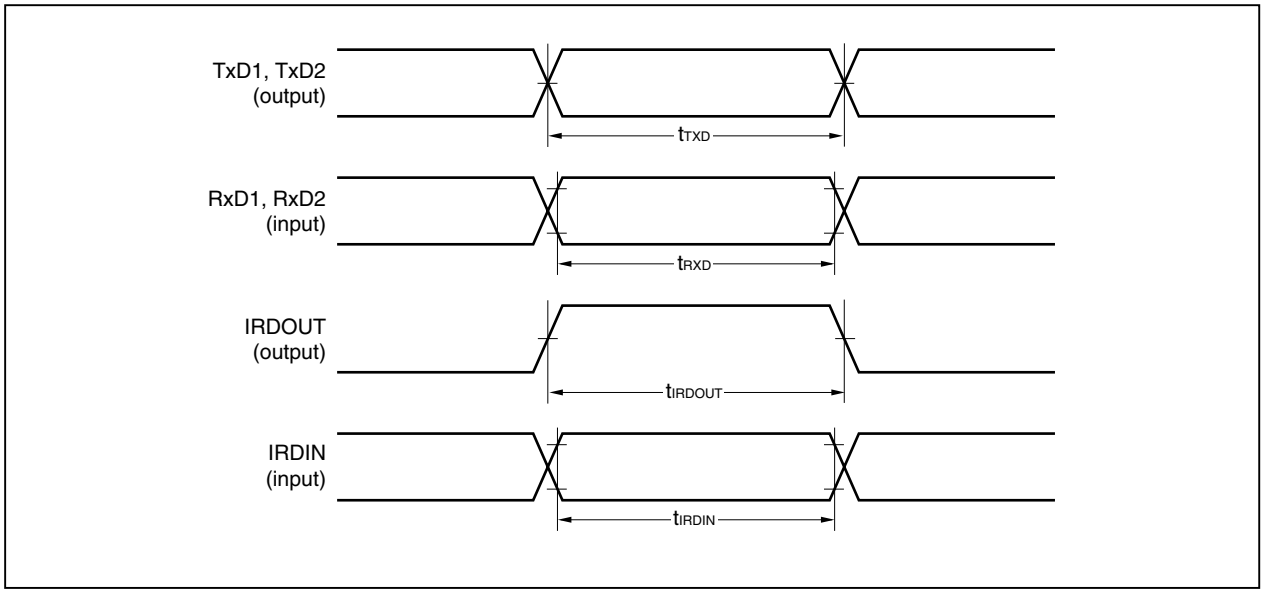
Note N: Data transfer rate per bit, which is determined by the divisor of the baud-rate generator that is set with the SIUDLL and SIUDLM registers.

★

Baud Rate (bps)	Divisor (SIUDLM, SIUDLL)	N (μs)
50	23,040	20,000.00
75	15,360	13,333.33
110	10,473	9,090.91
134.5	8,565	7,434.94
150	7,680	6,666.67
300	3,840	3,333.33
600	1,920	1,666.67
1,200	960	833.33
1,800	640	555.56
2,000	576	500.00
2,400	480	416.67
3,600	320	277.78
4,800	240	208.33
7,200	160	138.89
9,600	120	104.17
19,200	60	52.08
38,400	30	26.04
57,600	20	17.36
115,200	10	8.68
128,000	9	7.81
144,000	8	6.94
192,000	6	5.21
230,400	5	4.34
288,000	4	3.47
384,000	3	2.60
576,000	2	1.74
1,152,000	1	0.868

Remark Baud rate = (18.432 MHz/16)/(the value of SIUDLM and SIUDLL registers)

(16) Serial interface parameter (2/2)



(17) CompactFlash interface parameter (1/2)

Parameter	Symbol	Condition	MIN.	MAX.	Unit
CF_CE(2:1)#, CF_REG#, CF_DEN#, and CF_DIR delay time from ADD(10:0)	t_{CSD}			6	ns
CF_CE(2:1)# and CF_REG# setup time (to command signal↓)[Note 1, 2]	t_{SU}		2S		ns
CF_CE(2:1)# and CF_REG# hold time (from command signal↑)[Note 1, 2]	t_{HD}		0.5S		ns
Command signal low-level width[Note 1, 2, 3]	t_{CND}		S × W		ns
CF_WAIT# setup time (to SYSCLK↓)	t_{SWA}		10		ns
CF_WAIT# hold time (from SYSCLK↓)	t_{HWA}		0		ns
Data input setup time (to command signal↑)[Note 1]	t_{DIS}		20		ns
Data input hold time (from command signal↑)[Note 1]	t_{DIH}		0		ns
Data output setup time (to command signal↑)[Note 1, 2, 3]	t_{DOS}		S × W		ns
Data output hold time (from command signal↑)[Note 1]	t_{DOH}		30		ns

Notes 1. With the V_R4181, the CF_OE#, CF_WE#, CF_IOR#, and CF_IOW# are called the command signals for the CompactFlash interface.

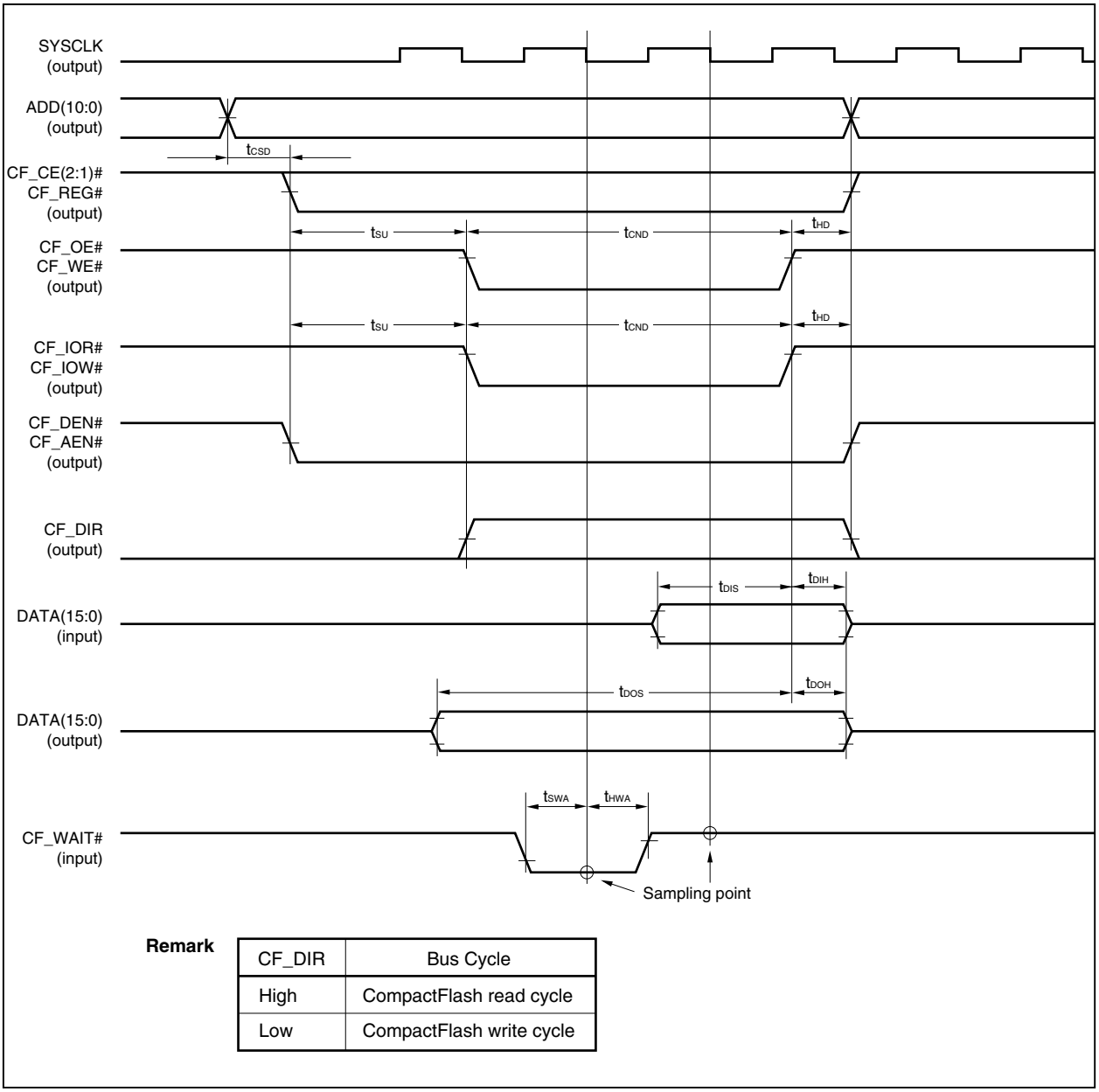
2. S (ns) = 1000/f_{SYSCLK}

3. The value of W is as follows.

★

Cycle	W
I/O card standard 8-bit Cycle	4.5
I/O card standard 16-bit Cycle	2.5
Memory card 8-bit Zero Wait State Cycle	1.5
Memory card 16-bit Zero Wait State Cycle	0.5

(17) CompactFlash interface parameter (2/2)

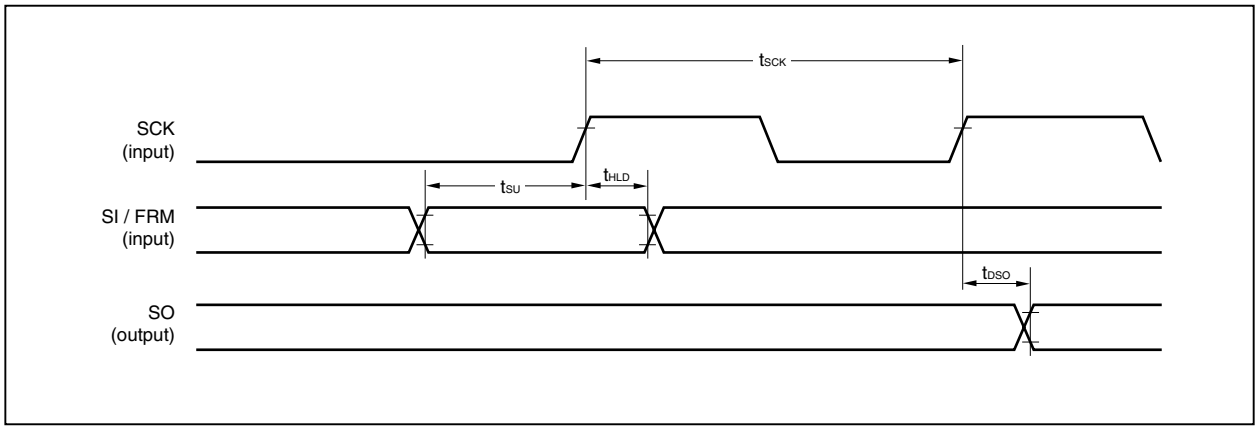


Remark

CF_DIR	Bus Cycle
High	CompactFlash read cycle
Low	CompactFlash write cycle

(18) Clocked serial interface parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
SCK pulse width	t_{SCK}		600		ns
SI / FRM setup time (to SCK↑)	t_{SU}		20		ns
SI / FRM hold time (from SCK↑)	t_{HLD}		0		ns
SO delay time from SCK	t_{DSO}			30	ns



A/D Converter Characteristics (T_A = −10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Zero-scale error[Notes 1, 2]	ZSE			±4.0		LSB
Full-scale error[Notes 1, 2]	RSE			±5.0		LSB
Integral linearity error[Notes 1, 2]	INL			±3.0		LSB
Differential linearity error[Notes 1, 2]	DNL			±3.0		LSB
Analog input voltage[Notes 1, 3]	VIAN		–0.3		AV_{DD} + 0.3	V

Notes 1. Applied to TPX (0:1), TPY (0:1), ADIN (0:2), and AUDIOIN pins.

2. Quantization error is excluded.

3. AV_{DD} is a voltage on the VDD_AD pin that is V_{DD} dedicated to the A/D converter.

D/A Converter Characteristics (T_A = −10 to +70°C, V_{DD2} = 2.3 to 2.7 V, V_{DD3} = 3.0 to 3.6 V)

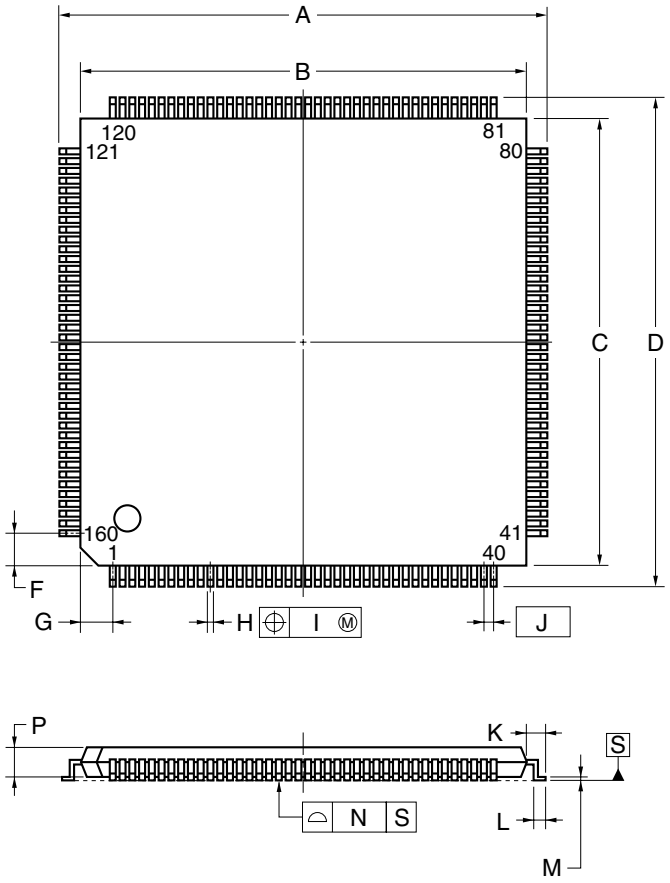
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Integral linearity error[Notes 1, 2]	INL			±3.0		LSB
Differential linearity error[Notes 1, 2]	DNL			±3.0		LSB

Notes 1. Applied to AUDIOOUT pin.

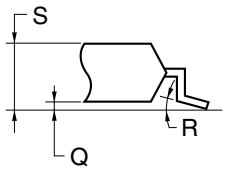
2. Quantization error is excluded.

3. PACKAGE DRAWING

160-PIN PLASTIC LQFP (FINE PITCH) (24x24)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	26.0±0.2
B	24.0±0.2
C	24.0±0.2
D	26.0±0.2
F	2.25
G	2.25
H	$0.22^{+0.05}_{-0.04}$
I	0.10
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.145^{+0.055}_{-0.045}$
N	0.10
P	1.4±0.1
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.

S160GM-50-8ED-3

4. RECOMMENDED SOLDERING CONDITIONS

The conditions listed below shall be met when soldering the μPD30181.

For details of the recommended soldering conditions, refer to our document **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case any other soldering process is used, or in case soldering is done under different conditions.

Table 4-1. Soldering Conditions for Surface-Mount Devices

Soldering Process	Soldering Conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 235°C Reflow time: 30 seconds or less (210°C or more) Maximum allowable number of reflow processes: 2 Exposure limit: 3 days[Note] (10 hours of pre-baking is required at 125°C afterward).	IR35-103-2
★ VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: 2 times max., Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours.)	VP15-103-2
Partial heating method	Terminal temperature: 300°C or less Heat time: 3 seconds or less (for one side of a device)	—

Note Maximum number of days during which the product can be stored at a temperature of 25°C and a relative humidity of 65% or less after dry-pack package is opened.

Caution Do not apply two or more different soldering methods to one chip (except for partial heating method for terminal sections).

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Related documents VR4181 User's Manual Hardware (U14272E)
VR4100 Series User's Manual Architecture (U15509E)
VR4111™ User's Manual (U13137E)

Reference document Electrical Characteristics for Microcomputer (U15170J)[Note]

Note This document number is that of the Japanese version.

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