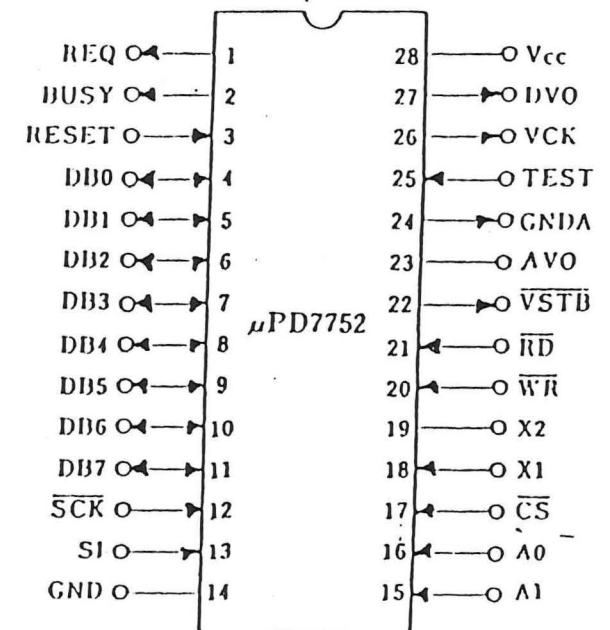# SPEECH SYNTHESIZER

µPD7752
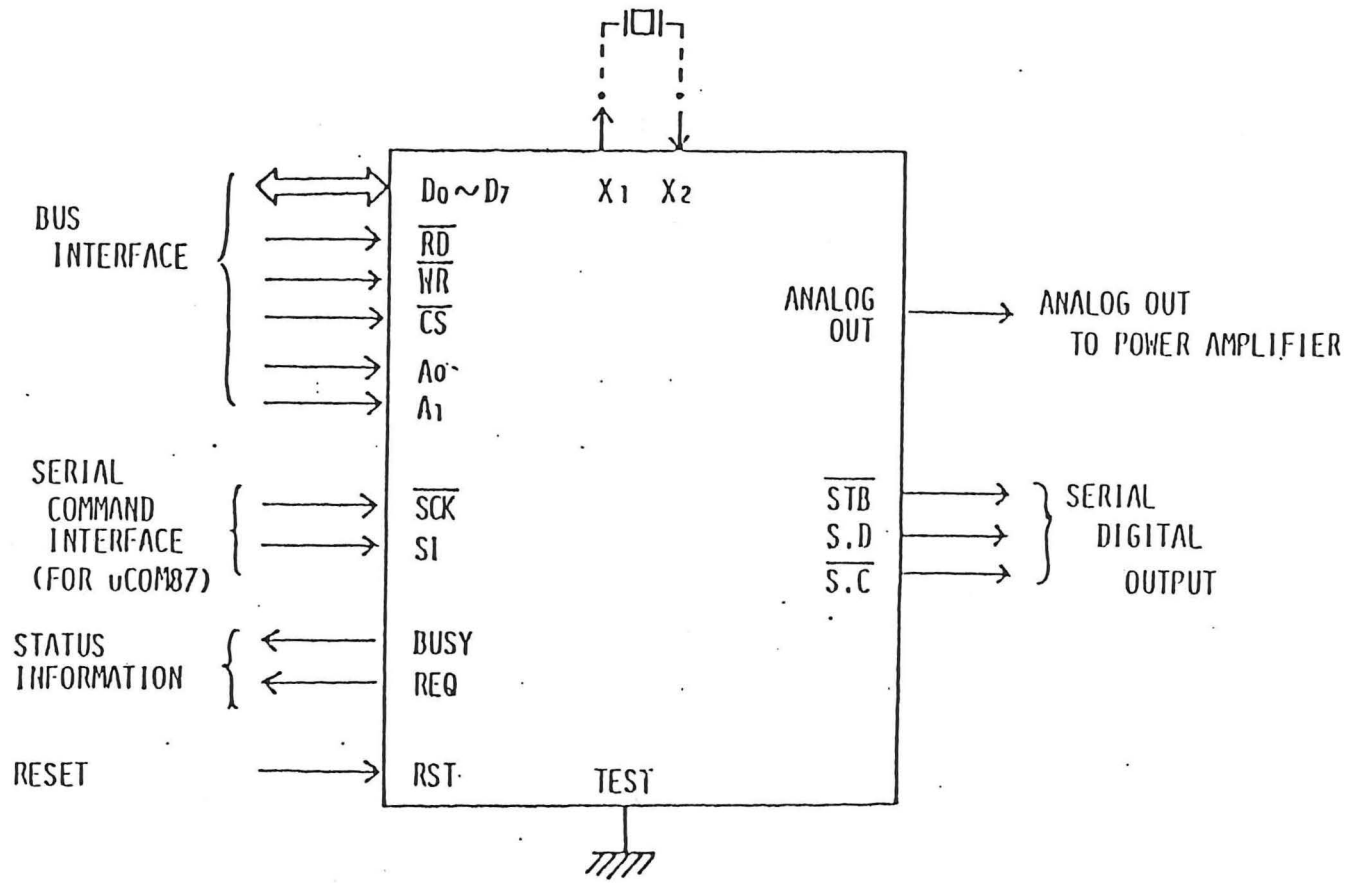
SPEECH SYNTHESIZER
(uPD7752)

FEATURES

- FORMANT TYPE SPEECH SYNTHESIZER

- VARIABLE BIT RATES   1.2 K - 5.6 K BPS

- PROGRAMMABLE SPEECH SPEED   SLOW / NORMAL / FAST

- PROGRAMMABLE FRAME PERIOD   10 MS / 20 MS

- INTERNAL DATA ROM   32 K BITS (MAX 27 S)

- MAX 63 SENTENCES   (WORDS)

- FULLY BUS COMPATIBLE WITH µPD8080

- SERIAL INTERFACE COMPATIBLE WITH µCOM87, µPD75XX

- 9 BITS DA CONVERTER ON CHIP

- 7 x 8 BITS INPUT BUFFER FOR EXTERNAL DATA MEMORY

- CLOCK GENERATOR ON CHIP (3.579545MHz)

- C-MOS SILICON GATE TECHNOLOGY

- SINGLE +5V POWER SUPPLY
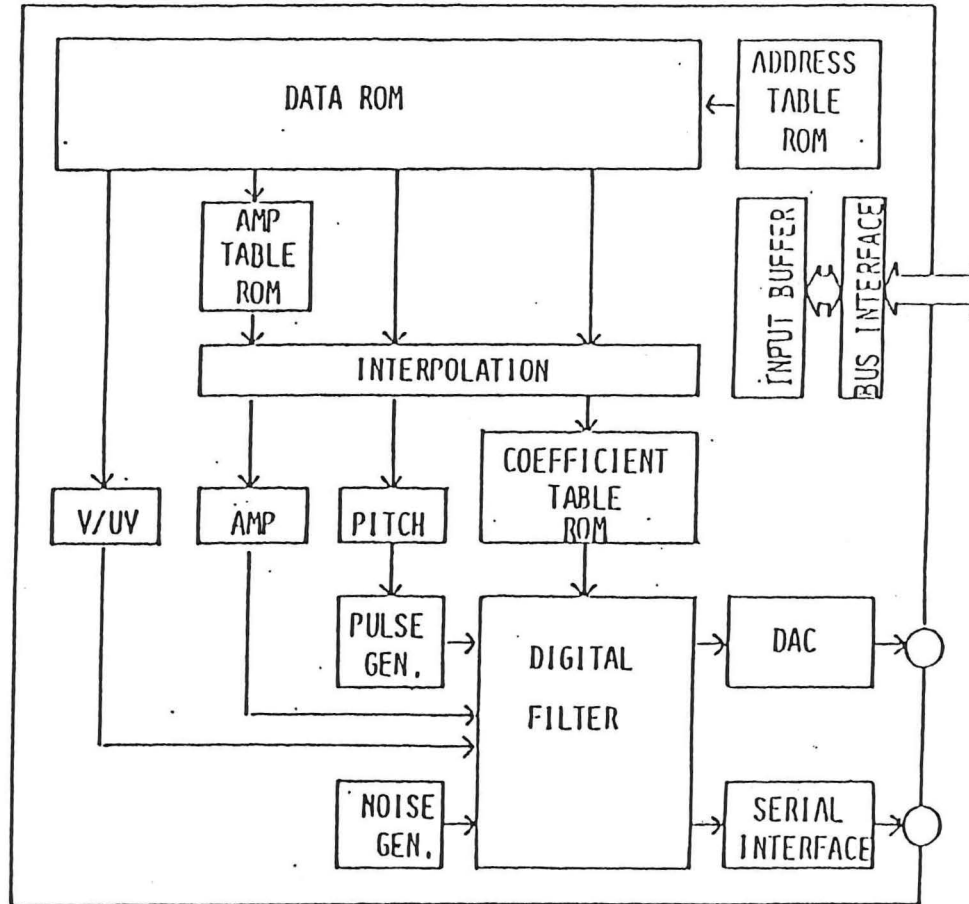
- 28 PIN DUAL IN-LINE PACKAGE
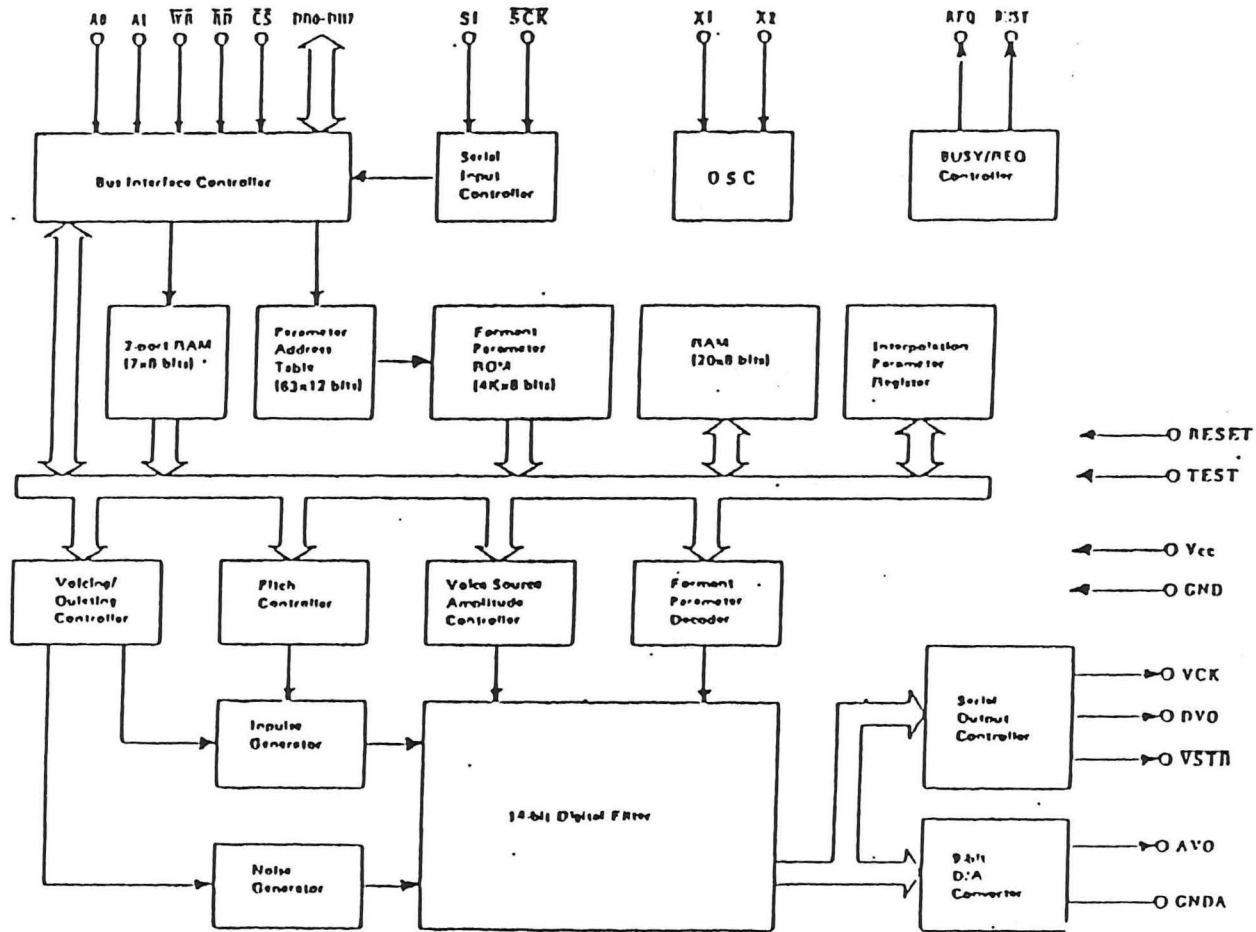
PIN CONFIGURATION
(TOP VIEW)

Pin	Signal		Signal	Pin
1	REQ		Vcc	28
2	BUSY		DVO	27
3	RESET		VCK	26
4	DB0		TEST	25
5	DB1		GNDA	24
6	DB2		AVO	23
7	DB3	µPD7752	$\overline{VSTB}$	22
8	DB4		$\overline{RD}$	21
9	DB5		$\overline{WR}$	20
10	DB6		X2	19
11	DB7		X1	18
12	$\overline{SCK}$		$\overline{CS}$	17
13	SI		A0	16
14	GND		A1	15

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PIN FUNCTION

BUS INTERFACE
- $D_0 \sim D_7$
- $\overline{RD}$
- $\overline{WR}$
- $\overline{CS}$
- A_0
- A_1

X_1 X_2

ANALOG OUT → ANALOG OUT TO POWER AMPLIFIER

SERIAL COMMAND INTERFACE (FOR uCOM87)
- $\overline{SCK}$
- SI

SERIAL DIGITAL OUTPUT
- $\overline{STB}$
- S.D
- $\overline{S.C}$

STATUS INFORMATION
- BUSY
- REQ

RESET → RST

TEST

BLOCK DIAGRAM

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Block Diagram

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FREQUENCY RESPONSE OF VOCAL TRACT

ACOUSTIC WAVEFORM

F_i: FORMANT FREQ.

B_i: BAND WIDTH

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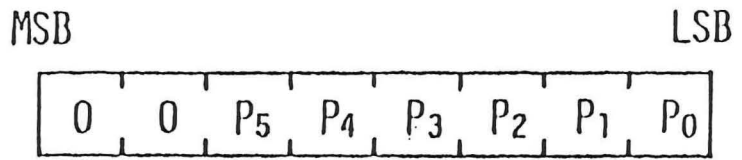
FUNDAMENTAL FORMANT TYPE SPEECH SYNTHESIS ALGORITHM

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```
         ┌──────────┐
         │  START   │
         └────┬─────┘
              ▼
      ┌───────────────┐
      │   MODE SET    │
      └───────┬───────┘
              ▼
      ┌───────────────┐
      │  COMMAND SET  │
      └───────┬───────┘
   ┌ ─ ─ ─ ─ ─┼─ ─ ─ ─ ─ ┐
              ▼
   │  ┌───────────────┐   │
      │   PARAMETER   │
   │  │   TRANSFER    │   │
      └───────┊───────┘
   │          ┊           │
              ┊
   │  ┌───────────────┐   │
      │ LAST PARAMETER│
   │  │   TRANSFER    │   │
      └───────┬───────┘
   └ ─ ─ ─ ─ ─┼─ ─ ─ ─ ─ ┘
              ▼
         ┌──────────┐
         │  STOP    │
         └──────────┘
```

SYNTHESIZING

THIS CHIP WILL AUTOMATICALLY

ISSUE THIS SEQUENCE WHEN

INTERNAL DATA ROM IS SELECTED.

8/14

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A_1 A_0 MSB   LSB

| 1 | 1 | | 0 | 0 | P_5 | P_4 | P_3 | P_2 | P_1 | P_0 | INTERNAL SENTENCE SELECTION COMMAND
$P_0 \sim P_1$ BITS SHOW SENTENCE NUMBER:

| 1 | 1 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | STOP COMMAND

| 1 | 1 | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | EXTERNAL SENTENCE SELECTION COMMAND

COMMAND   FORMAT

NEC

```
A₁  A₀        MSB                                    LSB
┌───┬───┐     ┌───┬───┬───┬───┬───┬───┬───┬───┐
│ 1 │ 0 │     │ 0 │ 0 │ 0 │ 0 │ 0 │ F │ S₁│ S₀│
└───┴───┘     └───┴───┴───┴───┴───┴───┴───┴───┘
```

F : FRAME RATE BIT

$F = 0$ 20 ms / FRAME

$F = 1$ 10 ms / FRAME

S_1, S_0 : SPEED BIT

$S_1 = 0$, $S_0 = 0$ NORMAL SPEED

$S_1 = 0$, $S_0 = 1$ SLOW

$S_1 = 1$, $S_0 = 0$ FAST

MODE FORMAT

NEC

VOICE SOURCE
MAG. TAPE

MINICOMPUTER SYSTEMS

ANALYSIS
SYNTHESIS (SIMULATION)
ENCODING FOR ROM

MONITORING
BY SIMULATION

FLOPPY DISK

MASKS
FOR ROM

PROM
FOR EVALUATION

COMPUTER ANALYSIS SYSTEMS

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SYSTEM EXAMPLE 1.

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ADDRESS

DATA ROM

D0-D7

PORT

μCOM43, 8022

ETC. PORT

SCK
SI
WR
A0
A1
BUSY
REQ

SPEECH

SYNTHESIZER

FILTER → AMP → S.P

SYSTEM EXAMPLE 3.

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SYSTEM EXAMPLE 2.

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