1. SYSTEM OVERVIEW

The OakNote™ Notebook PC subsystem is a set of highly integrated, semi-custom ICs designed from 80286 and 80386SX notebook PCs with clock speeds ranging from 8 Mhz to 20 Mhz. The subsystem consists of:

- OTI041 : System Support and Address Generation Logic
- OTI042 : I/O Control and Data Path Control Logic
- OTI043 : Flat Panel VGA Controller

The OakNote™ subsystem brings to systems designers an optimal solution for implementing a low cost and high performance PC/AT Laptop/Notebook system. To implement a full function PC/AT system, all that is required are: OTI041, OTI042, OTI043, CPU, ROM, RAM, I/O Controller, 8042 & one 7406. This system provides an amazing savings in PC board area. The OakNote™ also features a tightly-coupled video subsystem. The Flat Panel VGA Controller (OTI043) achieves the highest possible video performance by utilizing local bus architecture.

With the OakNote™ subsystem, there is no need for extensive BIOS development to implement your power management scheme. The O/S Independent Power Management Scheme and Activities Monitors, inside the subsystem, can bring the Laptop/Notebook system into power savings mode automatically without BIOS intervention.

The OTI041 integrates all the system support logic functions and address generation logic. It is implemented with 1.2 micron HCMOS technology and packaged in a 160 -pin PJQFP. The OTI041 features the following functions:

- Supports 80286 and 80386SX processors.
- Supports local bus video
- Supports local bus programmable memory range
- CPU clock control for power savings in Laptop/Notebook design
- Supports cartridge ROM
- Command state machine generates memory, I/O & Interrupt Acknowledge commands.
- Address and data path control that includes byte swapping for 16 bit to 8 bit memory or I/O devices.
- Memory controller, refresh cycle generator, EMS logic that supports EMS 4.0 specifications.
- Bus arbiter arbitrates the system bus between CPU, DMA, and DRAM refresh requests.
- Two 82C37 DMA controller running up to 8 Mhz.
- DMA support logic provides 7 channels of DMA page map address and burst mode DMA.
- Integrates all address buffers for the AT-bus.
- Supports fast reset to switch from protected mode to real mode for optimized OS/2 operations.

The OTI042 integrates peripheral devices, data and command buffers. It is implemented with a 1.2 micron HCMOS technology and packaged in a 144-pin PJQFP. The OTI042 features the following functions :

- 3 Activities Monitors for power management
- Automatic power-up functions
- Programmable bidirectional control pins
- Programmable I/O chip select pins
- 8254 compatible timer/counter
- Two 8259 compatible interrupt controllers
- Chip select logic for serial/parallel ports, disk controllers, video controller,and keyboard controller.
- Supports both 80287 & 80387SX with 80386 CPU
- Supports 80287 with 80286 CPU
- Memory parity checker & generator
- NMI generation logic
- 146818 compatible real-time clock with 128 bytes of CMOS RAM.
- Integrates all data buffers on the AT-bus.
- 82385SX support
- Optional external data buffer support

The OTI043 integrates all the key system elements for supporting a variety of flat panels on a single chip. It is implemented with a 1.0 micron HCMOS technology and packaged in a 160-pin PJQFP. The OTI043 features the following functions :

- Fully compatible to IBM VGA Hardware
- Supports CRT monitors and flat panel displays
- 800x600 resolution with 64 gray levels for flat panels and 256 colors for CRTs
- Supports 256Kx4 and 64Kx16 DRAMs
- O/S independent power management scheme
- Internal data cache
- Maximum pixel clock frequency up to 50Mhz
- Intelligent color summing and contrast adjusting logic
- Automatic video compensation logic adapts to different panel resolutions
- Integrated palette and separate LCD video timing circuit
- Local bus option with OTI40 Core Logic Subsystem

2.0 Introduction

The OTI043 is a highly integrated flat panel controller which provides a cost-effective, high performance graphics solution for notebook/laptop PCs. It supports a variety of flat panels including gas plasma, electro-luminescent(EL), and liquid crystal (LCD) displays. By integrating the key system elements on a single chip, this controller simplifies the design and reduces the implementation cost of a VGA graphics subsystem.

LCD panel displays are supported in up to 800x600 mode with 64 gray levels. Output signals for an external CRT support up to VESA-compatible 800x600 resolution with 256 colors. A flexible DRAM configuration supports both 256K x 4 and 64K x 16 DRAMs. This allows the system designer to optimize board layout to specific requirements. Utilizing 64K x 16 DRAMs can double system video performance.

Because power management is critical in notebook and laptop PCs, the OTI043 can be directly accessed by hardware to optimize system power management control. Specific sections of the controller can be disabled through various power management modes to extend battery life. Produced using 1.0u CMOS process technology, the chip itself consumes very little power.

The OTI043 provides full hardware support for context switching. All of the internal registers can be accessed for both reading and writing. There are also separate registers for flat panel control, providing fast switching between LCD and CRT displays.

An automatic video compensation feature enables the OTI043 to be used for different VGA display resolutions on a fixed size panel. Internal data caching speeds CPU access time for faster screen refreshes.

A proprietary local bus scheme enables the OTI043 to reside on the CPU bus instead of the conventional PC bus. This tightly-coupled video system increases video performance by more than 70%.

A summary of the special features provided by OTI043 is listed as follows:

- Highly integrated, single chip design
- Fully Hardware IBM VGA compatible
- Supports CRT monitors and flat panel displays
- 800x600 resolution with 64 shades of gray for flat panels and 256 colors for CRTs
- Supports 256Kx4 and 64Kx16 DRAMs
- Operating system independent power management scheme
- Internal data cache
- Maximum pixel clock frequency up to 50Mhz
- Intelligent color summing and contrast adjusting logic
- Automatic video compensation logic adapts to different panel resolutions
- Integrated palette and separate LCD video timing circuit
- Local bus option with OTI-40 Core Logic Subsystem
- 160-pin PQFP

3.0 Pin Description

Pin Name	Pin Number	Pin Type	Description
	***** CPU BUS INTERFACE *****		
AEN	TBA	I	ADDRESS ENABLE. This signal is used to qualify the video memory/IO access from CPU. When it is active high, the DMA controller has control of the address bus, data bus, and command lines.
RFSHn	TBA	I	REFRESH. This signal is used to qualify the video memory access from CPU. When it is active low, it indicate a memory refresh cycle.
IORn	TBA	I	I/O READ. This is an active low I/O read strobe, asserted in 8/16 bit I/O read cycle.
IOWn	TBA	I	I/O WRITE. This is an active low I/O write strobe, asserted in 8/16 bit I/O write cycle.
MRDn	TBA	I	MEMORY READ. This is an active low memory read strobe, asserted in 8/16 bit memory read cycle.
MWRn	TBA	I	MEMORY WRITE. This is an active low memory write strobe, asserted in 8/16 bit memory write cycle.
RSET	TBA	I	RESET. Active high system reset signal. This input signal will reset the flat panel controller and initialize the configuration register based on the logic level on BD[7:0] pins at power-up reset time. In on-board mode, this pin is connected to CPUreset and it is used to determine the phase of the processor clock.
VGARDY	TBA	O	VGA READY. An open drain active high output to signal processor that it ready for memory access. This signal is used to add wait states to bus cycle during video memory access. It is pulled low by flat panel controller right after the video memory access request by CPU to allow additional time to finish the memory cycle.
CINTn	TBA	O	CRT INTERRUPT REQUEST. An interrupt request is generated when vertical retrace occurs if it is enabled by bit 5 in the Vertical Retrace End register. It is an active low open collector output.

M16n	TBA	O	16-BIT MEMORY. It is an active low open drain output signal used to (SRDY) indicate to the system that the present data transfer is a 16-bit memory cycle. It is derived from the decode of LA17 through LA23. In local bus mode, this pin functions as an open drain active low output used to indicate the termination of a CPU bus cycle.
IO16n	TBA	O	16-BIT I/O. It is an active low open collector output signal used to indicate to the system that the present data transfer is a 16-bit I/O cycle. It is derived from an address decode.
BHEn	TBA	I	BYTE HIGH ENABLE. When the flat panel controller is in 16 bit mode, this active low signal indicates a transfer of data on the high byte of the data bus (SD[15-8]). In on-board mode, this pin is connected to the on-board byte enable.
SD[15:8]	TBA	I/O	DATA LINE 15-8. CPU data bus bit 15-8.
SD[7:0]	TBA	I/O	DATA LINE 7-0. CPU data bus bit 7-0.
SA[23:0]	TBA	I	ADDRESS LINE 23-0. In add-on card mode, SA[19:0] are connected toCPU address bus bit 19-0, SA[23:20] are connected to LA[23:20]. In local bus mode, SA[23:0] are connected to the CPU address bus.
ADS	TBA	I	ADDRESS STATUS. It indicates a validCPU bus cycl in local bus (ALE) mode. In regular on-board mode, it is used to latch valid address and decode from the microprocessor.
PROCLK	TBA	I	PROCESSOR CLOCK. In local bus mode, this pin is used to sample CPU status and address.
MIOn	TBA	I	MEMORY IO SELECT. This pin is used to distinguish between (ASEL) memory cycles and I/O cycles. In non-local bus mode, this pin acts as the address select for the controller.
WRn	TBA	I	WRITE/READ. This pin is used to distinguish between read cycles and write cycles.
DCn	TBA	I	DATA/CONTROL. This pin is used to distinguish between data cycles and control cycles.

******* BIOS ROM CONTROL *******

ROMENLn	TBA	I/O	ROM LOW BYTE ENABLE. An active low signal to enable/control the (HLDA) low byte of BIOS data to the low byte of CPU data bus in 16bit BIOS mode. This bit is not used in 8 bit mode. In local busmode, it functions as hold acknowledge signal from the CPU to indicate a DMA cyle or a master cycle.
BD[7:0]	TBA	I/O	DATA LINE 7-0. Data bit 7-0 of BIOS high byte data in 16 bit BIOS mode or single byte data in 8 bit BIOS mode. Also, data bit of DAC and dipswitch.

******* CLOCK INTERFACE *******

VCLK	TBA	I	VIDEO CLOCK. This is the master input dot clock for flat panel controller chip.
MCLK	TBA	I	MEMORY CLOCK. This is a direct input clock used for DRAM access timing.
CSEL0-1	TBA	I/O	CLOCK SELECT 0-1. Clock select line 0-1. This two pins reflect the (CLK0-1) value of the miscellaneous output register 3C3 bits 2,3. This pin can be redefined as input clocks through the status register.

******* CRT, FLAT PANEL AND RAMDAC INTERFACE *******

HSYNC	TBA	I/O	HORIZONTAL SYNC. Horizontal synchronization pulse to display monitor. The polarity of the pulse is determined by bit 6 of the Miscellaneous Output Register. (Bit 7 of 3DF index 12.)
VSYNC	TBA	I/O	VERTICAL SYNC. Vertical synchronization pulse to display monitor. The polarity of the pulse is determined by bit 7 of the Miscellaneous Output Register. (Bit 6 of 3DF index 12.)
BLANKn	TBA	O	BLANK. Active low output signal to RAMDAC to blank the pixel data or the display monitor.
P[7:0]	TBA	O	PIXEL DATA. Pixel data bit 7-0, output to external color palette for color mapping during CRT display. It also output to the flat panel as the display data.

FRAME	TBA	O	FRAME. Active high output signal to the flat panel. It will go active every other frame.
SHFCK	TBA	O	SHIFT CLOCK. Clock output to flat panel to latch the pixel data P7-P0. It is derived from the internal character clock.
LP	TBA	O	LOAD PULSE. An active high output signal to the flat panel to latch the data from the panel's internal shift register.
FSYNC	TBA	O	FRAME SYNC. Frame synchronization pulse to the flat panel.
WGTCK/DE	TBA	O	WEIGHT CLOCK or DISPLAY ENABLE. An active high output signal. Reference clock for the pulse width modulation to achieve different grayscale. It also redefined as display enable and will go active during display time.
DACRDn	TBA	O	RAMDAC READ. An active low I/O read signal generated for reading external color palette registers.
DACWn	TBA	O	RAMDAC WRITE. An active low I/O write signal generated for writing external color palette registers.
PCLK	TBA	O	PIXEL CLOCK. Pixel clock output to DAC to latch the pixel data P7-P0. It is derived from the current dot clock rate of operating mode.

******* VIDEO MEMORY INTERFACE *******

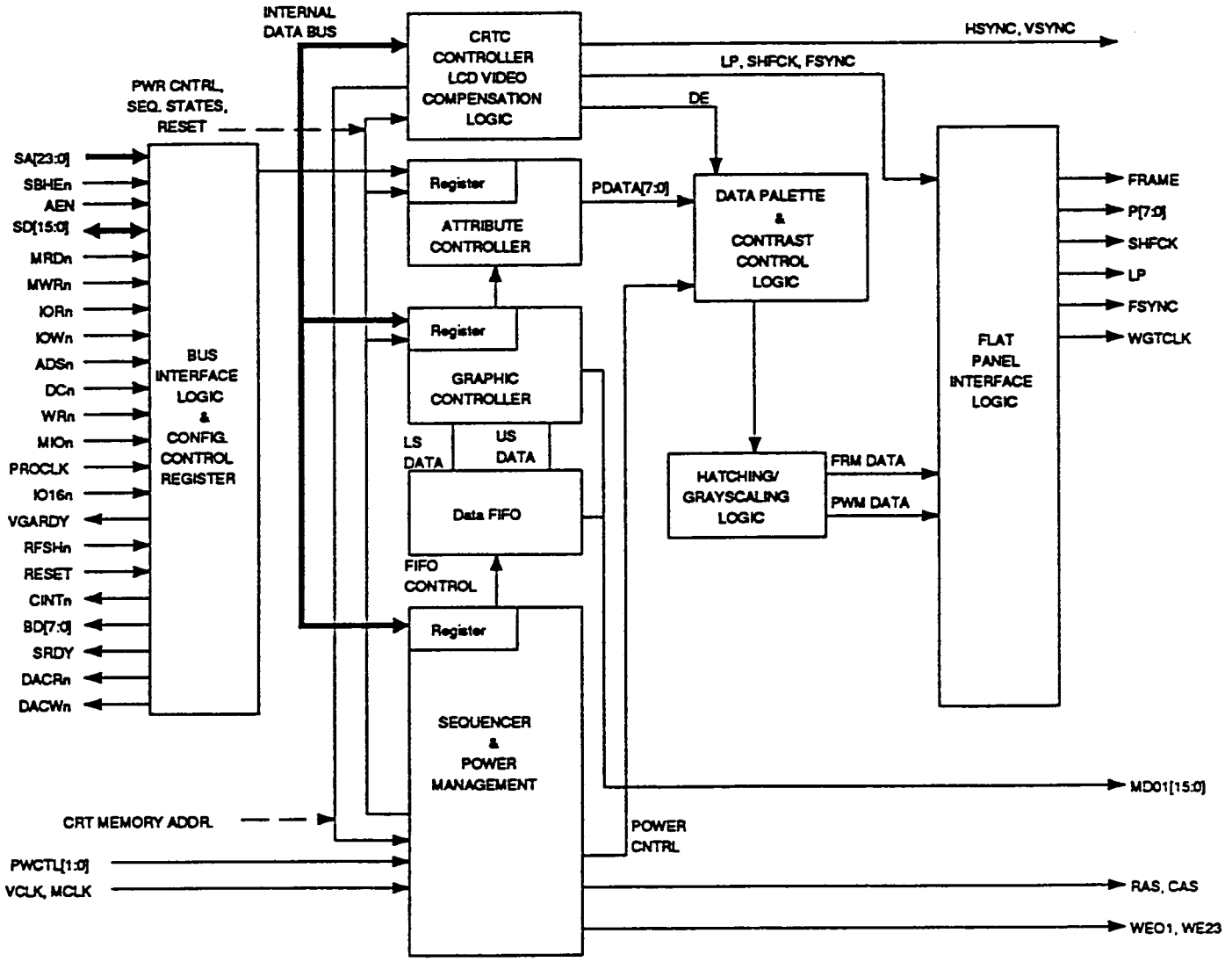
MA01[7:0]	TBA	O	MEMORY ADDRESS. Memory address line 0-7 for memory maps 0, 1.
MA23[7:0]	TBA	O	MEMORY ADDRESS. Memory address line 0-7 for memory maps 2, 3.
MD01[15:0]	TBA	I/O	MEMORY DATA. Memory data line 15-0 for map 0,1. In 64Kx16 DRAM configuration, these are the memory data bits 0-15 for maps 0,1.With 2 DRAMS (256Kx4) bits 0-3 are for maps 0, 1 and bits 4-7 are for maps 2, 3. With 4 DRAMS (256Kx4) bits 0-3, 8-11 are for maps 0, 1 and bits 4-7, 12-15 are for maps 2, 3.
MD23[15:0]	TBA	I/O	MEMORY DATA. Memory data line 15-0 for map 2,3. In 64K x16 DRAM configuration, these bits are used as the

			memory data bits 0-15 for maps 2,3. In 256x4 DRAM configuration, these bits are not used.
RASn	TBA	O	ROW ADDRESS STROBE. Active low output signal to all video memory maps.
CASAn	TBA	O	COLUMN ADDRESS STROBE. Active low output signal to all video memory maps.
CASBn	TBA	O	COLUMN ADDRESS STROBE. Active low output signal bank B video memory maps in 64Kx16 DRAM configuration .
WE01n	TBA	O	WRITE ENABLE. Active low write enable pulse to memory map 0 and 1in 256Kx4 DRAM configuration. Active low write enable pulse to memory map 0 in 64Kx4 DRAM configuration.
WE23n	TBA	O	WRITE ENABLE. Active low write enable pulse to memory map 2 and 3 in 256Kx4 DRAM configuration. Active low write enable pulse to memory map 2 in 64Kx4 DRAM configuration.
MA/WE01Hn	TBA	O	MEMORY ADDRESS BIT 8 for maps 0,1 in 256Kx4 DRAM configuration. WRITE ENABLE for map1in 64Kx16 DRAM configuration.
MA/WE23Hn	TBA	O	MEMORY ADDRESS BIT 8 for maps 2,3 in 256Kx4 DRAM configuration. WRITE ENABLE for map 3 in 64Kx16 DRAM configuration.

******* MISCELLANEOUS *******

SWSENSE	TBA	I	SWITCH SENSE. An input signal used to auto detect the monitor type.
PWCTL[1:0]	TBA	I	POWER CONTROL. These 2 bit is used to indicate various modes of power saving.

4.0 Chip Block Diagram



5.0 Features

CPU Interface

The OTI-043 can support three different types of bus interfaces, the on-board local bus VGA, the on-board pc-bus VGA and the add-on VGA. Among the three different interfaces, the local bus delivers the highest performance because the local bus has much higher bandwidth than the PC-bus. The local bus VGA operates together with the OTI-041 and OTI-042 (or chip sets confront to the OTI-040 local bus standard) to form a tightly coupled system. For system chip sets from other manufacturers, the OTI-043 will be configured as either an on-board pc-bus VGA or as an add-on VGA. In the add-on VGA implementation, both 8 bits and 16 bits PC-bus are supported. All the necessary CPU control signals, address decode and buffer controls are integrated into the OTI-067 to minimize external circuit complexity and parts count. A sixteen bit data path for I/O, display memory, and BIOS ROM is supported. Special I/O ports; 46E8H for setup and 102H for VGA enable; are implemented internally to the OTI-043 to achieve complete IBM VGA display adapter compatibility.

Display Memory

The OTI-043 supports both 64Kx16 DRAM and 256Kx4 DRAM in all video modes. It supports 256 KBytes of DRAM by using two 64Kx16 or 256Kx4 DRAM chips; 512 KBytes of DRAM by using four 64Kx16 or 256Kx4 DRAM chips. The OTI-067 provides all the necessary control signals and address/data lines to access the video memory in page mode. For a 45 Mhz memory clock, DRAMS with an access speed of 80 ns are required, 70ns DRAMS are required for a 50Mhz memory clock.
In extended modes with 256 colors, the video memory is organized in a packed pixel mode; 1 byte from 1 plane as a pixel. This requires programming of an OTI extended register and requires 512 KBytes of DRAM. For 16 color extended modes, the video memory is organized as planar mode (1 bit from each of 4 planes) which is compatible with the IBM 16 color graphics mode. All the extended graphics mode programming is compatible with the OTI-067.

CLOCK INTERFACE

Up to 4 external clock frequencies can be selected by two clock select pins. The memory clock is continuous free running and therefore is not a selectable frequency.
The OTI-043 can support either a clock oscillator or a frequency synthesizer as clock sources. An external multiplexer is required if clock oscillators are used as the clock source instead of the frequency synthesizer. The synthesizer can generate all of the required clock frequencies to support all OTI-043 video modes.

Video Compensation

This feature increases the usable display area and also improves the appearance of display area smaller than the panel size. Flat panel is a fixed resolution device, the display of lower resolution video modes will not be able to fill the panel completely. The flat panel controller provides various compensation modes to

improve the appearance of the display. The controller can be programmed to automatically center the display leaving the border evenly in both vertical and horizontal direction. It can also be programmed to duplicate the previous scan line for N lines at a fixed interval M so that the unused display area is filled. This insertion mechanism applies to the vertical direction only. The third mode of operation is blank line insertion. This mode is especially useful in text mode where deformation of characters is undesirable. N blank lines are inserted at M lines interval, where M is the same as the number of lines per character.

Operating System Independence

The OTI-043 is designed to operate in different O/S environments. The controller re-interpretes the definition of the VGA registers when it is in the flat panel mode. No system traps (NMIs) will be generated from the OTI-043 for software emulation purpose. There are two general purpose PIO ports available in the OTI-043 for system use. They may be used in controlling the DISPOFF signal available in some of the LCD panel to prevent DC voltage accumulation. They can also be used as the signal to indicate the presence of a analog monitor so that the system can automatically use the CRT as its primary display.

Intelligent Color Mapping and Contrast Control

The color mapping logic performs color summing with programmable coefficient and stores the result into the internal color mapper. The programmable color summing scheme enables the display of image that is not color balanced. For example, if the display is mostly composed of blue color, the differentiation between different intensities of blue will not be sufficient. The use of a different weighting scheme will improves the contrast between different level of blue color. The default summing coefficient is the same as that defined by NTSC. (Gray intensity = 0.3 of red + 0.59 of green + 0.11 of blue).

The color mapper can also be programmed to take advantage of the characteristic of the human eyes. The human eye is sensitive to the relative intensity level rather than their absolute values. Our eyes perceive the difference between an intensity of 0.1 and 0.11 the same as that of 0.5 and 0.55. A mapping that maps the 256 colors into 64 gray level linearly does not yield the best display contrast. The contrast control logic is used to optimize the contrast between foreground and background display during text mode operation. The number of gray levels difference between the foreground and background can be programmed. This feature enables the user to easily distinguish the attributes of application using multiple colors in text mode.

Power Management Control

The OTI-043 supports various of power management mode through both the power control pins or register programming. The various power saving mode are listed below:

Shutdown mode

This mode is activated by pulling the PWCTL[1] and PWCTL[0] pins low or through the programming of the power control registers. This mode is used to reduce the power consumption of the display system by shutting down the LCD VGA. All the control signals to the flat panel are forced to their inactive states and the panel should be turned off. The video RAM is not refreshed in this mode so the content of the display memory is lost. When the controller wake up from this mode, CPU needed to reload the video memory but the register state of the controller will stay in the same mode before the shut down. This mode can be used in conjunction with the shutdown mode of OTI040 where the CPU is stopped, and it will be reset when it wakes up.

Sleep mode
In this mode, the content of the video memory will be preserved but there will be no display output. The video pipeline of the OTI043 is completely turn off. Only portion of the sequencer is active to perform the refresh operation at a programmable rate.

Normal mode
This is the normal operating mode of the LCD controller. All the registers and video memory can be accessed. The video DRAM is refreshed at the normal rate.

The operation of the LCD controller is also effected by the programming of some the VGA registers. When the asynchronous reset bit, synchronous reset bit, the sequencer, the CRTC and the video pipeline is disabled to conserve power. When the screen off bit is active, the whole video pipeline will be turned off.

6.0 FUNCTIONAL DESCRIPTION

As shown in the system block diagram, the OTI-043 LCD VGA graphics controller consists of eight major functional blocks:

- Color mapper
- Grayscaling logic
- Flat panel interface
- CRT controller (CRTC)
- Attribute controller
- Graphics controller
- Sequencer
- Bus interface

Color mapper

The color-mapper acts as a lookup table for the color display to monochrome display conversion. Color summing is done automatically by the hardware, and the coefficient for the red, green and blue color can be programmed. The mapped pixel values are send to the grayscaling logic for display.

Grayscaling Logic

The grayscaling logic modulates the pixel data on a frame by frame basis to generate different level of gray shading. The modulation algorithm can be programmed to adapt to panels from different manufacturers.

Flat Panel Interface

The flat panel interface logic provides all the necessary interface signals for single drive, dual drive monochrome LCD panels, EL panels and gas plasma display. The panel interface supports 8 bit wide pixel format, and the polarity and pulse width of the panel control signal is programmable through the OTI extension registers.

CRT Controller

The CRTC generates horizontal and vertical timing signals, addresses for the dynamic RAM display buffer, and cursor and underline timing signals for both the flat panel display and CRT display. The CRTC supports dual panel without the use of external frame buffer.

Attribute Controller

The attribute controller receives video memory data from the graphics controller and formats the data for display. The attribute controller also controls blinking, underlining, cursor insertion, and pixel (bit) panning.

Graphics Controller

This section controls the data flow between the display memory and the attribute controller during the active display period. In addition, it supports data flow between the host processor and the display memory. During the active display time, memory data is fetched from memory to fill the FIFO which is then used to supply data to the attribute controller as required. The graphics controller support 8bits, 16bits or 32bits memory data path depending on the memory configuration. In APA (All-Points-Addressable) modes, sometimes referred to as graphics mode, parallel memory data is converted to serial bit-plane data before sending it to the attribute controller. In A/N (Alphanumeric) modes, the parallel memory data is sent to the attribute controller without conversion. During video memory read or write operations, the graphics controller can perform logical operations on the parallel memory data.

Sequencer

The sequencer generates basic DRAM timing signals and all clock and reset signals. It also arbitrates access to video memory between the system microprocessor and the CRTC during active display intervals by inserting system microprocessor memory cycles between display memory cycles, and provides memory mapping of the video memory. Map mask registers can be used to protect entire memory maps from being altered.

Bus Interface

The bus interface decodes memory addresses and I/O addresses to the video memory or VGA registers, generates all handshake signals to the system microprocessor. It supports a proprietary local bus which delivers 70% increase in performance when operated with the OTI040 system.