AN8812SC, AN8812SCR

4ch. Linear Driver IC for CD/CD-ROM

■ Overview

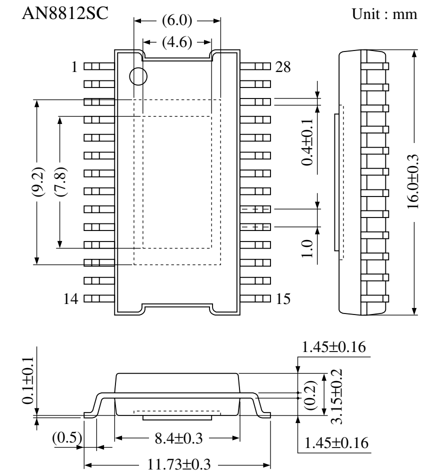
The AN8812SC and AN8812SCR are 4ch. drivers using the power operational-amplifier method. They employ the surface mounting type package superior in radiation characteristics.

■ Features

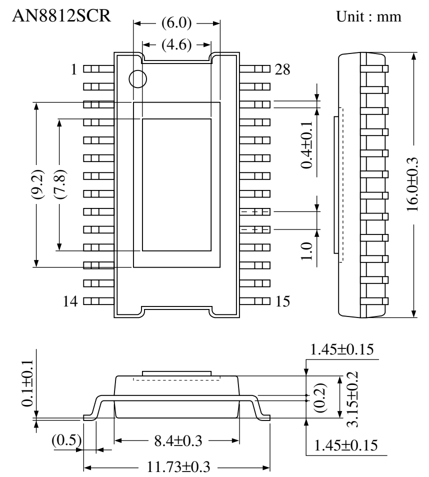
- Wide output D-range is available regardless of reference voltage on the system
- Setting of driver input/output gain enabled by external resistance
- 2ch. independently controllable PC (Power Cut) feature built-in
- Thermal shut down circuit (with hysteresis) built-in
- Proper heat of IC controllable by separating the output supply and setting each independently for 2ch.
- Construction of 5V supply enabled by external PNP Tr
- Accessary operational amplifier built in
- Relatively easy pattern design by separating and concentrating the input line and output line

■ Application

Actuator for CD/CD-ROM, motor driver

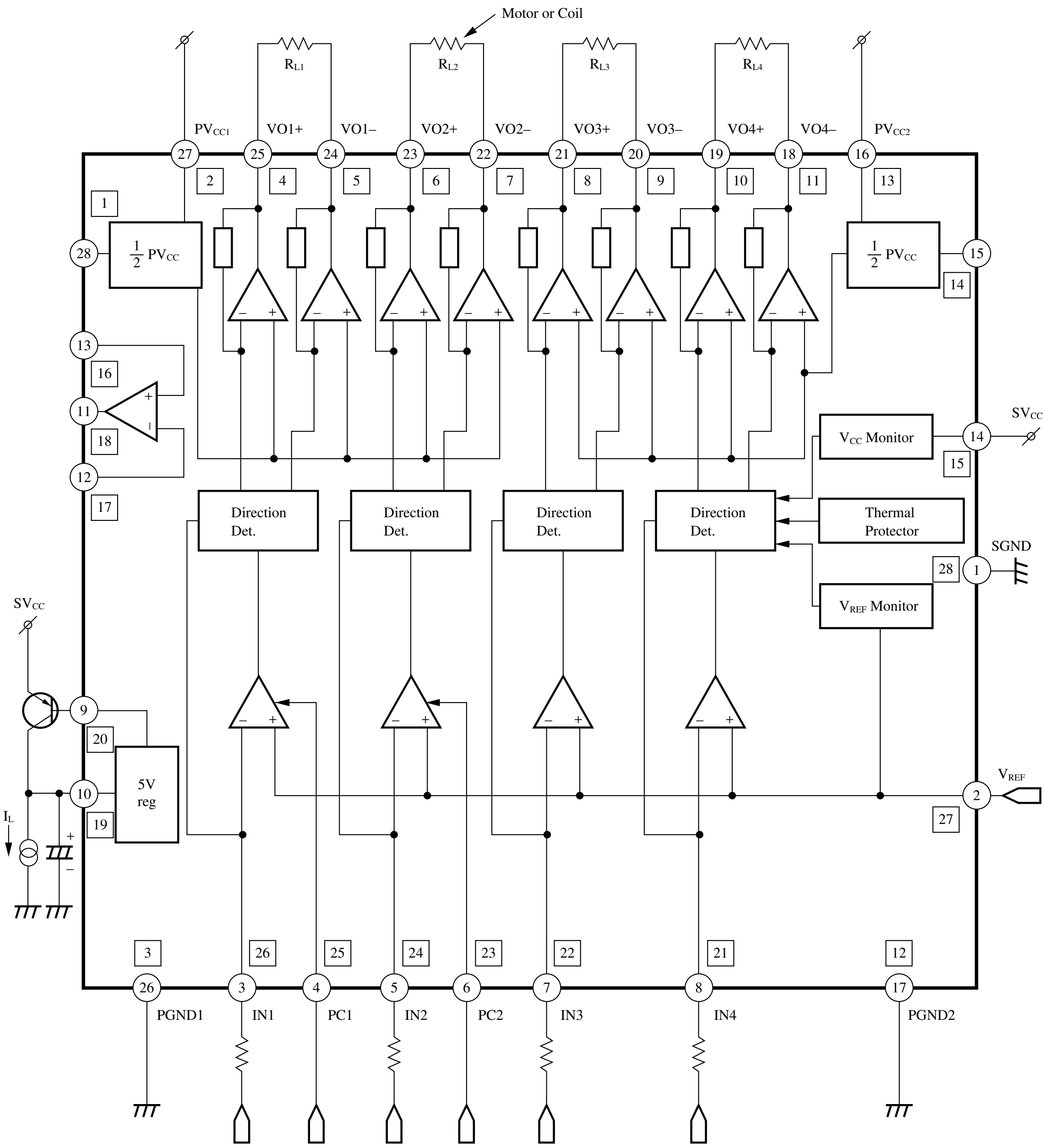


Fin-attached 28-lead SOP package (HSOP028-P-0450)



Fin-attached 28-lead SOP package (SOP028-P-0450)

■ Block Diagram



Pin No. in a circle, ◯ is for AN8812SC
Pin No. in a square, □ is for AN8812SCR

■ Absolute Maximum Ratings (Ta=25˚C)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	18	V
Supply Curren	I_{CC}	—	mA
Power Dissipation Note)	P_D	2083	mW
Operating Ambient Temperature	T_{opr}	–30 ~ + 85	˚C
Storage Temperature	T_{stg}	–55 ~ + 150	˚C

Note) For surface mounting on 50 × 50 × 1.2mm glass epoxy board

■ Recommended Operating Range (Ta=25˚C)

Parameter	Symbol	Range
Operating Supply Voltage Range	SV_{CC} Note)	5.5V ~ 14V
	PV_{CC1}, PV_{CC2}	

Note) Set SV_{CC} to the maximum electric potential.

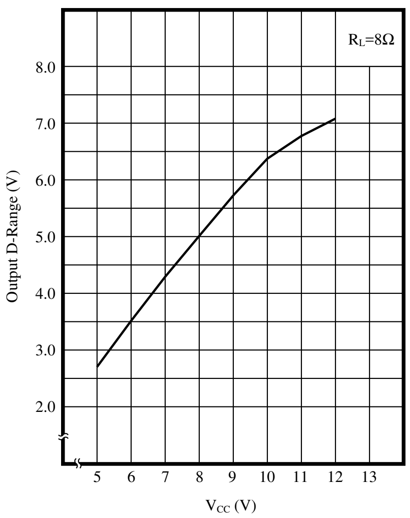
■ Electrical Characteristics (Ta=25˚C)

Parameter	Symbol	Condition	min.	typ.	max.	Unit
No Load Consumption Current	I_{tot}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	5	10	15	mA
Drivers 1 to 4						
Input Offset Voltage	V_{IOF}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$ $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	–10	—	10	mV
Output Offset Voltage	V_{OOF}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$ $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	–50	—	50	mV
Gain	G	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$ $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	18	20	22	dB
Maximum Output Amplitude (+)	V_{L+}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$ $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	4.4	5.0	—	V
Maximum Output Amplitude (–)	V_{L-}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$ $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	—	–5.0	–4.4	V
Threshold H	V_{PCH}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$ $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	2.0	—	—	V
Threshold L	V_{PCL}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$ $R_L = 8\Omega$, $R_{IN} = 10k\Omega$	—	—	0.3	V
Reset circuit						
Reset Operation Release Supply Voltage	V_{RST}	$I_{IN} = 10\mu A$, $R_{IN} = 10k\Omega$	3.0	3.2	3.3	V
V_{REF} Detection	V_{REF}		2.0	—	—	V
5 V Regulator						
Output Voltage	V_{REG}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	4.75	5.0	5.25	V
Output Load Fluctuation	DV_R	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	–50	—	50	mV
Supply Voltage Fluctuation	DV_V	$PV_{CC1} = PV_{CC2} = SV_{CC}$ $= 8V \sim 12V$	–5	—	5	mV
OP Amp.						
Input Offset Voltage	V_{OF}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	–5	—	5	mV
Input Bias Current	I_{BOP}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	—	150	500	nA
High-Level Output Voltage	V_{OH}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	6.0	—	—	V
Low-Level Output Voltage	V_{OL}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	—	—	1.7	V
Output Drive Current Sink	I_{SIN}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	2.0	—	—	mA
Output Drive Current Source	I_{SOU}	$PV_{CC1} = PV_{CC2} = SV_{CC} = 8V$	2.0	—	—	mA
Heat Protection Circuit						
Operation Temperature Equilibrium Value Note)	T_{THD}		(—)	(180)	(—)	˚C
Operation Temperature Hysteresis Width Note)	DT_{THD}		(—)	(45)	(—)	˚C

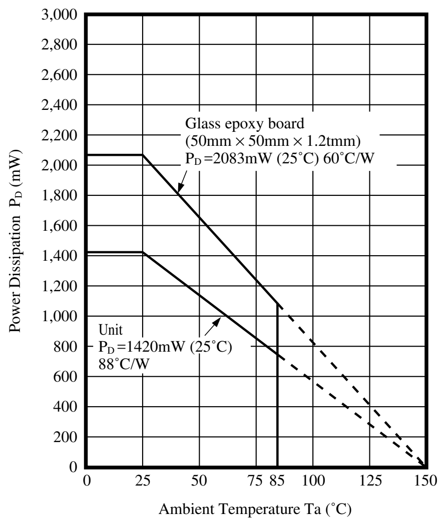
Note 1) Characteristic value in parentheses is a reference value for design but not a guaranteed value.

■ Characteristic Curve

V_{CC} – Maximum Output Amplitude Characteristics



P_D–Ta



■ Description for Use

(Pin No. in the following text are for the AN8812SC. For the AN8812SCR, refer to the block diagram.)

• Driver Portion

Calculate the driver gain by using the following formula for setting.

$$G = \frac{60k\Omega}{R_{IN1}+100\ (\Omega)} \times 2$$

The power supply for Ch.1 and 2 is supplied from Pin27 and the power supply for Ch.3 and 4 is supplied from Pin16 independently.

Output amplitude is increased by increasing the supply voltage. Set the power supply voltage as necessary. However, always set Pin 14 of V_{CC} to the maximum electric potential.

Pins15 and 28 may require a capacitor for ripple removal.

As protection functions, V_{CC} reset circuit, V_{REF} detector and heat protection circuit are incorporated.

The V_{CC} reset circuit operates at approx. 3V and is released at 3.2V, when the supply (Pin14) decreases. For the V_{REF} detector, the protection function works at approx. 1V (max. 2V).

Also, the set temperature for operation of the heat protection circuit is approx. 180°C.

In Ch.1 and 2, independently controllable PC (Power Cut) functions are incorporated respectively.

• 5V Supply

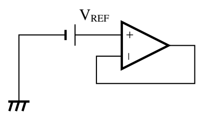
By adding the external PNP transistor, 5V regulator can be constructed. Attach an external capacitor for loop filter to Output Pin10.

In Pin9, the base current limiting circuit (typ. 10mA) is incorporated.

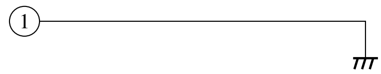
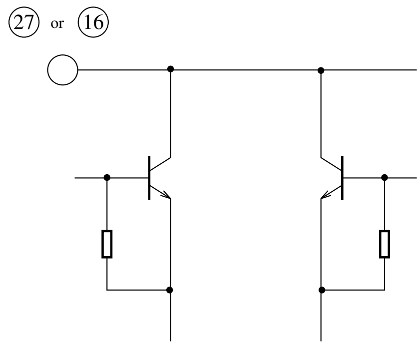
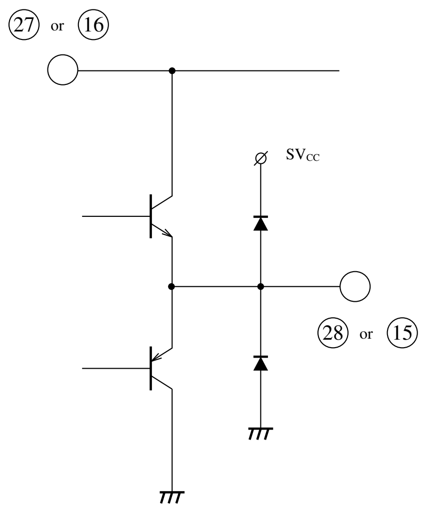
When 5V supply is used, the external PNP Tr emitter must be connected to Pin14 (V_{CC} pin).

• Operational Amplifier

When the operational amplifier is not used, make connection as follows :

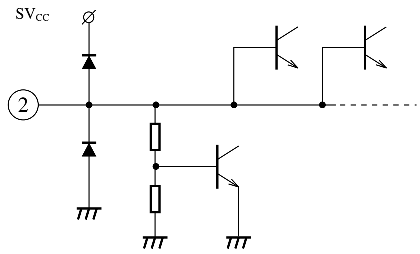
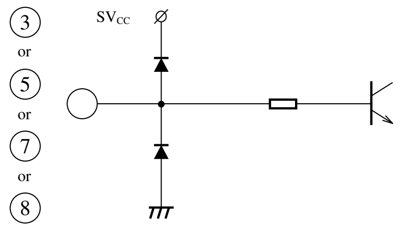
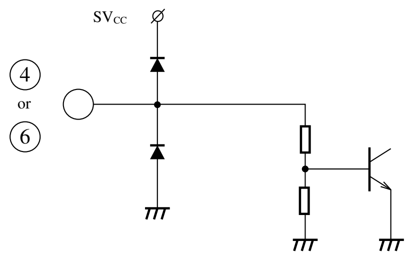
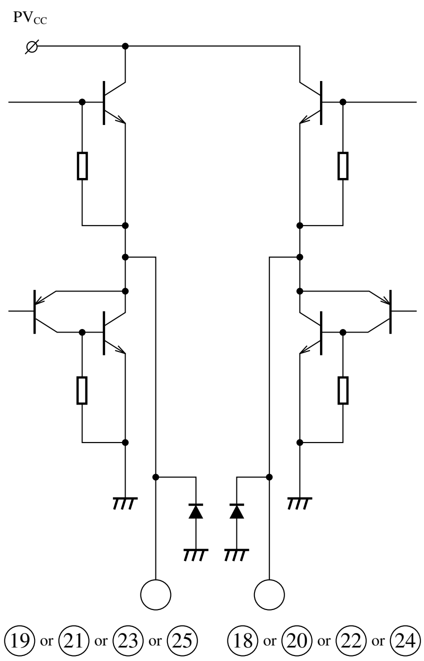


■ Pin Description

Pin No. AN8812SC	Pin No. AN8812SCR	Symbol	I/O	Pin Description	Equivalent Circuit
1	28	SGND	—	SGND pin for driver control circuit	
27	2	$PV_{CC}1$	—	Power V_{CC} pin supplying the current flowing in output power transistors, 22, 23, 24 and 25	
16	13	$PV_{CC}2$	—	Power V_{CC} pin supplying the current flowing in output power transistors, 18, 19, 20 and 21	
26	3	PGND1	—	GND pin for output transistors, 22, 23, 24 and 25	
17	12	PGND2	—	GND pin for output transistors, 18, 19, 20 and 21	
28	1	$\frac{1}{2}$ $PV_{CC}1$	O	$\frac{1}{2}$ PV_{CC} output pin 1	
15	14	$\frac{1}{2}$ $PV_{CC}2$	O	$\frac{1}{2}$ PV_{CC} output pin 2	

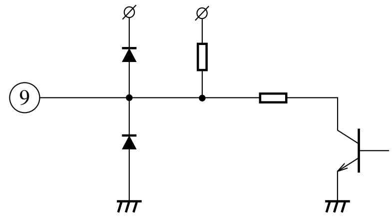
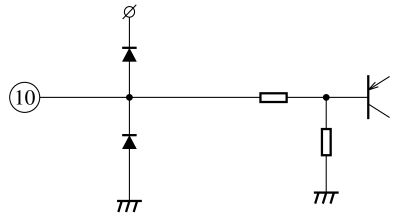
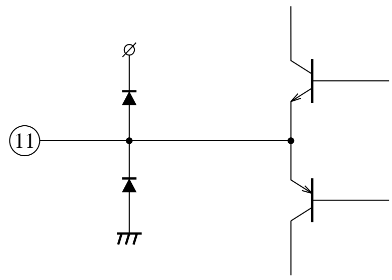
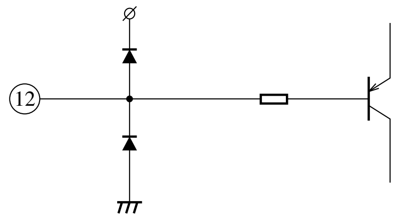
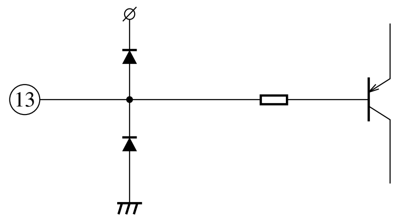
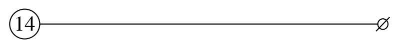
Note) Pin No. shown in the equivalent circuit diagram are only for the AN8812SC. For the AN8812SCR, they must be replaced.

■ Pin Description

Pin No. AN8812SC	Pin No. AN8812SCR	Symbol	I/O	Pin Description	Equivalent Circuit
2	27	V_{REF}	I	V_{REF} input pin	
3	26	IN1	I	Input pin of Driver 1	
5	24	IN2	I	Input pin of Driver 2	
7	22	IN3	I	Input pin of Driver 3	
8	21	IN4	I	Input pin of Driver 1	
4	25	PC1	I	Power cut input pin of Driver 1	
6	23	PC2	I	Power cut input pin of Driver 2	
18	11	VO4–	O	Reverse rotation output pin of Driver 4	
19	10	VO4+	O	Normal rotation output pin of Driver 4	
20	9	VO3–	O	Reverse rotation output pin of Driver 3	
21	8	VO3+	O	Normal rotation output pin of Driver 3	
22	7	VO2–	O	Reverse rotation output pin of Driver 2	
23	6	VO2+	O	Normal rotation output pin of Driver 2	
24	5	VO1–	O	Reverse rotation output pin of Driver 1	
25	4	VO1+	O	Normal rotation output pin of Driver 2	

Note) Pin No. shown in the equivalent circuit diagram are only for the AN8812SC. For the AN8812SCR, they must be replaced.

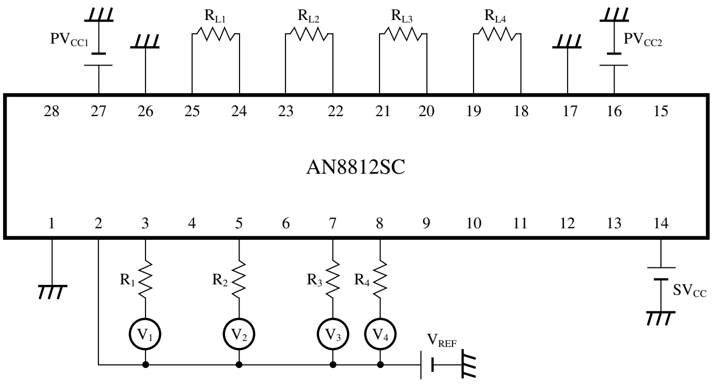
■ Pin Description

Pin No.		Symbol	I/O	Pin Description	Equivalent Circuit
AN8812SC	AN8812SCR				
9	20	TB	O	Output pin for controlling the power transistor base of 5V regulator	
10	19	V_{MON}	I	Monitor input pin for 5V regulator output	
11	18	OPO	O	Output pin of operational amplifier	
12	17	IN–	I	Inverting input pin of operational amplifier	
13	16	IN+	I	Non-inverting input pin of operational amplifier	
14	15	SV_{CC}	—	SV_{CC} pin for driver control circuit, not connected with power V_{CC} pin	

Note) Pin No. for the AN8812SC are only shown in the equivalent circuit diagram. For the AN8812SCR, they must be replaced.

■ Cautions for use

• AN8812SC



When the AN8812SC is used, take into account the following cautions and follow the power dissipation characteristic curve.

(1) Load current, I_{P1} flowing in loads R_{L1} and R_{L2} is supplied through Pin27.

$$I_{P1} = \frac{|V_{25}-V_{24}|}{R_{L1}} + \frac{|V_{23}-V_{22}|}{R_{L2}}$$

(2) Load current, I_{P2} flowing in loads R_{L3} and R_{L4} is supplied through Pin16.

$$I_{P2} = \frac{|V_{21}-V_{20}|}{R_{L3}} + \frac{|V_{19}-V_{18}|}{R_{L4}}$$

(3) Dissipation increase (ΔP_d) inside the IC (power output stage) caused by loads R_{L1}, R_{L2}, R_{L3} and R_{L4} is as follows :

$$\Delta P_d = (PV_{CC1} - |V_{25}-V_{24}|) \times \frac{|V_{25}-V_{24}|}{R_{L1}} + (PV_{CC1} - |V_{23}-V_{22}|) \times \frac{|V_{23}-V_{22}|}{R_{L2}} + (PV_{CC2} - |V_{21}-V_{20}|) \times \frac{|V_{21}-V_{20}|}{R_{L3}} + (PV_{CC2} - |V_{19}-V_{18}|) \times \frac{|V_{19}-V_{18}|}{R_{L4}}$$

(4) Dissipation increase (ΔP_d) inside the IC (signal block supplied from Pin14) caused by loads R_{L1}, R_{L2}, R_{L3} and R_{L4} is almost as follows :

$$\Delta P_d = 3\left\{\frac{V_1}{R_1}(2SV_{CC} + |V_{25}-V_{24}|) + \frac{V_2}{R_2}(2SV_{CC} + |V_{23}-V_{22}|) + \frac{V_3}{R_3}(2SV_{CC} + |V_{21}-V_{20}|) + \frac{V_4}{R_4}(2SV_{CC} + |V_{19}-V_{18}|)\right\}$$

(5) Dissipation increase inside the IC during driver running is $\Delta P_d + \Delta P_S$.

(6) Inside loss under no load (P_{d1}) is almost as follows :

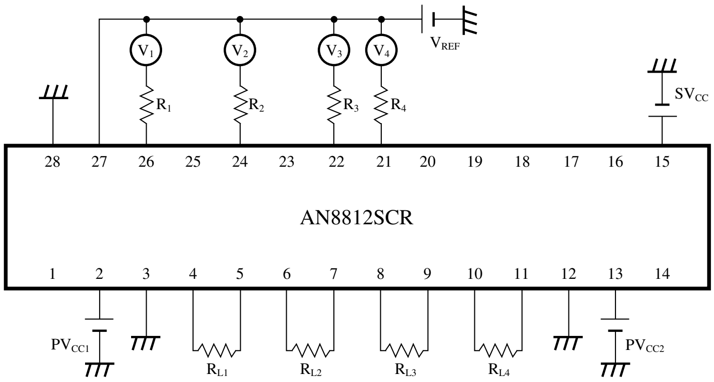
$$P_{d1} = SV_{CC} \times I(SV_{CC}) + PV_{CC1} \times I(PV_{CC1}) + PV_{CC2} \times I(PV_{CC2})$$

(7) Entire IC inside loss (ΔP_d) is almost as follows :

$$P_d = P_{d1} + \Delta P_d + \Delta P_S$$

■ Cautions for use

• AN8812SCR



When the AN8812SCR is used, take into account the following cautions and follow the power dissipation characteristic curve.

(1) Load current, I_{P1} flowing in loads R_{L1} and R_{L2} is supplied through Pin2.

$$I_{P1} = \frac{|V_4 - V_5|}{R_{L1}} + \frac{|V_6 - V_7|}{R_{L2}}$$

(2) Load current, I_{P2} flowing in loads R_{L3} and R_{L4} is supplied through Pin13.

$$I_{P2} = \frac{|V_8 - V_9|}{R_{L3}} + \frac{|V_{10} - V_{11}|}{R_{L4}}$$

(3) Dissipation increase (ΔP_d) inside the IC (power output stage) caused by loads R_{L1}, R_{L2}, R_{L3} and R_{L4} is as follows :

$$\Delta P_d = (PV_{CC1} - |V_4 - V_5|) \times \frac{|V_4 - V_5|}{R_{L1}} + (PV_{CC1} - |V_6 - V_7|) \times \frac{|V_6 - V_7|}{R_{L2}}$$
$$+ (PV_{CC2} - |V_8 - V_9|) \times \frac{|V_8 - V_9|}{R_{L3}} + (PV_{CC2} - |V_{10} - V_{11}|) \times \frac{|V_{10} - V_{11}|}{R_{L4}}$$

(4) Dissipation increase (ΔP_S) inside the IC (signal block supplied from Pin15) caused by loads R_{L1}, R_{L2}, R_{L3} and R_{L4} is almost as follows :

$$\Delta P_S = 3 \left\{ \frac{V_1}{R_1} (2SV_{CC} + |V_4 - V_5|) + \frac{V_2}{R_2} (2SV_{CC} + |V_6 - V_7|) \right.$$
$$\left. + \frac{V_3}{R_3} (2SV_{CC} + |V_8 - V_9|) + \frac{V_4}{R_4} (2SV_{CC} + |V_{10} - V_{11}|) \right\}$$

(5) Dissipation increase inside the IC during driver running is $\Delta P_d + \Delta P_S$.

(6) Inside loss under no load (P_{d1}) is almost as follows :

$$P_{d1} = SV_{CC} \times I_{SVCC} + PV_{CC1} \times I_{PVCC1} + PV_{CC2} \times I_{PVCC2}$$

(7) Entire IC inside loss (P_d) is almost as follows :

$$P_d = P_{d1} + \Delta P_d + \Delta P_S$$