Active Power Management Using SuperI/O™ Low Power ICs Make Possible the Ultimate Low Power PC

The PC87334VJG SuperI/O integrated PC I/O controller and PC87912VJG single-chip keyboard controller/real-time clock provide the most sophisticated active power management available for notebook, PDA and palmtop PCs.

OVERVIEW

In the relentless drive to produce a smaller, lighter, less power-hungry PC, the choice is often made to achieve low power consumption with low voltage devices operating at slow clock speeds. The result: lower system performance. With the recently introduced SuperI/O PC87334VJG and PC87912VJG, however, that performance barrier has just been lifted.

Now the PC designer can utilize high performance CPU, memory and I/O components and still dramatically cut power consumption through sophisticated active management schemes. These methods are available in the SuperI/O devices and compatible core logic devices.

There are three enabling factors at work. First, the SuperI/O family packs all of the basic set of PC I/O device controllers into two TQFP (14mm x 14mm) chips. This reduces size and power consumption. Second, these devices provide for both selective operating conditions (one device on, others off) and fine-grain tuning of the operating conditions. This means that in addition to turning an I/O channel on or off, the designer can selectively block inputs to that channel and even TRI-STATE the bus lines to effectively eliminate all but a tiny current leakage. Third, due to the enhancements made in the family's 8051-based keyboard controller/RTC, exceptionally quick wakeup modes make it possible for the major components of the PC system to remain in sleep mode for far longer than other approaches.

Of course, to achieve maximum system-wide power savings, the SuperI/O low power devices must be complemented by a core logic chipset that also provides active power management, such as the Redwood and Fir devices from PicoPower Technology. These devices, and any core logic devices that use the ISA interface, are easily integrated with the SuperI/O family of devices.

The Next Generation PDA-TQFP Packaging and Active Power Management are Key

In the past, passive power management and primitive active management schemes cut power consumption to a level that could meet the widely popularized Green PC or Energy Star Logo program of the EPA. This praiseworthy effort defined systems that would be able to cut power to less than 30 Watts in standby mode. While this effort alone will save countless billions in wasted energy from PC left on while not being used, it falls far short of the leading edge in power conservation.

The high-performance PDA or palmtop PC is the technology driver for sophisticated power management and package miniaturization. The next generation handheld systems will require the full resources of the latest 32-bit and even 64-bit microprocessors running a full Windows™ or a Windows subset operating system. To achieve this, simply turning off resources when they are not in use for a few minutes will not achieve the necessary reduction in power consumption.

Advanced PDAs are driving the miniaturization of IC packages. TQFPs or Thin Quad Flat Packages are the current state of the art for standard devices. The SuperI/O PC87334VJG and PC87912VJG devices and the PicoPower "Fir" core logic device are available in these packages. With these devices, along with a TQFP 486 CPU, a TQFP VGA controller, and two TQFP PCMCIA controllers, a powerful 486-based system can be designed—in less than 7 sq. inches of board space.

Of course, an extraordinary small system does not complete the task. The power consumption in high performance CPU, memory and I/O devices, if not kept to a very low level will still require a large power supply and/or a ready supply of batteries.

The solution is active power management. National Semiconductor responded first with active power management in its SuperI/O III PC87332VLJ CMOS integrated I/O controller. The most recent generation extends this technology to the 3V/5V PC87334VJG SuperI/O and the PC87912VJG devices.

The PC87334VJG integrates on a single-chip all of the input/output controllers used in a typical personal computer configuration. This includes a floppy disk controller, an IDE hard disk controller, two PC-standard serial ports, an HP infrared serial port mode, and an IEEE1284 compatible parallel port—all in an ultra-thin (1.4mm) 100-pin TQFP package drawing only 10 μA in standby mode and a maximum of 100 mW fully loaded.

The PC87912VJG integrates an enhanced 8051-based keyboard controller and a real-time clock. It is also packaged in a 196 sq. mm. 100-pin TQFP, drawing only 10 μA in standby mode.

Naturally, there are power savings achieved by the packing of the multiple I/O drivers into a single device, as compared to multi-chip implementations. This is due to the elimination of redundant and power-hungry bus drivers and resistor networks.

Active Power Management

But much greater power savings are achieved by the programmable nature of the devices. The PC87334VJG has many programmable power management modes. Each individual I/O channel can be selectively turned off when not being used. Also, the inputs can be blocked for further power reduction. In addition, the output pins can be put into TRI-STATE® mode to eliminate all but a tiny leakage current. Finally, the crystal oscillator can be stopped entirely. Depending on the level of the I/O usage, operating power can be dramatically cut through this active power management scheme.
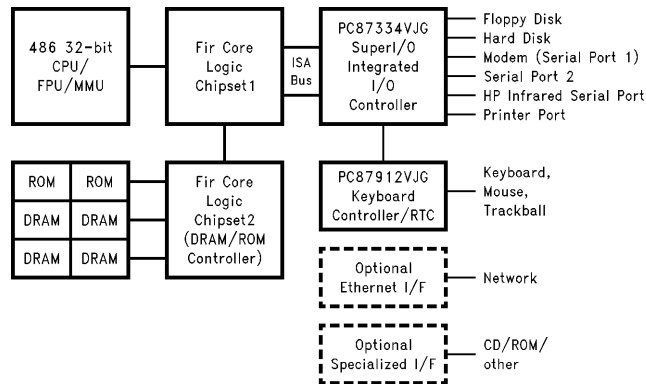
The Shrinking PDA Motherboard: Higher Integration, TQFP Packages, Active Power Management
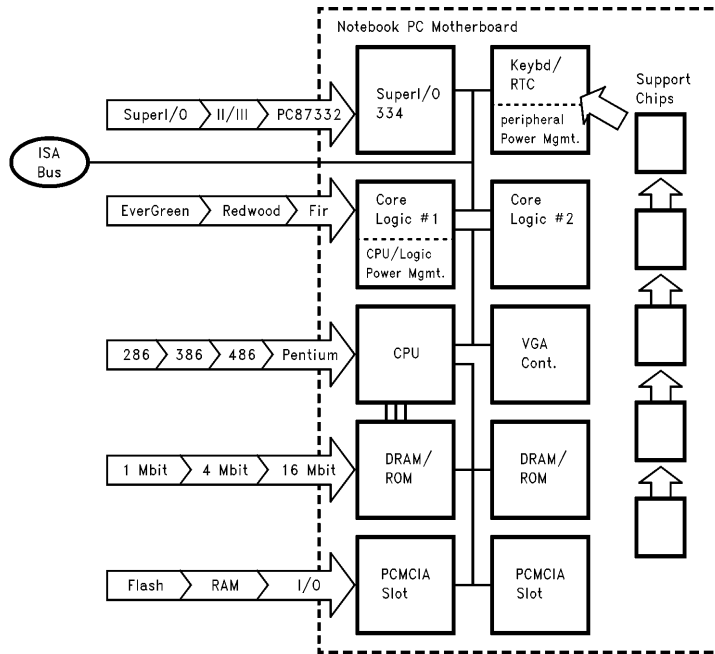
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Advanced PDA PC Electronics Block Diagram
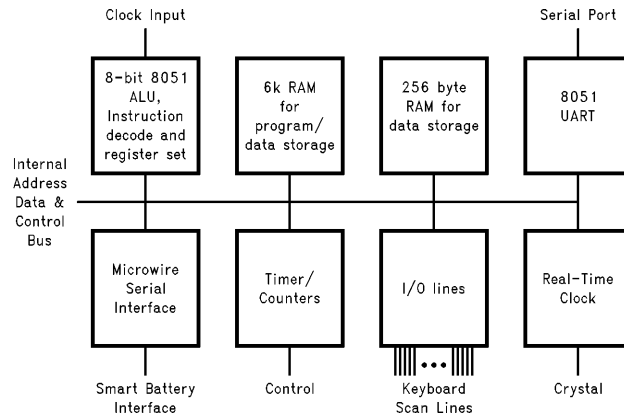

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When used with the PC87912VJG keyboard controller/RTC, however, even more dramatic reductions in operating power consumption can be obtained.

The PC87912VJG is a single-chip solution for keyboard control, keyboard scan, real-time clock and system-wide power management. It provides an enhanced performance 8051 8-bit microcontroller core with a RAM-based program storage of 6k, multiple I/O ports, a serial 8051-type UART, MICROWIRE™ serial bus lines, and a PC-standard real-time clock. While the PC87912VJG takes less space because of a smaller package (the TQFP), it also absorbs all of the glue logic needed in previous solutions.

The PC87912VJG can be a very important component of an active power management system and it represents a major improvement over previous keyboard/RTC approaches. First, it provides a much more powerful microcontroller—the 8051 vs. the widely used 8042/8048 combinations used in the past. Second, the 8051 throughput is effectively doubled because instructions are executed in only six clock cycles versus the 12 cycles in the standard 8051.

This means that the system operates faster at a slower clock—reducing power consumption without compromising performance. Of possibly more significance, however, is that by allowing the software to complete its tasks more

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PC87912 Keyboard Controller/RTC Block Diagram

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rapidly, the overall system can spend more of its time in sleep mode—using no power at all.

This goal of having the system complete its tasks quickly and then spend more time in the near zero power consumption standby or sleep mode is facilitated by two other PC87912VJG features. One is its hardware assisted serial keyboard scan functions and the other is the multi-input wakeup interrupt handler.

Hardware assist for serial keyboard and mouse operation greatly cuts the amount of time the microcontroller spends in a software loop waiting for key presses and then decoding them. Normally, the 8051 must read keyboard or mouse data one bit at a time (serially). This is time consuming because it takes a lot of program overhead to execute through a loop reading bits and then assembling into meaningful bytes of information. The PC87912VJG includes a small amount of on-chip logic that captures and transforms serial information into parallel information, one byte at a time. This means that the 8051 now communicates with the serial keyboard or mouse a byte at a time, greatly reducing the amount of program code (and execution time) needed to support external serial keyboard or mouse operation.

This hardware assist also supports receiving a serial keyboard or serial mouse input while the 8051 is in sleep or halt mode, without losing any data. This means that the 8051 can be powered down without the risk of missing any keystrokes. The microcontroller can spend more time in sleep mode with no loss of perceived performance. This savings over several hours of operation can significantly increase battery life—an important issue to the end user and a key differentiator for the PC OEM.

Another beneficial feature of the PC87912VJG is the multi-input wakeup that allows a number of different inputs to wakeup the microcontroller quickly from sleep mode. An internal 8-bit register provides flags for internal keyboard scan hardware (key press), an external keyboard scan (key press), a PS/2 mouse input, the three internal 8051 timers, the 8051 UART, the real-time clock, and two user definable external inputs to awake the microcontroller.

This feature greatly enhances the ability of the 8051 to respond quickly to external and internal events. A technology first implemented in the National COPS series of 4- and 8-bit microcontrollers, it greatly increases the flexibility and power of the active power management scheme.

Previous 8051 implementations required a full reset when waking from a halt condition. This is very time-consuming. For example, the 8051 requires a minimum of 10 milliseconds for the external oscillator to stabilize—before entering its reset vectors and going through its initialization routines. The PC87912VJG on the other hand can go directly from a wakeup interrupt to a vectored address and back to a waiting application very quickly.

The combination of the high throughput processing power of the enhanced 8051 microcontroller, the high speed scanning of keystrokes, and the fast wakeup capability from a number of different sources make the PC87912VJG a very potent energy saver.

It saves power by requiring less time to complete basic tasks. More importantly, it saves even more power by remaining in sleep mode much of the time even between keystrokes.

Partitioning the RTC Allows Flexible Schemes

Finally, because the RTC is isolated in the keyboard IC and not in the CPU or core logic ICs, those power hungry chips can be left in sleep mode while only the RTC, and when necessary, the 8051, monitor and react to system level events. For example, the RTC can be programmed to send a periodic wakeup to the 8051. The 8051 can then check the system to determine the state of the system. If nothing needs attending, it can go back to sleep. If conditions warrant action, the 8051 can take the appropriate action with or without the main CPU. If an application is open, but the system has not been used for several minutes, for example, but the battery is slowly becoming drained, the 8051 may want to alert the CPU and have the open application saved to disk, before the battery goes completely dead.

The internal 8051 UART can also be used to wake up the system when a modem ring detect signal is received. In addition, the PC87912VJG 8051 I/O lines can be connected to monitor any system event and to make any change of state a wakeup event.

Developing a 486 Sub-Notebook PC with SuperI/O Low Power Devices

An advanced sub-notebook personal computer will feature a 32-bit 486 CPU, a core logic chipset that includes active power management (such as the "Fir" from PicoPower Technology), a VGA/flat panel controller, DRAM, ROM, a

parallel printer port, two serial ports, a floppy disk drive, a hard disk drive, and two PCMCIA slots. The system electronics can be broken down into the following system blocks:

CPU— 486 32-bit processor (1)

Memory— DRAM/ROM (9-27)

Logic— PT86C568 Fir Core logic chipset (2)

I/O— SuperI/O III PC87334VJG and PC87912VJG controllers (2)

VGA— Flat panel VGA controller (1)

PCMCIA— PCMCIA controllers (2)

A key issue in sub-notebook PC design is reducing power consumption and board real estate. The 486 CPU is now available in TQFP packages as are the other elements of the system. The only requirement for interconnection is the ISA standard bus for address, data and control signals. All of the components operate at 3.3V and with the SuperI/O III Ultra components, no additional glue logic is required. (The RTC typically uses a lithium battery.) The rest of the system can operate from standard NiCd batteries.

The total area of this system, using all TQFPs, is less than 7 sq. inches. With the tiny 1.4mm height of the TQFP, the PC motherboard can be manufactured using double-sided surface mount assembly techniques.

A key advantage of such a system is the open architecture approach. Using the ISA bus allows the OEM to pick and choose devices from a number of vendors—providing an opportunity to create product line variety with a minimum of design effort. Of course, this also provides a security factor should supplies of any one device become limited for any reason. A quick redesign capability is great insurance when product life cycles are less than 9 to 12 months.

Inside the SuperI/O PC87334VJG

The PC87334VJG block diagram shows the internal blocks of this device. In addition to dual UARTs, an infrared serial port, an IEEE1284 parallel port, a floppy disk controller, and an IDE hard drive interface, there are address, data and control signals from the processor, a set of configuration registers and the power control logic.

To insure easy integration with many different chipsets, the PC87334VJG uses the widely supported ISA bus for address, data and control signals. This makes the I/O controller accessible to almost any system.

In addition to offering the standard capabilities of the SuperI/O family, National can also use these devices as building blocks for integrating OEM-specific communications and other I/O technologies on a single chip. In the future, the SuperI/O family may be extended with devices incorporating other National communications technologies.

The PC87334VJG reduces power consumption in three ways. A major reduction comes by eliminating a large number of devices and ancillary support logic. The PC87334VJG is a single device needing almost no supporting logic or external components. The PC87334VJG can also operate at 3V, reducing standard operating power consumption—and making possible system operation from AA batteries. Finally, the PC87334VJG supports several programmable power-down modes. In standby mode, it draws only 10 μA. Since I/O devices often are utilized only a fraction of the time, this can greatly reduce overall system power requirements and extend battery life by powering down individual or groups of I/O devices when they are not being used.

**486 Sub-Notebook PDA PC:
Motherboard Can Be under 7 sq. inches in Size**
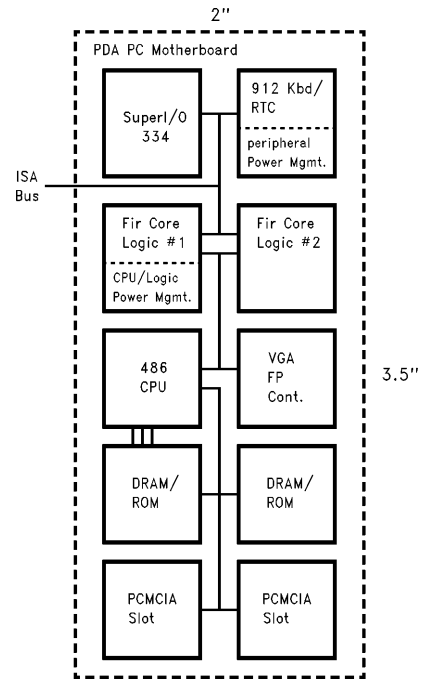
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High Performance Internal I/O Functions

The PC87334VJG achieves its system level advantages without sacrificing performance. It provides a rich, full-featured set of I/O controllers. The Floppy Disk Controller is a superset of popular FDC controllers (the DP8473, NEC μPD765, and N82077 FDCs) and includes a digital data separator requiring no external filter components. It can also support the 2 Mb/s data rates required by the newest streaming tape drives. The UARTs can operate in either industry standard PC16C550 or PC16450 mode. The IEEE1284 parallel port is fully compatible with the high performance aspects of this specification, including the Enhanced Parallel Port (EPP) and the very fast (2 Mb/s) Extended Capabilities Port (ECP). The IDE Hard Disk Drive interface is a complete IDE interface, although external signal buffers are recommended for full 24 mA IDE bus drive capability. (This is not needed in typical notebook PC designs.)

Of special note is the inclusion of an Hewlett-Packard-compatible infrared serial port mode. This provides the capability of wireless communications between sub-notebook PC and a printer, for example. For portable systems, this can be a major advantage and leading peripheral manufacturers (and portable PC makers) are aggressively adding this capability to their printers, modems, fax machines and similar PC peripherals.

The PC87334VJG provides standard AT address decoding for on-chip functions and selection of all primary and secondary ISA addresses including COM1-4 and LPT1-3.

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Power Consumption

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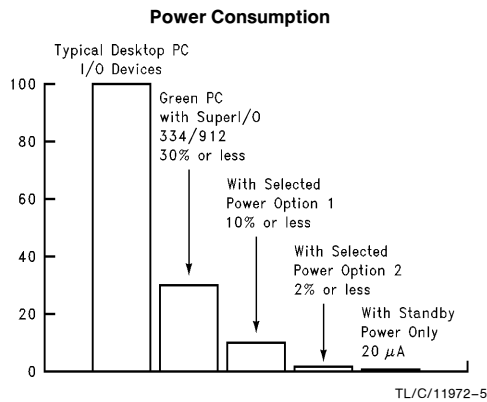
Option 1 -

Group 2 specific function power down:
FDC powered down, UARTs powered-down,
IDE on, parallel ports powered-down

Option 2 -

Group 2 specific function power down:
FDC powered down, FDC pins TRI-STATE, FDC inputs blocked, UARTs powered-down, UART pins TRi-STATE and inputs blocked, IDE powered-down, IDE pins TRI-STATE, IDE inputs blocked, Parallel port operating

A set of eight configuration registers are used to control the PC87334VJG resources. These are:

Configuration Registers

Name	Description	Index Address
FER	Function Enable Register	00h
FAR	Function Address Register	01h
PTR	Power and Test Register	02h
FCR	Function Control Register	03h
PCR	Printer Control Register	04h
PMC	Power Management and Control	05h
TUP	Tape, UARTs and Par. Port Conf.	06h
SID	SIO Identification Register	07h

During reset, default values selected by hardware jumpers are loaded into these registers. After power-on, the registers can be read and written using an index register and data register pair. The index points to the individual configuration register. The data register contains the data to be written or the contents of the selected register. This scheme permits access to the entire PC87334VJG resource configuration register set through the use of only two I/O addresses.

The configuration registers permit the enabling and disabling of major chip functions. When disabled, the I/O function is powered down, but any internal data registers maintain their information.

Other functions controlled by these registers include setting of addresses, test modes, floppy and hard drive configuration settings, setting printer port modes, configuring UART settings, and power management controls.

Power Management Features

The PC87334VJG provides extensive control of power management functions. They can be grouped into two major categories; Group 1, full power-down and Group 2, individual function power-down.

A key to power savings in both groups is the PC87334VJG's ability to TRI-STATE the output pins associated with a given I/O function. This greatly reduces power output by eliminating the current leakage to the pull-up resistors on the outputs.

Another aspect of power reduction involves those I/O functions that utilize internal clocks. They are the FDC, both UARTs and the parallel port when in ECP mode. For these functions, power can be saved by either stopping their associated internal clocks or by stopping the external crystal oscillator.

Non-clock driven functions such as the parallel port in standard parallel port or enhanced parallel port modes and the IDE interface can be powered-down by blocking access to these resources.

In the Group 1 category, full device power-down, there are four power-down modes:

Group 1 - Full Power-Down Modes

Mode	Description	Current Consumption
1	The entire chip is powered-down. The crystal oscillator is stopped, pins are TRI-STATE, and the Inputs are blocked. This is the maximum power saving mode.	10 μA
2	The entire chip a powered-own. The crystal oscillator is stopped. Pins are driven.	1.5 mA
3	The entire chip is powered-down, pins are TRI-STATE, and the inputs are blocked. The crystal oscillator operates and provides fast wake-up.	7 mA
4	The entire chip is powered-down. Pins are driven. The crystal oscillator operates.	8.5 mA

In the Group 2 category, individual function power-down, there are ten power-down modes. Depending on the I/O function (parallel port, UART, FDC or IDE) and the combination of configuration states (function power-down, pins TRI-STATE, inputs blocked), the potential power savings can range from 0.5 mA to 5 mA per function.

SOME SYSTEM DESIGN CONSIDERATIONS

3.3V or 5V Components

There are several other system design considerations when using the PC87334VJG device. An important decision is whether to use a 3.3V or 5V supply. The choice depends on economics and system trade-offs.

Using 3.3V components can result in a system that needs smaller batteries or a smaller supply. This can be of great benefit for some notebook and sub-notebook systems. On the other hand, 3.3V components generally are more ex-

pensive and sometimes in limited supply. In the price competitive market of today, 5V components can help reduce system costs.

The PC87334VJG supports both 3.3V and 5V operating supplies and simplifies the design of mixed 3V/5V systems. Its I/O cells can tolerate 5V external components while operating on a 3.3V power supply. This means that the systems designer can make more trade-offs between power consumption and price than when using other approaches.

Minimal Support Logic

The PC87334VJG needs very little support logic. A crystal oscillator, two 3.3V DS14C335 TIA/EIA-232E (standard RS-232) driver/receivers for the two UARTs, two 3.3V 74HC245 octal bidirectional transceivers and one 3.3V 74HC244 octal buffer for the IDE bus are all the external logic required for a complete system.

In fact, the transceivers are needed only if the IDE bus requires the full 24 milliamps drive capability defined in the IDE specification. Typically such drive capability is required only in systems requiring access to drives through extended cabling. Since most notebooks have single hard drives closely linked to the motherboard, these devices can be safely eliminated in most cases.
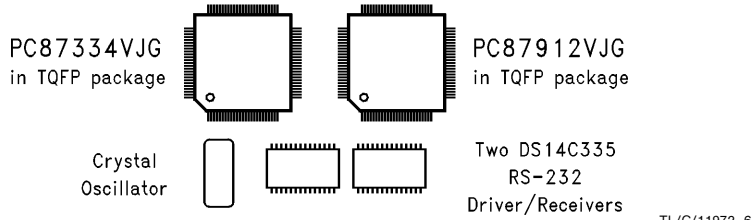
The RS-232 drivers include internal charge pump circuitry for generating the necessary 12V $\pm$ from the standard 3.3V supply. This eliminates any external circuitry for this function. The DS14C335 also includes an internal shut-down mode to conserve power and with one active receiver, draws only a maximum of 10 microamps. An additional advantage of the DS14C335 is its high speed data transfer speeds of up to 128 kbs/s, six times faster than the standard 20 kbs RS-232 transfer speed.

Packaging

The PC87334VJG is available in a compact 100-pin TQFP package, requiring only 196 square mm. of board space. The PC87912VJG is available in the same package. The DS14C335 is available in a 28-lead SSOP EIAJ Type II package measuring only 7.5mm wide and 10mm long. The optional 74VHC245 is available in a 20-lead plastic EIAJ SSOP Type 1 package measuring only 5.5mm by 6.4mm.

This figure shows the actual size of the PC87334VJG, the PC87912VJG and their support circuitry.

PC87334VJG SuperI/O and PC87912 Will All Support Circuitry (Actual Size)

PC87334VJG in TQFP package

PC87912VJG in TQFP package

Crystal Oscillator

Two DS14C335 RS-232 Driver/Receivers

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