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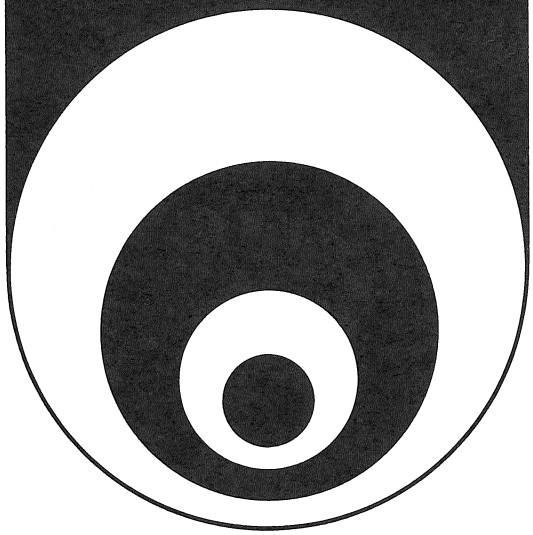


2650 DEMO SYSTEM SP51

GENERAL

The Demo System (DS) is a hardware base for use with the 2650 CPU printed circuit board (PC1001). The DS provides the user of the 2650 with a convenient "lab bench" set-up for exercising the PC1001 CPU board. The user may expand memory, implement I/O functions, and step through program instructions one at a time using the DS. When the DS is combined with a CPU board (PC1001) and a keyboard terminal, the user is equipped with everything he needs to exercise any of the software or hardware features of the 2650. There are two versions of the DS, the DS1000 and the DS2000. The two Demo Systems are the same except that the DS2000 has a built-in power supply and therefore does not have the power supply binding posts.

FEATURES

The DS provides several connectors to aid the user in exercising the PC1001 CPU board including one for the CPU board itself, one for a memory expansion board, four for I/O ports, and two for communicating with the user's terminal. There are four sets of LED lamps that display the information on the address bus, the data bus, and the two non-extended I/O ports. Two control switches (RUN/PAUSE, and STEP) allow the user to place the 2650 in the WAIT mode and step through program execution one instruction at a time. A reset button is provided on the DS. The DS1000 version has five-way binding posts for connection to external power supplies. The DS2000 has built-in power supplies and does not have the five-way binding posts.

CONNECTORS:

2650 CPU Board Edge Connector (J8). The CPU board connector is an Amphenol dual 50-pin connector (series 225) with 0.125-inch contact centers. The 2650 CPU board (PC1001) is inserted into J8 to complete the Demo

CPU BOARD AND USER BOARD CONNECTORS

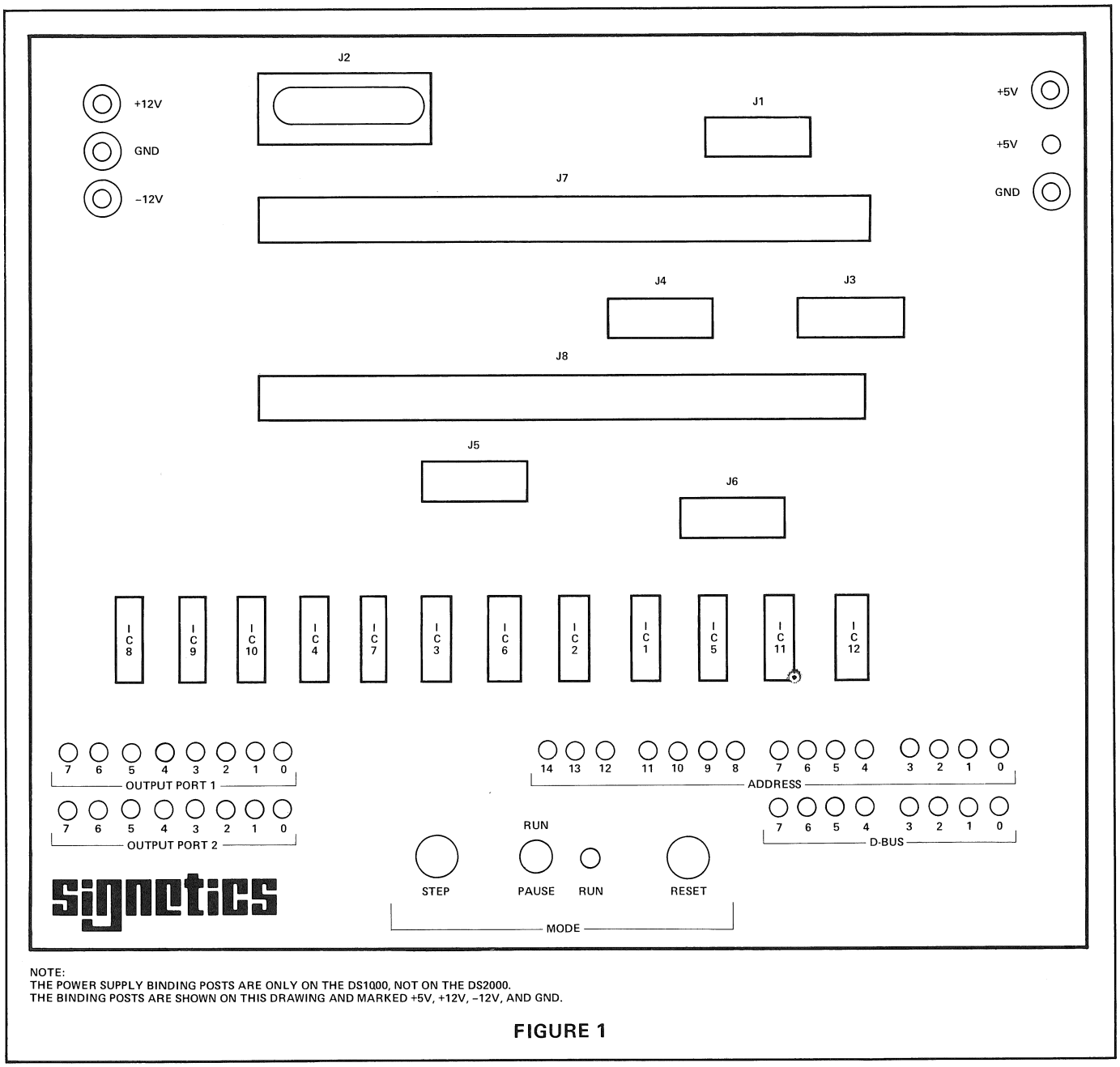
PIN#	FUNCTION (J7 & J8)	PIN#	FUNCTION (J8 ONLY)*
1	GND	A	GND
2	GND	B	GND
3	NC**	C	NC
4	$\overline{\text{DBUS0}}$	D	OPD 0
5	$\overline{\text{DBUS1}}$	E	OPD 1
6	$\overline{\text{DBUS2}}$	F	OPD 2
7	$\overline{\text{DBUS3}}$	H	OPD 3
8	$\overline{\text{DBUS4}}$	J	OPD 4
9	$\overline{\text{DBUS5}}$	K	OPD 5
10	$\overline{\text{DBUS6}}$	L	OPD 6
11	$\overline{\text{DBUS7}}$	M	OPD 7
12*	EIPD	N	COPD
13	D/$\overline{\text{C}}$	P	TTY SERIAL IN +
14	$\overline{\text{DMA}}$	R	TTY SERIAL IN -
15	E/$\overline{\text{NE}}$	S	TTY SERIAL OUT +
16	INTACK	T	TTY SERIAL OUT -
17	$\overline{\text{R}}$/W	U	RS232 GROUND
18	WRP	V	RS232 OUTPUT
19	RUN/$\overline{\text{WAIT}}$	W	TTY TAPE READER OUT -
20	OPREQ	X	TTY TAPE READER OUT +
21	M/$\overline{\text{IO}}$	Y	RS232 INPUT
22	$\overline{\text{OPACK}}$	Z	COPC
23	CLOCK	a	OPC 0
24	$\overline{\text{OPEX}}$	b	OPC 1
25	$\overline{\text{RESET}}$	c	OPC 2

PIN#	FUNCTION (J7 & J8)	PIN#	FUNCTION (J8 ONLY)*
26	$\overline{\text{INTREQ}}$	d	OPC 3
27	$\overline{\text{PAUSE}}$	e	OPC 4
28	NC	f	OPC 5
29	NC	g	OPC 6
30	NC	h	OPC 7
31	NC	j	EIPC
32	NC	k	IPD 0
33	ABUS 11	m	IPD 1
34	ABUS 13	n	IPD 2
35	ABUS 12	p	IPD 3
36	ABUS 14	r	IPD 4
37	ABUS 9	s	IPD 5
38	ABUS 10	t	IPD 6
39	ABUS 8	u	IPD 7
40	ABUS 7	v	IPC 0
41	ABUS 6	w	IPC 1
42	ABUS 5	x	IPC 2
43	ABUS 3	y	IPC 3
44	ABUS 0	z	IPC 4
45	ABUS 1	$\overline{\text{a}}$	IPC 5
46	ABUS 4	$\overline{\text{b}}$	IPC 6
47	ABUS 2	$\overline{\text{c}}$	IPC 7
48	+12V	$\overline{\text{d}}$	+12V
49	-12V	$\overline{\text{e}}$	-12V
50	+5V	$\overline{\text{g}}$	+5V

*J7 has no connections to these pins.
**NC = No Connection

TABLE 1

DEMO SYSTEM LAYOUT



NOTE:
THE POWER SUPPLY BINDING POSTS ARE ONLY ON THE DS1000, NOT ON THE DS2000.
THE BINDING POSTS ARE SHOWN ON THIS DRAWING AND MARKED +5V, +12V, -12V, AND GND.

FIGURE 1

CONNECTORS (Continued)

System. The correlation between signal names and pin numbers for J8 is given in Table 1. The location of J8 on the DS is shown in Figure 1.

User Printed Circuit Board Edge Connector (J7). The user board connector is the same type of connector as J8 (the CPU board connector), and makes address, data and control lines available for user-defined interface functions. As shown in Table 1, the numbered pins of J7 and J8 have the same signals on them (except pin 12), while the lettered pins of J7 (pins A through $\bar{g}$) are not used. The J7 connector is typically used for memory expansion. The location of J7 on the DS is shown in Figure 1.

Extended Input/Output DIP Sockets (J5 & J6). The extended I/O DIP sockets make the signals shown in Table 2 available to the user of the DS system. With the signals available on J5 and J6, any type of I/O interface to the 2650 may be implemented. The user of these sockets must supply the cable between his system and the DS, as well as the two 18-pin DIP plugs. The location of J5 and J6 is shown in Figure 1.

EXTENDED INPUT/OUTPUT DIP SOCKETS

PIN #	FUNCTION	
	J5	J6
1	$\overline{\text{DBUS 0}}$	ABUS 0
2	$\overline{\text{DBUS 1}}$	ABUS 1
3	$\overline{\text{DBUS 2}}$	ABUS 2
4	$\overline{\text{DBUS 3}}$	ABUS 3
5	$\overline{\text{DBUS 4}}$	ABUS 4
6	$\overline{\text{DBUS 5}}$	ABUS 5
7	$\overline{\text{DBUS 6}}$	ABUS 6
8	$\overline{\text{DBUS 7}}$	ABUS 7
9	$\overline{\text{OPACK}}$	ABUS 8
10	M/$\overline{\text{IO}}$	ABUS 9
11	OPREQ	ABUS 10
12	RUN/$\overline{\text{WAIT}}$	ABUS 11
13	WRP	ABUS 12
14	$\overline{\text{R}}$/W	ABUS 13
15	INTACK	ABUS 14
16	E/$\overline{\text{NE}}$	$\overline{\text{PAUSE}}$
17	$\overline{\text{DMA}}$	$\overline{\text{INTREQ}}$
18	D/$\overline{\text{C}}$	CLOCK

TABLE 2

Non-Extended Input/Output DIP Sockets (J3 & J4). Each non-extended I/O DIP socket (J3 and J4) makes the signals shown in Table 3 available to the user of the DS system. These sockets may be used for data or command transfer between the 2650 CPU and a user-defined function, but transfers via these channels are initiated by the CPU only. The user of these sockets must supply the cable between his system and the DS, as well as the 18-pin DIP plugs. The location of J3 and J4 is shown in Figure 1.

NON-EXTENDED INPUT/OUTPUT DIP SOCKETS

PIN #	FUNCTION	
	J3	J4
1	OPC 0	OPD 0
2	OPC 1	OPD 1
3	OPC 2	OPD 2
4	OPC 3	OPD 3
5	OPC 4	OPD 4
6	OPC 5	OPD 5
7	OPC 6	OPD 6
8	OPC 7	OPD 7
9	COPC	COPD
10	EIPC	EIPD
11	IPC 7	IPD 7
12	IPC 6	IPD 6
13	IPC 5	IPD 5
14	IPC 4	IPD 4
15	IPC 3	IPD 3
16	IPC 2	IPD 2
17	IPC 1	IPD 1
18	IPC 0	IPD 0

TABLE 3

RS232 Interface Connector (J2). The RS232 interface connector is a TRW 25-pin connector (part #DB25S) for communicating with RS232-compatible input/output devices. The pins used on this connector are shown in Table 4 along with the corresponding signal names. The RS232 driver and receiver are on the PC1001 circuit board and are wired to J2 through the DS circuit board. The location of J2 on the DS board is shown in Figure 1.

RS232 INTERFACE CONNECTOR (J2)

PIN #	FUNCTION – J2
1	RS232 GROUND
2	RS232 INPUT
3	RS232 OUTPUT
5	JUMPER
6	JUMPER
7	RS232 GROUND
8	JUMPER
20	JUMPER

TTY INTERFACE DIP SOCKET (J1)

PIN #	FUNCTION – J1
1	TTY SERIAL IN +
2	TTY SERIAL IN –
8	TTY TAPE READER OUT –
9	TTY TAPE READER OUT +
13	TTL SERIAL OUT –
14	TTL SERIAL OUT +

TABLE 4

TTY Interface DIP Socket (J1). The TTY interface socket is a 14-pin DIP socket and is used for communicating with a current loop serial interface. The pins used on this connector are shown in Table 4 along with the corresponding signal names. The current loop driver and receiver circuits are on the PC1001 board and are wired to J1 through the DS circuit board. The location of J1 on the DS board is shown in Figure 1.

DISPLAYS:

Address Display LEDs. The address display LEDs reflect the information on the address bus (ABUS 0-ABUS 14) when the PC1001 board is plugged into J8. The logic circuits on the DS board loads the information from the address bus into D-type latches on the occurrence of every Operation Request (OPREQ) pulse. Open collector inverters at the output of the D-type latches drive the LED's in a common anode configuration.

Data Bus Display LEDs. The data bus display LEDs reflect the information on the data bus (DBUS 0-DBUS 7) when the PC1001 board is plugged into J8. The information on the data bus is stored into D-type latches on every OPREQ pulse. The LEDs are driven directly from the D-type latches in a common anode configuration.

DISPLAYS (Continued)

Non-Extended Input/Output Channel LEDs. The non-extended I/O channel LEDs are driven by open collector inverters in a common anode configuration. The inverters are driven by the output latches of the two non-extended I/O ports on the PC1001 printed circuit board. Output Port 1 (2), bit 0 corresponds to DBUS 0 and Output Port 1 (2), bit 7 corresponds to DBUS 7. A logic "1" output from the 2650 turns on the LEDs, and a logic "0" turns off the LED.

+5V LED and RUN LED. The +5V LED will glow when a +5 volt power supply is connected to the Demo System. The DS1000 requires an external power supply, but the DS2000 has the +5 volt power supply built into the base. The RUN LED will glow when the RUN/WAIT line from the 2650 is in the "high" logic state. The location of these LED's is shown in Figure 1.

CONTROLS:

RESET Button. The reset button is a momentary switch that is tied directly to the Reset input on J8 (pin 25), and pulls that pin "low" when the button is pushed. This button clears the program counter in the 2650 to zero. The location of the reset button is shown in Figure 1.

PAUSE Switch and STEP Button. The pause switch and the step button are used together to cause the 2650 microprocessor to execute one instruction at a time. When the pause switch is in the RUN position, the step button does not affect the operation of the microprocessor.

When the pause switch is placed into the PAUSE position, the $\overline{\text{PAUSE}}$ line on the 2650 is pulled "low". When the execution of the current instruction is completed, the 2650 will enter the WAIT mode and the RUN/$\overline{\text{WAIT}}$ line will go "low". If the step button is pressed, the $\overline{\text{PAUSE}}$ line to the 2650 will be pulled "high" until the RUN/$\overline{\text{WAIT}}$ line goes "high", indicating that the 2650 is in the RUN mode. As soon as the RUN/$\overline{\text{WAIT}}$ line goes "high", the DS will again pull the $\overline{\text{PAUSE}}$ line "low". The step button will allow one instruction to be executed each time it is pushed as long as the pause switch is in the PAUSE position. When the pause switch is placed back onto the RUN position, the $\overline{\text{PAUSE}}$ line will be pulled "high" and the 2650 will execute instructions in a continuous manner. The address and data displayed on the DS LEDs in the WAIT mode reflect the address and the first byte of the next instruction to be executed. The location of the pause and step switches on the DS base is shown in Figure 1.

LOGIC CIRCUITS

The logic circuits on the DS base are shown in Figure 2. The logic circuits consist of address bus (ABUS) and data bus (DBUS) latches, the pause and step logic, LED drivers, and a reset switch. The address and data bus are loaded into latches on the DS during every OPREQ. The displays for the address and data bus will flicker while the run LED is "lighted", and will display the address and first byte of the *next* instruction to be executed when in the step mode (run LED off). The pause and step logic allows one instruction to be executed at a time by pushing the step button when the run/pause switch is in the PAUSE position. The non-extended output ports are displayed on the DS, and the reset button provides complete system reset by pushing the button.

ADDRESS BUS:

The address bus latches are 74174 Hex D-type flip-flops (IC1, IC2, IC3). Open collector inverters (IC5, IC6, IC7) invert the "positive true" levels from the ABUS latches and drive the address bus LEDs (L1-L15) in a common anode configuration. A logic ONE on the address bus "lights" the corresponding LED, and ABUS 0 corresponds to the ADDRESS bit 0 LED. The ABUS latch is clocked by the STRB signal which is generated by 4 inverters (IC7, IC10). The inverters provide the logic function STRB = OPREQ · CLOCK. The ABUS latches are reset by $\overline{\text{RESET}}$.

DATA BUS:

The data bus latches are also 74174 Hex D-type flip-flops (IC3, IC4). Since the DBUS leaves the PC1001 with "negative true" logic levels, the DBUS latches drive the LEDs directly in a common anode configuration. A logic ONE in the DBUS latches is a low voltage level and "lights" the corresponding LED. The DBUS bit 0 LED corresponds to DBUS 0. The DBUS latch is also clocked by the signal STRB, and reset by $\overline{\text{RESET}}$.

PAUSE AND STEP:

The pause and step switches are de-bounced with S/R latches. The step switch uses two NAND gates (IC11), while the pause switch uses a D-type latch (IC12) to accomplish the de-bounce function. When the pause switch is in the RUN position, SPAUSE is a logic ZERO and the $\overline{\text{PAUSE}}$ line is held at logic ZERO (de-activated).

When the pause switch is set to the PAUSE position, SPAUSE is a logic ONE and $\overline{\text{PAUSE}}$ will switch to a logic ONE. When the $\overline{\text{PAUSE}}$ line switches to a logic ONE, the 2650 will finish executing the current instruction, fetch the first byte of the next instruction from memory, and enter the wait state. The RUN/$\overline{\text{WAIT}}$ line goes to a logic ZERO when the 2650 enters the wait state. If the step switch is pushed, LSTEP clocks a logic ONE into the CLSTEP latch (IC12) which sets $\overline{\text{PAUSE}}$ to a logic ZERO. The 2650 then returns to the run mode, and the RUN/$\overline{\text{WAIT}}$ line goes to a logic ONE. When the RUN/$\overline{\text{WAIT}}$ line switches to a logic ONE, the CLSTEP latch is reset and

DS1000 LOGIC DIAGRAM

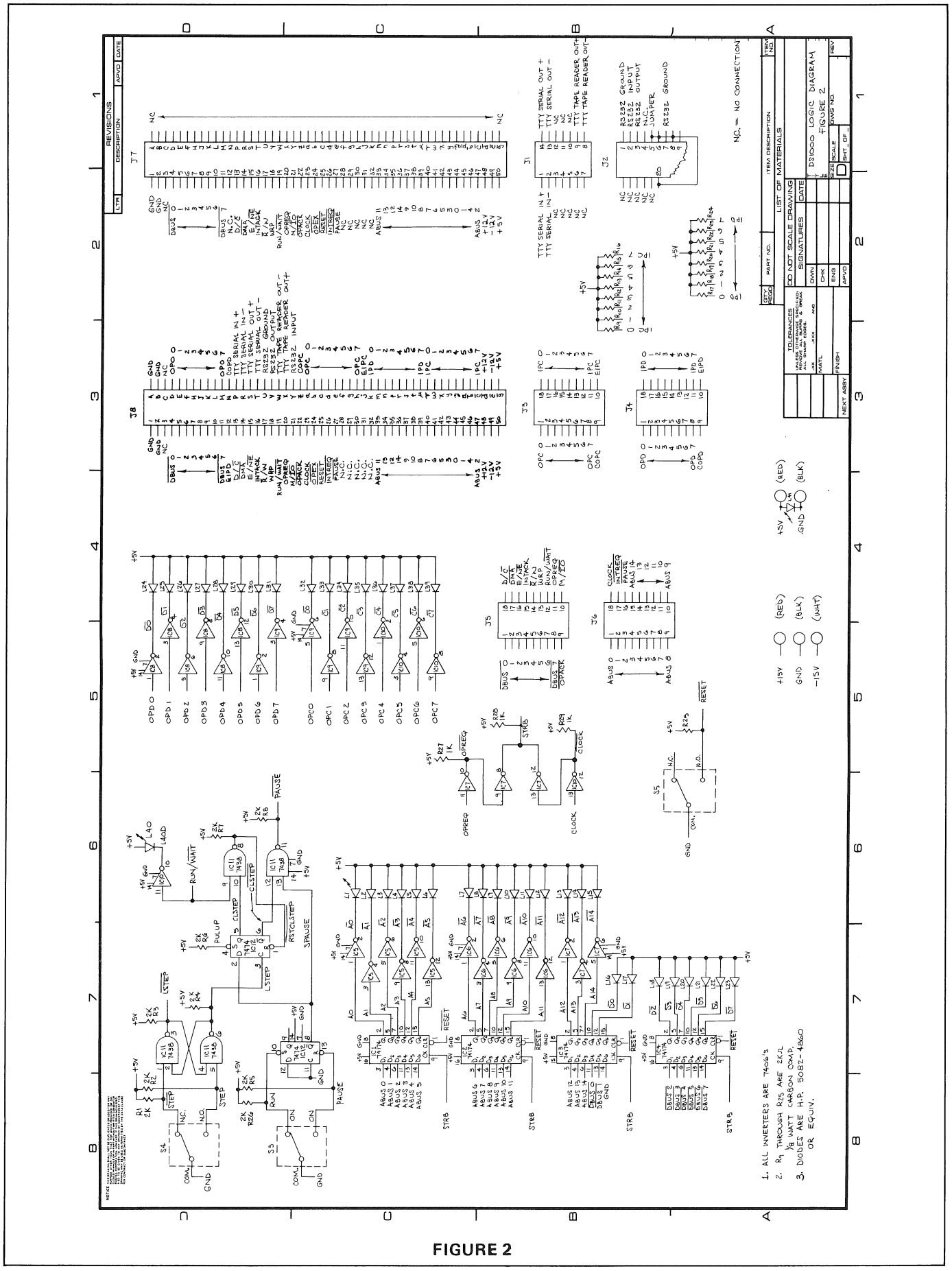


FIGURE 2

$\overline{\text{PAUSE}}$ returns to a logic ONE. This process is repeated once each time the step button is pushed. When the pause switch is returned to the RUN position, the $\overline{\text{PAUSE}}$ line is set to a logic ZERO and the 2650 will return to the run mode. The step/pause function is implemented with IC11 (NAND gate) and IC12 (D-type latch).

OUTPUT CHANNEL DISPLAYS:

The two non-extended output channels implemented on the PC1001 board are displayed on the DS. The output bits, (OPD 0 - OPC 7) are received by open collector inverters which in turn drive the LEDs. A logic ONE output to port 1 (WRTD instruction) will "light" the corresponding OPD LED, while a logic ONE to port 2 (WRTC instruction) will "light" the corresponding OPC LED. Signal OPD 0 corresponds to Output Port 1 bit 0, and OPC 0 corresponds to Output Port 2 bit 0.

RUN AND +5V DISPLAYS:

When the 2650 is in the run mode, the run LED will be "lighted". When +5 volts is applied across the red and black terminals of the DS1000, the +5V LED will be "lighted." When a.c. power is applied to the DS2000 (internal power supply), the +5V LED will be "lighted".

RESET:

The reset switch (S5) pulls the $\overline{\text{RESET}}$ line to a logic ONE when pushed. The $\overline{\text{RESET}}$ line is tied to the corresponding pin on the PC1001 board (pin 25) as well as the ABUS and DBUS latches on the DS.

DEMO SYSTEM PARTS LIST

Item #	Description	ID#	Mfg. and Part #
1.	Base Box	—	—
2.	Printed Circuit Board	—	—
3.	100-Pin Connector	J7, J8	Amphenol, series 225
4.	18-Pin Dip Socket	J3, J4 J6, J6	Cambion 703-3787-01-04-16
5.	14-Pin Dip Socket	J1	Cambion 703-4000-01-04-16
6.	SPDT Push Button Switch	S4, S5	Alco, MSP105F
7.	SPDT Toggle Switch	S3	Alco, MTA106D
8.	LED	L1-L41	H.P. 5082-4870450
9.	5-Way Binding Post		H.H. Smith
10.	RS232 Connector	J2	TRW Cinch DB25S
11.	Carbon Composition Resistors — 2KΩ	R1-R29	Allan Bradley RC05GF202J
12.	Aluminum Standoff		H.H. Smith 8352
13.	Tinnerman Speed Nuts		Tinnerman C8093-632

POWER SUPPLY SPECIFICATIONS

(DS1000 Only, Power Supply Included With DS2000)

5 Volt Power Supply	Line Regulation 0.1% Load Regulation 0.1% Ripple 10m Volts (maximum) Response Time 30 usec (maximum) Output Current 4 amps (To supply PC1001 only) Overvoltage Protection Current Overload Protection
±12 Volt Power Supply	Line Regulation 0.1% Load Regulation 0.1% Ripple 10m Volts (maximum) Response Time 30 usec (maximum) Output Current 50 milliamps (To supply PC1001 only) Overvoltage Protection Current Overload Protection

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