SiI3124A PCI-X to Serial ATA Controller Data Sheet

Document # SiI-DS-0160-C

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Revision History

Revision	Comment	Date
A	Derived from SiI3124-2 Datasheet Rev B	04/10/06
B	Correct inconsistence sentence	10/10/06
C	This Document is no longer under NDA. Removed confidential markings	2/02/07

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1 Overview

The Silicon Image SiI3124 is a four-port PCI-X to Serial ATA controller. The SiI3124 is designed to provide multiple port serial ATA connectivity with minimal host overhead and host to device latency. The SiI3124 supports a 64-bit 133 MHz PCI-X bus and the Serial ATA Generation 2 transfer rate of 3.0 Gb/s (300 MB/s).

1.1 Features

1.1.1 Overall Features

- Host Protocol
  - Optimized for transaction oriented designs – minimal Host overhead
  - Supports two command issuance mechanisms
    - Efficient in both embedded and PC implementations
    - Reduces dependency on bridge behavior
  - Designed to leverage PCI-X burst capabilities
  - Full 64 bit functionality
- Supports up to 4Mbit external Flash for BIOS expansion
- Supports a multimaster I^2C interface
- Supports external Flash or serial EEPROM for programmable subsystem vendor ID / subsystem product ID
- Fabricated in a 0.18µ CMOS process with a 1.8 volt core and 3.3 volt I/Os
- Available in a 364-pin HSBGA package (21x21 mm, 1mm ball pitch)
- JTAG boundary scan

1.1.2 PCI-X Features

- Supports 133 MHz PCI-X with 64-bit data
- Internal application interface multiplexed to 4 ports
- All registers appear in unified memory space
- Full-chip command completion status accessible with single PCI-X burst access
- I/O port access to register space

1.1.3 Serial ATA Features

- Integrated Serial ATA Link and PHY logic
- Compliant with Serial ATA 1.0 and Serial ATA II Extensions to Serial ATA 1.0 Specifications
- Supports Serial ATA Generation 2 transfer rate of 3.0 Gb/s
- Supports Serial ATA II: Port Multiplier 1.0 Specifications
- Plesiochronous, Single PLL architecture, 1 PLL for 4 ports
- Output Swing Control
- Supports four independent Serial ATA channels
  - Independent Link, Transport, and data FIFO
  - Independent command fetch, scatter/gather, and command execution
    - Hard coded state machines – no code space or download
  - Supports Legacy Command Queuing (LCQ)
  - Supports Native Command Queuing (NCQ)
  - Supports Non-zero offsets NCQ
  - Supports Out of order data delivery NCQ
  - Supports FIS-based switching with Port Multipliers
- 31 Commands and Scatter/Gather Tables per Port on-chip
- Supports asynchronous notification
- Protocol Override per Command
- Staggered Spin-up Control
- Supports Far End Retimed Loopback BIST

1.2 References

- Serial ATA / High Speed Serialized AT Attachment specification, Revision 1.0
- Serial ATA II: Extensions to Serial ATA 1.0 Specification
- PCI Local Bus Specification Revision 2.3
- PCI-X Addendum to the Local PCI Bus Specification Revision 1.0a
- Serial ATA II: Port Multiplier 1.0 Specification

2 Electrical Characteristics

2.1 Device Electrical Characteristics

Specifications are for Commercial Temperature range, 0°C to +70°C, unless otherwise specified.

Symbol	Parameter	Ratings	Unit
VDDO	I/O Supply Voltage	4.0	V
VDDD	Core Supply Voltage	2.15	V
VDDRX VDDTX VDDPLL	Supply Voltage for S-ATA Receivers, Transmitters, PLLs and crystal circuitry respectively	2.15	V
V_{PCI_IN}	Input Voltage for PCI signals	-0.3 ~ 6.0	V
V_{NONPCI_IN}	Input Voltage for Non-PCI signals	-0.3 ~ VDDO+0.3	V
V_{CLKI_IN}	Input Voltage for CLKI	-0.3 ~ VDDRX+0.3	V
I_{OUT}	DC Output Current	16	mA
θ_{JA}	Thermal Resistance, Junction to Ambient, Still Air	17.6	°C/W
T_{STG}	Storage Temperature	-65 ~ 150	°C

Table 2-1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Type	Limits			Unit
				Min	Typ	Max	
VDDD	Core Supply Voltage	-	-	1.71	1.8	1.89	V
VDDRX	S-ATA Receiver and crystal Supply Voltage	-	-				
VDDTX	S-ATA Transmitter Supply Voltage	-	-				
VDDPLLA	SerDes PLL Supply Voltage	-	-				
VDDPLLB	PCI Deskew PLL Supply Voltage	-	-				
VDDO	Supply Voltage(I/O)	-	-	3.0	3.3	3.6	V
$IDD_{3.3V}$	Supply Current (3.3V Supply)	C_{LOAD}=20pF Activity LEDs off	-	-	70[1]	180[2]	mA
$IDD_{1.8V-3G}$	Supply Current (1.8V Supply)	3GHz Operating	-	-	690[1]	870[2]	mA
$IDD_{1.8V-1.5G}$	Supply Current (1.8V Supply)	1.5GHz Operating	-	-	570[1]	720[2]	mA
V_{IH}	Input High Voltage	-	3.3V PCI	0.5xVDDO	-	-	V
		-	Non-PCI	2.0	-	-	
V_{IL}	Input Low Voltage	-	3.3V PCI	-	-	0.3xVDDO	V
		-	Non-PCI	-	-	0.8	
V+	Input High Voltage	-	Schmitt	-	1.8	2.3	V
V-	Input Low Voltage	-	Schmitt	0.5	0.9	-	V
V_H	Hysteresis Voltage	-	Schmitt	0.4	-	-	V
I_{IH}	Input High Current	V_{IN} = VDD	-	-10	-	10	µA
I_{IL}	Input Low Current	V_{IN} = VSS	-	-10	-	10	µA
V_{OH}	Output High Voltage	I_{OUT}=-500uA	3.3V PCI	0.9xVDDO	-	-	V
		-	Non-PCI	2.4	-	-	
V_{OL}	Output Low Voltage	I_{OUT}=1500uA	3.3V PCI	-	-	0.1xVDDO	V

			Non-PCI	-	-	0.4	
Symbol	**Parameter**	**Condition**	**Type**	**Limits**			**Unit**
				Min	**Typ**	**Max**	
I_{ILOD}	Open Drain output sink current	-	-	-	-	12	mA
I_{OZ}	3-State Leakage Current	-	-	-10	-	10	µA

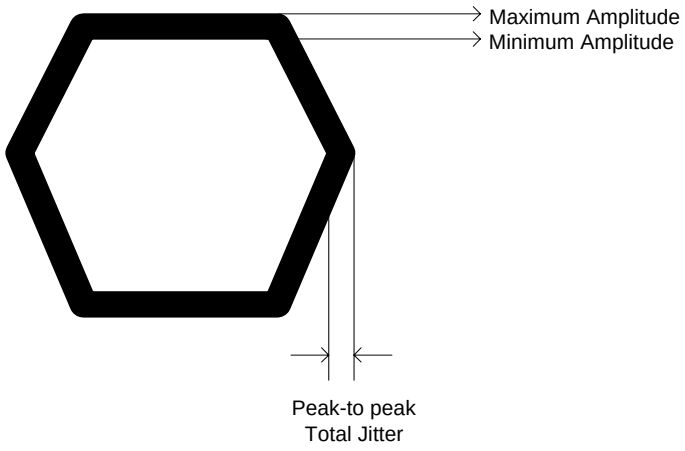
Notes: [1] Using the random data pattern (read/write operation) at 1.8V or 3.3V power supply, PCI interface = 133MHz
[2] Using the maximum toggling data pattern (read/write operation) at 1.89V or 3.6V power supply , PCI interface = 133MHz

Table 2-2 DC Specifications

Symbol	**Parameter**	**Condition**	**Limits**			**Unit**
			Min	**Typ**	**Max**	
V_{DOUT}	TX+/TX- differential peak-to-peak voltage swing.	Terminated by 50 Ohms. BAR1 1050h [4:0] = 0x0C[1]	400	500	700	mV
V_{DIN}	RX+/RX- differential peak-to-peak input sensitivity		240			mV
V_{SQ}	RX+/RX- OOB Signal Detection Threshold		50	125	240	mV
V_{DOH}	TX+/TX-differential Output common-mode voltage	Must be AC coupled	V_{DD}-375	V_{DD}-250	V_{DD}-125	mV
V_{ACCM}	Tx AC common-mode voltage				50	mV
V_{DIH}	RX+/RX- differential Input common-mode voltage	Must be AC coupled	-50	0	50	mV
Z_{DIN}	Tx Pair Differential impedance	REXT = 1k 1% for 25MHz CLKI REXT = 4.99k 1% for 100MHz CLKI	85	100	115	ohms
Z_{DOUT}	Rx Pair Differential impedance	REXT=1k, 1% for 25MHz CLKI REXT=4.99k, 1% for 100MHz CLKI	85	100	115	ohms
Z_{SIN}	Tx Single-Ended impedance	REXT=1k, 1% for 25MHz CLKI REXT=4.99k, 1% for 100MHz CLKI	40			ohms
Z_{SOUT}	Rx Single-Ended impedance	REXT=1k, 1% for 25MHz CLKI REXT=4.99k, 1% for 100MHz CLKI	40			ohms

Notes: [1] 0x0C is a reset value. S

Table 2-3 SATA Interface DC Specifications



Eye Diagram

2.2 SATA Interface Timing Specifications

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$T_{TX\_RISE\_FALL}$	Rise and Fall time at transmitter	20%-80% at Gen 1 20%-80% at Gen 2	100 67		273 136	ps
$T_{TX\_TOL\_FREQ}$	Tx Frequecny Long Term Stability		-350		+350	ppm
$T_{TX\_AC\_FREQ}$	Tx Spread-Sprectrum Modulation Deviation	CLKI = SSC AC modulation, subject to the "Downspread SSC" triangular modulation (30-33KHz) profile per 6.6.4.5 in SATA 1.0 specification	-5000		+0	ppm
T_{TX_SKEW}	Tx Differential Skew				15	ps

Table 2-4 SATA Interface Timing Specifications

2.3 SATA Interface Transmitter Output Jitter Characteristics

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
TJ_{5UI_15G}	Total Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		65		ps
DJ_{5UI_15G}	Deterministic Jitter, Data-Data 5UI	Measured at Tx output pins peak to peak phase variation Random data pattern		30		ps
TJ_{250UI_15G}	Total Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		85		ps
DJ_{250UI_15G}	Deterministic Jitter, Data-Data 250UI	Measured at Tx output pins peak to peak phase variation Random data pattern		40		ps

Table 2-5 SATA Interface Transmitter Output Jitter Characteristics, 1.5 Gb/s

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
$TJ_{fBAND/10\_3G}$	Total Jitter, $f_{C3dB}=f_{BAUD}/10$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		70		ps
$DJ_{fBAND/10\_3G}$	Deterministic Jitter, $f_{C3dB}=f_{BAUD}/10$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		30		ps
$TJ_{fBAND/500\_3G}$	Total Jitter, $f_{C3dB}=f_{BAUD}/500$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		85		ps
$DJ_{fBAND/500\_3G}$	Deterministic Jitter, $f_{C3dB}=f_{BAUD}/500$	Measured at SATA Compliance Point Random data pattern Load = LL Laboratory Load		45		ps

Table 2-6 SATA Interface Transmitter Output Jitter Characteristics, 3 Gb/s

2.4 CLKI SerDes Reference Clock Input Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
T_{CLKI_FREQ}	Nominal Frequency	REXT = 1k 1% REXT = 4.99k 1%		25 100		MHz
V_{CLKI_IH}	Input High Voltage	-	0.7xVDDRX			V
V_{CLKI_IL}	Input Low Voltage	-			0.3xVDDRX	V
T_{CLKI_J}	CLKI frequency tolerance	-	-50		+50	ppm
$T_{CLKI\_RISE\_FALL}$	Rise and Fall time at CLKI	25MHz reference, 20%-80%			4	ns
		100MHz reference, 20%-80%			2	
T_{CLKI_RJ}	Random Jitter	Measured at CLKI pin 10^{-12} Bit Error Ratio 1 sigma deviation			50	psrms
T_{CLKI_TJ}	Total Jitter	Measured at CLKI pin 10^{-12} Bit Error Ratio peak-to-peak phase noise			1	ns
$T_{CLKI\_RC\_DUTY}$	CLKI duty cycle	20%-80%	40		60	%

Table 2-7 CLKI SerDes Reference Clock Input Requirements

2.5 Power Supply Noise Requirements

Symbol	Parameter	Condition	Limits			Unit
			Min	Typ	Max	
V_{NOISE_VDDA}	1.8V Analog Power Noise	peak-to-peak sinewave across 500KHz to 3GHz frequency range. Measured with differential probe trigger by nois source (CLKI and PCI_CLK)			50	mV
V_{NOISE_VDDD}	1.8V Digital Power Noise				100	mV
V_{NOISE_VDDO}	3.3V IO Power Noise				200	mV

Table 2-8 Power Supply Noise Requirements

2.6 PCI 33 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	2.0	11.0	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	2.0	11.0	ns
T_{ON}	Float to Active Delay	2.0	-	ns
T_{OFF}	Active to Float Delay	-	28.0	ns
T_{SU}	Input Setup Time – Bussed Signals	7.0	-	ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	10.0	-	ns
T_{H}	Input Hold Time	0.0	-	ns

Table 2-9 PCI 33 MHz Timing Specifications

2.7 PCI 66 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	2.0	6.0	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	2.0	6.0	ns
T_{ON}	Float to Active Delay	2.0		ns
T_{OFF}	Active to Float Delay		14.0	ns
T_{SU}	Input Setup Time – Bussed Signals	3.0		ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	5.0		ns
T_{H}	Input Hold Time	0.0		ns

Table 2-10 PCI 66 MHz Timing Specifications

2.8 PCI-X 133 MHz Timing Specifications

Symbol	Parameter	Limits		Unit
		Min	Max	
T_{VAL}	CLK to Signal Valid – Bussed Signals	0.7	3.8	ns
$T_{VAL\ (PTP)}$	CLK to Signal Valid – Point to Point	0.7	3.8	ns
T_{ON}	Float to Active Delay	0.0		ns
T_{OFF}	Active to Float Delay		7.0	ns
T_{SU}	Input Setup Time – Bussed Signals	1.2		ns
$T_{SU\ (PTP)}$	Input Setup Time – Point to Point	1.2		ns
T_{H}	Input Hold Time	0.5		ns

Table 2-11 PCI-X 133 MHz Timing Specifications

3 Pin Definition

3.1 SiI3124 Pin Listing

This section describes the pin-out of the SiI3124 PCI-X to Serial ATA host controller. The table below gives the pin numbers, pin names, pin types, drive types where applicable, internal resistors where applicable, and descriptions. Power pins (VDDD, VDDO, VDDRX, VDDTX, VDDPLLA, VDDPLLB, VSSPLLB, VSSA, and VSSD) are excluded from this listing.

Table 3-1 SiI3124 Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
C1	RX3+	Diff In			Serial port 3 differential receiver + input
C2	RX3-	Diff In			Serial port 3 differential receiver – input
D1	TX3-	Diff Out			Serial port 3 differential transmitter – output
D2	TX3+	Diff Out			Serial port 3 differential transmitter + output
F1	RX2+	Diff In			Serial port 2 differential receiver + input
F2	RX2-	Diff In			Serial port 2 differential receiver – input
G1	TX2-	Diff Out			Serial port 2 differential transmitter – output
G2	TX2+	Diff Out			Serial port 2 differential transmitter + output
J4	REXT	Analog			External Reference Resistor
J1	XTALI/CLKI	Analog			Crystal or Clock Input
J2	XTALO	Analog			Crystal Output
L1	RX1+	Diff In			Serial port 1 differential receiver + input
L2	RX1-	Diff In			Serial port 1 differential receiver – input
M1	TX1-	Diff Out			Serial port 1 differential transmitter – output
M2	TX1+	Diff Out			Serial port 1 differential transmitter + output
P1	RX0+	Diff In			Serial port 0 differential receiver + input
P2	RX0-	Diff In			Serial port 0 differential receiver – input
R1	TX0-	Diff Out			Serial port 0 differential transmitter – output
R2	TX0+	Diff Out			Serial port 0 differential transmitter + output
U1	P_CLK	PCI			PCI Clock
Y2	LED0	OD	12 mA		Channel 0 activity LED indicator
Y1	LED1	OD	12 mA		Channel 1 activity LED indicator
W2	LED2	OD	12 mA		Channel 2 activity LED indicator
W1	LED3	OD	12 mA		Channel 3 activity LED indicator
Y3	SCAN_MODE	I		PD-60K	Internal Scan Mode Control
W3	TRSTN	I-Schmitt		PU-70K	JTAG Test Reset
Y4	TCK	I-Schmitt			JTAG Test Clock
W4	TMS	I		PU-70K	JTAG Test Mode Select
V4	TDI	I		PU-70K	JTAG Test Data In
Y5	TDO	O	4 mA		JTAG Test Data Out
W5	P_INTB#	PCI			PCI Interrupt B
V5	P_INTA#	PCI			PCI Interrupt A
Y6	P_INTD#	PCI			PCI Interrupt D
W6	P_INTC#	PCI			PCI Interrupt C
U6	P_RST#	PCI			PCI Reset
U7	P_GNT#	PCI			PCI Bus Grant
Y7	P_REQ#	PCI			PCI Bus Request
Y8	P_AD31	PCI			PCI Address/Data bit 31
U8	P_AD30	PCI			PCI Address/Data bit 30
W8	P_AD29	PCI			PCI Address/Data bit 29
W9	P_AD28	PCI			PCI Address/Data bit 28
Y9	P_AD27	PCI			PCI Address/Data bit 27
U9	P_AD26	PCI			PCI Address/Data bit 26

Table 3-1 SiI3124 Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
Y10	P_AD25	PCI			PCI Address/Data bit 25
U10	P_AD24	PCI			PCI Address/Data bit 24
W10	P_CBEN3	PCI			PCI Command/Byte Enable 3
W11	P_IDSEL	PCI			PCI Initialization Device Select
Y11	P_AD23	PCI			PCI Address/Data bit 23
U11	P_AD22	PCI			PCI Address/Data bit 22
Y12	P_AD21	PCI			PCI Address/Data bit 21
U12	P_AD20	PCI			PCI Address/Data bit 20
W12	P_AD19	PCI			PCI Address/Data bit 19
W13	P_AD18	PCI			PCI Address/Data bit 18
Y13	P_AD17	PCI			PCI Address/Data bit 17
U13	P_AD16	PCI			PCI Address/Data bit 16
Y14	P_CBEN2	PCI			PCI Command/Byte Enable 2
W14	P_IRDY	PCI			PCI Initiator Ready
U14	P_FRAME#	PCI			PCI Frame
Y15	P_LOCK#	PCI			PCI Lock
W15	P_DEVSEL	PCI			PCI Device Select
U15	P_STOP	PCI			PCI Stop
Y16	P_SERR#	PCI			PCI System Error
W16	P_PERR#	PCI			PCI Parity Error
U16	P_TRDY	PCI			PCI Target Ready
Y17	P_CBEN1	PCI			PCI Command/Byte Enable 1
W17	P_PAR	PCI			PCI Parity for lower half of 64-bit bus
U17	P_AD15	PCI			PCI Address/Data bit 15
Y18	P_AD14	PCI			PCI Address/Data bit 14
W18	P_AD13	PCI			PCI Address/Data bit 13
V20	P_AD12	PCI			PCI Address/Data bit 12
V19	P_AD11	PCI			PCI Address/Data bit 11
U20	P_AD10	PCI			PCI Address/Data bit 10
U19	P_AD9	PCI			PCI Address/Data bit 9
T20	M66EN	PCI			PCI 66 MHz Enable
T19	P_AD8	PCI			PCI Address/Data bit 8
T17	P_CBEN0	PCI			PCI Command/Byte Enable 0
R20	P_AD7	PCI			PCI Address/Data bit 7
R17	P_AD6	PCI			PCI Address/Data bit 6
R19	P_AD5	PCI			PCI Address/Data bit 5
P19	P_AD4	PCI			PCI Address/Data bit 4
P20	P_AD3	PCI			PCI Address/Data bit 3
P17	P_AD2	PCI			PCI Address/Data bit 2
N20	P_AD1	PCI			PCI Address/Data bit 1
N17	P_AD0	PCI			PCI Address/Data bit 0
N19	P_ACK64	PCI			PCI 64-Bit Bus Acknowledge
M20	P_CBEN6	PCI			PCI Command/Byte Enable 6
M19	P_CBEN7	PCI			PCI Command/Byte Enable 7
M17	P_REQ64	PCI			PCI 64-Bit Bus Request
L20	P_CBEN4	PCI			PCI Command/Byte Enable 4
L19	P_CBEN5	PCI			PCI Command/Byte Enable 5
L17	P_PAR64	PCI			PCI Parity for upper half of 64-bit bus
K20	P_AD63	PCI			PCI Address/Data bit 63
K17	P_AD62	PCI			PCI Address/Data bit 62
K19	P_AD61	PCI			PCI Address/Data bit 61
J19	P_AD60	PCI			PCI Address/Data bit 60
J20	P_AD59	PCI			PCI Address/Data bit 59

Table 3-1 SiI3124 Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
J17	P_AD58	PCI			PCI Address/Data bit 58
H20	P_AD57	PCI			PCI Address/Data bit 57
H17	P_AD56	PCI			PCI Address/Data bit 56
H19	P_AD55	PCI			PCI Address/Data bit 55
G19	P_AD54	PCI			PCI Address/Data bit 54
G20	P_AD53	PCI			PCI Address/Data bit 53
G17	P_AD52	PCI			PCI Address/Data bit 52
F20	P_AD51	PCI			PCI Address/Data bit 51
F17	P_AD50	PCI			PCI Address/Data bit 50
F19	P_AD49	PCI			PCI Address/Data bit 49
E19	P_AD48	PCI			PCI Address/Data bit 48
E20	P_AD47	PCI			PCI Address/Data bit 47
E17	P_AD46	PCI			PCI Address/Data bit 46
D20	P_AD45	PCI			PCI Address/Data bit 45
D19	P_AD44	PCI			PCI Address/Data bit 44
C20	P_AD43	PCI			PCI Address/Data bit 43
C19	P_AD42	PCI			PCI Address/Data bit 42
B20	P_AD41	PCI			PCI Address/Data bit 41
D17	P_AD40	PCI			PCI Address/Data bit 40
A19	P_AD39	PCI			PCI Address/Data bit 39
B18	P_AD38	PCI			PCI Address/Data bit 38
A18	P_AD37	PCI			PCI Address/Data bit 37
B17	P_AD36	PCI			PCI Address/Data bit 36
A17	P_AD35	PCI			PCI Address/Data bit 35
B16	P_AD34	PCI			PCI Address/Data bit 34
A16	P_AD33	PCI			PCI Address/Data bit 33
D16	P_AD32	PCI			PCI Address/Data bit 32
A15	FL_DATA0	I/O	8 mA	PU-70K	Flash Memory Data 0
B15	FL_DATA1	I/O	8 mA	PU-70K	Flash Memory Data 1
D15	FL_DATA2	I/O	8 mA	PU-70K	Flash Memory Data 2
A14	FL_DATA3	I/O	8 mA	PU-70K	Flash Memory Data 3
B14	FL_DATA4	I/O	8 mA	PU-70K	Flash Memory Data 4
D14	FL_DATA5	I/O	8 mA	PU-70K	Flash Memory Data 5
A13	FL_DATA6	I/O	8 mA	PU-70K	Flash Memory Data 6
B13	FL_DATA7	I/O	8 mA	PU-70K	Flash Memory Data 7
D13	FL_AD0	I/O	8 mA	PU-70K	Flash Memory Address 0
A12	FL_AD1	I/O	8 mA	PU-70K	Flash Memory Address 1
B12	FL_AD2	I/O	8 mA	PU-70K	Flash Memory Address 2
D12	FL_AD3	I/O	8 mA	PU-70K	Flash Memory Address 3
A11	FL_AD4	I/O	8 mA	PU-70K	Flash Memory Address 4
B11	FL_AD5	I/O	8 mA	PU-70K	Flash Memory Address 5
D11	FL_AD6	I/O	8 mA	PU-70K	Flash Memory Address 6
A10	FL_AD7	I/O	8 mA	PU-70K	Flash Memory Address 7
B10	FL_AD8	I/O	8 mA	PU-70K	Flash Memory Address 8
D10	FL_AD9	I/O	8 mA	PU-70K	Flash Memory Address 9
A9	FL_AD10	I/O	8 mA	PU-70K	Flash Memory Address 10
B9	FL_AD11	I/O	8 mA	PU-70K	Flash Memory Address 11
D9	FL_AD12	I/O	8 mA	PU-70K	Flash Memory Address 12
A8	FL_AD13	I/O	8 mA	PU-70K	Flash Memory Address 13
B8	FL_AD14	I/O	8 mA	PU-70K	Flash Memory Address 14
D8	FL_AD15	I/O	8 mA	PU-70K	Flash Memory Address 15
A7	FL_AD16	I/O	8 mA	PU-70K	Flash Memory Address 16
B7	FL_AD17	I/O	8 mA	PU-70K	Flash Memory Address 17

Table 3-1 SiI3124 Pin Listing

Pin #	Pin Name	Type	Drive	Internal Resistor	Description
D7	FL_AD18	I/O	8 mA	PU-70K	Flash Memory Address 18
A6	FL_RD	I/O	8 mA	PU-70K	Flash Memory Read Strobe
B6	FL_WR	I/O	8 mA	PU-70K	Flash Memory Write Strobe
D6	FL_CS	I/O	8 mA	PU-70K	Flash Memory Chip Select
A5	PHYTESTC	I/O	4 mA	PU-70K	PHY Test pin; no connection required
B5	I2C_SCLK	I/O	4 mA	PU-70K	I^2C Serial Clock
D5	I2C_SDAT	I/O	4 mA	PU-70K	I^2C Serial Data
C4	PHYTESTD	I/O	4 mA	PU-70K	PHY Test pin; no connection required

Table 3-2 Pin Types	
Pin Type	**Pin Description**
I	Input Pin with LVTTL Thresholds
I-Schmitt	Input Pin with Schmitt Trigger
O	Output Pin
PCI	PCI(X) Compliant Bi-directional Pin
I/O	Bi-directional Pin
OD	Open Drain Output Pin

3.2 SiI3124 Ball Mapping

The diagram below shows the ball mapping for the SiI3124. Some signal names have been abbreviated to fit.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	N/C	N/C	N/C	N/C	PHY TESTC	FL_RD	FL_AD16	FL_AD13	FL_AD10	FL_AD7	FL_AD4	FL_AD1	FL_DATA6	FL_DATA3	FL_DATA0	P_AD33	P_AD35	P_AD37	P_AD39	VSSD	A
B	VSSA	VSSA	VSSA	VSSA	I2C_SCLK	FL_WR	FL_AD17	FL_AD14	FL_AD11	FL_AD8	FL_AD5	FL_AD2	FL_DATA7	FL_DATA4	FL_DATA1	P_AD34	P_AD36	P_AD38	VSSD	P_AD41	B
C	RX3+	RX3-	VDD RX23	PHY TESTD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	P_AD42	P_AD43	C
D	TX3-	TX3+	VSSA	VSSA	I2C_SDAT	FL_CS	FL_AD18	FL_AD15	FL_AD12	FL_AD9	FL_AD6	FL_AD3	FL_AD0	FL_DATA5	FL_DATA2	P_AD32	P_AD40	VSSD	P_AD44	P_AD45	D
E	VDD RX23	VSSA	VDD RX23	VSSA	VSSA	NC	NC	VDDO	VDDO	VDDO	VDDD	VDDD	VDDD	VDDD	VDDD	VDDD	P_AD46	VSSD	P_AD48	P_AD47	E
F	RX2+	RX2-	VSSA	VDD RX23	VSSA											VDDD	P_AD50	VSSD	P_AD49	P_AD51	F
G	TX2-	TX2+	VDD TX23	VSSA	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_AD52	VSSD	P_AD54	P_AD53	G
H	VSSA	VDD TX23	VSSA	VDD TX23	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_AD56	VSSD	P_AD55	P_AD57	H
J	XTALI	XTALO	VDD PLLA	REXT	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_AD58	VSSD	P_AD60	P_AD59	J
K	VSSA	VDD PLLA	VSSA	VSSA	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_AD62	VSSD	P_AD61	P_AD63	K
L	RX1+	RX1-	VDD RX01	VSSA	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_PAR64	VSSD	P_CBEN5	P_CBEN4	L
M	TX1-	TX1+	VSSA	VDD RX01	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_REQ64	VSSD	P_CBEN7	P_CBEN6	M
N	VDD RX01	VSSA	VDD RX01	VSSA	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_AD0	VSSD	P_ACK64	P_AD1	N
P	RX0+	RX0-	VSSA	VDD TX01	VSSA		VSSA	VSSA	VSSA	VSSD	VSSD	VSSD	VSSD	VSSD		VDDO	P_AD2	VSSD	P_AD4	P_AD3	P
R	TX0-	TX0+	VDD TX01	VSSA	VSSA											VDDD	P_AD6	VSSD	P_AD5	P_AD7	R
T	VSSA	VDD TX01	VSSA	VSSA	VSSA	VDDO	VDDO	VDDO	VDDO	VDDO	VDDO	VDDD	VDDD	VDDD	VDDD	VDDD	P_CBEN0	VSSD	P_AD8	M66EN	T
U	P_CLK	VSS PLLB	VDD PLLB	VSS PLLB	VSS PLLB	P_RST#	P_GNT#	P_AD30	P_AD26	P_AD24	P_AD22	P_AD20	P_AD16	P_FRAME#	P_STOP	P_TRDY	P_AD15	VSSD	P_AD9	P_AD10	U
V	VSS PLLB	VDD PLLB	VSS PLLB	TDI	P_INTA#	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	VSSD	P_AD11	P_AD12	V
W	LED3	LED2	TRSTN	TMS	P_INTB#	P_INTC#	VSSD	P_AD29	P_AD28	P_CBEN3	P_IDSEL	P_AD19	P_AD18	P_IRDY	P_DEVSEL	P_PERR#	P_PAR	P_AD13	VSSD	VSSD	W
Y	LED1	LED0	SCAN_MODE	TCK	TDO	P_INTD#	P_REQ#	P_AD31	P_AD27	P_AD25	P_AD23	P_AD21	P_AD17	P_CBEN2	P_LOCK#	P_SERR#	P_CBEN1	P_AD14	VSSD	VSSD	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 3-1 Ball Mapping Diagram

3.3 SiI3124 Pin Descriptions

3.3.1 PCI(X) Pins

Signal Name	Pin Number(s)	Description
PCI_AD[63:0]	K20, K17, K19, J19, J20, J17, H20, H17, H19, G19, G20, G17, F20, F17, F19, E19, E20, E17, D20, D19, C20, C19, B20, D17, A19, B18, A18, B17, A17, B16, A16, D16, Y8, U8, W8, W9, Y9, U9, Y10, U10, Y11, U11, Y12, U12, W12, W13, Y13, U13, U17, Y18, W18, V20, V19, U20, U19, T19, R20, R17, R19, P19, P20, P17, N20, N17	**Address/Attribute/Data.** PCI_AD[63:0] is the multiplexed address/attribute/data bus. Each bus transaction consists of an address phase followed by an attribute phase (PCI-X only), then one ore more data phases.
PCI_CBEN[7:0]	M19, M20, L19, L20, W10, Y14, Y17, T17	**Command/Byte Enable.** PCI_CBEN is the multiplexed command/byte-enable bus. During the address phase this bus carries the command. During the attribute phase (PCI-X only) PCI_CBEN[3:0] carries the upper 4 bits of the byte count. During the data phase this bus carries byte enables.
PCI_IDSEL	W11	**Initialization Device Select.** This is the chip select for configuration read/write operations.
PCI_FRAME_N	U14	**Frame.** PCI_FRAME_N is asserted to indicate the beginning of a bus operation. It is deasserted when the transaction is in the final data phase or has completed.
PCI_IRDY_N	W14	**Initiator Ready.** PCI_IRDY_N is asserted by a bus master to indicate that it can complete a data transaction.
PCI_TRDY_N	U16	**Target Ready.** PCI_TRDY_N is asserted by a target to indicate that it can complete the current data transaction.
PCI_DEVSEL_N	W15	**Device Select.** PCI_DEVSEL_N is asserted to indicate that the target has decoded its own address or a Split Completion cycle (PCI-X only).
PCI_STOP_N	U15	**Stop.** PCI_STOP_N indicates the current target is requesting that the master stop the current transaction.
PCI_LOCK_N	Y15	**Lock.** PCI_LOCK_N indicates that the current transaction on the PCI bus needs to be a Locked transaction.
PCI_REQ_N	Y7	**Request.** PCI_REQ_N indicates to the system arbiter that the SiI3124 wants to gain control of the PCI bus to perform a transaction.
PCI_GNT_N	U7	**Grant.** PCI_GNT_N indicates that the SiI3124 has been given control of the bus to perform a transaction.
PCI_REQ64_N	M17	**Request64.** PCI_REQ64_N is asserted by a bus master to request a 64-bit transaction.
PCI_ACK64_N	N19	**Acknowledge64.** PCI_ACK64_N is asserted by a target to acknowledge that a 64-bit transaction is accepted.
PCI_PAR	W17	**Parity.** PCI_PAR carries even parity covering the PCI_AD[31:0] and PCI_CBEN[3:0] buses.
PCI_PAR64	L17	**Parity.** PCI_PAR64 carries even parity covering the PCI_AD[63:32] and PCI_CBEN[7:4] buses.
PCI_PERR_N	W16	**Parity Error.** PCI_PERR_N indicates the detection of a data parity error.
PCI_SERR_N	Y16	**System Error.** PCI_SERR_N indicates detection of an address or attribute parity error or of any other system error where the result will be catastrophic.

PCI_INTA_N, PCI_INTB_N, PCI_INTC_N, PCI_INTD_N	V5, W5, W6, Y6	**Interrupt.** PCI_INTA_N is asserted to request a system interrupt. The other interrupt pins may be enabled by means outside that specified by the PCI specification (see description for Port Interrupt Enable register).
PCI_CLK	U1	**Clock.** PCI_CLK is the reference clock for all PCI interface signals except PCI_RST_N and PCI_INTA_N.
PCI_RST_N	U6	**Reset.** PCI_RST_N initializes the PCI interface and sets internal registers to their initial state. All PCI outputs are tri-stated while PCI_RST_N is active.
M66EN	T20	**PCI 66 MHz Enable.**

3.3.2 Flash / I²C Pins

Signal Name	Pin Number(s)	Description
FL_ADDR[18:00]	D7, B7, A7, D8, B8, A8, D9, B9, A9, D10, B10, A10, D11, B11, A11, D12, B12, A12, D13	**Flash Address.** FL_ ADDR[18:00] is the Flash Memory address for up to 512K of Flash Memory.
FL_DATA[07:00]	B13, A13, D14, B14, A14, D15, B15, A15	**Flash Data.** 8-bit Flash memory data bus
FL_RD_N	A6	**Flash Read Enable.** Active low
FL_WR_N	B6	**Flash Write Enable.** Active low
FL_CS_N	D6	**Flash Chip Select.** Active low
I2C_SDAT	D5	**I²C Serial Data.** Serial Interface (I²C) data line
I2C_SCLK	B5	**I²C Serial Clock.** Serial Interface (I²C) clock

3.3.3 Serial ATA Signals

Signal Name	Pin Number(s)	Description
Rx[3:0]+	C1, F1, L1, P1	**Receive +.** Serial receiver differential signal, positive side.
Rx[3:0]-	C2, F2, L2, P2	**Receive -.** Serial receiver differential signal, negative side.
Tx[3:0]+	D2, G2, M2, R2	**Transmit +.** Serial transmitter differential signal, positive side.
Tx[3:0]-	D1, G1, M1, R1	**Transmit -.** Serial transmitter differential signal, negative side.
XTALI/CLKI	J1	**Crystal In.** Crystal oscillator pin for SerDes reference clock. When external clock source is selected, the external clock (either 25MHz or 100 MHz) will come in through this pin. The clock must be 1.8V swing and the precision recommendation is ±50ppm.
XTALO	J2	**Crystal Out.** Crystal oscillator pin for SerDes reference clock. A 25MHz crystal must be used.
REXT	J4	**External Reference.** External reference resistor pin for termination calibration. This pin provides the additional function of selecting frequency of the clock source. For 25MHz, a 1K, 1% resistor is connected to ground. For 100MHz, a 4.99K, 1% resistor is connected to ground.

3.3.4 Test Pins

Signal Name	Pin Number(s)	Description
TMS	W4	**JTAG Test Mode Select**
TCK	Y4	**JTAG Test Clock**
TDI	V4	**JTAG Test Data In**
TDO	Y5	**JTAG Test Data Out**
TRSTN	W3	**JTAG Test Reset. This pin must be tied to ground if JTAG function is not used.**
SCAN_MODE	Y3	**Scan Mode. Used for factory testing; do not connect.**
PHYTESTD	C4	**PHY Test D. Used for factory testing; do not connect.**
PHYTESTC	A5	**PHY Test C. Used for factory testing; do not connect.**

3.3.5 NC Pins

Signal Name	Pin Number(s)	Description
NC	E7, E6	**No Connection**

3.3.6 Power/Ground Pins

All like-named power/ground pins, in the table below, are connected together within the package.

Pin Name	Pin Number(s)	Description
VSSA	B1, B2, B3, B4, D3, D4, E2, E4, E5, F3, F5, G4, G5, H1, H3, H5, J5, K1, K3, K4, K5, L4, L5, M3, M5, N2, N4, N5, P3, P5, R4, R5, T1, T3, T4, T5, G7, G8, G9, H7, H8, H9, J7, J8, J9, K7, K8, K9, L7, L8, L9, M7, M8, M9, N7, N8, N9, P7, P8, P9	**Analog Ground.** These pins provide the Ground reference for the analog (SerDes) portion of the chip.
VSSD	V6, V7, W7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, W19, Y19, W20, Y20, U18, T18, R18, P18, N18, M18, L18, K18, J18, H18, G18, F18, E18, D18, C18, B19, A20, C17, C16, C15, C14, C13, C12, C11, C10, C9, C8, C7, C6, C5, G10, G11, G12, G13, G14, H10, H11, H12, H13, H14, J10, J11, J12, J13, J14, K10, K11, K12, K13, K14, L10, L11, L12, L13, L14, M10, M11, M12, M13, M14, N10, N11, N12, N13, N14, P10, P11, P12, P13, P14	**Digital Ground.** These pins provide the Ground reference for the digital portion of the chip.
VSSPLLB	V1, U2, V3, U4, U5	**PLL Ground.** These pins provide the Ground reference for the PCI clock deskew PLL.
VDDRX01	L3, M4, N1, N3	**Receiver and XTAL Power.** These pins provide 1.8V for the Serial ATA receivers for Ports 0 and 1, and crystal oscillator.
VDDTX01	P4, R3, T2	**Transmitter Power.** These pins provide 1.8V for the Serial ATA transmitters for Ports 0 and 1.
VDDRX23	C3, E1, E3, F4	**Receiver and XTAL Power.** These pins provide 1.8V for the Serial ATA receivers for Ports 2 and 3, and crystal oscillator.
VDDTX23	G3, H2, H4	**Transmitter Power.** These pins provide 1.8V for the Serial ATA transmitters for Ports 2 and 3.
VDDPLLA	J3, K2	**PLL Power.** These pins provide 1.8V for the Serial ATA PLL and crystal oscillator.
VDDPLLB	U3, V2	**PLL Power.** These pins provide 1.8V for the PCI clock deskew PLL.
VDDD	T12, T13, T14, T15, T16, R16, F16, E16, E15, E14, E13, E12, E11	**Digital Power.** These pins provide 1.8V for the digital logic.
VDDO	T6, T7, T8, T9, T10, T11, P16, N16, M16, L16, K16, J16, H16, G16, E10, E9, E8	**I/O Power.** These pins provide 3.3V for the digital I/O.

4 Package Drawing

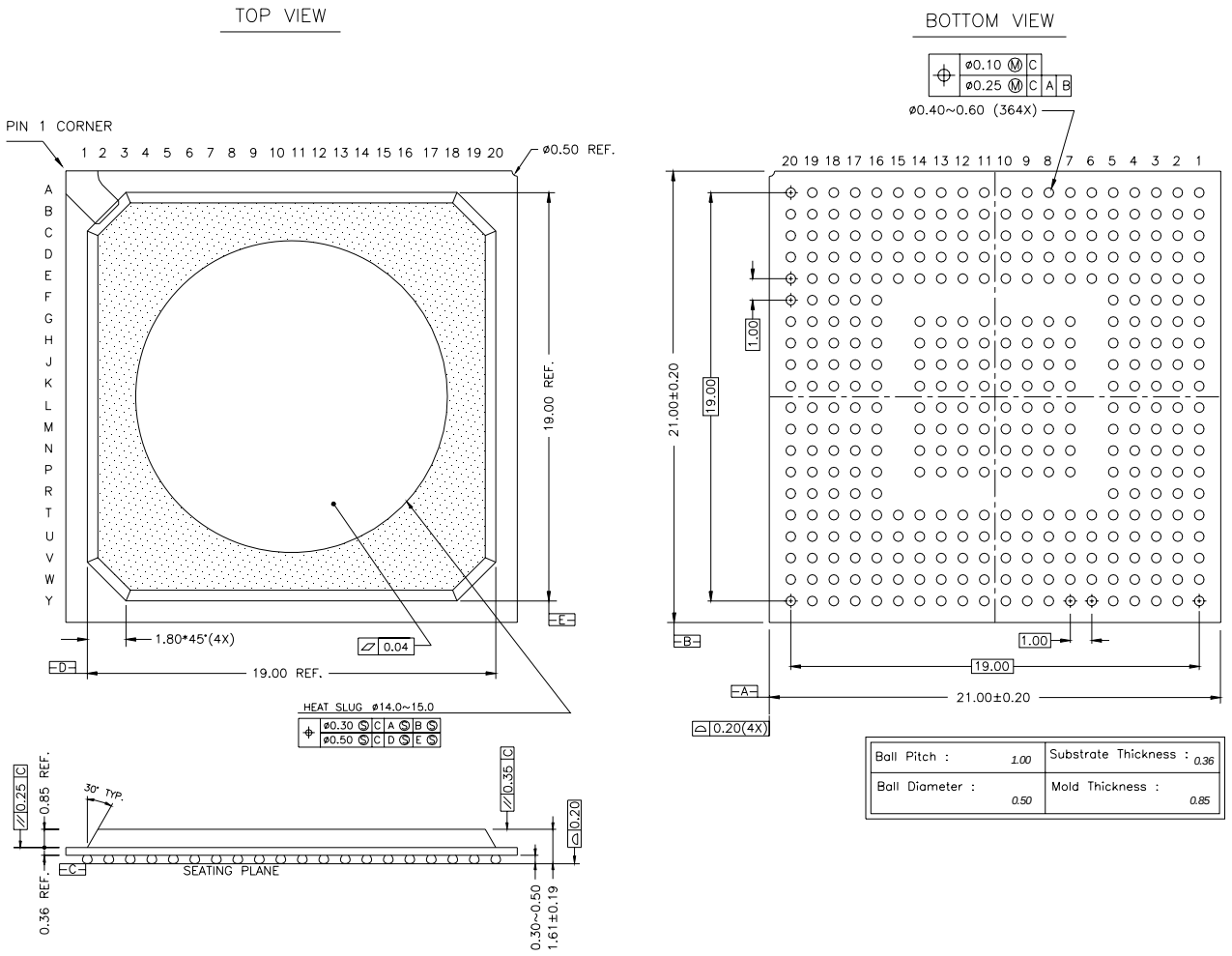


Figure 4-1 Package Drawing 364 BGA

Part Ordering Number:

SiI3124ACBHU (364 pin BGA green package)

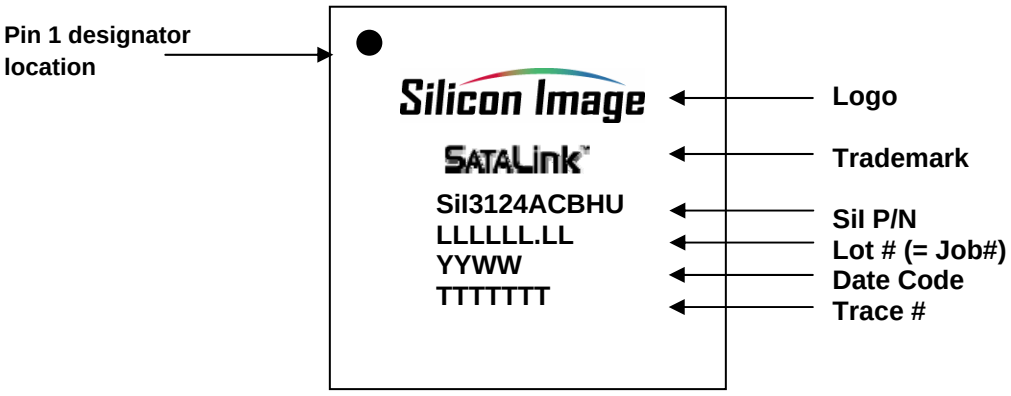


Figure 4-2 Marking Specification

5 Programming Model

5.1 SiI3124 Block Diagram

The SiI3124 contains the major logic modules shown below.

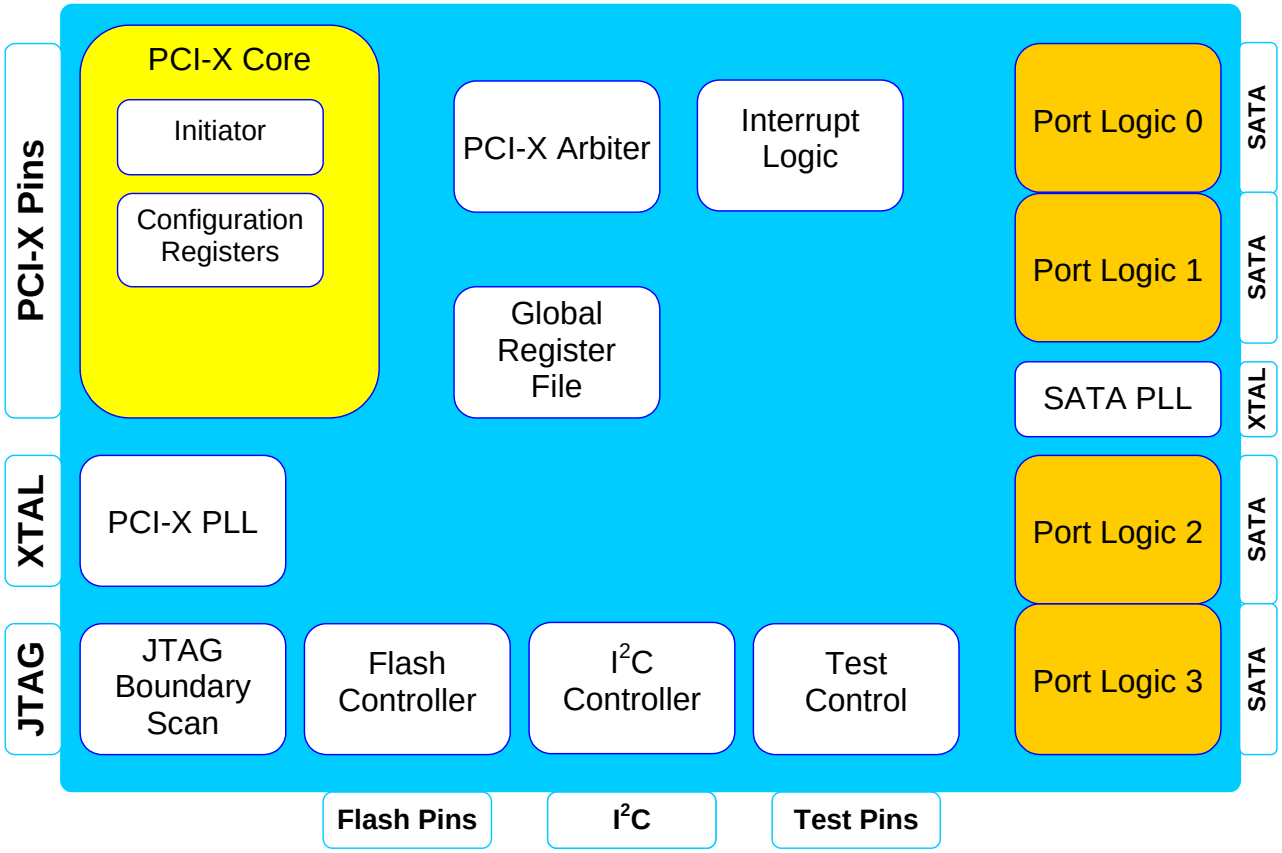


Figure 5-1: SiI3124 Block Diagram

The PCI-X Core logic block provides PCI 2.3 and PCI-X 1.0a compatibility. The PCI-X Arbiter logic block allows sharing of the PCI bus amongst the four Serial-ATA Ports. Similarly the Interrupt Logic block allows sharing of the four PCI interrupt signals amongst the Serial-ATA Ports. The Global Register File block corresponds to the registers addressed by Base Address Register 0; refer to Section 7.2, Internal Register Space – Base Address 0, on page 60.

The initialization function provided by the I^2C Controller and Flash Controller are described in Section 6, Auto-Initialization, on page 44.

5.2 SiI3124 S-ATA Port Block Diagram

The block diagram below shows the logic structure of each of the four SiI3124 Serial-ATA Ports.

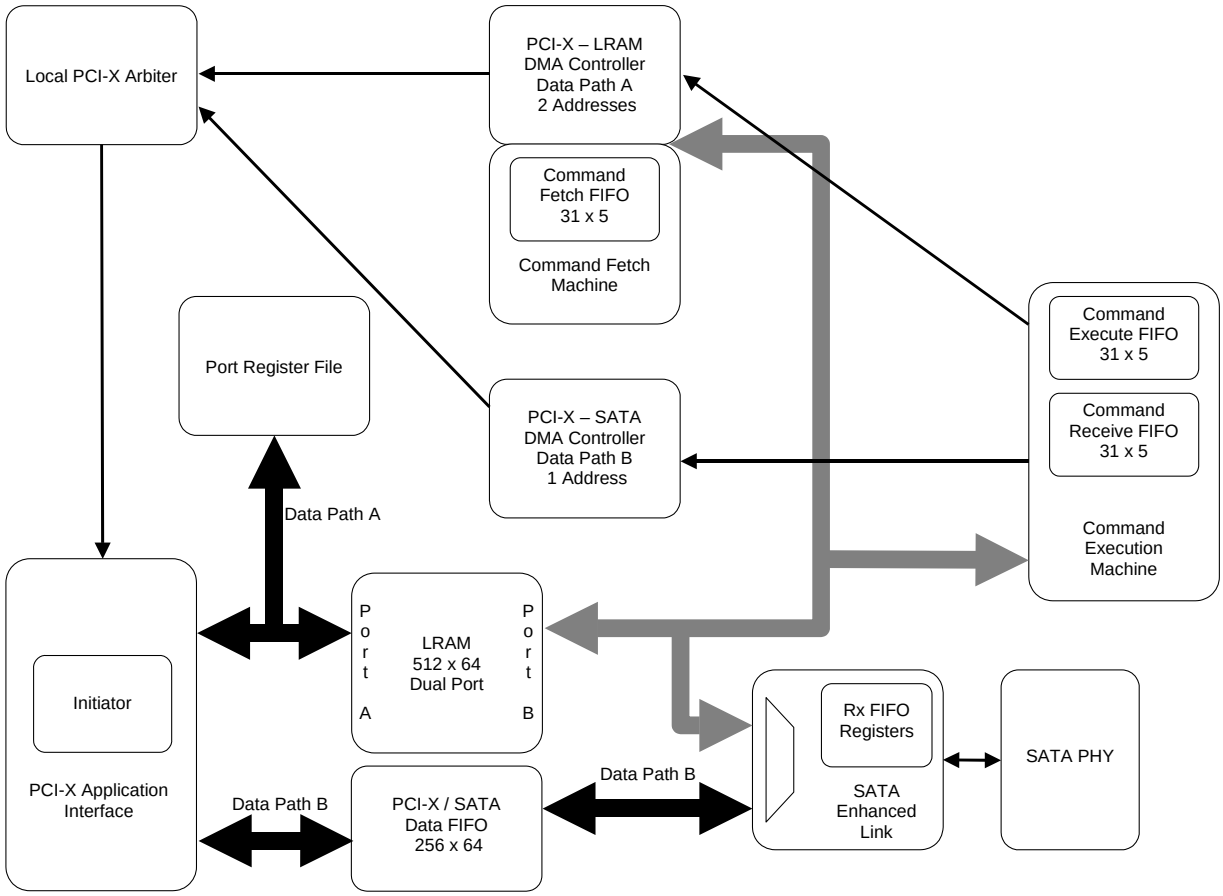


Figure 5-2 Port Logic Block Diagram

The Port Logic consists of:

- A Local PCI-X Arbiter that arbitrates between the two DMA Controllers
- A DMA Controller for the PCI-X to LRAM Data Path
- A DMA Controller for the PCI-X to Serial-ATA Data Path
- A 512x64 Local RAM (LRAM) that contains: 31 LRAM Slots each of which is 128 bytes (16 Qwords) and 128 bytes used to support 16 Port Multiplier devices (1 Qword per device)
- A Data FIFO that contains 2048 bytes (256 Qwords)
- A State Machine for Command Fetch
- A State Machine for Command Execution
- A Serial-ATA Link
- A Serial-ATA PHY

Each of the two state machines has an associated FIFO which, when non-empty, indicates that processing is required. The FIFO is loaded with a 5-bit command “slot” number to activate a state machine. The slot number can range from 0 to 30, corresponding to the maximum number of active commands supported.

Command flow begins with a host driver building a command in a non-cached region of host memory. The data structure is referred to as a PRB (Port Request Block). The 64-byte PRB is transferred into an available command slot in the LRAM by one of two methods: the direct method or the indirect method. The host driver is responsible for determining which slots are available. Either of the two command transfer methods may be used for each command transfer. The two methods are:

Direct Command Transfer Method – Host controlled write to Slot

In systems that have the capability to perform burst writes on the PCI-X bus, this is the preferred method of command transfer. Embedded systems would most likely use this method. LRAM is directly mapped through use of Base Address Register 1, and appears as a block of memory to the host driver. The host driver writes the PRB contents into the appropriate slot in LRAM. Ideally, this operation is performed as a single PCI-X burst transaction. The 5-bit slot number (0-30) is written to the *Command Execution FIFO*. The Active bit associated with the selected slot becomes set in the Port Slot Status register. Note that the *Command Fetch FIFO* and *Command Fetch State Machine* are not used for the direct method of command transfer.

Indirect Command Transfer Method – SiI3124 controlled command transfer as a PCI-X master

In systems that cannot guarantee burst write capability, such as PCs and servers, this method is more efficient, since the SiI3124 provides PCI-X burst capability. The host driver builds a PRB in host memory, selects a free slot, and writes the physical address of the PRB into the Activation register corresponding to the selected slot. This causes the SiI3124 to push the 5-bit slot number (0-30) into the *Command Fetch FIFO.* The *Command Fetch State Machine,* while in an idle state, continuously interrogates the *Command Fetch FIFO* for a "non-empty" condition. Upon retrieval of a 5-bit slot number from the FIFO, the *Command Fetch State Machine* retrieves the physical address of the PRB from the corresponding activation register*,* sets the Active bit associated with the selected slot in the Port Slot Status register, and queues a PCI-X master read of the PRB into the associated Slot in LRAM. The *Command Fetch State Machine* waits for completion of the transfer, pushes the 5-bit slot number into the *Command Execution FIFO,* and returns to the idle state, waiting for a non-empty condition in the *Command Fetch FIFO*.

The *Command Execution State Machine* is responsible for directing the flow of the command and response FISes between the command slot and the serial ATA link, directing the flow of data between the PCI-X bus and the serial ATA link, and posting completion status to the host. It is also responsible for error handling when exceptions occur in the normal command flow. Command execution begins when the idle *Command Execution State Machine* recognizes that the serial ATA bus is in a non-busy state and the *Command Execution FIFO* is non-empty. The *Command Execution State Machine* retrieves the 5-bit slot number (0-30) from the *Command Execution FIFO* and uses it to index the command slot in LRAM. The command FIS is addressed and sent to the serial ATA link to be sent to the device. Control flags in the command slot determine the type of data transfer. The *Command Execution State Machine* waits for a response FIS from the device and directs its activities accordingly. If the received FIS is a data FIS, the DMA address and count are determined by examining the Scatter/Gather Entries in the PRB and, if necessary, "walking" a Scatter/Gather Table. The DMA address and count are loaded into the DMA controller and the controller is armed. A DMA activate FIS causes similar behavior, with data flowing from the PCI-X bus to the serial ATA link. When the command has completed, the Command Completion bit in the Port Interrupt Status register is set to reflect the successful completion of the command. If an error occurred, the Command Error bit is set in the Port Interrupt Status register.

The basic command flow proceeds as follows:

1. The host builds a 64-byte Port Request Block (PRB) that contains:
   - The Register- Host to Device FIS to send to the SATA device
   - Up to two scatter/gather entries to define regions of host memory to be accessed for associated read/write data. Additional scatter/gather entries may be associated with the command.
   - Various optional control flags to direct the SiI3124 to perform special processing, control interrupt assertion, vary the normal protocol flow, etc.
2. The host issues the command to the SiI3124.
3. The SiI3124 executes the command, performing all interaction with the SATA device and transferring data between host memory and the SATA device as a PCI-X master.
4. The SiI3124 asserts a PCI-X interrupt to indicate command completion.
5. The host reads the SiI3124 port slot status to determine which command(s) have completed.

5.3 Data Structures

5.3.1 The Command Slot

Each port within the SiI3124 contains 31 command slots. The slots are numbered 0 through 30. Each command issued by the host occupies a single command slot. The host decides which slot to use and issues a command to the selected slot. A command slot occupies 128 bytes within the SiI3124 RAM array and consists of a 64 byte PRB (Port Request Block) and a 64-byte scatter/gather table. The host builds the PRB. It contains the Register-Host To Device FIS to transmit to the attached SATA device and up to two scatter/gather entries that define host memory regions to be used for any read/write data associated with the command. If more scatter/gather entries are required to define additional host memory regions, the SiI3124 will fetch them from host memory as needed. The host may simply append the additional SGT entries to the PRB, or one of the scatter/gather entries in the PRB may be used to define an SGT (scatter/gather table) that resides in host memory.

The host may issue commands to any number of available command slots. The host may freely intermix non-queued, legacy queued, native queued, PIO, and DMA command types in any available slot. Commands will always be executed in the order

that they were issued. The SiI3124 will enforce command type issuance to the SATA device and will not allow incompatible command types to be issued to a device. This relieves the host of the burden of making sure that incompatible command types are not intermixed in the device.

It is the host's responsibility to manage slot usage. The host must keep track of which slots have commands outstanding and which slots are available for new commands. Issuing a command to a slot that is currently in use will result in unpredictable behavior.

For queued commands, the slot number is used as the queue tag. It is the host's responsibility to ensure that the tag number in the Register-Host To Device FIS defined in the PRB matches the slot number to which the command is issued.

5.3.2 The Scatter/Gather Entry (SGE)

A scatter/gather entry (SGE) defines a region of host memory to be used for data transfer associated with a command. Each scatter/gather entry defines a single contiguous physically addressed region.

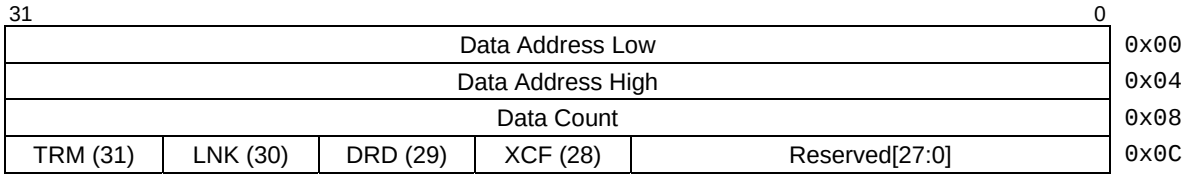


Table 5-1 Scatter/Gather Entry (SGE)

The first quadword, at offset 0, contains the physical address of the region in host memory. The entire 64-bit address must be defined. On 32-bit systems the upper 32 bits must be zero. The data address may point to a region to be used for data transfer, or it may point to a scatter/gather table (SGT), which is a collection of four SGEs. The LNK bit (bit 30 at offset 0x0c) defines the type of region. When LNK is zero, the region is a data region; when LNK is one, the region is a scatter/gather table that will be fetched by the SiI3124 to obtain a data region definition.

The Data Count field at offset 0x08 defines the length, in bytes, of the contiguous data region. When the LNK bit is set to one, indicating an SGT link, the SiI3124 ignores this field.

The TRM bit (bit 31 at offset 0x0c), when set to one, indicates that this is the final SGE associated with the command and no additional SGEs follow it.

The DRD bit (bit 29 at offset 0x0c), when set to one, directs the SiI3124 to discard the data read from the device for the length associated with the data count. When this bit is set to one, the SiI3124 ignores the data address.

The XCF bit (bit 28 at offset 0x0c) indicates whether the region defined by this SGE is to be used for data transfer (XCF set to zero) or an external command fetch (XCF set to one). See section 5.3.10 for additional information on external command processing.

5.3.3 The Scatter/Gather Table (SGT)

The SGT is simply a contiguous collection of four SGEs. The PRB contains two SGEs. When more than two SGEs are required to fully define the entire data transfer of a command, the SiI3124 fetches additional SGEs in groups of four at a time, or one SGT. The SGT occupies the upper 64 bytes of a command slot in SiI3124 RAM. When needed, only one SGT resides in RAM at a time. The SiI3124 fetches each required SGT, overwriting the previous SGT in RAM. Since the first two SGEs reside in the PRB RAM area, they are always available in case the SiI3124 needs to rescan the scatter/gather list for out of order data delivery.

SGTs must reside on a quadword (64-bit) naturally aligned boundary in host memory. In other words, bits[2:0] of the physical address of the SGT in host memory must be zero.

31				0	
SGE0 Data Address Low					0x00
SGE0 Data Address High					0x04
SGE0 Data Count					0x08
SGE0 TRM	SGE0 LNK	SGE0 DRD	SGE0 XCF	Reserved[27:0]	0x0C
SGE1 Data Address Low					0x10
SGE1 Data Address High					0x14
SGE1 Data Count					0x18
SGE1 TRM	SGE1 LNK	SGE1 DRD	SGE1 XCF	Reserved[27:0]	0x1C
SGE2 Data Address Low					0x20
SGE2 Data Address High					0x24
SGE2 Data Count					0x28
SGE2 TRM	SGE2 LNK	SGE2 DRD	SGE2 XCF	Reserved[27:0]	0x2C
SGE3 Data Address Low					0x30
SGE3 Data Address High					0x34
SGE3 Data Count					0x38
SGE3 TRM	SGE3 LNK	SGE3 DRD	SGE3 XCF	Reserved[27:0]	0x3C

Table 5-2 Scatter/Gather Table (SGT)

5.3.4 The Port Request Block (PRB)

The host builds a PRB to define a command to be executed by the SiI3124. The PRB occupies the first 64 bytes of a command slot in SiI3124 RAM. Once a command is issued, the PRB is overwritten in SiI3124 RAM as necessary to keep track of command context and execution status. The host should not depend on being able to read the contents of the PRB in slot RAM after command issuance. Upon command execution completion, the PRB area of the command slot may contain status information that can be read by the host, dependent upon the command type. The PRB structure can take several forms, dependent upon the command type that it defines.

The PRB contains the following major elements:

- A Control Field to indicate the type of PRB and any features to execute.
- A Protocol Override field used to optionally alter the normal SATA protocol flow.
- A FIS area that contains the initial FIS to be transmitted to the device upon PRB execution.
- Up to two Scatter/Gather entries (SGEs) to define areas of host memory that will be used for any data transfer associated with the PRB. For PACKET commands, the first SGE contains the 12 or 16-byte ATAPI command to be transmitted to the device.

Regardless of whether the command is to be issued with the direct or indirect method, the host driver should build the PRB as a structure in host memory. If the command is to be issued using the direct issuance method, the PRB can be copied from host RAM to the appropriate slot in SiI3124 RAM. If the command is to be issued using the indirect method, the host driver should write the physical address of the PRB to the command activation register associated with the desired command slot.

The PRB must reside on a quadword (64-bit) naturally aligned boundary in host memory. In other words, bits[2:0] of the physical address of the PRB in host memory must be zero.

The PRB can take various forms, depending on the type of command being issued. The command types are:

- Standard ATA Commands.
  This includes all the common ATA commands such as READ SECTORS, WRITE SECTORS, READ DMA, WRITE DMA, IDENTIFY DEVICE, SMART, etc. Also included are the queued commands in both legacy and SATA native queue modes. For these commands, the PRB contains the entire "Register – Host to Device" FIS containing the ATA command. By default, the SiI3124 decodes the ATA command type and executes the necessary SATA protocol automatically. The host driver may, optionally, execute any desired SATA protocol on a per-command basis.

- PACKET Commands.
  ATAPI PACKET commands operate in a similar fashion to the standard ATA commands. The "Register – Host to Device" FIS contains the ATA PACKET command. The 12 or 16-byte ATAPI command is placed in the area normally reserved for the first SGE. The SiI3124 does not decode the contents of the 12 or 16-byte ATAPI command, so the host driver indicates the direction of any data transfer associated with the command.

- Soft Reset
  A special form of the PRB instructs the SiI3124 to transmit a soft reset sequence to a device. The SiI3124 creates the necessary "Register – Host to Device" FISes required for the sequence. No SGEs are required for this PRB type. Other than the control field, the only item that needs to be populated is the PMP field, to direct the soft reset sequence to the proper device in the event that a port multiplier is attached. Upon successful command completion, the "Register – Device to Host" FIS is available in the command slot, allowing the host driver to view the device signature.

- External Command
  The external command feature allows the host driver to transmit any arbitrary FIS that will not fit in the FIS area of the PRB. This feature is useful in custom applications that have a need to send large FISes or Data FISes in a fashion that does not comply with the defined SATA protocol

- Interlocked FIS Reception
  The interlocked FIS feature allows the host driver to receive any desired FIS type directly to a host memory buffer, bypassing all SATA protocol for that FIS type. To use this feature, the host first specifies the FIS type(s) to be interlocked. Then, any number of available command slots can be reserved for the reception of FISes matching the defined type(s).

5.3.5 The PRB Control Field

The Control Field (offset 0x00, bits [15:0]) is used to indicate the type of PRB and features that are desired. For a standard ATA command, this field will normally contain a default value of 0x0000. Table 5-3 describes the bit functions for each bit in the Control Field.

Bit	Name	Description
0	control_protocol_override	The Protocol Override Field is to be used instead of the default protocol for this command.
1	control_retransmit	Allows retransmission if an error occurs during an external command transmission.
2	control_external_command	The command FIS shall be fetched from host memory. This feature is used to send arbitrary FISes that will not fit in the command FIS area of the PRB.
3	control_receive	Reserves a command slot to be used to receive an interlocked FIS as described by the port FIS_CONFIG register.
4	control_packet_read	Indicates that the packet command associated with this PRB will transfer data from the device to the host. This bit must be set for all packet commands that perform read data transfers.
5	control_packet_write	Indicates that the packet command associated with this PRB will transfer data from the host to the device. This bit must be set for all packet commands that perform write data transfers.
6	control_interrupt_mask	Setting this bit to one will prevent the SiI3124 from issuing a normal successful completion interrupt for this command.
7	control_soft_reset	Causes the SiI3124 to issue a soft reset FIS sequence to the device.
15:8	reserved	Must be zero

Table 5-3 Control Field Bit Definitions

5.3.6 The PRB Protocol Override Field

The Protocol Override Field (offset 0x00, bits [31:16]) is used to specify a protocol behavior other than the default for this PRB. PRBs for which the default protocol is to be used should set this field to 0x0000. The SiI3124 will decode the 8-bit ATA command at PRB offset 0x0a and automatically execute the default protocol for the command. In certain cases it might be desirable to specify a non-default protocol to be used, such as with vendor specific device commands. To override the protocol, the host driver must set control_protocol_override (Control Field, bit 0) to one and place the desired protocol in this field. Table 5-4 describes the Protocol Override bit positions.

Bit	Name	Description
16	protocol_packet	This command is to be executed as an ATAPI packet command.
17	protocol_legacy_queue	This command is to be executed as an ATA legacy queued command.
18	protocol_native_queue	This command is to be executed as a SATA native queued command.
19	protocol_read	This command is expected to transfer data from device to host.
20	protocol_write	This command is expected to transfer data from host to device.
21	protocol_transparent	This command is to be executed with no protocol. After the initial command FIS is successfully sent to the device, completion status will be posted without waiting for additional device transmissions.
31:22	Reserved	Must be zero.

Table 5-4 Protocol Override Bit Definitions

Note that there is no distinction between DMA and PIO data transfers in the protocol. The SiI3124 is a native serial ATA device and relies on the SATA interface protocol to determine the data transfer type between the device and the SiI3124. All data transfers between the SiI3124 and the Host are via DMA on the PCI(X) bus. From the host driver's perspective, all commands, whether PIO or DMA, transfer data through use of scatter/gather entries defined in the PRB and scatter/gather tables.

5.3.7 Standard ATA Command PRB Structure

Table 5-5 shows the layout for standard ATA commands. The Control and protocol override fields must be populated as described above.

31								0	
Protocol Override				Control					0x00
Received Transfer Count									0x04
Features / Error	Command / Status			C	R	R	R	PMP	FIS Type	0x08
Dev/Head	Cyl High			Cyl Low				Sector Number		0x0C
Features (Exp)	Cyl High (Exp)			Cyl Low (Exp)				Sector Num (Exp)		0x10
Device Control	Reserved			Sector Count (Exp)				Sector Count		0x14
Reserved	Reserved			Reserved				Reserved		0x18
Reserved – Must Be Zero										0x1C
SGE0 Data Address Low										0x20
SGE0 Data Address High										0x24
SGE0 Data Count										0x28
SGE0 TRM	SGE0 LNK	SGE0 DRD	SGE0 XCF	Reserved[27:0]						0x2C
SGE1 Data Address Low										0x30
SGE1 Data Address High										0x34
SGE1 Data Count										0x38
SGE1 TRM	SGE1 LNK	SGE1 DRD	SGE1 XCF	Reserved[27:0]						0x3C

Table 5-5 Port Request Block For Standard ATA Commands

The Received Transfer Count field (offset 0x04) is reserved as an input to the Sil3124 and should be populated with a value of all zeroes. Upon successful command completion, this field will contain the total number of data bytes received during the command execution. The host driver may use this field to determine the transfer size for commands in which the total transfer size is unknown, such as ATAPI inquiries.

The FIS area (offset 0x08 through 0x1f) must be populated with the initial FIS to be sent to the device. This area contains the FIS header and all task file registers to describe the ATA command. Table 5-6 describes the FIS area fields.

Offset	Bit(s)	Name	Description
0x08	7:0	FIS Type	The FIS type field must be populated with a valid SATA FIS type. In all but special custom cases this value will be 0x27, which defines a "Register – Host to Device" FIS type.
	11:8	PMP	4-bit Port Multiplier Port field that defines the port to which this command will be directed. If no port multiplier is attached, this field should be populated with all zeros
	14:12	Reserved	Must be zero.
	15	Command/Device Control	This bit must be set to one to indicate that this FIS contains a command.
	23:16	Task File Command	Populate with the desired ATA command type.
	31:24	Features	Populate with the desired features for this ATA command.
0x0c	7:0	Sector Number (LBA[7:0])	These fields should be populated with desired command-specific parameters.
	15:8	Cylinder Low (LBA[15:8])	
	23:16	Cylinder High (LBA[23:16])	
	31:24	Device/Head (LBA[27:24] for non-extended commands)	
0x10	7:0	Sector Number (Exp.) (LBA[31:24] for extended commands)	These fields should be populated with desired command-specific parameters.
	15:8	Cylinder Low (Exp.) (LBA[39:32] for extended commands)	
	23:16	Cylinder High (Exp.) (LBA[47:40] for extended commands)	
	31:24	Features (Exp.)	
0x14	7:0	Sector Count	These fields should be populated with desired command-specific parameters. The Reserved field must be zero for standard ATA commands that use the "Register –Host to Device" FIS to initiate a command.
	15:8	Sector Count (Exp.)	
	23:16	Reserved	
	31:24	Device Control	
0x18	31:0	Reserved	This field is reserved and must be zero for standard ATA commands that use the "Register – Host to Device" FIS to initiate a command.

Table 5-6 PRB FIS Area Definition

5.3.8 PACKET Command PRB Structure

Table 5-7 shows the layout for PACKET commands. The Control and protocol override fields must be populated as described above. The PACKET PRB FIS area is structured the same as a standard ATA command. The FIS area contains the PACKET ATA command. After the initial PACKET command is transmitted, the device will respond with a "PIO Setup" FIS, requesting a 12 or 16-byte ATAPI command. The host driver must populate the area normally used for the first SGE with the desired ATAPI command. The length of the ATAPI command is determined by the value of the packet length bit (Port Control, bit 5). If packet length is 0, 12 bytes will be transmitted. If packet length is one, 16 bytes will be transmitted. The packet length field must be initialized with the packet length value returned by the device in the IDENTIFY PACKET command. Table 5-7 shows a representative 12-byte ATAPI command layout.

31			0	
Protocol Override		Control		0x00
Received Transfer Count				0x04
Features / Error	Command / Status	C : R : R : R : PMP	FIS Type	0x08
Dev/Head	Cyl High	Cyl Low	Sector Number	0x0C
Features (Exp)	Cyl High (Exp)	Cyl Low (Exp)	Sector Num (Exp)	0x10
Device Control	Reserved	Sector Count (Exp)	Sector Count	0x14
Reserved	Reserved	Reserved	Reserved	0x18
Reserved – Must Be Zero				0x1C
LBA	LBA (MSB)	Reserved	ATAPI opcode	0x20
XFR Length (MSB)	Reserved	LBA (LSB)	LBA	0x24
Reserved	Reserved	Reserved	XFR Length (LSB)	0x28
Reserved	Reserved	Reserved	Reserved	0x2C
SGE1 Data Address Low				0x30
SGE1 Data Address High				0x34
SGE1Data Count				0x38
SGE1 TRM	SGE1 LNK	SGE1 DRD	SGE1 XCF	Reserved[27:0]	0x3C

*Highlighted ATAPI packet is an example typical of some commands; other command packets will have different formats within the highlighted bytes.

Table 5-7 Port Request Block For PACKET Command

The SiI3124 does not decode the ATAPI command to determine the necessity or direction of any associated data transfer. The host driver must supply this information by setting control_packet_read (control field, bit4) or control_packet_write (control field, bit 5) for any PACKET command that requires data transfer. Failure to set one of these bits for an ATAPI command that requests data transfer will result in an Overrun or Underrun Command Error condition.

5.3.9 Soft Reset PRB Structure

To send a soft reset sequence, the host driver need only fill in the PMP field (offset 0x8, bits[11:8]) and set control_soft_reset (control field, bit 7). The SiI3124 will send a soft reset sequence to the device and wait for a “Register – Device to Host” FIS to deliver the device signature and terminate the command. Upon successful command completion, the host may inspect the FIS area of the slot in SiI3124 RAM (offset 0x08 through 0x1f) to determine the returned device signature. Please note that a soft reset is executed in the same manner as other PRBs. It will be executed in the order in which it was issued. Port Ready (Port Status, bit 31) must be one in order to issue this command. In Table 5-8, shaded areas depict valid fields in slot RAM following successful command completion. These fields do not need to be supplied as inputs and may be in any state upon command issuance.

31							0	
N/A							Control (0x0080)	0x00
N/A								0x04
Features / Error	Command / Status	C	R	R	R	PMP	FIS Type	0x08
Dev/Head	Cyl High	Cyl Low					Sector Number	0x0C
Features (Exp)	Cyl High (Exp)	Cyl Low (Exp)					Sector Num (Exp)	0x10
Device Control	Reserved	Sector Count (Exp)					Sector Count	0x14
N/A								0x18
N/A								0x0C
N/A								0x10
N/A								0x14
N/A								0x18
N/A								0x1C
N/A								0x20
N/A								0x24
N/A								0x28
N/A								0x2C
N/A								0x30
N/A								0x34
N/A								0x38
N/A								0x3C

Table 5-8 Port Request Block For Soft Reset Command

5.3.10 External Command PRB Structure

An external command PRB is indicated by setting control_external_command (control field, bit 2). External commands execute in a manner similar to standard commands except that the initial command FIS is fetched from host memory instead of the PRB FIS area. By default, an external command uses the “transparent” protocol. That is, the command will be terminated immediately following the successful transmission of the external command FIS. If this is not the desired protocol, the host driver can set control_protocol_override (control field, bit 0) and place the desired protocol in the Protocol Override field (offset 0x00, bits [31:16]).

The external command FIS length may be any size (up to the 8K SATA limit) and will be automatically padded to a Dword boundary. The SiI3124 will frame the FIS, adding SOF, EOF, and CRC. The host memory FIS image must contain the FIS header (FIS Type, PMP, etc.). The PRB PMP field (offset 0x08, bits [11:8]) must be populated to direct the FIS to the desired port multiplier port, or must be zero if no port multiplier is attached. For port multiplier applications, it is important that the PMP field in the host-resident FIS and the PRB match for proper operation.

The location of the external command FIS is defined in additional SGEs with the XCF bit (SGE offset 0x0c, bit 28) set to one. Any type of command may be sent using an external command, including commands that have associated data transfers. Data transfer host memory locations are defined in SGEs with the XCF bit (SGE offset 0x0c, bit 28) set to zero. SGEs used to define the external command FIS and SGEs used to define data transfer may be freely mixed in any order. The presence or absence of the XCF bit informs the SiI3124 whether an SGE should be used for the current transfer operation.

31				0	
Protocol Override				Control	0x00
Received Transfer Count					0x04
Reserved			PMP	Reserved	0x08
					0x0C
					0x10
					0x14
					0x18
Reserved – Must Be Zero					0x1C
SGE0 Data Address Low					0x20
SGE0 Data Address High					0x24
SGE0 Data Count					0x28
SGE0 TRM	SGE0 LNK	SGE0 DRD	SGE0 XCF	Reserved[27:0]	0x2C
SGE1 Data Address Low					0x30
SGE1 Data Address High					0x34
SGE1 Data Count					0x38
SGE1 TRM	SGE1 LNK	SGE1 DRD	SGE1 XCF	Reserved[27:0]	0x3C

Table 5-9 Port Request Block For External Commands

5.3.11 Interlocked Receive PRB Structure

Reserving a command slot to receive an interlocked FIS is indicated by setting control_receive (control field, bit 3). To receive an interlocked FIS into host memory, the host driver first specifies the FIS type(s) to be interlocked by writing the appropriate value to the FIS Configuration register (port registers, offset 0x1028). The PRB is populated with SGEs that define the host memory region(s) that will be used to receive the interlocked FIS. When a FIS of the defined type is received, it will be written to the defined host memory area and the command will be completed. If an error occurs during receipt of the FIS, or the SGEs define an area that is not large enough to contain the entire FIS, the FIS will be rejected with an R_ERR response and the command will not complete. When an interlocked FIS is received without error into a memory region that is large enough to contain it, the command will be successfully completed and the host driver may use the received FIS in any manner. The command slot is then free to be redefined as a receive slot or as any other command type.

After successfully receiving an interlocked FIS, the low-level link will be receiving WTRM primitives from the transmitting device, which is expecting a response. By default, the SiI3124 waits for the host driver to write a response bit to the port control register. If the host driver writes Interlock Accept (Port Control Set register, bit 12), an R_OK response will be transmitted. If the host driver writes Interlock Reject (Port Control Set register, bit 11), an R_ERR response will be transmitted. The host driver may also elect to set Auto Interlock Accept (Port Control Set register, bit 14) before performing interlocked operations. Setting this bit will cause an R_OK response to be sent for all subsequently received interlocked FISes, without additional intervention from the host driver. It should be noted that in this mode, it is possible to receive one or more additional interlocked FISes before the host driver has had a chance to reserve command slots to receive them. If this occurs, any interlocked FIS that arrives without a reserved slot available will be acknowledged and discarded.

31				0	
Protocol Override				Control	0x00
Received Transfer Count					0x04
					0x08
					0x0C
					0x10
					0x14
					0x18
Reserved – Must Be Zero					0x1C
SGE0 Data Address Low					0x20
SGE0 Data Address High					0x24
SGE0 Data Count					0x28
SGE0 TRM	SGE0 LNK	SGE0 DRD	SGE0 XCF	Reserved[27:0]	0x2C
SGE1 Data Address Low					0x30
SGE1 Data Address High					0x34
SGE1 Data Count					0x38
SGE1 TRM	SGE1 LNK	SGE1 DRD	SGE1 XCF	Reserved[27:0]	0x3C

Table 5-10 Port Request Block For Receiving Interlocked FIS

5.4 Operation

5.4.1 Command Issuance

Before a command can be executed, it must reside in a slot in SiI3124 RAM and the SiI3124 must be informed that the PRB is ready to be executed. To accomplish this, the host must issue the command in one of two ways:

1. Indirect Command Issuance
   The indirect method is the most common and flexible method of issuing commands. With this method, the host builds the PRB in host memory and writes the physical address of the PRB into one of 31 command activation registers, each associated with a command slot. This causes the SiI3124 to fetch the PRB from host memory and deposit it in the selected slot of SiI3124 RAM. After the command is fetched, the SiI3124 automatically informs the execution unit that the command is ready for execution.
   The host may issue commands through additional command activation registers at any time without regard as to whether the previous PRB has been fetched. The SiI3124 will fetch the PRB's in the order requested when the necessary resources are available.

2. Direct Command Issuance
   The host may write the 64-byte PRB directly into SiI3124 slot RAM. The RAM area is defined in the port register map and the host can easily calculate the slot offset to write the PRB. After the PRB is written to RAM, the host informs the execution unit that it is ready to process by writing the slot number into the command execution FIFO register. The direct issue method is slightly more efficient than the indirect method on machines that support burst writes to the port register RAM space.
   Please note that when the direct command issue method is used, it is not possible to append scatter/gather entries to the PRB without defining a LNK in one of the PRB resident scatter/gather entries.

5.4.2 Reset and Initialization

The SiI3124 has a hierarchical reset structure that allows initialization of the entire chip, single port, an attached device, or the internal command queue. In general, asserting a reset at a high level will cause all underlying circuits to be reset. There are five levels of reset and initialization possible. The resets, listed from highest to lowest level, are:

5.4.2.1 PCI(X) Reset

The PCI(X) reset pin, when asserted, holds the entire chip in a reset state. All configuration, global, and port registers are initialized to their default state. When de-asserted, PCI(X) configuration space is programmable, but the global and port register spaces and the port state machines/command queue remain in a reset state until the Global and Port Resets are de-asserted through software control.

5.4.2.2 Global Reset

The Global Reset (Global Control Register, bit 31), when asserted, initializes all global registers, except PHY Configuration, and all port registers to the default state. All Port Resets are set to one (asserted) while Global Reset is asserted. The Global Reset must be cleared to zero to allow access to the global register space or to release any Port Reset. Software may use the Global Reset to initialize all ports with a single operation.

5.4.2.3 Port Reset

Each port contains a Port Reset (Port Control Set/Clear, bit 0) that remains set to one after the Global Reset is cleared to zero. While Port Reset is asserted, all port registers, except Port PHY Configuration, and OOB Bypass (Port Control Set/Clear, bit 25), are initialized to their default state. The port state machines are reset and the command queue is cleared. The Port Reset must be cleared to zero by writing a one to bit zero of the Port Control Clear Register to release the Port Reset condition. Software may assert the port reset condition at any time by writing a one to bit zero of the Port Control Set Register.

5.4.2.4 Device Reset

Each port contains a Device Reset (Port Control Set, bit 1) that may be used by software to reset an attached device without affecting the contents of the port registers. Writing a one to bit 1 of Port Control Set causes the execution state machines and pending command queue to be initialized. Then, a COMRESET is transmitted to the attached device. The effect of this sequence is to clear any outstanding commands and reset the attached device. The Device Reset bit is self-clearing. After the reset sequence has completed, the bit will be cleared to zero.

5.4.2.5 Port Initialize

Each port contains a Port Initialize (Port Control Set, bit 2) that may be used by software to initialize the port data structures without affecting the contents of the port registers or resetting the device. Writing a one to bit 1 of Port Control Set causes the execution state machines and pending command queue to be initialized. The effect of this sequence is to clear any outstanding commands. The Port Initialize bit is self-clearing. After the initialization sequence has completed, the bit will be cleared to zero.

5.4.3 Port Ready

Each port contains a Port Ready indicator (Port Status, bit 31) that is cleared to zero by any of the above reset conditions. The Port Ready signal, when one, indicates that the port is ready to execute commands. For all resets except Port Initialize, the Port Ready signal will not be asserted until a PHY ready condition is achieved. When Port Initialize is set, Port Ready will be cleared to zero then set to one after any currently active data transfers or FIS transmission/reception operations have completed and port initialization has completed.

5.4.4 Port Reset Operation

Upon release of Port Reset, the low-level power management state machine is enabled and OOB signaling is initiated to the device. The SiI3124 starts OOB signaling by transmitting a COMRESET to the device. If the device responds with COMINIT and the OOB sequence is successful, a PHY ready condition will result, indicating that a link has been successfully established and the device may transmit an initial register FIS. At this time, the Port Ready signal will be asserted, indicating that the host driver may issue commands. If the device does not respond within the prescribed time allowed for OOB, the low-level power management machine will initiate another OOB sequence after a fixed delay. The period between OOB attempts is approximately 100 milliseconds.

Upon receipt of an initial “Register – Device to Host” FIS that clears the task file status BSY state, the port is allowed to transmit commands to the device.

5.4.5 Initialization Sequence

The following is an example sequence of events that software might use to initialize the SiI3124 and enumerate an attached device or port multiplier. The sequence assumes that the system has powered up, the PCI(X) Reset has been de-asserted, and the system has enumerated the PCI(X) bus. Configuration space, including the Base Address Registers, has been initialized. It is now necessary to enable each port and determine the device type, if any, that is attached to each port.

1. Remove the Global Reset by writing 0x00000000 to the Global Control Register (Global offset 0x40).
2. For each Port to be initialized:
    a. Clear Port Reset by writing one to Port Reset of Port Control Clear Register (Port offset (port*0x2000)+0x1004, bit 0).
    b. If 32-bit platform and 32-bit activation is desired, write one to 32-bit Activation of Port Control Set Register (Port offset (port*0x2000)+0x1000, bit 10).
    c. To enable interrupts for command completion and command errors, write 0x00000003 to the Port Interrupt Enable Set Register (Port offset (port*0x2000)+0x1010).
    d. To determine if device is present, poll the SStatus Register (Port offset (port*0x2000)+0x1f04) for a PHYRDY condition indicated by the DET field (bits[3:0]) having a value of 0x3.
    e. Wait until Port Ready in Port Status Register (Port offset (port*0x2000)+0x1000, bit 31) is one. If desired, an interrupt may be armed in the Port Interrupt Set Register (bit 2). Any change in Port Ready state will assert an interrupt.
    f. If the software supports port multipliers, build a Soft Reset PRB in host memory. Set the PMP field to 0x0f to direct the command to the control port of a port multiplier. Issue the command to any available slot. If the software does not support port multipliers, skip this step, as sending this command will cause the port multiplier to disable legacy access to device 0.
    g. Upon successful command completion of the soft reset command, read the device signature from the command slot (Port offset (port*0x2000)+(slot*0x80)+0x14(LSB), 0x0c, 0x0d, 0x0e(MSB)).
    h. If the signature is 0x96690101, then the attached device is a Port Multiplier. Perform the Port Multiplier Enumeration procedure:
        i. Enable Port Multiplier context switching by writing a one to PM Enable in the Port Control Set Register (Port offset (port*0x2000)+0x1000, bit 13).
        ii. Read the Port Multiplier GSCR[2] register by issuing a Read Port Multiplier command to the control port. This register contains the number of device ports on the Port Multiplier.
        iii. For each Port Multiplier Device Port:
            1. Enable the PHY by writing a 1, then a 0 to the Scontrol Register (PSCR[2]) DET field. Issue a Port Multiplier Write command for each of these operations.
            2. Wait for a PHYRDY condition in the port by polling the SStatus Register (PSCR[0]) .
            3. Clear the X-bit and all other error bits in the Serror Register (PSCR[1]) by writing all ones to the register with a Write Port Multiplier command. The port is now ready for operation.
            4. Issue a Soft Reset command with the PMP field set to the appropriate port. This will return a device signature for the attached device.
            5. Issue the appropriate Identify Device or Identify Packet Device command and any associated Set Features, Set Write Multiple commands as may be necessary to initialize the device.
    i. If the signature is 0xeb140101, then the attached device is an ATAPI PACKET device.

i. Issue Identify Packet Device command to get device specific parameters
ii. While drive is not ready and timeout has not expired:
    1. Issue Test unit ready PACKET command
    2. If the command completes successfully, drive is ready
    3. Else, if command error indicates Device error condition due to drive not ready, write Initialize Port to the Port Control Register (port*0x2000)+0x1000, bit 2)
    4. Wait until Port Ready in Port Status Register (Port offset (port*0x2000)+0x1000, bit 31) is one. If desired, an interrupt may be armed in the Port Interrupt Set Register (bit 2). Any change in Port Ready state will assert an interrupt.
iii. Drive is ready for use. Issue appropriate Set Features, Set Read Multiple commands as needed.

j. If the signature is 0x00000101, then the attached device is a disk drive.
    i. Issue Identify Device command to get device specific parameters
    ii. Drive is ready for use. Issue appropriate Set Features, Set Read Multiple commands as needed.

5.4.6 Interrupts and Command Completion

Each port of the SiI3124 produces a single interrupt signal, which is an accumulation of various possible interrupt events. In its default mode, the SiI3124 combines the interrupts from the ports into a single interrupt that is used to drive the INTA PCI(X) pin. In certain embedded environments, it might be desirable for each port to drive an independent interrupt pin, or to combine various ports to drive one of the four available interrupt pins. Software may configure each port to direct its interrupt to one of four interrupt pins. The Interrupt Steering field in the Port Interrupt Enable Set/Clear register (Port offset 0x1010/1014, bit [31:30]) is used to direct the port interrupt to the appropriate pin. By default, this field is set to a value of zero, indicating that the interrupt is directed to the INTA pin. The register may be set to one of four values:

Interrupt Steering Value	Pin Used for Interrupt
0	INTA
1	INTB
2	INTC
3	INTD

Table 5-11 Interrupt Steering

5.4.7 Interrupt Sources

Figure 5-3 on page 43 depicts a logical representation of the interrupt routing for the SiI3124. For Each port, the possible interrupt causes are:

- Command Completion. Indicates that one or more commands have successfully completed. This interrupt is cleared in one of two ways, dependent upon the state of Interrupt NCoR (Port Control Register, bit 3). Reading the port Slot Status Register will clear this interrupt condition if Interrupt NCoR is zero. Writing a one to bit 0 or 16 of the port Interrupt Status Register will clear this interrupt condition if Interrupt NCoR is one. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.
- Command Error. Indicates that a command did not complete successfully. The port Command Error register will contain an error code indicating the actual cause of failure. When this bit is set, Port Ready will be set to zero and no additional commands will be processed until the port is initialized by one of the reset methods and Port Ready is asserted. Writing a one to bit 1 or 17 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.
- Port Ready. Indicates that the Port Ready state has changed from zero to one. Writing a one to bit 2 or 18 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.
- Power Management Change. Indicates that the port power management state has been modified. The current power management state can be determined by reading the port SStatus Register. Writing a one to bit 3 or 19 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.
- PHY Ready Change. Indicates that the PHY state has changed from Not Ready to Ready or from Ready to Not Ready. The current PHY state can be determined by reading the port SStatus Register. Writing a one to bit 4 or 20 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.
- COMWAKE Received. Indicates that a COMWAKE OOB signal has been decoded on the receiver. Writing a one to bit 5 or 21 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.

- Unrecognized FIS. Indicates that the F-bit has been set in the Serror Diag field. Writing a one to bit 6 or 22 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.
- Device Exchanged. Indicates that the X-bit has been set in the Serror Diag field. The X-bit is set upon receipt of a COMINIT from the device. Writing a one to bit 7 or 23 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.
- 8b/10b Decode Error Threshold Exceeded. Indicates that the 8b/10b Decode Error counter has exceeded the programmed non-zero threshold value. Writing any value to the port 8b/10b Decode Error Counter Register or writing a one to bit 8 or 24 of the Interrupt Status Clear Register will clear this interrupt condition. This interrupt is enabled by writing a non-zero value to the threshold field (bit[31:16]) of the port 8b/10b Decode Error Counter Register. Writing a zero the threshold field will disable this interrupt.
- CRC Error Threshold Exceeded. Indicates that the CRC Error counter has exceeded the programmed non-zero threshold value. Writing any value to the port CRC Error Counter Register or writing a one to bit 9 or 25 of the Interrupt Status Clear Register will clear this interrupt condition. This interrupt is enabled by writing a non-zero value to the threshold field (bit[31:16]) of the port CRC Error Counter Register. Writing a zero to the threshold field will disable this interrupt.
- Handshake Error Threshold Exceeded. Indicates that the Handshake Error counter has exceeded the programmed non-zero threshold value. A handshake error occurs when an R_ERR primitive is received. Writing any value to the port Handshake Error Counter Register or writing a one to bit 10 or 26 of the Interrupt Status Clear Register will clear this interrupt condition. This interrupt is enabled by writing a non-zero value to the threshold field (bit[31:16]) of the port Handshake Error Counter Register. Writing a zero to the threshold field will disable this interrupt.
- SDB Notify. Indicates that a “Set Device Bits” FIS has been received with the N-bit set in the control field. ATAPI and Port Multiplier devices optionally use this feature to signal the host that an event has occurred that requires further scrutiny. Writing a one to bit 11 or 27 of the port Interrupt Status Register clears this interrupt condition. This interrupt is enabled or disabled with the corresponding bit in the port Interrupt Enable Set/Clear Register.

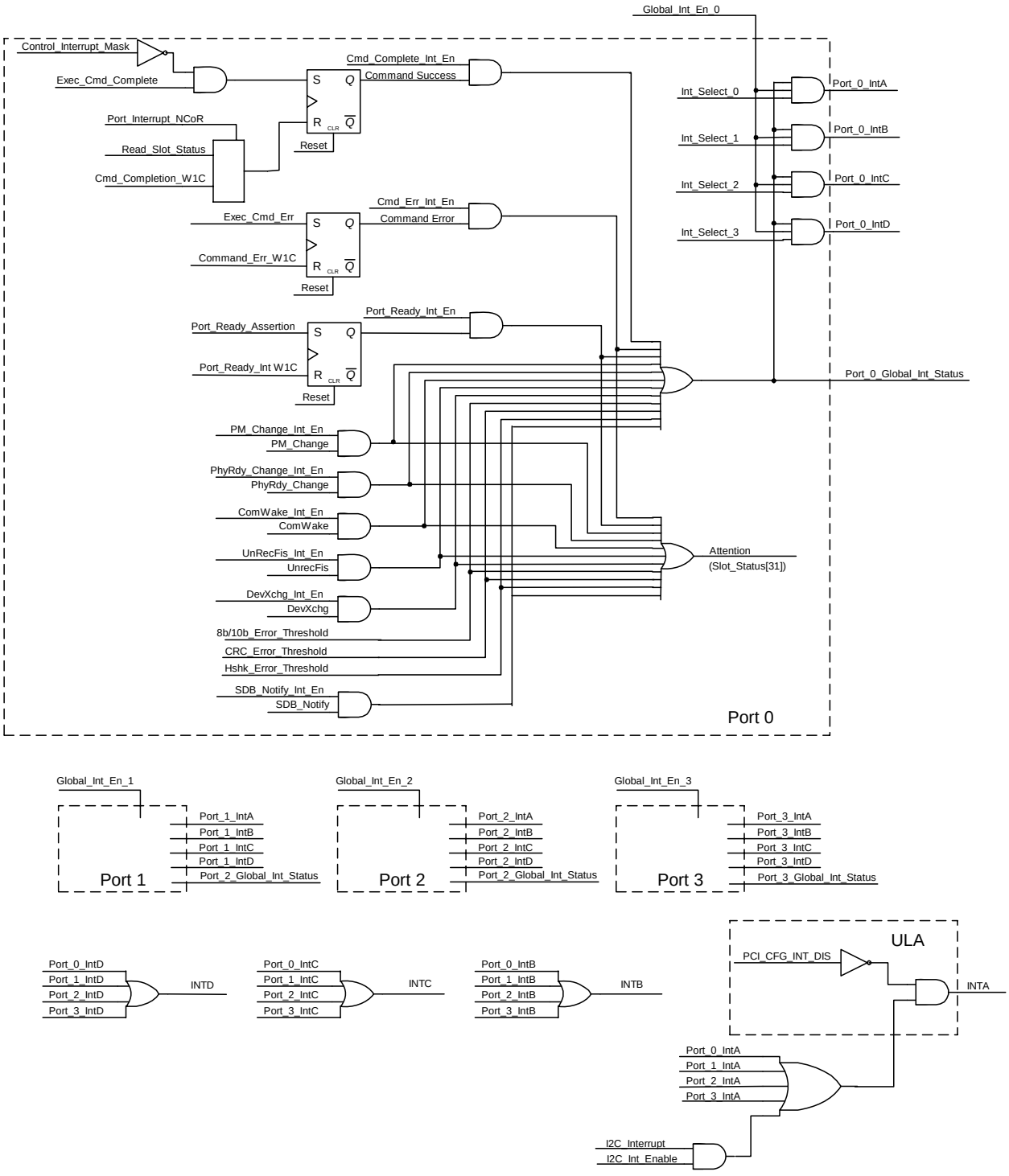


Figure 5-3 Sil3124 Interrupt Map

Interrupt Cause	Interrupt Status Bit		To Clear:	To Enable:	To Disable:
	Masked	Raw			
Command Complete	0	16	If Interrupt W1C == 0 Read Slot Status If Interrupt W1C == 1 Write 1 to Port Interrupt Status bit 0 or 16, OR, write one to desired port bit(s) in Global Interrupt Status.	Write 1 to Interrupt Enable Set bit 0	Write 1 to Interrupt Enable Clear bit 0 OR Write 1 to control_interrupt_mask in PRB Control field
Command Error	1	17	Write 1 to Interrupt Status bit 1 or 17	Write 1 to Interrupt Enable Set bit 1	Write 1 to Interrupt Enable Clear bit 1
Port Ready	2	18	Write 1 to Interrupt Status bit 2 or 18	Write 1 to Interrupt Enable Set bit 2	Write 1 to Interrupt Enable Clear bit 2
Power Management Change	3	19	Write 1 to Interrupt Status bit 3 or 19	Write 1 to Interrupt Enable Set bit 3	Write 1 to Interrupt Enable Clear bit 3
PHY Ready Change	4	20	Write 1 to Interrupt Status bit 4 or 20	Write 1 to Interrupt Enable Set bit 4	Write 1 to Interrupt Enable Clear bit 4
COMWAKE Received	5	21	Write 1 to Interrupt Status bit 5 or 21	Write 1 to Interrupt Enable Set bit 5	Write 1 to Interrupt Enable Clear bit 5
Unrecognized FIS Received	6	22	Write 1 to Interrupt Status bit 6 or 22	Write 1 to Interrupt Enable Set bit 6	Write 1 to Interrupt Enable Clear bit 6
Device Exchanged	7	23	Write 1 to Interrupt Status bit 7 or 23	Write 1 to Interrupt Enable Set bit 7	Write 1 to Interrupt Enable Clear bit 7
8b/10b Decode Error Threshold	8	24	Write 1 to Interrupt Status bit 8 or 24 OR Write any value to 8b/10b Decode Error Counter bits[15:0]	Write non-zero value to 8b/10b Decode Error Counter bits[31:16]	Write zero to 8b/10b Decode Error Counter bits[31:16]
CRC Error Threshold	9	25	Write 1 to Interrupt Status bit 9 or 25 OR Write any value to CRC Error Counter bits[15:0]	Write non-zero value to CRC Error Counter bits[31:16]	Write zero to CRC Error Counter bits[31:16]
Handshake Error Threshold	10	26	Write 1 to Interrupt Status bit 10 or 26 OR Write any value to Handshake Error Counter bits[15:0]	Write non-zero value to Handshake Error Counter bits[31:16]	Write zero to Handshake Error Counter bits[31:16]
Set Device Bits Notification Received	11	27	Write 1 to Interrupt Status bit 11 or 27	Write 1 to Interrupt Enable Set bit 11	Write 1 to Interrupt Enable Clear bit 11

Table 5-12 Port Interrupt Causes And Control

5.4.8 Command Completion – The Slot Status Register

The Slot Status register is designed such that an interrupt service routine can determine the successful completion state of outstanding commands, dismiss the command completion interrupt, and determine if any other enabled interrupt events are pending in a port with a single read of the Slot Status register.

The Slot Status Register (Port offset 0x1800 or Global offset 0x00 + (port * 4)) bits 0 through 30 reflect the status of each of the 31 command slots in a port. When a PRB is issued to a command slot, the corresponding bit in the Slot Status register is set to one, indicating that the command is in progress. When a command is successfully completed, the corresponding command slot bit is cleared in the Slot Status register. The host driver may read the Slot Status register at any time to determine the activity state of any issued commands.

By default, a successfully completed command will set the command complete bit in the port Interrupt Status register. If the Command Complete interrupt is enabled, an interrupt will be asserted simultaneously. The host driver may optionally set control_interrupt_mask in the PRB Control field to prevent the command complete bit from being set on a per-command basis. This is useful when the host issues a series of commands and wants to be interrupted only after a selected command completes.

The command complete bit and associated interrupt will be cleared when the Slot Status register is read, unless the host driver has set Interrupt No Clear on Read (Port Control Set/Clear register, bit 3). If Interrupt No Clear on Read is set to one, the host driver must write a one to the Command Complete bit in the Interrupt Status Clear register in order to clear the command complete bit and associated interrupt.

5.4.9 The Attention Bit

Bit 31 of the Slot Status register is the Attention bit. When set to one, it indicates that an enabled interrupt source, other than command completion, is asserted. It is possible that the Slot Status register can indicate an Attention condition while also showing that commands have successfully completed in bits 0 through 30. The interrupt service routine should always post-process any completed commands in addition to servicing a possible Attention condition. The Attention bit is set only for interrupt conditions that have been enabled as described in the *Interrupt Sources* section. The Attention bit will remain set to one in the Slot Status register until all enabled interrupt conditions have been cleared.

5.4.10 Interrupt Service Procedure

The SiI3124 is designed to efficiently service interrupt events with minimal host overhead. There are a number of methods that the host may use to quickly determine the interrupt cause within any of the ports. The Global Interrupt Status Register (Global offset 0x44) may be read to determine which ports are interrupting. Then, the Slot Status Register for the interrupting ports may be read to determine the interrupt cause. Alternately, if the bridge configuration allows bursting of pre-fetched read data, all port Slot Status Registers may be read in a single burst operation from the Global Register space starting at Global offset 0x00. If Interrupt No Clear on Read (port Control Register, Bit 3) is zero, any command complete interrupt will be cleared when the Slot Status registers are read. The host driver should then compare the outstanding command status in bits 0 through 30 to its internal copy of outstanding commands to determine which, if any, commands have successfully completed. Once the successful command completions have been noted, the host should check the Attention bit (bit 31) to determine if any other enabled interrupt events are pending on the port. If the Attention bit is one, the host should read the port Interrupt Status Register (Port offset (port*0x2000)+0x1008) to ascertain the cause for the Attention condition. Once the Attention condition has been resolved and cleared, normal processing may continue.

5.4.11 Interrupt No Clear on Read

By default, the Command Completion interrupt condition is cleared when the port Slot Status Register is read. In some cases, such as debug environments, clearing of the Command Completion interrupt might not be the desired effect of reading the Slot Status Register. In these cases, the host driver should set the Interrupt No Clear on Read bit (bit 3) in the port Control Register. When this bit is set, the host must clear the Command Completion interrupt by one of the following methods:

1. Write a one to the corresponding port interrupt status bit(s) in the Global Interrupt Status Register (Global offset 0x44). Or,
2. Write a one to bit 0 or bit 16 of the port Interrupt Status Register (Port offset (port*0x2000)+ 0x1008).

Method 1 allows Command Complete interrupts for multiple ports to be cleared in a single write operation. Method 2 will clear Command Complete only for the corresponding port.

5.4.12 Error Processing

When an error occurs during command processing, the SiI3124 records the error condition and halts execution until the host driver is able to restore normal operation. The SiI3124 does not attempt to automatically recover from error conditions. Rather, it provides the host with the necessary information to handle the error condition. Errors that occur during command execution cause the Command Error bit to be set to one in the port Interrupt Status Register (Port offset (port*0x2000)+ 0x1008) and an error code to be placed in the port Command Error Register (Port offset (port*0x2000)+ 0x1024). Please see section (xxx- Port Command Error register) for a complete list of possible error codes. Execution is then halted. Port Ready (Port Status Register, bit 31) will be cleared to zero. Only the port with the error condition is halted. All other ports will continue to process normally. If the Command Error interrupt is enabled, an interrupt is asserted and the Attention bit is asserted in the port Slot Status Register. The corresponding Slot Status bit for the command in error will NOT be cleared to zero, since the command did not complete successfully. If only non-queued commands are outstanding, the slot number for the command in error is available in the Port Status Register, bits[20:16]. The host may use this information to ascertain which outstanding command caused the error condition.

To recover from a Command Error condition, it is necessary to initialize the port by one of the Port Reset methods described in section 5.4.2 Reset and Initialization. It might not be necessary to reset the device in all error cases. In fact, to properly recover from native queued error conditions, it may be necessary to send additional commands to the device in error to obtain additional error information. At the minimum, it will be necessary to assert a Port Initialize and wait for Port Ready before additional commands may be issued.

Errors may be grouped into three categories to determine the proper recovery action:

- Recoverable errors. Error codes 1 and 2 are device specific errors. These errors occur when the device returns an error bit in the final register FIS or in a Set Device Bits FIS. Depending upon the severity of the error type reported by the device, it might not be necessary to reset the device. If the error code is 1, the register FIS received from the device is available in the command slot PRB. The host may determine the error reported by the device by examining the error register field of this structure. Please see section 5.4.13for more information regarding error recovery procedures.
- Locally detected data errors. Error code 3 is a unique error type. It indicates that the SiI3124 detected an error during command execution but the device failed to report the error upon command completion. For non-queued commands, this error type may be treated the same as a recoverable error. If queued commands are outstanding, the device must be reset since it is necessary to make sure that all queued commands are flushed from the device upon an error condition. Since the device did not report an error, it is unlikely that the queue has been flushed in the device.
- Fatal Errors. All other error codes indicate that an error condition has occurred that requires both the device and the internal operational state of the SiI3124 to be reset. The most common method to perform this function is to issue a Device Reset as described in section 5.4.2 Reset and Initialization.

5.4.13 Error recovery procedures

When a device returns error status for an outstanding command, the SiI3124 will halt command processing, post an error type of 1 or 2 in the Port Command Error register, set the command error bit in the interrupt status register and, if enabled, assert an interrupt to the host. The host driver may wish to attempt error recovery without resetting the device that issued the error. Note that error recovery procedures should only be attempted for error types 1 and 2. Error type 3 is also recoverable if no queued commands are outstanding. It is recommended that all other error types result in a reset of the affected device(s).

If the device in error is directly attached to the SiI3124 device port, the host may simply issue a Port Initialize by setting bit 2 in the Port Control Set register and waiting for a Port Ready condition. The host may then re-issue any commands that were outstanding when the error occurred. If native queued commands were outstanding, the host should issue a READ LOG EXTENDED for Log Page 10h to determine the details of the error condition. Refer to the Serial ATA II specification for further details on error handling with native queuing.

If the device in error is attached to a port multiplier, it is necessary for the host driver to wait until all outstanding commands to other devices attached to the port multiplier have completed before issuing the Port Initialize function. This is accomplished through a series of steps:

1. The host driver must note the PM port number for the device in error by extracting the PMP field (bit[8:5]) from the Port Context Register (port offset 0x1e04). The PMP field contains the PM port number for the device in error. It is then necessary to determine if any commands are outstanding for non-error devices. If there are no commands outstanding for non-error devices, the host driver may simply proceed to step 4 to issue a Port Initialize and wait for a Port Ready condition before reissuing commands.
2. If commands are outstanding to non-error devices, the host should set the Port Resume bit (bit 6) in the Port Control Set Register. Setting this bit will cause the following actions:
    a. Force a Device Busy condition for the currently selected PM port (the port to which the device in error is attached) so that no additional issued commands will be sent to the device in error.
    b. Continue processing of commands that have been issued.
3. The host driver must monitor command completion progress and determine when all commands for non-error devices have completed. Please note that the Port Slot Status register will still have a bit set for each outstanding command on the device in error. These bits will not be cleared and the host must ignore them while waiting for command completion on non-error devices. If another recoverable error occurs while waiting for commands to complete, the host driver must follow the same recovery steps for the new device in error, starting with step 1 above. It is possible to have multiple devices in an error recovery state concurrently. When the host driver has detected that all commands for non-error devices have completed, it must perform the following steps.
    a. Clear Port Resume (Port Control Clear Register, Bit 6).
    b. Clear bit[16:13] in the Port Device Status Register for the device(s) in error ((port*0x2000) + 0xf80 + (PM port of device in error * 8)). This action clears the device_busy, native_queue, legacy_queue, and service_pending bits to ready the device for further command processing.

c. Write zeroes (0x00000000) to the Port Device QActive Register for the device(s) in error ((port*0x2000) + 0xf84 + (PM port of device in error * 8)). This action ensures that all queued command context is removed before re-issuing commands.
d. Issue a Port Initialize and wait for Port Ready condition.

4. The host driver may now resume normal command processing. The host driver must determine which commands need to be re-issued to the device in error. Note that if native queued commands were outstanding to the device in error, the host must issue a READ LOG EXTENDED command to clear the pending error condition and determine the tag number (slot number) of the command in error before resuming command processing.

Note: It is a good idea to clear Port Resume (Port Control Clear Register, Bit 6) whenever a Port Initialize or Port Device Reset is issued. This ensures that the Port Resume bit is always cleared when starting normal processing in the event that an abnormal exit is taken from the error recovery procedure.

6 Auto-Initialization

The SiI3124 supports an external Flash and/or EEPROM device for BIOS extensions and user-defined PCI configuration header data.

6.1 Auto-Initialization from Flash

The SiI3124 initiates the Flash detection and configuration space loading sequence upon the release of PCI_RST_N. It begins by reading the highest two addresses ($7FFFF_H$ and $7FFFE_H$), checking for the correct data signature pattern – AA_H and 55_H, respectively. If the data signature pattern is correct, the SiI3124 continues to sequence the address downward, reading a total of twelve bytes. If the Data Signature is correct (55_H at $7FFFC_H$), the last eight bytes are loaded into the PCI Configuration Space registers.

If both Flash and EEPROM are installed, the PCI Configuration Space registers will be loaded with the EEPROM's data.

While the sequence is active, the SiI3124 responds to all PCI bus accesses with a Target Retry.

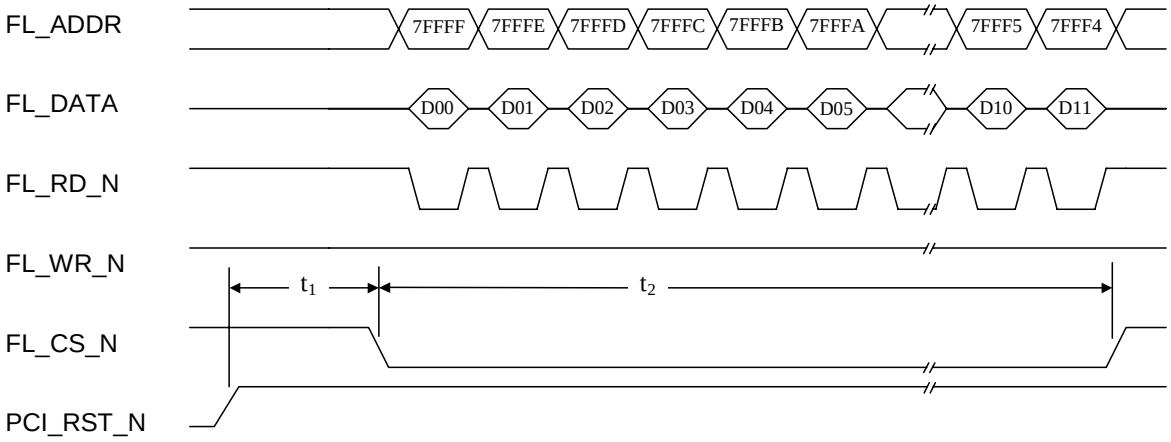


Figure 6-1 Auto-Initialization from Flash Timing

Parameter	Value	Description
t_1	660 ns	PCI reset to Flash Auto-Initialization cycle begin
t_2	4700 ns	Flash Auto-Initialization cycle time

Table 6-1 Auto-Initialization from Flash Timing

Address	Data Byte	Description
$7FFFF_H$	D00	Data Signature = AA_H
$7FFFE_H$	D01	Data Signature = 55_H
$7FFFD_H$	D02	AA = 120 ns Flash device / Else, 240 ns Flash device
$7FFFC_H$	D03	Data Signature = 55_H
$7FFFB_H$	D04	PCI Device ID [23:16]
$7FFFA_H$	D05	PCI Device ID [31:24]
$7FFF9_H$	D06	PCI Class Code [23:16]
$7FFF8_H$	D07	PCI Class Code [15:08]
$7FFF7_H$	D08	PCI Sub-System Vendor ID [07:00]
$7FFF6_H$	D09	PCI Sub-System Vendor ID [15:08]
$7FFF5_H$	D10	PCI Sub-System ID [23:16]
$7FFF4_H$	D11	PCI Sub-System ID [31:24]

Table 6-2 Flash Data Description

6.2 Auto-Initialization from EEPROM

The SiI3124 initiates the EEPROM detection and configuration space loading sequence after the Flash read sequence. The SiI3124 supports EEPROMs with an I^2C serial interface. The sequence of operations consists of the following.

1) START condition defined as a high-to-low transition on I2C_SDAT while I2C_SCLK is high.
2) Control byte = 1010 (Control Code) + 000 (Chip Select) + 0 (Write Address)
3) Acknowledge
4) Starting address field = 00000000.
5) Acknowledge
6) Sequential data bytes separated by Acknowledges.
7) STOP condition.

While the sequence is active, the SiI3124 responds to all PCI bus accesses with a Target Retry.

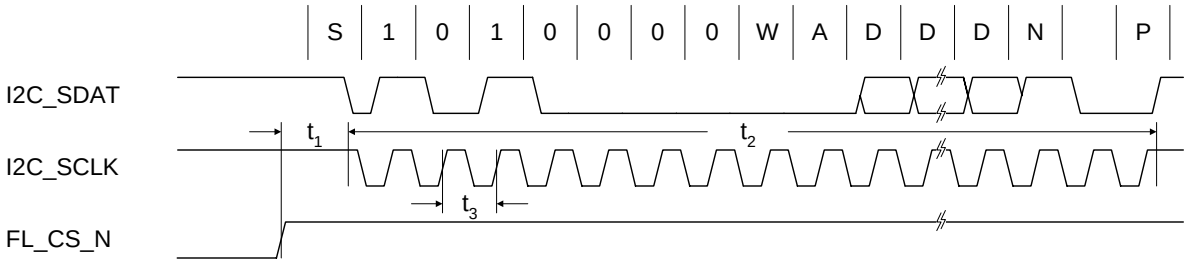


Figure 6-2 Auto-Initialization from EEPROM Timing

Parameter	Value	Description
t_1	26.00 µs	End of Auto-Initialization from Flash to start of Auto-Initialization from EEPROM
t_2	1.6 ms	Auto-Initialization from EEPROM cycle time
t_3	10 µs	EEPROM serial clock period

Table 6-3 Auto-Initialization from EEPROM Timing

Parameter	Description
S	START condition
W	R/W 0 = Write Command, 1 = Read Command
A	Acknowledge
D	Serial data
N	No-Acknowledge
P	STOP condition

Table 6-4 Auto-Initialization from EEPROM Timing Symbols

Address	Data Byte	Description
00_H	D00	Memory Present Pattern = AA_H
01_H	D01	Memory Present Pattern = 55_H
02_H	D02	Data Signature = AA_H
03_H	D03	Data Signature = 55_H
04_H	D04	PCI Device ID [23:16]
05_H	D05	PCI Device ID [31:24]
06_H	D06	PCI Class Code [23:16]
07_H	D07	PCI Class Code [15:08]
08_H	D08	PCI Sub-System Vendor ID [07:00]
09_H	D09	PCI Sub-System Vendor ID [15:08]
$0A_H$	D10	PCI Sub-System ID [23:16]
$0B_H$	D11	PCI Sub-System ID [31:24]

Table 6-5 EEPROM Data Description

7 Register Definitions

This section describes the registers within the SiI3124.

7.1 PCI Configuration Space

The PCI Configuration Space registers define the operation of the SiI3124 on the PCI bus. These registers are accessible only when the SiI3124 detects a Configuration Read or Write operation, with its IDSEL asserted, on the PCI bus.

Address Offset	Register Name			
00_H	Device ID		Vendor ID	
04_H	PCI Status		PCI Command	
08_H	PCI Class Code			Revision ID
$0C_H$	BIST	Header Type	Latency Timer	Cache Line Size
10_H	Base Address Register 0			
14_H				
18_H	Base Address Register 1			
$1C_H$				
20_H	Base Address Register 2			
24_H	Reserved			
28_H	Reserved			
$2C_H$	Subsystem ID		Subsystem Vendor ID	
30_H	Expansion ROM Base Address			
34_H	Reserved			Capabilities Ptr
38_H	Reserved			
$3C_H$	Max Latency	Min Grant	Interrupt Pin	Interrupt Line
40_H	PCI-X Command		Next Capability	PCI-X Cap ID
44_H	PCI-X Status			
48_H	Reserved			Hdr Wr Ena
$4C_H$	Reserved			
50_H	Reserved			
54_H	Message Control		Next Capability	MSI Cap ID
58_H	Message Address			
$5C_H$				
60_H	Reserved		Message Data	
64_H	Power Management Capabilities		Next Capability	Pwr Mgt Cap ID
68_H	Data	Reserved	Control and Status	

Table 7-1 SiI3124 PCI Configuration Space

7.1.1 Device ID – Vendor ID

Address Offset: 00_H
Access Type: Read /Write
Reset Value: 0x3124_1095

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Device ID																Vendor ID															

This register defines the Device ID and Vendor ID associated with the SiI3124. The register bits are defined below.

- **Bit [31:16]**: Device ID (R/W) – Device ID. The value in this bit field is one of the following three:
  - the default value of 0x3124 to identify the device as a Silicon Image SiI3124.
  - the value loaded from an external memory device; if an external memory device – Flash or EEPROM – is present with the correct signature, the Device ID is loaded from that device after reset. See section 6 on page 44.
  - system programmed value; if bit 0 of the Configuration register (48_H) is set, the Device ID is system programmable.
- **Bit [15:00]**: Vendor ID (R) – Vendor ID. This field defaults to 0x1095 to identify the vendor as Silicon Image.

7.1.2 PCI Status – PCI Command

Address Offset: 04_H
Access Type: Read/Write/Write-One-to-Clear
Reset Value: 0x02B0_0080 (PCI) / 0x0230_0080 (PCI-X)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Det Par Err	Sig Sys Err	Rcvd M Abort	Rcvd T Abort	Sig T Abort	Devsel Timing		Det M Par Err	Fast B-to-B Cap	Reserved	66 MHz Capable	Capabilities List	Int Status	Reserved								Int Disable	Fast B-to-B En	SERR Enable	Addr Step	Par Error Resp	VGA Palette	Mem Wr & Inv	Special Cycles	Bus Master	Memory Space	IO Space

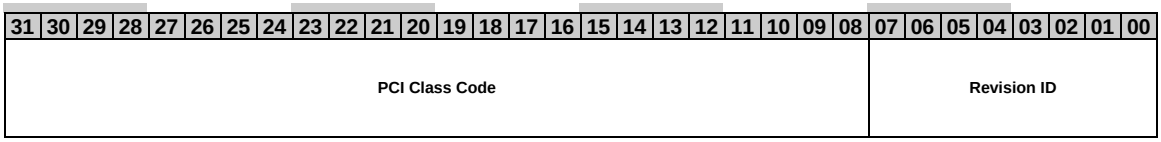
This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit 31**: Det Par Err (R/W1C) – Detected Parity Error. This bit set indicates that the SiI3124 detected a parity error on the PCI bus (either address or data parity error) while responding as a PCI target.
- **Bit 30**: Sig Sys Err (R/W1C) – Signaled System Error. This bit set indicates that the SiI3124 signaled SERR on the PCI bus.
- **Bit 29**: Rcvd M Abort (R/W1C) – Received Master Abort. This bit set indicates that the SiI3124 terminated a PCI bus operation with a Master Abort.
- **Bit 28**: Rcvd T Abort (R/W1C) – Received Target Abort. This bit set indicates that the SiI3124 received a Target Abort termination.
- **Bit 27**: Sig T Abort (R/W1C) – Signaled Target Abort. This bit set indicates that the SiI3124 terminated a PCI bus operation with a Target Abort.
- **Bit [26:25]**: Devsel Timing (R) – Device Select Timing. This bit field indicates the DEVSEL timing supported by the SiI3124. The hardwired value is 01_B for Medium decode timing.
- **Bit 24**: Det M Par Err (R/W1C) – Detected Master Data Parity Error. This bit set indicates that the SiI3124, as bus master, detected a parity error on the PCI bus. The parity error may be either reported by the target device via PERR# on a write operation or by the SiI3124 on a read operation.
- **Bit 23**: Fast B-to-B Cap (R) – Fast Back-to-Back Capable. This bit is 1 in PCI Mode to indicate that the SiI3124 is Fast Back-to-Back capable as a PCI target. This bit is 0 in PCI-X Mode.
- **Bit 22**: Reserved (R) – This bit is reserved and returns zero on a read.
- **Bit 21**: 66 MHz Capable (R) – 66 MHz PCI Operation Capable. This bit is hardwired to 1 to indicate that the SiI3124 is 66 MHz capable.
- **Bit 20**: Capabilities List (R) – PCI Capabilities List. This bit is hardwired to 1 to indicate that the SiI3124 implements Capabilities registers for Power Management, PCI-X, and Message Signaled Interrupt.
- **Bit [19]**: Interrupt Status (R).
- **Bit [18:11]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [10]**: Interrupt Disable (R/W).

- **Bit 09**: Fast B-to-B En (R) – Fast Back-to-Back Enable. This bit is hardwired to 0 to indicate that the SiI3124 does not support Fast Back-to-Back operations as bus master.
- **Bit 08**: SERR Enable (R/W) – SERR Output Enable. This bit set enables the SiI3124 to drive the PCI SERR# pin when it detects an address parity error. The Parity Error Response bit (06) must also be set to enable SERR# reporting.
- **Bit 07**: Addr Step (R) – Address Stepping Enable. This bit is hardwired to 1 to indicate that the SiI3124 does support Address Stepping.
- **Bit 06**: Par Error Resp (R/W) – Parity Error Response Enable. This bit set enables the SiI3124 to respond to parity errors on the PCI bus. If this bit is cleared, the SiI3124 will ignore PCI parity errors. The Detected Parity Error (bit 31) in this register is set regardless of the state of this bit.
- **Bit 05**: VGA Palette (R/W) – VGA Palette Snoop Enable. The feature is not implemented and this bit should always be written as 0.
- **Bit 04**: Mem Wr & Inv (R) – Memory Write and Invalidate Enable. This bit enables the use of Memory Write and Invalidate bus cycles.
- **Bit 03**: Special Cycles (R/W) – Special Cycles Enable. This bit should always be written with 0 to indicate that the SiI3124 does not respond to Special Cycles.
- **Bit 02**: Bus Master (R/W) – Bus Master Enable. This bit set enables the SiI3124 to act as PCI bus master. A PCI-X Split Completion cycle may be initiated even if this bit is set to 0.
- **Bit 01**: Memory Space (R/W) – Memory Space Enable. This bit set enables the SiI3124 to respond to PCI memory space accesses.
- **Bit 00**: I/O Space (R/W) – I/O Space Enable. This bit set enables the SiI3124 to respond to PCI I/O space accesses.

7.1.3 PCI Class Code – Revision ID

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0180_0002



This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:08]**: PCI Class Code (R) – PCI Class Code. This value in this bit field is one of the following three:
  - the default value of 018000h for Mass Storage Class.
  - the value loaded from an external memory device; if an external memory device – Flash or EEPROM – is present with the correct signature, the PCI Class Code is loaded from that device after reset. See section 6 on page 44.
  - system programmed value; if bit 0 of the Configuration register (48_H) is set the PCI Class Code is system programmable.
- **Bit [07:00]**: Revision ID (R) – Chip Revision ID. This bit field is hardwired to indicate the revision level of the chip design; revision 02_H is defined by this specification.

7.1.4 BIST – Header Type – Latency Timer – Cache Line Size

Address Offset: $0C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000 (PCI) / 0x0000_4000 (PCI-X)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BIST								Header Type								Latency Timer								Cache Line Size							

This register defines the various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: BIST (R). This bit field is hardwired to 00_H.
- **Bit [23:16]**: Header Type (R). This bit field is hardwired to 00_H.
- **Bit [15:08]**: Latency Timer (R/W). This bit field is used to specify the time in number of PCI clocks, the SiI3124 as a master is still allowed to control the PCI bus after its GRANT_L is deasserted. The lower four bits [0B:08] are hardwired to 0_H, resulting in a time granularity of 16 clocks. The reset value is 00_H for PCI; 40_H for PCI-X.
- **Bit [07:00]**: Cache Line Size (R/W). This bit field is used to specify the system cacheline size in terms of 32-bit words. The SiI3124, when initiating a read transaction, will issue the Read Multiple PCI command if empty space in its FIFO is greater than the value programmed in this register.

7.1.5 Base Address Register 0

Address Offset: 10_H
Access Type: Read/Write
Reset Value: 0x0000_0000_0000_0004

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Base Address Register 0																															

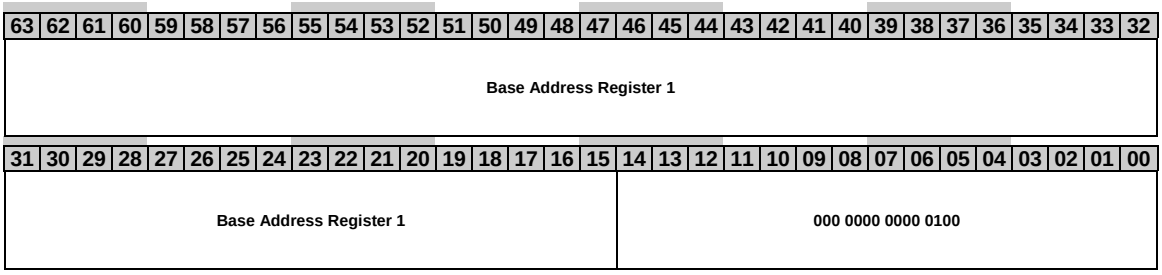
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Base Address Register 0																									0000100						

This register defines the addressing of the Global Registers within the SiI3124. The register bits are defined below.

- **Bit [63:07]**: Base Address Register 0 (R/W). This register defines the base address for the 128-byte Memory Space containing the Global Registers.
- **Bit [06:00]**: (R). This bit field is hardwired to 0000100_B to indicate a 64-bit base address.

7.1.6 Base Address Register 1

Address Offset: 18_H
Access Type: Read/Write
Reset Value: 0x0000_0000_0000_0004

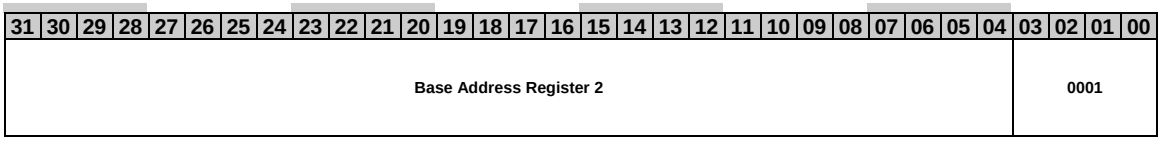


This register defines the addressing of the Port Registers and LRAM within the SiI3124. The register bits are defined below.

- **Bit [63:15]**: Base Address Register 1 (R/W). This register defines the base address for the 32Kbyte Memory Space containing the Port Registers.
- **Bit [14:00]**: (R). This bit field is hardwired to 0004_H to indicate a 64-bit base address.

7.1.7 Base Address Register 2

Address Offset: 20_H
Access Type: Read/Write
Reset Value: 0x0000_0001



This register defines the addressing of the Indirect I/O registers within the SiI3124. The register bits are defined below.

- **Bit [31:04]**: Base Address Register 2 (R/W). This register defines the base address for the 16-byte I/O Space.
- **Bit [03:00]**: (R). This bit field is hardwired to 0001_B.

7.1.8 Subsystem ID – Subsystem Vendor ID

Address Offset: $2C_H$
Access Type: Read/Write
Reset Value: 0x3124_1095

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Subsystem ID																Subsystem Vendor ID															

This register defines the Subsystem ID fields associated with the PCI bus. The register bits are defined below.

- **Bit [31:16]**: Subsystem ID (R) – Subsystem ID.

The value in this bit field is one of the following three:

  - the default value of 0x3124
  - the value loaded from an external memory device; if an external memory device – Flash or EEPROM – is present with the correct signature, the Subsystem ID is loaded from that device after reset. See section 6 on page 44.
  - system programmed value; if bit 0 of the Configuration register (48_H) is set the Subsystem ID is system programmable.

- **Bit [15:00]**: Subsystem Vendor ID (R) – Subsystem Vendor ID.

The value in this bit field is one of the following three:

  - the default value of 0x1095
  - the value loaded from an external memory device; if an external memory device – Flash or EEPROM – is present with the correct signature, the Subsystem Vendor ID is loaded from that device after reset. See section 6 on page 44.
  - system programmed value; if bit 0 of the Configuration register (48_H) is set the Subsystem Vendor ID is system programmable.

7.1.9 Expansion ROM Base Address

Address Offset: 30_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Expansion ROM Base Address													000_0000_0000_0000_000																		Exp ROM Enable

This register defines the Expansion ROM base address associated with the PCI bus. The register bits are defined below.

- **Bit [31:19]**: Expansion ROM Base Address (R/W) – Expansion ROM Base Address. This bit field defines the upper bits of the Expansion ROM base address.
- **Bit [18:01]**: (R). This bit field is hardwired to 00000_H to indicate that the Expansion ROM address range is 512K bytes.
- **Bit [00]**: Exp ROM Enable (R/W) – Expansion ROM Enable. This bit is set to enable Expansion ROM access.

7.1.10 Capabilities Pointer

Address Offset: 34_H
Access Type: Read
Reset Value: 0x0000_0064

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																								Capabilities Pointer							

This register defines the link to a list of new capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:00]**: Capabilities Pointer (R) – Capabilities Pointer. This bit field contains 64_H, the address for the 1st Capabilities register set, the PCI Power Management Capability.

7.1.11 Max Latency – Min Grant – Interrupt Pin – Interrupt Line

Address Offset: $3C_H$
Access Type: Read/Write
Reset Value: 0x0000_0100

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Max Latency								Min Grant								Interrupt Pin								Interrupt Line							

This register defines various control functions associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: Max Latency (R) – Maximum Latency. This bit field is hardwired to 00_H.
- **Bit [23:16]**: Min Grant (R) – Minimum Grant. This bit field is hardwired to 00_H.
- **Bit [15:08]**: Interrupt Pin (R) – Interrupt Pin Used. This bit field is hardwired to 01_H to indicate that the SiI3124 uses the INTA# interrupt. The INTB#, INTC#, and INTD# interrupts may be used by enabling them in the Port Interrupt Enable registers; this use is outside the PCI specification.
- **Bit [07:00]**: Interrupt Line (R/W) – Interrupt Line. This bit field is used by the system to indicate interrupt line routing information. The SiI3124 does not use this information.

7.1.12 PCI-X Capability

Address Offset: 40_H
Access Type: Read/Write
Reset Value: 0x0052_5407

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved									Max Split			Max Mem Rd		En Rlxd Ord	PERR Rcvr	Next Capability Pointer								Capability ID							

This register defines the PCI-X Capability. The register bits are defined below.

- **Bit [31:23]**: Reserved (R) – This bit field is reserved and returns zeros on a read.
- **Bit [22:20]**: Max Split (R/W) – Maximum Outstanding Split Transactions. This bit field sets the maximum number of split transactions the device is permitted to have outstanding. This field is initialized to 101_B to indicate a maximum of 12 outstanding split transactions possible.
- **Bit [19:18]**: Max Mem Rd (R/W) – Maximum Memory Read Byte Count. This bit field is initialized to 00_B.
- **Bit [17]**: En Rlxd Ord (R/W) – Enable Relaxed Ordering. This bit field defaults to 1 to enable relaxed ordering of memory transactions.
- **Bit [16]**: PERR Rcvr (R/W) – Data Parity Recovery Enable. The host driver may set this bit if it can attempt to recover from data parity errors. If this bit is 0, a System Error will be generated if a data parity error is detected.
- **Bit [15:08]**: Next Capability Pointer (R) –Next Capability Pointer. This bit field is hardwired to 54_H to point to the 3rd Capabilities register, the MSI Capability.
- **Bit [07:00]**: Capability ID (R) – PCI Capability ID. This bit field is hardwired to 07_H to indicate that this is a PCI-X Capability.

7.1.13 PCI-X Status

Address Offset: 44_H
Access Type: Read/Write/W1C
Reset Value: 0x12C3_FFF8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved		Split Comp Err		Max Cum Rd			Max Split			Max Rd BC		Dvc Cmplx	UnExp Split	Split Discard	133 MHz	64-bit	Bus Number							Device Number					Function Number		

This register defines the PCI-X capabilities and current operating status of the PCI-X bus. The register bits are defined below.

- **Bit [31:30]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [29]**: Split Comp Err (R/W1C) – Received Split Completion Error Message. This bit is set if a split completion message is received with the split completion error attribute bit set.
- **Bit [28:26]**: Max Cum Rd (R) – Designed Maximum Cumulative Read Size. This bit field is hardwired to 100_B; this corresponds to a maximum 16K byte cumulative outstanding burst memory read transactions.
- **Bit [25:23]**: Max Split (R) – Designed Maximum Outstanding Split Transactions. This bit field is hardwired to 101_B; this corresponds to a maximum of 12 outstanding split transactions.
- **Bit [22:21]**: Max Rd BC (R) – Designed Maximum Memory Read Byte Count. This bit field is hardwired to 10_B; this corresponds to a maximum of 2K bytes for a memory read transaction.
- **Bit [20]**: DVC Cmplx (R) – Device Complexity. This bit is hardwired to 0; the SiI3124 is not a bridge.
- **Bit [19]**: UnExp Split (W1C) – Unexpected Split Completion. This bit indicates that an unexpected split completion was received.
- **Bit [18]**: Split Discard (W1C) – Split Completion Discarded. This bit indicates that a split completion has been discarded.
- **Bit [17]**: 133 MHz (R) – 133 MHz Capable. This bit is hardwired to 1.
- **Bit [16]**: 64-bit (R) – 64-bit Device. This bit is hardwired to 1.
- **Bit [15:8]**: Bus Number (R) – This bit field is initialized to FF_H.
- **Bit [7:3]**: Device Number (R) – This bit field is initialized to $1F_H$.
- **Bit [2:0]**: Function Number (R) – This bit field is hardwired to 0_H.

7.1.14 Header Write Enable

Address Offset: 48_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																															Hdr Wr Ena

This register contains the Hdr Wr Ena bit (in bit 0) used to enable writing to registers defined as read-only by the PCI specification. This bit is required to meet PCI compliance testing that expects certain registers to be read-only. This bit is set to enable write access to the following registers in the PCI Configuration Header: Device ID ($03\text{-}02_H$), PCI Class Code ($09\text{-}0B_H$), Subsystem Vendor ID ($2D\text{-}2C_H$), and Subsystem ID ($2F\text{-}2E_H$).

7.1.15 MSI Capability

Address Offset: 54_H
Access Type: Read/Write
Reset Value: 0x0080_0005

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								64-bit Addr	Multiple Message Enable			Multiple Message Capable			MSI Enable	Next Capability Pointer								Capability ID							

This register defines the MSI Capability Message Control. The register bits are defined below.

- **Bit [31:24]**: Reserved (R) – This bit field is reserved and returns zeros on a read.
- **Bit [23]**: 64-bit Addr (R) – 64-bit Address Capable. This bit is hardwired to 1.
- **Bit [22:20]**: Multiple Message Enable (R/W) – This bit field defaults to 000_B.
- **Bit [19:17]**: Multiple Message Capable (R/W) – This bit field defaults to 000_B.
- **Bit [16]**: MSI Enable (R/W) – This bit is set to enable Message Signaled Interrupts.
- **Bit [15:08]**: Next Capability Pointer (R) –Next Capability Pointer. This bit field is hardwired to 00_H; this is the last Capability.
- **Bit [07:00]**: Capability ID (R) – This bit field is hardwired to 05_H to indicate that this is a MSI Capability.

7.1.16 Message Address

Address Offset: $58_H\text{-}5F_H$
Access Type: Read/Write
Reset Value: 0x0000_0000_0000_0000

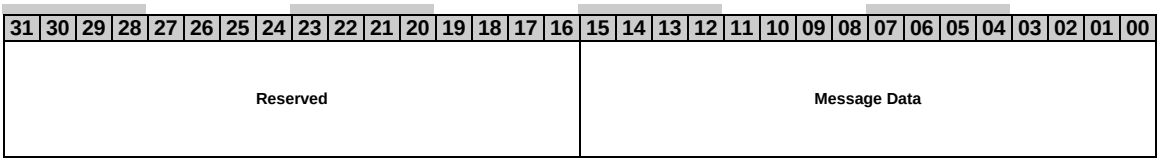
63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
Message Address Upper																															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Message Address																														00	

This register specifies the memory address for an MSI memory write transaction. The memory address must be of a Dword (bits 1:0 must be 0).

7.1.17 MSI Message Data

Address Offset: 60_H
Access Type: Read/Write
Reset Value: 0x0000_0000

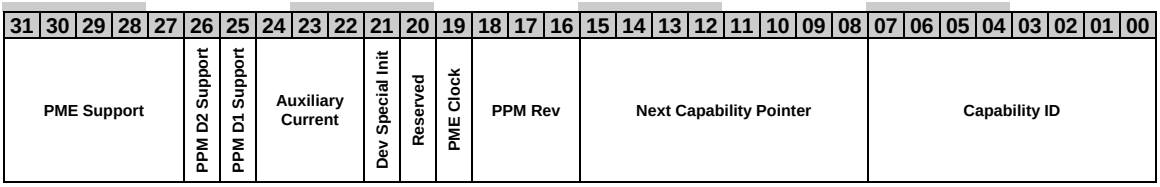


This register specifies the MSI Message Data. The register bits are defined below.

- **Bit [31:16]**: Reserved (R) – This bit field is reserved and returns zeros on a read.
- **Bit [15:00]**: Message Data (R/W) – This bit field specifies the Message Data for an MSI memory write transaction.

7.1.18 Power Management Capability

Address Offset: 64_H
Access Type: Read Only
Reset Value: 0x0622_4001

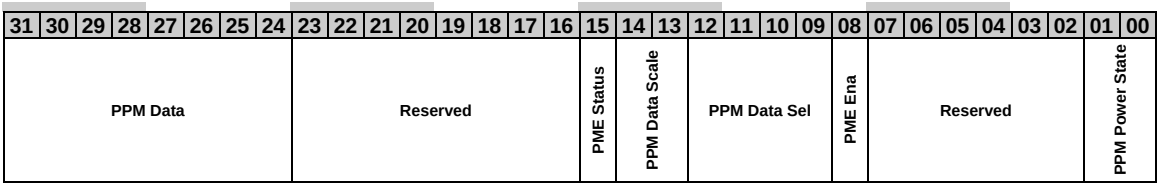


This register defines the power management capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:27]**: PME Support (R) – Power Management Event Support. This bit field is hardwired to 00_H; the SiI3124 does not support PME.
- **Bit [26]**: PPM D2 Support (R) – PCI Power Management D2 Support. This bit is hardwired to 1.
- **Bit [25]**: PPM D1 Support (R) – PCI Power Management D1 Support. This bit is hardwired to 1.
- **Bit [24:22]**: Auxiliary Current (R) – Auxiliary Current. This bit field is hardwired to 000_B.
- **Bit [21]**: Dev Special Init (R) – Device Special Initialization. This bit is hardwired to 1 to indicate that the SiI3124 requires special initialization.
- **Bit [20]**: Reserved (R). This bit is reserved and returns zero on a read.
- **Bit [19]**: PME Clock (R) – Power Management Event Clock. This bit is hardwired to 0; the SiI3124 does not support PME.
- **Bit [18:16]**: PPM Rev (R) – PCI Power Management Revision. This bit field is hardwired to 010_B to indicate compliance with the PCI Power Management Interface Specification revision 1.1.
- **Bit [15:08]**: Next Capability Pointer (R) – PCI Next Capability Pointer. This bit field is hardwired to 40_H to point to the 2nd Capabilities register, the PCI-X Capability.
- **Bit [07:00]**: Capability ID (R) – PCI Capability ID. This bit field is hardwired to 01_H to indicate that this is a PCI Power Management Capability.

7.1.19 Power Management Control + Status

Address Offset: 68_H
Access Type: Read/Write
Reset Value: 0x1900_2000



This register defines the power management capabilities associated with the PCI bus. The register bits are defined below.

- **Bit [31:24]**: PPM Data (R) – PCI Power Management Data. This bit field is hardwired to 0x19 to indicate a power consumption of 2.5 Watt.
- **Bit [23:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [15]**: PME Status (R) – PME Status. This bit is hardwired to 0. The SiI3124 does not support PME.
- **Bit [14:13]**: PPM Data Scale (R) – PCI Power Management Data Scale. This bit field is hardwired to 01_B to indicate a scaling factor of 100 milliwatts.
- **Bit [12:09]**: PPM Data Sel (R/W) – PCI Power Management Data Select. This bit field is set by the system to indicate which data field is to be reported through the PPM Data bits (although current implementation hardwires the PPM Data to indicate 2.5 Watt).
- **Bit [08]**: PME Ena (R) – PME Enable. This bit is hardwired to 0. The SiI3124 does not support PME.
- **Bit [07:02]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [01:00]**: PPM Power State (R/W) – PCI Power Management Power State. This bit field is set by the system to dictate the current Power State: 00 = D0 (Normal Operation), 01 = D1, 10 = D2, and 11 = D3 (Hot).

7.2 Internal Register Space – Base Address 0

These registers are 32 or 64 bits wide and are the Global Registers of the SiI3124. Access to this register space is through the PCI Memory space. In the following table a dashed line separates the register pairs that may be accessed as a 64-bit register.

Address Offset	Register Name		
00_H	Port 0 Slot Status		
04_H	Port 1 Slot Status		
08_H	Port 2 Slot Status		
$0C_H$	Port 3 Slot Status		
10_H-$3F_H$	Reserved		
40_H	Global Control		
44_H	Global Interrupt Status		
48_H	PHY Configuration		
$4C_H$-$6F_H$	Reserved		
50_H	BIST Control		
54_H	BIST Pattern		
58_H	BIST Status		
70_H	Flash Address		
74_H	GPIO		Flash Data
78_H	I^2C Address		
$7C_H$	I^2C Control	Reserved	I^2C Data

Table 7-2 SiI3124 Internal Register Space – Base Address 0

7.2.1 Port Slot Status Registers

Address Offset: 00_H-$0F_H$
Access Type: Read
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Attention	Slot Status																														

These 4 registers provide the Status for the 31 Command Slots for each of the 4 ports. Adjacent pairs of registers may be accessed together as a single 64-bit access and all four registers can therefore be read in 2 bus cycles. These registers also appear in Port register space. Reading this register will clear the Command Completion Status for the port if the Interrupt No Clear on Read bit (bit 3) of the Port Control register is 0. The register bits are defined below.

- **Bit [31]**: Attention (R) – This bit indicates that something occurred in the corresponding port that requires the attention of the host. Other port registers must be examined to determine the origin of the error. This bit is the logical OR of the masked interrupt conditions, except for Command Completion, reported in the Port Interrupt Status register.
- **Bit [30:0]**: Slot Status (R) – These bits are the Active status bits corresponding to Slot numbers 30 to 0. The Active status bit for a slot is set when the Slot number is written to the Command Execution FIFO (direct command transfer method) or when a Command Activation register is written (indirect command transfer method).

7.2.2 Global Control

Address Offset: 40_H
Access Type: Read/Write
Reset Value: 0x8XXX_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Global Reset	MSIACK	I2C Int Enable	PERR Rpt Dsbl	Reserved			3Gb/s Capable	Reserved			REQ64 @RST	DEVSEL @RST	STOP @RST	TRDY @RST	M66EN	Reserved												Port 3 Int Enable	Port 2 Int Enable	Port 1 Int Enable	Port 0 Int Enable

This register controls various functions of the chip.

- **Bit [31]**: Global Reset (R/W). This bit, when set to one, asserts a port reset to all ports. This bit must be cleared to zero to allow normal operation. Once set by this bit, all port resets will remain set to one until explicitly cleared to zero through the individual port control clear registers. Refer to the port control set register description for more information.
- **Bit [30]**: MSI Acknowledge (W). Writing a one to this bit acknowledges a Message Signaled Interrupt and permits generation of another MSI. This bit is cleared immediately after the acknowledgement is recognized by the control logic, hence the bit will always be read as a zero.
- **Bit [29]**: I2C Int Enable (R/W). This bit, when set to one, allows assertion of an interrupt when the I2C Interrupt is asserted. When set to zero, the interrupt is masked.
- **Bit [28]**: PERR Rpt Dsbl (R/W) – PERR Report Disable. This bit, when set to one, disables reporting of PCI bus parity errors to the Command Execution State Machine (such errors would otherwise cause the state machine to stop and report an error in the Command Error register).
- **Bit [27:25,23:20,15:4]**: Reserved (R). These bits are reserved and will return zeroes when read.

- **Bit [24]**: 3Gb/s Capable (R). This bit indicates whether the device is configured and tested for 3Gb/s (S-ATA generation 2) operation. A zero indicates 1.5Gb/s operation. A one indicates 3Gb/s operation.
- **Bit [20:17]**: REQ64, DEVSEL, STOP, TRDY (R). These bits report the latched status of the corresponding PCI bus signals that are latched at the rising edge of PCI RST# (when FRAME# and IRDY# are deasserted). Latched REQ64 indicates whether the PCI bus is 32 bits or 64 bits. Latched DEVSEL, STOP, and TRDY are decoded as shown in the following table.

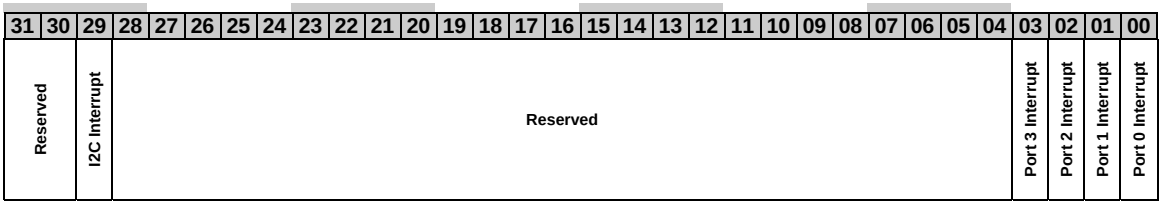
DEVSEL	STOP	TRDY	Mode	Min Clock	Max Clock
Off	Off	Off	PCI, M66EN Off	0	33
			PCI, M66EN On	33	66
Off	Off	On	PCI-X	50	66
Off	On	Off	PCI-X	66	100
Off	On	On	PCI-X	100	133
On	-	-	PCI-X	Reserved	Reserved

Table 7-3 PCI bus Mode

- **Bit [16]**: M66EN (R). This bit reports the status of the M66EN PCI bus signal that indicates whether the PCI clock is 33 MHz (or less) or up to 66 MHz as shown in the preceding table.
- **Bit [3:0]**: Port Interrupt Enable (R/W). These bits, when set to one, allow assertion of an interrupt when the corresponding port asserts an interrupt. When set to zero, the corresponding port interrupts are masked.

7.2.3 Global Interrupt Status

Address Offset: 44_H
Access Type: Read/Write 1 Clear
Reset Value: 0x0000_0000

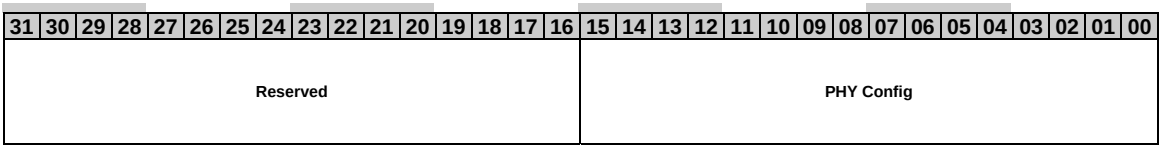


This register is used to determine the status of various chip functions.

- **Bit [31:30]**: Reserved (R). This bit field is reserved and returns zeroes when read.
- **Bit [29]**: I2C Interrupt (R/W1C). This bit indicates that the I2C Interrupt is pending. Writing a 1 to this bit clears the interrupt.
- **Bit [28:4]**: Reserved (R). This bit field is reserved and returns zeroes when read.
- **Bit [3:0]**: Port Interrupt Status (R/W1C). These bits, when set to one, indicate that the corresponding port has an interrupt condition pending. Writing a 1 to any of these bits clears the corresponding Command Completion Interrupt Status, but not other interrupt sources.

7.2.4 PHY Configuration

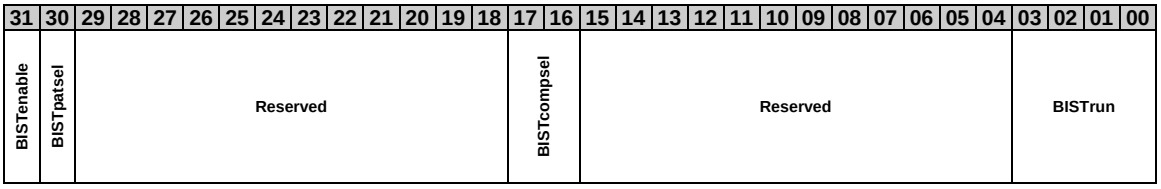
Address Offset: 48_H
Access Type: Read/Write
Reset Value: 0x0000_2C05



The PHY Configuration register is reset to 0x00002C05. These bits should not be changed from their defaults as erratic operation may result (including bits identified as Reserved).

7.2.5 BIST Control Register

Address Offset: 50_H
Access Type: Read/Write
Reset Value: 0x0000_0000

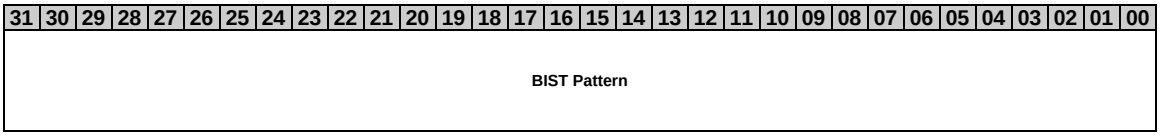


This register is used to control Data Loopback BIST.

- **Bit [31]**: BISTenable (R/W) – This bit enables the data paths for running data loopback BIST.
- **Bit [30]**: BISTpatsel (R/W) – This bit selects whether a repeating pattern (supplied from the BIST Pattern register) or a pseudorandom pattern is used for running data loopback BIST. Setting the bit to 1 selects the repeating pattern.
- **Bit [29:18]**: Reserved (R/W). These bits are reserved and must write zeros.
- **Bit [17:16]**: BISTcompsel (R/W). This bit field selects the port from which loopback data is selected for pattern comparison.
- **Bit [15:04]**: Reserved (R/W). These bits are reserved and must write zeros.
- **Bit [03:00]**: BISTrun (R/W). This bit field selects the port(s) that transmit loopback data.

7.2.6 BIST Pattern Register

Address Offset: 54_H
Access Type: Read/Write
Reset Value: 0x0000_0000



This register contains the 32-bit fixed pattern that is repeatedly transmitted in data loopback when the BISTpatsel bit (bit 30) of the BIST Control register is set to 1.

7.2.7 BIST Status Register

Address Offset: 58_H
Access Type: Read
Reset Value: 0x8000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
BISTgood	Reserved																			BISTerrcnt											

- **Bit [31]**: BISTgood (R) – This bit indicates that all comparisons have been good since initiating data loopback BIST. This bit is initialized (to 1) when the BISTenable bit is zero in the BIST Control register.
- **Bit [30:12]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [11:00]**: BISTerrcnt (R). This bit field indicates the number of comparisons that have been in error since initiation of data loopback BIST. This counter is a saturating counter (it stops counting at $0FFF_H$). This counter is cleared when the BISTenable bit is zero in the BIST Control register.

7.2.8 Flash Address

Address Offset: 70_H
Access Type: Read/Write
Reset Value: 0xXXXX_XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
GPIO Enable	Reserved '0001'				Mem Present	Mem Access Start	Mem Access Type	Reserved					Memory Address																			

This register is the address and command/status register for the Flash memory interface. The register bits are defined below.

- **Bit [31]**: GPIO Enable (R/W). This bit, when set to one, enables the use of the Flash Data pins for General Purpose I/O.
- **Bit [30:27]**: Reserved (R). This bit field is reserved and returns '0001' on a read.
- **Bit [26]**: Mem Present (R) – Memory Present. This bit set indicates that the auto-initialization signature was read correctly from the Flash Memory.
- **Bit [25]**: Mem Access Start (R/W) – Memory Access Start. This bit is set to initiate an operation to Flash memory. This bit is self-clearing when the operation is complete.
- **Bit [24]**: Mem Access Type (R/W) – Memory Access Type. This bit is set to define a read operation from Flash memory. This bit is cleared to define a write operation to Flash memory.
- **Bit [23:19]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [18:00]**: Memory Address (R/W). This bit field is programmed with the address for a Flash memory read or write access.

7.2.9 Flash Memory Data / GPIO Control

Address Offset: 74_H
Access Type: Read/Write
Reset Value: 0x00XX_XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved								GPIO Control								Transition Detect								Memory Data							

This register contains the GPIO data/control fields and the Flash memory data register.

- **Bit [31:24]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [23:16]**: GPIO Control (R/W). The bits of this field are written to control the output type for corresponding Flash data lines; if a bit is a 1 the corresponding output is an open drain output (only driven low); if a 0 the corresponding output is always driven. To use a GPIO pin as an input, the control bit must be set to 1 (open-drain output) and the data bit must be set to 1 (undriven).
- **Bit [15:08]**: Transition Detect (R/C). The bits of this field report signal transition detection on the corresponding FLASH data input; reading the register resets the transition detect bits.
- **Bit [07:00]**: Memory Data (R/W) – Flash Memory Data. This bit field is used for Flash write data on a write operation, and returns the Flash read data on a read operation. For GPIO, this field is used to write the GPIO output register and to read the GPIO input signals.

7.2.10 I²C Address

Address Offset: 78_H
Access Type: Read/Write
Reset Value: 0xXXXX_XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Control Byte								I²C Address (Addr Byte Cnt = '11')																							
Control Code				Chip Select			I²C Access Type																								
								Unused								I²C Address (Addr Byte Cnt = '10')															
								Unused																I²C Address (Addr Byte Cnt = '01')							

This register holds the Address Bytes and Control Byte for the I²C interface. The register bits are defined below.

- **Bit [31:24]**: Control Byte (R/W). This bit field contains the Control Code, Chip Select and Access Type for an I²C access. Access Type set to '1' defines a read operation.
- **Bit [23:00]**: I²C Address (R/W). This bit field contains the address for an I²C access. The number of address bytes used is determined by the setting of the Address Byte Count field in the I²C Data register.

7.2.11 I²C Data / Control

Address Offset: $7C_H$
Access Type: Read/Write
Reset Value: 0xXXXX_00XX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
I²C Access Start	Addr Byte Cnt		I²C Error	Reserved '1'	Mem Present	Read Buffer Full	Write Buffer Empty	Data Transfer Count								Reserved								I²C Data							

This register is the Data and Control register for the I²C interface.

- **Bit [31]**: I²C Access Start (R/W) – This bit is set to initiate an I²C operation. This bit is self-clearing when the operation is complete.
- **Bit [30:29]**: Addr Byte Cnt (R/W) – Address Byte Count. The value written to this bit field specifies the number of address bytes (0 to 3) to be transferred during an I²C access. If this field is '00' only the Control Byte is transferred; if it is '01' the Control Byte and bits 7:0 of the I²C Address register are transferred; it it is '10' the Control Byte and bits 15:0 of the I²C Address register are transferred; it it is '11' the Control Byte and bits 23:0 of the I²C Address register are transferred. The value read from this bit field indicates the number of address bytes that have been transferred. Once an I²C access has completed, as indicated by bit 31, the read value and write value of this field will be equal.
- **Bit [28]**: I²C Error (R/W1C) – I²C Access Error. This bit set indicates that the I²C interface logic has detected three NAKs on the I²C interface. This typically occurs if no I²C device is present.
- **Bit [27]**: Reserved (R) This bit is reserved and returns '1' on a read.
- **Bit [26]**: Mem Present (R) – Memory Present. This bit set indicates that the auto-initialization signature was read correctly from the EEPROM connected to the I²C interface.
- **Bit [25]**: Read Buffer Full (R). This bit indicates that read data from the I²C controller is ready.
- **Bit [24]**: Write Buffer Empty (R). This bit indicates that the I²C controller is ready to accept a byte for writing.
- **Bit [23:16]**: Data Transfer Count (R/W). The value written to this bit field specifies the number of data bytes (0 to 255) to be transferred during an I²C access. The value read from this bit field indicates the number of data bytes that have been transferred. Once an I²C access has completed, as indicated by bit 31, the read value and write value of this field will be equal.
- **Bit [15:08]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [07:00]**: I²C Data (R/W) – This bit field is used for I²C write data on a write operation, and returns the I²C read data on a read operation.

7.3 Internal Register Space – Base Address 1

These registers are 32 bits wide and are the Port Registers and LRAM of the SiI3124. Access to these registers is through the PCI Memory space. Register descriptions that follow specify the address offset for Port 0; subsequent port registers are at 2000_H offset increments, i.e., the upper 2 bits of the 15-bit address offset is the Port number (0-3).

Address Offset	Register Name
000_H-$F7F_H$	Port 0 LRAM Slots
$F80_H$-FFF_H	Port Multiplier Device Status/QActive Registers
1000_H	Write: Port 0 Control Set / Read: Port 0 Status
1004_H	Write: Port 0 Control Clear
1008_H	Port 0 Interrupt Status
$100C_H$	Reserved
1010_H	Port 0 Interrupt Enable Set
1014_H	Port 0 Interrupt Enable Clear
1018_H	Reserved
$101C_H$	32-bit Activation Upper Address
1020_H	Port 0 Command Execution FIFO
1024_H	Port 0 Command Error
1028_H	Port 0 FIS Configuration
$102C_H$	Port 0 PCI(X) Request FIFO Threshold
1030_H-$103F_H$	Reserved
1040_H	Port 0 8B/10B Decode Error Counter
1044_H	Port 0 CRC Error Counter
1048_H	Port 0 Handshake Error Counter
$104C_H$	Reserved
1050_H	Port PHY Configuration
1054_H-$17FF_H$	Reserved
1800_H	Port 0 Slot Status
1804_H-$1BFF_H$	Reserved
$1C00_H$-$1CF7_H$	Command Activation Registers
$1CF8_H$-$1E03_H$	Reserved
$1E04_H$	Port Context Register
$1E08_H$-$1EFF_H$	Reserved
$1F00_H$	Port 0 SControl
$1F04_H$	Port 0 SStatus
$1F08_H$	Port 0 SError
$1F0C_H$	Port 0 SActive (indirect location)
$1F10_H$-$1FFF_H$	Reserved
2000_H-$3FFF_H$	Port 1 Registers mapped as above
4000_H-$5FFF_H$	Port 2 Registers mapped as above
6000_H-$7FFF_H$	Port 3 Registers mapped as above

Table 7-4 SiI3124 Internal Register Space – Base Address 1

7.3.1 Port LRAM

Address Offset: 000_H-FFF_H
Access Type: Read/Write
Reset Value: indeterminate

The Port LRAM consists of 31 Slots of 128 bytes each and a 32nd "Slot" used to hold 16 Port Multiplier Device Specific Registers.

Address Offset	Description
000_H-$07F_H$	Slot 0
080_H-$0FF_H$	Slot 1
100_H-$17F_H$	Slot 2
180_H-EFF_H	Slots 3-29
$F00_H$-$F7F_H$	Slot 30
$F80_H$-$F83_H$	Port Multiplier Device 0 Status Register
$F84_H$-$F87_H$	Port Multiplier Device 0 QActive Register
$F88_H$-$F8B_H$	Port Multiplier Device 1 Status Register
$F8C_H$-$F8F_H$	Port Multiplier Device 1 QActive Register
$F90_H$-$FF7_H$	Port Multiplier Device Registers for Devices 2-14
$FF8_H$-FFB_H	Port Multiplier Device 15 Status Register
FFC_H-FFF_H	Port Multiplier Device 15 QActive Register

Table 7-5 Port LRAM layout

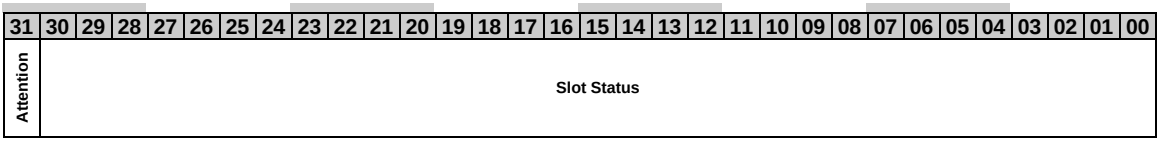
Address Offset	Description	
000_H-$01F_H$	Current FIS and Control	Port Request Block (PRB)
020_H-$02F_H$	Scatter/Gather Entry 0 or ATAPI command packet	
030_H-$03F_H$	Scatter/Gather Entry 1	
040_H-047_H	Command Activation Register (Actual)	
040_H-$07F_H$	Scatter/Gather Table	
$1C00_H$-$1C07_H$	Command Activation Register (Shadow)	

Table 7-6 Port LRAM Slot layout

A Port LRAM Slot is 128 bytes used to define Serial-ATA commands. The addresses shown above are for slot 0.

7.3.2 Port Slot Status

Address Offset: 1800_H
Access Type: Read
Reset Value: 0x0000_0000



This register provides the status for the 31 Command Slots for the Serial-ATA port. This register also appears along with the Port Status register of the other 3 ports in Global register space. Reading this register will clear the Command Completion Status for the port if the Interrupt No Clear on Read bit (bit 3) of the Port Control register is 0. The register bits are defined below.

- **Bit [31]**: Attention (R) – This bit indicates that something occurred in the port that requires the attention of the host. Other port registers must be examined to determine the origin of the error. This bit is the logical OR of the masked interrupt conditions reported in the Port Interrupt Status register.
- **Bit [30:0]**: Slot Status (R) – These bits are the Active status bits corresponding to Slot numbers 30 to 0. The Active status bit is set when a command is transferred to the Slot RAM.

7.3.3 Port Control Set

Address Offset: Set: 1000_H
Access Type: Write One To Set
Reset Value: N/A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved						OOB Bypass	Reserved									LED On	Auto Interlock Accept	PM Enable	Interlock Accept	Interlock Rejec t	32-bit Activation	Scramble Disable	CONT Disable	Transmit BIST	Resume	Packet Length	LED Disable	Interrupt NCoR	Port Initialize	Device Reset	Port Reset

This register is used to direct various port operations. A one written to a bit position sets that bit in the control register.

- **Bit [31:26,24:16,6]**: Reserved (R). These bits are reserved.
- **Bit [25]**: OOB Bypass (W1S). If this bit is set, the Link will bypass the OOB initialization sequence following a reset. This bit is reset by Global Reset, and not reset by Port Reset.
- **Bit [15]**: LED On (W1S). This bit turns on the LED Port Activity indicator regardless of the state of LED Disable (bit 4).
- **Bit [14]**: Auto Interlock Accept (W1S). When this bit is set the link will accept any interlocked FIS reception. The link will transmit R_OK in response to the received FIS.
- **Bit [13]**: PM Enable (W1S). This bit enables Port Multiplier support.
- **Bit [12]**: Interlock Accept (W1S). This bit is used to signal the link to accept an interlocked FIS reception. The link will transmit R_OK in response to the received FIS. This bit is self-clearing.
- **Bit [11]**: Interlock Reject (W1S). This bit is used to signal the link to reject an interlocked FIS reception. The link will transmit R_ERR in response to the received FIS. This bit is self-clearing.
- **Bit [10]**: 32-bit Activation (W1S). When this bit is set to one, a write to the low 32 bits of a Command Activation register will cause the 32-bit Activation Upper Address register contents to be written to the upper 32 bits of the Command Activation register and will trigger command execution. When this bit is zero, a write to the upper 32 bits or all 64 bits of a command activation register is required to trigger command execution. This bit is set for environments that do not address more than 2^{32} bytes of host memory.
- **Bit [9]**: Scrambler Disable (W1S). When this bit is set to one, the Link scrambler operation is disabled.
- **Bit [8]**: CONT Disable (W1S). When this bit is set to one, the Link will not generate a CONT following repeated primitives.
- **Bit [7]**: Transmit BIST (W1S). This bit causes transmission of a BIST FIS.
- **Bit [6]**: Resume (W1S).
- **Bit [5]**: Packet Length (W1S). This bit directs the length of the packet command to be sent for commands with packet protocol. When this bit is zero, a 12-byte packet will be sent. When this bit is one, a 16-byte packet will be sent. This bit should be set to the same value as derived from word 0 of the identify packet command returned data.
- **Bit [4]**: LED Disable (R/W). This bit disables the operation of the LED Port Activity indicator.
- **Bit [3]**: Interrupt No Clear on Read (W1S). When this bit is set to one, a command completion interrupt may be cleared only by writing a one to the Command Completion bit in the Port Interrupt Status register. When this bit is zero, reading the Port Slot Status register may also be used to clear the Command Completion interrupt.
- **Bit [2]**: Port Initialize (W1S). Setting this bit to one causes all commands to be flushed from the port and all command execution parameters to be set to an initialized state. Setting this bit to one causes the port ready bit in the port status register to be cleared to zero. When the initialization procedure is complete, the port ready bit will be set to one. This bit is self-clearing and will be cleared upon execution by the port.
- **Bit [1]**: Device Reset (W1S). Setting this bit to one causes all commands to be flushed from the port and all command execution parameters to be set to an initialized state. Setting this bit to one causes the port ready bit in the port status register to be cleared to zero. The port will generate the COMRESET primitive on the serial ATA bus. When the out of band sequence and initialization procedure is complete, the port ready bit will be set to one. This bit is self-clearing and will be cleared upon execution by the port.
- **Bit [0]**: Port Reset (W1S). Setting this bit to one causes the port to be held in a reset state. No commands will be executed while in this state. All port registers and functions are reset to their initial state, except as noted below. All commands are flushed from the port and all command execution parameters are set to an initialized state. Setting this bit to one causes the port ready bit in the port status register to be cleared to zero. Upon setting this bit to zero from an asserted state, the port will generate the COMRESET primitive on the serial ATA bus. When the out of band sequence and initialization procedure is complete, the port ready bit will be set to

one. This bit is set to one by the Global reset, which is set by a PCI reset, and remains set until cleared by the host (by writing a one to bit 0 of the Port Control Clear register).
The register bits that are not initialized by the Port Reset are:

- OOB Bypass (bit 25) in Port Control (this register)
- Port PHY Configuration register (all bits)

7.3.4 Port Status

Address Offset: 1000_H
Access Type: Read
Reset Value: 0x001F_0001

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Port Ready	Reserved					OOB Bypass	Reserved				Active Slot					LED On	Auto Interlock Accept	PM Enable	Interlock Accept	Interlock Reject	32-bit Activation	Scramble Disable	CONT Disable	Transmit BIST	Resume	Packet Length	LED Disable	Interrupt NCoR	Port Initialize	Device Reset	Port Reset

This register is used to determine the status of various port functions.

- **Bit [31]**: Port Ready (R). This bit reports the Port Ready status. The transition from 0 to 1 of this bit generates the Port Ready Interrupt Status (bit 18/2 of the Port Interrupt Status register).
- **Bit [30:26,24:21]**: Reserved (R). These bits are reserved.
- **Bit [20:16]**: Active Slot (R). This bit field contains the slot number of the command currently being executed. When a command error occurs, this bit field indicates the slot containing the command in error.
- **Bit [25,15:0]**: These bits reflect the current state of the corresponding bits in the Port Control register. Refer to the Port Control Set register for a complete description.

7.3.5 Port Control Clear

Address Offset: 1004_H
Access Type: Write One To Clear
Reset Value: N/A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved						OOB Bypass	Reserved									LED On	Auto Interlock Accept	PM Enable	Reserved		32-bit Activation	Scramble Disable	CONT Disable	Transmit BIST	Reserved	Packet Length	LED Disable	Interrupt NCoR	Reserved		Port Reset

This register is used to direct various port operations. A one written to a bit position clears that bit in the control register.

- **Bit [31:26,24:16,12:11,6,2:1]**: Reserved (R). These bits are reserved.
- **Bit [25,15:13,10:7,5:3,0]**: (W1C) Writing a one to these bits clears the associated bit position of the Port Control register. Refer to the Port Control Set register for bit descriptions.

7.3.6 Port Interrupt Status

Address Offset: 1008_H
Access Type: Read/Write 1 Clear
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Reserved	SDB Notify	Hshk Error Thresh	CRC Error Thresh	8b/10 Error Thresh	DevExchg	UnrecFIS	Comwake	PhyRdyChg	PM Change	Port Ready	Command Error	Cmd Completion	Reserved	SDB Notify	Hshk Error Thresh	CRC Error Thresh	8b/10 Error Thresh	DevExchg	UnrecFIS	Comwake	PhyRdyChg	PM Change	Port Ready	Command Error	Cmd Completion

This register is used to report the interrupt status. The status bits in the upper half of the register report the described condition. The status bits in the lower half of the register are masked by the corresponding interrupt enable bits or by the setting in the corresponding threshold registers. Writing a 1 to either interrupt status bit clears it.

- **Bit [31:28,15:12]**: Reserved (R). These bits are reserved.
- **Bit [27/11]**: SDB Notify (W1C). This bit indicates that a Set Device Bits FIS was received with the N-bit (bit 15 of first dword) set to one.
- **Bit [26/10]**: Handshake Error Threshold (W1C). This bit indicates that the Handshake error count is equal to or greater than the Handshake error threshold. Bit 10 is masked if the Handshake Error Threshold register contains a zero threshold setting. When a 1 is written to this bit, both the status bit and the Handshake Error Counter are cleared.
- **Bit [25/9]**: CRC Error Threshold (W1C). This bit indicates that the CRC error count is equal to or greater than the CRC error threshold. Bit 9 is masked if the CRC Error Threshold register contains a zero threshold setting. When a 1 is written to this bit, both the status bit and the CRC Error Counter are cleared.
- **Bit [24/8]**: 8b/10b Decode Error Threshold (W1C). This bit indicates that the 8b/10b Decode error count is equal to or greater than the 8b/10b Decode error threshold. Bit 8 is masked if the 8b/10b Decode Error Threshold register contains a zero threshold setting. When a 1 is written to this bit, both the status bit and the 8b/10b Decode Error Counter are cleared.
- **Bit [23/7]**: DevExchg (Device Exchanged) (W1C) – This bit is the X bit in the DIAG field of the SError register. It may be cleared by writing a corresponding one bit to either register.
- **Bit [22/6]**: UnrecFIS (Unrecognized FIS Type) (W1C) – This bit is the F bit in the DIAG field of the SError register. It may be cleared by writing a corresponding one bit to either register.
- **Bit [21/5]**: ComWake (W1C) – This bit is the W bit in the DIAG field of the SError register. It may be cleared by writing a corresponding one bit to either register.
- **Bit [20/4]**: PhyRdyChg (W1C) – This bit is the N bit in the DIAG field of the SError register. It may be cleared by writing a corresponding one bit to either register.
- **Bit [19/3]**: PM Change (W1C). This bit indicates that a change has occurred in the power management state.
- **Bit [18/2]**: Port Ready (W1C). This bit indicates that the port has become ready to accept and execute commands. This status indicates that Port Ready (bit 31 in the Port Status register) has made a 0 to 1 transition. Clearing this status does not change the Port Ready bit in the Port Status register and this status is not set subsequently until the Port Ready bit changes state.
- **Bit [17/1]**: Command Error (W1C). This bit indicates that an error occurred during command execution. The error type can be determined via the port error register.
- **Bit [16/0]**: Command Completion (W1C). This bit indicates that one or more commands have completed execution.

7.3.7 Port Interrupt Enable Set / Port Interrupt Enable Clear

Address Offset: 1010_H / 1014_H
Access Type: Read/Write 1 Set/Write 1 Clear
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Interrupt Steering																				SDB Notify				DevExchg	UnrecFIS	Comwake	PhyRdyChg	PM Change	Port Ready	Command Error	Cmd Completion
Reserved																					Reserved										

The Interrupt Enable register is controlled by these registers. Writing to the Interrupt Enable Set register sets the Interrupt Enable bits; the enable bit is set for each corresponding bit to which a 1 is written. Writing to the Interrupt Enable Clear register clears the Interrupt Enable bits; the enable bit is cleared for each corresponding bit to which a 1 is written. The Interrupt Enable register may be read at either address offset.

Note that bits 8, 9, and 10 do not have an enable bit; the corresponding interrupts are enabled by corresponding threshold registers.

- **Bit [31:30]**: Interrupt Steering (R/W). This bit field specifies which one of the four interrupt lines is to be used for interrupts from this port. INTA# is selected by 00_B; INTB# by 01_B; INTC# by 10_B; and INTD# by 11_B.
- **Bit [29:12,10:8]**: Reserved (R). These bits are reserved and return zeros on a read.
- **Bit [11,7:0]**: Interrupt Enables (R/W1S/W1C). These bits are the interrupt enables for the corresponding bits of the Interrupt Status register.

7.3.8 32-bit Activation Upper Address

Address Offset: $101C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Upper Address																															

This register contains the 32-bit value written to the upper half of the Command Activation register when the lower half of that register is written and the 32-bit Activation control bit (bit 10) is set in the Port Control register.

7.3.9 Port Command Execution FIFO

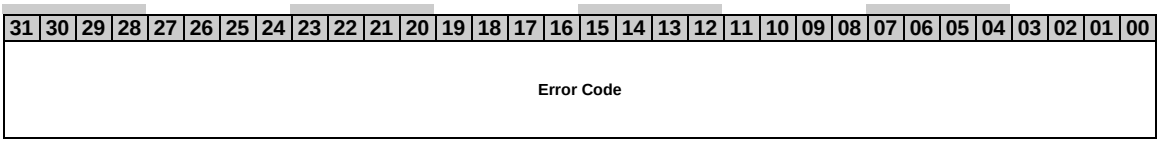
Address Offset: 1020_H
Access Type: Read/Write
Reset Value: 0x0000_00XX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																											Execution Slot Number				

When written, this register causes the supplied slot number to be pushed into the tail of the command execution FIFO. A valid PRB must be populated in the associated slot in port LRAM. When read, this register supplies the entry at the head of the command execution FIFO. The FIFO is not popped as a result of a read operation.

7.3.10 Port Command Error

Address Offset: 1024_H
Access Type: Read
Reset Value: 0x0000_0000



This register contains the error type resulting from a command error. The following table lists the error codes, error names, and error descriptions.

Table 7-7 Command Error Codes

Error Name	Code	Description
DEVICEERROR	1	The ERR bit was set in a "register - device to host" FIS received from the device. The task file registers are written back to PRB slot for host scrutiny.
SDBERROR	2	The ERR bit was set in a "set device bits" FIS received from the device.
DATAFISERROR	3	The SiI3124 detected an error during command execution that was not reported by the device upon command completion.
SENDFISERROR	4	The SiI3124 was unable to send the Initial command FIS for a command. This can occur if a low-level link error occurs during command transmission.
INCONSISTENTSTATE	5	The SiI3124 detected an inconsistency in protocol. Any departure from standard Serial ATA protocol that causes indecision in the internal sequencers will cause this error.
DIRECTIONERROR	6	A Data FIS was received when a write data protocol was specified or a DMA Activate FIS was received when a read data protocol was specified.
UNDERRUNERROR	7	While transferring data from the SiI3124 to a device, the end of the Scatter Gather list was encountered before the entire transfer was completed. The device is requesting additional data but there is no Scatter Gather Entry to define the source of data.
OVERRUNERROR	8	While transferring data from a device to the SiI3124, the end of the Scatter Gather list was encountered before the entire transfer was completed. Data was received from the device but there is no Scatter Gather Entry to define where the data should be deposited.
LINKFIFOOVERRUN	9	The link FIFO list was over run.
PACKETPROTOCOLERROR	11	During the first PIO setup of Packet command, the data direction bit was invalid, indicating a transfer from device to host.
PLDSGTERRORBOUNDARY	16	A requested Scatter Gather Table not aligned on a quadword boundary. All addresses defining Scatter Gather Tables must be quadword aligned. Bits[2:0] must be zeroes.
PLDSGTERRORTARGETABORT	17	A PCI Target Abort occurred while the SiI3124 was fetching a Scatter Gather Table from host memory.
PLDSGTERRORMASTERABORT	18	A PCI Master Abort occurred while the SiI3124 was fetching a Scatter Gather Table from host memory.
PLDSGTERRORPCIPERR	19	A PCI Parity Error occurred while the SiI3124 was fetching a Scatter Gather Table from host memory.
PLDCMDERRORBOUNDARY	24	The address of a PRB written to a command activation register was not aligned on a quadword boundary. All PRB addresses must be quadword aligned. Bits[2:0] must be zeroes.
PLDCMDERRORTARGETABORT	25	A PCI Target Abort occurred while the SiI3124 was fetching a Port Request Block (PRB) from host memory.
PLDCMDERRORMASTERABORT	26	A PCI Master Abort occurred while the SiI3124 was fetching a Port Request Block (PRB) from host memory.
PLDCMDERRORPCIPERR	27	A PCI Parity Error occurred while the SiI3124 was fetching a Port Request Block (PRB) from host memory.
PSDERRORTARGETABORT	33	A PCI Target Abort occurred while data transfer was underway between the SiI3124 and host memory.
PSDERRORMASTERABORT	34	A PCI Master Abort occurred while data transfer was underway between the SiI3124 and host memory.
PSDERRORPCIPERR	35	A PCI Parity Error occurred while data transfer was underway between the SiI3124 and host memory.
SENDSERVICEERROR	36	A FIS was received while attempting to transmit a Service FIS. Following the receipt of a Set Device Bits FIS containing a service request, the device sent another FIS before allowing the host to send a Service FIS.

7.3.11 Port FIS Configuration

Address Offset: 1028_H
Access Type: Read/Write
Reset Value: 0x1000_1555

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved		FIS27cfg		FIS34cfg		FIS39cfg		FIS41cfg		FIS46cfg		FIS58cfg		FIS5Fcfg		FISA1cfg		FISA6cfg		FISB8cfg		FISBFcfg		FISC7cfg		FISD4cfg		FISD9cfg		FISOcfg	

This register contains bits for controlling Serial ATA FIS reception. For each possible FIS type, a 2-bit code defines the desired reception behavior as follows:

- 00 – Accept FIS without interlock.
- 01 – Reject FIS without interlock
- 10 – Interlock FIS. Receive FIS into slot reserved for interlocked FIS reception. If no slot has been reserved, reject the FIS.
- 11 – Reserved.

Bit[1:0] (FISOcfg) defines the 2-bit code for all other FIS types not defined by bits [29:2].
The following table defines the default behavior of FIS configuration.

Table 7-8 Default FIS Configurations

FIS Code	FIS Name	Configuration Bits		Default Action
		Signals	Default Value	
27h	Register (Host to Device)	fis27cfg[1:0]	01b	reject FIS without interlock
34h	Register (Device to Host)	fis34cfg[1:0]	00b	accept FIS without interlock
39h	DMA Activate	fis39cfg[1:0]	00b	accept FIS without interlock
41h	DMA Setup	fis41cfg[1:0]	00b	accept FIS without interlock
46h	Data	fis46cfg[1:0]	00b	accept FIS without interlock
58h	BIST Activate	fis58cfg[1:0]	00b	accept far-end retimed loopback, reject any other
5Fh	PIO Setup	fis5Fcfg[1:0]	00b	accept FIS without interlock
A1h	Set Device Bits	fisa1cfg[1:0]	00b	accept FIS without interlock
A6h	reserved	fisa6cfg[1:0]	01b	reject FIS without interlock
B8h	reserved	fisb8cfg[1:0]	01b	reject FIS without interlock
BFh	reserved	fisbFcfg[1:0]	01b	reject FIS without interlock
C7h	reserved	fisc7cfg[1:0]	01b	reject FIS without interlock
D4h	reserved	fisd4cfg[1:0]	01b	reject FIS without interlock
D9h	reserved	fisd9cfg[1:0]	01b	reject FIS without interlock
Others	reserved	fisocfg[1:0]	01b	reject FIS without interlock

7.3.12 Port PCI(X) Request FIFO Threshold

Address Offset: $102C_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved					PCI(X) Write Request Threshold								Reserved			Reserved					PCI(X) Read Request Threshold								Reserved			

This register contains threshold levels at which the PCI(X) master state machine will request the PCI(X) bus relative to the amount of data or free space in the data FIFO. The data FIFO capacity is 2Kbyte (256 Qwords). When writing to host memory (reading data from a device), the PCI(X) Write Request Threshold is compared to the amount of data in the data FIFO. When the FIFO contents exceed the threshold value, a request is issued to write the data to host memory, emptying the contents of the data FIFO. When reading host memory (writing data to a device) the PCI(X) Read Request Threshold is compared to the amount of free space in the data FIFO. When the free space exceeds the threshold value, a request is issued to read data from host memory to fill the FIFO.

- **Bit [31:27]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [26:19]:** PCI(X) Write Request Threshold (R/W). This field defines the number of Qwords that must be in the data FIFO before issuing a PCI(X) request. A value of zero will cause a request if the FIFO contains any amount of data.
- **Bit [18:16]**: Reserved (R). This bit field is reserved and returns zeros on a read. This field is defined so that the host may write a byte count value into the threshold register.
- **Bit [15:11]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [10:3]:** PCI(X) Read Request Threshold (R/W). This field defines the number of Qwords that must be available in the data FIFO before issuing a PCI(X) request. A value of zero will cause a request if the FIFO contains any free space and the DMA is active.
- **Bit [2:0]**: Reserved (R). This bit field is reserved and returns zeros on a read. This field is defined so that the host may write a byte count value into the threshold register.

7.3.13 Port 8B/10B Decode Error Counter

Address Offset: 1040_H
Access Type: Read/Write/Clear
Reset Value: 0x0000_0000

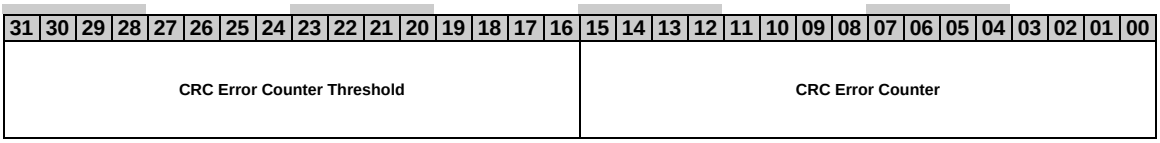
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
8B/10B Decode Error Threshold																8B/10B Decode Error Counter															

This register counts the number of 8B/10B Decode Errors that have occurred since last cleared.

- **Bit [31:16]**: 8B/10B Decode Error Threshold (R/W). This bit field defines the count at which an interrupt will be asserted. When the count in bits 15:0 is equal to this value, an 8B/10B interrupt will be latched. A threshold value of zero disables interrupt assertion and masks the corresponding interrupt status bit in the Port Interrupt Status register.
- **Bit [15:0]**: 8B/10B Decode Error Count (R/WC). This bit field represents the count of 8B/10B errors that have occurred since this register was last written. Any write to this register field will clear both the counter and the interrupt condition. Clearing the interrupt status bit will also clear the counter. The count will not overflow. Once this register reaches its maximum count, it will retain that count until cleared to zero by a write operation.

7.3.14 Port CRC Error Counter

Address Offset: 1044_H
Access Type: Read/Write/Clear
Reset Value: 0x0000_0000



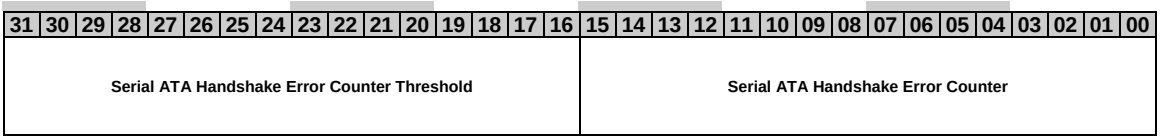
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CRC Error Counter Threshold																CRC Error Counter															

This register counts the number of Serial ATA CRC Errors that have occurred since last cleared.

- **Bit [31:16]**: Serial ATA CRC Error Threshold (R/W). This bit field defines the count at which an interrupt will be asserted. When the count in bits 15:0 is equal to this value, a serial ATA CRC interrupt will be latched. A threshold value of zero disables interrupt assertion and masks the corresponding interrupt status bit in the Port Interrupt Status register.
- **Bit [15:0]**: Serial ATA CRC Error Count (R/WC). This bit field represents the count of Serial ATA CRC errors that have occurred since this register was last written. Any write to this register will clear both the counter and the interrupt condition. Clearing the interrupt status bit will also clear the counter. The count will not overflow. Once this register reaches its maximum count, it will retain that count until cleared to zero by a write operation.

7.3.15 Port Handshake Error Counter

Address Offset: 1048_H
Access Type: Read/Write/Clear
Reset Value: 0x0000_0000



31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Serial ATA Handshake Error Counter Threshold																Serial ATA Handshake Error Counter															

This register counts the number of Serial ATA Handshake Errors that have occurred since last cleared.

- **Bit [31:16]**: Serial ATA Handshake Error Threshold (R/W). This bit field defines the count at which an interrupt will be asserted. When the count in bits 15:0 is equal to this value, a serial ATA Handshake interrupt will be latched. A threshold value of zero disables interrupt assertion and masks the corresponding interrupt status bit in the Port Interrupt Status register.
- **Bit [15:0]**: Serial ATA Handshake Error Count (R/WC). This bit field represents the count of Serial ATA Handshake errors that have occurred since this register was last written. Any write to this register will clear both the counter and the interrupt condition. Clearing the interrupt status bit will also clear the counter. The count will not overflow. Once this register reaches its maximum count, it will retain that count until cleared to zero by a write operation.

7.3.16 Port PHY Configuration

Address Offset: 1050_H
Access Type: Read/Write
Reset Value: 0x0000_020C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
PHY Status																PHY Config												Tx Amplitude			

The Port PHY Configuration register is reset by the Global Reset, not by the Port Reset. The reset value is 0x0000020C.

- **Bit[31:16]**: PHY Status (R). These bits report status of the PHY (currently always 0).
- **Bit[15:5]**: PHY Config (R/W). These bits configure the PHY. The value should not be changed as erratic operation may result.
- **Bit[4:0]**: Tx Amplitude (R/W) These bits set the nominal output swing for the Transmitter. The amplitude will be increased by 50mV by an increment of the value.

7.3.17 Port Device Status Register

Address Offset: $F80_H$ (PM Port 0)/ $F88_H$ (PM Port 1) / $F90_H$ (PM Port 2) / $F98_H$ (PM Port 3) / $FA0_H$ (PM Port 4) / $FA8_H$ (PM Port 5) / $FB0_H$ (PM Port 6) / $FB8_H$ (PM Port 7) / $FC0_H$ (PM Port 8) / $FC8_H$ (PM Port 9) / $FD0_H$ (PM Port 10) / $FD8_H$ (PM Port 11) / $FE0_H$ (PM Port 12) / $FE8_H$ (PM Port 13) / $FF0_H$ (PM Port 14) / $FF8_H$ (PM Port 15)
Access Type: Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved															service_pending	legacy_queue	native_queue	device_busy	exec_active_slot					pio_end_status							

These 16 registers contain information useful for diagnosing behavior of the execution unit. These 16 registers contain Port Multiplier device specific information. Address Offset bits 6 to 3 are the Port Multiplier Port number for the device to which the status bits apply. There is one register for each of 16 possible port multiplier ports. These registers are part of the LRAM.

- **Bit [31:17]**: Reserved
- **Bit [16]**: service_pending (R/W). Indicates that a service request has been received from this device and a SERVICE command has not yet been acknowledged.
- **Bit [15]**: legacy_queue (R/W). Indicates that one or more legacy queued commands are outstanding to this device.
- **Bit [14]**: native_queue (R/W). Indicates that one or more native queued commands are outstanding to this device.
- **Bit [13]**: device_busy (R/W). Virtual BSY bit indicating that a command has been issued to the device without receipt of a final register FIS or that a data transfer is in progress.
- **Bit [12:08]**: exec_active_slot (R/W). Contains the slot number of the last command active on this device.
- **Bit [07:00]**: pio_end_status (R/W). Contains the PIO ending status of the last PIO setup command received from this device.

7.3.18 Port Device QActive Register

Address Offset: $F84_H$ (PM Port 0)/ $F8C_H$ (PM Port 1) / $F94_H$ (PM Port 2) / $F9C_H$ (PM Port 3) / $FA4_H$ (PM Port 4) / FAC_H (PM Port 5) / $FB4_H$ (PM Port 6) / FBC_H (PM Port 7) / $FC4_H$ (PM Port 8) / FCC_H (PM Port 9) / $FD4_H$ (PM Port 10) / FDC_H (PM Port 11) / $FE4_H$ (PM Port 12) / FEC_H (PM Port 13) / $FF4_H$ (PM Port 14) / FFC_H (PM Port 15)
Access Type: Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
QActive[31:0]																															

These 16 registers contain Port Multiplier device specific status indicating outstanding queued commands in the device. For each bit set to one, a queued command, legacy or native, is outstanding associated with the slot number corresponding to the bit position. There is one register for each of 16 possible port multiplier ports. Address Offset bits 6 to 3 are the Port Multiplier Port number for the device to which the status bits apply.

- **Bit [31:00]**: Each bit corresponds to a slot number that contains an active outstanding legacy or native queued command.

7.3.19 Port Context Register

Address Offset: $1E04_H$
Access Type: Read

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																							PM Port				Slot				

- **Bit [31:09]**: Reserved
- **Bit [08:05]**: PM Port (R). This field contains the Port Multiplier port number corresponding to the last FIS transferred (transmit or receive). Upon a processing halt due to a device specific error, this field contains the PM port corresponding to the device that returned error status.
- **Bit [04:00]**: Slot (R). This field contains the slot number of the last command processed by the execution unit. Note that this slot number does not necessarily correspond to the command in error during error halt conditions. For native queue error recovery, the command slot in error must be determined by issuing a READ LOG EXTENDED to the device to determine the tag number of the command in error.

7.3.20 SControl

Address Offset: $1F00_H$
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved												PMP				SPM				IPM				SPD				DET			

This register is the SControl register as defined by the Serial ATA specification (section 10.1.3).

- **Bit [31:16]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [19:16]**: PMP (R/W). This field identifies the currently selected Port Multiplier port for accessing the SActive register and some bit fields of the Diagnostic registers.
- **Bit [15:12]**: SPM (R/W). This field selects a power management state. A non-zero value written to this field causes initiation of the select power management state. This field self-resets to 0 as soon as action begins to initiate the power management state transition.

Value	Definition
0000	No power management state transition requested
0001	Transition to the Partial power management state initiated
0010	Transition to the Slumber power management state initiated
0100	Transition from a power management state initiated (ComWake asserted)
others	Reserved

- **Bit [11:08]**: IPM (R/W) – This field identifies the interface power management states that may be invoked via the Serial ATA interface power management capabilities.

Value	Definition
0000	No interface power management restrictions (Partial and Slumber modes enabled)
0001	Transitions to the Partial power management state are disabled
0010	Transitions to the Slumber power management state are disabled
0011	Transitions to both the Partial and Slumber power management states are disabled
others	Reserved

- **Bit [07:04]**: SPD (R/W) – This field identifies the highest allowed communication speed the interface is allowed to negotiate.

Value	Definition
0000	No restrictions (default value)
0001	Limit to Generation 1 (1.5 Gb/s)
0010	Limit to Generation 2 (3.0 Gb/s)
others	Reserved

- **Bit [03:00]**: DET (R/W) – This field controls host adapter device detection and interface initialization.

Value	Action
0000	No action
0001	COMRESET is periodically generated until another value is written to the field
0100	No action
Others	Reserved, no action

7.3.21 SStatus

Address Offset: $1F04_H$
Access Type: Read
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																				IPM				SPD				DET			

This register is the SStatus register as defined by the Serial ATA specification (section 10.1.1).

- **Bit [31:12]**: Reserved (R). This bit field is reserved and returns zeros on a read.
- **Bit [11:08]**: IPM (R) – This field identifies the current interface power management state.

Value	Definition
0000	Device not present or communication not established
0001	Interface in active state
0010	Interface in Partial power management state
0110	Interface in Slumber power management state
Others	Reserved

- **Bit [07:04]**: SPD (R) – This field identifies the negotiated interface communication speed.

Value	Definition
0000	No negotiated speed
0001	Generation 1 communication rate (1.5 Gb/s)
0010	Generation 2 communication rate (3.0 Gb/s)
Others	Reserved

- **Bit [03:00]**: DET (R) – This field indicates the interface device detection and PHY state.

Value	Action
0000	No device detected and PHY communication not established
0001	Device presence detected but PHY communication not established
0011	Device presence detected and PHY communication established
0100	PHY in offline mode as a result of the interface being disabled or running in a BIST loopback mode
Others	Reserved, no action

7.3.22 SError

Address Offset: $1F08_H$
Access Type: Read/Write 1 Clear
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
R	R	R	R	R	**X**	**F**	**T**	**S**	**H**	**C**	**D**	**B**	**W**	**I**	**N**	R	R	R	R	**E**	**P**	**C**	**T**	R	R	R	R	R	R	**M**	**I**
DIAG																**ERR**															

This register is the SError register as defined by the Serial ATA specification (section 10.1.2).

- **Bit [31:16]**: DIAG (R/W1C) – This field contains bits defined as shown in the following table. Writing a 1 to the register bit clears the B, C, F, N, H, W, and X bits. Writing a 1 to the corresponding bits in the Port Interrupt Status register also clears the F, N, W, and X bits. The B, C, and H bits operate independently of the corresponding error counter registers; if the error counters are used, these bits should be ignored.

Bit	Definition	Description
B	10b to 8b decode error	Latched decode error or disparity error from the Serial ATA PHY
C	CRC error	Latched CRC error from the Serial ATA PHY
D	Disparity error	N/A, always 0; this error condition is combined with the decode error and reported as B error
F	Unrecognized FIS type	Latched Unrecognized FIS error from the Serial ATA Link
I	PHY Internal error	N/A, always 0
N	PHYRDY change	Indicates a change in the status of the Serial ATA PHY
H	Handshake error	Latched Handshake error from the Serial ATA PHY
R	Reserved	Always 0
S	Link Sequence error	N/A, always 0
T	Transport state transition error	N/A, always 0
W	ComWake	Latched ComWake status from the Serial ATA PHY
X	Device Exchanged	Latched ComInit status from the Serial ATA PHY

Table 7-9 SError Register Bits (DIAG Field)

- **Bit [15:00]**: ERR – This field is not implemented; all bits are always 0.

7.3.23 SActive

Address Offset: $1F0C_H$
Access Type: Read/Write
Reset Value: N/A

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Active bits																															

This register provides indirect access of the Port Device QActive registers (see section 7.3.18 for description). It contains the Active bits used to determine the activity of native queued commands for the selected Port Multiplier port (selection in SControl). A one in any bit position indicates that the corresponding command is still active in the device.

7.4 Internal Register Space – Base Address 2

These registers are 32-bits wide and provide Indirect Register Access to the registers of the SiI3124. Access to this register space is through the PCI I/O space.

Address Offset	Register Name
00_H	Global Register Offset
04_H	Global Register Data
08_H	Port Register Offset
$0C_H$	Port Register Data

Table 7-10 SiI3124 Internal Register Space – Base Address 2

7.4.1 Global Register Offset

Address Offset: 00_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																									Dword Offset					00	

This register provides indirect addressing of a Global Register otherwise accessible directly via Base Address Register 0. The Dword address offset for an indirect access is in bits 6 to 2; bits 31 to 7, 1, and 0 are reserved and should always be 0.

7.4.2 Global Register Data

Address Offset: 04_H
Access Type: Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
As defined for indirectly accessed register																															

This register provides the indirect access addressed by the Global Register Offset register.

7.4.3 Port Register Offset

Address Offset: 08_H
Access Type: Read/Write
Reset Value: 0x0000_0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
Reserved																Dword Offset														00	

This register provides indirect addressing of a Port Register otherwise accessible directly via Base Address Register 1. The Dword address offset for an indirect access is in bits 14 to 2; bits 31 to 15, 1, and 0 are reserved and should always be 0.

7.4.4 Port Register Data

Address Offset: $0C_H$
Access Type: Read/Write

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
As defined for indirectly accessed register																															

This register provides the indirect access addressed by the Port Register Offset register.

8 Power Management

The following register bits control Power Management in a SiI3124 Port.

Register	Bits	Description
Interrupt Status	PM Change Bit 3	This bit reports a change in the Power Management mode. It corresponds to the interrupt enabled by bit 3 of the Port Interrupt Enable register.
SError	W Bit 18	This bit reports a ComWake received from the Serial ATA bus. It corresponds to the interrupt enabled by bit 5 of the Port Interrupt Enable register.
Interrupt Status	ComWake Bit 5	
SControl	SPM Bits 15-12	This bit field initiates transitions to/from Partial or Slumber power management states; bit 14 corresponds to ComWake (exit power management); bit 13 corresponds to Slumber mode; bit 12 corresponds to Partial mode.
SControl	IPM Bits 11-8	This bit field disables transitions to Partial or Slumber power management states; bit 9 corresponds to Slumber mode; bit 8 corresponds to Partial mode.
SStatus	IPM Bits 11-8	This bit field reports the power management state; '0110' corresponds to Slumber mode; '0010' corresponds to Partial mode.

Table 8-1 Power Management Register Bits

There are two power management modes: Partial and Slumber. These power management modes may be software initiated through the SControl register or device initiated from the Serial ATA device.

Transitions to and from either power management mode generate an interrupt, the Power Management Mode Change Interrupt, which may be masked in the Port Interrupt Enable register (bit 3).

Partial/Slumber mode may be initiated by software through the SControl register. By setting the SPM field to either '0001' (Partial) or '0010' (Slumber), software causes a PMREQ to the Serial ATA device, which will respond with either a PMACK or PMNAK. If a PMACK is received the Partial/Slumber mode is entered. A PMNAK is ignored; the request remains asserted.

The Serial ATA device may initiate Partial/Slumber mode. Software enables the acknowledgement of this request by setting the IPM field in the SControl register to '0001' (Partial), '0010' (Slumber), or '0011' (Partial or Slumber). If enabled, a PMACK will be sent to the device; if not enabled, a PMNAK will be sent. When the request is received and its acknowledgement is enabled, Partial/Slumber mode is entered.

Partial/Slumber mode status is reported in the SStatus register ('0010'/'0110' in the IPM field).

Partial/Slumber mode is cleared by ComWake (asserted when the SPM field is set to '0100').

9 Flash, GPIO, EEPROM, and I²C Programming

9.1 Flash Memory Access

The SiI3124 supports an external Flash memory device of up to 4 Mbits (512 Kbytes) in capacity. Access to the Flash memory is available using either PCI Direct Access or Register Access.

9.1.1 PCI Direct Access

Access to the Expansion Rom is enabled by setting bit 0 in the Expansion Rom Base Address register at Offset 30h of the PCI Configuration Space. When this bit is set, bits [31:19] of the same register are programmable by the system to set the base address for all Flash memory accesses. Read and write operations with the Flash memory are initiated by Memory Read and Memory Write commands on the PCI bus. Accesses may be as Bytes, Words, or DWords.

9.1.2 Register Access

This type of Flash memory access is carried out through a sequence of internal register read and write operations. The proper programming sequences are detailed below.

9.1.2.1 Flash Write Operation

Verify that Flash Address register bit 25 (Mem Access Start) is zero. The bit is one when a memory access is in progress. It is zero when the memory access is complete and ready for another operation.

Program the write address for the Flash memory access. The address field is bits [18:0] in the Flash Address register.

Program the write data for the Flash memory access. The data field is bits [7:0] in the Flash Memory Data register.

Program Flash Address register bit 24 (Mem Access Type) to zero for a memory write.

Initiate the Flash memory access by setting bit 25 in the Flash Address register.

9.1.2.2 Flash Read Operation

Verify that Flash Address register bit 25 (Mem Access Start) is zero. The bit is one when a memory access is in progress. It is zero when the memory access is complete and ready for another operation.

Program the read address for the Flash memory access. The address field is bits [18:0] in the Flash Address register.

Program Flash Address register bit 24 (Mem Access Type) to one for a memory read.

Initiate the Flash memory access by setting bit 25 in the Flash Address register.

Verify that Flash Address register bit 25 (Mem Access Start) is clear. The bit is one when a memory access is in progress. It is zero when the memory access is complete.

Read the data from bits [7:0] in the Flash Memory Data register.

9.2 I²C Operation

The SiI3124 provides a Multimaster I²C interface. For Auto-initialization of some PCI Configuration registers an external 256-byte EEPROM memory device may be connected to this I²C interface (see section 6). Two registers are provided for programmed read/write access to the I²C interface: the I²C Address register and the I²C Data/Control register.

9.2.1.1 I²C Write Operation

Verify that I²C Data/Control register bit 31 (I²C Access Start) is zero. The bit is one when an access is in progress. It is zero when the access is complete and another operation may be started.

Write '1' to clear bit 28 in the I²C Data/Control register. This bit is set if an error occurred during a previous access.

Program the write address for the access in the I²C Address register.

Program the write data for the access in the I²C Data/Control register (bits 7:0).

Write zero to bit 24 (I²C Access Type) in the I²C Address register.

Initiate the I²C write by setting bit 31 (I²C Access Start) in the I²C Data/Control register.

Poll bit 31 in the I²C Data/Control register. The bit is one while an access is in progress. It becomes zero when the access completes. (Alternatively, the I²C Interrupt may be enabled. See the Global Control register and Global Interrupt Status register descriptions on page 61.)

Check bit 28 in the I²C Data/Control register. The bit is set if an error occurred during the access.

9.2.1.2 I²C Read Operation

Verify that I²C Data/Control register bit 31 (I²C Access Start) is zero. The bit is one when an access is in progress. It is zero when the access is complete and another operation may be started.

Write '1' to clear bit 28 in the I²C Data/Control register. The bit is set if an error occurred during a previous access.

Program the read address for the access in the I²C Address register.

Write one to bit 24 (I²C Access Type) in the I²C Address register.

Initiate the I²C read by setting bit 31 (I²C Access Start) in the I²C Data/Control register.

Poll bit 31 in the I²C Data/Control register. The bit is one while an access is in progress. It becomes zero when the access completes. (Alternatively, the I²C Interrupt may be enabled. See the Global Control register and Global Interrupt Status register descriptions on page 61.)

Check bit 28 in the I²C Data/Control register. The bit is set if an error occurred during the access.

Read the data from bits 7:0 in the I²C Data/Control register.

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