SONY

CXA1124BS/BQ
CXA1534S/Q

US Audio Multiplexing Decoder IC

Description

CXA1124/CXA1534 is an IC designed for the MTS decoding systems. This device contains a stereo signal demodulator, a SAP (Second Audio Program) signal demodulator and a dbx-TV noise reduction decoder, The Main 100% reference input level of the CXA1124 (CXA1534) is 245mVrms (100mVrms).

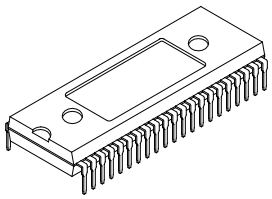
Features

- All functions of the MTS decoding system included on a chip
- Minimized external components using integrated active filtering technique
- Reduced adjustment points using optimized filter characteristics, a quasi-sine wave stereo demodulator and a SAP demodulator
- Has a sub output which allows independent setting of a mode
- Allows automatic changeover between ON and OFF in the SAP mode when SAP broadcasting is OFF
- Adjustment-free pilot cancel circuit
- Wide operating voltage range (4.7 to 10V)

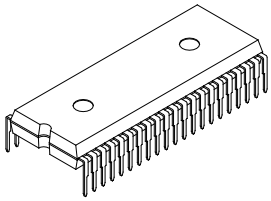
Structure

Bipolar silicon monolithic IC

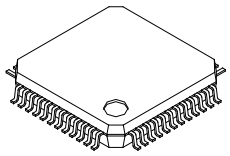
CXA1124BS/CXA1534S
42 pin SDIP (Plastic)



CXA1124BS
42 pin SDIP (Plastic)



CXA1124BQ/CXA1534Q
48 pin QFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{CC}	12	V
• LED drive current	I_O	25 (max.)	mA
• Allowable power dissipation	P_D	2200 (42pin SDIP)	mW
		600 (48pin QFP)	mW
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–55 to +150	°C

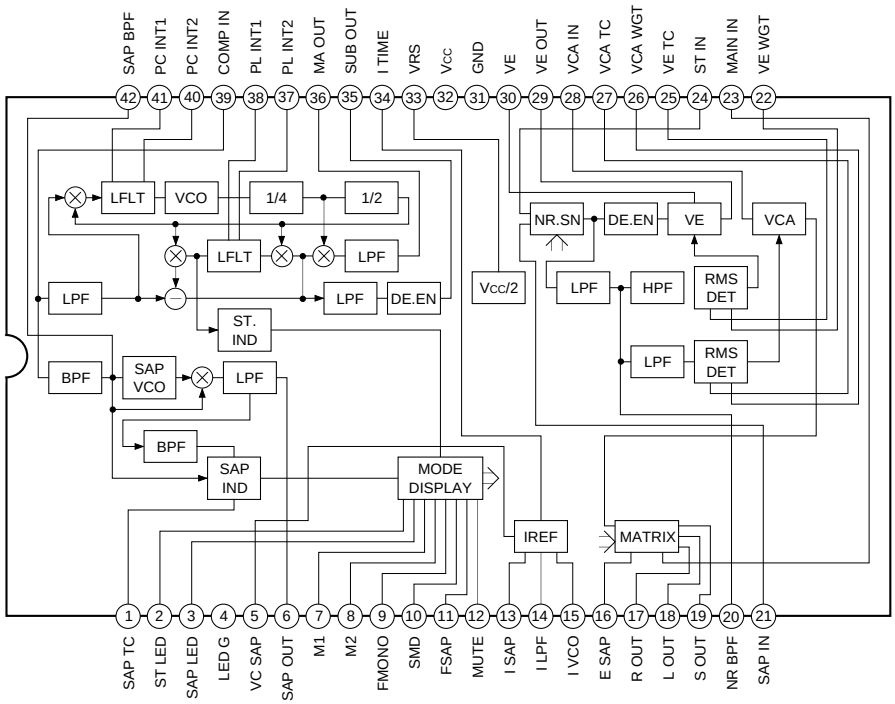
Operating Conditions

Supply voltage	V_{CC}	4.7 to 10.0	V

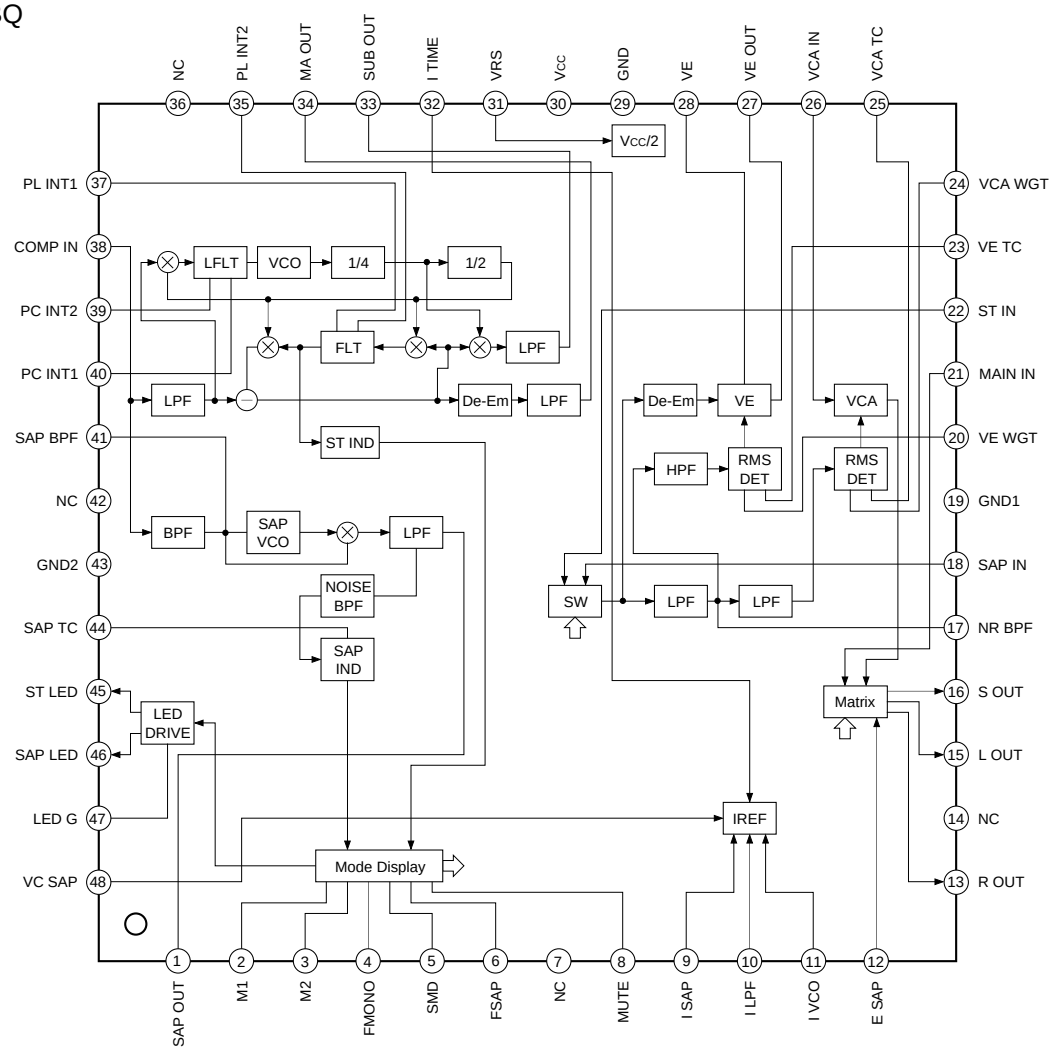
E91402C79

Block Diagram and Pin Configuration

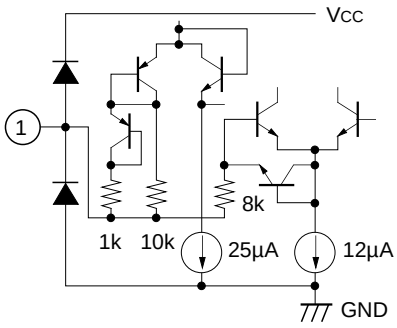
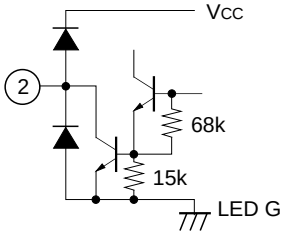
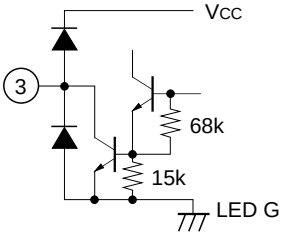
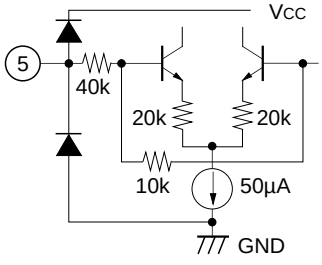
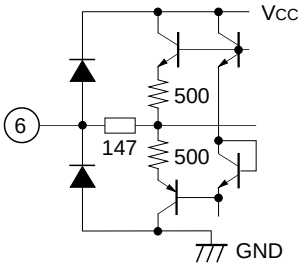
CXA1124BS

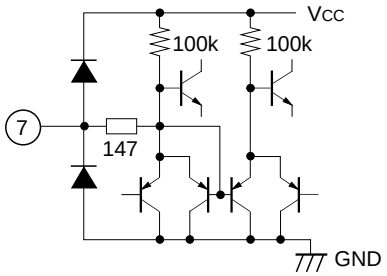
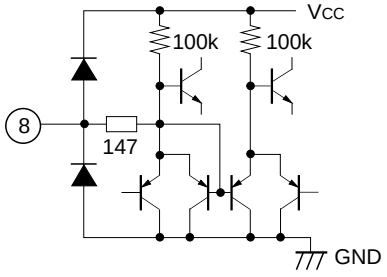
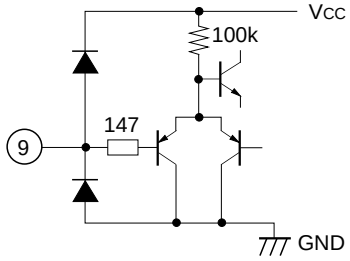
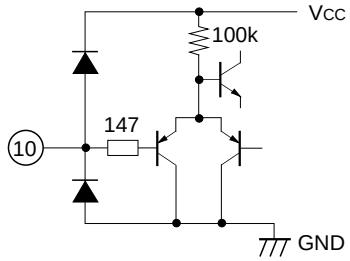
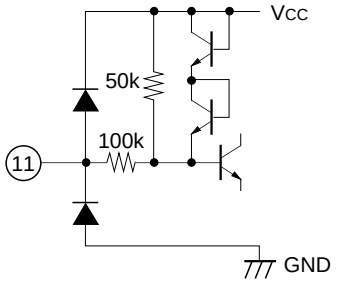


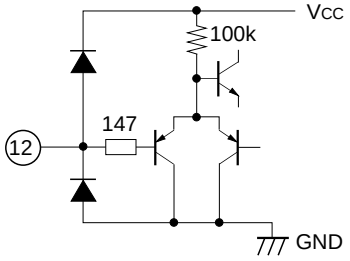
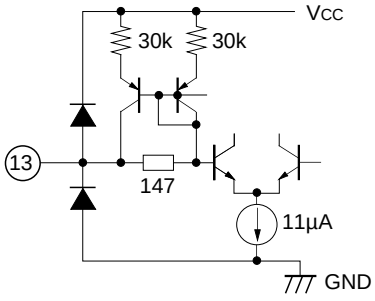
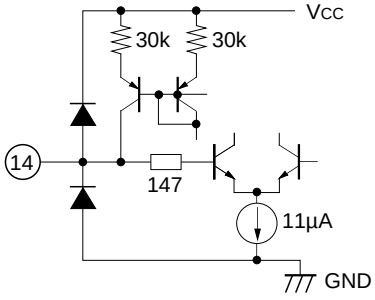
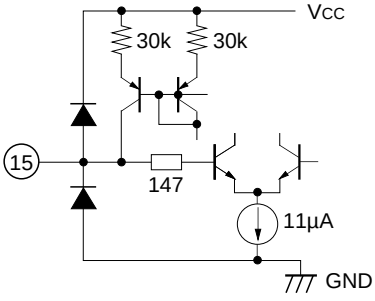
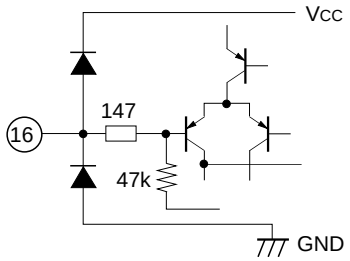
CXA1124BQ

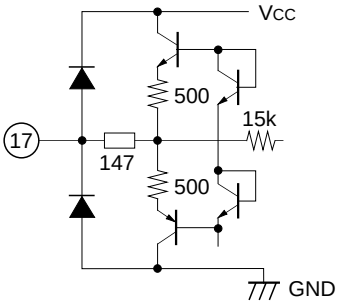
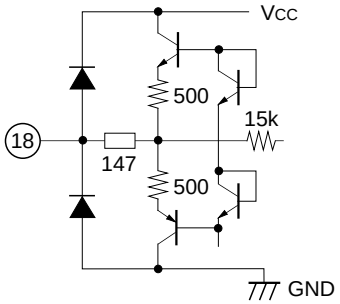
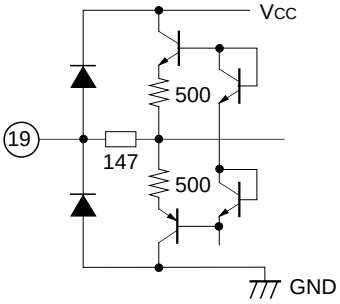
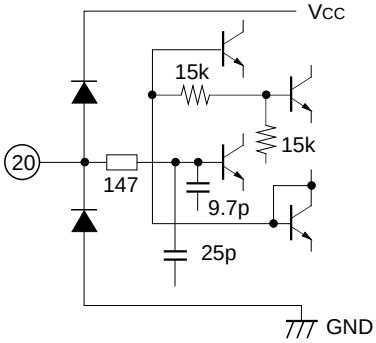
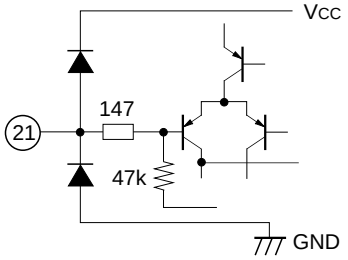


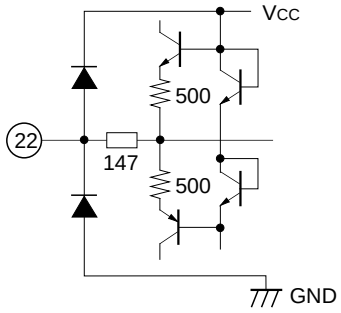
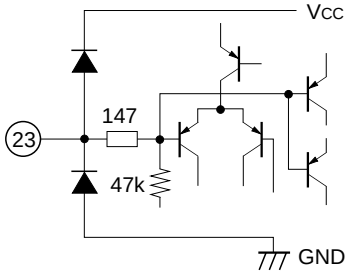
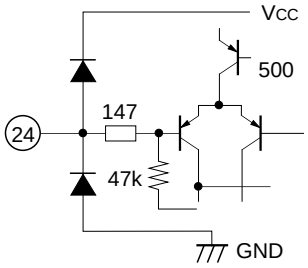
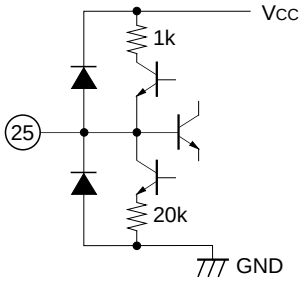
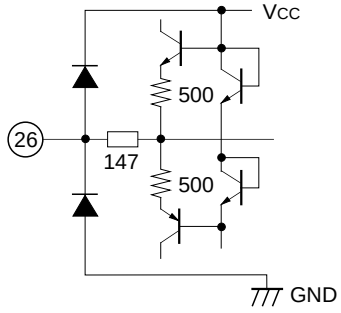
Pin Description and Equivalent Circuit (Ta = 25°C, V_{CC} = 9V)

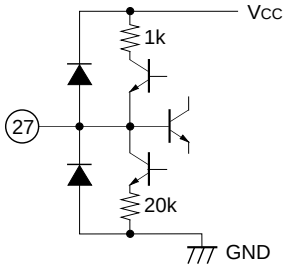
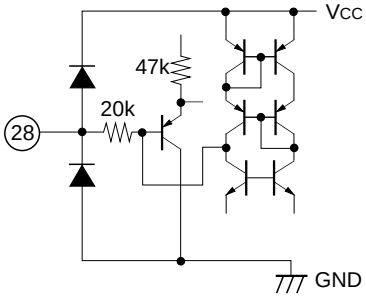
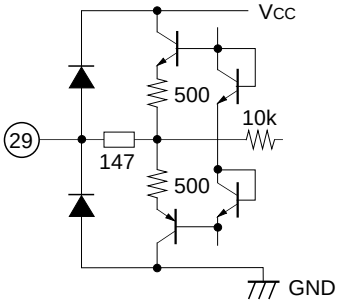
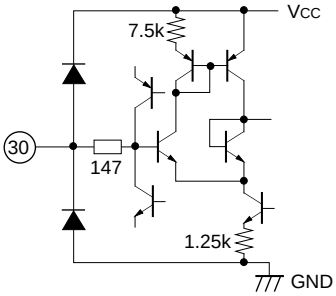
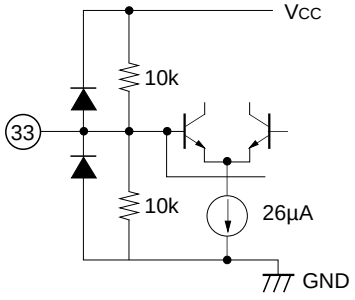
Pin No. SDIP	Pin No. QFP	Symbol	Voltage (Typ.)	Equivalent circuit	Description
1	44	SAP TC	3.4V		Sets the time constant of the SAP carrier detection circuit.
2	45	ST LED	0.2V		Drives LED when stereo broadcasting is on. Open collector output.
3	46	SAP LED	0.2V		Drives LED when SAP broadcasting is on.
4	47	LED G			GND of LED.
5	48	VC SAP	4.5V		Control pin of SAP VCO oscillation frequency. SAP VCO oscillating frequency can be varied by applying DC voltage to this pin. Normally a resistance or a variable resistance is connected.
6	1	SAP OUT	4.5V		Output pin of SAP FM detector.

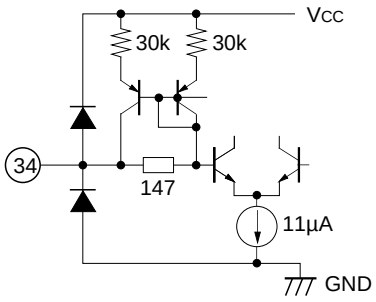
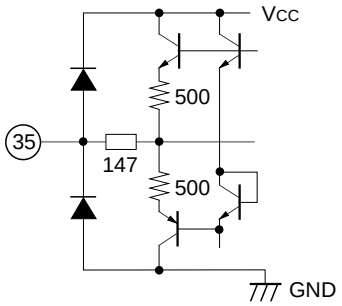
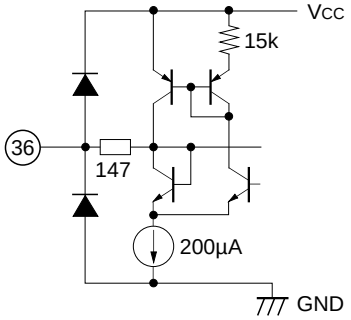
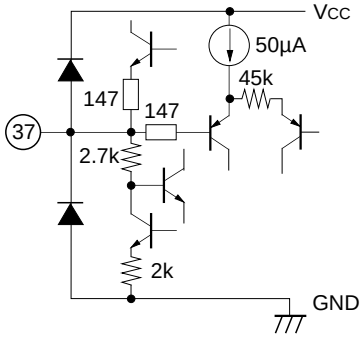
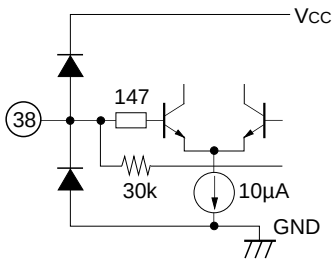
Pin No.		Symbol	Voltage (Typ.)	Equivalent circuit	Description
SDIP	QFP				
7	2	M1	L: GND to 0.8V H: 2.0V to Vcc		Mode control switch pin. This pin is used in conjunction with M2 of Pin 8.
8	3	M2	L: GND to 0.8V H: 2.0V to Vcc		Mode control switch pin. This pin is used in conjunction with M1 of pin 7.
9	4	FMONO	L: GND to 0.8V M: 2.0V to Vcc – 2.0 H: Vcc – 0.5 to Vcc		Mode control switch pin. Has 3 ranges of input, sets forced monoral mode and also controls ST.LED.
10	5	SMD	L: GND to 0.8V H: 2.0V to Vcc		Mode control switch pin. Controls SOUT pin output.
11	6	FSAP	L: GND H: Vcc		Mode control switch pin. This pin's control voltage is different from that of other mode control switch pins.

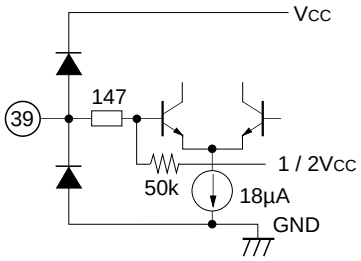
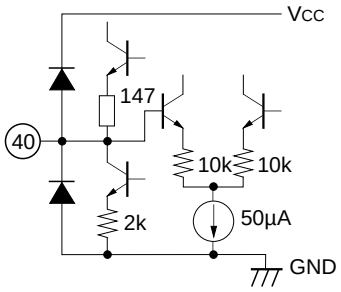
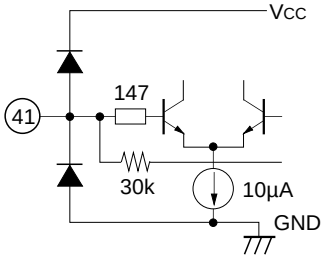
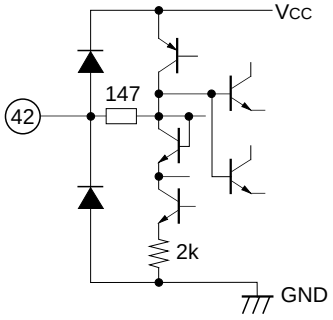
Pin No.		Symbol	Voltage (Typ.)	Equivalent circuit	Description
SDIP	QFP				
12	8	MUTE	L: GND to 0.8V H: 2.0V to Vcc		Mode control switch pin. By setting this pin to H level all outputs turn to mute.
13	9	I SAP	1.3V		Sets the reference current of SAP filters. By adjusting the current that flows into this pin the cut off frequency can be changed.
14	10	I LPF	1.3V		Sets the reference current of stereo and dbx-TV NR filters. By adjusting the current that flows into this pin the respective cut off frequency can be changed.
15	11	I VCO	1.3V		Sets the reference current of stereo VCO and SAP VCO. By adjusting the current that flows into this pin the respective oscillation frequency can be changed.
16	12	E SAP	4.5V		Inputs SAP signal from the external dbx-TV NR (option).

Pin No.		Symbol	Voltage (Typ.)	Equivalent circuit	Description
SDIP	QFP				
17	13	R OUT	4.5V		Rch output pin.
18	15	L OUT	4.5V		Lch output pin.
19	16	S OUT	4.5V		Optional output pin. From this pin monaural or SAP (only when the external dbx-TV NR is connected) is output.
20	17	NR BPF	4.5V		Pin for the filter monitor of dbx-TV block.
21	18	SAP IN	4.5V		Inputs the signal from SAP OUT of pin 6.

Pin No.		Symbol	Voltage (Typ.)	Equivalent circuit	Description
SDIP	QFP				
22	20	VE WGT	4.5V		Weighting pin of the variable de-emphasis control RMS value detection circuit.
23	21	MAIN IN	4.5V		Inputs (L + R) signal from MAIN OUT of pin 36.
24	22	ST IN	4.5V		Inputs (L – R) signal from SUB OUT of pin 35.
25	23	VE TC	2V		Determines the recovery time constant of the variable de-emphasis control RMS value detection circuit. By connecting a 3.3µF capacitance, normal recovery time constant can be obtained.
26	24	VCA WGT	4.5V		Weighting pin of VCA control RMS value detection circuit.

Pin No.		Symbol	Voltage (Typ.)	Equivalent circuit	Description
SDIP	QFP				
27	25	VCA TC	2V		Determines the recovery time constant of VCA control RMS value detection circuit. By connecting a 10µF capacitance, normal recovery time constant can be obtained.
28	26	VCA IN	4.5V		VCA input pin. Through a coupling capacitor, input the variable de-emphasis output signal of pin 29.
29	27	VE OUT	4.5V		Variable de-emphasis output pin.
30	28	VE	4.5V		Variable de-emphasis integral pin.
31	29	GND			
—	19	GND1			GND
—	43	GND2			GND
32	30	Vcc			
33	31	VRS	4.5V		Reference potential pin of the signal. Voltage becomes half that of the supply voltage.

Pin No.		Symbol	Voltage (Typ.)	Equivalent circuit	Description
SDIP	QFP				
34	32	I TIME	1.3V		Input pin for the timing current of the RMS value detection. The timing current determines the normal time constant of the detection circuit and the variable de-emphasis characteristics.
35	33	SUB OUT	4.5V		Output pin of L – R signal.
36	34	MA OUT	4.5V		Output pin of L + R signal.
37	35	PL INT2	For stereo: 5.5V For monaural: 3.5V		Integral pin of the pilot cancel circuit loop filter.
38	37	PL INT1	4.5V		

Pin No.		Symbol	Voltage (Typ.)	Equivalent circuit	Description
SDIP	QFP				
39	38	COMP IN	4.5V		Audio multiplex signals are input through this pin.
40	39	PC INT2	4.5V		Integral pin of the stereo block PLL loop filter.
41	40	PC INT1	4.5V		
42	41	SAP BPF	4.5V		SAP BPF monitor pin.

Electrical Characteristics

(Unless otherwise specified, Ta = 25°C, V_{CC} = 9V, 0dB = 100% modulation level, FH = 15.734kHz)
100% modulation level → Main (L + R) level = –10dBm (245mVrms) (Pre-Emphasis On)
(Reference level) Sub (L – R) level = –4dBm (490mVrms) (dbx-TV OFF)
Pilot level = –24.0dBm (49mVrms)
SAP level = –14.4dBm (147mVrms) (10kHz peak deviation, dbx-TV OFF)

The reference input levels of the CXA1534 (at Pin 39) are 1/2.45 times the equivalent values at the head of this page. The Main level is 100mVrms.

Stereo section (Including operation supply voltage and consumption circuit)

No.	Item	Symbol	Condition				Min.	Typ.	Max.	Unit
			Mode	Input	Output	Others				
1	Operating supply voltage	V_{CC}	—	—	—	No signal	4.7		10.0	V
2	Consumption current	I_{CC}	ST.	—	—	No signal	17	25	33.0	mA
3	Main output level	Vmain	ST.	Pin 39	Pin 17 Pin 18	Main 1kHz, 0dB, 75µs, pre-emphasis ON	–5.0	–4.0	–3.0	dBm
4	De-emphasis frequency response	FCdeem	ST.	Pin 39	Pin 17 Pin 18	Main 5kHz, –10dB, 75µs, pre-emphasis ON	–1.0	0	1.0	dB
5	Main LPF frequency response	FCmain	ST.	Pin 39	Pin 17 Pin 18	Main 12kHz, –20dB, 75µs, pre-emphasis ON	–3.0	–1.0	1.0	dB
6	Main distortion ratio	THDm	ST.	Pin 39	Pin 17 Pin 18	Main 1kHz, 0dB, 75µs, pre-emphasis ON 15kHz LPF used	—	0.1	0.5	%
7	Main Max. output level	Vmmax	ST.	Pin 39	Pin 17 Pin 18	Main 1kHz, THD = 3%, 75µs, pre-emphasis ON	2.0	9.0	—	dBm
8	Main noise	Vnmain	ST.	—	Pin 17 Pin 18	No signal 15kHz LPF used	—	–73	–65	dBm
9	Sub output level	Vsub	—	Pin 39	Pin 35	Sub 1kHz, 0dB	–10.5	–9.0	–5.5	dBm
10	Sub LPF frequency response	FCsub	—	Pin 39	Pin 35	Sub 12kHz, –10dB	–3.0	–0.4	1.0	dB
11	Sub distortion ratio	THDsub	—	Pin 39	Pin 35	Sub 1kHz, 0dB, 15kHz LPF used	—	0.1	1.0	%
12	Sub Max. output level	Vsmax	—	Pin 39	Pin 35	Sub 1kHz, THD = 3%	–2.0	6.0		dBm
13	Sub noise level	Vsubn	—	—	Pin 35	No signal 15kHz LPF used	—	–75	–65	dBm
14	Sub pilot cancel	PCsub	—	Pin 39	Pin 35	Pilot: fH (–24dBm) fH BPF used	—	–53	–40	dBm
15	Stereo On level	THst	—	Pin 39	—	Varies Pilot input. Tests the level where LED lights up. Turns Pin 9 (FMONO) to L or M.	–9.5	–6.5	–4.0	dB

SAP section

No.	Item	Symbol	Condition				Min.	Typ.	Max.	Unit
			Mode	Input	Output	Others				
16	SAP output level	Vsap	—	Pin 39	Pin 6	1kHz, 0dB	–10.5	–9.4	–7.5	dBm
17	SAP frequency characteristics	FCsap	—	Pin 39	Pin 6	10kHz, –10dB	–3.0	–0.6	+2.0	dB
18	SAP distortion ratio	THDsap	—	Pin 39	Pin 6	1kHz, 0dB, 15kHz LPF used	—	2.5	6.0	%
19	SAP noise level	VNsap	—	Pin 39	Pin 6	Input 5fH (–14.4dBm) 15kHz LPF used	—	–65	–40	dBm
20	SAP ON level	THsap	—	Pin 39		Varies SAP carrier (no demodulation) input level. Tests level where Pin 3 LED lights up.	–14.0	–10.0	–7.0	dB

dbx-TV section

Note) To test the dbx-TV timing current of other than pin 34 input pilot to COMP IN (Pin 39) and turn it to ST mode. Also, turn MAIN IN (Pin 23) open.

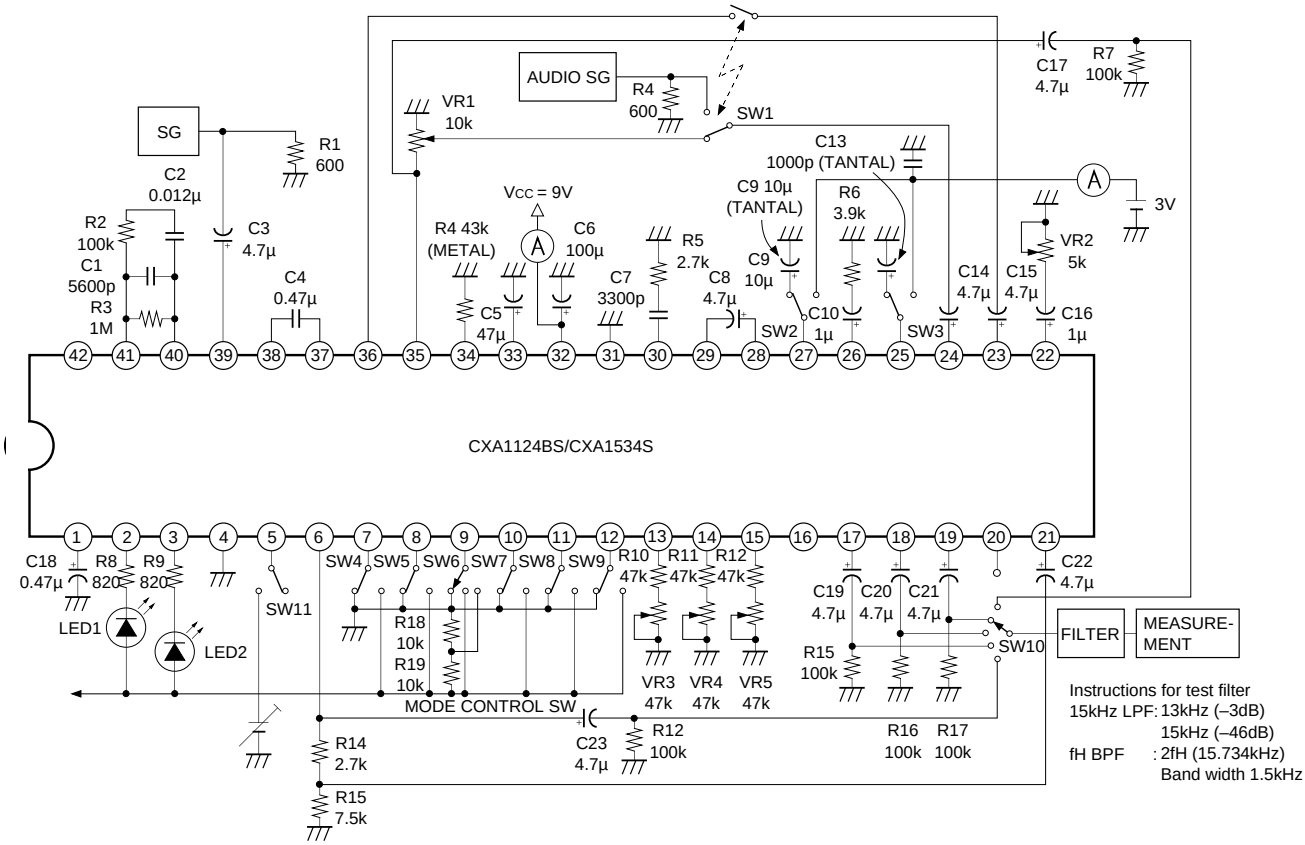
No.	Item	Symbol	Condition				Min.	Typ.	Max.	Unit
			Mode	Input	Output	Others				
21	dbx-TV decode characteristics 300Hz, –5dB	Vdc-1	ST.	Pin 24	Pin 17 Pin 18	300Hz, –17dBm	1.5	3.0	4.5	dBm
22	dbx-TV decode characteristics 300Hz, –15dB	Vdc-2	ST.	Pin 24	Pin 17 Pin 18	300Hz, –27dBm	–18.5	–17.0	–15.5	dBm
23	dbx-TV decode characteristics 300Hz, –30dB	Vdc-3	ST.	Pin 24	Pin 17 Pin 18	300Hz, –42dBm	–48.5	–47.0	–45.5	dBm
24	dbx-TV decode characteristics 1kHz, 0dB	Vdc-4	ST.	Pin 24	Pin 17 Pin 18	1kHz, –12dBm	–2.7	–0.7	+1.3	dBm
25	dbx-TV decode characteristics 1kHz, –10dB	Vdc-5	ST.	Pin 24	Pin 17 Pin 18	1kHz, –22dBm	–23.4	–21.4	–19.4	dBm
26	dbx-TV decode characteristics 1kHz, –20dB	Vdc-6	ST.	Pin 24	Pin 17 Pin 18	1kHz, –32dBm	–43.6	–41.6	–39.6	dBm
27	dbx-TV decode characteristics 8kHz, 0dB	Vdc-7	ST.	Pin 24	Pin 17 Pin 18	8kHz, –12dBm	–8.3	–5.8	–3.3	dBm

No.	Item	Symbol	Condition				Min.	Typ.	Max.	Unit
			Mode	Input	Output	Others				
28	dbx-TV decode characteristics 8kHz, –10dB	Vdc-8	ST.	Pin 24	Pin 17 Pin 18	8kHz, –22dBm	–34.9	–32.4	–29.9	dBm
29	dbx-TV decode characteristics 8kHz, –15dB	Vdc-9	ST.	Pin 24	Pin 17 Pin 18	8kHz, –27dBm	–49.2	–46.7	–44.2	dBm
30	dbx-TV distortion ratio	THDnr	ST.	Pin 24	Pin 17 Pin 18	1kHz, –15dBm	—	0.3	0.8	%
31	dbx-TV Max. output level 300Hz	Vnrmax L	ST.	Pin 24	Pin 17 Pin 18	THD = 3%	2.0	9.0	—	dBm
32	dbx-TV Max. output level 8kHz	Vnrmax H	ST.	Pin 24	Pin 17 Pin 18	THD = 3%	2.0	8.0	—	dBm
33	dbx-TV Noise level	Vnnr	ST.	—	Pin 17 Pin 18	15kHz LPF used	—	–88	–80	dBm
34	dbx-TV Timing current	Itime	—	—	—	Applies 3V voltage to pins 25 and 27 and tests respective input current	7.1	7.5	7.9	µA

Mode Matrix Control Voltage section

No.	Item	Symbol	Condition				Min.	Typ.	Max.	Unit
			Mode	Input	Output	Others				
35	Control voltage 1 H level	V-HC1	—	—	—	Pin 7, 8, 10, 12	2.0		V_{CC}	V
36	Control voltage 1 L level	V-LC1	—	—	—		GND		0.8	V
37	Control voltage 2 H level	V-HC2	—	—	—	Control voltage for pin 9 (FMONO) only	V_{CC} – 0.5	—	V_{CC}	V
38	Control voltage 2 M level	V-MC2	—	—	—		2.0	—	V_{CC} – 2.0	V
39	Control voltage 2 L level	V-LC2	—	—	—		GND		0.8	V

Electrical Characteristics Test Circuit



Adjustment Procedure

(1) Adjustment of stereo and dbx filters

Input 1.5fH (23.6kHz: –10dBm) sine wave to pin 39 (COMP IN) and monitor pin 36 (MAIN OUT). Adjust the variable resistor of pin 14 (I LPF) to reduce the output to a minimum.

(2) Adjustment of SAP filter

Input 6.2fH (97.55kHz: –14.4dBm) sine wave to pin 39 and monitor pin 42 (SAP BPF). Adjust the variable resistor of pin (I SAP) to reduce the output to a minimum.

(3) VCO adjustment

Adjust pin 15 (I VCO) volume so as to obtain an identical value whether Pin 40 (PC INT2) DC value has input pilot (fH = 15.734kHz: –24dBm) or not.

Note) At this point, check to see that the ST.LED of pin 2 is ON.
If the LED is OFF, turn up the variable resistor until the ST.LED lights up.

(4) Adjustment of stereo seperation

1. Create the stereo mode (by causing the 1 pin (pin 7) to be H and the M2 pin (pin 8) to be L) and input Lch-only signal (30% modulation depth and 300Hz frequency) to pin 39. Then adjust the variable resistor of pin 35 (SUB OUT) to reduce the Rch output to a minimum.
2. Then change only the frequency of the input signal to 3kHz and adjust the variable resistor of pin 22 (VE WGT) to reduce the Rch output to a minimum.
3. Repeat Steps 1 and 2 described above until an optimum separation is achieved.
   The adjustment frequency is a combination of either 300Hz and 3kHz or 400Hz and 2kHz.

Mode Matrix No.1

* FSAP → GND (SAP discrimination Automatic select mode)

Broadcast Mode	LED		Pin				Output	
	ST.	SAP	M1	M2	FMONO	FSAP*	LOUT	ROUT
MONO	OFF	OFF	L	L	—	GND	L + R	L + R
			L	H	—		L + R	L + R
			H	L	—		L + R	L + R
	↓	↓	H	H	—	↓	MUTE	MUTE
MONO + SAP	OFF	ON	L	L	—	GND	L + R	SAP
			L	H	—		SAP	SAP
			H	L	—		L + R	L + R
	↓	↓	H	H	—	↓	MUTE	MUTE
STEREO	ON	OFF	L	L	L	GND	L	R
	ON		L	L	M		L + R	L + R
	OFF		L	L	H*		L + R	L + R
	ON		L	H	L		L	R
	ON		L	H	M		L + R	L + R
	OFF		L	H	H*		L + R	L + R
	ON		H	L	L		L	R
	ON		H	L	M		L + R	L + R
	OFF		H	L	H*		L + R	L + R
	ON		H	H	L, M		MUTE	MUTE
	OFF	↓	H	H	H*	↓	MUTE	MUTE
STEREO + SAP	ON	ON	L	L	L	GND	L + R	SAP
	ON		L	L	M		L + R	SAP
	OFF		L	L	H*		L + R	SAP
	ON		L	H	L		SAP	SAP
	ON		L	H	M		SAP	SAP
	OFF		L	H	H*		SAP	SAP
	ON		H	L	L		L	R
	ON		H	L	M		L + R	L + R
	OFF		H	L	H*		L + R	L + R
	ON		H	H	L, M		MUTE	MUTE
	OFF	↓	H	H	H*	↓	MUTE	MUTE

* H; V_{CC} – 0.5 to V_{CC}

Mode Matrix No.2

* FSAP → Vcc (SAP discrimination fixing mode)

Broadcast Mode	LED		Pin				Output	
	ST.	SAP	M1	M2	FMONO	FSAP*	LOUT	ROUT
MONO	OFF	OFF	L	L	—	Vcc	L + R	MUTE
			L	H	—		MUTE	MUTE
			H	L	—		L + R	L + R
	↓	↓	H	H	—	↓	MUTE	MUTE
MONO + SAP	OFF	ON	L	L	—	Vcc	L + R	SAP
			L	H	—		SAP	SAP
			H	L	—		L + R	L + R
	↓	↓	H	H	—	↓	MUTE	MUTE
STEREO	ON	OFF	L	L	L	Vcc	L + R	MUTE
	ON		L	L	M		L + R	MUTE
	OFF		L	L	H*		L + R	MUTE
	ON		L	H	L		MUTE	MUTE
	ON		L	H	M		MUTE	MUTE
	OFF		L	H	H*		MUTE	MUTE
	ON		H	L	L		L	R
	ON		H	L	M		L + R	L + R
	OFF		H	L	H*		L + R	L + R
	ON		H	H	L, M		MUTE	MUTE
	OFF	↓	H	H	H*	↓	MUTE	MUTE
STEREO + SAP	ON	ON	L	L	L	Vcc	L + R	SAP
	ON		L	L	M		L + R	SAP
	OFF		L	L	H*		L + R	SAP
	ON		L	H	L		SAP	SAP
	ON		L	H	M		SAP	SAP
	OFF		L	H	H*		SAP	SAP
	ON		H	L	L		L	R
	ON		H	L	M		L + R	L + R
	OFF		H	L	H*		L + R	L + R
	ON		H	H	L, M		MUTE	MUTE
	OFF	↓	H	H	H*	↓	MUTE	MUTE

* H: Vcc – 0.5 to Vcc

Mode Matrix No.3

* SMD, FMONO pin mode control function

SMD · FUNCTION

Broadcast Mode	SAP LED	Pin		Output
		SMD	FSAP	SOUT
• MONO • STEREO	OFF	L	Vcc	L + R
		H	Vcc	Ext*
		L	GND	L + R
		H	GND	L + R
• MONO + SAP • STEREO + SAP	ON	L	Vcc	L + R
		H	Vcc	SAP*
		L	GND	L + R
		H	GND	SAP*

* SAP: When external dbx-TV (Option) is connected

* EXT: Signal input to pin16 (ESAP)

MUTE · FUNCTION

Pin	Output
MUTE	LOUT ROUT SOUT
L	Mute OFF
H	Mute ON

Description of Operation

The U.S. dbx system has the base band spectrum shown in Fig. 1.

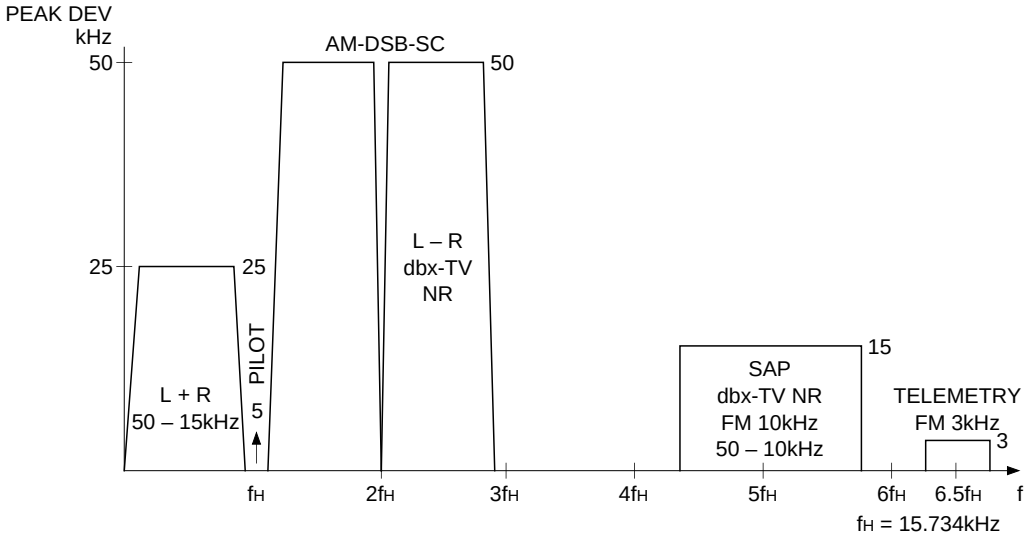


Fig. 1. Base band spectrum

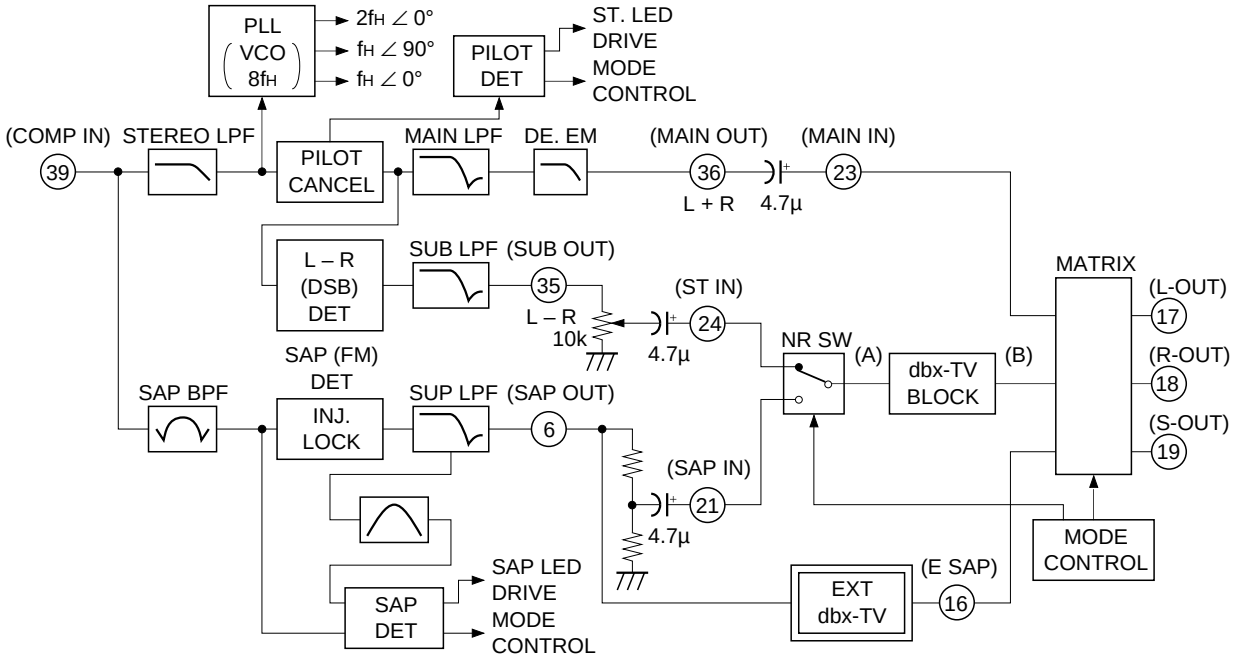


Fig. 2. Whole block diagram (See Fig. 3 for dbx-TV block)

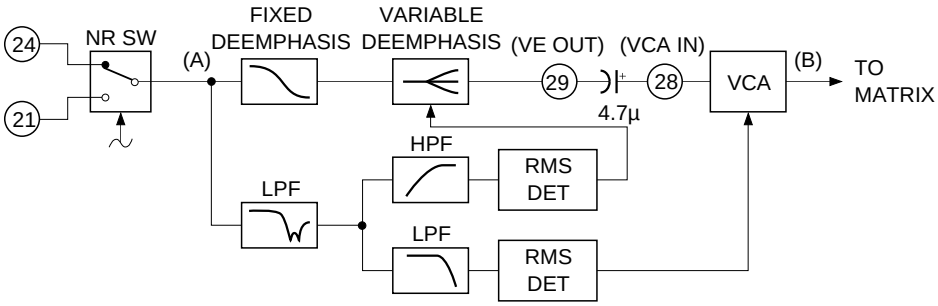


Fig. 3. dbx-TV block

(1) L + R (MAIN)

The dbx signal is input from pin 39 (COMP IN) and led to the STEREO LPF which suppresses the SAP and telemetry signals. Then the pilot signal is cannceled. In the last stage the L – R and SAP signals are removed by the MAIN LPF and the frequency response made flat by the de-emphasis before the L + R signal is input to the matrix.

(2) L – R (SUB)

The L – R signal follows the same route as does the L + R signal before the pilot signal is canceled. The L – R signal has no carrier signal, as it is a suppressed-carrier double-sideband amplitude-modulated (DSB-AM) signal. For this reason, the pilot signal is used to regenerate the carrier signal (quasi-sine wave) to be used for demodulation of the L – R signal. In the last stage the residual high frequency components are removed by the SUB LPF before the L – R signal is input through the NRSW circuit to the dbx-TV block.

(3) SAP

The SAP, as shown in Fig. 1, is an FM signal using 5fH as carrier. The SAP signal alone is first extracted, then FM components are detected. Finally, residual high-frequency components are removed by the SAP-LPF, the f characteristics are flattened, and the SAP signal is input through the NRSW circuit to the dbx-TV block. If there is no SAP signal, the output from Pin 6 is muted.

(4) Mode discrimination

Stereo mode is identified by detecting the pilot signal amplitude. SAP mode is identified by detecting the 5fH carrier and noise around 20kHz after FM detection.

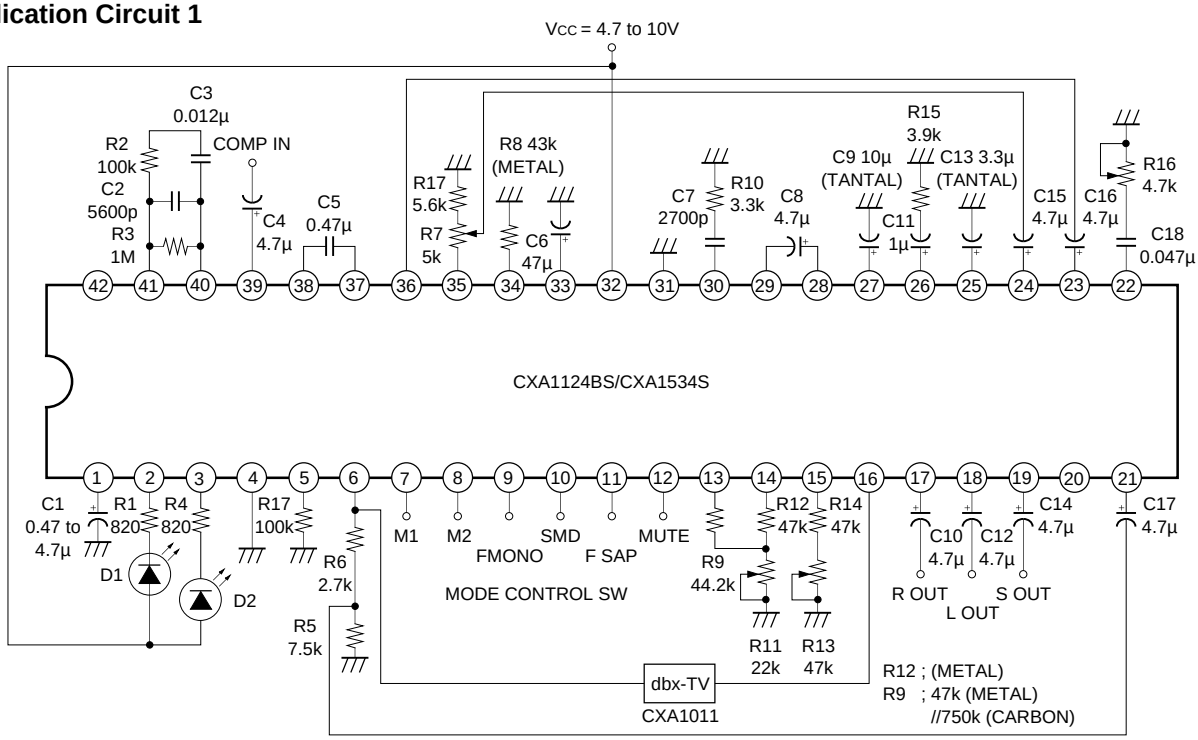
(5) dbx-TV block

The SAP and L – R signals respectively input to pin 24 (ST IN) and pin 21 (SAP IN) are fed to the NRSW circuit where either one of them is selected by the mode control and is input to the dbx-TV block.

The input signal to the block is passed through the fixed de-emphasis circuit and is applied to the variable de-emphasis circuit. The output from the circuit is passed through an externally mounted capacitance and applied to the VCA (Voltage Controlled Amplifier). The output from VCA is converted from a current to a voltage by the operational amplifier before it is input to the matrix.

The transfer function of the variable de-emphasis circuit and the gain of the VCA are controlled by the respective RMS detector circuits. Each of the RMS detector circuits passes the input signal through a predetermined filter to properly weight it befor detecting the rms value of the weighted signal to provide a control signal.

Application Circuit 1



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Precautions in usage of application circuit 1

1) Use V_{CC} at 4.7 to 10V. (recommended value: 9V)

2) Adjustment of stereo and SAP filters is executed simultaneously.
   Adjustment is performed through the stereo filter (Pin 14 (I LPF) volume). Here, to obtain the most suitable stereo separation, set the adjustment signal frequency to 22.9kHz.

3) dbx-TV connected between Pin 6 (SAP OUT) and Pin 16 (E SAP) is an option.
   Connect a dbx-TV system LSI (CXA1011 for example). Then SAP or L + R signal can be output from Pin 19 (S OUT).

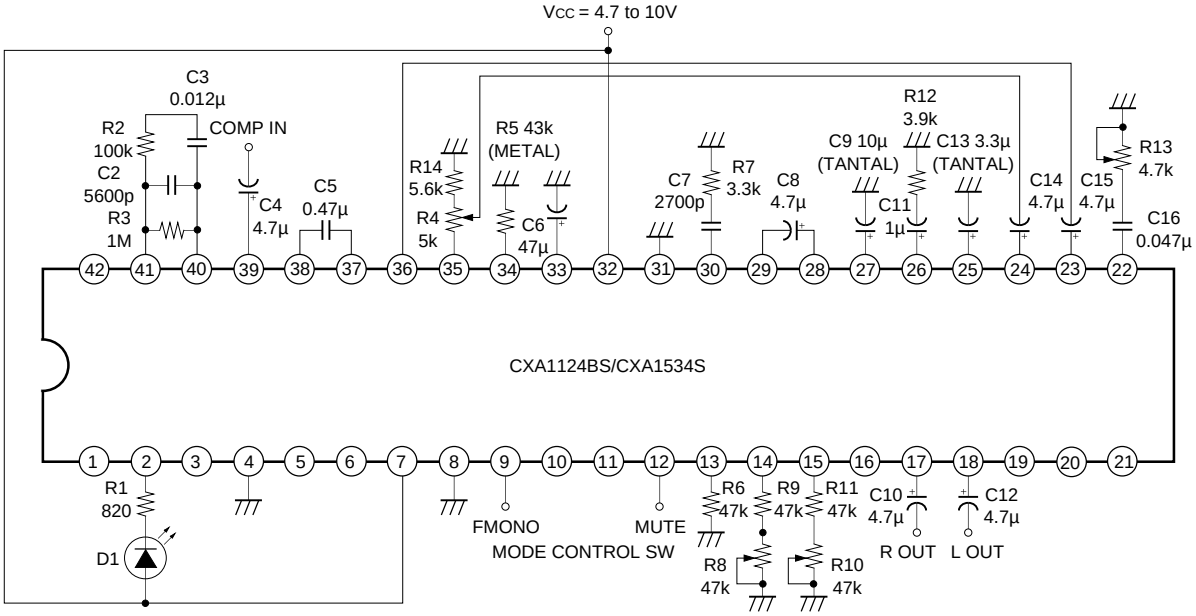
4) Pin 1 capacity value determines mute (or Stereo automatic select) speed when SAP carrier is OFF and SAP discriminating stability at a low intensity electric field. Shrinking the capacitance raises MUTE speed to minimize the switching noise. However discriminating stability is adversely affected. Inversely, when the capacitance is increased it improves stability whereas switching noise grows bigger.

5) Pin 5 is used for fine adjustment of the free-running frequency of the SAP V_{CC}. It is used under normal open conditions if the DC offset at Pin 6 (SAP OUT) causes problems, with the SAP carrier either there or not, connect a resistor of about 100kΩ between Pin 6 and GND.

6) Use a nonpolarized capacitor for C5.

7) If a noise channel is received is at Pin 6 (SAP OUT) noise of several tens of mVp-p will be output (because of soft mute).

Application Circuit 2 (When SAP is not used)

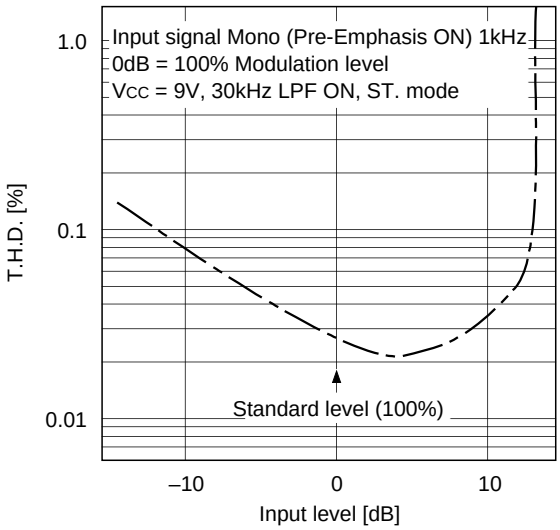


Note) Use a nonpolarized capacitor for C5.

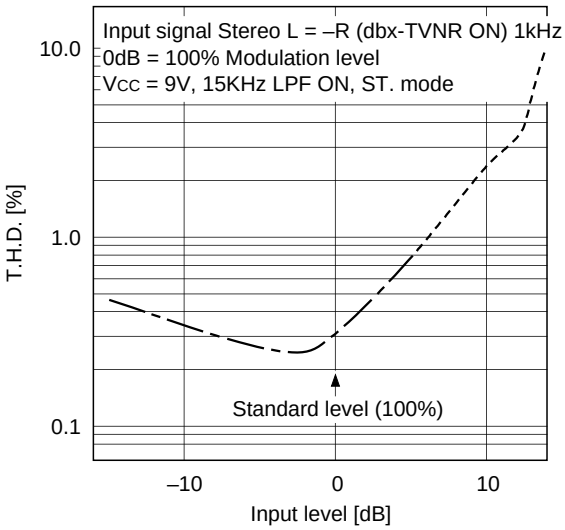
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Examples of Representative Characteristics

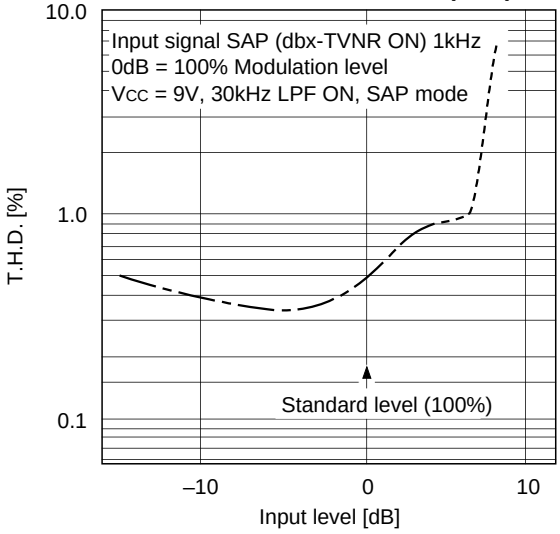
**LINE OUT input vs.
Distortion characteristics 1 (Mono)**



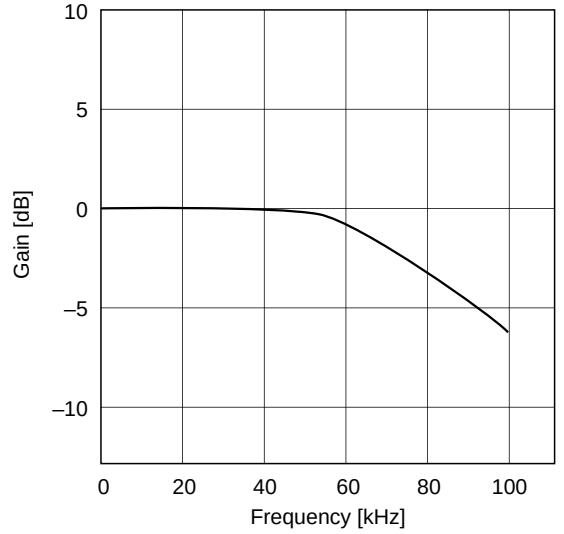
**LINE OUT input vs.
Distortion characteristics 2 (stereo)**



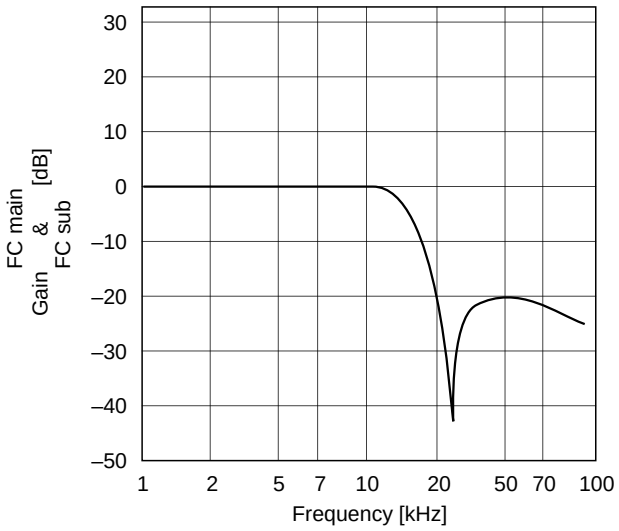
**LINE OUT input vs.
Distortion characteristics 3 (SAP)**



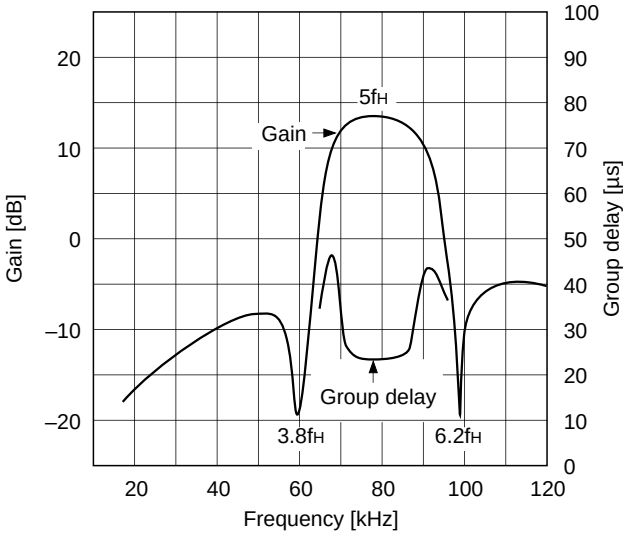
Stereo LPF Frequency characteristics



**Main LPF
Sub LPF Frequency characteristics**



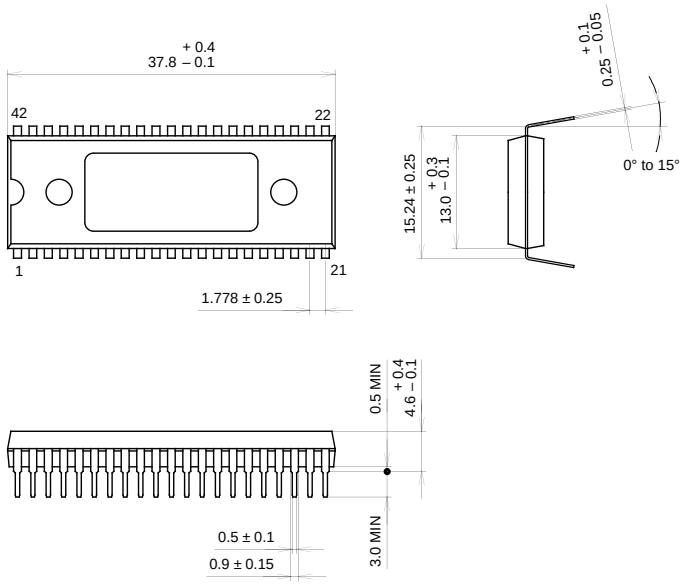
SAP Frequency characteristics and Group delay



Package Outline Unit: mm

CXA1124BS/CXA1534S

42PIN SDIP (PLASTIC) 600mil



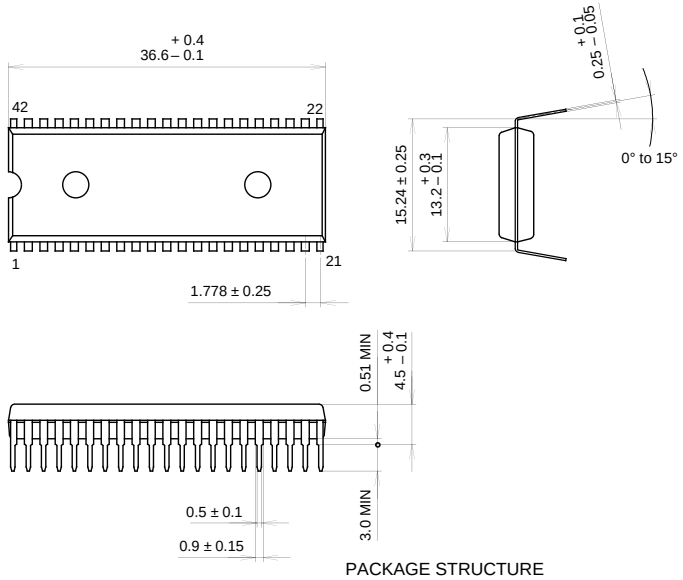
SONY CODE	SDIP-42P-02
EIAJ CODE	SDIP042-P-0600-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	4.4g

CXA1124BS

42PIN SDIP (PLASTIC) 600mil



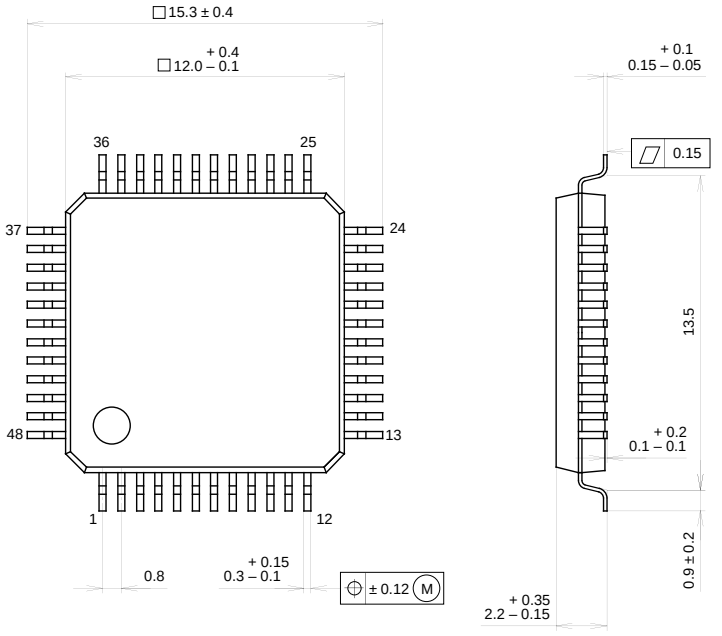
SONY CODE	SDIP-42P-04
EIAJ CODE	*SDIP042-P-0600-C
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	4.4g

CXA1124BQ/CXA1534Q

48PIN QFP (PLASTIC)



SONY CODE	QFP-48P-L04
EIAJ CODE	*QFP048-P-1212-B
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).