

# STANDARD MICROSYSTEMS CORPORATION

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## CRT92C07 PRELIMINARY

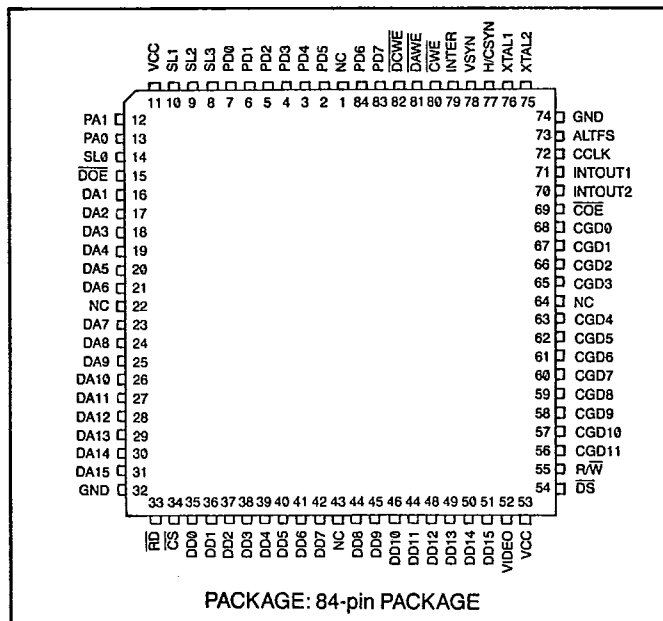
T-52-33-47

# Advanced Terminal Logic Controller ATLC

## FEATURES

- ☐ Internal 12 Bit 42 MHZ Video Shift Register
- ☐ Internal Crystal Oscillator (10 MHZ to 42 MHZ) or External TTL Clock
- ☐ Internal Clock Divider to Generate Alternate 2/3 Dot Clock for 80/132 Column Display
- ☐ Separate 16 Bit Wide Private Display Memory Bus Resolves Memory Contention
- ☐ Row Table Indirect Video Memory Addressing
- ☐ X-Y Cursor Addressing
- ☐ Multiple Bi-Directional Partial Page Smooth Scroll Horizontal Windows
- ☐ Line-Lock Capability
- ☐ Programmable Interrupt Generation
- ☐ Programmable Display Format
  - Dots per Character (9-12)
  - Characters per Data Row (2-192)
  - Data Rows per Frame (2-64)
  - Scan Lines per Data Row (1-16)
- ☐ Programmable Sync Format
  - Horizontal Blanking Time (8-128 Characters)
  - Horizontal Sync Delay (0-64 Characters)
  - Horizontal Sync Pulse (1-64 Characters)
  - Vertical Blanking Time (8-255 Scan Lines)
  - Vertical Sync Delay (0-63 Scan Lines)
  - Vertical Sync Pulse (1-63 Scan Lines)
- ☐ Programmable Attribute Features
  - Character Underline Position
  - Cursor Underline Position
  - Character Blink Rate and Duty Cycle
  - Cursor Blink Rate and Duty Cycle
  - Blink Mode

## PIN CONFIGURATION



- ☐ Mask Programmable Features
  - Vertical Sync Polarity
  - Horizontal Sync Polarity
  - Video Output Polarity
- ☐ Parallel and Tag Character Video Attributes
- ☐ External Character Generator—Writable Character Fonts
- ☐ CMOS Technology for Low Power Consumption
- ☐ All Inputs and Outputs TTL Compatible

## GENERAL DESCRIPTION

The CRT92C07 Advanced Terminal Logic Controller (ATLC) is a CMOS VLSI implementation of all the logic functions required for generation of the timing and video outputs for a terminal design.

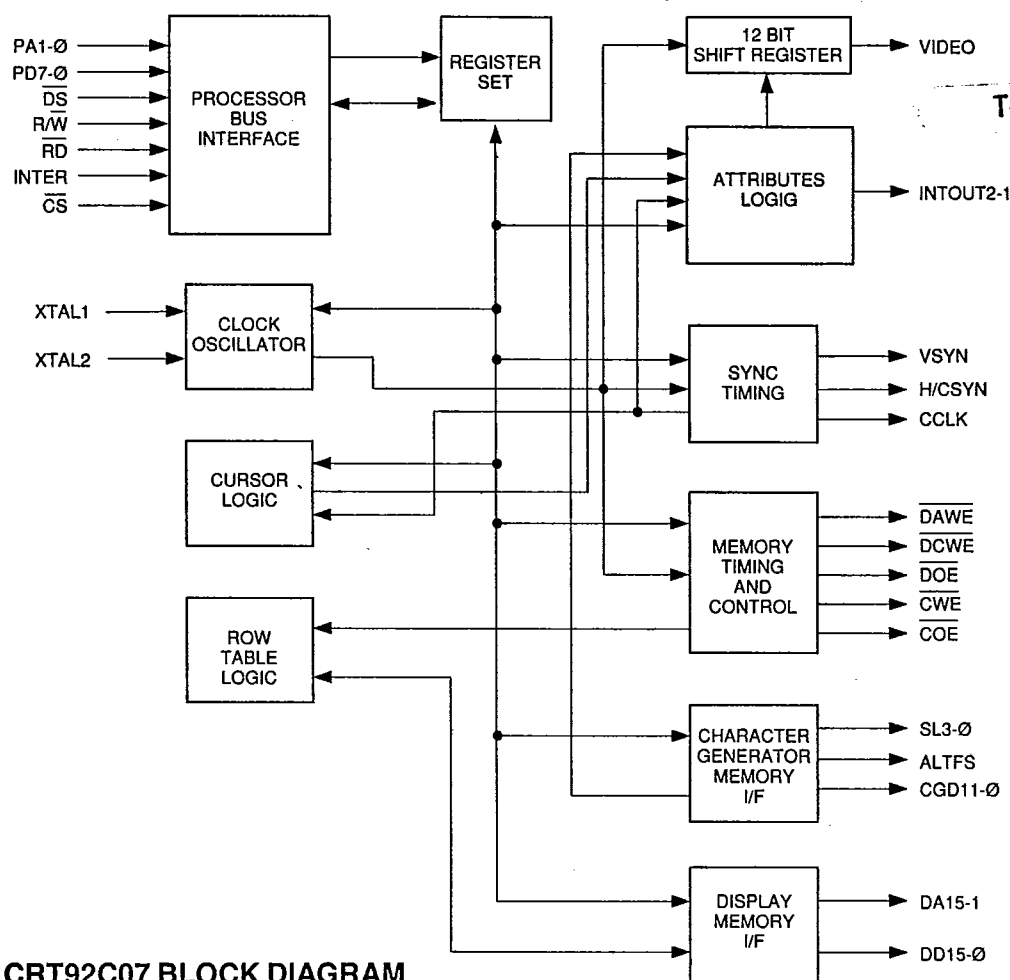
The ATLC incorporates all of the functions associated with a CRT controller, such as the CRT9007, and an attributes controller, such as the CRT9041. These functions include register programmability of all timing parameters, positioning of cursor, addressing of display memory, control of screen partitions, generation of video and timing signals and application of attributes.

The ATLC provides three independent bus interfaces—the system processor, display memory, and character generator memory. Data is transferred from the processor to the display memory and character generator memory through the ATLC. The double speed architecture of the ATLC

provides access to display memory at the character rate for both display refresh and data update functions. The external character generator can be implemented with either EPROM or static RAM.

A row table addressing method is used to access character data from display memory. This method provides the capability to create multiple horizontal split screens and to smooth scroll each screen region independently. The use of a link within the row table allows flexible manipulation of the sequence of character rows on screen.

The built in attributes controller, equivalent to the CRT9041 Video Attributes Controller, can support parallel or tag attributes. All commonly used video terminal attributes are supported, in particular those required for DEC VT100/220 emulation.



CRT92C07 BLOCK DIAGRAM

## DESCRIPTION OF PIN FUNCTIONS

| DISPLAY MEMORY INTERFACE             |                                       |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------------------------------------|---------------------------------------|--------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| PIN NO.                              | NAME                                  | SYMBOL | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 31-23<br>21-16                       | Display Memory Address                | DA15-1 | Output. Fifteen bit Display Memory Address bus. DA15 is the MSB and DA1 is the LSB.                                                                                                                                                                                                                                                                                                                                                                                  |
| 51-44<br>42-35                       | Display Memory Data                   | DD15-0 | Input/Output. Sixteen bit bi-directional Display Memory Data bus. Character data is transferred on DD7-0 and attribute data on DD15-8. DD15 is the MSB and DD0 is the LSB.                                                                                                                                                                                                                                                                                           |
| 82                                   | Display Memory Character Write Enable | DCWE   | Output. Active low write strobe to Display Memory. This signal is active when character data is being written to the display memory.                                                                                                                                                                                                                                                                                                                                 |
| 81                                   | Display Memory Attribute Write Enable | DAWE   | Output. Active low write strobe to Display Memory. This signal is active when attribute data is being written to the display memory.                                                                                                                                                                                                                                                                                                                                 |
| 15                                   | Display Memory Output Enable          | DOE    | Output. Active low output enable strobe to Display Memory. This signal is active whenever character and/or attribute data is read from memory.                                                                                                                                                                                                                                                                                                                       |
| CHARACTER GENERATOR MEMORY INTERFACE |                                       |        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| PIN NO.                              | NAME                                  | SYMBOL | FUNCTION                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 72                                   | Character Clock                       | CCLK   | Output. This output defines the rate at which characters are output to the screen. This signal is also used to externally latch the 8 address bits output from the Display Character RAM for the external character generator. This clock output does not stop as a result of the Reset or Stop commands.                                                                                                                                                            |
| 73                                   | Alternate Font Select                 | ALTFS  | Output. This signal reflects the state of the Underline 2/Alternate Font Select attribute bit (DD0) or the Font Select bit in the Mode4 register. When it reflects the state of the attribute bit, it is internally pipelined such that it is output at the same time that the associated character data is presented to the address inputs of the character generator. This output is typically connected to the MSB of the address bus to the character generator. |

## DESCRIPTION OF PIN FUNCTIONS CONTINUED

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## CHARACTER GENERATOR MEMORY INTERFACE CONTINUED

| PIN NO.        | NAME                              | SYMBOL           | FUNCTION                                                                                                                                                                        |
|----------------|-----------------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 8-10, 14       | Scan Line Data                    | SL3-0            | Output. These signals represent scan line data that are used to provide the four LSB's of the character generator address. SL3 is the MSB and SL0 is the LSB.                   |
| 56-63<br>65-68 | Character Generator Data          | CGD11-0          | Input/Output. Twelve bit bi-directional data bus to the Character Generator Memory.                                                                                             |
| 80             | Character Generator Write Enable  | $\overline{CWE}$ | Output. Active low write strobe to the external Character Generator Memory. This signal is active when the processor is writing pattern data to the Character Generator Memory. |
| 69             | Character Generator Output Enable | $\overline{COE}$ | Output. Active low output enable strobe to Character Generator Memory. This output is active whenever character pattern data is read from memory.                               |

## PROCESSOR INTERFACE

| PIN NO.      | NAME              | SYMBOL           | FUNCTION                                                                                                                                                                                                                                                                                                                                   |
|--------------|-------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 12-13        | Processor Address | PA1-0            | Input. These signals represent a 2-bit address bus from the processor which selects for access either the Status, Pointer, Character Data, RAM Address registers or the internal registers pointed to by the Pointer Register.                                                                                                             |
| 83-84<br>2-7 | Processor Data    | PD7-0            | Input/Output. Eight bit bi-directional Processor Data bus. PD7 is the MSB and PD0 is the LSB.                                                                                                                                                                                                                                              |
| 33           | Read Strobe       | $\overline{RD}$  | Input. This signal is used to strobe data from the ATLC onto the processor bus. A design using $\overline{DS}$ and $R/\overline{W}$ should tie $\overline{RD}$ to ground. A design using $\overline{RD}$ and $\overline{WR}$ should tie $\overline{DS}$ to ground.                                                                         |
| 55           | Read/Write Select | $R/\overline{W}$ | Input. This signal determines if the processor is reading or writing to the ATLC. A design using $\overline{DS}$ and $R/\overline{W}$ should tie $\overline{RD}$ to ground. A design using $\overline{RD}$ and $\overline{WR}$ should tie $\overline{DS}$ to ground.                                                                       |
| 54           | Data Strobe       | $\overline{DS}$  | Input. This signal causes data to be strobed into or out of the ATLC from the Processor Data bus depending on the state of the $R/\overline{W}$ signal. A design using $\overline{DS}$ and $R/\overline{W}$ should tie $\overline{RD}$ to ground. A design using $\overline{RD}$ and $\overline{WR}$ should tie $\overline{DS}$ to ground. |
| 34           | Chip Select       | $\overline{CS}$  | Input. This signal is active low and enables all read and write operations between the processor and the ATLC.                                                                                                                                                                                                                             |
| 79           | Interrupt         | INTER            | Output. This signal is active low and occurs when the ATLC encounters an enabled interrupt causing condition. This signal is reset by reading the Interrupt Status register or a Reset comand. The output is a standard TTL compatible output.                                                                                             |

## VIDEO INTERFACE

| PIN NO. | NAME                      | SYMBOL    | FUNCTION                                                                                                                                                                                                                                                                                                                                                   |
|---------|---------------------------|-----------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 77      | Horizontal/Composite Sync | H/CSYN    | Input/Output. This signal provides either a horizontal or composite synchronization output. It can also be driven as an input to allow synchronization of horizontal sync to an external source. The function of this signal is register programmable. After reset, this signal defaults to the input mode. The polarity of the signal is negative active. |
| 78      | Vertical Sync             | VSYN      | Input/Output. This signal provides a vertical synchronization output. It can also be driven as an input to allow synchronization of vertical sync to an external source. After reset, this signal defaults to the input mode. The polarity of the signal is positive active.                                                                               |
| 52      | Video                     | VIDEO     | Output. This signal provides the serial dot stream for the video interface. The polarity of this signal is active high for pixels ON which provides white characters on a black background.                                                                                                                                                                |
| 70-71   | Intensity Out             | INTOUT2-1 | Output. These signals provide the two bits of the intensity attribute for use with an external mixing circuit to create variable intensity on screen. This signal is modified at the character rate and is synchronized with the VIDEO output.                                                                                                             |

## MISCELLANEOUS

| PIN NO. | NAME          | SYMBOL  | FUNCTION                                                                                                                                                              |
|---------|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 75-76   | Crystal Input | XTAL1-2 | Input. These inputs are used for direct connection to a crystal. An external TTL level clock may be used to drive XTAL1, in which case XTAL2 should be left floating. |
| 11,53   | Power         | VCC     | 5.0 volt power connection.                                                                                                                                            |
| 32,74   | Ground        | GND     | Ground connection.                                                                                                                                                    |

## SYSTEM DESCRIPTION

The system diagram shown in Figure 1 illustrates the hardware required to implement the display interface for a terminal design using the ATLC. There are three bus interfaces, the video interface and the clock inputs. The only external logic required is a decoder for generating the chip select on the processor bus and an 8 bit latch between the Character Generator RAM and the Display Character RAM.

### Processor Bus

The processor bus consists of a 2 bit address bus (PA1-0), 8 bit data bus (PD7-0) and three control signals. The MSB's of the processor address bus are decoded to generate the Chip Select (CS) signal for the ATLC. Three control signals are available as inputs to the ATLC for data transfers over the bus—Read Strobe (RD), Data Strobe (DS) and Read/Write Select (R/W). Only two of these three signals will typically be used depending on the type of system processor being used. One option would be RD and R/W, where R/W would serve as a write strobe input (DS must be grounded), and the other option would be DS and R/W (RD must be grounded).

There are five directly accessible registers in the ATLC which are selected by two address inputs (PA1-0). All other registers in the ATLC are indirectly accessible via one of the direct registers, the Register Pointer. There is also an Interrupt (INTER) output provided identifying key internal events.

### Display Memory Bus

The display memory bus consists of a 15 bit address bus (DA15-1), a 16 bit data bus (DD15-0) and three control signals. The 15 bit Display Memory Address bus provides access to 32K 16 bit words which are divided into 8 bits for character data and 8 bits for attribute data. The last 512 memory locations (highest memory addresses) are used to store the row table. The 8 MSB's of the Display Memory Data bus are the attribute data and are used by the ATLC to generate unique attributes for each character output to the screen. The 8 LSB's of the Display Memory Data bus are the character data and this data is latched externally, as shown in Figure 1, to provide 8 of the 13 bits of the address for the Character Generator Memory. There are three control signals—separate write enables for the character and attribute RAM's and an output enable when reading from both RAMs simultaneously.

The processor can access the display memory through the ATLC. The processor writes an address to the RAM Address Register which serves as a pointer to the display memory location to be accessed. Next the processor either reads data from or writes data to the display memory through the Character Register. The ATLC actually performs the transfer with the display memory using a Busy status bit as a flag to indicate when the transfer has been completed. The ATLC is capable of performing two display memory accesses during each character period. One access is for refresh of the screen (during visible scan time) and the other is for data transfers from the processor (at any time). This architecture eliminates the memory contention problem and provides maximum throughput from the processor to display memory.

### Character Generator Memory Bus

The Character Generator Memory bus consists of a 13 bit address bus, a 12 bit data bus (CGD11-0) and two control signals. Five of the 13 address bits are output by the ATLC (ALTFS, SL3-0) while the other eight come from the external latch that stores the ASCII character data coming from the Display Character RAM. The 12 bits of pixel data are transferred to the ATLC, processed by the attribute logic and

converted to serial form for output on the Video signal. The Character Generator Memory can be implemented with either ROM (EPROM or masked ROM) or RAM. If RAM is used then the processor can make use of registers in the ATLC to download the character font. The control signals provided are a write enable and an output enable.

### Video Interface

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The ATLC outputs all the signals required by the video interface. These include the serial video data signal, two intensity signals and the vertical sync and horizontal/composite sync signals. The dot clock can be generated by a crystal oscillator internal to the ATLC. The crystal placed on the XTAL1/XTAL2 inputs should be that required for the dot clock used for a 132 column display. When switching between 80 and 132 column displays, the ATLC will automatically perform a divide by 2/3 of the dot clock internally. There is also the option of driving the XTAL1 input with a TTL clock.

## FUNCTIONAL DESCRIPTION

### DISPLAY MEMORY OPERATIONS

#### Display Memory Organization

The ATLC has access to an isolated display memory bus with a maximum addressing range of 32K words or 64K bytes. As illustrated in Figure 2 the display memory is divided into four parts. The top 32,256 words of memory are used to store character information. The last 512 words are used to store the row table.

Each word of memory is divided into an odd and even addressed byte. For the portion of memory storing character information, character data is stored in the even bytes and attribute data is stored in the odd bytes. For the portion of memory storing the row table, the data items of the row table are stored only in the even bytes. The odd bytes are not used.

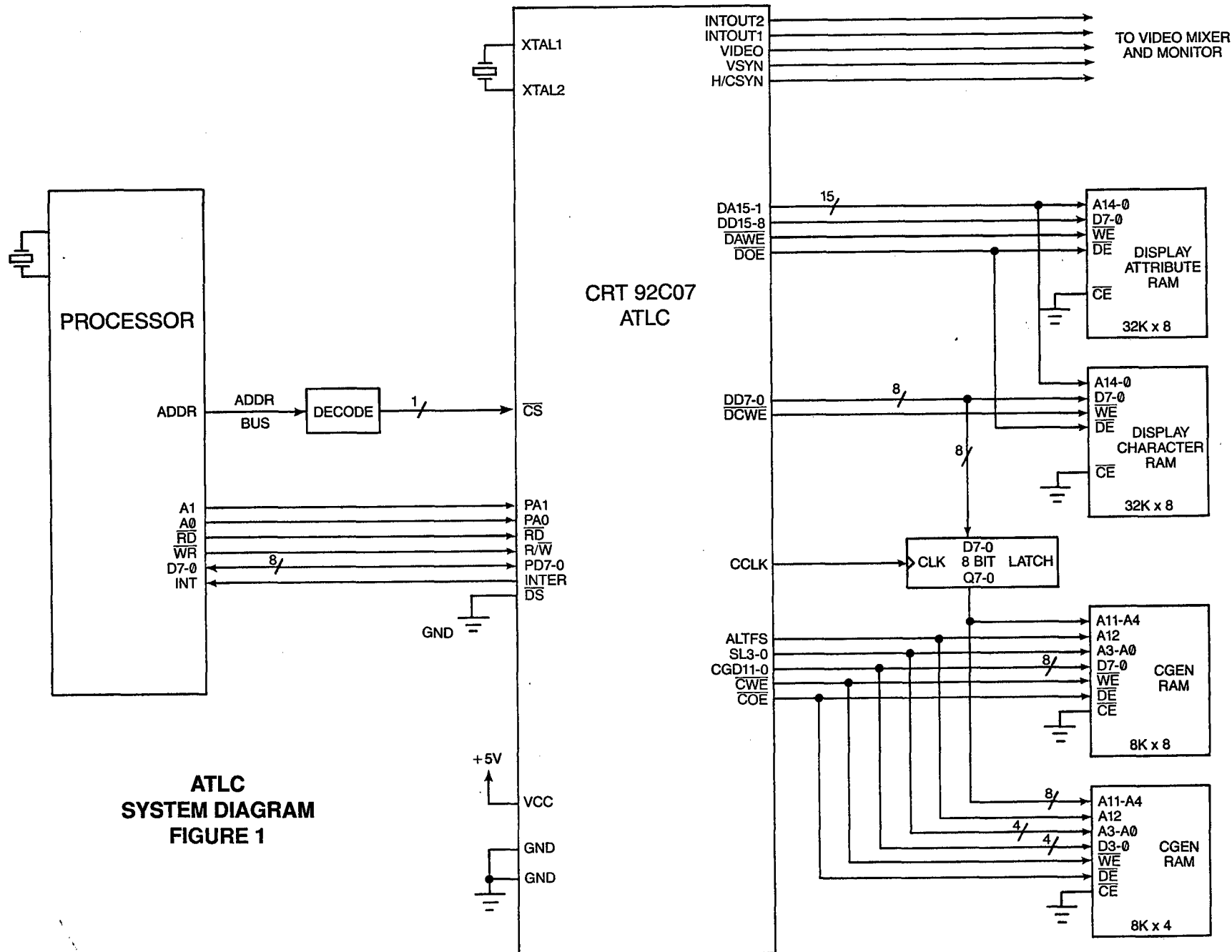
In the parallel attribute mode (IWR3[3]—see Operational Description section for the definition of registers and their labels), both even and odd bytes are addressed. In the tag attribute mode, only the even bytes are addressed—the odd bytes are not used. When operating in the tag attribute mode, the RAM Address Counter Auto-Increment Mode (IWR4 [1-0]) should be programmed for incrementing or decrementing by 2. The RAM Address Register should be set to an even address.

Independent of the attribute mode, the row table is always accessed at even addresses. Each entry in the row table is two bytes long and each entry is accessed by reading or writing 2 sequential bytes, higher address first followed by the lower address byte (always even bytes). When less than the full 32K memory is implemented, the most significant address outputs are not utilized.

### Display Memory Access

The internal RAM Address Counter is an incrementing/decrementing counter used for addressing the external display memory. The system processor accesses this RAM through the ATLC by means of this address counter. The following data transfer operations with the display memory are supported by the ATLC:

- Read/write character AND attribute with RAM address auto-increment or decrement by 1.
- Read/write character OR attribute with RAM address auto-increment or decrement by 2.
- Read/write row table with RAM address auto-increment or decrement by 2.



### Processor Reads From Display Memory

At the beginning of a read operation the RAM Address Register is initialized to the first display memory location to be read—an even address will result in the character data RAM being read while an odd address will result in the character attribute RAM being read. Only byte operations are performed when reading the contents of display memory. The processor performs an initial dummy read of the Character Register. This causes the ATLC to set the Busy status bit, fetch the specified data from the RAM and latch it in the Character Register. The ATLC will then increment or decrement its RAM Address Counter by one or two before it resets the Busy status bit.

The processor should then read the data from the Character Register after Busy goes low. Reading the data will automatically cause the ATLC to set the Busy status bit again and fetch the next byte of data from display memory. Once again, the RAM Address Counter will be incremented or decremented by one or two and Busy will be set. This sequence will continue as long as the processor continues to read data. The processor must not change the RAM Address Register when Busy is high.

### Processor Writes To Display Memory

Two types of write operations are available—byte and word. At the beginning of a write operation the RAM Address Register is initialized to the first display memory location to be modified. The processor then writes the first byte of data to the Character Register causing the ATLC to set the Busy status bit. If the Fill Command Mode bit (IWR4[2]) is reset, the ATLC writes a single byte (either character data or attribute) to the appropriate display RAM. This is controlled by the contents of the RAM Address Register. If the contents are even, then the data is written to the character data portion of memory and if the contents are odd, then the data is stored in the character attribute portion of the memory. Depending on the state of the RAM Address Counter Mode (IWR4[1-0]), the ATLC increments or decrements its internal RAM address counter by one (writing alternate character data and character attribute bytes) or two (writing only character data or character attribute bytes) before it resets the Busy status bit. When the processor verifies that the Busy status bit is reset, then the next byte of data (character data or attribute) to be written can be loaded into the Character Register. This sequence will continue as long as the processor continues to write data to the ATLC Character Register. The processor must not change the RAM Address Register when the Busy bit is set.

For word operations the following sequence of actions will occur. This type of operation is most useful when storing of a sequence of characters with the same attribute.

#### Processor operations—

- Set the RAM Address Counter Mode (IWR4[1-0]) to increment or decrement by two.
- Initialize the RAM Address Register to point to the first character attribute location to be modified.
- Reset the Fill Command Mode bit (byte operation).
- Write the character attribute byte to the Character Register.

#### ATLC operations—

- Sets the Busy bit.
- Writes the character attribute byte to the attribute memory (this byte of data is also buffered internally for subsequent use in write word operations).
- Increments or decrements the RAM Address Counter by two.
- Resets the Busy bit.

#### Processor operations—

- Initialize the RAM Address Register to point to the first character data location to be modified (typically one less than the address set above).
- Set the Fill Command Mode bit (word operation).
- Write the character data byte to the Character Register.

#### ATLC operations—

- Sets the Busy bit.
- Writes the character data byte and the previously stored character attribute byte simultaneously to the display memory.
- Increments or decrements the RAM Address Counter by two.
- Resets the Busy bit.

#### Processor operations—

- The processor may now write consecutive character data bytes to the Character Register (using the Busy bit to monitor the ATLC operations—see NOTE below), while the ATLC will be storing both the character data byte and the common character attribute byte in memory.

**NOTE:** It takes up to five character clock cycles for the ATLC to perform a display memory access. If the processor transfer period of data to the ATLC is greater than 5 character clock (CCLK) cycles, then it is possible to perform accesses of display memory without performing a handshake with the Busy status bit.

### FILL OPERATIONS

The FILL command is used to store a fixed data item (for example, the space character which is used to clear the screen) in consecutive display memory locations. This data can be character data, attribute data or row table entries. The RAM Address, Fill Data, and Fill Count registers as well as the Fill Command Mode bits should contain the desired values before the FILL command is issued.

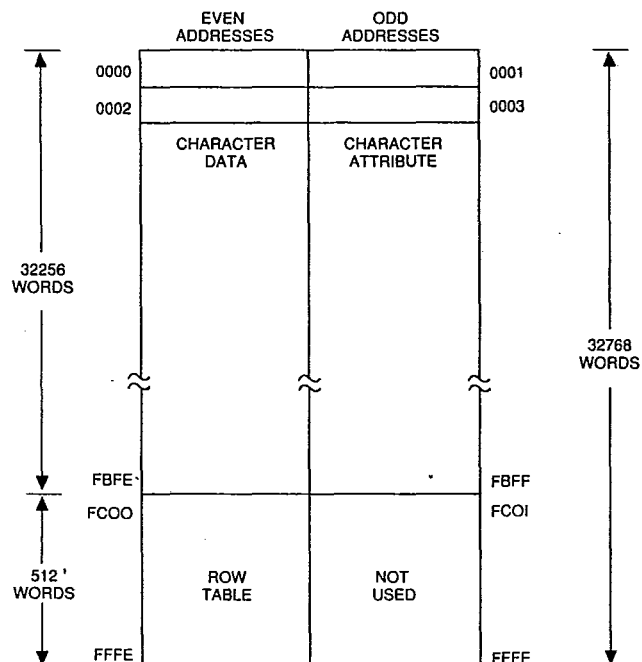
The ATLC implements two FILL commands—Fill Display Memory for Fill Count and Fill Display Memory to End of Display Memory. A FILL command can operate on either the even bytes (character data), odd bytes (attribute data) or all words in display memory. When filling both character and attribute data locations, the fill data is loaded into the Character registers by sequential writes to the Fill Data Register (attribute data should be loaded first followed by character data). When filling only character or attribute data locations, the fill data is loaded into the Character Register by a single write to the Fill Data Register.

The FILL operations are as follows—

- Fill all memory from location pointed to by RAM Address Register—both characters and attributes.
- Fill all memory from location pointed to by RAM Address Register—characters only.
- Fill all memory from location pointed to by RAM Address Register—attributes only.
- Fill from location pointed to by RAM Address Register for Fill Count—both characters and attributes.
- Fill from location pointed to by RAM Address Register for Fill Count—characters only.
- Fill from location pointed to by RAM Address Register for Fill Count—attributes only.

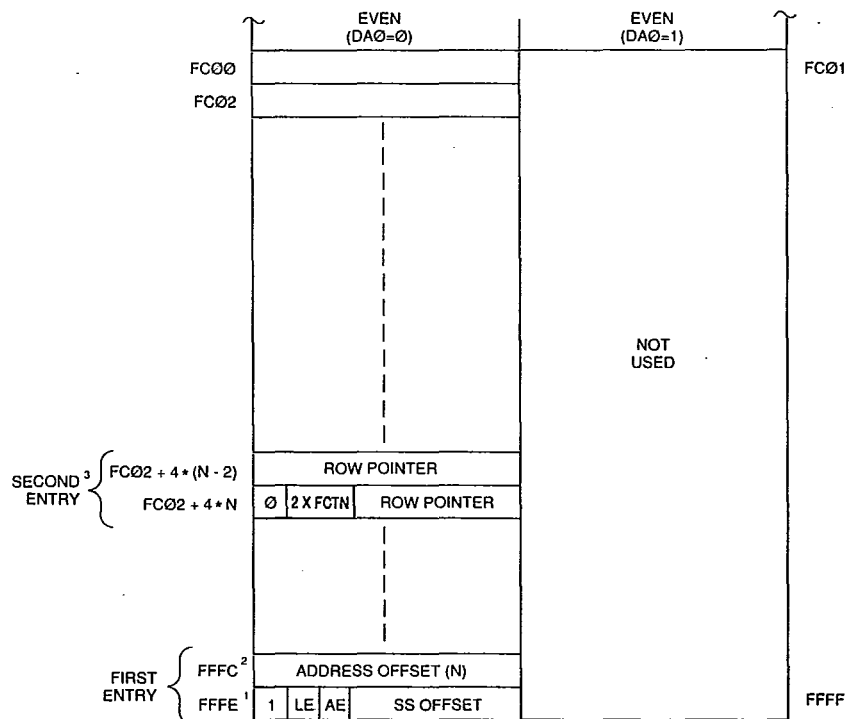
Determination of whether characters, attributes, or both characters and attributes will be filled by the FILL command is made by the values programmed into the Fill Command Mode bit and the RAM Address Counter. If the Fill Command Mode bit is set, then both character data and attribute

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NOTE: 1. Addresses shown in this diagram assume the full 32K word range of memory is implemented. The row table always occupies the highest 512 words of memory (ie—for a 16K word display memory, the row table will be located at addresses 7C00 thru 7FFE.)

**FIGURE 2**  
**DISPLAY MEMORY ORGANIZATION**



NOTES: 1. Most significant byte of first row table entry.  
2. Least significant byte of first row table entry.  
3. N is the value programmed in the LINK's Address Offset field.

**FIGURE 3**  
**ROW TABLE ORGANIZATION**

locations will be filled in a single write operation. If the Fill Command Mode bit is reset, then either character data or attribute locations will be filled one byte at a time. Character data locations will be filled if the RAM Address Register is programmed to an even address and attribute data locations if the RAM Address Register is programmed to an odd address.

In Tag Attribute mode the attribute memory is not used and the RAM Address Register should always be programmed to an even address. The ATLC will automatically increment or decrement the RAM Address Counter by two when executing FILL commands in this mode. When the ATLC is operating in the Parallel Attribute mode and the Fill Command Mode bit is set (both character and attribute RAM's will be filled), then the LSB of the RAM Address Counter is ignored and both RAM's will be filled simultaneously. In this case the RAM Address Register should be programmed to the even character address prior to issuing the FILL Command.

The Fill to End of Display Memory command will cause the ATLC to fill the character and/or attribute RAM in decrementing order starting with the location programmed into the RAM Address Register. The command will terminate after the ATLC fills RAM address 0001H or 0000H.

For Fill Display Memory for Fill Count commands, the Fill Count Register is loaded into an internal counter that is decremented after each character data or attribute byte is written to RAM. This command will cause the ATLC to fill the character and/or attribute RAM in incrementing order starting with the location programmed into the RAM Address Register. The command terminates when the Fill Counter is decremented to zero. The contents of the Fill Count and Character Registers are not affected by the execution of the Fill Command. This allows successive fills to be executed without requiring the Fill Count Register to be reloaded for each one. When filling N bytes (character data or character attributes), the Fill Count Register should be loaded with the value N (the only exception is 0 which equates to a fill count of 256). When filling both character data and character attributes (a word fill), the Fill Count Register should be loaded with the number of character locations to be filled (the number of character data/attribute pairs).

To perform a FILL command, the following actions must occur in the order given:

- 1) Initialize IWR4[2]—FILL COMMAND MODE bit  
Set—Fill word mode.  
Reset—Fill byte mode.
- 2) Load DWR3[15-0]—RAM ADDRESS REGISTER  
Fill word mode—  
LSB = 0 for all addresses.  
Fill byte mode—  
LSB = 0 to fill character data.  
LSB = 1 to fill character attributes.
- 3) Load IWR24[7-0]—FILL DATA REGISTER  
Fill word mode—  
Load two data bytes—character attribute followed by character data.  
Fill byte mode—  
Load one byte of data (see step 2 above).
- 4) Load IWR25[7-0]—FILL COUNT REGISTER  
Required only for FILL DISPLAY MEMORY FOR FILL COUNT command.  
Can be loaded at any time and does not have to be reloaded after each command unless count parameter is to be changed.
- 5) Set command bit in IWR31[1-0]—COMMAND REGISTER

Set bit 1 for FILL DISPLAY MEMORY TO END OF RAM command.

Set bit 0 for FILL DISPLAY MEMORY FOR FILL COUNT command.

Upon completion of the FILL operation the ATLC will generate an interrupt internally and set the DONE INTERRUPT flag (IRR3[0]) and externally, by activating the INTER signal, when the COMMAND COMPLETE INTERRUPT ENABLE bit (IWR4[4]) is set.

## ROW TABLE

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### Row Table Access

The row table is located at the end of display memory. As illustrated in Figure 2, if 32K words of display memory are implemented then the addressing range for the row table would be from FC00H to FFFE. If less memory is implemented, then the MSB's of the address are ignored. For example, with 16K of memory the row table would be located from 7C00H to 7FFE. Within this addressing range there is room for up to 256 2-byte entries in the row table.

Two types of entries may be found in the row table—POINTERS and LINKS. Each row table entry is sixteen bits in length and are located in two sequential bytes in the character data portion of display memory. The LSB of the entry is located at the even addresses (DA1 = 0) and the MSB's at the odd addresses (DA1 = 1). Figure 3 illustrates the row table portion of display memory and shows how the entries are stored. The first row table entry accessed by the ATLC prior to the start of screen refresh will be located at FFFE. (NOTE: This entry must be a LINK.) The entries are fetched MSB's first.

### Row Table Entries

Figure 4 illustrates the format of the two types of entries. If D15 contains a 0 then the entry is a POINTER and if it contains a 1 then the entry is a LINK. The POINTER entry contains two fields of information—the 2X FCTN which controls the Double Height/Double Width attribute of a given row (see Attributes section for a definition of these bits) and the ROW POINTER.

The ROW POINTER is used to indirectly address the first character of a given data row on screen. Character addressing then proceeds sequentially incrementing from the start address defined by the ROW POINTER until the end of the data row is reached. The only restriction in the storing of character data in display memory is that data rows must always begin on even address boundaries within the character data portion of memory (DA1 = 0 for the first character of any data row). This allows the 13 bit ROW POINTER to effectively create a 14 bit memory address. The most significant bit of the Display Memory Address (DA15) is determined by the AE bit in the LINK entry. Figure 5 illustrates how the display memory address is created. (NOTE: The first entry in the row table must be a LINK. This is required so that the DA15 bit can be initialized to the value of the AE bit.) After reading a LINK entry, the AE bit which is output stays fixed until another LINK is read.

The LINK entry is used to implement jumps within the row table and to control the smooth scroll function. Normal row table addressing proceeds sequentially down from the higher order addresses until a link is detected. When a LINK entry is accessed, the DA9-2 bits of the Display Memory Address are forced to the values stored in the Address Offset of the LINK data (see Figure 6). The 6 most significant bits of the Display Memory Address are forced to ones and the two least significant bits are forced to "10" (providing a base address of FC02H). As indicated earlier, the MSB of the row table entry (DA1 = 1) is accessed first and then the LSB (DA1 = 0) is accessed.

|         | D15 | D14 | D13  | D12         | D11 | D10 | D9 | D8 | D7             | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---------|-----|-----|------|-------------|-----|-----|----|----|----------------|----|----|----|----|----|----|----|
| POINTER | 0   | 2X  | FCTN | ROW POINTER |     |     |    |    |                |    |    |    |    |    |    |    |
| LINK    | 1   | LE  | AE   | SS OFFSET   |     |     |    |    | ADDRESS OFFSET |    |    |    |    |    |    |    |

**POINTER—****T-52-33-47**

- D15 : Always a 0.  
 D14-D13 : 2X FCTN controls the Double Height/Double Width attribute for each character row.  
 D12-D0 : ROW POINTER provides 13 of the 15 display memory address bits which define the location of the first character for each character row.

**LINK—**

- D15 : Always a 1.  
 D14 : LE bit, when set, enables the loading of the internal smooth scroll scan line counter with the contents of the SS OFFSET field.  
 D13 : AE bit provides the most significant bit of the display memory address.  
 D12-D8 : SS OFFSET is used to define the first scan line to be displayed for the first character row in a smooth scrolled region.  
 D7-D0 : ADDRESS OFFSET serves as a pointer to the next entry in the row table.

**ROW TABLE ENTRY FORMATS****FIGURE 4**

| DA | DA          | DA | DA | DA | DA | DA | DA | DA | DA | DA | DA | DA | DA | DA | DA |
|----|-------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 15 | 14          | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| AE | ROW POINTER |    |    |    |    |    |    |    |    |    |    |    |    | 0  | WE |

- DA15 : Address Extension (AE) bit from LINK entry.  
 DA14-DA2 : Row Pointer contents from POINTER entry.  
 DA1 : Forced to zero—first character of every data row must be stored in an even memory address.  
 DA0 : This bit is decoded internally and used to generate the appropriate write enable (WE) signals (DAWE, DCWE) which determine whether the character attribute or character data RAM is being accessed.

**DISPLAY MEMORY ADDRESS****FIGURE 5**

| DA | DA | DA | DA | DA | DA | DA  | DA  | DA  | DA  | DA  | DA  | DA  | DA  | DA  | DA |
|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|----|
| 15 | 14 | 13 | 12 | 11 | 10 | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0  |
| 1  | 1  | 1  | 1  | 1  | 1  | AO7 | AO6 | AO5 | AO4 | AO3 | AO2 | AO1 | AO0 | 1/0 | 0  |

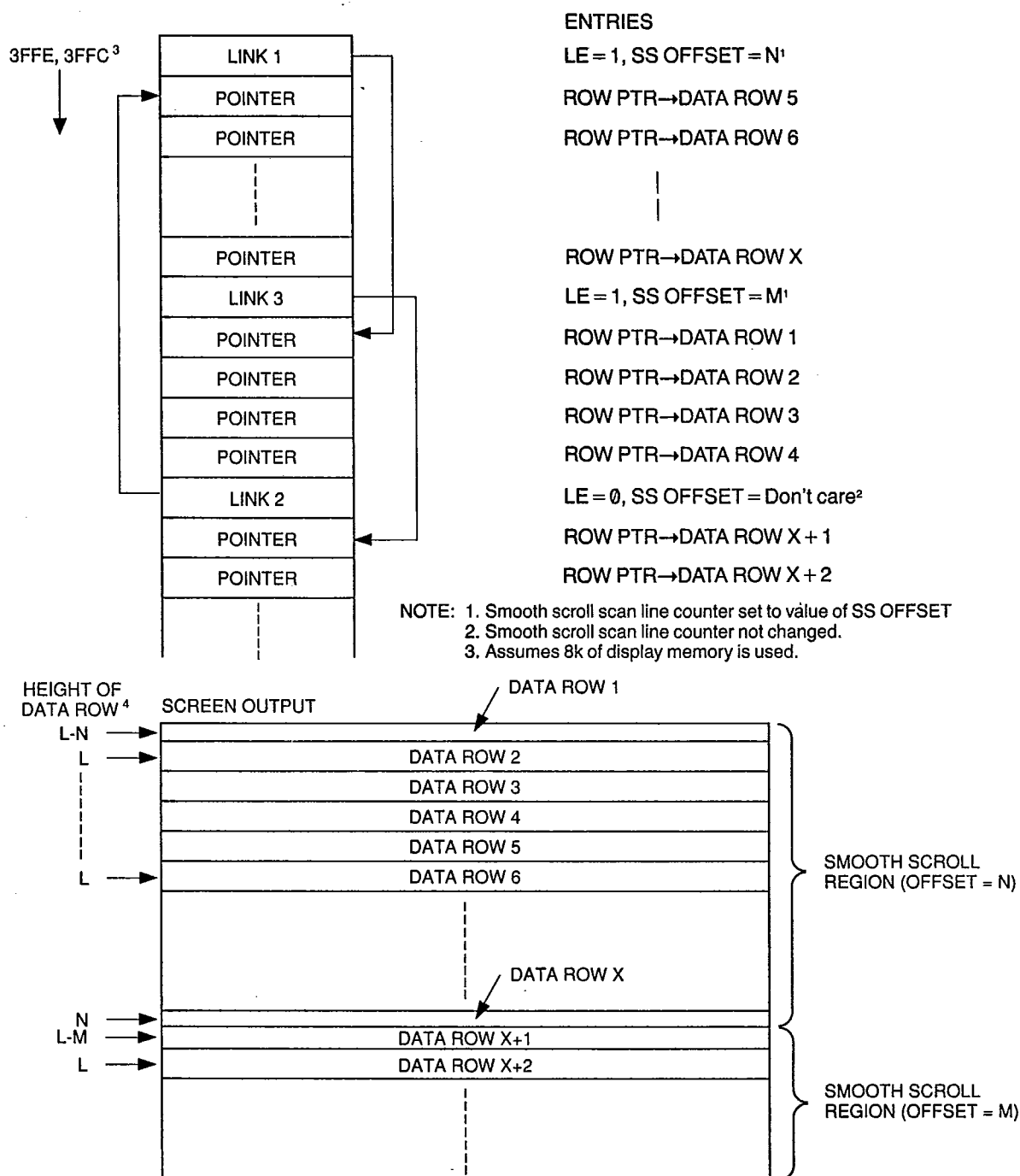
BASE ADDRESS
ADDRESS OFFSET

**LINK WITHIN ROW TABLE****FIGURE 6**

The LINK entry contains two fields of information that control smooth scroll—the Load Enable (LE) control bit and a five bit Smooth Scroll Offset (SS OFFSET) value. An internal smooth scroll scan line counter is initialized with the contents of the SS OFFSET field only when the ATLC encounters a LINK entry with the LE bit set. NOTE: The exception is the first LINK entry at the top of the row table. For this entry only, the SS OFFSET is automatically loaded (independent of the value of the LE bit). Controlling the smooth scroll function for that region requires the update of only the first link within that region (where the LE bit is set). Additional links may be inserted within the region by resetting the LE bit in each LINK

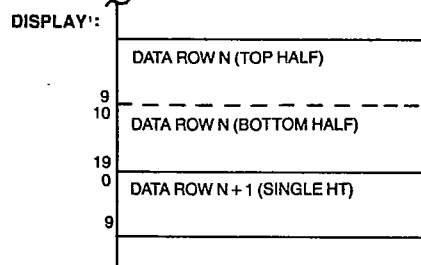
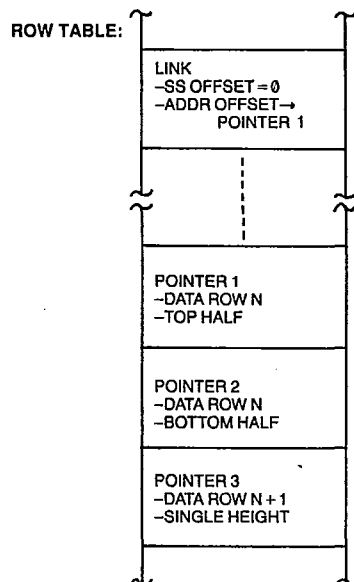
entry which assures that the smooth scroll scan line counter is not modified. This provides the flexibility of inserting and deleting character rows in the middle of any region, even if that region is being smooth scrolled.

Figure 7 shows an example row table and illustrates the control of the smooth scroll function. The first entry is LINK1 which establishes a smooth scroll offset of N. The ADDRESS OFFSET in the LINK entry points to the first POINTER entry which contains the address in Display Memory of the first data row on screen. Three additional pointers are shown before LINK2 is encountered. LINK2 does not modify the smooth scroll scan line counter and



**FIGURE 7**  
**ROW TABLE EXAMPLE**

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NOTE: 1. Assumes 10 scan lines per data row is programmed.

## LINK ENTRY:

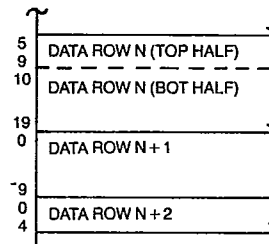
ADDR OFFSET

A. POINTER 1

SS OFFSET

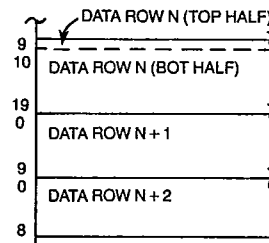
5

## DISPLAY:

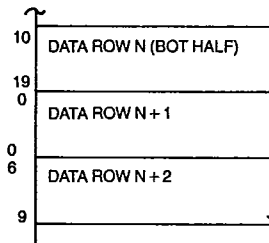


B. POINTER 1

9

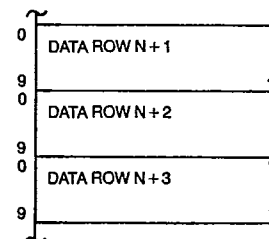


C. POINTER 2

10<sup>2</sup>

D. POINTER 3

0



NOTE 2. For the bottom half of a double height data row the smooth scroll offset values range from 10 to 19 instead of the normal 0 to 9.

**FIGURE 8**  
**DOUBLE HEIGHT ROW SMOOTH SCROLL**

simply points to the remaining POINTERS for this smooth scroll region. LINK3 is encountered next and reinitializes the smooth scroll scan line counter to M and identifies the start of a new region.

### SMOOTH SCROLLING

Smooth scrolling a display region up or down is accomplished by incrementing or decrementing the SS OFFSET value in the LINK that starts the smooth scroll region. Note that when a data row is smooth scrolled, an additional ROW POINTER must be established at the beginning or end of the region depending on the direction of the scrolling function.

When scrolling a row that has been assigned the double high attribute, the full five bit range of the SS OFFSET field must be used (this assumes that a single high row is more than 8 scan lines high). When a smooth scroll region begins with a double high (top or bottom half) data row, care must be taken to ensure that the SS OFFSET value in the row table is properly initialized. Figure 8 illustrates this process. Two factors must be addressed when performing the smooth scroll of double height data rows—one is the pointer to the first data row of the region and the second is the setting of the SS OFFSET field in the LINK entry. Figure 8 shows a display with a double height data row (Data Row N = 20 scan lines) followed by a number of single height data rows (10 scan lines). Data Row N is divided into a top half and a bottom half and requires two consecutive pointers (Pointers 1 and 2). Operations A, B, C, and D in Figure 8 illustrate the following. The ADDRESS OFFSET points to Pointer 1 until the SS OFFSET reaches a value of 9. The next increment of smooth scroll to the value of 10 requires the additional operation of changing the ADDRESS OFFSET to Pointer 2. The remaining portion of Data Row N is smooth scrolled by incrementing the SS OFFSET until it reaches 19. At this time the SS OFFSET is set back to zero and the ADDRESS OFFSET is changed to Pointer 3, completing the smooth scroll of a double height data row. Only the four MSB's of the SS OFFSET value are used when smooth scrolling a single high data row.

A fixed, or jump, scroll region is implemented by setting the SS OFFSET value to zero. Data rows are inserted or deleted by changing the LINK entries or the ROW POINTER values in the POINTER entries. The ATLC will switch from one scrolling region, fixed or smooth, to another at set scan line boundaries with respect to the physical screen (as determined by the values programmed for Scan Lines Per Data Row (IWR15[3-0]) and for Visible Data Rows Per Frame (IWR16[7-0])). The diagram in Figure 9 illustrates how the ATLC accesses row table entries and the relationship between the internal physical screen and smooth scroll scan line counters.

The upper portion of the diagram shows three data rows being smooth scrolled at the top of the screen, followed by a fixed scroll region. The lower portion of the diagram shows the state of the scan line counters and the actions taken during the horizontal blanking periods prior to the display of the first scan line of each row. SL N is the last scan line of the vertical blanking period.

The first row table access takes place during the horizontal blanking period preceding the first visible scan line on the screen. The first row table entry must be a LINK. This LINK will cause the most significant bit of the Display Memory Address to be set equal to the AE bit and the LE bit must be set to enable the initialization of the smooth scroll scan line counter to the value stored in the SS OFFSET field. Within a given region, when the smooth scroll scan line counter reaches its maximum count, row table accesses for the next

data row will be made. The row table accesses are always made prior to the display of the first scan line of the next data row. There will always be a minimum of three accesses—the first two to access the ROW POINTER (two bytes) for initializing the Display Memory Address for the next data row and the third to look ahead at the next row table entry (upper byte only) and determine whether a LINK is present by examining the most significant bit. If a LINK is encountered then the ATLC will detect whether a new smooth scroll region will be started (as determined by the LE bit being set). If the start of a new region is detected then the occurrence of the next row table access will be determined by the physical screen scan line counter reaching its maximum count rather than the smooth scroll scan line counter.

The above events are illustrated in Figure 9. The top of the screen contains three data rows that are being smooth scrolled. Row table accesses occur after the first two data rows when the smooth scroll scan line counter reaches a count of 9 (assumes 10 scan lines per data row). Prior to the start of data row 3, the ATLC detects a LINK with the LE bit set and therefore performs the next row table access when the physical screen scan line counter reaches 9. Note that the ATLC looks at every region on screen as being a smooth scroll region, however a fixed scroll region is effectively created by setting the SS OFFSET value at the beginning of the region to zero and leaving it at that value. The flexibility of the row table allows the creation of multiple independent regions on screen which can be simultaneously scrolled at different speeds and in different directions.

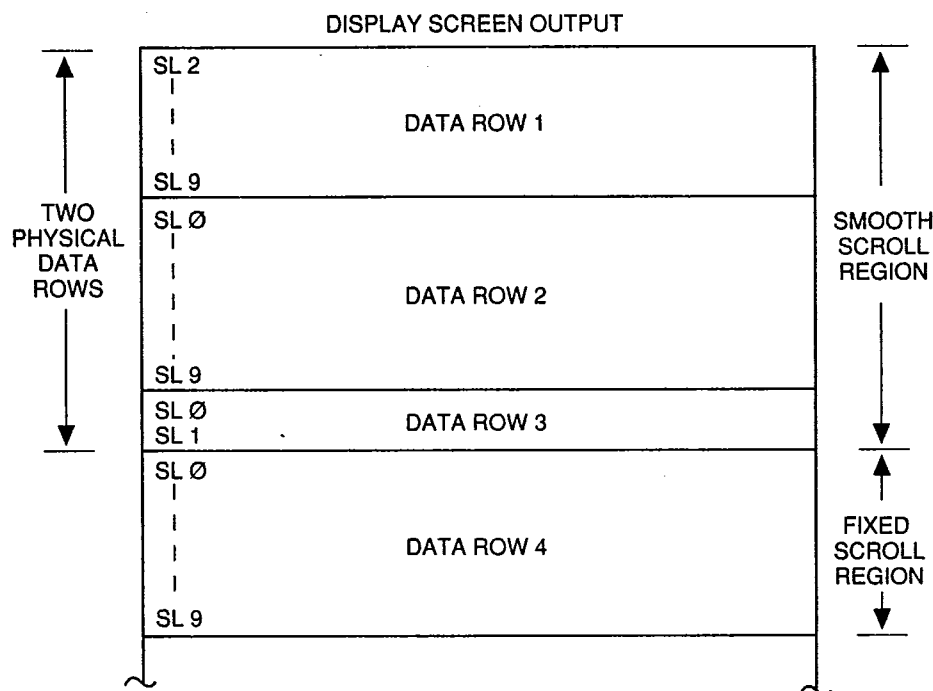
### EXTERNAL CHARACTER GENERATOR

The ATLC accesses scan line pixel data from an external character generator. The character generator can be based on either ROM or RAM. The system diagram in Figure 1 shows that an 8 bit latch is required to buffer the character address used to access the character generator memory. During normal screen refresh the character data is read from the Display Character RAM and clocked into the latch by the CCLK signal.

When using a RAM for the character generator, the character font is transferred by the system processor to the RAM through the ATLC. Transfers take place by writing to four registers (IWR17, 18, 19, and 20). NOTE: The processor should write to these registers only after a RESET or STOP command. When the complete transfer is finished and the BUSY bit is reset, a RESET, STOP or START command must be issued. When writing to the character generator memory, accesses of display memory should not be performed.

The program sequence for writing to the character generator memory is as follows—

- Issue a RESET or STOP command.
- Set the UNDERLINE2 ENABLE bit in the MODE 4 register (IWR3[6]).
- Set/reset the FONT SELECT bit in the MODE 4 register (IWR3[7]).
- For each character in the font—
  - Write to the CHGEN MSB ADDRESS REGISTER (IWR17). Typically this would be the ASCII value of the character.
- For each scan line of the character—
  - Write the scan line number to the CHGEN LSB ADDRESS REGISTER (IWR18).
  - Write 4 MSB bits of font to the CHGEN MSB DATA REGISTER (IWR19).



| DATA ROW | SCAN LINE COUNTER STATE |                       | ROW TABLE ACTIVITY <sup>3</sup>                                                                                                                                                                           | DISPLAY PERIOD    |
|----------|-------------------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|
|          | PS <sup>1</sup>         | SS <sup>2</sup>       |                                                                                                                                                                                                           |                   |
|          |                         |                       | -Detect link to start of new smooth scroll region (LE = 1)<br>-Set smooth scroll scan line counter <sup>4</sup><br>-Fetch POINTER to data row 1<br>-Look ahead to data row 2 (detect presence of POINTER) | VERTICAL BLANKING |
| 1        | 0<br>:<br>7             | 2<br>:<br>9           | -Fetch POINTER to data row 2<br>-Look ahead to data row 3 (detect presence of POINTER)                                                                                                                    | VERTICAL DISPLAY  |
| 2        | 8<br>9<br>0<br>:<br>7   | 0<br>1<br>2<br>:<br>9 | -Fetch POINTER to data row 3<br>-Look ahead to data row 4 (detect presence of LINK)<br>-Detect link to start of new smooth scroll region (LE = 1)                                                         |                   |
| 3        | 8<br>9                  | 0<br>1                | -Fetch POINTER to data row 4<br>-Set smooth scroll scan line counter <sup>4</sup><br>-Look ahead to data row 5 (detect presence of POINTER)                                                               |                   |
| 4        | 0<br>:<br>9             | 0<br>:<br>9           | -Fetch POINTER to data row 5<br>-Look ahead to data row 6                                                                                                                                                 |                   |
| 5        | 0<br>:<br>:             | 0<br>:<br>:           |                                                                                                                                                                                                           |                   |

NOTES: 1. PS—Physical screen scan line counter

2. SS—Smooth scroll scan line counter

3. Row table accesses take place during the horizontal blanking portion of the scan line period.

4. Smooth scroll scan line counter is loaded with SS OFFSET field from LINK entry in row table.

A SS OFFSET = 0 is used to establish a fixed scroll region.

**FIGURE 9  
ROW TABLE ACCESS**

- Write 8 LSB bits of font to the CHGEN LSB DATA REGISTER (IWR20).
- Wait for BUSY bit in the STATUS REGISTER (DRRO) to be reset.
- Issue a RESET, STOP or START command.

Writing to any of the CHGEN registers will cause the following events to occur—

- The contents of the CHGEN MSB ADDRESS REGISTER (IWR17) are output on DD7-0. CCLK will latch this data into the external character latch.
- The contents of the CHGEN LSB ADDRESS REGISTER (IWR18) are output on SL3-0.
- $\overline{DAWE}$ ,  $\overline{DCWE}$  and  $\overline{DOE}$  will go to a high state. This will prevent any bus conflicts between the ATLC's DD7-0 outputs and the display character RAM data signals.
- $\overline{COE}$  will go to a high state and remain there until a RESET, STOP or START command is given.

One additional event takes place when writing to the CHGEN LSB DATA REGISTER (IWR20). The contents of the CHGEN MSB and LSB DATA REGISTERS are output on CGD11-0,  $\overline{CWE}$  is activated and the BUSY bit in the STATUS REGISTER is set. As indicated in the algorithm above, after writing to the CHGEN LSB DATA REGISTER, the processor polls the BUSY bit and waits for it to go to low before writing to the CHGEN registers for the next transfer.

Figure 10 illustrates the maximum size of the character generator font and the tables below define the relationship

between the programming of the character cell size and the actual cell pixels that are displayed.

The width of the character cell is determined by the value programmed in IWR1[1,0] and the actual pixels displayed are shown in Table 1. Pixel C11 is always the first to be shifted out.

| CELL WIDTH   | PIXELS DISPLAYED |
|--------------|------------------|
| 9 Dots/Char  | C11-C3           |
| 10 Dots/Char | C11-C2           |
| 11 Dots/Char | C11-C1           |
| 12 Dots/Char | C11-C0           |

TABLE 1—Character Cell Width

The height of the character cell is determined by the value programmed in IWR15[3-0] and the actual scan lines displayed are shown in Table 2. SLO is always the first scan line to be shifted out.

| CELL HEIGHT | SCAN LINES DISPLAYED |
|-------------|----------------------|
| 10 SL/Char  | SLO - SL9            |
| 11 SL/Char  | SLO - SL10           |
| 12 SL/Char  | SLO - SL11           |
| 13 SL/Char  | SLO - SL12           |
| 14 SL/Char  | SLO - SL13           |
| 15 SL/Char  | SLO - SL14           |
| 16 SL/Char  | SLO - SL15           |

TABLE 2—Character Cell Height

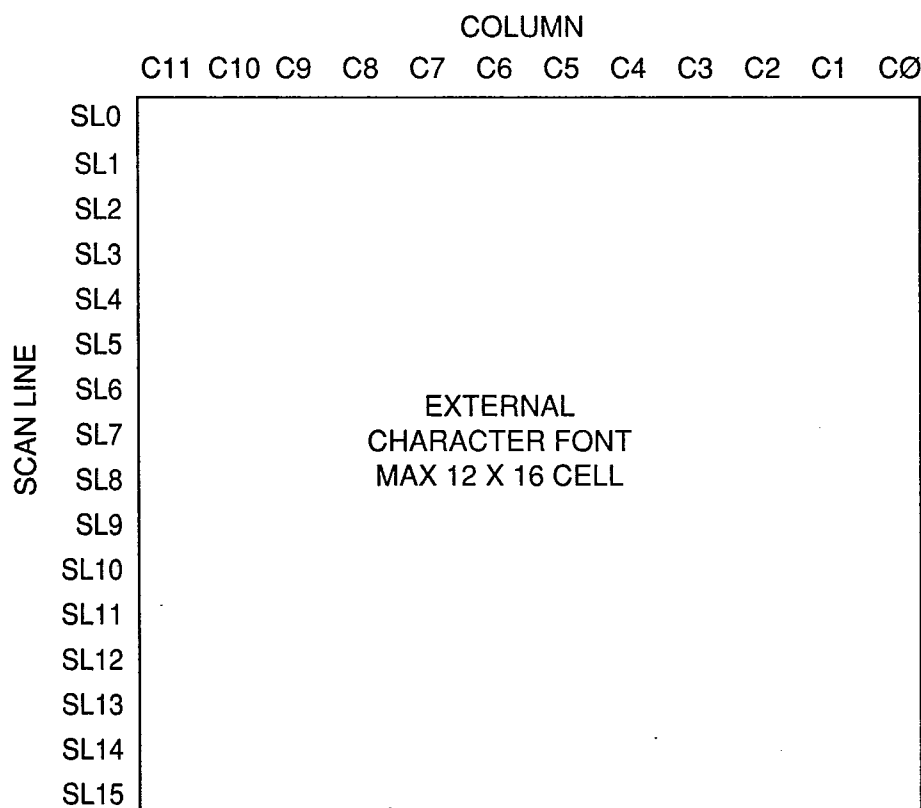


FIGURE 10—CHARACTER CELL

**ATTRIBUTES****Screen Attributes****Dot Stretch**

This attribute is controlled by IWR1[2]. When this register bit is set, the attribute is enabled for the entire screen. When this register bit is reset, the attribute is disabled. Dot stretch is an attribute that assures that single pixels on a horizontal scan line do not occur. The apparent intensity of two consecutive pixels on a scan line may be greater than that of a single pixel. The dot stretch attribute eliminates this problem. Each illuminated pixel is extended into the next pixel location. The following example illustrates the dot stretch mechanism—each illuminated pixel is represented by a "1".

Input bit pattern (CGD11-0) 1 0 0 1 0 1 1 0 0 1 0 0  
Output bit pattern 1 1 0 1 1 1 1 1 0 1 1 0

For a reverse video pattern, the character pixels are also extended as shown above. However, in this case the pixels are not illuminated and in the example shown below are represented by a "0".

Input bit pattern (CGD11-0) 0 1 0 0 1 1 0 0 1 0 0 0  
Reverse video pattern 1 0 1 1 0 0 1 1 0 1 1 1  
Output bit pattern 1 0 0 1 0 0 0 1 0 0 1 1

**Reverse Screen**

This attribute is controlled by IWR3[5]. When this register bit is reset, the normal display mode will be active, with white character pixels on a black background. When this register bit is set, the reverse screen mode will be active, with black character pixels on a white background.

**Row Attributes****Double High and Double Wide Attributes**

The double high and double wide character attributes are enabled on a row by row basis. These attributes are controlled by the value found in bits D14 and D13 of each POINTER entry in the row table. The following table defines the meaning of these bits—

| D14 | D13 | MODE                                |
|-----|-----|-------------------------------------|
| 0   | 0   | Single high/single wide             |
| 0   | 1   | Single high/double wide             |
| 1   | 0   | Double high/double wide top half    |
| 1   | 1   | Double high/double wide bottom half |

**Single High/Single Wide—**

Normal character display mode with a single character occupying a single character cell.

**Single High/Double Wide—**

Each character is displayed in two sequential character cells on a given data row resulting in half the number of characters per data row. Video pixels are shifted out at half the dot frequency used in the single wide character mode.

**Double High/Double Wide—**

Each double high/double wide character occupies four character cells on two sequential data rows. The same character data must be stored in display memory for the two character rows and D14 and D13 in the POINTER for the top row is equal to "10" and for the bottom row is equal to "11".

**Character Attributes****Tag Mode**

In this mode an attribute is applied to all characters that have their TAG bit set. The TAG bit is the most significant bit of each character data byte accessed

from display memory. The attribute that is applied to the character is determined by the contents of the Tag Attribute register (IWR21)—see Attributes Control section of the Register Descriptions for a definition of the attribute bits. The following illustrates the format of the character data from display memory. The display attribute memory is not used in this mode.

DD7 - Tag Bit

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DD6 -

DD5 -

DD4 -

DD3 -

DD2 -

DD1 -

DD0 -

Character Data

**Parallel Mode**

In this mode a unique attribute can be applied to each character. Each character data byte in display memory has an attribute data byte associated with it (see section on Display Memory Organization). The bit assignments for the attribute data byte are defined as follows—

DD15 - Protected Field

DD14 - Blink

DD13 - Blank

DD12 - Intensity 1

DD11 - Intensity 2

DD10 - Reverse Video

DD9 - Underline 1

DD8 - Underline 2/Alternate Font Select

NOTE: The protected field attribute will not effect the video data. It functions as a software flag for the processor indicating which fields are protected. It has no hardware function.

NOTE: Embedded attributes can be emulated by using the parallel mode and storing a common character attribute byte for specific fields of characters using either the FILL DISPLAY MEMORY FOR FILL COUNT command or the write word operations to display memory.

**Blink Options**

Tables 3, 4, and 5 define the interaction between the Video data, the Cursor and the Reverse Screen, Reverse Video character, Intensity Out 1 and 2, and Blink attributes. The Mode 4 register (IWR3[1-0]) is used to select which blink option (as defined by the three tables) will be used by the internal attributes logic. The notation used in the tables is defined as follows—

DATA = Non-inverted video data

DATA = Inverted video data

REVERSE VIDEO = (Reverse Screen) XOR  
(Reverse Video Character)

For each of the three options, two tables are provided. Table A defines the INTOUT1 and 2 signals for a non-blinking character. Table B defines the INTOUT1 and 2 signals for a blinking character. Neither table takes into account the effect of the cursor.

For Tables 3 and 5 (which are compatible with the CRT9041 attributes controller), a block cursor will add one more level of inversion to the video data stream for all scan lines that the cursor appears on. With reference to the tables, the one more level of inversion can be defined as adding one more level of exclusive OR to the Reverse Video parameter. For example—

REVERSE VIDEO = [(Reverse Screen) XOR  
(Reverse Video Character)] XOR (Active Cursor)

**TABLE 3A: NON-BLINK COMBINATIONS  
OPTION TABLE**

| INPUTS         |                  |                |                | VIDEO | OUTPUTS |         |
|----------------|------------------|----------------|----------------|-------|---------|---------|
| BLINK<br>VIDEO | REVERSE<br>VIDEO | INTENSITY<br>1 | INTENSITY<br>2 |       | INTOUT1 | INTOUT2 |
| 0              | 0                | 0              | 0              | DATA  | 0       | 0       |
| 0              | 0                | 0              | 1              | DATA  | 0       | 1       |
| 0              | 0                | 1              | 0              | DATA  | 1       | 0       |
| 0              | 0                | 1              | 1              | DATA  | 1       | 1       |
| 0              | 1                | 0              | 0              | DATA  | 0       | 1       |
| 0              | 1                | 0              | 1              | DATA  | 0       | 1       |
| 0              | 1                | 1              | 0              | DATA  | 0       | 0       |
| 0              | 1                | 1              | 1              | DATA  | 1       | 1       |

**TABLE 3B: BLINK COMBINATIONS OPTION TABLE**

| INPUTS         |              |                |         | CHARACTER<br>BLINK<br>WITHOUT<br>CURSOR (1) | OUTPUTS |     |     |     |     |
|----------------|--------------|----------------|---------|---------------------------------------------|---------|-----|-----|-----|-----|
| BLINK<br>VIDEO | REVERSE<br>1 | INTENSITY<br>2 | INTOUT1 |                                             | INTOUT2 |     |     |     |     |
| 1              | 0            | 0              | 0       | A DATA                                      | B DATA  | A 0 | B 0 | A 0 | B 1 |
| 1              | 0            | 0              | 1       | A DATA                                      | B DATA  | A 0 | B 0 | A 1 | B 0 |
| 1              | 0            | 1              | 0       | A DATA                                      | B DATA  | A 1 | B 0 | A 0 | B 0 |
| 1              | 0            | 1              | 1       | A DATA                                      | B DATA  | A 1 | B 0 | A 1 | B 0 |
| 1              | 1            | 0              | 0       | A DATA                                      | B DATA  | A 0 | B 0 | A 0 | B 1 |
| 1              | 1            | 0              | 1       | A DATA                                      | B DATA  | A 0 | B 0 | A 0 | B 1 |
| 1              | 1            | 1              | 0       | A DATA                                      | B DATA  | A 0 | B 1 | A 0 | B 0 |
| 1              | 1            | 1              | 1       | A DATA                                      | B DATA  | A 0 | B 1 | A 0 | B 1 |

**TABLE 4A: NON-BLINK COMBINATIONS  
OPTION TABLE**

| INPUTS         |                  |                |                | VIDEO | OUTPUTS |         |
|----------------|------------------|----------------|----------------|-------|---------|---------|
| BLINK<br>VIDEO | REVERSE<br>VIDEO | INTENSITY<br>1 | INTENSITY<br>2 |       | INTOUT1 | INTOUT2 |
| 0              | 0                | 0              | 0              | DATA  | 0       | 0       |
| 0              | 0                | 0              | 1              | DATA  | 0       | 1       |
| 0              | 0                | 1              | 0              | DATA  | 1       | 0       |
| 0              | 0                | 1              | 1              | DATA  | 1       | 1       |
| 0              | 1                | 0              | 0              | DATA  | 0       | 0       |
| 0              | 1                | 0              | 1              | DATA  | 0       | 1       |
| 0              | 1                | 1              | 0              | DATA  | 1       | 0       |
| 0              | 1                | 1              | 1              | DATA  | 1       | 1       |

**TABLE 4B: BLINK COMBINATIONS OPTION TABLE**

| INPUTS         |              |                |         | CHARACTER<br>BLINK<br>WITHOUT<br>CURSOR (1) | OUTPUTS |     |  |  |
|----------------|--------------|----------------|---------|---------------------------------------------|---------|-----|--|--|
| BLINK<br>VIDEO | REVERSE<br>1 | INTENSITY<br>2 | INTOUT1 |                                             | INTOUT2 |     |  |  |
| 1              | 0            | 0              | 0       | A B                                         | A B     | A B |  |  |
| 1              | 0            | 0              | 1       | DATA BKGD                                   | 0 0     | 0 0 |  |  |
| 1              | 0            | 1              | 0       | DATA BKGD                                   | 0 0     | 1 1 |  |  |
| 1              | 0            | 1              | 1       | DATA BKGD                                   | 1 1     | 0 0 |  |  |
| 1              | 1            | 0              | 0       | DATA BKGD                                   | 1 1     | 1 1 |  |  |
| 1              | 1            | 0              | 1       | DATA BKGD                                   | 0 0     | 0 0 |  |  |
| 1              | 1            | 1              | 0       | DATA BKGD                                   | 0 0     | 1 1 |  |  |
| 1              | 1            | 1              | 1       | DATA BKGD                                   | 1 1     | 0 0 |  |  |
| 1              | 1            | 1              | 1       | DATA BKGD                                   | 1 1     | 1 1 |  |  |

**TABLE 5A: NON-BLINK COMBINATIONS  
OPTION TABLE**

| INPUTS         |                  |                |                | VIDEO | OUTPUTS |         |
|----------------|------------------|----------------|----------------|-------|---------|---------|
| BLINK<br>VIDEO | REVERSE<br>VIDEO | INTENSITY<br>1 | INTENSITY<br>2 |       | INTOUT1 | INTOUT2 |
| 0              | 0                | 0              | 0              | DATA  | 0       | 0       |
| 0              | 0                | 0              | 1              | DATA  | 0       | 1       |
| 0              | 0                | 1              | 0              | DATA  | 1       | 0       |
| 0              | 0                | 1              | 1              | DATA  | 1       | 1       |
| 0              | 1                | 0              | 0              | DATA  | 0       | 0       |
| 0              | 1                | 0              | 1              | DATA  | 0       | 1       |
| 0              | 1                | 1              | 0              | DATA  | 1       | 0       |
| 0              | 1                | 1              | 1              | DATA  | 1       | 1       |

**TABLE 5B: BLINK COMBINATIONS OPTION TABLE**

| INPUTS         |              |                |         | CHARACTER<br>BLINK<br>WITHOUT<br>CURSOR (1) | OUTPUTS |   |   |  |
|----------------|--------------|----------------|---------|---------------------------------------------|---------|---|---|--|
| BLINK<br>VIDEO | REVERSE<br>1 | INTENSITY<br>2 | INTOUT1 |                                             | INTOUT2 |   |   |  |
| 1              | 0            | 0              | 0       | A                                           | B       | A | B |  |
| 1              | 0            | 0              | 1       | DATA                                        | DATA    | 0 | 0 |  |
| 1              | 0            | 1              | 0       | DATA                                        | DATA    | 0 | 1 |  |
| 1              | 0            | 1              | 1       | DATA                                        | DATA    | 1 | 0 |  |
| 1              | 1            | 0              | 0       | DATA                                        | DATA    | 1 | 1 |  |
| 1              | 1            | 0              | 1       | DATA                                        | DATA    | 0 | 0 |  |
| 1              | 1            | 1              | 0       | DATA                                        | DATA    | 0 | 1 |  |
| 1              | 1            | 1              | 1       | DATA                                        | DATA    | 1 | 1 |  |

NOTE: 1. Duty cycle for character blink is programmed in MODE 6 register (IWR5[1,0]). Table indicate the states of the Video DATA and INTOUT1/2 outputs during the OFF (A) and ON (B) periods. BKGD means background video level.

An underline cursor will be combined with the video data with a logical OR operation. A blinking block cursor adds and then removes one more level of inversion to the video data as described above. Character blink and cursor blink will be active together resulting in the mixing of the two blink rates.

For Table 4 (which is compatible with the CRT9021 attributes controller), a blinking character always blinks to background and a blinking cursor (block or underline) overrides a character blink for all scan lines that the cursor appears on. A blinking underline cursor on top of a blinking character will inhibit the character blink action for the scan line on which the cursor is active. A non-blinking cursor adds one more level of inversion to either a non-blinking character or a blinking character.

If the Cursor Disable Intensity bit (IWR3[2]) is set, then the Intensity Out 1 and 2 signals will be forced to zero for all scan lines under the cursor. This inhibits character blinking in the blink option modes associated with Tables 3 and 5. If the Cursor Disable Intensity bit is reset, then Tables 3, 4, and 5 define the states of the INTOUT1 and 2 signals.

#### Cursor

Cursor control is achieved through the programming of three registers—IWR0, IWR22 and IWR23. IWR22 and IWR23 are used to define the location of the cursor on screen. This location is absolute with respect to the screen and will not change when smooth scrolling data rows. The MODE 1 register (IWR0) is used to blank the cursor, to control its display mode (blinking and underline or block), to control what scan line the underline cursor will appear on, and to enable a double high/double wide cursor.

When a cursor appears in a double high/double wide data row, the following must be taken into consideration. The cursor location programmed should be the Nth character position in the row for IWR22 (same as for a single wide character row—the actual cursor position on screen will be shifted to the right because of the double wide attribute) and the character row in which the top half of the double high character will be located for IWR23. (NOTE: Character row position of double high cursor must be incremented by two (software controlled) when moving the cursor to the next row.) If the cursor is a block cursor, then the DH/DW Cursor Enable bit (IWR0[3]) should be set if a full double high cursor is desired. For an underline cursor, this bit should be reset, otherwise underline cursors will appear in both the top and bottom halves of the character location.

#### HORIZONTAL AND VERTICAL SYNCHRONIZATION

The horizontal and vertical synchronization outputs are register programmable with respect to their pulse widths and positions relative to the horizontal and vertical visible display times. See the register definitions under the Operational Description section for details of the timing parameters.

If these signals are configured to be inputs, then an external source can be used to synchronize the operation of the ATLC. If the External HSYNC Enable register bit (IWR1[5]) is set then the H/CSYN signal (pin 77) is configured as an input. When an external signal drives this input low, then the ATLC will initiate a horizontal retrace cycle two CCLK's later. This will lock the ATLC's horizontal frequency to that of the external signal. The horizontal timing registers should be programmed to a value greater than the timing of the external signal for external synchronization.

If the External VSYNC Enable register bit (IWR1[4]) is set then the VSYN signal (pin 78) is configured as an input. When an external signal drives this input low, then the ATLC will initiate a vertical retrace cycle on the leading edge of the next HSYN pulse. This will lock the ATLC's vertical frequency to that of the external signal. The vertical timing registers should be programmed to a value greater than the timing of the external signal for external synchronization.

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#### OPERATIONAL DESCRIPTION REGISTERS ACCESSIBILITY

Figures 11 to 14 illustrate the bit layout of all addressable registers within the ATLC. All registers are 8 bits wide. The RAM Address Register is 16 bits internally and requires a double access to the same register address (see Register Descriptions below). Access to these registers takes place via four control inputs (RD, R/W, DS, CS), two address inputs (PA1-0), and an 8 bit bi-directional data bus (PD7-0). The register set of the ATLC is divided into 5 registers that are directly accessible via the address inputs (PA1-0) with the remaining registers being indirectly accessible via the Register Pointer.

The four control inputs provide the flexibility to implement one of two different processor interfaces. The two options available are as follows—

- Option 1 - Processor that uses  $\overline{RD}$  and  $\overline{WR}$
- Option 2 - Processor that uses  $\overline{DS}$  and R/W

As shown in Table 6 below, option 1 is implemented by grounding the  $\overline{DS}$  input which allows the  $\overline{RD}$  signal to be used as a Read Strobe input and the R/W signal to be used as a Write Strobe input. Option 2 is implemented by grounding the  $\overline{RD}$  input which allows the  $\overline{DS}$  signal to be used as a Data Strobe input and the R/W signal to be used as a Read/Write Select input.

| ATLC INPUTS     | OPTION 1        | OPTION 2        |
|-----------------|-----------------|-----------------|
| $\overline{DS}$ | GND             | $\overline{DS}$ |
| $\overline{RD}$ | $\overline{RD}$ | GND             |
| R/W             | $\overline{WR}$ | R/W             |

Table 6—Processor/ATLC Interface

In the Register Descriptions section that follows a 4 or 5 character designation is used to identify the registers. This designation is defined below—

- 1st Character: D - Directly addressed register.  
I - Indirectly addressed register.
- 2nd Character: R - Indicates register contents can be read.  
W - Indicates register contents can be written.
- 3rd Character: R - Indicates register.
- 4th/5th Character: N - N equals the address of the register.  
Direct - N determined by state of PA1-0 inputs to ATLC (see Tables 7 & 8).  
Indirect - N determined by contents of Register Pointer (see Tables 9 & 10).

In the Register Description section that follows the registers are divided into 6 groups. In the Tables 7 thru 10 the groups and register designations are identified and the specific page on which the register description is found are provided for ease of reference to the descriptions. Directly accessible registers include those shown in Tables 7 and 8. Access to these registers takes place via the PA1-0 address inputs, the PD7-0 data inputs and the control signals described above.

| PA1 | PA0 | REG DES | REGISTER SELECTED    | REGISTER GROUP     | SECTION |
|-----|-----|---------|----------------------|--------------------|---------|
| 0   | 0   | DWR0    | Register Pointer     | ATLC Control       | II      |
| 0   | 1   | DWR1    | Indirect Register    | ATLC Control       | II      |
| 1   | 0   | DWR2    | Character Register   | Display Memory I/F | V       |
| 1   | 1   | DWR3    | RAM Address Register | Display Memory I/F | V       |

Table 7—Direct Write Registers

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| PA1 | PA0 | REG DES | REGISTER SELECTED    | REGISTER GROUP     | SECTION |
|-----|-----|---------|----------------------|--------------------|---------|
| 0   | 0   | DRR0    | Status Register      | ATLC Control       | II      |
| 0   | 1   | DRR1    | Indirect Register    | ATLC Control       | II      |
| 1   | 0   | DRR2    | Character Register   | Display Memory I/F | V       |
| 1   | 1   | DRR3    | RAM Address Register | Display Memory I/F | V       |

Table 8—Direct Read Registers

All other registers are accessed by first loading the Register Pointer and then performing a read or write access to the Indirect Register. Registers that can be read (only three) are

identified in Table 10, while registers to which data can be written are identified in Table 9.

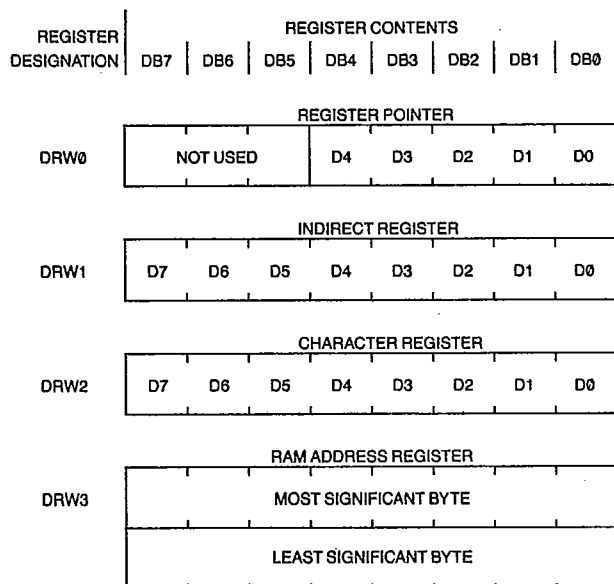
| REGISTER POINTER<br>DB4 DB3 DB2 DB1 DB0 |   |   |   |   | REG DES | REGISTER SELECTED          | REGISTER GROUP     | SECTION |
|-----------------------------------------|---|---|---|---|---------|----------------------------|--------------------|---------|
| 0                                       | 0 | 0 | 0 | 0 | IWR0    | Mode 1                     | Cursor Control     | III     |
| 0                                       | 0 | 0 | 0 | 1 | IWR1    | Mode 2                     | Timing             | I       |
| 0                                       | 0 | 0 | 1 | 0 | IWR2    | Mode 3                     | Attribute Control  | IV      |
| 0                                       | 0 | 0 | 1 | 1 | IWR3    | Mode 4                     | Attribute Control  | IV      |
| 0                                       | 0 | 1 | 0 | 0 | IWR4    | Mode 5                     | ATLC Control       | II      |
| 0                                       | 0 | 1 | 0 | 1 | IWR5    | Mode 6                     | Attribute Control  | IV      |
| 0                                       | 0 | 1 | 1 | 0 | IWR6    | Mode 7                     | Cursor Control     | III     |
| 0                                       | 0 | 1 | 1 | 1 | IWR7    | Mode 8                     | Timing             | I       |
| 0                                       | 1 | 0 | 0 | 0 | IWR8    | Mode 9                     | Timing             | I       |
| 0                                       | 1 | 0 | 0 | 1 | IWR9    | Mode 10                    | Timing             | I       |
| 0                                       | 1 | 0 | 1 | 0 | IWR10   | Mode 11                    | Timing             | I       |
| 0                                       | 1 | 0 | 1 | 1 | IWR11   | Mode 12                    | Timing             | I       |
| 0                                       | 1 | 1 | 0 | 0 | IWR12   | Mode 13                    | Timing             | I       |
| 0                                       | 1 | 1 | 0 | 1 | IWR13   | Mode 14                    | Timing             | I       |
| 0                                       | 1 | 1 | 1 | 0 | IWR14   | Mode 15                    | Timing             | I       |
| 0                                       | 1 | 1 | 1 | 1 | IWR15   | Mode 16                    | Timing             | I       |
| 1                                       | 0 | 0 | 0 | 0 | IWR16   | Mode 17                    | Timing             | I       |
| 1                                       | 0 | 0 | 0 | 1 | IWR17   | CHGEN MSB Addr             | CHGEN Memory I/F   | VI      |
| 1                                       | 0 | 0 | 1 | 0 | IWR18   | CHGEN LSB Addr             | CHGEN Memory I/F   | VI      |
| 1                                       | 0 | 0 | 1 | 1 | IWR19   | CHGEN MSB Data             | CHGEN Memory I/F   | VI      |
| 1                                       | 0 | 1 | 0 | 0 | IWR20   | CHGEN LSB Data             | CHGEN Memory I/F   | VI      |
| 1                                       | 0 | 1 | 0 | 1 | IWR21   | Tag Attribute              | Attribute Control  | IV      |
| 1                                       | 0 | 1 | 1 | 0 | IWR22   | Horizontal Cursor Position | Cursor Control     | III     |
| 1                                       | 0 | 1 | 1 | 1 | IWR23   | Vertical Cursor Position   | Cursor Control     | III     |
| 1                                       | 1 | 0 | 0 | 0 | IWR24   | Fill Data                  | Display Memory I/F | V       |
| 1                                       | 1 | 0 | 0 | 1 | IWR25   | Fill Count                 | Display Memory I/F | V       |
| 1                                       | 1 | 0 | 1 | 0 | IWR26   | Reserved                   |                    |         |
| 1                                       | 1 | 0 | 1 | 1 | IWR27   | Reserved                   |                    |         |
| 1                                       | 1 | 1 | 0 | 0 | IWR28   | Reset Register             | ATLC Control       | II      |
| 1                                       | 1 | 1 | 0 | 1 | IWR29   | Stop Register              | ATLC Control       | II      |
| 1                                       | 1 | 1 | 1 | 0 | IWR30   | Start Register             | ATLC Control       | II      |
| 1                                       | 1 | 1 | 1 | 1 | IWR31   | Command Register           | ATLC Control       | II      |

Table 9—Indirect Write Registers

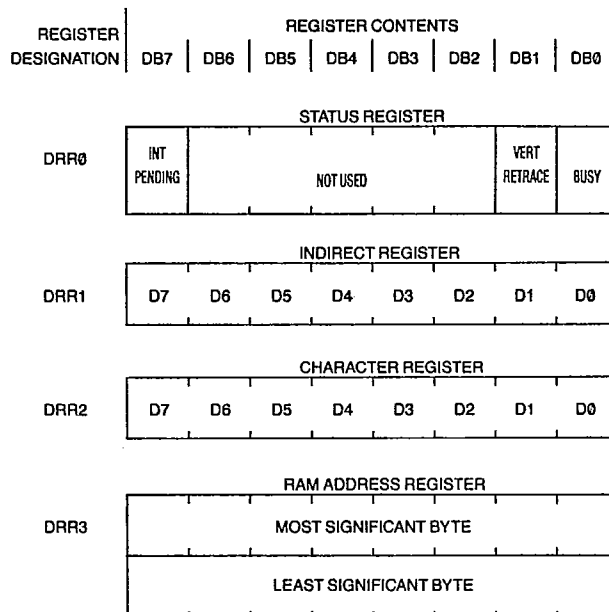
| REGISTER POINTER<br>DB4 DB3 DB2 DB1 DB0 |   |   |   |   | REG DES | REGISTER SELECTED          | REGISTER GROUP | SECTION |
|-----------------------------------------|---|---|---|---|---------|----------------------------|----------------|---------|
| 0                                       | 0 | 0 | 0 | 0 |         | Reserved                   |                |         |
| .                                       | . | . | . | . |         | .                          |                |         |
| .                                       | . | . | . | . |         | .                          |                |         |
| 1                                       | 0 | 1 | 0 | 1 |         | Reserved                   |                |         |
| 1                                       | 0 | 1 | 1 | 0 | IRR22   | Horizontal Cursor Position | Cursor Control | III     |
| 1                                       | 0 | 1 | 1 | 1 | IRR23   | Vertical Cursor Position   | Cursor Control | III     |
| 1                                       | 1 | 0 | 0 | 0 |         | Reserved                   |                |         |
| .                                       | . | . | . | . |         | .                          |                |         |
| .                                       | . | . | . | . |         | .                          |                |         |
| 1                                       | 1 | 1 | 1 | 0 |         | Reserved                   |                |         |
| 1                                       | 1 | 1 | 1 | 1 | IRR31   | Interrupt Status           | ATLC Control   | II      |

Table 10—Indirect Read Registers

**FIGURE 11**  
**DIRECT WRITE REGISTER FORMATS**



**FIGURE 12**  
**DIRECT READ REGISTER FORMATS**



**FIGURE 13**  
**INDIRECT WRITE REGISTER FORMATS**

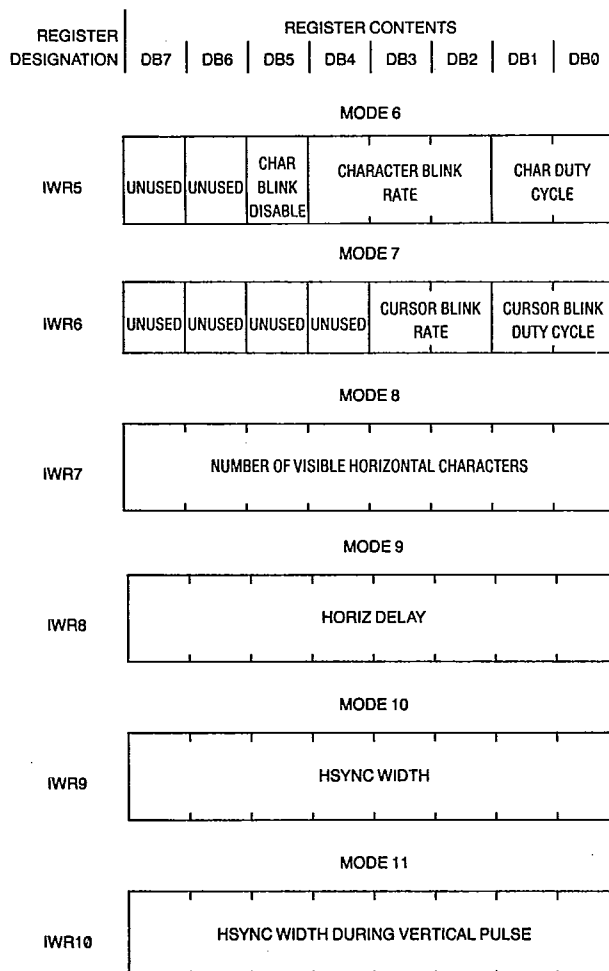
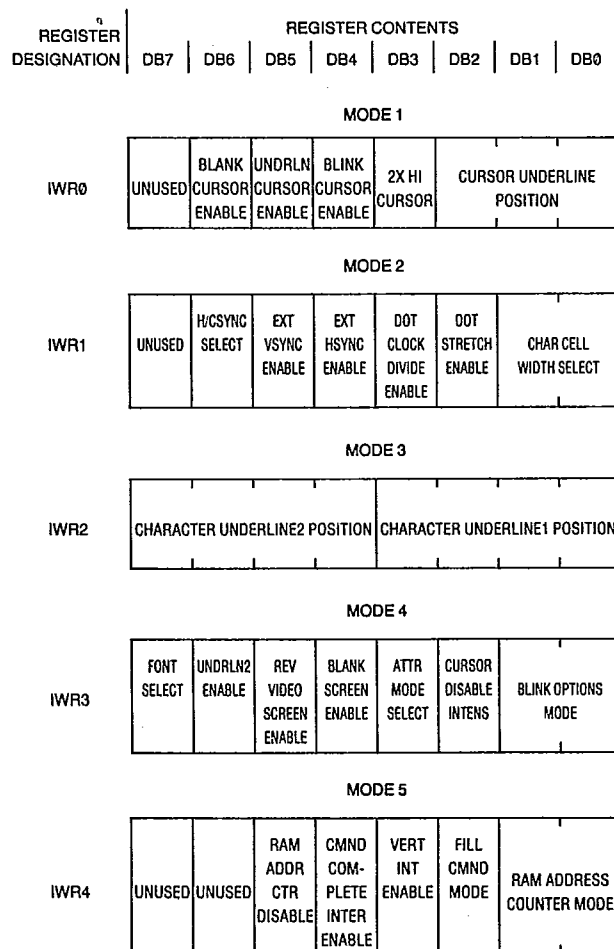


FIGURE 13, cont'd  
INDIRECT WRITE REGISTER FORMATS

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| REGISTER<br>DESIGNATION | REGISTER CONTENTS |     |     |     |     |     |     |     |
|-------------------------|-------------------|-----|-----|-----|-----|-----|-----|-----|
|                         | DB7               | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |

## MODE 12

|       |                        |  |  |  |  |  |  |  |
|-------|------------------------|--|--|--|--|--|--|--|
| IWR11 | HORIZONTAL LINE LENGTH |  |  |  |  |  |  |  |
|-------|------------------------|--|--|--|--|--|--|--|

## MODE 13

|       |                |  |  |  |  |  |  |  |
|-------|----------------|--|--|--|--|--|--|--|
| IWR12 | VERTICAL DELAY |  |  |  |  |  |  |  |
|-------|----------------|--|--|--|--|--|--|--|

## MODE 14

|       |                     |  |  |  |  |  |  |  |
|-------|---------------------|--|--|--|--|--|--|--|
| IWR13 | VERTICAL SYNC WIDTH |  |  |  |  |  |  |  |
|-------|---------------------|--|--|--|--|--|--|--|

## MODE 15

|       |                               |  |  |  |  |  |  |  |
|-------|-------------------------------|--|--|--|--|--|--|--|
| IWR14 | VERTICAL FRAME LENGTH 8 LSB's |  |  |  |  |  |  |  |
|-------|-------------------------------|--|--|--|--|--|--|--|

## MODE 16

|       |        |        |                                      |  |                                      |  |  |  |
|-------|--------|--------|--------------------------------------|--|--------------------------------------|--|--|--|
| IWR15 | UNUSED | UNUSED | MSB's OF<br>VERTICAL FRAME<br>LENGTH |  | NUMBER OF SCAN LINES<br>PER DATA ROW |  |  |  |
|-------|--------|--------|--------------------------------------|--|--------------------------------------|--|--|--|

## MODE 17

|       |                                        |  |  |  |  |  |  |  |
|-------|----------------------------------------|--|--|--|--|--|--|--|
| IWR16 | NUMBER OF VISIBLE DATA ROWS PER SCREEN |  |  |  |  |  |  |  |
|-------|----------------------------------------|--|--|--|--|--|--|--|

## CGEN MSB ADDRESS REGISTER

|       |     |     |    |    |    |    |    |    |
|-------|-----|-----|----|----|----|----|----|----|
| IWR17 | A11 | A10 | A9 | A8 | A7 | A6 | A5 | A4 |
|-------|-----|-----|----|----|----|----|----|----|

## CGEN LSB ADDRESS REGISTER

|       |        |        |        |        |    |    |    |    |
|-------|--------|--------|--------|--------|----|----|----|----|
| IWR18 | UNUSED | UNUSED | UNUSED | UNUSED | A3 | A2 | A1 | A0 |
|-------|--------|--------|--------|--------|----|----|----|----|

## CGEN MSB DATA REGISTER

|       |        |        |        |        |     |     |    |    |
|-------|--------|--------|--------|--------|-----|-----|----|----|
| IWR19 | UNUSED | UNUSED | UNUSED | UNUSED | C11 | C10 | C9 | C8 |
|-------|--------|--------|--------|--------|-----|-----|----|----|

## CGEN LSB DATA REGISTER

|       |    |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|----|
| IWR20 | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
|-------|----|----|----|----|----|----|----|----|

| REGISTER<br>DESIGNATION | REGISTER CONTENTS |     |     |     |     |     |     |     |
|-------------------------|-------------------|-----|-----|-----|-----|-----|-----|-----|
|                         | DB7               | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |

## TAG ATTRIBUTE REGISTER

|       |   |       |       |         |         |         |        |                     |
|-------|---|-------|-------|---------|---------|---------|--------|---------------------|
| IWR21 | 0 | BLINK | BLANK | INTEN 1 | INTEN 2 | REV VID | UNDRL1 | UNDRL2/<br>ALT FONT |
|-------|---|-------|-------|---------|---------|---------|--------|---------------------|

## HORIZONTAL CURSOR POSITION

|       |    |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|----|
| IWR22 | X7 | X6 | X5 | X4 | X3 | X2 | X1 | X0 |
|-------|----|----|----|----|----|----|----|----|

## VERTICAL CURSOR POSITION

|       |        |        |    |    |    |    |    |    |
|-------|--------|--------|----|----|----|----|----|----|
| IWR23 | UNUSED | UNUSED | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 |
|-------|--------|--------|----|----|----|----|----|----|

## FILL DATA REGISTER

|       |    |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|----|
| IWR24 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------|----|----|----|----|----|----|----|----|

## FILL COUNT REGISTER

|       |    |    |    |    |    |    |    |    |
|-------|----|----|----|----|----|----|----|----|
| IWR25 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|-------|----|----|----|----|----|----|----|----|

## RESERVED

|       |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|
| IWR26 |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|

## RESERVED

|       |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|
| IWR27 |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|

## RESET

|       |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|
| IWR28 |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|

## STOP

|       |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|
| IWR29 |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|

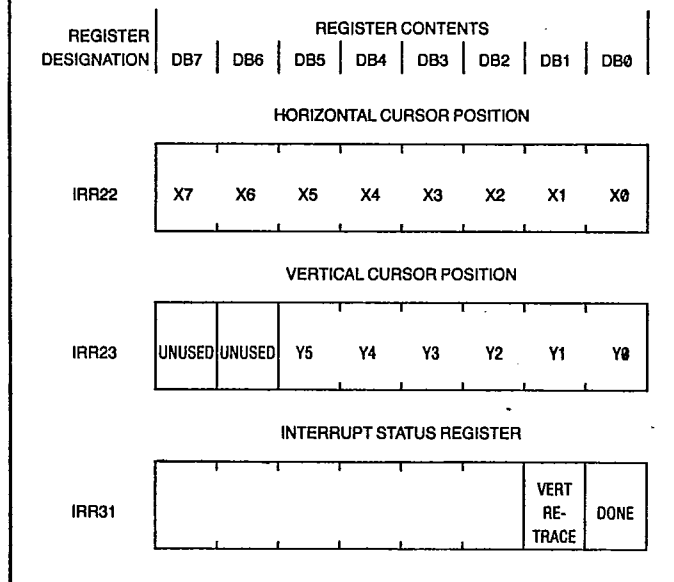
## START

|       |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|
| IWR30 |  |  |  |  |  |  |  |  |
|-------|--|--|--|--|--|--|--|--|

## COMMAND REGISTER

|       |      |      |      |        |        |        |                            |                              |
|-------|------|------|------|--------|--------|--------|----------------------------|------------------------------|
| IWR31 | TEST | TEST | TEST | UNUSED | UNUSED | UNUSED | FILL DM<br>TO END<br>OF DM | FILL DM<br>FOR FILL<br>COUNT |
|-------|------|------|------|--------|--------|--------|----------------------------|------------------------------|

**FIGURE 14**  
**INDIRECT READ REGISTER FORMATS**



## REGISTER DESCRIPTIONS

Figures 11 and 14 define the bit layouts for the Direct Read/Write Registers and the Indirect Read/Write Registers in address order. This section will provide descriptions of the registers in functional order. The registers can be divided into Timing, ATLC Control, Cursor Control, Attribute Control, Display Memory Interface, and Character Generator Memory Interface functions.

## I. TIMING

### MODE 2 (7 Bits—IWR1[6-0])—Write only.

After RESET only bits 4 and 5 are set—all other bits are not affected (reset.state equals xx11 xxxx). IWR1[7] is not used and should be programmed to 0.

#### Bit 6 (HSYNC/CSYNC Select)

When reset, this bit enables the HSYNC output on the H/CSYN signal. When set, the CSYNC output is enabled.

#### Bit 5 (External VSYNC Enable)

When reset, this bit enables the generation of the VSYNC signal from the internal clock source. When set, the VSYNC signal is synchronized to the signal provided on the VSYN input.

#### Bit 4 (External HSYNC Enable)

When reset, this bit enables the generation of the HSYNC signal from the internal clock source. When set, the HSYNC signal is synchronized to the signal provided on the H/CSYN input.

#### Bit 3 (Dot Clock Divide Enable)

When reset, this bit will disable the divide function allowing the clock to run at its maximum rate as determined by the crystal attached to the XTAL1-2 inputs or the direct TTL clock signal input on XTAL1. When set, this bit will cause the Dot Clock to be divided internally by a factor of 2/3. This feature is typically used to generate the dot rate required for an 80 character/data row display from a clock used to generate a 132 character/data row display. If a divide ratio other than 2/3 is required then external clock circuitry should be used with the divide function performed externally.

### Bit 2 (Dot Stretch Enable)

When reset, this bit enables the dot stretch attribute for the entire screen. When set, this attribute is disabled.

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### Bit 1-0 (Character Cell Width Select)

These two bits select the number of video dots displayed per character cell as defined in the following table.

| BIT 1 | BIT 0 | CELL WIDTH |
|-------|-------|------------|
| 0     | 0     | 9 DOTS     |
| 0     | 1     | 10 DOTS    |
| 1     | 0     | 11 DOTS    |
| 1     | 1     | 12 DOTS    |

### MODE 8 (8 Bits—IWR7[7-0])—Write only.

**CHARACTERS PER DATA ROW.** The contents of this register determines the number of visible characters per data row. The number programmed into this register should equal the number of visible characters per data row. See Figure 15 for the relationship between the horizontal timing and this register.

### MODE 9 (8 Bits—IWR8[7-0])—Write only.

**HORIZONTAL DELAY.** The contents of this register determines the time, in character clocks, between the leading edge of the horizontal sync pulse and the leading edge of the visible scan time. This register should be programmed with N-6 where N represents the actual number of character clocks in the Horizontal Delay period. The minimum value for this parameter is 6. See Figure 15 for the relationship between the horizontal timing and this register.

### MODE 10 (8 Bits—IWR9[7-0])—Write only.

**HORIZONTAL SYNC WIDTH.** The contents of this register determines the width of the horizontal sync pulse in character times. This register should be programmed with the actual desired value for the horizontal synch pulse width. See Figure 15 and 16 for the relationship between the horizontal timing and this register.

### MODE 11 (8 Bits—IWR10[7-0])—Write only.

**HORIZONTAL SYNC WIDTH FOR CSYNC.** The contents of this register determines the width of the horizontal sync pulse in character times during the vertical sync pulse period when the H/CSYN output is programmed for the CSYN output. This register should be programmed with the actual desired value for the horizontal sync pulse width. See Figure 16 for the relationship between the composite timing and this register.

### MODE 12 (8 Bits—IWR11[7-0])—Write only.

**CHARACTERS PER HORIZONTAL SCAN LINE.** The contents of this register determines the total number of character times in a horizontal scan line. This register should be programmed with N-1 where N is the total number of character times equal to the characters per data row plus the number of characters in the horizontal blanking period. See Figure 15 for the relationship between the horizontal timing and this register.

### MODE 13 (8 Bits—IWR12[7-0])—Write only.

**VERTICAL DELAY.** The contents of this register determines the time, in scan lines, between the leading edge of the vertical sync pulse and the leading edge of the visible frame time. This register should be programmed with N-1 where N represents the actual number of scan lines in the Vertical Delay period. See

Figure 17 for the relationship between the vertical timing and this register.

**MODE 14 (8 Bits—IWR13[7-0])—Write only.**

**VERTICAL SYNC WIDTH.** The contents of this register determines the width of the vertical sync pulse in scan line times. This register should be programmed with the actual desired value for the vertical sync pulse width. See Figure 17 for the relationship between the vertical timing and this register.

**MODE 15 (8 Bits—IWR14[7-0])—Write only.**

**SCAN LINES PER VERTICAL FRAME.** The contents of this register combined with two bits from IWR15 determines the total number of scan lines in the vertical frame. This register contains the 8 LSB's and the two bits of IWR15 contain the 2 MSB's and this value should be programmed with the actual value desired for the length of the vertical frame. See Figure 17 for the relationship between the vertical timing and this register.

**MODE 16 (6 Bits—IWR15[5-0])—Write only.**

IWR15[6-7] are not used and should be programmed to 00.

**Bit 5-4 (SCAN LINES PER VERTICAL FRAME)**

These two bits, as described above, define the 2 MSB's of the parameter which determines the total scan lines per vertical frame.

**Bit 3-0 (SCAN LINES PER DATA ROW)**

These 4 bits determine the total number of scan lines which define the height of a data row. This register should be programmed with N-1 where N is the number of scan lines per data row.

**MODE 17 (8 Bits—IWR16[7-0])—Write only.**

**VISIBLE DATA ROWS PER FRAME.** The contents of this register determines the total number of data rows that are displayed on the screen. This register should be programmed with N-1 where N represents the number of visible data rows. See Figure 17 for the relationship between the vertical timing and this register.

## II. ATLC CONTROL

**REGISTER POINTER (5 Bits—DWR0[4-0])—Write only.**

The contents of this register are used to indirectly address registers that are internal to the ATLC. After the Register Pointer is loaded, then either the DWR1 or DRR1 registers are addressed to access the contents of the indirect register. Bits 7 to 5 are not used and should be programmed to zero.

**INDIRECT REGISTER (8 Bits—DRR1[7-0]/DWR[7-0])—Read only.**

The contents of this register represents the contents of the indirect register pointed to by the Register Pointer.

**STATUS REGISTER (3 Bits—DRR0[7,1,0])—Read only.**

The contents of this register provide an indication of the status of pending interrupts and also the Busy Flag bit. Direct access to this register provides faster interaction between the ATLC and the processor. Reading this register will not reset the actual status bits in the Interrupt Status register.

**Bit 7 (ENABLED INTERRUPT PENDING)**

This bit is set when an enabled interrupt status bit (see Mode 5 register) in the Interrupt Status register is set.

**Bit 1 (VERTICAL RETRACE INTERRUPT)**

This bit is set when the ATLC begins to blank the video at the start of the vertical retrace period. This

bit will remain high throughout the vertical retrace period and it will go low at the end of vertical retrace. Reading this register will not affect the state of this bit.

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**Bit 0 (BUSY FLAG)**

This bit is set when the ATLC is performing a FILL command, a single character data or character attribute transfer to display memory, or writing to the Character Generator RAM. This bit is set at the start and reset after the completion of any of the above functions. Reading this register will not affect the state of this bit. This status bit cannot cause an interrupt to be generated.

**INTERRUPT STATUS REGISTER (2 Bits—IRR31[1-0])—Read only.**

The contents of this register provide an indication of the interrupt conditions that have occurred and that are enabled in the Mode 5 register. This register can be read at any time, but the contents are valid only when the Enabled Interrupt Pending bit in the Status Register is set. Reading this register will always clear the interrupts at the leading edge of the Read Strobe. The status bits will be cleared at the trailing edge of the Read Strobe.

**Bit 1 (VERTICAL RETRACE INTERRUPT)**

This bit will be set when the ATLC begins to blank the video at the start of the vertical retrace period. When enabled in the Mode 5 register, this condition will cause the ATLC to generate an interrupt. Reading this register will cause this bit to be reset.

**Bit 0 (DONE INTERRUPT)**

This bit will be set when the ATLC completes a FILL command. When enabled in the Mode 5 register, this condition will cause the ATLC to generate an interrupt. Reading this register will cause this bit to be reset.

**MODE 5 (6 Bits—IWR4[5-0])—Write only.**

IWR4[7-6] are not used and should be programmed to zero. After a RESET this register is set to a 00H.

**Bit 5 (RAM ADDRESS COUNTER DISABLE)**

When set, this bit disables the automatic incrementing or decrementing of the RAM Address counter. This will allow the processor to perform read-modify-write operations to display memory. When reset, the RAM Address counter will automatically increment or decrement based on the value programmed in bits 1-0 of this register.

**Bit 4 (VERTICAL RETRACE START INTERRUPT ENABLE)**

When set, this bit allows the ATLC to generate an interrupt when the VERTICAL RETRACE status bit (IRR3[1]) is set. When reset, the state of the VERTICAL RETRACE status bit cannot cause an external interrupt to be generated.

**Bit 3 (COMMAND COMPLETE INTERRUPT ENABLE)**

When set, this bit allows the ATLC to generate an interrupt when the DONE status bit (IRR3[0]) is set. When reset, the state of the DONE status bit cannot cause an interrupt to be generated.

**Bit 2 (FILL COMMAND MODE)**

When set, this bit causes the FILL command to fill both character and attribute locations with data. In this mode, when the RAM Address Register contents are even, writing data to the Character

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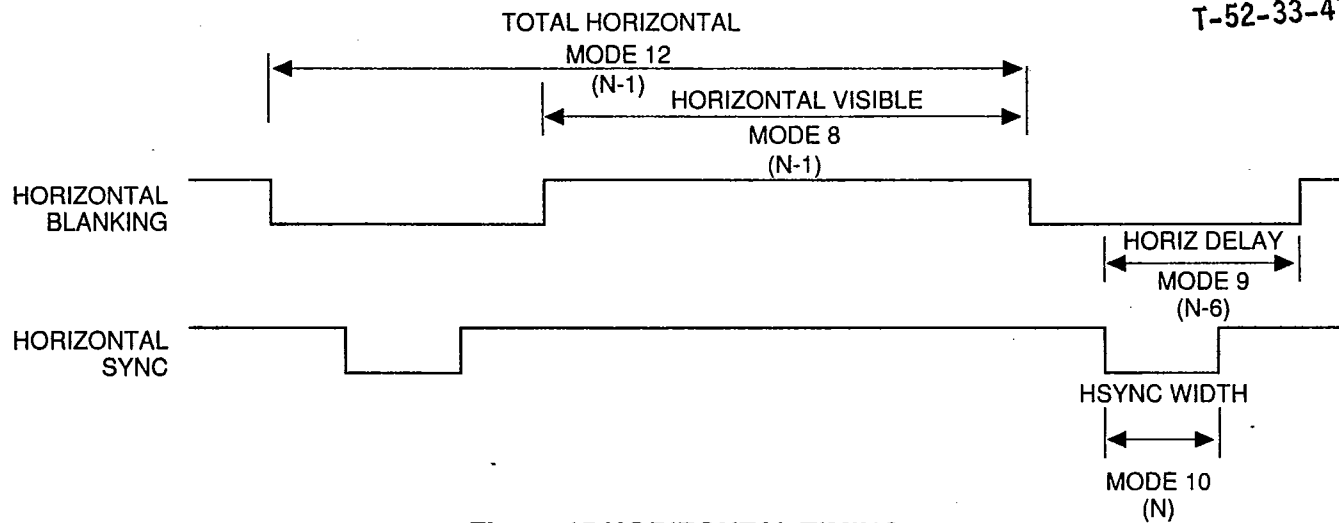


Figure 15 HORIZONTAL TIMING

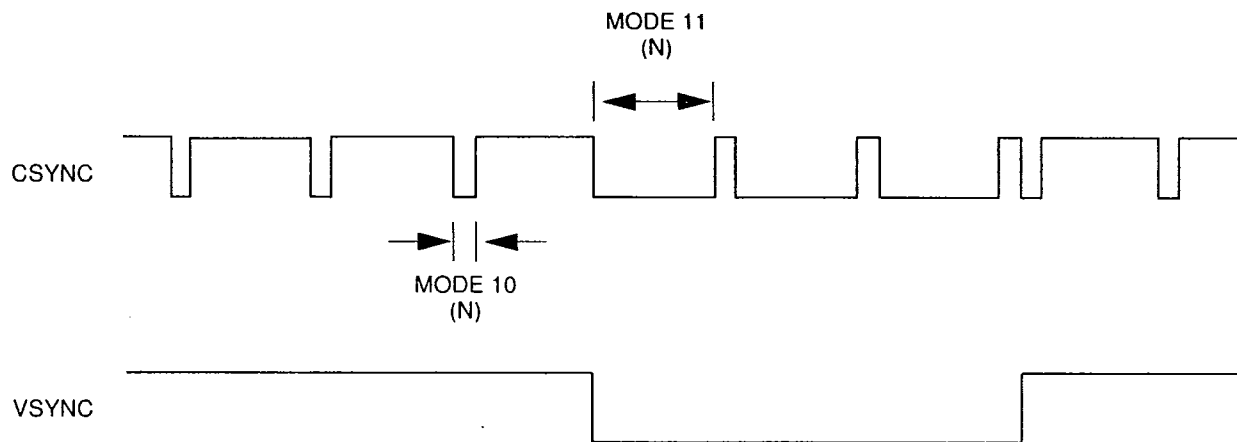
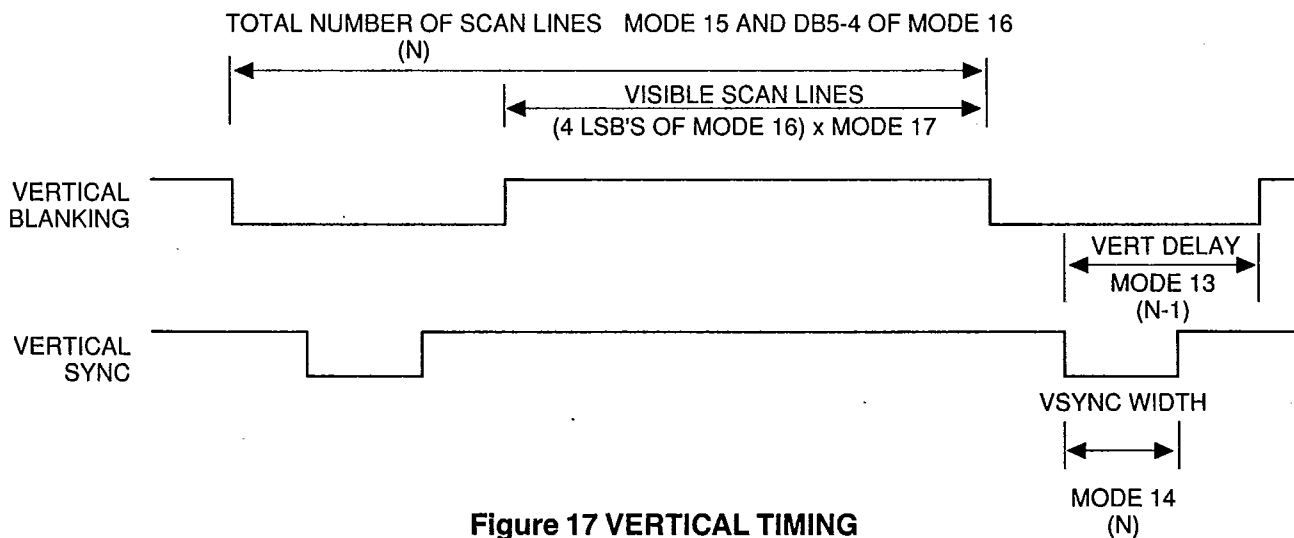
Figure 16  
COMPOSITE SYNC TIMING

Figure 17 VERTICAL TIMING

Register will result in both the new character data and the old character attribute to be written to the character and attribute memories respectively (2 bytes are written) upon execution of the FILL command. Similarly, when the RAM Address Register contents are odd, writing data to the Character Register will result in both the new character attribute and the old character data to be written to the attribute and character memories respectively upon execution of the FILL command. When reset, this bit causes the FILL command to write only the character data or character attribute bytes of the Character Register to the character or attribute memories respectively.

#### Bit 1-0 (RAM ADDRESS COUNTER MODE)

These 2 bits determine whether the ATLC will increment or decrement the RAM Address counter by one or two. The RAM Address Counter will automatically be incremented/decremented after each transfer of data between the ATLC and Display RAM. Display Attribute RAM is accessed for all odd addresses and Display Character RAM is accessed for all even addresses. The least significant bit of the Display Memory Address is not output, however, it is decoded internally and output as the DCWE, DAW, and the DOE signals. The following table defines the four modes—

| BIT 1 | BIT 0 | MODE                |
|-------|-------|---------------------|
| 0     | 0     | Auto-increment by 1 |
| 0     | 1     | Auto-increment by 2 |
| 1     | 0     | Auto-decrement by 1 |
| 1     | 1     | Auto-decrement by 2 |

#### RESET REGISTER (0 Bits—IWR28[ ])—Write only.

The contents of this register are not accessible. The RESET command is initiated by addressing this dummy register. This command will cause the ATLC to stop generation of display memory addresses and to reset its raster counters. The Register Pointer will be set to 00H. Character Clock will continue to be output. The following identifies the states assumed by the signals listed—

|           |                    |
|-----------|--------------------|
| H/CSYN    | Input (HSYN)       |
| VSYN      | Input              |
| INTOUT1   | 0                  |
| INTOUT2   | 0                  |
| INTER     | 0                  |
| CCLK      | Free running clock |
| DD15-0    | Outputs            |
| DCWE, DAW | 1                  |
| DOE       | 1                  |
| CGD11-0   | Inputs             |
| CWE, COE  | 1                  |
| ALTFS     | Value of IWR3[7]   |
| SL3-0     | 0                  |

#### STOP REGISTER (0 Bits—IWR29)—Write only.

The contents of this register are not accessible. The STOP command is initiated by addressing this dummy register. This command will not affect the raster counters (H/SYN and VSYN will continue to be generated) but the video will be blanked. Character Clock will continue to be output. The following identifies the states assumed by the signals listed—

|         |                              |
|---------|------------------------------|
| H/CSYN  | In accordance with IWR1[6-5] |
| VSYN    | In accordance with IWR1[4]   |
| INTOUT1 | 0                            |

|           |                                           |            |
|-----------|-------------------------------------------|------------|
| INTOUT2   | 0                                         | T-52-33-47 |
| INTER     | 0                                         |            |
| CCLK      | Free running clock                        |            |
| DD15-0    | Outputs                                   |            |
| DCWE, DAW | 1                                         |            |
| DOE       | 1                                         |            |
| CGD11-0   | Inputs                                    |            |
| CWE, COE  | 1                                         |            |
| ALTFS     | Value of IWR3[7]                          |            |
| SL3-0     | 0                                         |            |
| VIDEO     | Mask programmed background blanking level |            |

#### START REGISTER (0 Bits—IWR30)—Write only.

The contents of this register are not accessible. The START command is initiated by addressing this dummy register. Following a RESET or STOP command, this command will cause the ATLC to initiate all operations and activate all its outputs.

#### COMMAND REGISTER (2 Bits—IWR31[1-0])—Write only. IWR31[7-2] are not used and should be programmed to 0.

##### Bit 1 (FILL DISPLAY MEMORY TO END OF RAM)

This command is initiated by writing a 1 to this bit. This command will cause the ATLC to fill display memory from the current RAM Address Register location down to RAM address 0000H or 0001H depending on setting of IWR4[1-0].

##### Bit 0 (FILL DISPLAY MEMORY FOR FILL COUNT)

This command is initiated by writing a 1 to this bit. This command will cause the ATLC to fill display memory from the current RAM Address Register location for the number of locations specified in the Fill Count Register (IWR24).

### III. CURSOR CONTROL

#### HORIZONTAL CURSOR POSITION (8 Bits—IWR22/IRR22[7-0])—Read/Write.

The contents of this register specifies the character position within a row at which the cursor appears. This register combined with the contents of the Vertical Cursor Position register uniquely locates the cursor using an X-Y format independent of the display location where the character data is stored.

#### VERTICAL CURSOR POSITION (8 Bits—IWR23/IRR23[5-0])—Read/Write.

The contents of this register specifies the character row in which the cursor appears. This register combined with the contents of the Horizontal Cursor Position register uniquely locates the cursor using an X-Y format independent of the display memory location where the character data is stored.

#### MODE 1 (7 Bits—IWR0[6-0])—Write only.

IWR0[7] is not used and should be programmed to 0.

##### Bit 6 (BLANK CURSOR ENABLE)

When set, this bit causes the cursor to be blanked to the background level. When reset, this bit allows the cursor to be displayed.

##### Bit 5 (UNDERLINE CURSOR ENABLE)

When set, this bit causes an underline cursor to be displayed on the programmed scan line (see Bits 2-0). When reset, this bit will cause a block cursor to be displayed.

##### Bit 4 (BLINK CURSOR ENABLE)

When set, this bit will cause the cursor to blink at the programmed rate and duty cycle (see IWR6). When reset, this bit will cause a steady cursor to be displayed.

##### Bit 3 (DH/DW CURSOR ENABLE)

When set, this bit allows a cursor to be displayed as double high/double wide in the top and bottom half of a data row which has been assigned a double high/double wide attribute. When reset, then the cursor will always be single height in any data row that it appears. The cursor will be double wide only if the data row it is in has been assigned a single high/double wide attribute.

#### Bit 2-0 (CURSOR UNDERLINE POSITION)

These bits select the scan line on which an underline cursor will appear.

| BIT 2 | BIT 1 | BIT 0 | SCAN LINE |
|-------|-------|-------|-----------|
| 0     | 0     | 0     | SL 8      |
| 0     | 0     | 1     | SL 9      |
| 0     | 1     | 0     | SL 10     |
| 0     | 1     | 1     | SL 11     |
| 1     | 0     | 0     | SL 12     |
| 1     | 0     | 1     | SL 13     |
| 1     | 1     | 0     | SL 14     |
| 1     | 1     | 1     | SL 15     |

#### MODE 7 (4 Bits—IWR6[3-0])—Write only.

##### Bit 3-2 (CURSOR BLINK RATE)

These 2 bits determine the rate at which the cursor will blink. The actual rate is determined by the Character Blink Rate and the value programmed here.

| BIT 3 | BIT 2 | CURSOR BLINK RATE              |
|-------|-------|--------------------------------|
| 0     | 0     | Twice the character blink rate |
| 0     | 1     | Same as character blink rate   |
| 1     | 0     | Half of character blink rate   |
| 1     | 1     | Not used                       |

##### Bit 1-0 (CURSOR BLINK DUTY CYCLE)

These 2 bits determine the duty cycle of the blinking cursor. The numbers listed in the table below identify the percentage of time that the cursor is OFF and the percentage of time that the cursor is ON.

| BIT 1 | BIT 0 | CURSOR BLINK DUTY CYCLE (OFF/ON) |
|-------|-------|----------------------------------|
| 0     | 0     | 50/50                            |
| 0     | 1     | 25/75                            |
| 1     | 0     | 75/25                            |
| 1     | 1     | Not used                         |

## IV. ATTRIBUTE CONTROL

#### MODE 3 (8 Bits—IWR2[7-0])—Write only.

##### Bit 7-4 (CHARACTER UNDERLINE2 POSITION)

##### Bit 3-0 (CHARACTER UNDERLINE1 POSITION)

These bits select independently the scan lines on which the two character underline attributes will appear. If Underline2 Enable (IWR3[6]) is reset, then underline 2 is disabled and bits 7-4 of this register are ignored.

| BIT 7<br>BIT 3 | BIT 6<br>BIT 2 | BIT 5<br>BIT 1 | BIT 4<br>BIT 0 | SCAN LINE |
|----------------|----------------|----------------|----------------|-----------|
| 0              | 0              | 0              | 0              | SL 0      |
| 0              | 0              | 0              | 1              | SL 1      |
| 0              | 0              | 1              | 0              | SL 2      |
| 0              | 0              | 1              | 1              | SL 3      |
| 0              | 1              | 0              | 0              | SL 4      |
| 0              | 1              | 0              | 1              | SL 5      |
| 0              | 1              | 1              | 0              | SL 6      |
| 0              | 1              | 1              | 1              | SL 7      |
| 1              | 0              | 0              | 0              | SL 8      |

| BIT 7<br>BIT 3 | BIT 6<br>BIT 2 | BIT 5<br>BIT 1 | BIT 4<br>BIT 0 | SCAN LINE |
|----------------|----------------|----------------|----------------|-----------|
| 1              | 0              | 0              | 1              | SL 9      |
| 1              | 0              | 1              | 0              | SL 10     |
| 1              | 0              | 1              | 1              | SL 11     |
| 1              | 1              | 0              | 0              | SL 12     |
| 1              | 1              | 0              | 1              | SL 13     |
| 1              | 1              | 1              | 0              | SL 14     |
| 1              | 1              | 1              | 1              | SL 15     |

#### MODE 4 (8 Bits—IWR3[7-0])—Write only.

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##### Bit 7 (FONT SELECT)

When the Underline2 Enable mode bit (IWR3[6]) is set, the ALTFS output (pin 73) will reflect the state of this bit. When the Underline2 Enable mode bit is reset, this bit is ignored and the ALTFS output is controlled by the state of the Underline2/Alternate Font Select attribute bit (see the Attributes section of the Functional Description).

##### Bit 6 (UNDERLINE2 ENABLE)

When set, the Underline2 attribute for a given character is controlled by the appropriate Underline2/Alternate Font Select Parallel or Tag attribute bit. When reset, the Underline2 attribute is disabled and the Underline2/Alternate Font Select attribute bit will be output on the ALTFS signal (pin 73). The following table summarizes the effect of bits 6 and 7 of this register on the Underline2 attribute and on the ALTFS output signal.

| BIT 6 | BIT 7 | UNDERLINE2 ATTR             | ALTFS OUTPUT                |
|-------|-------|-----------------------------|-----------------------------|
| 0     | 0     | Disabled                    | Controlled by attribute bit |
| 0     | 1     | Disabled                    | Controlled by attribute bit |
| 1     | 0     | Controlled by attribute bit | 0                           |
| 1     | 1     | Controlled by attribute bit | 1                           |

##### Bit 5 (REVERSE VIDEO SCREEN ENABLE)

When set, this bit causes the entire active display area of the screen to be reverse video. When reset, this function is disabled.

##### Bit 4 (BLANK SCREEN ENABLE)

When set, this bit forces the VIDEO signal output to the background level for the entire active display area on the screen. When reset, this function is disabled.

##### Bit 3 (ATTRIBUTE MODE)

When set, this bit enables the Tag attribute mode. When reset, this bit enables the Parallel attribute mode.

##### Bit 2 (CURSOR DISABLE INTENSITY)

This bit determines how the cursor will affect the intensity attributes of a character when one of the two 9041 attribute modes is active (IWR3[0] = 0). It has no effect when the 9021 attribute mode is active (IWR3[0] = 1). When set, this bit will cause the intensity outputs (pins 70 and 71) to be disabled (forced to 0) for all programmed cursor scan lines. Thus any character with a cursor on it will not blink since blinking occurs only between intensities. When reset, the cursor will have no effect on the intensity output signals.

**Bit 1-0 (BLINK OPTIONS MODE)**

These 2 bits select one of three modes for the blinking of characters as defined in the table below. Two of the options emulate the modes offered by the CRT9041 and one option emulates the CRT9021. See the Attributes section of the Functional Description for a description of these blink modes.

| BIT 1 | BIT 0 | BLINK OPTIONS MODE |
|-------|-------|--------------------|
| 0     | 0     | TABLE 1            |
| 0     | 1     | TABLE 2            |
| 1     | 0     | TABLE 3            |
| 1     | 1     | NOT USED           |

**MODE 6 (6 Bits—IWR5[5-0])—Write only.****Bit 5 (CHARACTER BLINK DISABLE)**

When set, this bit disables the character blink attribute for all characters on screen. Specific blink character attributes that are set do not have to be modified. When this bit is reset, those characters with the blink attribute set will exhibit the blink attribute.

**Bit 4-2 (CHARACTER BLINK RATE)**

These 3 bits determine the rate at which the character will blink. The actual rate is determined by dividing the vertical refresh rate (frequency at which screen is refreshed) by the number selected in the table below.

| BIT 4 | BIT 3 | BIT 2 | BLINK RATE DIVIDER |
|-------|-------|-------|--------------------|
| 0     | 0     | 0     | 8                  |
| 0     | 0     | 1     | 16                 |
| 0     | 1     | 0     | 32                 |
| 0     | 1     | 1     | 64                 |
| 1     | 0     | 0     | 128                |
| 1     | 0     | 1     | UNUSED             |
| 1     | 1     | 0     | UNUSED             |
| 1     | 1     | 1     | UNUSED             |

**Bit 1-0 (CHARACTER BLINK DUTY CYCLE)**

These 2 bits determine the duty cycle of blinking characters. The numbers listed in the table below identify the percentage of time that the character is OFF and the percentage of time that the character is ON.

| BIT 1 | BIT 0 | CHARACTER BLINK DUTY CYCLE (OFF/ON) |
|-------|-------|-------------------------------------|
| 0     | 0     | 50/50                               |
| 0     | 1     | 25/75                               |
| 1     | 0     | 75/25                               |
| 1     | 1     | Not used                            |

**TAG ATTRIBUTE REGISTER (7 Bits—IWR21[6-0])—Write only.**

The contents of this register identifies the active attributes to be used in the Tag Attribute mode. The attributes controlled by this register are listed below and each is activated by setting the appropriate bit. See the Attributes section of the Functional Description for more details. IWR21[7] is not used and should be programmed to 0.

- IWR21[6]—Blink
- IWR21[5]—Blank
- IWR21[4]—Intensity 1
- IWR21[3]—Intensity 2
- IWR21[2]—Reverse Video
- IWR21[1]—Underline 1
- IWR21[0]—Underline 2/Alternate Font Select

**V. DISPLAY MEMORY INTERFACE****CHARACTER REGISTER (8 Bits—DWR2/DDR2[7-0])—Read/Write.**

This register is used to store either character data and/or character attribute bytes that are being transferred between display memory and the system processor. Writing to or reading from the Character Register will cause the ATLC to set the BUSY status bit and to initiate the transfer of data with the display memory location pointed to by the RAM Address Register. If the RAM Address Register contains an even address then the character data byte is being accessed. If the RAM Address Register contains an odd address then the character attribute byte is being accessed.

**RAM ADDRESS REGISTER (16 Bits—DWR3/DDR3[15-0])—Read/Write.**

This register is used to store the display memory address for data transfers between display memory and the system processor and for FILL operations. Two bytes must always be read from or written to this location, least significant byte first.

**FILL DATA REGISTER (8 Bits—IWR24[7-0])—Write only.**

This register provides indirect access to the Character Registers. It is used in FILL operations. Character data and/or attribute bytes are written to this register before the FILL command is issued. If both character data and attribute are to be transferred, then the first byte loaded should be the character attribute and the second byte loaded should be the character data. Writing to the Fill Data Register will not cause the ATLC to initiate any action. See the Fill Operations section under Functional Description for more detail.

**FILL COUNT REGISTER (8 Bits—IWR25[7-0])—Write only.**

The contents of this register determines the number of character data and/or attribute bytes that will be filled during a FILL operation. If N bytes/words are to be filled then the register should be programmed with N. The only exception is the value 0 which will result in the fill of 256 byte/word locations. See the Command Register.

**VI. CHARACTER GENERATOR MEMORY INTERFACE****CHGEN MSB ADDRESS REGISTER (8 Bits—IWR17[7-0])—Write only.**

The contents of this register holds the MSB's of the Character Generator Memory Address for transferring character generator data to the external Character Generator RAM. The contents of this register are output on the DD7-0 (pins 42-35) bits of the Display Memory Data bus and are latched in an external latch after writing to any of the CHGEN registers. These bits will be output on the DD7-0 pins until the ATLC receives a RESET, START, or STOP command. Any of these commands will cause the DD7-0 pins to return to their normal function. This register should be written to only after a RESET or STOP command.

**CHGEN LSB ADDRESS REGISTER (4 Bits—IWR18[3-0])—Write only.**

The contents of this register holds the 4 LSB's of the Character Generator Memory Address for transferring the character generator data to the external Character Generator RAM. These bits are output on the SL3-0 (pins 8-10, 14) signals. Following the first write to any CHGEN register, the contents of this register will be output on the SL3-0 pins until the ATLC receives a RESET, START, or STOP command.

**CHGEN MSB DATA REGISTER** (4 Bits—IWR19[3-0])—  
Write only.

**CHGEN LSB DATA REGISTER** (8 Bits—IWR20[7-0])—  
Write only.

The contents of these two registers hold the character generator dot pattern to be transferred to the external Character Generator RAM. Writing to any CHGEN register will cause the contents of these registers to be output on the CGD11-0 (pins 56-63, 65-68) signals and to be written into the Character Generator RAM. The mapping of these two registers to the CGDxx outputs are listed below—

|                |               |
|----------------|---------------|
| CGD11—IWR20[0] | CGD3—IWR19[0] |
| CGD10—IWR20[1] | CGD2—IWR19[1] |
| CGD9—IWR20[2]  | CGD1—IWR19[2] |
| CGD8—IWR20[3]  | CGD0—IWR19[3] |
| CGD7—IWR20[4]  |               |
| CGD6—IWR20[5]  |               |
| CGD5—IWR20[6]  |               |
| CGD4—IWR20[7]  |               |

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IWR20[0]/CGD11 will be the first bit shifted out of the internal video shift register during the output of the VIDEO signal. This register should only be written to after a RESET or STOP command.

### MAXIMUM GUARANTEED RATINGS\*

|                                          |                       |
|------------------------------------------|-----------------------|
| Operating Temperature Range              | .....0°C to +70°C     |
| Storage Temperature Range                | .....-55°C to +150°C  |
| Lead Temperature (Soldering, 10 sec)     | .....+300°C           |
| Positive voltage on any pin (WRT ground) | ..... $V_{cc} + 0.3V$ |
| Negative voltage on any pin (WRT ground) | .....-0.3V            |
| Maximum $V_{cc}$                         | .....+7.0V            |

\*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

### DC ELECTRICAL CHARACTERISTICS $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ , $V_{cc} = 5.0V \pm 5\%$

| SYMBOL    | PARAMETER              | MIN. | TYP | MAX | UNITS   |                           |
|-----------|------------------------|------|-----|-----|---------|---------------------------|
| $V_{IL}$  | Input voltage:         |      |     |     | V       |                           |
| $V_H$     | Low                    |      |     | 0.8 | V       |                           |
| $V_{IL}$  | High                   | 2.0  |     |     | V       |                           |
| $V_H$     | Low                    |      |     | 1.0 | V       | TTL drive on XTAL1 input. |
| $V_H$     | High                   | 4.0  |     |     | V       | TTL drive on XTAL1 input. |
| $V_{OL}$  | Output voltage:        |      |     |     | V       |                           |
| $V_{OH}$  | Low                    |      |     | 0.4 | V       | $I_{DL} = 1.6 \mu A$      |
|           | High                   | 2.4  |     |     | V       | $I_{DM} = -40 \mu A$      |
| $I_{IL}$  | Input leakage current: |      |     | 10  | $\mu A$ |                           |
| $I_{IH}$  |                        |      |     | 10  | $\mu A$ |                           |
| $C_N$     | Input capacitance:     |      |     | 25  | pF      | All inputs                |
| $C_{OUT}$ |                        |      |     | 50  | pF      |                           |
| $I_{cc}$  | Power supply current:  |      |     | 50  | mA      |                           |

NOTES: 1. The  $V_{IM}$  MIN and  $V_{IL}$  MAX of XTAL1 input is 80% and 20% of  $V_{cc}$  respectively.

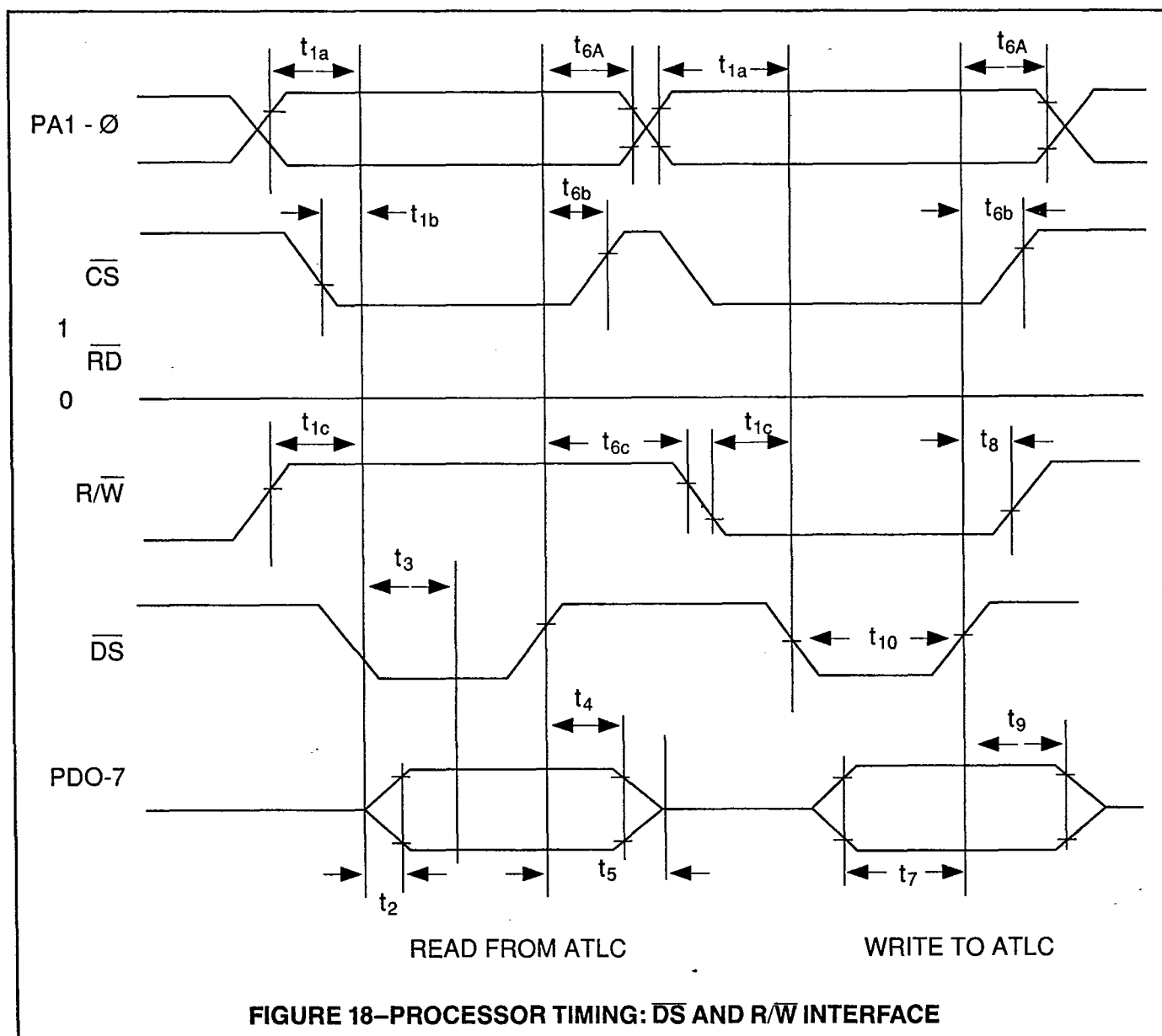
**PRELIMINARY**  
Notice: This is not a final specification.  
Some parametric limits are subject to change.

## AC ELECTRICAL CHARACTERISTICS

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| SYMBOL                                                                                          | PARAMETER                                              | MIN | TYP | MAX  | UNITS |
|-------------------------------------------------------------------------------------------------|--------------------------------------------------------|-----|-----|------|-------|
| $f_{OT}$                                                                                        | Clock frequency                                        |     |     | 42.0 | MHz   |
| <b>Processor Timing: <math>\overline{DS}</math> and R/W Interface<sup>1</sup> (See Fig. 18)</b> |                                                        |     |     |      |       |
| $t_{1a}$                                                                                        | PA1- $\emptyset$ valid to $\overline{DS}$ falling edge | 30  |     |      | ns    |
| $t_{1b}$                                                                                        | $\overline{CS}$ active to $\overline{DS}$ falling edge | 0   |     |      | ns    |
| $t_{1c}$                                                                                        | R/W valid to $\overline{DS}$ falling edge              | 30  |     |      | ns    |
| $t_2$                                                                                           | $\overline{DS}$ falling edge to data bus Lo Z          | 0   |     |      | ns    |
| $t_3$                                                                                           | $\overline{DS}$ falling edge to read data valid        |     |     | 130  | ns    |
| $t_4$                                                                                           | Read data hold from $\overline{DS}$ rising edge        | 30  |     |      | ns    |
| $t_5$                                                                                           | $\overline{DS}$ rising edge to data bus Hi Z           |     |     | 35   | ns    |
| $t_{6a}$                                                                                        | PA1- $\emptyset$ hold from $\overline{DS}$ rising edge | 35  |     |      | ns    |
| $t_{6b}$                                                                                        | $\overline{CS}$ hold from $\overline{DS}$ rising edge  | 0   |     |      | ns    |
| $t_{6c}$                                                                                        | R/W hold from $\overline{DS}$ rising edge              | 0   |     |      | ns    |
| $t_7$                                                                                           | Data setup to $\overline{DS}$ rising edge              | 100 |     |      | ns    |
| $t_8$                                                                                           | R/W hold from $\overline{DS}$ rising edge              | 0   |     |      | ns    |
| $t_9$                                                                                           | Write data hold from $\overline{DS}$ rising edge       | 30  |     |      | ns    |
| $t_{10}$                                                                                        | $\overline{DS}$ pulse width (write)                    | 100 |     |      | ns    |

NOTE: 1. Reference points are 2.4V high and 0.4V low.

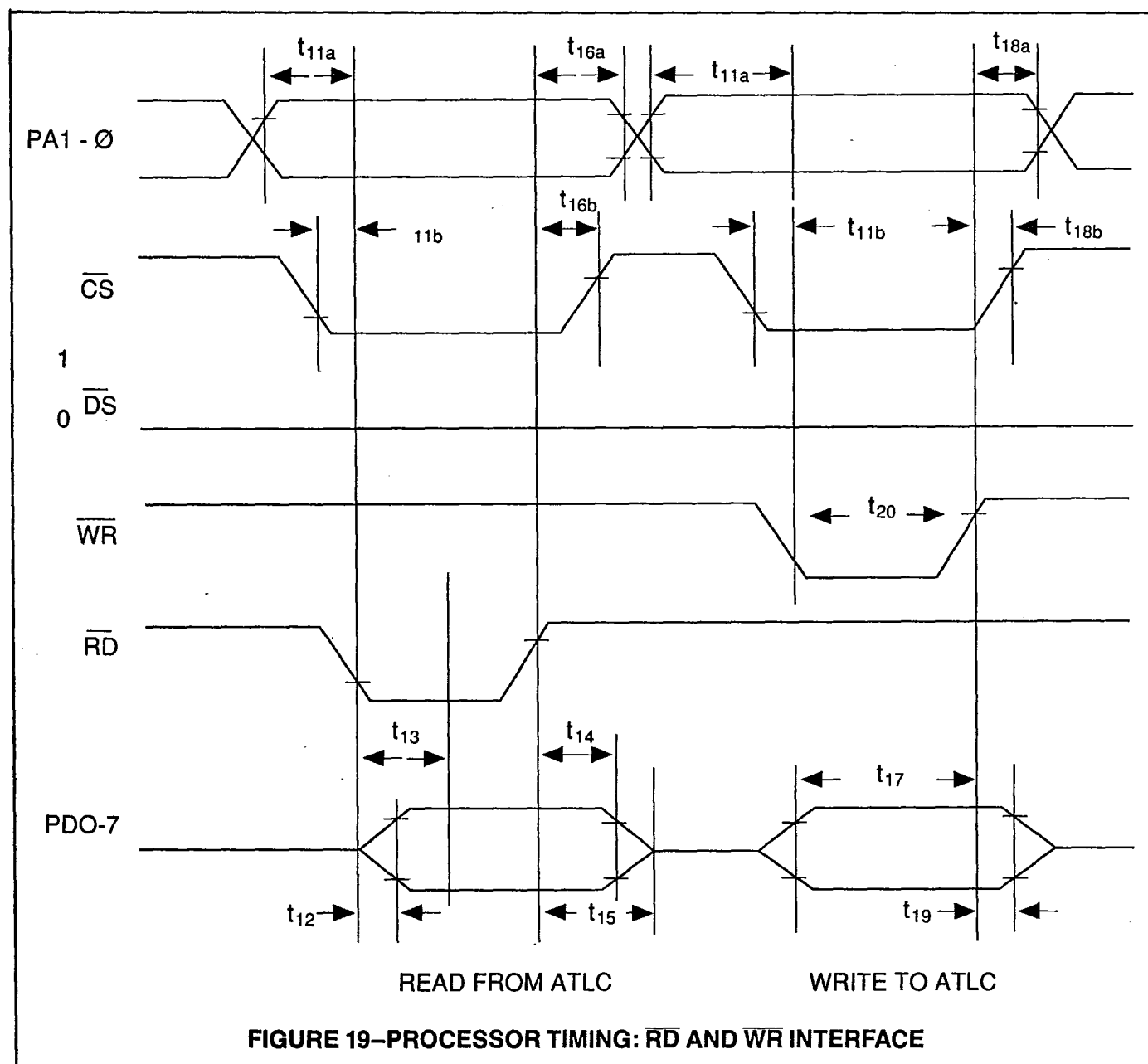


## AC ELECTRICAL CHARACTERISTICS

T-52-33-47

| SYMBOL                                                                                                                 | PARAMETER                                                                 | MIN | TYP | MAX | UNITS |
|------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|-----|-----|-----|-------|
| <b>Processor Timing: <math>\overline{RD}</math> and <math>\overline{WR}</math> Interface<sup>1</sup> (See Fig. 19)</b> |                                                                           |     |     |     |       |
| $t_{11a}$                                                                                                              | PA1- $\emptyset$ valid to $\overline{RD}$ or $\overline{WR}$ falling edge | 30  |     |     | ns    |
| $t_{11b}$                                                                                                              | $\overline{CS}$ active to $\overline{RD}$ or $\overline{WR}$ falling edge | 0   |     |     | ns    |
| $t_{12}$                                                                                                               | $\overline{RD}$ falling edge to data bus Lo Z                             | 0   |     |     | ns    |
| $t_{13}$                                                                                                               | $\overline{RD}$ falling edge to read data valid                           |     |     | 130 | ns    |
| $t_{14}$                                                                                                               | Read data hold from $\overline{RD}$ rising edge                           | 30  |     |     | ns    |
| $t_{15}$                                                                                                               | $\overline{RD}$ rising edge to data bus Hi Z                              |     |     | 35  | ns    |
| $t_{16a}$                                                                                                              | PA1- $\emptyset$ hold from $\overline{RD}$ rising edge                    | 0   |     |     | ns    |
| $t_{16b}$                                                                                                              | $\overline{CS}$ hold from $\overline{RD}$ rising edge                     | 0   |     |     | ns    |
| $t_{17}$                                                                                                               | Data setup to $\overline{WR}$ rising edge                                 | 100 |     |     | ns    |
| $t_{18a}$                                                                                                              | PA1- $\emptyset$ hold from $\overline{WR}$ rising edge                    | 0   |     |     | ns    |
| $t_{18b}$                                                                                                              | $\overline{CS}$ hold from $\overline{WR}$ rising edge                     | 0   |     |     | ns    |
| $t_{19}$                                                                                                               | Write data hold from $\overline{WR}$ rising edge                          | 30  |     |     | ns    |
| $t_{20}$                                                                                                               | $\overline{WR}$ pulse width                                               | 100 |     |     | ns    |

NOTE: 1. Reference points are 2.4V high and 0.4V low.



| SYMBOL                                           | PARAMETER                                             | MIN | TYP | MAX                                    | UNITS |
|--------------------------------------------------|-------------------------------------------------------|-----|-----|----------------------------------------|-------|
| <b>Character Generator Timing' (See Fig. 20)</b> |                                                       |     |     |                                        |       |
| $t_{21}$                                         | $\overline{CWE}$ pulse width (See notes 2 & 3)        |     |     | $(\# \text{ Dots}^2-3) \cdot t_{cy}^3$ | ns    |
| $t_{22}$                                         | Data setup to $\overline{CWE}$ rising edge            |     |     | $3 \cdot t_{cy}^3$                     | ns    |
| $t_{23}$                                         | Font data hold from $\overline{CWE}$ rising edge      |     |     | Note 4                                 | ns    |
| $t_{24}$                                         | Scan line addr to $\overline{CWE}$ falling edge       |     |     | $3 \cdot t_{cy}^3$                     | ns    |
| $t_{25}$                                         | Scan line addr hold from $\overline{CWE}$ rising edge |     |     | Note 4                                 | ns    |
| $t_{26}$                                         | CCLK rising edge to $\overline{CWE}$ falling edge     |     |     | $3 \cdot t_{cy}^3$                     | ns    |
| $t_{27}$                                         | Font data setup to CCLK rising edge                   | 35  |     |                                        | ns    |
| $t_{28}$                                         | Font data hold from CCLK rising edge                  | 0   |     |                                        | ns    |
| $t_{29}$                                         | CCLK rising edge to $\overline{COE}$ falling edge     |     | TBD |                                        |       |
| $t_{30}$                                         | CCLK rising edge to FONTSEL rising edge               |     | TBD |                                        |       |

NOTES: 1. Reference points are 2.4V high and 0.4V low.

2. # Dots is determined by programming of IWR[1-0].

3.  $t_{cy} = 1/f_{DOR}$ .

4. Scan line data (SL3-0) and font data (CGD11-0) will remain active at the outputs until the next data write (see Section on External Character Generator in Functional Description.)

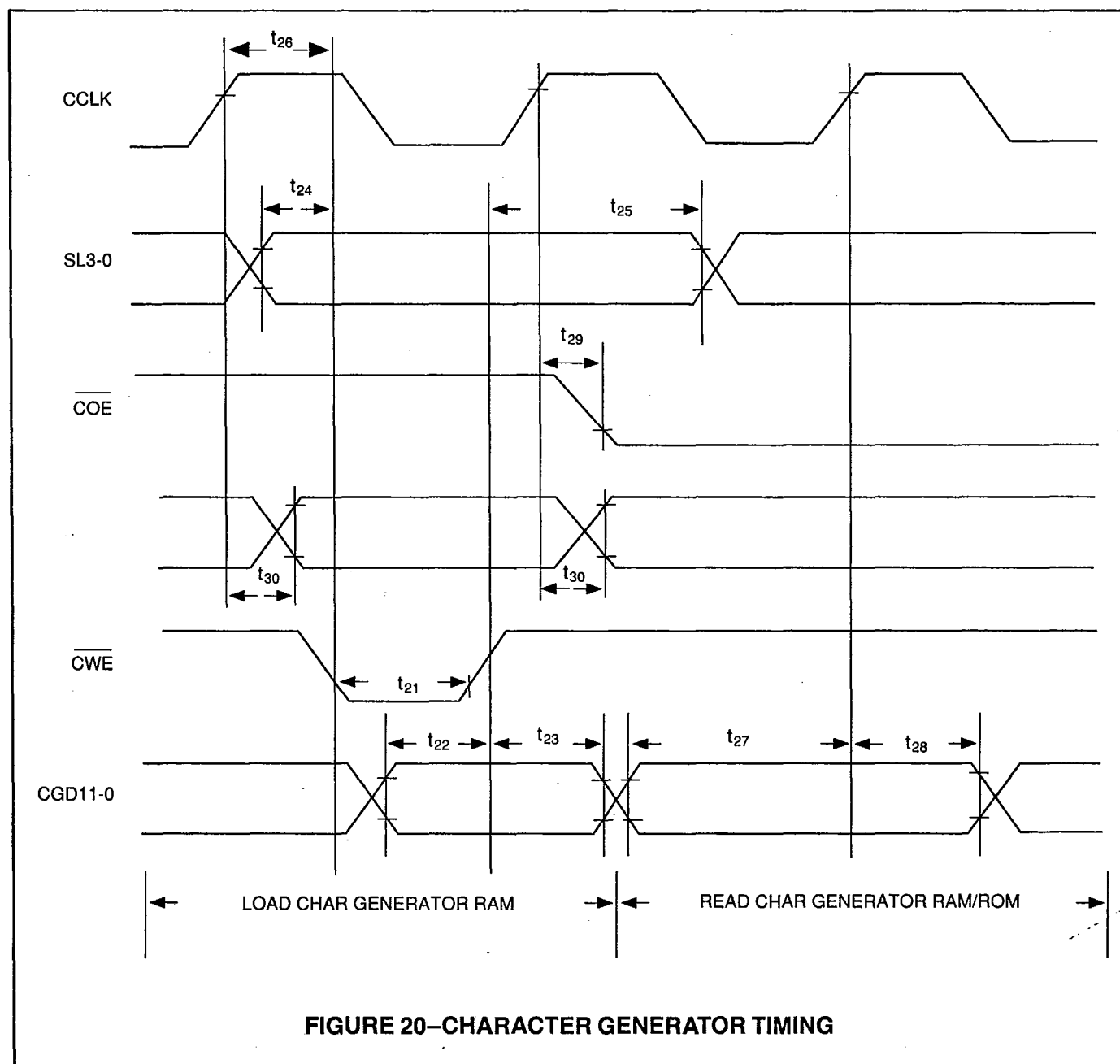
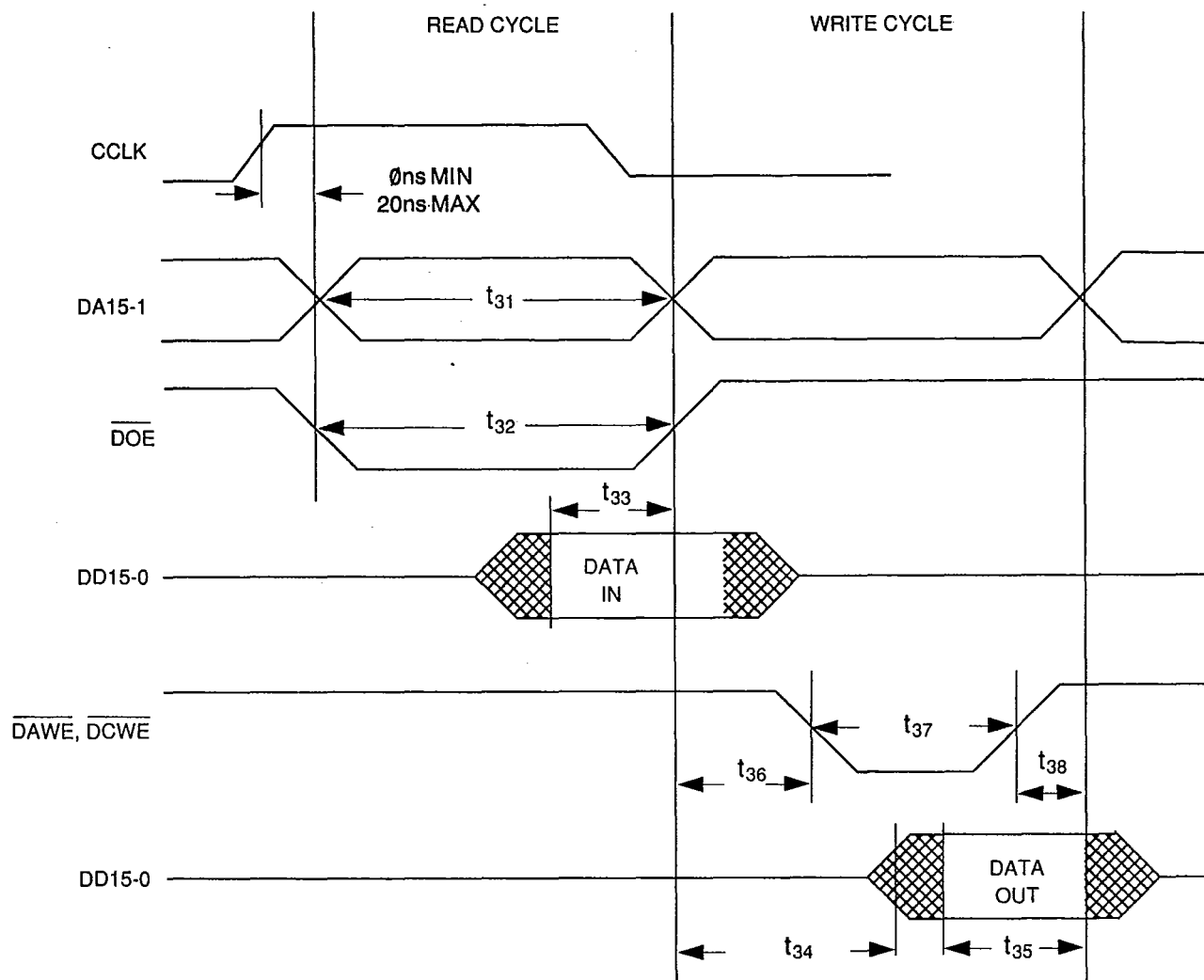


FIGURE 20-CHARACTER GENERATOR TIMING



Timing parameters are typical and are defined in terms of the number of dot clock periods ( $t_{cy}$ ) as follows:

| Dots/<br>Char | READ <sup>1</sup> |          |          |          |          |          |          |          | WRITE <sup>2</sup> |          |          |          |          |          |          |          |
|---------------|-------------------|----------|----------|----------|----------|----------|----------|----------|--------------------|----------|----------|----------|----------|----------|----------|----------|
|               | $t_{31}$          | $t_{32}$ | $t_{33}$ | $t_{34}$ | $t_{35}$ | $t_{36}$ | $t_{37}$ | $t_{38}$ | $t_{31}$           | $t_{32}$ | $t_{33}$ | $t_{34}$ | $t_{35}$ | $t_{36}$ | $t_{37}$ | $t_{38}$ |
| 9             | 4                 | 4        | 25       | N/A      | N/A      | N/A      | N/A      | N/A      | 5                  | N/A      | N/A      | 2        | 3        | 1        | 3        | 1        |
| 10            | 5                 | 5        | 25       | N/A      | N/A      | N/A      | N/A      | N/A      | 5                  | N/A      | N/A      | 2        | 3        | 1        | 3        | 1        |
| 11            | 5                 | 5        | 25       | N/A      | N/A      | N/A      | N/A      | N/A      | 6                  | N/A      | N/A      | 2        | 4        | 1        | 4        | 1        |
| 12            | 6                 | 6        | 25       | N/A      | N/A      | N/A      | N/A      | N/A      | 6                  | N/A      | N/A      | 2        | 4        | 1        | 4        | 1        |

- NOTES: 1. Read cycle timing reflects refresh portion of character cycle (a read cycle during the processor half of the character cycle would be 1 dot time extra for 9 and 11 dot characters).  
 2. Write cycle timing occurs only during the processor portion of the character cycle.  
 3. This is an absolute minimum parameter of 25 nsec.  
 4. Reference level for display memory timing is 1.4V.

FIGURE 21—DISPLAY MEMORY TIMING<sup>4</sup>