STANDARD
MICROSYSTEMS
CORPORATION

DAC97S01
PRELIMINARY

MULTIMEDIA AUDIO CODEC FOR AC '97

FEATURES

- High Performance ΣΔ Technology
- 18 Bit Full Duplex Stereo A/D, D/A
- AC-Link Protocol Compliance
- Operates at Either 5 VDC or 3.3 VDC
- AC '97 Compliant Mixer
- Energy Saving Power Down Modes
- 48k Sample/Second Rate
- Six Analog Line-Level Inputs
- Available in 48 Pin TQFP
- SNR > 95 dB Through the DAC and Mixer

GENERAL DESCRIPTION

SMSCs DAC97S01 is a general purpose 18 bit, full duplex, audio codec that conforms to the analog component specification of AC'97 (Audio Codec '97 Component Specification rev. 1.03). The DACs, ADCs, and mixers are integrated with analog I/Os which include four analog line-level stereo inputs, two analog line-level mono inputs, and 3 output channels. The Audio Codec '97 specification calls for separation of the basic analog codec functions from the high level digital control functions for improved noise immunity. The DAC97S01 communicates via the five wire AC Link to any digital component of AC'97 providing flexibility in the audio system design. Packaged in a small AC'97 compliant 48 pin TQFP, the DAC97S01 can be placed on the motherboard, daughter boards, add-on cards, PCMCIA cards, or outside the main chassis such as in a speaker.

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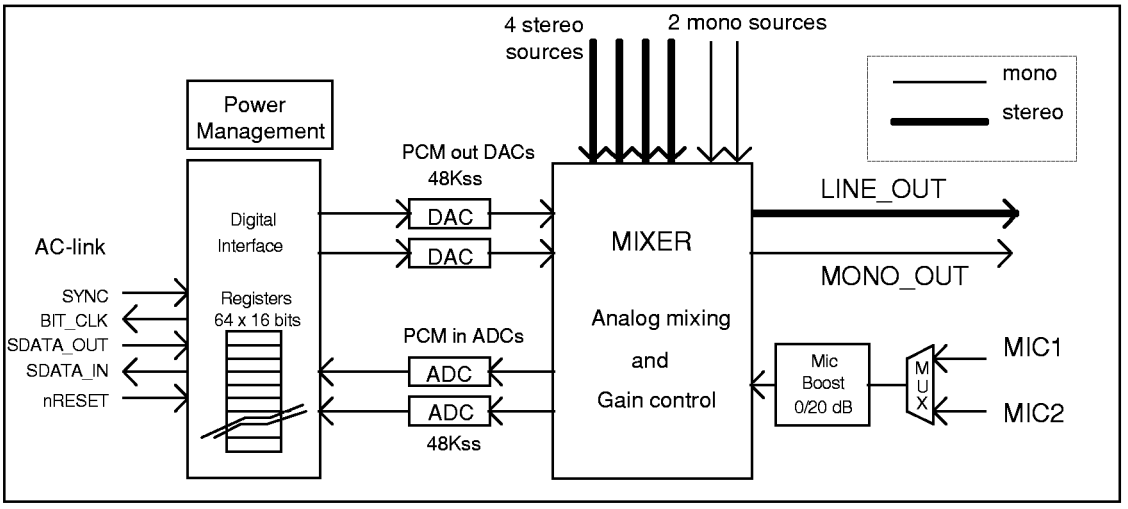

FIGURE 1 - DAC97S01 BLOCK DIAGRAM

The DAC97S01 block diagram, above, illustrates its primary functional blocks. It performs fixed 48K sample rate D-A & A-D conversion, mixing, and analog processing. The digital interface communicates with the AC'97 controller via the five wire AC-link and contains the 64 word by 16 bit registers. Two fixed 48Kss DAC's support a stereo PCM-out channel which contains a mix generated in the AC'97 controller of all software sources, including the internal synthesizer and any other digital sources. The Mixer block mixes the PCM-out with any analog sources, then outputs to LINE_OUT. The MONO_OUT delivers either mic only or a mono mix of sources from the mixer. The two fixed 48Kss ADC's take any mix of mono or stereo sources and convert it to a stereo PCM-in signal.

The DAC97S01 is designed primarily to support stereo, 2-speaker PC audio. However, multi-channel encoded stereo can be played out through the LINE_OUT. This encoded signal can be played on normal stereo speakers, or sent to consumer equipment or other decoding devices via LINE_OUT to an analog input connection for multi-channel playback.

See appendixes A and B for sample schematics showing mixed 3.3v/5v operation and 5v only operation.

Together with the logic component (controller) of AC'97, DAC97S01 can be SoundBlaster and Windows Sound System compatible. SoundBlaster is a registered trademark of Creative Labs. Windows is a registered trademark of Microsoft Corporation.

PIN/SIGNAL DESCRIPTIONS

Digital I/O

These signals connect the DAC97S01 to its AC'97 controller counterpart and an external crystal.

TABLE 1 - DIGITAL SIGNAL LIST

SIGNAL NAME	TYPE	DESCRIPTION
nRESET	I	AC'97 Master H/W Reset
XTL_IN	I	24.576 MHz Crystal
XTL_OUT	O	24.576 MHz Crystal
SYNC	I	48 kHz fixed rate sample sync
BIT_CLK	O	12.288 MHz serial data clock
SDATA_OUT	I	Serial, time division multiplexed, AC'97 input stream
SDATA_IN	O	Serial, time division multiplexed, AC'97 output stream

'n' denotes active low

Analog I/O

These signals connect the DAC97S01 to analog sources and sinks, including microphones and speakers.

TABLE 2 - ANALOG SIGNAL LIST

SIGNAL NAME	TYPE	DESCRIPTION
PC-BEEP	I	PC Speaker beep pass through
PHONE	I	From telephony subsystem speakerphone (or DLP - Down Line Phone)
MIC1	I	Desktop Microphone Input
MIC2	I	Second Microphone Input
LINE-IN-L	I	Line In Left Channel
LINE-IN-R	I	Line In Right Channel
CD-L	I	CD Audio Left Channel
CD-GND	I	CD Audio analog ground
CD-R	I	CD Audio Right Channel
VIDEO-L	I	Video Audio Left Channel
VIDEO-R	I	Video Audio Right Channel
AUX-L	I	Aux Left Channel
AUX-R	I	Aux Right Channel
LINE-OUT-L	O	Line Out Left Channel
LINE-OUT-R	O	Line Out Right Channel
MONO-OUT	O	To telephony subsystem speakerphone (or DLP - Down Line Phone)

* Note: Any unused input pins should have a capacitor (1 uF suggested) to ground.

Filter/References

These signals are connected to resistors, capacitors, or specific voltages.

TABLE 3 - FILTERING AND VOLTAGE REFERENCES

SIGNAL NAME	TYPE	DESCRIPTION
Vref	O	Reference Voltage
Vrefout	O	Reference Voltage out 5mA drive (intended for mic bias)
AFILT1	O	Anti-Aliasing Filter Cap - ADC channel
AFILT2	O	Anti-Aliasing Filter Cap - ADC channel
CAP2	O	ADC reference Cap

Power and Ground Signals

TABLE 4 - POWER SIGNAL LIST DAC97S01

SIGNAL NAME	TYPE	DESCRIPTION
AVdd1	I	Analog Vdd = 5.0V
AVdd2	I	Analog Vdd = 5.0V
AVss1	I	Analog Gnd
AVss2	I	Analog Gnd
DVdd1	I	Digital Vdd = 5.0V or 3.3V
DVdd2	I	Digital Vdd = 5.0V or 3.3V
DVss1	I	Digital Gnd
DVss2	I	Digital Gnd

AC-LINK

Below is the figure of the AC-link point to point serial interconnect between the DAC97S01 and its companion controller. All digital audio streams and command/status information are communicated over this AC-link. Please refer to the "Digital Interface" section for details.

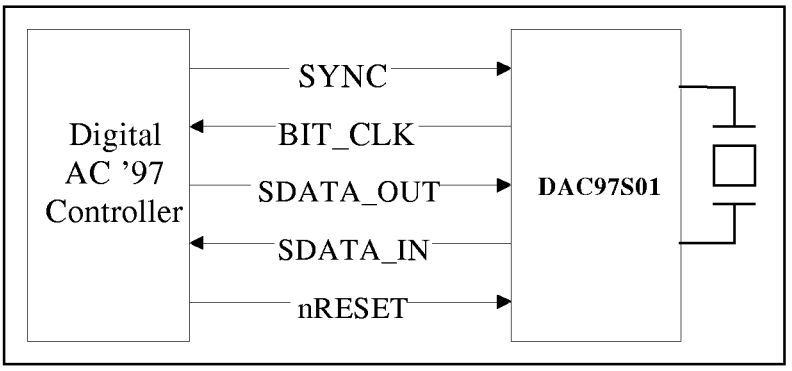

FIGURE 2 - DAC97S01's AC97-LINK TO ITS COMPANION CONTROLLER

Clocking

DAC97S01 derives its clock internally from an externally connected 24.576 MHz crystal or an oscillator through the XTAL_IN pin. Synchronization with the AC'97 controller is achieved through the BIT_CLK pin at 12.288 MHz (half of crystal frequency).

The beginning of all audio sample packets, or "Audio Frames", transferred over AC-link is synchronized to the rising edge of the "SYNC" signal driven by the AC'97 controller. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled by the receiving side on each immediately following falling edge of BIT_CLK.

Reset

There are 3 types of resets as detailed under "Timing Characteristics":

1. A "cold" reset where all DAC97S01 logic is initialized to its default state
2. A "warm" reset where the contents of the DAC97S01 register set are left unaltered
3. A "register" reset which only initializes the DAC97S01 registers to their default states

After signaling a reset to the DAC97S01, the AC'97 controller should not attempt to play or capture audio data until it has sampled a "Codec Ready" indication from the DAC97S01.

In order for proper operation SDATA_OUT should be "0" during "cold" reset.

DIGITAL INTERFACE

AC-link Digital Serial Interface Protocol

The DAC97S01 communicates to the AC'97 controller via a 5 pin digital serial interface called AC-link which is a bi-directional, fixed rate, serial PCM digital stream. All digital audio streams, commands and status information are communicated over this point to point serial interconnect. This link handles multiple inputs, and output audio streams, as well as control register accesses using a time division multiplexed (TDM) scheme. The AC'97 controller synchronizes all AC-link data transaction. The following data streams are available on the DAC97S01:

• **PCM Playback**	**2 output slots**	2 Channel composite PCM output stream
• **PCM Record data**	**2 input slots**	2 Channel composite PCM input stream
• **Control**	**2 output slots**	Control register write port
• **Status**	**2 input slots**	Control register read port

Synchronization of all AC-link data transactions is signaled by the AC'97 controller. The DAC97S01 drives the serial bit clock onto AC-link. The AC'97 controller then qualifies with a synchronization signal to construct audio frames.

SYNC, fixed at 48 kHz, is derived by dividing down the serial bit clock (BIT_CLK). BIT_CLK, fixed at 12.288 MHz, provides the necessary clocking granularity to support 12, 20 bit outgoing and incoming time slots. AC-link serial data is transitioned on each rising edge of BIT_CLK. The receiver of AC-link data, DAC97S01 for outgoing data and AC'97 controller for incoming data, samples each serial bit on the falling edges of BIT_CLK.

The AC-link protocol provides for a special 16 bit (13 bits defined, with 3 reserved trailing bit positions) time slot (Slot 0) wherein each bit conveys a valid tag for its corresponding time slot within the current audio frame. A "1" in a given bit position of slot 0 indicates that the corresponding time slot within the current audio frame has been assigned to a data stream, and contains valid data. If a slot is "tagged" invalid, it is the responsibility of the source of the data, (DAC97S01 for the input stream, AC'97 controller for the output stream), to stuff all bit positions with 0's during that slot's active time.

SYNC remains high for a total duration of 16 BIT_CLKs at the beginning of each audio frame. The portion of the audio frame where SYNC is high is defined as the "Tag Phase". The remainder of the audio frame where SYNC is low is defined as the "Data Phase".

Additionally, for power savings, all clock, sync, and data signals can be halted.

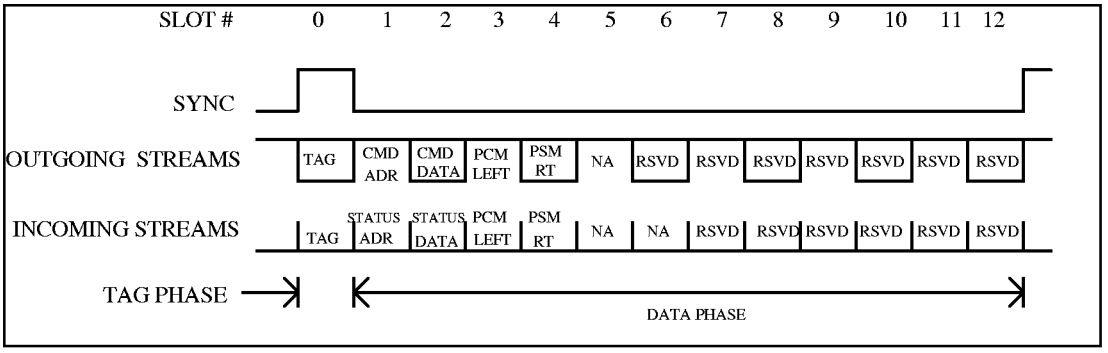

FIGURE 3 - AC'97 STANDARD BI-DIRECTIONAL AUDIO FRAME

AC-link Audio Output Frame (SDATA_OUT)

The audio output frame data streams correspond to the multiplexed bundles of all digital output data targeting the DAC97S01 DAC inputs, and control registers. Each audio output frame supports up to 12 20 bit outgoing data time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Within slot 0, the first bit is a global bit (SDATA_OUT slot 0, bit 15) which flags the validity for the entire audio frame. If the "Valid Frame" bit is a 1, this indicates that the current audio frame contains at least one slot time of valid data. The next 12 bit positions sampled by the DAC97S01 indicate which of the corresponding 12 times slots contain valid data. In this way data streams of differing sample rates can be transmitted across AC-link at its fixed 48 kHz audio frame rate. The following diagram illustrates the time slot based AC-link protocol.

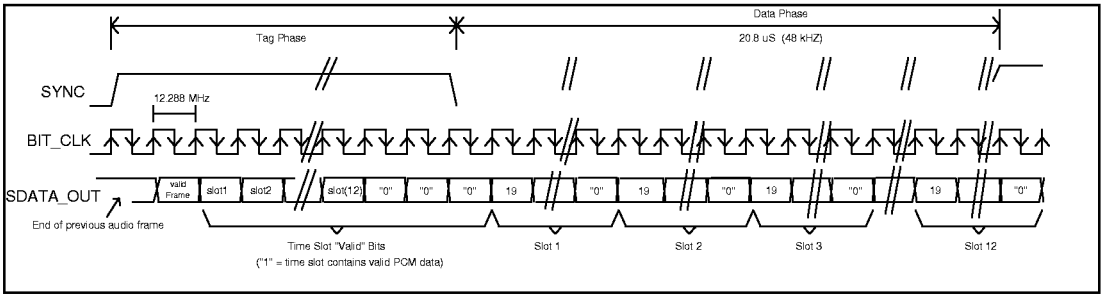

FIGURE 4 - AC-LINK AUDIO OUTPUT FRAME

A new audio output frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, the DAC97S01 samples the assertion of SYNC. This following edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising edge of BIT_CLK, the AC'97 controller transitions SDATA_OUT into the first bit position of slot 0 (Valid Frame bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK, and subsequently sampled by the DAC97S01 on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

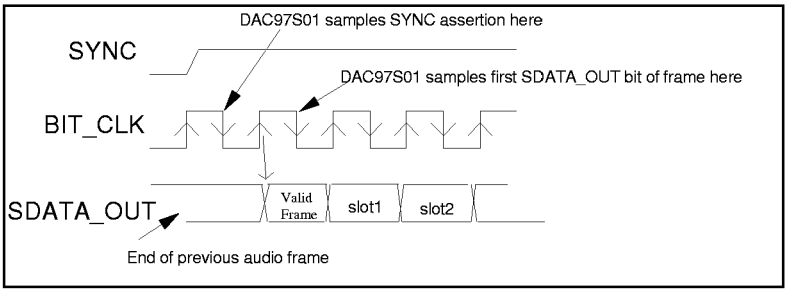

FIGURE 5 - START OF AN AUDIO OUTPUT FRAME

SDATA_OUT's composite stream is MSB justified (MSB first) with all non-valid slots' bit positions stuffed with 0's by the AC'97 controller.

When mono audio sample streams are sent from the AC'97 controller it is necessary that BOTH left and right sample stream time slots be filled with the same data.

Slot 1: Command Address Port

The command port is used to control features, and monitor status (see Audio Input Frame Slots 1 and 2) of the DAC97S01 functions including, but not limited to, mixer settings, and power management (refer to the control register section of this specification).

The control interface architecture supports up to 64 16 bit read/write registers, addressable on even byte boundaries. Only the even registers (00h, 02h, etc.) are valid.

Audio output frame slot 1 communicates control register address, and write/read command information to the DAC97S01.

Command Address Port bit assignments:

Bit (19) - Read/Write command (1= read, 0=write)
Bit (18:12) - Control Register Index (64 16 bit locations, addressed on even byte boundaries)
Bit (11:0) - Reserved (Stuffed with 0's)

The first bit (MSB) sampled by DAC97S01 indicates whether the current control transaction is a read or a write operation. The following 7 bit positions communicate the targeted control register address. The trailing 12 bit positions within the slot are reserved and must he stuffed with 0's by the AC '97 controller.

Slot 2: Command Data Port

The command data port is used to deliver 16 bit control register write data in the event that the current command port operation is a write cycle. (As indicated by Slot 1, bit 19)

Bit (19:4) - Control Register Write Data (Stuffed with 0's if current operation is a read)
Bit (3:0) - Reserved (Stuffed with 0's)

If the current command port operation is a read then the entire slot time must be stuffed with 0's by the AC '97 controller.

Slot 3: PCM Playback Left Channel

Audio output frame slot 3 is the composite digital audio left playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (wav) output samples digitally mixed (on the AC '97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20 bits is transferred, the AC '97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

Slot 4: PCM Playback Right Channel

Audio output frame slot 4 is the composite digital audio right playback stream. In a typical "Games Compatible" PC this slot is composed of standard PCM (wav) output samples digitally mixed (on the AC '97 controller or host processor) with music synthesis output samples. If a sample stream of resolution less than 20 bits is transferred, the AC '97 controller must stuff all trailing non-valid bit positions within this time slot with 0's.

Slots 5-12: Reserved

Audio output frame slots 5-12 are reserved for future use and are always stuffed with 0's by the AC '97 controller.

AC-link Audio Input Frame (SDATA_IN)

The audio input frame data streams correspond to the multiplexed bundles of all digital input data targeting the AC'97 controller. As is the case for audio output frame, each AC-link audio input frame consists of 12, 20 bit time slots. Slot 0 is a special reserved time slot containing 16 bits which are used for AC-link protocol infrastructure.

Within slot 0 the first bit is a global bit (SDATA_IN slot 0, bit 15) which flags whether the DAC97S01 is in the "Codec Ready" state or not. If the "Codec Ready" bit is a 0, this indicates that DAC97S01 is not ready for normal operation. This condition is normal following the de-assertion of power on reset, for example, while DAC97S01's voltage references settle. When the AC-link "Codec Ready" indicator bit is a 1, it indicates that the AC-link and DAC97S01 control/status registers are in a fully operational state. The AC '97 controller must further probe the Powerdown Control Status Register (refer to Mixer Register section) to determine exactly which subsections, if any, are ready.

Prior to any attempts at putting DAC97S01 into operation the AC '97 controller should poll the first bit in the audio input frame (SDATA_IN slot 0, bit 15) for an indication that DAC97S01 has become "Codec Ready". Once the DAC97S01 is sampled "Codec Ready", the next 12 bit positions sampled by the AC '97 controller indicate which of the corresponding 12 time slots are assigned to input data streams, and that they contain valid data. The following diagram illustrates the time slot based AC-link protocol.

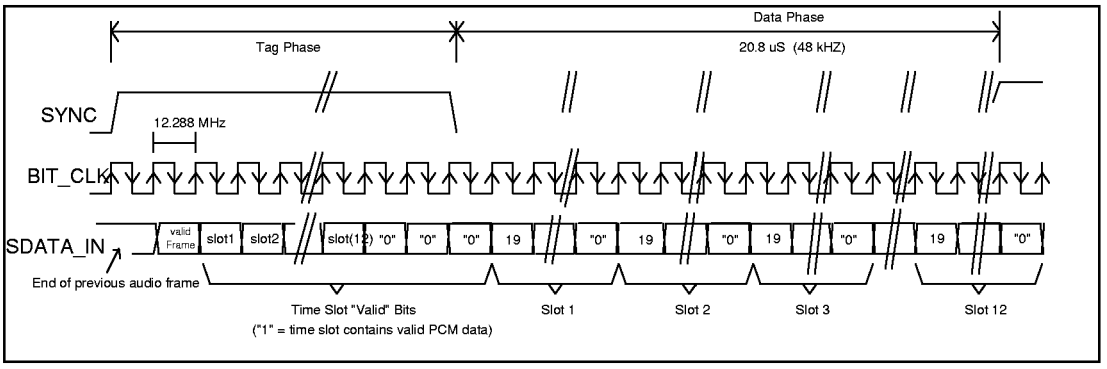

FIGURE 6 - DAC97S01 AUDIO INPUT FRAME

A new audio input frame begins with a low to high transition of SYNC. SYNC is synchronous to the rising edge of BIT_CLK. On the immediately following falling edge of BIT_CLK, DAC97S01 samples the assertion of SYNC. This falling edge marks the time when both sides of AC-link are aware of the start of a new audio frame. On the next rising of BIT_CLK, the DAC97S01 transitions SDATA_IN into the first bit position of slot 0 ("Codec Ready" bit). Each new bit position is presented to AC-link on a rising edge of BIT_CLK and subsequently sampled by the AC'97 controller on the following falling edge of BIT_CLK. This sequence ensures that data transitions, and subsequent sample points for both incoming and outgoing data streams are time aligned.

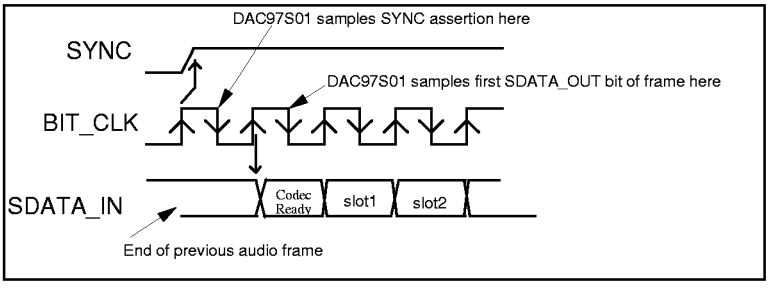

FIGURE 7 - START OF AN AUDIO INPUT FRAME

SDATA_IN's composite stream is MSB justified (MSB first) with all non-valid bit positions (for assigned and/or unassigned time slots) stuffed with 0's by DAC97S01. SDATA_IN data is sampled on the falling edges of BIT_CLK.

Slot1: Status Address Port

The status port is used to monitor status for DAC97S01 functions including, but not limited to, mixer settings, and power management.

Audio input frame slot 1's stream echoes the control register index, for historical reference, for the data to be returned in slot 2. (Assuming that slots 1 and 2 had been tagged "valid" by DAC97S01 during slot 0).

Status Address Port Bit Assignments:

Bit (19) - RESERVED/(Stuffed with 0)
Bit (18;12) - Control Register Index (Echo of register index for which data is being returned)
Bit (11:0) – RESERVED/(Stuffed with 0's)

The first bit (MSB) generated by DAC97S01 is always stuffed with a 0. The following 7 bit positions communicate the associated control register address, and the trailing 12 bit positions are stuffed with 0's by DAC97S01.

Slot 2: Status Data Port

The status data port delivers 16 bit control register read data.

Bit (19:4) - Control Register Read Data/ (Stuffed with 0's if tagged "invalid")
Bit (3:0) - RESERVED/(Stuffed with 0's)

If Slot 2 is tagged "invalid" by DAC97S01, then the entire slot will be stuffed with 0's.

Slot 3: PCM Record Left Channel

Audio input frame slot 3 is the left channel output of DAC97S01 input MUX, post-ADC. DAC97S01 ADCs are implemented to support 18 bit resolution.

DAC97S01 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20 bit time slot.

Slot 4: PCM Record Right Channel

Audio input frame slot 4 is the right channel output of DAC97S01 input MUX, post-ADC.

DAC97S01 outputs its ADC data (MSB first), and stuffs any trailing non-valid bit positions with 0's to fill out its 20 bit time slot.

Slots 5-12: Reserved

Audio input frame slots 5-12 are reserved for future use and are always stuffed with 0's.

AC-link Low Power Mode

The DAC97S01 can be placed in the low power mode by programming Register 26h to the appropriate value. Both BIT_CLK and SDATA_IN will be brought to, and held at a logic low voltage level. The AC'97 controller can wake up the DAC97S01 by providing the appropriate reset signals.

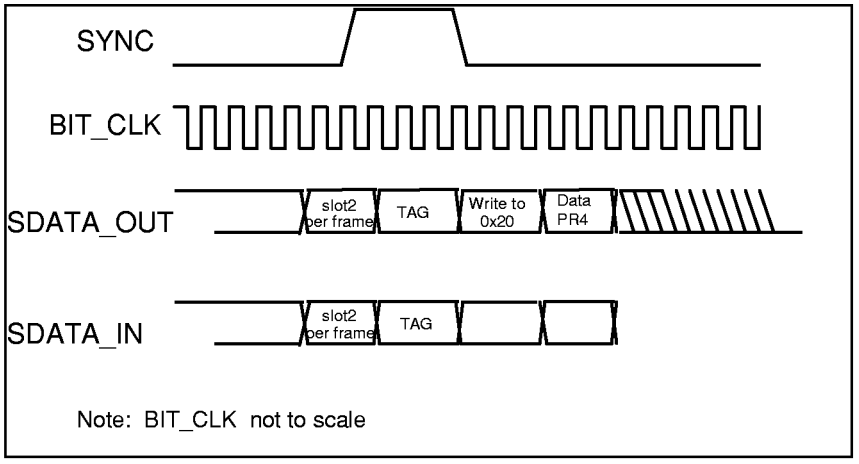

FIGURE 8 - DAC97S01 POWERDOWN TIMING

BIT_CLK and SDATA_IN are transitioned low immediately (within the maximum specified time) following the decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 controller driver is at the point where it is ready to program the AC-link into its low power mode, slots (1 and 2) are assumed to be the only valid stream in the audio output frame (all sources of audio input have been neutralized).

The AC'97 controller should also drive SYNC, and SDATA_OUT low after programming the DAC97S01 to this low power mode.

Waking up the AC-link

Once the DAC97S01 has halted BIT_CLK, there are only two ways to "wake up" the AC-link. Both methods must be activated by the AC'97 controller.

The AC-link protocol provides for a "Cold AC'97 Reset", and a "Warm AC'97 Reset". The current power down state would ultimately dictate which form of reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all power down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of 4 audio frame times following the frame in which the power down was triggered. When AC-link powers up it indicates readiness via the Codec Ready bit (input slot 0, bit 15).

Cold Reset - A cold reset is achieved by asserting nRESET for the minimum specified time. By driving nRESET low, BIT_CLK, and SDATA_IN will be activated, or re-activated as the case may be, and all DAC97S01 control registers will be initialized to their default power on reset values. Note: nRESET is an asynchronous input. 'n' denotes active low.

Warm Reset - a warm reset will re-activate the AC-link without altering the current DAC97S01 register values. A warm reset is signaled by driving SYNC high for a minimum of 1 uS in the absence of BIT_CLK. Note: Within normal audio frames, SYNC is a synchronous input. However, in the absence of BIT_CLK, SYNC is treated as an asynchronous input used in the generation of a warm reset to the DAC97S01.

DAC97S01 MIXER

The DAC97S01 mixer is designed to the AC'97 specification to manage the playback and record of all digital and analog audio sources in the PC environment. These include:

- **System Audio**: Digital PCM input and output for business, games and multimedia
- **CD/DVD**: Analog CD/DVD-ROM Redbook audio with internal connections to Codec mixer
- **Mono microphone**: Choice of desktop mic, with programmable boost and gain
- **Speakerphone**: Use of system mic and speakers for telephone, DSVD, and video conferencing
- **Video**: TV tuner or video capture card with internal connections to Codec mixer
- **AUX/synth**: Analog FM or wavetable synthesizer, or other internal source

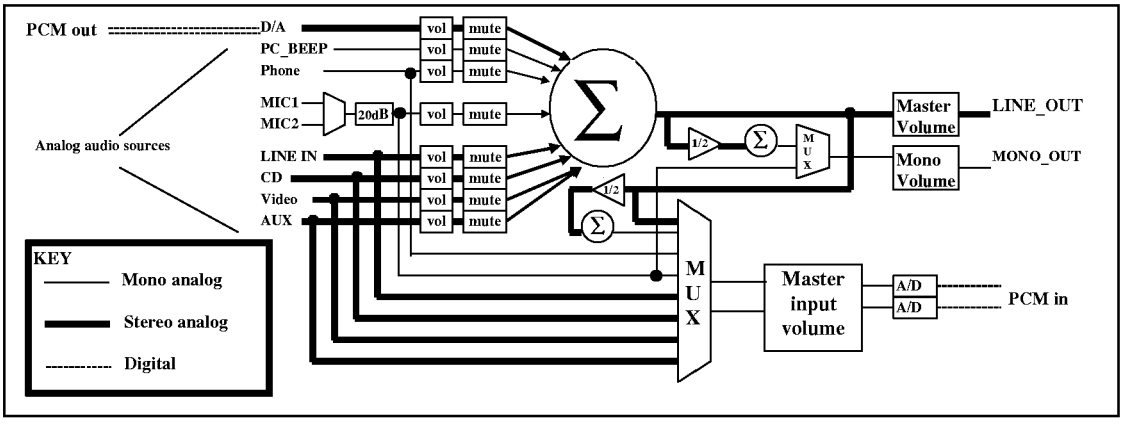

FIGURE 9 - DAC97S01 MIXER FUNCTIONAL DIAGRAM

TABLE 5 - MIXER FUNCTIONAL CONNECTIONS

SOURCE	FUNCTION	CONNECTION
PC_Beep	PC beep pass through	from PC beeper output
PHONE	speakerphone or DLP in	from telephony subsystem
MIC1	desktop microphone	from mic jack
MIC2	second microphone	from second mic jack
LINE_IN	external audio source	from line-in jack
CD	audio from CD-ROM	cable from CD-ROM
VIDEO	audio from TV tuner or video camera	cable from TV or VidCap card
AUX	upgrade synth or other external source	internal connector
PCM out	digital audio output from AC'97 Controller	AC-link
LINE_OUT	stereo mix of all sources	to output jack
MONO_OUT	mic or mix for speakerphone or DLP out	to telephony subsystem
PCM in	digital audio input to AC'97 Controller	AC-link

Mixer Input

The mixer provides recording and playback of any audio sources or output mix of all sources. The DAC97S01 supports the following input sources:

- Any mono or stereo source
- Mono or stereo mix of all sources
- 2-channel input w/mono output reference (mic + stereo mix)

Note: Any unused input pins must have a capacitor (1 uF suggested) to ground.

Mixer Output

The mixer generates two distinct outputs:

- A stereo mix of all sources for output to the LINE_OUT
- A mono, mic only or mix of all sources for MONO_OUT

*Note: Mono output of stereo mix is attenuated by ½.

PC Beep Implementation

PC Beep is active on power up and defaults to an unmuted state. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation.

Mixer Registers

TABLE 6 - MIXER REGISTERS

REG #	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DE-FAULT
00h	Reset	X	SE4	SE3	SE2	SE1	SE0	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	NA
02h	Master Volume	Mute	X	X	ML4	ML3	ML2	ML1	ML0	X	X	X	MR4	MR3	MR2	MR1	MR0	8000h
06h	Master Volume Mono	Mute	X	X	X	X	X	X	X	X	X	X	MM4	MM3	MM2	MM1	MM0	8000h
0Ah	PC_BEEP Volume	Mute	X	X	X	X	X	X	X	X	X	X	PV3	PV2	PV1	PV0	X	x000h
0Ch	Phone volume	Mute	X	X	X	X	X	X	X	X	X	X	GN4	GN3	GN2	GN1	GN0	8008h
0Eh	Mic Volume	Mute	X	X	X	X	X	X	X	X	20dB	X	GN4	GN3	GN2	GN1	GN0	8008h
10h	Line In Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
12h	CD Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
14h	Video Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
16h	AUX Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
18h	PCM Out Volume	Mute	X	X	GL4	GL3	GL2	GL1	GL0	X	X	X	GR4	GR3	GR2	GR1	GR0	8808h
1Ah	Record Select	X	X	X	X	X	SL2	SL1	SL0	X	X	X	X	X	SR2	SR1	SR0	0000h
1Ch	Record Gain	Mute	X	X	X	GL3	GL2	GL1	GL0	X	X	X	X	GR3	GR2	GR1	GR0	8000h
20h	General Purpose	X	ST	X	X	X	X	MIX	MS	LPBK	X	X	X	X	X	X	X	000h
26h	Powerdown Ctrl/Stat	PR7	PR6	PR5	PR4	PR3	PR2	PR1	PR0	X	X	X	X	REF	ANL	DAC	ADC	NA

REG #	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	DE-FAULT
7Ch	Vendor ID1	1	0	0	0	0	0	1	1	1	0	0	0	0	1	0	0	NA
7Eh	Vendor ID2	0	1	1	1	0	1	1	0	0	0	0	0	0	1	0	0	NA

Notes:

1. All registers not shown and bits containing an X are reserved.
2. Any reserved bits, marked X, can be written to but are don't care upon read back.
3. PC_BEEP default to 0000h, mute off.
4. If optional bits D13, D5 of register 02H or D5 of register 06H are set to 1, then the corresponding attenuation is set to 46dB and the register reads will produce 3fH as a value for this attenuation/gain block.

Reset Register (Index 00h)

Writing any value to this register performs a register reset, which causes all registers to revert to their default values. Reading this register returns the ID code of the part.

All DACs operate at the same resolution. All ADCs operate at the same resolution.

Play Master Volume Registers (Index 02h, 04h, and 06h)

These registers manage the output signal volumes. Register 02h controls the stereo master volume (both right and left channels), register 04h controls the optional stereo headphone out, register 06h controls the mono volume output. Each step corresponds to 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. ML5 through ML0 is for left channel level, MR5 through MR0 is for the right channel and MM5 through MM0 is for the mono out channel.

The default value is 8000h (1000 0000 0000 0000), which corresponds to 0 dB attenuation with mute on.

TABLE 7 - PLAY MASTER VOLUME REGISTER

MUTE	MX5…MX0	FUNCTION	RANGE
0	00 0000	0dB Attenuation	Req.
0	01 1111	46.5 Attenuation	Req.
1	xx xxxx	∞ dB Attenuation	Req.

PC Beep Register (Index 0Ah)

This controls the level for the PC Beep input. Each step corresponds to approximately 3 dB of attenuation. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. PC_BEEP supports motherboard implementations. The intention of routing PC_BEEP through the DAC97S01 mixer is to eliminate the requirement for an onboard speaker by guaranteeing a connection to speakers connected via the output jack. In order for this to be viable the PC_BEEP signal needs to reach the output jack at all times. NOTE: The PC_BEEP is recommended to be routed to L & R Line outputs even when the DAC97S01 is in a RESET state. This is so that Power On Self Test (POST) codes can be heard by the user in case of a hardware problem with the PC. For further PC_BEEP implementation details please refer to the AC'97 Technical FAQ sheet. The default value can be 0000h or 8000h, which corresponds to 0 dB attenuation with mute off or on.

TABLE 8 - PC_BEEP REGISTER

MUTE	PV3...PV0	FUNCTION
0	0000	0 dB Attenuation
0	1111	45 dB Attenuation
1	xxxx	∞ dB Attenuation

Analog Mixer Input Gain Registers (Index 0Ch - 18h)

This controls the gain/attenuation for each of the analog inputs. Each step corresponds to approximately 1.5 dB. The MSB of the register is the mute bit. When this bit is set to 1 the level for that channel is set at -∞ dB. Register 0Eh (Mic Volume Register) has an extra bit that is for a 20dB boost. When bit 6 is set to 1, the 20 dB boost is on. The default value is 8008, which corresponds to 0 dB gain with mute on. The default value for the mono registers is 8008h, which corresponds to 0dB gain with mute on. The default value for stereo registers is 8808h, which corresponds to 0 dB gain with mute on.

TABLE 9 - ANALOG MIXER INPUT GAIN REGISTER

MUTE	GX4...GX0	FUNCTION
0	00000	+12 dB gain
0	01000	0 dB gain
0	11111	-34.5 dB gain
1	xxxxx	-∞ dB gain

Record Select Control Register (Index 1Ah)

Used to select the record source independently for right and left. The default value is 0000h, which corresponds to Mic in.

TABLE 10 - RECORD SELECT CONTROL REGISTERS

SR2…SR0	RIGHT RECORD SOURCE
0	Mic
1	CD In (right)
2	Video In (right)
3	Aux In (right)
4	Line In (right)
5	Stereo Mix (right)
6	Mono Mix
7	Phone

SL2…SL0	LEFT RECORD SOURCE
0	Mic
1	CD In (L)
2	Video In (L)
3	Aux In (L)
4	Line In (L)
5	Stereo Mix (L)
6	Mono Mix
7	Phone

Record Gain Registers (Index 1Ch and 1Eh)

1Ch is for the stereo input and 1Eh is for the optional special purpose correlated audio mic channel. Each step corresponds to 1.5 dB. 22.5 dB corresponds to 0F0Fh and 000Fh respectively. The MSB of the register is the mute bit. When this bit is set to 1, the level for that channel(s) is set at -∞ dB.

The default value is 8000h, which corresponds to 0 dB gain with mute on.

TABLE 11 - RECORD GAIN REGISTERS

MUTE	GX3… GX0	FUNCTION
0	1111	+22.5 dB gain
0	0000	0 dB gain
1	xxxx	-∞ gain

General Purpose Register (Index 20h)

This register is used to control some miscellaneous functions. Below is a summary of each bit and its function. The MS bit controls the mic selector. The LPBK bit enables loopback of the ADC output to the DAC input without involving the AC-link, allowing for full system performance measurements.

TABLE 12 - GENERAL PURPOSE REGISTERS

BIT	FUNCTION
MIX	Mono output select 0 = Mix, 1= Mic
MS	Mic select 0 = Mic1, 1 = Mic2
LPBK	ADC/DAC loopback mode

Powerdown Control/Status Register (Index 26h)

This read/write register is used to program powerdown states and monitor subsystem readiness. The lower half of this register is read only status, a "1" indicating that the subsecton is "ready". *Ready* is defined as the subsection's ability to perform in its nominal state. When this register is written, the bit values that come in on AC-link will have no effect on read only bits 0-7.

When the AC-link "Codec Ready" indicator bit (SDATA_IN slot 0, bit 15) is a 1, it indicates that the AC-link and AC'97 control and status registers are in a fully operational state. The AC'97 controller must further probe this Powerdown Control/Status Register to determine exactly which subsections, if any are ready.

TABLE 13 - POWERDOWN STATUS REGISTERS

BIT	FUNCTION
REF	VREF's up to nominal level
ANL	Analog mixers, etc. ready
DAC	DAC section ready to playback data
ADC	ADC section ready to playback data

The power down modes are as per Table 13. The first three bits are to be used individually rather than in combination with each other. The last bit PR3 can be used in combination with PR2 or by itself. PR0 and PR1 control the PCM ADC's and DAC's only.

LOW POWER MODES

The DAC97S01 is capable of operating at reduced power when no activity is required. The state of power down is controlled by the Powerdown Register (26h). There are 7 commands of separate power down. See the table below for the different modes.

TABLE 14 - LOW POWER MODES

GRP BITS	FUNCTION
PR0	PCM in ADC's & Input Mux Powerdown
PR1	PCM out DACs Powerdown
PR2	Analog Mixer powerdown (Vref still on)
PR3	Analog Mixer powerdown (Vref off)
PR4	Digital Interface (AC-link) powerdown (extnl clk off)
PR5	Internal Clk disable
PR6	Not implemented

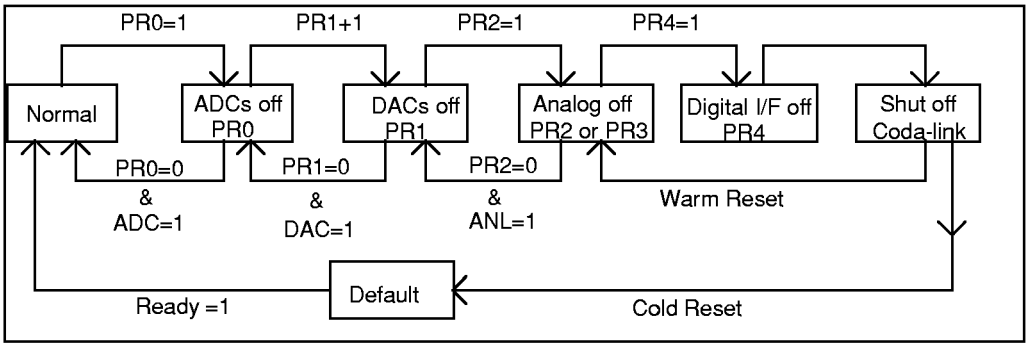

FIGURE 10 - EXAMPLE OF DAC97S01 POWERDOWN/POWERUP FLOW

The above figure illustrates one example procedure to do a complete powerdown of DAC97S01. From normal operation, sequential writes to the Powerdown Register are performed to power down DAC97S01 a piece at a time. After everything has been shut off, a final write (of PR4) can be executed to shut down the AC-link. The part will remain in sleep mode with all its registers holding their static values. To wake up, the AC'97 controller will send pulse on the sync line issuing a warm reset. This will restart AC-link (resetting PR4 to zero). The DAC97S01 can also be woken up with a cold reset. A cold reset will cause a loss of values of the registers as a cold reset will reset them to their default states. When a section is powered back on, the Powerdown Control/Status register (index 26h) should be read to verify that the section is ready (stable) before attempting any operation that requires it.

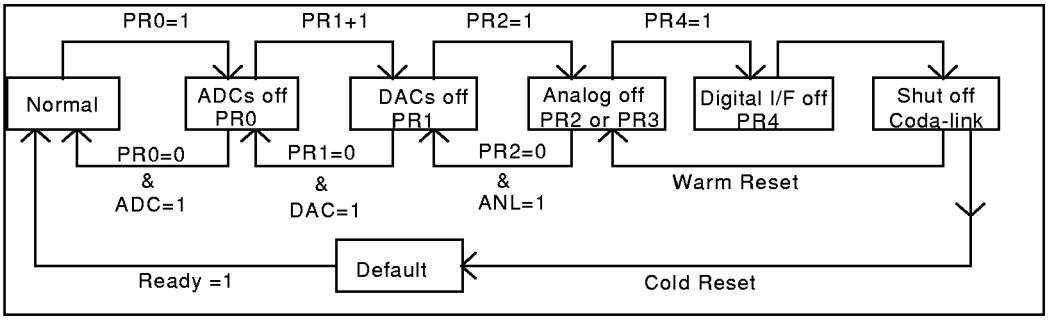

FIGURE 11 - DAC97S01 POWERDOWN/POWERUP FLOW WITH ANALOG STILL ALIVE

The above figure illustrates a state when all the mixers should work with the static volume settings that are contained in their associated registers. This is used when the user could be playing a CD (or external LINE_IN source) through DAC97S01 to the speakers but have most of the system in low power mode. The procedure for this follows the previous except that the analog mixer is never shut down.

TESTABILITY

The DAC97S01 has two test modes. One is for ATE in-circuit test and the other is restricted for internal use only. DAC97S01 enters the ATE in circuit test mode if SDATA_OUT is sampled high at the trailing edge of nRESET. Once in the ATE test mode, the digital AC-link outputs (BIT_CLK and SDATA_IN) are driven to a high impedance state. This allows ATE in-circuit testing of the AC'97 controller. This case will never occur during standard operating conditions.

AC TIMING CHARACTERISTICS

($T_{ambient}$ = 25°C, AVdd = 5.0V, DVdd = 5.0V or 3.3V +/- 10%, AVss=DVss+0V; 50pF external load)

Cold Reset

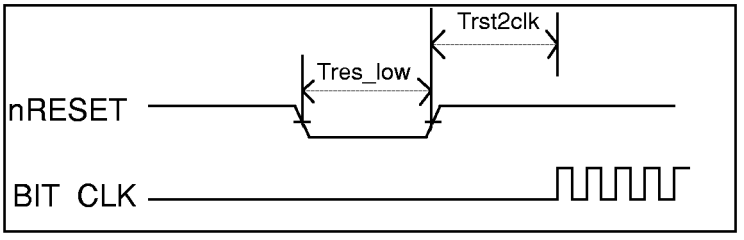

FIGURE 12 - COLD RESET

TABLE 15 - COLD RESET

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
nRESET active low pulse width	Tres_low	1.0	-	-	us
nRESET inactive to BIT_CLK startup delay	Trst2clk	162.8	-	-	ns

'n' denotes active low.

Warm Reset

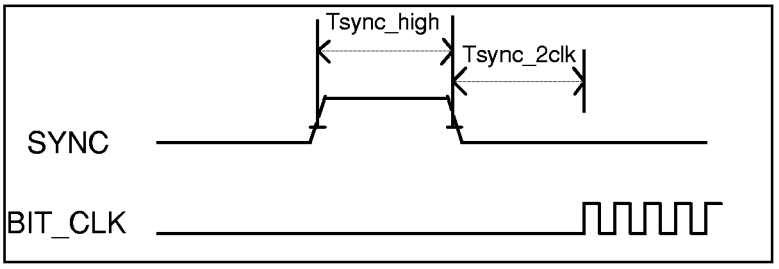

FIGURE 13 - WARM RESET

TABLE 16 - WARM RESET

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SYNC active high pulse width	Tsync_high	-	1.3	-	us
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

Clocks

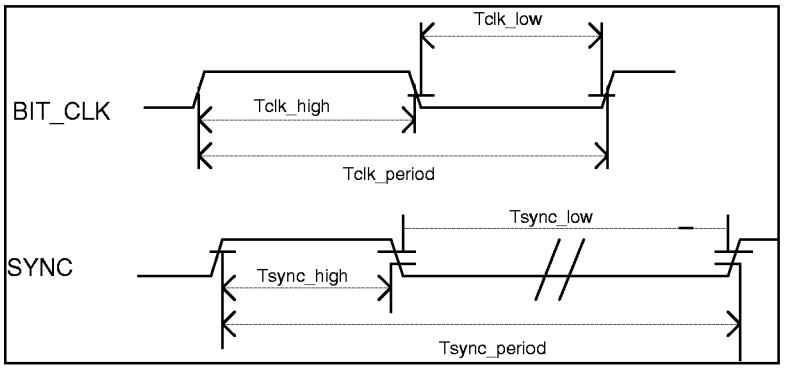

FIGURE 14 - CLOCKS

TABLE 17 - CLOCKS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	-	750	ps
BLT_CLK high pulsewidth (Note 1)	Tclk_high	32.56	40.7	48.84	ns
BIT_CLK low pulse width (Note 1)	Tclk_low	32.56	40.7	48.84	ns
SYNC frequency		-	48.0	-	kHz
SYNC period	Tsync_period	-	20.8	-	us
SYNC high pulse width	Tsync_high	-	1.3	-	us
SYNC low_pulse width	Tsync_low	-	19.5	-	us

Note 1: Worst case duty cycle restricted to 40/60.

Data Setup and Hold (50pF external load)

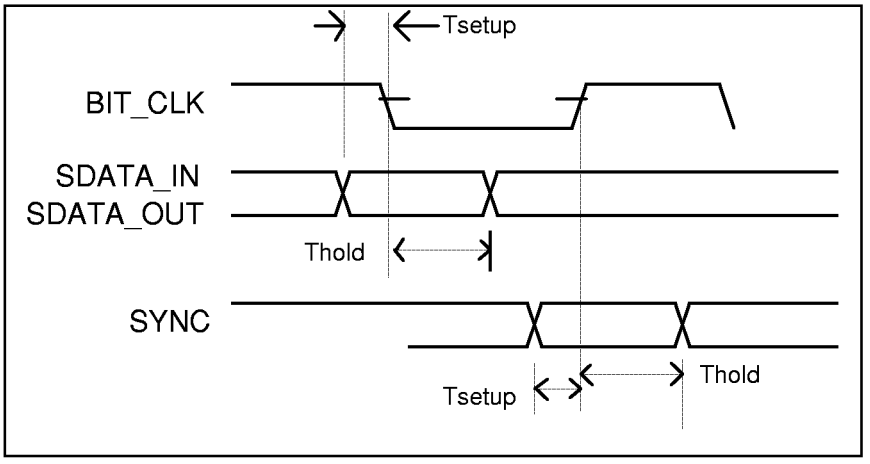

FIGURE 15 - DATA SETUP AND HOLD

TABLE 18 - DATA SETUP AND HOLD

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup to falling edge of BIT_CLK	Tsetup	15.0	-	-	ns
Hold from falling edge of BIT_CLK	Thold	5.0	-	-	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

Signal Rise and Fall Times
(50pF external load; from 10% to 90% of Vdd)

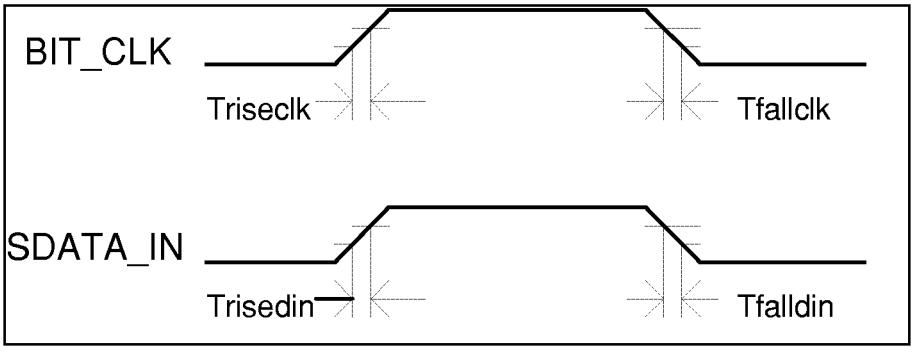

FIGURE 16 - SIGNAL RISE AND FALL TIMES

TABLE 19 - SIGNAL RISE AND FALL TIMES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
BIT_CLK rise time	Triseclk	2	-	6	ns
BIT_CLK fall time	Tfallclk	2	-	6	ns
SDATA_IN rise time	Trisedin	2	-	6	ns
SDATA_IN fall time	Tfalldin	2	-	6	ns

AC-link Low Power Mode Timing

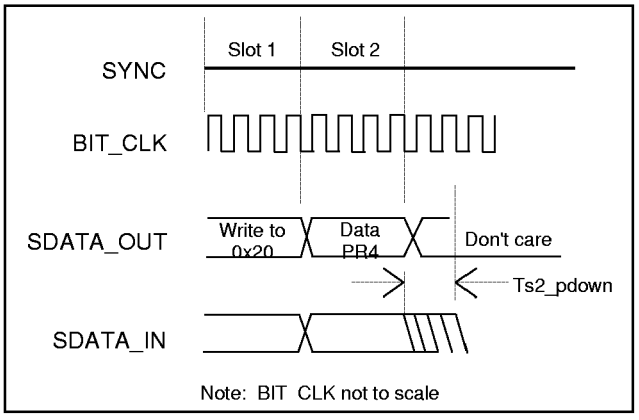

FIGURE 17 - AC-LINK LOW POWER MODE TIMING

TABLE 20 - AC-LINK LOW POWER MODE TIMING

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	us

ATE Test Mode

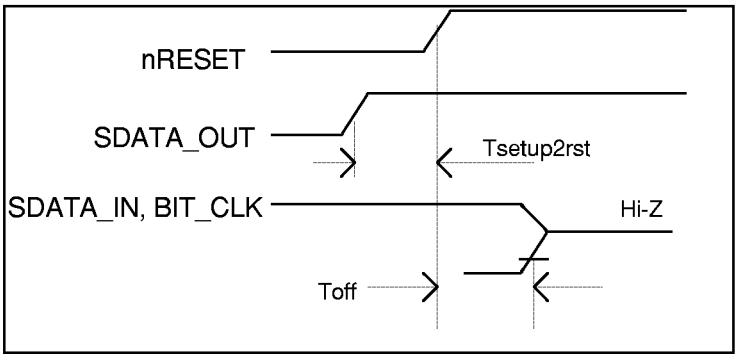

FIGURE 18 - ATE TEST MODE

TABLE 21 - ATE TEST MODE

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Setup to trailing edge of nRESET (also applies to SYNC)	Toff	15.0	-	-	ns
Rising edge of nRESET to Hi-Z delay	Toff	-	-	25.0	ns

Notes:

1. All AC-link signals are normally low through the trailing edge of nRESET. Bringing SDATA_OUT high for the trailing edge of nRESET causes DAC97S01's AC-link outputs to go high impedance which is suitable for ATE in circuit testing.
2. Once either of the two test modes have been entered, the DAC97S01 must be issued another nRESET with all AC-link signals low to return to the normal operating mode.

'n' denotes active low.

ELECTRICAL SPECIFICATIONS:

Absolute Maximum Ratings

Voltage on any pin relative to Ground	-0.3V TO +6.0V
Operating Temperature	0° TO 70° C
Storage Temperature	-55° TO +125° C
Soldering Temperature	260° C FOR 10 SECONDS
Output Current per Pin	+/- 4 mA except Vrefout = +/- 5mA

Recommended Operating Conditions

TABLE 22 - OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNITS
Power Supplies	+ 3.3v Digital	3.0	3.3	3.6	V
	+ 5v Digital	4.5	5	5.5	V
	+ 5v Analog	4.5	5	5.5	V
Ambient Temperature		0	-	70	^{o}C

Power Consumption

TABLE 23 - POWER CONSUMPTION

PARAMETER		MIN	TYP	MAX	UNITS
Digital Supply Current	+ 5v Digital		45		mA
	+ 3.3v Digital		29		mA
Analog Supply Current	+ 5v Analog		60		mA
Power Down Status					
PR0 +5v Analog Supply Current			47		mA
PR1 +5v Analog Supply Current			33		mA
PR2 +5v Analog Supply Current			TBD		mA
PR3 +5v Analog Supply Current			TBD		mA
PR4 +3.3v Digital Supply Current			TBD		mA
PR5 +3.3v Digital Supply Current			TBD		mA
PR4 +5v Digital Supply Current			TBD		mA
PR5 +5v Digital Supply Current			TBD		mA

AC-link Static Digital Specifications

($T_{ambient}$ = 25 deg C, DVdd = 5.0V or 3.3V +/- 10%, AVss=DVss+0V; 50pF external load)

TABLE 24 - AC-LINK STATIC SPECIFICATIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Input Voltage Range	Vin	-0.30		DVdd + 0.30	V
Low level input range	Vil	-	-	0.30xDVdd	V
High level input voltage	Vih	0.40xDVdd	-	-	V
High level output voltage	Voh	0.50xDVdd	-	-	V
Low level output voltage	Vol	-	-		V
Input Leakage Current (AC-link inputs)	-	-10	-	10	uA
Output Leakage Current (Hi-Z'd AC-link outputs)	-	-10	-	10	uA
Output buffer drive current	-	-	4		mA

DAC97S01 Analog Performance Characteristics

($T_{ambient}$ = 25 deg C, AVdd = DVdd = 5.0V +/- 10%, AVss=DVss+0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0dB = 1 Vrms, 10K ohm/ 50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0dB settings on all gain stages)

TABLE 25 - ANALOG PERFORMANCE CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage:				
Line Inputs	-	1.0	-	Vrms
Mic Inputs[1]	-	0.1	-	
Full Scale Output Voltage:				
Line Output 5V	-	1.0	-	Vrms
Analog S/N:				
CD to LINE_OUT 5V	90	98	-	dB
Other to LINE_OUT 5V	-	98	-	
Analog Frequency Response[2]	20	-	20,000	Hz
Digital S/N[3]				
D/A 5V	85	96	-	dB
A/D 5V	75	88	-	
Total Harmonic Distortion:				
Line Output[4]	-	-	0.02	%
D/A & A/D Frequency Response[5]	20	-	19,200	Hz
Transition Band	19,200	-	28,800	Hz
Stop Band	28,800	-	∞	Hz
Stop Band Rejection[6]	+85	-	-	dB

PARAMETER	MIN	TYP	MAX	UNITS
Out-of-Band Rejection[7]	-	+40	-	dB
Group Delay	-	-	-	ms
Power Supply Rejection Ratio (1kHz)	-	+40	-	dB
Crosstalk between Input channels	-	-	-70	dB
Spurious Tone Rejection	-	+100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	10	-	-	K Ohm
Input Capacitance	-	15	-	pF
Vrefout	-	0.41 x AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/deg. C
DAC Offset Voltage	-	10	50	mV
Deviation from Linear Phase	-	-	1	degree
External Load Impedance	10	-	-	K ohm
Mute Attenuation (Vrms input)	90	96	-	dB

Notes:

1. With +20 dB Boost on, 1.0Vrms with Boost off
2. +/- 1 dB limits
3. The ratio of the rms output level with 1 kHz full scale input to the rms output level with all zeros into the digital input. Measured "A weighted" over a 20 Hz to a 20 kHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
4. 0 dB gain, 20 kHz BW, 48 kHz Sample Frequency
5. +/-0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 kHz, with respect to a 1 Vrms DAC output.

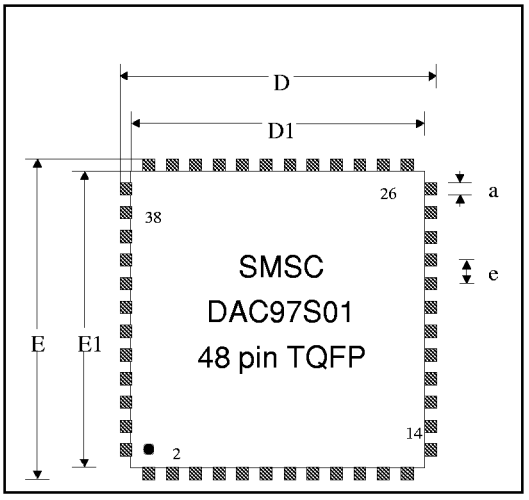

FIGURE 19 – PACKAGE OUTLINE

TABLE 26 - PACKAGE DIMENSIONS

KEY	DAC97S01 DIMENSION TQFP
D	9.00 mm
D1	7.00 mm
E	9.00 mm
E1	7.00 mm
a (lead width)	0.20 mm
e (pitch)	0.50 mm
thickness	1.4 mm

TABLE 27 - PIN DESIGNATION

PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME	PIN #	SIGNAL NAME
1	DVdd1	13	PHONE	25	AVdd1	37	MONO_OUT
2	XTL_IN	14	AUX_L	26	AVss1	38	AVdd2
3	XTL_OUT	15	AUX_R	27	Vref	39	NC
4	DVss1	16	VIDEO_L	28	Vrefout	40	NC
5	SDATA_OUT	17	VIDEO_R	29	AFILT1	41	NC
6	BIT_CLK	18	CD_L	30	AFILT2	42	AVss2
7	DVss2	19	CD_GND	31	NC	43	NC
8	SDATA_IN	20	CD_R	32	CAP2	44	NC
9	DVdd2	21	MIC1	33	NC	45	NC
10	SYNC	22	MIC2	34	NC	46	NC
11	nRESET	23	LINE_IN_L	35	LINE_OUT_L	47	NC
12	PC_BEEP	24	LINE_IN_R	36	LINE_OUT_R	48	NC

'n' denotes active low

APPENDIX A

APPLICATION NOTE FOR MIXED SUPPLY OPERATION

The DAC97S01 can operate from a 3.3V supply connected to DVdd while maintaining a 5V supply on AVdd. On-chip level shifters ensure accurate logic transfers between the analog and digital portions of the DAC97S01. If digital interface signals above 3.3V are used, then appropriate level shifting circuitry must be provided to ensure adequate digital noise immunity and to prevent on-chip ESD protection diodes from turning on.

In PC applications, one power supply input to the DAC97S01 may be derived from a supply regulator (as shown in Figure 20) and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the I.C. will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, the codec would be subject to on-chip SCR type latch-up.

SMSCs DAC97S01 allows power-up sequencing between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the codec. The I.C. is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.

Refer to Figure 20 on the following page.

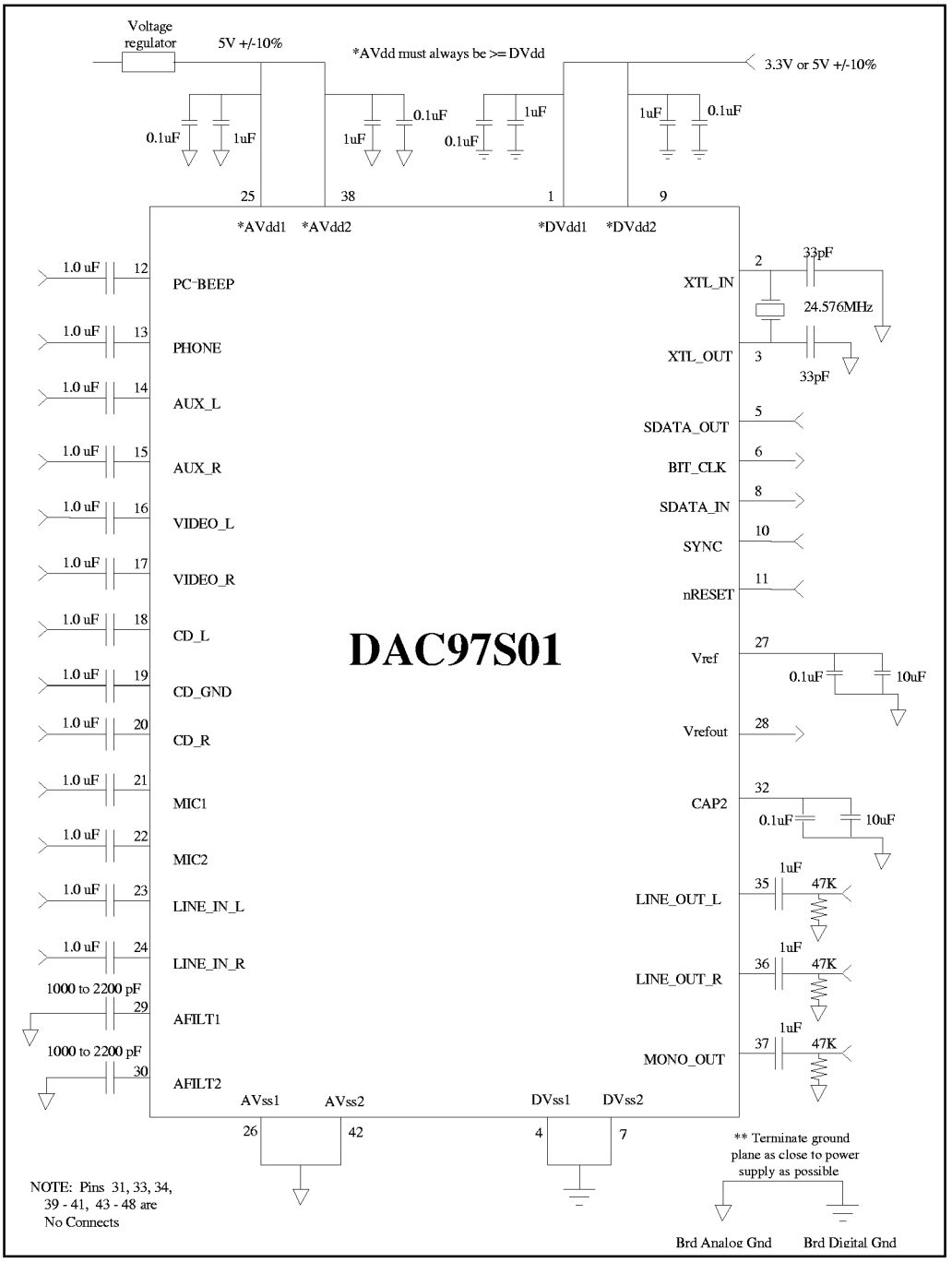

FIGURE 20 – MIXED SUPPLY OPERATION

APPENDIX B

The DAC97S01 is capable of operating from a single 5V supply connected to both DVdd and Avdd (as shown in Figure 21). Even though the DAC97S01 has digital switching levels of 0.2Vdd to 0.5Vdd (See AC Link Electrical Characteristics in this data book), we recommend that all digital interface signals to the AC-Link be 5V. If digital interface signals below 5V are used, then appropriate level shifting circuitry must be provided to ensure adequate digital noise immunity and to prevent on-chip ESD protection diodes from forward biasing. Refer to Figure 21 on the following page.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	SUPPLY RANGE
DAC97S01T	48 Pin TQFP 7mmx 7mm x 1.4mm	0^{o} C to $+70^{o}$ C	DVdd = 3.3V – 5V, AVdd = 5V

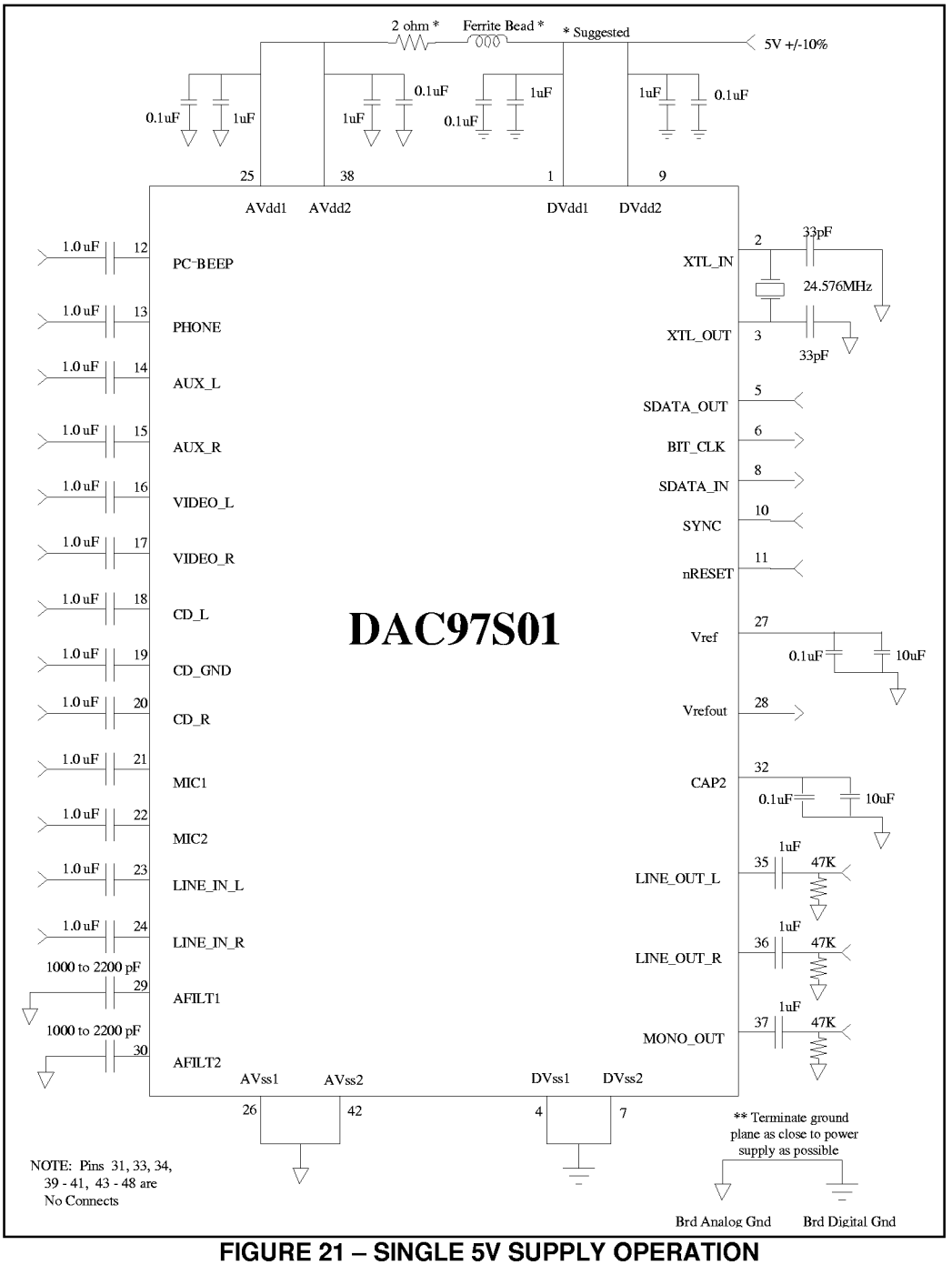

FIGURE 21 – SINGLE 5V SUPPLY OPERATION

Circuit diagrams utilizing SMSC products are included as a means of illustrating typical applications; consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any licenses under the patent rights of SMSC or others. SMSC reserves the right to make changes at any time in order to improve design and supply the best product possible. SMSC products are not designed, intended, authorized or warranted for use in any life support or other application where product failure could cause or contribute to personal injury or severe property damage. Any and all such uses without prior written approval of an Officer of SMSC and further testing and/or modification will be fully at the risk of the customer.

DAC97S01 Rev. 4/17/98