1024-Bit Dynamic Shift Registers Quad, Dual, Single

SY1402A, SY1403A, SY1404A

MEMORY PRODUCTS

Synertek® INCORPORATED

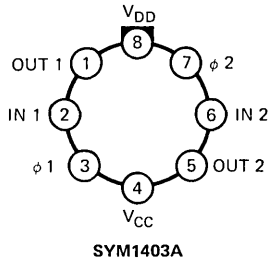
- Synertek ion implanted silicon gate process
- 5 MHz data rate—minimum
- 2.5 MHz clock rate
- TTL, DTL compatible
- Reduced clock capacitance, 85 pF
- Reduced power dissipation, 80 μW/bit at 1.0 MHz

The SY1402A, 1403A and 1404A 2ϕ dynamic shift registers utilize I/O multiplexing techniques to attain a 5.0 MHz data rate with a clock rate of only 2.5 MHz. The inputs and outputs are bipolar and MOS compatible for ease of implementation in a TTL, DTL and a high- or low-threshold MOS system.

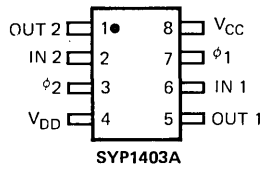
Clock power and V_{DD} current have been significantly reduced due to the advantages inherent in an ion implanted silicon gate design over a conventional silicon gate design. These savings directly affect the cost of the overhead circuitry (clock drivers, power supplies) for a shift register memory system.

The SY1402A, 1403A and 1404A are used effectively in applications requiring low cost serial memory such as CRT refresh, line and page storage for facsimile transmitters and receivers, and character storage for high speed printers.

PIN CONFIGURATION

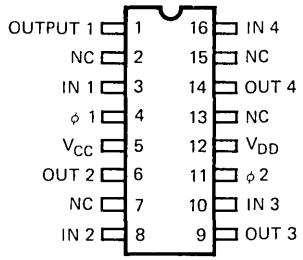


SYM1403A



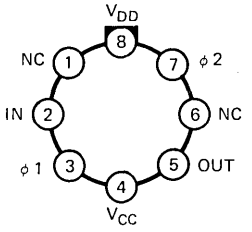
SYP1403A

PIN CONFIGURATION

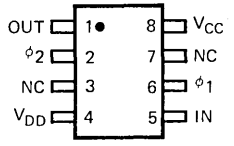


SYP1402A
SYC1402A

PIN CONFIGURATION



SYM1404A



SYP1404A

ORDERING INFORMATION

Order Number	Package Type	Organization	Temperature Range
SYP1404A	Plastic Dip	1024 x 1	0°C to +70°C
SYM1404A	TO Can	1024 x 1	0°C to +70°C
SYP1403A	Plastic Dip	512 x 2	0°C to +70°C
SYM1403A	TO Can	512 x 2	0°C to +70°C
SYP1402A	Plastic Dip	256 x 4	0°C to +70°C
SYC1402A	Ceramic Dip	256 x 4	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS [1]

Temperature Under Bias	0°C to 70°C	Data and Clock Input Voltages and Supply Voltages with respect to V_{CC}	+0.5V to −20V
Storage Temperature	−65°C to +160°C		
Power Dissipation [2]	1 Watt		

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = +5V ±5%, unless otherwise specified

V_{DD} = −5V ±5% or −9V ±5%

Symbol	Test	Min.	Typ.[3]	Max.	Unit	Conditions
I_{LI}	Input Load Current		<10	500	nA	T_A = 25°C
I_{LO}	Output Leakage Current		<10	1000	nA	V_{OUT} = 0.0V, T_A = 25°C
I_{LC}	Clock Leakage Current		10	1000	nA	Max. V_{ILC}, T_A = 25°C
V_{IL}	Input "Low" Voltage	V_{CC}−10		V_{CC}−4.2	V	
V_{IH}	Input "High" Voltage	V_{CC}−2		V_{CC}+.3	V	
V_{DD} = −5V ±5%						
I_{DD1}	Power Supply Current		15	20	mA	T_A = 25°C; Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC} = V_{CC}−17V
I_{DD2}	Power Supply Current			22	mA	T_C = 0°C; Output at Logic "0", 5 MHz Data Rate, 33% Duty Cycle, Continuous Operation, V_{ILC} = V_{CC}−17V
V_{ILC}	Clock Input Low Voltage	V_{CC}−17		V_{CC}−15	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1} = 3K to V_{DD}, I_{OL} = 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1} = 3K to V_{DD}, I_{OH} = −100μA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.6	V_{CC}−1		V	R_{L2} = 4.7K to V_{DD} (See p. 4 for connection)
V_{DD} = −9V ±5%						
I_{DD3}	Power Supply Current		15	20	mA	T_A = 25°C; Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC} = V_{CC}−14.7V
I_{DD4}	Power Supply Current			22	mA	T_C = 0°C; Output at Logic "0", 3 MHz Data Rate, 26% Duty Cycle, Continuous Operation, V_{ILC} = V_{CC}−14.7V
V_{ILC}	Clock Input Low Voltage	V_{CC}−14.7		V_{CC}−12.6	V	
V_{IHC}	Clock Input High Voltage	V_{CC}−1		V_{CC}+.3	V	R_{L1} = 4.7K to V_{DD}, I_{OL} = 1.6 mA
V_{OL}	Output Low Voltage		−.3	0.5	V	R_{L1} = 4.7K to V_{DD}, I_{OL} = 1.6 mA
V_{OH1}	Output High Voltage Driving TTL	2.4	3.5		V	R_{L1} = 4.7K to V_{DD}, I_{OH} = −100 μA
V_{OH2}	Output High Voltage Driving MOS	V_{CC}−1.9	V_{CC}−1		V	R_{L2} = 6.2K to V_{DD}, R_{L3} = 3.9K to V_{CC} (See p. 4 for connection)

Note 1: Stresses listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The 1 watt dissipation is not to be construed,as an operating rating (see note 1). For operating at elevated temperatures the device must be derated based as shown on page 4. When operating at V_{DD} = −5V±5% the maximum duty cycle is 33% and at V_{DD} = −9V+5% the maximum duty cycle is 26%. In applications the duty cycle should be a minimum to reduce power dissipation. Duty cycle = $[t_{\phi PW} + 1/2\,(t_R + t_F)]$ x clock rate.

Note 3: Typical values are at T_A = 25°C and at nominal voltages.

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

Symbol	Test	$V_{DD} = -5V \pm 5\%$ (Test Load 1)		$V_{DD} = -9V \pm 5\%$ (Test Load 2)		Unit
		Min.	Max.	Min.	Max.	
Frequency	Clock Rep Rate		2.5		1.5	MHz
Frequency	Data Rep Rate	Note 1	5.0	Note 1	3.0	MHz
$t_{\phi PW}$	Clock Pulse Width	.130	10	.170	10	μsec
$t_{\phi D}$	Clock Pulse Delay	10	Note 1	10	Note 1	nsec
t_R, t_F	Clock Pulse Transition		1000		1000	nsec
t_{DW}	Data Write Time (Set Up)	30		60		nsec
t_{DH}	Data To Clock Hold Time	20		20		nsec
t_{A+}, t_{A-}	Clock To Data Out Delay		90		110	nsec

CAPACITANCE [2] $V_{CC} = +5V \pm 5\%$, $V_{DD} = -5V \pm 5\%$ or $-9V \pm 5\%$, $T_A = 25°C$

Symbol	Test	Typ.	Max.	Conditions	
C_{IN}	Input Capacitance	5 pF	10 pF	$V_{IN} = V_{CC}$	f = 1 MHz
C_{OUT}	Output Capacitance	5 pF	10 pF	$V_{OUT} = V_{CC}$	
C_ϕ	Clock Capacitance	70 pF	85 pF	$V_\phi = V_{CC}$	
$C_{\phi 1 \phi 2}$	Clock to Clock Capacitance	11 pF	16 pF	$V_\phi = V_{CC}$	

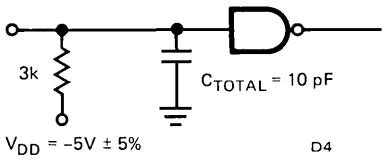
Note 1: See page 4 for guaranteed curve. Note 2: This parameter is periodically sampled and is not 100% tested.

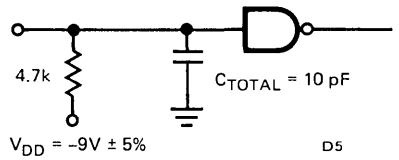
SWITCHING CHARACTERISTICS

Conditions of Test

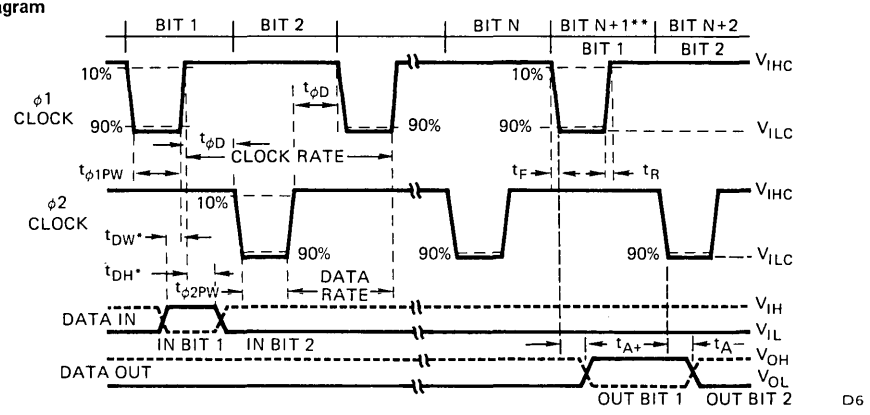
Input rise and fall times: 10 nsec

Output Load is 1 TTL gate



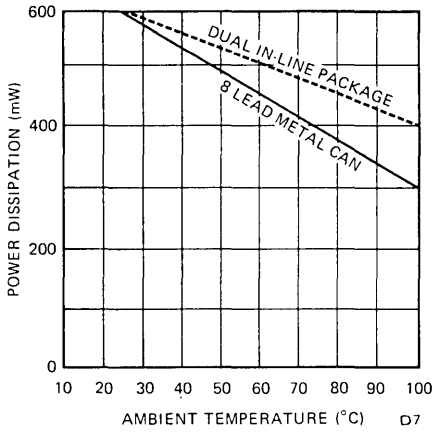


Timing Diagram

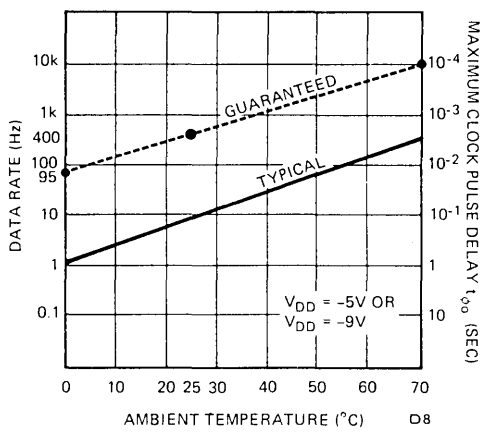


*t_{DW} and t_{DH} same for $t_{\phi 2}$ **N: 256 for SY1402A, N=512 for SY1403A, N=1024 for SY1404A

TYPICAL CHARACTERISTICS

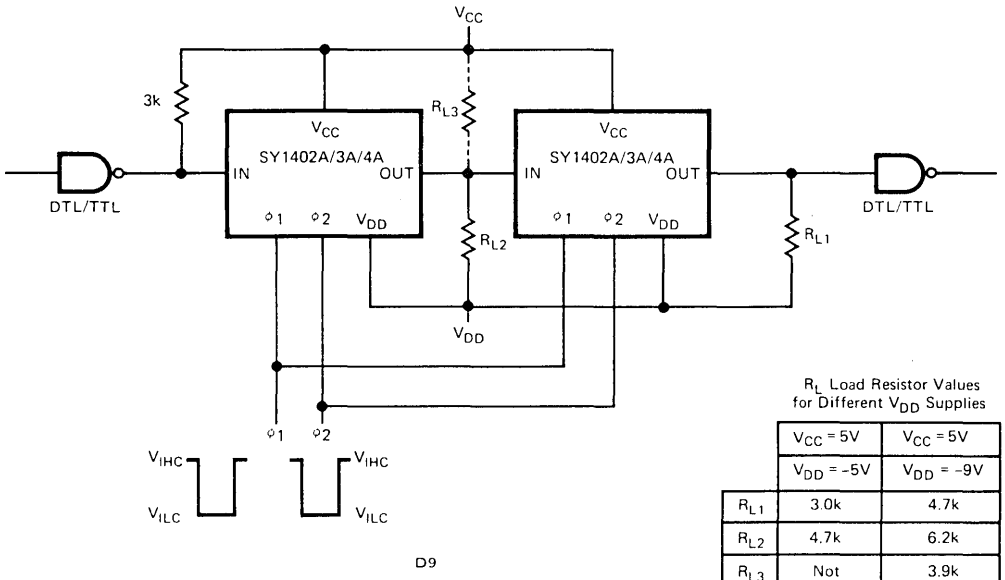


MAXIMUM ALLOWABLE POWER DISSIPATION



MINIMUM OPERATING DATA RATE OR MAXIMUM CLOCK PULSE DELAY VS. TEMPERATURE

DTL/TTL MOS Interfaces



R_L Load Resistor Values for Different V_{DD} Supplies

	V_{CC} = 5V, V_{DD} = -5V	V_{CC} = 5V, V_{DD} = -9V
R_{L1}	3.0k	4.7k
R_{L2}	4.7k	6.2k
R_{L3}	Not required	3.9k