TC8607F

Floppy Disk Mechanism Controller

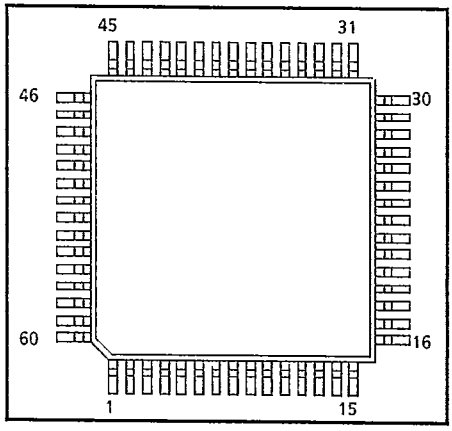
1. GENERAL DESCRIPTION

TC8607F is a single chip C-MOS LSI for the floppy disk drive digital control logic, consisting of a 4 bit CPU and required random logic. This LSI has input terminal for direct reception of the floppy disk drive system interface terminal inputs, such controls as step-motor, etc, which are the internal mechanisms of floppy drive, and read/write circuit control signal inputs, and the digital control board in the present floppy disk drive can be replaced by this LSI.

TC8607F has a firmware already mounted to the ROM of the built-in CPU and therefore, is readily usable for 5.25inch floppy disk drive.

2. FEATURES

- Low power consumption by the Si-gate C-MOS technology
- Fully compatible with TLCS-47 4 bit CPU
- System interface directly connected input terminals (TTL compatible threshold)
- Various specifications on 5.25inch floppy disk drive
- Various application for stepping motor driver
- Built-in R/W IC control circuit
- FDD aging function
- Built-in sensor (Photo-diode) input
- 60 PIN mini FP



NO.	IO	PIN NAME	NO.	IO	PIN NAME
1	I	-DIR	31	I	AUTOCK
2	I	-SISEL	32	O	NC
3	I	-DC1R	33	O	DSOUT
4	I	-DS	34	O	HLEN (SWEL0)
5	I	RDDPI	35	O	HLPS (SWTP2)
6	O	HD0	36	O	-HISP
7	O	-ERA	37	O	RWFTR1
8	O	-WE	38	O	DSKIN
9	O	SWFTR1	39	O	IUOUT
10	I	TEST	40	O	MTREN
11	I	XIN	41	O	PHASE2
12	O	XOUT	42	O	PHASE1
13	I	-CLR	43	O	SMPS
14	I	NC	44	O	PWRON
15	I	-WPSNS	45	G	VSS
16	I	-TZSNS	46	O	DSKCHG
17	I	IXSNS	47	O	TRK00
18	I	-DC2R	48	O	INDEX
19	I	-DISNS	49	O	READY
20	I	-INUSE	50	O	WP
21	I	-HLOAD	51	O	RDDPO
22	I	FWSEL0	52	O	HLDRDY
23	V	VDD	53	V	VDD
24	G	VSS	54	G	VSS
25	I	FWSEL1	55	I	-HACTV
26	I	MECNT	56	I	-HMHD (SWSEL0)
27	I	MODE	57	I	-WG
28	I	DCSEL	58	I	-LWDEN
29	I	MPSTP	59	I	-MTRON
30	I	SPSEEK	60	I	-STEP

3. TC8607F and APPLICATION SYSTEM

3.1 OUTLINE

TC8607F is a floppy disk mechanism controller (FDMC) provided with the various option selecting functions for 5.25 inch floppy disk drive (FDD). Through selecting the functions, the standard 5.25 inch FDD can be fabricated with the functions shown below.

3.1.1 DISK TYPE SELECT

□ 500K byte and 1.0M byte drive

These types are of the FDD construction which can fabricate the 96 TPI and the 48 TPI models by means of employing the 1-phase/1-track or 2-phase/1-track as the stepping motor track shifting mode through using the same structural parts except the R/W head.

□ 1.0M byte/1.6M byte compatible drive

This is the user programmable drive type with the external input of the drive.

1.0M byte mode :	Rotation speed 300 rpm Data transfer rate 250 Kbps Number of tracks 80
1.6M byte mode :	Rotation speed 360 rpm Data transfer rate 500 Kbps Number of tracks 77

These modes are changed over during the normal operation.

3.1.2 OPTION SELECT

□ MULTI PHASE SHIFTING FUNCTION

TC8607F has a function that can select 3 kinds mode, 1 phase/1 track, 2 phase/1 track and 4 phase/1 track for 1 step pulse. This function is effective for the case which products FDD both 48 TPI and 96 TPI model using the same structural parts except for head parts and which advances precision of positioning the heads.

□ AUTOMATIC CHUCKING FUNCTION

The FDMC has a function that rotates spindle motor instantaneously when the disk is inserted, so as to get correct chucking of diskette holing mechanism. The spindle motor rotation sustains until detecting internal READY or till one second passed.

☐ SPECIAL SEEK FUNCTION

The special seek is a function that postpones the recalibrate function at power on time, so as to avoid rush current through the all drives by doing the recalibrate operation. The function is suitable for battery operation type personal computer. If this function is selected the FDMC do nothing when the power is on. But the FDMC memorized the status for executing special seek operation when the FDMC receives first step pulse. In that case, when the FDMC receives first step pulse after power is up, the FDMC examines TRACK 0 status and if it is active (ACTIVE means on track 0), the FDMC transfer motor phase toward inner direction even if [DIR] input was outer seek. This operation will continue until detecting non-track 0 in each operation. This function is same as the step in sequence in the automatic return to zero (refer to Section 5.1.2). And because of the first step pulse applied for disk drive is outer direction issued by floppy disk controller, the recalibrate operation completes precisely.

3.2 SYSTEM OUTLINE

The position of the FDMC in the FDD (Floppy Disk Drive) is shown in FIG.3.2. The TC8607F receives the control signal from the host to control the drive digitally. While the read/write signal of the FDD is processed by the R/W IC, the timing of the write enable and the erase enable are properly controlled by the TC8607F. As the structural parts of FDD, the stepping motor for head positioning and the spindle motor for media rotating are provided. The TC8607F generates the signals necessary for controlling these structural parts.

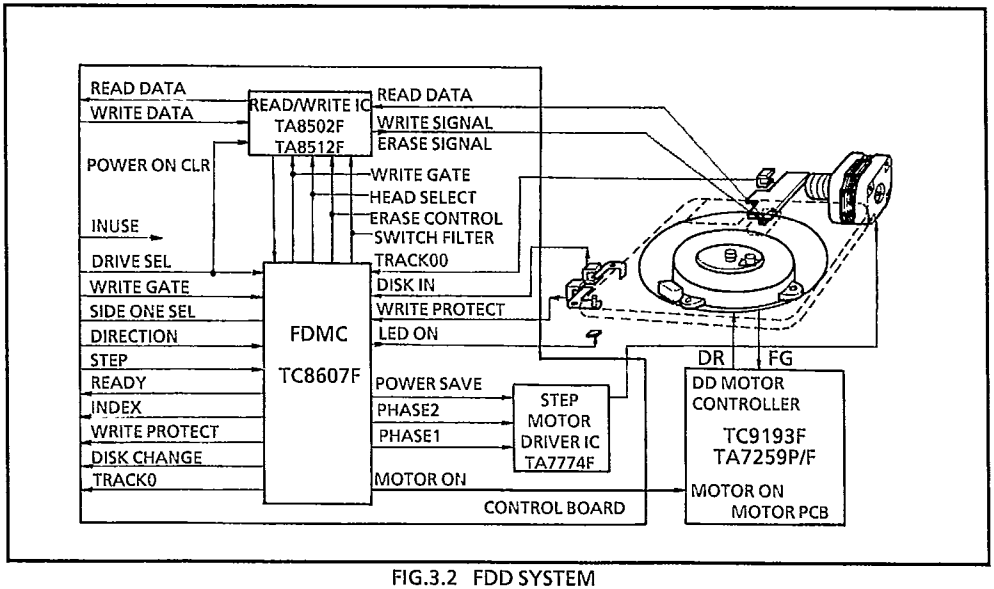


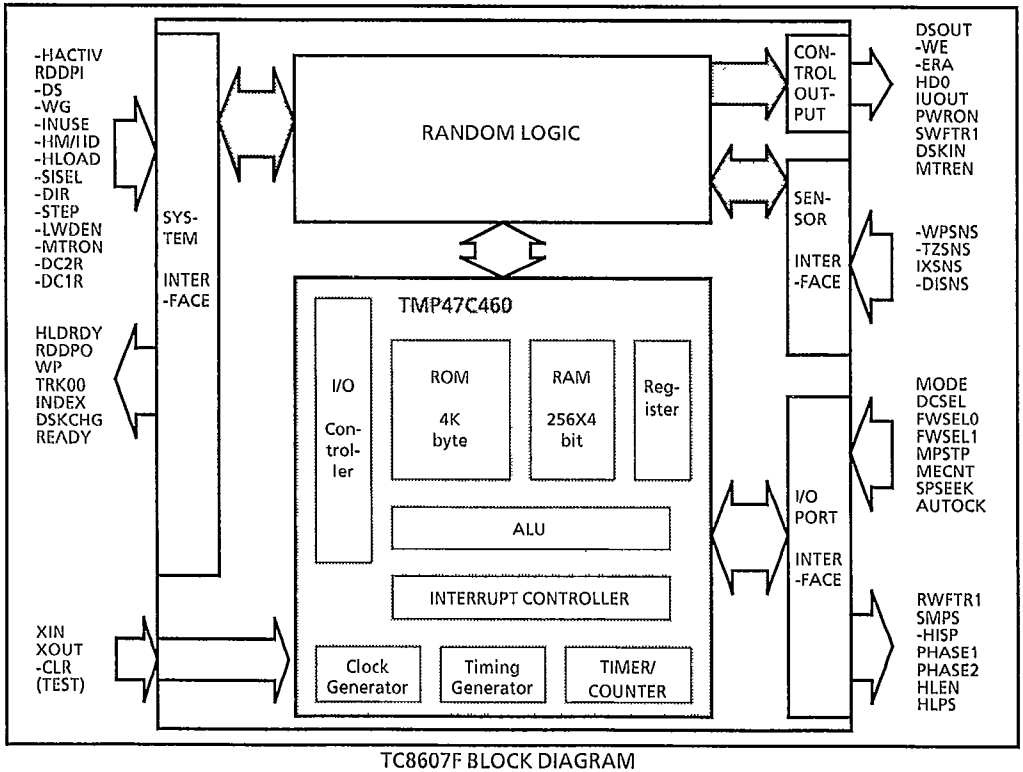
FIG.3.2 FDD SYSTEM

3.2.1 OUTLINE of SYSTEM OPERATION

The initializing operation and the normal operation are available as the system operation using the TC8607F. By the initializing operation, the function selection input is read to select the various functions and the initialization of the structural parts is performed. As the initialization of the structural parts, the operation (re-calibration) is available which moves the head to the track 0 to make the track counter is the TC8607F matched to the physical position of the head.

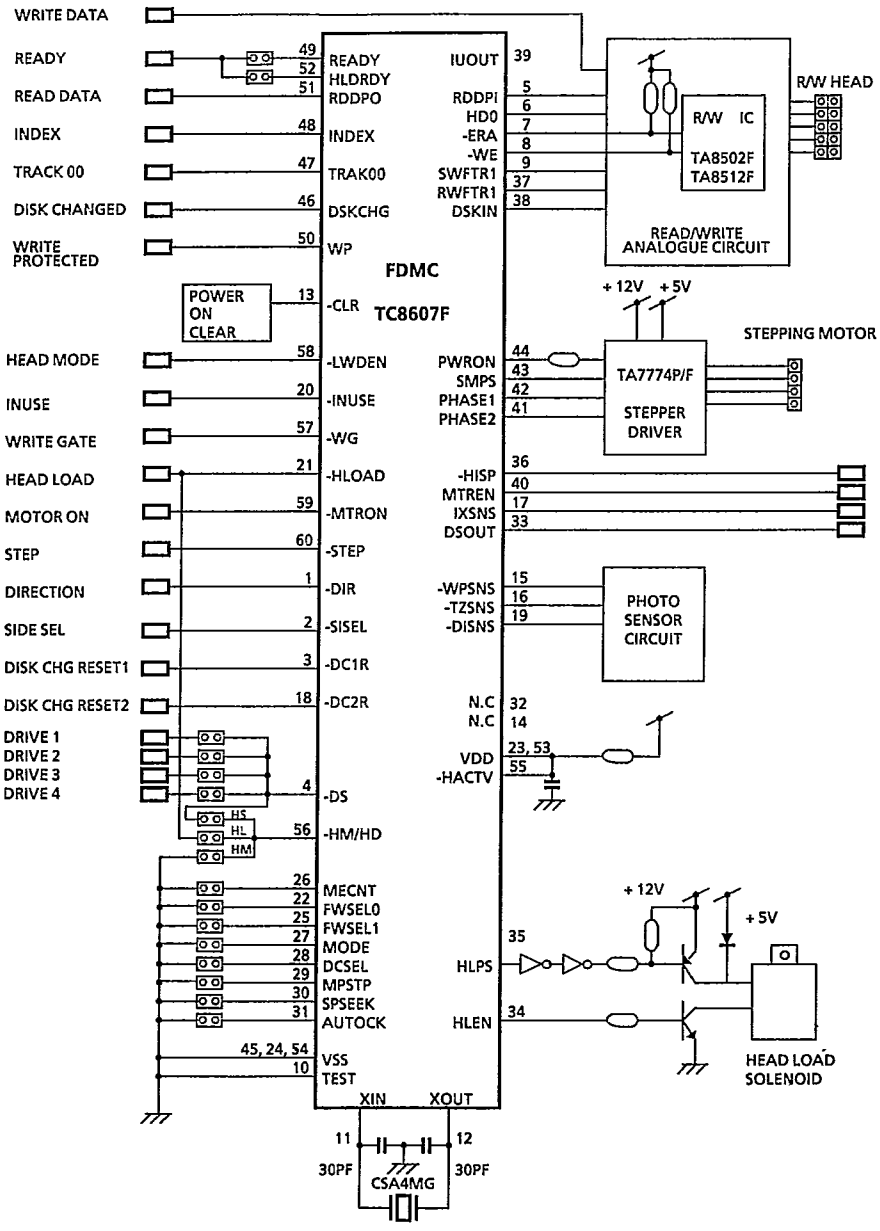
The operation of the stepping motor with the external step pulse, the generation of the ready signal with the index pulse detection, the automatic chucking operation with the disk-in detection and the processing of the write enable (WE) and erase enable (ERA) generated depending on the write signal from the system are available as the normal operations. In these processing, the parameters for various timings are available, of which values are determined by the value that is read during the initializing operation and the state of the program terminal which is repeatedly by the polling loop during the normal operation.

3.3 BLOCK DIAGRAM



TC8607F BLOCK DIAGRAM

3.4 EXAMPLE of SYSTEM STRUCTURE



FLOPPY DISK MECHANISM CONTROLLER

4. PIN DESCRIPTION

NO.	PIN NAME	IO	FUNCTION
1	-DIR	I	Connect to DIRECTION terminal of system interface.
2	-SISEL	I	Connect to SIDE SELECT terminal of system interface.
3	-DC1R	I	Disk Change Reset signal input terminal.
4	-DS	I	Connect to DRIVE SELECT n terminals of system interface.
5	RDDPI	I	Input for READ DATA output of read/write IC.
6	HD0	O	R/W circuit control signal. Head 0 select signal.
7	-ERA	O	R/W circuit control signal. The delayed erase signal for tunnel erase head is supplied in negative logic. Open drain output.
8	-WE	O	R/W circuit control signal. Write enable signal for head is supplied in negative logic. Open drain output.
9	SWFTR1	O	R/W circuit control signal. Output for controlling the parameter of read/write circuit with relation to track position. This signal will be activated when the track position is inner than 44 track (60 track is also selectable).
10	TEST	I	Test pin of LSI which is normally kept at low level.
11	XIN	I	Ceramic oscillating resonator connection pin.
12	XOUT	O	Ceramic oscillating resonator connection pin.
13	-CLR	I	System reset pin of LSI. Low level signal is needed for the initialization of LSI when power is on application.
14	NC	I	This terminal don't use, normally is kept at low level or open (Non connect).
15	-WPSNS	I	Sensor input. Signal, which becomes Low level in state the disk is protected, is input.
16	-TZSNS	I	Sensor input. Signal, which becomes low level in state the head is located on 0 track, is input.
17	IXSNS	I	Sensor input. Index signal is input in positive logic.
18	-DC2R	I	Disk Change Reset signal input terminal.
19	-DISNS	I	Sensor input. Signal, which becomes low level in state the disk is inserted, is input.
20	-INUSE	I	Connect to INUSE terminal of system interface.
21	-HLOAD	I	Connect to HEAD LOAD terminal of system interface.
22	FWSEL0	I	Program input for function selection. 3-valued threshould input terminal.
23	[VDD]	I	Power supply input of LSI. + 5V is supplied.
24	[VSS]	I	Power supply input of LSI. Connection to GND of FDD circuit.

NO.	PIN NAME	IO	FUNCTION
25	FWSEL1	I	Program input for function selection. 3-valued threshould input terminal.
26	MECNT	I	Program input for function selection and for rotate condition selection of spindle motor.
27	MODE	I	Input for operation mode selection. Program input for function selection of HEAD LOAD, low-density output and track-zero output.
28	DCSEL	I	Input for selection of DISK CHANGE RESET. Open this terminal, and select DC1R, low level this terminal, and select DC2R.
29	MPSTP	I	Program input for function selection. This terminal can select for 4 kinds mode, (1 phase, 2phase and 4 phase sending) to 1 step.
30	SPSEEK	I	Program input for function selection.
31	AUTOCK	I	Program input for function selection.
32	NC	O	This terminal don't use.
33	DSOUT	O	Positive logic output of [-DS] input of system interface. When [-CLR] is at high level and [-DS] is at low level at the same time, output becomes high level.
34	HLEN	O	Head load control output. High level output on Head Road Solenoid at power on time.
	-LWDLHO	O	Signal output for latch -LWDLH input by falling edge of -DS input.
35	HLPS	O	Head Load Power save control output. This output pin will be activated to High level when the system cut off + 12V power supply to Head-Load -Power.
	-SWFTR2	O	R/W head drive circuit control signal. Output for control a fixed number of read-write circuit relation to track position. Track number becomes high level more than 60.
36	-HISP	O	Spindle motor control output. When the rotation speed of spindle motor is 300rpm, output becomes high level, and when it is 360rpm, output becomes low level.
37	RWFTR1	O	R / W head drive circuit control output. Output becomes high level in 1MB mode, and output becomes low level in 1.6MB mode.
38	DSKIN	O	Disk-in output.
39	IUOUT	O	Positive logic output of -INUSE input.
40	MTREN	O	Spindle motor control output. Used at high level with spindle motor set to on. Controlled by [-MTRON] of system interface input and auto chucking function.
41	PHASE2	O	Stepping motor phase control output. 2nd phase.
42	PHASE1	O	Stepping motor phase control output. 1st phase.

FLOPPY DISK MECHANISM CONTROLLER

NO.	PIN NAME	IO	FUNCTION
43	SMPS	O	This output pin will be activated to High level when the system cut off the + 12V power supply to stepping motor.
44	PWRON	O	Power supply control output for stepping motor. Output becomes low level for power-down on the condition of stand-by. Power control of stepping motor and R/W circuit.
45	[VSS]	I	Power supply pin of LSI. Connected to GND of FDD circuit.
46	DSKCHG	O	Connect to -DISK CHANGE terminal of system interface.
47	TRK00	O	Connect to -TRACK0 terminal of system interface.
48	INDEX	O	Connect to -INDEX terminal of system interface.
49	READY	O	Connect to -READY terminal of system interface.
50	WP	O	Connect to -WRITE PROTECTED terminal of system interface.
51	RDDPO	O	AND output of READ DATA from read/write IC and DRIVE SELECT of system interface.
52	HLDRDY	O	Hold ready output terminal. Though the preparing condition for hold ready is the same as that for READY, once the ready state is obtained, the active state is maintained until the power supply is turned off or the disk is pulled out.
53	[VDD]	I	Power supply pin of LSI. + 5V is supplied.
54	[VSS]	I	System ground pin of LSI.
55	-HACTV	I	Output mode of each output terminal of [WP], [TRK00], [INDEX], [DSKCHG], [READY], [HLDRDY] or [RDDPO] is controlled. When this terminal is at low level, each output terminal is turned into the mode in which each terminal is connected to the system interface terminal via the open collector inverting buffer. When this terminal is at high level, each output terminal is turned into the mode in which each output terminal is directly connected to system interface terminal.
56	-HM/HD	I	Input terminal for selection of head load condition.
	-LWDLH	I	Input of output signal for -LWDLHO latch.
57	-WG	I	Connect to WRITE GATE terminal of system interface.
58	-LWDEN	I	Connect to low density terminal of system interface.
59	-MTRON	I	Input terminals for spindle motor control. Connect to Motor on terminal of system interface on low active signal.
60	-STEP	I	Connect to STEP terminal of system interface.

5. FUNCTIONAL SPECIFICATION

5.1 FUNCTION SELECTION

5.1.1 DRIVE MODE SELECTION

The TC8607F is provided with nine kind of function selection terminals (FWSEL0, FWSEL1, -LWDEN, DCSEL, MPSTP, SPSEEK, AUTOCK, MECNT, MODE). Among them, four inputs of -LWDEN, FWSEL0, FWSEL1, DCSEL are repeatedly evaluated during the normal operation, however, the other five inputs are evaluated only when LSI's power is on (after -CLR is released from low level to high level).

The function selection performs the control over the index interval (ready preparing requirement) effective for each drive model, the change for rotation mode of motor and the fixed number selection for R/W head drive circuit as shown in TABLE 5.1.1a by the three terminals of -LWDEN, FWSEL0, and FWSEL1. Also at of high density/low density compatible drive mode, the erase delay timing is set to make read/write possible in both modes. TABLE 5.1.1b shows the erase delay timings determined by the function selection terminals (-LWDEN, FWSEL0, and FWSEL1)

TABLE 5.1.1a FUNCTION SELECTION MAP 1

FWSEL0	FWSEL1	-LWDEN	FDD MODEL *1	MODEL MODE	NUMBER OF TRACKS	Spindle Rotational Frequency*2	Rotation MODE	-HISP OUTPUT	INDEX INTERVAL
L	L	L	0.5MB	0.5MB	40	300rpm	300rpm	H	160-240ms
L	L	H						H	160-240ms
L	H	L	0.5MB	1.0MB	80	300rpm	300rpm	H	160-240ms
L	H	H						H	160-240ms
H	L	L	1.6/1MB	1.0MB	80	300/360rpm	300rpm	H	160-240ms
H	L	H	1.6/1MB	1.6MB	77	300/360rpm	360rpm	L	126-240ms
H	H	L	1.6/1MB	1.0MB	80	360rpm	360rpm	L	126-240ms
H	H	H	1.6/1MB	1.6MB	77	360rpm	360rpm	L	126-240ms

TABLE 5.1.1b FUNCTION SELECTION MAP 2

FWSEL0	FWSEL1	-LWDEN	FDD MODEL *1	MODEL MODE	ERASE TIMING (μs)		RWFTR1	CHANGE OVER TRACK POSITION
					ON DELAY	OFF DELAY		
L	L	L	0.5MB	0.5MB	296-312	916-932	H	22
L	L	H			296-312	916-932	L	44
L	H	L	0.5MB	1.0MB	296-312	916-932	H	44
L	H	H			296-312	916-932	L	44
H	L	L	1.6/1MB	1.0MB	104-118	596-612	H	44
H	L	H	1.6/1MB	1.6MB	152-168	484-500	L	44
H	H	L	1.6/1MB	1.0MB	104-118	500-512	H	44
H	H	H	1.6/1MB	1.6MB	152-168	484-500	L	44

*1 : 1.6/1MB means a type of FDD which can be modified 1.6M byte or 1M byte in using same mechanism

*2 : Rotation speed prepared for the drive is indicated.

5.1.2 FUNCTIONAL SELECTION by SPSEEK and AUTOCK

Special seek function can be always selected by High or Open on [MODE] input. In case of "Low" on [MODE] input, special seek function can be selected by making [SPSEEK] input high level and Automatic-Return-to-Zero Function can be selected by making [SPSEEK] input low level. Also, by making [AUTOCK] input high level, Automatic Chucking Function can be selected.

SPECIAL SEEK FUNCTION

The special seek is a function that postpones the recalibrate function at power on time, so as to avoid rush current through the all drives by doing the recalibrate operation. This function is suitable for battery operation type personal computer.

☐ AUTOMATIC RETURN-to-ZERO FUNCTION

The automatic Return-to-Zero function is a kind of initializing operation which performs re-calibration of track position. This sequence is divided two parts that is, power-on-step-in and Return-to-Zero seek.

POWER-ON-STEP-IN OPERATION

In this operation, for the first time, the track-zero sensor input is evaluated and if the evaluation result is active (ACTIVE means that [-TZSNS] input is low level), then FDMC executes inner seek step by step until track-zero sensor is non active. 12 steps (24 phases) are passed over at maximum with the seek rate of 3ms per track. After the track-zero sensor is non active, even if before first time of stepping operation, FDMC goes to next procedure, (the Return-to-Zero operation) starts after settling time of 15ms for head assembly.

Return-to-Zero OPERATION

In this operation, FDMC executes outer seek operation until the stepping motor phase becomes 00 ([PHASE1], [PHASE2], are both at high level) with the track-zero-sensor being active. The seeking is performed 100 tracks (200phases) at maximum. After 100 tracks seek is done, the operation ends even if the head does not reach the track-zero position.

The power on step in sequence is for the safe operation in such a drive that has elastic carriage stopper at the track zero position, so as to keep precision avoiding mechanical collision. But using such mechanism causes wrong track recalibration, in case that head is located outer track 0, even if start at negative track position by the residue of former status of disk drive.

☐ AUTOMATIC CHUCKING FUNCTION

The FDMC has a function that rotates spindle motor instantaneously when disk is inserted, so as to get correct chucking of diskette holing mechanism. The spindle motor rotation sustains until detecting internal READY or till one second passed.

5.1.3 MULTI-PHASE SENDING FUNCTION

By matching [MPSTP], [FWSEL0] and [FWSEL1], 2 phase/1tack, 4 phase/1track mode are selected as shown TABLE 5.1.3. After the output of the first phase, the second phase in 2 phase/1 track mode and the second, the third, the forth phase in 4 phase/1 track mode are outputted for 1 step of system interface at the phase rate as defined in TABLE 5.1.3. This function is effective in case of producing both 48TPI and 96TPI model FDD using the same structural parts except for the head, or developing accuracy of positioning the head.

TABLE 5.1.3 PHASE RATE, STEP RATE SELECTION FUNCTION

MPSTP	FWSEL0	FWSEL1	STEP MODE	PHASE RATE	Phase rate (at ARZ) *1
L	L	L	1 PHASE/1TRACK	–	6.0ms
L	L	H	1 PHASE/1TRACK	–	3.0ms
L	H	L	1 PHASE/1TRACK	–	3.0ms
L	H	H	1 PHASE/1TRACK	–	3.0ms
Z	L	L	2 PHASE/1TRACK	3.0ms	6.0ms
Z	L	H	2 PHASE/1TRACK	2.0 + 1.0ms	3.0ms
Z	H	L	2 PHASE/1TRACK	2.0 + 1.0ms	3.0ms
Z	H	H	2 PHASE/1TRACK	2.0 + 1.0ms	3.0ms
H	L	L	4 PHASE/1TRACK	2.0ms + 1.0ms + 2.0ms + 1.0ms	6.0ms
H	L	H	4 PHASE/1TRACK	2.0ms + 1.0ms + 2.0ms + 1.0ms	3.0ms
H	H	L	4 PHASE/1TRACK	2.0ms + 1.0ms + 2.0ms + 1.0ms	3.0ms
H	H	H	4 PHASE/1TRACK	2.0ms + 1.0ms + 2.0ms + 1.0ms	3.0ms

*1 : Automatic-Return-to-Zero

5.1.4 SPINDLE MOTOR ROTATING CONDITION SELECTION FUNCTION

By [MECNT] input, spindle motor rotating condition are selected as shown TABLE 5.1.4

TABLE 5.1.4 SPINDLE MOTOR ROTATING CONDITION SELECTION FUNCTION

MECNT	SPINDLE MOTOR ROTATION CONDITION
High	Only MTRON, without off-delay
Open	MTRON*DI, without off-delay
Low	MTRON*DI, with off-delay

Off-delay time is set in 2.5ms

FLOPPY DISK MECHANISM CONTROLLER

5.1.5 DISK CHANGE RESET INPUT SELECTION FUNCTION

Either [-DC1R] or [-DC2R] can be selected as the disk change reset input by [DCSEL] input. The internal equivalence circuit of [-DC1R] and [-DC2R] is shown TABLE 5.1.5

[DSKCHG] output is the logical AND of the internal FF output which is selected by [DCSEL] input of two internal FF as shown FIG. 5.1.5 and the positive logic signal of [-DS] input.

TABLE 5.1.5 DISK CHANGE RESET INPUT SELECTION FUNCTION

DCSEL	DCR INPUT	FUNCTION
High	-DC1R	Test mode is selected. Aging mode or track zero regulation mode can select by mode input.
Open	-DC1R	[-DC1R] has logical add with outer input [-DS], and its signal rise resets internal FF.
Low	-DC2R	When [-DC2R] falls on the disk-in condition, it resets internal FF.

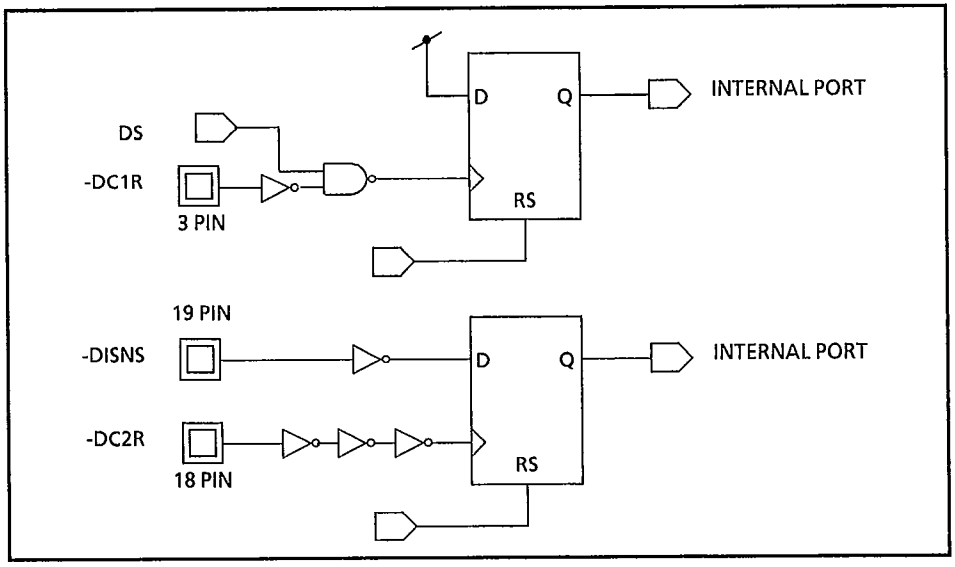


FIG. 5.1.5 DISK CHANGE MONITORING CIRCUIT

5.1.6 TRACK-ZERO REGULATION, AGING MODE SELECTION FUNCTION

Either Track-zero Regulation or Aging mode can be selected by [DCSEL] and [MODE] input. When [DCSEL] is at High level in power on time, then Track zero Regulation Mode or Aging Mode can be selected as shown TABLE 5.1.6 by [MODE] input. TC8607F has logical stopper in the seek operation and doesn't seek outer 0 track and inner than 83 track. When Track zero Regulation Mode is selected, logic stopper comes off, then it is possible to seek to minus track. Step mode and phase rate are selected by [MPSTP], [FWSEL0] and [FWSEL1] shown in TABLE 5.1.3. When Aging Mode is selected, it seeks between the most inner track in the selected drive mode and 0 track repeatedly. Step mode and phase rate are selected by [MPSTP], [FWSEL0] and [FWSEL1].

TABLE 5.1.6 TRACK-ZERO REGULATION, AGING MODE SELECTION FUNCTION

DCSEL	MODE	OPERATION MODE
High	Low	Aging mode
	Open	Track zero regulation mode
	High	
Open	*	Normal operation mode
Low	*	

* : Don't care

5.1.7 DRIVE MODE SELECTION FUNCTION

Either the drive which has the head load function or the drive which has the low density output and use [SWFTR2] as the switch filter can be selected by [MODE] input as shown in TABLE 5.1.7. At the same time, Track Zero output condition is selected by [MODE] input as shown in below.

TABLE 5.1.7 DRIVE MODE SELECTION FUNCTION

MODE	34 PIN	36 PIN	56 PIN	TRACK ZERO OUTPUT CONDITION	
				1 PHASE/1 TRACK	2 PHASE, 4 PHASE /1 TRACK
High	HLEN	HLPS	-HM/HD	Condition 1	Condition 1
Open	-LWDLHO	SWFTR2	-LWDLH	Condition 1	Condition 2
Low	HLEN	HLPS	-HM/HD	Condition 1	Condition 2

Condition 1 : [-TZSNS] = Low and [PHASE1] = [PHASE2] = High
Condition 2 : [-TZSNS] = Low and [PHASE2] = High

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6. ELECTRICAL CHARACTERISTICS

6.1 ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V (GND)

SYMBOL	PARAMETER	RATINGS	UNIT
V_{DD}	Supply Voltage	-0.5 ~ +6.5	V
V_{IN}	Input Voltage	V_{SS}-0.5 ~ V_{DD} + 0.5	V
V_{OUT}	Output Voltage	V_{SS}-0.5 ~ V_{DD} + 0.5	V
T_{STG}	Storage Temperature	-55 ~ +125	°C
T_{OPR}	Operating Temperature	-30 ~ +70	°C
I_{OUT1}	Output Current each Terminal	± 3 (Output Group 1) *	mA
I_{OUT2}	Output Current each Terminal	± 8 (Output Group 2) *	mA
P_D	Power Dissipation	300	mW

(note) If LSI is used above the maximum ratings, permanent destruction of LSI can result. In addition, it is desirable to use LSI for normal operation under the recommended conditions. If these conditions are exceeded, reliability of LSI may be adversely affected.

*Output Group 1 : HD0 , -ERA , -WE , SWFTR1 , XOUT , DSOUT, HLEN , HLPS, -HISP, RWFTR1, DSKIN, IUOUT, MTREN, PHASE2, PHASE1, SMPS, PWRON
*Output Group 2 : DSKCHG , TRK00 , INDEX , READY , WP , RDDPO , HLDRDY

6.1.1 RECOMMENDED OPERATING CONDITIONS

V_{DD} = 5.0V , V_{SS} = 0V (GND)

SYMBOL	PARAMETER	CONDITION	MIN.	MAX.	UNIT
T_{OPR}	Operating Temperature		-30	+70	°C
V_{DD}	Supply Voltage		4.5	5.5	V
f_c	Clock Frequency		3.9	4.1	MHz

6.2 DC CHARACTERISTICS

V_{DD} = 5.0V , V_{SS} = 0V (GND) , T_{OPR} = -30~70°C

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
V_{HS1}	Hysteresis Width (1)	Input Group 1	0.2	0.4		V
V_{HS2}	Hysteresis Width (2)	Input Group 2	0.4	0.6		V
I_{IH}	Input High Level Current	V_{IH} = 5.0V	-2.0		2.0	μA
I_{IL1}	Input Low Level Current (1)	V_{IL} = 0.0V Input Group A with Pull-up device	-30		-5	μA
I_{IL2}	Input Low Level Current (2)	V_{IL} = 0.0V Input Group B with Pull-up device	-150		-25	μA
I_{IL3}	Input Low Level Current (3)	V_{IL} = 0.0V RDDPI, TEST Input	-2.0		2.0	μA
V_{IH1}	Input High Level Voltage (1)	Input Group 1	2.1		V_{DD}	V
V_{IL1}	Input Low Level Voltage (1)	Input Group 1	0.0		0.6	V
V_{IH2}	Input High Level Voltage (2)	Input Group 2	2.8		V_{DD}	V
V_{IL2}	Input Low Level Voltage (2)	Input Group 2	0.0		1.0	V
V_{IH3}	Input High Level Voltage (3)	Input Group 3	3.0		V_{DD}	V
V_{IL3}	Input Low Level Voltage (3)	Input Group 3	0.0		2.0	V
V_{IH4}	Input High Level Voltage (4)	Input Group 4	3.5		V_{DD}	V
V_{IL4}	Input Low Level Voltage (4)	Input Group 4	0.0		1.5	V

FLOPPY DISK MECHANISM CONTROLLER

V_{DD} = 5.0V , V_{SS} = 0V (GND) , T_{OPR} = -30~70°C

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.	MAX.	UNIT
I_{OH1}	Output High Level Current (1)	V_{OH} = 4.6V Output Group 1			-2.0	mA
I_{OL1}	Output Low Level Current (1)	V_{OL} = 0.4V Output Group 1	2.0			mA
I_{OH2}	Output High Level Current (2)	V_{OH} = 4.6V Output Group 2			-6.0	mA
I_{OL2}	Output Low Level Current (2)	V_{OL} = 0.4V Output Group 2	6.0			mA
I_{OL1}	Output Low Level Current (3)	V_{OL} = 0.4V -WE, -ERA output	2.0			mA
I_{OFL1}	Output Off Leak Current (1)	V_0 = 0~5V Output Group 2 and、-WE,-ERA output	-2.0		2.0	μA
I_{DD}	Operating Consumption Current	f_c = 4MHz		2	4	mA

*Input Group 1 : -DIR, -SISEL , -DC1R , -DS , RDDPI , -INUSE, -HLOAD, -HM/HD, -WG, -LWDEN, -MTRON, -STEP
*Input Group 2 : -CLR , -WPSNS , IXSNS, -DC2R, -DISNS
*Input Group 3 : -TZSNS
*Input Group 4 : TEST , XIN , FWSEL0 , FWSEL1, MECNT, MODE, DCSEL, MPSTP, SPSEEK, AUTOCK, -HACTV
*Input with Pull-up device (RIN = 500KΩ)
Input Group A : -WPSNS , IXSNS , -DISNS , -DC2R
*Input with Pull-up device (RIN = 100KΩ)
Input Group B : All input terminals except -WPSNS , IXSNS , -DISNS , -DC2R, RDDPI, TEST, XIN, and -TZSNS
*Output Group 1 : HD0, SWFTR1, XOUT, DSOUT, HLEN, HLPS, -HISP, RWFTR1, DSKIN, IUOUT, MTREN, PHASE1, PHASE2, PWRON, SMPS
*Output Group 2 : DSKCHG , TRK00 , INDEX , READY , WP , RDDPO , HLDRDY

6.3 AC CHARACTERISTICS

6.3.1 PULSE WIDTH

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{WSP}	Step Pulse Width	500			ns

6.3.2 TRANSMISSION DELAY CHARACTERISTICS

SYMBOL	PARAMETER				MIN.	TYP.	MAX.	UNIT
t_{WEL}	-WG FALL	→ -WE FALL			–	–	200	ns
t_{WEH}	-WG RISE	→ -WE OFF			–	–	500	ns
t_{IFL}	-DS FALL	→ DSOUT DSKCHG TRK00 INDEX READY WP RDDP0 HLDRDY	RISE RISE RISE RISE RISE RISE RISE RISE	*1	–	–	200	ns
t_{IFH}	-DS RISE	→ DSOUT DSKCHG TRK00 INDEX READY WP RDDP0 HLDRDY	FALL FALL FALL FALL FALL FALL FALL FALL	*1	–	–	200	ns
t_{IEN}	-DS FALL	→ ENABLE SYSTEM INTERFACE OUTPUT		*2	–	–	200	ns
t_{IDE}	-DS RISE	→ DISABLE SYSTEM INTERFACE OUTPUT		*2	–	–	200	ns
t_{HDH}	-SISEL RISE/-WE and -ERA RISE	→ HD0	RISE		–	–	200	ns
t_{HDL}	-SISEL FALL/-WE and -ERA RISE	→ HD0	FALL		–	–	200	ns
t_{RDH}	RDDPI RISE	→ RDDP0	RISE/FALL	*3	–	–	200	ns
t_{RDL}	RDDPI FALL	→ RDDP0	FALL/RISE	*3	–	–	200	ns
t_{SNH}	IXSNS RISE WPSNS RISE	→ INDEX → WP	RISE/FALL RISE/FALL	*3	–	–	200	ns
t_{SNL}	IXSNS FALL WPSNS FALL	→ INDEX → WP	FALL/RISE FALL/RISE	*3	–	–	200	ns
t_{DS}	SET UP TIME	-STEP ↓ → DIR			–	–	200	ns
t_{DH}	HOLD TIME	-STEP ↓ → DIR			–	–	200	ns

*1 : -HACTV = LOW
*2 : -HACTV = HIGH
*3 : -DS = Low, -HACTV = High

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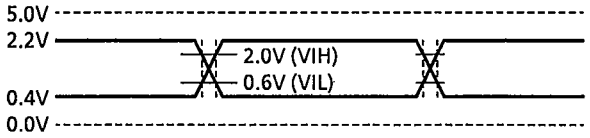
6.3.3 TESTING WAVEFORM

(VDD = + 5V)

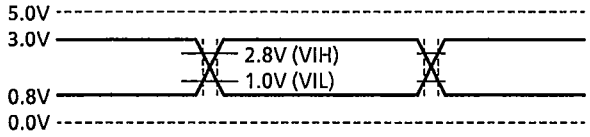
LSTTL Compatible Input Terminals

Input terminal Group 1 : -DIR, -SISEL, -DC1R , -DS , RDDPI, -INUSE, -HLOAD, -HM/HD, -WG, -LWDEN, -MTRON , -STEP



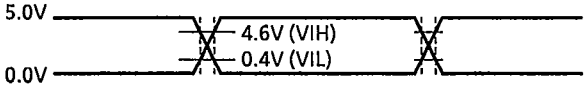
Sensor Input Terminals

Input terminal group 2 : -CLR, -WPSNS, -TZSNS, IXSNS, -DC2R, -DISNS

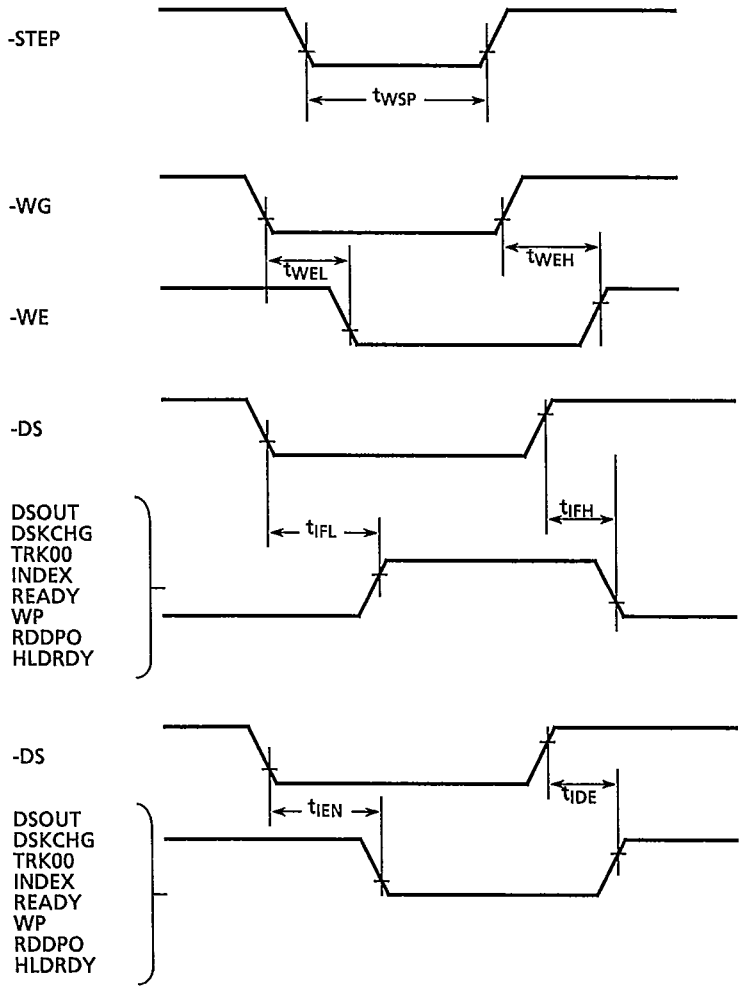


The Other Input Terminals

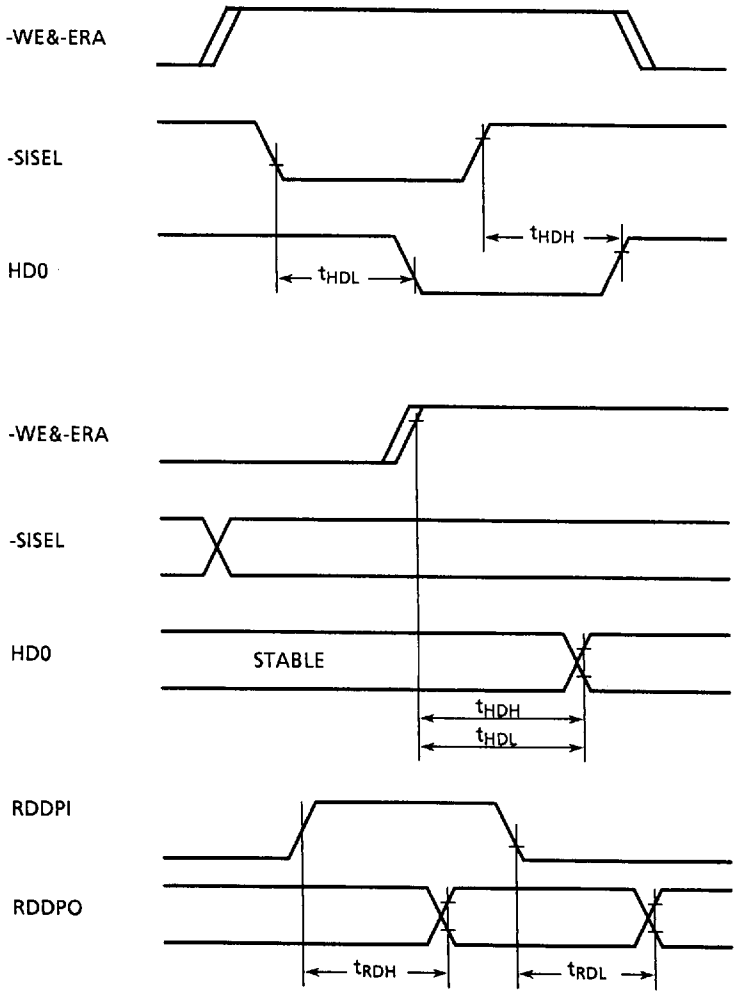
Input terminal group 3 : TEST, XIN, FWSEL0, FWSEL1, MECNT, MODE, DCSEL, MPSTP, SPSEEK, AUTOCK, -HACTV

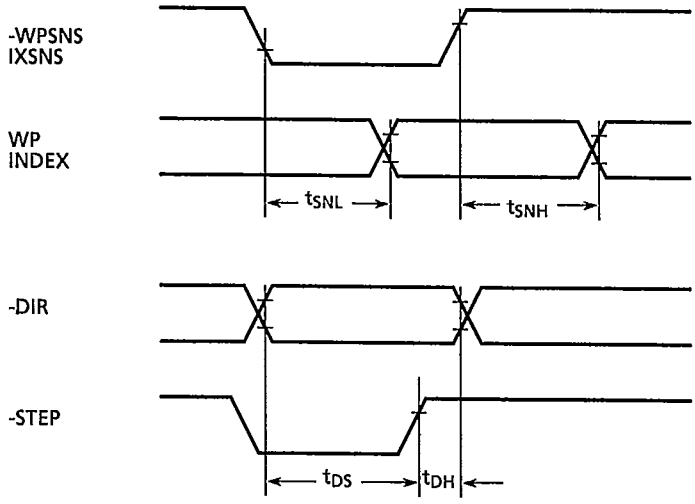


6.3.4 TIMING WAVEFORM



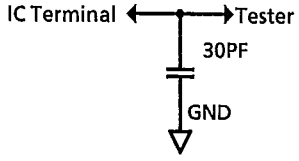
FLOPPY DISK MECHANISM CONTROLLER



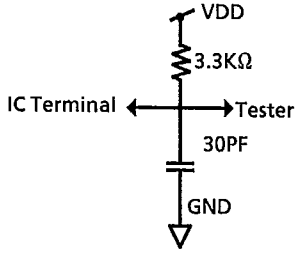


6.3.5 TESTING TERMINAL LOAD

CMOS OUTPUT TERMINAL



OPEN DRAIN OUTPUT



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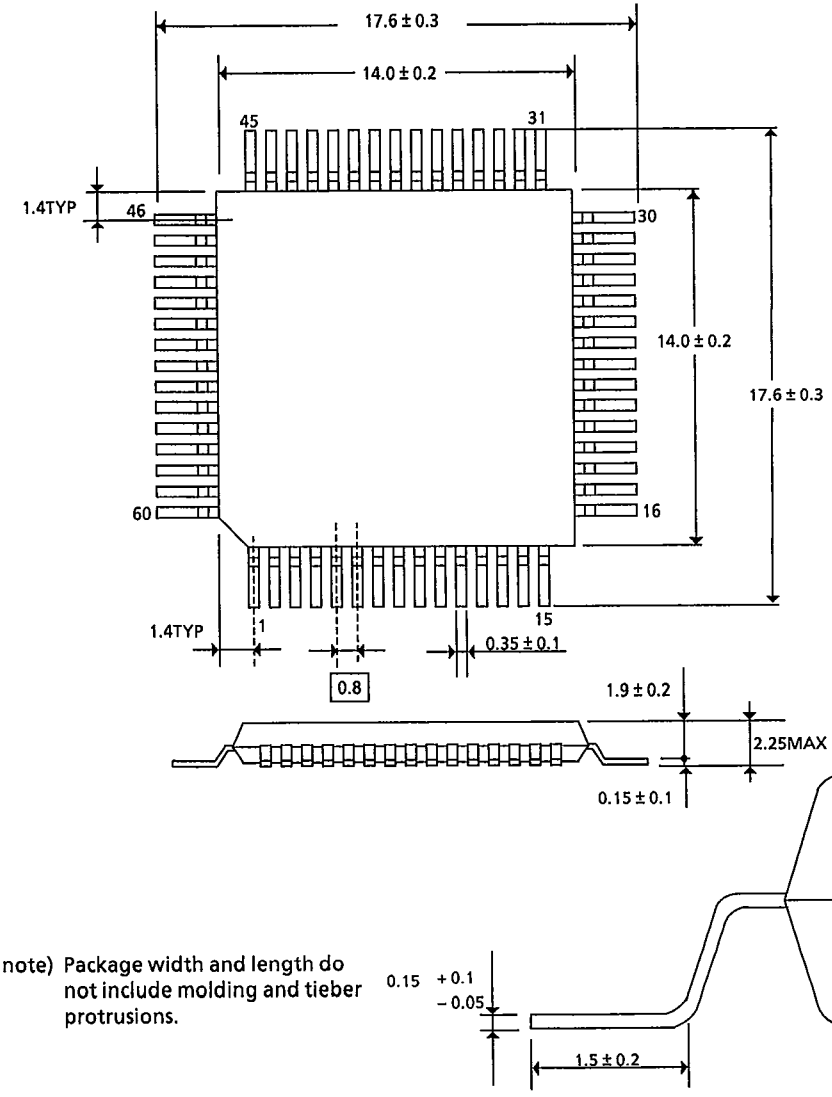
7. PACKAGE DIMENSION

QFP60-P-1414A

Unit : mm



note) Package width and length do not include molding and tieber protrusions.