The FlexSet™ PC/AT Integrated Peripheral Controller SL9030

PRELIMINARY

FEATURES

- Pin to Pin Replacement for VLSI VL82C100.
- IBM PC/AT Compatible.
- Replaces 22 Logic Devices.
- Supports up to 25 MHz System Clock.
- Seven DMA Channels.
- 14 External Interrupt Requests.
- Three Programmable Timer/Counter Channels.
- Compatible with all VIA FlexSet Chipsets.
- Designed in 1.2 micron CMOS Process.
- JEDEC - Standard 84-pin PLCC.

DESCRIPTION

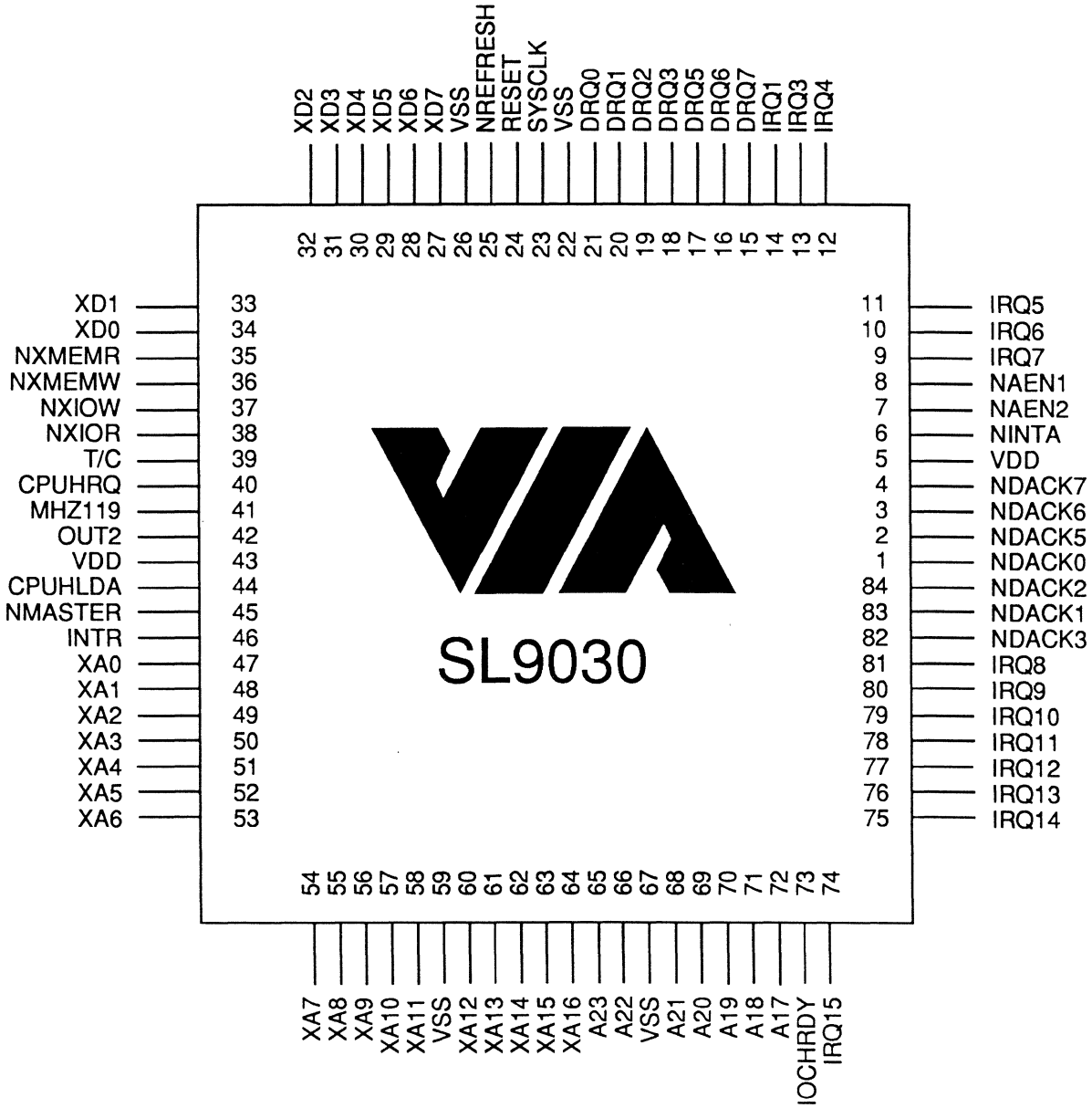
The SL9030 Integrated Peripheral Controller replaces two 82C37A Direct Memory Access Controllers, two 82C59A Interrupt Controllers, an 82C54 Programmable Counter, a 74LS612 AT Memory Mapper, two 74ALS373 Octal Three-State Latches, a 74ALS138 3-to-8 Decoder, and other less-complex TTL devices. The SL9030 provides 24 address bits for 16M bytes of DMA address space. It also interfaces directly to the CPU to handle all interrupts. Arbitration between refresh and DMA hold requests are performed by the SL9030.

The device is manufactured with an advanced high-performance 1.2 micron CMOS process and is available in a JEDEC-standard 84-pin plastic leaded chip carrier (PLCC) package. The SL9030 is part of the PC/AT-compatible FlexSet chip sets from VIA Technologies.

June 1991
2.061391

VIA Technologies, Inc. (408) 746-2200
860 East Arques Avenue
Sunnyvale, CA 94086

PINOUT


XD2 32
XD3 31
XD4 30
XD5 29
XD6 28
XD7 27
VSS 26
NREFRESH 25
RESET 24
SYSCLK 23
VSS 22
DRQ0 21
DRQ1 20
DRQ2 19
DRQ3 18
DRQ5 17
DRQ6 16
DRQ7 15
IRQ1 14
IRQ3 13
IRQ4 12
XD1 33
XD0 34
NXMEMR 35
NXMEMW 36
NXIOW 37
NXIOR 38
T/C 39
CPUHRQ 40
MHZ119 41
OUT2 42
VDD 43
CPUHLDA 44
NMASTER 45
INTR 46
XA0 47
XA1 48
XA2 49
XA3 50
XA4 51
XA5 52
XA6 53
11 IRQ5
10 IRQ6
9 IRQ7
8 NAEN1
7 NAEN2
6 NINTA
5 VDD
4 NDACK7
3 NDACK6
2 NDACK5
1 NDACK0
84 NDACK2
83 NDACK1
82 NDACK3
81 IRQ8
80 IRQ9
79 IRQ10
78 IRQ11
77 IRQ12
76 IRQ13
75 IRQ14
SL9030
54 XA7
55 XA8
56 XA9
57 XA10
58 XA11
59 VSS
60 XA12
61 XA13
62 XA14
63 XA15
64 XA16
65 A23
66 A22
67 VSS
68 A21
69 A20
70 A19
71 A18
72 A17
73 IOCHRDY
74 IRQ15

FUNCTIONAL DESCRIPTION

The SL9030 Integrated Peripheral Controller integrates two 8237 DMA controllers, two 8259 interrupt controllers, one 8254 counter/timer and a 74LS612 equivalent along with support logic onto a single chip. The peripheral controller will replace all of the logic on the X bus of an AT-compatible design except the KeyboardController and Real Time Clock.

The SL9030 consists of five major subsections. The megacell chip select subsection decodes the signals MASTER, CPUHLDA, and the address bus XA0-XA9. This decoder is used to generate the chip select signals for each of the megacells within the SL9030.

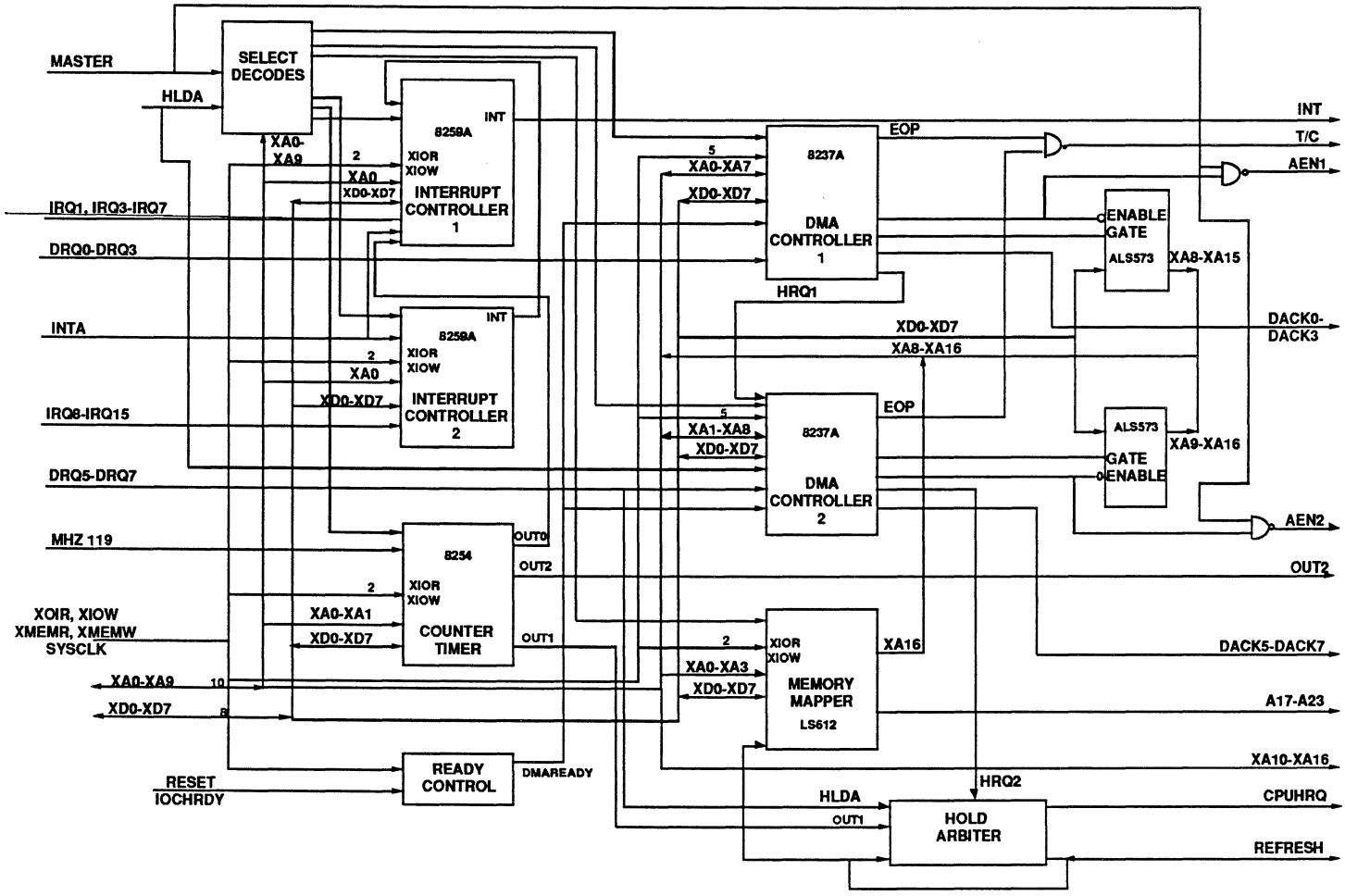
The DMA subsection consists of two 8237 megacells, two 8 bit latches to hold the middle range address bits during a DMA cycle and a 74LS612 equivalent megacell to generate the upper range address bits during a DMA operation. The DMA subsection also has logic to force all DMA cycles to have one wait state inserted and additional logic to delay the leading edge of the XMEMR signal for one DMA clock cycle. These functions are used to maintain AT-compatibility. The DMA subsection provides a total of seven external DMA channels. Four of these channels are used for 8 bit I/O adapters and the other three are used for 16 bit I/O adapters. All channels are capable of addressing all memory locations in a 16 megabyte address space.

The interrupt controller subsection consists of two 8259 megacells cascaded together to accept 14 possible interrupt sources.

The counter/timer subsection contains a single 8254 megacell. This megacell has three internal counters. All of the counters are clocked at a 1.19 MHz rate. Gate inputs to counter 0 and 1 are always enabled (tied high). Gate 2 is connected to the Q output of a flip-flop. The D input of this flip-flop is bit 0 of the X Data and is clocked by port B write decode. The output of Counter 0 is routed to the interrupt controller subsection to be used as interrupt request 0. The output from Counter 1 is routed to the hold request arbiter to initiate refresh cycles. Counter 2's output is available as an external pin.

The hold request arbiter and refresh subsection is used to arbitrate between a possible hold request from the DMA subsection or Counter 1 of the counter/timer subsection. This block of logic also controls the REFRESH output signal.

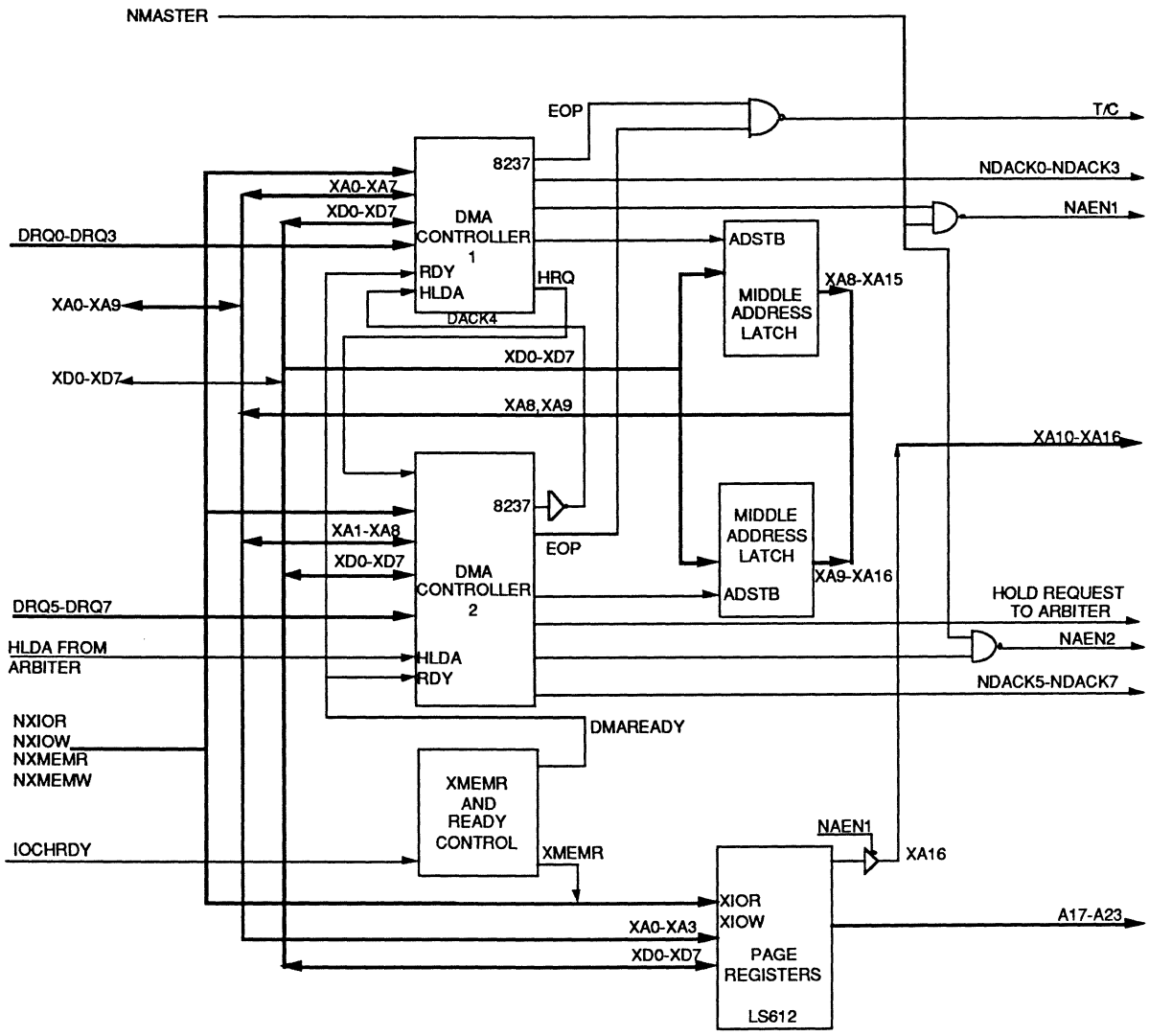
BLOCK DIAGRAM SL9030



DMA SUBSECTION

The DMA subsection controls DMA transfers between an I/O channel and on-board or off-board memory. It generates a hold request to the CPU when an I/O channel requests a DMA operation. Once the hold has been acknowledged, the DMA controller will drive all 24 address bits for a total addressing capability of 16 megabytes, and drive the appropriate bus command signals depending on whether the DMA is a memory read or write. The DMA controllers are 8237 compatible, internal latches are provided for latching the middle address bits output by the 8237 megacells on the data bus and the function of a 74LS612 memory mapper is provided to generate the upper address bits.

Fig. 1 DMA Subsection



DMA CONTROLLERS

The SL9030 supports seven DMA channels using two 8237 equivalent megacells capable of running at a 5 MHz DMA clock (10 MHz SYSCLK) rate. DMA Controller 1 contains channels 0 through 3. These channels support 8 bit I/O adapters. Channels 0 through 3 are used to transfer data between 8 bit peripherals and 8 or 16 bit memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data up to a maximum of 64 kilobytes per page.

DMA Controller 2 contains channels 4 through 7. Channel 4 is used to cascade DMA Controller 1, so it is not available externally. Channels 5 through 7 support 16 bit I/O adapters to transfer data between 16 bit I/O adapters and 16 bit system memory. A full 24 bit address is output for each channel so they can all transfer data throughout the entire 16 megabyte system address space. Each channel can transfer data up to a maximum of 128 kilobytes per page. Channels 5, 6, and 7 are meant to transfer 16 bit words only and cannot address single bytes in system memory.

The 8237 can assume seven separate states, each composed of one full clock period. State 1 (S1) is the idle state. It is entered when the 8237 has no valid DMA requests pending, at the end of a DMA transfer sequence or when a reset or master clear has occurred.

State 0 (S0) is the first state of a DMA service. The 8237 has requested a hold but the processor has not yet returned an acknowledge. An acknowledge from the processor will signal that DMA transfers may begin. S1, S2, S3 and S4 are the working states of the DMA service. Wait States (SW) are inserted when more time is needed to complete a transfer.

The system clock to the SL9030 may be stopped when the DMA controllers are in the S1 state and the Refresh signal from the SL9030 is not used.

Note that for standby operation where the clock has been stopped, DMA requests will be ignored.

MEGACELL CHIP SELECTS

Address bits XA0-XA9 are used to generate chip selects for each of the individual megacells. A map of the address decode is shown in Table 1.

For all the address decodes shown, the chip selects are disabled if both CPUHLDA and MASTER are high. The address decode at address 061 hex goes to a single flip-flop used to clock in the value of TMGAT2 in an AT-compatible design. This flip-flop will clock in the value of XD0 on the rising edge of XIOW whenever that address decode is valid. The output of the flip-flop is used to gate counter 2 in the 8254 megacell. This is the only bit of Port B that is decoded by the SL9030 and it cannot be read externally. The entire Port B is decoded in the SL9025 of the FlexSet. Bit 0 is duplicated in the SL9030 only to save an input pin.

Table 1. Address Decode for Megacell Selects

XA9	XA8	XA7	XA6	XA5	XA4	XA3	XA2	XA1	XA0	Address Range	Megacell Selected
0	0	0	0	0	X	X	X	X	X	000-01F	DMA Controller 1 (8237)
0	0	0	0	1	X	X	X	X	X	020-03F	Int. Controller 1 (8259)
0	0	0	1	0	X	X	X	X	X	040-05F	Counter/Timer (8254)
0	0	0	1	1	0	X	X	X	1	061	Port B (TMGAT2)
0	0	1	0	0	X	X	X	X	X	080-09F	DMA Page Reg.
0	0	1	0	1	X	X	X	X	X	0A0-0BF	(74LS612)
0	0	1	1	0	X	X	X	X	X	0C0-0DF	Int. Controller 2 (8259)

DMA CONTROLLER REGISTERS

The 8237 megacells can be programmed any time CPUHLDA is inactive. Table 2 lists the addresses of all registers which can be read or written in the 8237 megacells. Addresses under DMA 2 are for the 16 bit DMA channels and DMA 1 corresponds to the 8 bit channels. When writing to a channel's address or word count register the data is written into both the base register and current register simultaneously. When reading a channel's address or word count register only the current address or word count can be read. The base address and base word count are not accessible for reading.

The address and word count registers for each channel are 16 bit registers. The value on the Xdata bus is written into the upper byte or lower byte depending on the state of the internal addressing flip-flop. This flip-flop can be cleared by the Clear Byte Pointer Flip-Flop command. After this command the first read/write to an address or word count register will read/write to the low byte of the 16 bit register and the byte pointer flip-flop will toggle to a one. The next read/write to an address or word count register will read/write to the high byte of the 16 bit register and the byte pointer flip-flop will toggle back to a zero.

The 8237 DMA controller megacells allow the user to program the active level (low or high) of the DRQ and DACK signals. Since the two megacells are cascaded together internally on the chip, these signals should always be programmed with the DRQ signals active high and the DACK signals active low.

When programming the 16 bit channels (channels 5, 6, and 7) the address which is written to the base address register must be the real address divided by two. Also, the base word count for the 16 bit channels is the number of 16 bit words to be transferred, not the number of bytes as is the case for the 8 bit channels. It is recommended that all internal locations, especially the mode register, in the 8237 megacells be loaded with some valid value. This should be done even if the channels are not used.

MIDDLE ADDRESS BIT LATCHES

The middle address bits of the 24 bit address range are held in two sets of 8 bit registers, one register for each DMA controller. The DMA controller will drive the value to be loaded onto the data bus and then issue an address strobe signal to latch the data bus value into these register. An address strobe is issued at the beginning of a DMA cycle and any time the lower 8 bit address increments across the 8 bit subpage boundary during block transfers. These registers cannot be written to or read externally. They are loaded only from the address strobe signals from the megacells and the outputs go only to the XA8-XA16 pins.

Table 2. DMA Controller Registers Addresses

Hex Address		Register Function
DMA2	DMA1	
0C0	000	Channel 0 Base and Current Address Register
0C2	001	Channel 0 Base and Current Word Count Register
0C4	002	Channel 1 Base and Current Address Register
0C6	003	Channel 1 Base and Current Word Count Register
0C8	004	Channel 2 Base and Current Address Register
0CA	005	Channel 2 Base and Current Word Count Register
0CC	006	Channel 3 Base and Current Address Register
0CE	007	Channel 3 Base and Current Word Count Register
0D0	008	Read Status Register/Write Command Register
0D2	009	Write Request Register
0D4	00A	Write Single Mask Register Bit
0D6	00B	Write Mode Register
0D8	00C	Clear Byte Pointer Flip-Flop
0DA	00D	Read Temporary Register/Write Master Clear
0DC	00E	Clear Mask Register
0DE	00F	Write All Mask Register Bits

PAGE REGISTERS

The equivalent of a 74LS612 is used in the SL9030 to generate the page registers for each DMA channel. The page registers provide the upper address bits during a DMA cycle. DMA addresses do not increment or decrement across page boundaries. Page boundaries for the 8 bit channels (channels 0 through 3) are every 64 kilobytes and page boundaries for the 16 bit channels (channels 5, 6, and 7) are every 128 kilobytes. There are a total of 16 eight bit registers in the 74LS612 megacell. The page registers are in the I/O address space as shown.

Page Register	Hex I/O Address
DMA channel 0	087
DMA channel 1	083
DMA channel 2	081
DMA channel 3	082
DMA channel 5	08B
DMA channel 6	089
DMA channel 7	08A
Refresh	08F

These registers must be written to select the correct page for each DMA channel before any DMA operations are performed. The other address locations between 080 and 08F that are not shown, are not used by the DMA channels but can be read or written to by the CPU. Address 08F is used to drive a value onto the upper address bits A17-A23 of the CPU's address bus during a refresh cycle.

Table 3. Address Source Generation

Outputs from 74LS612 Page Registers	Outputs from Middle Address Latches	Address Outputs from 8237	8 Bit DMA Address Bits	16 Bit DMA Address Bits
M7			A23	A23
M6			A22	A22
M5			A21	A21
M4			A20	A20
M3			A19	A19
M2			A18	A18
M1			A17	A17
M0			XA16	
	D7		XA15	XA16
	D6		XA14	XA15
	D5		XA13	XA14
	D4		XA12	XA13
	D3		XA11	XA12
	D2		XA10	XA11
	D1		XA9	XA10
	D0		XA8	XA9
		A7	XA7	XA8
		A6	XA6	XA7
		A5	XA5	XA6
		A4	XA4	XA5
		A3	XA3	XA4
		A2	XA2	XA3
		A1	XA1	XA2
		A0	XA0	XA1
		LOW		XA0

ADDRESS GENERATION

The DMA addresses are setup such that there is an upper address portion, used to select a specific page, a middle address portion, used to select a block within the page, and a lower address portion.

The upper address portion is generated by the page register, in the 74LS612 equivalent megacell. The page registers for each channel must be setup by the CPU before a DMA operation. DMA addresses do not increment or decrement across page boundaries. Page sizes are 64 kilobytes for 8 bit channels (channels 0 through 3) and 128 kilobytes for 16 bit channels (channels 5, 6, and 7). The DMA page register values are output on A17-A23 and XA16 for 8 bit channels, and A17-A23 for 16 bit channels.

The middle address portion, used to select a block within the page, is generated by the 8237 megacells at the beginning of a DMA operation and any time the DMA address increments or decrements through a block of boundary. Block sizes are 256 bytes for 8 bit channels (channels 0 through 3) and 512 bytes for 16 bit channels (channels 5, 6, and 7). This middle address portion is output by the 8237 megacells onto the data bus during state S1. The internal middle address bit latches will latch in this value. The middle address bit latches are output on XA8-XA15 for 8 bit channels, and XA9-XA16 for 16 bit channels.

The lower address portion is generated directly by the 8237 megacells during DMA operations. The lower address bits are output on XA0-XA7 for 8 bit channels, and XA1-XA8 for 16 bit channels. XA0 is forced low during 16 bit DMA operations.

Table 3 is shown to illustrate the source for all address bits during both 8 and 16 bit transfers.

READY CONTROL

The ready input to each of the 8237 megacells is driven from the same source within the ready control logic. To maintain an AT-compatible design, the SL9030 ready control logic forces one wait state on every DMA transfer. The external signal IOCHRDY goes into the ready control logic to extend transfer cycles longer than one wait state if needed. To add extra wait states, an external device should pull IOCHRDY low within the setup time before the second phase of the internal DMA clock during the forced wait state. The current DMA cycle will then be extended by inserting wait states until IOCHRDY is returned high. IOCHRDY going high must meet the setup time before the second phase of a wait state cycle or an extra wait state will be inserted before the DMA controller transitions to state S4 (see timing diagrams).

XMEMR DELAY

To maintain an AT-compatible design, the SL9030 inserts a DMA clock cycle delay in the falling edge of the XMEMR signal. XMEMR will go low one DMA clock (two SYSCLKs) later than the MEMR signal coming out of the 8237 megacell. The rising edge is not altered and will go high at the same time as the MEMR signal from the megacell goes high.

EXTERNAL CASCADING

An external DMA controller or bus master can be attached to an AT-compatible design through the DMA controllers. To add an external DMA controller, one of the seven available DMA channels must be programmed in cascade mode. That channel's DRQ signal should then be connected to the external DMA controller's HRQ output. The corresponding DACK signal for that channel should be connected to the external DMA controller's HLDA input. When one of the seven channels is programmed in cascade mode and that channel is acknowledged the DMA controller will not drive the data bus, the command signals, or the XA address bus. However, the upper address bits A17-A23 will be driven with the value programmed into the page register for the channel programmed in cascade mode.

An external device can become a bus master and control the system address, data, and command buses in much the same manner. One of the DMA channels must be programmed in cascade mode. The external device then asserts the DRQ line for that channel. When that channel's DACK line goes active, the external device can then pull the MASTER signal low to force the system buses to a high impedance state. As in the DMA controller cascading, the SL9030 will not drive the X buses while the cascaded channels DACK signal is active. Also, the SL9030 will force the upper address bits A17-A23 to a high impedance state while MASTER is held low.

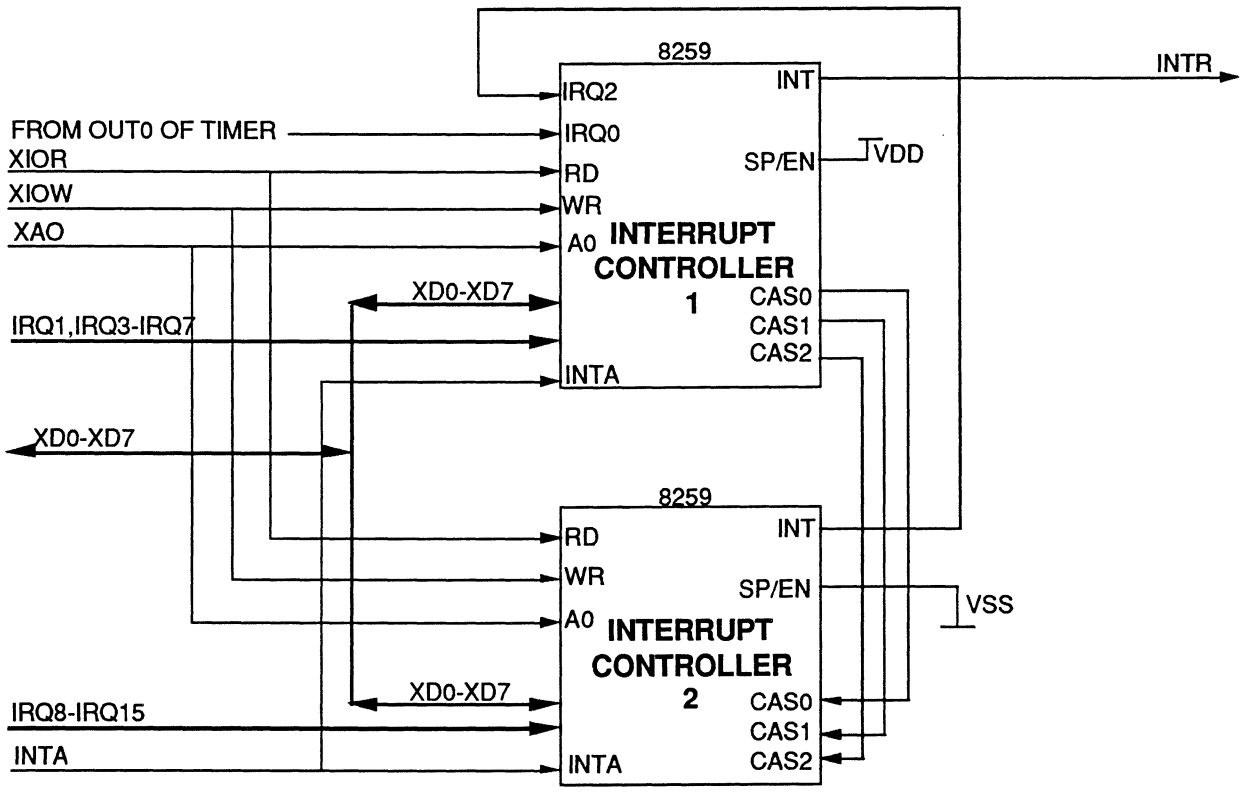
INTERRUPT CONTROLLER SUBSECTION

The interrupt controller subsection is made up of two 8259 megacells with eight interrupt request lines each for a total of 16 interrupts. The two megacells are cascaded internally through IRQ2 and IRQ0 is internally connected to a OUT0 of the 8254 counter/timer megacell. This allows a total of 14 external interrupt request.

A typical interrupt sequence would be as follows. Any unmasked interrupt will generate the INTR signal to the CPU. The interrupt controller megacells will then respond to the INTA pulses from the CPU. On the first INTA cycle the cascading priority is resolved to determine which of the two 8259 megacells will output the interrupt vector onto the data bus. On the second INTA cycle the appropriate 8259 megacell will drive the data bus with the correct interrupt vector for the highest priority interrupt.

Because the two megacells are cascaded in the SL9030, they should always be programmed to operate in the cascade mode.

Fig. 2. Interrupt Controller Subsection



INTERRUPT CONTROLLER INTERNAL REGISTERS

The internal registers of the 8259 megacells are written to in the same way as in the standard part. Table 4 shows the correct addressing for each of the 8259 registers. Before normal operation can begin, each 8259 megacell must follow an initialization sequence. The sequence is started by writing Initialization Command Word 1 (ICW1). After ICW1 has been written the 8259 megacell expects the next writes to follow in the sequence ICW2, ICW3, and ICW4 if it is needed. The Operation Control Words (OCW0) can be written at any time after initialization.

In the standard 8259 megacell ICW3 is optional. But since the two 8259's in this chip are cascaded together, they should always be programmed in cascade mode and ICW3 will always be needed.

When reading at address 020 or 0A0 hex, the register read will depend on how Operation Control Word 3 was setup prior to the read.

Table 4. Write Operations

Hex Address		XD4	XD3	Register Function
INT1	INT2			
020	0A0	1	X	Write ICW1
021	0A1	X	X	Write ICW2
021	0A1	X	X	Write ICW3
021	0A1	X	X	Write ICW4 (If needed)
021	0A1	X	X	Write OCW1
020	0A0	0	0	Write OCW2
020	0A0	0	1	Write OCW3

Table 5. Read Operations

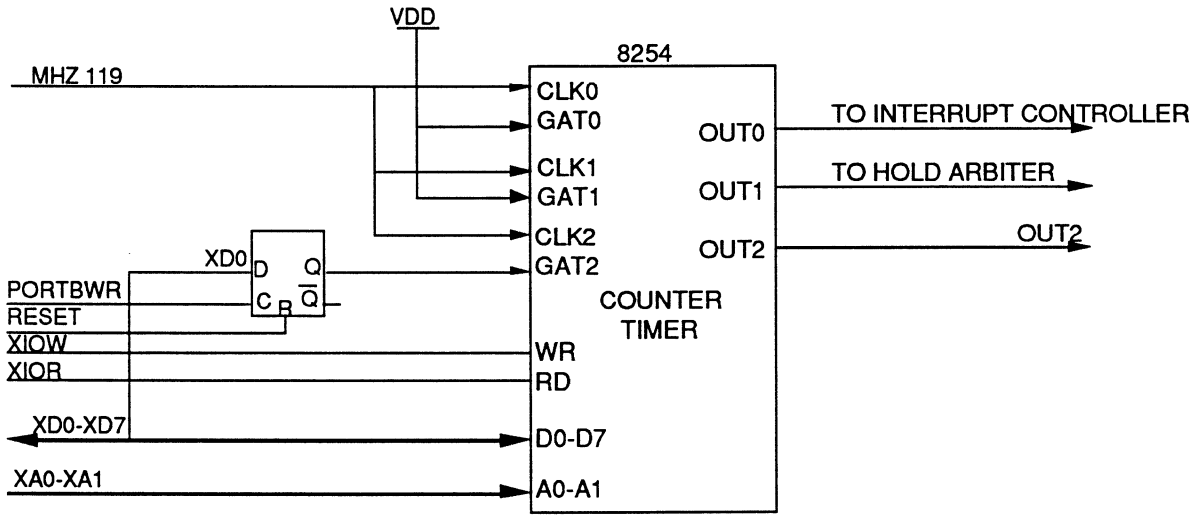
Hex Address		Register Function
INT1	INT2	
020	0A0	Interrupt Request Reg., In-Service Reg., or Poll Command
021	0A1	Interrupt Mask Register

TIMER/COUNTER SUBSECTION

The timer subsection consists of one 8254 counter/timer megacell configured as shown in the diagram. The clocks for each of the three internal counters are tied to the single input pin MHz 119. The gate inputs of Counters 0 and 1 are tied high to enable those Counters at all times. The gate input of Counter 2 is tied to the output of a flip-flop inside the SL9030. This flip-flop will clock in the value on XD0 during an I/O write to Port B. The output of the flip-flop is used to gate Counter 2 in the 8254 megacell on and off.

Only one of the 8254 megacell counter outputs is directly available at an external pin. Counter 0's output is connected to the IRQ0 input of interrupt controller 1. Counter 1's output goes to the hold request arbiter and refresh subsection to initiate a refresh cycle. Finally, Counter 2's output goes directly to the output pin OUT2.

Fig. 3. Timer/Counter Subsection



TIMER/COUNTER INTERNAL REGISTERS

The internal registers of the 8254 counter/timer megacell are written to in the same way as in the standard part. Table 6 shows the correct addressing for each of the 8254 registers.

The write control word at address 043 hex could also be the counter latch command or read back command depending on the values on the data bus. Refer to the 8254 data sheet for more information on programming the 8254 megacell.

Table 6. Timer/Counter Registers

Hex Address	XIOR	XIOW	Register Function
040	1	0	Write Initial Count to Counter 0
040	0	1	Read Latched Count or Status from Counter 0
041	1	0	Write Intitial Count to Counter 1
041	0	1	Read Latched Count or Status from Counter 1
042	1	0	Write Intital Count to Counter 2
042	0	1	Read Latched Count or Status from Counter 2
043	1	0	Write Control Word
043	0	1	No Operation

HOLD REQUEST ARBITER AND REFRESH SUBSECTION

The hold request arbiter and refresh subsection is used to select between the two possible sources for a hold request to the CPU. A hold request can be generated when DMA Controller 2 issues a hold request or when the output of counter 1 in the 8254 megacell makes a low to high transition. To provide equal weight to these two possible sources for a hold request, the hold request from the DMA controller is sampled on the rising edge of the internal DMA clock and the request from the counter/timer is sampled on the falling edge of the internal DMA clock. The request which is clocked in first will be granted by the arbiter and the other request inhibited until the first request is finished.

At the end of a hold request form either source the arbiter checks to see if the other source is still requesting a hold. If it is, the arbiter will give an acknowledge signal to that source and leave the CPUHRQ line active. This will continue as long as one of the two sources is requesting a hold. Only if neither source is requesting a hold will the arbiter negate the CPUHRQ signal and return control back to the CPU.

In the case of the DMA controller's hold request winning in the arbiter, the arbiter will assert the CPUHRQ output and wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause a hold acknowledge to be sent to the DMA controller. When the DMA controller is finished it will negate its hold request signal to the arbiter. The arbiter will then switch to a REFRESH cycle, if a hold request is pending from the 8254 counter/timer, or negate the CPUHRQ line and return control to the CPU.

In the case of a refresh cycle winning the arbitration, the CPUHRQ output will be asserted and the arbiter subsection will wait for a CPUHLDA signal back from the CPU. The assertion of CPUHLDA will cause the SL9030 to pull the REFRESH pin low. REFRESH will remain low for four SYSCLK rising edges. On the fourth rising edge of SYSCLK the REFRESH pin will go to a high impedance state enabling it to be pulled up by an external resistor, and the CPUHRQ signal will be negated. If the hold request arbiter has a hold request from the DMA controller pending on the fourth rising edge of SYSCLK cycle (see waveforms). The hold request arbiter will then acknowledge the hold request of the DMA controller.

Refresh cycles can be extended by an external source by forcing the IOCHRDY input low a setup time before the third rising edge of SYSCLK. REFRESH will remain low until IOCHRDY is returned high.

The pin REFRESH is a bidirectional open drain I/O pin and requires an external pull-up. It can also be used as an input if a refresh cycle is to be initiated from an external source.

PIN DESCRIPTION SL9030

SYMBOL	PIN	TYPE	DESCRIPTION
A17-A21 A22, A23	72-68 66, 65	O	CPU Address Bus Bits (A17 - 23) are connected to the CPU's address but and are driven from the LS612 memory mapper any time CPUHLDA is active (HIGH) and NMASTER is inactive (HIGH). They are in a three-state condition during all other times.
CPUHLDA	44	I	CPU Hold Acknowledge is an input from the CPU and indicates that it is acknowledging the hold request and is no longer driving the system bus. It indicated that the SL9030 can now drive the address and control buses.
CPUHRQ	40	O	CPU Hold Request output is the hold request to the CPU and is used to request control of the system bus. It can be issued by a request from the DMA controllers or the timer when it is time for a refresh cycle.
DRQO-DRQ3 DRQ5-DRQ7	21-18 17-15	I	Input signals, DMA Request Bits 0-3, 5-7, are the individual asynchronous requests for DMA service connected to the 8237 megacell. DRQ0 through DRQ3 supports transfers form 8 bit I/O adapters to/from 8 or 16 bit system memory. DRQ5 through DRQ7 support transfers form 16 bit I/O adapters to/from 16 bit system memory. DRQ4 is not available as it is used to cascade the two DMA controllers together.
INTR	46	O	Interrupt Request is an output used to interrupt the CPU and is generated whenever a valid IRQ is received.
NINTA	6	I	Interrupt Acknowledge is an input used to enable the 8259 interrupt controllers to vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
IOCHRDY	73	I	I/O Channel Ready is an input used to extend the memory read and write pulses from the 8237 to accommodate slow external devices.
IRQ1, IRQ3-IRQ7 IRQ8-IRQ15	14, 13-9, 81-74	I	Interrupt Request bits 1, 3-7, 8-15 are asynchronous interrupt request inputs to the 8259 megacells. IRQ2 and IRQ0 are not available as inputs to the chip. IRQ2 is used to cascade the two 8259's together and IRQ0 is connected to the out0 signal of the 8254 counter.
MHZ119	41	I	This is the 1.19 MHz clock input for the 8254 counter.
NAEN1	8	O	Address Enable 1 is an active LOW signal. It indicates when DMA Controller 1 is enabling addresses onto the peripheral address bus for a DMA transfer.

PIN DESCRIPTION SL9030 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
NAEN2	7	O	Address Enable 2 is an active LOW signal. It indicates when DMA Controller 2 is enabling addresses onto the peripheral address bus for a DMA transfer.
NDACK0-NDACK3 NDACK5-NDACK7	1, 83, 84, 82 2-4	O	DMA Acknowledge Bits 0-3, 5-7 output signals are the acknowledge signals for the corresponding DMA requests. The active polarity of these lines is programmable and is set to active LOW on reset.
NMASTER	45	I	Master - An external device will pull this input LOW to disable the DMA controllers to gain access to the system bus. It indicates an I/O device controls the system buses.
NREFRESH	25	I/O	The Refresh I/O signal will be pulled LOW by the SL9030 whenever the 8254 counter 1 issues a CPUHRQ to the CPU and a hold acknowledge is received from the CPU. It is used internally to select a location in the memory mapper which drives the upper address bus A17-A23. Refresh can also be used as an input if the refresh timing is to come from a source other than the 8254 channel 1 counter. Refresh is an open drain output capable of sinking 20 mA and requires an external pull-up resistor.
NXIOR	38	I/O	I/O Read is a bidirectional active LOW three-state line. It is an output during a DMA cycle and will be an input at all other times.
NXIOW	37	I/O	I/O Write is a bidirectional active LOW three-state line. It is an output during a DMA cycle and will be an input at all other times.
NXMEMR	35	O	Memory Read is a three-state output which will be active during a DMA cycle.
NXMEMW	36	I/O	Memory Write is a bidirectional active LOW three-state line. It is an output during a DMA cycle and will be an input at all other times. In the input mode XMEMW is used to enable the hold request arbiter after an interrupt acknowledge cycle.
OUT2	42	O	Out 2 is the output of counter 2 in the 8254 megacell.
RESET	24	I	Reset is an active HIGH input used to clear the DMA controller and hold request arbiter.

PIN DESCRIPTION SL9030 (Cont'd.)

SYMBOL	PIN	TYPE	DESCRIPTION
SYSCLK	23	I	System Clock Input. This pin is divided by two internally to generate DMACLK for the 8237 DMA controllers. It is also used in the hold request arbiter. SYSCLK can be driven at a frequency of up to 20 MHz.
T/C	39	O	Terminal Count indicates one of the DMA channel's terminal count has been reached.
VDD	5, 43		System Power : 5 V.
VSS	22, 26, 59, 67		System Ground.
XA0-XA9	47-56	I/0	Peripheral Address bus Bits 0-9 are bidirectional pins. They are outputs during DMA cycles and are inputs all other times. As inputs they are used to generate chip selects for the 82XX megacells.
XA10, XA11 XA12-XA16	57, 58 60-64	O	The seven most significant address bits on the XA bus (XA10-16) are three-state outputs only. They actively drive the XA bus during DMA cycles.
XD0-XD7	34-27	I/O	Peripheral Data Bus Bits 0-7. The eight least significant data bits on the XD bus are bidirectional.

ABSOLUT MAXIMUM RATINGS SL9030 *note 1

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	-.5	6.0	V
Input Voltage	V_I	-.5	V_{DD}+.5	V
Output Voltage	V_O	-.5	V_{DD}+.5	V
Output Current	I_{OS}	-40	+40	mA
Output Current	I_{OS}	-40	+80	mA
Output Current	I_{OS}	-60	+120	mA
Output Current	I_{OS}	-90	+180	mA
Storage Temp.	T_{STL}	-40	+125	°C
Storage Temp.	T_{BIOS}	-25	+85	°C

* NOTES:

1. Permanent devices damage may occur if device ratings are excluded. Reliability may be affected by sustained exposure to absolute maximum values.

RECOMMENDED OPERATING CONDITIONS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}	4.75	5.25	V
Temperature	T_A	0	70	°C

DC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS	CONDITIONS
Output High Voltage	VOH	3.0		V	IOH = 4mA
Output Low Voltage	VOL1		0.4	V	IOL = 20 mA, NREFRESH
Output Low Voltage	VOL2		0.4	V	IOL = 4 mA, All Other Pins
Input High Voltage	VIH	2.2	VDD+.5	V	TTL
Input Low Voltage	VIL	-0.5	0.8	V	TTL
Output Capacitance	CO		10	pF	
Input Capacitance	CI		10	pF	
Input/Output Capacitance	CIO		10	pF	
Three-state Leakage Current	IO2H		10	mA	VOH = VDD
	IO2L	-10		mA	VOL = GND
Input Leakage Current	ILI	-10	10	µA	All Inputs
Power Supply Current	ICC		30	mA	Note

NOTE:
VIN = VDD or GND, VDD = 5.25V, ouputs unloaded

ABSOLUTE MAXIMUM RATINGS:

Ambient Operating Temperature	QC = 0°C to +70C QI = -40°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
Applied Input Voltage	-0.5V to VDD to .5V
Power Dissipation	500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operations of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

AC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

Symbol	Description	Min.	Max.	Units	Notes
tSET3	DRQ to SYSCLK High Setup Time	0	-	ns	1
tD10	CPUHRQ Valid from SYSCLK High Delay Time	-	60	ns	
tSET4	CPUHLDA to SYSCLK High Setup Time	25	-	ns	
tD11	NAEN1 Valid from SYSCLK High Delay Time	-	75	ns	
tD12	NDACK Valid from SYSCLK High Delay Time	-	90	ns	
tD13	XD Bus Valid from SYSCLK High Delay Time	-	100	ns	
tD14	XD Bus Active to Float Delay from SYSCLK High	-	55	ns	
tD15	A17-A23 Float to Active from CPUHLDA High Delay Time	-	35	ns	
tD16	Upper Address Bits Valid from SYSCLK High Delay Time	-	110	ns	2
tD17	A17-A23 Active to Float from CPUHLDA Low Delay Time	-	25	ns	
tD18	Middle Address Bits Valid from SYSCLK High Delay Time	-	110	ns	3
tD19	Lower Address Bits Valid from SYSCLK High Delay Time	-	85	ns	4
tD20	XA Address Bus Active to Float from SYSCLK High Delay Time	-	60	ns	7
tD21	NREAD and NWRITE Active from SYSCLK High Delay Time	-	75	ns	
tD22	NREAD and NWRITE Valid from SYSCLK High Delay Time	-	80	ns	
tD23	NREAD and NWRITE Float from SYSCLK High Delay Time	-	60	ns	7
tD24	T/C Valid from SYSCLK High Delay Time	-	85	ns	7
tHD2	XA Address From NREAD or NWRITE	2 TCY -50	-	ns	TCY=SYSCLK cycle time
tD25	NAEN2 Valid from SYSCLK High Delay Time	-	75	ns	
tD26	NAEN2 High from SYSCLK High	-	125	ns	
tD27	XA Address Bus Float from SYSCLK High Delay Time	-	120	ns	8
tD28	NREAD or NWRITE Float from SYSCLK High Delay Time	-	120	ns	8
tD29	NREAD or NWRITE Float from NREAD or NWRITE High at end of DMA Cycle	5	-	ns	8
tSET5	IOCHRDY Valid to SYSCLK High Setup Time	15	-	ns	
tHD3	IOCHRDY from SYSCLK High Hold Time	5	-	ns	
tD30	A17-A23 Float from NMASTER Low Delay Time	-	25	ns	
tD31	A17-A23 Float from NMASTER High Delay Time	-	40	ns	
tD32	NREFRESH Low from CPUHLDA High Delay Time	-	50	ns	
tD33	NREFRESH Inactive from SYSCLK High Delay Time	-	50	ns	5
tSET6	NREFRESH Low to SYSCLK High Setup Time	20	-	ns	6
tD34	A17-A23 Valid from NREFRESH Valid Delay Time	-	80	ns	
t35	SYSCLK Cycle Time	50	-	ns	
tPW55	SYSCLK Pulse Width Low	20	-	ns	
tPW56	SYSCLK Pulse Width High	20	-	ns	
t36	SYSCLK Rise/Fall Time	-	7	ns	

NOTES:
1. The DRQ signals are asynchronous inputs. Setup times are shown to assure recognition at a specific clock edge for testing.
2. Upper address bits are defined as A17-A23 for 16 bit DMA cycles, and A17-A23 plus XA16 for 8 bit DMA cycles.
3. Middle address bits are defined as XA9-XA16 for 16 bit DMA cycles and XA8-XA15 for 8 bit DMA cycles.
4. Lower address bits are defined as XA0-XA8 for 16 bit DMA cycles and XA0-XA7 for 8 bit DMA cycles.
5. NREFRESH is an open drain output. This specification is the time until the output is in an inactive state. Rise time of the external signal will depend on the external pull-up value and capacitive load.
6. When used as an input, NREFRESH is an asynchronous signal.
7. 8 Bit Cycles Only.
8. 16 Bit Cycles Only.

AC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

Symbol	Description	Min.	Max.	Units
tRW	NXIOR or NXIOW Pulse Width Low	150	-	ns
tSET1	XA Address Valid to NXIOR or NXIOW Low Setup Time	25	-	ns
tHD1	XA Address from NXIOR or NXIOW High Hold Time	15	-	ns
tD1	XD Data Valid Delay from NXIOR Low	-	100	ns
tD2	XD Data Float Delay from NXIOR High	-	60	ns
tSET2	XD Data Valid to NXIOW High Setup Time	100	-	ns
tHD2	XD Data Valid from NXIOW High Hold Time	10	-	ns
tRST	RESET Pulse Width High	200	-	ns
t1	RESET Inactive to first NXIOR or NXIOW Command	200	-	ns
t2	Comand Recovery Time Between Successive NXIOR or NXIOW Pulses	200	-	ns

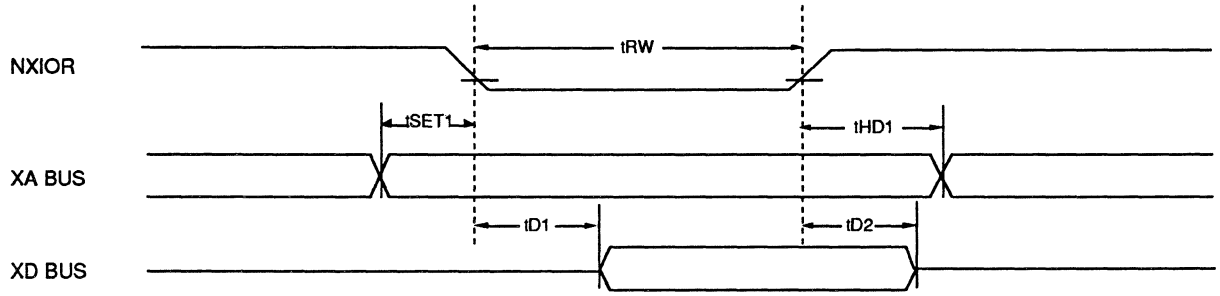


Fig. 4. READ TIMING

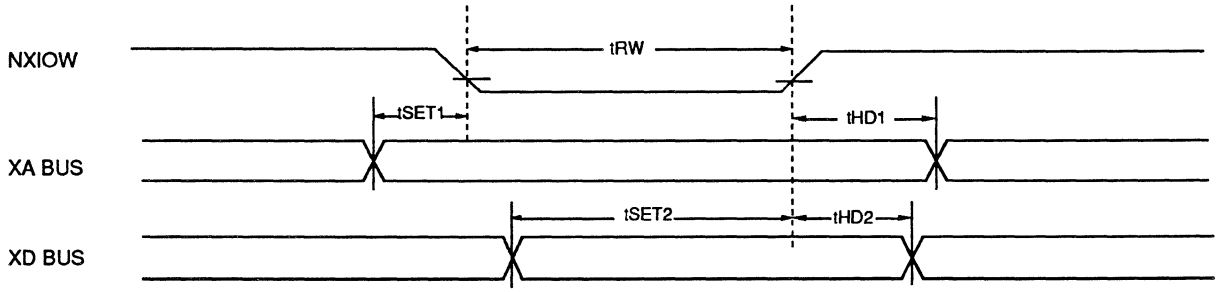


Fig. 5. WRITE TIMING

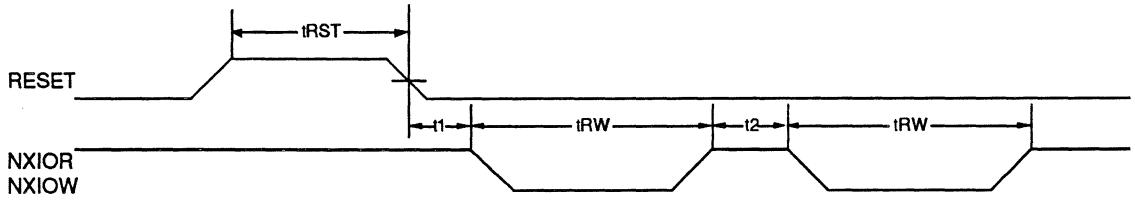


Fig. 6. COMMAND AND RESET TIMING

AC CHARACTERISTICS SL9030

(TA = 0 ° C to +70 ° C, VDD = 5V ± 5%, VSS = 0V)

Symbol	Description	Min.	Max.	Units	Notes
tPW1	Interrupt Request Pulse Width Low	90	-	ns	
tD3	Interrupt Output Delay	130	-	ns	
tPW2	NINTA Pulse Width Low	180	-	ns	
tD4	End of NINTA Pulse to next NINTA Pulse	180	-	ns	
tD5	XD Data Valid Delay from NINTA Low	-	110	ns	1
tD6	XD Data Float Delay from NINTA High	0	45	ns	2
tPW3	MHz 119 Clock Pulse Widht High	50	-	ns	
tPW4	MHz 119 Clock Pulse Width Low	50	-	ns	
tD7	MHz 119 Clock Rise/Fall Time	-	20	ns	
tD8	OUT2 Valid from NXIOW High Delay Time when writing to Counter 2 Mode Register or TMGATE2 in Port B	-	100	ns	
tD9	Out2 Valid from MHz 119 Low Delay Time	-	100	ns	

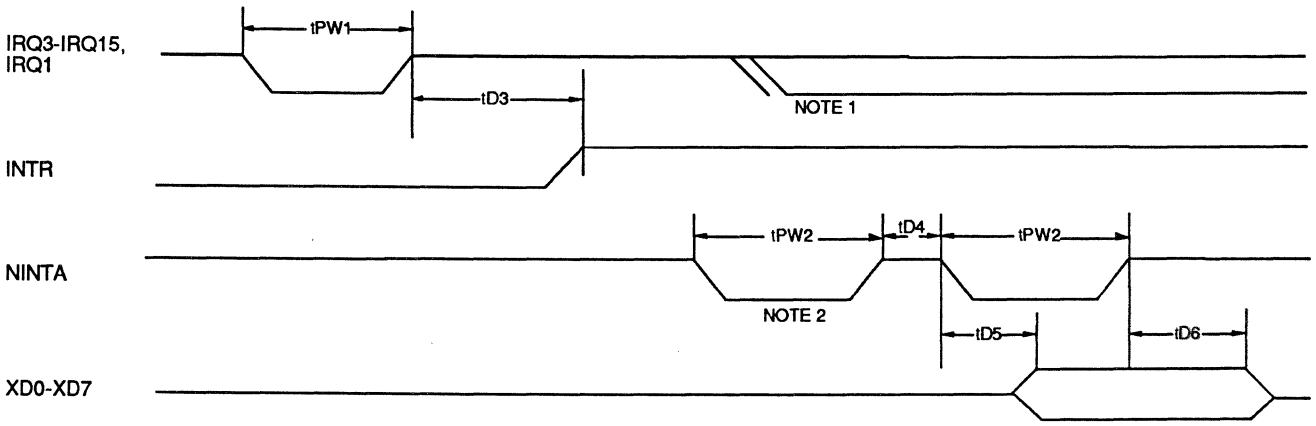


Fig. 7. INTERRUPT TIMING

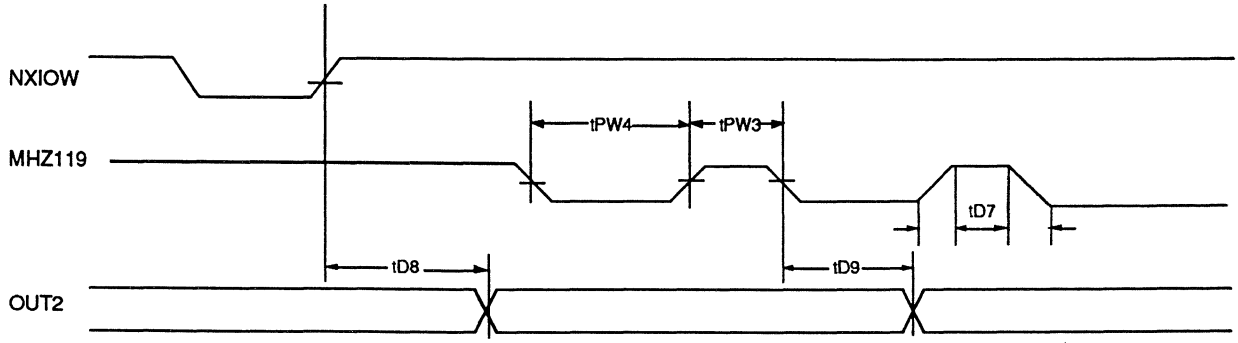


Fig. 8. TIMER/COUNTER TIMING

NOTES: 1. IRQ must remain HIGH until first NINTA pulse
2. Cascade priority is resolved on this NINTA cycle.

AC TIMING DIAGRAMS SL9030

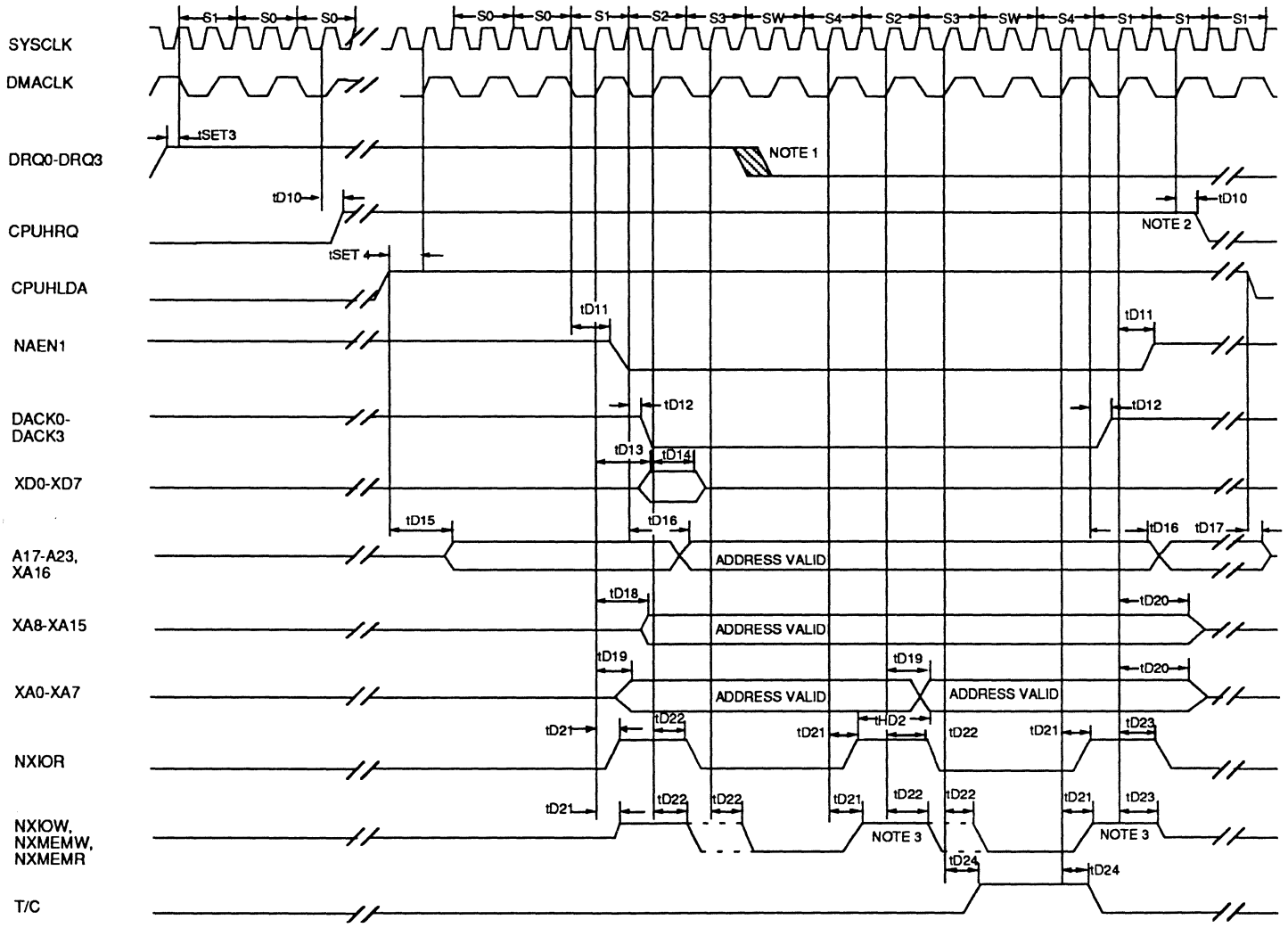


Figure 9. 8 BIT DMA TIMING

NOTES:
1. DRQ should be held active until NDACK is returned.
2. The falling edge of CPUHRQ could occur one clock cycle earlier or later depending on how many bytes are transferred.
3. The first high to low transition shown here is for extended NXIOW and NXMEMW. The second high to low transition shown is for NXMEMR and late write on NXIOW and NXMEMW.

AC TIMING DIAGRAMS SL9030

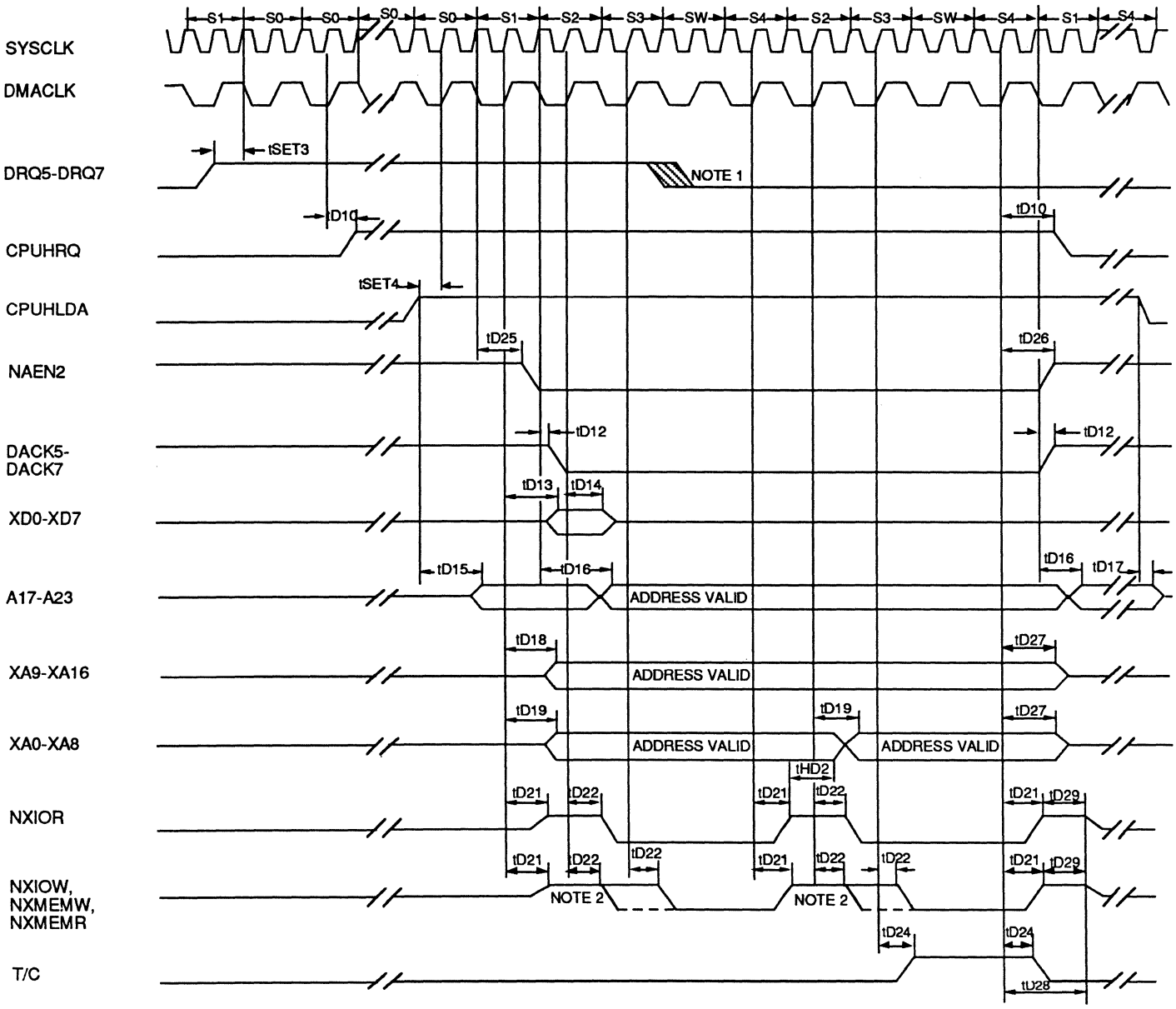


Figure 10. 16 BIT DMA TIMING

NOTES:
1. DRQ should be held active until NDACK is returned.
2. The first high to low transition shown here is for extended NXIOW and NXMEMW. The second high to low transition shown is for NXMEMR and late write on NXIOW and NXMEMW.

AC TIMING DIAGRAMS SL9030

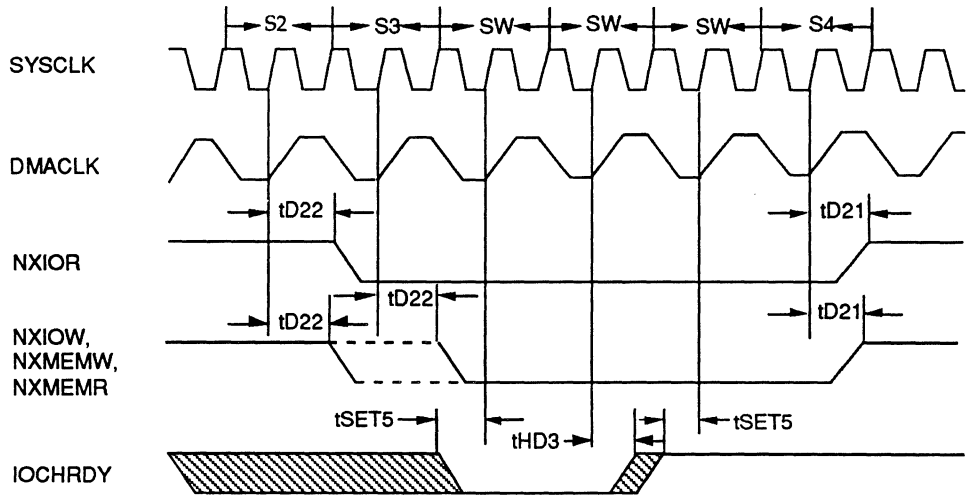


Figure 11. IOCHRDY TIMING

NOTE: The first wait state is inserted by internal circuitry in the SL9030 for all DMA cycles. Any additional wait states must by inserted using IOCHRDY.

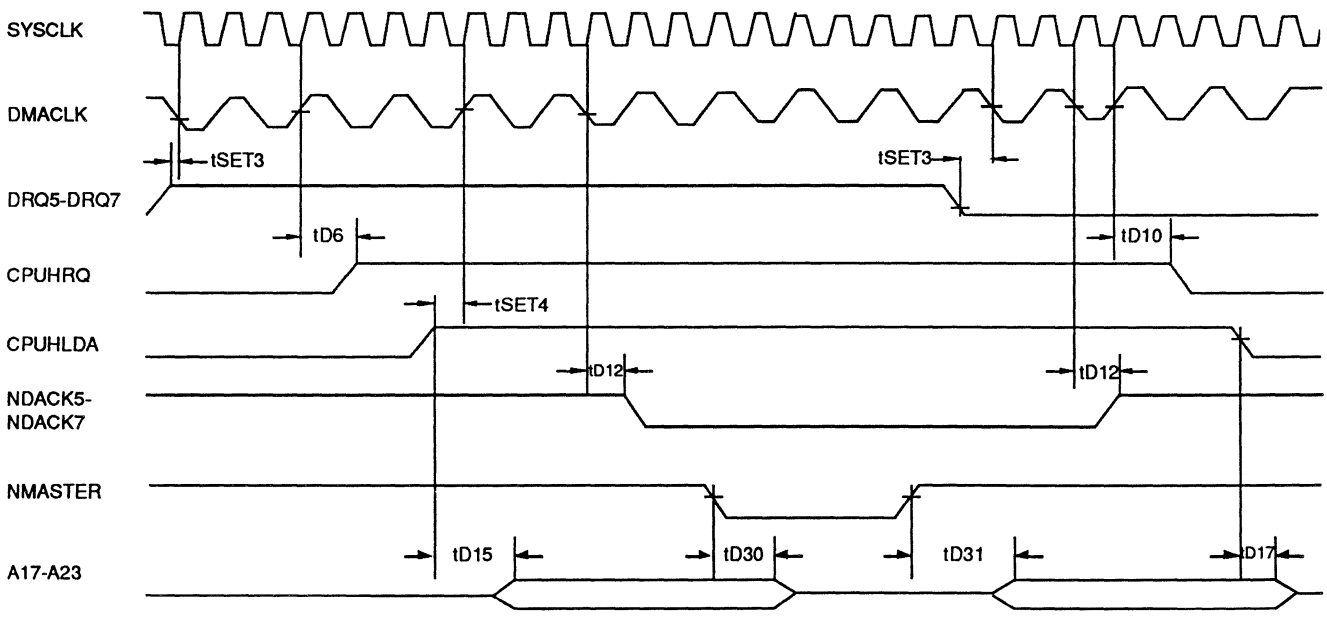


Figure 12. NMASTER TIMING

NOTES:
1. The DMA channel used for requesting control of the bus by a new bus master must be programmed in cascade mode. The new master should not pull NMASTER low until it has received the corresponding NDACK signal.
2. The timing shown is assuming one of the 16 bit DMAchannels is used. There will be extra cycles between DRQ and CPUHRQ before and after the request cycle when using an 8 bit DMA channel. These extra cycles are caused by the cascade delay from the slave 8237 through the master 8237.

AC TIMING DIAGRAMS SL9030

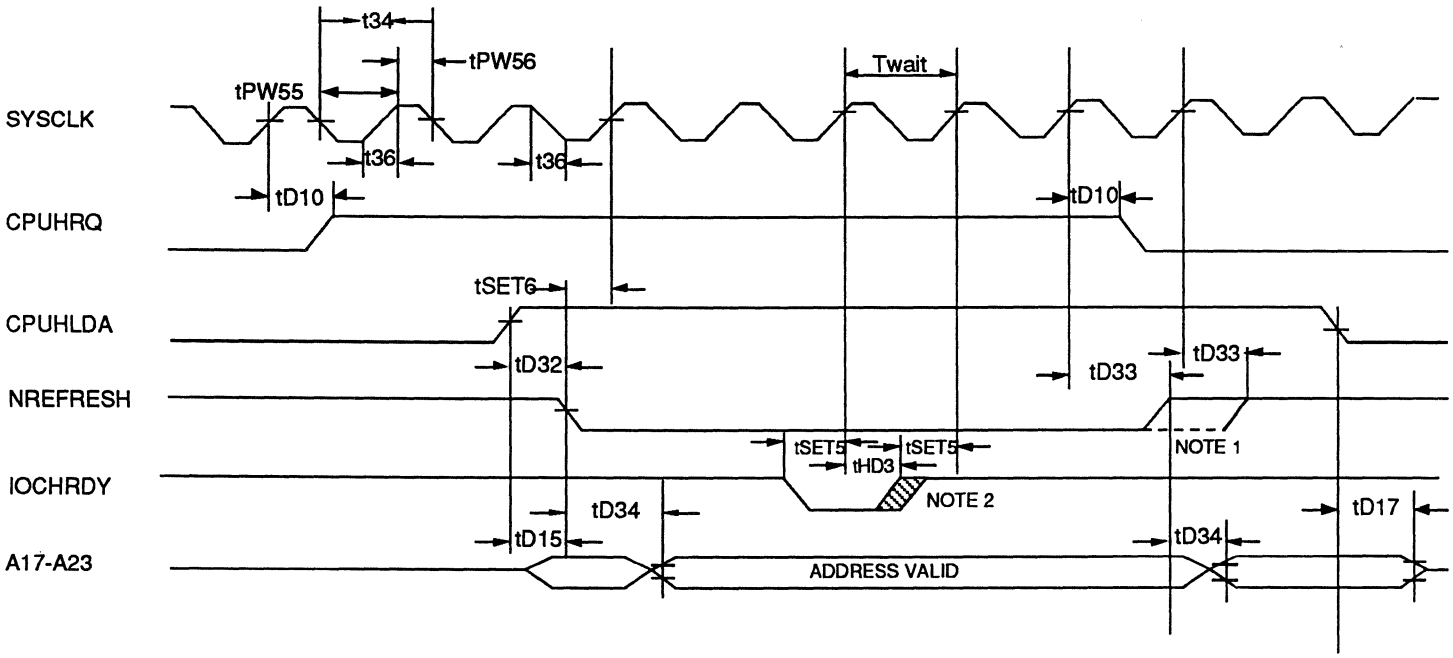
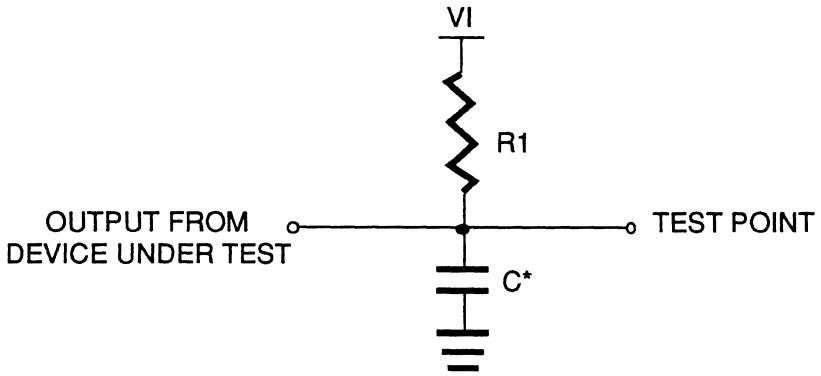


Figure 13. NREFRESH TIMING

NOTES:
1. A refresh pulse is normally three SYSCLK cycles long (with no wait states). Refresh pulses will be four SYSCLK cycles if a hold request is pending from the DMA controllers.
2. REFRESH cycles can be extended by inserting wait states using IOCHRDY.

AC TIMING DIAGRAMS SL9030

FIG. 14 A.C. TEST CIRCUITS

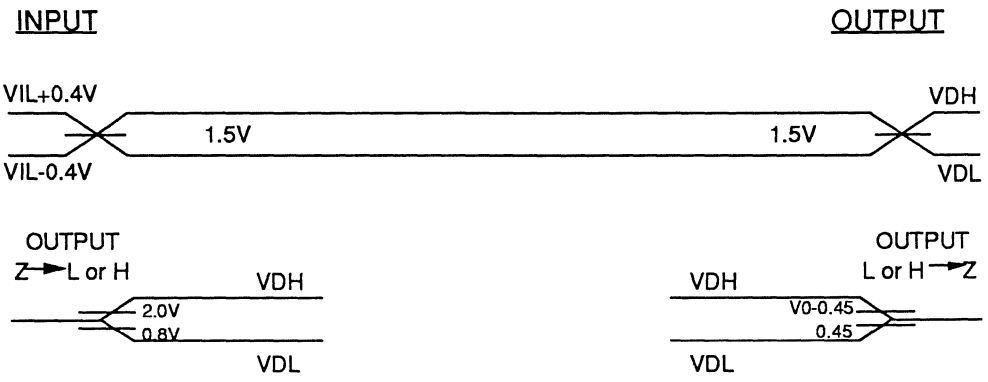


* Includes STRAY and JIG capacitance

TEST CONDITION DEFINITION TABLE

PINS	VI	R1	C1
All Outputs Except EOP	1.7V	520	100pF
EOP	VCC	1.6K	50pF

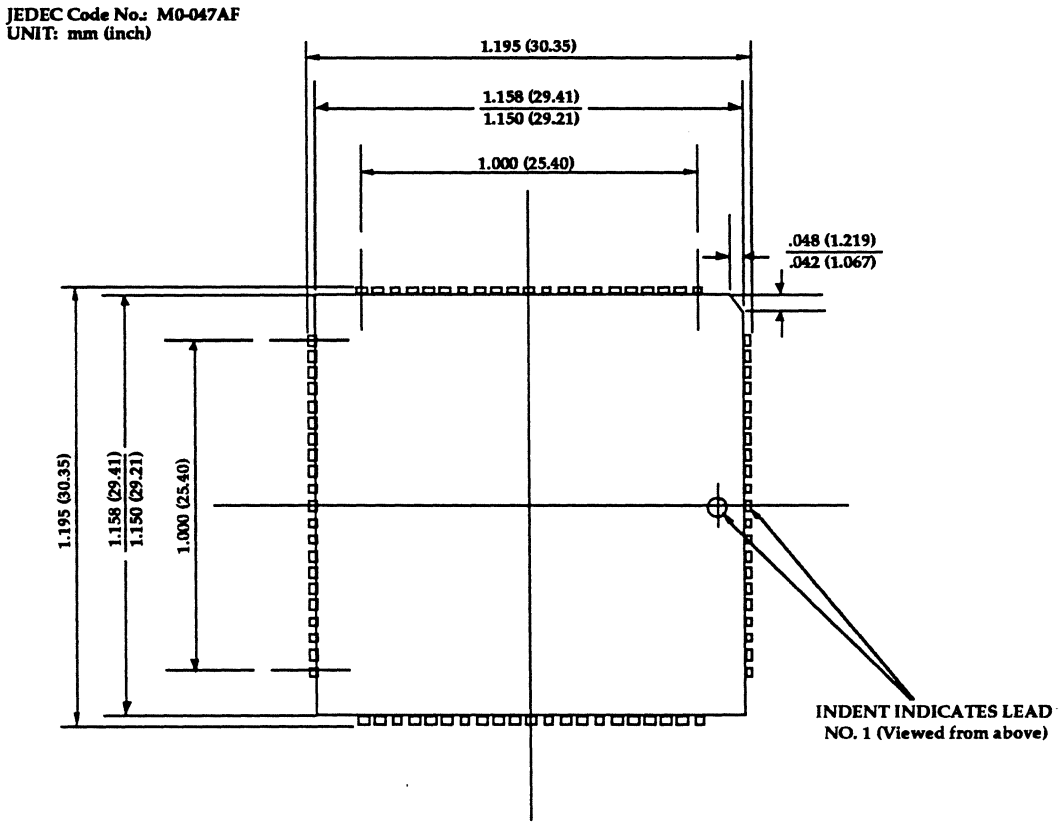
FIG. 15 A.C. TESTING INPUT, OUTPUT



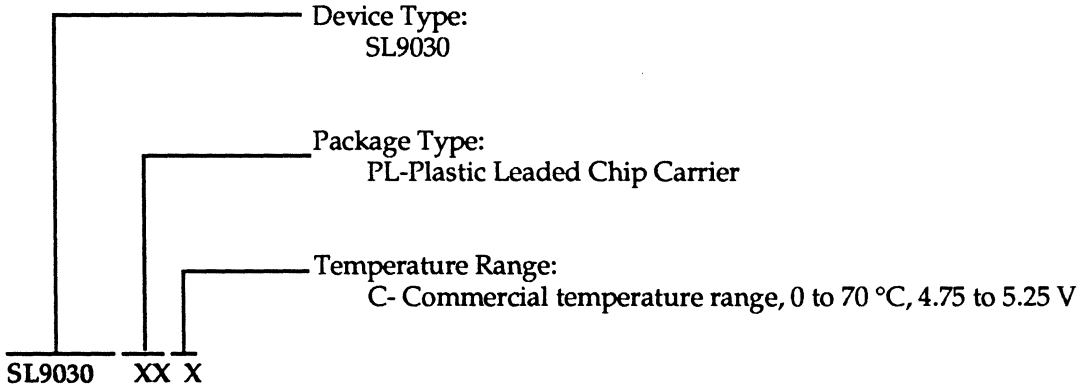
A.C. Testing: All A.C. Parameters tested as per test circuits. Input RISE and FALL times are driven at 1ns/V.

Package Information

84 Pin Plastic Leaded Chip Carrier (PLCC)



ORDERING INFORMATION



IBM, AT are the trademarks of International Business Machines.
Intel is a trademark of Intel Corporation.

June 1991

VIA Technologies, Inc. (408) 746-2200
860 East Arques Avenue
Sunnyvale, CA 94086