Data Sheet

VT1637

LVDS Transmitter

Preliminary Revision 1.0
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VIA TECHNOLOGIES, INC.

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VT1637

LVDS Transmitter

PRODUCT FEATURES

- **Supports Single / Dual LVDS Transmitter Function**
- **Compatible with TIA/EIA-644 LVDS Standard**
- **Supports LVDS 18-bit Output**
- **Supports Dual Channel UXGA Panel Display**
- **Supports 2D Dither for 18-bit Panel**
- **Supports DVO Input Mode with 25 to 165 MHz Input Clock**
- **Programmable Input Clock and Strobe Select**
- **Narrow Bus Reduces Cable Size and Cost**
- **PLL Requires No External Components**
- **2.5V core power for low power consumption**
- **48-pin LQFP Package (7x7x1.4 mm)**
- **Available for Lead-Free Package**

OVERVIEW

The VIA VT1637 is a powerful LVDS transmitter. The input format can be DVO (12 data pin per port) digital interface. Operating on DVO mode, its output can support single / dual channels with 18-bit color type panel. The VT1637 implements a 2D dithering engine option for 18-bit / 36-bit color type panel.

Figure 1 shows the functional block diagram for VT1637 LVDS Transmitter.

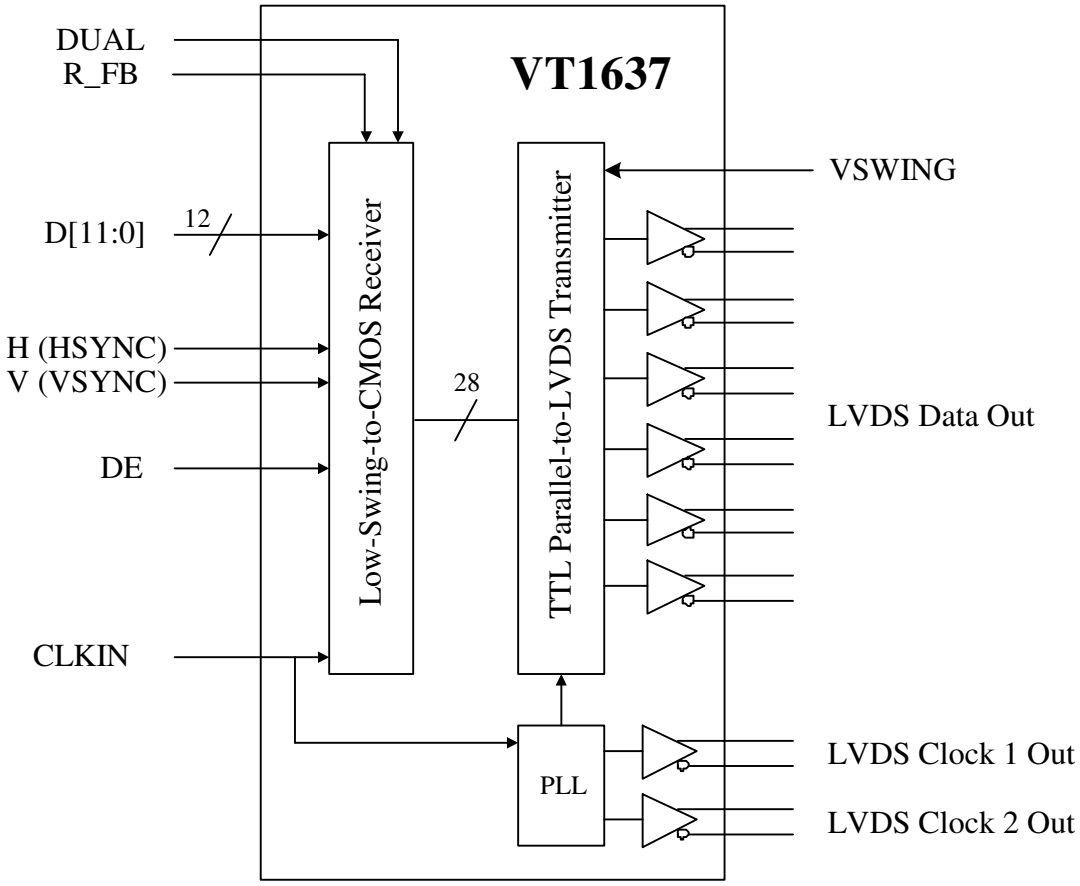


Figure 1. Functional Block Diagram

The LVDS transmitter operates at pixel speed up to 165 MHz per link, supporting UXGA panel display. It converts 24 / 48 bits of CMOS/TTL data into 3-6 LVDS data streams. The LVDS transmitter supports dither function for 18-bit panel. Data is encoded into commonly used formats. A phase-locked transmit clock is transmitted in parallel with the data streams over 3-6 LVDS link.

PINOUTS

Pin Diagram

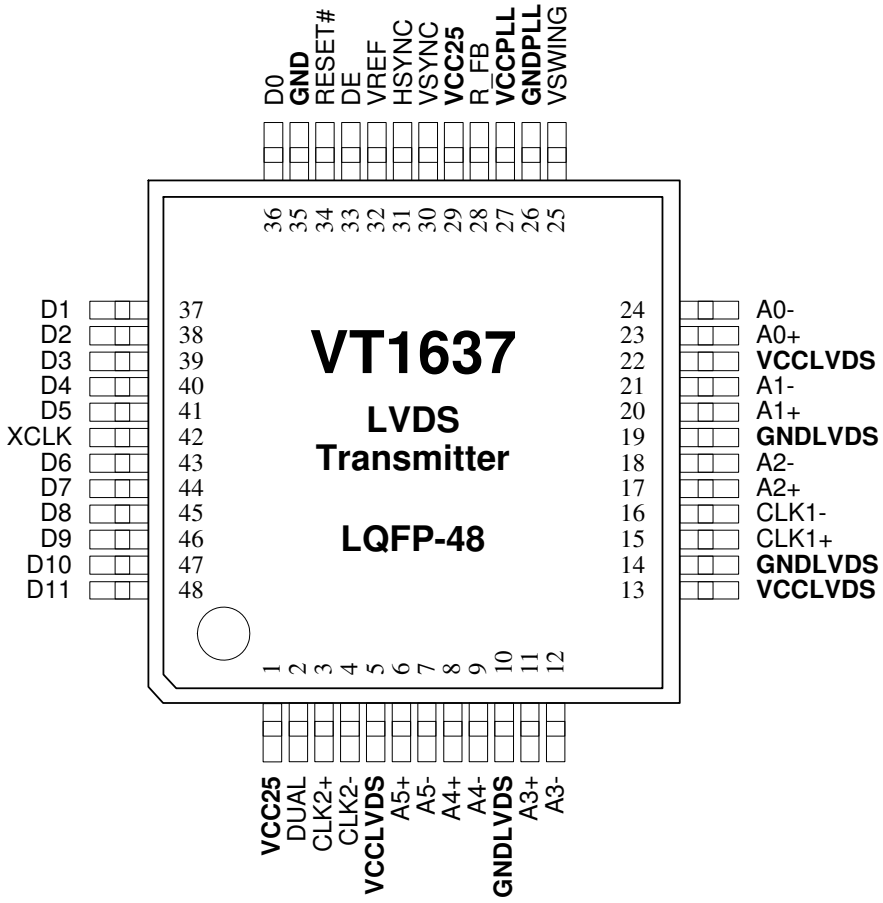


Figure 2. Pin Diagram (Top View)

Pin Lists

Table 1. Pin List (Alphabetical Order)

Pin	Pin Name	Pin	Pin Name
24	A0-	45	D[8]
23	A0+	46	D[9]
21	A1-	47	D[10]
20	A1+	48	D[11]
18	A2-	33	DE
17	A2+	2	DUAL
12	A3-	**35**	**GND**
11	A3+	**10**	**GNDLVDS**
9	A4-	**14**	**GNDLVDS**
8	A4+	**19**	**GNDLVDS**
7	A5-	**26**	**GNDPLL**
6	A5+	31	HSYNC
16	CLK1-	34	RESET#
15	CLK1+	28	R_FB
4	CLK2-	**1**	**VCC25**
3	CLK2+	**29**	**VCC25**
36	D[0]	**5**	**VCCLVDS**
37	D[1]	**13**	**VCCLVDS**
38	D[2]	**22**	**VCCLVDS**
39	D[3]	**27**	**VCCPLL**
40	D[4]	25	VSWING
41	D[5]	32	VREF
43	D[6]	30	VSYNC
44	D[7]	42	XCLK

Pin Descriptions

Table 2. Pin Descriptions

Pixel Data Input			
Signal Name	**Pin #**	**Type**	**Description**
D[11-00]	48, 47, 46, 45, 44, 42, 41, 40, 39, 38, 37, 36	I	**Channel Data Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.
DE	33	I	**Data Enable Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.
HSYNC	31	I	**HSYNC Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.
VSYNC	30	I	**VSYNC Input.** LVTTL level single-ended data inputs or low swing inputs. Reference to VREF pin.

Control Pins			
Signal Name	**Pin #**	**Type**	**Description**
DUAL	2	I/O	**LVDS Single or Dual Channel Select Pin** DUAL = L, chip is for single channel. DUAL = H, chip is for dual channel.
RESET#	34	I	When this pin is low, the device is held in the power-on reset condition.
VSWING	25	I	**LVDS Voltage Swing Control**
VREF	32	I	**Input Reference Voltage** Select the swing range of the digital parallel data inputs. VREF = Vcc is LVTTL input mode (3.3V) VREF = 1/2 Vccq is low swing input mode (1.0V - 1.8V)
R_FB	28	I	**Rising / Falling Sample Select Pin** R_FB = H, rising sample R_FB = L, falling sample.

LVDS Output			
Signal Name	**Pin #**	**Type**	**Description**
A[5:0]+	6, 8, 11, 17, 20, 23	O	**Positive LVDS Differential Data Output**
A[5:0]-	7, 9, 12, 18, 21, 24	O	**Negative LVDS Differential Data Output**
CLK1+	15	O	**Positive LVDS Differential Clock Output for 1st Link**
CLK1-	16	O	**Negative LVDS Differential Clock Output for 1st Link**
CLK2+	3	O	**Positive LVDS Differential Clock Output for 2nd Link**
CLK2-	4	O	**Negative LVDS Differential Clock Output for 2nd Link**

Clock			
Signal Name	**Pin #**	**Type**	**Description**
XCLK	42	I	**External Clock Input** This input clock signals to the device for use with H1, V1 and D[11-00].

Power and Ground			
Signal Name	**Pin #**	**Type**	**Description**
GND	35	P	**Digital Ground Pin**
GNDLVDS	10, 14, 19	P	**LVDS Ground Pin for LVDS Outputs**
GNDPLL	26	P	**LVDS PLL Ground**
VCC25	1, 29	P	**Digital Power Supply Pin (2.5V)**
VCCLVDS	5, 13, 22	P	**LVDS Power Supply Pin for LVDS Outputs (2.5V)**
VCCPLL	27	P	**LVDS PLL Power Supply (2.5V)**

LVDS Interface Data Mapping

Table 3. 12-bit DVO Mode (DDR), "Two Data per Clock" Input Color Data Mapping

Pin Name	P0		P1	
	P0L	P0H	P1L	P1H
	Low	High	Low	High
D[11]	G0[3]	R0[7]	G1[3]	R1[7]
D[10]	G0[2]	R0[6]	G1[2]	R1[6]
D[09]	G0[1]	R0[5]	G1[1]	R1[5]
D[08]	G0[0]	R0[4]	G1[0]	R1[4]
D[07]	B0[7]	R0[3]	B1[7]	R1[3]
D[06]	B0[6]	R0[2]	B1[6]	R1[2]
D[05]	B0[5]	R0[1]	B1[5]	R1[1]
D[04]	B0[4]	R0[0]	B1[4]	R1[0]
D[03]	B0[3]	G0[7]	B1[3]	G1[7]
D[02]	B0[2]	G0[6]	B1[2]	G1[6]
D[01]	B0[1]	G0[5]	B1[1]	G1[5]
D[00]	B0[0]	G0[4]	B1[0]	G1[4]

Table 4. Single Channel Color Mapping for Single LVDS Channel

Pin Name	18-bit Color Mapping Format
LDC[0](1)	R0*
LDC[0](2)	R1*
LDC[0](3)	R2*
LDC[0](4)	R3*
LDC[0](5)	R4*
LDC[0](6)	R5*
LDC[0](7)	G0*
LDC[1](1)	G1*
LDC[1](2)	G2*
LDC[1](3)	G3*
LDC[1](4)	G4*
LDC[1](5)	G5*
LDC[1](6)	B0*
LDC[1](7)	B1*
LDC[2](1)	B2*
LDC[2](2)	B3*
LDC[2](3)	B4*
LDC[2](4)	B5*
LDC[2](5)	HSYNC
LDC[2](6)	VSYNC
LDC[2](7)	DE

VT1637 internal dither engine converts 24-bit color (R0-R7,G0-G7,B0-B7) per pixel to 18-bit color (R0*-R5*,G0*-G5*,B0*-B5*) per pixel. VT1637 supports dual channels LVDS output, A0 ~ A2 output for odd pixel, A3 ~ A5 output for even pixel. A3 ~ A5 color data mapping is same as A0 ~ A2.

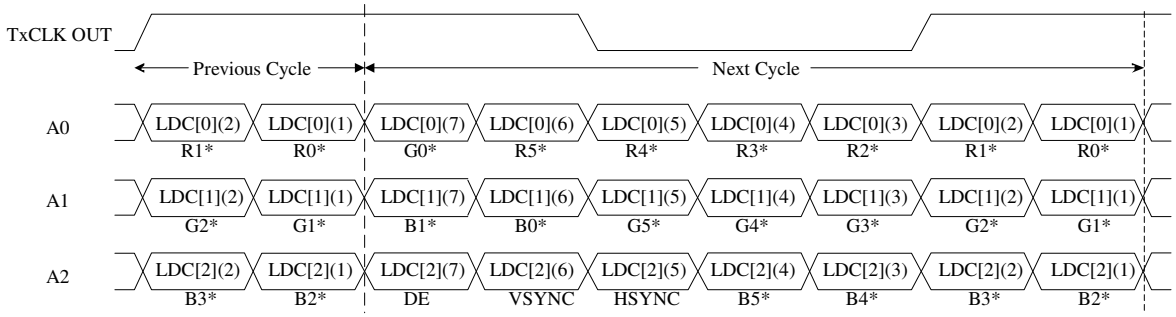


Figure 3. LVDS output Color Mapping for 18-bit format

ELECTRICAL SPECIFICATIONS

CMOS/TTL Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	High Level Input Voltage	-	2.0	-	V_{DD}	V
V_{IL}	Low Level Input Voltage	-	GND	-	0.8	V
I_{IN}	Input Current	V_{IN}=GND or V_{DD}	-	±5.1	±10	uA

LVDS Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OD}	Differential Output Voltage	R_L=100Ω	-	275	-	mV
$\Delta\|V_{OD}\|$	Change in Differential Output Voltage		-	25	-	mV
V_{OS}	Common Mode Output Voltage		-	1.250	-	V
$\Delta\|V_{OS}\|$	Change in Common Mode Output Voltage		-	25	-	mV
I_{IN}	Input Current	V_{IN}=3.3V	-	-	+10	uA
		V_{IN}=GND	-10	-	-	uA
$\|I_{OS}\|$	Short Circuit Output Current	V_{OUT}=0V; R_L=100Ω	-	3.5	-	mA
$\|I_{OZ}\|$	High Impedance State Output Current	PDB= 0V V_{OUT}=GND or VCC25	-	1	-	uA
P_{TOTAL}	Total Power Consumption	PDB= 0V	-	-	225	mW

Low Voltage Mode DC Specification (Pixel Data Input)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ref}	Differential Input Reference Voltage, VCC25=2.25V					

AC Specifications

Symbol	Parameter	Frequency	Min.	Typ.	Max.	Unit
LLHT	LVDS low to high transition time	-	-	0.75	1.5	nS
LHLT	LVDS high to low transition time	-	-	0.75	1.5	nS
T_{PPOS0}	Output pulse position for bit 0	85MHz	-0.2	0	0.2	nS
T_{PPOS1}	Output pulse position for bit 1		1.48	1.68	1.88	nS
T_{PPOS2}	Output pulse position for bit 2		3.16	3.36	3.56	nS
T_{PPOS3}	Output pulse position for bit 3		4.88	5.08	5.28	nS
T_{PPOS4}	Output pulse position for bit 4		6.52	6.72	6.92	nS
T_{PPOS5}	Output pulse position for bit 5		8.2	8.4	8.6	nS
T_{PPOS6}	Output pulse position for bit 6		9.88	10.08	10.28	nS
T_{CIP0}	TxCLK IN period (single output mode)	-	11.76	T	40	nS
T_{CIP1}	TxCLK IN period (dual output mode)	-	5.88	T/2	20	nS
T_{STC}	TxIN setup to TxCLK IN in low swing mode	25 ~ 165 MHz	0.9	-	-	nS
T_{HTC}	TxIN hold to TxCLK IN in low swing mode		1	-	-	nS
T_{CIH}	TxCLK IN high time	-	0.4T	0.5T	0.6T	nS
T_{CIL}	TxCLK IN low time	-	0.4T	0.5T	0.6T	nS
T_{CIT}	TxCLK IN transition time	-	0.8	1	1.2	nS
T_{PLLS}	Phase lock loop set	-	-	-	10	mS
T_{PDD}	Power down delay	-	-	-	100	nS

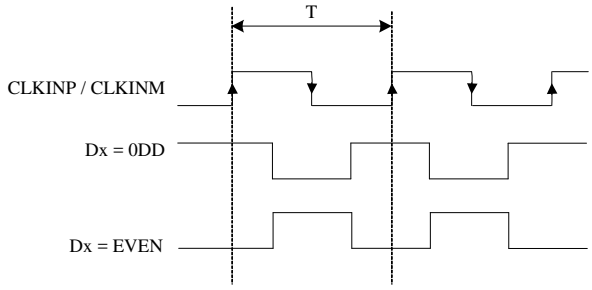


Figure 4. Worst Case Test Pattern

Figure 5. Tx Input Clock Transition Time

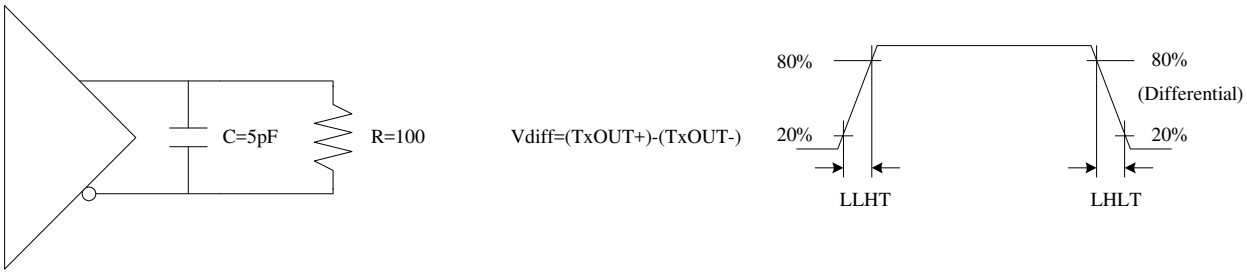


Figure 6. LVDS Output Load and Transition Time

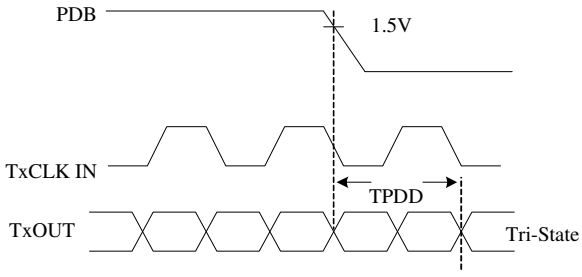


Figure 7. Tx Power Down Delay

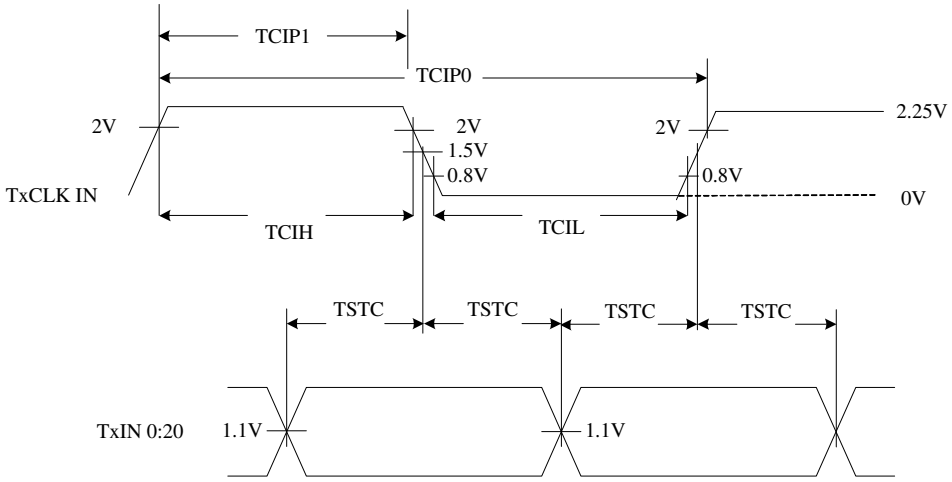


Figure 8. Tx Setup/Hold and High/Low Time

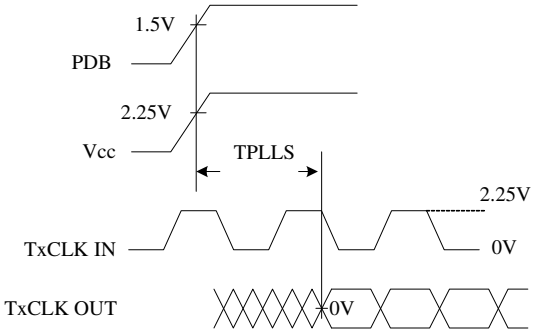


Figure 9. Tx PLL Set Time

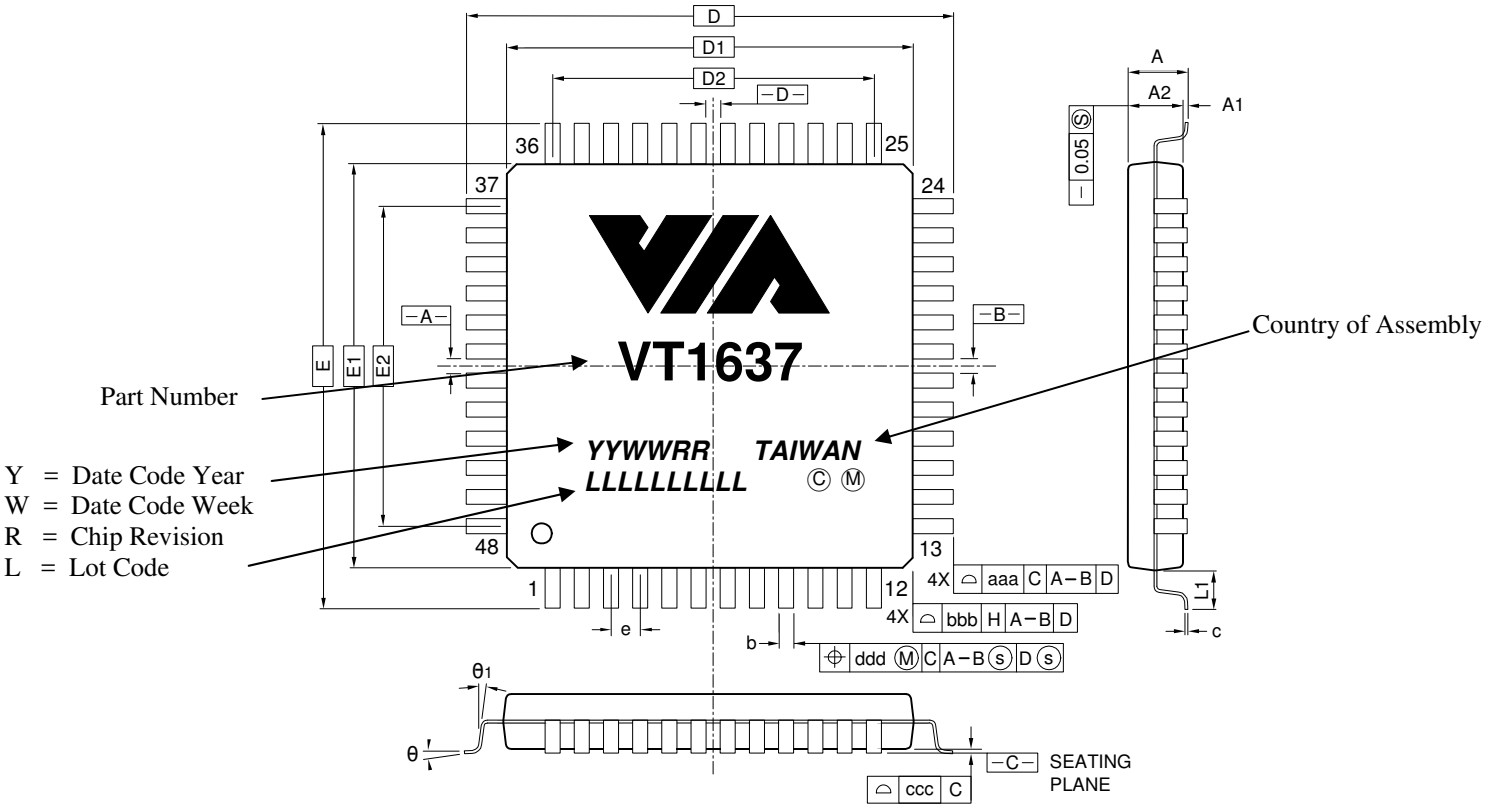
Recommended Operating Conditions

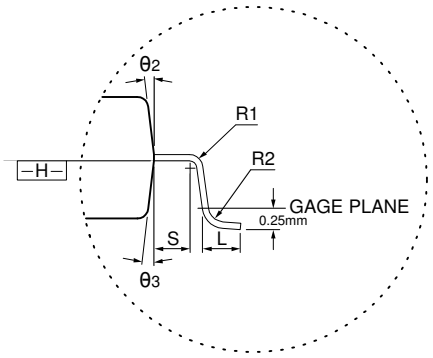
Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{cc}	Supply voltage	2.25	2.5	2.75	V
T_A	Operating free air temperature	0	25	85	°C

Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{STG}	Storage temperature	-25	-	150	°C
V_{ESD}	Electrostatic Discharge (Human Body)	-	-	2.5	KV
T_{VPS}	Vapor Phase Soldering (1 min.)	-	-	255	°C

Package Mechanical Specifications





CONTROL DIMENSIONS ARE IN MILLIMETERS.

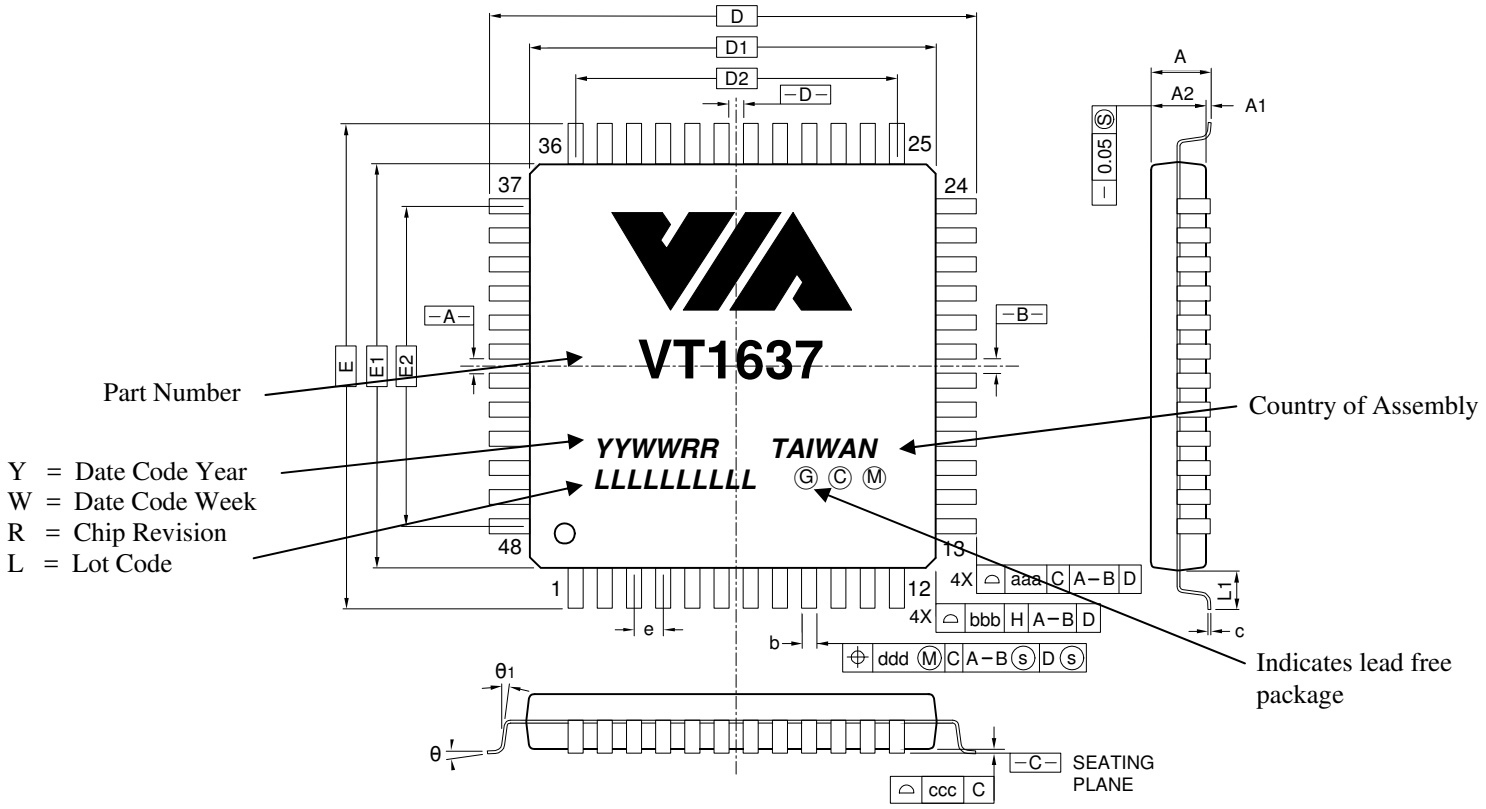
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

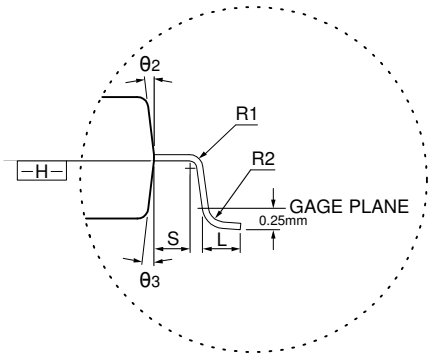
NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 10. Mechanical Specification – 48-Pin LQFP (7x7 mm)





CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BASIC			0.354 BASIC		
E	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E1	7.00 BASIC			0.276 BASIC		
D2	5.50 BASIC			0.217 BASIC		
E2	5.50 BASIC			0.217 BASIC		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BASIC			0.020 BASIC		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 11. Mechanical Specification for Lead-Free – 48-Pin LQFP (7x7 mm)