Data Sheet

VT2021
High Definition Audio Codec

June 26, 2012
Revision 1.02

Revision History

Rev	Date	Initial	Note
1.0	Jul. 9, 10	TL	Initial public release
1.01	Jun. 14, 12	TL	Updated Section 1 Product Features, 2 Overview, and 3 Functional Block Diagram Added Link Reset and Initialization Timing, Link Timing Parameters at the Codec, and SPDIF AC Timing Characteristic in Section 10 Electrical Specification Corrected typos Updated legal page
1.02	Jun. 26, 12	TL	Updated SPDIF AC Timing Characteristics in 10.3 AC Characteristics

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1 Product Features

VT2021

High Definition Audio Codec

1.1 Hardware Features

- **Compliant with Intel High Definition Audio Specification Rev. 1.1**
- **Exceeds Microsoft Windows Logo Program (WLP) and Windows Hardware Certification (WHC) Requirements**
- **Five Stereo Digital-to-analog Converters**
  - 16-, 20-, 24-bit Resolution
  - Audio Sampling Rates: 48 kHz, 96 kHz, 192 kHz, 44.1 kHz, and 88.2 kHz
  - DAC SNR: 110 dB
- **Two Stereo Analog-to-digital Converters**
  - 16-, 20-, 24-bit Resolution
  - Audio Sampling Rates: 48 kHz, 96 kHz, 192 kHz, and 44.1 kHz
  - ADC SNR: 100 dB
- **Jack Presence Detection**
  - Two Jack Detection Pins; Each Detects up to Four Jacks Plugging
  - Jack-detect Circuit with Unsolicited Response
- **Two Independent S/PDIF TX Outputs Supporting Two Output Pins**
  - 16-, 20-, 24-bit Resolution
  - Audio Sampling Rates: 48 kHz, 96 kHz, 192 kHz, 44.1 kHz, and 88.2 kHz
  - Primary S/PDIF TX for Connecting to an External High Quality Digital Decoder or Speaker
  - Secondary S/PDIF TX for Digital Audio Output to a HDMI Transmitter.
- **One S/PDIF RX Input**
  - 16-, 20-, 24-bit Resolution
  - Audio Sampling Rates: 32 kHz, 48 kHz, 96 kHz, 44.1 kHz, and 88.2 kHz
- **Analog Microphone**
  - Software Selectable Boost Gain (10 dB/ 20 dB/ 30 dB) for Analog Microphone Input
  - Four Sets of Adjustable Vref-Out Pins for Microphone Bias
- **Four Built-in Headphone Amplifiers**
- **Functionality of Pins:**
  - Headphone, Line Out, Line In, and Microphone
    - Pin 14 and Pin 15 (Port E)
    - Pin 16 and Pin 17 (Port F)
  - Line Out, Line In, and Microphone
    - Pin 21 and Pin 22 (Port B)
    - Pin 23 and Pin 24 (Port C)
  - Headphone and Line Out
    - Pin 35 and Pin 36 (Port D)
    - Pin 39 and Pin 41 (Port A)
  - Line Out
    - Pin 43 and Pin 44(Port G)
    - Pin 45 and Pin 46 (Port H)
- **Front Panel Jack Re-tasking**
- **Supports Smart 5.1 Output and Mono-out**
- **High Performance Analog Mixer (for AA-path)**
- **Two GPIO (General Purpose Input and Output) Pins for Customized Application**
- **High Quality Differential CD Input**
- **HPF in ADC Path for DC Removal**
- **Supports EAPD (External Amplifier Power Down**)
- **Supports 1.5 ~ 3.3V I/O for HD Audio Link**
- **Optimized Management of Pop Mitigation**
- **Power Management and Enhanced Power Saving Features**
  - Reduced Power Consumption in Compliance with EC Energy Using Products Directive (EuP) Lot 6 in Standby and Off-mode.

- **Blu-ray and HD DVD Audio Content Protection**
  - Content Protection for Full Rate Loss-less DVD Audio, and Blu-ray DVD and HD-DVD Audio Content Play-back (with Selected Versions of Win DVD/Power DVD)
- **Package**
  - Available in 48-Pin LQFP Lead-free and RoHS Compliant Package

1.2 Software Features

- **Meets Microsoft WLK1.6 and Conforms to the Requirements of Windows Hardware Quality Labs Testing (WHQL)**
- **Functions of Speaker Device**
  - Equalizer (EQ)
  - Room Correction (RC)
  - Bass Management (BM)
  - Environment Modeling (EM)
  - Loudness Equalization (LE)
  - Speaker Fill (SF)
- **General Features for Mic-Array Application**
  - Acoustic Echo Cancellation (AEC)
  - Noise Suppression (NS)
  - Beam Forming (BF)
- **Recording Control for Microphone Input**
- **Digital Output Control UI**
- **VIA Driver Support**
  - Microsoft Windows 7
  - Microsoft Windows Vista (32-bit/ 64-bit)
  - Microsoft Windows XP
  - Microsoft Windows Server 2003
  - Microsoft Windows 2000
  - WinCE 4.2/ 5.0/ 6.0
  - Linux (Fedora Core 7, 8 / Suse SLED Desktop 10SP1 / UBUNTU 7.1 / Redhat)
- **Optional Sound Effect**
  - QSound 3D Audio Effects
  - DTS CONNECT / DTS Surround Sensation
  - Dolby PCEE Program
  - Creative Audio Program
  - Third Party Microphone Array Technology
- **Optional Software Feature**
  - Karaoke Mode for Home Entertainment
  - Dynamic Range Control with Adjustable Parameters

2 Overview

The VT2021 is a low-power optimized, high fidelity, 10-channel High Definition Audio Codec which is compatible with Intel High Definition Audio specification. The VT2021 codec supports stereo 24-bit resolution and up to 192 kHz sample rate for DACs/ADCs.

The VT2021 features five stereo DACs, two stereo ADCs, four built-in headphone amplifiers, high performance analog mixer for AA-path, two independent S/PDIF outputs, and one S/PDIF input. It can achieve 110 dB Signal-to-Noise Ratio (SNR) for DACs and 100 dB SNR for ADCs. The SPDIF transmitter supports sampling rates of 44.1 kHz, 48 kHz, 88.2 KHz, 96 kHz, and 192 kHz.

The VT2021 supports Content Protection with AES Decipher Module for Full Rate Loss-less DVD Audio, Blu-ray DVD and HD-DVD Audio Content Playback (with selected Versions of WinDVD / Power DVD) for optimal 24-bit/192 kHz audio output and bringing cinema-level audio experience. Without content protection support, audio quality is dramatically reduced to that of a regular CD with a sampling rate of only 16-bit/48 kHz. The VT2021 also features advanced VoIP and music enhanced functions.

The stereo ADCs and microphone array can support Acoustic Echo Cancellation (AEC), Beam Forming (BF), and Noise Suppression (NS) technologies. The VT2021 uses two jack detection pins for presence detection on up to eight audio jacks. This function allows software to determine if there is a device plugged into the circuit. VT2021 also supports front-panel jack re-tasking feature that allows flexible configurations.

The VT2021 High Definition Audio Codec is embedded with software utilities such as environment emulation, dynamic range compressor, EQ and extender, and the optional sound effects, including QSound, DTS[1] Connect, Dolby[2] Digital Live, Dolby PCEE program, and Creative audio program. The VT2021 is available in a 48-Pin LQFP Pb-free and RoHS compliant package. The VT2021 is an integrated and high-performance audio solution for high-end desktops and notebooks.

[1] Supply of this implementation of DTS technology does not convey a license or imply a right under any patent, or any other industrial or intellectual property right of DTS to use such implementation in any finished end-user or ready-to-use final product. Notice is hereby provided that a license from DTS is required prior to such use.

[2] Supply of this Implementation of Dolby technology does not convey a license nor imply a right under any patent, or any other industrial or intellectual property right of Dolby Laboratories, to use this Implementation in any finished end-user or ready-to-use final product. It is hereby notified that a license for such use is required from Dolby Laboratories.

3 Functional Block Diagram

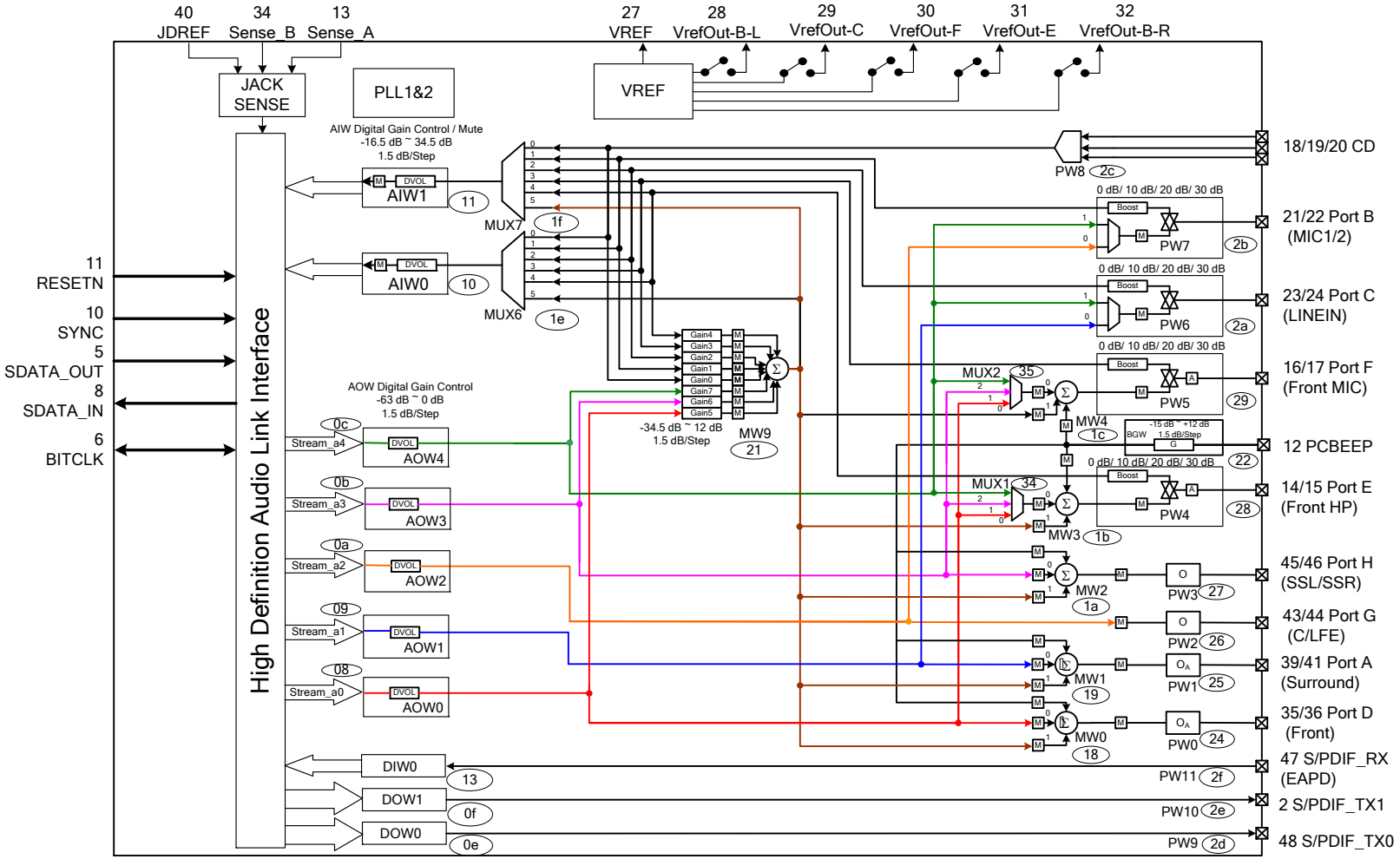


Figure 1 – VT2021 Functional Block Diagram

4 Pinout

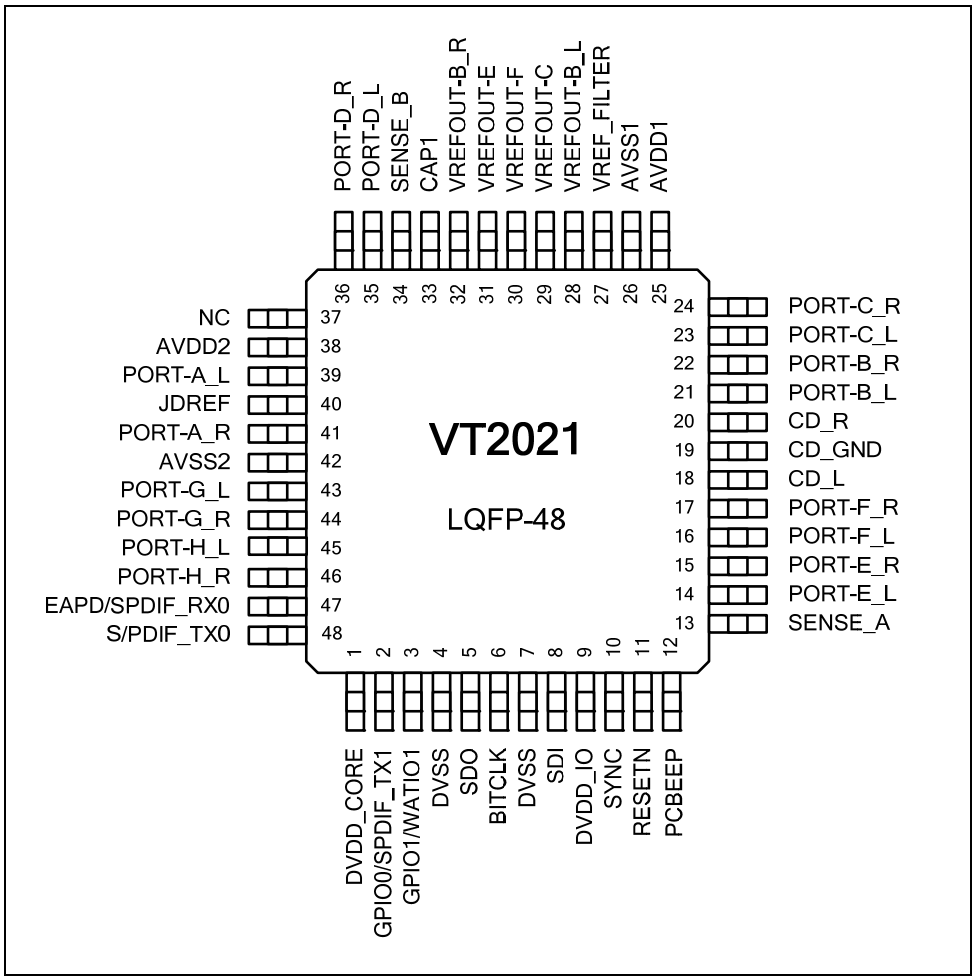


Figure 2 – VT2021 Pin Diagram for LQFP-48 (Top View)

5 Pin List

Table 1 – VT2021 Pin List

Pin #	Pin Name	Pin #	Pin Name
1	DVDD_CORE	25	AVDD1
2	GPIO0/SPDIF_TX1	26	AVSS1
3	GPIO1	27	VREF_FILTER
4	DVSS	28	VREFOUT-B_L
5	SDO	29	VREFOUT-C
6	BITCLK	30	VREFOUT-F
7	DVSS	31	VREFOUT-E
8	SDI	32	VREFOUT-B_R
9	DVDD_IO	33	CAP1
10	SYNC	34	SENSE_B
11	RESETN	35	PORT-D_L (Front Left)
12	PCBEEP	36	PORT-D_R (Front Right)
13	SENSE_A	37	NC
14	PORT-E_L (Front HP Left)	38	AVDD2
15	PORT-E_R (Front HP Right)	39	PORT-A_L (Surr. Left)
16	PORT-F_L (Front MIC 1)	40	JDREF
17	PORT-F_R (Front MIC 2)	41	PORT-A_R (Surr. Right)
18	CD_L	42	AVSS2
19	CD_GND	43	PORT-G_L (Center / LFE)
20	CD_R	44	PORT-G_R (LFE / Center)
21	PORT-B_L (MIC 1)	45	PORT-H_L (Side Surr. Left)
22	PORT-B_R (MIC 2)	46	PORT-H_R (Side Surr. Right)
23	PORT-C_L (LINE IN L)	47	EAPD / SPDIF_RX0
24	PORT-C_R (LINE IN R)	48	S/PDIF_TX0

6 Pin Description

Table 2 – Signal Type Definitions

Type	Description
I	**Input.** Standard input-only signal.
O	**Output.** Standard active output driver.
IO	**Input/output.** An input/output signal.
P	**Power.**

6.1 Digital I/O Pins

Pin #	Pin Name	I/O	Signal Description
2	GPIO0/ SPDIF_TX1	I/O	GPIO0, 2nd S/PDIF Output
3	GPIO1	I/O	GPIO1
5	SDO	I	Serial Data Input from Controller
6	BITCLK	I	24 MHz Bit Clock from Controller
8	SDI	I/O	Serial Data Output to Controller
10	SYNC	I	Sample SYNC from Controller
11	RESETN	I	Hardware Reset from Controller
47	EAPD / SPDIF_RX0	I/O	1st S/PDIF_RX; External Amplifier Power-down
48	S/PDIF_TX0	O	1st S/PDIF Output

6.2 Analog I/O Pins

Pin #	Pin Name	I/O	Signal Description
13	SENSE_A	I	Jack Detect Pin 1
34	SENSE_B	I	Jack Detect Pin 2
14	PORT-E_L	I/O	Analog Output for Front Panel HP Out Left
15	PORT-E_R	I/O	Analog Output for Front Panel HP Out Right
16	PORT-F_L	I/O	Analog I/O. Default is Input for Front MIC.
17	PORT-F_R	I/O	Analog I/O. Default is Input for Front MIC.
18	CD-L	I	CD Input Left Channel
20	CD-R	I	CD Input Right Channel
21	PORT-B_L	I/O	Analog I/O. Default is Input for MIC1 Left.
22	PORT-B_R	I/O	Analog I/O. Default is Input for MIC1 Right.
23	PORT-C_L	I/O	Analog I/O. Default is Input for Line-in Left.
24	PORT-C_R	I/O	Analog I/O. Default is Input for Line-in Right.
35	PORT-D_L	O	Analog Output for Line-out Left
36	PORT-D_R	O	Analog Output for Line-out Right
39	PORT-A_L	O	Analog Output for Surround-out Left
41	PORT-A_R	O	Analog Output for Surround-out Right
43	PORT-G_L	O	Analog Output for Center
44	PORT-G_R	O	Analog Output for LFE
45	PORT-H_L	O	Analog Output for Surround Back Left
46	PORT-H_R	O	Analog Output for Surround Back Right

Pin #	Pin Name	I/O	Signal Description
12	PCBEEP	I	PC Beep Signal Input
27	VREF_FILTER	O	Reference Voltage Capacitor
28	VREFOUT-B_L	O	Reference Voltage Output for Port B Left
29	VREFOUT-C	O	Reference Voltage Output for Port C
30	VREFOUT-F	O	Reference Voltage Output for Port F
31	VREFOUT-E	O	Reference Voltage Output for Port E
32	VREFOUT-B_R	O	Reference Voltage Output for Port B Right
33	CAP1	O	Optional Capacitor for ADC Reference
40	JDREF	O	External Resistor for Jack Detect Circuit

6.3 Power and Ground

Pin #	Pin Name	I/O	Signal Description
1	DVDD_CORE	P	Digital Core Power: 3.3V
9	DVDD_IO	P	Digital Power for HDA Link: 1.5V~3.3V
4	DVSS	P	Digital VSS
7	DVSS	P	Digital VSS
19	CD_GND		
25	AVDD1	P	Analog VDD
38	AVDD2	P	Analog VDD
26	AVSS1	P	Analog VSS
42	AVSS2	P	Analog VSS

6.4 NC Pins (No-connection Pins)

Pin #	Pin Name	I/O	Signal Description
37	NC	N.A.	N.A.

7 High Definition Audio Link Protocol

7.1 Link Signaling

The link protocol defines the digital serial interface that connects the High Definition Audio Codec to the audio controller, and is not compatible with the previous AC97 protocol. The link is controller synchronous, based on a fixed 24 MHz BITCLK and is purely isochronous without any flow control.

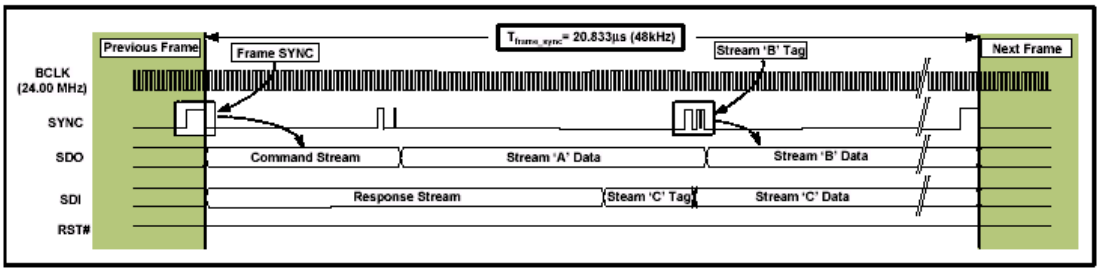


Figure 3 – High Definition Audio Link Conceptual View

7.2 Signal Definitions

Table 3 – High Definition Audio Link Signal Description

Signal Name	Source	Type	Description
BITCLK	Controller	I	24 MHz Clock
SYNC	Controller	I	Global 48 kHz Frame Sync and Outbound Tag Signal.
SDO	Controller	I	Bussed Serial Data Output from Controller.
SDI	Codec & controller	IO	Point-to-point Serial Data. The controller has a weak pull down.
RESETN	Controller	I	Global Active Low Reset Signal.

BITCLK is the 24-MHz clock sourced from the controller and connecting to all codec on the link.

SYNC marks input and output frame boundaries (Frame Sync) as well as identifying outbound data streams (stream tags). SYNC is always sourced from the controller and connects to all codec on the link.

SDO is driven by the controller to all codec on the link. Compared with AC97, the SDO is double pumped with respect to both rising and falling edges of BITCLK in order to increase the bandwidth required for High Definition Audio link.

SDI is a point-to-point data signal driven by the codec to the controller. Because the bandwidth requirement is not that high compared with SDO, the data is single pumped with respect to only the rising edge of BITCLK. The controller is required to implement weak pull-down on all SDI signals.

RESETN is sourced from the controller and connects to all codec on the link. Assertion of RESETN results in all link interface logic being reset to Default power on state.

The following figure shows the timing diagram of BITCLK, SYNC, SDO and SDI.

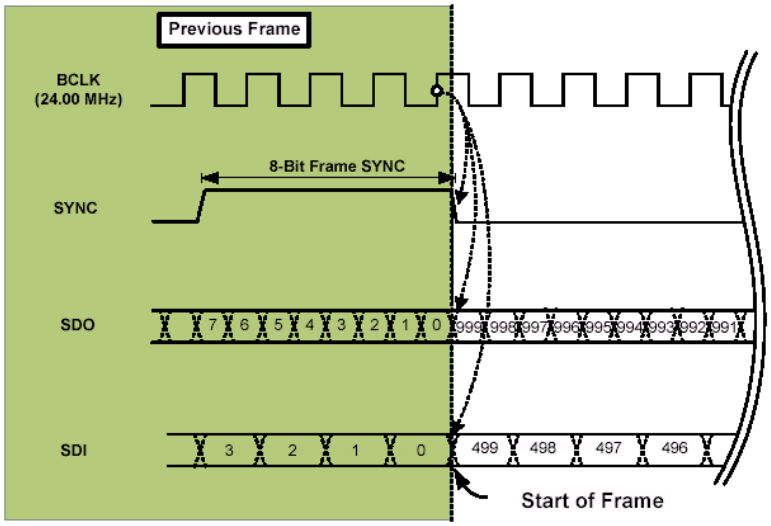


Figure 4 – Bit Timing Diagram

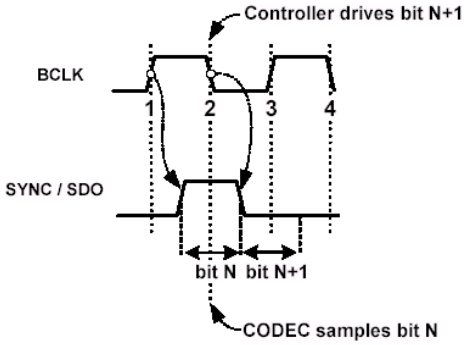


Figure 5 – SYNC and SDO Timing Relative to BITCLK

Figure 5 shows that both SYNC and SDO may be toggled with respect to either edge of BITCLK. In particular, bit cell n+1 is driven by the controller on SDO with respect to clock edge #2, and is sampled by the codec with respect to the subsequent clock edge, #3, and so forth.

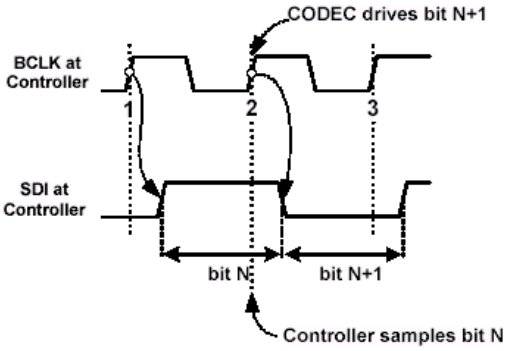


Figure 6 – SDI Timing Relative to BITCLK

Figure 6 shows that SID may only be toggled with respect to the rising edge of BITCLK. In particular, bit cell n+1 is driven by the codec on SDI with respect to rising clock edge #2 and is sampled by the controller with respect to the subsequent rising clock edge, #3, and so forth.

7.3 Signaling Topology

The following diagram shows a typical system with one controller and its associated codec.

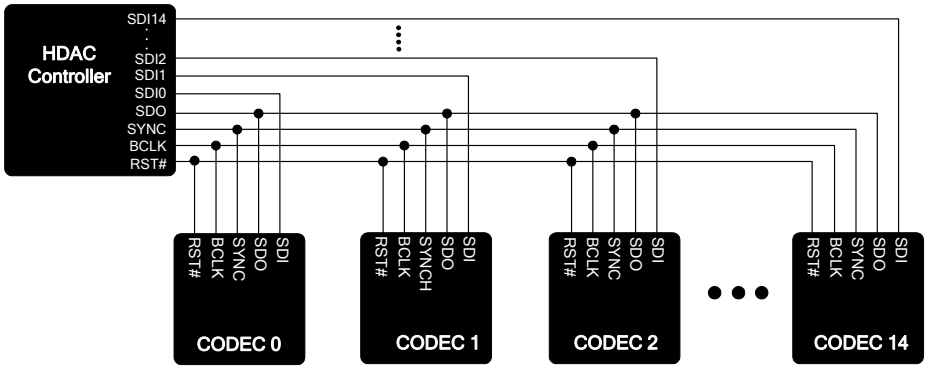


Figure 7 – Basic High Definition Audio System

7.4 Frame Composition

A frame is defined as a 20.833 µs window of time marked by the falling edge of the Frame Sync marker, which identifies the start of each frame. The controller is responsible for generating the Frame Sync marker, which is a high-going pulse on SYNC, exactly four BITCLK in width.

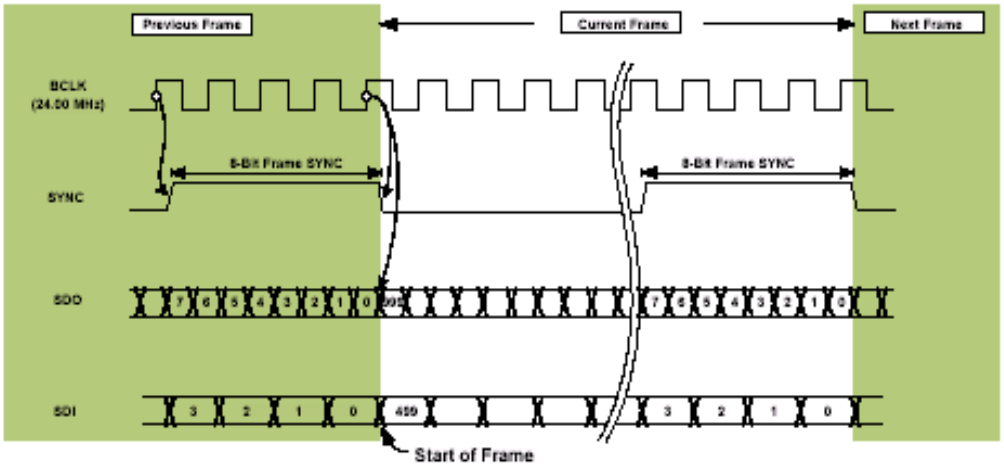


Figure 8 – Frames Demarcation

Both inbound and outbound frames are made up of three major components, specifically:

- A single Command / Response Field
- Zero or more Stream Packets
- A Null Field to fill out the frame

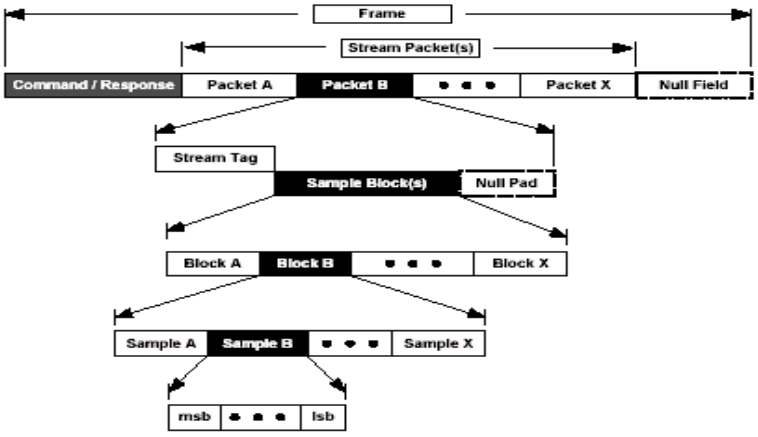


Figure 9 – Frame Composition

Command / Response Field is used for link and codec management. One of these fields appears exactly once per frame, MSB first, and is always the first field in the frame. It is composed of a 40-bit Command Field on each outbound frame from the controller and a 36-bit Response Field on each inbound frame from the codec.

Stream Tag is the label at the beginning of each stream packet that provides the associated stream ID. All data in one stream packet belongs to a single stream.

Sample Block is a set of one or more samples, the number of which is specified by the "Channels" field of the Stream Descriptor Format registers. Samples in a given sample block are associated with a single given stream, have the same sample size, and have the same time reference. And no padding is permitted between samples.

Ordering of samples within a block is always the same for all blocks in a given stream.

Sample is a set of bits providing a single sample point of a single analog waveform.

Null Field is used to fill up the remainder of the bits in each frame that are not used for Command / Response or packets. A null field must be transmitted as logical 0's.

7.5 Output Frame

7.5.1 Stream Tags

Outbound stream tags are 8 bits in length and are transmitted at a double pumped rate as side band information on SYNC. It is composed of a 4-bit preamble which is signaled as three SDO bit times high followed by one SDO bit time low. This is immediately followed by a 4-bit Stream ID. Outbound stream tags are transmitted on SYNC so as to align with the last eight data bits of the preceding stream packet or Command Field.

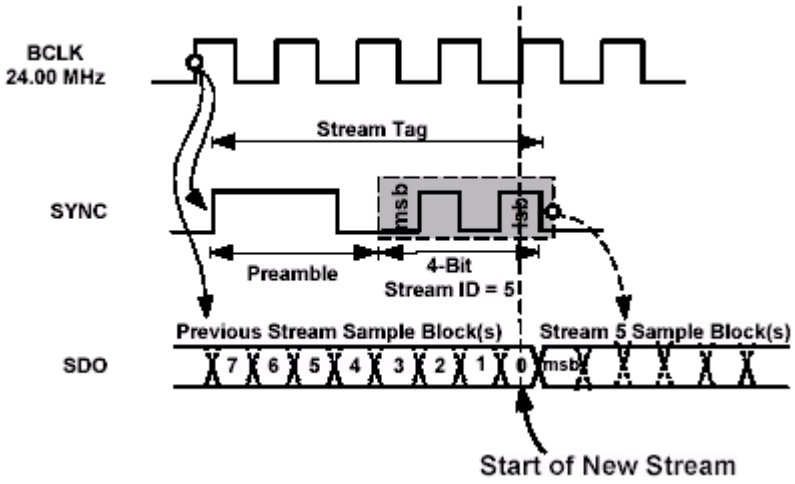


Figure 10 – Outbound Stream Tag Format and Transmission

7.5.2 Outbound Frames

Outbound frames start and end between the falling edges of successive Frame Syncs. The first 40 bits are dedicated for the Command field and are sued to send commands to codec. The controller transmits the tag for the first outbound packet on SYNC during the last eight bit times of the Command field. The sample blocks for the first packet are transmitted on SDO immediately following the Command field. There is no proscribed order in which the different stream packets are to be transmitted. The controllers are required to transmit a null field for the remaining bits within an outbound frame when the transmission of the stream packets completes before the end of the frame.

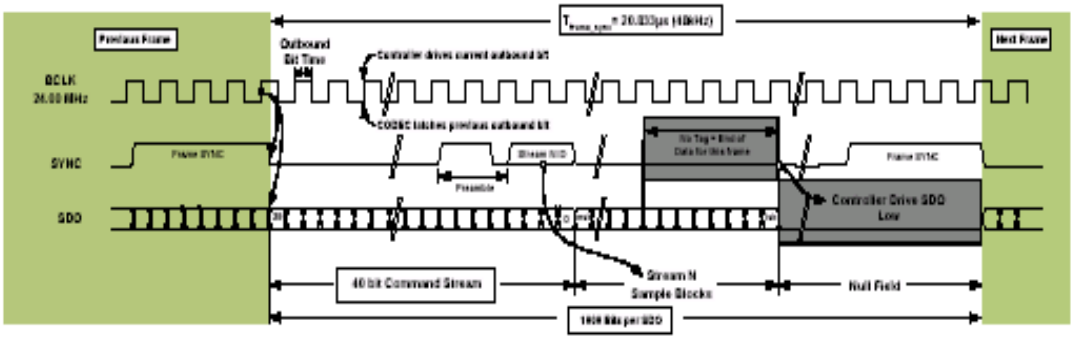


Figure 11 – Outbound Frame with Null Field

7.6 Input Frame

7.6.1 Stream Tags

An inbound stream tag is 10 bits in length, and is transmitted "in-line" at a single pumped rate on SDI, immediately preceding the associated inbound sample blocks. It is composed of a 4-bit stream ID, followed by a 6-bit data length field that provides the length, in bytes, of all sample blocks with the given stream packet.

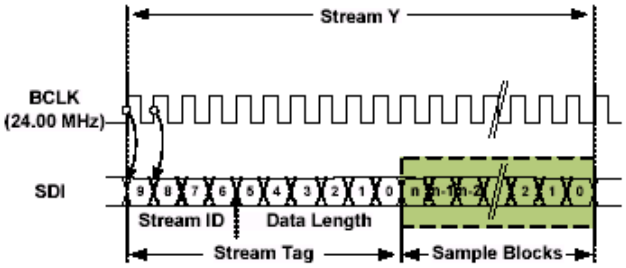


Figure 12 – Inbound Tag Format and Transmission

7.6.2 Inbound Frames

Inbound frames start and end between the falling edges of successive Frame Syncs. The first 36 bits of an inbound frame are dedicated for the Response Field, which codec use for sending responses to controller commands. The codec transmits the first stream packet on SID immediately following the Response Field. A stream tag indicating a packet length of zero must immediately follow the last stream packet to be transmitted. Such a stream tag marks the completion of data transmission within that frame, and the remaining valid bit positions are set to the null field. In the event there are less than 10 valid bit positions remaining in the frame after the last stream packet, then no termination tag is transmitted, and the remaining bits are the null field.

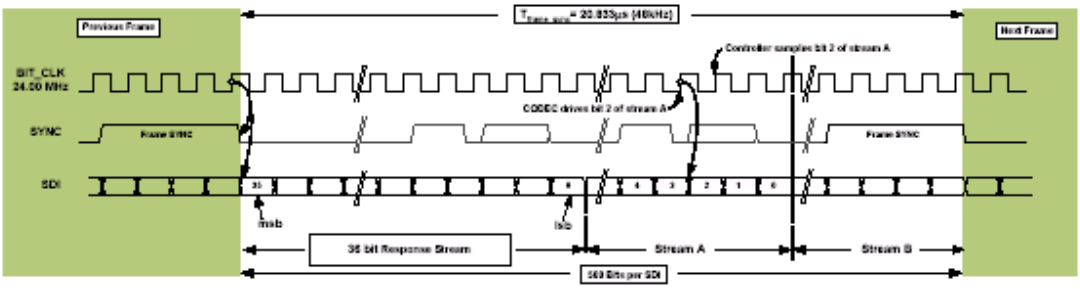


Figure 13 – Inbound Frame with No Null Field

7.7 Reset and Initialization

7.7.1 Link Reset

A link reset is signaled on the link by assertion of the RESETN signal, and results in all Link interface logic in both codec and controller, including registers, being initialized to their Default state. The controller drives all SDO and SYNC outputs low when entering or exiting link reset.

A controller may only initiate the link reset entry sequence after completing any currently pending initialization or state change requests.

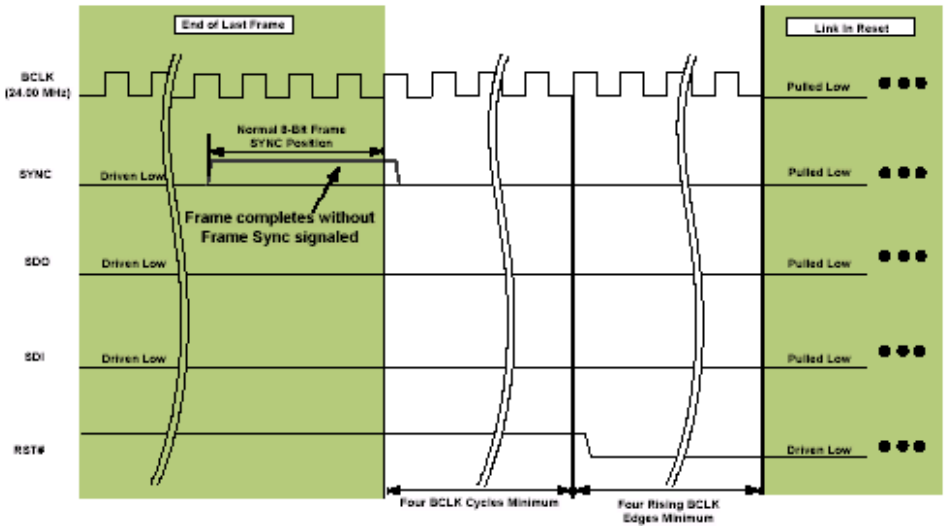


Figure 14 – Link Reset Entry Sequence

The sequence when entering link reset is described as the following.

1. The controller synchronously completes the current frame but does not signal Frame Sync during the last eight SDO bit times.
2. The Controller synchronously asserts RESETN four or more BITCLK cycles after the completion of the current frame.
3. BITCLK is stopped a minimum of four clocks after the assertion of RESETN.

In the event of a host bus reset, the above sequence does not complete, and RESETN is asynchronously asserted immediately and unconditionally.

Regardless of the reason for entering Link Reset, it may be exited only under software control and in a synchronous manner.

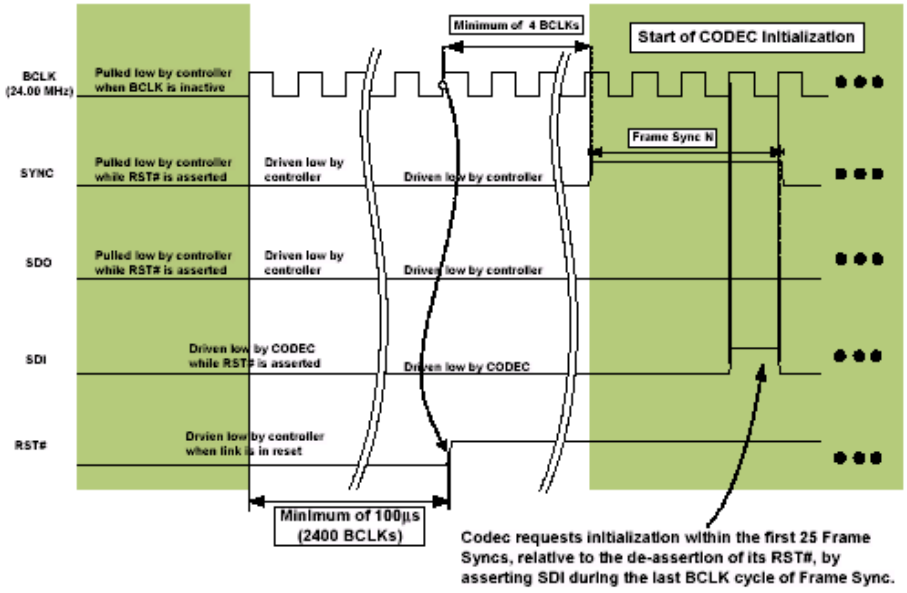


Figure 15 – Link Reset Exit Sequence

The sequence when exiting link reset is described in the following.

1. The controller provides a properly running BITCLK for a minimum of 100 μs (2400 BITCLK cycles or more) before the de-assertion of RESETN. This allows time for codec PLLs to lock.
2. The RESETN signal is de-asserted.
3. The SYNC commences signaling valid frames on the link with the first Frame Sync that occurs at a minimum of four BITCLK cycles after the de-assertion of RESETN.
4. The codec must signal an initialization request via SID within the first 25 Frame Syncs relative to the de-assertion of their respective RESETN signal.

7.7.2 Codec Function Group Reset

A codec function group reset is initiated via the Function_Reset verb and results in all logic within the targeted function group being driven to its Default or reset state. By Default VT2021 does not signal a state change and initialization request on SDI after the Function_Reset verb, and still keeps its codec address previously assigned by the controller. This behavior can be changed by setting a vendor defined register bit for backward compatible with the High Definition Audio Spec. See the Vendor Defined verbs in the Audio Function Group for the detail.

7.7.3 Codec Initialization

Immediately following the completion of Link Reset sequence (or Function_Reset verb, if enabled by the vendor-defined verb), VT2021 proceeds through a codec initialization sequence, which provides each codec with a unique address by which it can thereafter be referenced to Commands on the SDO signal. During this sequence, the controller provides each requesting codec with a unique address using its attached SDI signals.

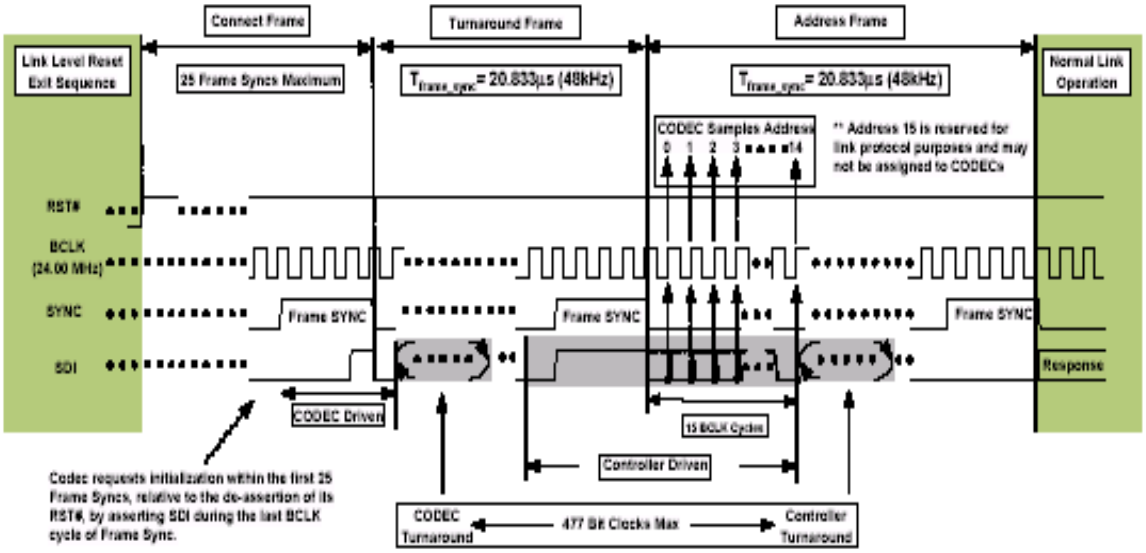


Figure 16 – Codec Initialization Sequence

The codec initialization sequence occurs across three contiguous frames immediately following any reset sequence. During these three frames, the codec are required to ignore all outbound traffic present on SYNC & SDO. These three frames, labeled as the "Connect Frame", the "Turnaround Frame", and the "Address Frame", are described in the following sub-section.

7.7.3.1 Connect and Turnaround Frames

In the Connect and Turnaround Frames, the codec signals its request for initialization on SDI and then releases SDI (turnaround) to be driven by the controller in the subsequent address frame.

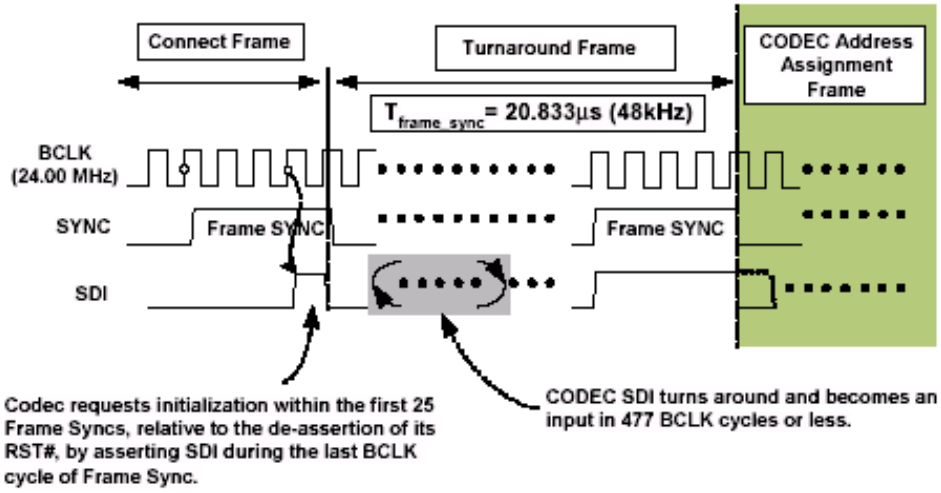


Figure 17 – Connect and Turnaround Frames

The codec signals an initialization request by synchronously driving SDI high during last bit clock cycle of Frame Sync. SDI must be asserted for the entire BITCLK cycle and must be synchronously de-asserted the same rising edge of BITCLK as the de-assertion of the Frame Sync. The codec are only permitted to signal an initialization request on a null input frame, a frame in which no response stream or input streams are being sent.

In the Turnaround Frame, the codec and controllers are required to turn SDI around upon the completion of the Connect Frame. To do this, the codec actively drives SDI low for one BITCLK cycle immediately following the de-assertion of SYNC at the end of the Connect Frame. The codec then puts its SDI drivers in a high impedance state at the end of the first BITCLK cycle in the Turnaround Frame. Four BITCLK cycles before the end of the Turnaround Frame, SYNC and SID are driven high by the controller. The SDI remains driven high through the end of the Turnaround Frame in preparation for the subsequent address frame.

7.7.3.2 Address Frames

During the Address Frame, SDI is a codec input and is driven by the controller beginning in the last four BITCLK periods (Frame Sync) of the Turnaround Frame. The falling edge of Frame Sync marks the start of codec address assignment. Address assignment is indicated by the controller holding each SDI high for the number of BITCLK cycles equal to the numeric ID of that particular SDI. Thus the unique address of the codec becomes the ID of its attached SDI.

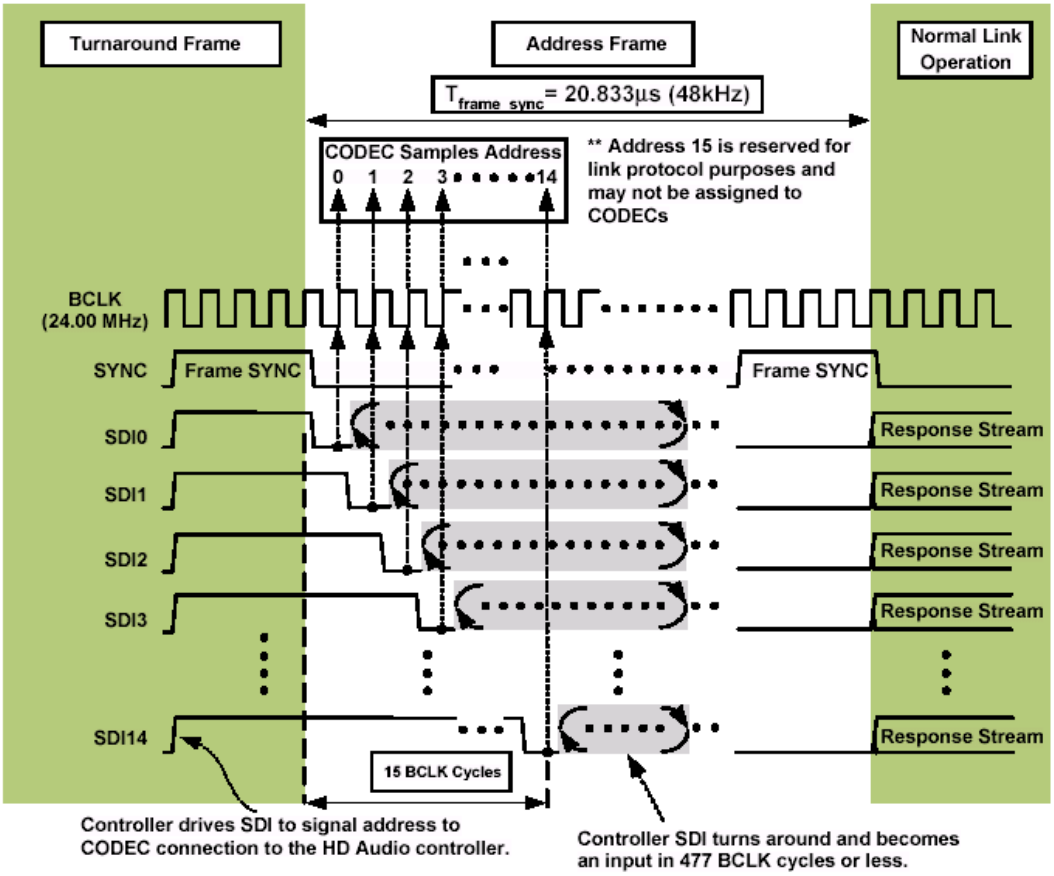


Figure 18 – Address Frame

The codec count from zero to fourteen starting on the rising edge of BITCKL following the de-assertion of Frame Sync, and sample the value of this count for their unique address on the first rising edge of BITCLK in which SYNC and SDI are both sampled low.

The controller must put its SDI drivers in a high impedance state by the rising edge of the 18th BITCLK of the address frame but not before driving each SDI low for at least one clock cycle. The SDI then becomes an input to the controller. Normal link operation starts on the frame following the completion of the Address Frame, and the codec is required to actively drive a valid response field and to be ready to accept commands in this and subsequent frames.

7.8 Handling Stream Independent Sample Rates

Unlike AC97, the Link is source synchronous and has no codec initiated flow control, the controller generates all sample transfer timing.

7.8.1 Codec Sample Rendering Timing

VT2021 supports the all the multiples and submultiples of the base rates of 48 kHz & 44.1 kHz, up to the maximum rate respectively of the DAC and ADC. For DAC, up to 192 kHz sample rate is supported. For ADC, the maximum rate is 96 kHz.

Table 4 – Sample Rate Supported

Multiple	Base Rate 48 kHz	Base Rate 44.1 kHz
1/6	8 kHz	
1/4		11.025 kHz
1/3	16 kHz	
1/2		22.05 kHz
2/3	32 kHz	
1	48 kHz	44.1 kHz
2	96 kHz	88.2 kHz
4	192 kHz	176.4 kHz

7.8.2 Link Sample Delivering Timing

For streams whose sample rate is a natural harmonic of 48 kHz, the timing is relatively straightforward. The rates in multiple (N) of 48 kHz are containing N sample blocks in one frame. For the rates in sub-multiple (1/N) of 48 kHz, there must be one sample block transmitted every one in N frames, and the intervening N-1 frames will contain no sample for this stream.

Since the link frame rate is fixed at 48 kHz, streams using a base rate of 44.1 kHz must have samples transmitted on a cadence creating the slightly lower aggregate transmission rate to match the slightly lower rendering rate. For streams running at a sample rate of 44.1 kHz, there're occasional frames that will not contain a sample generating the following cadence.

12-11-11-12-11-11-12-11-11-12-11-11-11- (repeat)

The dashes indicate frames that do not contain a sample block. The cadence repeats continuously generating exactly 147 sample blocks every 160 frames, and avoids any long term drift between sample delivery and rendering clock.

Sample rates that are integral multiples of 44.1 kHz apply the "12-11" cadence rule just as a 44.1 kHz sample rate would, except that non-empty frames contain multiple (2 or 4) sample blocks, instead of just one.

For a sample rate of 22.05 kHz, the transmission pattern becomes:

{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{12}-*{11}-*{11}-*{11}-* (repeat)
where
{12} = 1*1*1*1*1*1*1*1*1*1*1*1*
{11} = 1*1*1*1*1*1*1*1*1*1*1*

and the asterisks * represent a frame in which there is no sample block.

For a sample rate of 11.025 kHz, the transmission pattern becomes:

[12]-*[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[12]-***[11]-***[11]-***[11]-*** (repeat)**
where
[12] = 1*1***1***1***1***1***1***1***1***1***1***1*****
[11] = 1*1***1***1***1***1***1***1***1***1***1*****

and the asterisks * represent a frame in which there is no sample block.

These framing sequences apply only to the outbound (SDO) data from the controller. Inbound (SDI) data transmitted by the codec is permitted to deviate for minimizing codec buffer management.

7.9 Power Management

Whenever the Link is commanded to enter a low power state, it enters the link-reset state. This state is only exited in response to a software command and follows all link rules for exiting the link reset state.

The Audio Function Group and the analog input / output converter widgets support power control function. The whole chip power states can be controlled through the Audio Function Group, while individual DACs and ADCs can also be controlled through the corresponding power state control verbs. The following table describes the definition of the power states.

Power States	Definitions	Referenced with AC97
D0	All power on. Individual ADCs & DACs can be controlled.	
D1	All amplifiers and analog converters are powered down. Register values maintained, and analog reference voltage is still on.	PR0 & PR1 & PR2
D2	Register values maintained, but analog reference voltage is also down.	PR3
D3	Same as D2 state.	PR3

7.10 Unsolicited Response Behavior Description

- The "unsolicited response" occurs as the jack is plugged in and pulled out.
- At the initial state (boot-up or wake-up), the jack is already plugged-in, and the "unsolicited response" does not report. Bit 31 of pin sense register needs to correctly report whether anything is plugged in.
- All pin widgets except SPDIF TX, analog jacks externally exposed, and the 3.55 mm (1/8'') mini jack type, need "unsolicited response".
- "Unsolicited response" is a capability that could be reported by any type of widgets. Microsoft class driver only takes advantage of pin widget on this because it's not clear what other widget types (AOW, AIW) are going to use this response.
- While Microsoft spec. is not very clear about what its Default should be, Microsoft recommendation is to set it to disabled by Default. Class driver will enable it before using unsolicited response.

8 Widget Description

8.1 Node ID List

Table 5 – Node ID List

Node ID	Name	Input Connection List	Note
00	Root Node	N.A.	
01	AFG	N.A.	Audio Function Group
08	AOW0	N.A.	Analog Output Widget 0
09	AOW1	N.A.	Analog Output Widget 1
0A	AOW2	N.A.	Analog Output Widget 2
0B	AOW3	N.A.	Analog Output Widget 3
0C	AOW4	N.A.	Analog Output Widget 4
0D	VD0	N.A.	Vendor Widget 0
0E	DOW0	N.A.	Digital Output Widget 0 for S/PDIF TX0
0F	DOW1	N.A.	Digital Output Widget 1 for S/PDIF TX1
10	AIW0	1E	Analog Input Widget 0
11	AIW1	1F	Analog Input Widget 1
12	VD1	N.A.	Vendor Widget 1
13	DIW0	2F	Digital Input Widget 0 for S/PDIF RX0
14	VDMW0	08, 20	Vendor Digital Mixer Widget
15	VDMW1	09, 23	Vendor Digital Mixer Widget
16	VDMW2	0A, 30	Vendor Digital Mixer Widget
17	VDMW3	0B,31	Vendor Digital Mixer Widget
18	MW0	08, 21	Analog Mixer Widget 0 for PW0
19	MW1	09, 21	Analog Mixer Widget 0 for PW1
1A	MW2	0B, 21	Analog Mixer Widget 0 for PW3
1B	MW3	34, 21	Analog Mixer Widget 3 for PW4
1C	MW4	35, 21	Analog Mixer Widget 4 for PW5
1D	VDMW4	0C, 32	Vendor Digital Mixer Widget
1E	MUX6	2C, 2B, 2A, 29, 28, 21	ADC Input Select Widget 6 for AIW0
1F	MUX7	2C, 2B, 2A, 29, 28, 21	ADC Input Select Widget 7 for AIW1
20	VAOW0	N.A.	Vendor Secondary Analog Output Widget
21	MW9	2C, 2B, 2A, 29, 28, 08, 0B, 0C	Analog Mixer Widget 9
22	BGW	N.A.	Beep Generator Widget
23	VAOW1	N.A.	Vendor Secondary Analog Output Widget
24	PW0	18	Port D (Line out)
25	PW1	19	Port A (Surround)
26	PW2	0A	Port G (Center/LFE)
27	PW3	1A	Port H (Side Surround)
28	PW4	1B	Port E (Front Headphone)
29	PW5	1C	Port F (Front Microphone)
2A	PW6	09, 0C	Port C (Line in)
2B	PW7	0A, 0C	Port B (MIC)

Node ID	Name	Input Connection List	Note
2C	PW8	N.A.	Pin Widget 8 for CD Input
2D	PW9	0E	Pin Widget 9 for S/PDIF TX0
2E	PW10	0F	Pin Widget 10 for S/PDIF TX1
2F	PW11	N.A.	Pin Widget 11 for S/PDIF RX0
30	VAOW2	N.A.	Vendor Secondary Analog Output Widget
31	VAOW3	N.A.	Vendor Secondary Analog Output Widget
32	VAOW4	N.A.	Vendor Secondary Analog Output Widget
33	VCPW	N.A.	Vendor Content Protection Widget
34	MUX1	08, 0B, 0C	DAC Output Select Widget 1 for MW3
35	MUX2	08, 0B, 0C	DAC Output Select Widget 2 for MW4

8.2 Root Node (Node ID = 00)

8.2.1 Get Parameter Verb (Verb ID = F00h)

Offset

Get Vendor ID (Payload = 00h) Response: 1106 0441h

Bit	Attribute	Default	Description
31:16	R	1106h	Vendor ID
15:0	R	0441h	Device ID

Offset

Get Revision ID (Payload = 02h) Response: 0010 0000h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0001b	MajRev The major revision number (left of the decimal) of the HD Audio Spec to which the codec is fully compliant.
19:16	R	0	MinRev The minor revision number (right of the decimal) of the HD Audio Spec to which the codec is fully compliant.
15:8	R	0	Revision ID
7:0	R	0	Stepping ID

Offset

Get Subordinate Node Count (Payload = 04h) Response: 0001 0001h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:16	R	01h	Starting Node Number
15:8	R	0	Reserved
7:0	R	01h	Total Number of Nodes (Only 1 Audio Function Group in the Codec)

8.3 Audio Function Group (Node ID = 01)

8.3.1 Get Parameter Verb (Verb ID = F00h)

Offset

Get Subordinate Node Count (Payload = 04h) Response: 0008 002Eh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:16	R	08h	Starting Node Number.
15:8	R	0	Reserved
7:0	R	2Eh	Total Number of Nodes

Offset

Get Function Group Type (Payload = 05h) Response: 0000 0001h

Bit	Attribute	Default	Description
31:9	R	0	Reserved
8	R	0	Unsolicited Response (Not Supported)
7:0	R	01h	Audio Function Group

Offset

Get Function Group Capabilities (Payload = 08h) Response: 0001 0306h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	1b	Beep Gen
15:12	R	0	Reserved
11:8	R	3h	Input Delay
7:4	R	0	Reserved
3:0	R	6h	Output Delay

Offset

Get Supported Power States (Payload = 0Fh) Response: C000 000Fh

Bit	Attribute	Default	Description
31	R	1b	EPSS(Extend Power Status Supported)
30	R	1b	CLKSTOP
29	R	0	S3D3coldSup
28:5	R	0	Reserved
4	R	0	D3coldSup
3	R	0	D3Sup
2	R	0	D2Sup
1	R	0	D1Sup
0	R	0	D0Sup

Offset

Get GPIO Capabilities (Payload = 11h) Response: 4000 0001h

Bit	Attribute	Default	Description
31	R	0	GPIOWake= 0
30	R	1b	GPIOUnsol =1. GPIO Unsolicited Response Supported.
29:24	R	0	Reserved

23:16	R	0	NumGPIs= 00h. No GPI Pin Supported
15:8	R	0	NumGPOs= 00h. No GPO Pin Supported
7:0	R	01h	NumGPIOs =01h. One GPIO Pins Supported When Pin 2 is not configured as SPDIF_TX1 (F83h, bit4=0), the number of GPIO pins will be 2.

8.3.2 Subsystem ID Control Verb (Verb ID = F20h & 720h-723h)

	Description	Verb ID	Payload
Get	Get Subsystem ID	F20h	8'b0
Set1	Set Subsystem ID[7:0]	720h	Subsystem ID [7:0]
Set2	Set Subsystem ID[15:8]	721h	Subsystem ID [15:8]
Set3	Set Subsystem ID[23:16]	722h	Subsystem ID [23:16]
Set4	Set Subsystem ID[31:24]	723h	Subsystem ID [31:24]

Offset

Subsystem ID Register Response: 1106 0000h

Bit	Attribute	Default	Description
31:16	RW	1106h	Manufacturer ID
15:8	RW	00h	Board SKU
7:0	RW	00h	Assembly ID

Note:
All 32 bits in the Subsystem ID register are writeable, with the power-on default value of 1106 0000h. The system board BIOS can change the values during power up sequence to precisely describe the information about the motherboard so that the OS can load the correct driver.

8.3.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

The Whole Chip Power-down Control Register Response: - h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9	R	0	PS-ClkStopOk.
8	R	0	PS-Error (Not Supported)
7:4	R	0	PS-Act. Same as PS-Set for AFG.
3:0	RW	0	PS-Set

8.3.4 GPIO Unsolicited Response (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response	F08h	8'b0
Set	Set Unsolicited Response	708h	Enable unsolicited response

Offset

GPIO Unsolicited Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Unsolicited Response Control 0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine which node generated the unsolicited response.

8.3.5 GPIO Data (Verb ID = F15h & 715h)

	Description	Verb ID	Payload
Get	Get GPIO data Response	F15h	8'b0
Set	Set GPIO data	715h	GPIO Data [7:0]

Offset

Set GPIO Data Format Response: -h

Bit	Attribute	Default	Description
7:2	R	0	Reserved
1	W	-	GPIO1 Data, when GPIO1 Pin is Configured as GPO.
0	W	-	GPIO0 Data, when GPIO0 Pin is Configured as GPO.

Offset

Get GPIO Data Response Format Response: -h

Bit	Attribute	Default	Description
31:2	R	0	Reserved
1	R	-	GPIO1 Data
0	R	-	GPIO0 Data

8.3.6 GPIO Enable Mask (Verb ID = F16h & 716h)

	Description	Verb ID	Payload
Get	Get GPIO Enable Mask Response	F16h	8'b0
Set	Set GPIO Enable Mask	716h	GPIO Enable Mask [7:0]

Offset

Get/ Set GPIO Enable Mask Format Response: 0000 0000h

Bit	Attribute	Default	Description
31:2	R	0	Reserved
1	RW	0	0: GPIO1 pin is disabled and in Hi-Z state. 1: GPIO1 pin is enabled and the pin's behavior will be determined by the GPIO1 Direction control.
0	RW	0	0: GPIO0 pin is disabled and in Hi-Z state. 1: GPIO0 pin is enabled and the pin's behavior will be determined by the GPIO0 Direction control.

8.3.7 GPIO Direction (Verb ID = F17h & 717h)

	Description	Verb ID	Payload
Get	Get GPIO Direction Response	F17h	8'b0
Set	Set GPIO Direction	717h	GPIO Direction [7:0]

Offset

Get/Set GPIO Data Response Format Response: 0000 0000h

Bit	Attribute	Default	Description
31:2	R	0	Reserved
1	RW	0	GPIO1 Direction 0:Input 1:Output
0	RW	0	GPIO0 Direction 0: Input 1: Output

8.3.8 GPIO Unsolicited Response Enable Mask (Verb ID = F19h & 719h)

	Description	Verb ID	Payload
Get	Get GPIO Unsolicited Response Enable Mask Response	F19h	8'b0
Set	Set GPIO Unsolicited Response Enable Mask	719h	GPIO Unsolicited Response Enable Mask[7:0]

Offset

Get/ Set GPIO Unsolicited Response Enable Mask Format Response: 0000 0000h

Bit	Attribute	Default	Description
31:2	R	0	Reserved
1	RW	0	0: An unsolicited response will NOT be sent when a GPIO1 line changes state. 1: An unsolicited response will be sent when a GPIO1 line changes state.
0	RW	0	0: An unsolicited response will NOT be sent when a GPIO0 line changes state. 1: An unsolicited response will be sent when a GPIO0 line changes state.

8.3.9 Vendor Defined Verbs (Verb ID = F70h – F74h) - Reserved

8.3.10 Vendor Defined Verbs (Verb ID = F78h – F7Ch) - Reserved

8.3.11 Vendor Defined Verbs (Verb ID = F80h – F84h) - Reserved

8.3.12 Vendor Defined Verbs (Verb ID = F88h – F8Ch) – Reserved

8.3.13 Vendor Defined Verbs (Verb ID = F90h – F94h) - Reserved

8.3.14 Vendor Defined Verbs (Verb ID = F98h – F9Ch) - Reserved

8.3.15 Vendor Defined Verbs (Verb ID = FA0h – FA4h) - Reserved

8.3.16 Vendor Defined Verbs (Verb ID = FA8h – FACh) - Reserved

8.3.17 Vendor Defined Verbs (Verb ID = FB0h – FB4h) - Reserved

8.3.18 Vendor Defined Verbs (Verb ID = FB8h – FBCh) - Reserved

8.3.19 Function Reset Verb (Verb ID = 7FFh)

	Description	Verb ID	Payload
Set	Function Reset	7FFh	8'b0

8.4 Audio Analog Output Converter Widget AOW0 ~ AOW4 (Node ID = 08h, 09h, 0Ah, 0Bh, 0Ch)

8.4.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0000 041Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0	Audio Output Converter Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	0	Connection List is not Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	1b	Contain Format Information
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp Presented
1	R	0	In Amp not Present
0	R	1b	Stereo

Offset

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 05E0h

Bit	Attribute	Default	Description
31:21	R	0	Reserved
20	R	0	No 32-bit Audio Format Support
19	R	1b	24-bit Audio Format Support
18	R	1b	20-bit Audio Format Support
17	R	1b	16-bit Audio Format Support
16	R	0	8-bit Audio Format Support
15:12	R	0	Reserved
11	R	0	384 kHz not Supported
10	R	1b	192 kHz Supported
9	R	0	176.4 kHz Supported
8	R	1b	96 kHz Supported
7	R	1b	88.2 kHz Supported
6	R	1b	48 kHz Supported
5	R	1b	44.1 kHz Supported
4	R	0	32 kHz not Supported
3	R	0	22.05 kHz not Supported
2	R	0	16 kHz not Supported
1	R	0	11.025 kHz not Supported
0	R	0	8 kHz not Supported

Offset

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:3	R	0	Reserved
2	R	0	No AC3 Support
1	R	0	No Float32 Support
0	R	1b	PCM Supported

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

Offset

Output Amplifier Capabilities (Payload = 12h) Response: 0005 2A2Ah

Bit	Attribute	Default	Description
31	R	0	No Mute Capability
30:23	R	0	Reserved
22:16	R	0000101b	Step Size 0000101: Step size is 1.5 dB
15	R	0	Reserved
14:8	R	0101010b	Number of Steps 0101010: Number of steps is 43 (-63 dB ~ 0 dB).
7	R	0	Reserved
6:0	R	0101010b	Offset 0101010: Offset 2Ah is 0 dB.

8.4.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

DAC Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.4.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

Response: 0000 0000h

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit [7:4], and Channel in bit [3:0].

8.4.4 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Offset

Converter Format Response: 0000 0031h

Bit	Attribute	Default	Description
15	R	0	Stream Type 0: PCM 1: Non-PCM (not supported)
14	RW	0	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	0	Sample Base Rate Multiple 000: x1; 48 kHz, 44.1 kHz 001: x2; 96 kHz, 88.2 kHz 010: x3; 144 kHz (not supported) 011: x4; 192 kHz 100-111: Reserved
10:8	RW	0	Sample Base Rate Divisor 000: /1; 48 kHz Others: Not supported
7	R	0	Reserved
6:4	RW	011b	Bits per Sample 000: 8-bit (not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (not supported)
3:0	RW	0001b	Number of Channels (CHAN) Refers to the number of channels for the stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

8.4.5 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Offset

Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested (Ignored) 1: The output amplifier is being requested
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested 1: The left amplifier is being requested
12:4	W	-	Reserved
3:0	W	-	Index

Offset

Get Response Format Response: 0000 002Ah

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Amplifier is Un-muted.
6:0	R	0101010b	Amplifier Gain Setting 0101010b: Offset 2Ah is 0 dB.

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set (Ignored).
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	Un-mute
6:0	W	-	Gain Setting

8.5 Audio Digital Output Converter (S/PDIF TX) Widget DOW0, DOW1 (Node ID = 0Eh, 0Fh)

8.5.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0000 0611h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0000b	Audio Output Converter Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	1b	Digital Widget, not Analog
8	R	0	Connection List not Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	1b	Contains Format Information
3	R	0	Contains Amplifier Parameter
2	R	0	Out Amp Present
1	R	0	In Amp not Present
0	R	1b	Stereo

Offset

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 05E0h

Bit	Attribute	Default	Description
31:21	R	0	Reserved
20	R	0	No 32-bit Audio Format Support
19	R	1b	24-bit Audio Format Support
18	R	1b	20-bit Audio Format Support
17	R	1b	16-bit Audio Format Support
16	R	0	8-bit Audio Format Support
15:12	R	0	Reserved
11	R	0	384 kHz not Supported
10	R	1b	192 kHz Supported
9	R	0	176.4 kHz not Supported
8	R	1b	96 kHz Supported
7	R	1b	88.2 kHz Supported
6	R	1b	48 kHz Supported
5	R	1b	44.1 kHz Supported
4	R	0	32 kHz not Supported
3	R	0	22.05 kHz not Supported
2	R	0	16 kHz not Supported
1	R	0	11.025 kHz not Supported
0	R	0	8 kHz not Supported

Offset

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:3	R	0	Reserved
2	R	0	No AC3 Support
1	R	0	No Float32 Support
0	R	1b	PCM Supported

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.5.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

S/PDIF TX Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.5.3 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

Response: 0000 0000h

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit [7:4]. Channel is in bit [3:0].

8.5.4 S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh & 70Dh, 70Eh, 73Eh, 73Fh)

	Description	Verb ID	Payload
Get	Get Converter Control State	F0Dh	8'b0
Set	Set Converter Control 1	70Dh	SIC[7:0]
Set	Set Converter Control 2	70Eh	SIC[15:8]
Set	Set Converter Control 3	73Eh	SIC[23:16]
Set	Set Converter Control 3	73Fh	SIC[31:24]

Offset

S/PDIF IEC Control Bits Format Response: 0000 0000h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23	RW	0	Keep Alive Enable
22:15	R	0	Reserved
14:8	RW	0	CC[6:0] Category Code
7	RW	0	L: Generation Level
6	RW	0	PRO 0: Consumer mode 1: Professional mode
5	RW	0	AUDIO 0: Data is PCM format. 1: Data is non PCM format.
4	RW	0	Copy 0: Copyright is not asserted. 1: Copyright is asserted.
3	RW	0	Pre 0: Pre-emphasis is none. 1: Filter pre-emphasis is 50/15 μs.
2	RW	0	VCFG Determine S/PDIF transmitter behavior when data is not being transmitted.
1	RW	0	Validity Flag
0	RW	0	DigEn 0: S/PDIF TX disabled 1: S/PDIF TX enabled

Note:
When the "Keep Alive Enable" is set to 1, the output will supply a continuous clock, and a valid but "silent" data stream, even when no stream is selected by this Converter Widget, while the Digital Converter and/or Digital Pin Widget connected to this Converter Widget is in D0~D3. If D3cold state is supported, then the "Keep Alive" shall not be operational while in the D3code state.

8.5.5 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Offset

Converter Format Response: 0000 0031h

Bit	Attribute	Default	Description
15	R	0	Stream Type 0: PCM 1: Non-PCM
14	RW	0	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	0	Sample Base Rate Multiple 000: x1; 48 kHz, 44.1 kHz 001: x2; 96 kHz, 88.2 kHz 010: x3; 144 kHz (Not supported) 011: x4; 192 kHz, 176.4 kHz (176.4 kHz not supported) 100-111: Reserved
10:8	RW	0	Sample Base Rate Divisor 000: /1; 48 kHz Others : Not supported
7	R	0	Reserved
6:4	RW	011b	Bits per Sample 000: 8-bit (Not supported) 001: 16-bit 010: 20-bit (Not supported) 011: 24-bit 100: 32-bit (Not supported)
3:0	RW	1h	Number of Channels (CHAN) Refer to the number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

8.6 Audio Analog Input Converter Widget AIW0, AIW1 (Node ID = 10h, 11h)

8.6.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0010 051Bh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0001b	Audio Input Converter Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	1b	Contains Format Information
3	R	1b	Contains Amplifier Parameter
2	R	0	Out Amp is not Present.
1	R	1b	In Amp is Present.
0	R	1b	Stereo

Offset

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 0560h

Bit	Attribute	Default	Description
31:21	R	0	Reserved
20	R	0	No 32-bit Audio Format Support
19	R	1b	24-bit Audio Format Support
18	R	1b	20-bit Audio Format Support
17	R	1b	16-bit Audio Format Support
16	R	0	8-bit Audio Format Support
15:12	R	0	Reserved
11	R	0	384 kHz not Supported
10	R	1b	192 kHz Supported
9	R	0	176.4 kHz not Supported
8	R	1b	96 kHz Supported
7	R	0	88.2 kHz Supported
6	R	1b	48 kHz Supported
5	R	1b	44.1 kHz Supported
4	R	0	32 kHz not Supported
3	R	0	22.05 kHz not Supported
2	R	0	16 kHz not Supported
1	R	0	11.025 kHz not Supported
0	R	0	8 kHz not Supported

Offset

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:3	R	0	Reserved
2	R	0	No AC3 Support
1	R	0	No Float32 Support
0	R	1b	PCM Supported

Offset

Input Amplifier Capabilities (Payload = 0Dh) Response: 8005 1F0Bh

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0000101b	Step Size 0000101b: Step size is 1.5 dB.
15	R	0	Reserved
14:8	R	0011111b	Number of steps 0011111b: Number of steps is 32 (-16.5 dB ~ 30 dB).
7	R	0	Reserved
6:0	R	0001011b	Offset 0001011b: Offset 0Bh is 0 dB.

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	1 Input Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.6.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset Index n

Offset

Response: 0000 001Eh
or 0000 001Fh

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0	0011110b: From MUX6 (NID = 1Eh) for AIW0 0011111b: From MUX7 (NID = 1Fh) for AIW1

8.6.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

ADC Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the actual power state of the widget.
3:0	RW	0	PS-Set

8.6.4 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

Response: 0000 0000h

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit[7:4]. Channel is in bit[3:0].

8.6.5 Converter Format Verbs (Verb ID = Ah & 2h)

Response: 0000 0031h

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	Format

Offset

Converter Format Response: -h

Bit	Attribute	Default	Description
15	R	0	Stream Type 0: PCM 1: Non-PCM (Not supported)
14	RW	0	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	0	Sample Base Rate Multiple 000: x1; 48 kHz, 44.1 kHz 001: x2; 96 kHz 010: x3; 144 kHz (not supported) 011: x4; 192 kHz 100-111: Reserved
10:8	RW	0	Sample Base Rate Divisor 000: /1; 48 kHz Others: Not supported
7	R	0	Reserved
6:4	RW	011b	Bits per Sample 000: 8-bit (not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (not supported)
3:0	RW	0001b	Number of Channels (CHAN) Refers to the number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

8.6.6 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Offset

Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested. 1: The output amplifier is being requested (ignored).
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index Ignored

Offset

Get Response Format Response: 0000 008Bh

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	0001011b	Amplifier Gain Setting 0001011: 0 dB

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set (Ignored).
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

8.7 Audio Digital Input Converter (S/PDIF RX) Widget DIW0 (Node ID = 13h)

8.7.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0010 0711h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0001b	Audio Input Converter Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	1b	Digital Widget, not Analog
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	1b	Contains Format Information
3	R	0	Contains no Amplifier Parameter
2	R	0	Out Amp Not Present
1	R	0	In Amp Not Present
0	R	1b	Stereo

Offset

Supported PCM Size, Rates (Payload = 0Ah) Response: 000E 01F0h

Bit	Attribute	Default	Description
31:21	R	0	Reserved
20	R	0	No 32-bit Audio Format Support
19	R	1b	24-bit Audio Format Support
18	R	1b	20-bit Audio Format Support
17	R	1b	16-bit Audio Format Support
16	R	0	8-bit Audio Format Support
15:12	R	0	Reserved
11	R	0	384 kHz not Supported
10	R	0	192 kHz not Supported
9	R	0	176.4 kHz not Supported
8	R	1b	96 kHz Supported
7	R	1b	88.2 kHz Supported
6	R	1b	48 kHz Supported
5	R	1b	44.1 kHz Supported
4	R	1b	32 kHz Supported
3	R	0	22.05 kHz not Supported
2	R	0	16 kHz not Supported
1	R	0	11.025 kHz not Supported
0	R	0	8 kHz not Supported

Offset

Supported Stream Formats (Payload = 0Bh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:3	R	0	Reserved
2	R	0	NoAC3 Support
1	R	0	No Float32 Support
0	R	1b	PCM Supported

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Hard Wired Input

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.7.2 Get Connection List Entry Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 002Fh

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0101111b	From PW11 (NID = 2Fh)

8.7.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

S/PDIF RX Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.7.4 Converter Stream, Channel Verbs (Verb ID = F06h & 706h)

	Description	Verb ID	Payload
Get	Get Converter Stream / Channel	F06h	8'b0
Set	Set Converter Stream / Channel	706h	Stream is in bit [7:4]. Channel is in bit [3:0].

8.7.5 S/PDIF Converter Control 1 & 2 Verbs (Verb ID = F0Dh & 70Dh, 70Eh)

	Description	Verb ID	Payload
Get	Get Converter Control State	F0Dh	8'b0
Set	Set Converter Control State	70Dh	

Offset

S/PDIF IEC Control Bits Format Response: - h

Bit	Attribute	Default	Description
15	R	0	Reserved
14:8	R	-	CC[6:0] Category Code
7	R	-	L: Generation Level
6	R	-	PRO 0: Consumer mode 1: Professional mode
5	R	-	AUDIO 0: Data is PCM format. 1: Data is non PCM format.
4	R	-	Copy 0: Copyright is not asserted. 1: Copyright is asserted.
3	R	-	Pre 0: Pre-emphasis is none. 1: Filter pre-emphasis is 50/15 μs.
2	R	0	Reserved
1	R	-	Validity Flag

0	RW	-	DigEn 0: S/PDIF RX disabled 1: S/PDIF RX enabled

8.7.6 Converter Format Verbs (Verb ID = Ah & 2h)

	Description	Verb ID	Payload
Get	Get Converter Format	Ah	16'b0
Set	Set Converter Format	2h	

Offset

Converter Format Response: - h

Bit	Attribute	Default	Description
15	R	0	Stream Type 0: PCM 1: Non-PCM
14	RW	-	Sample Base Rate 0: 48 kHz 1: 44.1 kHz
13:11	RW	-	Sample Base Rate Multiple 000: x1; 48 kHz, 44.1 kHz 001: x2; 96 kHz, 88.2 kHz 010: x3; 144 kHz (not supported) 011: x4; 192 kHz, 176.4 kHz (not supported) 100-111: Reserved
10:8	RW	-	Sample Base Rate Divisor 000: /1; 48 kHz, 44.1 kHz 001: /2; 24 kHz, 22.05 kHz (not supported) 010: /3; 16 kHz (not supported), 32 kHz 011: /4; 11.025 kHz (not supported) 100: /5; 9.6 kHz (not supported) 101: /6; 8 kHz (not supported) 110: /7 (not supported) 111: /8; 6 kHz (not supported)
7	R	-	Reserved
6:4	RW	-	Bits per Sample 000: 8-bit (not supported) 001: 16-bit 010: 20-bit 011: 24-bit 100: 32-bit (not supported)
3:0	RW	-	Number of Channels (CHAN) Indicate the number of channels for this stream in each "sample block" of the "packets" in each "frame" on the link. 0000: 1 0001: 2 …… 1111: 16

8.8 Mixer Widget MW0, MW1, MW2, MW3, MW4 (Node ID = 18h, 19h, 1Ah, 1Bh, 1Ch)

8.8.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0020 050Bh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0010b	Audio Mixer Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	1b	Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	1b	In Amp Present
0	R	1b	Stereo

Offset

Input Amplifier Capabilities (Payload = 0Dh) Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Step Size 0000000: Step size is 0 dB.
22:16	R	0	Reserved
15	R	0	Number of Steps 0: Number of steps is 0.
14:8	R	0	Reserved
7	R	0	Offset
6:0	R	0	Step Size 0000000b: Step size is 0 dB.

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0002h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000010b	2 Inputs Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.8.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 2108h or 0000 2109h
or 0000 210B or 0000 2134h
or 0000 2135h

Bit	Attribute	Default	Description
31:16	R	0	Reserved
15:8	R	-	Connection List Entry n+1 21h: MW9
7:0	R	-	Connection List Entry n 08h: AOW0 for MW0 09h: AOW1 for MW1 0Bh: AOW3 for MW2 34h: MUX1 for MW3 35h: MUX2 for MW4

8.8.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Mixer Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.8.4 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Offset

Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested. 1: The output amplifier is being requested (ignored).
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

Offset

Get Response Format Response: 0000 0080h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	0	Reserved

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set (ignored).
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Reserved

8.9 Mixer Widget MW9 (Node ID = 21h)

8.9.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0020 050Bh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0010b	Audio Mixer Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	0	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	1b	Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	1b	In Amp Present
0	R	1b	Stereo

Offset

Input Amplifier Capabilities (Payload = 0Dh) Response: 8005 1F17h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0000101b	Step Size 0000101: Step size is 1.5 dB.
15	R	0	Reserved
14:8	R	0011111b	Number of Steps 0011111: Number of steps is 32 (-34.5dB – 12dB).
7	R	0	Reserved
6:0	R	0010111b	Offset 0010111: Offset 17h is 0 dB.

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0005h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000101b	5 Inputs Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.9.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 292A 2B2Ch (n=0)
or 0000 0028h (n=4)

Bit	Attribute	Default	Description	
			Offset index n = 0	**Offset index n = 4**
31:24	R	-	Connection List Entry n+3 29h: PW5, Port F	Connection List Entry n+3
23:16	R	-	Connection List Entry n+2 2Ah: PW6, Port C	Connection List Entry n+2
15:8	R	-	Connection List Entry n+1 2Bh: PW7, Port B	Connection List Entry n+1
7:0	R	-	Connection List Entry n 2Ch: PW8, CD	Connection List Entry n 28h: PW4, Port E

8.9.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Mixer Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.9.4 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Offset

Get Payload Format Response: - h

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested. 1: The output amplifier is being requested (ignored).
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	-	Reserved
3:0	W	-	Index

Offset

Get Response format Response: 0000 0097h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted. 1: Amplifier is muted.
6:0	R	0010111b	Amplifier Gain Setting 0010111b: Offset 17h is 0 dB.

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set (ignored).
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

8.10 Selector Widget MUX1, MUX2 (Node ID = 34h, 35h)

8.10.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0030 0501h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0011b	Audio Selector Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	0	Amplifier Parameter
2	R	0	Out Amp not Present
1	R	0	In Amp not Present
0	R	1b	Stereo

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0003h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000011b	3 Inputs Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.10.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0 Default: 0000 0000h(AOW0)
Set	Set Connection Select	701h	The connection index value to be set

8.10.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 000C 0B08h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:16	R	0Ch	Connection List Entry n+2 0Ch: AOW4
15:8	R	0Bh	Connection List Entry n+1 0Bh: AOW3
7:0	R	08h	Connection List Entry n 08h: AOW0

8.10.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.11 Selector Widget MUX6, MUX7 (Node ID = 1Eh, 1Fh)

8.11.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0030 0501h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0011b	Audio Selector Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present
7	R	0	Does not Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	0	Amplifier Parameter
2	R	0	Out Amp not presented
1	R	0	In Amp not Present
0	R	1b	Stereo

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0006h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000110b	6 Inputs Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.11.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8’b0 Default: 0000 0001h (MIC)
Set	Set Connection Select	701h	The connection index value to be set.

8.11.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 292A 2B2Ch (n=0)
or 0000 2128h (n=4)

Bit	Attribute	Default	Description	
			Offset index n = 0	**Offset index n = 4**
31:24	R	29h or 00h	Connection List Entry n+3 29h: PW5, Port F	Connection List Entry n+3 00h
23:16	R	2Ah or 00h	Connection List Entry n+2 2Ah: PW6, Port C	Connection List Entry n+2 00h
15:8	R	2Bh or 21h	Connection List Entry n+1 2Bh: PW7, Port B	Connection List Entry n+1 21h: MW9
7:0	R	2Ch or 28h	Connection List Entry n 2Ch: PW8, CD	Connection List Entry n 28h: PW4, Port E

8.11.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.12 Pin Widget PW0, PW1(Node ID = 24h, 25h)

8.12.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp not Present
1	R	0	In Amp not Present
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0001 001Ch or 0000 001Ch

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	-	EAPD Capable. Read as 1 for PW0 EAPD Capable. Read as 0 for PW1
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	1b	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

Offset

Output Amplifier Capabilities (Payload = 12h) Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset

8.12.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 0018h
or 0000 0019h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	-	0011000b: From MW0 for PW0 0011001b: From MW1 for PW1

8.12.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

PW0, PW1 Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset

9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.12.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Headphone Enable 0: Disabled(default) 1: Headphone enabled
6	RW	0	Output Enable 0: Disabled(default) 1: Output enabled
5	RW	0	Input Enable (Not Supported)
4:0	R	0	Reserved

8.12.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Offset

Unsolicited Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine the node that generated the unsolicited response.

8.12.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

Offset

PinCntl Format Response: - h

Bit	Attribute	Default	Description
7:1	R	-	Reserved
0	R	-	Right Channel Sense (Not Supported)

Offset

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	0	Reserved

8.12.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Config Bits Format

Response: 0101 4010h
or 0101 1012h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity 0: Connected to a jack
29:24	RW	000001b	Location
23:20	RW	0	Default Device 0: Line-out
19:16	RW	0001b	Connection Type
15:12	RW	-	Color 0100b: for PW0 0001b: for PW1
11:8	RW	0	Misc
7:4	RW	0001b	Default Association
3:0	RW	-	Sequence 0000b: Line out in association # 1 for PW0 0010b: Surround out in association # 1 for PW1

8.12.8 EAPD Enable Verbs (Verb ID = F0Ch & 70Ch) (only for PW0)

Response: 0000 0000h

	Description	Verb ID	Payload
Get	EAPD Control	F0Ch	8'b0
Set		70Ch	Bit 1 is EAPD. 0: EAPD output 0 1: EAPD output 1

8.12.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Offset

Get Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	0	0: The input amplifier is being requested. 1: The output amplifier is being requested.
14	W	0	Reserved
13	W	0	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	0	Reserved
3:0	W	0	Index

Offset

Get Response Format Response: 0000 0080h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted. 1: Amplifier is muted (output default).
6:0	R	0	Amplifier Gain Setting

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

8.13 Pin Widget PW2, PW3 (Node ID = 26h, 27h)

8.13.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp not Presented
1	R	0	In Amp not Presented
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0000 0014h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R‘	1b	D0Sup

Offset

Output Amplifier Capabilities (Payload = 12h) Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset

8.13.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 000Ah (for PW2)
0000 001Ah (for PW3)

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	-	0001010b: From AOW2 for PW2 0011010b: From MW2 for PW3

8.13.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.13.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable (Not Supported)
6	RW	0	Output Enable 0: Disabled 1: Output enabled
5	RW	0	Input Enable (Not Supported)
4:0	R	0	Reserved

8.13.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Offset

Unsolicited Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	0	Reserved
5:0	RW	0	Tag Used by software to determine the node that generated the unsolicited response.

8.13.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

Offset

PinCntl Format Response: - h

Bit	Attribute	Default	Description
7:1	R	-	Reserved
0	R	-	Right Channel Sense (Not Supported)

Offset

Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	0	Reserved

8.13.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Response: 0101 6011h for PW2,
0101 2014h for PW3

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000001b	Location
23:20	RW	0	Default Device
19:16	RW	0001b	Connection Type
15:12	RW	-	Color 0110b: for PW2 0010b: for PW3
11:8	RW	0	Misc.
7:4	RW	0001b	Default Association
3:0	RW	-	Sequence 0001b: for PW2 0100b: for PW3

8.13.8 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	-
Set	Set Amplifier Gain/Mute	3h	-

Offset

Get Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	0	0: The input amplifier is being requested. 1: The output amplifier is being requested.
14	W	0	Reserved
13	W	0	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	0	Reserved
3:0	W	0	Index

Offset

Get Response Format Response: 0000 0080h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	1b	0: Amplifier is un-muted 1: Amplifier is muted (output default).
6:0	R	0	Amplifier Gain Setting

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

8.14 Pin Widget PW4, PW5 (Node ID =28h, 29h)

8.14.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp Present
1	R	0	In Amp Present
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0000 233Ch

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	23h	VRef Control (100% & 50% & Hi-Z)
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	1b	Output Capable
3	R	1b	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	1 Input Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R‘	1b	D0Sup

Offset

Input Amplifier Capabilities (Payload = 0Dh) Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset 0: Offset 00h is 0 dB.

Offset

Output Amplifier Capabilities (Payload = 12h) Response: 8000 0000h

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset

8.14.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 001Bh
or 0000 001Ch

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	-	0011011b: From MW4 for PW4 0011100b: From MW3 for PW5

8.14.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.14.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	RW	0	Headphone Enable 0: Disabled (default) 1: Headphone enabled
6	RW	0	Output Enable 0: Disabled (default) 1: Output enabled
5	RW	0	Input Enable 0: Disabled (default) 1: Input enabled
4:3	R	0	Reserved
2:0	RW	0	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z (default) 001: 50% (half of AVdd) 010: 0V (not supported) 101: AVdd Others: Reserved

8.14.5 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Offset

Unsolicited Format Response: - h

Bit	Attribute	Default	Description
7	RW	-	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	-	Reserved
5:0	RW	-	Tag Used by software to determine the node that generated the unsolicited response.

8.14.6 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

Offset

PinCntl Format Response: - h

Bit	Attribute	Default	Description
7:1	R	-	Reserved
0	R	-	Right Channel Sense (Not Supported)

Offset

Response Response: - h

Bit	Attribute	Default	Description
31	R	-	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	-	Reserved

8.14.7 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Config Bits Format Response: 0221 40F0h or 02A1 9027h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000010b	Location

23:20	RW	-	Default Device 0010b: For PW4	1010b: For PW5
19:16	RW	0001b	Connection Type	
15:12	RW	-	Color 0100b: For PW4	1001b: For PW5
11:8	RW	0	Misc	
7:4	RW	-	Default Association 1111b: For PW4	0010b: For PW5
3:0	RW	-	Sequence 0000b: For PW4	0111b: For PW5

8.14.8 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	-
Set	Set Amplifier Gain/Mute	3h	-

Offset

Get Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	0	0: The input amplifier is being requested. 1: The output amplifier is being requested.
14	W	0	Reserved
13	W	0	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	0	Reserved
3:0	W	0	Index

Offset

Get Response Format Response: - h

Bit	Attribute	Default	Description
31:8	R	-	Reserved
7	R	-	0: Amplifier is un-muted (input default). 1: Amplifier is muted (output default).
6:0	R	-	Amplifier Gain Setting

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

8.15 Pin Widget PW6, PW7 (Node ID = 2Ah, 2Bh)

8.15.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 058Dh

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	1b	Connection List is Present.
7	R	1b	Support Unsolicited Response
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp not Presented
1	R	0	In Amp Presented
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0000 2334h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	23h	VRef Control (100% & 50% & Hi-Z)
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	1b	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Offset

Input Amplifier Capabilities (Payload = 0Dh) Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset 0: Offset 00h

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0002h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000002b	Only 2 Inputs Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

Offset

Output Amplifier Capabilities (Payload = 12h) Response: 0000 0000h

Bit	Attribute	Default	Description
31	R	0	Mute Capable
30:23	R	0	Reserved
22:16	R	0	Step Size 0: Step size is 0 dB.
15	R	0	Reserved
14:8	R	0	Number of Steps 0: Number of steps is 0h.
7	R	0	Reserved
6:0	R	0	Offset

8.15.2 Connection Select Control Verbs (Verb ID = F01h & 701h)

	Description	Verb ID	Payload
Get	Get Connection Select	F01h	8'b0
Set	Set Connection Select	701h	The connection index value to be set. For PW6 8'b0: from AOW1 8'b1: from AOW4 For PW7 8'b0: from AOW2 8'b1: from AOW4

Offset

Get Response Format Response: - h

Bit	Attribute	Default	Description
31:8	R	-	Reserved
7:0	R	-	Connection Index Currently Set For PW6 8'b0: Connection from AOW1 8'b1: Connection form AOW4 For PW7 8'b0: Connection from AOW2 8'b1: Connection form AOW4

8.15.3 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 0C09h (for PW6)
0000 0C0Ah (for PW7)

Bit	Attribute	Default	Description
31:16	R	0	Reserved
15:8	R	0001100b	From AOW4 for PW6, PW7
7	R	0	Independent NID
6:0	R	-	0100110b: From AOW1 for PW6 0011000b: From AOW2 for PW7

8.15.4 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.15.5 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	RW	0	Output Enable (for Smart 5.1 Configuration) 0: Disabled 1: Output enabled
5	RW	0	Input Enable 0: Disabled 1: Input enabled
4:3	R	0	Reserved
2:0	RW	0	VRef Enable These bits control the VRef signal associated with the pin widget. 000: Hi-Z 001: 50% (half of AVdd) 010: 0V (not supported) 101: AVdd Others: Reserved

8.15.6 Unsolicited Response Control (Verb ID = F08h & 708h)

	Description	Verb ID	Payload
Get	Get Unsolicited Response Control	F08h	8'b0
Set	Set Unsolicited Response Control	708h	Enable unsolicited response

Offset

Unsolicited Format Response: - h

Bit	Attribute	Default	Description
7	RW	-	0: Unsolicited Response Disabled 1: Unsolicited Response Enabled
6	R	-	Reserved
5:0	RW	-	Tag Used by software to determine which node generated the unsolicited response.

8.15.7 Pin Sense Control Verbs (Verb ID = F09h & 709h)

	Description	Verb ID	Payload
Get	Get Pin Sense Control	F09h	8'b0
Set	Set Pin Sense Control	709h	PinCntl

Offset

PinCntl Format Response: - h

Bit	Attribute	Default	Description
7:1	R	-	Reserved
0	R	-	Right Channel Sense (Not Supported)

Offset

Response: - h

Bit	Attribute	Default	Description
31	R	-	Presence Detect 0: Nothing plugged in 1: Jack plugged in
30:0	R	-	Reserved

8.15.8 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Config Bits Format Response: 0181 302Eh for PW6
01A1 9026h for PW7

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	-	Location 000001: For PW6 000001: For PW7

23:20	RW	-	Default Device 1000: For PW6	1010: For PW7
19:16	RW	0001b	Connection Type	
15:12	RW	-	Color 0011: For PW6	1001: For PW7
11:8	RW	0	Misc	
7:4	RW	-	Default Association 0010: For PW6	0010: For PW7
3:0	RW	-	Sequence 1110: For PW6	0110: For PW7

8.15.9 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	
Set	Set Amplifier Gain/Mute	3h	

Offset

Get Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	0	0: The input amplifier is being requested. 1: The output amplifier is being requested (Ignored).
14	W	0	Reserved
13	W	0	0: The right amplifier is being requested. 1: The left amplifier is being requested.
12:4	W	0	Reserved
3:0	W	0	Index

Offset

Get Response Format Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	0: Amplifier is un-muted (input default). 1: Amplifier is muted.
6:0	R	0	Amplifier Gain Setting

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set (ignored).
14	W	-	The Input Amplifier is being Set.
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

8.16 Pin Widget PW8 (Node ID = 2Ch) CD Analog Input

8.16.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 0401h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	0	Connection List is not Presented.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Doe not Contain Format Information.
3	R	0	Does not Contain Amplifier Parameter.
2	R	0	Out Amp not Presented
1	R	0	In Amp not Presented
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0000 0020h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	0	Output Capable
3	R	0	Headphone Drive Capable.
2	R	0	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R`	1b	D0Sup

8.16.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

For PW8 Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.16.3 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	R	0	Output Enable 0: Disabled
5	RW	0	Input Enable 0: Disabled 1: Input enabled
4:3	R	0	Reserved
2:0	R	0	VRef Enable

8.16.4 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Config Bits Format Response: 5933 11F8h

Bit	Attribute	Default	Description
31:30	RW	01b	Port Connectivity
29:24	RW	011001b	Location 011001: Internal
23:20	RW	0011b	Default Device 0011: CD
19:16	RW	0011b	Connection Type
15:12	RW	0001b	Color
11:8	RW	0001b	Misc.
7:4	RW	1111b	Default Association
3:0	RW	1000b	Sequence

8.17 Pin Widget PW9 (Node ID = 2Dh) S/PDIF TX Pin

8.17.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 0701h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	1b	Digital Widget
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information.
3	R	0	Does not Contain Amplifier Parameter.
2	R	0	Out Amp not Presented
1	R	0	In Amp not Presented
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0000 0010h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	HDMI
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	0	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Note:
HDMI capability report is depended on TX0_HDMI_SEL and TX0_HDMI_EN, and its pin configuration value.

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.17.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 000Eh

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0001110b	From DOW0, NID = 0Eh

8.17.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

PW9 Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.17.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	RW	0	Output Enable 0: Disabled 1: Output enabled
5	R	0	Input Enable 0: Disabled
4:3	R	0	Reserved
2:0	R	0	VRef Enable

8.17.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Config Bits Format Response: 0744 11F0h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000111b	Location
23:20	RW	0100b	Default Device 0100: SPDIF Out
19:16	RW	0100b	Connection Type
15:12	RW	0001b	Color
11:8	RW	0001b	Misc.
7:4	RW	1111b	Default Association
3:0	RW	0	Sequence

8.18 Pin Widget PW10 (Node ID = 2Eh) HDMI Audio Output Pin

8.18.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 0701h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	1b	Digital Widget
8	R	1b	Connection List is Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information.
3	R	0	Does not Contain Amplifier Parameter.
2	R	0	Out Amp not Presented
1	R	0	In Amp not Presented
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0000 0010h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	HDMI
6	R	0	Balanced I/O Pins
5	R	0	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	0	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Note:
HDMI capability report is depended on TX1_HDMI_SEL and TX1_HDMI_EN, and its pin configuration value.

Offset

Connection List Length (Payload = 0Eh) Response: 0000 0001h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Short Form
6:0	R	0000001b	Only 1 Input Available

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R‘	1b	D0Sup

8.18.2 Connection List Entry Control Verbs (Verb ID = F02h)

	Description	Verb ID	Payload
Get	Get Connection List Entry	F02h	Offset index n

Offset

Response: 0000 000Fh

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	Independent NID
6:0	R	0001111b	From DOW1, NID = 0Fh

8.18.3 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8’b0
Set	Set Converter Power State	705h	PS-Set 8’h00: Power State is D0. 8’h01: Power State is D1. 8’h02: Power State is D2. 8’h03: Power State is D3.

Offset

PW10 Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.18.4 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	RW	0	Output Enable 0: Disabled 1: Output enabled
5	R	0	Input Enable 0: Disabled
4:3	R	0	Reserved
2:0	R	0	VRef Enable

8.18.5 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Config Bits Format Response: 9856 01F0h

Bit	Attribute	Default	Description
31:30	RW	10b	Port Connectivity
29:24	RW	011000b	Location
23:20	RW	0101b	Default Device 0101: SPDIF Out
19:16	RW	0110b	Connection Type
15:12	RW	0	Color
11:8	RW	0001b	Misc.
7:4	RW	1111b	Default Association
3:0	RW	0	Sequence

8.19 Pin Widget PW11 (Node ID = 2Fh) S/PDIF RX / EAPD Pin

8.19.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0040 0601h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0100b	Pin Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	1b	Power Control Supported
9	R	1b	Digital Widget
8	R	0	Connection List is not Presented.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	Does not Contain Format Information.
3	R	0	Does not Contain Amplifier Parameter.
2	R	0	Out Amp not Presented
1	R	0	In Amp not Presented
0	R	1b	Stereo

Offset

Pin Capabilities (Payload = 0Ch) Response: 0000 0030h

Bit	Attribute	Default	Description
31:17	R	0	Reserved
16	R	0	EAPD Capable
15:8	R	0	VRef Control
7	R	0	Reserved
6	R	0	Balanced I/O Pins
5	R	1b	Input Capable
4	R	1b	Output Capable
3	R	0	Headphone Drive Capable
2	R	0	Presence Detect Capable
1	R	0	Trigger Required
0	R	0	Impedance Sense Capable

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

8.19.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

PW11 Power-down Control Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.19.3 Pin Widget Control Verbs (Verb ID = F07h & 707h)

	Description	Verb ID	Payload
Get	Get Pin Widget Control	F07h	8'b0
Set	Set Pin Widget Control	707h	PinCntl

Offset

PinCntl Format Response: 0000 0000h

Bit	Attribute	Default	Description
7	R	0	Headphone Enable 0: Disabled
6	RW	0	Output Enable 0: Disabled 1: Output enabled
5	RW	0	Input Enable 0: Disabled 1: Input enabled
4:3	R	0	Reserved
2:0	R	0	VRef Enable

8.19.4 Pin Widget Configuration Default Verbs (Verb ID = F1Ch & 71Ch-71Fh)

	Description	Verb ID	Payload
Get	Get Pin Widget Configuration Default	F1Ch	8'b0
Set	Set Pin Widget Configuration Default	71Ch	Config bits [7:0]
Set	Set Pin Widget Configuration Default	71Dh	Config bits [15:8]
Set	Set Pin Widget Configuration Default	71Eh	Config bits [23:16]
Set	Set Pin Widget Configuration Default	71Fh	Config bits [31:24]

Offset

Config Bits Format Response: 07C4 21F0h

Bit	Attribute	Default	Description
31:30	RW	0	Port Connectivity
29:24	RW	000111b	Location
23:20	RW	1100b	Default Device 1100: SPDIF In
19:16	RW	0100b	Connection Type
15:12	RW	0010b	Color
11:8	RW	0001b	Misc
7:4	RW	1111b	Default Association
3:0	RW	0	Sequence

8.20 Beep Generator Widget (Node ID = 22h)

8.20.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 0070 040Ch

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	0111b	Beep Generator Widget
19:11	R	0	Reserved
10	R	1b	Power Control Supported
9:4	R	0	Reserved
3	R	1b	Contain Amplifier Parameter
2	R	1b	Out Amp Present
1:0	R	0	Reserved

Offset

Supported Power States (Payload = 0Fh) Response: 0000 000Fh

Bit	Attribute	Default	Description
31:4	R	0	Reserved
3	R	1b	D3Sup
2	R	1b	D2Sup
1	R	1b	D1Sup
0	R	1b	D0Sup

Offset

Output Amplifier Capabilities (Payload = 12h) Response: 8005 120Ah

Bit	Attribute	Default	Description
31	R	1b	Mute Capable
30:23	R	0	Reserved
22:16	R	0000101b	Step Size. 0000101b: Step size is 1.5 dB.
15	R	0	Reserved
14:8	R	0010010b	Number of Steps 0010010b: Number of steps is 19 (-15 dB ~ +12 dB).
7	R	0	Reserved
6:0	R	0001010b	Offset 0001010b: Offset 0Ah is 0 dB.

8.20.2 Power State Verbs (Verb ID = F05h & 705h)

	Description	Verb ID	Payload
Get	Get Converter Power State	F05h	8'b0
Set	Set Converter Power State	705h	PS-Set 8'h00: Power State is D0. 8'h01: Power State is D1. 8'h02: Power State is D2. 8'h03: Power State is D3.

Offset

Response: 0000 0400h

Bit	Attribute	Default	Description
31:11	R	0	Reserved
10	R	1b	PS-SettingsReset
9:8	R	0	Reserved
7:4	R	0	PS-Act. Reports the Actual Power State of the Widget.
3:0	RW	0	PS-Set

8.20.3 Beep Generation Verbs (Verb ID = F0Ah & 70Ah)

	Description	Verb ID	Payload
Get	Get divider	F0Ah	8'b0
Set	Set divider	70Ah	Bits [7:0] are Divider.

Offset

Response Format Response: 0000 0000h

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7:0	RW	0	Divider 00h: Disable internal PC Beep generation. Non-zero value enables the Beep, and the codec generates the beep tone. Frequency of beep tone is [48k / (Divider*4)].

8.20.4 Amplifier Gain/Mute Verbs (Verb ID = Bh & 3h)

	Description	Verb ID	Payload
Get	Get Amplifier Gain/Mute	Bh	Format
Set	Set Amplifier Gain/Mute	3h	Format

Offset

Get Payload Format

Bit	Attribute	Default	Description
15	W	-	0: The input amplifier is being requested (ignored). 1: The output amplifier is being requested.
14	W	-	Reserved
13	W	-	0: The right amplifier is being requested (ignored). 1: The left amplifier is being requested
12:4	W	-	Reserved
3:0	W	-	Index (Ignored)

Offset

Get Response Format Response: 0000 000Ah

Bit	Attribute	Default	Description
31:8	R	0	Reserved
7	R	0	0: Amplifier is un-muted 1: Amplifier is muted.
6:0	R	0001010b	Amplifier Gain Setting 0001010b: Offset 0Ah is 0 dB.

Offset

Set Payload Format Response: 0000 0000h

Bit	Attribute	Default	Description
15	W	-	The Output Amplifier is being Set.
14	W	-	The Input Amplifier is being Set (Ignored).
13	W	-	The Left Amplifier is being Set.
12	W	-	The Right Amplifier is being Set.
11:8	W	-	Index Ignored
7	W	-	0: Un-mute 1: Mute
6:0	W	-	Gain Setting

8.21 Vendor Widget VD0 ~ VD1 (Node ID = 0Dh, 12h)

8.21.1 Get Parameter Verb (Verb ID = F00h)

Offset

Audio Widget Capabilities (Payload = 09h) Response: 00F0 0000h

Bit	Attribute	Default	Description
31:24	R	0	Reserved
23:20	R	1111b	Vendor Widget
19:16	R	0	Delay
15:12	R	0	Reserved
11	R	0	No L-R Swap
10	R	0	Power Control Supported
9	R	0	Analog Widget, not Digital
8	R	0	Connection List is Present.
7	R	0	Does not Support Unsolicited Response.
6	R	0	No Processing Control
5	R	0	Reserved
4	R	0	No Format Information
3	R	0	Amplifier Parameter
2	R	0	Out Amp not Presented
1	R	0	In Amp Present
0	R	0	Stereo

8.22 Vendor Widget for Content Protection (Node ID = 33h) - Reserved

8.23 Vendor Secondary Audio Analog Output Converter Widget VAOW0 ~ VAOW4 (Node ID = 22h, 23h, 30h, 31h, 32h) – Reserved

8.24 Vendor Digital Mixer Widget VDMW0~VDMW4 (Node ID = 15h, 16h, 17h, 1Dh, 20h) - Reserved

9 Functional Descriptions

9.1 Clock Control

One of the major differences between High Definition Audio Spec and AC97 is the clock source. The HD Audio controller provides a 24 MHz clock (BITCLK). An internal PLL (PLL1) in the codec uses BITCLK (24 MHz) as the reference clock and generates 49.152 MHz clocks for internal use. A second PLL (PLL2) also takes the 24 MHz BITCLK and generates 22.5792 MHz clock for 44.1 kHz based rates. The PLLs can be powered down by the Power Widget for power management. **Both PLL output clocks can be routed to pin 48 by a vendor defined verb for testing**.

The interface signals between digital block and the 2 PLLs are listed below.

PLL1 (49.152 MHz)		
Pin Name	**Direction (From PLL)**	**Pin Description**
REFCLK	I	Connect to a 24-MHz clock input.
CLK49152	O	49.152-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

22.5792 MHz		
Pin Name	**Direction (From PLL)**	**Pin Description**
REFCLK	I	Connect to a 24-MHz clock input.
CLK225792	O	22.5792-MHz clock output.
RST	I	When RST is high, the PLL enters a low power mode and all internal states are reset.
PWRPD	I	When PWRPD is high, the PLL enters a power-down mode.
VDD	IO	Digital power supply for PFD and Dividers. Nominally 3.3V.
GND	IO	Ground for PFD and Dividers.
VCOPWR	IO	Analog power supply for VCO. Nominally 3.3V.
VCOGND	IO	Ground for VCO.
CHGPPWR	IO	Analog power supply for Bias and Charge Pump. Nominally 3.3V.
CHGPGND	IO	Ground for Bias and Charge Pump.

9.2 Interpolation / Decimation

To take advantage the high bandwidth provided by the new audio interface, the hardware only supports native 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz sample rates, and the driver is responsible for converting the data to / from 192 kHz. This way the large area previously required for implementing the digital interpolation / decimation filters can be saved.

9.3 HPF for ADC DC Removal

The built-in high-pass filter for each ADC can remove the DC component in the ADC data.

9.4 Audio Jack Detection Circuits

Based on the jack detection circuit defined in the High Definition Audio Specification, the figure below summarizes the equivalent resistance values to the SENSE Pin in different scenario.

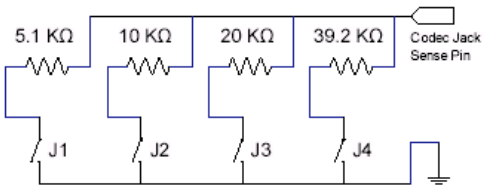


Figure 19 – Jack Detect Circuit

9.5 Internal Loop-back and Peak Detection for Low Cost Production Test

Internal loop-back paths can be used to test all DACs and ADCs functions. The output of each DAC can be routed back to the input of the ADC. The ADC output data is analyzed by a specially designed block to detect the zero-crossing point and the peak values. These information can be read back to decide whether the digital & analog functions are normal. Refer to the descriptions in the Vendor-Defined Verbs in the Audio Function Group.

9.6 GPIO Implementation

9.6.1 GPIO Pinout

- Pin 47: SPDIF_RX0 / EAPD
- Pin 48: SPDIF_TX0
- Pin 2: GPIO0 / **SPDIF_TX1**
- Pin 3: GPIO1

Note:
The pinout description with bold type is defined by vendor specific command; otherwise it claims default function.

9.6.2 GPIO Usage

- GPI:
  - Front Panel Sense
  - Others
- GPO:
  - EAPD-like Control
  - Others

	NB 1	**NB 2**	**NB 3**	**Desk-top 1**	**Desk-top 2**	**I/O**
GPO for EAPD0 (Line Out)	√	√	√	-	-	-
GPO for EAPD1 (Head Phone)	√	√	√	-	-	-
SPDIF_TX0	√	√	√	√	√	-
SPDIF_TX1	-	-	-	√	√	-
GPI (Front Panel Sense)	√	√	-	√	-	-
Pin 47: EAPD	GPO	GPO	GPO	-	-	O
Pin 48: SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	SPDIF_TX0	O
Pin 2: GPIO0/SPDIF_TX1	GPO	GPO	GPO	SPDIF_TX1	SPDIF_TX1	I/O
Pin 3: GPIO1	GPI	GPI	-	GPI	-	I/O

9.7 Digital Pin Reuse

Pin #	Pin Name	Type	Description
2	GPIO0	I/O	General Purpose Input 0/Output 0
	SPDIF_TX1	O	2nd S/PDIF Output
3	GPIO1	I/O	General Purpose Input 1/Output 1
5	SDO	I	Serial Data Input From Controller
8	SDI	I/O	Serial Data Output to Controller
10	SYNC	I	Sample SYNC From Controller
47	EAPD	O	External Amplifier Power-down
	SPDIF_RX0	I	1st S/PDIF_RX
48	S/PDIF_TX0	O	1st S/PDIF Output

9.8 SPDIF/TX Output Pin Behavior

AFG Power State	RESETN	Output Enable	Converter Dig Enable	Stream ID	Keep Alive Enable	Pin Behavior
D0~D3	Low	-	-	-	-	Hi-Z (Internal Pull-down Enabled.) 3'b111
D0	High	Disabled	-	-	-	Hi-Z (Internal Pull-down Enabled.) 3'b111
		Enabled	Disabled	---	---	Active – Pin drives 0. (Internal Pull-down N.A.) 3'b010
			Enabled	0	---	Active – Pin drives SPDIF format, but data is zero. (Internal Pull-down N.A.) 3'b010
				1~15	---	Active – Pin drives SPDIF data. (Internal Pull-down N.A.) 3'b010
D1~D3	High	Disabled	---	---	---	Hi-Z (Internal Pull-down Enabled.) 3'b111
		Enabled	---	---	0	Active – Pin drives 0. (Internal pull-down N.A.) 3'b010
			Enabled	---	1	Active – Pin drives SPDIF format, but data is zero. (Internal Pull-down N.A.) 3'b010
D3cold	---	---	---	---	---	Hi-Z (Internal Pull-down Enabled) 3'b111

Note:

1. The Stream ID of SPDIF_TX will be reset, and SPDIF_TX will send 0 when the Digital Output Converter and corresponding Pin Widget are put in D1~D3 state. But if the stream ID is set again, and Keep Alive is enabled, SPDIF_TX will continue to send data.
2. 3'bxxx = {SPTX1_OEN_N, SPTX1_PU_N, SPTX1_PD}

10 Electrical Specification

10.1 DC Characteristics

Absolute Maximum Rating

Symbol	Parameter	Min.	Max.	Unit	Note
T_S	Storage Temperature	-55	125	°C	—
T_A	Ambient Operating Temperature	0	85	°C	—
V_{ESD}	Electrostatic Discharge (human body model)	—	2	kV	—

Note:
Stress above conditions may cause permanent damage to the device. Functional operation of this device should be restricted to the conditions described.

Recommended Operating Conditions

Symbol	Parameter	Min.	Max.	Unit	Note
AVDD	Analog Power Supplies (preferred)	–	5	–	V
AVDD	Analog Power Supplies (for low-power apps)	–	3.3	–	V

DC Performance Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
DVdd	Digital Power Supply	3.135	3.3	3.465	V
V_{IN}	Input Voltage Range	-0.3		DVdd + 0.3	V
V_{IL}	Low Level Input Voltage			0.35 x DVdd	V
V_{IH}	High Level Input Voltage	0.65 x DVdd			V
V_{OH}	High Level Output Voltage	0.9 x DVdd			V
V_{OL}	Low Level Output Voltage			0.1 x DVdd	V
	Input Leakage Current (AC-Link inputs)	-10		10	μA
	Output Leakage Current (Hi-Z'd AC-Link outputs)	-10		10	μA
	Input / Output Pin Capacitance			7.5	pF

10.2 Analog Performance Characteristics

Parameter	Min.	Typ.	Max.	Unit
Analog Input				
Full Scale Input Voltage Line Inputs Mic Inputs with 20 dB Gain Mic inputs with 0 dB Gain		 1.0 0.1 1		 Vrms
Input Impedance	10			kΩ
Input Capacitance		7.5		pF
Power Supply Rejection Ratio (10 kHz)		-91.9		dB
Power Supply Rejection Ratio (1 kHz)		-77.5		dB
Power Supply Rejection Ratio (100 Hz)		-57.5		dB
Analog Output				
Full Scale Output Voltage Line Output Headphone Output		 1.0	 1.41	 Vrms
Analog S/N Other to LINE_OUT		 100		 dB
Analog Frequency Response	20		20,000	Hz
Vrefout		2.25-2.75		V
Power Supply Rejection Ratio (10 kHz)		-96.5		dB
Power Supply Rejection Ratio (1 kHz)		-81		dB
Power Supply Rejection Ratio (100 Hz)		-57.9		dB
ADC Converters				
Dynamic Range (-60 dB Full Scale, A-Weight)		100		dB FSA
Total Harmonic Distortion			0.003	%
Frequency Response	20		21,600	Hz
Transition Band	21,600		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	-74			dB
Out-of-Band Rejection		-40		dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB
DAC Converters				
Dynamic Range (-60 dB Full Scale, A-Weight)		110		dB FSA
Total Harmonic Distortion			0.003	%
Frequency Response	20		21,600	Hz
Transition Band	21,600		28,800	Hz
Stop Band	28,800			Hz
Stop Band Rejection	-74			dB
Out-of-Band Rejection		-40		dB
Channel Separation		-90		dB
Spurious Tone Reduction		-100		dB
Attenuation, Gain Step Size		1.5		dB

Note:
The frequency response, transition band and stop band specified in the table is based on fs = 48 kHz, and scale with fs.

10.3 AC Characteristics

Link Reset and Initialization Timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
RESET# Active Low Pulse Width	T_{RST}	1.0	-	-	μs
RESET# Inactive to BCLK Startup Delay for PLL Ready Time	T_{PLL}	-	200	-	μs
SDI Initialization Request	T_{Frame}	17	-	25	Frame Time

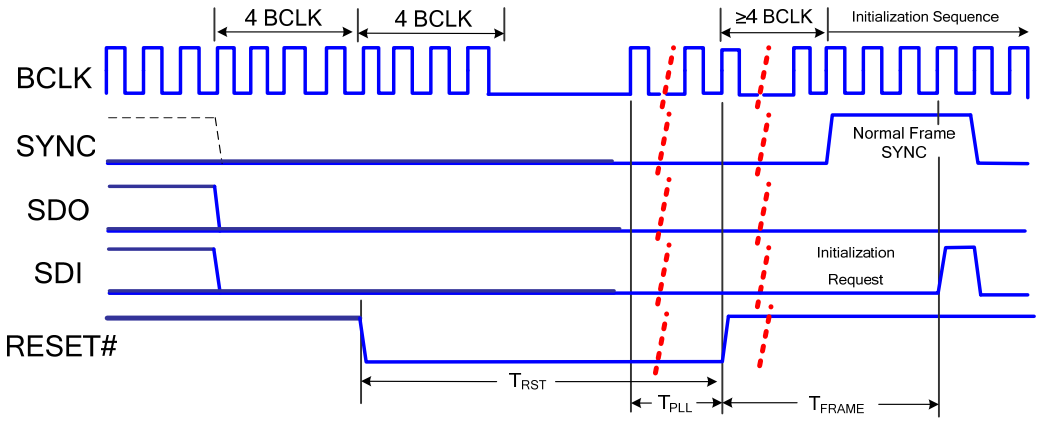


Figure 20 – Link Reset and Initialization Timing Diagram

Link Timing Parameters at the Codec

Parameter	Symbol	Min.	Typ.	Max.	Unit
BCLK Frequency		-	24.0	-	MHz
BCLK Period	T_{Cycle}	-	41.67	-	ns
BCLK Jitter	T_{Jitter}	-	-	2.0	ns
BCLK High Pulse Width	T_{High}	17.5	-	24.16	ns
BCLK Low Pulse Width	T_{Low}	17.5	-	24.16	ns
SDO Setup Time at both Rising and Falling Edge of BCLK	T_{Setup}	5.0	-	-	ns
SDO Hold Time at both Rising and Falling Edge of BCLK	T_{Hold}	5.0	-	-	ns
SDI Valid Time after Rising Edge of BCLK (1:50 pF External Load)	T_{TCO}	3		11.0	ns
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Input High Voltage	V_{IH}	-	0.65 V_{CC}	-	V
Input Test Voltage	V_T	-	0.5 V_{CC}	-	V
Input Low Voltage	V_{IL}	-	0.35 V_{CC}	-	V

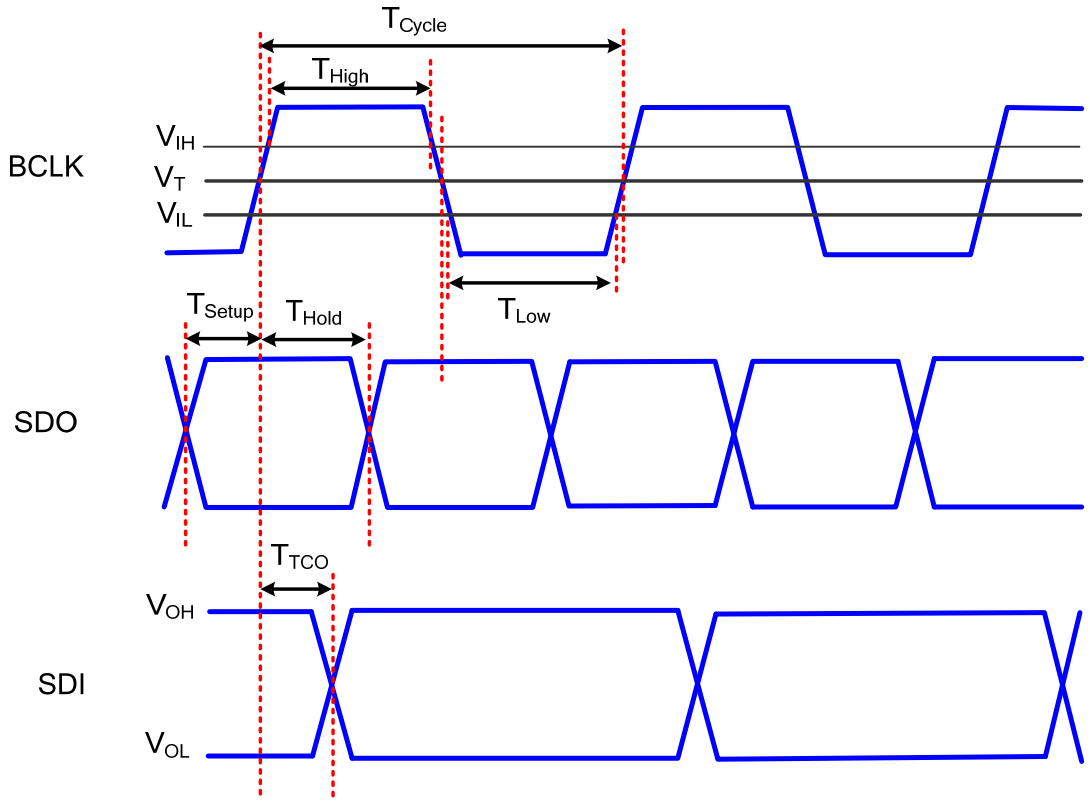


Figure 21 – Link Signals Timing Diagram

SPDIF AC Timing Characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit
SPDIF Out Frequency	-	-	3.072	-	MHz
SPDIF Out Period (48 kHz Sample Rate)	T_{Cycle}	-	325.6	-	ns
SPDIF Out Jitter	T_{Jitter}	-	-	2	ns
SPDIF Out High Level Width	T_{High}	-	162.8 (50%)	-	ns (%)
SPDIF Out Low Level Width	T_{Low}	-	162.8 (50%)	-	ns (%)
SPDIF Out Rising Time	T_{Rise}	-	4	-	ns
SPDIF Out Falling Time	T_{Fall}	-	6	-	ns

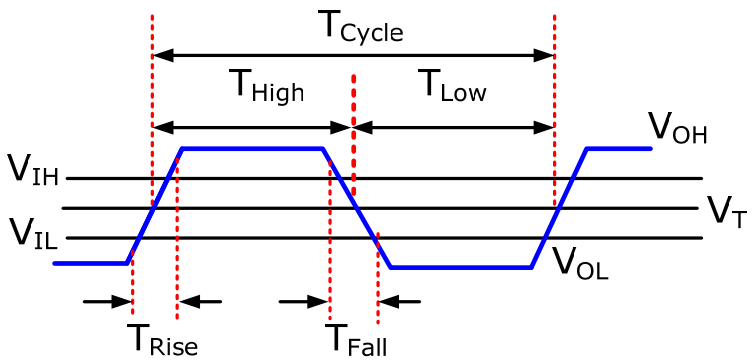
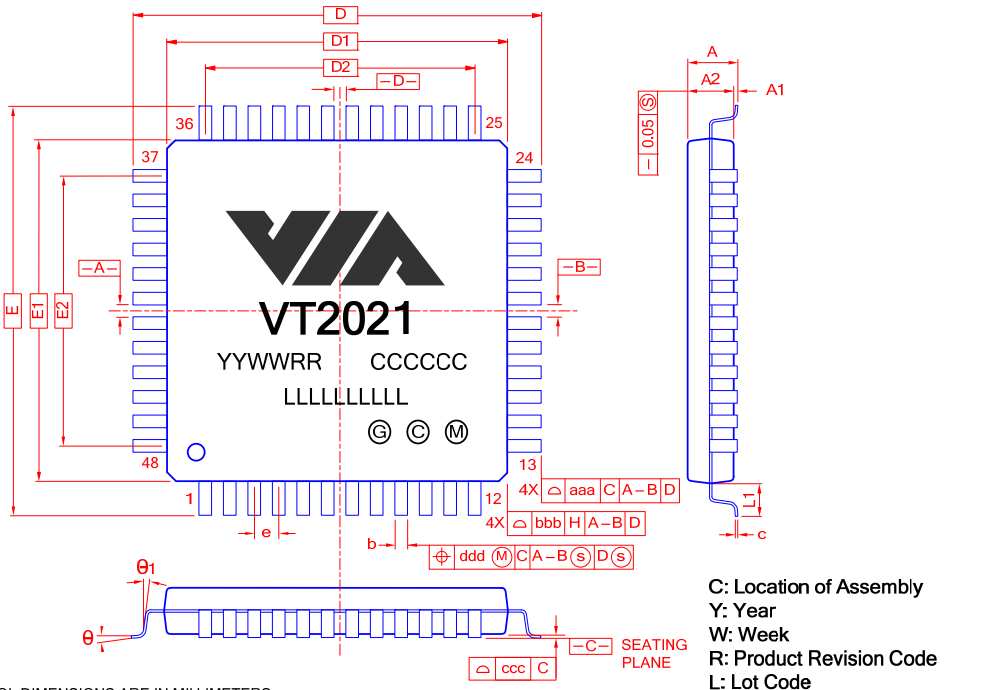


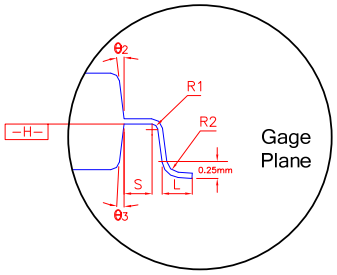
Figure 22 – SPDIF AC Timing Diagram

11 Mechanical Specification



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.60	–	–	0.063
A1	0.05	–	0.15	0.002	–	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R1	0.08	–	–	0.003	–	–
R2	0.08	–	0.20	0.003	–	0.008
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ1	0°	–	–	0°	–	–
Θ2	11°	12°	13°	11°	12°	13°
Θ3	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	–	–	0.008	–	–
48L						
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	5.50			0.217		
E2	5.50			0.217		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		



NOTES :

1. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

2. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07mm.

Figure 23 – VT2021 LQFP-48 Package (7 mm×7 mm)

12 Reference Applications

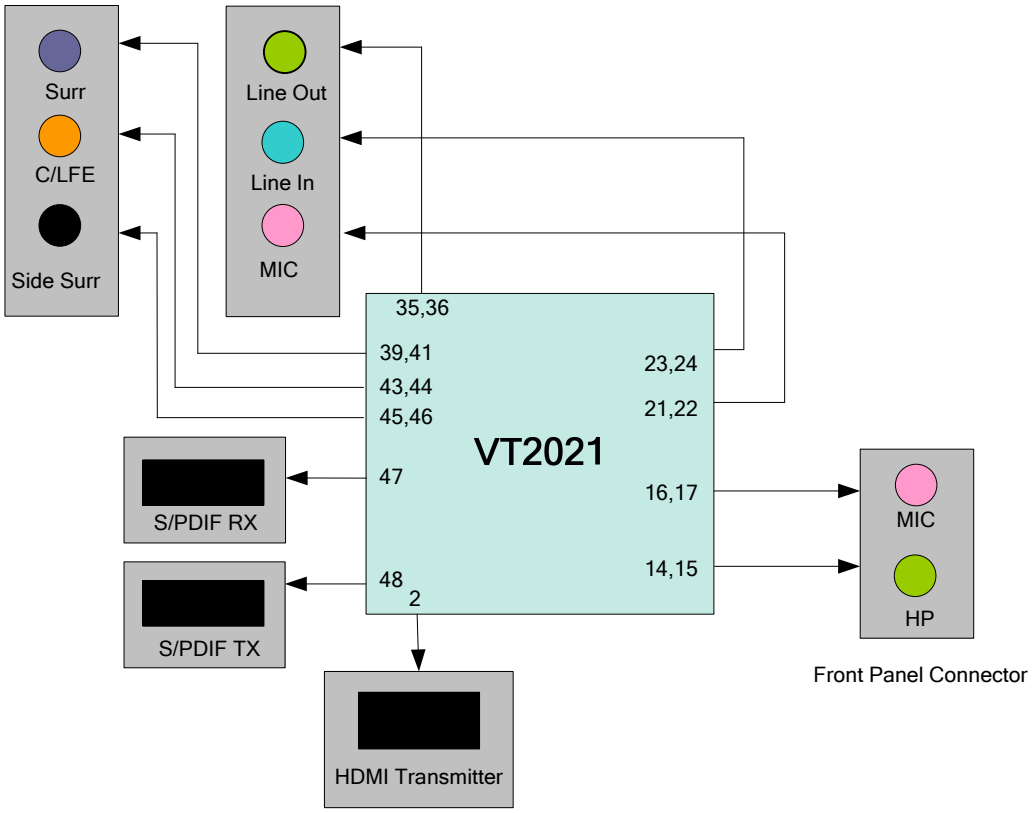


Figure 24 – The System with Front Panel Design

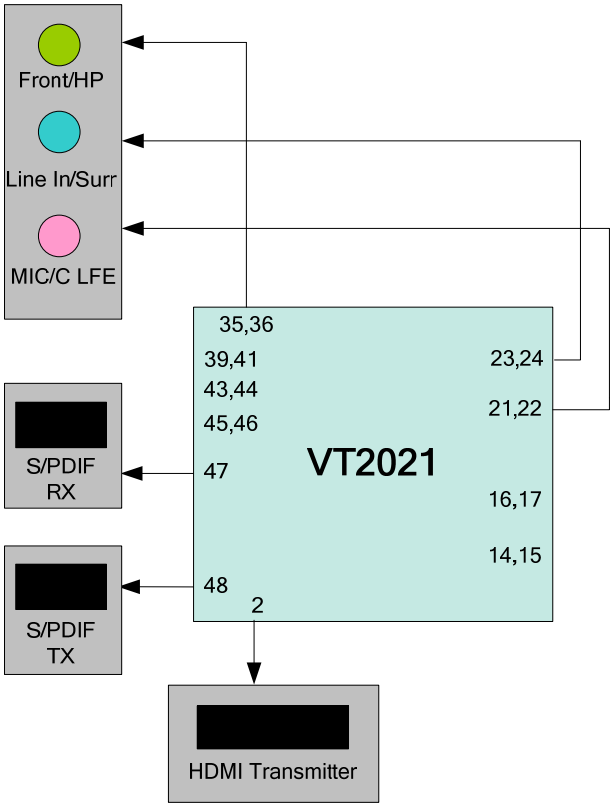


Figure 25 – The System without Front Panel Design

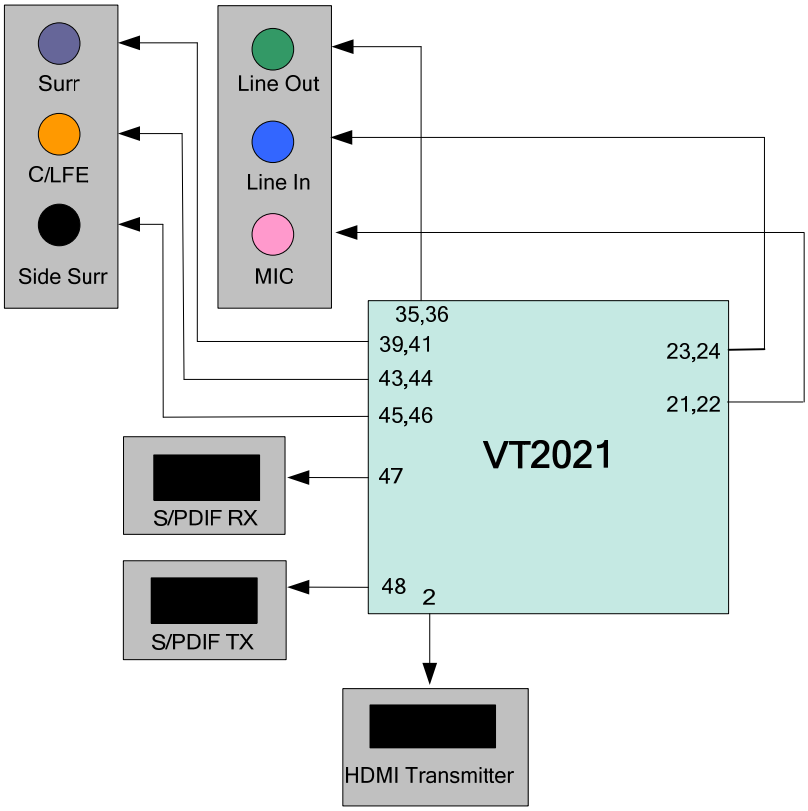


Figure 26 – The System with Only One Back Panel Connector Design

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