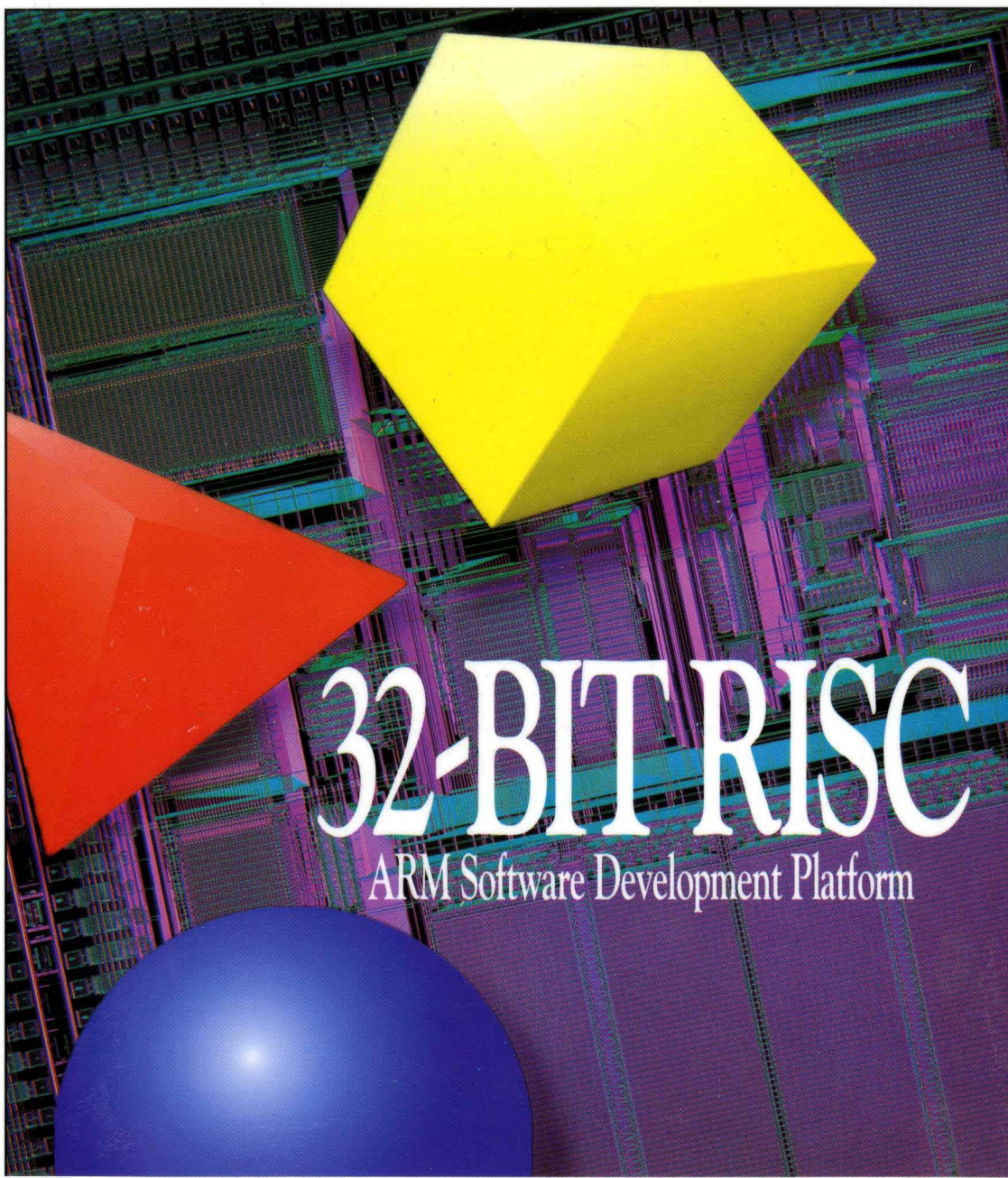
VLSI TECHNOLOGY, INC.

ARM600 DEVELOPMENT CARD



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SECTION — PAGE NUMBER

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1. INTRODUCTION

The ARM™ RISC processor family provides more computing power per silicon area than other processors, and is a cost-effective way to higher performance in many embedded applications.

The VY86PID is a development board designed to enable ARM developers to use the ARM600 to generate software and hardware applications for the ARM product line. The VY86PID incorporates ARM600 MPU, fast PGAs (Programmable Gate Arrays), and inexpensive PC-based, high-integration peripheral components.The initial operating environment is monitor-based with an expected progression to a real-time multitasking kernel. Program development is aided by incorporation of a dedicated logic analyzer connector.

The VY86PID is made for users who will generate designs and write code for fast I/O control, video games and graphics, disk caching, page printer controllers, OCR, etc.

1.1 Features

PROCESSOR	VY86C600- ARM600 with Cache and Memory Management
ROM	4x 27C256 to 4x 27C080 (128K to 4 MB) EPROM
MAIN MEMORY	1,4,16 MByte memory with 256K, 1M, 4M DRAMS
ENDIANESS	Little Endian
OPERATING SYSTEMS	ROM Monitor with remote debugger interface
COMMUNICATIONS	RS-232 serial port, Centronics printer port
EXPANSION	32-bit data, 4 Mbyte Address, dual row connector. All major components are on the main board.

2. HARDWARE DESCRIPTION

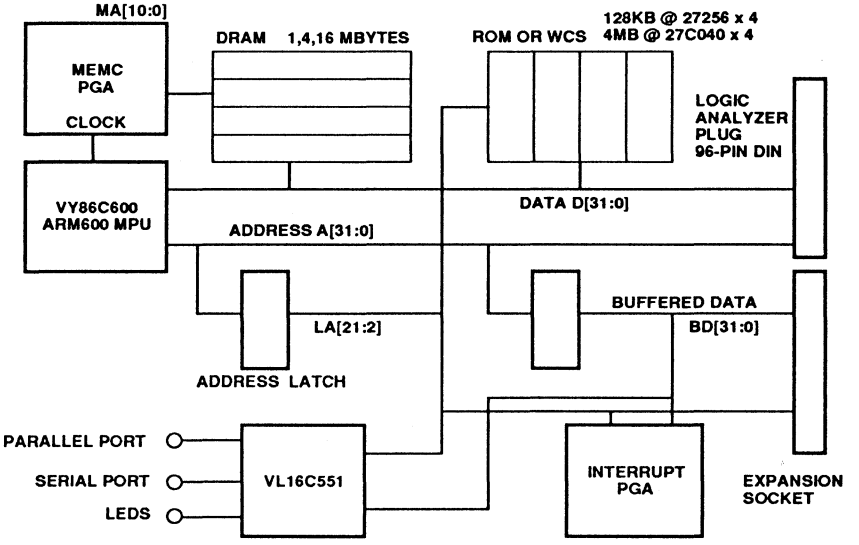
2.1 Main Memory

The main memory is dynamic and consists of one bank of four 8-bit SIMMs (single in-line memory modules). If 256K DRAMs are used, the main memory is 1 MByte. If 1 MByte DRAMs are used, the main memory is 4 MBytes. If 4 Meg DRAMs are used, the main memory is 16 MBytes. Main memory organized as 32-bits wide.

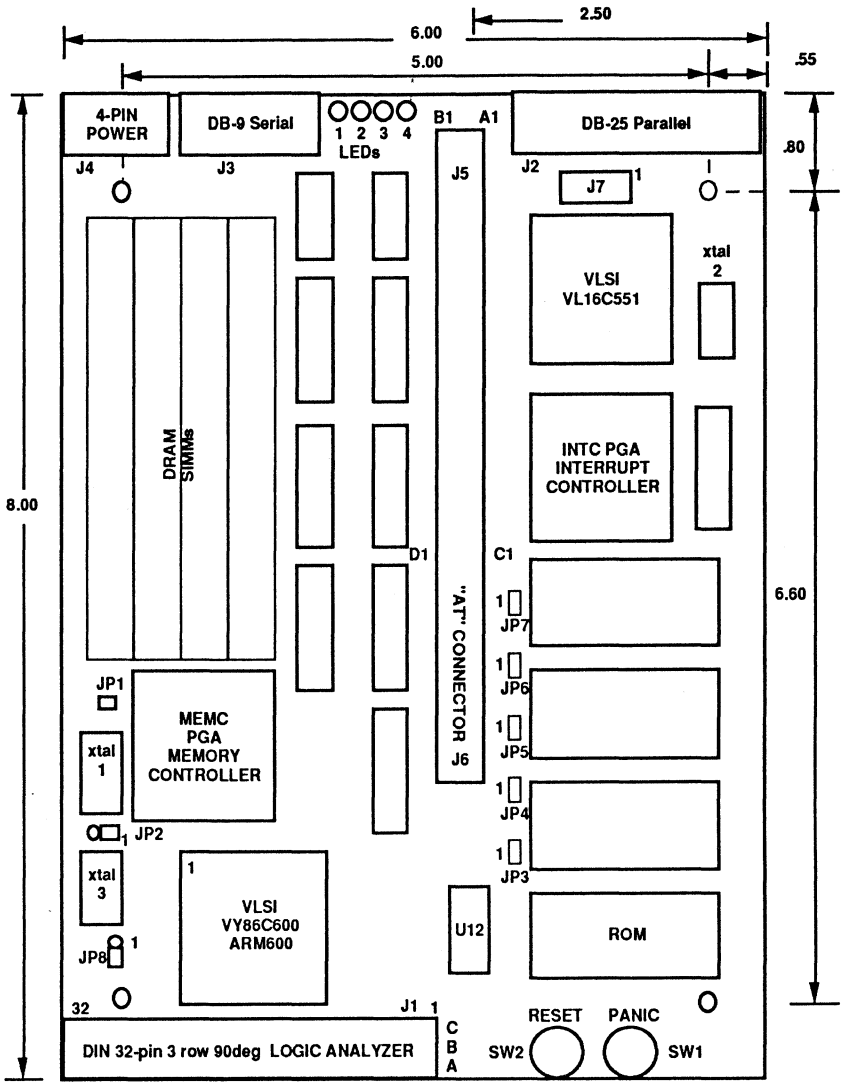
2.2 Connectors

Serial port to 38.4 Kbaud (DB-9, Male, PC pinout)
Centronics printer port (DB-25, Female, PC pinout)

2.3 VY86PID Block Diagram



2.4 VY86PID Board Layout*



* Note: Drawing dimensions specified in inches.

2.5 Component List

Part Number	Description	Vendor
VY86C600A	32-bit RISC processor with cache MMU, and write buffer	VLSI/ARM
QL8X12	Memory Controller PGA	VLSI/QuickLogic
QL8X12	Interrupt Controller PGA	VLSI/QuickLogic
VL16C551	Serial Port with FIFO Bidirectional Parallel Port General-Purpose Port used for LEDs	VLSI
30-pin SIMMs	256K x 8 bit by 4 Bytes = 1 MByte 1M x 8 bit by 4 Bytes = 4 MByte 4M x 8 bit by 4 Bytes = 16 MBytes	
28/32-Pin EPROM	27C256 = 128K Bytes 27C040 = 2 MBytes	

2.6 Option Bus

The Option Bus has been derived from the IBM PC/AT™ and PC/XT™ personal computers, from where the basic card shape and pin out are obtained. No automatic byte packing is supported. The expansion cards are for I/O such as laser printer interface. The main memory is in the SIMM modules on the motherboard. The I/O Channel is designed to work with a DTC-5180/7CR hard disk controller, therefore, expansion pins not connected to this controller are free to be used for 32-bit expansion. Four slots are supported.

32 Data Lines
20 Address lines (4 Megabyte address range per MEMR/W and IOR/W)
3 Interrupts (IRQs)
3 Pseudo DMAs (at DRQ locations)

2.7 32-Bit Expansion Connector

Option Connector Description:

Pinout	A	B (circuit)	C	D (circuit)
1	GND	GND	BE1*	GND
2	D07	RESET	BE2*	GND
3	D06	+5V	D24	NC
4	D05	NC	D25	NC
5	D04	NC	D26	DRQ4
6	D03	DRQ2	D27	DACK0*
7	D02	NC(-12V)	D28	DRQ0
8	D01	NC	D29	D16
9	D00	+12V	D30	D17
10	NC	GND	D31	D18
11	BE0*	MEMW*	D08	D19
12	LA21	MEMR*	D09	D20
13	LA20	IOW*	D10	D21
14	LA19	IOR*	D11	D22
15	LA18	DACK3*	D12	D23
16	LA17	DRQ3	D13	+5
17	LA16	DACK1*	D14	BE3*
18	LA15	DRQ1	D15	GND
19	LA14	NC		
20	LA13	12 MHz MCLK		
21	LA12	NC		
22	LA11	IRQ6		
23	LA10	IRQ5		
24	LA09	IRQ4		
25	LA08	IRQ3		
26	LA07	DACK2*		
27	LA06	NC		
28	LA05	NC		
29	LA04	+5V		
30	LA03	NC		
31	LA02	GND		

2.8 Bus Line Description

D0 to D7	Lowest significant byte of data (A0=0 A1=0).
D8 to D15	Middle significant byte of data (A0=1, A1=0).
D16 to D23	Higher significant byte of data (A0=0, A1=1).
D24 to D31	Highest significant byte of data (A0=1, A1=1).
LA2 to LA21	Latched Address 20-Bit Memory Address defines 4 MBytes of expansion addressing (32-bit word Addressable). A 4 MByte address space is defined for both memory space (MEMR/W) and for IO space (IOR/W).
BE0	Byte Enable 0 enables the drivers for the lowest byte (Bits 0 to 7) on the bus.
BE1	Byte Enable 1 enables the drivers for the middle byte (Bits 8 to 15) on the bus.
BE2	Byte Enable 2 enables the drivers for the upper middle byte (Bits 16 to 23) on the bus.
BE3	Byte Enable 3 enables the drivers for the highest byte (Bits 24 to 31) on the bus.
MRD	Memory Read - Active Low pulse indicates that the bus master is reading data from memory on the bus.
MWR	Memory Write - Active low pulse indicates that the bus master is writing to memory on the bus.
IORD	Input/ Output Read - Active Low pulse indicates that the bus master is reading data from I/O devices on the bus.
IOWR	Input/ Output Write - Active low pulse indicates that the bus master is writing to I/O devices on the bus.
12CLK	Bus Clock - 12 MHz Clock originating from the motherboard.
RESET	Power on reset or Bus reset both active high.
IRQ3-6	Pre-decoded interrupt vectors / active high. Hardwired to the IOC controller on the motherboard.
DRQ 0-4	Pseudo DMA (Fast interrupt request).
DACK 0-3	Pseudo DMA Acknowledge.
GND	Ground +5 Volts. Main power for boards.
+12 Volts	Auxiliary supplies for varied uses.

2.9 Logic Analyzer/ WCS Connector

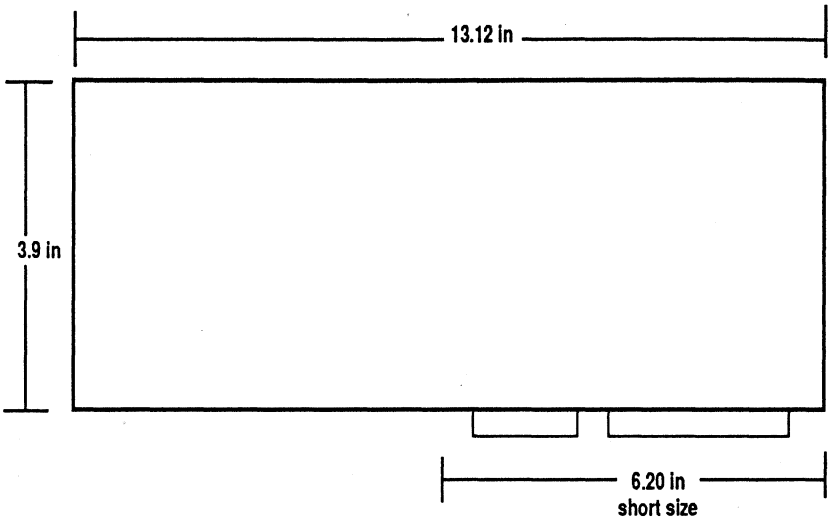
Pin	A	B	C
1	D[0]	D[1]	D[2]
2	D[3]	D[4]	D[5]
3	D[6]	D[7]	D[8]
4	D[9]	D[10]	D[11]
5	D[12]	D[13]	D[14]
6	D[15]	D[16]	D[17]
7	D[18]	D[19]	D[20]
8	D[21]	D[22]	D[23]
9	D[24]	D[25]	D[26]
10	D[27]	D[28]	D[29]
11	D[30]	D[31]	-
12	MCLK	GND	FCLK
13	MREQ	GND	NOPC
14	NWAIT	GND	CPCL
15	NRW	+5V	ABE
16	NBW	+5V	DBE
17	ABORT	+5V	CBE
18	-	+5V	MBE
19	-	GND	NRESET
20	ROMOE	GND	NMI
21	DISAROM	GND	NHALT
22	A[0]	A[1]	A[2]
23	A[3]	A[4]	A[5]
24	A[6]	A[7]	A[8]
25	A[9]	A[10]	A[11]
26	A[12]	A[13]	A[14]
27	A[15]	A[16]	A[17]
28	A[18]	A[19]	A[20]
29	A[21]	A[22]	A[23]
30	A[24]	A[25]	A[26]
31	A[27]	A[28]	A[29]
32	A[30]	A[31]	GND

2.10 Logic Analyzer Signal Description

Signal	Source	Destination	Description
D[0:31]	ARM600	System	Processor Data Bus
A[0:31]	ARM600	System	Processor Address Bus
FCLK	MEMC	ARM600	25 MHz Processor Bus
MCLK	MEMC	ARM600	12.5 MHz Memory Bus
NWAIT	MEMC	ARM600	Wait State Signal
NRW	ARM600	System	Not Read / Write
NBW	ARM600	System	Not Byte / Word
ABORT	Break Point Board	ARM600	Detection of Break Point Address condition
STRB1	Break Point Board	Logic Analyzer	Observable strobe for Logic Analyzer
STRB2	Break Point Board	Logic Analyzer	Observable strobe for Logic Analyzer
ROMOE	MEMC	ROM	ROM output enable: Used for Writable control store (WCS)
MREQ	ARM600	MEMC	Memory Request Signal
nOPC	ARM600	Logic Analyzer	Opcode Request - Instruction on CPD bus
CPCLK	ARM600	Logic Analyzer	Coprocessor Clock
ABE	Break Point Board	ARM600	Address Bus Enable
DBE	Break Point Board	ARM600	Data Bus Enable
CMBE	Break Point Board	ARM600	Control Bus Enable
NRESET	Reset Logic	System	Negative Reset Signal
NMI	Break Point Board	INTC	Non-Maskable FIQ input
HALT	Break Point Board	MEMC	Force NWAIT Condition

2.11 Option Boards

Option cards are 13.12 x 3.9 inches with external I/O side-mounted.



2.12 Serial Port

A serial port is provided for communication to the host or for applications.

D-S Eqiv Pin	Description
1	
2	Receive Data (Input)
3	Transmitter Data (Output)
4	
5	
6	
7	RTS - Ready to Send (Output)
8	CTS - Clear to Send (Input)
9	

2.13 Parallel Port

The parallel port is bidirectional, and it can be used for input as well as output. Typically, it has been used for the control of a printer, yet several plug-in peripherals, such as Ethernet adapters, have now taken advantage of this useful interface.

D-Shell Pin	Description
1	-STROBE
2	Data0
3	Data1
4	Data2
5	Data3
6	Data4
7	Data5
8	Data6
9	Data7
10	-ACK
11	BUSY
12	PE
13	SLCT
14	-AUTOFEED XT
15	-ERROR
16	-INIT
17	-SLCTIN
18	GND
19	GND
20	GND
21	GND
22	GND
23	GND
24	GND
25	GND
	NU

3. SYSTEM MEMORY SPACE ALLOCATION

3.1 Memory Map

000 0000 to 0FF FFFF	DRAM - 1 to 16 MBytes. One Bank of DRAM in four SIMMs 8 256K x 4 = 1 MByte 4 512K x 8 = 2 MByte 8 1MB x 4 = 4 MByte 32 4MB x 1 = 16 MByte DRAM is repeated within the 16 MByte space. After Reset ROM is located here.
100 0000 to 1FF FFFF	DRAM - Bank 2 (Not used on this board)
200 0000 to 2FF FFFF	I/O control is mapped to this space: 16 MByte, used for both internal and external peripherals.
300 0000 to 3FF FFFF	ROM, EPROM, or Writable Control Store

3.2 Software Vectors

Address	Vector	Instruction	Description
000 0000	Reset Vector	LDR PC,[PC,#Vector offset]	Load Soft Vector to ROM Reset
000 0004	Undef Instr	LDR PC,[PC,#Vector offset]	Load Soft Vector to ROM FP Emulator
000 0008	Software Int	LDR PC,[PC,#Vector offset]	Load Soft Vector to ROM SWI Dispatcher
000 000C	Abort Inst	LDR PC,[PC,#Vector offset]	Load Soft Vector to ROM Routine
000 0010	Abort Data	LDR PC,[PC,#Vector offset]	Load Soft Vector to ROM Routine
000 0014	Reserved		
000 0018	Normal Int	LDR PC,[PC,#Vector offset]	Load Soft Vector to IRQ Dispatcher
000 001C	Fast Int	LDR PC,[PC,#Vector offset]	Load Soft Vector to FIRQ Dispatcher

3.3 I/O Memory Map

200 0000 to 2FF FFFF General I/O area divided as show below:

200 0000 to 23F FFFF Internal Functions

240 0000 to 270 001C Expansion Slot Pseudo DMA

Reg	Name	R/W	Description
0000	DACK0	R/W	IOR/W asserted with DACK0
0004	DACK1	R/W	IOR/W asserted with DACK2
0008	DACK2	R/W	IOR/W asserted with DACK3
000C	DACK3	R/W	IOR/W asserted with DACK3
0010	DACK0 TC	R/W	IOR/W asserted with DACK0 and TC
0014	DACK1 TC	R/W	IOR/W asserted with DACK1 and TC
0018	DACK2 TC	R/W	IOR/W asserted with DACK2 and TC
001C	DACK3 TC	R/W	IOR/W asserted with DACK3 and TC

280 0000 to 2BF FFFF Expansion Slot I/O Space (-IOR, -IOW generated)

2C0 0000 to 2FF FFFF Expansion Slot Memory Space (-MRD, -MWR generated)

200 0000 to 204 FFFF Internal Functions

INTC PGA addressed from 200 0000 to 200 000C

Reg	Name	R/W	Description
0000	IRQS	R	IRQ Status
0000	IRQRST	W	IRQ RESET
0004	IRQM	W	IRQ Enable
0008	FIQS	R	FIQ Status
000C	FIQM	W	FIQ Enable

200 0000 to 2FF FFFF 16C551 Integrated Functions

200 0020 to 200 003C 16C551 Serial Port

Reg	Name	R/W	Description
0020	RBR/THR	R/W	Receive Buffer Register - Transmitter Holding Register
0024	IER	R/W	Interrupt Enable Register(bidirectional)
0028	IIR	R	Interrupt Identification (read only)
002C	LCR	R/W	Line Control Register
0030	MCR		Modem Control Register
0034	LSR		Line Status Register
0038	MSR		Modem Status Register
003C	SR	R/W	Scratch Register
0020	(DLAB)	R/W	Divisor Latch LSB
0024	(DLAB)	R/W	Divisor Latch MSB

200 0040 to 200 005C AUX Chip Select

200 0060 to 200 006C 16C551 Parallel Port

Reg	Name	R/W	Description
0060	PDOUT	R/W	Data Input/Output Register
0064	PSTAT	R	Printer Status Register
0068	PCON	R/W	Printer Control Register
006C	GPIO	R/W	General-Purpose Input/Output Pins

4. INPUT/ OUTPUT REGISTER DESCRIPTION

4.1 INTC PGA Registers

200 0000 to 200 000C

Reg	Name	R/W	Description
0000	IRQS	R	IRQ Status
0000	IRQRST	W	IRQ Reset
0004	IRQM	W	IRQ Mask
0008	FIQS	R	FIQ Status
000C	FIQM	W	FIQ Mask

4.2 IRQ Status Register (IRQS)

(address 200 0000)

This register contains the raw interrupt input (without masking). A bit in this register is "anded" with the corresponding mask bit in the IRQM register and then "ored" with all the other bits to generate the IRQ.

Reg	7	6	5	4	3	2	1	0
IRQS	PANIC	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0

Bit 7	PANIC[1]	This bit is set when the panic button input is pulsed low. Reset by writing reset location with Bit 7 set.
Bit 6	IRQ6	Connected to Expansion Slot IRQ6
Bit 5	IRQ5	Connected to Expansion Slot IRQ5
Bit 4	IRQ4	Connected to Expansion Slot IRQ4
Bit 3	IRQ3	Connected to Expansion Slot IRQ3
Bit 2	IRQ2	Parallel Port Interrupt
Bit 1	IRQ1	Timer Interrupt - Reset by writing reset location with Bit 1 set.
Bit 0	IRQ0	Serial Port 1

Note: 1. Panic is always enabled.

4.3 IRQ Reset Port (IRQRST)

(address 200 0000)

Bit 7; Writing this bit will reset the PANIC[1] interrupt bit.

Bit 1; Writing this bit will reset the timer interrupt bit.

4.4 IRQ Mask Register (IRQM)

(address 200 0004)

Writing a "one" to Bits 6-0 will enable the corresponding interrupt bit. This register is reset on power on.

Reg	7	6	5	4	3	2	1	0
IRQM	ON	ENIRQ6	ENIRQ5	ENIRQ4	ENIRQ3	ENIRQ2	ENIRQ1	ENIRQ0

4.5 FIQ Status Register (FIQS)

(address 2FE 0008)

This register contains the raw fast interrupt input (without masking). A bit in this register is "anded" with the corresponding mask bit in the FIQM register and then "ored" with all the other bits to generate the FIQ.

Reg	7	6	5	4	3	2	1	0
FIQS	DRQ3	DRQ2	DRQ1	DRQ0	NMI	DRQ2	RXRQ1	TXRQ1

Bits 7-4	DRQ3-0	Expansion Slot DMA Request
Bit 3	NMI	Logic Analyzer Port
Bit 2	DRQ4	Expansion Slot
Bit 1	RXRQ1	Serial Port 1 Receive DMA Request
Bit 0	TXRQ1	Serial Port 1 Transmit DMA Request

4.6 FIQ Mask Register (FIQM)

(address 200 000C)

Writing a "one" to Bits 7-0 will enable the corresponding interrupt bit. This register is reset on power on.

5. VL16C551 I/O REGISTERS

(200 0020 to 200 006C)

The VL16C551, 1 - 8252 UART (with FIFO, and an 8-bit parallel bidirectional Centronics printer interface).

5.1 Serial Interfaces

(200 0020 to 200 005C):

One UART is included in the VL16C551. The UART has a VL16C550 cell with a 16-byte data FIFO for maximum performance in data transfers from the host computer. The UART is described in detail below. For more information, see the VLSI Technology VL16C551 datasheet.

UART Register contents are:

Reg	Ser1	Type	D7	D6	D5	D4	D3	D2	D1	D0
RBR	0020	R	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
THR	0020	W	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
IER	0024	R/W	-	-	-	-	EDSSI	ELSI	ETBEI	ERBFI
IIR	0028	R	IIR7	IIR6	-	-	FIFEN	IID1	IID0	IPENDN
FCR	0028	W	FTL1	FTL0	-	-	RMODE	TFCLR	RFCLR	FIFOEN
LCR	002C	R/W	DLAB	BREAK	STICK	EVPAR	PAREN	SBSEL	WLS1	WLS0
MCR	0030	R/W	-	-	-	LBACK	-	-	RTS	DTR
LSR	0034	R/W	ERFIFO	TEMT	THRE	ERBRK	ERFRM	ERPAR	EROVR	RDR
MSR	0038	R/W	-	-	DSR	-	-	-	DDSR	-
SCR	003C	R/W	D7	D6	D5	D4	D3	D2	D1	D0
DLL	0020	W	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
DLM	0024	W	DL15	DL14	DL13	DL12	DL11	DL10	DL9	DL8

5.2 Serial Port Data Registers (RBR, THR)

Received data at the SRXD input pin is shifted into the Receiver Shift Register by the 16X clock provided from the baud rate generator. This clock is synchronized to the incoming data based on the position of the start bit. When a complete character is shifted into the Receiver Shift Register, the assembled data bits are parallel loaded into the Receiver Buffer Data Register (RBR). The Read Data Ready (RDR) flag in the Serial Port Status Register (LSR) is set.

FIFO (and double) buffering of the received data permits continuous reception of data without losing received data. While the Receiver Shift Register is shifting a new character into the serial channel, the Receiver Buffer Register is holding a previously received character for the CPU to

read. Failure to read the data in the RBR before complete reception of the next character result in the overflow of the data in the register. The Overrun Error (EROVO) flag in the LSR register indicates the overrun condition.

During Transmit operation, the Transmitter Holding Register holds parallel data from the internal data bus until the Transmitter Shift Register is empty and ready to accept a new character. Data Bit 0 is the first bit transmitted. The Transmit Holding Register Empty (THRE) flag in LSR reflects the current status.

Receive Buffer Register contents are:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
RBR	0000	R	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	RD0	R	undef	Serial Port Receive Buffer Data Bit 0
. . .				
7	RD7	R	undef	Serial Port Receive Buffer Data Bit 7

Transmit Holding Register contents are:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
THR	0x030	W	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	TD0	W	undef	Serial Port Transmit Holding Data Bit 0
. . .				
7	TD7	W	undef	Serial Port Transmit Holding Data Bit 7

5.3 Interrupt Enable Register (IER)

The Interrupt Enable Register is used to independently enable the four types of serial channel interrupts.

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
IER	0x031	R	-	-	-	-	EDSSI	ELSI	ETBEI	ERBFI

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	ERBFI	R	0	Enable Received Data Available Interrupt [and Timeout Interrupt in FIFO mode for Host UART only]
1	ETBEI	R	0	Enable Transmitter Holding Reg Empty Interrupt
2	ELSI	R	0	Enable Receiver Line Status Interrupt
3	EDSSI	R	0	Enable Modem Status Interrupt
7:4	RESV	-	-	Not Used

5.4 Interrupt Identification Register (IIR)

The Interrupt Identification Register is a read only register used to identify the four types of serial channel interrupts.

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
IIR	0028	R	IIR7	IIR6	-	-	FIFEN	IID1	IID0	IPENDN

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	IPENDN	-	R/O	Set to 0 if ANY Interrupt is pending.
2:1	IID[1:0]	-	R/O	0 Interrupt Type bits [1:0] (see page 19).
3	FIFEN	R	0	0=16C450 Mode, 1=16C550 Mode (FIFO enabled).
5:4	RESV	-	-	Not Used - Always 0.
7:6	IIR[7:6]	R	0	FCR[0]=1 sets these two bits.

5.5 IIR Table of Pending Interrupts

Int ID Bits	Priority	Description
3 2 1 0 Level	Int Flag, Int Source	Int Reset Control
X X X 1	None	None
0 1 1 0 First	Recvr Line Status	LSR Read
0 1 0 0 Second	Recvd Data Avail	RBR Read
1 1 0 0 Second	FIFO Status, FIFO thresh, wait timeout	RBR Read
0 0 1 0 Third	THRE	IIR Read if THRE is the source, else THR Write
0 0 0 0 Fourth	Modem Status	MSR Read

5.6 FIFO Control Register (FCR)

The FIFO Control Register is used to control the operation of the built-in data FIFOs.

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
FCR	0028	W	FTL1	FTL0	–	–	RMODE	TFCLR	RFCLR	FIFOEN

Bit	Name	R/W	Reset	Use
0	FIFOEN	W	0	When set to 1, enables both receive and transmit FIFOs.
1	RFCLR	W	0	Writing a 1 to this bit clears the Receive FIFO.
2	TFCLR	W	0	Writing a 1 to this bit clears the Transmit FIFO.
3	RMODE	W	0	Changes the RXRDY and TXRDY pins from mode 0 to mode 1
5:4	RESV	–	–	Not Used.
7:6	FTL[1:0]	W	00?	Receive FIFO trigger level:

FTL1	FTL0	Trigger Level
0	0	1 byte
0	1	4 bytes
1	0	8 bytes
1	1	14 bytes

5.7 Line Control Registers (LCR)

The format of the characters transmitted and received are controlled by the Line Control Registers.

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
LCR	002C	R/W	DLAB	BREAK	STICK	EVPAR	PAREN	SBSEL	WLS1	WLS0

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
1:0	WLS[1:0]	R/W	0	Word Length Select:

WLS1	WLS0	Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

2	SBSEL	R/W	0	Stop Bit Select. This bit specifies the number of stop bits in each transmitted character. When set to 0, one stop bit is generated. When set to 1, 1.5 stop bits are generated if 5 data bits are selected, but 2 stop bits are generated if 6, 7, or 8 data bits are selected. The receiver checks for the appropriate number of stop bits.
3	PAREN	R/W	0	Parity Enable. When set to 1, a parity bit is generated and checked.
4	EVPAR	R/W	0	Parity Select. When parity is enabled, this bit selects odd parity (0) or even parity (1).
5	STICK	R/W	0	Stick Parity. When parity is enabled, a 1 causes transmission and reception of a parity bit to be in the opposite state from that indicated by EVPAR. This allows forced parity to a known state.

Detailed Bit Definition (Cont.)

Bit	Name	R/W	Reset	Use
6	BREAK	R/W	0	Force Break. When set to 1, the serial output (TXD) is forced to the spacing (0) state. The break is disabled by setting this bit to 0. The width of the break pulse created is a function of software. As a result, the first character transmitted following a break condition might have a framing error, and should be discarded. If the following sequence is used, no erroneous or extraneous characters will be transmitted due to the break: after THRE load THR with all zeros, set BREAK bit in response to the next THRE. Wait for TEMT=1, then reset BREAK when normal transmission has to be restored.
7	DLAB	R/W	0	Divisor Latch Bit. When set, addresses 020 and 024 access the UART clock divider latches.

5.8 Modem Control Register (MCR)

The DTR pin and loop back function are controlled by the Modem Control Registers:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
HMCR	0030	R/W	-	-	-	LBACK	-	-	RTS	DTR

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	DTR	R/W	0	Data Transmitter Ready. When set to 1, the DTR output pin is forced low.
1	RTS	R/W	0	Request to Send. When set to 1, the RTS output is forced low.
3:2	RESV	-	-	Reserved.
4	LBACK	R/W	0	Loopback Enable. This bit provides a local loopback feature for diagnostic testing of the serial channel. When set to 1, the Transmit Data output pin (TXD) is set to the marking state (1), and the Receive Data input pin (RXD) is disconnected. The output of the Transmitter is looped back into the Receiver. The handshake input pin (DSR or VUDSR) is disconnected. The handshake output pins (DTR) are held in their inactive state (1). In the diagnostic mode, data transmitted is immediately received. This allows the processor to verify the transmit and receive data paths of the serial channels.
7:5	RESV	-	-	Reserved.

5.9 Line Status Registers (LSR)

The Line Status Registers hold the current status of the UART:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
HLSR	0034	R/W	ERFIFO	TEMT	THRE	ERBRK	ERFRM	ERPAR	EROVR	RDR

Error flags ERBRK, ERFRM, ERPAR, ERFIFO, and EROVR provide the status of any error conditions detected in the receiver. During reception of the stop bit(s), the error flags are set by an error condition. The error flags are not reset by the absence of an error condition in the next received character. The flags reflect the last character only if no overrun occurred.

In the LSR, the setting of status bits is inhibited during status register read operations by the CPU. If a status condition is generated during a read operation, the status bit is not set until the trailing edge of the read.

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	RDR	R/W	0	Receive Data Ready. This bit indicates that the Receiver Buffer Register has been loaded with a received character (including Break) and that the CPU may access this data. Reset whenever register is read.
1	EROVR	R/W	0	Receive Overrun Error. This bit indicates that the character in the Receiver Buffer Register has been overwritten by a character from the Receiver Shift Register before being read by the CPU. The first character is thereby lost. Reset whenever register is read.
2	ERPAR	R/W	0	Parity Error. This bit is set when the last character received has a parity error based on the programmed versus calculated parity. Reset whenever register is read.
3	ERFRM	R/W	0	Framing Error. This bit indicates that the last character received contained an incorrect number of stop bits. This is caused by the absence of the required stop bit or by a stop bit that is too short to be detected. Reset when ever register is read.

Detailed Bit Definition (Cont.)

Bit	Name	R/W	Reset	Use
4	ERBRK	R/W	0	Break Detect Error. This bit indicates that the last character received was a break character, i.e. the received data input was held low (0) for longer than a full word transmission time (start bit + data bits + parity + stop bits). Reset whenever register is read.
5	THRE	R/W	1	Transmitter Holding Register Empty. This bit indicates that the THR register is empty and may receive another character. Reset whenever THR is written to.
6	TEMT	R/W	1	Transmitter Empty. This bit is set to 1 when the Transmitter Holding Register (THR) and the Transmitter Shift Register are both empty. It is reset whenever THR is written to, and remains low until the character is transferred out of the TXD pin.
7	ERFIFO	R/W	0	FIFO Error. This bit is set to 1 if the receiver FIFO is full and another character is received.

5.10 Modem Status Register (MSR)

The Modem Status Register holds the current status of the DSR pin:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
MSR	0038	R/W	DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	DCTS	R	-	Delta clear to send.
1	DDSR	R	-	Delta DSR. This bit indicates that the DSR pin has changed state since the last time it was read. Not used on this board.
2	TERI	R	-	Trailing edge ring indicator. Not used on this board.
4	CTS	R	-	Clear to send. Reflects status of CTS pin on serial interfaces used on this board.
5	DSR	R	-	Data Set Ready. This bit always reflects the value of the DSR pin.Not used on this board.
6	RI	R	-	Ring indicator. Not used on this board.
7	RESV	R	-	Data carrier direct. Not used on this board.

5.11 Scratch Registers (SCR)

The Scratch Register holds the a read/write byte that affects no operations in the UART:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
SCR	003C	R/W	D7	D6	D5	D4	D3	D2	D1	D0

5.12 Divisor Latch Registers (DLL and DLM)

These registers control the Baud Rate Generator divisor, and are only accessible when Bit 7 (DLAB) in the LCR registers are set.

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
DLL	0020	R/W[1]	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0
DLM	0024	R/W[1]	DL15	DL14	DL13	DL12	DL11	DL10	DL9	DL8

Note:

1. Accessible only when LCR[7]=1.

The baud rate generator can use a 1.8432, 2.4576, or 3.072 MHz input clock. This clock is input on the SCLK pin and is used by both the Host and Video UARTs. With these frequencies, standard bit rates from 50 to 38.5K baud are available. Divisors for some popular baud rates are shown below:

Baud Rate	1.8432 MHz	2.4576 MHz	3.072 MHz
1200	96	128	160
2400	48	64	80
9600	12	16	20
19200	6	8	10
38400	3	4	5

5.13 Parallel Interface

(200 0060 to 200 007C)

5.14 Register Overview

Parallel Port Logic Register contents are:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
PDRW	0060	R/W	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
PSR	0064	R	-BSY	-ACK	PE	SLCT	-ERR	1	1	1
PCR	0068	R/W	1	1	DIR	ENIRQ	SLIN	-INIT	AFD	STB
GPIO	006C	R/W	GOUT7	GOUT6	GOUT5	GOUT4	GIN3	GIN2	GIN1	GIN0

5.15 Parallel Data Read and Write Registers (PDRW)

A single address is used for these two registers - one for reads and one for writes. A read from PDR reflects the current state of the Printer Data Port (PRD[7:0]) pins, while a write to PDW sets the state of the Printer Data Port pins (if the port is set to output).

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
PDR	0060	R	PDI7	PDI6	PDI5	PDI4	PDI3	PDI2	PDI1	PDI0
PDW	0060	W	PDO7	PDO6	PDO5	PDO4	PDO3	PDO2	PDO1	PDO0

Detailed Bit Definition of the PDR is:

Bit	Name	R/W	Reset	Use
0	PDI0	R	0	Printer Data Port Input Bit 0
				. . .
7	PDI7	R	0	Printer Data Port Input Bit 7

The PDW register is not normally used in data transfers, but it is useful in testing and in customer-specific applications.

Detailed Bit Definition of the PDW is:

Bit	Name	R/W	Reset	Use
0	PDO0	W	0	Printer Data Port Output Bit 0
				. . .
7	PDO7	W	0	Printer Data Port Output Bit 7

5.16 Parallel Status Register (PSR)

This register senses the status of the handshake signals from the host computer:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
PSR	0064	R	-BSY	-ACK	PE	SLCT	-ERR	1	1	1

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0-2	resv	R		Always read as 1
3	-ERR	R		Status of ERR pin
4	SLCT	R		Status of SLCT pin
5	PE	R		Status of PE pin
6	-ACK	R		Status of ACK pin
7	-BSY	R		Status of BSY pin

5.17 Parallel Control Register (PCR)

This register controls printer status that is returned to the host computer.

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
PCR	0068	R/W	1	1	DIR	ENIRQ	SLIN	-INIT	AFD	STB

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0	-STB	R/W	0	1=STB pin low
1	-AFD	R/W	0	1=AFD pin low
2	-INIT	R/W	0	1=INIT pin high
3	SLIN	R/W	0	1=SLIN pin high
4	ENIRQ	R/W	0	1=Enable interrupt from the ACK signal asserted low
5	DIR	R/W	0	1=Ouput buffers are disabled allowing PD bus to be input.
6-7	RESV			

5.18 General-Purpose Input/Output Register (GPID)

The GPID register is used to control the four LEDs. On reset, all LEDs are on.

Revision ID Register contents are:

Reg	Addr	Type	D7	D6	D5	D4	D3	D2	D1	D0
GPIO	006C	W/R	GOUT7	GOUT6	GOUT5	GOUT4	GIN3	GIN2	GIN1	GIN0

Detailed Bit Definition is:

Bit	Name	R/W	Reset	Use
0-3	GIN	R		4 input bits
4	GOUT	W	0	LED1
5	GOUT	W	0	LED1
6	GOUT	W	0	LED1
7	GOUT	W	0	LED1

APPENDIX A. BOARD OPTIONS

VY86PID Options

Jumper Function		Normal Postion		Option	
JP1	Oscillator Disconnect	IN	MEMC connect to OSC1	Out	External Oscillator Connected
JP2	FCLK Select	1-2	FCLK=OSC2 divided by 2	2-3	FCLK=OSC3
JP8	SNA Select	2-3	Asyncronous FCLK to MCLK	1-2	Syncronous FCLK to MCLK

EPROM Options

			27C080	27C040	27C020	27C010	27C512	27C256		
JP3	Pin 3	[SA17]	1-2	1-2	1-2	1-2	1-2	2-3	1-2=LA17	2-3=VCC
JP4	Pin 3	[SA17]	1-2	1-2	1-2	1-2	1-2	2-3	1-2=LA17	2-3=VCC
JP5	Pin 3	[SA17]	1-2	1-2	1-2	1-2	1-2	2-3	1-2=LA17	2-3=VCC
JP6	Pin 3	[SA17]	1-2	1-2	1-2	1-2	1-2	2-3	1-2=LA17	2-3=VCC
JP7	Pin 3	[SA17]	1-2	1-2	1-2	1-2	1-2	2-3	1-2=LA17	2-3=VCC

APPENDIX B. INTERRUPT CONTROLLER (INTC)

INTC PGA - Address Decode and Interrupt Registers

Inputs	Source	Pin #	Description
IOCS	MEMC PGA	40	Asserted in address range 200 000 thru 2FF FFFF (16 MBytes)
IORD	MEMC PGA	41	160 ns low true strobe
IOWR	MEMC PGA	42	160 ns low true strobe
NRESET	System	51	Power On Reset from capacitor and switch (and HC14 Schmidt trigger)
PANIC	Button	55	Panic Button interrupt
MCLK	MEMC PGA	19	MEMORY CLOCK - Address bits are latched during neg level
LA[24:18]	HC573	14-9	Latched Address bits 24:18
LA[6:0]	HC573	26-21	Latched Address bits 6 to 0
NRW	ARM600	38	Not Read Write signal
NBW	ARM600	39	Not Byte Word signal
IRQ[0]	16C551	49	Serial Init
TIMETST		48	Test Timer
IRQ[2]	16C551	47	Parallel Interrupt
IRQ[6:3]		46-43	Expansion Interrupts
FIQ[7:0]	16C551	60-67	Fast Interrupt Inputs
Bidirect	BD[7:0]	34-27	Buffered Data Bus

Output	Destination	Pin #	Description
BE[3:0]	Expansion	2-5	Byte enable signals for expansion Slot
IOW	Expansion	56	Expansion Connector IOW pin
IOR	Expansion	57	Expansion Connector IOR pin
MEMW	Expansion	58	Expansion Connector MEMW pin
MEMR	Expansion	59	Expansion Connector MEMR pin
CS0	16C551	6	Serial Port Select
CS1		7	Not used for anything
CS2		8	16C551 Parallel Port Select
BPCS	Expansion	68	Break Point Expansion Select
IRQ	ARM600	37	Normal Interrupt
FIQ	ARM600	36	Fast Interrupt

APPENDIX C. MEMORY CONTROLLER (MEMC)

MEMC PGA for ARM600, ARM60, ARM61

Inputs	Source	Pin #	Description
CLOCK	XTAL	16	50 MHz master clock
TESTRST	Testpin	49	High resets chip for simulation purposes
RESET	INTC PGA	51	Low is Reset of chip that enables ROM in low memory
A[25:0]	ARM600	47-36 34-21	Raw Address bits from ARM600 processor
NRW	ARM600	12	Not Read/ Write 0 = Read
NBW	ARM600	13	Not Byte/ Word 0 = Byte Write
NMREQ	ARM600	59	Memory Request
MCLKIN	MCLK	17	Return of MCLK for speed compensation
NHALT	P1	11	When low forces NWAIT low

Outputs	Destination	Pin #	Description
FCLK	ARM600	14	Processor Clock @ 25 MHz
MCLK	ARM600	15	Memory Access Clock @ 12.5 MHz
NWAIT	ARM600	58	Forces the processor to wait while low
MA[10:0]	DRAM	60-68 2-3	Memory addresses that are multiplexed for Row and Column Addresses
WE[3:0]	DRAM	4-7	Memory Write Strobes
RAS[1:0]	DRAM	8-9	Row Address Strobes
CAS[1:0]	DRAM	10	Column Address Strobes
IOCS	INTC PGA	57	Decode of IO space cycle
IOWR	Internal IO	56	Attached peripheral Write
IORD	Internal IO	55	Attached peripheral Read
ROMOE	EPROM	48	Decode and output enable for ROM and or EPROM

APPENDIX C. MEMORY CONTROLLER (Cont.)

Memory Address

MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0

DRAM ROW

A22	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11

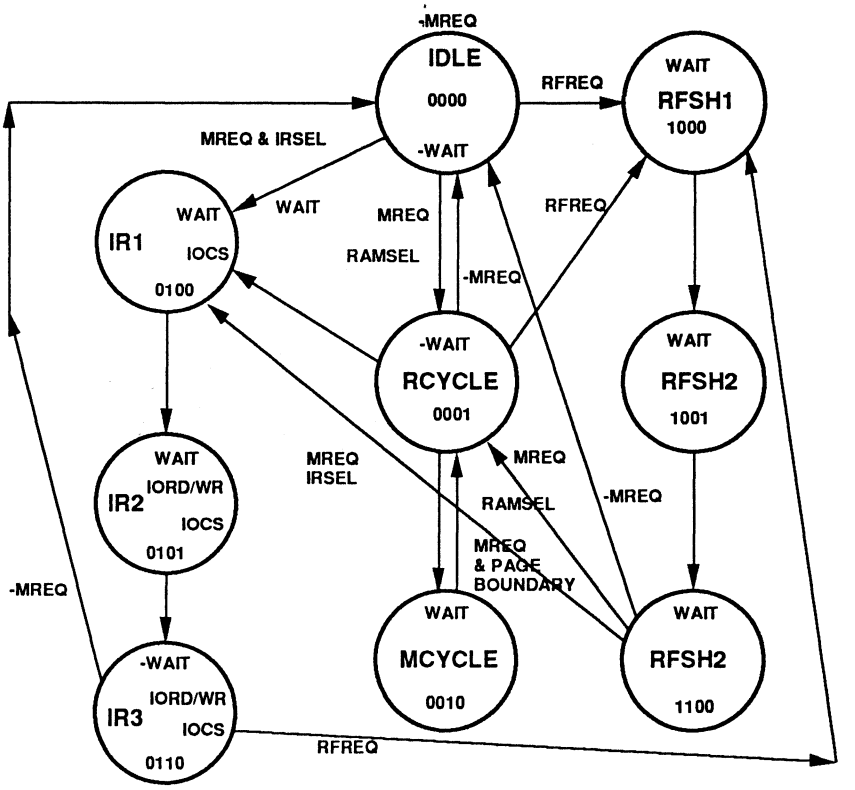
DRAM COL

A23	A21	A10	A9	A8	A7	A6	A5	A4	A3	A2

SELECT AREA	A[25:24]
DRAM0	00
DRAM1	01
I/O	10
ROM	11

APPENDIX C. MEMORY CONTROLLER (Cont.)

MEMC2 Memory Controller State Diagram



APPENDIX C. MEMORY CONTROLLER (Cont.)

Tabular form of MEMC2 Memory Controller State Diagram

Pres. State	Inputs					Next State	Outputs					
Label #	L[1] MREQ	R[2] AMRQ	I[3] RRQ	R[4] FRQ	M[5] ISS	Label #	NWAIT	DRAS	RAS	LCAS	CAS	IOSB
Idle 0000	0	-	-	0	-	Idle 0000	0	0	0	0	0	0
Idle 0000	1	1	-	0	-	Rcyc 0001	0	1	0	0	0	0
Idle 0000	1	-	1	0	-	IR1 0100	0	0	0	0	0	0
Idle 0000	-	-	-	1	-	RF1 1000	0	0	0	0	0	0
Rcyc 0001	0	-	-	0	-	Idle 0000	0	0	1	0	1	0
Rcyc 0001	1	1	-	0	0	Rcyc 0001	0	0	1	0	1	0
Rcyc 0001	-	-	-	1	-	RF1 1000	0	0	1	0	1	0
Rcyc 0001	1	1	-	0	1	Mcyc 0010	1	0	0	0	0	0
IR1 0100	-	-	-	-	-	IR2 0101	1	0	0	0	0	0
IR2 0100	-	-	-	-	-	IR3 0110	1	0	0	0	0	1
IR3 0110	1	-	1	0	-	IR1 0100	0	0	0	0	0	1
IR3 0110	0	-	-	0	-	Idle 0000	0	0	0	0	0	1
IR3 0110	-	-	-	1	-	RF1 1000	0	0	0	0	0	1
RF1 0100	-	-	-	-	-	RF2 1001	1	0	0	1	0	0
RF2 0101	-	-	-	-	-	RF3 1010	1	0	1	0	0	0
RF3 0110	0	-	-	-	-	Idle 0000	1	0	0	0	0	0
RF3 0110	1	1	-	-	-	Rcyc 0001	1	1	0	0	0	0
RF3 0110	1	-	1	-	-	IR1 0100	1	0	0	0	0	0
Mcyc 0010	-	-	-	-	-	Rcyc 0001	1	1	0	0	0	0

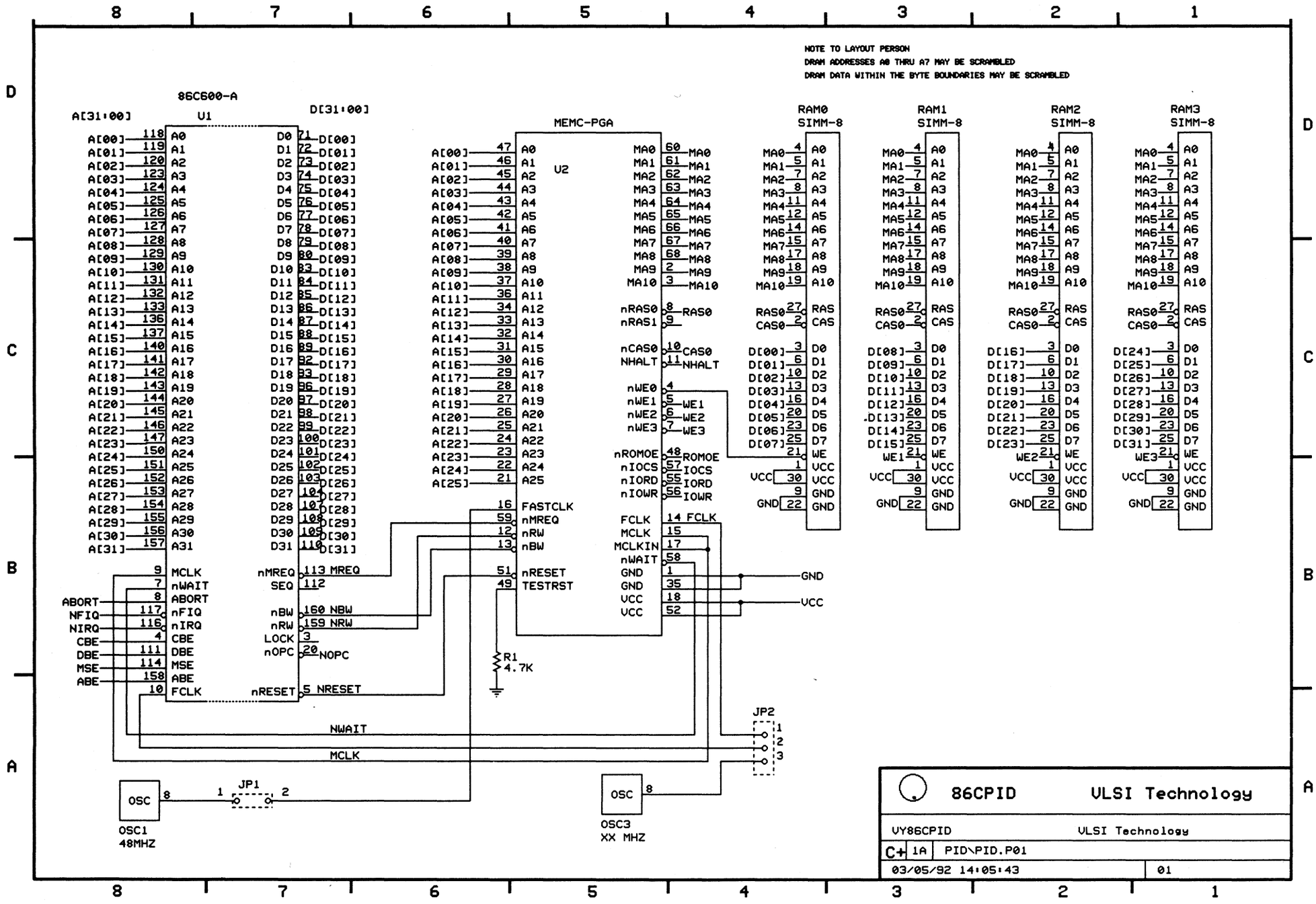
Notes:

1. LMREQ — Latched NMREQ on positive edge of MCLK and NWAIT
2. RAMRQ — RAM Request (not Reset mode and A25 low)
3. IRRQ — I/O or ROM (Reset mode or A25 high)
4. RFRQ — Refresh Request
5. MISS — Last address was on page boundary (RAS needs to be regenerated)

APPENDIX D. SCHEMATICS

Four schematics are included in this appendix and can be found in the following pages.

- PID Schematics
- Cable Schematic (for IBM PC™ and SUN SPARCStation2™)
- Memory Controller (MEMC2) Schematics
- Interrupt Controller (INTC) Schematics


NOTE TO LAYOUT PERSON
DRAM ADDRESSES A0 THRU A7 MAY BE SCRAMBLED
DRAM DATA WITHIN THE BYTE BOUNDARIES MAY BE SCRAMBLED
86C600-A
U1
A[31:00]
D[31:00]
MEMC-PGA
U2
RAM0 SIMM-8
RAM1 SIMM-8
RAM2 SIMM-8
RAM3 SIMM-8
MCLK
nWAIT
ABORT
nFIQ
nIRQ
CBE
DBE
MSE
ABE
FCLK
nMREQ
SEQ
nBW
nRW
LOCK
nOPC
nRESET
FASTCLK
nRW
nBW
nRESET
TESTRST
nRAS0
nRAS1
nCAS0
NHALT
nWE0
nWE1
nWE2
nWE3
nROMOE
nIOCS
nIORD
nIOWR
MCLKIN
GND
VCC
R1
4.7K
NWAIT
MCLK
JP1
JP2
OSC
OSC1
48MHZ
OSC3
XX MHZ
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VLSI Technology
VY86CPID
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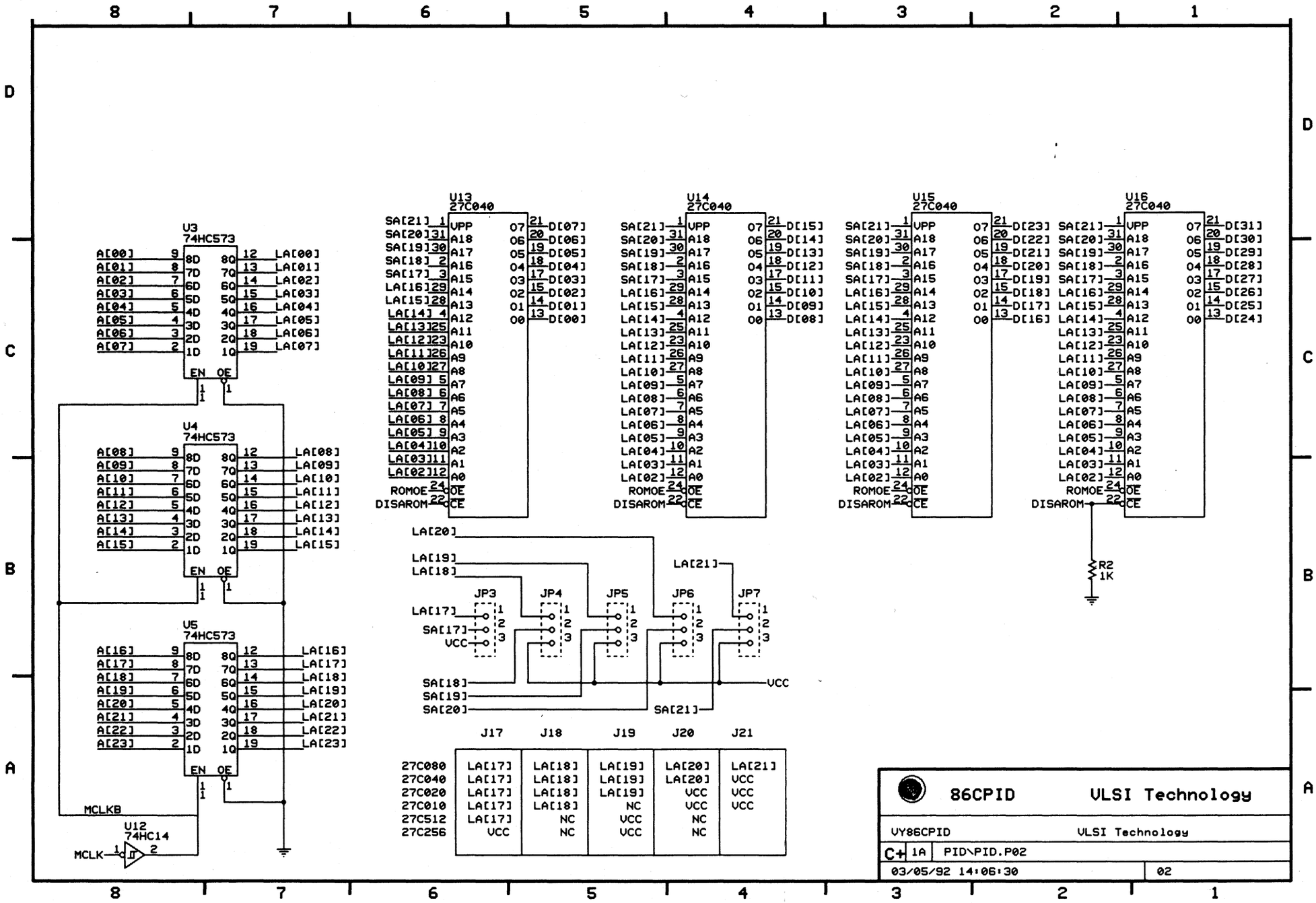
U3
74HC573
A[00] A[01] A[02] A[03] A[04] A[05] A[06] A[07]
LA[00] LA[01] LA[02] LA[03] LA[04] LA[05] LA[06] LA[07]
EN OE
U4
74HC573
A[08] A[09] A[10] A[11] A[12] A[13] A[14] A[15]
LA[08] LA[09] LA[10] LA[11] LA[12] LA[13] LA[14] LA[15]
EN OE
U5
74HC573
A[16] A[17] A[18] A[19] A[20] A[21] A[22] A[23]
LA[16] LA[17] LA[18] LA[19] LA[20] LA[21] LA[22] LA[23]
EN OE
MCLKB
U12
74HC14
MCLK
U13
27C040
SA[21] SA[20] SA[19] SA[18] SA[17] LA[16] LA[15] LA[14] LA[13] LA[12] LA[11] LA[10] LA[09] LA[08] LA[07] LA[06] LA[05] LA[04] LA[03] LA[02]
VPP A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D[07] D[06] D[05] D[04] D[03] D[02] D[01] D[00]
ROMOE OE
DISAROM CE
U14
27C040
SA[21] SA[20] SA[19] SA[18] SA[17] LA[16] LA[15] LA[14] LA[13] LA[12] LA[11] LA[10] LA[09] LA[08] LA[07] LA[06] LA[05] LA[04] LA[03] LA[02]
VPP A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D[15] D[14] D[13] D[12] D[11] D[10] D[09] D[08]
ROMOE OE
DISAROM CE
U15
27C040
SA[21] SA[20] SA[19] SA[18] SA[17] LA[16] LA[15] LA[14] LA[13] LA[12] LA[11] LA[10] LA[09] LA[08] LA[07] LA[06] LA[05] LA[04] LA[03] LA[02]
VPP A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D[23] D[22] D[21] D[20] D[19] D[18] D[17] D[16]
ROMOE OE
DISAROM CE
U16
27C040
SA[21] SA[20] SA[19] SA[18] SA[17] LA[16] LA[15] LA[14] LA[13] LA[12] LA[11] LA[10] LA[09] LA[08] LA[07] LA[06] LA[05] LA[04] LA[03] LA[02]
VPP A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D[31] D[30] D[29] D[28] D[27] D[26] D[25] D[24]
ROMOE OE
DISAROM CE
R2
1K
LA[20]
LA[19]
LA[18]
LA[21]
JP3 JP4 JP5 JP6 JP7
LA[17]
SA[17]
VCC
SA[18]
SA[19]
SA[20]
SA[21]
VCC
J17 J18 J19 J20 J21
27C080 LA[17] LA[18] LA[19] LA[20] LA[21]
27C040 LA[17] LA[18] LA[19] LA[20] VCC
27C020 LA[17] LA[18] LA[19] VCC VCC
27C010 LA[17] LA[18] NC VCC VCC
27C512 LA[17] NC VCC NC
27C256 VCC NC VCC NC
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VLSI Technology
VY86CPID
VLSI Technology
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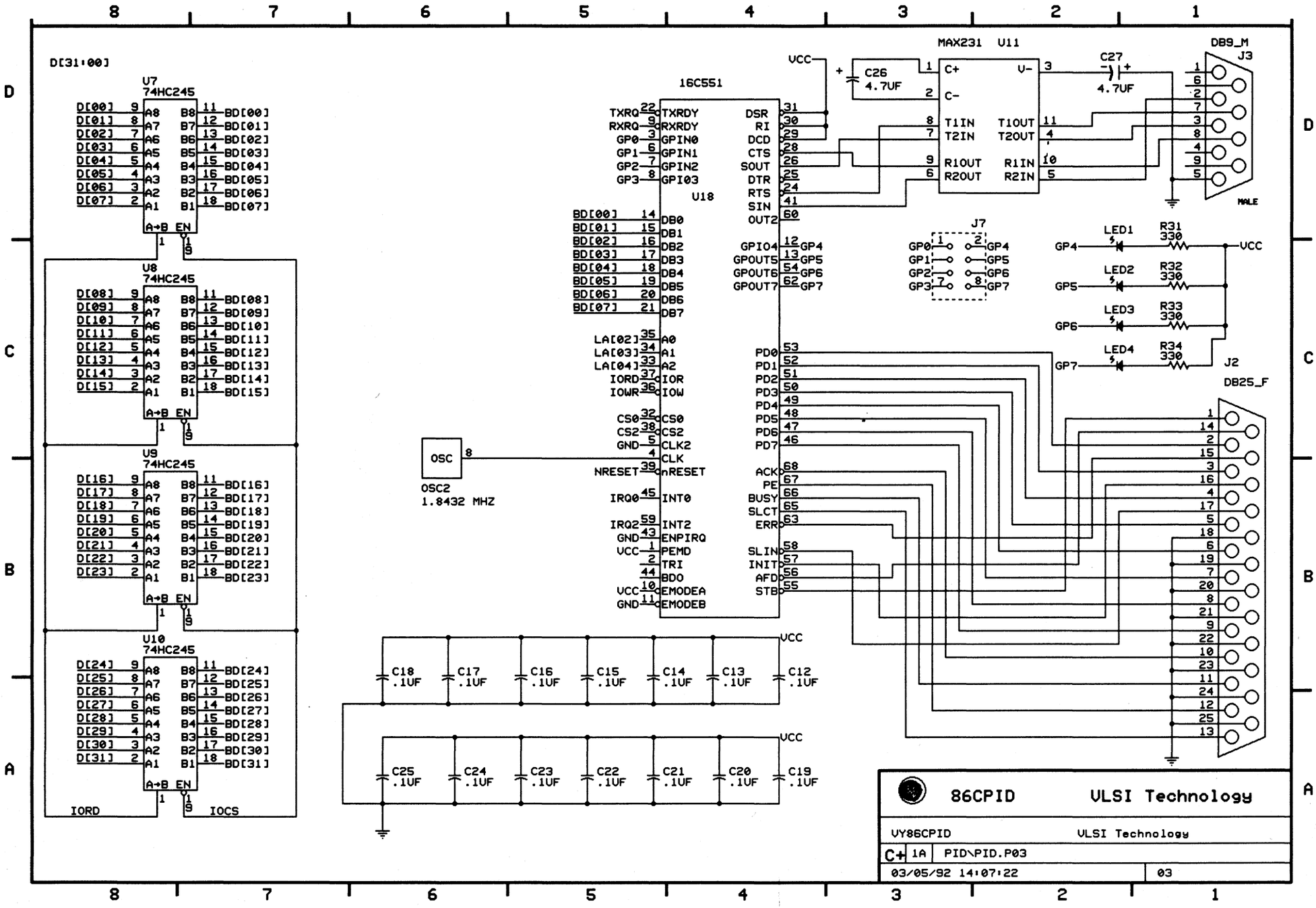
02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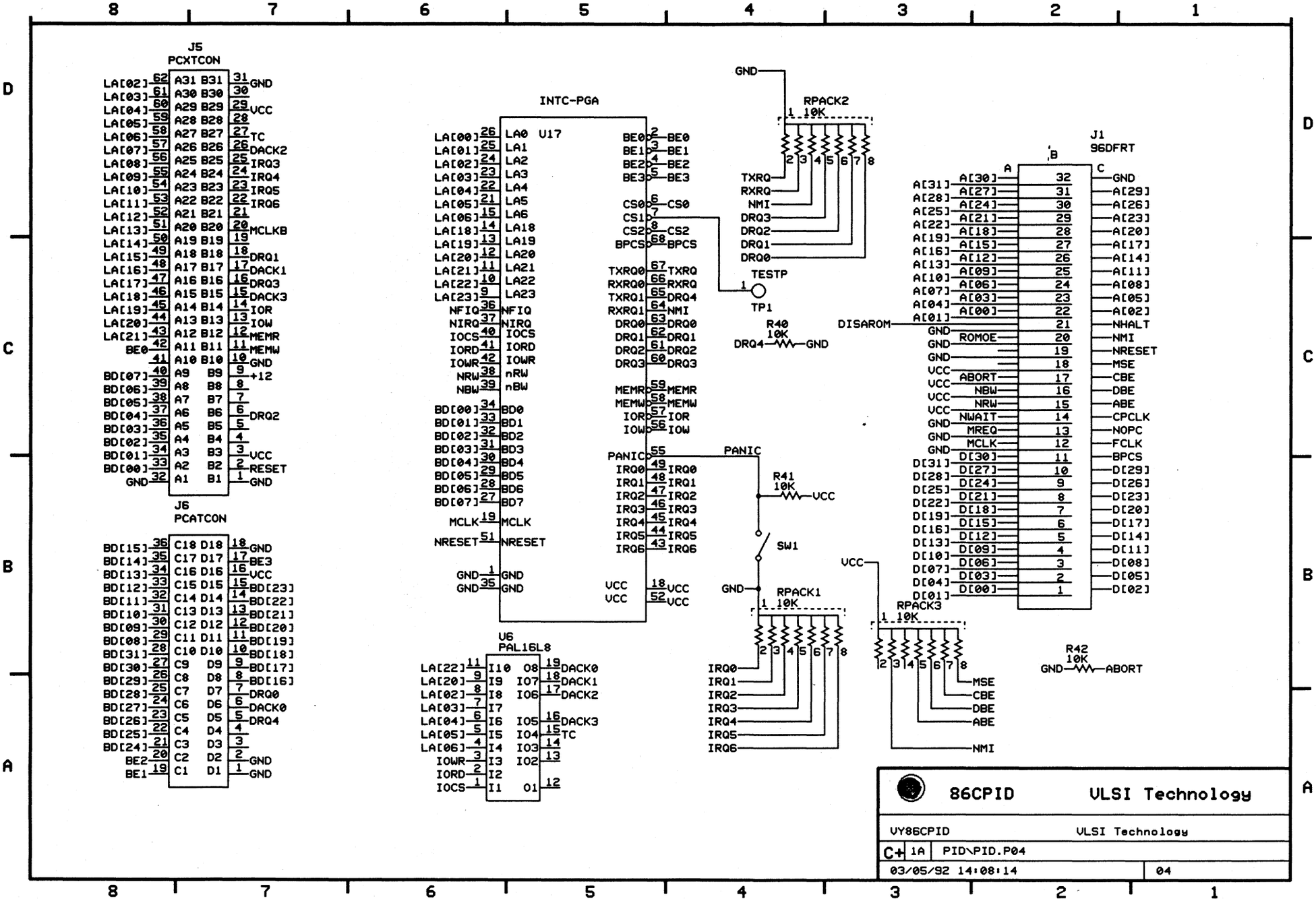
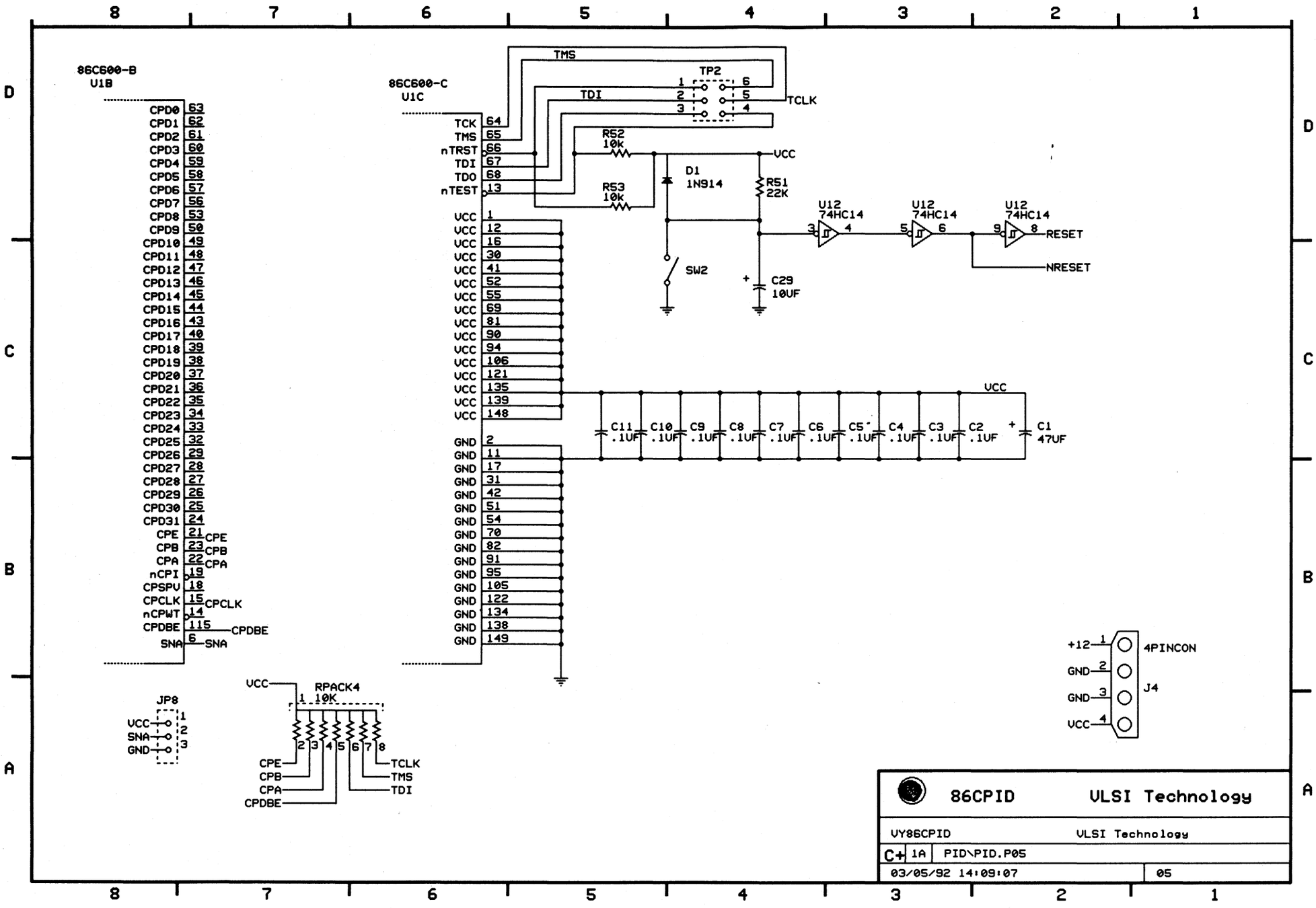
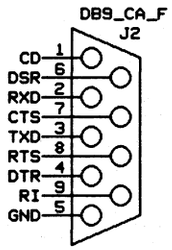
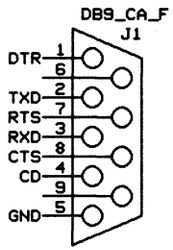
74HC245
U8
74HC245
U9
74HC245
U10
74HC245
A→B EN
IORD
IOCS
16C551
U18
TXRQ
RXRQ
GP0
GP1
GP2
GP3
TXRDY
RXRDY
GPIN0
GPIN1
GPIN2
GPI03
DSR
RI
DCD
CTS
SOUT
DTR
RTS
SIN
OUT2
BD[00]
BD[01]
BD[02]
BD[03]
BD[04]
BD[05]
BD[06]
BD[07]
DB0
DB1
DB2
DB3
DB4
DB5
DB6
DB7
GPIO4
GPOUT5
GPOUT6
GPOUT7
LA[02]
LA[03]
LA[04]
IORD
IOWR
A0
A1
A2
IOR
IOW
CS0
CS2
GND
CLK2
CLK
NRESET
nRESET
IRQ0
INT0
IRQ2
INT2
ENPIRQ
PEMD
TRI
BDO
EMODEA
EMODEB
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
ACK
PE
BUSY
SLCT
ERR
SLIN
INIT
AFD
STB
OSC
OSC2
1.8432 MHZ
VCC
MAX231 U11
C+
C-
V-
T1IN
T2IN
T1OUT
T2OUT
R1OUT
R2OUT
R1IN
R2IN
C26
4.7UF
C27
4.7UF
DB9_M
J3
MALE
J7
GP0
GP1
GP2
GP3
GP4
GP5
GP6
GP7
LED1
LED2
LED3
LED4
R31
R32
R33
R34
330
J2
DB25_F
C18 .1UF
C17 .1UF
C16 .1UF
C15 .1UF
C14 .1UF
C13 .1UF
C12 .1UF
C25 .1UF
C24 .1UF
C23 .1UF
C22 .1UF
C21 .1UF
C20 .1UF
C19 .1UF
86CPID
VLSI Technology
VY86CPID
VLSI Technology
C+ 1A
PID\PID.P03
03/05/92 14:07:22
03


J5
PCXTCON
J6
PCATCON
INTC-PGA
U17
V6
PAL16L8
RPACK2
RPACK1
RPACK3
R40
R41
R42
SW1
TESTP
TP1
J1
96DFRT
86CPID
VLSI Technology
VY86CPID
PID\PID.P04
03/05/92 14:08:14
04


86C600-B
U1B
CPD0 63
CPD1 62
CPD2 61
CPD3 60
CPD4 59
CPD5 58
CPD6 57
CPD7 56
CPD8 53
CPD9 50
CPD10 49
CPD11 48
CPD12 47
CPD13 46
CPD14 45
CPD15 44
CPD16 43
CPD17 40
CPD18 39
CPD19 38
CPD20 37
CPD21 36
CPD22 35
CPD23 34
CPD24 33
CPD25 32
CPD26 29
CPD27 28
CPD28 27
CPD29 26
CPD30 25
CPD31 24
CPE 21 CPE
CPB 23 CPB
CPA 22 CPA
nCPI 19
CPSPU 18
CPCLK 15 CPCLK
nCPWT 14
CPDBE 115 CPDBE
SNA 6 SNA
86C600-C
U1C
TCK 64
TMS 65
nTRST 66
TDI 67
TDO 68
nTEST 13
VCC 1
VCC 12
VCC 16
VCC 30
VCC 41
VCC 52
VCC 55
VCC 69
VCC 81
VCC 90
VCC 94
VCC 106
VCC 121
VCC 135
VCC 139
VCC 148
GND 2
GND 11
GND 17
GND 31
GND 42
GND 51
GND 54
GND 70
GND 82
GND 91
GND 95
GND 105
GND 122
GND 134
GND 138
GND 149
TMS
TDI
TP2
TCLK
R52 10k
R53 10k
VCC
D1 1N914
R51 22K
SW2
C29 10UF
U12 74HC14
RESET
NRESET
C11 .1UF
C10 .1UF
C9 .1UF
C8 .1UF
C7 .1UF
C6 .1UF
C5 .1UF
C4 .1UF
C3 .1UF
C2 .1UF
C1 47UF
JP8
VCC
SNA
GND
RPACK4 10K
CPE
CPB
CPA
CPDBE
TCLK
TMS
TDI
+12
GND
GND
VCC
4PINCON
J4
86CPID
VLSI Technology
VY86CPID
VLSI Technology
C+ 1A PID\PID.P05
03/05/92 14:09:07
05



PC SIDE DB9 FEMALE



RC-600 SIDE DB9 FEMALE

PC	RC-600
1 CD	1 DTR
2 RXD	2 TXD
3 TXD	3 RXD
4 DTR	4 CD
5 GND	5 GND
6 DSR	6 NC
7 CTS	7 RTS
8 RTS	8 CTS
9 RI	9 NC

SIGNALS REFERED FROM PC SIDE

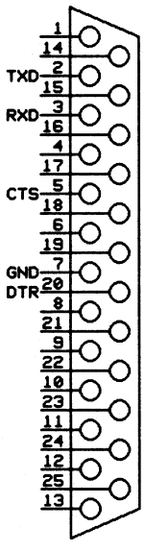
PC may require pins 1 and 4 connected on PID side

STANDARD NULL MODEM CABLE

86CPID	VLSI Technology	
100-0001-001	SCHEMA III	
C+ 1A	PID_R2\PC_CABL.P01	
07/25/92 23:36:19		01

P1

DB25_C_M

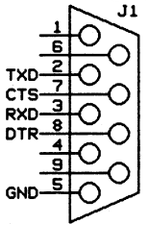


SUN SIDE DB 25 MALE

SIGNALS NAMES FROM SUN SIDE

DB9_CA_F

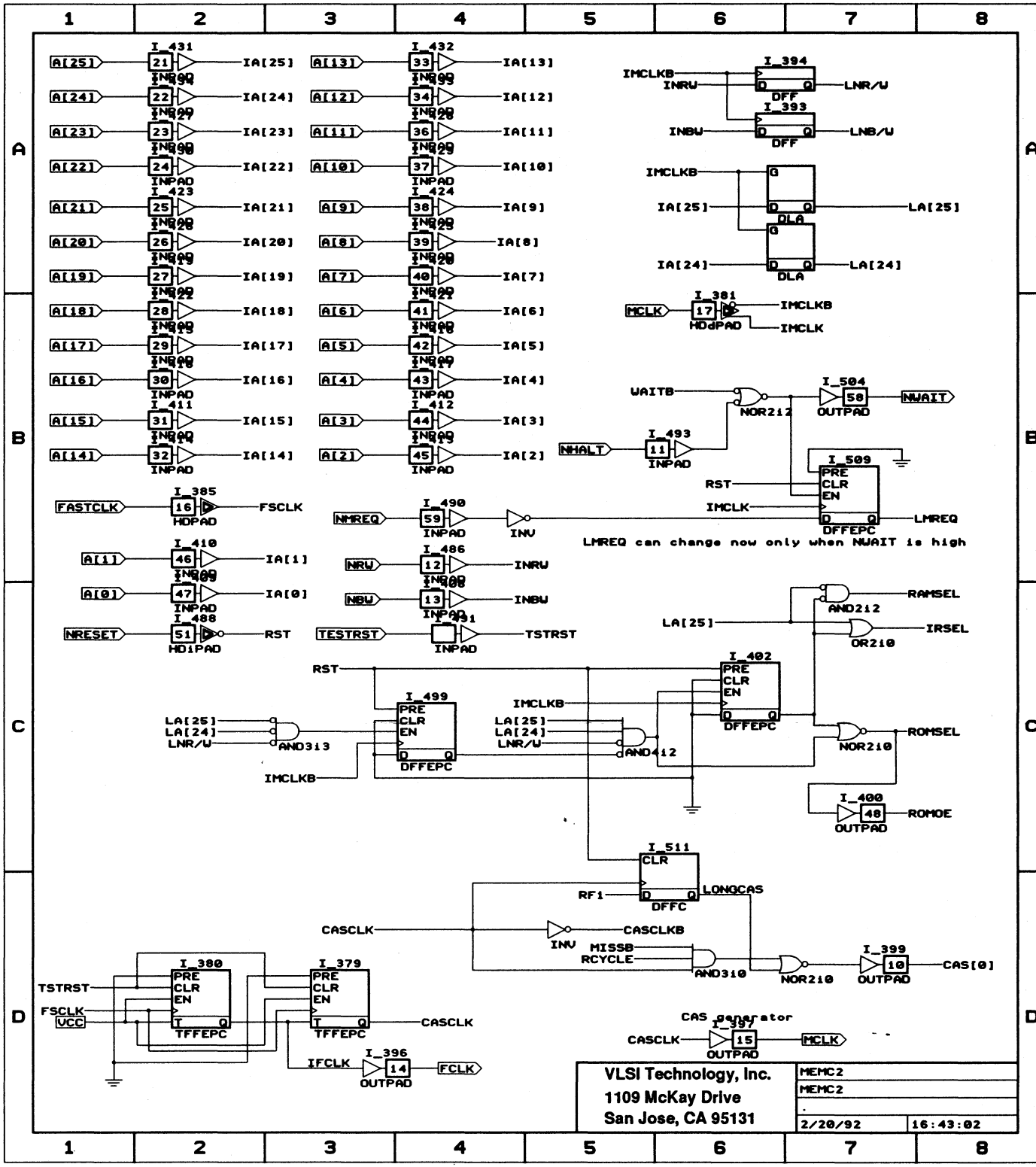
J1

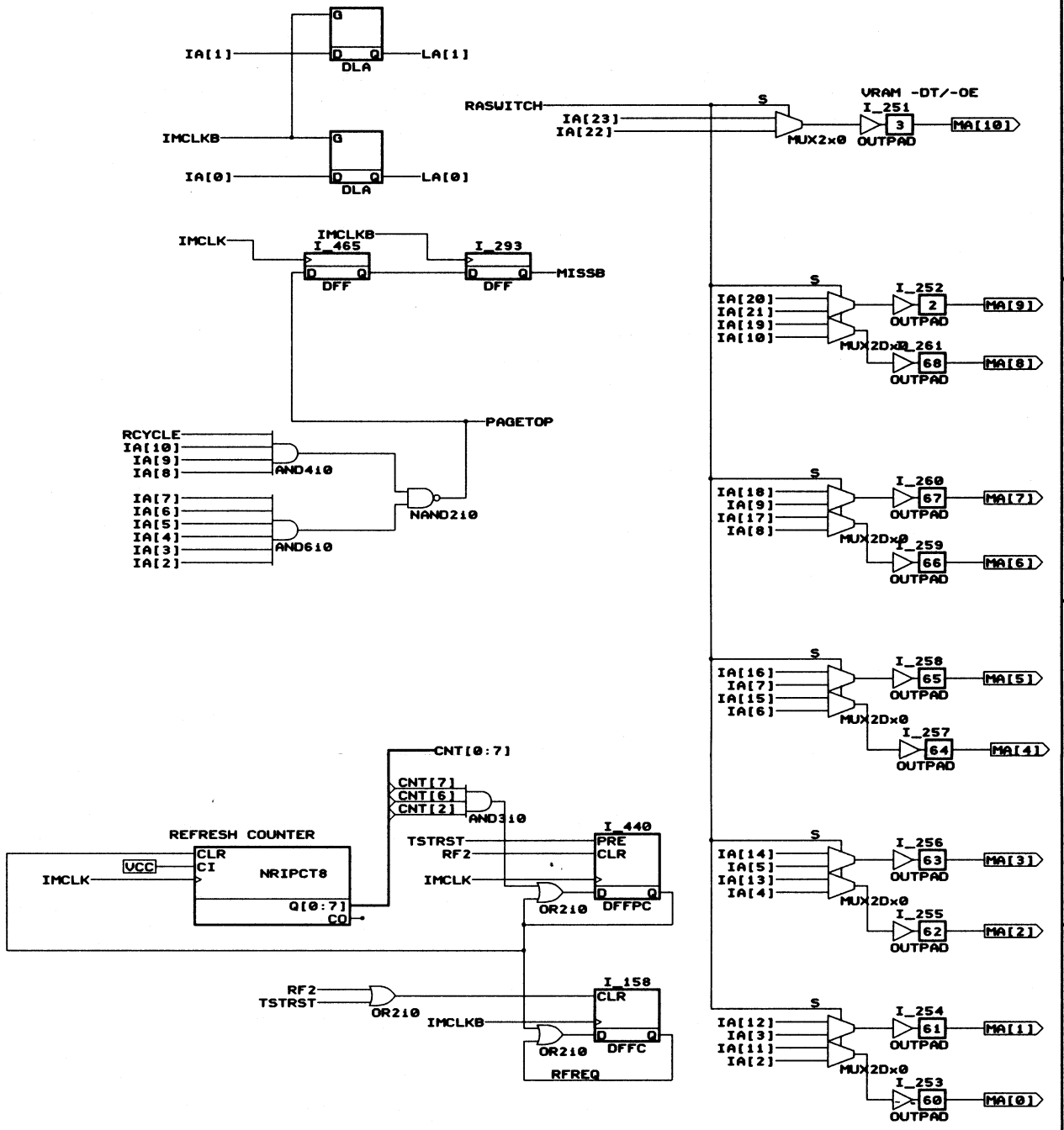


PID SIDE DB9 FEMALE

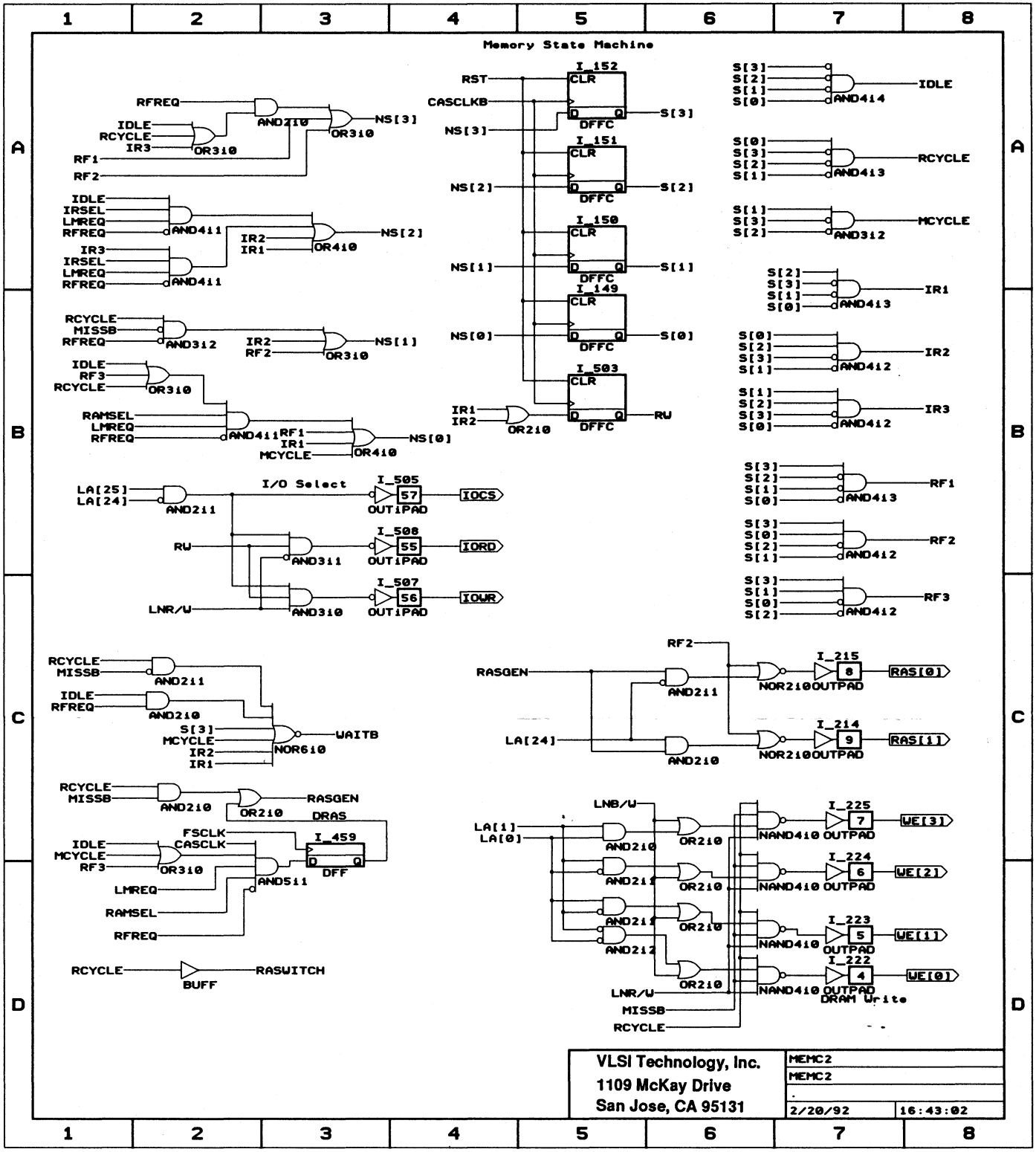
SUN	PID
2 TXD	2 RXD
3 RXD	3 TXD
20 DTR	8 CTS
5 CTS	7 RTS
7 GND	5 GND

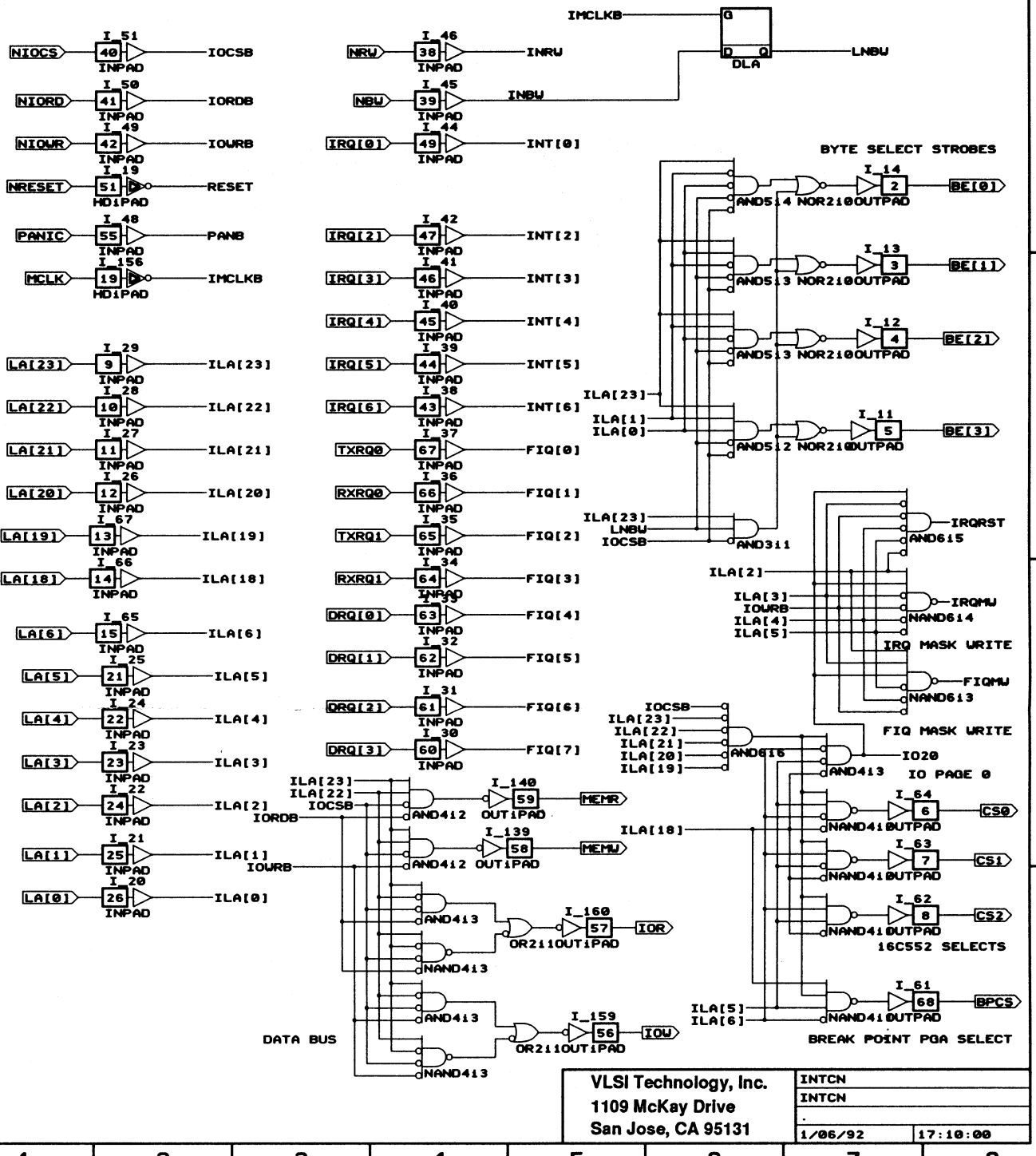
86CPID	VLSI Technology	
100-0001-001	SCHEMA III	
C+ 1A	PID_R2\SUN_CABL.P01	
07/25/92 23:37:39		01

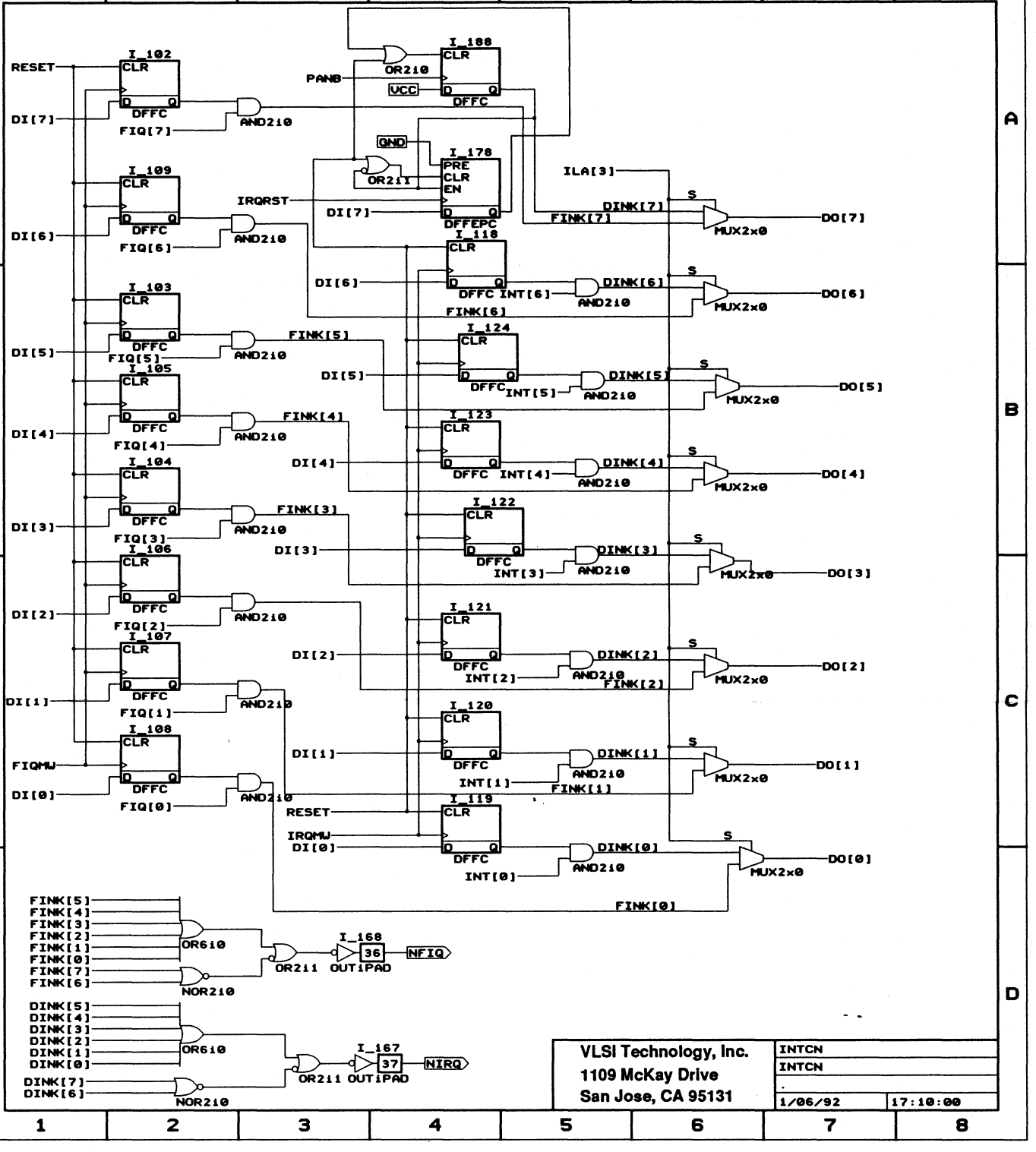

A[25]
I_431
21
INPAD
IA[25]
A[24]
22
IA[24]
A[23]
23
IA[23]
A[22]
24
IA[22]
A[21]
I_423
25
IA[21]
A[20]
26
IA[20]
A[19]
27
IA[19]
A[18]
28
IA[18]
A[17]
29
IA[17]
A[16]
30
IA[16]
A[15]
I_411
31
IA[15]
A[14]
32
IA[14]
A[13]
I_432
33
IA[13]
A[12]
34
IA[12]
A[11]
36
IA[11]
A[10]
37
IA[10]
A[9]
I_424
38
IA[9]
A[8]
39
IA[8]
A[7]
40
IA[7]
A[6]
41
IA[6]
A[5]
42
IA[5]
A[4]
43
IA[4]
A[3]
44
IA[3]
A[2]
45
IA[2]
IMCLKB
INRW
I_394
DFF
LNR/W
INBW
I_393
LNB/W
IA[25]
DLA
LA[25]
IA[24]
LA[24]
MCLK
I_381
17
HDdPAD
IMCLK
WAITB
NOR212
I_504
58
OUTPAD
NWAIT
NHALT
I_493
11
I_509
PRE
CLR
EN
RST
D
Q
DFFEPC
LMREQ
LMREQ can change now only when NWAIT is high
FASTCLK
I_385
16
HDPAD
FSCLK
NMREQ
I_490
59
INV
A[1]
I_410
46
IA[1]
A[0]
47
IA[0]
NRESET
I_488
51
HDiPAD
NRW
I_486
12
INRW
NBW
13
INBW
TESTRST
I_491
TSTRST
AND212
RAMSEL
LA[25]
OR210
IRSEL
I_402
ROMSEL
NOR210
I_400
40
ROMOE
I_499
LA[25]
LA[24]
LNR/W
AND313
AND412
I_511
CLR
RF1
LONGCAS
DFFC
CASCLK
CASCLKB
MISSB
RCYCLE
AND310
I_399
10
CAS[0]
I_380
I_379
TSTRST
FSCLK
VCC
TFFEPC
CASCLK
IFCLK
I_396
14
FCLK
CAS generator
I_397
15
MCLK
VLSI Technology, Inc.
1109 McKay Drive
San Jose, CA 95131
MEMC2
MEMC2
2/20/92
16:43:02

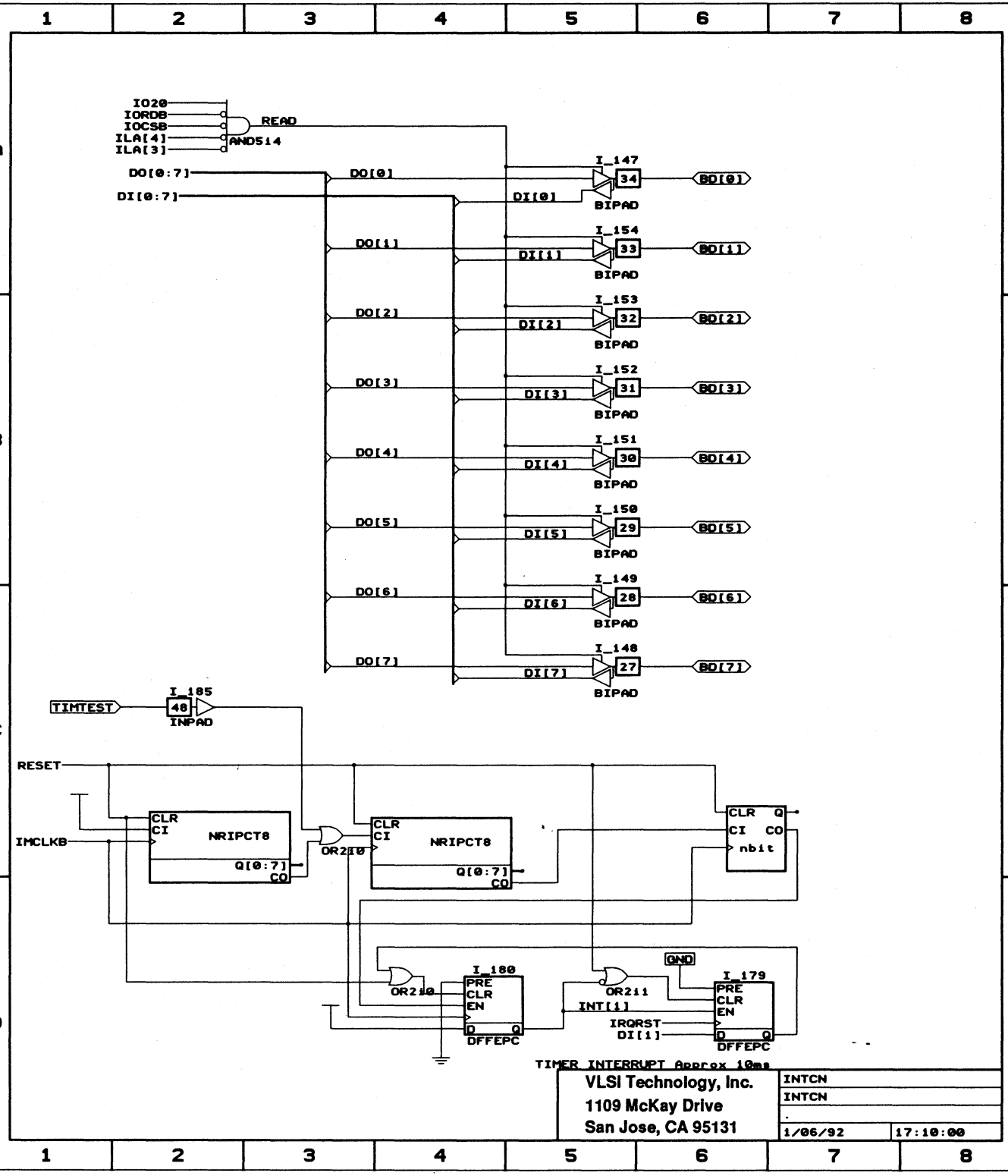


VLSI Technology, Inc. 1109 McKay Drive San Jose, CA 95131	MEMC2 MEMC2 . 2/20/92 16:43:02


Memory State Machine
RFREQ
IDLE
RCYCLE
IR3
RF1
RF2
AND2i0
OR3i0
NS[3]
IDLE
IRSEL
LMREQ
RFREQ
AND4i1
IR2
IR1
OR4i0
NS[2]
IR3
IRSEL
LMREQ
RFREQ
AND4i1
RCYCLE
MISSB
RFREQ
AND3i2
IR2
RF2
OR3i0
NS[1]
IDLE
RF3
RCYCLE
OR3i0
RAMSEL
LMREQ
RFREQ
AND4i1
RF1
IR1
MCYCLE
OR4i0
NS[0]
RST
CASCLKB
NS[3]
NS[2]
NS[1]
NS[0]
IR1
IR2
OR2i0
I_152
I_151
I_150
I_149
I_503
CLR
D
Q
DFFC
S[3]
S[2]
S[1]
S[0]
RW
S[3]
S[2]
S[1]
S[0]
AND4i4
IDLE
S[0]
S[3]
S[2]
S[1]
AND4i3
RCYCLE
S[1]
S[3]
S[2]
AND3i2
MCYCLE
S[2]
S[3]
S[1]
S[0]
AND4i3
IR1
S[0]
S[2]
S[3]
S[1]
AND4i2
IR2
S[1]
S[2]
S[3]
S[0]
AND4i2
IR3
S[3]
S[2]
S[1]
S[0]
AND4i3
RF1
S[3]
S[0]
S[2]
S[1]
AND4i2
RF2
S[3]
S[1]
S[0]
S[2]
AND4i2
RF3
I/O Select
LA[25]
LA[24]
AND2i1
I_505
57
OUTiPAD
IOCS
RW
AND3i1
I_508
55
OUTiPAD
IORD
LNR/W
AND3i0
I_507
56
OUTiPAD
IOWR
RCYCLE
MISSB
AND2i1
IDLE
RFREQ
AND2i0
S[3]
MCYCLE
IR2
IR1
NOR6i0
WAITB
RCYCLE
MISSB
AND2i0
OR2i0
RASGEN
DRAS
FSCLK
CASCLK
IDLE
MCYCLE
RF3
OR3i0
I_459
DFF
AND5i1
LMREQ
RAMSEL
RFREQ
RCYCLE
BUFF
RASWITCH
RF2
RASGEN
AND2i1
NOR2i0
OUTPAD
I_215
8
RAS[0]
LA[24]
AND2i0
NOR2i0
OUTPAD
I_214
9
RAS[1]
LNB/W
LA[1]
LA[0]
AND2i0
AND2i1
AND2i1
AND2i2
OR2i0
NAND4i0
OUTPAD
I_225
7
WE[3]
I_224
6
WE[2]
I_223
5
WE[1]
I_222
4
WE[0]
LNR/W
MISSB
RCYCLE
DRAM Write
VLSI Technology, Inc.
1109 McKay Drive
San Jose, CA 95131
MEMC2
MEMC2
2/20/92
16:43:02


IMCLKB
G
D
Q
DLA
LNBW
NIOCS
I_51
40
INPAD
IOCSB
NRW
I_46
38
INRW
NIORD
I_50
41
IORDB
NBW
I_45
39
INBW
NIOWR
I_49
42
IOWRB
IRQ[0]
I_44
49
INT[0]
NRESET
I_19
51
HDiPAD
RESET
BYTE SELECT STROBES
PANIC
I_48
55
PANB
I_42
47
IRQ[2]
INT[2]
MCLK
I_156
19
IMCLKB
I_41
46
IRQ[3]
INT[3]
I_40
45
IRQ[4]
INT[4]
I_14
2
BE[0]
AND514
NOR210OUTPAD
I_13
3
BE[1]
AND513
NOR210OUTPAD
I_12
4
BE[2]
AND513
NOR210OUTPAD
I_11
5
BE[3]
AND512
NOR210OUTPAD
LA[23]
I_29
9
ILA[23]
I_39
44
IRQ[5]
INT[5]
LA[22]
I_28
10
ILA[22]
I_38
43
IRQ[6]
INT[6]
ILA[23]
ILA[1]
ILA[0]
LA[21]
I_27
11
ILA[21]
I_37
67
TXRQ0
FIQ[0]
LA[20]
I_26
12
ILA[20]
I_36
66
RXRQ0
FIQ[1]
ILA[23]
LNBW
IOCSB
AND311
LA[19]
I_67
13
ILA[19]
I_35
65
TXRQ1
FIQ[2]
IRQRST
AND615
LA[18]
I_66
14
ILA[18]
I_34
64
RXRQ1
FIQ[3]
ILA[2]
ILA[3]
IOWRB
ILA[4]
ILA[5]
IRQMW
NAND614
IRQ MASK WRITE
I_33
63
DRQ[0]
FIQ[4]
LA[6]
I_65
15
ILA[6]
I_32
62
DRQ[1]
FIQ[5]
FIQMW
NAND613
FIQ MASK WRITE
LA[5]
I_25
21
ILA[5]
I_31
61
DRQ[2]
FIQ[6]
IOCSB
ILA[23]
ILA[22]
ILA[21]
ILA[20]
ILA[19]
AND616
LA[4]
I_24
22
ILA[4]
I_30
60
DRQ[3]
FIQ[7]
IO20
AND413
IO PAGE 0
LA[3]
I_23
23
ILA[3]
ILA[23]
ILA[22]
IOCSB
IORDB
AND412
I_140
59
OUTiPAD
MEMR
I_64
6
CS0
NAND410UTPAD
LA[2]
I_22
24
ILA[2]
ILA[18]
IOWRB
AND412
I_139
58
OUTiPAD
MEMW
I_63
7
CS1
NAND410UTPAD
LA[1]
I_21
25
ILA[1]
AND413
I_160
57
IOR
OR2110UTiPAD
I_62
8
CS2
NAND410UTPAD
16C552 SELECTS
LA[0]
I_20
26
ILA[0]
NAND413
AND413
I_159
56
IOW
OR2110UTiPAD
I_61
68
BPCS
ILA[5]
ILA[6]
NAND410UTPAD
DATA BUS
BREAK POINT PGA SELECT
NAND413
VLSI Technology, Inc.
1109 McKay Drive
San Jose, CA 95131
INTCN
INTCN
1/06/92
17:10:00


RESET
DI[7]
DI[6]
DI[5]
DI[4]
DI[3]
DI[2]
DI[1]
FIQMJ
DI[0]
I_102
I_109
I_103
I_105
I_104
I_106
I_107
I_108
CLR
D
Q
DFFC
FIQ[7]
FIQ[6]
FIQ[5]
FIQ[4]
FIQ[3]
FIQ[2]
FIQ[1]
FIQ[0]
AND2i0
PANB
VCC
I_188
OR2i0
GND
OR2i1
I_178
PRE
CLR
EN
DFFEPC
IRQRST
ILA[3]
DINK[7]
FINK[7]
S
MUX2x0
DO[7]
I_118
DFFC INT[6]
DINK[6]
FINK[6]
DO[6]
FINK[5]
I_124
DFFC INT[5]
DINK[5]
DO[5]
FINK[4]
I_123
DFFC INT[4]
DINK[4]
DO[4]
FINK[3]
I_122
DFFC INT[3]
DINK[3]
DO[3]
I_121
DFFC INT[2]
DINK[2]
FINK[2]
DO[2]
I_120
DFFC INT[1]
DINK[1]
FINK[1]
DO[1]
I_119
IRQMJ
DFFC INT[0]
DINK[0]
DO[0]
FINK[0]
OR6i0
NOR2i0
I_168
36
OUTiPAD
NFIQ
DINK[5]
DINK[4]
DINK[3]
DINK[2]
DINK[1]
DINK[0]
DINK[7]
DINK[6]
I_167
37
NIRQ
VLSI Technology, Inc.
1109 McKay Drive
San Jose, CA 95131
INTCN
INTCN
1/06/92
17:10:00


IO20
IORDB
IOCSB
ILA[4]
ILA[3]
AND5I4
READ
DO[0:7]
DI[0:7]
DO[0]
DO[1]
DO[2]
DO[3]
DO[4]
DO[5]
DO[6]
DO[7]
DI[0]
DI[1]
DI[2]
DI[3]
DI[4]
DI[5]
DI[6]
DI[7]
I_147
I_154
I_153
I_152
I_151
I_150
I_149
I_148
34
33
32
31
30
29
28
27
BIPAD
BD[0]
BD[1]
BD[2]
BD[3]
BD[4]
BD[5]
BD[6]
BD[7]
TIMTEST
I_185
48
INPAD
RESET
IMCLKB
CLR
CI
NRIPCT8
Q[0:7]
CO
OR2I0
CLR
CI
NRIPCT8
Q[0:7]
CO
CLR
Q
CI
CO
nbit
OR2I0
I_180
PRE
CLR
EN
D
Q
DFFEPC
GND
OR2I1
I_179
INT[1]
IRQRST
DI[1]
PRE
CLR
EN
D
Q
DFFEPC
TIMER INTERRUPT Approx 10ms
VLSI Technology, Inc.
1109 McKay Drive
San Jose, CA 95131
INTCN
INTCN
.
1/06/92
17:10:00

VLSI Technology, Inc.
1109 McKay Drive
San Jose, CA 95131
408-434-3100