486 CACHE CONTROLLER

FEATURES

- Single chip second-level cache controller optimized for use with the VL82C486 System Controller
- Look-aside architecture allows cache to be board-level option
- Write-back architecture for increased write performance
- Direct Map with external tags
- Up to 33 MHz operation
- Supports single motherboard designs for the following cache sizes:
  - 64 KB (caches 8 or 16 MB DRAM)
  - 128 KB (caches 16 or 32 MB DRAM)
  - 256 KB (caches 32 or 64 MB DRAM)
  - 512 KB (caches 64 or 128 MB DRAM)
  - 1 MB (caches 128 or 256 MB DRAM)
- Low total cache system cost:
  - Uses commodity SRAMs for Cache Tag and Cache Data
  - 25 ns data SRAMs, 20 ns tag SRAMs at 33 MHz
- High Performance:
  - 2-1-1-1 Burst Mode read cycles with two banks of data SRAM
  - 2-2-2-2 Burst Mode read cycles with one bank of data SRAM
  - One wait state writes on cache-hits
  - Minimum cache-miss penalty
- Flexibility:
  - Supports 8-bit or 9-bit TAG RAM (inclusive of DIRTY bit)
  - Supports one or two banks of SRAM
- Maintains full coherency during DMA/ Master Mode Cycles
  - The VL82C425 is transparent to software, acting as a front-end to system DRAM
- Setup/sizing mode provides direct access to cache SRAMs
- 128-lead metric quad flat pack (MQFP)

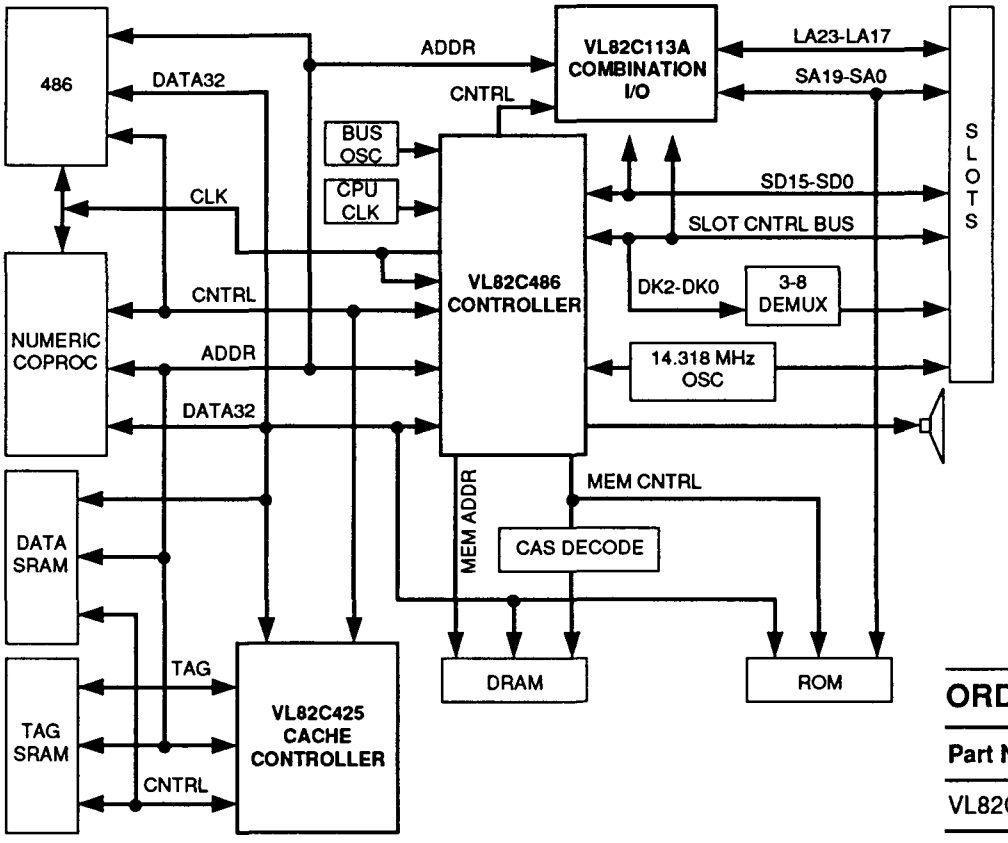
DESCRIPTION

The VL82C425 Cache Controller provides a low-cost direct map, look-aside write-back cache option for use with the VL82C486 System Controller. It supports from 64 KB to 1 MB cache sizes. It can cache from the first 8 MB to the first 256 MB of on-board DRAM, depending on the cache size and tag option selected. The cache line size is 16 bytes (four double words).

One or two 32-bit wide banks of asynchronous cache SRAM may be used to hold the data. Increased read performance is obtained by using two banks which allow interleaved accesses during burst read cycles.

Only one 8- or 9-bit (optional) tag SRAM is required to hold the upper memory address bits and the dirty bit. The number of tag SRAM locations required is equal to the size of the data cache (in bytes) divided by 16.

SYSTEM DIAGRAM (VL82C486/VL82C425-BASED PC/AT)



ORDER INFORMATION

Part Number	Package
VL82C425-FC	Metric Quad Flat Pack

Note: Operating temperature range is 0°C to + 70°C.

DESCRIPTION (Cont.)

On a read-hit, the VL82C425 performs a 2-1-1-1 (zero wait state) burst read if two banks of SRAM are used. It performs a 2-2-2-2 (three wait states) burst read if one bank of SRAM is used.

On a write-hit, the VL82C425 performs a one wait state (three clock cycle) write. Burst writes are not supported.

For read-misses the VL82C425 uses an internal line buffer for increased performance. On a read-miss the data is always read immediately from on-board DRAM and returned to the CPU to allow the 486 to complete its primary cache line-fill without delay. The data is also loaded into the VL82C425's 16 byte internal line buffer. The VL82C425 then becomes a Local Bus Master and writes the contents of the line buffer to the cache SRAMs. If the location in cache to which the data is to be written is dirty, then the old data is first written back to DRAM. The VL82C425 will accomodate any burst order during the read-miss read phase.

Cacheability of data returned from DRAM memory read is determined from the state of the -KEN input plus the states of -RDY and –BRDY during memory read.

On write-misses, the VL82C425 is bypassed and the data is written directly to DRAM (no cache line is allocated).

Local bus mastership for performing cache line fills and write-backs is obtained by asserting CHOLD and waiting for CHLDA back from the CPU before taking ownership of the bus. Bus arbitration for other local bus requesters (such as the VL82C486 during DMA/Master Mode cycles) is provided through daisy-chaining using the SHOLD and SHLDA signals.

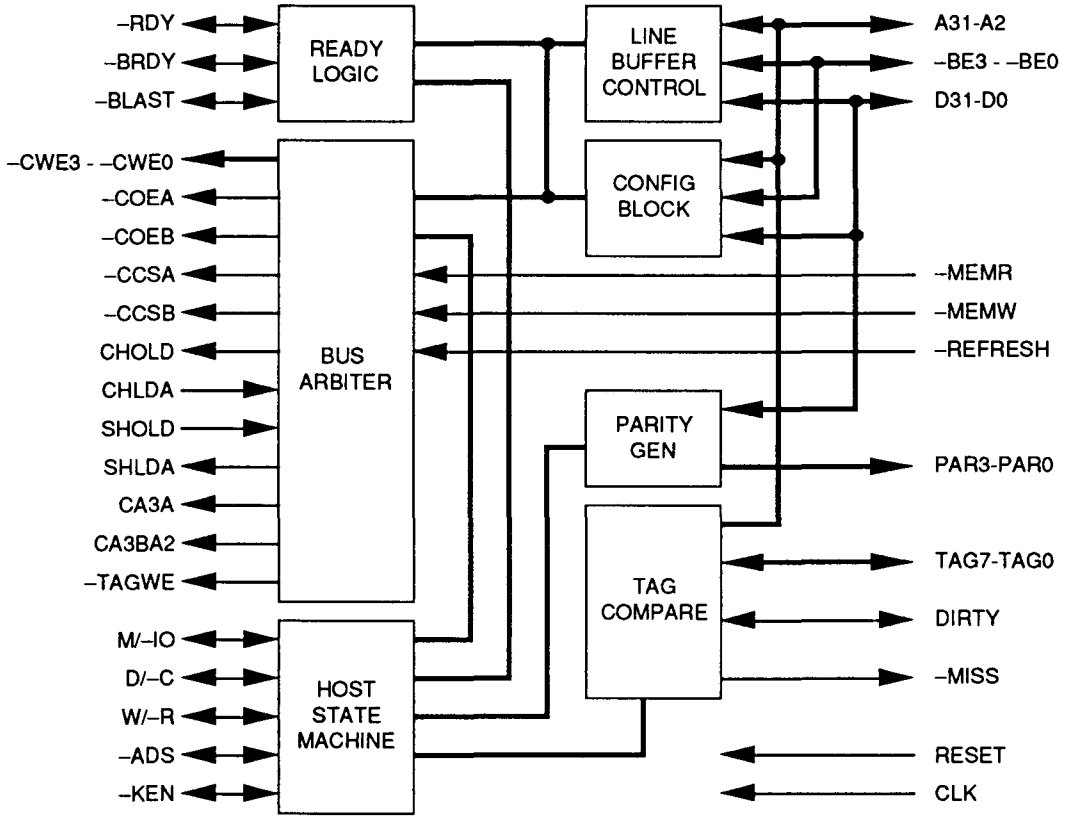
During DMA and Master Mode memory read cycles, the VL82C425 checks to see if the contents of a requested memory location are valid in cache. If a cache-hit occurs on a DMA or Master Mode read, then the –MISS signal is made inactive to inhibit the DRAM controller and the contents of the selected cache location are enabled onto D31-D0. If a cache-hit occurs on a DMA or Master Mode write, then the selected cache location is updated with the new data. DMA and Master Mode cycles are ignored on a cache-miss.

The VL82C425 will detect and respond as above to both synchronous local bus DMA and Master Mode cycles (that use –ADS, M/–IO etc.), as well as asynchronous ISA bus type DMA and Master Mode cycles (that use –MEMR and –MEMW). In both cases, SHOLD must be active.

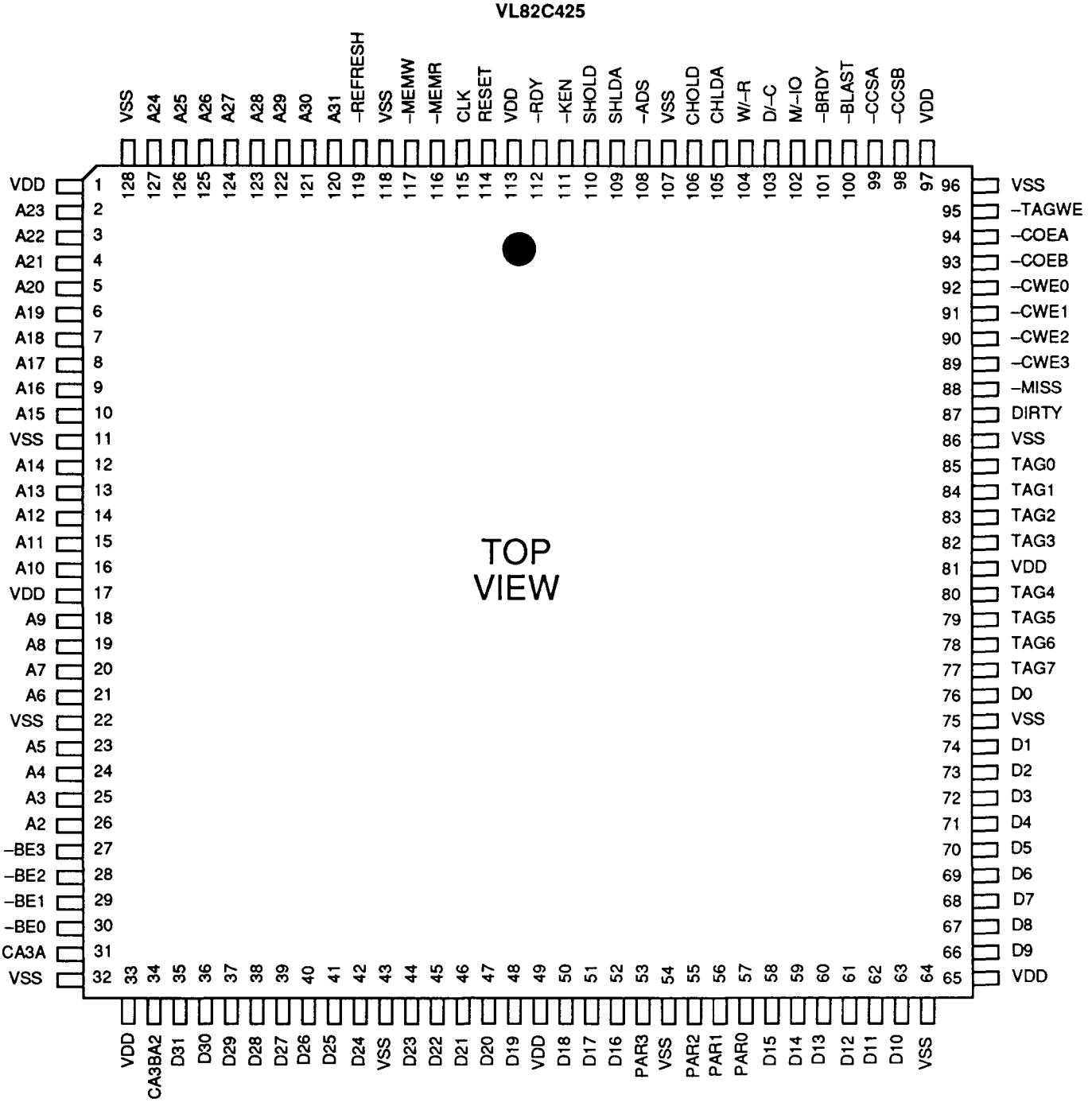
The VL82C425 contains a set of write-protection registers that may be used to protect cached memory in the range from 640 KB to 1 MB from being written. This is to ensure that cached ROM locations cannot become corrupted.

A "Direct Access" mode of operation is provided which allows the cache to appear as ordinary memory on the CPU local bus. This allows BIOS to easily size the cache memory at power-on reset.

BLOCK DIAGRAM



PIN DIAGRAM


VL82C425
TOP VIEW
1 VDD
2 A23
3 A22
4 A21
5 A20
6 A19
7 A18
8 A17
9 A16
10 A15
11 VSS
12 A14
13 A13
14 A12
15 A11
16 A10
17 VDD
18 A9
19 A8
20 A7
21 A6
22 VSS
23 A5
24 A4
25 A3
26 A2
27 –BE3
28 –BE2
29 –BE1
30 –BE0
31 CA3A
32 VSS
33 VDD
34 CA3BA2
35 D31
36 D30
37 D29
38 D28
39 D27
40 D26
41 D25
42 D24
43 VSS
44 D23
45 D22
46 D21
47 D20
48 D19
49 VDD
50 D18
51 D17
52 D16
53 PAR3
54 VSS
55 PAR2
56 PAR1
57 PAR0
58 D15
59 D14
60 D13
61 D12
62 D11
63 D10
64 VSS
65 VDD
66 D9
67 D8
68 D7
69 D6
70 D5
71 D4
72 D3
73 D2
74 D1
75 VSS
76 D0
77 TAG7
78 TAG6
79 TAG5
80 TAG4
81 VDD
82 TAG3
83 TAG2
84 TAG1
85 TAG0
86 VSS
87 DIRTY
88 –MISS
89 –CWE3
90 –CWE2
91 –CWE1
92 –CWE0
93 –COEB
94 –COEA
95 –TAGWE
96 VSS
97 VDD
98 –CCSB
99 –CCSA
100 –BLAST
101 –BRDY
102 M/–IO
103 D/–C
104 W/–R
105 CHLDA
106 CHOLD
107 VSS
108 –ADS
109 SHLDA
110 SHOLD
111 –KEN
112 –RDY
113 VDD
114 RESET
115 CLK
116 –MEMR
117 –MEMW
118 VSS
119 –REFRESH
120 A31
121 A30
122 A29
123 A28
124 A27
125 A26
126 A25
127 A24
128 VSS

PIN TYPE BY OPERATIONAL STATE

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
1	VDD	PWR			35	D31	IO	TTL	8
2	A23	IO	TTL	8	36	D30	IO	TTL	8
3	A22	IO	TTL	8	37	D29	IO	TTL	8
4	A21	IO	TTL	8	38	D28	IO	TTL	8
5	A20	IO	TTL	8	39	D27	IO	TTL	8
6	A19	IO	TTL	8	40	D26	IO	TTL	8
7	A18	IO	TTL	8	41	D25	IO	TTL	8
8	A17	IO	TTL	8	42	D24	IO	TTL	8
9	A16	IO	TTL	8	43	VSS	GND		
10	A15	IO	TTL	8	44	D23	IO	TTL	8
11	VSS	GND			45	D22	IO	TTL	8
12	A14	IO	TTL	8	46	D21	IO	TTL	8
13	A13	IO	TTL	8	47	D20	IO	TTL	8
14	A12	IO	TTL	8	48	D19	IO	TTL	8
15	A11	IO	TTL	8	49	VDD	PWR		
16	A10	IO	TTL	8	50	D18	IO	TTL	8
17	VDD	PWR			51	D17	IO	TTL	8
18	A9	IO	TTL	8	52	D16	IO	TTL	8
19	A8	IO	TTL	8	53	PAR3	O		8
20	A7	IO	TTL	8	54	VSS	GND		
21	A6	IO	TTL	8	55	PAR2	O		8
22	VSS	GND			56	PAR1	O		8
23	A5	IO	TTL	8	57	PAR0	O		8
24	A4	IO	TTL	8	58	D15	IO	TTL	8
25	A3	IO	TTL	8	59	D14	IO	TTL	8
26	A2	IO	TTL	8	60	D13	IO	TTL	8
27	–BE3	IO	TTL	8	61	D12	IO	TTL	8
28	–BE2	IO	TTL	8	62	D11	IO	TTL	8
29	–BE1	IO	TTL	8	63	D10	IO	TTL	8
30	–BE0	IO	TTL	8	64	VSS	GND		
31	CA3A	O		16	65	VDD	PWR		
32	VSS	GND		8	66	D9	IO	TTL	8
33	VDD	PWR			67	D8	IO	TTL	8
34	CA3BA2	O		16	68	D7	IO	TTL	8

PIN TYPE BY OPERATIONAL STATE (Cont.)

Pin #	Pin Name	Pin Type	Input Type	Drive (mA)	Pin #	Pin Name	Pin Type	Input Type	Drive (mA)
69	D6	IO	TTL	8	99	–CCSA	O		16
70	D5	IO	TTL	8	100	–BLAST	IO	TTL	8
71	D4	IO	TTL	8	101	–BRDY	IO	TTL	16
72	D3	IO	TTL	8	102	M/–IO	IO	TTL	8
73	D2	IO	TTL	8	103	D/–C	IO	TTL	8
74	D1	IO	TTL	8	104	W/–R	IO	TTL	8
75	VSS	GND			105	CHLDA	I	TTL	
76	D0	IO	TTL	8	106	CHOLD	O		8
77	TAG7	IO	TTL	8	107	VSS	GND		
78	TAG6	IO	TTL	8	108	–ADS	IO	TTL	8
79	TAG5	IO	TTL	8	109	SHLDA/–TRI	IO	TPU	8
80	TAG4	IO	TTL	8	110	SHOLD	I	TTL	
81	VDD	PWR			111	–KEN	I	TTL	
82	TAG3	IO	TTL	8	112	–RDY	IO	TTL	8
83	TAG2	IO	TTL	8	113	VDD	PWR		
84	TAG1	IO	TTL	8	114	RESET	I - S	TTL	
85	TAG0	IO	TTL	8	115	CLK	I	CMOS	
86	VSS	GND			116	–MEMR	I	TTL	
87	DIRTY	IO	TTL	8	117	–MEMW	I	TTL	
88	–MISS	O		16	118	VSS	GND		
89	–CWE3	O		16	119	–REFRESH	I	TTL	
90	–CWE2	O		16	120	A31	IO	TTL	8
91	–CWE1	O		16	121	A30	IO	TTL	8
92	–CWE0	O		16	122	A29	IO	TTL	8
93	–COEB	O		16	123	A28	IO	TTL	8
94	–COEA	O		16	124	A27	IO	TTL	8
95	–TAGWE	O		16	125	A26	IO	TTL	8
96	VSS	GND			126	A25	IO	TTL	8
97	VDD	PWR			127	A24	IO	TTL	8
98	–CCSB	O		16	128	VSS	GND		

Legend:

-PU	Indicates a pull-up resistor with approximately 10 kΩ minimum resistance to VDD.
TTL	TTL-compatible input.
CMOS	CMOS-compatible input.
-S	Indicates a Schmitt-trigger input with hystersis for noise immunity.
I	Input-only pin.
IO	Bidirectional pin.
PWR	Power supply pin.
GND	Ground pin.

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
LOCAL BUS INTERFACE SIGNALS		
A31-A2	120-127, 2-10, 12-16, 18-21, 23-26	Address Bus - The bidirectional address bus is an input from the local bus during memory or I/O cycles. The bus is driven out by the VL82C425 during write-back cycles to the system controller, or with the line buffer address output to data SRAMs during line swaps.
–ADS	108	Address Strobe - An active low I/O signal that is an input from CPU or output to the system controller during write-back cycles.
–BE3 - –BE0	27-30	Byte Enables bits 3 through 0 - Active low bidirectional byte enable signals are normally inputs from the local bus. They are outputs to the system controller during write-back cycles.
–BLAST	100	Burst Last - This bidirectional active low signal is used to confirm the last transfer of a burst cycle. It is an input from the CPU during read cycles and an output to the system controller during write-back cycles.
–BRDY	101	Burst Ready - A bidirectional, active low signal which indicates that the current burst cycle is complete. It is an input from the system controller during read-miss or write-back cycles. The VL82C425 monitors this signal to determine whether a memory read has completed successfully on a read-miss, and will invalidate the line swap if not. –BRDY is driven out by the VL82C425 during read-hit cycles. The VL82C425 enables the –BRDY three-state output only when driving it low and leaves it enabled for just one CPU clock cycle after it has driven it high again.
CLK	115	Clock - 1x CPU clock input.
D31-D0	35-42, 44-48, 50-52, 58-63, 66-74, 76	CPU Data Bus bits 31 through 0 - These signals are data inputs from the system memory during a read-miss cycle or from the CPU during an I/O write. They are output to cache SRAMs during a line swap.
PAR3-PAR0	53, 55-57	Parity bits 3 through 0 - These outputs reflect the even parity of bytes 3-0 of D31-D0. They are driven out by the VL82C425 only during write-back and DMA read-hit cycles. Otherwise they are three-stated (high-impedance).
D/–C	103	Data/Control - This cycle definition signal is normally an input from the CPU. During write-back cycles it is driven out by the VL82C425 to the system controller and is always driven high.
CHLDA	105	CPU Hold Acknowledge - An input signal from the CPU in response to HOLD, indicating that the CPU has released control of the local bus.
CHOLD	106	CPU Hold Request - An output to the CPU requesting control of the local bus. This output is generated from an internally generated hold or from a one clock delayed SHOLD input.
SHLDA/–TRI	109	Serial Hold Acknowledge - Output to the VL82C486 system controller indicating that control of the local bus has been released. This output is driven high (active) one clock cycle after the CHLDA input is driven high, only if no internal VL82C425 hold requests have been generated. SHLDA is deasserted one clock after the SHOLD input is deasserted. During power-on reset, when RESET input is high, this signal is an input which controls the In-Circuit (three-state) Test Mode. If the input is low, all output and bidirectional pins are driven to a high-impedance state. This pin has an internal pull-up resistor.
SHOLD	110	Serial Hold Request - A hold request input from the VL82C486 system controller requesting control of the local bus. This active high input is clocked in and delayed one clock cycle to generate the CHOLD output, if an internal hold request is not pending.
–KEN	111	Cache Enable - This is an active low input from the system controller. It is sampled only during the first and fourth double word transfers of read-miss cycles at the same time –BRDY is returned to determine cacheability of the line being read from system memory.
M/–IO	102	Memory/Input-Output - This cycle definition signal is normally an input from the CPU. During write-back cycles it is driven out by the VL82C425 to the system controller and is always driven high.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
–RDY	112	Ready (Non-Burst) - A ready input from system controller during read-miss cycles or an output to the CPU during write-hit cycles or configuration register read/write cycles when the WPTREN bit is set. The VL82C425 enables the –RDY three-state output only when driving it low and leaves it enabled for just one CPU clock cycle after it has driven it high again.
RESET	114	Reset - This signal is the power-on reset input and typically is connected to the RSTDRV from the VL82C486 System Controller.
W/–R	104	Write/Read - This cycle definition signal is normally an input from the CPU. During write-back cycles it is driven out by the VL82C425 to the system controller and is always driven high.
CACHE INTERFACE SIGNALS		
CA3A	31	Cache Address 3 Bank A - This output bit represents address bit 3 to cache Bank A. It is normally equivalent to A3, except during a read-hit in a two bank configuration. In this case, it is toggled between 1 and 0 in conjunction with CA3BA2 during a burst read in order to interleave access to the two banks of SRAM. This is done to meet the SRAM timing requirements.
CA3BA2	34	Cache Address 3 Bank B, Address 2, Bank A - When two banks of SRAM are used, this output bit represents address bit 3 to cache Bank B. It is normally equivalent to A3, except during a read-hit in a two bank configuration. In this case, it is toggled between 1 and 0 in conjunction with CA3A during a burst read in order to interleave access to the two banks of SRAM. This is done to meet the SRAM timing requirements. When one bank of SRAM is used, this bit represents address bit 2 to cache Bank A and is equivalent to A2.
–CCSA	99	Cache Chip Select, Bank A - This active low output signal is normally active and is de-asserted only when two banks of cache memory are used and a write to Bank B takes place. It is also inactive during the read phase of a read miss cycle.
–CCSB	98	Cache Chip Select, Bank B - This active low output is normally active and is de-asserted only when a write to Bank A takes place and during the read phase of a read miss cycle.
–COEA	94	Cache Output Enable, Bank A - This active low output is normally de-asserted and is made active only during read-hit cycles (CPU or DMA) or write-back cycles from Bank A.
–COEB	93	Cache Write Enable, Bank B - This active low output is normally de-asserted and is made active only during read-hit cycles (CPU or DMA) or write-back cycles from Bank B.
–CWE3 - -CWE0	89-92	Cache Write Enables - There is one active low cache write enable per byte, which drives both banks of data SRAM. These signals are asserted during a CPU write-hit, a DMA/ Master Mode write-hit, and when performing a line swap to write a new line into SRAM from the line buffer. For CPU and DMA write-hits, these signals are qualified with –BE3 to –BE0. When writing a new line into SRAM they are all made active.
DIRTY	87	Cache Line Dirty - This bidirectional bit to/from the tag SRAM indicates whether the cache line contents have been written by the CPU since being filled from system memory.
–MISS	88	Cache Miss - This active low output to the system controller is normally low. It is driven high to indicate a hit only during T2 cycles of read- or write-hits, or when SHLDA is active and the selected tag matches the address on A31-A2.
TAG7-TAG0	77-80, 82-85	Tag SRAM bits 7 through 0 - These bidirectional signals are the tag data inputs from the tag SRAM. They are outputs during write-hit and read-miss cycles. TAG7 is optional and may be left unconnected. It has an internal pull-up resistor to assist tag-width determination on initialization.
–TAGWE	95	Tag Write Enable - This active low output is asserted during a CPU write-hit and when performing a line swap to write a new line into SRAM from the line buffer.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
–MEMR	116	Memory Read - This active low input is used for initiating a read-snoop on a read-hit during a DMA or Master Mode cycle.
–MEMW	117	Memory Write - This active low input is used for initiating an update to the cache on a write-hit during a DMA or Master Mode cycle.
–REFRESH	119	Memory Refresh - This active low ISA Bus refresh input is used to qualify –MEMR to avoid driving cache SRAM data onto the D bus during a refresh cycle.
POWER AND GROUND PINS		
VDD	1, 17, 33, 49, 65, 81, 97, 113	Power +5.0 V or 3.3 V
VSS	11, 22, 32, 43, 54, 64, 75, 86, 96, 107, 118, 128	Ground

FUNCTIONAL DESCRIPTION

MAJOR COMPONENTS

TAG Control and Comparator:
- Contains cache miss logic and tag address comparator

Swap Line Buffer:
- Contains the 16-byte swap line buffer plus the line address and line valid bit

Data and TAG SRAM Control Logic:
- Controls cache SRAM chip enables, output enables, and byte write enables
- Provides interleaved SRAM control

Local Bus Interface Logic:
- Provides data, address, and control interface to the local bus

VL82C486 Interface Logic:
- Controls DMA/Master Mode Interface
- Controls local bus arbitration
- Provides write-protect logic
- –MISS output to VL82C486

Host State Machine:
- Controls the VL82C425's operational states
- Provides control interface to local bus

Configuration, Initialization and Test Mode Logic:
- Configuration options for:
  - Cache sizes
  - Number of tag bits
  - Number of cache banks
  - Write protection registers
  - Direct Access Mode

CACHE SIZE AND CONFIGURATION SUPPORT

Cache Size and Range Options

The VL82C425 is a very versatile cache controller. By using internal register settings, it can be programmed to support:

- Cache sizes from 64 KB to 1 MB
- Cacheable DRAM address ranges from 8 MB to 256 MB
- It can use an 8-bit tag RAM (7-bit tag address plus Dirty bit) or a 9-bit tag RAM (8-bit tag address plus Dirty bit).

The cache sizes and cacheable memory ranges which are supported are given in Table 1.

Tag Address Assignment

Table 2 shows the assignment of the upper address bits to the TAG7-TAG6 signals to/from the tag SRAM. Note that in the 7-Bit Tag Mode, it is always TAG7 that becomes unused for all cache sizes, allowing this bit to be omitted from the tag SRAM without having to select different jumper options for the tag arrangement when upgrading the cache size. Also note that use of the Dirty bit is optional; it may be pulled high rather than connected to SRAM, forcing a write-back cycle on any read miss.

TABLE 1. CACHES SIZES AND MEMORY RANGES

Cache Size	Tag Field Address	Cache RAM Address/Cache RAMS	Cacheable Main Memory	No. of Banks
64 KB	A16-A22 (7 Bits)	A3-A15 (eight 8K x 8)	8 MB	2
64 KB	A16-A23 (8 Bits)	A3-A15 (eight 8K x 8)	16 MB	2
128 KB	A17-A23 (7 Bits)	A2-A16 (four 32K x 8)	16 MB	1
128 KB	A17-A24 (8 Bits)	A2-A16 (four 32K x 8)	32 MB	1
256 KB	A18-A24 (7 Bits)	A3-A17 (eight 32K x 8)	32 MB	2
256 KB	A18-A25 (8 Bits)	A3-A17 (eight 32K x 8)	64 MB	2
512 KB	A19-A25 (7 Bits)	A2-A18 (four 128K x 8)	64 MB	1
512 KB	A19-A26 (8 Bits)	A2-A18 (four 128K x 8)	128 MB	1
1 MB	A20-A26 (7 Bits)	A3-A19 (eight 128K x 8)	128 MB	2
1 MB	A20-A27 (8 Bits)	A3-A19 (eight 128K x 8)	256 MB	2

TABLE 2. TAG ADDRESS ASSIGNMENT

Cache Size	Tag Size (Bits)	TAG0	TAG1	TAG2	TAG3	TAG4	TAG5	TAG6	TAG7
64 KB	7	A16	A17	A18	A19	A20	A21	A22	X
64 KB	8	A16	A17	A18	A19	A20	A21	A22	A23
128 KB	7	A22	A17	A18	A19	A20	A21	A23	X
128 KB	8	A22	A17	A18	A19	A20	A21	A23	A24
256 KB	7	A22	A23	A18	A19	A20	A21	A24	X
256 KB	8	A22	A23	A18	A19	A20	A21	A24	A25
512 KB	7	A22	A23	A24	A19	A20	A21	A25	X
512 KB	8	A22	A23	A24	A19	A20	A21	A25	A26
1 MB	7	A22	A23	A24	A25	A20	A21	A26	X
1 MB	8	A22	A23	A24	A25	A20	A21	A26	A27

Notes: X = Unused.

TAG7 has a weak pull-up in its input pad to assist tag width determination on initialization (see the section titled "Use of Direct Access Mode for Cache Sizing and Initialization").

FIGURE 1. 128KB, ONE BANK CACHE EXAMPLE

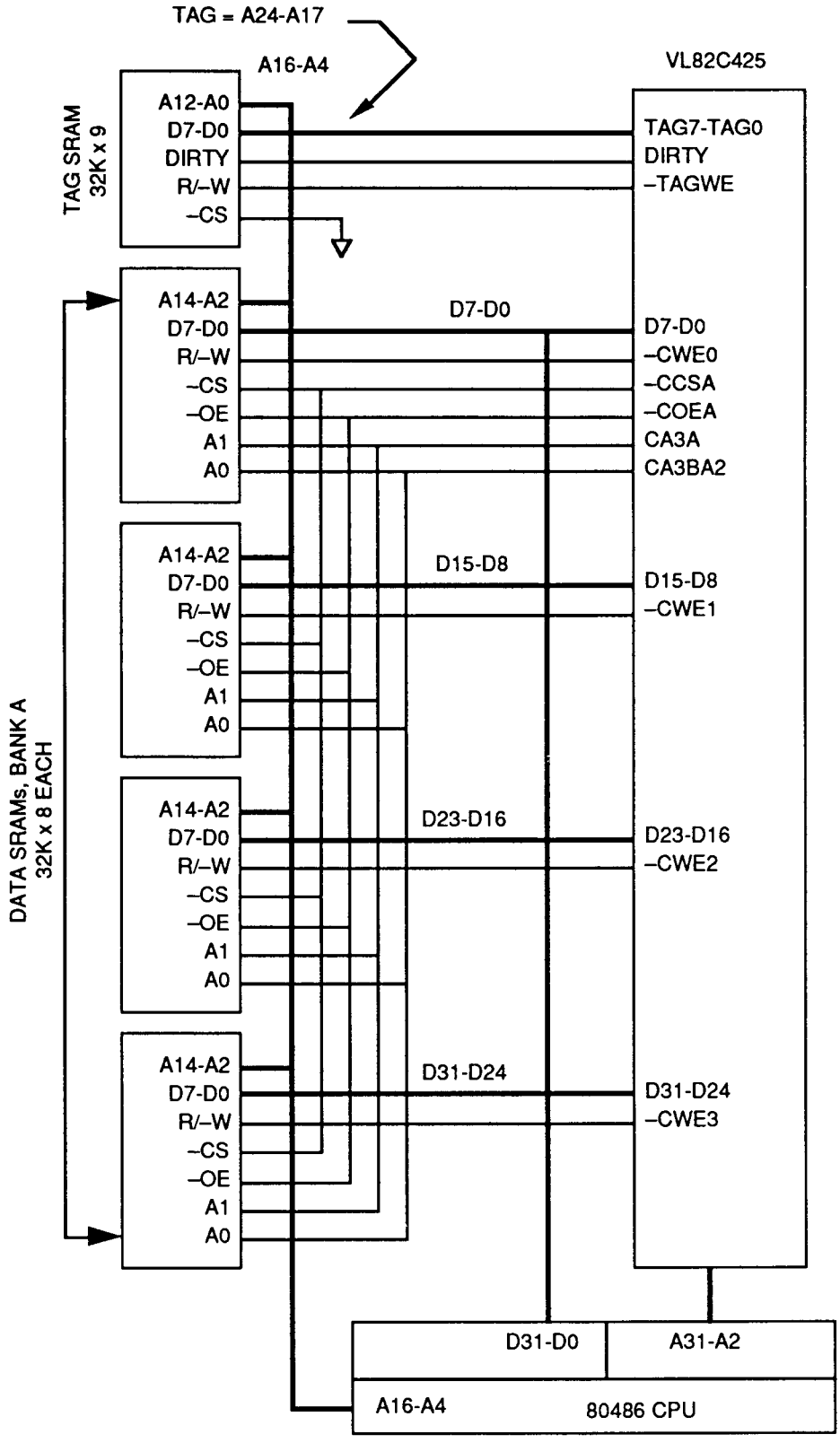
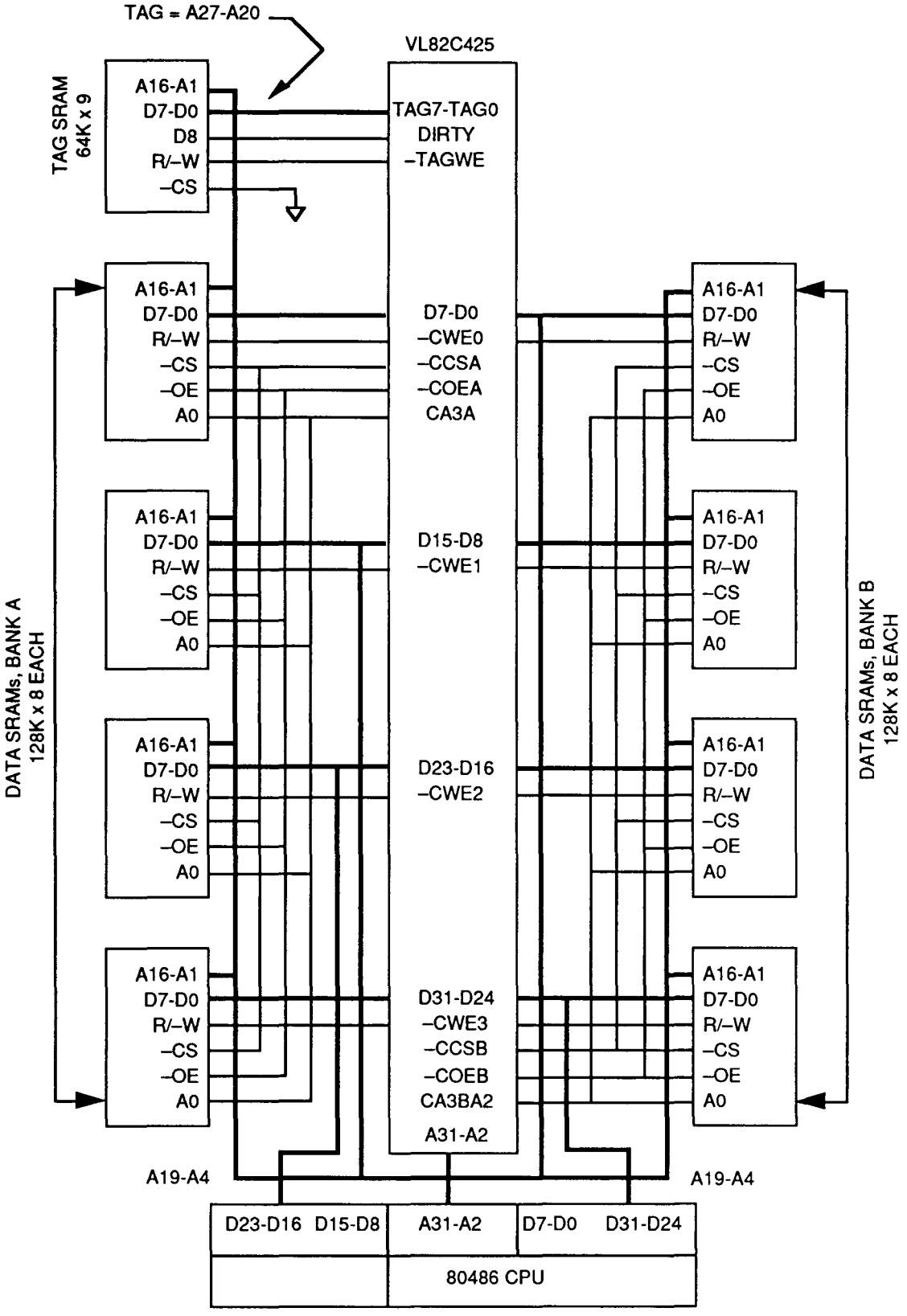


FIGURE 2. 1MB, DOUBLE BANK CACHE EXAMPLE



CACHE CYCLE DEFINITION

Overview

Table 3 summarizes the actions taken by the VL82C425 in response to all local bus and ISA bus cycles. The sections which follow explain each of the cycle types.

CPU Read-Hit Cycles

If the VL82C425 detects a cache-hit on a 486 code or memory read, it generates a burst read cycle of up to four double words from the cache data SRAMs. Operation is as follows:

- The VL82C425 constantly monitors the 486 local bus for valid addresses to start the VL82C425 cache tag access. A matched tag entry during a memory read cycle indicates a cache-hit.
- The VL82C425 informs the VL82C486 of a cache-hit by de-asserting –MISS before the end of the first T2. The VL82C486 will then abort its memory access and will not assert –BRDY or –RDY.
- The VL82C425 then enables the cache data SRAMs to sequentially send the requested 16 bytes of data back to the CPU via the local bus and asserts –BRDY for each double word returned.
- The state of the –KEN input is not monitored during a cache-hit.

If two banks of cache data SRAM are present, then the VL82C425 generates 2-1-1-1 burst reads as shown in Figure 3. If only one bank of cache data SRAM is present then the VL82C425 generates 2-2-2-2 burst reads as shown in Figure 4. If –BLAST is asserted before four double words are read, the burst read cycle will terminate.

TABLE 3. VL82C425 CYCLE TYPES

Local Bus Cycle Type	Line Status	Tag RAM	Cache Data SRAM	Dirty Bit	Internal Line Buffer
Read-Hit	X	NOP	Burst read four double words from cache to CPU	NOP	NOP
Read-Miss Clean	Clean	Update	Wait for DRAM read, then load cache with contents of line buffer	Clear	Load line (4 double words) from DRAM, then transfer line to cache data SRAM
Read-Miss Dirty	Dirty	Read, Update	Wait for DRAM read, then write-back old line from cache to DRAM, then load cache with contents of line buffer	Clear	Load line (4 double words) from DRAM, then wait for write-back of old line, then transfer new line to cache data SRAM
Write-Hit	X	Update*	WRITE	Set	NOP
Write-Miss	X	NOP	NOP	NOP	NOP
Non-Cacheable Read	X	NOP	NOP	NOP	NOP
I/O Read	X	NOP	NOP	NOP	NOP
Non-Cacheable Write	X	NOP	NOP	NOP	NOP
DMA Read-Hit	X	NOP	READ	NOP	NOP
DMA Read-Miss	X	NOP	NOP	NOP	NOP
DMA Write-Hit	X	NOP	WRITE	NOP	NOP
DMA Write-Miss	X	NOP	NOP	NOP	NOP

Notes: X = Don't care.
NOP = No operation.
READ = Read byte, word or double word from data SRAM onto D bus.
WRITE = Write byte, word or double word from D bus into data SRAM.
* = Tag is rewritten with old value.

CPU Read-Miss Cycles
A read-miss cycle occurs when the CPU performs a memory access that does not generate a cache-hit (i.e. data from the requested memory location has not been previously loaded into the cache). On detection of a read-miss, the VL82C425 updates the cache with the requested data from system memory, provided that the memory access is defined as cacheable. Since the VL82C425 is a write-back cache, the cache location allocated to the new data may already contain modified (dirty) data from another memory location; if so, then that data must first be written back to memory.

Note that –COEA/B pulse low in the first T2 of a read-miss cycle in anticipation of a read-hit. They are returned high before any real data transfer occurs on the bus. See Figure 5.

CPU Read-Miss Clean Cycles
A read-miss clean cycle is generated when the VL82C425 detects a cacheable memory read cycle on the local bus where the target data is not present in the cache memory, and the cache location allocated to hold the new data does not contain a modified line from a different memory address. The sequence is as follows:

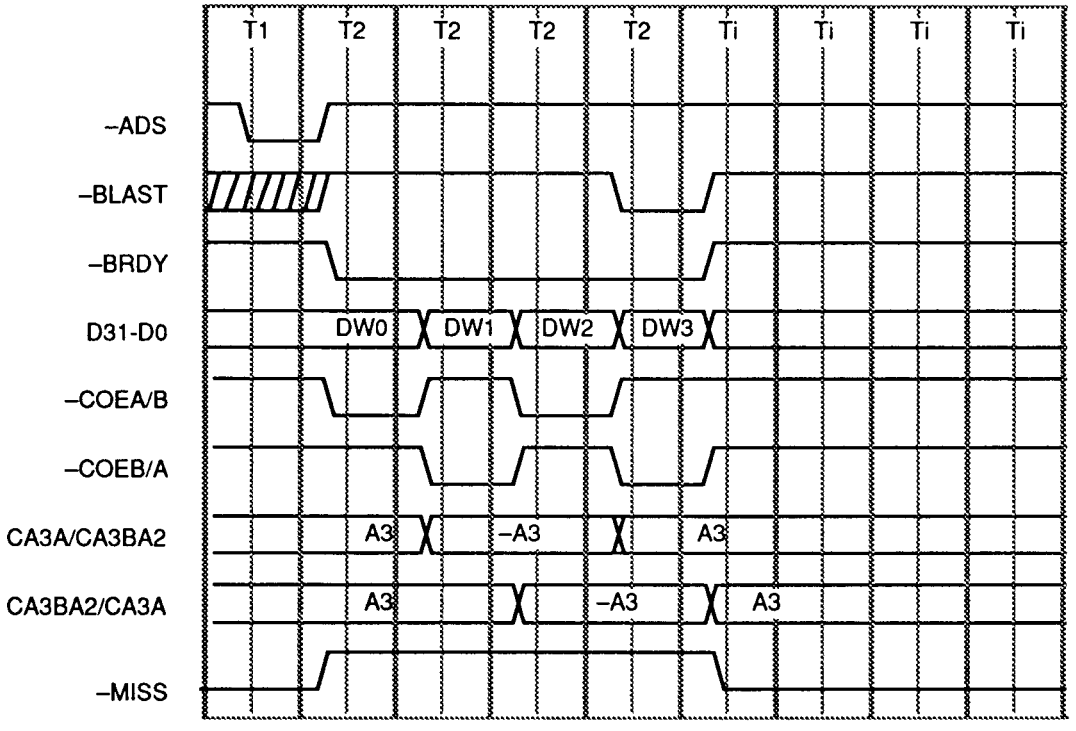
- The VL82C425 monitors the 486 local bus for valid addresses to start the VL82C425 cache tag access. An unmatched tag entry during a memory read cycle indicates a cache-miss.
- The VL82C425 informs the VL82C486 of a cache-miss by leaving –MISS asserted (–MISS is normally low, and is not de-asserted for this case) before the end of the first T2. The VL82C486 then performs the memory read and asserts –BRDY or –RDY.
- The VL82C425 loads the data returned by the VL82C486 into its internal line buffer at the same time as the data is returned to the CPU.
- If –KEN is sampled active at the same time as –BRDY is returned by the VL82C486 for the first double word, then the VL82C425 requests mastership of the local bus by asserting CHOLD.
- If –KEN is sampled active at the same time as –BRDY is returned for the fourth double word, then the VL82C425 waits until it is granted the local bus (when CHLDA is asserted), and then performs a line swap and transfers the contents of the line buffer to the selected cache location. The tag RAM is updated with the new address and the Dirty bit is cleared.

If these conditions are not met, the line buffer is invalidated. See section entitled "Read Miss Line Buffer Invalidation" for details. The read-miss clean sequence comprising the read phase (from DRAM) and the line swap phase is shown in figures 5 and 6 respectively.

CPU Read-Miss Dirty Cycles
A read-miss dirty cycle is generated when the VL82C486 detects a cacheable memory read cycle on the local bus where the target data is not present in cache memory, and the cache location allocated to hold the new data contains a modified line from a different memory address. The sequence is as follows:

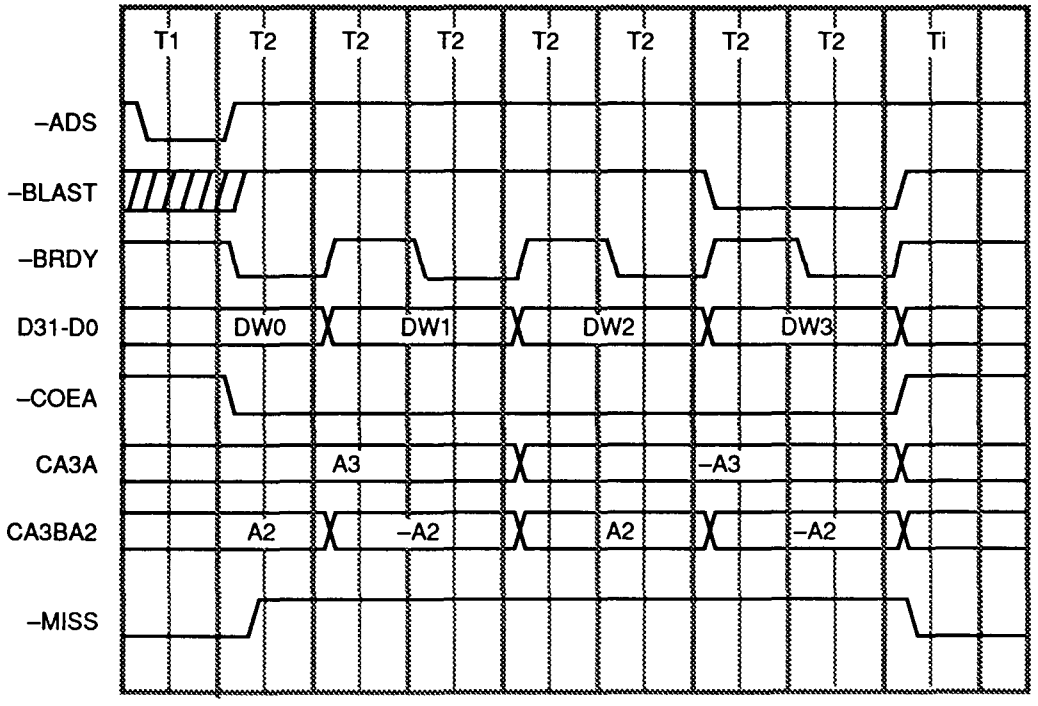
- The VL82C425 monitors the 486 local bus for valid addresses to start the VL82C425 cache tag access. An unmatched tag entry during a memory read cycle indicates a cache-miss.

FIGURE 3. 2-BANK READ HIT TIMING



Note: –CCSA and –CCSB are active (LOW) throughout the cycle

FIGURE 4. 1-BANK READ HIT TIMING



Note: –CCSA and –CCSB are active (LOW) throughout the cycle

- The VL82C425 informs the VL82C486 of a cache-miss by asserting –MISS before the end of the first T2. The VL82C486 then performs the memory read and asserts –BRDY or –RDY.
- The VL82C425 loads the data returned by the VL82C486 into its internal line buffer at the same time as the data is returned to the CPU.
- If –KEN is sampled active at the same time as –BRDY is returned by the VL82C486 for the first double word, then the VL82C425 requests mastership of the local bus by asserting CHOLD.
- If –KEN is sampled active at the same time as –BRDY is returned for the fourth double word, then the VL82C425 waits until it is granted the local bus (when CHLDA is asserted). It then performs a write-back by generating four write cycles to the VL82C486 to return the old cache line back to DRAM. The VL82C425 also generates the correct parity and drives it onto PAR3-PAR0.
- The VL82C425 then transfers the contents of the line buffer to the selected cache location. The tag RAM is updated with the new address and the Dirty bit is cleared.

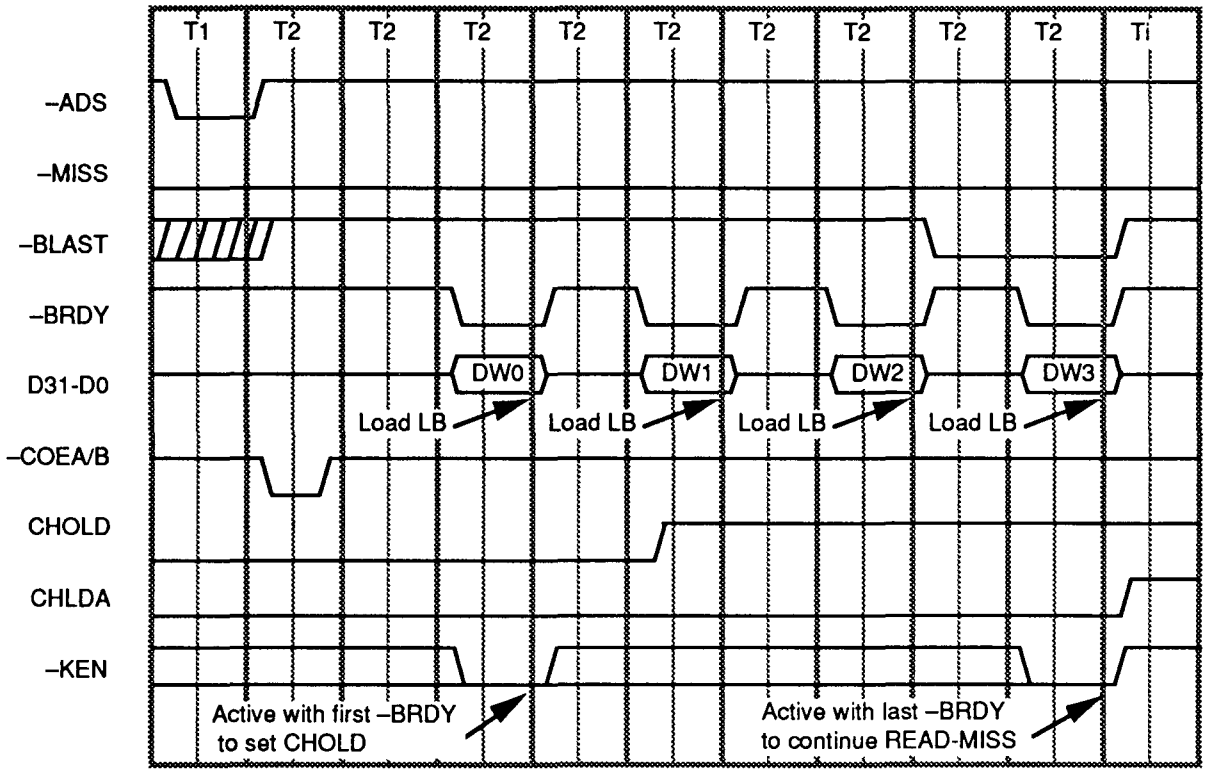
If these conditions are not met, the line buffer is invalidated. See section entitled "Read Miss Line Buffer Invalidation" for details. The read-miss dirty sequence comprises the read phase (from DRAM), the write-back phase, and the line swap phase, in that order. The timing for these operations is shown in figures 5, 6 and 7 respectively.

Read-Miss Line Buffer Invalidation
During a read-miss sequence, there are five cases which may cause the line buffer to be invalidated and the operation of writing its contents to the cache SRAMs aborted (write-back of dirty data to system memory is also aborted). These are as follows:

- If –KEN is sampled inactive during the DRAM read on the first or fourth double word transfer when –BRDY is asserted, then CHOLD is de-asserted and the the line buffer is invalidated.
- The line buffer is invalidated and CHOLD de-asserted when –RDY instead of –BRDY is asserted at the end of the memory read. Assertion of both –RDY and –BRDY during any double word transfer will not invalidate the line buffer.
- The line buffer is invalidated and CHOLD de-asserted if –BRDY is asserted less than four times during the memory read before –BLAST is asserted.
- The line buffer is invalidated and CHOLD immediately de-asserted if CHLDA is not made active prior to the next cycle in which –ADS becomes active after the memory read. This ensures that the line buffer is available for a subsequent read-miss when the bus is not granted due to locked cycles, etc. If the Ti cycle after the memory read shown in Figure 5 is actually a T1 cycle of the next memory read or write, then the VL82C425 will handle it as normal due to –ADS becoming active.
- The line buffer is invalidated and CHOLD de-asserted if –BLAST is not asserted on the fourth (final) double word transfer of the memory read.

CPU WRITE-HIT CYCLES
If the VL82C425 detects a cache-hit on a 486 memory write, it will write the byte, word, or double word (as selected

FIGURE 5. READ MISS TIMING - READ PHASE



Note: –COEA/B are active in the first T2 to anticipate a READ-HIT

by the byte-enables –BE3 - –BE0) into the cache and return –RDY. The write-hit is a one wait-state cycle. Operation is as follows:

- The VL82C425 monitors the 486 LOCAL Bus for valid addresses to start the VL82C425 cache tag access. A matched tag entry during a memory write cycle indicates a cache-hit.
- The VL82C425 informs the VL82C486 of a cache-hit by de-asserting –MISS before the end of the first T2. The VL82C486 will then abort its memory access and will not assert –BRDY or –RDY. The VL82C425 guarantees that –MISS is held inactive until at least the end of the first T2, despite the tag-write starting in the middle of the first T2.
- The VL82C425 asserts –CWE3 to –CWE0 according to which bytes are being written in the middle of the first T2. At the same time it asserts –TAGWE in order to set the Dirty bit.
- All write enables are de-asserted in the middle of the second T2 and –RDY is asserted during the second T2.
- The state of the –KEN input is not monitored during a cache-hit.
- If the VL82C425 detects that the address to be written to is write-protected by its internal write protection registers, then –CWE3 - –CWE0 and –TAGWE will be inhibited, however, the VL82C425 will still assert –RDY.

If two banks of cache data SRAM are present, then the VL82C425 will de-assert –CCSA or –CCSB, according to which bank is not selected by A2. The operation is shown in Figure 8.

CPU Write-Miss Cycles

On a write-miss cycle, the VL82C425 asserts –MISS before the end of the first T2. This causes the VL82C486 to perform the write to DRAM. No action is taken by the VL82C425 (write allocates are not supported).

MISCELLANEOUS CPU CYCLES

The VL82C425 takes no action on interrupt acknowledge cycles, or halt/special cycles. It also ignores I/O cycles except for those directed towards loading or reading the internal configuration registers. See section 6 on configuration register access.

DMA/MASTER MODE CYCLES

ISA Bus DMA/Master Mode Read Cycles

The VL82C425 monitors SHLDA, –MEMR, and –REFRESH to recognize the start of an ISA bus DMA/Master Mode memory read. When the address is available on A31-A2, it looks for a match with the selected tag entry. There are two possible outcomes:

1. Cache-Miss (no tag match). No action is required.
2. Cache-Hit (tag match). In this case the VL82C425 will perform the following asynchronous operation (see Figure 9):
   - Drive –MISS high to inhibit the VL82C486 memory read.
   - Enable the selected cache data SRAMs onto D31-D0 when –MEMR goes active.
   - Generate even parity for cache data, drive onto PAR3-PAR0.

FIGURE 6. READ MISS TIMING - LINE SWAP PHASE

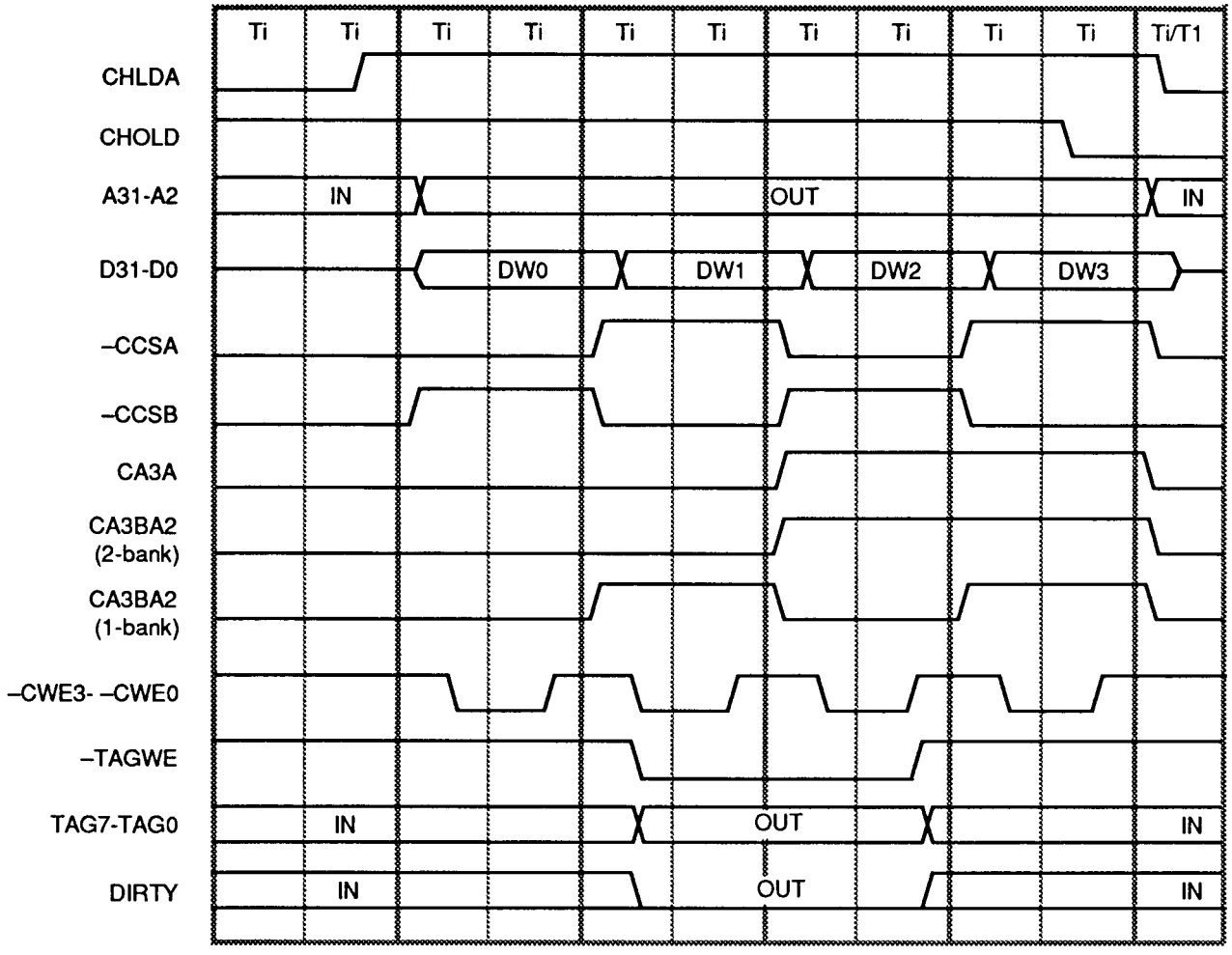
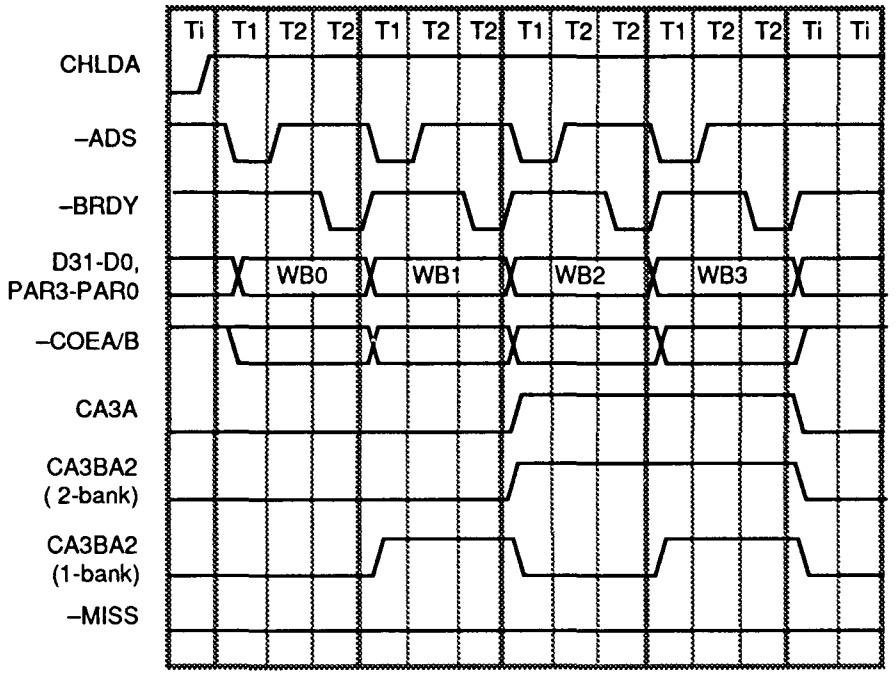
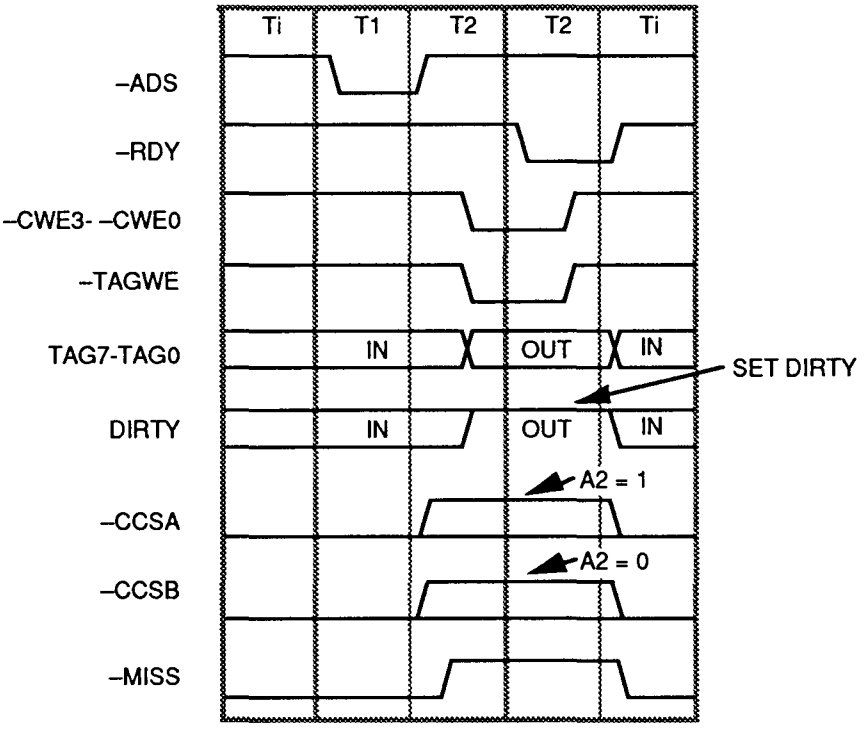


FIGURE 7. READ MISS DIRTY TIMING - WRITE-BACK PHASE



Note: –CCSA and –CCSB are active (LOW) throughout the cycle

FIGURE 8. WRITE HIT TIMING



ISA Bus DMA/Master Mode Write Cycles

The VL82C425 monitors SHLDA and –MEMW to recognize the start of a DMA/Master Mode memory write. When the address is available on A31-A2, it looks for a match with the selected tag entry. There are two possible outcomes:

1. Cache-Miss (no tag match). No action is required.
2. Cache-Hit (tag match). When –MEMW goes active, the VL82C425 asserts –CWE3 - –CWE0 to update the selected line in the cache data SRAM with a byte, word or double word (depending on the byte enables). If two banks of data SRAM are used then the unselected one is disabled by de-asserting its –CCSA or –CCSB. (The VL82C425 actually deasserts both –CCSA and –CCSB at the beginning of an asynchronous DMA Master Mode cycle, then reasserts the appropriate one). The tag and dirty bits are unchanged (–TAGWE is not asserted). The operation is asynchronous and is depicted in Figure 10.

Synchronous DMA/Master Mode Cycles

When SHLDA is active, the local bus has been granted to an alternate local bus master (i.e., one other than the CPU) which is then free to generate synchronous local bus cycles. The VL82C425 responds to such cycles in the following way:

- Read and write cache-hits are treated in exactly the same way as read and write-hits for CPU generated cycles as described in sections entitled "CPU Read Hit Cycles" and "CPU Write Hit Cycles" (i.e., as if SHLDA was not active), with the exception of parity generation on read-hits. On read-hits, the VL82C425 calculates the correct parity (even) for the data read from the cache and drives it onto PAR3-PAR0. This is necessary to prevent the VL82C486 from generating an interrupt to the CPU.
- Both read- and write-misses are completely ignored (other than ensuring –MISS is low throughout the read or write cycle). This prevents the cache from being filled with DMA generated data.

FIGURE 9. ISA BUS DMA / MASTER MODE READ HIT

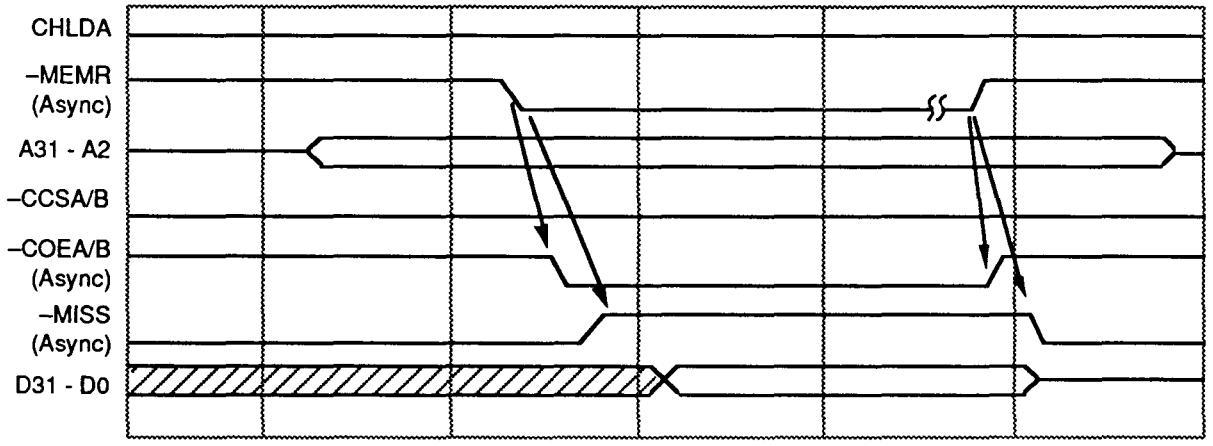
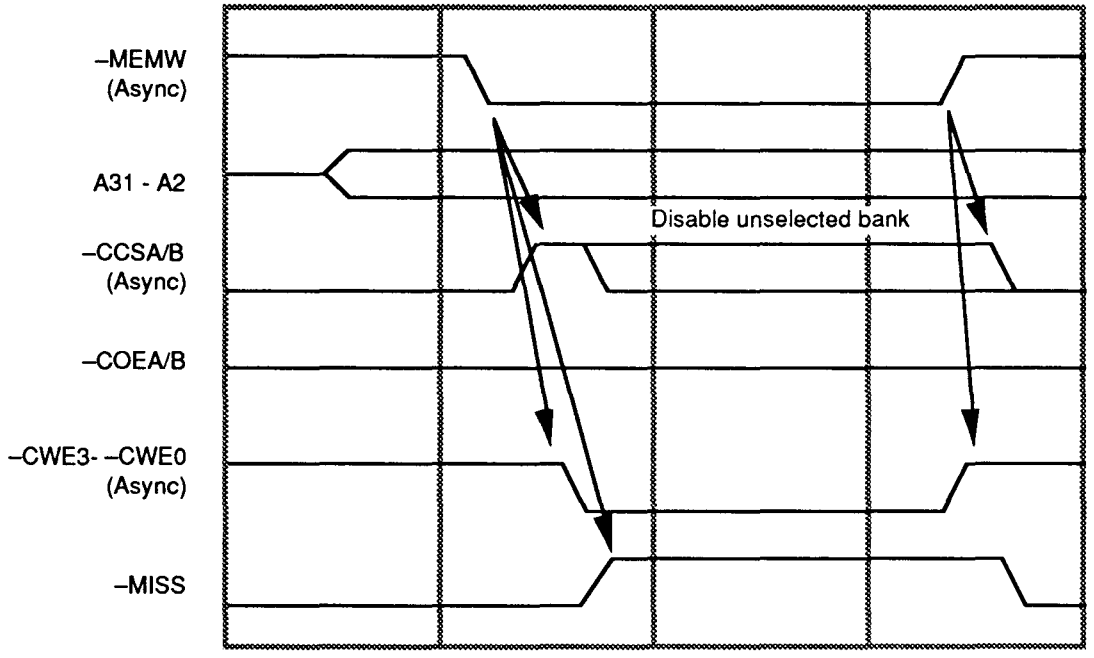


FIGURE 10. ISA BUS DMA / MASTER MODE WRITE HIT



TIMING OF –MISS PIN

In order to meet the timing requirements of the VL82C486, the –MISS pin must always be low (active) except during T2 cycles of a read-hit or write-hit, or when SHLDA is active and the current local bus address indicates a cache-hit. Specifically, the VL82C486 requires the –MISS pin to be low during:

- T1/Ti of all local bus cycles.
- The DRAM read phase of a read-miss
- The write-back phase of a read-miss
- Tag miscompare during DMA/Master Mode read cycles
- When the cache is disabled

CACHEABILITY CONTROL

The VL82C425 is designed to cache only memory locations from on-board DRAM, since coherency cannot be maintained if ISA bus or local bus peripheral memory locations are cached. There are several ways to ensure this:

- When used with the VL82C486 without local bus peripherals that drive –BRDY, the –KEN input may be tied active (low). The VL82C425 will only cache data on read cycles that return –BRDY, which the VL82C486 asserts only during on-board DRAM cycles.
- When used with local bus peripherals that assert –BRDY, or with system controllers that assert –BRDY for accesses other than on-board DRAM accesses, the –KEN output of the VL82C486 or other system controllers may be connected to the –KEN input of the VL82C425. The VL82C486 or other system controllers must then be programmed to ensure that all memory except on-board DRAM is non-cacheable.
- Alternatively, any active low signal that is asserted at the same time as –BRDY only during on-board DRAM accesses may be used to drive the –KEN input. The NOR of the –MDENX and –MDENY signals from the VL82C486 meet this criterion.

READY CONTROL

The VL82C425 generates –BRDY for all read-hit cycles and –RDY for all write-hit cycles. The output buffers for –RDY and –BRDY are normally three-stated. The output buffers are enabled only when the VL82C425 drives these signals low and for one clock cycle after it drives them from low back to high. This protocol allows the –RDY and –BRDY signals to be driven by other local bus devices such as the system controller and local bus peripherals without external gating.

WRITE PROTECTION SUPPORT

There are six configuration registers that allow any 16K block in the 640K-1M range to be marked as write-protected. Write-protection is used to prevent the 486 processor from writing into its primary cache at locations defined as ROM or shadow ROM areas. The registers mirror those in the VL82C486 which are used for write-protecting the CPU primary cache. The VL82C425 detects writes to protected areas and inhibits the generation of –CWE3 - –CWE0 and –TAGWE on a write-hit.

Registers AWPT, BWPT, CWPT, DWPT, EWPT and FWPT are used to define the Segment Cacheability. They are indexed configuration registers and are accessed via the index and data ports at I/O addresses ECh and EDh. They have the following format and index address:

The registers are written by writing the register index address (13h to 18h) into I/O port ECh. The data to be loaded into the selected register is then written to the data port EDh (see "Configuration Registers" section).

For compatibility with the VL82C486 Controller, the Write-Protect Registers cannot be read unless the WPTREN bit is set in the Cache Mode Register. An I/O read of these registers is ignored when WPTREN is 0 and all VL82C425 interface signals remain inactive or three-state. An IO write occurs regardless of the state of WPTREN but –RDY is returned by the VL82C425 only if WPTREN is 1. The data is latched into the VL82C425 at the end of the second T2 (1 wait state write)

TABLE 4. WRITE-PROTECT REGISTERS

STARTING ADDRESS (A19-A0) OF EACH 16KB REGION (A31-A20=0)

WRITE ONLY (unless WPTREN bit is set)

Data Port EDh	D7	D6	D5	D4	D3	D2	D1	D0
AWPT (13h)	AC000	0	A8000	0	A4000	0	A0000	0
BWPT (14h)	BC000	0	B8000	0	B4000	0	B0000	0
CWPT (15h)	CC000	0	C8000	0	C4000	0	C0000	0
DWPT (16h)	DC000	0	D8000	0	D4000	0	D0000	0
EWPT (17h)	EC000	0	E8000	0	E4000	0	E0000	0
FWPT (18h)	FC000	0	F8000	0	F4000	0	F0000	0
Reset Value	0	0	0	0	0	0	0	0

0 = Not Write Protected
1 = Write Protected

regardless of the response of the VL82C486 or other system controller to the I/O cycle.

DIRECT ACCESS MODE AND DISABLE MODE

DIRECT ACCESS AND DISABLE MODE OPERATION

The Direct Access Mode allows the cache data SRAMs to be accessed as if they are ordinary memory on the local bus. This permits the BIOS to size the cache after power-on reset, hence avoiding the need for a different BIOS for each cache size.

When the Direct Access Mode is set the VL82C425 behaves as follows:

- Reads and writes to cache data SRAMs are both one wait-state cycles.
- The cache data RAM appears as regular memory in the CPU address space whenever A20 = 1 or A19 =0. All reads are forced to be read-hits and all writes are forced to be write-hits, regardless of the tag compare result, and the –MISS pin is forced high. In this mode, one wait state writes will update the tag RAM with the current address as normal, but the DIRTY bit will be cleared instead of set.
- When A20 = 0 and A19 = 1 the cache is disabled and the –MISS pin is forced low. All reads and writes are forced to be misses regardless of the tag compare result.
- The cache size is assumed to be the maximum possible; 1MB. This allows correct initialization of the TAG values, as only A26-A20 will be loaded into the TAG SRAM(s). A26-A22 will always be zero, and A21-A20 map to the same TAG bit regardless of the cache size (see section entitled "Tag Address Assignment").

This mode allows the cache to be correctly sized and the tag to be initialized to values that map to cacheable memory locations.

When the cache is disabled (CSIZE2-CSIZE0 == 000) all memory accesses are forced to miss the cache, the cache RAM is never read or written to, and the –MISS pin is forced permanently low.

USE OF DIRECT ACCESS MODE FOR CACHE SIZING AND INITIALIZATION

The Direct Access Mode is used to size the cache at system initialization as follows:

1. The VL82C425 is put in the Direct Access Mode by setting CSIZE = 111 in the Mode Register.
2. With DBLBNK = 0 in the Mode Register and the 486 primary cache turned off, four double words are written to location 0. They are then read back and the data compared with that written. If the compare is good, then only one bank of SRAM is present. If the compare is bad, then two banks are present and the DBLBNK bit in the Mode Register must be set.
3. Location 00100000h (at 1MB) is cleared.
4. A unique value is written to location 00110000h (1M + 64K). Location 00100000h is read; if the value written to location 00110000h aliases to location 00100000h then the cache size is 64 KB and steps 5, 6, and 7 are skipped.
5. A unique value is written to location 00120000h (1M + 128K). Location 00100000h is read; if the value written to location 00120000h aliases to location 00100000h then the cache size is 128KB and steps 6 and 7 are skipped.
6. A unique value is written to location 00140000h (1M + 256K). Location 00100000h is read; if the value written to location 00140000h aliases to location 00100000h then the cache size is 256KB and step 7 is skipped.
7. A unique value is written to location 00180000h (1M + 512K). Location 00100000h is read; if the value written to location 00180000h aliases to location 00100000h then the cache size is 512KB. If not, then the cache size is 1MB.
8. The cache tags are initialized to point to valid DRAM locations by writing any value from location 0 to location [0 + cache-size] up to address 0007FFFFh (512K). Direct access mode forces write hits during this operation. If the cache size is 1 MB, then the second-half of the cache is initialized by writing locations 00180000h to 001FFFFFh This higher address range is used to meet the requirement of A20 = 1; at least 2MB of DRAM must be installed. Note that during this initialization, the DIRTY bit is cleared for all tags. Following completion of all steps of this procedure, these addresses must be rewritten, with the cache operating normally, in order to set the DIRTY bit for all tags if the data written during initialization is expected to be valid memory data.
9. The CSIZE field in the Mode Register is set to the computed cache size to enable the cache.
10. If the amount of DRAM installed is less than or equal to the cacheable range for a 7-bit tag (see section entitled "Cache Size and Range Options), then the TSIZE8 bit in the Mode Register may be left set at 0. If not, then the presence of an 8-bit tag may be tested for as follows:
    - Initialize and enable the cache (steps 1 to 9).
    - Set TSIZE8 = 1.
    - Write a unique value to DRAM location 0 and read it back to load cache location 0.
    - Read:
      location 0080000h (8MB) if cache size = 64KB
      or location 01000000h (16 MB) if cache size = 128KB
      or location 02000000h (32MB) if cache size = 256KB
      or location 04000000h (64MB) if cache size = 512KB
      or location 08000000h (128MB) if cache size = 1MB
    - If the location read aliases to location 0 (i.e., the value read is the same as that written to location 0) then only 7 tag bits exist and TSIZE8 must be set to 0.

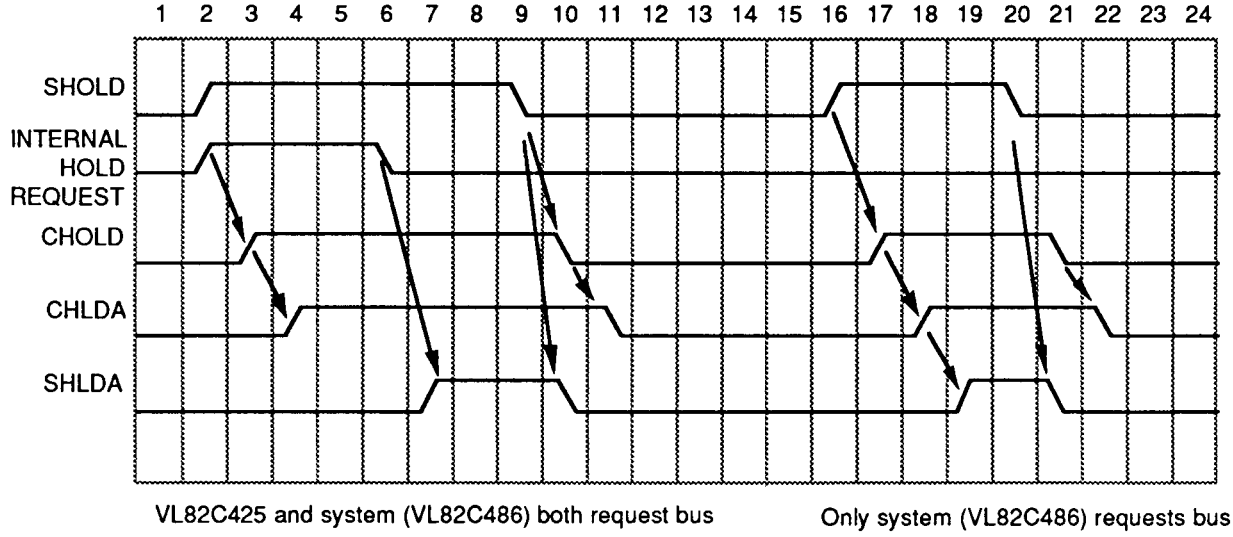
BUS ARBITRATION

Bus arbitration is performed by daisy chaining the SHOLD and CHOLD signals, and the SHLDA and CHLDA signals. The VL82C425 uses the CHOLD output and CHLDA input to request mastership of the local bus for performing line swapping during read-misses. It also passes on requests and acknowledges for the VL82C486 and other bus masters as follows:

- The SHOLD input signal is delayed by one clock cycle and sets the CHOLD output when active.
- The CHLDA input is delayed by one clock cycle and asserts the SHLDA output when active only if the VL82C425 is not also requesting bus mastership by asserting its internal HOLD request.
- SHLDA is de-asserted one clock after SHOLD is de-asserted.

The local bus arbitration timing is shown in Figure 11.

FIGURE 11. LOCAL BUS ARBITRATION TIMING



CONFIGURATION REGISTERS

REGISTER ACCESS

There are seven configuration registers comprising one mode register and six write-protect registers. Each of these registers is accessed via the indexed configuration ports at ECh and EDh. To access one of the registers, its configuration index is first written to I/O port ECh (the index will be loaded from byte 0 of the data bus). Data may then be read from or written to the selected register by reading or writing I/O port EDh (the data will be read from/enabled onto byte 1 of the data bus). See Figures 12 and 13.

The response of the VL82C425 to these accesses is controlled by the WPTREN bit of mode register 19h, see below. It defaults to write-only, with no –RDY returned by the VL82C425; the VL82C425 will not respond to reads of ECh or EDh. All accesses of these configuration registers are treated as one wait-state cycles.

The configuration index for the cache mode register is 19h. The configuration indexes for the write-protect registers are 13h to 18h.

The write-protect registers are normally shadows of the write-protect registers in the VL82C486. Therefore the VL82C425 ignores reads of these registers, since the data and assertion of –RDY will be supplied by the VL82C486. Similarly on writes to these registers, the VL82C425 updates them from byte 1 of the data bus, but does not assert –RDY, as this will be done by the VL82C486. When the VL82C425 is used with system controllers other than the VL82C486, the WPTREN (write-protect register read-enable) bit may be set which causes the VL82C425 to place the contents of the registers on byte 1 of the data bus during read accesses, and to assert –RDY during both read and write accesses. I/O reads and writes of the cache mode register behave identically to those of the write-protect registers. On an I/O read of this location, the VL82C486 will drive undefined data from the ISA bus onto the local bus and return RDY, thus the VL82C425 must

FIGURE 12. CONFIGURATION REGISTER ACCESS - WPTREN = 1

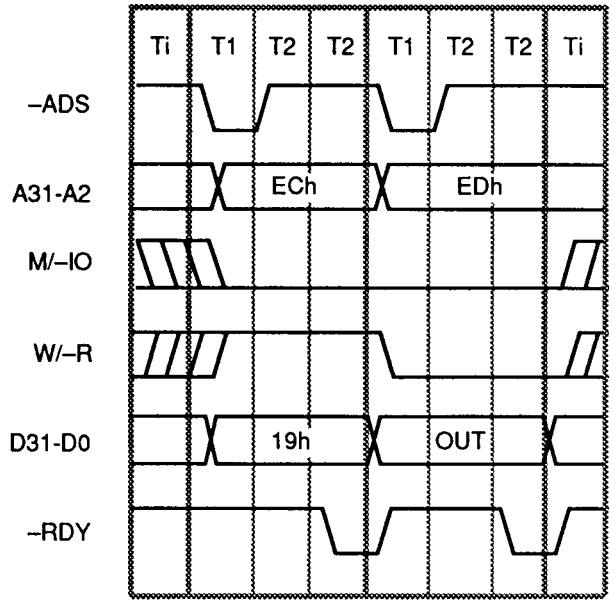
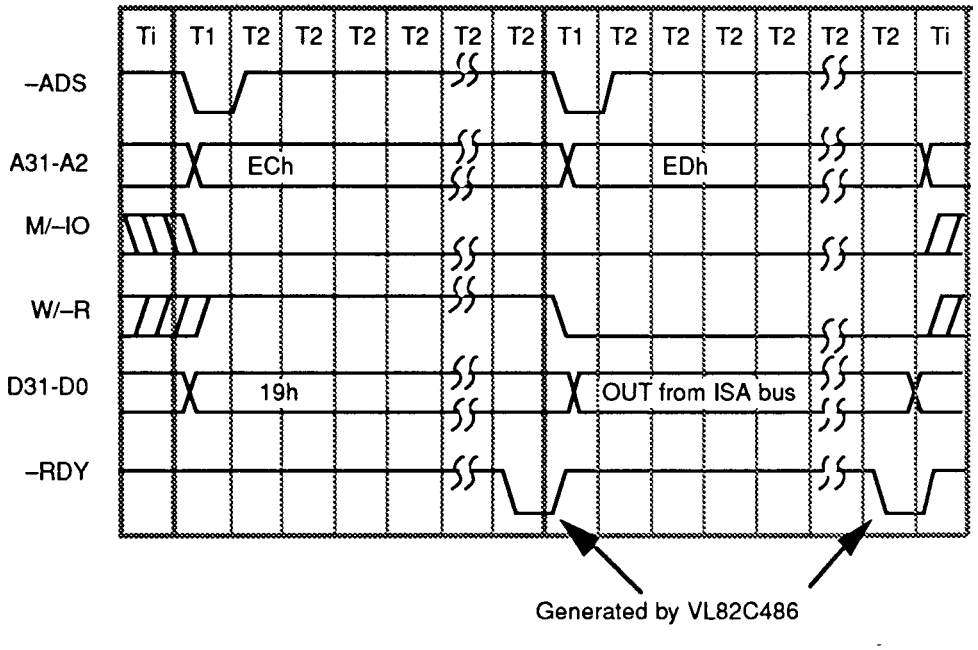


FIGURE 13. CONFIGURATION REGISTER ACCESS - WPTREN = 0



not respond, as with the write-protect registers.

Similarly, the index register at ECh is also a shadow of a VL82C486 register, and when the WPTREN bit is cleared, it is assumed that a VL82C486 is present and will respond by supplying data on reads and by asserting –RDY for reads and writes on accesses to the index register, and the VL82C425 is inhibited from doing the same. Again, by setting WPTREN, the VL82C425 will supply the value of ECh on byte 0 of the data bus and will assert –RDY for reads/ writes of ECh. On reads of ECh, if WPTREN is set, the VL82C425 will also drive the contents of EDh onto byte 1 of the data bus. Similarly, on reads of EDh with WPTREN set, the VL82C425 will also drive the contents of ECh onto byte 0 of the data bus.

REGISTER FORMATS

The format of the write-protect registers is described in section entitled "Cacheability Control". The format of the mode register is shown in Table 5.

All VL82C425 registers are summarized by Table 6.

TEST MODES

The VL82C425 incorporates logic to ease system board testing. Pulling the SHLDA/–TRI input low while RESET is high causes all output and bidirectional pins on the VL82C425 Cache Controller to go to a high-impedance state. This mode isolates the VL82C425 so that other components in the system can be tested.

TABLE 5. MODE REGISTER FORMAT

READ/WRITE

DATAPORT 0EDh	D7	D6	D5	D4	D3	D2	D1	D0
MODE	DBLBNK (19h)	RES	TSIZE8	WPTREN	RES	CSIZE2	CSIZE1	CSIZE0
Reset Value	0	0	0	0	0	0	0	0

BIT	NAME	FUNCTION
7	DBLBNK	Indicates number of cache banks. 0 = single cache bank 1 = two cache banks
6	RES	Reserved; Must be written as 0.
5	TSIZE8	Sets tag size as follows: 0 = 7 bits of tag address are used 1 = 8 bits of tag address are used
4	WPTREN	Write-protect and mode configuration registers read-enable 0 = configuration registers cannot be read, read cycle is ignored 1 = configuration registers can be read.
3	RES	Reserved; Must be written as 0.
2-0	CSIZE2 CSIZE0	Sets cache size as follows: 000 - cache disabled 001 - unused 010 - cache size is 64 KB 011 - cache size is 128 KB 100 - cache size is 256 KB 101 - cache size is 512 KB 110 - cache size is 1 MB 111 - Direct Access Mode (see section entitled "Direct Access Mode and Disable Mode")

TABLE 6. REGISTER SUMMARY

INDEX PORT (R/W) **ECh**

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

INDEX ADDRESS OF A CONFIGURATION REGISTER

DATA PORT (R/W) **EDh**

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

DATA FOR A CONFIGURATION REGISTER

MODE (R/W) **19h**

7	6	5	4	3	2	1	0
0	0	0	0	0	000		
DBLBNK	RES	TSIZE8	WPTREN	RES	CSIZE2 - CSIZE0		

Data SRAMs:
0 = 1 Bank
1 = 2 Banks

Tag Size:
0 = 7 bit
1 = 8 bit

Write-protect
read-enable

Cache Size:
000 - Cache Disable
001 - Unused
010 - 64 KB
011 - 128 KB
100 - 256 KB
101 - 512 KB
110 - 1 MB
111 - Direct Access

A0000h-FFFFFh SEGMENT WRITE-PROTECTION CONTROL REGISTERS **13h - 18h**
AWPT, BWPT, CWPT, DWPT, EWPT, FWPT (WRITE ONLY UNLESS WPTREN SET)

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0
AC000	0	A8000	0	A4000	0	A0000	0
BC000	0	B8000	0	B4000	0	B0000	0
CC000	0	C8000	0	C4000	0	C0000	0
DC000	0	D8000	0	D4000	0	D0000	0
EC000	0	E8000	0	E4000	0	E0000	0
FC000	0	F8000	0	F4000	0	F0000	0

0 -> NOT WRITE PROTECTED
1 -> WRITE PROTECTED

FIGURE 14. CLOCK WAVEFORMS

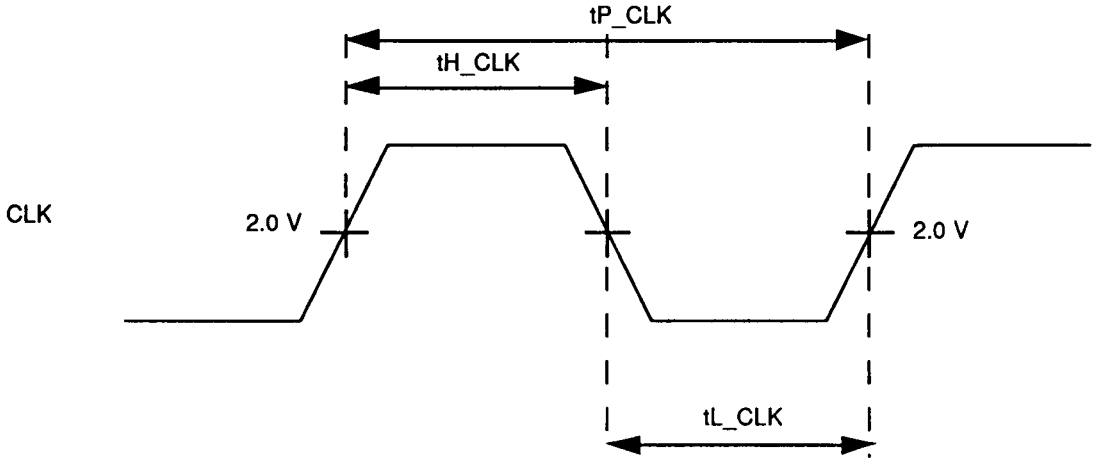
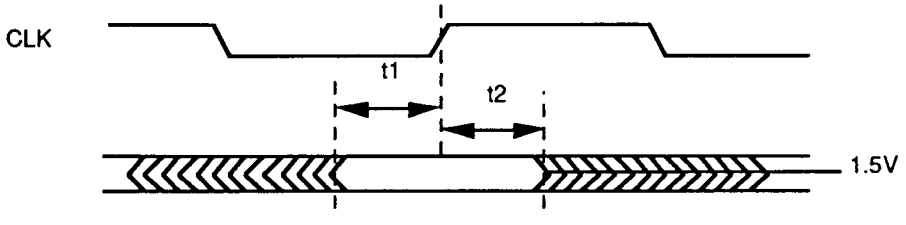


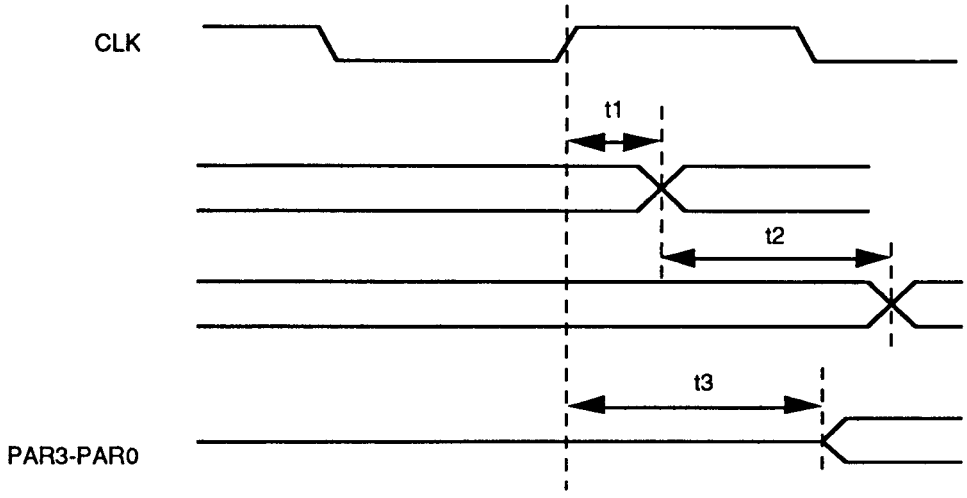
FIGURE 15. AC TIMING - CPU INTERFACE



t1 = tS1_CPU, tS3_CPU, tS4_CPU, tS5_CPU
tS6_CPU, tS7_CPU, tS8_CPU

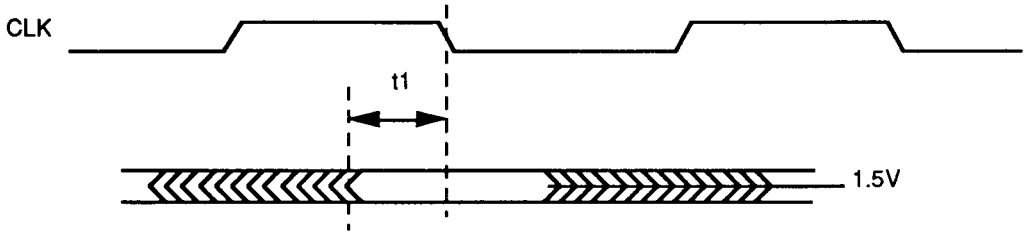
t2 = tH3_CPU, tH4_CPU, tH5_CPU
tH6_CPU, tH7_CPU, tH8_CPU,

FIGURE 16. AC TIMING - CPU INTERFACE



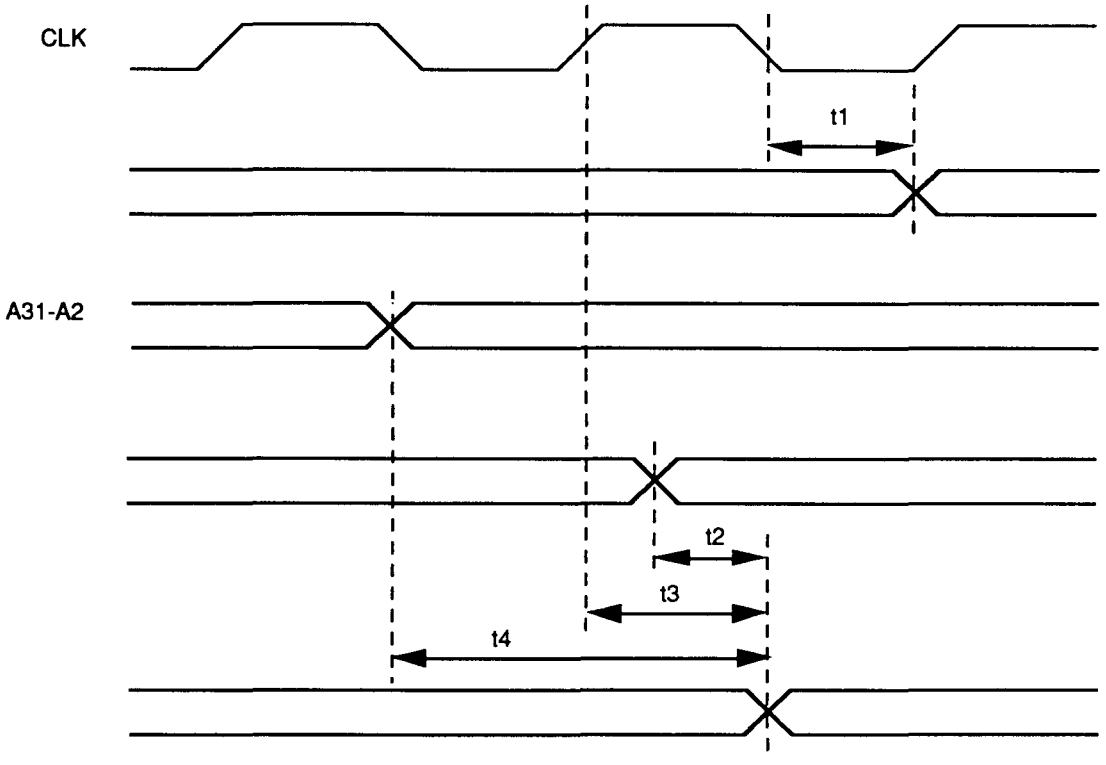
t1 = tD1_CPU, tD2_CPU, tD5_CPU, tD5a_CPU, tD8_CPU, tD9_CPU
t2 = tD3_CPU, tD4_CPU, tD6_CPU
t3 = tD7_CPU

FIGURE 17. AC TIMING - CACHE INTERFACE



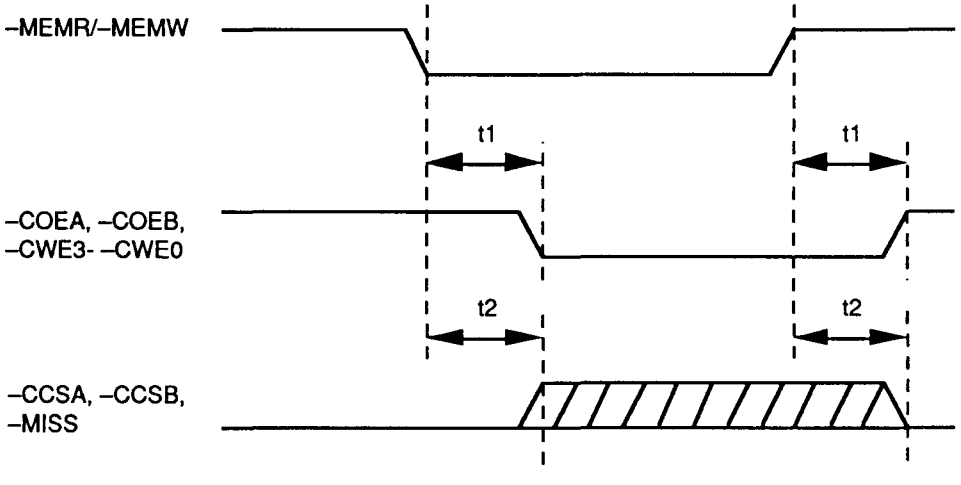
t1 = tS1_CH

FIGURE 18. AC TIMING - CACHE INTERFACE



t1 = tD8_CH, tD9_CH
t2 = tD6_CH
t3 = tD1_CH, tD1a_CH, tD1b_CH, tD2_CH, tD3_CH, tD5_CH
t4 = tD4_CH, tD7_CH

FIGURE 19. AC TIMINGS - ISA BUS INTERFACE



t1 = tD1_ISA, tD3_ISA
t2 = tD2_ISA, tD4_ISA

AC CHARACTERISTICS: TA = 0°C to +70°C, VDD = 5.0 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
Clocks						
f_CLK	CLK Frequency		33	MHz		Processor Clock
tP_CLK	CLK Period	30		ns	14	
tH_CLK	CLK High Time	13		ns	14	VIL = VIH = 2.0 V
tL_CLK	CLK Low Time	13		ns	14	VIL = VIH = 2.0 V
CPU Interface Timing						
tS1_CPU	–ADS, A31-A2, –BE3- –BE0, M/–O, W/–R, D/–C, to CLK setup time	13		ns	15	When clocked at the end of T1
tS3_CPU	–BLAST to CLK setup time	9		ns	15	During read hit cycles
tS4_CPU	–RDY, –BRDY to CLK setup time	5		ns	15	During read miss and write-back cycles
tS5_CPU	D31-D0 to CLK setup time	5		ns	15	During read miss cycles, configuration reg. write cycles
tS6_CPU	–KEN to CLK setup time	5		ns	15	During read miss cycles
tS7_CPU	CHLDA to CLK setup time	13		ns	15	Local bus grant
tS8_CPU	SHOLD to CLK setup time	6		ns	15	Arbitration Request
tH3_CPU	–BLAST from CLK hold time	5		ns	15	
tH4_CPU	–RDY, –BRDY from CLK hold time	5		ns	15	
tH5_CPU	D31-D0 from CLK hold time	5		ns	15	
tH6_CPU	–KEN from CLK hold time	5		ns	15	
tH7_CPU	CHLDA from CLK hold time	5		ns	15	
tH8_CPU	SHOLD from CLK hold time	5		ns	15	
tD1_CPU	CLK to –ADS, A31-A2, –BE3- –BE0, M/–O, W/–R, D/–C output delay		15	ns	16	During write-back cycles or line swaps
tD2_CPU	DLK to –RDY, –BRDY output delay		24	ns	16	During read hit and write hit cycles
tD3_CPU	A31-A16 to –RDY, –BRDY output delay		39	ns	16	For first –BRDY for read hits
tD4_CPU	TAG7-TAG0 to –RDY, –BRDY output delay		19	ns	16	First –BRDY for read hit
tD5_CPU	CLK to D31-D0 output delay		24	ns	16	During read-miss cycles for line-buffer write to cache
tD5a_CPU	CLK to D31-D0 output delay		28	ns	16	During configuration register reads (with WPTREN set)
tD6_CPU	D31-D0 to PAR3-PAR0 output delay		20	ns	16	Generate parity during write-backs
tD7_CPU	CLK to PAR3-PAR0 enable delay		20	ns	16	PAR3-PAR0 outputs enabled at beginning of write-back cycle
tD8_CPU	CLK to SHLDA output delay		16	ns	16	Arbitration grant
tD9_CPU	CLK to CHOLD output delay		23	ns	16	Local bus request

AC CHARACTERISTICS (Cont.): TA = 0°C to +70°C, VDD = 5.0 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Unit	Figure	Condition
Cache Controller Interface Timing						
tS1_CH	TAG7-TAG0, DIRTY to CLK falling setup time	8		ns	17	Cache write hit, to negative edge of CLK in T2
tD1_CH	CLK to –COEA, –COEB delay		12	ns	18	Double-bank read hit
tD1a_CH	CLK to –COEA, –COEB delay		18	ns	18	First double word of write-back
tD1b_CH	CLK to –COEA delay		22	ns	18	Single-bank read hit
tD2_CH	CLK to –CCSA, –CCSB delay		15	ns	18	To de-assert for unselected bank during cache writes (write hits/line swaps)
tD3_CH	CLK to CA3A, CA3BA2 delay		15	ns	18	During read hit cycles, write-back cycles, and line-swap cycles
tD4_CH	A3, A2 to CA3A, CA3BA2 delay		14	ns	18	During T1/T2 of read hit cycle
tD5_CH	CLK to –MISS output delay		16	ns	18	
tD6_CH	TAG7-TAG0 to –MISS output delay		11	ns	18	
tD7_CH	A31-A16 to –MISS output delay		30	ns	18	
tD8_CH	CLK falling to –TAGWE, –CWE3- –CWE0 output delay		14	ns	18	TAG and data SRAM update on write hit and read miss
tD9_CH	CLK falling to TAG7-TAG0, DIRTY output delay		19	ns	18	During line swap phase of read miss cycles
ISA Bus Interface Timing						
tD1_ISA	–MEMR to –COEA, –COEB delay		25	ns	19	Snoop data on ISA read hit
tD2_ISA	–MEMW to –CCSA, –CCSB delay		25	ns	19	Disable unselected bank on ISA write hit
tD3_ISA	–MEMW to –CWE3- –CWE0 delay		25	ns	19	Update data RAM on ISA write hit
tD4_ISA	–MEMR/W to –MISS delay		20	ns	19	

Notes:

The following loads are used for measurement of all AC Characteristics.

Load (pF)	Pin(s)
50	–BE3- –BE0, TAG7-TAG0, DIRTY, –MISS, –TAGWE, –BLAST, –BRDY, M/–IO, D/–C, W/–R, CHOLD, –ADS, SHLDA, –RDY
100	A31-A2
120	CA3A, CA3BA2, –CWE3- –CWE0, –COEA, –COEB, –CCSA, –CCSB
150	PAR3-PAR0
170	D31-D0

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature –10°C to +70°C

Storage Temperature –65°C to +150°C

Supply Voltage to Ground Potential –0.5 V to 7.0 V

Applied Output Voltage –0.5 V to VDD + 0.3 V

Applied Input Voltage –0.5 V to VDD + 0.3 V

Power Dissipation 500 mW

Stresses above those listed may cause permanent damage to the device. These are stress ratings only, functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

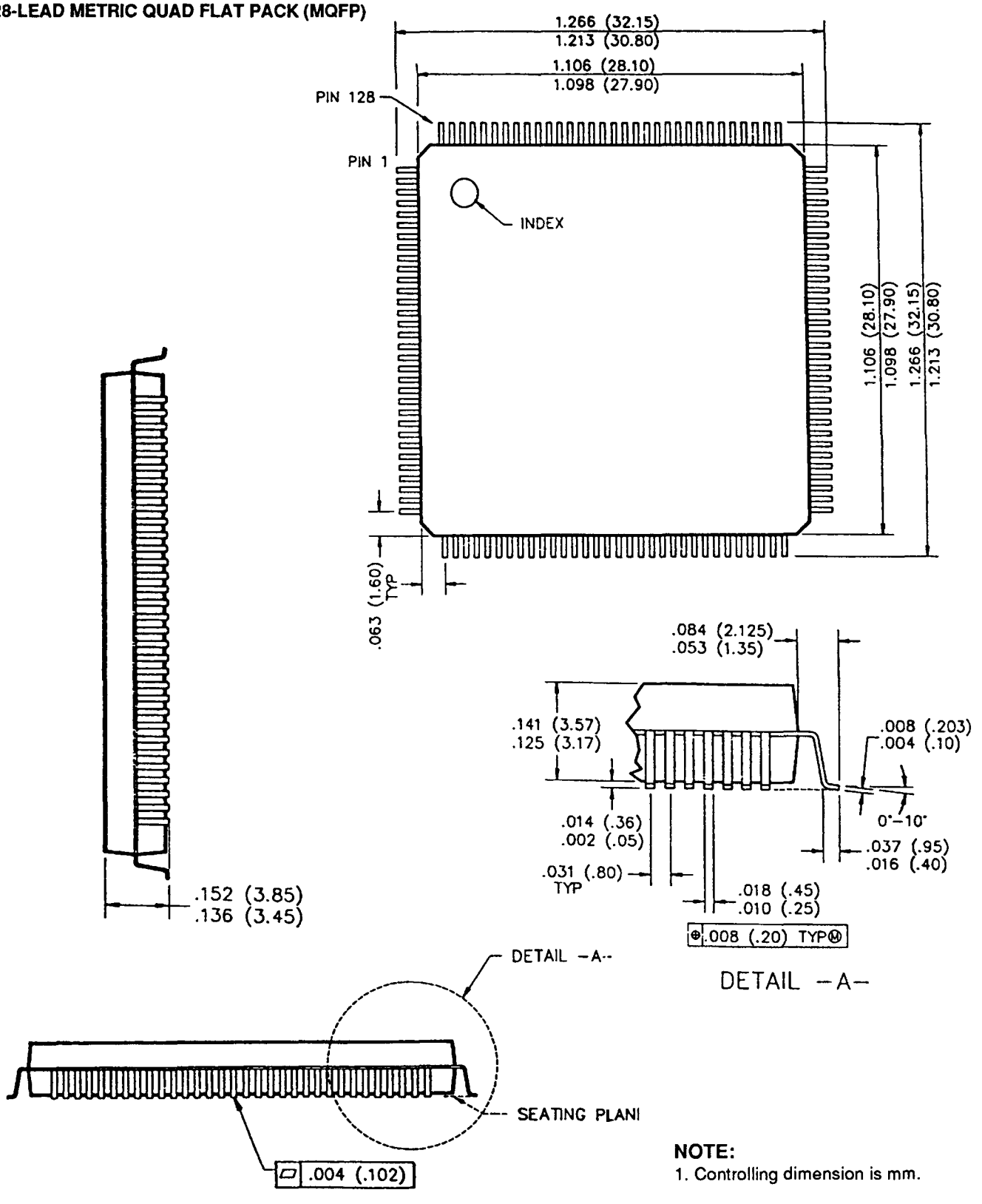
DC CHARACTERISTICS - 5.0 VOLT OPERATION: TA = 0°C to 70°C, VDD = 5.0 V ±5%, VSS = 0 V

Symbol	Parameter	Min	Max	Units	Conditions
VIL	Input Low Voltage	–0.5	0.8	V	TTL Level Inputs, Notes 1,2
VIH	Input High Voltage	2.0	VDD + 0.5	V	TTL Level Inputs, Note 1
VIH2	Input High Voltage	2.4	VDD + 0.5	V	Schmitt Trigger Input, Note 2
VILC	Input Low Voltage	–0.5	0.8	V	CMOS Level Inputs, Note 3
VIHC	Input High Voltage	VDD - 0.8	VDD + 0.5	V	CMOS Level Inputs, Note 3
VOL1	Output Low Voltage		0.45	V	IOL = 8 mA, Note 4
VOH1	Output High Voltage	VDD - 0.45		V	IOH = –2 mA, Note 5
VOL2	Output Low Voltage		0.45	V	IOL = 16 mA, Note 6
VOH2	Output High Voltage	VDD - 0.45		V	IOH = –3 mA, Note 6
IIL1	Input Low Current	–10		µA	VIN = 0.2 V, Note 7
IIL2	Input Low Current	–500	–50	µA	VIN = 0.8 V, Note 8
IIH	Input Leakage Current		10	µA	VIN = VDD, Note 7
ILO	Output Three-state	–100		µA	VIN = 0.2 V, Note 9
	Leakage Current		100	µA	VIN = VDD
IDDSB	Static Power Supply Current		50	µA	
IDDOP	Dynamic Power Supply Current		4	mA/ MHz	No DC Loads
CI	Input or I/O Capacitance		10	pF	Not tested
CO	Output Capacitance		10	pF	Not tested

Notes:
1. Pins: CHLDA, SHOLD, –KEN, SHLDA, –MEMR, –MEMW, –REFRESH, A31-A2, –BE3 - –BE0, CA3A, CA3BA2, D31-D0, TAG7-TAG0, DIRTY, –BLAST, –BRDY, M/–IO, D/–C, W/–R, –ADS, –RDY
2. RESET
3. Pin: CLK
4. Pins: A31-A2, –BE3- –BE0, D31-D0, PAR3-PAR0, TAG7-TAG0, DIRTY, –CCSA, –CCSB, –BLAST, CHOLD, –ADS, SHLDA
5. Pins: A27-A2, D31-D0, PAR3-PAR0, TAG7-TAG0, DIRTY, –CCSA, –CCSB, M/–IO, D/–C, W/–R, CHOLD, –ADS, SHLDA
6. Pins: –MISS, –CWE3- –CWE0, CA3A, CA3BA2, –COEA, –COEB, –TAGWE, –BRDY, –RDY
7. Pins: CHLDA, SHOLD, –KEN, RESET, –MEMR, –MEMW, –REFRESH, CLK
8. Pins: TAG7, SHLDA
9. Pins: A31-A2, –BE3- –BE0, CA3A, CA3BA2, D31-D0, PAR3-PAR0, TAG6-TAG0, DIRTY, –BLAST, –BRDY, M/–IO, D/–C, W/–R, –ADS, –RDY, –CCSA, –CCSB, –MISS, –CWE3- –CWE0, –COEA, –COEB, –TAGWE, CHOLD

PACKAGE OUTLINE

128-LEAD METRIC QUAD FLAT PACK (MQFP)



NOTE:

1. Controlling dimension is mm.

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7/92

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