386SX MICRO CHANNEL CHIP SET
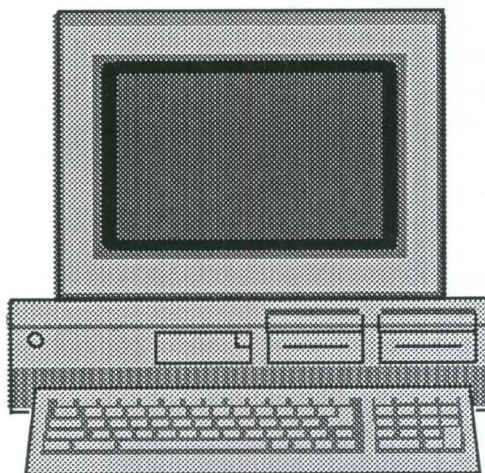## VL82C700 BUS/MEMORY CONTROLLER
VL82C701 I/O CONTROLLER

GUARANTEED 100% COMPATIBLE

COMPLETE TWO-CHIP SOLUTION

20 MHz

LOCAL/MCA BUS, MEMORY, AND I/O CONTROL

OVERVIEW

The VL82C700 and VL82C701 from VLSI Technology, Inc. compose a Micro Channel® chip set for 80386SX-based systems running at 20 MHz. The chip set is guaranteed to be 100% compatible with IBM® PS/2® model 57 computers. It is a highly integrated solution which helps to reduce time-to-market, motherboard real estate and cost, and system NRE costs.

All local and system (MCA®) bus interface, conversion, and arbitration functions are implemented on-chip, along with a very complete array of I/O control blocks: keyboard/mouse controller, serial and parallel ports, dual digital joystick interface, 15-level programmable priority interrupt controller, eight-channel DMA controller, programmable peripheral interface Port B, port 91/92, and 82077 floppy controller support. In addition, these devices provide numeric coprocessor support, system reset logic, DRAM refresh and parity, a three-channel timer and a 32-bit free-running timer.

The VL82C700 integrates all the local and system bus arbitration and conversion, DRAM control, reset logic, and coprocessor support; the VL82C701 controls the I/O ports, interrupts, timers, and real-time clock.

Both devices are implemented in 1.0-micron CMOS technology and are available in a 208-lead plastic quad flat pack (PQFP) with lead spacing of 0.5 mm (20 mils).

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Bus/memory controller

The VL82C700 bus/memory controller is a Micro Channel level B device: 16 bits data, 24-bit address. It will support the fastest local bus cycle possible for any given operation. Whenever feasible, it will operate with two bus states in the pipelined or non-pipelined mode of operation (both are supported). As a slave, the device will request address pipelining from any bus master to insure that the address decode and cycle definition can be determined as early as possible. Pipelining is supported on both DRAM cycles and Micro Channel cycles. Local bus masters and slaves are supported.

An extension to the 386SX bus has been defined to accommodate local bus masters. The VL82C700 is the central arbitration point for the local bus, allowing each local bus device to request and compete for control of the bus. Each local bus master is assigned an arbitration level on the Micro Channel (MC) bus, and is allowed to perform MC cycles under arbitration. All other MC masters are restricted to cycles during bus grant.

An interface between the MC and the 386SX bus is accomplished by snooping both buses looking for cycles that cross between the buses. The VL82C700 behaves as a MC master when a local bus master owns the MC and as a MC slave when when an alternate MC master owns the MC. Data steering for transfers between the buses is provided on-chip.

Direct Memory Access (DMA) to peripheral I/O devices is also provided by the bus/memory controller. The DMA controller also provides central arbitration control for the memory system. DMA clock frequency is 10 MHz.

The memory controller section provides interface to, and control of, system memory for all devices, including local and MC bus masters. DRAM SIMMs with 70 ns page access times are supported (SIMM implementations of 1M/2M x 36 DRAM). The controller is designed for zero wait-state page-hit read and page-hit write modes, as well as page interleaving mode for certain DRAM configurations.

In addition, the memory controller supports: up to three SIMMs on the motherboard, each holding 1, 2, 4, or 8MB for a maximum of 16MB; memory remapping which allows memory in the 640KB-1MB range to be accessed from a different address range; memory enabling which allows bad memory to be removed from the system without pulling the memory card; 150 ns ROM, which may be copied into RAM for faster BIOS execution; a second 128KB ROM using the ROM_PAGE command; DBCS, insuring compatibility with Kanji video; and one wait-state I/O cycles.

RAS-only refresh is also performed by the VL82C700 memory controller, using RAS select with CAS held inactive. The frequency of refresh is selectable to 2.0 msec or 15.0 msec. The first setting is usually used during memory

initialization, and the second is used during normal operation. Refresh rate is the same for both 1Mb and 4Mb DRAMs.

The VL82C700 provides additional support such as numeric coprocessor interface logic, in-circuit test mode, and 386SX isolation for attachment of an in-circuit emulator.

I/O controller

The VL82C701 I/O Controller operates in conjunction with the VL82C700 Bus/Memory Controller. The VL82C701 provides MC interface to the system's dedicated I/O subsystems, such as floppy controller, parallel port, serial ports, RTC, keyboard, etc. The I/O Controller monitors arbitration levels on the MC arbitration bus and presents this bus with arbitration levels from the peripherals. These arbitration patterns are used by "local arbiters" in determining whether a particular peripheral has sufficient arbitration level to win control of the MC, and by the VL82C700 chip to determine when to grant the bus.

The I/O Controller also implements several advanced I/O subsystems on-chip: an enhanced parallel printer port (utilizing DMA, bidirectional communication and bidirectional interrupt, scanner and streaming tape support); two enhanced RS232 serial ports (programmable into FIFO or DMA mode, four DMA channels for transmit and receive, received data status, new start and stop transmit commands, modem pacing,

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386SX MICRO CHANNEL CHIP SET

FEATURES

- Two-chip, MCA chip set designed for use in 20 MHz 80386SX systems

- Two 208-lead plastic quad flat packs

- Highly integrated solution: VL82C700 includes bus arbitration, DMA control, DRAM control, system reset logic, refresh control

- Highly integrated solution: VL82C701 includes interrupt controller, RTC interface, timers, keyboard/mouse controller, joystick port, serial and parallel ports, floppy controller support plus MC interface and arbitration logic for I/O devices

- Advanced serial and parallel ports: DMA access, enhanced command set

- Guaranteed 100% IBM MCA compatible

- Memory control up to three SIMMs of 1, 2, 4, or 8MB DRAM

- DRAM parity generation and checking on-chip

- Programmable refresh timing

- Zero wait-state page-hit reads and page-hit writes

- In-circuit test modes

- 80386SX isolation/emulator support

BENEFITS

- Improves reliability, reduces NRE and production costs

- Reduces motherboard real estate requirements

- No need for external memory or bus interface and control chips; reduces NRE, board production cost

- No need for extensive glue logic or separate controller chips (except floppy and RTC); reduces NRE, board real estate and cost, increases reliability

- Increases product differentiation of the system

- Reduces compatibility testing time and time-to-market

- Allows flexible memory designs

- Reduces real estate requirements and provides a reliable design

- Optimizes system startup timing

- Enables high-performance system design and product differentiation

- Provides a means of in-board electrical testing and simplifies solder joint verification

- Easy access during development and debug

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386SX MICRO CHANNEL CHIP SET

I/O CONTROLLER (Cont.)

character-oriented pacing, byte pacing, receive character count, enhanced interrupts); keyboard and mouse controller (serial links to keyboard and mouse, error detection, processor interface, security lockout, priority control,

loop mode); 15-level programmable priority interrupt controller; tri-mode dual digital joystick controller (compatible, polling, and interrupt-driven modes).

A high level of integration has been employed in the design of the VL82C701. In addition to the functions described above, this device includes: Port B (audio

subsystem control, parity error check, I/O channel check, timer gate and IRQ0 reset) and Port 91/92 (feedback, hardfile light, hot reset, pass A20); a three-channel timer (system, tone, and watchdog); a 32-bit free-running timer; programmable option select (Port 94H - replaces switches from motherboard and slot cards with programmable latches); and support for a floppy disk drive controller and RTC.
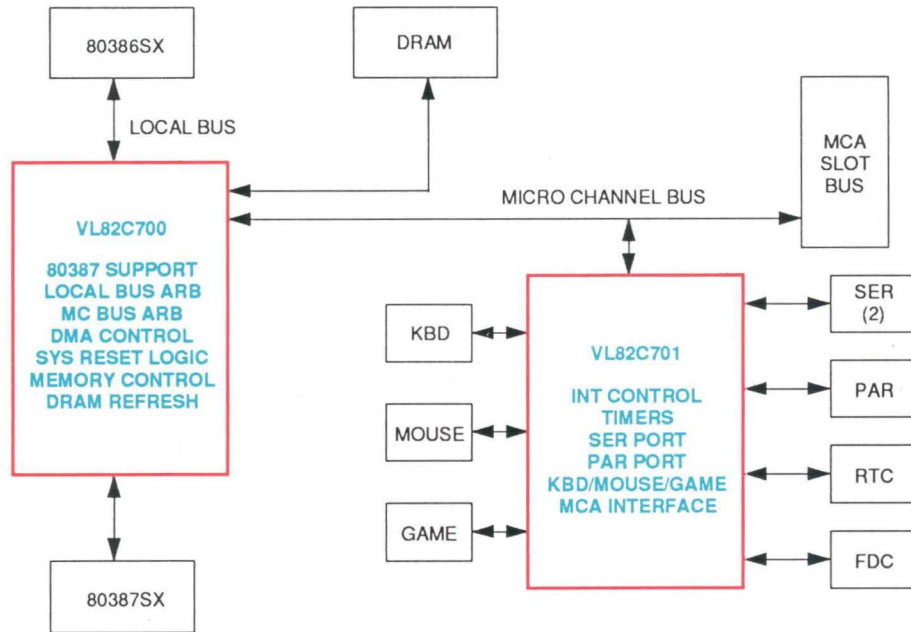
PACKAGING

PART NUMBER	DESCRIPTION	PACKAGE
VL82C700	MCA Bus/Memory Controller	208-lead Plastic Quad Flat Pack
VL82C701	MCA I/O Controller	208-lead Plastic Quad Flat Pack
NOTE: Operating temperature range is 0°C to +70°C		

SYSTEM SUPPORT

VLSI Technology offers extensive support for system designers to assist them in their design applications:

- Samples of the VL82C700 and VL82C701 MCA chip set
- Evaluation boards:
  - PS/2 model 57-compatible motherboard (20 MHz 80386SX-based system)
- Documentation:
  - Data sheets for the VL82C700/VL82C701
  - Sample schematics for 20 MHz 80386SX-based MCA system
  - Application notes
- Software
  - BIOS support by Phoenix Technologies (617-551-4282)

RELATED
PRODUCTS LISTING

VL82C286-SET – The TOPCAT 286/386SX is a very high-integration two-chip set for use in the design of PC/AT-compatible based systems. This chip set is intended for use in 80286 and 80386SX microprocessor-based systems with clock speeds from 12 to 25 MHz.

VL82C386-SET – The TOPCAT 386DX is a very high-integration three-chip set for use in the design of PC/AT-compatible based systems. This chip set is intended for use in 80386DX microprocessor-based systems with clock speeds from 16 to 33 MHz.

VL82C310/VL82C311/VL82C311L – The SCAMP Controller chips are very cost-effective mid-range featured chips that are designed for use in note-book, laptop, portable, and cached desktop PC/AT-compatible based systems. These chips are intended for use in 80286 microprocessor-based systems with clock speeds from 10 to 20 MHz and in the 80386SX microprocessor-based systems with clock speeds from 10 to 25 MHz.

VL82C106 – The Combination I/O chip, when used with the VLSI PC/AT-compatible chip set, allows designers to implement a very cost-effective minimum chip count motherboard containing functions that are common to virtually al l PCs.

VL82C107 – The SCAMP Combination I/O chip, when used with the VLSI SCAMP chips, allows designers to implement a very cost-effective minimum chip count motherboard. This chip combines a keyboard controller and a real-time clock with the address latches/buffers and DMA Acknowledge decoders which are normally required in SCAMP-based systems. The VL82C107 additionally contains circuitry necessary to interface PC Memory Cards to the system or provide the chip select and control signals for an external VL16C552 UART I/O device, FDC, and IDE interface.

VL82C113 – The SCAMP Combination I/O chip is an integrated peripheral controller that has been optimized for use with VLSI's VL82C486, VL82C310, VL82C311, and VL82C311L single chip controllers in PC/AT-compatible computer systems. This chip combines a keyboard controller and a real-time clock with the address latches/buffers which are normally required in PC/AT-compatible systems. The VL82C113 was developed with VLSI's 1.0 micron CMOS technology and is available in a 100-lead PQFP. When used with VLSI's single chip controllers, this chip allows designers to implement a very cost-effective minimum chip count motherboard.

VL82C312 – The SCAMP Power Management Unit (PMU) chip is intended to be used in conjunction with the VL82C310 SCAMP-LT chip and the VL82C107 SCAMP Combination chip. The PMU dramatically reduces overall system power consumption and provides special features for laptop/notebook PC/AT-compatible computers.

VL82C325 – The VL82C325 is a high-performance, highly integrated Cache Controller that is for systems based on VLSI's TOPCAT 286/386SX or SCAMP chip sets up to 25 MHz. It improves the overall system performance by reducing the number of wait states during non-cache cycles when compared to conventional cache controllers.

UART Family – Asynchronous communications elements that serve as serial data input/output interfaces in microcomputer systems. They perform serial-to-parallel conversion on data characters received from peripheral devices or modems, and parallel-to-serial conversion on data characters transmitted by the CPU.

- VL16C450 Single UART
- VL16C451B Single UART (enhanced VL16C451)
- VL16C452B Dual UART (enhanced VL16C452)
- VL16C550 Single enhanced UART (NSC-compatible)
- VL16C551 Single enhanced UART
- VL16C552 Dual enhanced UART
- VL16C554 Quad UART

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