WD10C27

Data

Separator

WESTERN DIGITAL

TABLE OF CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

LIST OF TABLES

1.0 INTRODUCTION

1.1 GENERAL DESCRIPTION

The WD10C27 Read/Write Channel is a fully integrated LSI device intended for variable frequency applications in conjunction with the WD61C22 Hard Disk Controller/Buffer Manager.

In a typical application, the WD10C27 performs all of the handling of the sensitive read/write signals between a disk controller and data drivers and receivers. Raw read data corresponds to previous write data, with added phase, frequency, and write splice noise added during read-back. The fundamental purpose of the WD10C27 is to remove these noise components and present a clean digital recovered data and reference clock to the controller. See Figure 1-1 - Signal/Pin Assignments.

1.2 FEATURES

- General
  - Specifically designed for the WD61C22 Hard Disk Controller/Buffer Manager
  - Supports Constant Density Recording with no component changes
  - 1.25 micron +5 volt only CMOS technology
  - Available in 64-pin SQFP and MQFP packages
- Frequency Synthesizer
  - Range of 7.5 - 33 MBps with resolution ≤140 KHz
  - Programmable input reference frequency to 40 MHz
- Microprocessor Interface
  - Eight bit Intel compatible multiplexed address/data port
  - Programmable test and low power modes
- Write Data Conditioner
  - Crystal controlled processing of the write data to eliminate pulse pairing
  - Programmable pattern dependent Skew Symmetric Precompensation matrix for precomp. of up to ±25% with 1.5% resolution
- Encoder/Decoder
  - IBM Compatible 1,7 RLL
  - Hard/soft sector support and Address Mark Detection/Generation
- Data Synchronizer
  - Precision internal self adjusting VCO compensates for component, temperature, voltage, and aging variations
  - Internal gain/bandwidth modulation linearizes loop gain and increases phase margin across zones
  - Dual gain charge pump for faster acquisition and better jitter rejection while tracking
  - Dual mode phase/phase-frequency detector eliminating quadrature and harmonic lock
  - µP controlled Window Shift Synthesis for window shifting from 0% to ±50% of the window
  - Window monitoring capability
- Channel Control
  - 5-bit DACs specifically designed for use with the SSI3040 Electronic Filter/Pulse Detector
  - Independent Servo/Data Filter Optimization
  - Bandwidth, Boost and Hysteresis Control for ZBR
  - Five Programmable Microprocessor Ports

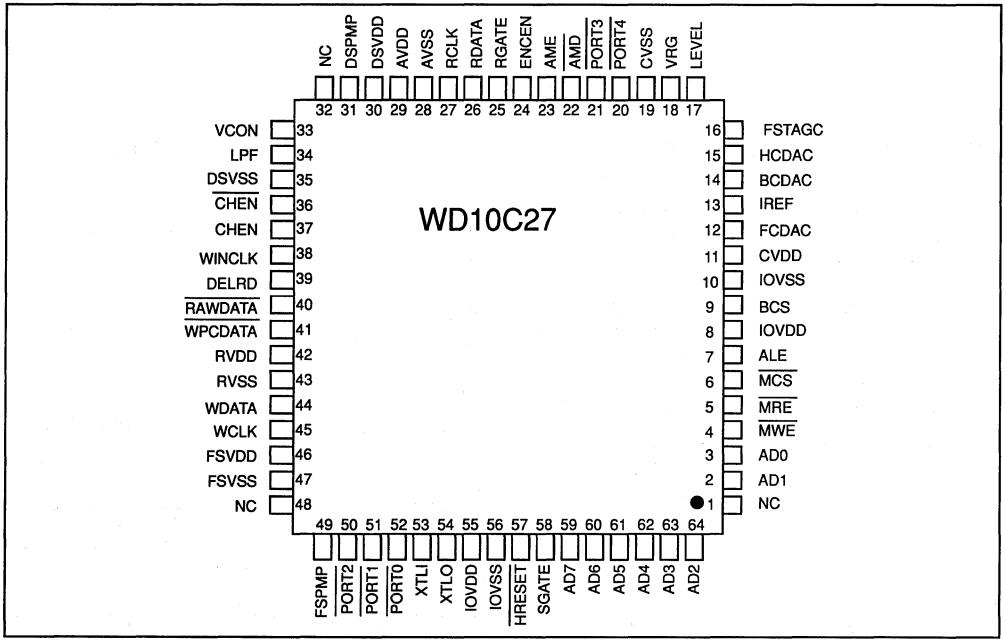


FIGURE 1-1. SIGNAL/PIN ASSIGNMENTS

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
59-64, 2-3	AD7-0	I/O	**Address/Data Bus** ADDRESS inputs used in conjunction with ALE to select the internal register to be transmitted or received on the DATA input/outputs.
4	$\overline{\text{MWE}}$	I	**$\overline{\text{Microprocessor Write Enable}}$** When asserted will transmit data from the AD bus into internal registers.
5	$\overline{\text{MRE}}$	I	**$\overline{\text{Microprocessor Read Enable}}$** When asserted will transmit data from internal registers onto the AD bus.
6(9†)	$\overline{\text{MCS}}$	I	**$\overline{\text{Microprocessor Chip Select}}$** When asserted allows information to be read from or written to the AD bus.
7	ALE	I	**Address Latch Enable** Address information is latched on the falling edge.
8,55	IOVDD	S	**I/O Supply** +5 volt supply to all I/O except $\overline{\text{WPCDATA}}$, $\overline{\text{RAWDATA}}$, and analog pins.
9(6†)	BCS	O	**Buffered Chip Select** This pin is the inverted, buffered version of the $\overline{\text{MCS}}$ input.
10,56	IOVSS	S	**I/O Ground** Dedicated ground to all I/O except $\overline{\text{WPCDATA}}$, $\overline{\text{RAWDATA}}$, and analog pins (designated "A").
11	CVDD	S	**Analog Supply** Dedicated +5v for the Channel Control DAC circuitry.
12(17)	FCDAC	A	**Freq. Ctl. DAC** Frequency Control current DAC output.
13(15)	IREF	A	**Current Reference** External current reference used to set the compliance of IDAC. When not used, IREF should be connected to CVSS.
14(18)	BCDAC	A	**Boost Ctl. DAC** Boost Control voltage DAC output.
15(13)	HCDAC	A	**Hyst. Ctl. DAC** Hysteresis Control voltage DAC output.
16(57)	FSTAGC	A	**Fast AGC** Discharge path to force fast AGC response.
17(12)	LEVEL	A	**Level** External voltage used to adjust the Hysteresis DAC offset. Should be tied to CVSS when not used.
18(14)	VRG	A	**Voltage Reference** External voltage reference used by the DAC circuits. Should be tied to CVSS when the Boost Control, Frequency Control, and Hysteresis Control DACs are not used.

TABLE 1-1. SIGNAL DESCRIPTIONS

21

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
19	CVSS	S	**Analog Ground** Dedicated ground for the Channel Control DAC circuitry.
20(58)	$\overline{\text{PORT4}}$	O	**$\overline{\text{Port Four}}$** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
21(36)	$\overline{\text{PORT3}}$	O	**$\overline{\text{Port Three}}$** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
22(24)	$\overline{\text{AMD}}$	O	**$\overline{\text{Address Mark Detect}}$** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
23(26)	AME	I	**Address Mark Enable** In soft sector, AME initiates an address mark search during reads, or address mark generation during writes.
24(22)	ENCEN	I	**Encode Enable** Asserted during write commands to enable the Encoder and associated write circuits.
25(27)	RGATE	I	**Read Gate** In soft sector, RGATE responds to $\overline{\text{AMD}}$ to validate the acquisition sequence during reads. In hard sector, RGATE initiates the acquisition sequence w/o $\overline{\text{AMD}}$ qualification.
26(23)	RDATA	O	**Recovered Data** Recovered NRZ read data represents the decoded RLL raw read data with all phase and frequency noise removed.
27(25)	RCLK	O	**Reference Clock** Nominally at the NRZ data frequency, RCLK tracks the low frequency variations on $\overline{\text{RAWDATA}}$ during reads, otherwise tracks the crystal reference.
28	AVSS	S	**Main Analog Ground** Main ground dedicated primarily to analog support circuitry (i.e., Delay Locked Loop, PLL Phase Detectors, etc.). This supply also supports the sensitive $\overline{\text{WPCDATA}}$ and $\overline{\text{RAWDATA}}$ I/O to prevent intermodulation with IOVDD /IOVSS.
29	AVDD	S	**Main Analog Supply** Main +5v supply dedicated primarily to analog support circuitry (i.e., Delay Locked Loop, PLL Phase Detectors, etc.) This supply also supports the sensitive $\overline{\text{WPCDATA}}$ and $\overline{\text{RAWDATA}}$ I/O to prevent intermodulation with IOVDD/IOVSS.
30	DSVDD	S	**Analog Supply** Dedicated +5v for the Data Synchronizer circuitry.
31(34)	DSPMP	A	**Data Synchronizer Pump** Charge pump to the data synchronizer PLL filter.
33(38)	VCON	A	**N-Channel Voltage Control** N-channel control voltage for the internal VCO and charge pump. This voltage is the filtered output of the charge pump.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
34(31)	LPF	A	**Low Pass Filter** Controls low pass filter characteristics under zone control via the AD bus.
35	DSVSS	S	**Analog Ground** Ground dedicated to the Data Synchronizer PLL.
36(21)	$\overline{\text{CHEN}}$	O	**$\overline{\text{Channel Enable}}$** This pin is an inverted, buffered version of the channel enable input, CHEN.
37(50)	CHEN	I	**Channel Enable** This input, active high when the Read/Write Channel Electronics are enabled, controls the state of the on-board DACs.
38(33)	WINCLK	O	**Window Clock** This output, when enabled, represents the window clock at the Data Detector and may be used for window monitoring. Phase detector pump down output in test mode.
39(41)	DELRD	O	**Delayed Read Data** This output, when enabled, represents the latched RAWDATA at the Data Detector and may be used for window monitoring. Phase detector pump up output in test mode.
40(45)	$\overline{\text{RAWDATA}}$	I	**$\overline{\text{Raw Data}}$** Disk drive raw read data from the read channel circuits. Leading edge timing, programmable polarity.
41(39)	$\overline{\text{WPCDATA}}$	O	**$\overline{\text{Write Precomp Data}}$** Precompensated/Conditioned encoded write data sent to the write channel drivers. Leading edge timing, programmable polarity.
42	RVDD	S	**Analog Supply** Dedicated +5v supply to Ramp Locked Loop circuits.
43	RVSS	S	**Analog Ground** Dedicated ground to Ramp Locked Loop circuits.
44(51)	WDATA	I	**Write Data** NRZ write data from the controller. This data is conditioned and precompensated and sent out on $\overline{\text{WPCDATA}}$.
45(40)	WCLK	I	**Write Clock** Running at the NRZ data frequency. WCLK is provided from the the hard disk controller and serves as a reference clock for sampling the incoming WDATA.
46	FSVDD	S	**Analog Supply** Dedicated +5v for the Frequency Synthesizer circuitry.

* XTLO and BCS are inversions of XTLI and MCS respectively and this IOMAP is not bidirectional.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

PIN (IO MAP)	MNEUMONIC	I/O A/S	DESCRIPTION
47	FSVSS	S	**Analog Ground** Dedicated ground for the Frequency Synthesizer circuitry.
49(52)	FSPMP	A	**Frequency Synthesizer Pump** Charge pump for the frequency synthesizer PLL.
50-52 (37,44,49)	$\overline{\text{PORT2-0}}$	O	**Port Two through Zero** Open drain TTL output. These outputs are directly programmable via the microprocessor interface.
53(54†)	XTLI	I	**Crystal Input** Input to active stage of integrated oscillator circuit, this frequency establishes the frequency synthesizer reference. The reference frequency is programmable via the AD bus.
54(53†)	XTLO	O	**Crystal Output** Output from active state of integrated oscillator circuit. This output is left open if an external source is desired.
57(16)	$\overline{\text{HRESET}}$	I	**Hard Reset** When low, this input latches the reset/power-down mode.
58(20)	SGATE	I	**Servo Gate** When high, this input indicates servo operations.

* XTLO and BCS are inversions of XTLI and MCS respectively and this IOMAP is not bidirectional.

TABLE 1-1. SIGNAL DESCRIPTIONS (Continued)

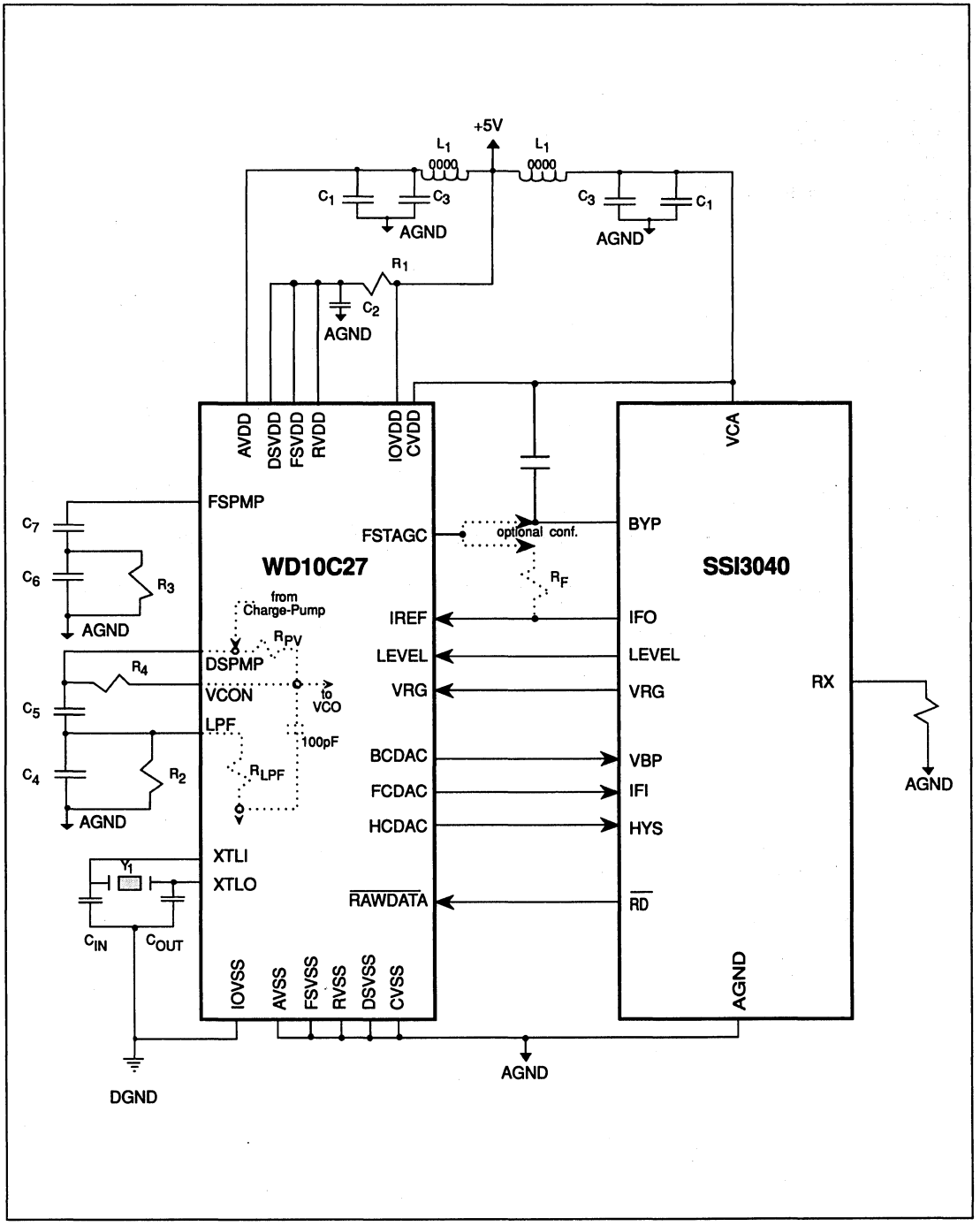


FIGURE 1-2. VARIABLE FREQUENCY CHANNEL SCHEMATIC

WD PART NUMBER	COMPONENT CHARACTERISTICS	REFERENCE DESIGNATOR
39-600000-001	Inductor, 4.7µH, 20% 4532 (3Ω max. DC Resistance)	L_1
19-600000-180	Capacitor, TANT, 22µF, 10V, 20% (C)	C_1
19-600000-171	Capacitor, TANT, 47µF, 10V, 20% (D)	C_2
17-602000-006	Capacitor, CER, 0.1µF, +80%/-20%, 50V, Z5R (1206)	C_3
17-600002-151	Capacitor, CER, 150pF, 5%, 50V, NPO (0805)	C_4
17-601000-046	Capacitor, CER, 4700pF, 5%, 50V, X7R (1206)	C_5
17-601000-098	Capacitor, CER,0.033µF, 5%, 50V, X7R (1206)	C_6
972666-022	Capacitor, CER,0.22µF, 10%, 50V, X7R (1210)	C_7
15-600003-338	Resistor, CM, 5.1Ω, 5%, 1/10 Watt, 200PPM (0805)	R_1
15-601003-346	Resistor, CM, 590Ω, 1%, 1/10 Watt, 200PPM (0805)	R_2
15-601003-347	Resistor, CM, 604Ω, 1%, 1/10 Watt, 200PPM (0805)	R_3
15-601003-414	Resistor, CM, 3.01kΩ, 1%, 1/10 Watt, 200PPM (0805)	R_4
17-600002-220†	Capacitor, CER, 22pF (/47pF/68pF), 5%, NPO, (0805)	C_{OUT}
17-600002-330†	Capacitor, CER, 33pF (/68pF/100pF), 5%, NPO, (0805)	C_{IN}
	Crystal Oscillator (≤40 MHz)‡	Y_1

† Loading capacitor values are dependent on the selection of crystal frequency. These part numbers are given as examples only. See Table 9-11 - Crystal Oscillator Timing Specifications for appropriate load capacitor values. Not required when an external source is supplied.

‡ When an external source is provided, XTLO is left floating.

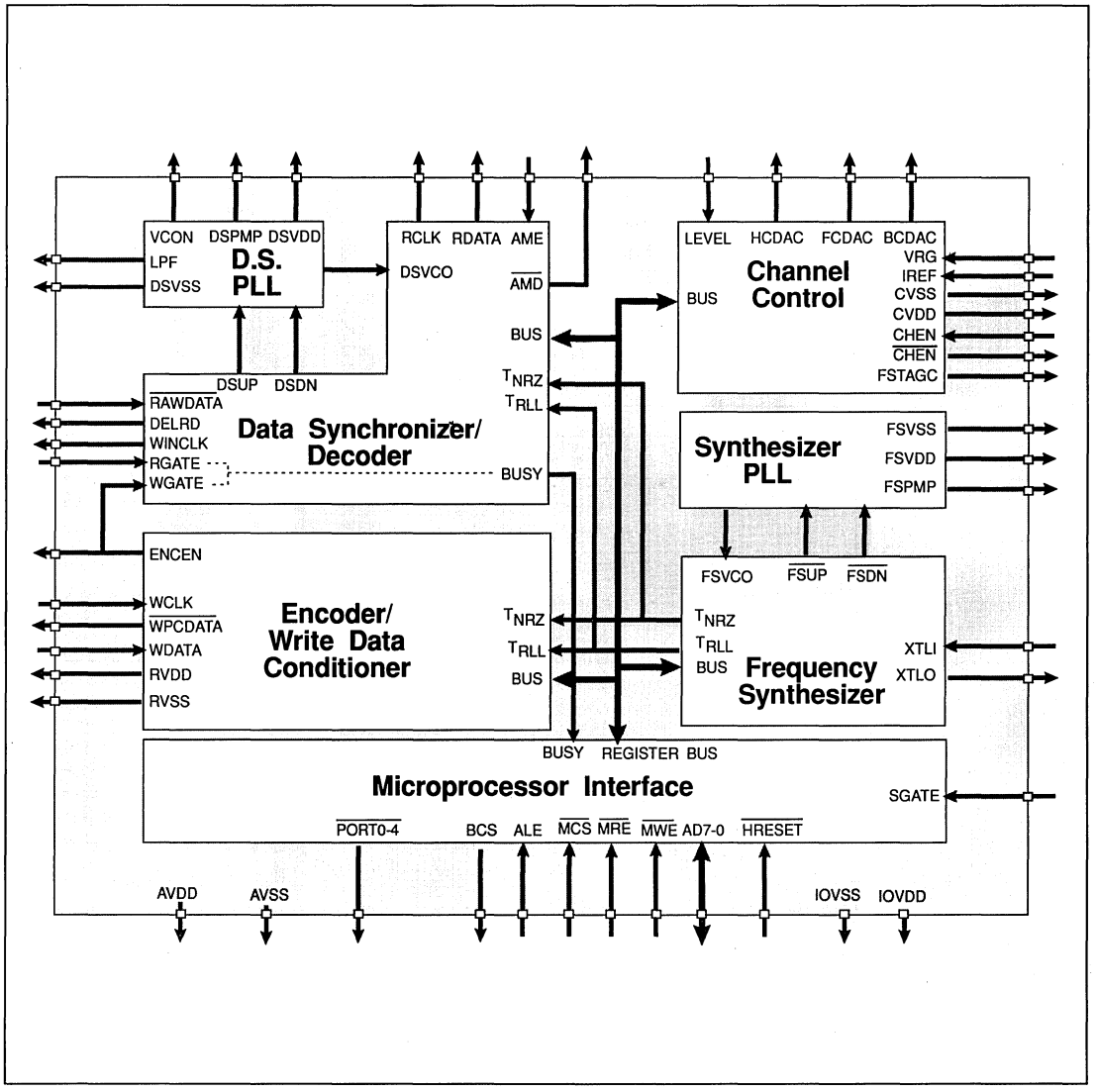


FIGURE 1-3. WD10C27 BLOCK DIAGRAM

2.0 MICROPROCESSOR INTERFACE

The WD10C27 provides an 8- bit interface to the microprocessor for programmability. The interface is compatible with the Intel multiplexed address/data bus architecture. Virtually all of the sub-systems within the WD10C27 are accessible via this interface. The processor interface is decoupled from the input pads during disk reads/writes (i.e., RGATE or ENCEN true) to reduce the possibility of unwanted disturbances to sensitive signal processing. Ensuring that de-coupling is performed is accomplished by deactivating the BZOVR (busy override) bit in the Configuration register. In either configuration, registers should never be modified unless the Hard Disk Controller is not indicating a busy status.

2.1 REGISTER ACCESS

Registers are accessed by placing the correct address word on the AD bus and latching this address on the falling edge of ALE. Subsequent reads/writes will access the addressed registers. Read/writes are performed when MCS is low and the MRE/MWE lines are strobed.

7 ADDRESS 0	SYMBOL	REGISTER ACCESSED
1 1 0 0 0 0 0 0	TEST0	Test Modes Zero
1 1 0 0 0 0 0 1	TEST1	Test Modes One
1 1 0 0 0 0 1 0	TEST2	Test Modes Two
1 1 0 0 0 0 1 1	TSTADD1	Test Address One
1 1 0 0 0 1 0 0	TSTADD2	Test Address Two
1 1 0 0 0 1 0 1	WSCOD	Window Synthesizer Clock Oscillator Divider
1 1 0 0 0 1 1 0	WSVCOD	Window Synthesizer VCO Divider
1 1 0 0 0 1 1 1	SAM	Window Synthesizer Amplifier
1 1 0 0 1 0 0 0	FCDAC	Frequency Control DAC
1 1 0 0 1 0 0 1	BCDAC	Boost Control DAC
1 1 0 0 1 0 1 0	HCDAC	Hysteresis Control DAC
1 1 0 0 1 0 1 1	SFCDAC	Servo Frequency Control DAC
1 1 0 0 1 1 0 0	SBCDAC	Servo Boost Control DAC
1 1 0 0 1 1 0 1	SHCDAC	Servo Hysteresis Control DAC
1 1 0 0 1 1 1 0	FSCOD	Frequency Synthesizer Clock Oscillator Divider
1 1 0 0 1 1 1 1	FSVCOD	Frequency Synthesizer VCO Divider
1 1 0 1 0 0 0 0	WPC10	Write Precompensation One/Zero
1 1 0 1 0 0 0 1	WPC32	Write Precompensation Three/Two
1 1 0 1 0 0 1 0	WPC54	Write Precompensation Five/Four
1 1 0 1 0 0 1 1	WPC76	Write Precompensation Seven/Six
1 1 0 1 0 1 0 0	WPC98	Write Precompensation Nine/Eight
1 1 0 1 0 1 0 1	WPC1110	Write Precompensation Eleven/Ten
1 1 0 1 0 1 1 0	WPC1312	Write Precompensation Thirteen/Twelve
1 1 0 1 0 1 1 1	WPC1514	Write Precompensation Fifteen/Fourteen
1 1 0 1 1 0 0 0	WPC1716	Write Precompensation Seventeen/Sixteen
1 1 0 1 1 0 0 1	WPC1918	Write Precompensation Nineteen/Eighteen

TABLE 2-1. REGISTER ADDRESS MAP

7 ADDRESS 0	SYMBOL	REGISTER ACCESSED
1 1 0 1 1 0 1 0	WFC2021	Write Precompensation Twenty/Twenty-One
1 1 0 1 1 0 1 1	-	Unused
1 1 0 1 1 1 0 0	CFG0	Configuration Zero
1 1 0 1 1 1 0 1	CFG1	Configuration One
1 1 0 1 1 1 1 0	CFG2	Configuration Two
1 1 0 1 1 1 1 1	CFG3	Configuration Three

TABLE 2-1. REGISTER ADDRESS MAP (Continued)

All registers in the WD10C27 are read/write registers, with the exception of the Version ID Register. As previously stated, register access is limited to times when disk read/write operations are inactive. In addition, registers are not readable during low power modes (i.e., RSTPDN and ARSTPDN active.) Register bits correspond to bits 7-0 of the AD bus such that the most significant maps to AD7, the least significant to AD0.

The internal read data bus utilizes a repeater which will latch this bus to the value of the register which was last read and for which the address is not "unused." All registers load asynchronously, thereby requiring no clocks to the device. Exceptions are the Frequency Synthesizer and the Window Shift Synthesizer Registers.

For the Frequency Synthesizer, reads/writes are performed to a master stage. The slave is not updated until synchronization circuitry has deemed it appropriate. This requires XTLI and Frequency Synthesizer VCO clocks.

The WSS will not allow loads to its registers when WSSEN is active.

Following a hard reset on $\overline{\text{HRESET}}$ input, the ARSTPDN bit in the Configuration register will be latched and all other register bits placed in their specified initial state.

Following a soft reset/power down mode, the reset must first be deactivated and then all registers re-configured (excluding CFG3). While re-configuration may be performed immediately following deactivation of the low power modes, reads may not be performed until after the specified setting time, ensuring the output drver's bias generators have become fully operational.

2.2 REGISTER DESCRIPTION

There are six main registers banks in the WD10C27:

- Configuration
- Frequency Synthesizer Dividers
- Window Synthesizer Control
- Skew Symmetric Precompensation
- Channel Control
- Test

2.2.1 Configuration Registers

The configuration (CFG) registers control the basic functions of the sub-circuits. These registers are eight bits wide.

CFG0 Register:

7:RLLEN	6:WPCEN	5:WSSEN	4:PWSEN	3:PWSI	2:PWS0	1:FBS1	0:FBS0

Bit 0: Frequency Band Select Zero.
In conjunction with FBS1, FBS0 controls the Data Synchronizer, Frequency Synthesizer, and Ramp Lock Loop characteristics. See "Table 4-2 - Frequency Band Selection" for band selection.

Bit 1: Frequency Band Select One.
See Bit 0 above.

Bit 2: Percentage Window Shift Zero.
Used in conjunction with PWS1, PWS0 controls the direction of window shift when PWSEN is active.

Bit 3: Percentage Window Shift One.
See Bit 2 above.

Bit 4: Percentage Window Shift Enable.
When active, this bit enables the PWS system.

Bit 5: Window Shift Synthesis Enable.
When active, this bit enables the WSS system. Must be inactive during loads to the WSS registers. (See section 4.2.4, "Window Shifting").

Bit 6: Write Precompensation Enable.
When active, this bit enables the Pattern Dependent Precompensation system (RLLEN must be set to utilize fine resolution capabilities). (See section 5.1, "Pattern Dependent Precompensation").

Bit 7: Ramp Locked Loop Enable.
This bit, when set in conjunction with WPCEN, activates the fine resolution capabilities of the write precompensation sub-circuit. (See section 5.1, "Pattern Dependent Precompensation").

CFG1 Register:

7:TSTEN	6:ENODD	5:AMODD	4:ARSTPDN	3:RSTPDN	2:$\overline{\text{BZOVR}}$	1:IOMAP	0:BYPMODE

Bit 0: Bypass Mode.
When active, this bit enables the bypass mode of the FSTATT pin. when inactive, the FSTATT pin is used to force fast attack in CHEN applications. See section 8.0, "Channel Control DACs".

Bit 1: Input/Output Mapping.
When set, this bit configures the WD10C27 input/output in accordance with the I/O map. IOMAP is logically or'd with HIZEN to ensure all outputs and analog pins are tri-stated during I/O mapping. (See "Table 1-1- Signal Description").

Bit 2: $\overline{\text{Busy Override}}$.
When active, this bit defeats the decoupling of the AD7-0 pads from the Microprocessor Interface during disk read/write operations. Override mode is not recommended. Busy should be defeated during certain test modes. (See section 2.2.6, "Test Registers".)

Bit 3: Reset/Power Down.
When active, this bit will reset/power down all functions and set all register bits to a logic zero for initialization and/or reduced power. All outputs are held inactive, and the crystal oscillator stopped. Exceptions include: FCDAC, HCDAC, and BCDAC registers and related functions, all of which are not effected by this bit; the COD and VCOD registers in both the Frequency and Window Shift Synthesizers, which are set to logic ones; and PORT0-4 bits and $\overline{\text{PORT0-4}}$ pins, which are not effected; and the $\overline{\text{CHEN}}$ and BCS outputs will remain operational. The microprocessor interface is operable during rest/power down, and reset/power down remains active until the RSTPDN bit is written off.

Bit 4: All Reset/Power Down.
This bit, when active, performs the same functions as the RSTPDN bit, with the addition that it will reset/power down the FCDAC, HCDAC and BCDAC registers and circuitry, as well as the RSTPDN bit itself. This bit will be latched upon $\overline{\text{HRESET}}$.

Bit 5: $\overline{\text{AME Odd}}$. This bit controls relationship between the AME input and the NRZ code word boundary. With $\overline{\text{AMODD}}$ active, the data word is assumed to start on an odd bit in the NRZ synchronization byte (i.e. the first non-zero bit is bit 1,3,5,7); when inactive, the data word starts on an even bit (i.e., 0,2,4,6).

Bit 6: $\overline{\text{ENCEN}}$ Odd.
This bit controls relationship between the ENCEN input and the NRZ data word boundary. With $\overline{\text{ENODD}}$ active, the data word is assumed to start on an odd bit in the NRZ synchronization byte (i.e., the first non-zero bit is bit 1,3,5,7); when inactive, the data word starts on an even bit (i.e., 0,2,4,6). This bit reflects the data word boundary for GAP prior to address mark in ID fields, as well as the sync. byte following the synchronization field in DATA fields. This implies that the GAP data and synchronization byte must have the same data word odd/even boundary.

Bit 7: Test Enable.
When active, this bit enables the activation of test modes based on the contents of TEST0-3 registers. When not active, this bit serves to lockout all test modes. (See section 2.2.6, "Test Registers").

CFG2 Register:

7:$\overline{\text{HFCEN}}$	6:VLOCK1	5:VLOCK0	4:WPCPOL	3:RAWPOL	2:WMEN	1:ERRPAT	0:DECERR

Bit 0: Decoder Error.
When set, this bit represents an error detected in the $\overline{\text{RAWDATA}}$ bit stream into the Decoder. This bit should be cleared via a soft reset or an explicit write to this bit. (See section 7.2, "Decoding").

Bit 1: Error Pattern.
When high, forces the Decoder to output NRZ ones when illegal 1,7 codes sequences are encountered on the $\overline{\text{RAWDATA}}$ input. When low, NRZ zeros will be output for illegal sequences.

Bit 2: Window Monitor Enable.
When set, this bit enables the DELRD and WINCLK outputs for window monitoring capabilities. (See section 4.2.3, "Window Monitoring").

Bit 3: Raw Data Polarity.
When set, this bit selects active high leading edge polarity on the $\overline{\text{RAWDATA}}$ input. When not set, active low leading edge polarity is selected.

Bit 4: Write Precomp. Data Polarity.
When set, this bit selects active high leading edge polarity on the $\overline{\text{WPCDATA}}$ output. When not set, active low leading edge polarity is selected.

Bit 5: Velocity Lock Zero.
In conjunction with VCLOCK1, this bit set the velocity lock time for the acquisition sequence. (See section 4.1, "Acquisition Sequencer").

Bit 6: Velocity Lock One.
See Velocity Lock Zero above.

Bit 7: $\overline{\text{High Frequency Clock Enable}}$.
When active, this bit will divide the XTLI frequency by two at the HFCOD prior to the division which occurs at the FSCOD. (See section 3.0, "Frequency Synthesizer").

CFG3 Register:

7:VID2	6:VID1	5:VID0	4:PORT4	3:PORT3	2:PORT2	1:PORT1	0:PORT0

The upper four bits of this register are read only.

Bit 0: Port Zero.
This bit is used to set or reset the $\overline{\text{PORT0}}$ open drain output. Note that setting this bit forces $\overline{\text{PORT0}}$ low. Although these ports are unaffected by the soft reset states invoked via RSTPDN and ARSTPDN, a hard reset issued to the $\overline{\text{HRESET}}$ pin will reset the port pins effectively floating $\overline{\text{PORT0-3}}$.

Bit 1: Port One.
See PORT0 above.

Bit 2: Port One.
See PORT0 above.

Bit 3: Port One.
See PORT0 above.

Bit 4: Port One.
See PORT0 above.

Bit 5: Version Identification Zero.
VID2-0 are used to store a binary number which represents the version number of the device. The version number may be used to verify the correct iteration by the system. This bit is read only.

Bit 6: Version Identification Two.
See VID0 above.

Bit 7: Version Identification Three.
See VID0 above.

2.2.2 Frequency Synthesizer Registers

The Frequency Synthesizer is controlled by the Clock Oscillator Divider (FSCOD) and the VCO Divider (FSVCOD) which are programmed via the contents of the FSCOD and FSVCOD registers. These registers hold eight bit unsigned integers. Programming is performed using the information given in section 3.3, "Programming the FS Dividers". Pre-scaling of the input to the FSCOD is performed based on the state of the $\overline{\text{HFCEN}}$ bit in the Configuration registers.

FSCOD Register:

7:Divide 128	6:Divide 64	5:Divide 32	4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

FSVCOD Register:

7:Divide 128	6:Divide 64	5:Divide 32	4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

2.2.3 Window Synthesizer Registers

The Window Synthesizer Clock Oscillator Divider (WS-COD), VCO Divider (WSVCOD), and Shift Amplifier are controlled by the WSCOD, WSVCOD, and SAM registers respectively. The WSCOD, WSVCOD, and SAM registers hold four and five bit unsigned integers. These registers should be programmed using the information given in section 4.2.4, "Window Shift Synthesis."

WSCOD Register:

3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

WSVCOD Register:

4:Divide 16	3:Divide 8	2:Divide 4	1:Divide 2	0:Divide 1

SAM Register:

3:SAM 8	2:SAM 4	1:SAM 2	0:SAM 1

2.2.4 Skew-Symmetric Precomp. Registers

There are twenty-two 4 bit wide nibbles which control the magnitude of precompensation for the Skew-Symmetric Precompensation system. Each nibble corresponds to a phase shift value in percent of the code bit window, T, for a given three bit sequence. The upper two bits are programmed to generate a coarse setting, while the lower two bits generate a fine setting. Eleven registers are used to hold the complete precompensation matrix, each register holding two consecutive nibbles. *Note that WPC2021 has the nibbles reversed.* See section 5.1, "Pattern Dependent Precompensation."

WPCxxxx Registers:

7:HiCoarse 1	6:HiCoarse 0	5:HiFine 1	4:HiFine 0	3:LoCoarse 1	2:LoCoarse 0	1:LoFine 1	0:LoFine 0

2.2.5 Channel Control Registers

The Channel Control registers consist of registers for controlling the three on board DACs. These registers and their associated functions remain unaffected by the RSTPDN bit. Resetting and power reduction are accomplished by the ARSTPDN bit. SGATE multiplexes the input code to the DACs between the Data bank and the Servo bank.

The DAC registers hold five bit unsigned integers representing the DAC conversion values for each of the three DACs. In addition, each register has a bit which can be used to disable the DAC for reduced power. The HCDAC has one additional bit for function control.

21

FCDAC & BCDAC Registers:

5:DACEN	4:DAC 16	3:DAC 8	2:DAC 4	1:DAC 2	0:DAC 1

HCDAC Registers:

6:$\overline{\text{HCTL}}$	5:DACEN	4:DAC 16	3:DAC 8	2:DAC 4	1:DAC 2	0:DAC 1

SFCDAC, SBCDAC, and SHCDAC Registers:

4:DAC16	3:DAC8	2:DAC4	1:DAC2	0:DAC1

2.2.6 Test Registers

There are three registers which control test functions on the WD10C27 called TEST0-2. TSTEN must be active in the Configuration register before the test modes will be invoked.

Each bit in the TEST registers represents a unique mode which has been created to ensure the quality of the product through design for testability. Some of the test modes provide synchronization of otherwise asynchronous circuits, while others provide visibility of internal logic structures to ensure high fault coverage.

In addition, mutually exclusive test modes (i.e., RLBTST/NLBTST, WSUSDTST/WSLSDTST, DSFUPTST/DSFDNTST, WSFUPTST/WSFDNTST, DSPLKTST/DSVLKTST) are leveraged to enable additional test modes when both are selected.

TEST0 Register:

7:PATREC	6:WPCDC	5:ILBTST	4:CNTRS	3:FSSYNC	2:FSFDN	1:FSFUP	0:PDIO

Bit 0: Frequency and Window Shift Synthesizer Phase Detector I/O Test.
This test takes the Frequency Synthesizer's phase detector pump up and pump down outputs to AD0-1 respectively, the Frequency Synthesizer's phase detector inputs (the FSVCOD and FSCOD outputs) to AD2-3 respectively, the Window Synthesizer's phase detector pump up and pump down outputs to AD4-5 respectively, and the Window Synthesizer's phase detector inputs (the WSVCOD and WSCOD outputs) to AD6-7 respectively during reads of the special address, TSTADD1. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 1: Frequency Synthesizer Frequency Up Test.
This test forces a DC pump up error in the Frequency Synthesizer by gating off the FSCOD input to the phase detector. If both FSFUP and FSFDN are set, neither test is activated. Also see NLBTST and RLBTST modes.

Bit 2: Frequency Synthesizer Frequency Down Test.
This test forces a DC pump down error in the Frequency Synthesizer by gating off the FSVCOD input to the phase detector. If both FSFUP and FSFDN are set, neither test is activated. Also see NLBTST and RLBTST modes.

Bit 3: Frequency Synthesizer Synchronization Test.
This test takes the output of the HFCOD to the input of the FSVCOD as well as to the Frequency Synthesizer output for synchronous open loop testing. The ring oscillator is halted.

Bit 4: Frequency Synthesizer and Window Shift Synthesizer COD/VCOD Counts.
This test takes each of the eight counts out of the Frequency Synthesizer's FSCOD to the AD bus during reads of the FSCOD, each of the eight counts out of the Frequency Synthesizer's FSVCOD to the AD bus during reads of the FSVCOD, each of the four counts of the Window Shift Synthesizer's WSCOD to AD0-3 during reads of the WSCOD, and each of the five counts of the Window Shift Synthesizer's WSVCOD to AD0-4 during reads of the WSVCOD. Note that $\overline{\text{BSOVR}}$ must not be active.

Bit 5: Internal Loopback Test.
This bit, when set, internally activates RGATE and ENCEN, and is intended to be used in conjunction with either RLBTST or NLBTST. When used, for example with NLBTST, 3T $\overline{\text{WPCDATA}}$ will be steered internally to $\overline{\text{RAWDATA}}$ and PLL lockup achieved without a disk drive present.

Bit 6: $\overline{\text{WPCDATA}}$ DC Test.
When active, this bit causes the output on $\overline{\text{WPCDATA}}$ to remain inactive during disk write operations, resulting in DC erasure of the media. This bit will not affect the in-

ternal WPCDATA signal used during loop-back testing.

Bit 7: Pattern Recognizer Test.
When active, this bit allows special control of the precompensation circuits. Used in conjunction with a read from any of the WPC registers, the Pattern Recognizer's register selection will be dynamically directed to the AD4-0, with AD4 reflecting precompensation direction (high is late, low is early). In addition, unprecompensated data out of the Pattern Recognizer is available on AD7, AD6 and AD5 are grounded. Used in conjunction with writes to any of the WPC registers, the value written on AD4-0 will subsequently be used as a constant precompensation value, thus bypassing the Pattern Recognizer. Writes must be at least two T long, and must not be followed by a read unless XTLI is temporarily stopped.

TEST1 Register:

7:NLBTST	6:RLBTST	5:DLLTST	4:WSUSDTST	3:WSLSDTST	2:WSSYNCTST	1:WSFDNTST	0:WSFUPTST

Bit 0: Window Shift Synthesizer Frequency Up Test.
This test forces a DC pump up error in the Window Shift Synthesizer by gating off the WSCOD input to the phase detector. If both WSFUPTST and WSFDNTST are set, neither test is activated and ENCBYP test mode is enabled. During this test mode, WDATA (or RDATA is RLBTST is set) is presented to the precompensation circuits directly, bypassing the FIFO, Encoder and Pattern Recognizer.

Bit 1: Window Shift Synthesizer Frequency Down Test.
This test forces a DC pump down error in the Window Shift Synthesizer by gating off the WSVCOD input to the phase detector. If both WSFUPTST and WSFDNTST are set, neither test is activated and ENCBYP test mode is enabled. See WSFUPTST for details.

Bit 2: Window Shift Synthesizer Synchronization Test.
This test takes the input of the WSCOD to the input of the WSVCOD for synchronous open loop testing.

Bit 3: Window Shift Synthesizer Lower SAM Decode Test.
This test takes the Window Shift Synthesizer's lower eight of sixteen SAM decode values to the AD bus during reads of the SAM register. The decode is active low. Note that BZOVR must not be active. Note that if both Upper and Lower SAM Decode tests are selected, neither will be activated and the CLKRST test mode is invoked. During the CLKRST test mode, the Data Synchronizer and Frequency Synthesizer are reset. This is useful following selection of FSSYNC and/or XVCOTST modes to reset clock paths (i.e., dividers and counters, including the FSCOD and FSVCOD registers) to known states.

Bit 4: Window Shift Synthesizer Upper SAM Decode Test.
This test takes the Window Shift Synthesizer's upper eight of sixteen SAM decode values to AD bus during reads of the SAM register. The decode is active low. Note that BZOVR must not be active. Note that if both Upper and Lower SAM Decode tests are selected, neither will be activated and the CLKRST test mode is invoked. See WSLSDTST for details.

Bit 5: Delay Locked Loop Test.
When set, this bit forces the DLL control voltages to the rails and bypasses the RLL, allowing low frequency functional testing without concern for DLL/RLL frequency limitations. RAWDATA and WPCDATA pulse forming are disabled.

Bit 6: RLL Loop Back Test.
When set, this bit will internally connect

the RDATA/RCLK outputs to the WDATA/WCLK inputs for simultaneous testing of the Data Synchronizer, Decoder, Encoder, and Write Data Conditioner functions by driving RLL $\overline{\text{RAWDATA}}$ and inspecting RLL $\overline{\text{WPCDATA}}$. If both NLBTST and RLBTST are set, neither loopback test is activated and FSFUP/FSFDN and DSFUPTST /DSFDNTST test modes are modified so as to drive the Charge Pump circuits directly, requiring no digital stimulation to test pump currents. See ILBTST in TEST0.

Bit 7: NRZ Loop Back Test.
When set, this bit internally connects the $\overline{\text{WPCDATA}}$ output to the $\overline{\text{RAWDATA}}$ input for simultaneous testing of the Encoder, Write Data Conditioner, Data Synchronizer, and Decoder functions by driving NRZ WDATA/WCLK and inspecting NRZ RDATA/RCLK. If both NLBTST and RLBTST are set, neither loopback test is activated and FSFUP /FSFDN and DSFUPTST /DSFDNTST test modes are modified so as to drive the Charge Pump circuits directly, requiring no digital stimulation to test pump currents. Note that loopback tests force internal polarity consistency between $\overline{\text{WPCDATA}}$ and $\overline{\text{RAWDATA}}$. See ILBTST in TEST0.

TEST2 Register:

7:PDMXTST	6:DSPLKTST	5:DSVLKTST	4:XVCOTST	3:OLPTST	2:DSFDNTST	1:DSFUPTST	0:ACQTST

Bit 0: Acquisition Sequencer Test.
This test takes the Acquisition Sequencer outputs DET6, DET9, HFDET, TIMEOUT, PLOCK, FRAMED, FIFORST, and DECERR to AD0-7 respectively during reads of the special address, TSTADD2. If the PWSD test has also been selected, neither test mode will be activated. Note that $\overline{\text{BZOVR}}$ must not be active.

Bit 1: Data Synchronizer Frequency Down Test. This test force a DC pump up error in the Data Synchronizer by gating off the data input to the phase detector. If both DSFUPTST and DSFDNTST are set, neither are activated. Also see NLBTST and RLBTST modes.

Bit 2: Data Synchronizer Frequency Up Test. This test force a DC pump down error in the Data Synchronizer by gating off the VCO input to the phase detector. If both DSFUPTST and DSFDNTST are set, neither are activated. Also see NLBTST and RLBTST modes.

Bit 3: Open Loop Test.
This test disconnects the Data Synchronizer's charge pump output, DSPMP, from the VCON pin to allow for testing of the charge pump and VCO characteristics. It also disables the voltage clamps on both the Data Synchronizer's and Frequency Synthesizer's VCOs while leaving these ring oscillators fully operational.

Bit 4: External VCO Enable Test.
When active, this bit allows for an external VCO signal to be applied on the LPF pin. The VCO signal should be at TTL levels and at a frequency which equals three times the NRZ data rate. The ring oscillator is halted.

Bit 5: Data Synchronizer Velocity Lock Test. This test will force the Data Synchronizer to remain in Velocity Lock mode by stalling the Acquisition Sequencer prior to entering Phase Lock. If both DSVLKTST and DSPLKTST are set, neither are activated, HIZEN mode is activated. When active, this mode will cause all output drivers and analog pins to be placed in a high impedance state. Exceptions include the microprocessor pins and XTL0. The microprocessor outputs may be tri-stated by asserting either RGATE or ENCEN

with $\overline{BZOVR}$ inactive, and all outputs are placed in a high impedance state.

Bit 6: Data Synchronizer Phase Lock Test. This test forces the Acquisition Sequencer and Data Synchronizer charge pump and filter into phase lock configuration to allow for testing of the PLL tracking characteristics without the need to stimulate the Acquisition Sequencer or Address Mark Detector. VCO clocks are required to synchronize phase lock to the digital circuits. $\overline{BZOVR}$ should be activated prior to setting this bit, as this test mode forces internal RGATE true and places the device in the BUSY state. Without $\overline{BZOVR}$ active, permanent lockout of the Microprocessor interface will result, requiring power down to escape the test mode. See $\overline{BZOVR}$ in the Configuration register for details. If both DSVLKTST and DSPLKTST are set, neither are activated, HIZEN mode is activated. When active, this mode will cause all output drivers and analog pins to be placed in a high impedance state. Exceptions include the microprocessor pins and XTL0. The microprocessor outputs may be tri-stated by asserting either RGATE or ENCEN with $\overline{BZOVR}$ inactive, and all outputs are placed in a high impedance state.

Bit 7: Phase Detection Multiplex Enable Test. When active, this bit directs the phase detector frequency up/down error signals to the DELRD/WINCLK outputs respectively. The WMEN bit must be set in the configuration register. (See section 2.2.1, "Configuration Registers").

3.0 FREQUENCY SYNTHESIZER

The frequency synthesizer output serves as the "crystal" reference for several sub-circuits: the Delay Locked Loop and Ramp Locked Loop circuits for scaling with data rate; the Data Synchronizer for reference when the PLL is not locked to RAWDATA; the Address Mark Detector and Acquisition Sequencer; and the Write Data Conditioner/Encoder for processing of sensitive write signals.

The WD10C27 utilizes a dual divider frequency synthesizer architecture to generate frequencies which never exceeds 140 KHz. Given this, and the flexibility of the programmable crystal input frequency, highly efficient use of zones may be accomplished.

3.1 PROGRAMMABLE FS CRYSTAL REFERENCE (XTLI)

The crystal input is designed to accept input frequencies up to 16 MHz when using the active stage, or up to 40 MHz when an external source is provided. If an external source is used, XTLO is left open. The crystal input frequency should never exceed 20 MHz unless $\overline{\text{HFCEN}}$ is active in the Configuration register. To avoid harmonic lock-up of the various PLLs, the crystal input frequency should never be removed unless a soft reset is issued after the crystal input is re-applied.

3.2 FS DIVIDER OPERATION

The digital portion of the synthesizer consists of a High Frequency Clock Oscillator Divider, a Clock Oscillator Divider to divide the input reference (XTLI), and a VCO Divider to divide the VCO output. The crystal input frequency is divided down based on the contents of the $\overline{\text{HFCEN}}$ bit in the Configuration registers, and the contents of the FSCOD register. The VCO output frequency from the PLL is similarly divided, based on the contents of the FSVCOD register, to match the frequency output of the FSCOD output.

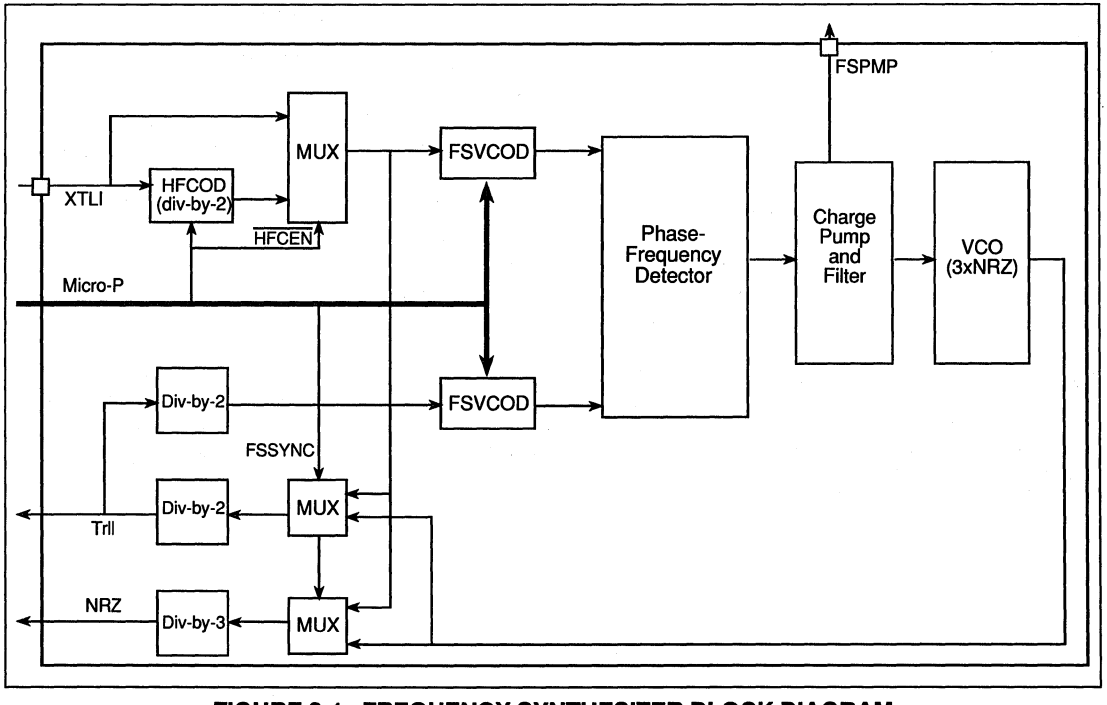


FIGURE 3-1. FREQUENCY SYNTHESIZER BLOCK DIAGRAM

The PLL architecture is almost identical to that of the Data Synchronizer. Phase-frequency locked loop synchronization is performed on the output of the FSCOD. The Charge Pump drives a VCO which utilizes a ring oscillator architecture at three times the NRZ data rate. The output of the charge pump is filtered at a very low bandwidth for high jitter rejection, while the VCO gain is modified based on the current zonal frequency to establish loop gain constancy. At the output of the Frequency Synthesizer, the VCO is operating at three times the NRZ data frequency. The NRZ and channel rate frequencies are ultimately steered to the other sub-circuits as their "crystal references". The coded rate, channel rate, or window clock, is herein referred to as T_{RLL}. The period, T, of the window clock defines the width of the phase and data detection windows. The frequency of T_{RLL} defined with respect to the NRZ data rate (f_{NRZ}), is therefore given by

EQ. 1.0

$$f_{RLL} = \frac{3 \times f_{NRZ}}{2}$$

where

EQ. 2.0

$$T_{RLL} = \frac{1}{f_{RLL}}$$

and

EQ. 3.0

$$7.5 \text{ MHz} \leq f_{NRZ} \leq 33 \text{ MHz}$$

Finally, the 3X NRZ VCO output is divided by four and used as the input to the FSVCOD.

3.3 PROGRAMMING THE FS DIVIDERS

Frequency Synthesis is accomplished by programming the FSCOD and FSVCOD registers such that the equality

EQ 4.0

$$\frac{3/4 \times f_{NRZ}}{FSVCOD + 1} = \frac{f_{HFCOD}}{FSCOD + 1} = f_{FSPLL}$$

is satisfied, where f_{HFCOD} is the pre-scaled crystal input frequency, and f_{FSPLL} is the Frequency Synthesizer PLL operating frequency range and is given by

EQ. 5.0

$$95 \text{ KHz} \leq f_{FSPLL} \leq 105 \text{ KHz}$$

Rearranging EQ. 4.0,

EQ. 6.0

$$f_{NRZ} = \frac{(4)}{(3)} \times \frac{(FSVCOD + 1)}{(FSCOD + 1)} \times f_{HFCOD}$$

it can easily be seen that the NRZ frequency is simply a ratio of the crystal reference frequency which may be pre-scaled in the HFCOD.

Because each side of EQ. 4.0 must not only satisfy the equality, but satisfy EQ. 5.0, selection of VCOD value can now be determined based on the NRZ data rate and the preferred crystal frequency. Note that to program a value of N, the registers must be loaded with a value of N-1.

The FSCOD and FSVCOD registers are eight bits, allowing for division up to 256 in both dividers. In addition, if the $\overline{\text{HFCEN}}$ (high frequency clock enable) bit in the Configuration registers is active, the XTLI frequency is divided by two in the HFCOD prior to entering the FSCOD. This results in the FSCOD values effectively being doubled, allowing for division of the input from 2 up to 512 in multiples of 2. $\overline{\text{HFCEN}}$ will be active on power up.

Minimum and maximum divider values are determined from EQ. 3.0 through EQ. 5.0 as follows. For the legal range of FSVCOD values, given the NRZ frequency range and the FS PLL range, we have

EQ. 7.0

$$\frac{3/4 \times f_{NRZ}\ (min)}{f_{FSPLL}\ (max)} \leq FSVCOD + 1 \leq \frac{3/4 \times f_{NRZ}\ (max)}{f_{FSPLL}\ (min)}$$

EQ. 7.1

$$\frac{5.625\ MHz}{105\ KHz} \leq FSVCOD + 1 \leq \frac{24.75\ MHz}{95\ KHz}$$

EQ. 7.2

$$53 \leq FSVCOD \leq 255$$

For the FSCOD values, the legal maximum is constrained by the maximum frequency of the crystal reference. This reference may never exceed 40 MHz. Since the $\overline{HFCEN}$ bit must be set for crystal reference frequencies greater than 20 MHz, the output of the HFCOD will never exceed 20 MHz.

Therefore, we have

EQ. 8.0

$$\frac{f_{HFCOD}\ (min)}{f_{FSPLL}\ (max)} \leq FSCOD + 1 \leq \frac{f_{HFCOD}\ (max)}{f_{FSPLL}\ (min)}$$

EQ. 8.1

$$\frac{0\ MHz}{105\ KHz} \leq FSCOD + 1 \leq \frac{20\ MHz}{95\ KHz}$$

EQ. 9.0

$$0 \leq FSCOD \leq 209$$

See section A.1, "Frequency Synthesizer" for software automation of these calculations.

4.0 READ CHANNEL

4.1 ACQUISITION SEQUENCER

The WD10C27 supports both hard and soft sector formats. The acquisition sequence is initiated when either RGATE or $\overline{AMD}$ are asserted. Other than the Address Mark search and timing of data acquisition off of $\overline{AMD}$, there are no further distinctions between hard and soft sector operations.

4.1.1 Soft Sector Sequencing

In soft sector formats, the Acquisition Sequence is initiated upon receipt of $\overline{AMD}$. When AME is asserted, and neither SGATE or ENCEN are active, pulse formed raw read data is synchronized to T_{RLL} and sent to the Address Mark Detection circuitry. The previously written address mark (AM) is matched, $\overline{AMD}$ is asserted and the AM search is complete.

Redundancy in the address mark creates an inherent uncertainty in the timing of $\overline{AMD}$ with respect to the synchronization field. It is therefore necessary to delay the start of the acquisition sequence to avoid acquisition to the end of the address mark. Unlike other designs which simply count three raw read data transitions from the assertion of RGATE, the WD10C27's Address Mark Detector actually uses pulse period discrimination to further qualify address mark detection. Thus, $\overline{AMD}$ is asserted only after three high frequency periods have been sensed on the raw read data following the occurrence of an address mark. This additional qualification serves to reduce the chances of false detection due to servo fields, write splices, unformated surface, defects, etc. Additionally, the acquisition sequence begins immediately upon assertion of $\overline{AMD}$, saving several bits of synchronization field lost in other schemes due to the $\overline{AMD}$-to-RGATE round trip delay.

Upon receipt of AMD, the hard disk controller should respond by asserting RGATE and de-asserting AME. The acquisition sequence is initiated upon receipt of AMD. At the end of the velocity lock time, if the hard disk controller has not yet responded with RGATE, the acquisition sequence is terminated.

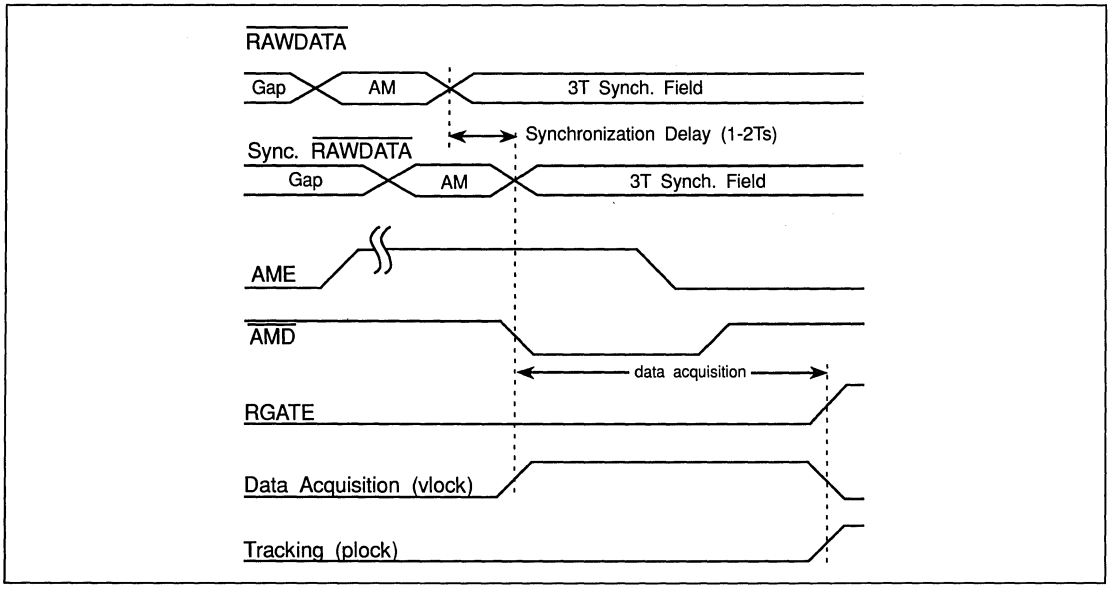


FIGURE 4-1. SOFT SECTOR TIMING

4.1.2 Data Acquisition and Tracking

For both hard and soft sector formats, upon receipt of either RGATE or $\overline{AMD}$ respectively, phase-frequency detection (velocity lock) is used to quickly and reliably acquire lock to the incoming raw read data. Use of this technique eliminates susceptibility to harmonics and asymmetry. The velocity lock time is programmable from 5 to 8 NRZ byte times via the VLOCK0/1 bits in the Configuration register, although eight byte times is recommended.

VLOCK1	VLOCK0	Vlock Time Tvlk
0	0	60 T (5 NRZ Bytes)
0	1	72 T (6 NRZ Bytes)
1	0	84 T (7 NRZ Bytes)
1	1	96 T (8 NRZ Bytes)

TABLE 4-1. VELOCITY LOCK TIME SELECTION

At the end of the programmed velocity lock time, the Acquisition Sequencer switches the PLL to phase-only detection (phase lock). Phase lock is used to complete phase acquisition before the end of the synchronization field and enable tracking of the average channel rate as seen on the random raw read data. The phase jump at the acquisition-to-tracking switch-over due to multiplexing seen in other circuits is avoided through the use of a patented frequency switch-over circuit which guarantees zero-phase jump. However, due to the possibility of defects in the synchronization field, a minimum of four NRZ byte times (16 "001"s) are recommended to eliminate any residual phase/frequency errors.

At the switch-over from velocity lock to phase lock, several critical events occur:

- as mentioned, phase-only detection begins in the PLL
- the charge pumps/filter are switched for low gain and reduced bandwidth following synchronization to two pump pulses
- the RCLK source is redirected from the Frequency Synthesizer's reference to the Data Synchronizer's VCO, divided to the NRZ data frequency
- the Decoder begins a pattern match for 3 consecutive "001"s - when complete, framing is assured and decoded raw read data is presented on the RDATA output

When reading is complete, RGATE is de-asserted and the RCLK source will return to the Frequency Synthesizer reference, the PLL returns to high gain acquisition of the reference frequency, and the Acquisition Sequencer is re-armed to repeat sequencing when appropriate.

4.1.3 RCLK Source

In the WD10C27 architecture, it is assumed that the hard disk controller will be using RCLK during write commands as its NRZ reference clock, WCLK. To accommodate the fast ID read-to-data write times (i.e., RGATE de-assertion to WGATE assertion), RCLK must switch back to the crystal reference without the transients that are associated with acquisition back to the Data Synchronizer's reference. Therefore, at both the onset and termination of phase lock, the Frequency Synthesizer or Data Synchronizer's VCO, divided down to the NRZ data rate, is steered to the RCLK output accordingly. During this transition, RCLK will be stopped for up to two NRZ clock cycles to perform synchronization and provide a glitch-free RCLK transition.

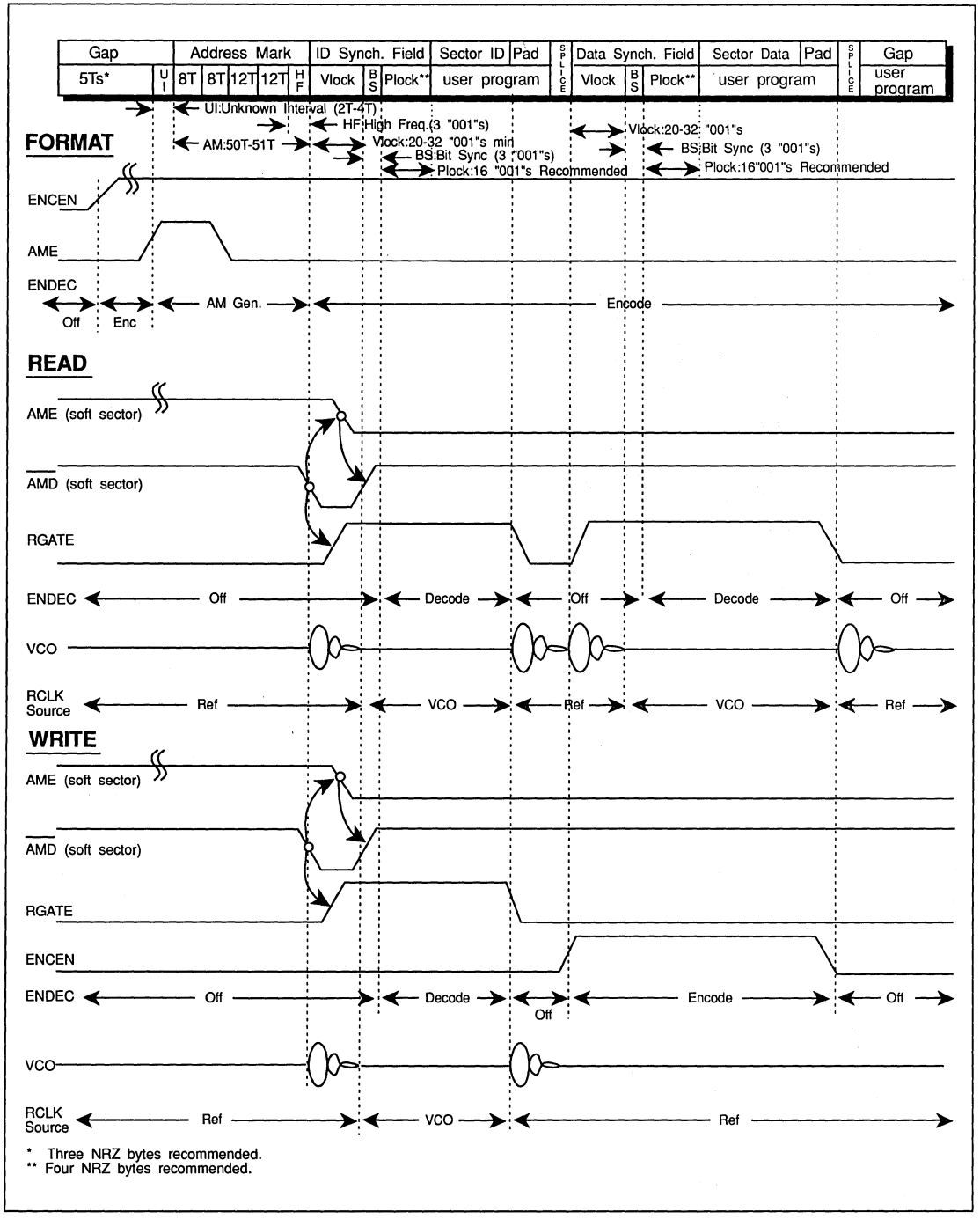


FIGURE 4-2. THE ACQUISITION SEQUENCE

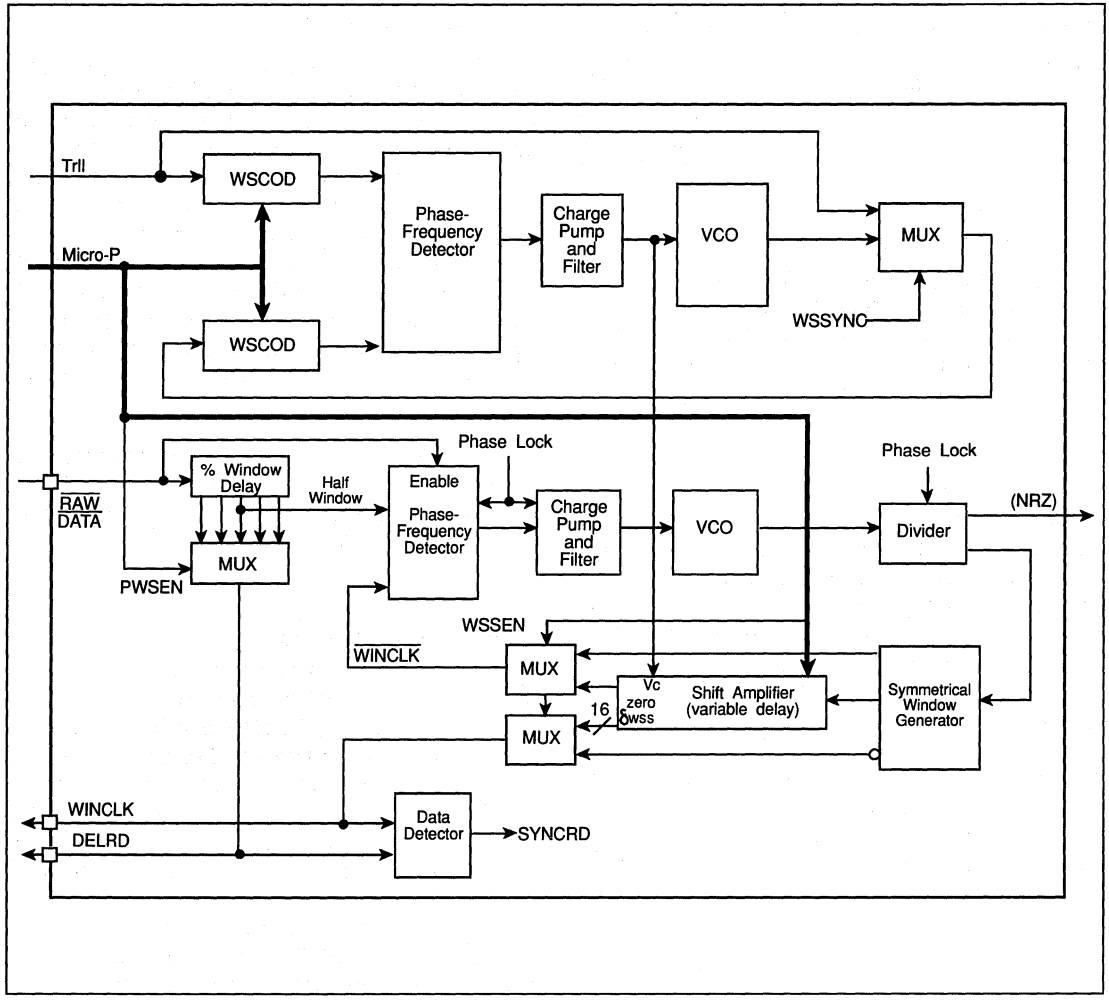


FIGURE 4-3. DATA SYNCHRONIZER BLOCK DIAGRAM

4.2 DATA SYNCHRONIZER

4.2.1 Phase-Locked Loop

The PLL is uniquely designed to eliminate the typically non-linear loop characteristics inherent in other architectures. Using a proprietary technique, the charge pump and VCO gains are inter-dependent. As VCO gain changes, the charge pumps are compensated, thus maintaining charge pump symmetry and loop gain linearity.

In most PLL designs, increased or decreased sample rates into the PLL for zoned media results in an undesirable change in loop gain. Some designs compensate by allowing for gain changes based on zonal information. This can result in phase margin loss and necessitates a compromised loop design. In contrast, the WD10C27 makes use of the zonal information not only to modify gain, but to optimize the filter characteristics. This is accomplished with no external component changes.

The VCO ring oscillator architecture is fully integrated, allowing for precise compensation of temperature, voltage, processing, and aging effects. The VCO operates at three times the NRZ data rate (two times the channel rate) and is divided down to the NRZ data rate at the RCLK output.

The WD10C27 optimizes loop gain and bandwidth using frequency information obtained via the processor interface. PLL characteristics are modified at pre-determined frequency bands, selectable via the frequency band selection bits FBS0 and FBS1 in the CFG register.

4.2.2 Window Generation

The Data Synchronizer utilizes Western Digitals proven DLL technology to generate precision phase detection window centering. The data detection window generation is accomplished via a proprietary symmetrical window generation scheme employing the 3xNRZ VCO and symmetrical CMOS circuit/layout structures. Window centering automatically tracks frequency changes, either due to components such as motor speed variations, or as a result of zonal frequency changes. This system suffers no digital losses due to setup/hold times, rise/fall variations, current imbalance, inaccurate 180 degree phase shifts, parasitics, etc.

4.2.3 Window Monitoring

Window monitoring may be performed through inspection of the DELRD and WINCLK outputs. Window centering is achieved when DELRD rising edges are centered within the rising edges of WINCLK. With the PDMXTST (phase detector multiplex test) bit active in the test registers, these outputs will reflect the digital phase error signals out of the phase detector. DELRD will represent frequency up errors, while WINCLK will represent frequency down errors. Used differentially, these signals may be used to reconstruct the error amplifier envelope during acquisition and/or tracking.

Window monitoring is enabled by activating the WMEN bit in the configuration registers. When WMEN is not set, the DELRD and WINCLK outputs will be held low.

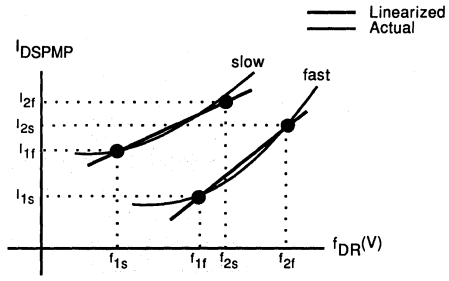
4.2.4 Window Shifting

Window shifting takes place at the Data Detector by two methods which result in a shift in the relationship between DELRD and WINCLK. The first method, Percentage Window Shift, uses the half-window delay line to advance or delay DELRD by an amount determined via the microprocessor, and which automatically scales with changes in the data rate. The second method, Window Shift Synthesis, synthesizes a delay value selected via the microprocessor and advances or delays WINCLK by the programmed amount. Both methods may be used simultaneously.

Band	FBS1	FBS0	NRZ Data Rate (MBps)	Phase Detector Gain † K_D	VCO Gain K_O	Open Loop Gain K_V	Filter Resistors			
							R_{PV} ‡		R_{LPF}	
							Int.	Ext.	Int.	Ext.
0	0	0	$7.5 \le f_{dr} \le 9.6$	K_{D0}	K_{O0}	K_{V0}	∞	3.01kΩ	∞	0Ω
1	0	1	$9.6 < f_{dr} \le 13.5$	K_{D1}	K_{O1}	K_{V1}			2.2kΩ	
2	1	0	$13.5 < f_{dr} \le 19.1$	K_{D2}	K_{O2}	K_{V2}	3kΩ		1.4Ω	
3	1	1	$19.1 < f_{dr} \le 33.0$	K_{D3}	K_{O3}	K_{V3}	1.5kΩ			

† Halved during data acquisition ‡ Shorted during data acquisition

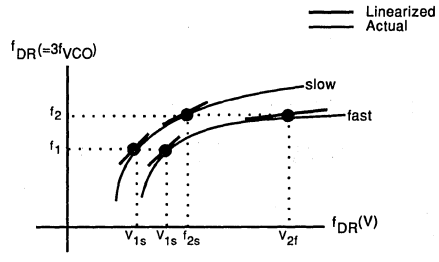
TABLE 4-2. FREQUENCY BAND SELECTION



$$K_{Dx} = \left(\frac{1}{2\pi}\right)\left(\left(\frac{I_{2x}-I_{1x}}{f_2-f_1}\right)(f_{DR}-f_1) + I_{1x}\right)\left(\frac{\mu A}{rad}\right)$$

KD_x is the linearized Phase Detector gain. I_1 and I_2 are the charge pump currents obtained at the frequency limits of the frequency bands, f_1 and f_2.

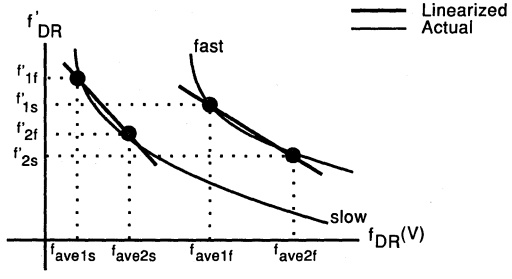
FIGURE 4-4. CHARGE PUMP GAIN CHARACTERISTIC



$$f'_{DR} = 100x\left(\frac{f(V) - f(V+\Delta V)}{f_{ave\Delta V}}\right)\left(\frac{percent}{volt}\right)$$

f'_{DR} is the VCO gain in %Δf/V at data rates f_1 and f_2, where f_1 and f_2 are the limits of the ZBR bands. ΔV is a 5-mV Change in VCON in a direction away from the band edge. f_{ave} is the average of f(V) and f(V+ΔV).

FIGURE 4-5. VCO IV CHARACTERISTIC



$$K_{Ox} = \left(\frac{f'_{2x}-f'_{1x}}{f_{ave2x}-f_{ave1x}}\right)(f_{DR}-f_{ave1x}) + f_{1x}\left(\frac{percent}{volt}\right)$$

K_{Ox} is the linearized VCO gain in %Δf/Vas a function of data rate. The gain is linearized between f'_{1x} and f'_{2x}, where f'_{1x} and f'_{2x} are defined in "Fig. 4-5, VCO IV Characteristic", and subscript "x" reflects the variation in gain associated with the fast and slow operating corners.

FIGURE 4-6. VCO GAIN CHARACTERISTIC

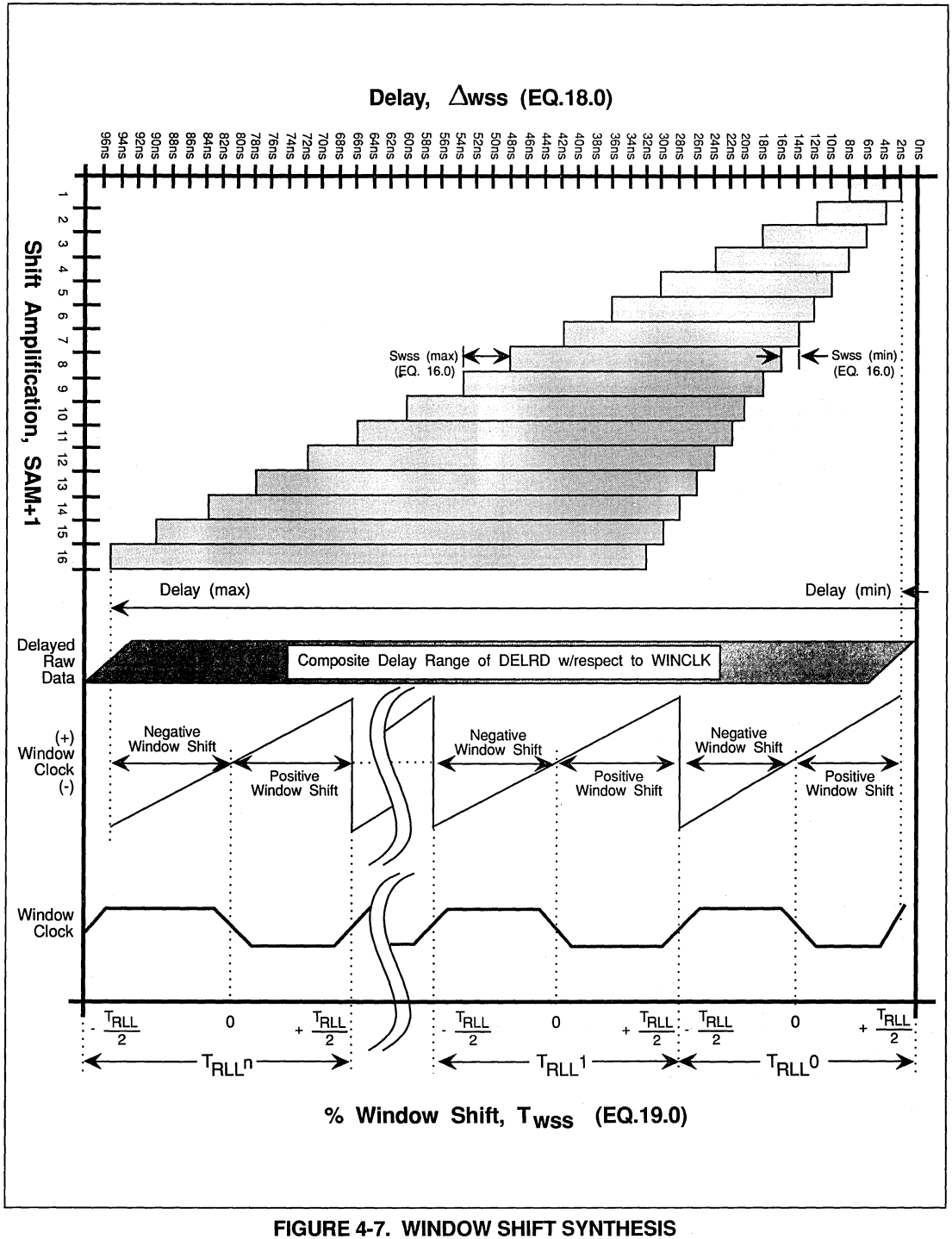


FIGURE 4-7. WINDOW SHIFT SYNTHESIS

Percentage Window Shifting

The Percentage Window Shift (PWS) approach allows for window shifting as a percentage of the window, T. This system is convenient as it is simple to use and scales with data frequencies. Window shifting can be programmed to 6.25% or 12.5% of T using this system.

PWS is enabled by activating the PWSEN bit in the CFG register, while direction and magnitude are selected by programming the PWS0 and PWS1 bits in the CFG register.

PWS1	PWS0	WINDOW SHIFT (%T_{RLL})
0	0	6.25% Early
0	1	6.25% Late
1	0	12.50% Early
1	1	12.50% Late

TABLE 4-3. PERCENTAGE WINDOW SHIFT SELECTION

Window Shift Synthesizer

The Window Shift Synthesis (WSS) system (patent pending) employed on the WD10C27 uses information programmed through the microprocessor interface to synthesize virtually any value of window shift which may be desired. Synthesis is achieved in a manner similar to the Frequency Synthesizer.

WSS is a 4-bit time DAC with a programmable synthesized LSB. Using T_{RLL} as its reference, the system synthesizes the user selected LSB value in a servo controlled delay element. Delay elements may be programmed essentially continuously across the range of 2ns to 6ns. Sixteen of these delay stages are chained back-to-back to create a tapped delay line which serves to create a user programmable amplification of the shift value developed in the servo delay element. Thus, a resultant delay of 2ns to 96ns is generated in the position of delayed raw data (DELRD) with respect to the leading edge of the detection window (WINCLK).

WSS is enabled by activating the WSSEN bit in the CFG register.

WSS Divider/Shift Amp. Operation

The digital portion of the synthesizer consists of a Clock Oscillator Divider to divide the input reference (T_{RLL}), and a VCO Divider to divide the VCO output. The T_{RLL} input frequency is divided down based on the contents of the WSCOD register. The VCO output frequency from the PLL is similarly divided, based on the contents of the WSVCOD register, to match the frequency output of the WSCOD.

Care should be taken never to modify the registers while WSSEN is active. Correct load sequencing is as follows: de-assert WSSEN; load the WSCOD and WSVCOD values; and assert WSSEN.

The VCO design utilizes 4.5 double inverting stages in a ring oscillator architecture. When phase-frequency lock is achieved on the output of the WSCOD, the delay through each VCO stage will be precisely controlled. These stages are duplicated in the Shift Amplifier to generate a precision delay line. The delay may be amplified by selecting anywhere from one to sixteen delay stages. Selection of the amplification is accomplished via the contents of the SAM register.

Programming the WSS Dividers/Amp.

Window synthesis calculations are similar to those in section 3.0, "Frequency Synthesizer". Programming the Window Shift Synthesizer is accomplished by programming the WSCOD and WSVCOD registers such that the equality

EQ. 10.0

$$\frac{f_{WSVCO}}{WSVCOD + 1} = \frac{f_{RLL}}{WSCOD + 1} = Fwspll$$

is satisfied. F_{RLL} is given by EQ. 1.0, and Fwspll is the Window Synthesizer PLL operating frequency range, limited such that

EQ. 11.0

$$3\ MHz \leq f_{WSPLL} \leq 15\ MHz$$

Fwsvco is the Window Synthesizer VCO frequency and is limited such that

EQ. 12.0

$$18.52\ MHz \leq f_{WSVCO} \leq 55.56\ MHz$$

Note that to program the register to a value of N, a value of N-1 must be loaded.

The WSCOD and WSVCOD registers are 4 and 5 bits respectively. Minimum and maximum divider values are determined from EQ. 4.0 through EQ. 12.0 as follows.

For the legal range of WSVCOD values, given the WSS VCO range and the WSS PLL range, we have

EQ 13.0

$$\frac{f_{WSVCO}\ (min)}{f_{WSPLL}\ (max)} \leq WSVCOD + 1 \leq \frac{f_{WSVCO}\ (max)}{f_{WSPLL}\ (min)}$$

EQ. 13.1

$$\frac{18.52\ MHz}{15\ MHz} \leq WSVCOD + 1 \leq \frac{55.56\ MHz}{3\ MHz}$$

EQ. 13.2

$$1 \leq WSVCOD \leq 17$$

For the WSCOD values, we have

EQ. 14.0

$$\frac{f_{RLL}\ (min)}{f_{WSPLL}\ (max)} \leq WSCOD + 1 \leq \frac{f_{RLL}\ (max)}{f_{WSPLL}\ (min)}$$

EQ. 14.1

$$\frac{11.25\ MHz}{15\ MHz} \leq WSCOD + 1 \leq \frac{40.5\ MHz}{3\ MHz}$$

EQ. 14.2

$$0 \leq WSCOD \leq 12$$

The Window Shift value, Twss, may now be determined as follows. As stated previously, the VCO has 4.5 double inverting stages. The frequency of the WSS VCO can therefore be given in terms of the delay of each stage, δwss, by

EQ. 15.0

$$f_{WSVCO} = \frac{1000}{9 \times \delta wss}$$

Combining EQ. 2.0, EQ. 4.0, and EQ. 15.0, we derive the relationship for the synthesized theoretical LSB, LSB_T

EQ. 16.0

$$\delta wss = LSB_T = \left(\frac{T_{RLL}}{9}\right) = \left(\frac{WSCOD + 1}{WSVCOD + 1}\right)$$

where, substituting EQ.12.0 into EQ. 16.0, we have

EQ. 16.1

$$2ns \leq LSB_T \leq 6ns$$

Since the SAM selects from one to sixteen LSB_Ts, the legal SAM values are bounded by

EQ. 17.0

$$1 \leq SAM + 1 \leq 16$$

EQ. 17.1

$$0 \leq SAM \leq 15$$

Therefore, Δwss, the total delay, from the rising edge of DELRD to the late edge of the detection window (as defined by WINCLK), may be generated by amplifying δwss by the SAM value, and is given by

EQ. 18.0

$$\Delta wss = \left(\frac{T_{RLL}}{9}\right)\left(\frac{WSCOD + 1}{WSVCOD + 1}\right)(SAM + 1)$$

Finally, the normalized window shift T*wss*, in percent T_{RLL} is given by

EQ. 19.0

$$T_{WSS} = 100 \times \left(\frac{1}{2} - MOD\left[\frac{\Delta wss}{T_{RLL}}\right]\right)$$

Where the "MOD" function in EQ 19.0 returns the fractional part of the operand.

5.0 WRITE CHANNEL

The Write Data Conditioner processes the NRZ write data (WDATA) from the hard disk controller. Encoded data is resynchronized from the encoder off of the crystal reference from the Frequency Synthesizer (T_{RLL}) to remove any sources of timing jitter. The re-conditioned write data is sent out to the write channel electronics on the $\overline{\text{WPCDATA}}$ pin, where high-to-low transitions represent the accurate crystal controlled timing edges. When $\overline{\text{WGATE}}$ is inactive, the Write Data Conditioner sleeps to conserve power. $\overline{\text{WPCDATA}}$ is held high during this time.

5.1 PATTERN DEPENDENT PRECOMPENSATION

Write precompensation is accomplished by implementation of a pattern dependent skew-symmetric precompensation matrix. A skew-symmetric matrix is defined as having zeroes along the diagonal while being symmetrical about the diagonal (except for signs). Thus, for the 7-by-7 matrix of all possible consecutive pulse period pairs (three bit combinations) in a 1,7 RLL code, if we assume no precompensation for symmetrically spaced bits (the diagonal), and precompensation of the same magnitude for non-symmetrical pulse period pairs and their mirror images.

One exception to the skew-symmetric rule is the inclusion of the 2T/2T pulse period pair. This pair has a matrix entry to account for write induced peak shift on 2T runs. Also note that although entries exist for 7T8T and 8T7T pulse period pairs, these are pairs which cannot be realized by virtue of the encode rules (8T8T is another such pair, although it has no entry due to its position along the diagonal). These entries may however be utilized at the gap-to-Address Mark transition.

The Pattern Recognizer has been designed to recognize two special cases of run length violations which can occur in soft sector applications during formats: pulse periods greater than 8T (i.e. 12T) generated in the Address Mark; pulse periods less than 2T or greater than 8T (i.e. 1T or 9T) generated at the gap-to-Address Mark transition. To handle the "greater than 8T" run length violations, the Pattern Recognizer will always force a pulse period of greater than 8T to be precompensated as an 8T. This does not effect what actually gets sent out on $\overline{\text{WPCDATA}}$. Therefore, the 8T/12T, 12T/12T, and 12T/3T intervals in the Address Mark will be precompensated as 8T/8T, 8T/8T, and 8T/3T respectively. For the case "less than 2T" run length violations, consecutive "1"s will be modified such that the second "1" in the sequence is converted to a "0" prior to entering the Pattern Recognition circuitry. Therefore, if a "11" is generated at the gap-to-Address Mark transition, the Pattern Recognizer, as well as $\overline{\text{WPCDATA}}$, will actually be a "10".

COARSE 1	COARSE 0	FINE 1	FINE 0	PHASE SHIFT
0	0	0	0	0.0000%
0	0	0	1	1.5625%
0	0	1	0	3.1250%
0	0	1	1	4.6875%
0	1	0	0	6.2500%
0	1	0	1	7.8125%
0	1	1	0	9.3750%
0	1	1	1	10.9375%
1	0	0	0	12.5000%
1	0	0	1	14.0625%
1	0	1	0	15.6250%
1	0	1	1	17.1875%
1	1	0	0	18.750%
1	1	0	1	20.3125%
1	1	1	0	21.8750%
1	1	1	1	23.4375%

TABLE 5-1. PRECOMPENSATION SELECTION

Write precompensation is enabled through the microprocessor interface by activating the WPCEN bit in the CFG register. Precompensation takes place by means of a pattern detector which determines the distance of the previous and next bits to the current bit.

The pulse period pair which has been detected addresses the WPC registers, keeping track of the order of the pulse periods, or sign. This information is passed to the Write Precompensation circuits for appropriate phase shifting of the WPCDATA output.

The WPC registers have two bits for coarse precompensation selection and two bits for fine resolution, both based on a percentage of the code bit window, T. The value of the coarse setting will be summed with the value of the fine setting to produce a resultant precompensation value, as depicted in "Table 5-1, Precompensation Selection".

RLLEN must be set in the configuration registers to utilize the fine resolution capabilities. If RLLEN is disabled, the Ramp Locked Loop (RLL), which performs fine resolution precompensation, will be powered down and the fine resolution settings in the WPC registers disregarded. Because the RLL needs time to acquire and lock to its internal reference, this bit should be enabled well in advance of a write operation, as indicated by the timing specifications of the RLL.

21

Next Pulse Period (Trailing)	Previous Pulse Period (Leading) 2T	3T	4T	5T	6T	7T	8T
8T	+WPC16	+WPC17	+WPC18	+WPC19	+WPC20	+WPC21	
7T	+WPC12	+WPC13	+WPC14	+WPC15	+WPC7		-WPC21
6T	+WPC8	+WPC9	+WPC10	+WPC11		-WPC7	-WPC20
5T	+WPC4	+WPC5	+WPC6		-WPC11	-WPC15	-WPC19
4T	+WPC2	+WPC3		-WPC6	-WPC10	-WPC14	-WPC18
3T	+WPC0		-WPC3	-WPC5	-WPC9	-WPC13	-WPC17
2T	+WPC1	-WPC0	-WPC2	-WPC4	-WPC8	-WPC12	-WPC16

TABLE 5-2. SKEW SYMMETRIC MATRIX MAP

6.0 ADDRESS MARK GENERATION/DETECTION

For soft sector formats, the WD10C27 supports address mark generation and detection. The following describes the AM detection rules and considerations of format during AM generation to reduce false AM detection.

6.1 ADDRESS MARK DETECTION RULES

Address mark detection is assumed to be successful only when specific pattern sequences have been detected on the synchronized raw read data. The patterns must be found in sequence according to the following rules, and only following assertion of AME. (See Table 6-1, "Address Mark Detect Sequences"):

1. Detect a "1" followed by at least six consecutive "0"s (i.e., 1...00000...)
2. Detect a "1" followed by at least nine consecutive "0"s (i.e., 1...000000000...) no more than 3 NRZ byte times following detection of sequence 1.
3. Detect a "1" followed by at least three consecutive high frequency (HF) intervals (i.e., ...1001001001) no more than 3NRZ byte times following detection of sequence 2.

Address marks are formatted with several unique qualities which are important in ensuring high probability of correct detection. The AM used by the WD10C27 is formatted as 8T8T12T12T3T3T3T. The leading "1" in the AM is always formatted preceding the first 8T interval in order to guarantee the interval width.

6.2 ADDRESS MARK GENERATION

When AME is asserted during disk write operations, the AM is "jammed" into the serial encoded bit stream. This is necessary to ensure that the AM placement is exact and does not depend upon synchronization to a previous interval. Jamming of the AM therefore will create an arbitrary run length between the user programmed gap and the AM. This may result in a violation of the *d* constraints of the 1,7 code, such that a 1T interval is created.

In the event that a 1T interval is created at the leading edge of the AM, the second of the two "1"s will be suppressed, and the AM sent to the write electronics will be

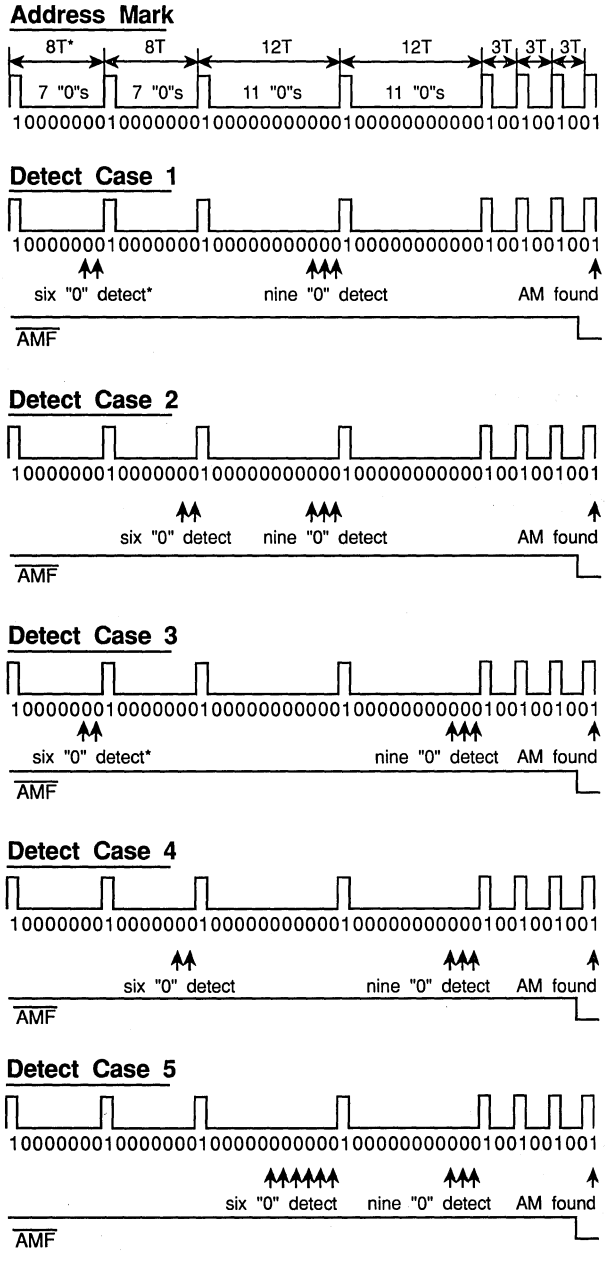
9T8T12T12T3T3T3T.

HF intervals will be formatted as three 3T (001) intervals during AM generation. The threshold of the HF detection circuitry will actually allow any interval in the range of 2T to 4T to account for asynchronisms. The frequency detection portion of the AM recognition process provides additional protection against false detection during write splices and unformated surface. Programming the user gap prior to the AM with a constant 5T pattern will guarantee that any false detection of six and/or nine "0" intervals, will not result in an address mark detection, as the 5T gap falls outside the threshold of the HF detection circuitry. False detections of this kind are not unlikely, as a 6T interval in a data field CRC, followed by a 9T interval in the write splice is entirely possible.

To prevent lockup of the detection circuitry, time-outs are provided for nine "0" detection and for HF detection. As can be seen from "Table 6-1, Address Mark Detect Sequences", several AM detection sequences are possible. In the most extreme case (Case 3), nine "0"s should be detected no more that 34T after the six "0" detect, remembering that the six "0" detect may actually occur 1T earlier in the event that the AM begins with a 9T. Similarly, HF must be detected no later than 24T following detection of nine "0"s.

In the event that either a six "0" detect or a six "0"/nine "0" detect is tripped in the write splice preceding the gap, the gap length needs to be long enough that the respective time-outs do not occur within the real AM following the gap. This is accomplished by formatting a gap length of no less than 3 NRZ bytes.

In summary, formatting a minimum of 3 NRZ bytes of 5T gap prior to any AM will greatly reduce the susceptibility to false AM detection. This can be done with a repeating $735CD_H$ NRZ gap pattern assuming even framing, or a $35CD7_H$ repeating for odd framing.



* The leading 8T interval may increase to 9T, thus the six "0"s will be detected 1T earlier.

TABLE 6-1. ADDRESS MARK DETECT SEQUENCES

7.0 ENCODER/DECODER

Encoding and Decoding in the WD10C27 is based on the IBM 2/3, 1, 7 RLL code. The following sections describe the Encoder, Decoder, and related framing issues.

7.1 ENCODING

NRZ data is encoded based on five bits: the current NRZ data word, C_1C_0, the next NRZ data word, N_1N_0, and the last bit of the previous RLL code word, R_0. These five bits are used to produce the current three bit RLL code word, $R_2R_1R_0$.

Although intended to reflect the Decode process, Figure 7-1 - Code Word to Data Word Relationship exemplifies the 2/3 rate relationship between the NRZ data word and RLL code word.

7.2 DECODING

Synchronized RLL data is decoded based on seven bits: the current three bit RLL code word, $C_2C_1C_0$; the last two bits of the previous code word, P_1P_0; and the first two bits of the next code word, N_2N_1. The seven bit sequence is analyzed and the appropriate two bit NRZ data word, Z_1Z_0, is output.

At the velocity lock-to-phase lock transition, the Data Detector is enabled and the Decoder begins to see synchronized RLL data and clock. Although the synchronization field of repeating "001" is self framing for a 2/3 rate code, pattern matching is performed on the synchronized data to further ensure correct framing. When the pattern "001001001" has been detected, the Decoder is enabled and the synchronized RLL data is decoded to NRZ and presented at the RDATA output.

The NRZ data words are clocked into a FIFO at the channel rate established by the Data Synchronizer. The FIFO output is clocked off of the Data Synchronizer's NRZ clock and presented at the RDATA output centered about the rising edges on RCLK.

CASE NO.	NRZ DATA WORD IN		RLL CODE WORD OUT	
	Current C_1C_0	Next N_1N_0	Previous R_0	Current $R_2R_1R_0$
1	00	00	0	001
2	00	00	1	001
3	00	01	0	001
4	00	01	1	001
5	00	10	0	000
6	00	10	1	010
7	00	11	0	000
8	01	11	1	010
9	01	00	0	001
10	01	00	1	010
11	01	01	0	001
12	01	01	1	000
13	01	10	0	000
14	01	10	1	000
15	01	11	0	000
16	01	11	1	000
17	10	00	0	101
18	10	01	0	101
19	10	10	0	010
20	10	11	0	010
21	11	00	0	010
22	11	01	0	100
23	11	10	0	100
24	11	11	0	100
Exhaustive encode pattern: $0132149AD7E3770_{HEX}$				

TABLE 7-1. EXPANDED 1,7 ENCODE RULES

Of the 128 possible combinations of the seven bit decode word given by $P_1P_0C_2C_1C_0N_2N_1$, all but 34 have adjacent ones and are therefore illegal due to the *d* constraints of the 1,7 RLL code. Although the decode table may be reduced to less than 34 entries, the expanded table has been presented here for your convenience.

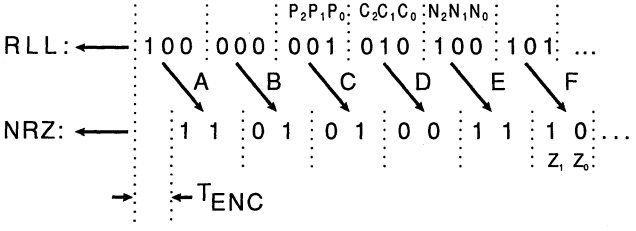
If the Decoder sees a "11" anywhere in the decode word, the NRZ data word will be forced to either a "00" or "11" based on the stated of the ERRPAT bit in the Configuration register, and the DECERR bit will be set to indicate that a decode error has occurred.

There are other RLL sequences which may not be realized by virtue of the encode rules, however these do not result in decode errors, In other words, since the encode rules are a subset of the decode rules, there are many RLL sequences which may be decoded legally, but which could never have been encoded to start with. This is evident when the Encode-Decode process is run in reverse. For certain RLL sequences, including those containing 7T7T7T...7T, 7T87, 8787...87, and 8T7T, the RLL output of the Encoder will not match the original RLL input to the Decoder. Another obvious example is a sequence of more than seven zeroes. While this is an illegal Encode due to the *k* constraints in the 1,7 RLL code, the Decoder will simply output 0101... (case 1) in response to this constant zero input.

Therefore, determination of a NRZ sequence which results in a specific RLL sequence may not necessarily be accomplished by use of the Decoder. The Encode-Decode process is not guaranteed to run in reverse.

21

Code Word Relationship



Decode Table Entry

	$P_1P_0C_2C_1C_0N_2N_1 \rightarrow Z_1Z_0$
A) Case 9	XX10000 → 11
B) Case 1	0000000 → 01
C) Case 5	0000101 → 01
D) Case 21	0101010 → 00
E) Case 12	1010010 → 11
F) Case 10	00101XX → 10

FIGURE 7-1. CODE WORD TO DATA WORD RELATIONSHIP

Case No.	1,7 RLL Code Word			NRZ Data Word
	Previous $P_1 P_0$	Current $C_2C_1C_0$	Next $N_2 N_1$	NRZ $Z_1 Z_0$
1	00	000	00	01
2	00	000	01	01
3	00	000	10	01
4	00	001	00	01
5	00	001	01	01
6	00	010	00	11
7	00	010	01	10
8	00	010	10	10
9	00	100	00	11
10	00	100	01	11
11	00	100	10	11
12	00	101	00	10
13	00	101	01	10
14	00	000	00	01
15	01	000	01	01
16	01	000	10	01
17	01	001	00	00
18	01	001	01	00
19	01	010	00	01
20	01	010	01	00
21	01	010	10	00
22	10	000	00	00
23	10	000	01	00
24	10	000	10	00
25	10	001	00	00
26	10	001	01	00
27	10	010	00	11
28	10	010	01	10
29	10	100	00	11
30	10	100	01	11
31	10	100	10	11
32	10	101	00	10
33	10	101	01	10
34	10	101	01	10
Exhaustive decode pattern: 010200402202412122512445104205210124 25 OCT				

TABLE 7-2. EXPANDED 1,7 DECODE RULES

7.3 FRAMING

Framing is the determination of a specific data word to code word boundary. Framing during the decode process is assured by the 001 pattern in the synchronization field. This pattern is self-framing in the sense that the code work boundary is unambiguous. However, as the encode process has no synchronization byte, the Encoder must make some assumptions about the data word boundary. For example, if the NRZ sequence on WDATA is ...000000101001000..., it is important to know if this should be encoded as ...00/10/10/01/00... or as ...00/01/01/00/10/00..., as these will produce different encoded sequences.

7.3.1 Framing in Hard Sector Formats

Upon assertion of ENCEN and after some synchronization delay, WDATA is shifted into a FIFO on the rising edges of WCLK. The output of the FIFO is clocked using the channel rate clock, T_{RLL}. In this way, two bits of WDATA are presented to the Decoder for every 3 T_{RLL}'s satisfying the 2/3 code rate requirement of 1,7 RLL.

Framing during the encode process is accomplished via the $\overline{\text{AMODD}}$ and $\overline{\text{ENODD}}$ bits in the configuraiton register. Framing following address marks is based on the sense of $\overline{\text{AMODD}}$, and is discussed in 7.3.2 Framing In Soft Sector Formats.

$\overline{\text{ENODD}}$ established framing for encoding following assertion of ENCEN. In soft sector formats, this applies to gap data which precedes the AM, and to user data following the synchronization field. When $\overline{\text{ENODD}}$ is active (low), framing will be established assuming that the two bit NRZ data word begins on an odd numbered bit in the NRZ data byte. Thus, the first transition on WDATA must occur in bits 7, 5, 3 or 1 of the NRZ byte $N_7N_6N_5N_4N_3N_2N_1N_0$, and the NRZ data words N_7N_6, N_5N_4, N_3N_2, N_1N_0, etc., will be encoded. If $\overline{\text{ENODD}}$ is inactive (high), framing will be even such that the NRZ data words N_6N_5, N_4N_3, N_2N_1, N_0N_7, etc., are encoded. In this case, the first transition on WDATA must occur in bits 6, 4, 2 or 0.

As an example, the sequence ...00AA$_H$..., if intended to be encoded as ...00/00/10/10..., would require $\overline{ENODD}$ = 0 to establish odd framing. $\overline{ENODD}$ = 1 would result in encoding this same sequence as ...00/00/01/01... It can be seen from Table 7-1 - Expanded 1,7 Encode Rules that these two Encoder inputs will result in different RLL outputs.

Since ENCEN is asserted prior to gap during formats, and prior to data fields during writes, the odd/even framing requirement must be consistent. This implies that the data field synchronization byte, usually written just after the synchronization field, and the 5T gap data must both have either odd or even framing.

7.3.2 Framing in Soft Sector Formats

Framing must be re-established following the insertion of address. While $\overline{ENODD}$ is used to establish framing following assertion of ENCEN for gaps and data field synchronization bytes, $\overline{AMODD}$ is similarly used following assertion of AME to establish framing for ID synchronization bytes.

Following the address mark generation, WDATA is once again encoded and shifted out to $\overline{WPCDATA}$. Because WDATA must be 00H following the AM to generate the 3T synchronization field, framing does not take place until the first non-zero transition is seen on WDATA. At this time, framing is forced to be either odd or even as described above.

21

8.0 CHANNEL CONTROL DACS

The WD10C27 provided three DACs which have been specifically designed to optimize the variable frequency read channel's frequency, boost, and hysteresis characteristics. The DACs have been specifically designed to be compatible with the SSI3040 Electronic Filter/Pulse Detector. In addition, a unique method of maintaining servo field optimization is also incorporated.

In a typical application, each DAC is programmed based on the optimization cut-off frequency, hysteresis, and boost settings for a given zone. These values are loaded into the DAC control registers as a 5-bit unsigned integer. Independent values, optimized for the servo fields, are loaded into the equivalent servo control registers. The DAC outputs are then dynamically switched between the logical and servo settings via the SGATE input.

DACs should be enabled by setting the DACEN bit in the respective DAC control register. When a DAC is disabled, the output is placed in a high impedance state and power shut off to the relevant circuits. The reset/low power states invoked via the ARSTPDN bit in the Configuration regists clear the DAC registers and thereby leave the DACs disabled. Reset/low power mode, issued via the RSTPDN bit, will not have any effect on the DAC functions.

8.1 FAST AGC

When DAC settings are being modified "on-the-fly", special considerations must be made to keep the AGC recovery times at a minimum. This includes not only the "data-to-servo" and servo-to-data" recovery at the SGATE transitions, but the recovery times encountered at the leading edge of CHEN when duty cycling CHEN for power management. See 8-2, "Duty Cycling with CHEN".

In much the same way as a "write-to-read" recovery scenario, it is desirable to assure that AGC is in a fast attach whenever the DACs are switched. Whenever a modification to the cutoff frequency is made such that the cutoff frequeency is reduced, the effect is to place the AGC circuits in a slow dacay mode. This is highly undesirable as the AGC recovery time may be extremely long. Unfortunately, this situation arises whenever the cutoff frequency in the servo fields is lower than in the data zones.

The FSTABC (fast AGAC) pin has been provided to force fast AGC recovery. By setting the BYPMODE bit in the configuration register, this pin may be connected to the BYP capacitor of the AFC circuits and used to force fast attack. On either edge of SGATE, when the DAC values switch from servo to data or vice versa, the FSTAGC pin will discharge the BYP capacitor by pulling up towards +4V. In this way, fast attack can be guaranteed.

8.2 DUTY CYCLING WITH CHEN

To provide for minimal power consumption by the channel electronics, a CHEN (channel enable) signal may be used for power management. Since servo fields represent a small percentage of the total surface format, a significant power savings may be accomplished by de-asserting CHEN during the logical fields, and asserting CHEN over the servo fields. This technique is known as "CHENing".

When CHEN is low, the DACs are forced into a configuration which will optimize read channel recovery time and minimize power consumption: the FCDAC will be forced to 8 LSB's; the BCDAC will be forced to ground; and the HCDAC will be forced to +5V.

To minimize transient response upon re-assertion of CHEN, it is desirable to keep current flowing at the IREF (IFO) and FCDAC (IFI) pins. As the current reference from the SSI3040 will be disabled when CHEN is low, a current into the IREF input may be established in one of two ways:

1. With the BYPMODE bit in the configuration register disabled, FSTAGC will be pulled towards +5V during CHEN low. By placing an external resistor between FSTAGC and IREF, a programmable current may be established. This current should be programmed such that upon re-assertion of CHEN, fast attack is guaranteed in the AGC.

2. With the BYPMODE in the configuration register enabled, an internal current source is steered to the IREF input. This current source is of sufficient tolerance to keep FCDAC and SSI3040 related circuits out of saturation. AGC fast attack is ensured via the connection of FSTAGC to the BYP capacitor.

8.3 FREQUENCY CONTROL

The Frequency Control DAC, FCDAC, has been specifically designed to allow for bandwidth optimization of the read channel. In a typical variable frequency application, selection of the channel bandwidth is made based on signal-to-noise ratio and recording frequency considerations.

FCDAC is a current DAC whose compliance is set by an external current reference applied at the IREF input. FCDAC is enabled and programmed via the FCDAC register described in section 2.2.5, "Channel Control Registers."

The FCDAC will be forced to 8 LSBs when CHEN is low.

8.4 BOOST CONTROL

The Boost Control DAC, BCDAC, has been specifically designed to allow for programmable pulse slimming. BCDAC is a voltage DAC whose compliance is set by an external voltage reference applied at the VRG input. BCDAC is enabled and programmed via the BCDAC register described in section 2.2.5, "Channel Control Registers."

Although BCDAC is a five bit DAC, the lower two counts (00000 and 00001) are used to indicate a no boost control state. When the lower two counts are programmed, the BCDAC output is clamped to ground rather than following the normal DAC progression. When used in conjunction with the SSI3040, this stated will be sensed and the 3040 will assume a nominal boost value.

Note that after ARSTPDN, BCDAC will be set to a zero count but will be disabled. Enabling the DAC without modifying the count will result in the no boost configuration.

The HCDAC will be forced to ground when CHEN is low.

8.5 HYSTERESIS CONTROL

Hysteresis Control DAC, HCDAC, has been specifically designed to allow for threshold optimization under microprocessor control. HCDAC is a voltage DAC whose compliance is set as a programmable ratio of the voltage difference seen between the LEVEL and VRG inputs. When HCDAC is connected to the hysteresis input of the pulse detector, the threshold will automatically maintain the programmed ratio as the amplitude of the voltage on the LEVEL input changes.

HCDAC is enabled and programmed via the HCDAC and SHCDAC registers described in section 2.2.5, "Channel Control Registers."

If desired, HCDAC may be converted into a voltage DAC configuration identical to that the BCDAC by disabling the HCTL bit in the HCDAC resister. When HCTL is inactive, the DAC characteristics will be as described in section 8.4, "Boost Control". In this configuration, the LEVEL input is used as a voltage reference, and the VRG input is unused.

The HCDAC will be forced to +5V when CHEN is low, regardless of the state of the HCTL bit in the HCDAC register.

9.0 PERFORMANCE SPECIFICATIONS

9.1 MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical Characteristics.

PARAMETER	RATING	UNIT
V_{DD} with respect to V_{SS}	+7	V
Voltage on any pin with respect to V_{SS} (ground)	-0.5 to +7	V
Ambient Operating Temperature (T_A)	0 to 70	°C
Storage Temperature	-55 to +125	°C
ESD Protection	5000	V
Latchup Immunity	40	mA

TABLE 9-1. ABSOLUTE MAXIMUM RATINGS

9.2 DC ELECTRICAL CHARACTERISTICS

The following specifications are over T_A = 0°C to 70°C, T_J = 0°C to 90°C and V_{DD} = +5V ± 250mV. When indicated (*), limits represent characterized values and are not tested.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{DDA} †	Active Power Supply Current		25 50 60	30 75 85	mA mA mA	@ 7.5 MBps @ 27 MBps @ 33 MBps
I_{DDLP} ‡	Power Down Supply Current		2.0 0.6	4.0 1.5	mA mA	RSTPDN=1, CHEN=1 RSTPDN=1, CHEN=0
I_{DDLPA} ‡	All Power Down Supply Current		0.3	1	mA	ARSTPDN = 1
t_{RDY}*	Time from valid configuration to full operating capability (e.g., lockup of PLLs)			3	ms	

† Measured during write operations with V_{DD} = 5.25V at 0°C.
Typical values are at ambient temperature and V_{DD} = 5.0V.

‡ Measured with all inputs at ground (or V_{DD}), V_{DD} = 5.25V, and 0°C.
Typical values are at ambient temperature and V_{DD} = 5.0V.

TABLE 9-2. POWER SUPPLY SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): XTLI, XTLO						
V_{IH}	Input High Voltage	2.0	1.4		V	$f_{XTL} \leq 16$ MHz
V_{IL}	Input Low Voltage		1.4	0.8	V	$f_{XTL} \leq 16$ MHz
V_{IBIAS}	Input Bias Voltage	1.0		1.8	V	XTLO floating, V_{DD} = 5V
I_{ILKX}	Crystal Input Leakage Current			±100	nA	XTLI = XTLO = V_{IBIAS}
I_{OLS}	Short Circuit Sink Current	1.8		10	mA	XTLO=V_{DD}=5V.XTLI=2.5V
I_{OHS}	Short Circuit Source Current	0.6		4.0	mA	V_{DD}=5V.XTLO=XTLI=0V
R_{BO}	Operating Bias Resistance	2.0		2.7	MΩ	V_{DD}=5V.XTLI=V_{IBIAS}, XTLO=0V

TABLE 9-3. CRYSTAL OSCILLATOR DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AD7-0, $\overline{\text{MWE}}$, $\overline{\text{MRE}}$, $\overline{\text{MCS}}$, *ALE, AME, ENCEN, RGATE, LPF (test),* $\overline{\text{RAWDATA}}$, *WDATA, WCLK, CHEN,* $\overline{\textit{HRESET}}$						
V_{IH}	Input High Voltage	2.0	1.4		V	
V_{IL}	Input Low Voltage		1.4	0.8	V	
I_{ILK}	Input Leakage Current			±10	µA	

TABLE 9-4. INPUT RECEIVERS DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): $\overline{\text{AMD}}$, RDATA, RCLK						
V_{OH}	Output High Voltage	2.4			V	IOH = -20 µA
V_{OL}	Output Low Voltage			0.4	V	IOL = +20 µA
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT} = V_{SS} TO V_{DD}, HIZEN=1
T_{RS}*	Output Rise Time			2.5	ns	V_{OUT} = 0.8V TO 2.0V C_L = 20 pF
T_{FL}*	Output Fall Time			2.1	ns	V_{OUT} = 2.0V TO 0.8V C_L = 20 pF
PIN(S): WINCLK, DELRD, $\overline{\text{WPCDATA}}$, $\overline{\text{CHEN}}$, BCS						
V_{OH}	Output High Voltage	2.4			V	IOH = -1mA
V_{OL}	Output Low Voltage			0.4	V	IOL = +1mA
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT}=V_{SS} TO V_{DD}, HIZEN=1
T_{RS}*	Output Rise Time			2.3	ns	V_{OUT} = 0.8V TO 2.0V C_L = 20pF. R_L = 20kΩ to V_{SS}
T_{FL}*	Output Fall Time			1.4	ns	V_{OUT} = 0.8V TO 2.0V C_L = 20pF. R_L = 2kΩ to V_{DD}
PIN(S): $\overline{\text{PORT0-4}}$						
V_{OL}	Output Low Voltage			0.4	V	IOH = +8mA. Open Drain
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
PIN(S): AD7-0						
V_{OH}	Output High Voltage	2.4			V	IOH = -1mA
V_{OL}	Output Low Voltage			0.4	V	IOL = +1mA
I_{OZ}	Output Tri-state Leakage Current			±10	µA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
t_{RS}*	Output Rise Time			13	ns	V_{OUT} = 0.8V to 2.0V CL = 100 pF R_L = 20kΩ to V_{SS}

TABLE 9-5. OUTPUT DRIVE DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): DSPMP, VCON, LPF						
I_{ILKP}	DSPMP Input Leakage Current			±100	nA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
I_{ILKV}	VCON Input Leakage Current			±100	nA	V_{CON} = V_{DD}, HIZEN=1
I_{ILKL}	LPF Input Leakage Current			±10	µA	V_{OUT}=V_{SS} to V_{DD}, HIZEN=1
R_{PV0}	DSPMP to VCON Resistance. BAND0		∞		Ω	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{PV1}	DSPMP to VCON Resistance. BAND1		∞		Ω	DSPMP=1.5V. VCON=2V, V_{CC}=5V
R_{PV2}	DSPMP to VCON Resistance. BAND2	2.0	3.01	4.9	kΩ	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{PV3}	DSPMP to VCON Resistance. BAND3	1.0	1.5	2.45	kΩ	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{PVV}	DSPMP to VCON Vlock Resistance	50		1700	Ω	DSPMP=1.5V. VCON=2V, V_{DD}=5V
R_{LPF0}	LPF Resistance to ground. BAND0		∞		Ω	LPF = 200mV, V_{DD}=5V
R_{LPF1}	LPF Resistance to ground. BAND1	1.3	2.2	4.3	kΩ	LPF = 200mV, V_{DD}=5V
R_{LPF2}	LPF Resistance to ground. BAND2	0.8	1.4	2.7	kΩ	LPF = 200mV, V_{DD}=5V
R_{LPF3}	LPF Resistance to ground. BAND3	0.48	0.7	1.65	kΩ	LPF = 200mV, V_{DD}=5V

TABLE 9-6. DATA SYNC. INTERNAL FILTER DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): DSPMP, VCON						
V_{HFCA}	VCO High Freq. Clamp Act. Voltage †	2.7		3.9	V	$I_{DSPMP} \geq 2.5mA$, $V_{DD}=5V$
V_{HFCD}	VCO High Freq. Clamp De-act. Voltage †	0.45		1.15	V	$I_{DSPMP} \leq 2.5mA$, $V_{DD}=5V$
V_{LFC}	VCO Low Frequency Clamp Voltage ‡	0.5		0.95	V	$I_{VCON} = -1\mu A$, $V_{DD}=5V$
I_{HFC}	VCO High Frequency Clamp Current †	4		15	mA	VCON=DSPMP=V_{DD}=5V
I_{LFC}	VCO Low Frequency Clamp Current ‡	1.3		4.5	mA	VCON = 0V, V_{DD}=5V

† The VCO high frequency clamp will activate when the voltage sensed on VCON rises above the high frequency clamp activation voltage, V_{HFCA}. The clamp is latched, pulling DSPMP low and discharging the filter. When all of the VCO energy is discharged and internal VCO control voltages fall below the VCO High Frequency Clamp De-activation Voltage, V_{HFCD}, the clamp is released. V_{HFCD} is BAND dependent. Clamp voltages and currents should be measured after stopping all clocks and tri-stating the phase detector by pulsing HIZEN.

‡ The VCO low frequency clamp on when the voltage sensed on VCON falls below the VCO Low Frequency Clamp Voltage, V_{LFC}. Voltage and currents should be measured after stopping all clocks and tri-stating the phase detector by pulsing HIZEN

TABLE 9-7. DATA SYNCHRONIZER INTERNAL VCO DC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): IREF, VRG, FCDAC (with CHEN=1)						
I_{REF}	External Current Reference	100		400	µA	$0.7V \leq V_{IREF} \leq 1.6V$
I_{OZ}	FCDAC Tri-state Output Leakage			±100	nA	$V_{OUT}=V_{SS}$ to V_{DD}, DACEN=0
LSB_T‡	Theoretical Resolution (5-bit)		I_{REF}/12		mA	for codes 0 through 31
GAIN‡	Gain (LSB) Accuracy			±8.0	%LSB_T	100*(LSB_R-LSB_T)/LSB_T
$I_{INITIAL}$‡	Code Zero Current		8		LSB_R	
I_{OFFSET}‡	Offset Current			±7.0	%I_{REF}	
INL†	Integral Non-Linearity			±0.5	LSB_R	
DNL‡	Differential Non-Linearity			±0.5	LSB_R	
R_L*	External Series Resistive Load			2k	kΩ	
PSRR*	Power Supply Rejection Ratio	30	40		dB	w/o external filtering
t_S*	Setting Time from SGATE Transitions			150	ns	w/ 10pF and R_L external load to 90% of final value
PIN(S): IREF, FCDAC (with CHEN = 0)						
V_{IREF}	IREF Voltage Accuracy	0.65		1.5	mV	error from (0.48) VRG
I_{CFC}	CHEN Mode Forced FCDAC Current	40 50		235 75	µA µA	BYPMODE=1, Internal I_{REF} BYPMODE=0, R_F = 40KΩ
PIN(S): FSTAGC						
I_{FSTAGC}	Source Current	3			mA	$V_{FSTAGC} \leq V_{RST}$
V_{RST}	Fast AGC Threshold Voltage			.8V_{DD}	V	BYPMODE=1
I_{OZ}	Tri-state Output Leakage			±100	nA	$V_{OUT}=V_{SS}$ to V_{DD}, DACEN=0

† LSB_T is the theoretical resolution. It should not be confused with LSB_R which is derived from the regression analysis. The regression equation is given by:

$$I_R \text{ (code)} = LSB_R^* \text{ (code+8)} + I_{OFFSET} = LSB_R^* \text{ code} + I_{INITIAL} + I_{OFFSET}$$

The theoretical equation is given by:

$$I_T \text{ (code)} = LSB_T^* \text{ (code+8)} + 0 = (I_{REF}/12)^* \text{(code+8)} + 0.$$

The offset, I_{OFFSET}, is defined to exclude all gain error. Therefore, the offset is determined at the "zero LSB" point extrapolated from the regression equation, I_R (code = -8).

TABLE 9-8. FREQUENCY CONTROL DAC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): VRG, LEVEL, HCDAC w/$\overline{HCTL}$ = 0 and CHEN = 1 (See "Boost Control DAC Specifications" when $\overline{HCTL}$ = 1)						
V_{RG}	External Voltage Reference	2.2		2.45	V	$I_{IN} \leq$ 2 mA maximum sink
$V_{INITIAL}$†	Measured Code Zero Voltage	[V_{DD}-(30/31)*V_{RG}] ±0.04			V	
LSB_T†	Theoretical Resolution (5-bit)		V_{DIF}/31		V	$V_{DIF}=V_{LEVEL} - V_{INITIAL}$ $0.5V \leq V_{DIF} \leq 1.0V$
GAIN†	Gain (LSB) Accuracy			±0.4	%LSB_T	100*(LSB_R-LSB_T)/LSB_T
INL†	Integral Non-Linearity			±0.5	LSB_R	
DNL†	Differential Non-Linearity			±0.5	LSB_R	
PSRR*	Power Supply Rejection Ratio	35	40		dB	
t_S*	Setting Time from SGATE Transitions			2	µs	to 90% of final value with 10pF external load
PIN(S): HCDAC (w/$\overline{HCTL}$=0 or 1 and CHEN=0)						
V_{CHC}	CHEN Mode Forced HCDAC Voltage		CV_{DD}		V	

† LSB_T is the theoretical resolution. It should not be confused with LSB_R which is derived from the regression analysis. The regression equation is given by:

$$V_R(code) = LSB_R * code + V0.$$

The theoretical equation is given by:

$$V_T(code) = LSB_T * code + V_{INITIAL} = (V_{LEVEL} - V_{INITIAL}) * (code/31) + V_{INITIAL}.$$

TABLE 9-9. HYSTERESIS CONTROL DAC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): VRG, BCDAC (with CHEN = 1)						
V_{RG}	External Voltage Reference	2.2		2.45	V	$I_{IN} \leq 2$ mA maximum sink
V_{OFFSET}†	Offset Voltage		±15	±30	mV	Extrapolated Regression Code 0
$V_{INITIAL}$†	Code Zero/One Voltage		0	+20	mV	for codes 0 through 1
LSB_T†	Theoretical Resolution (5-bit)		V_{RG}/31		V	for codes 2 through 31
GAIN†	Gain (LSB) Accuracy		±0.1	±0.4	%LSB_T	100*(LSB_R-LSB_T)/LSB_T
INL†	Integral Non-Linearity			±0.5	LSB_R	for codes 2 through 31
DNL†	Differential Non-Linearity			±0.5	LSB_R	for codes 2 through 31
PSRR*	Power Supply Rejection Ratio	40	45		dB	w/o external filtering
t_S*	Setting Time from SGATE Transitions			2	µs	to 90% of final value with 10pF external load
PIN(S): BCDAC (w/CHEN=0)						
V_{cbc}	CHEN Mode Forced BCDAC Voltage		CV_{SS}		V	

† LSBT is the theoretical resolution. It should not be confused with LSBR which is derived from the regression analysis. The regression equation is given by:

$V_R(code) = LSB_R*code + V_{OFFSET}$ (for codes 2 through 31).

The theoretical equation is given by:

$V_T(code)=LSB_T*code + 0 = (V_{RG}/31)*code + 0$ (for codes 2 through 31).

The offset, V_{OFFSET}, is defined to exclude all gain error. Therefore, the offset is determined at the "zero LSB" point extrapolated from the regression equation, $V_R(code=0)$.

TABLE 9-10. BOOST CONTROL DAC SPECIFICATIONS

9.3 AC ELECTRICAL AND TIMING CHARACTERISTICS

The following specifications are over T_A = 0°C to 70°C, T_J = 0°C to 90°C, V_{SS} = 0V, V_{DD} = +5V ± 250mv (max of 50mV p-p ripple), V_{OH} = 2.0V, V_{OL} = 0.8V, V_{IL} = 0.4V, V_{IH} = 2.4V, and $f_{XTL} \leq 40$ MHz unless otherwise specified. When indicated (*), limits represent characterized values and are not tested.

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
			PIN(S): XTLI, XTLO			
f_{XTL}	Crystal Input Frequency			16 20 40	MHz MHz MHz	Active Stage, $\overline{HFCEN}$-1 Ext., $\overline{HFCEN}$=1, 40/60% D_{CYC} Ext., $\overline{HFCEN}$=0, 40/60% D_{CYC}
t_{XS}*	Crystal Start-up Time Following Reset		1	3	ms	
C_{IN}	Crystal External Input Capacitance		100 68 33		pF pF pF	$f_{XTL} \leq 5$ MHz 5 MHz $\leq f_{XTL} \leq$ 10 MHz 10 MHz $\leq f_{XTL} \leq$ 16 MHz
C_{OUT}	Crystal External Output Capacitance		68 47 22		pF pF pF	$f_{XTL} \leq 5$ MHz 5 MHz $\leq f_{XTL} \leq$ 10 MHz 10 MHz $\leq f_{XTL} \leq$ 16 MHz

TABLE 9-11. CRYSTAL OSCILLATOR TIMING SPECIFICATIONS

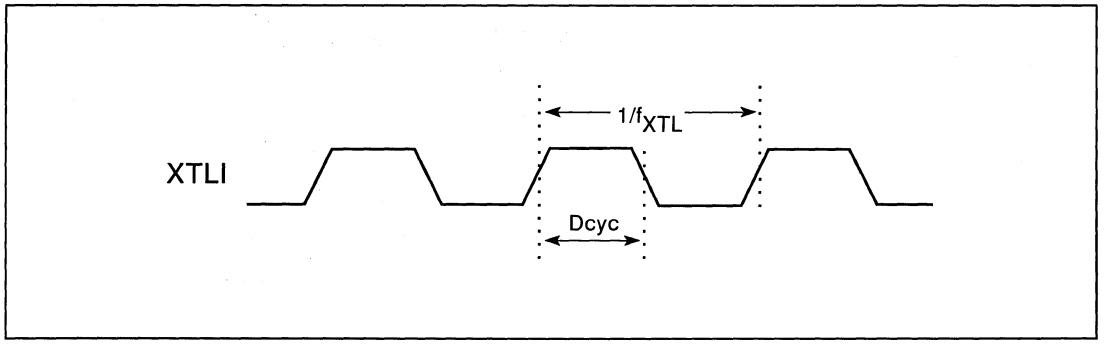


FIGURE 9-1. CRYSTAL INPUT TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AME, ENCEN, WDATA, WCLK, $\overline{\text{WPCDATA}}$						
t_{SWC}	Setup of ENCEN and WDATA to WCLK Rising	5			ns	
t_{HWC}	Hold of ENCEN and WDATA from WCLK Rising	5			ns	
f_{NRZ}	WCLK Frequency ($1/T_{NRZ}$)	7.5		33	MHz	40/60% Duty Cycle
t_{ENCON1}	ENCEN Rising to Encode On	t_{SWC}		t_{SWC} +1	T_{NRZ}	
t_{ENCOFF}	ENCEN Falling to $\overline{\text{WPCDATA}}$ Off	t_{SWC}		tSWC +2	T_{NRZ}	
t_{ENC}	WDATA to $\overline{\text{WPCDATA}}$ Encode Delay	10		16	T_{NRZ}	w/o RLL and w/max. precomp.

TABLE 9-12. ENCODER TIMING SPECIFICATIONS

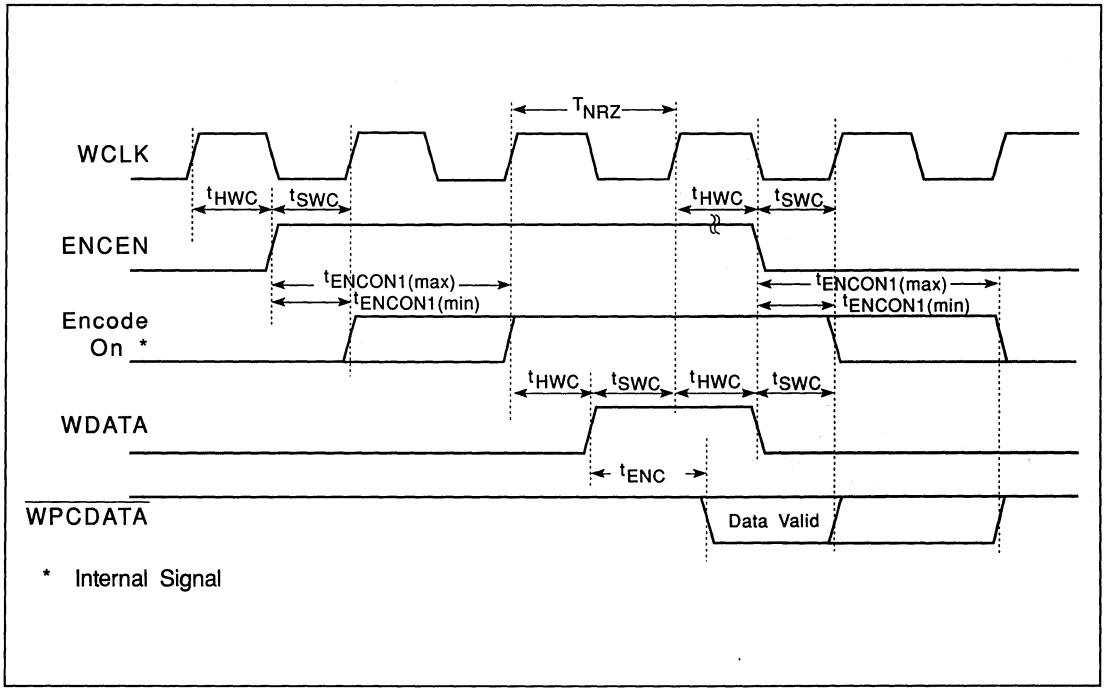


FIGURE 9-2. ENCODER TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AME, ENCEN, WDATA, WCLK, $\overline{\text{WPCDATA}}$						
t_{SWC}	Setup of AME to WCLK Rising	5			ns	
t_{HWC}	Hold of AME from WCLK Rising	5			ns	
t_{AME}	AME Pulse Width	1			T_{NRZ}	
t_{ENCON2}	AME Rising to Encode On			36	T_{NRZ}	
t_{DAM}	AME to AM on $\overline{\text{WPCDATA}}$ Delay	10		13	T_{NRZ}	w/o RLL and w/max. precomp.
t_{AM}	Address Mark Length			34	T_{NRZ}	(e.g., 51 TRLL)
t_{SAMG}	Setup of AME to End of Gap on WDATA	0			ns	
t_{GAPL}	GAP Loss (due to superposition of AM)	t_{SAMG}-(t_{ENCON2}-t_{AM})			T_{NRZ}	positive or zero means no loss
t_{PLOL}	PLO Loss (due to superposition of AM)	t_{ENCON2}-t_{SAMG}			T_{NRZ}	positive or zero means no loss

TABLE 9-13. ADDRESS MARK GENERATION TIMING SPECIFICATIONS

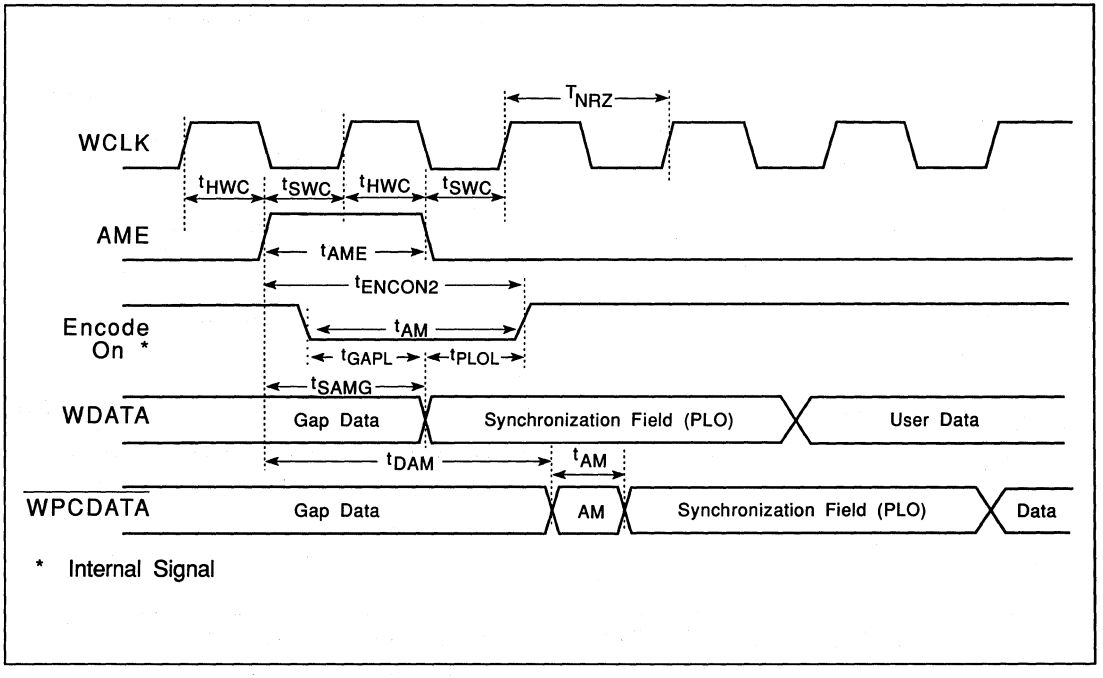


FIGURE 9-3. ADDRESS MARK GENERATION TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
			PIN(S): $\overline{\text{WPCDATA}}$			
LSB_T†	Resolution		T_{RLL} /64			for codes 0 to 15
INL	Integral Non-Linearity			±0.5	LSB_R	
DNL	Differential Non-Linearity			±0.5	LSB_R	
GAIN	Gain Accuracy			±3	$\%LSB_T$	$100*(LSB_R-LSB_T)/LSB_T$
t_{WPC}	$\overline{\text{WPCDATA}}$ Pulse Width	11/16		17/16+x	T_{RLL}	x is 10ns max. and ind. of T_{RLL}
t_{WTJ}*	$\overline{\text{WPCDATA}}$ Timing Jitter		±200 ±200		ps ps	one σ, lab supply one σ , w/filtered‡ 50mv p-p power supply ripple
t_{RL}*	Ramp Lock Loop Lock-Up Time		1.5	3	ms	from assertion of RLLEN

† LSB_T is the theoretical resolution. It should not be confused with the LSB_R which is derived from the regression analysis.

‡ See Figure 1-2 - Variable Frequency Channel Schematic.

TABLE 9-14. WRITE PRECOMPENSATION TIMING SPECIFICATIONS

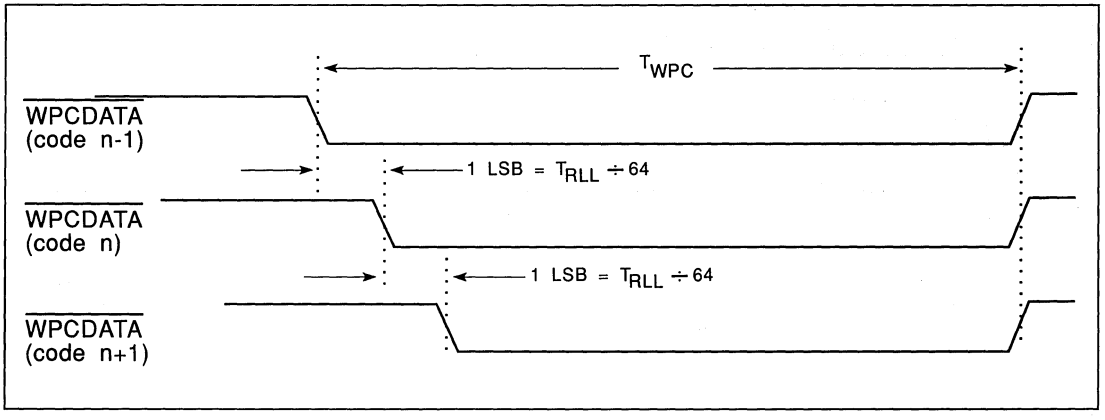


FIGURE 9-4. WRITE PRECOMPENSATION TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): AME, $\overline{\text{AMD}}$, $\overline{\text{RAWDATA}}$, RDATA, RCLK						
t_{AMD}	End of AM to $\overline{\text{AMD}}$ Valid	1		3	T_{RLL}	
t_{RG}	$\overline{\text{AMD}}$ Valid to RGATE Valid			1	Byte	
t_{LG}	End of AM† to End of Velocity Lock	60		96	T_{RLL}	user programmable 5-8 Bytes
t_{DET}	End of AM† to Start of Data Detection	t_{LG}-3		t_{LG}	T_{RLL}	
t_{DECON}	End of AM† to Decode On			t_{DET}+10	T_{RLL}	
t_{DEC}	$\overline{\text{RAWDATA}}$ to RDATA Decode Delay	1		1.25	Bytes	
t_{RAW}	$\overline{\text{RAWDATA}}$ pulse width high/low	10			ns	
t_{RDT}	Minimum $\overline{\text{RAWDATA}}$ period	1.5			T_{RLL}	w/o internal drop out
t_{RDC}	Centering of RDATA rising to RCLK rising	-5		+5	ns	from center (T_{NRZ}/2) measured during closed loop
t_{RCD}	RCLK Duty Cycle (during Read & Write)	45		55	$\%T_{NRZ}$	measured during closed loop at 0.8V and 2.0V crossings

† Specified from RGATE rising for hard sector operations.

TABLE 9-15. READ TIMING SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): $\overline{\text{RAWDATA}}$, RDATA, RCLK, DELRD, WINCLK						
t_{DWL}	Data Detection Window Loss			250	ps	open loop fixed losses
t_{DWC}	Data Detection Window Centering Error			± 1	$\%T_{RLL}$	
t_{PWC}	Phase Detection Window Centering Error			± 2	$\%T_{RLL}$	
t_{WM}	Window Monitoring Error			± 250	ps	Matching of DELRD/WINCLK to internal Data Det. Window

TABLE 9-16. PHASE & DATA DETECTION WINDOW TIMING SPECS

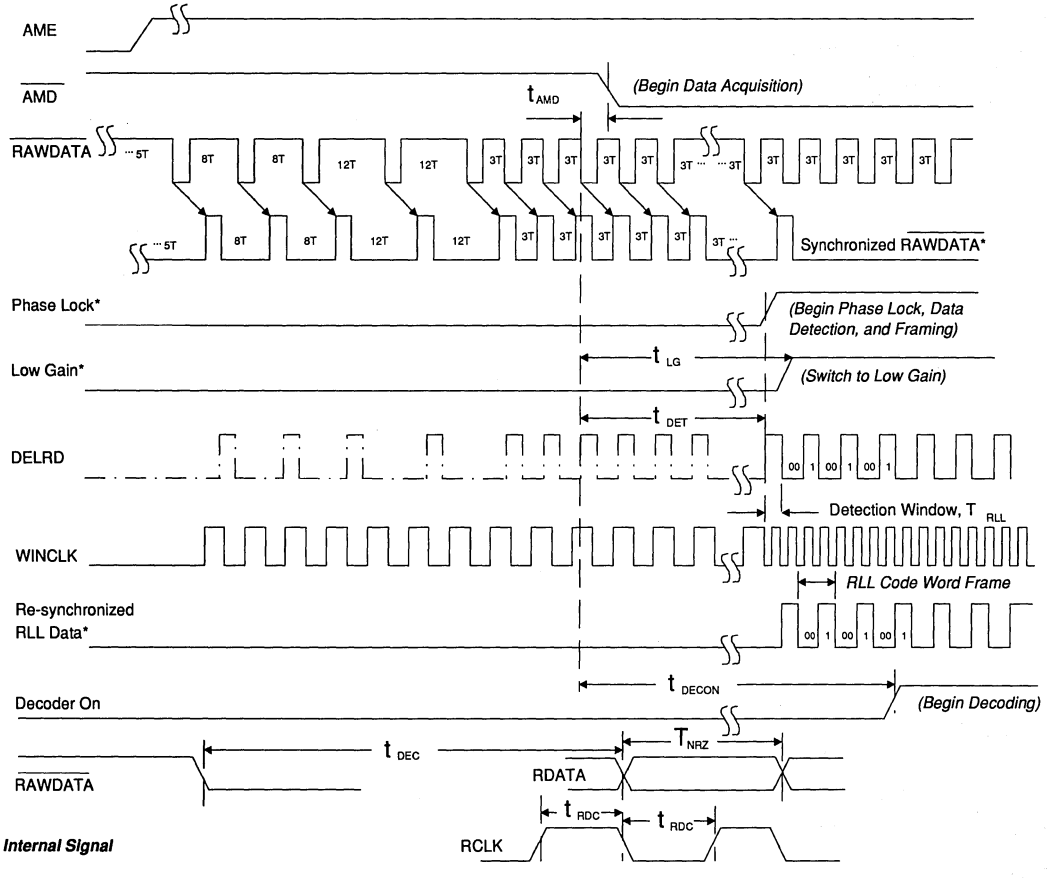


FIGURE 9-5. READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): $\overline{\text{RAWDATA}}$, RDATA, RCLK						
t_{PWS}	Percentage Window Shift Accuracy			±2	$\%T_{RLL}$	
LSB_T	Theoretical Resolution	2	δ_{wss}	6	ns	See EQ. 16.0
GAIN†	Gain (LSB) Accuracy			±TBD	$\%LSB_T$	$100*(LSB_R-LSB_T)/LSB_T$
INL†	SAM Integral Non-Linearity (Δ_{wss})		±250	±500	ps	See EQ. 18.0
DNL†	SAM Differential Non-Linearity (Δ_{wss})		±250	±500	ps	See EQ. 18.0
t_{OFFSET}†	SAM Code Zero Offset			±TBD	ns	Extrapolated Regression Code 0
t_{WL}*	WSS Lock-Up Time			3	ms	From assertion of WSSEN

† Specifications are for the full range of LSB_T, LSB_T is the theoretical resolution. It should not be confused with LSB_R which is derived from the regression analysis. The regression equation is given by:

$$\Delta_{WSSR}(code)=LSB_R*(code+1)+t_{OFFSET}.$$

The theoretical equation is given by:

$$\Delta_{WSST}(code)=LSB_T*(code+1)+0=\delta_{WSS}*(code+1)+0.$$

The offset, t_{OFFSET}, is defined to exclude all gain error. Therefore, the offset is determined at the "zero LSB" point extrapolated from the regression equation, $\Delta_{WSSR}(code=-1)$.

TABLE 9-17. WINDOW SHIFT TIMING SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): FSPMP						
t_{FTJ}*	Frequency Synthesizer Timing Jitter		±50 ±100		ps ps	one σ, lab supply one σ , w/filtered‡ 50mv p-p power supply ripple at 1-2KHz
t_{FSL}*	Frequency Synthesizer Lock-up Time		1.5	3	ms	Following COD/VCOD load

† See Figure 1-2 - Variable Frequency Channel Schematic.

TABLE 9-18. FREQUENCY SYNCHRONIZER PLL AC SPECIFICATIONS

SYM.	CHARAC-TERISTIC	SLOW	NOMINAL	FAST	UNITS	CONDITIONS
PIN(S): DSPMP, LPF, VCON (Specified for Phase Lock. V_{DD}=5V)						
K_{D0}†	Phase Detector Gain, BAND0	$1/2\pi(52f_{dr}-129)$	$1/2\pi(29f_{dr}-17)$	$1/2\pi(26f_{dr}-28)$	µA/rad	
K_{D1}†	Phase Detector Gain, BAND1	$1/2\pi(28f_{dr}-54)$	$1/2\pi(23f_{dr}-18)$	$1/2\pi(21f_{dr}-33)$	µA/rad	
K_{D2}†	Phase Detector Gain, BAND2	$1/2\pi(38f_{dr}-182)$	$1/2\pi(27f_{dr}-109)$	$1/2\pi(18f_{dr}-24)$	µA/rad	
K_{D3}†	Phase Detector Gain, BAND3	$1/2\pi(31f_{dr}-131)$ $1/2\pi(208f_{dr}-4800)$	$1/2\pi(17f_{dr}-3)$ $1/2\pi(23.2f_{dr}-117)$	$1/2\pi(15f_{dr}-33)$ $1/2\pi(14.3f_{dr}-1)$	µA/rad µA/rad	$19.1\le f_{dr}\le 27$ MHz $27.0\le f_{dr}\le 33$ MHz
K_{O0}†	VCO Gain, BAND0	$-17f_{dr}+218$	$-12f_{dr}+308$	$-23f_{dr}+469$	%/V	
K_{O1}†	VCO Gain, BAND1	$-13f_{dr}+254$	$-13f_{dr}+363$	$-8f_{dr}+356$	%/V	
K_{O2}†	VCO Gain, BAND2	$-11f_{dr}+251$	$-8f_{dr}+331$	$-14f_{dr}+513$	%/V	
K_{O3}†	VCO Gain, BAND3	$-6f_{dr}+177$	$-7f_{dr}+362$	$-9f_{dr}+510$	%/V	$19.1\le f_{dr}\le 27$ MHz $27.0\le f_{dr}\le 33$ MHz
K_{V3}†	Open Loop Gain Limit, BAND3	$1/2\pi(60000)$	$1/2\pi(76000)$	$1/2\pi(92000)$	%µA/V	f_{dr}=33 MHz
R_{KDG}	Acquisition to Tracking Gain Ratio	1.9	2.0	2.1		$K_{D(ACQ)}$:$K_{D(TRACK)}$
R_{KDS}	Up to Down Symmetry Ratio	0.95	1.0	1.05		$K_{D(UP)}$:$K_{D(DOWN)}$
t_{DTJ}*	Data Synchronizer Timing Jitter		±0.25 ±0.25		%T_{DR} %T_{DR}	one σ, lab supply, 3T data (001) one σ, w/filtered‡ 50mv p-p power supply ripple at open loop unity gain, 3T data (001)

† K_D varies with frequency, inversely as K_O, to linearize loop gain product (K_V=K_D*K_O). K_D and K_O are specified as linearized gains, using the measured VCON voltages found at the frequency extremes of each of the frequency bands. Slow and fast values represent variations in the linear approximation due to process, temperature, and voltage variations. The open loop gain product K_V should be calculated within a given speed corner. Note that K_D doubles during high gain acquisition.
‡ See Figure 1-2 - Variable Frequency Channel Schematic.

TABLE 9-19. DATA SYNCHRONIZER PLL AC SPECIFICATIONS

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
PIN(S): ALE, $\overline{MCS}$ (Chip Select), $\overline{MRE}$ (Read), $\overline{MWE}$ (Write), AD7-0 (Address/Data)						
t_{ALw}	ALE pulse width high	15			ns	
t_{AsALl}	Address setup to ALE low	10			ns	
$t_{AhldALl}$	Address hold after ALE low	5			ns	
t_{AzRDl}	Read low to Address tri-state			15	ns	
t_{RDw}	Read pulse width	110			ns	
t_{RDhALh}	Read high to next ALE high	15			ns	
t_{RDax}	Read (data) access time	18		90	ns	C_L = 30pF to 100pF
t_{DzRDh}	Data tri-state after Read high	5		30	ns	@ V_{OH}-0.5V & V_{OL}+ 0.5V
t_{AvWRl}	Address valid to Write low	25			ns	
t_{WRw}	Write pulse width	70			ns	
t_{WRhALh}	Write high to next ALE high	10			ns	
t_{DsWRh}	Data setup to Write high	50			ns	
$t_{DhldWRh}$	Data hold after Write high	5			ns	
T_{CSlRWl}	Chip Select low to Read/Write low	10			ns	
T_{RWhCSh}	Read/Write high to Chip Select high	5			ns	
t_{LPSRD}	Setup of Low Power Mode Deactivation to Register Reads (i.e. settling time of output driver bias from RSTPDN off)	100			µs	Does not effect register writes
t_{BCS}	$\overline{MCS}$ to $\overline{BCS}$ Propagation Delay			19	ns	
t_{RST}	$\overline{HRESET}$ Minimum Pulse Width Low			20	ns	

TABLE 9-20. MICROPROCESSOR INTERFACE TIMING SPECIFCATIONS

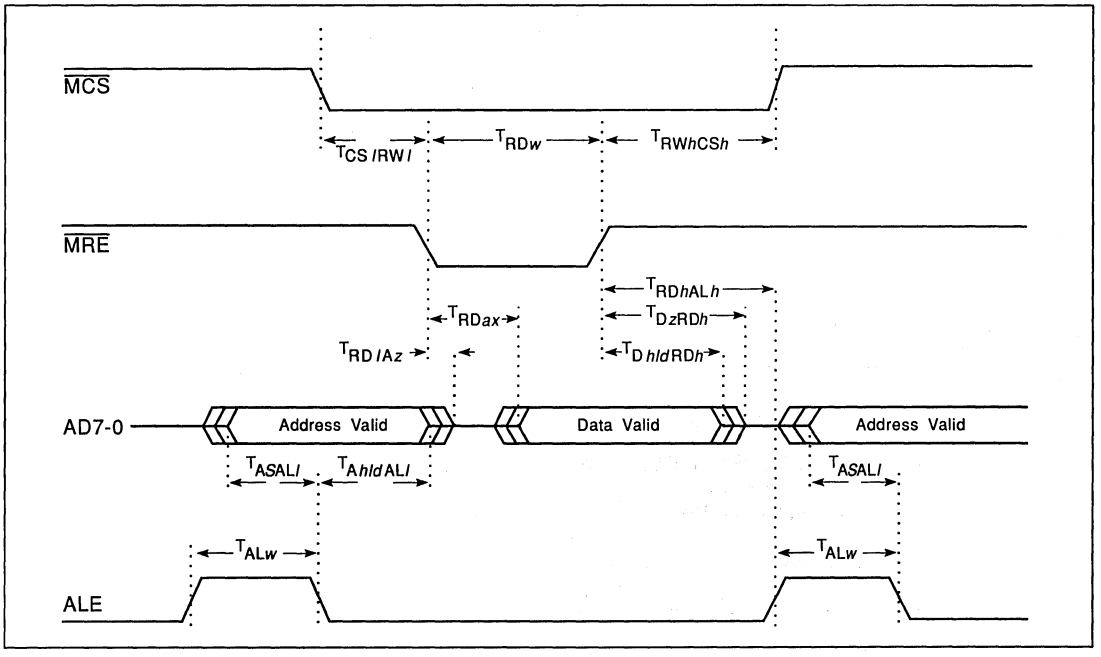


FIGURE 9-6. MICROPROCESSOR READ TIMING DIAGRAM

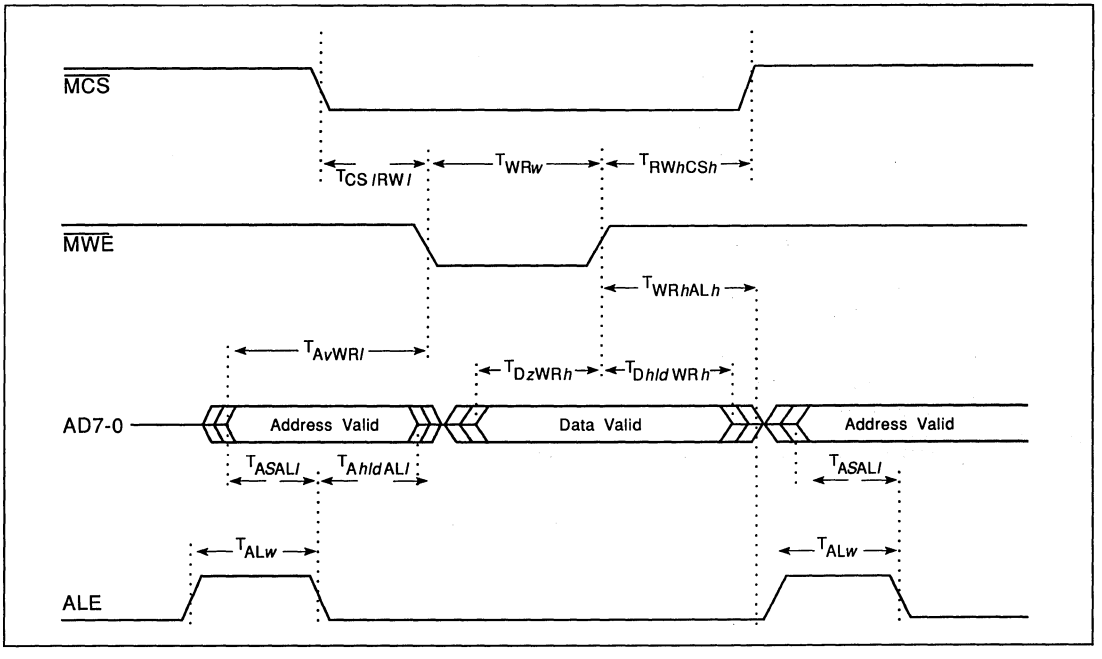


FIGURE 9-7. MICROPROCESSOR WRITE TIMING DIAGRAM

APPENDIX

A.0 APPLICATION NOTES

A.1 FREQUENCY SYNTHESIZER

As discussed in section 3.0, "Frequency Synthesizer", the Frequency Synthesizer utilizes one divider to divide the crystal reference (COD) and one for the VCO (VCOD). This leads to some confusion as to the resolution which can be expected in generating the NRZ data rate.

As can be seen from EQ. 6.0, the output of the Synthesizer is simply a ratio of the crystal input frequency pre-scaled by the HFCOD. That is, for any given crystal frequency, there is a set of ratios which may be generated by programming the value of the VCOD and COD registers. The resulting VCOD/COD ratios will be contained by the input frequency limits to the PLL, and the maximum and minimum data rates allowable (EQ. 3.0 and EQ. 5.0). Disregarding these constraints for the time being, the ratios have certain characteristics which are of interest and which greatly effect the resolution of the system.

Take, for example, the ratios generated by x/y where x and y range from 1 to 10. Let's further bound these ratios by zero and one. If we create an axis on which to plot the ratios, we can begin to see an interesting phenomenon. Starting with the ratio 1/2, place a mark at this point on the axis.We have reduced the distance between the marks at zero and one by a factor or two. If we take the next ratio, 1/3 and 2/3, we further reduce the distance from zero and one to the next nearest mark, down to 1/3. As this process continues, we see that the distance from zero and one to the next nearest mark will be equal to the smallest ratio we generate. In this case it will be 1/10. There is a mark at 9/10 and a mark at 1/10, both of which are 1/10 away from their respective neighboring integer ratios, one and zero. In the mean time, the intervals created between one and zero have been reduced to much less than 1/10. For example, the distance between 1/10 and 1/9 is 1/90. This phenomena repeats at all integer ratios. In fact, it can be show that the resolution similarly degrades around multiples of 1/2, but to a much lesser degree. This process continues, with the resolution around multiples of 1/3 being better an 1/2, but worse than 1/4, etc.

Following this same pattern, the Frequency Synthesizer will have resolutions which are coarser at and around integer ratios of the VCOD/COD, and it can be said that the worst possible resolution will be equal to 1/COD, in the same fashion as the worst resolution in the illustration given above was 1/10. However, in general, the resolution will be much better, as was also illustrated with the example of 1/90 above.

Another way of visualizing the resolution question is as follows. Since the COD serves to divide the crystal input frequency down to the range of 95 to 105 KHz, the VCO can only be generated as a multiple of this (i.e. EQ. 6.0). It is therefore easily seen that the best resolution will occur when the PLL is operated at 95 KHz. However, in order to reach the higher data rates, the PLL will ultimately have to be operated at up to 105 KHz. The actual NRZ output of the synthesizer will therefore have a resolution which is never worse than, and almost always much better than 105kHz times 4/3, or 140 KHz.

The C program on the following page is provided to assist in programming the Synthesizer. The program requires as its input, the desired crystal frequency. The output will be the exhaustive set of all possible data rates along with the necessary COD and VCOD values. Taking the output of this program and sorting based on the first column (NRZ data rate) produces a convenient look up table of data rates for the given crystal frequency.

```
#include <stdio.h, math.h. string.h>
main(argc, argv)
int argc;
char *argv[ ];
{
        float fxtli = 0.0;
        float fxtlicod      = 0.0;
        float fvco          = 0.0;
        float fnrz          = 0.0;
        float cod           = 1.0;
        float vcod          = 1.0;
        char *fxtliptr;
        fxtliptr = argv[1];
        fxtli = (float) atof(fxtliptr);
        printf("fxtli =%02f MHz \n", (fxtli/1e6));
        while (cod <= 256.0)
        {
                fxtlicod = fxtli/cod/1e3;
                if ((fxtlicod <= 105) && (fxtlicod >= 95))
                {
                        while (vcod  <= 256.0)
                        {
                                fnrz = 4.0*fxtlicod*vcod/3e3;
                                if ((fnrz  <= 33.0) && (fnrz >= 7.5))
                                printf("%02f MHz: cod =%02f vcod =
                                        %02f fpll =%02f kHz \n",
                                        fnrz, (cod-1), (vcod-1), fxtlicod);
                                 vcod = vcod + 1.0;
                        }
                        vcod = 1.0;
                }
                cod = cod + 1.0;
        }
}
```

A.2 WINDOW SHIFT SYNTHESIZER

For discussion of the resolution, refer to "A-1 Frequency Synthesizer". The following C program is provided to assist in programming the Synthesizer. The program requires as its input the expected data rate. The output will be the exhaustive set of all possible data rates along with the necessary COD and VCOD values. Taking the output of this program and sorting based on the first column (NRZ data rate) produces a convenient look up table of data rates for the given crystal frequency.

```
#include <stdio.h, math.h, string.h
main(argc, argv)
int argc;
char *argv[];
{
        float delay = 0;
        int wsi = 0;
        float fdr = 0.0;
        float fclk = 0.0;
        float tclk = 0.0;
        float ftclkcod = 0.0;
        float fvco = 0.0;
        float fvcovcod = 0.0;
        float SAM = 1.0;
        float range = 0.0;
        float cod = 1.0;
        float vcod = 1.0;
        float ws = 0.0;
        float wsf = 0.0;
        float delta = 0.0;
        char *fdrptr;
        fdrptr = argv[1];
        fdr = (float) atof(fdrptr);
        ftclk = 1.5*fdr;
        tclk = 1e9/ftclk;
        printf("Data Rate =%02f MHz\n", (fdr/1e6));
        while (cod ≤16.0)
        {
                ftclkcod = (ftclk/cod)/1e6;
                if ((ftclkcod <= 15) && (ftclkcod >= 3))
                {
                        while (vcod <= 32)
                        {
```

```
                                        fvco = ftclkcod*vcod;
                                        delta = (1000.0/fvco)/9.0;
                                        if ((delta <= 6) && (delta >= 2))
                                        {
                                                while (SAM ≤16)
                                                {
                                                        delay = (SAM*delta);
                                                        wsi = (int) (delay/tclk);
                                                        wsf = (float) wsi;
                                                        ws = 100*((((tclk/2) * ((2*wsf) + 1))-delay)/tclk)
                                                        printf("%02f percent (delay =%02f ns):
                                                           cod =%02f vcod =%02f
                                                           SAM =  %02f/n".ws, delay,(cod-1).
                                                           (vcod-1), ( SAM-1)):
                                                SAM=SAM+1.0;
                                                }
                                                SAM=1.0;
                                        }
                                        vcod=vcod+1.0;
                                }
                                vcod=1.0;
                        }
                        cod=cod+1.0;
                }
        }
```