PRELIMINARY W86C451

I/O CONTROLLER FOR IBM PC/AT/XT™ *

GENERAL DESCRIPTION

The W86C451 is an enhanced version of the popular W86C450 asynchronous communication element (ACE) fabricated using WINBOND'S CMOS process. The device surports one serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the UART at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the UART as well as any error conditions (parity, overrun, framing, or break interrupt).

The UART includes a programmable baud rate generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16}-1)$, and producing a 16 × clock for driving the internal transmitter logic. Provisions are also included to use this 16 × clock to drive the receiver logic. The UART includes a complete MODEM-control capability and a processor-interrupt system. Interrupts can be programmed to the user's requirements, minimizing the computing required to handle the communications link.

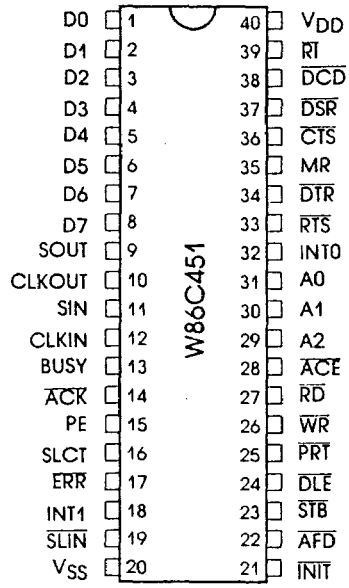
In addition to its communication interface capabilities, the W86C451 provides the user with a parallel Centronics type printer.

FEATURES

- Easily interfaces to most popular microprocessors.
- One-channel version of W86C450
- Centronix printer interface
- Independently controlled transmit, receive, line status, and data set interrupts.
- Programmable baud generator allows division of any input clock by 1 to $(2^{16}-1)$ and generates the internal 16 × clock.
- Uses system's 14.31818MHz clock input.
- MODEM control functions (CTS, RTS, DSR, DTR, RI, and DCD).
- Fully programmable serial-interface characteristics:
  - -5, 6, 7, or 8-bit characters
  - -Even, odd, or no-parity bit generation and detection.
  - -1, 1.5 or 2-stop bit generation.
- •False start bit detection.
- •Internal diagnostic capabilities:
  - -Loopback controls for communications link fault isolation
  - -Break, parity, overrun, framing error simulation.
- •Fully prioritized interrupt system controls.

PIN CONFIGURATION

TOP VIEW



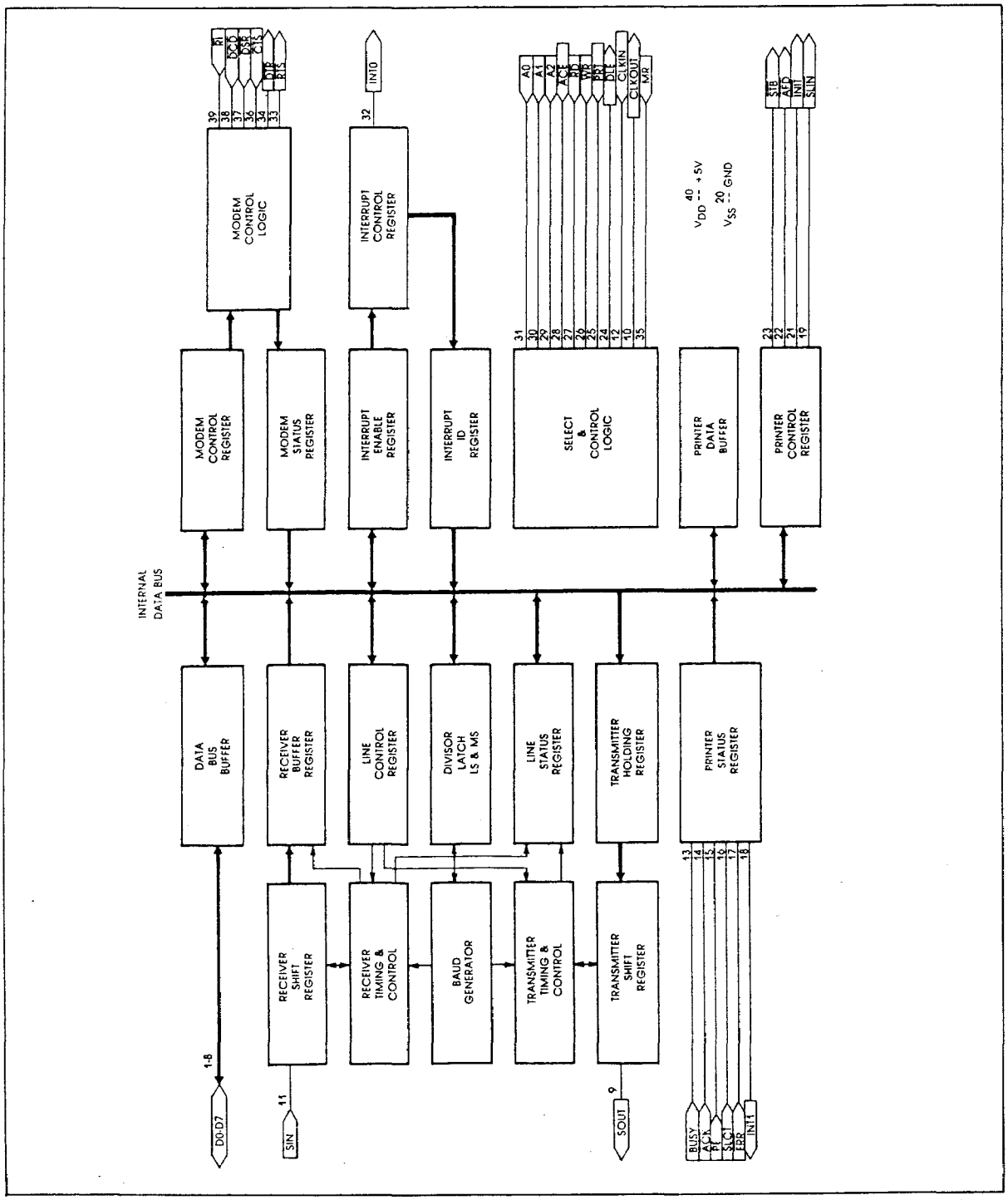
PIN DESCRIPTION

SYMBOL	TYPE	PIN NO.	NAME AND FUNCTION
$\overline{RD}$	I	27	I/O Read is an active LOW input signal used to instruct the W86C451 to drive its data onto the data bus.
$\overline{WR}$	I	26	I/O Write is an active LOW input signal used to instruct the W86C451 to read the data on the data bus.
A2-A0	I	29-31	Address Lines are input signals used to address the registers to be loaded or read.
$\overline{RI}$	I	39	Ring Indicator: When LOW, indicates that a ringing signal is being received by the MODEM or data set.
$\overline{DCD}$	I	38	Data Carrier Detect: When LOW, indicates the MODEM or data set detected a data carrier.
$\overline{CTS}$	I	36	Clear To Send is a MODEM control function input whose functions can be tested by the CPU by reading bit 4 of the MODEM Status register.
$\overline{DTR}$	O	34	Data Terminal Ready: When LOW, informs the MODEM or data set that the controller is ready to communicate.

SYMBOL	TYPE	PIN NO.	NAME AND FUNCTION
$\overline{RTS}$	O	33	Request To Send: When LOW, informs the MODEM or data set that the controller is ready to send data.
INT0	O	32	Interrupt: It goes HIGH whenever any one of the following interrupt types has an active HIGH condition and is enabled via the IER: receiver error flag, receiver data available, Transmitter Holding register empty, and MODEM status. The signal is high-impedence upon a Reset operation.
SOUT	O	9	Serial Output is used to transmit serial data out to the communication link. The output signal is set to a marking condition upon a Reset.
SIN	I	11	Serial Input is used to receive serial data from the communication link.
CLKIN	I	12	Connects to system's 14.31818MHz clock.
CLKOUT	O	10	Clock Output: 1.8432MHz output.
MR	I	35	Reset: When HIGH, clears the registers to states as indicated in Table 1.
$\overline{ERR}$	I	17	Error: When LOW, means the printer has encountered an error condition. $\overline{ERR}$ is separately used for Printer Interface.
SLCT	I	16	Select: When High, means the printer is selected. SLCT is separately used for Printer Interface.
PE	I	15	End of Paper: When HIGH, means the printer has detected the end of paper PE is separately used for Printer Interface.
$\overline{ACK}$	I	14	Acknowledge: When LOW, means the printer has received the character and is ready to accept another. $\overline{ACK}$ is separately used for Printer Interface.
BUSY	I	13	Busy: When HIGH, the printer is busy can not accept data. BUSY is separately used for Printer Interface.
INT1	O	18	Interrupt: This pin has tristate outputs. Control Latch is in active condition and the ACK, input changes from LOW to HIGH, the interrupt goes active. PRTINT is separately used for Printer Interface.
$\overline{DLE}$	O	24	Enable of Data Latch is an active LOW output signal used for latch the external data latch which is transmitting the data to Printer.
$\overline{SLIN}$	O	19	Select Input: A LOW in this pin is used to select the printer. $\overline{SLIN}$ is separately used for Printer Interface.
$\overline{INIT}$	O	21	Initialization: A LOW in this pin is used to start the printer. $\overline{INIT}$ is separately used for Printer Interface.

SYMBOL	TYPE	PIN NO.	NAME AND FUNCTION
$\overline{AFD}$	O	22	AUTO FD XT: A LOW in this pin causes the printer to line-feed after a line is printed. $\overline{AFD}$ is Separately used for Printer Interface.
$\overline{STB}$	O	23	Strobe: A 0.5 microsecond minimum, LOW active pulse clocks data into the printer. $\overline{STB}$ is separately used for Printer Interface.
D7~D0	I/O	1-8	Data Bus: This bus comprises eight tri-state I/O lines. The bus provides bidirectional communications between the W86C451 and the CPU. Data, control word, and status information are transferred via the D7~D0 data bus.
$\overline{ACE}$ $\overline{PRT}$	I	28 25	$\overline{ACE}$ selectes RS232 port. $\overline{PRT}$ selectes printer port.
$\overline{DSR}$	I	37	Data Set Ready: When LOW, indicates the MODEM or data set is ready to establish the communications link and transfer data with the W86C451.
V_{DD}	I	40	System Power: 5 Volts power supply.
V_{SS}	I	20	System Ground: 0 Volts.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

A. ADDRESS DECODER

Table 1. Register Addresses

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read). Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

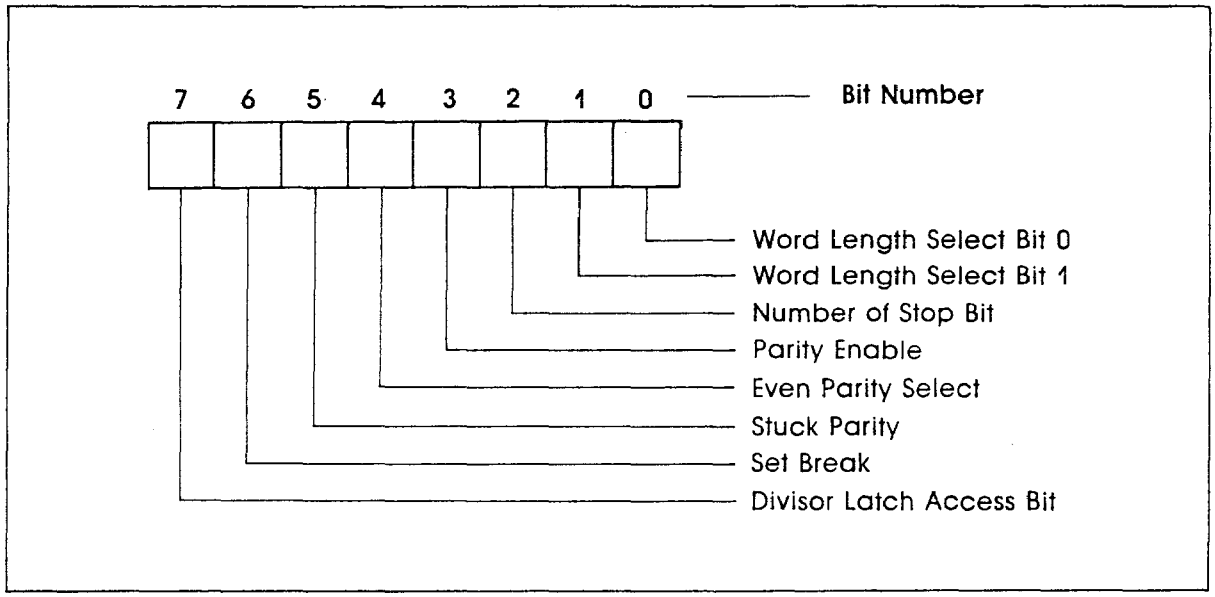
A0	A1	$\overline{IOR}$	$\overline{IOW}$	OPERATION
0	0	1	0	$\overline{DLE}$ Pin (for External Data Latch)
0	0	0	1	Data Swapper
1	0	0	1	Printer Status Buffer
0	1	1	0	Printer Control Latch
0	1	0	1	Printer Control Swapper

B. ASYNCHRONOUS COMMUNICATIONS ELEMENTS

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and half (five bit format only) or two stop bits. The ACE includes a programmable baud generator that is capable of driving the timing reference clock input by divisors of 1 to $(2^{16}-1)$, and producting a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE is a complete MODEM control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

a. Line Control Register

The system programmer specifies the format of the asynchronous data communications exchange through the Line Control register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control register for inspection.



Bits 0, 1: These two bits specify the number of bits in each serial character that is sent or received. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length (Bits)
0	0	5
0	1	6
1	0	7
1	1	8

Bit 2: This bit specifies the number of stop bits in each serial character that is sent or received. If bit 2 is a logic 0, one stop bit is generated or checked in the data sent or received. If bit 2 is logic 1 when a 5-bit word length is selected through bits 0 and 1, one and a half stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 stop bits are generated or checked.

Bit 3: This bit is the parity-enable bit. When bit 3 is logic 1, a parity bit is generated (transmit data) or check (receive data) between the last data word and stop bit of the serial data. (The parity bit is used to product an even or odd number of 1's when the data-word bits and parity bit are summed).

Bit 4: This bit is the even-parity-select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logical 1's is sent or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is sent or checked.

Bit 5: This bit is the stuck-parity bit. When bit 3 is a logical 1 and bit 5 is a logical 1, the parity bit is sent and then detected by the receiver as a logical 0, if bit 4 is a logical, 1 or as a logical 1 if bit 4 is a logical 0.

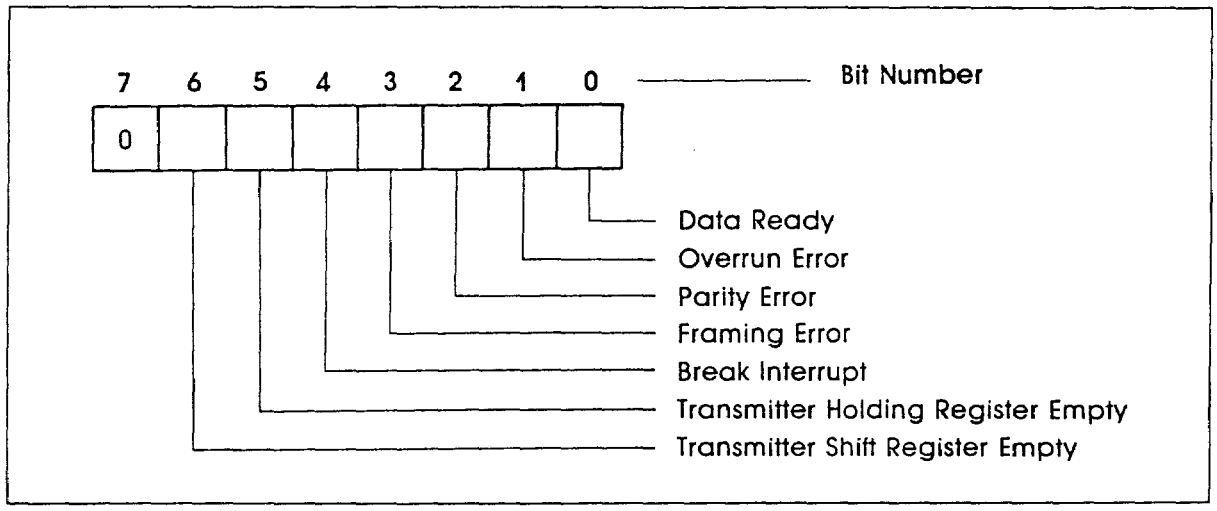
Bit 6: This bit is the set-break control bit. When bit 6 is set to a logical 1, the serial output

(SOUT) is forced to the spacing (logical 0) state. The break is disabled by setting bit 6 to a logical 0.

Bit 7: This bit is the divisor-latch access bit (DLAB). It must be set to high (logical 1) to gain access to the divisor latches of Baud Generator during a read or write operation. It must be set to low (logical 0) to gain access to the Receiver Buffer, the Transmitter Holding register, or the Interrupt Enable register.

b. Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status register are described below.



Bit 0: This bit is the receiver data ready (DR) indicator. It is set to logical 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer register. Bit 0 may be reset to logical 0 by the processor either reading the data in the Receiver Buffer register or writing logical 0 in it.

Bit 1: This bit is the overrun error (OE) indicator. It indicates that data in the Receiver Buffer register was not read by the processor before the next character was transferred into the register, thereby destroying the previous character. The OE indicator is reset whenever the processor reads the contents of the Line Status register.

Bit 2: This is the parity error (PE) indicator and indicates the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to logical 1 upon detection of a parity error, and is reset to logical 0 whenever the transmission time (that is, the total Time of start bit + data bits + parity stop bits). This BI indicator is reset whenever the CPU reads the contents of Line Status register.

Note: Bits 1 through 4 are error conditions that product a receiver line-status interrupt whenever any of the corresponding conditions are detected.

Bit 3: This bit is the framing error (FE) indicator. It indicates the received character did not have a valid stop bit. Bit 3 is set to logical 1 whenever the stop bit following the last data bit or parity bit is detected as a zero bit (spacing level). The FE indicator is reset whenever the CPU read the contents of the Line Status register.

Bit 4: This bit is the break interrupt (BI) indicator. It is set to logical 1 whenever the received data input is held in the spacing state (logical 0) for longer than a fullword of the Line Status register.

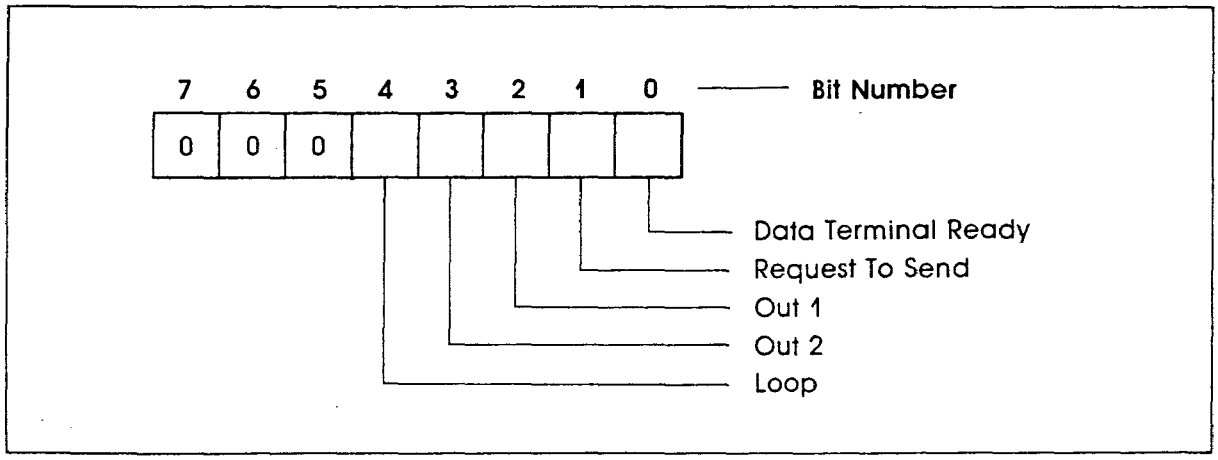
Bit 5: This bit is the Transmitter Holding register empty (THRE) indicator. It indicates the controller is ready to accept. It indicates the controller is ready to accept a new character for transmission. In addition, this bit causes the controller to issue an interrupt to the processor when the THRE interrupt enable is set active. The THRE bit is set to logical 1 when a character is transferred from the Transmitter Holding register into the Transmitter Shift register. It is reset to logical 0 when the processor loads the Transmitter Holding register PE bit is set to logical 1 upon detection of a parity error, and is reset to logical 0 whenever the processor reads the contents processor reads the contents of the Line Status register.

Bit 6: This bit is the transmitter empty (TEME) indicator. It is set to logical 1 whenever the transmitter Holding register (THR) and the Transmitter Shift register (TSR) are both empty. It is reset to logical 0 whenever THR or TSR contains a data character.

Bit 7: This bit is permanently set to logical 0.

c. Modem Control Register (MCR)

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM)



Bit 0: This bit controls the $\overline{DTR}$ output. When bit 0 is set to logical, 1 the $\overline{DTR}$ output is forced active. When bit 0 is reset to logical 0, the $\overline{DTR}$ output is forced inactive.

Bit 1: This bit controls the $\overline{RTS}$ output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit is only used in the diagnostic mode.

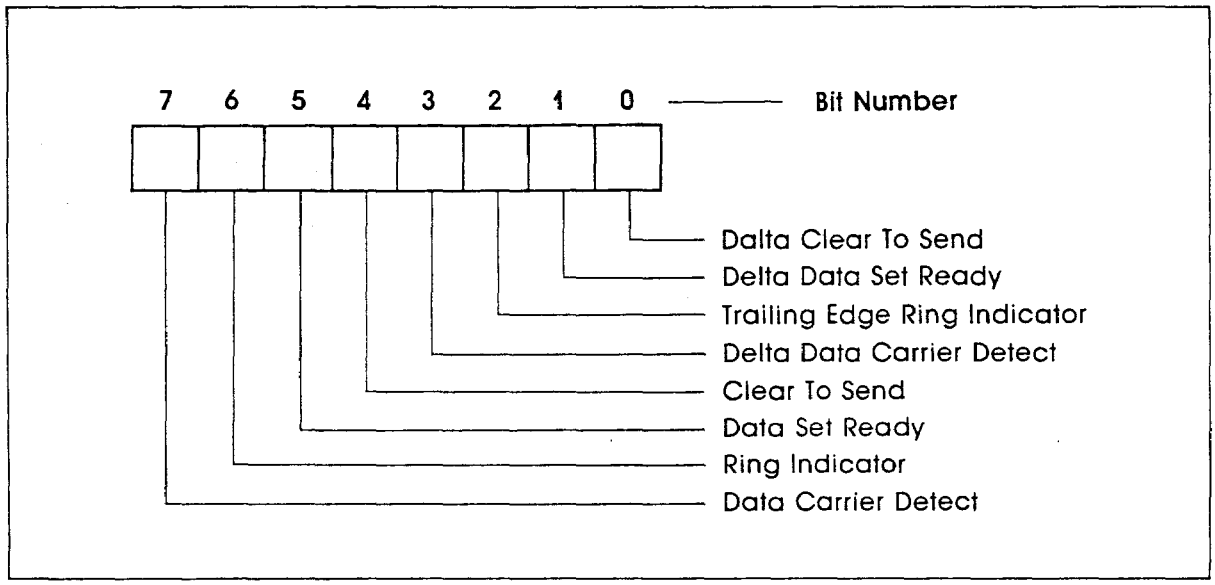
Bit 3: The enable of the interrupt output can be set to an active state by programming this bit to a high level.

Bit 4: This bit provides a loopback feature for diagnostic testing of the controller. When bit 4 is set to logical 1, the following occur: the SOUT is set to the marking (logical 1) state; the SIN is disconnected; the output of the Transmitter Shift register is "loop back" into the Receiver Shift register input; the four MODEM control inputs ($\overline{CTS}$, $\overline{CSR}$, $\overline{DCD}$, and $\overline{RI}$) are disconnected; and the four MODEM control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$, and $\overline{OUT2}$) are internally connected to the four MODEM control inputs, and the MODEM control output pins are forced to their inactive state (high). In the diagnostic mode, data sent is immediately received. This feature allows the processor to verify the transmit-data and receive-data path of the controller.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational as are the MODEM control interrupts. But the interrupts' sources are now the lower four bits of the MODEM control register (MCR) instead of the four MODEM control inputs. The interrupts are still controlled by the Interrupt Enable Register. The controller's interrupt system can be tested by writing to the lower six bits of the Line Status register, and the lower four bits of the MODEM Status register. Setting any of these bits to logical 1 generates the appropriate interrupt (if enabled). Resetting these interrupts is the same as for normal controller operation. To return to normal operation, the registers must be reprogrammed for normal operation, and then bit 4 of the MCR must be reset to logical 0.

d. Modem Status Register (MSR)

The 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the processor. In addition, four bits of the MSR provide change information. These four bits are set to logical 1 whenever a control input from the MODEM changes state. They are reset to logical 0 whenever the processor reads this register.



Bit 0: This bit is the delta clear-to-send indicator. It indicates the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the processor.

Bit 1: This bit is the delta data-set-ready indicator. It indicates the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the processors.

Bit 2: This bit is the trailing-edge ring-indicator detector. It indicates the $\overline{RI}$ input to the chip has changed from an active condition to an inactive condition.

Bit 3: This bit is the delta data-carrier-detect indicator. It indicates the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2 or 3 is set to logical 1, a MODEM status interrupt is generated.

Bit 4: This bit is the opposite of the $\overline{CTS}$ input. If bit 4 of the MCR loop is set to a logical 1, this bit is equivalent to RTS of the MCR.

Bit 5: This bit is the opposite of the $\overline{DSR}$ input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to DTR of the MCR.

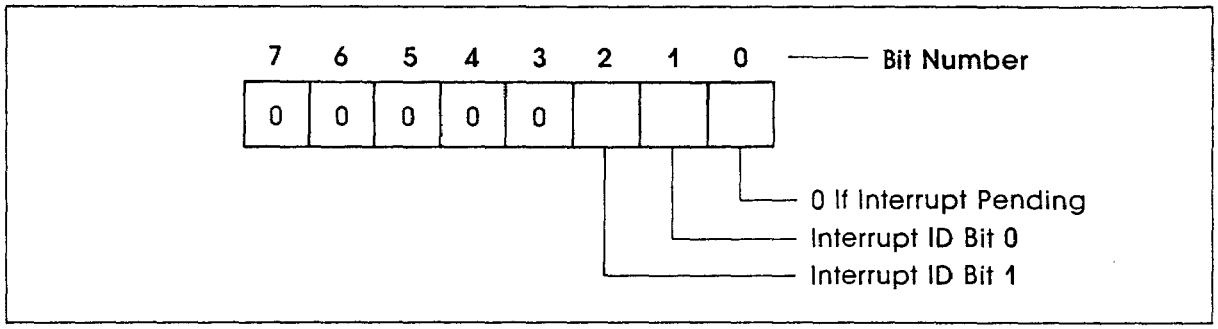
Bit 6: This bit is the opposite of the $\overline{RI}$ input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT1 of the MCR.

Bit 7: This bit is the opposite of the $\overline{DCD}$ input. If bit 4 of the MCR is set to a logical 1, this bit is equivalent to OUT2 of the MCR.

e. Interrupt Identification Register

The controller has an on-chip interrupt capability that makes communications possible with all of the currently popular microprocessors. In order to provide minimum software overhead during data

character transfers, the controller prioritizes interrupts into four levels: receiver line status (priority 1), received data ready (priority 2), Transmitter Holding register empty (priority 3), and MODEM status (priority 4).
Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). The IIR, when addressed during chip-select time, stops the pending interrupt with the highest priority, and no other interrupts are acknowledged until the processor services that particular interrupt.



Bit 0: The bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is logical 0, an interrupt is pending, and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is logical 1, no interrupt is pending, and polling (if used) continues.

Bit 1-2: These two bits identify the pending interrupt that has the highest priority interrupt pending, as shown in the following Table 2.

Bit 3-7: These five bits are always logical 0.

Table 2.

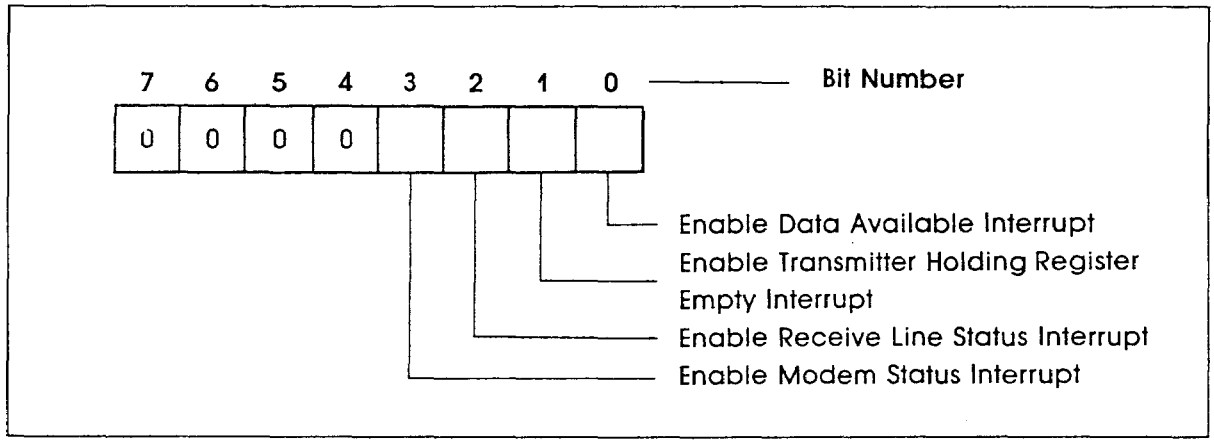
INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	–	None	None	–
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register

(Continued)

INTERRUPT IDENTIFICATION REGISTER				INTERRUPT SET AND RESET FUNCTIONS		
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

f. Interrupt Enable Register (IER)

This 8-bit register allows the four types of controller interrupts to separately activate the interrupt output signal. The interrupt system can be totally disabled by resetting bits 0 through 3 of the Interrupt Enable Register (IER). Similarly, by setting the appropriate bits of this register to a logical 1, selected interrupts can be enabled.



Bit 0: When set to logical 1, enables the received-data-available interrupt.

Bit 1: When set to logical 1, enables the transmitter-holding-register-empty interrupt.

Bit 2: When set to logical 1, enables the receiver-line-status interrupt.

Bit 3: When set to logical 1, enables the modem-status interrupt.

Bit 4-7: These four bits are always logical 0.

g. Programmable Baud Generator

The controller contains a programmable Baud Generator that is capable of taking any clock input (DC to 14.31818MHz) and dividing it by any divisor from 1 to $(2^{16}-1)$. The output frequency of the Baud Generator is the baud rate multiplied by 16. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded

during initialization in order to ensure desired operation of the Baud Generator. When either of the Divisor Latches is loaded, a 16-bit counter is immediately loaded. Table 3 illustrates the use of the Baud generator with crystal frequencies of 1.8432MHz. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

Table 3. **Baud Rates Using 14.31818MHz Input to generate 1.8432MHz**

DESIRED BAUD RATE	DECIMAL DIVISOR USED TO GENERATE 16 × CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
	1.8432M	1.8432M
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

C. PRINTER INTERFACE LOGIC

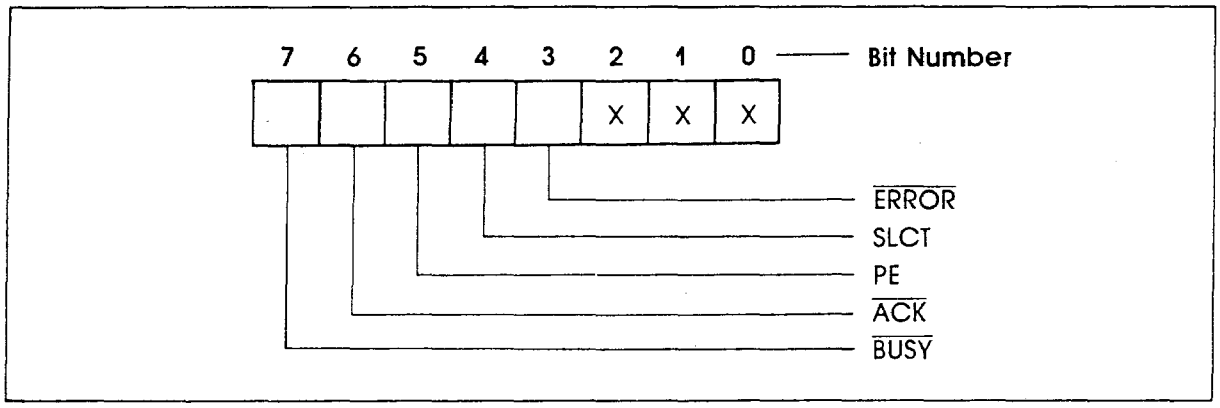
The parallel portion of the W86C451 makes possible the attachment of various devices that accept eight bits of parallel data at standard TTL levels. The following discusses the use of the parallel portion to connect a parallel printer.

a. Data Swapper

The system microprocessor can get the contents of the printer's Data Latch through the Data Swapper by reading its address.

b. Printer Status Buffer

The system microprocessor can get the printer status by reading the address of the Printer Status Buffer. The following are bit definitions for these bytes.



Bit 7: $\overline{\text{BUSY}}$—This signal may become active during data entry, while the printer is offline, during printing, when the print head is changing positions, or while in an error state. When it is active, the printer is busy and can not accept data.

Bit 6: $\overline{\text{ACK}}$—This bit represents the current, state of the printer's $\overline{\text{ACK}}$ signal. A "0" means the printer has received the character and is ready to accept another. Normally, this signal will be active for approximately 5 microseconds before $\overline{\text{BUSY}}$ stops.

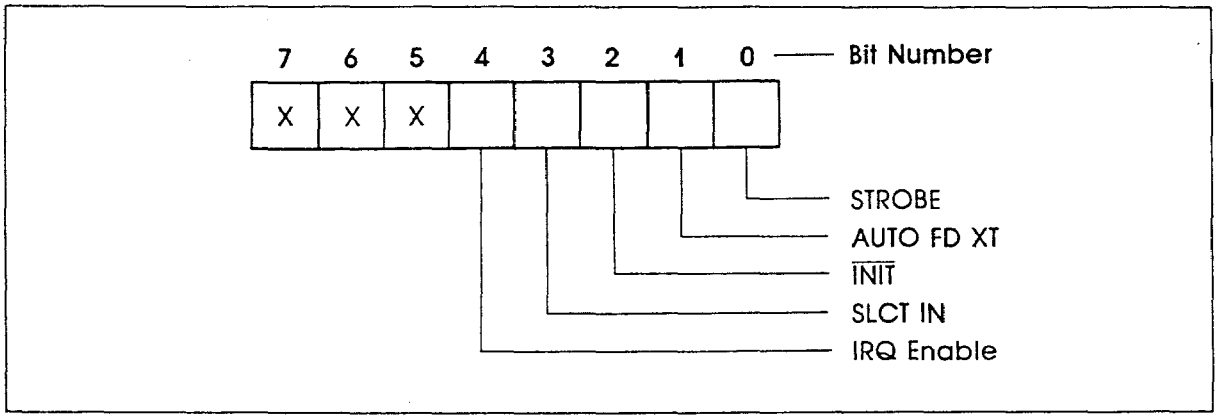
Bit 5: PE—A "1" means the printer has detected the end of paper.

Bit 4: SLCT—A "1" means the printer is selected.

Bit 3: $\overline{\text{ERROR}}$—A "0" means the printer has encountered an error conditions.

c. Printer Control Latch & Printer Control Swapper

Writing to the address of the Printer Control Latch causes Printer control signals to be stored in it. The system microprocessor can get the contents of the Printer Control Latch through the Printer Control Swapper by reading its address. The following are bit definitions for this byte.



Bit 4: IRQ Enable—A "1" in this position allows an interrupt to occur when $\overline{ACK}$ changes from low state to high state.

Bit 3: SLCT IN—A "1" in this bit position selects the Printer.

Bit 2: $\overline{INIT}$—A "0" starts the printer (50 microsecond pulse, minimum).

Bit 1: AUTO FD XT—A "1" causes the printer to line-feed after a line is printed.

Bit 0: STROBE—A 0.5microsecond minimum, high, active pulse clocks data into the printer. Valid data must be present for a minimum of 0.5 microsecond before and after the strobe pulse.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYM.	RATING	UNIT
Supply Voltage	V_{DD} - V_{SS}	−0.3 ~ 7	V
Input Voltage	V_I	V_{SS} − 0.3 ~ V_{DD} + 0.3	V
Operating Temp.	T_{OPR}	0 ~ 70	°C
Storage Temp.	T_{STG}	−65 ~ 150	°C

D.C. CHARACTERISTICS

(T_A = 0°C ~ 70°C, V_{DD} = 5.0V ±5%, V_{SS} = 0V)

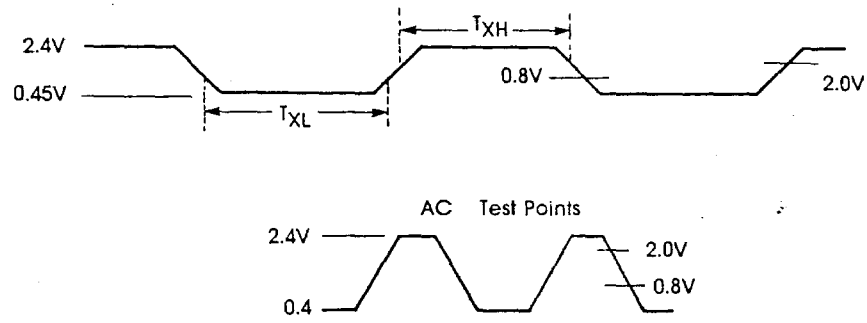
PARAMETER	SYM.	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{ILX}	Clock Input	−0.3	—	0.8	V
	V_{IHX}		2.4	—	V_{DD} + 0.3	V
Input Voltage	V_{IL}	other inputs	−0.3	—	0.8	V
	V_{IH}		2.0	—	V_{DD}	V
Output Voltage	V_{OL}	I_{OL} = 1.6mA on all output	—	—	0.45	V
	V_{OH}	I_{OH} = −1.0mA on all output	2.4	—	—	V
Average Power Supply Current (V_{DD})	I_{CCA}	V_{DD} = 5.25V, T_A = 25°C No load on output SIN, DSR, DCD, CTS, RI = 2.4V All other inputs = 0.4V	—	—	30	mA
Input Leakage	I_{IL}	V_{DD} = 5.25V, V_{SS} = 0V All other pins floating. V_I = 0V, 5.25V	—	—	±10	μA
Clock Leakage	I_{CL}		—	—	±10	μA
Stand by Current	I_{CCB}	V_I = V_{DD} or 0V, Output open	—	—	20	μA

A.C. CHARACTERISTICS

PARAMETER	SYM.	CONDITIONS	MIN.	MAX.	UNIT
Clock High Time	T_{XH}	External Clock	110		nS
Clock Low Time	T_{XL}		110		nS
Address & Chip Select Setup Time	T_{ACS}		60		nS
Address & Chip Select Hold Time	T_{ACH}		40		nS
$\overline{IOW}$ pulse width	T_{WW}		100		nS
Data Setup Time	T_{DS}		40		nS
Data Hold Time	T_{DH}		40		nS
RESET Pulse Width	T_{RPW}		5		mS
Delay From Stop To Set Interrupt	T_{SINT}		9/16	9/16	Baud Rate
Delay From $\overline{IOR}$ To Reset Interrupt	T_{RINT}	100pF Loading		1	μS
Delay From Initial IRQ Reset To Transmit Start	T_{IRS}		1/16	8/16	Baud Rate
Delay From $\overline{IOW}$ To Reset Interrupt	T_{HR}	100pF Loading		175	nS
Delay From Initial $\overline{IOW}$ To Interrupt	T_{SI}		9/16	16/16	Baud Rate
Delay From Stop To Interrupt	T_{STI}		1/2	1/2	Baud Rate
Delay From $\overline{IOR}$ To Reset Interrupt	T_{IR}	100pF Loading		250	nS
Delay From $\overline{IOW}$ To Output	T_{MWO}	100pF Loading		200	nS
Set Interrupt Delay From MODEM Input	T_{SIM}	100pF Loading		250	nS
Reset Interrupt Delay From $\overline{IOR}$	T_{RIM}	100pF Loading		250	nS
Interrupt Active Delay	T_{IAD}			25	nS
Interrupt Inactive Delay	T_{IID}			30	nS
Baud Divisor	N		1	$2^{16}-1$	
$\overline{DLE}$ Active Delay From $\overline{IOW}$ Active	T_{DLA}			20	nS
$\overline{DLE}$ Inactive Delay From $\overline{IOW}$ Inactive	T_{DLI}			20	nS
Address & Chip Select Setup Time From $\overline{IOR}$	T_{ACSR}		60		nS
Address & Chip Select Hold Time From $\overline{IOR}$	T_{ACHR}		20		nS
$\overline{IOR}$ pulse width	T_{RW}		125	10^6	nS
Data Delay From $\overline{IOR}$ Active	T_{DR}	100pF Loading	0	100	nS
Data Floating Delay From IOR Inactive	T_{DF}	100pF Loading		125	nS

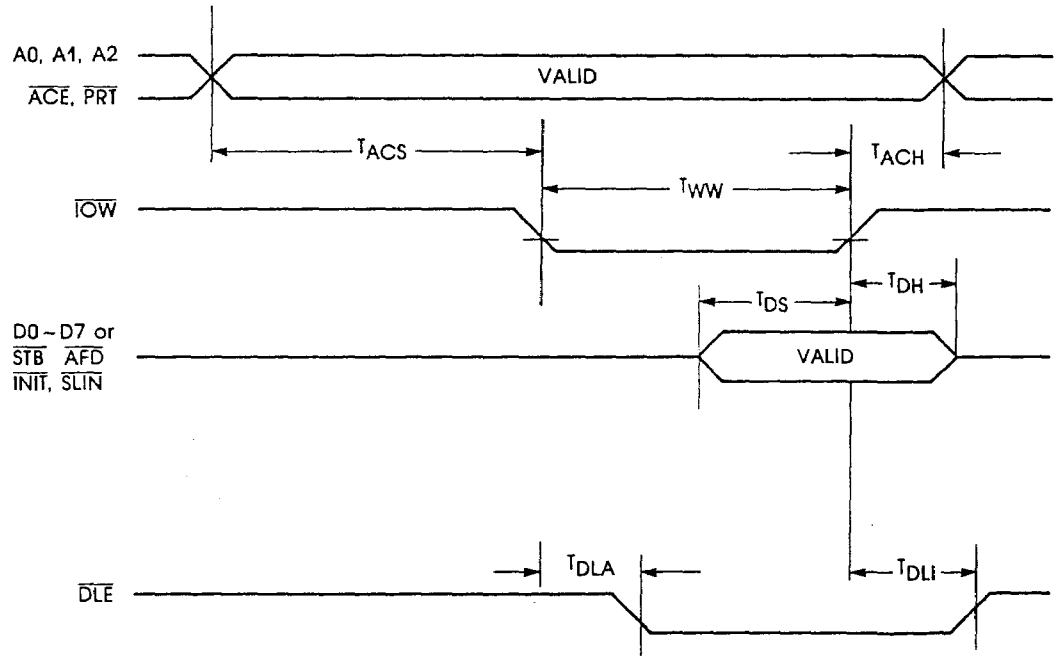
TIMING WAVEFORM

A. EXTERNAL CLOCK INPUT

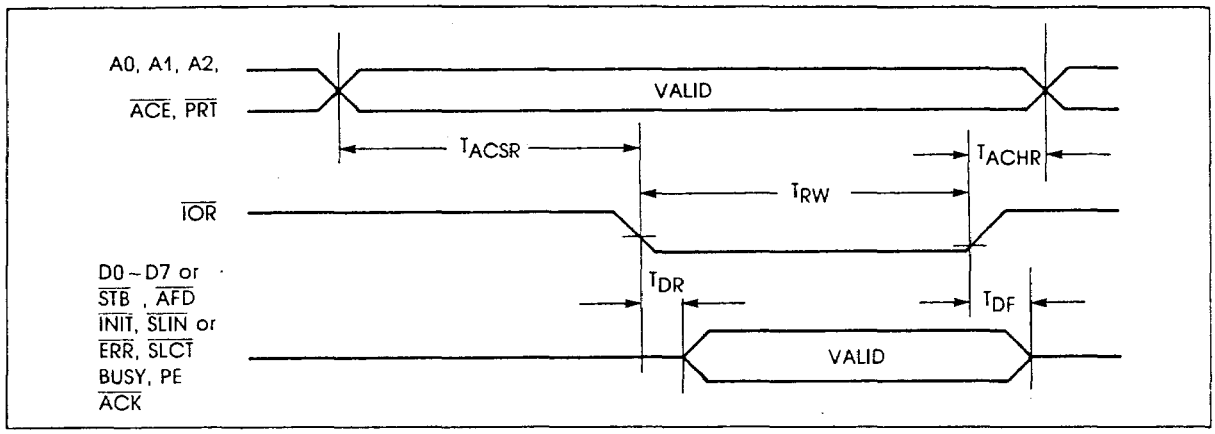


A.C. Testing: Input are drived at 2.4V for logic "1", and 0.45V for a logic "0". Timing measurements are made at 2.0V for logic "1", and 0.8V for a logic "0".

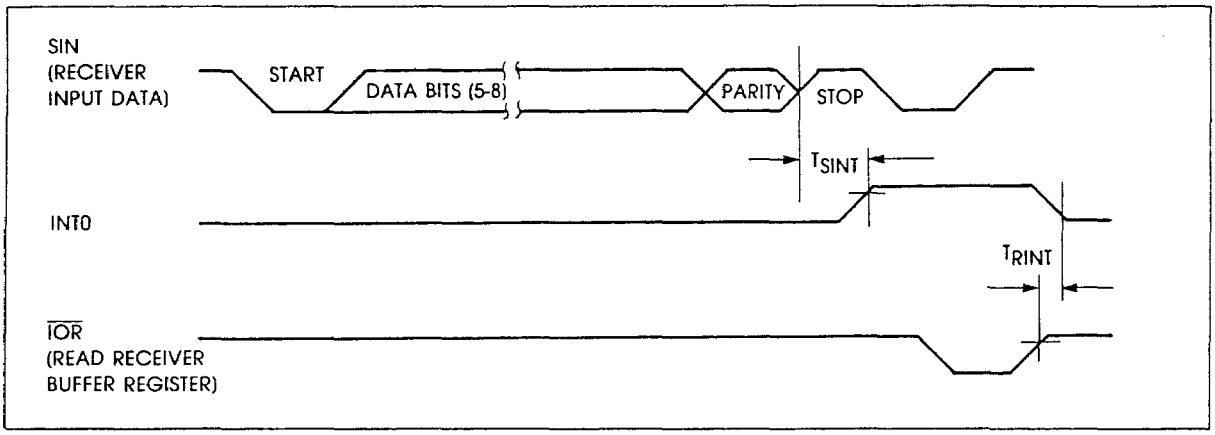
B. WRITE CYCLE



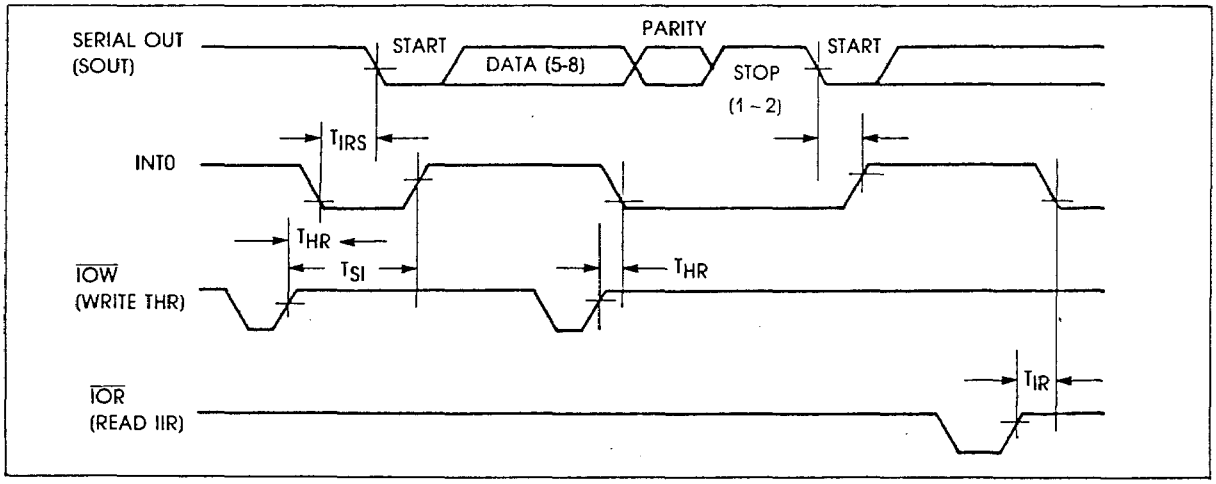
C. READ CYCLE



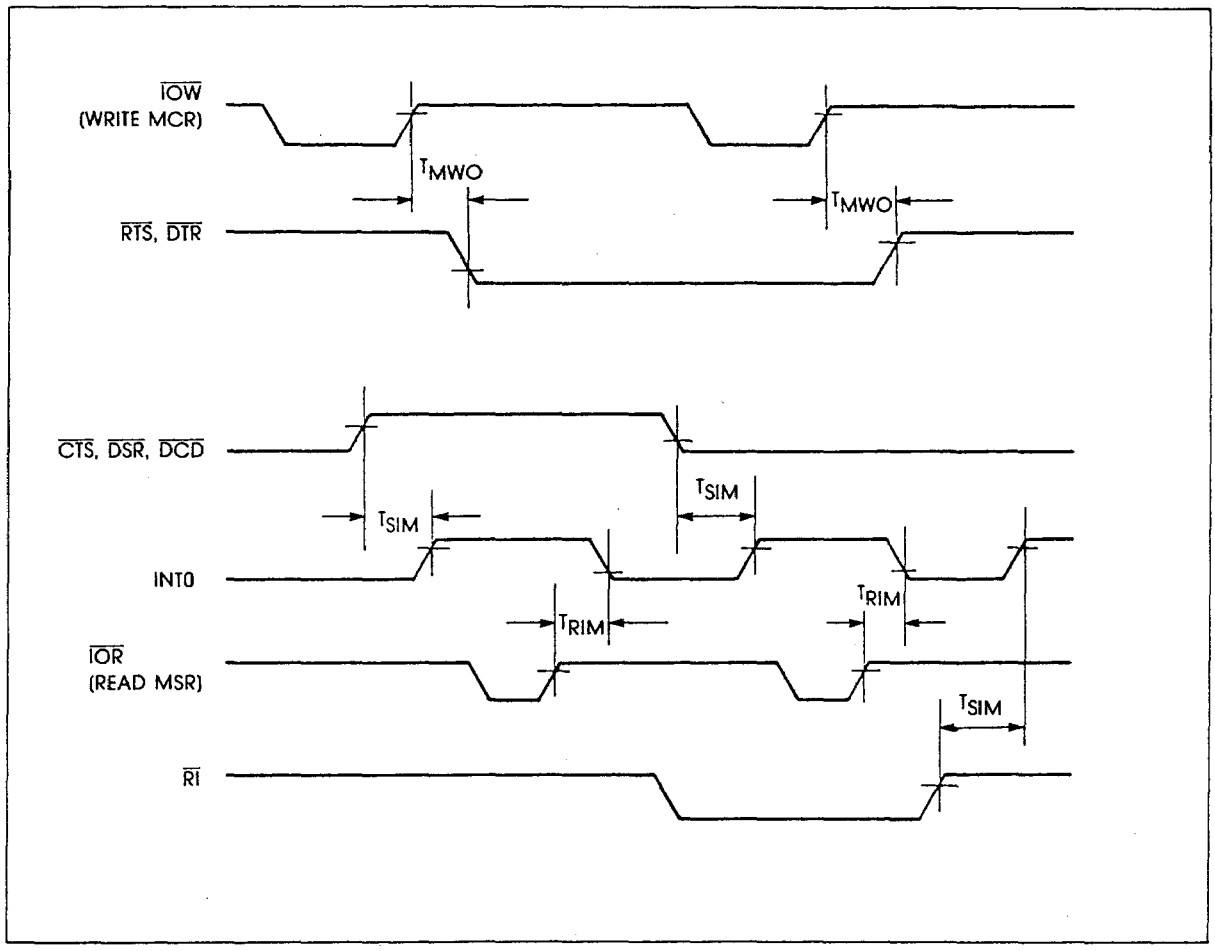
D. RECEIVER TIMING



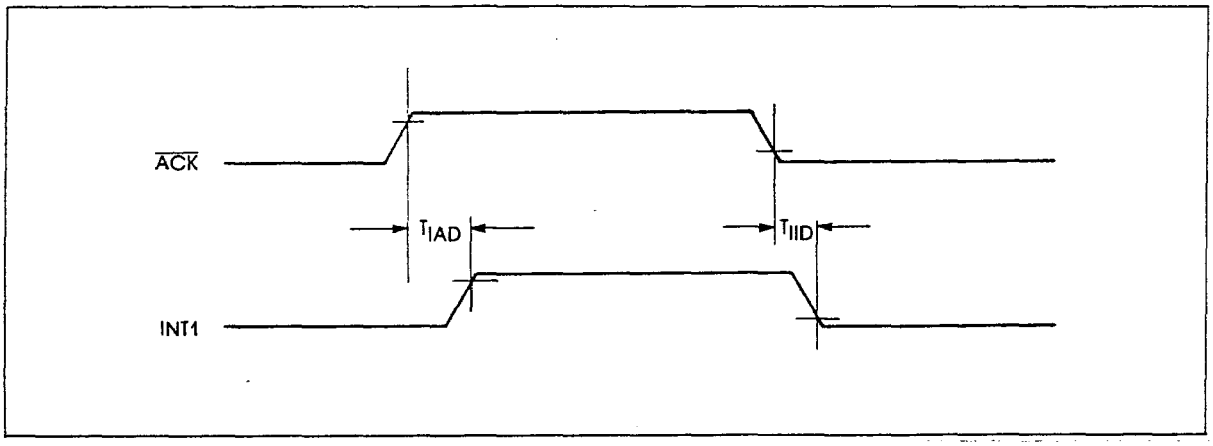
E. TRANSMITTER TIMING



F. MODEM CONTROLS TIMING

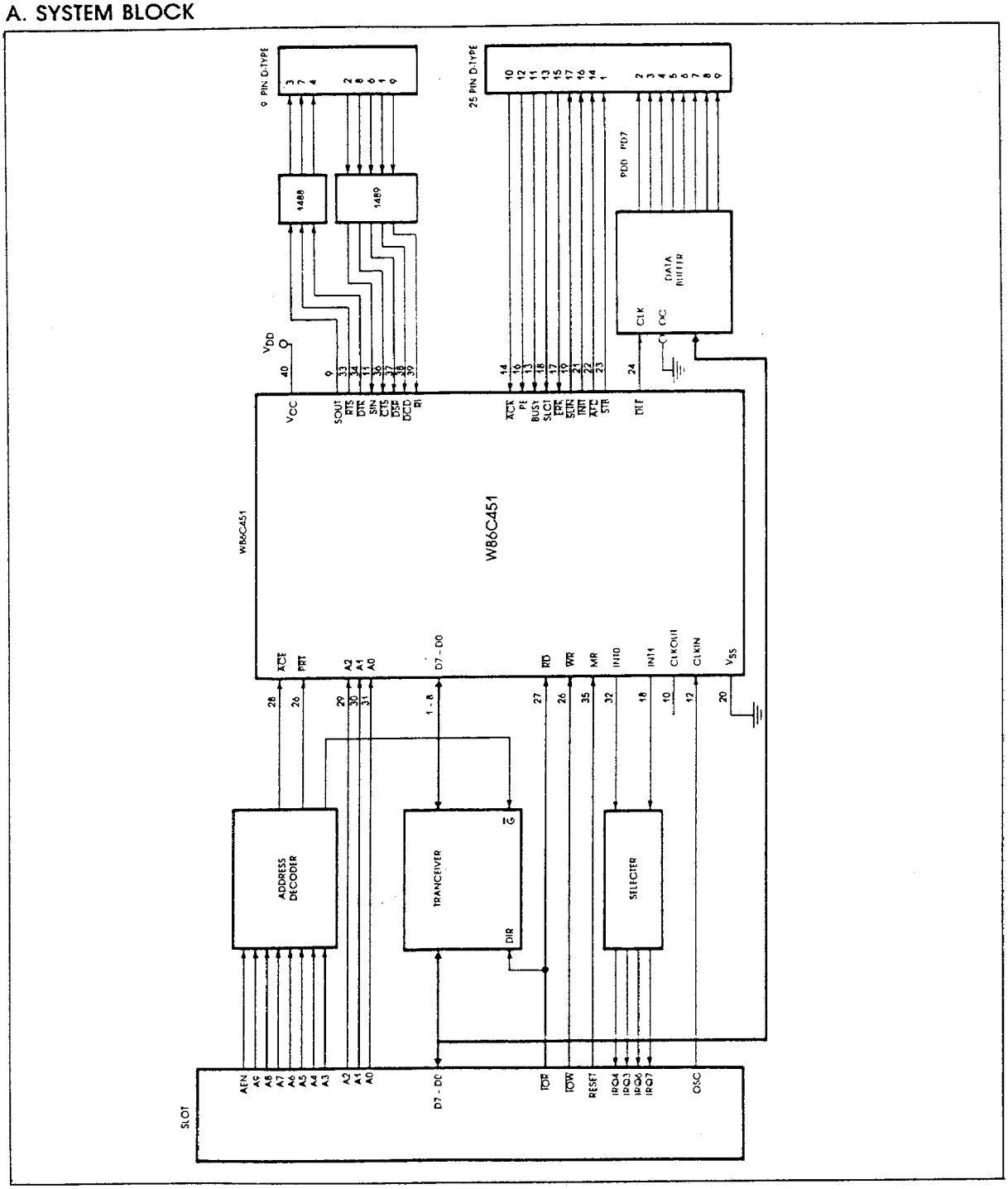


G. PRINTER INTERRUPT TIMING

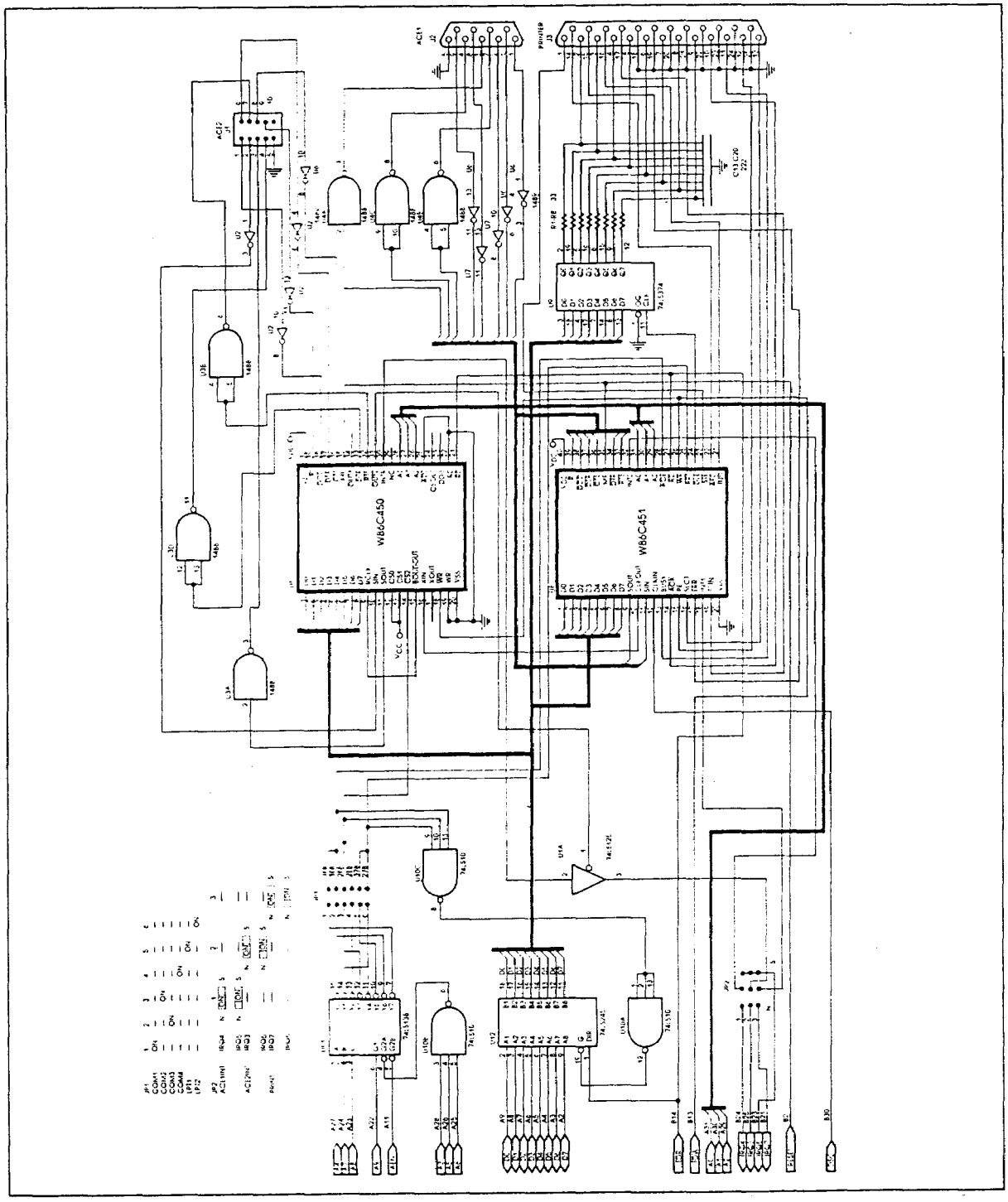


TYPICAL APPLICATION

A. SYSTEM BLOCK



CIRCUIT



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