Xicor®

DATA BOOK Supplement

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Please use this Xicor Data Book Supplement in conjunction with the Xicor 1988 Data Book, Stock No. 100-080, which contains additional product line information, product reliability reports and application notes.

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Xicor, Inc.
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First Edition
First Printing
Printed in U.S.A.

Precautions for the Handling of MOS Devices

Xicor products are designed with effective input protection to prevent damage to the devices under most conditions. However, any MOS circuit can be catastrophically damaged by excessive electrostatic discharge or transient voltages. The following procedures are recommended to avoid accidental circuit damage.

I. Testing MOS Circuits:

1. All units should be handled directly from the conductive or antistatic plastic tube in which they were shipped if possible. This action minimizes touching of individual leads.
2. If units are to be tested without using the tube carrier, the following precautions should be taken:
   a. Table surfaces which potentially will come in contact with the devices either directly or indirectly (such as through shipping tubes) must be metal or of another conductive material and should be electrically connected to the test equipment and to the test operator (a grounding bracelet is recommended).
   b. The units should be transported in bundled antistatic tubes or metal trays, both of which will assume a common potential when placed on a conductive table top.
   c. Do not band tubes together with adhesive tape or rubber bands without first wrapping them in a conductive layer.

II. Test Equipment (Including Environmental Equipment):

1. All equipment must be properly returned to the same reference potential (ground) as the devices, the operator, and the container for the devices.
2. Devices to be tested should be protected from high voltage surges developed by:
   a. Turning electrical equipment on or off.
   b. Relay switching.
   c. Transients from voltage sources (AC line or power supplies).

III. Assembling MOS Devices Onto PC Boards:

1. The MOS circuits should be mounted on the PC board last.
2. Similar precautions should be taken as in Item I above, at the assembly work station.
3. Soldering irons or solder baths should be at the same reference (ground) potential as the devices.
4. Plastic materials which are not antistatic treated should be kept away from devices as they develop and maintain high levels of static charge.

IV. Device Handling:

1. Handling of devices should be kept to a minimum. If handling is required, avoid touching the leads directly.

V. General:

1. The handler should take every precaution that the device will see the same reference potential when moved.
2. Anyone handling individual devices should develop a habit of first touching the container in which the units are stored before touching the units.
3. Before placing the units into a PC board, the handler should touch the PC board first.
4. Personnel should not wear clothing which will build up static charge. They should wear smocks and clothing made of 100% cotton rather than wool or synthetic fibers.
5. Be careful of electrostatic build up through the movement of air over plastic material. This is especially true of acid sinks.
6. Personnel or operators should always wear grounded wrist straps when working with MOS devices.
7. A 1 meg ohm resistance ground strap is recommended and will protect people up to 5,000 volts AC RMS or DC by limiting current to 5 milliamperes.
8. Antistatic ionized air equipment is very effective and useful in preventing electrostatic damage.
9. Low humidity maximizes potential static problems. Maintaining humidity levels above 45% is one of the most effective ways to guard against static handling problems.

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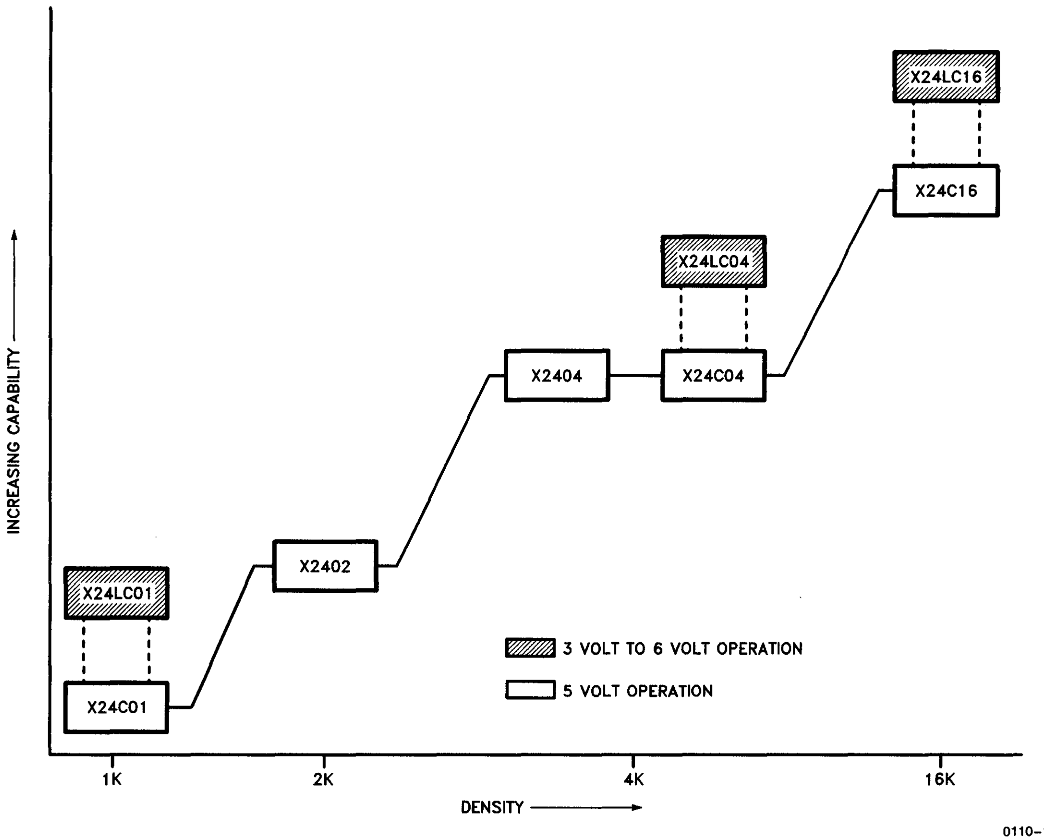
SERIAL MIGRATION PATH



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ADVANCED INFORMATION

1K	Commercial Industrial	X24C01 X24C01I	128 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **Low Power CMOS**
  - **—2 mA Active Current Typical**
  - **—60 μA Standby Current Typical**
- **Internally Organized 128 x 8**
- **2 Wire Serial Interface**
  - **—Provides Bidirectional Data Transfer Protocol**
- **Four Byte Page Write Mode**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **Inherent 100+ Years Data Retention**
- **8-Pin Mini-DIP Package**
- **8-Pin SOIC Package**

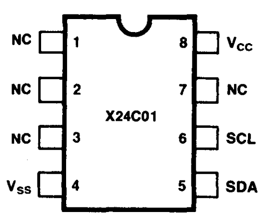
DESCRIPTION

The X24C01 is a CMOS 1024 bit serial E^2PROM, internally organized as 128 x 8. The X24C01 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance.

PIN CONFIGURATIONS

PLASTIC



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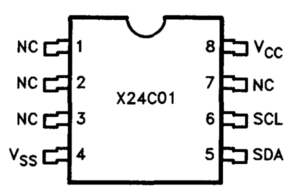
SOIC



0107-2

PIN NAMES

1 to 3	No Connect
4	V_{SS}
5	SDA Serial Data
6	SCL Serial Clock
7	No Connect → to V_{SS}
8	V_{CC}

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
  X24C01 .... −10°C to +85°C
  X24C01I .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
  Respect to V_{SS} .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
  (Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24C01 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X24C01I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	Power Supply Current		2.0	3.0	mA	f_{SCL} = 100 KHz
I_{SB}(2)	Standby Current		60	100	μA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current		0.1	10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	μA	V_{OUT} = GND to V_{CC}
V_{IL}(3)	Input Low Voltage	−1.0		V_{CC} ×0.3	V	
V_{IH}(3)	Input High Voltage	V_{CC} ×0.7		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

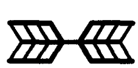
Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) SDA and SCL require pull-up resistor.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS LIMITS

X24C01 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X24C01I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

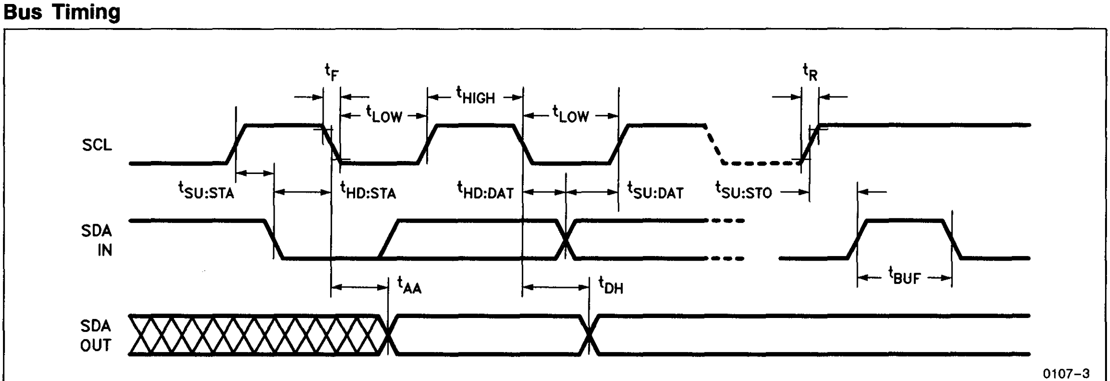
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Typical Power-Up Timing

Symbol	Parameter	Max.	Units
t_{PUR}(5)	Power-Up to Read Operation	1	ms
t_{PUW}(5)	Power-Up to Write Operation	5	ms

Bus Timing



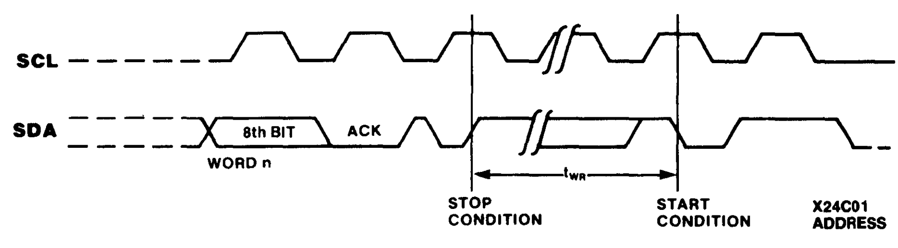
Note: (5) This parameter is periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WR}(7)	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24C01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

DEVICE OPERATION

The X24C01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. A controller initiates data transfers, and provides the clock for both transmit and receive operations.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24C01 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. This is true only if the previous sequence was correctly terminated with a stop condition.

Notes: (6) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).

(7) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Figure 1: Data Validity

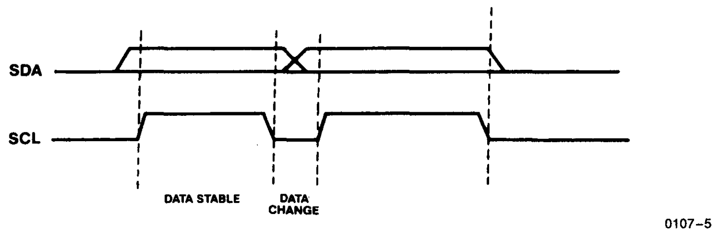
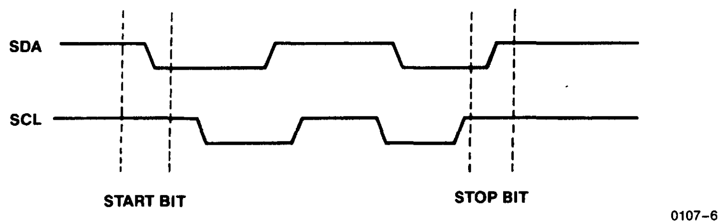


Figure 2: Definition of Start and Stop



Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24C01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

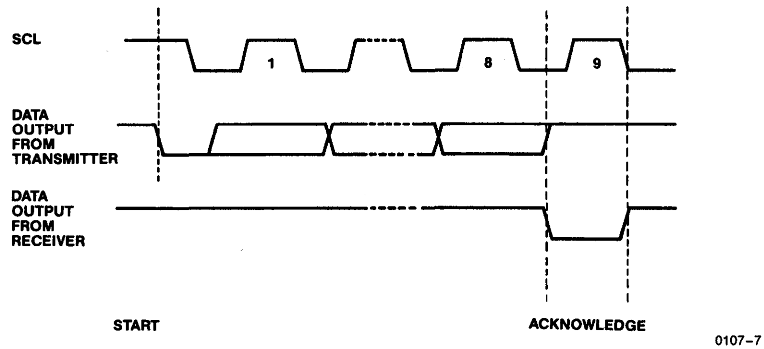
Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24C01 will always respond with an acknowledge after recognition of a start condition, a seven bit word address and a $R/\overline{W}$ bit. If a write operation has been selected, the X24C01 will respond with an acknowledge after each byte of data is received.

In the read mode the X24C01 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the controller, the X24C01 will continue to transmit data. If an acknowledge is not detected, the X24C01 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Figure 3: Acknowledge Response From Receiver

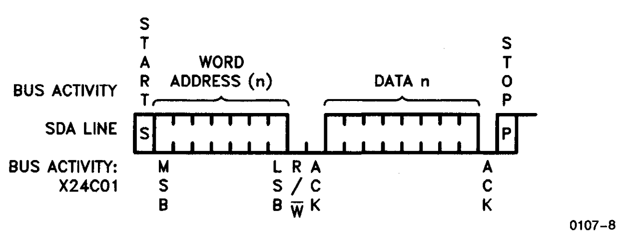


WRITE OPERATIONS

Byte Write

To initiate a write operation, the controller sends a start condition followed by a seven bit word address and a write bit. The X24C01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The controller then terminates the transfer by generating a stop condition, at which time the X24C01 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress, the X24C01 inputs are disabled, and the device will not respond to any requests from the controller. Refer to Figure 4 for the address, acknowledge and data transfer sequence.

Figure 4: Byte Write



Page Write

The most significant five bits of the word address define the page address. The X24C01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the controller can transmit up to three more bytes. After the receipt of each data byte, the X24C01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the controller should transmit more than four data bytes prior to generating the stop condition, the address counter will "roll over" and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24C01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a read or write operation. If the X24C01 is still busy with the write operation no ACK will be returned. If the X24C01 has completed the write operation an ACK will be returned and the controller can then proceed with the next read or write operation.

READ OPERATIONS

To terminate a read operation, the controller must **either** issue a stop condition during the ninth cycle **or** hold SDA high during the ninth clock cycle (i.e. not issue an acknowledge) and then issue a stop condition later.

Byte Read

To initiate a read operation, the controller sends a start condition followed by a seven bit word address and a read bit. The X24C01 responds with an acknowledge and then transmits the eight bits of data. If the controller does not acknowledge the transfer and generates a stop condition, the X24C01 will discontinue transmission. Refer to Figure 6 for the start, word address, read bit, acknowledge and data transfer sequence.

Figure 5: Page Write

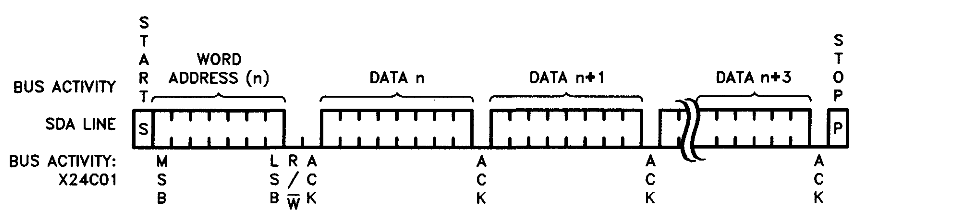
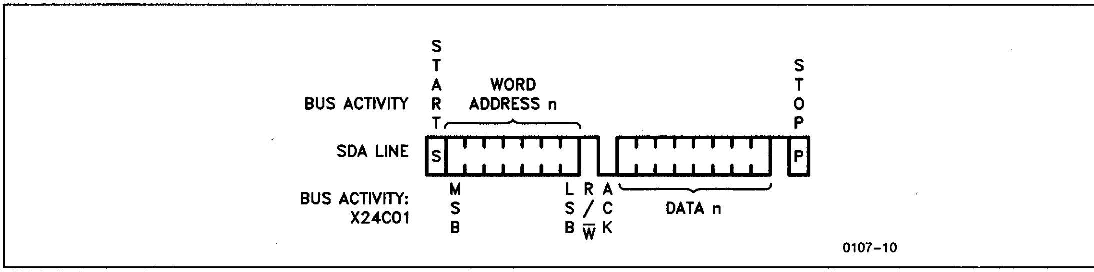


Figure 6: Byte Read

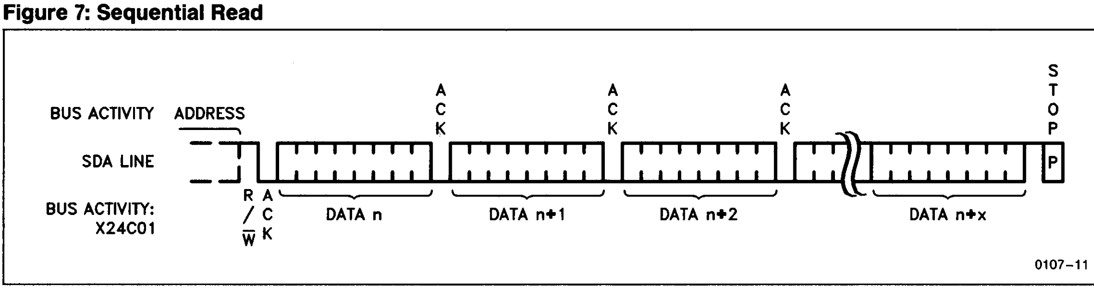


Sequential Read

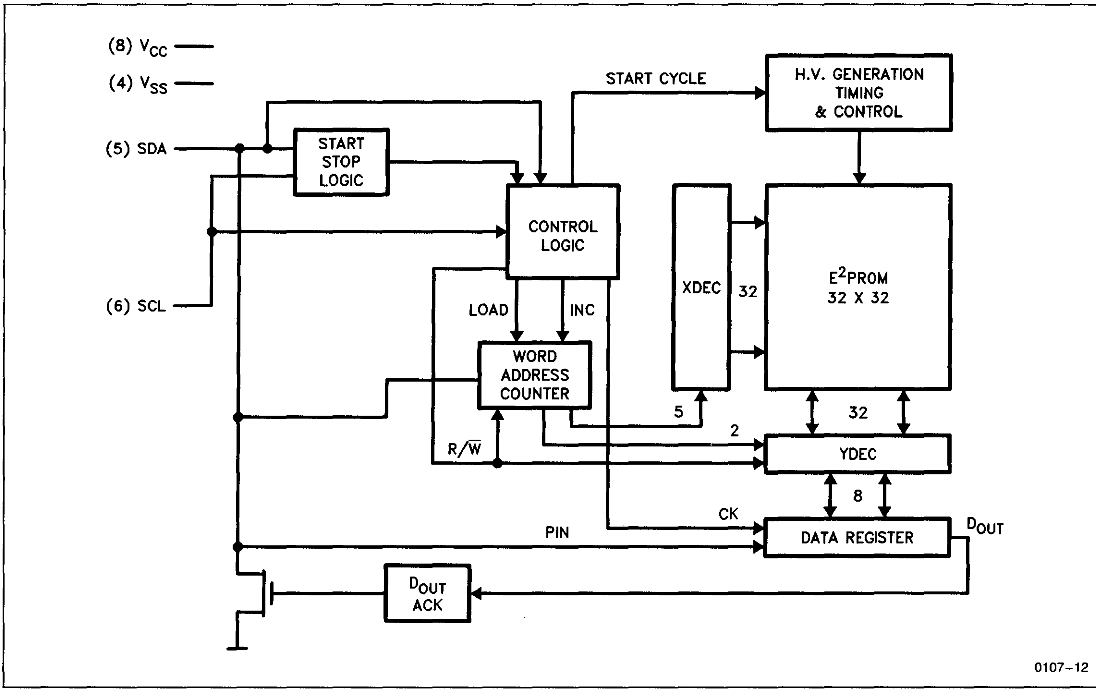
Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the controller now responds with an acknowledge, indicating it requires additional data. The X24C01 continues to output data for each acknowledge received. The read operation is terminated by the controller not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. When the highest address is reached, the counter "rolls over" to address 0 and the X24C01 continues to output data for each acknowledge received. Refer to Figure 7 for the address, acknowledge and data transfer sequence.

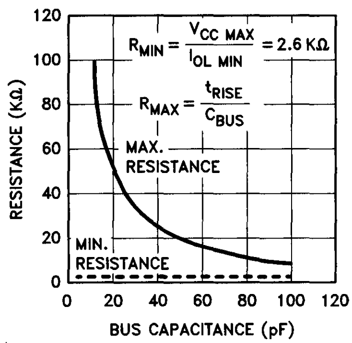
Figure 7: Sequential Read



FUNCTIONAL DIAGRAM



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



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ORDERING INFORMATION
SERIAL E2PROMs

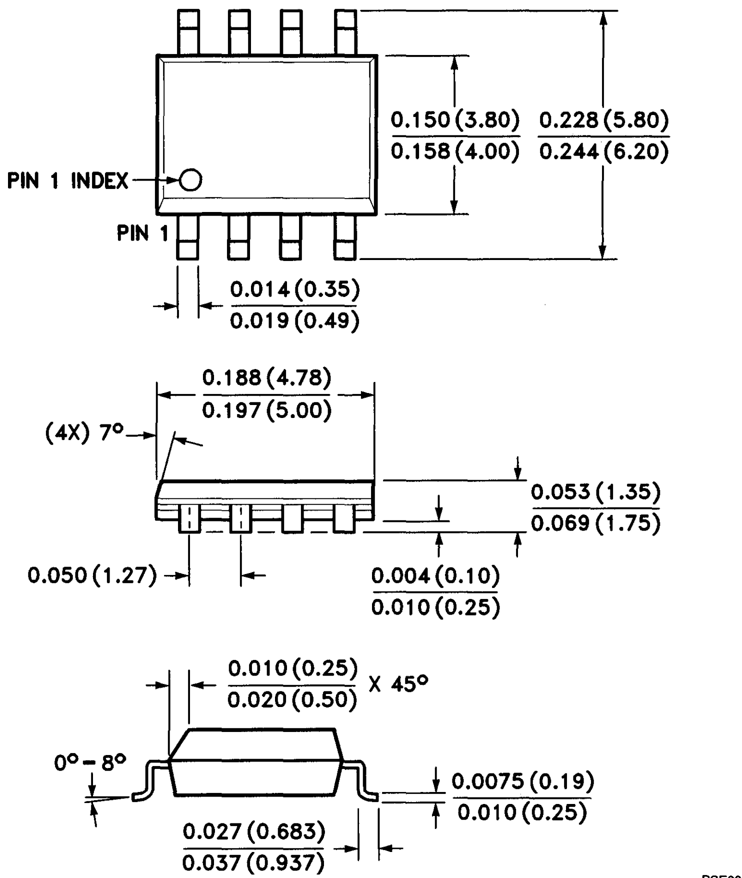
Device Order Number	Organization	Package										Temp. Range	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G			
X24C01S	128 x 8	•										†	CMOS	Standard
X24C01SI	128 x 8	•										I	CMOS	Standard
X24C01P	128 x 8		•									†	CMOS	Standard
X24C01PI	128 x 8		•									I	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 8-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

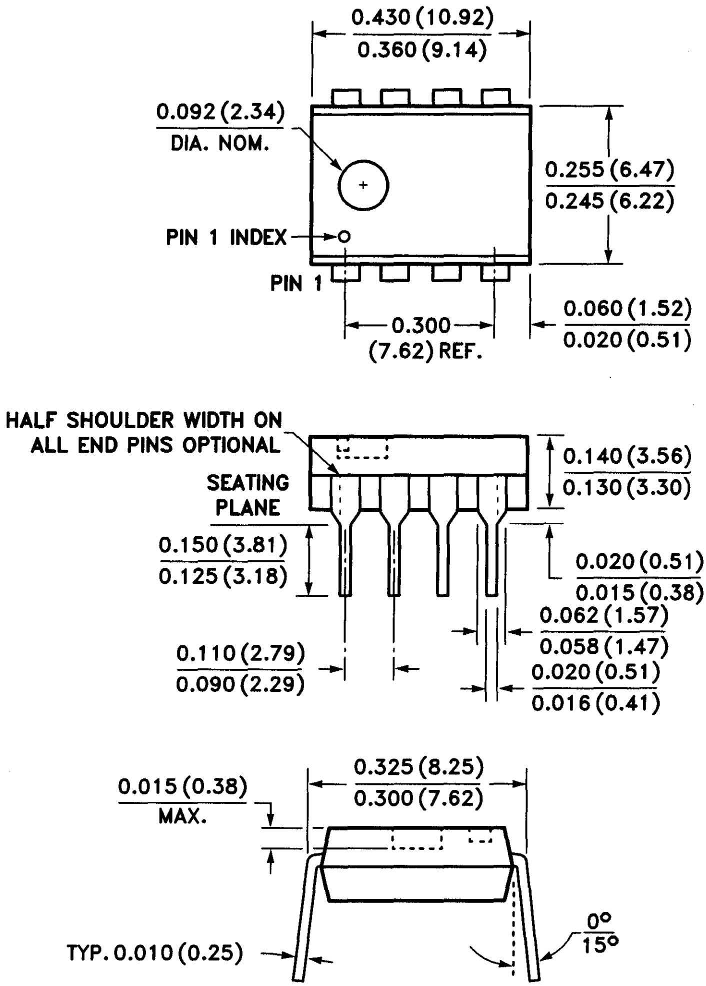
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



PPI008

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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ADVANCED INFORMATION

1K	Commercial Industrial	X24LC01 X24LC01I	128 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **3V–6V V_{CC} Operation**
- **Low Power CMOS**
  - **—2 mA Active Current Typical**
  - **—60 μA Standby Current Typical**
- **Internally Organized 128 x 8**
- **2 Wire Serial Interface**
  - **—Provides Bidirectional Data Transfer Protocol**
- **Four Byte Page Write Mode**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **Inherent 100+ Years Data Retention**
- **8-Pin Mini-DIP Package**
- **8-Pin SOIC Package**

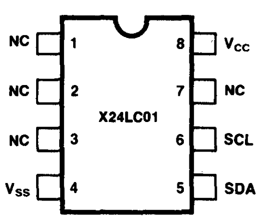
DESCRIPTION

The X24LC01 is a CMOS 1024 bit serial E^2PROM, internally organized as 128 x 8. The X24LC01 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance.

PIN CONFIGURATIONS

PLASTIC



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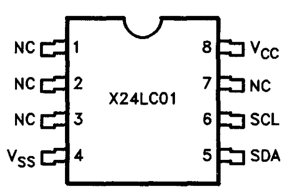
SOIC



0109-3

PIN NAMES

1 to 3	No Connect
4	V_{SS}
5	SDA Serial Data
6	SCL Serial Clock
7	No Connect
8	V_{CC} +3V to +6V

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
- X24LC01 .... −10°C to +85°C
- X24LC01I .... −65°C to +135°C

Storage Temperature .... −65°C to +150°C

Voltage on any Pin with
- Respect to V_{SS} .... −1.0V to +7V

D.C. Output Current .... 5 mA

Lead Temperature
- (Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24LC01 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC01I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	Power Supply Current		2.0	3.0	mA	f_{SCL} = 100 KHz
I_{SB}(2)	Standby Current V_{CC} = 6V			150	µA	V_{IN} = GND or V_{CC}
I_{SB}(2)	Standby Current V_{CC} = 3V			50	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current		0.1	10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(3)	Input Low Voltage	−1.0		V_{CC} ×0.3	V	
V_{IH}(3)	Input High Voltage	V_{CC} ×0.7		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

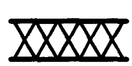
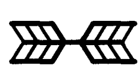
Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (SCL)	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(2) SDA and SCL require pull-up resistor.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS LIMITS

X24LC01 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC01I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

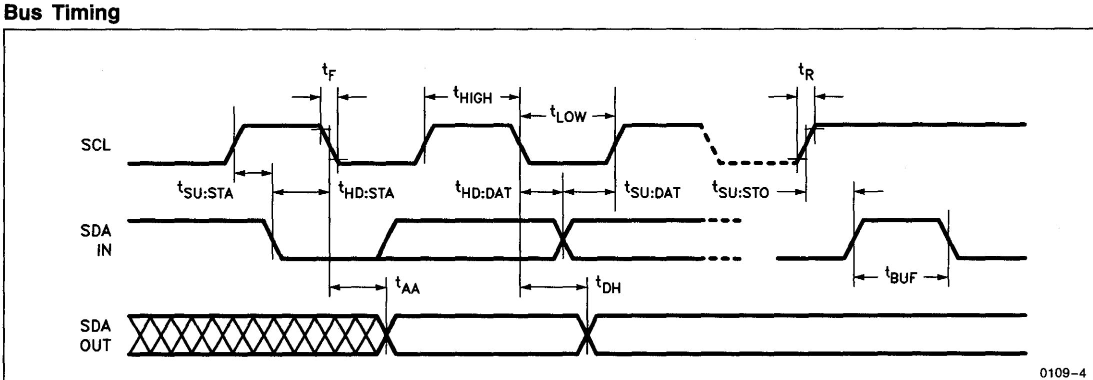
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Typical Power-Up Timing

Symbol	Parameter	Typ.(5)	Units
t_{PUR}(6)	Power-Up to Read Operation	2.0	ms
t_{PUW}(6)	Power-Up to Write Operation	2.0	ms

Bus Timing



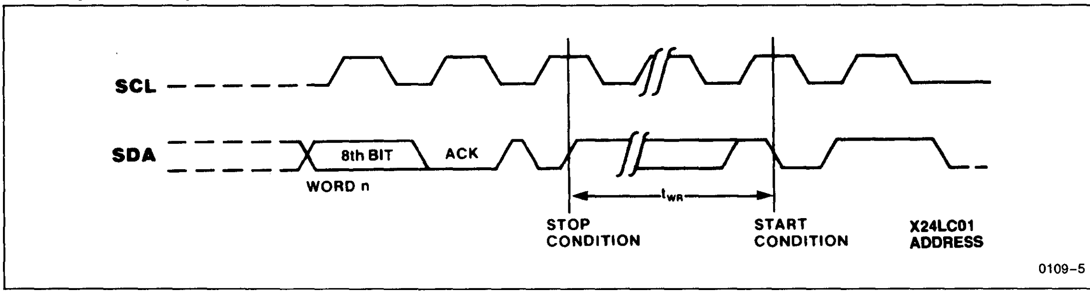
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage (5V).
(6) This parameter is periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{WR}(8)	Write Cycle Time		5	10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC01 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its word address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output requires the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

DEVICE OPERATION

The X24LC01 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. A controller initiates data transfers, and provides the clock for both transmit and receive operations.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC01 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. This is true only if the previous sequence was correctly terminated with a stop condition.

Notes: (7) Typical values are for T_A = 25°C and nominal supply voltage (5V).

(8) t_{WR} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

Figure 1: Data Validity

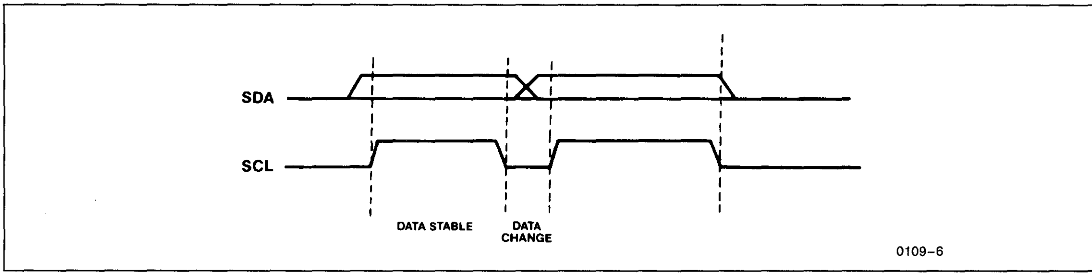
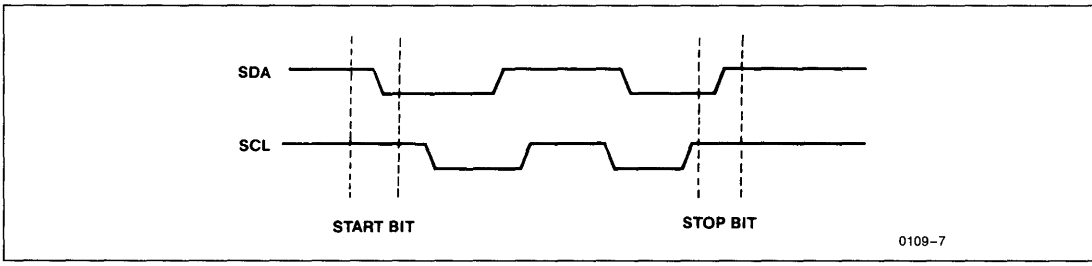


Figure 2: Definition of Start and Stop



Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC01 to place the device in the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

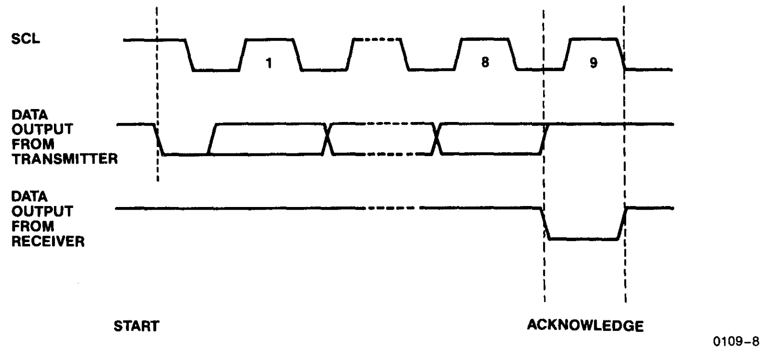
Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC01 will always respond with an acknowledge after recognition of a start condition, a seven bit word address and a R/$\overline{W}$ bit. If a write operation has been selected, the X24LC01 will respond with an acknowledge after each byte of data is received.

In the read mode the X24LC01 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the controller, the X24LC01 will continue to transmit data. If an acknowledge is not detected, the X24LC01 will terminate further data transmissions and await the stop condition to return to the standby power mode.

Figure 3: Acknowledge Response From Receiver

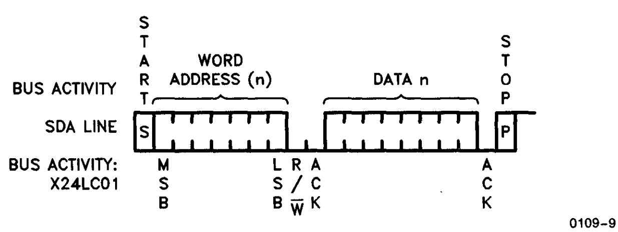


WRITE OPERATIONS

Byte Write

To initiate a write operation, the controller sends a start condition followed by a seven bit word address and a write bit. The X24LC01 responds with an acknowledge, then waits for eight bits of data and then responds with an acknowledge. The controller then terminates the transfer by generating a stop condition, at which time the X24LC01 begins the internal write cycle to the non-volatile memory. While the internal write cycle is in progress, the X24LC01 inputs are disabled, and the device will not respond to any requests from the controller. Refer to Figure 4 for the address, acknowledge and data transfer sequence.

Figure 4: Byte Write



Page Write

The most significant five bits of the word address define the page address. The X24LC01 is capable of a four byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the transfer of data after the first data byte, the controller can transmit up to three more bytes. After the receipt of each data byte, the X24LC01 will respond with an acknowledge.

After the receipt of each data byte, the two low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the controller should transmit more than four data bytes prior to generating the stop condition, the address counter will "roll over" and the previously transmitted data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC01 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the word address for a read or write operation. If the X24LC01 is still busy with the write operation no ACK will be returned. If the X24LC01 has completed the write operation an ACK will be returned and the controller can then proceed with the next read or write operation.

READ OPERATIONS

To terminate a read operation, the controller must **either** issue a stop condition during the ninth cycle **or** hold SDA high during the ninth clock cycle (i.e. not issue an acknowledge) and then issue a stop condition later.

Byte Read

To initiate a read operation, the controller sends a start condition followed by a seven bit word address and a read bit. The X24LC01 responds with an acknowledge and then transmits the eight bits of data. If the controller does not acknowledge the transfer and generates a stop condition, the X24LC01 will discontinue transmission. Refer to Figure 6 for the start, word address, read bit, acknowledge and data transfer sequence.

Figure 5: Page Write

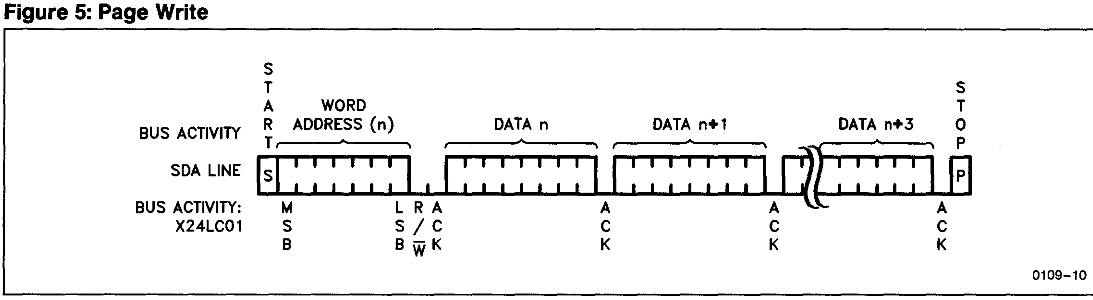
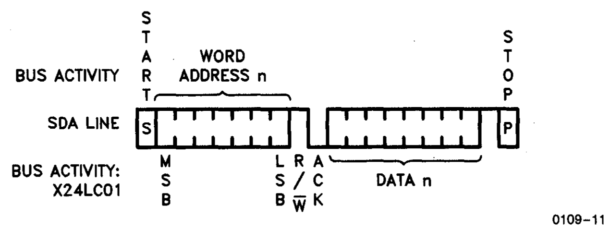


Figure 6: Byte Read

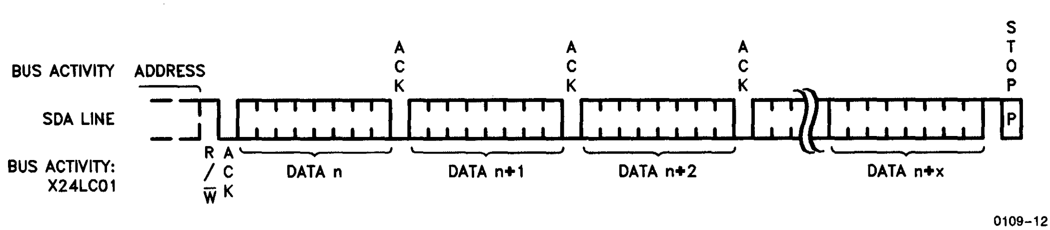


Sequential Read

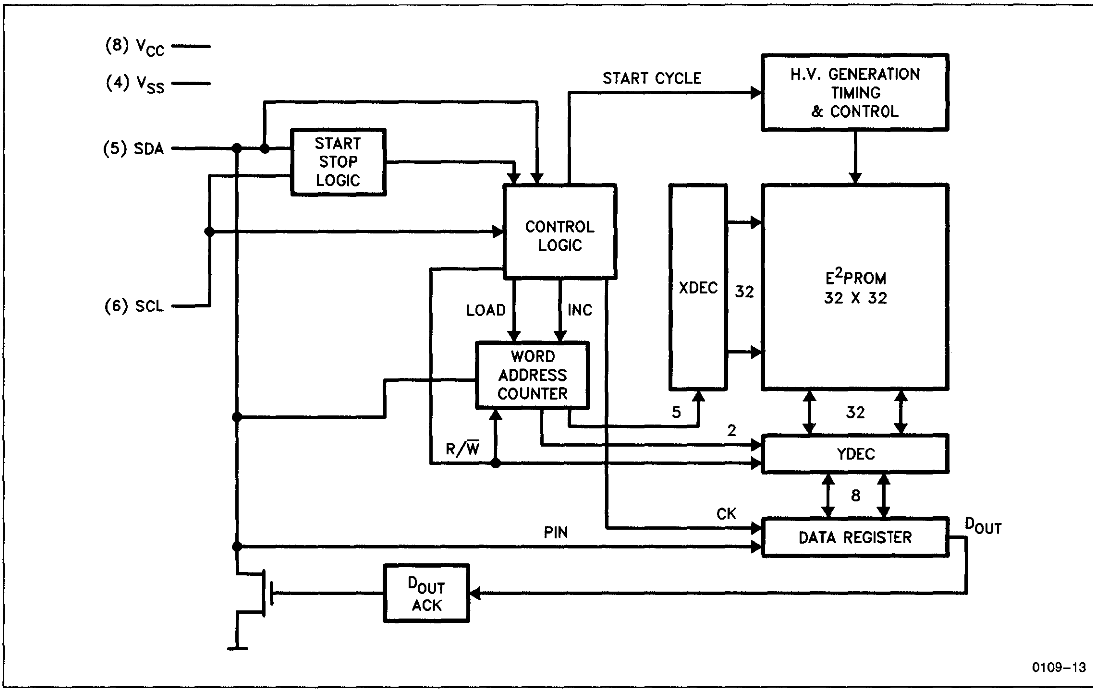
Sequential read is initiated in the same manner as the byte read. The first data byte is transmitted as with the byte read mode, however, the controller now responds with an acknowledge, indicating it requires additional data. The X24LC01 continues to output data for each acknowledge received. The read operation is terminated by the controller not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. When the highest address is reached, the counter "rolls over" to address 0 and the X24LC01 continues to output data for each acknowledge received. Refer to Figure 7 for the address, acknowledge and data transfer sequence.

Figure 7: Sequential Read

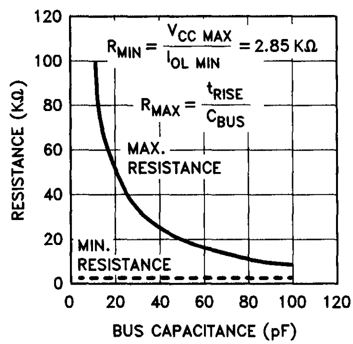


FUNCTIONAL DIAGRAM



0109–13

Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



0109–14

ORDERING INFORMATION

SERIAL E2PROMs

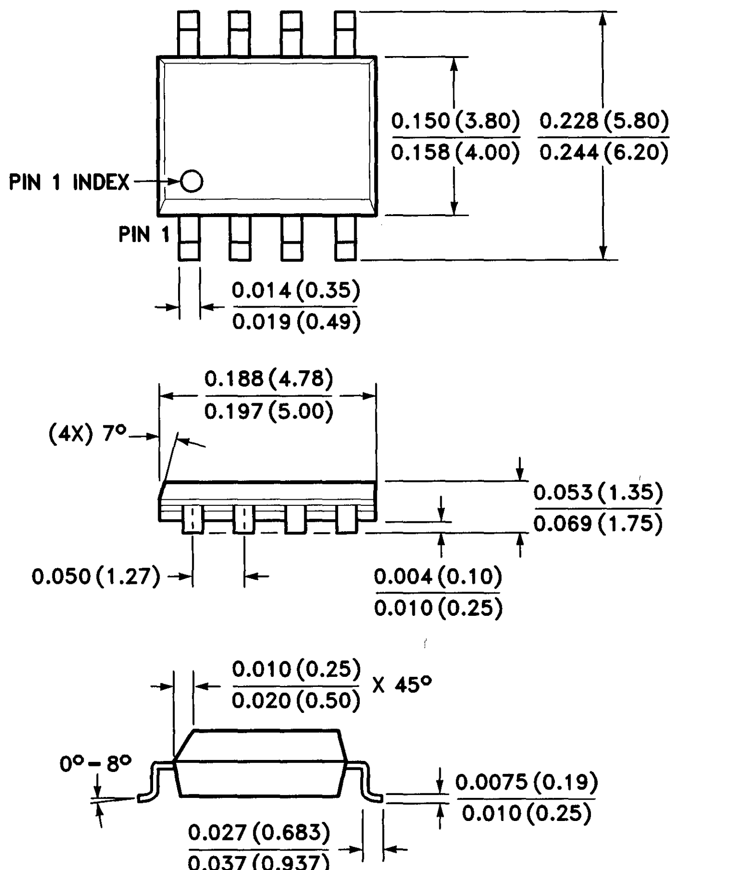
Device Order Number	Organization	Package										Temp. Range	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G			
X24LC01S	128 x 8	•										†	CMOS	Standard
X24LC01SI	128 x 8	•										I	CMOS	Standard
X24LC01P	128 x 8		•									†	CMOS	Standard
X24LC01PI	128 x 8		•									I	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 8-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

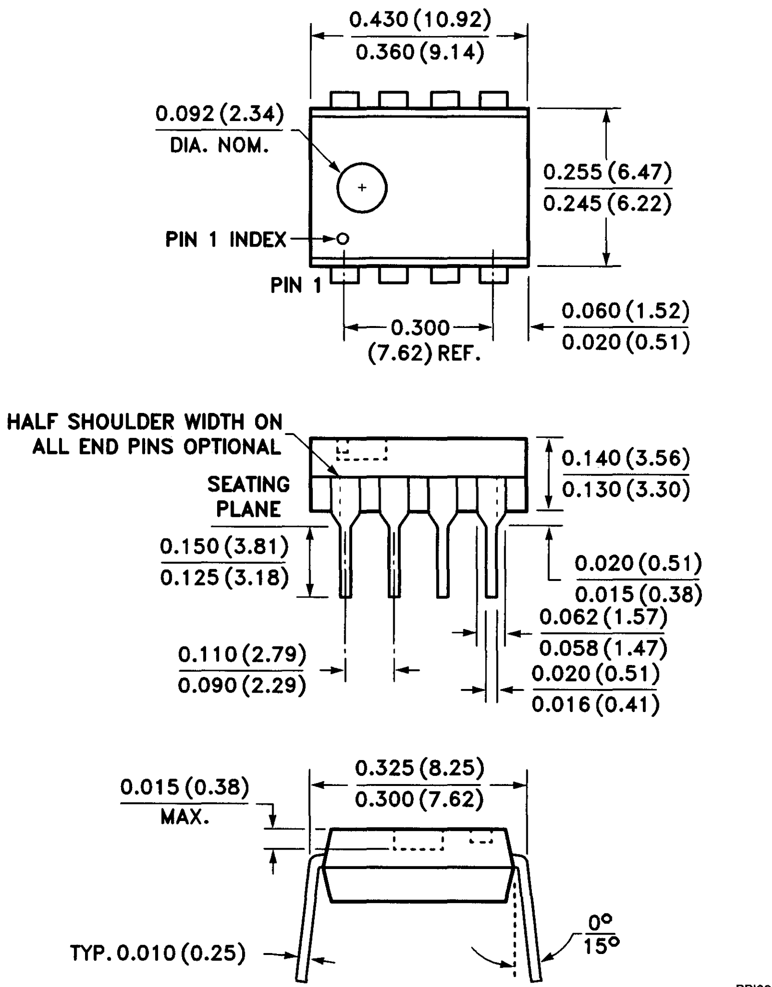
8-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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PRELIMINARY INFORMATION

4K	Commercial Industrial	X24LC04 X24LC04I	512 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **3V–6V V_{CC} Operation**
- **Low Power CMOS**
  - **—2 mA Active Current Typical**
  - **—60 μA Standby Current Typical**
- **Internally Organized as Two Pages**
  - **—Each 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Sixteen Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **Inherent 100+ Years Data Retention**
- **8-Pin Mini-DIP Package**
- **14-Pin SOIC Package**

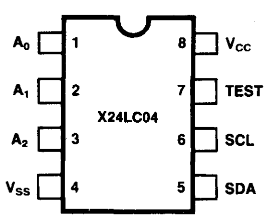
DESCRIPTION

The X24LC04 is a CMOS 4096 bit serial E^2PROM, internally organized as two 256 x 8 pages. The X24LC04 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance.

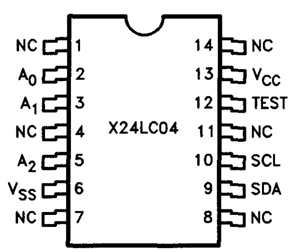
PIN CONFIGURATIONS

PLASTIC CERDIP



0106-1

SOIC



0106-2

PIN NAMES

A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V_{SS}
V_{SS}	Ground
V_{CC}	+3V to +6V
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24LC04 .... −10°C to +85°C
X24LC04I .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24LC04 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC04I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	Power Supply Current		2.0	3.0	mA	f_{SCL} = 100 KHz
I_{SB}(2)	Standby Current V_{CC} = 6V			150	µA	V_{IN} = GND or V_{CC}
I_{SB}(2)	Standby Current V_{CC} = 3V			50	µA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current		0.1	10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(3)	Input Low Voltage	−1.0		V_{CC} ×0.3	V	
V_{IH}(3)	Input High Voltage	V_{CC} ×0.7		V_{CC} +0.5	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

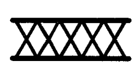
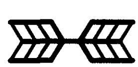
Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	V_{CC} ×0.1 to V_{CC} ×0.9
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	V_{CC} ×0.5
Output Load	1 TTL Gate and C_L = 100 pF

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) SDA and SCL require pull-up resistor.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS LIMITS

X24LC04 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC04I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

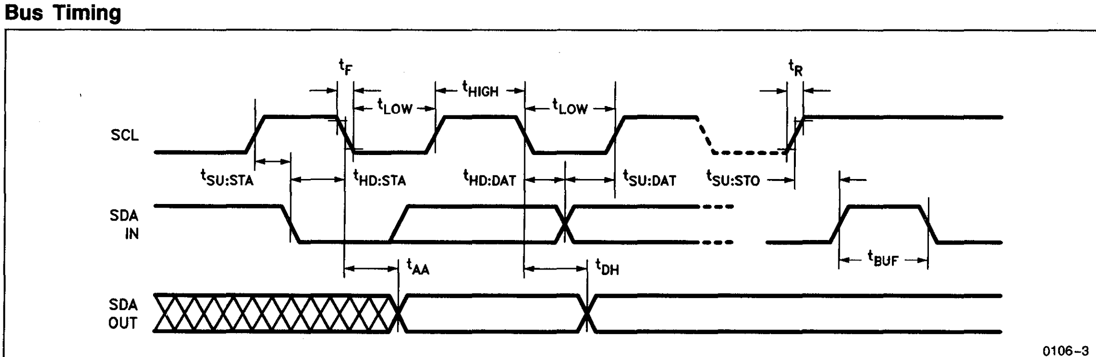
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		µs
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs
t_{LOW}	Clock Low Period	4.7		µs
t_{HIGH}	Clock High Period	4.0		µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	µs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs
t_{DH}	Data Out Hold Time	300		ns

Typical Power-Up Timing

Symbol	Parameter	Typ.(5)	Units
t_{PUR}(6)	Power-Up to Read Operation	2.0	µs
t_{PUW}(6)	Power-Up to Write Operation	2.0	µs

Bus Timing



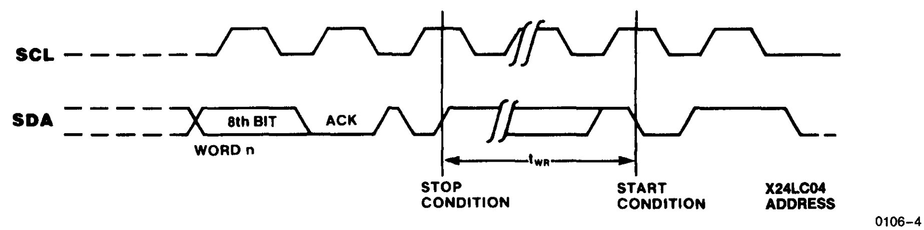
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage.
(6) This parameter is periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{WR}(8)	Write Cycle Time	10	5		ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC04 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output implies the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

Address (A_0)

A_0 is unused by the X24LC04, however, it must be tied to V_{SS} to insure proper device operation.

Address (A_1, A_2)

The Address inputs are used to set the least significant two bits of the six bit slave address. These inputs can be used static or driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If driven they must be driven by open collector outputs with resistor pull-ups to V_{CC}.

DEVICE OPERATION

The X24LC04 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24LC04 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC04 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (7) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).

(8) t_{WR} is the minimum cycle time from the system perspective; it is the maximum time the device requires to perform the internal write operation.

Figure 1: Data Validity

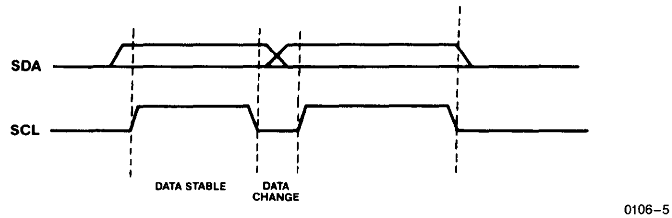
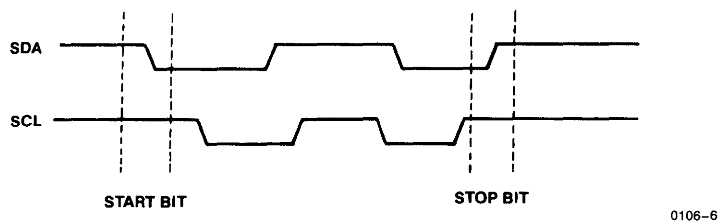


Figure 2: Definition of Start and Stop



Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC04 to place the device in the standby power mode.

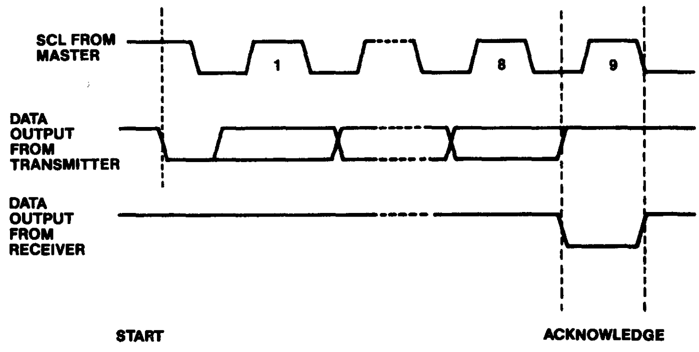
Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC04 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24LC04 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24LC04 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24LC04 will continue to transmit data. If an acknowledge is not detected, the X24LC04 will terminate further data transmissions and await the stop condition to return to the standby power mode.

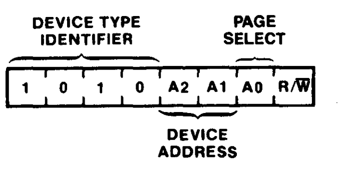
Figure 3: Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24LC04 this is fixed as 1010[B].

Figure 4: Slave Address



The next two significant bits address a particular device. A system could have up to four X24LC04 devices on the bus (see Figure 10). The four addresses are defined by the state of the A_1 and A_2 inputs.

The next bit of the slave address field (bit 1) is the page select bit. It is used by the host to toggle between the two 256 word pages of memory. This is, in effect the most significant bit for the word address.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

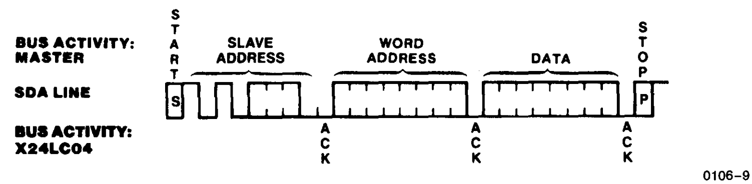
Following the start condition, the X24LC04 monitors the SDA bus comparing the slave address being transmitted with its address (device type and state of A_1 and A_2 inputs). Upon a compare the X24LC04 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24LC04 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24LC04 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words of memory. Upon receipt of the word address the X24LC04 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24LC04 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24LC04 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write



Page Write

The X24LC04 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24LC04 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC04 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24LC04 is still busy with the write operation no ACK will be returned. If the X24LC04 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

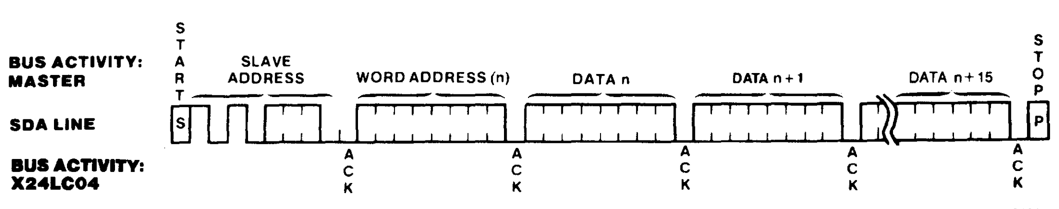
Read operations are initiated in the same manner as write operations with the exception that the bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Note: For each read operation, SDA must be brought back to a high level prior to the stop bit.

Current Address Read

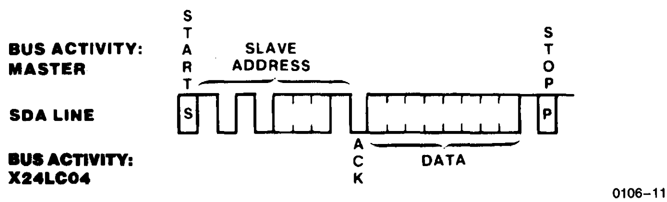
Internally the X24LC04 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with $R/\overline{W}$ set to one, the X24LC04 issues an acknowledge and transmits the eight bit word. The master does not acknowledge the transfer but does generate a stop condition and the X24LC04 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Figure 6: Page Write



NOTE: In this example n = XXXX 0000(B); X = 1 or 0

Figure 7: Current Address Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24LC04 and then by the eight bit word. The master does not acknowledge the transfer but does generate the stop condition and the X24LC04 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24LC04 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. If more than 512 words are read, the counter "rolls over" and the X24LC04 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 8: Random Read

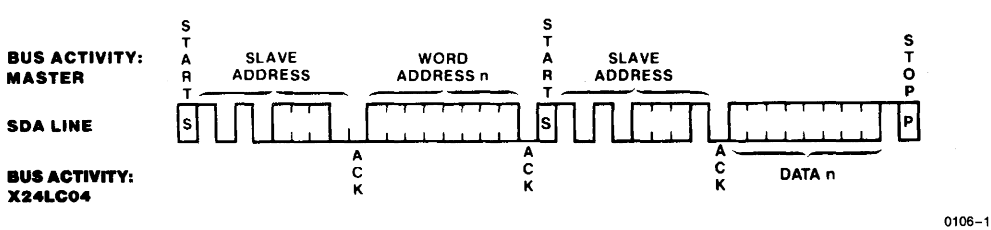


Figure 9: Sequential Read

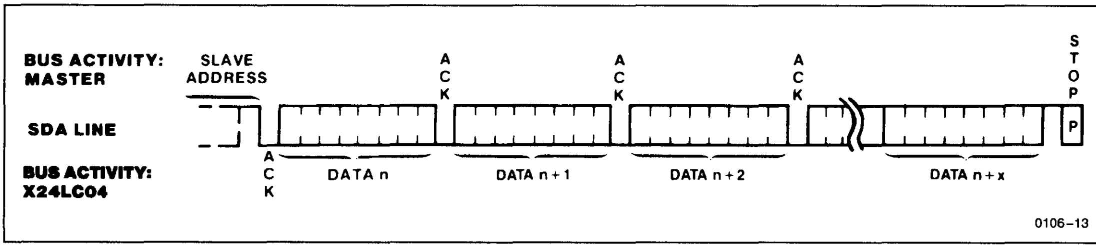
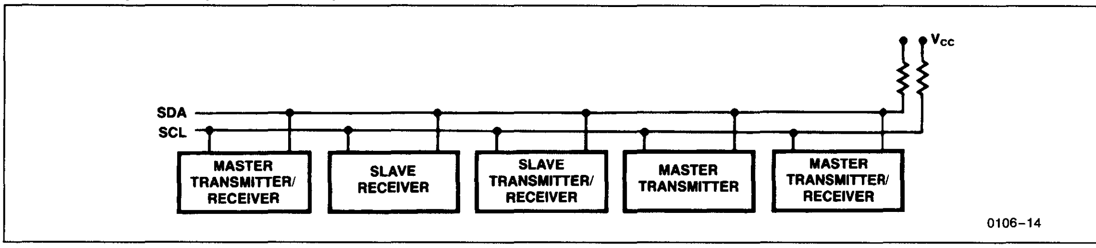
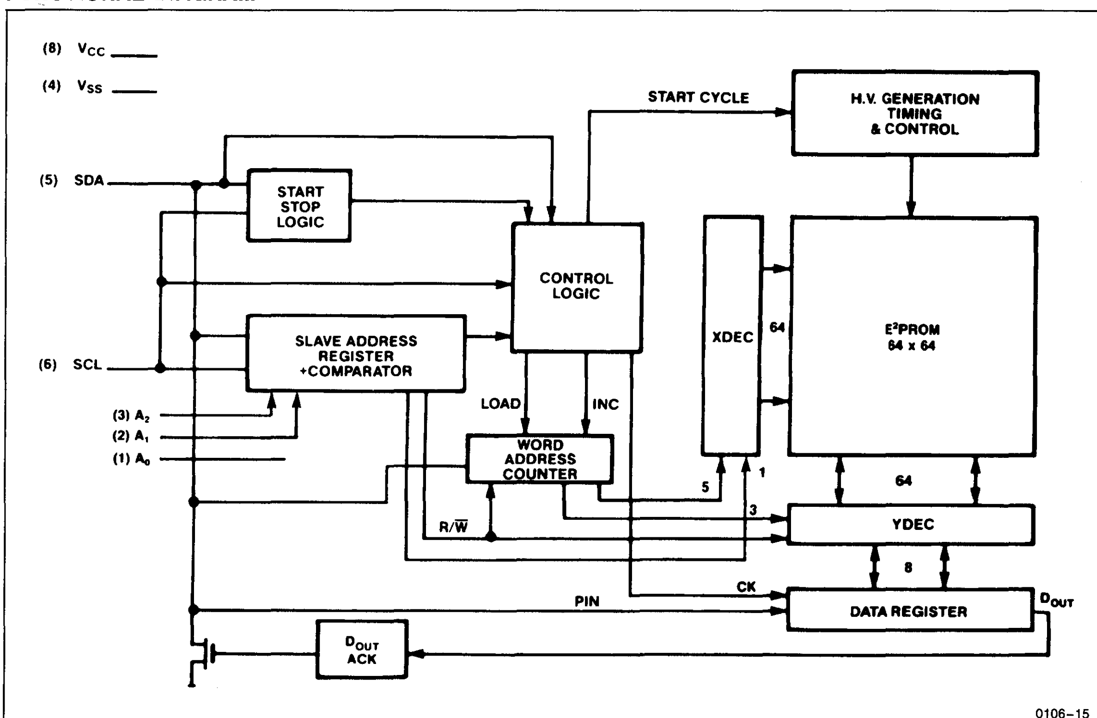


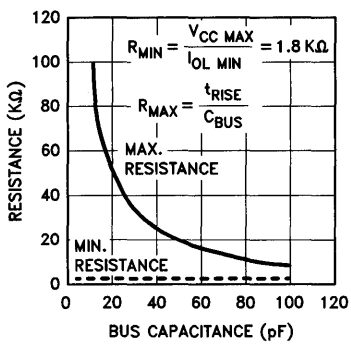
Figure 10: Typical System Configuration



FUNCTIONAL DIAGRAM



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



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ORDERING INFORMATION

SERIAL E^2PROMs

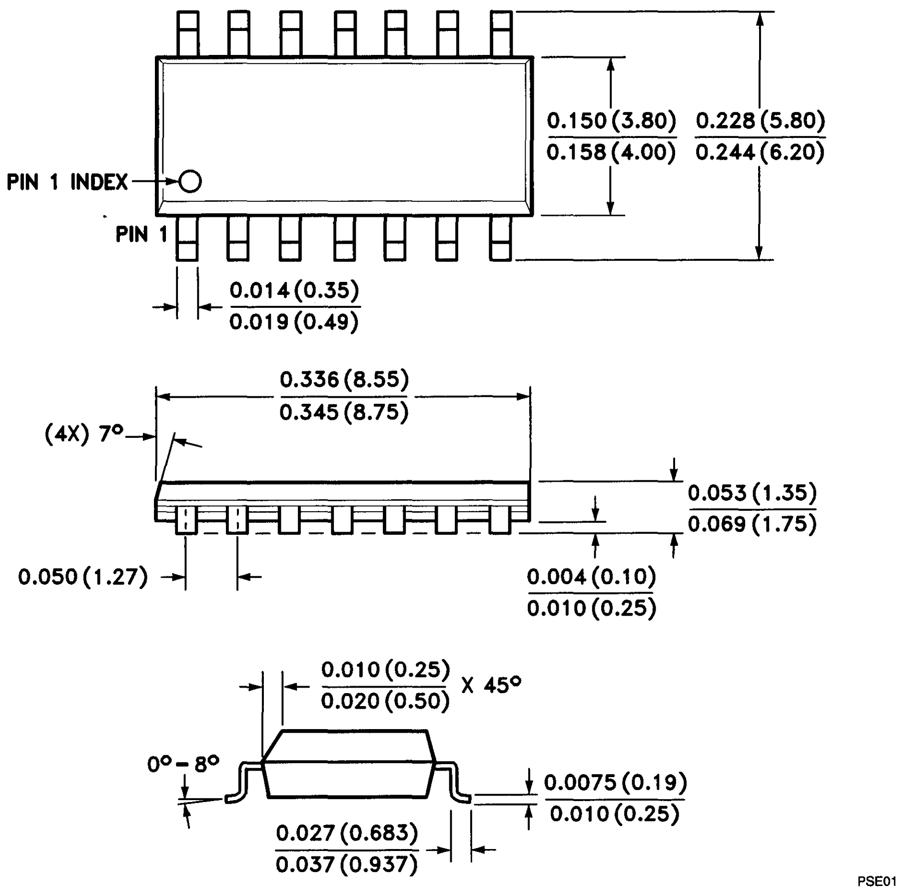
Device Order Number	Organization	Package										Temp. Range	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G			
X24LC04S	512 x 8	•										†	CMOS	Standard
X24LC04SI	512 x 8	•										I	CMOS	Standard
X24LC04P	512 x 8		•									†	CMOS	Standard
X24LC04PI	512 x 8		•									I	CMOS	Standard
X24LC04D	512 x 8			•								†	CMOS	Standard
X24LC04DI	512 x 8			•								I	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 14-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = 8-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

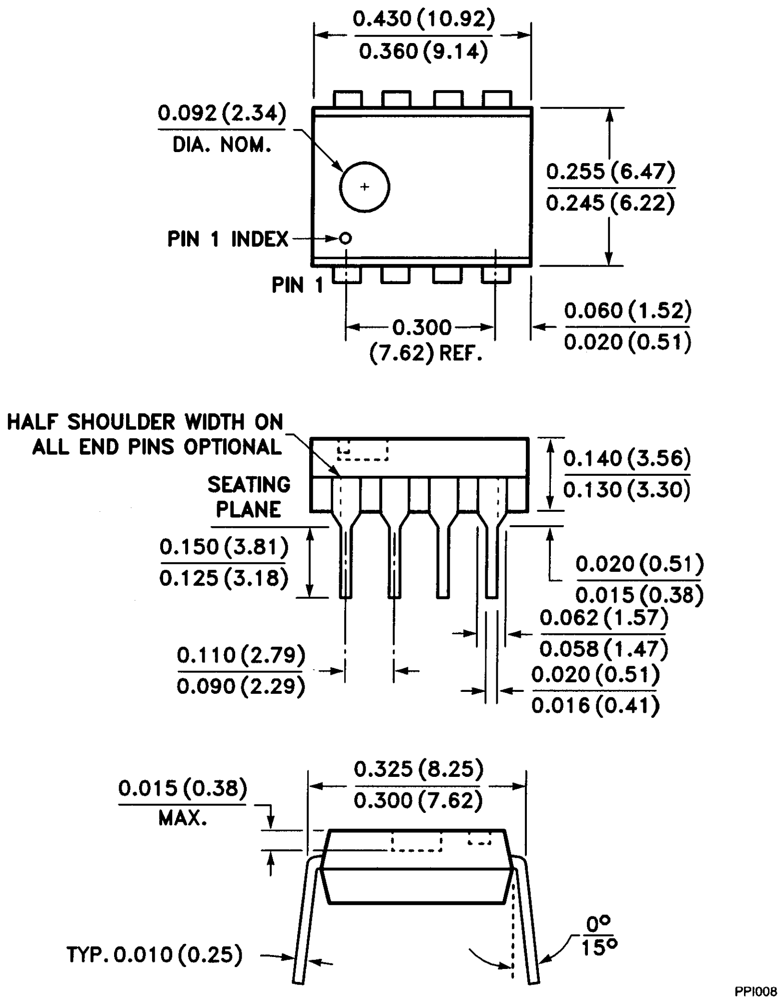
14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

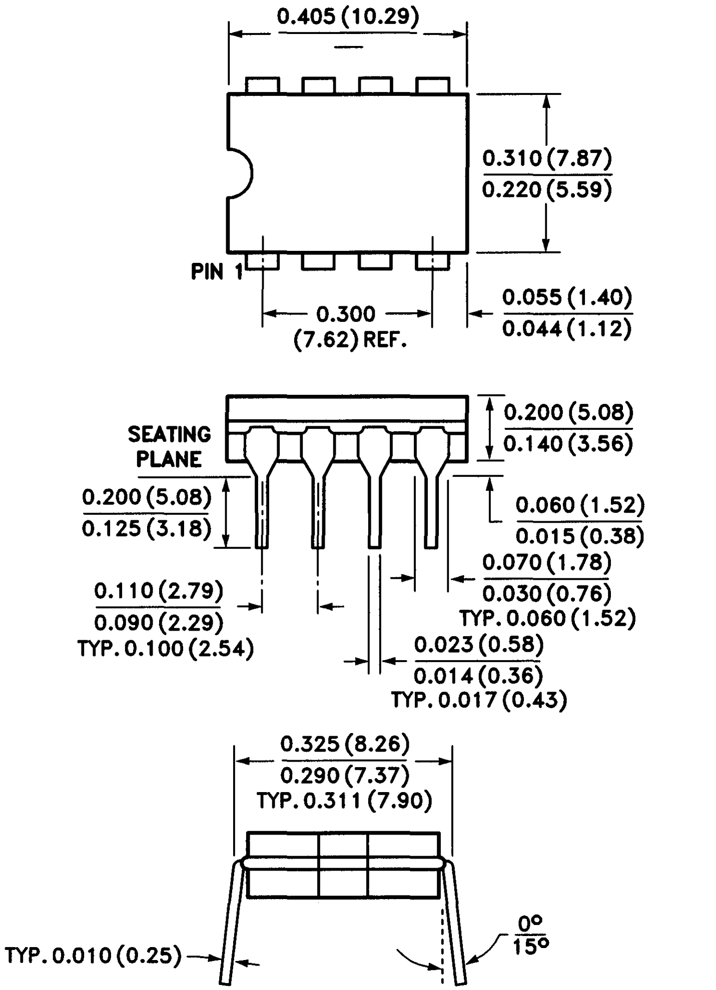
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

NOTES

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PRELIMINARY INFORMATION

16K	Commercial Industrial	X24LC16 X24LC16I	2048 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **3V–6V V_{CC} Operation**
- **Low Power CMOS**
  - **—2 mA Active Current Typical**
  - **—60 μA Standby Current Typical**
- **Internally Organized as Eight Pages**
  - **—Each 256 x 8**
- **2 Wire Serial Interface**
- **Provides Bidirectional Data Transfer Protocol**
- **Sixteen Byte Page Write Mode**
  - **—Minimizes Total Write Time Per Byte**
- **Self Timed Write Cycle**
  - **—Typical Write Cycle Time of 5 ms**
- **Inherent 100+ Years Data Retention**
- **8-Pin Mini-DIP Package**
- **14-Pin SOIC Package**

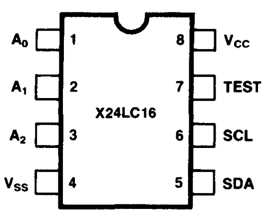
DESCRIPTION

The X24LC16 is a CMOS 16,384 bit serial E^{2}PROM, internally organized as eight 256 x 8 pages. The X24LC16 features a serial interface and software protocol allowing operation on a two wire bus.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance.

PIN CONFIGURATIONS

PLASTIC CERDIP



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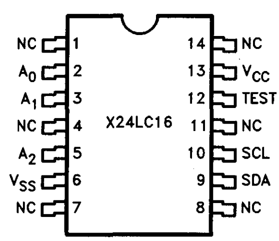
SOIC



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PIN NAMES

A_0–A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock
TEST	Hold at V_{SS}
V_{SS}	Ground
V_{CC}	+3V to +6V
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X24LC16 .... −10°C to +85°C
X24LC16I.............................. −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} .... −1.0V to +7V
D.C. Output Current.................................5 mA
Lead Temperature
(Soldering, 10 Seconds) ....300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X24LC16 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC16I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	Power Supply Current		2.0	3.0	mA	f_{SCL} = 100 KHz
I_{SB}(2)	Standby Current V_{CC} = 6V			150	μA	V_{IN} = GND or V_{CC}
I_{SB}(2)	Standby Current V_{CC} = 3V			50	μA	V_{IN} = GND or V_{CC}
I_{LI}	Input Leakage Current		0.1	10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		0.1	10	μA	V_{OUT} = GND to V_{CC}
V_{IL}(3)	Input Low Voltage	−1.0		$V_{CC} \times 0.3$	V	
V_{IH}(3)	Input High Voltage	$V_{CC} \times 0.7$		$V_{CC} + 0.5$	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3 mA

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

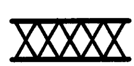
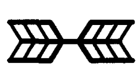
Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(4)	Input/Output Capacitance (SDA)	8	pF	$V_{I/O}$ = 0V
C_{IN}(4)	Input Capacitance (A_0, A_1, A_2, SCL)	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	$V_{CC} \times 0.1$ to $V_{CC} \times 0.9$
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	$V_{CC} \times 0.5$
Output Load	1 TTL Gate and C_L = 100 pF

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) SDA and SCL require pull-up resistor.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is periodically sampled and not 100% tested.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS LIMITS

X24LC16 T_A = 0°C to +70°C, V_{CC} = +3V to +6V, unless otherwise specified.
X24LC16I T_A = −40°C to +85°C, V_{CC} = +3V to +6V, unless otherwise specified.

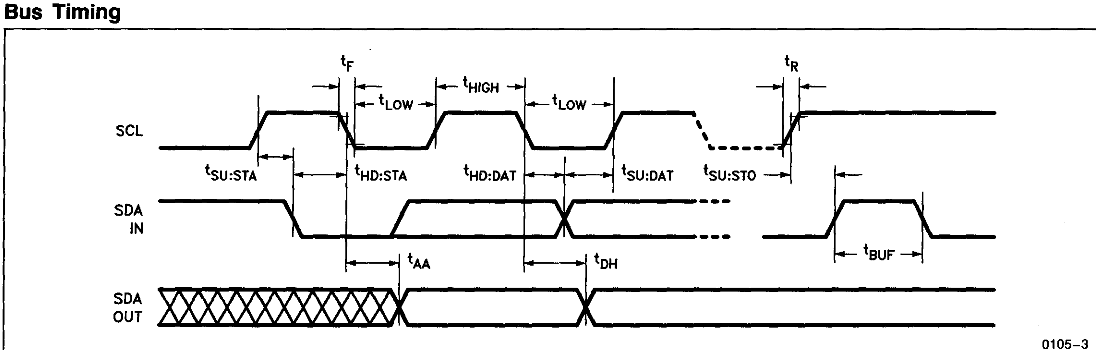
Read & Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
f_{SCL}	SCL Clock Frequency	0	100	KHz
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	μs
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4.7		μs
$t_{HD:STA}$	Start Condition Hold Time	4.0		μs
t_{LOW}	Clock Low Period	4.7		μs
t_{HIGH}	Clock High Period	4.0		μs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		μs
$t_{HD:DAT}$	Data In Hold Time	0		μs
$t_{SU:DAT}$	Data In Setup Time	250		ns
t_R	SDA and SCL Rise Time		1	μs
t_F	SDA and SCL Fall Time		300	ns
$t_{SU:STO}$	Stop Condition Setup Time	4.7		μs
t_{DH}	Data Out Hold Time	300		ns

Typical Power-Up Timing

Symbol	Parameter	Typ.(5)	Units
t_{PUR}(6)	Power-Up to Read Operation	2.0	μs
t_{PUW}(6)	Power-Up to Write Operation	2.0	μs

Bus Timing



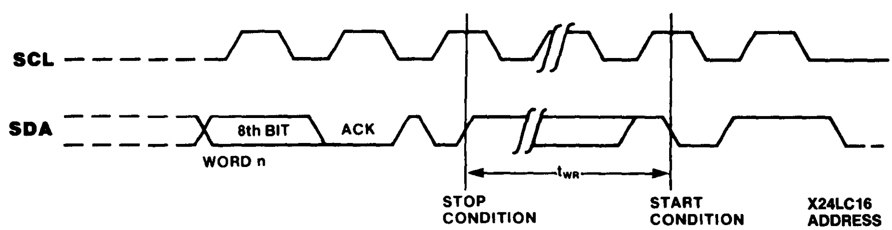
Notes: (5) Typical values are for T_A = 25°C and nominal supply voltage.
(6) This parameter is periodically sampled and not 100% tested.

Write Cycle Limits

Symbol	Parameter	Min.	Typ.(7)	Max.	Units
t_{WR}(8)	Write Cycle Time	10	5		ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the X24LC16 bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

Write Cycle Timing



0105-4

PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open collector output implies the use of a pull-up resistor. For selecting typical values, refer to the Guidelines for Calculating Typical Values of Bus Pull-Up Resistors graph.

Address (A_0, A_1, A_2)

The A_0, A_1 and A_2 inputs are unused by the X24LC16, however, they must be tied to V_{SS} to insure proper device operation.

DEVICE OPERATION

The X24LC16 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the X24LC16 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The X24LC16 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Notes: (7) Typical values are for $T_A = 25°C$ and nominal supply voltage (5V).

(8) t_{WR} is the minimum cycle time from the system perspective; it is the maximum time the device requires to perform the internal write operation.

Figure 1: Data Validity

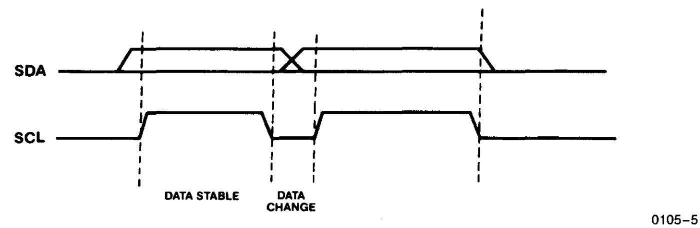
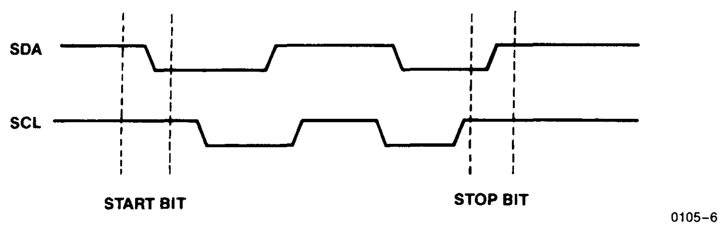


Figure 2: Definition of Start and Stop



Stop Condition

All communications are terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used by the X24LC16 to place the device in the standby power mode.

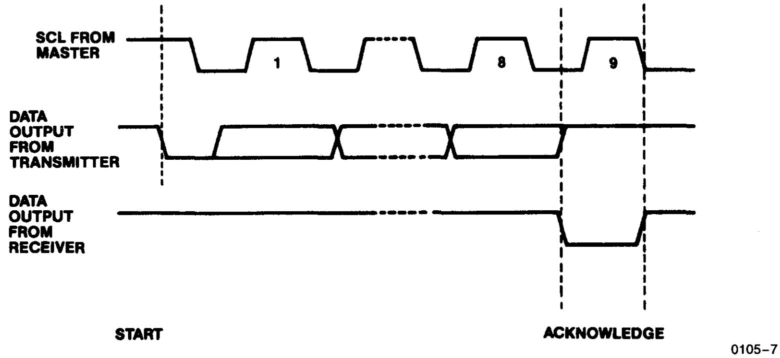
Acknowledge

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The X24LC16 will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the X24LC16 will respond with an acknowledge after the receipt of each subsequent eight bit word.

In the read mode the X24LC16 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the X24LC16 will continue to transmit data. If an acknowledge is not detected, the X24LC16 will terminate further data transmissions and await the stop condition to return to the standby power mode.

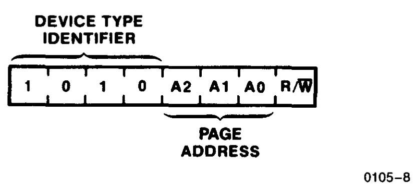
Figure 3: Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition the bus master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see Figure 4). For the X24LC16 this is fixed as 1010[B].

Figure 4: Slave Address



The next three bits of the slave address field are the page select bits. They are used by the master device to select which of the eight 256 word pages of memory are to be accessed. These bits are, in effect, the three most significant bits of the word address. It should be noted, the protocol limits the size of memory to eight pages of 256 words; therefore, the protocol can support only one X24LC16 per system.

The last bit of the slave address defines the operation to be performed. When set to one a read operation is selected, when set to zero a write operation is selected.

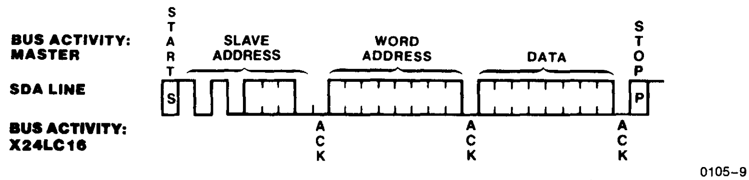
Following the start condition, the X24LC16 monitors the SDA bus comparing the slave address being transmitted with its slave address. Upon a compare the X24LC16 outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the X24LC16 will execute a read or write operation.

WRITE OPERATIONS

Byte Write

For a write operation, the X24LC16 requires a second address field. This address field is the word address, comprised of eight bits, providing access to any one of the 256 words in the selected page of memory. Upon receipt of the word address the X24LC16 responds with an acknowledge, and awaits the next eight bits of data, again responding with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the X24LC16 begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the X24LC16 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 5 for the address, acknowledge and data transfer sequence.

Figure 5: Byte Write



Page Write

The X24LC16 is capable of a sixteen byte page write operation. It is initiated in the same manner as the byte write operation, but instead of terminating the write cycle after the first data word is transferred, the master can transmit up to fifteen more words. After the receipt of each word, the X24LC16 will respond with an acknowledge.

After the receipt of each word, the four low order address bits are internally incremented by one. The high order seven bits of the word address remain constant. If the master should transmit more than sixteen words prior to generating the stop condition, the address counter will "roll over" and the previously written data will be overwritten. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 6 for the address, acknowledge and data transfer sequence.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical 5 ms write cycle time. Once the stop condition is issued to indicate the end of the host's write operation the X24LC16 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the X24LC16 is still busy with the write operation no ACK will be returned. If the X24LC16 has completed the write operation an ACK will be returned and the host can then proceed with the next read or write operation.

READ OPERATIONS

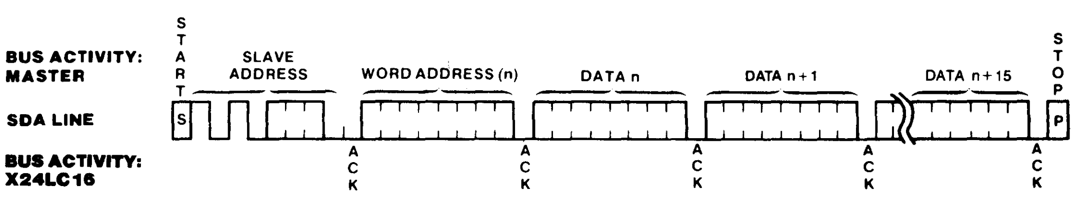
Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the slave address is set to a one. There are three basic read operations: current address read, random read and sequential read.

Note: For each read operation, SDA must be brought back to a high level prior to the stop bit.

Current Address Read

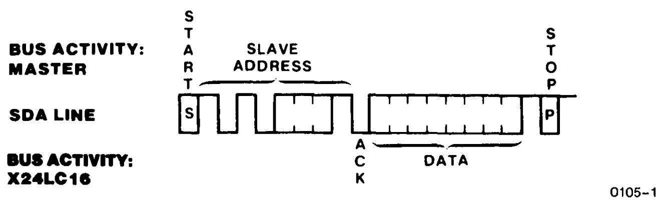
Internally the X24LC16 contains an address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address n, the next read operation would access data from address n+1. Upon receipt of the slave address with R/$\overline{W}$ set to one, the X24LC16 issues an acknowledge and transmits the eight bit word. The master will not acknowledge the transfer but does generate a stop condition and the X24LC16 discontinues transmission. Refer to Figure 7 for the sequence of address, acknowledge and data transfer.

Figure 6: Page Write



NOTE: In this example n = xxxx 0000(B); x = 1 or 0

Figure 7: Current Address Read



Random Read

Random read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to one, the master must first perform a "dummy" write operation. The master issues the start condition, and the slave address followed by the word address it is to read. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit set to one. This will be followed by an acknowledge from the X24LC16 and then by the eight bit word. The master will not acknowledge the transfer but does generate the stop condition and the X24LC16 discontinues transmission. Refer to Figure 8 for the address, acknowledge and data transfer sequence.

Sequential Read

Sequential reads can be initiated as either a current address read or random access read. The first word is transmitted as with the other read modes, however, the master now responds with an acknowledge, indicating it requires additional data. The X24LC16 continues to output data for each acknowledge received. The read operation is terminated by the master not responding with an acknowledge and generating a stop condition.

The data output is sequential, with the data from address n followed by the data from n+1. The address counter for read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. If more than 2048 words are read, the counter "rolls over" and the X24LC16 continues to output data for each acknowledge received. Refer to Figure 9 for the address, acknowledge and data transfer sequence.

Figure 8: Random Read

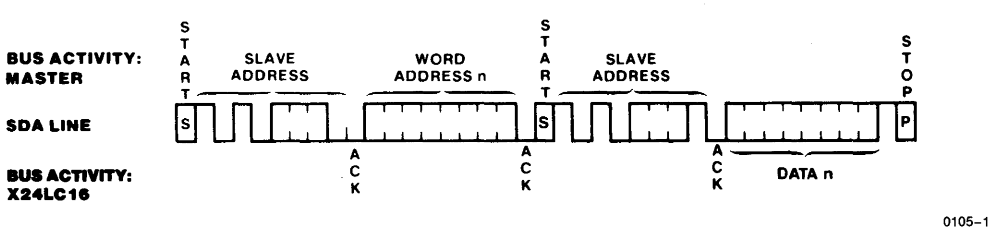


Figure 9: Sequential Read

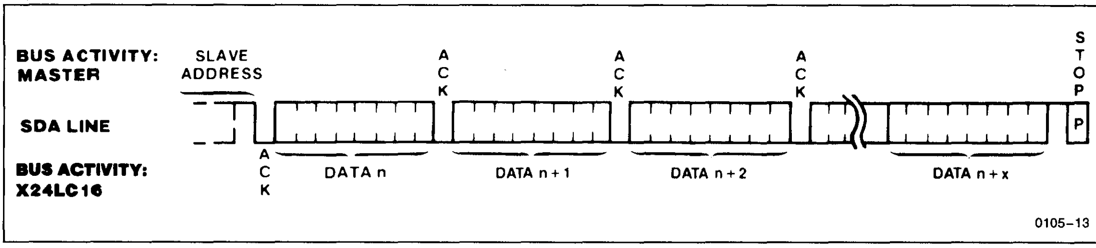
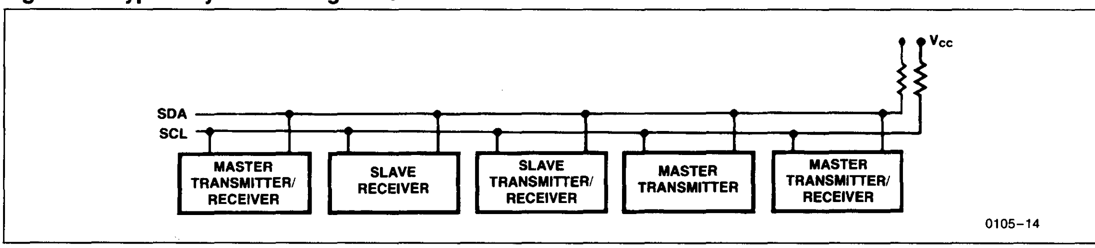
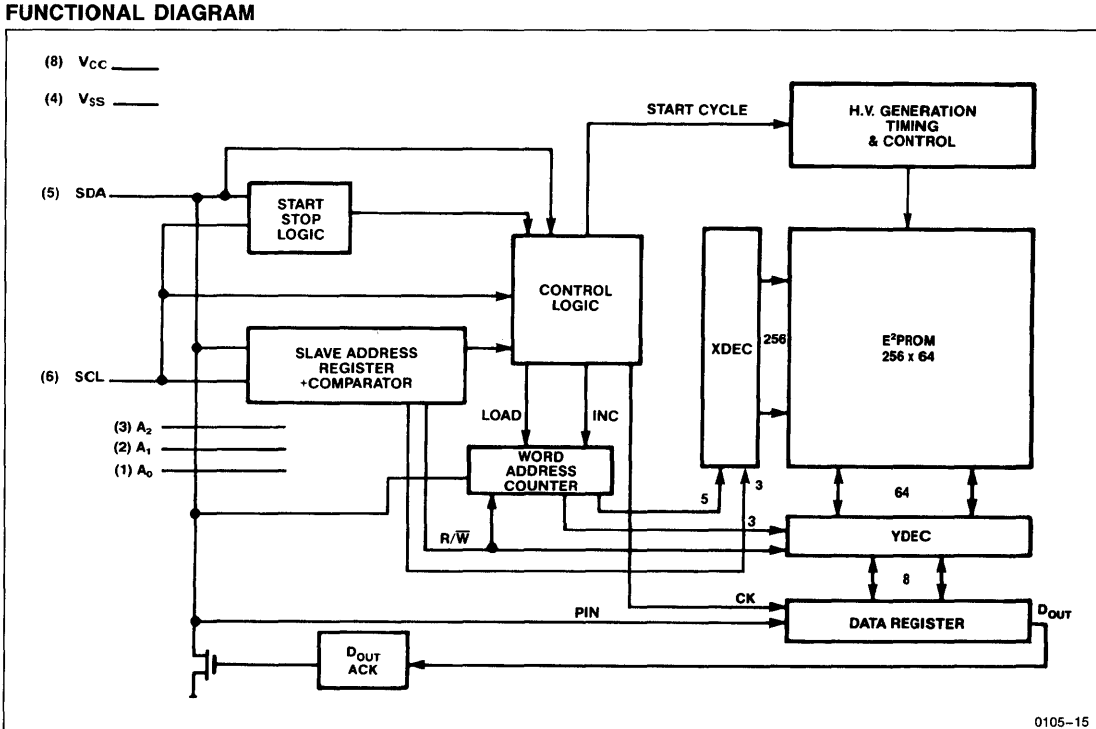


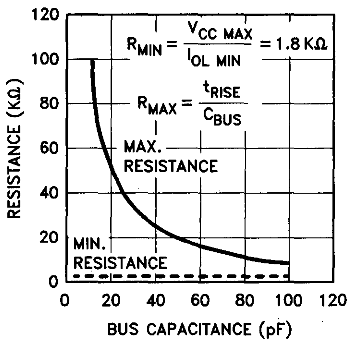
Figure 10: Typical System Configuration



FUNCTIONAL DIAGRAM



Guidelines for Calculating Typical Values of Bus Pull-Up Resistors



0105-16

ORDERING INFORMATION

SERIAL E2PROMs

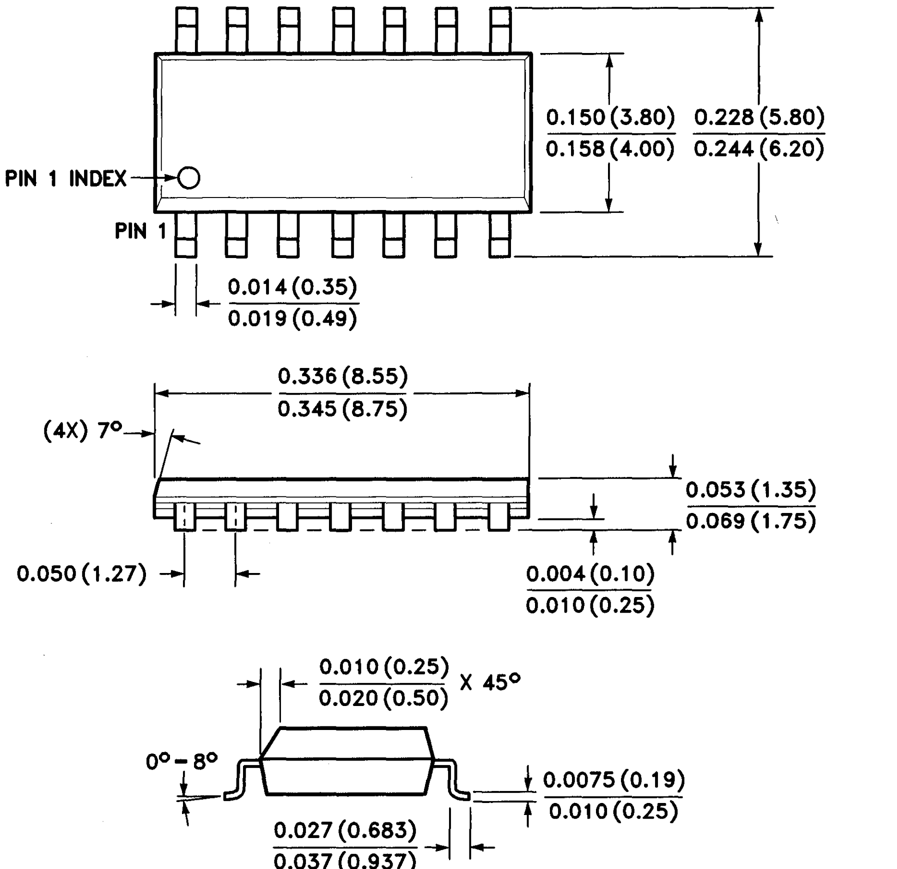
Device Order Number	Organization	Package										Temp. Range	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G			
X24LC16S	2048 x 8	•										†	CMOS	Standard
X24LC16SI	2048 x 8	•										I	CMOS	Standard
X24LC16P	2048 x 8		•									†	CMOS	Standard
X24LC16PI	2048 x 8		•									I	CMOS	Standard
X24LC16D	2048 x 8			•								†	CMOS	Standard
X24LC16DI	2048 x 8			•								I	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 14-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = 8-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

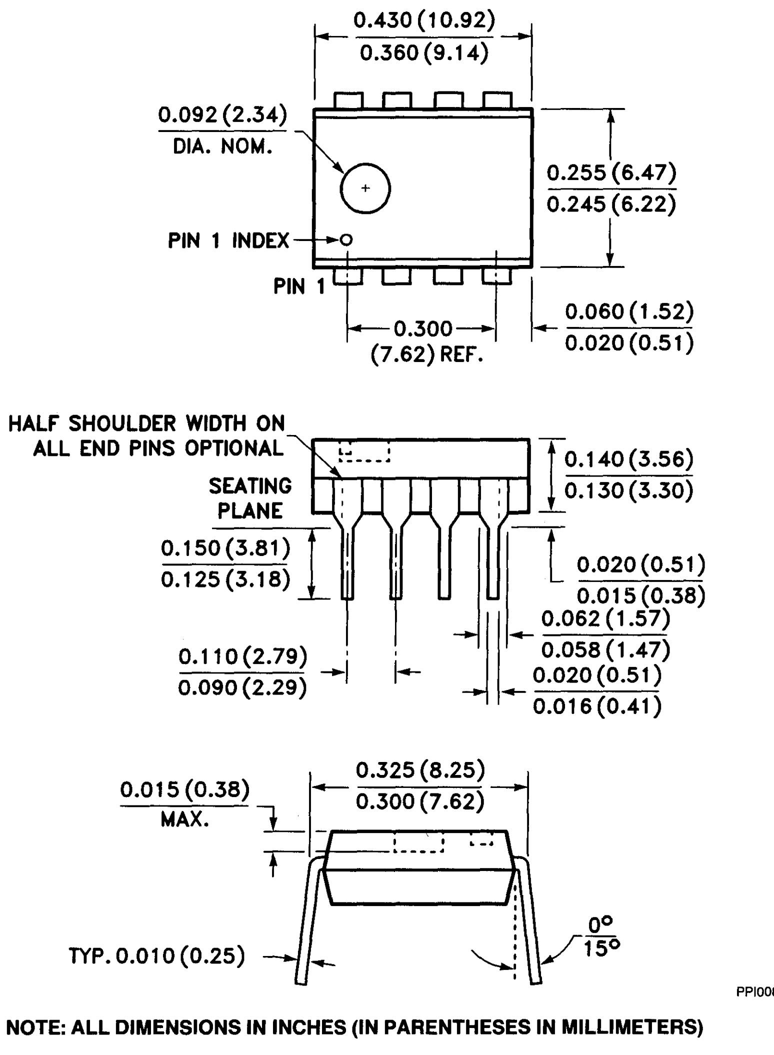
14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

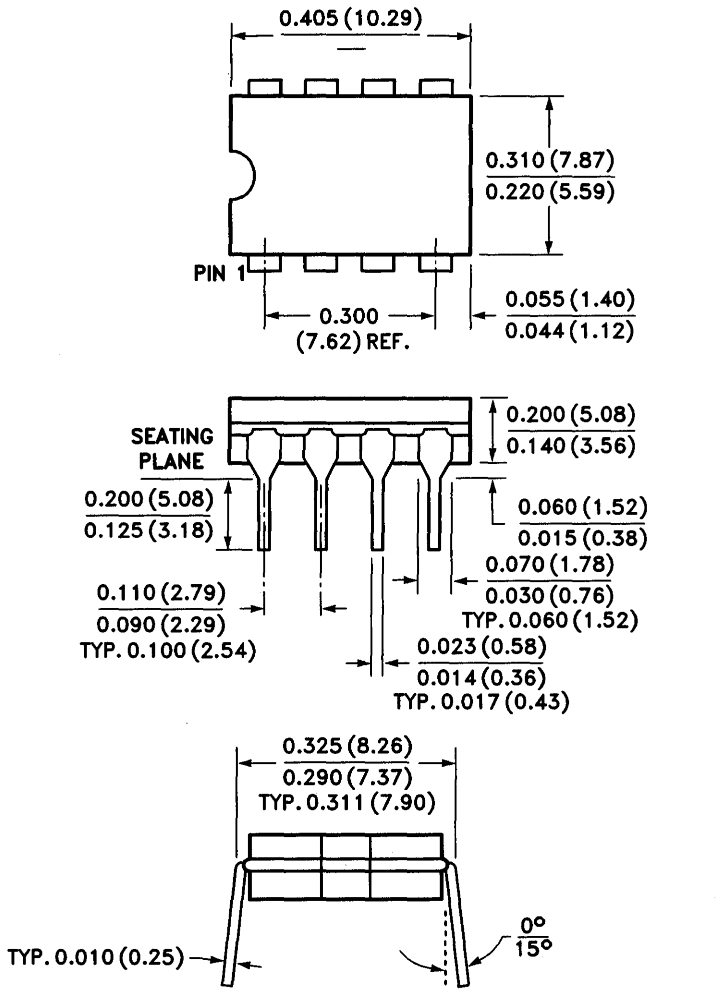
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

NOTES

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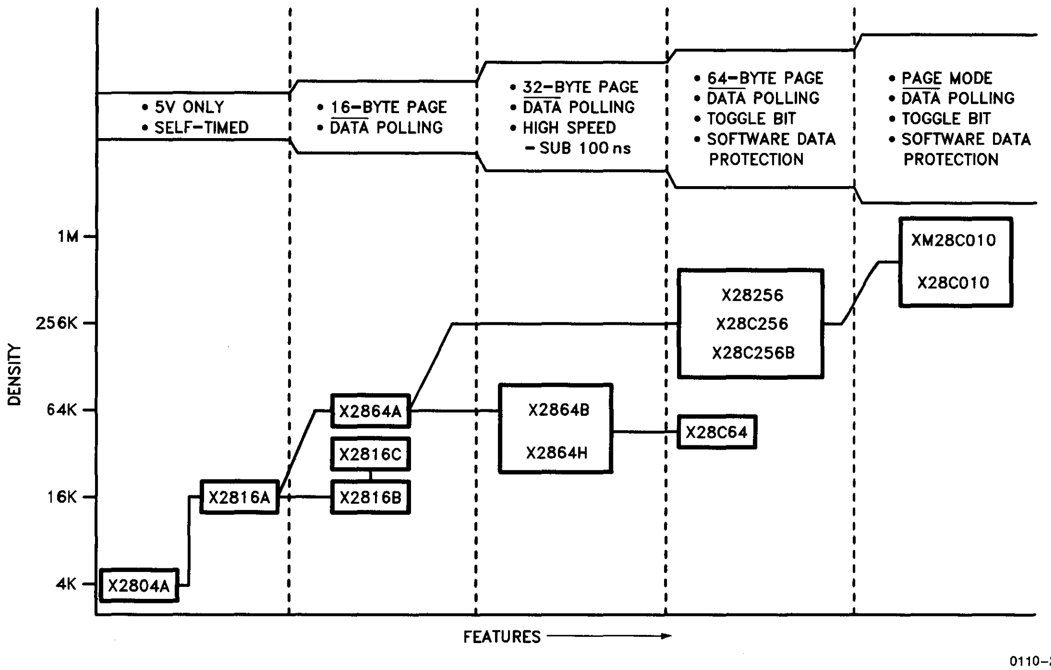
E²PROM GENEALOGY



Please use this Xicor Data Book Supplement in conjunction with the Xicor 1988 Data Book, Stock No. 100-080, which contains additional product line information, product reliability reports and application notes.

16K | Commercial Industrial | X2816C X2816CI | 2048 x 8 Bit

Electrically Erasable PROM

FEATURES

- 200 ns Access Time
- High Performance Advanced NMOS Technology
- Fast Write Cycle Times
  - —16-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 640 ms Typical
  - —Effective Byte Write Cycle Time of 300 μs Typical
- $\overline{\text{DATA}}$ Polling
  - —Allows User to Minimize Write Cycle Time
- Simple Byte and Page Write
  - —Single TTL Level $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout
- Inherent 100+ Years Data Retention

DESCRIPTION

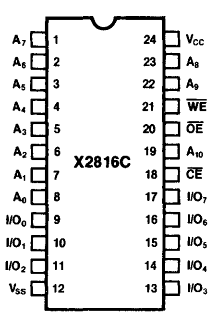
The Xicor X2816C is a 2K x 8 E^{2}PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2816C features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2816C supports a 16-byte page write operation, typically providing a 300 μs/byte write cycle, enabling the entire memory to be written in less than 640 ms. The X2816C also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance.

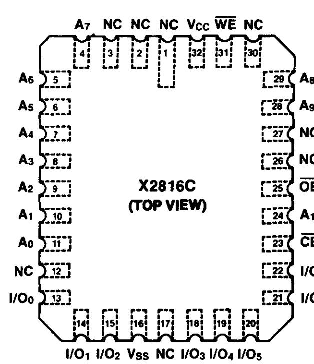
PIN CONFIGURATIONS

PLASTIC



0108-1

PLCC



0108-2

PIN NAMES

A_0–A_{10}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2816C .... −10°C to +85°C
X2816CI .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2816C T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2816CI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	120	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		45	60	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

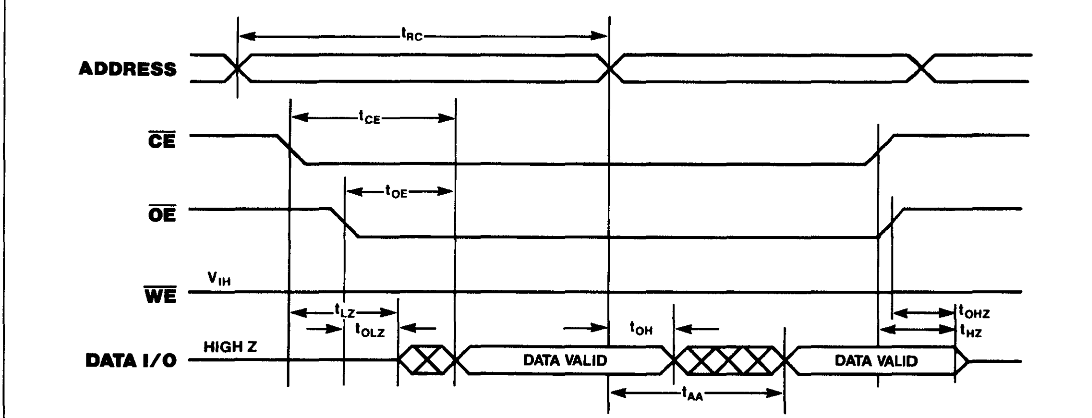
A.C. CHARACTERISTICS

X2816C T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X2816CI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	200		ns
t_{CE}	Chip Enable Access Time		200	ns
t_{AA}	Address Access Time		200	ns
t_{OE}	Output Enable Access Time		100	ns
$t_{LZ}^{(4)}$	Chip Enable to Output in Low Z	10		ns
$t_{HZ}^{(5)}$	Chip Disable to Output in High Z	10	60	ns
$t_{OLZ}^{(4)}$	Output Enable to Output in Low Z	10		ns
$t_{OHZ}^{(5)}$	Output Disable to Output in High Z	10	60	ns
t_{OH}	Output Hold from Address Change	10		ns

Read Cycle



0108-4

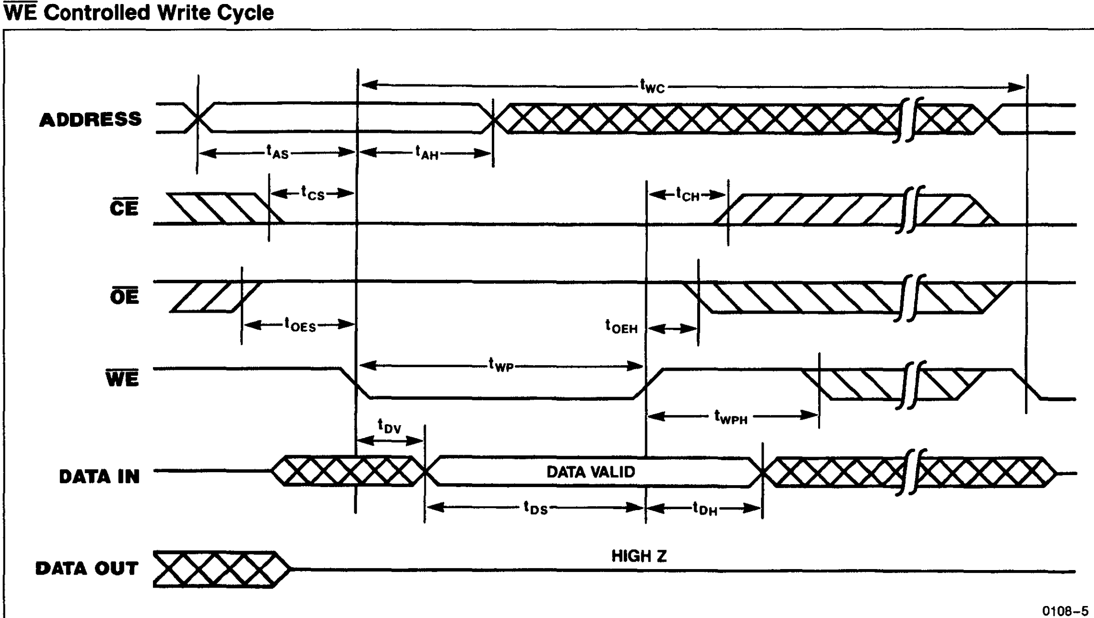
Notes: (4) t_{LZ} min. and t_{OLZ} min. are periodically sampled and not 100% tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are periodically sampled and not 100% tested.

Write Cycle Limits

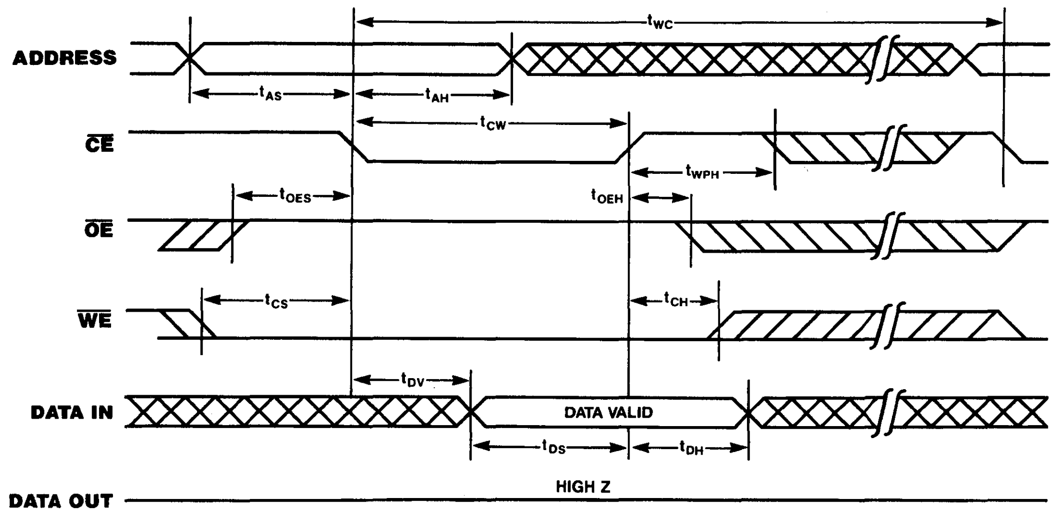
Symbol	Parameter	Min.	Typ.[6]	Max.	Units
t_{WC}[7]	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	10			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	150			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	150			ns
t_{WPH}	$\overline{WE}$ High Recovery	50			ns
t_{DV}	Data Valid			300	ns
t_{DS}	Data Setup	100			ns
t_{DH}	Data Hold	15			ns
t_{DW}	Delay to Next Write	500			μs
t_{BLC}	Byte Load Cycle	3		20	μs

$\overline{WE}$ Controlled Write Cycle

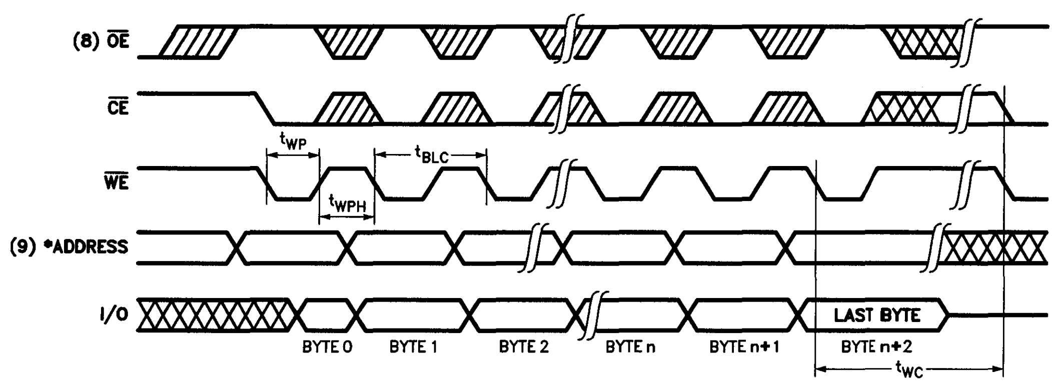


Notes: (6) Typical values are for T_A = 25°C and nominal supply voltage.
(7) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

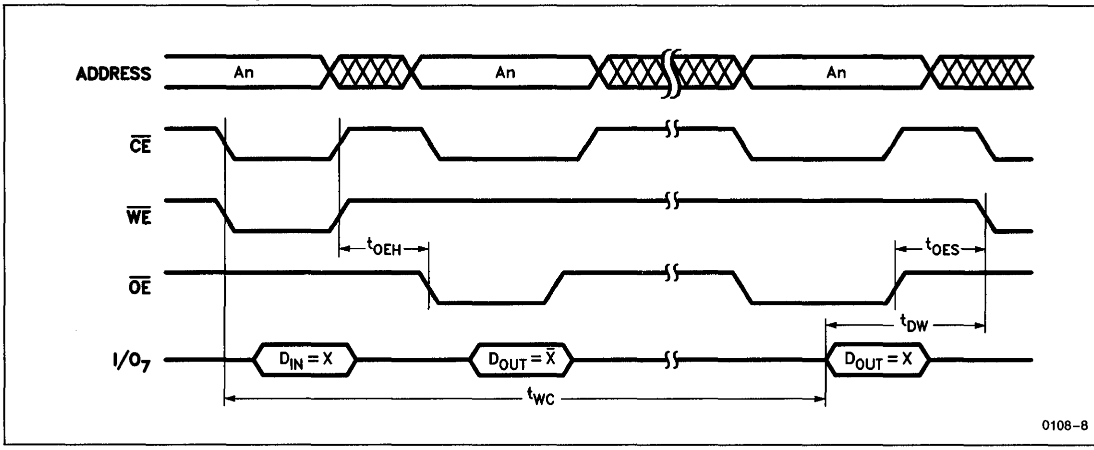


*For each successive write within the page write operation, A_4–A_{10} should be the same or writes to an unknown address could occur.

Notes: (8) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(10)



Note: (10) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PIN DESCRIPTIONS

Addresses (A_0–A_{10})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2816C through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2816C.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2816C supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

The page write feature of the X2816C allows the entire memory to be typically written in 640 ms. Page write allows two to sixteen bytes of data to be consecutively written to the X2816C prior to the commencement of the internal programming cycle. Although the host system may read data from any location in the system to transfer to the X2816C, the destination page address of the X2816C should be the same on each subsequent strobe of the $\overline{WE}$ and $\overline{CE}$ inputs. That is, A_4 through A_{10} must be the same for each transfer of data to the X2816C during a page write cycle.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to fifteen bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 20 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 20 μs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 20 μs.

$\overline{DATA}$ Polling

The X2816C features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2816C, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are three features that protect the nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse which is typically less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V, typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes. Write cycle timing specifications must be observed concurrently.

ENDURANCE

Xicor E^2PROMs are designed and tested for applications requiring extended endurance.

SYSTEM CONSIDERATIONS

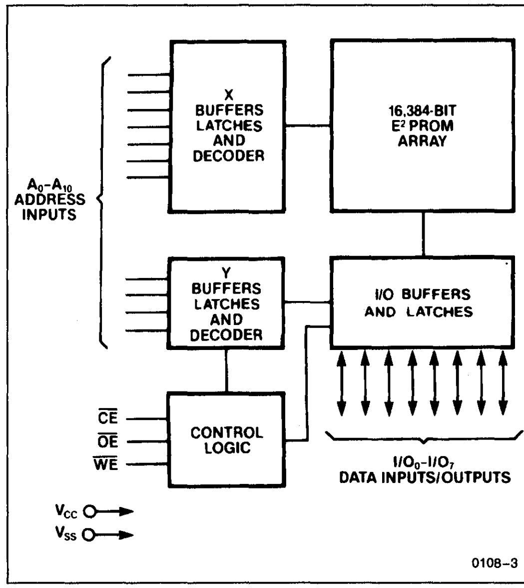
Because the X2816C is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

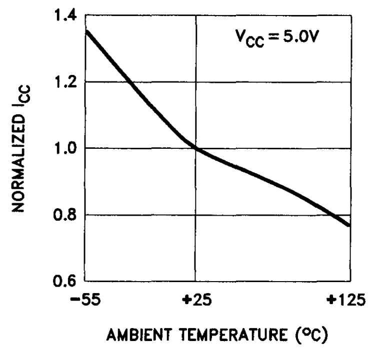
Because the X2816C has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM

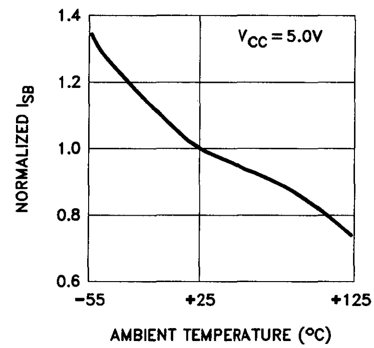


Normalized Active Supply Current vs. Ambient Temperature



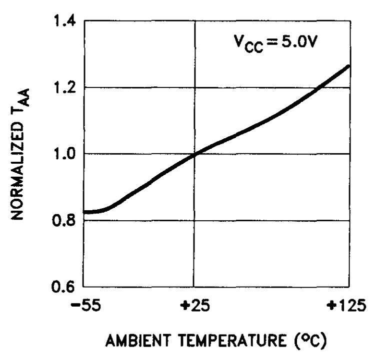
0108-9

Normalized Standby Supply Current vs. Ambient Temperature



0108-10

Normalized Access Time vs. Ambient Temperature



0108-11

ORDERING INFORMATION

16K E²PROMs

Device Order Number	Organization	Package S	P	D	C	F1	F2	K	J	E	G	Temp. Range	Access Time	Process Technology	Processing Level
X2816CP-20	2048 x 8		●									†	200 ns	NMOS	Standard
X2816CPI-20	2048 x 8		●									I	200 ns	NMOS	Standard
X2816CJ-20	2048 x 8								●			†	200 ns	NMOS	Standard
X2816CJI-20	2048 x 8								●			I	200 ns	NMOS	Standard

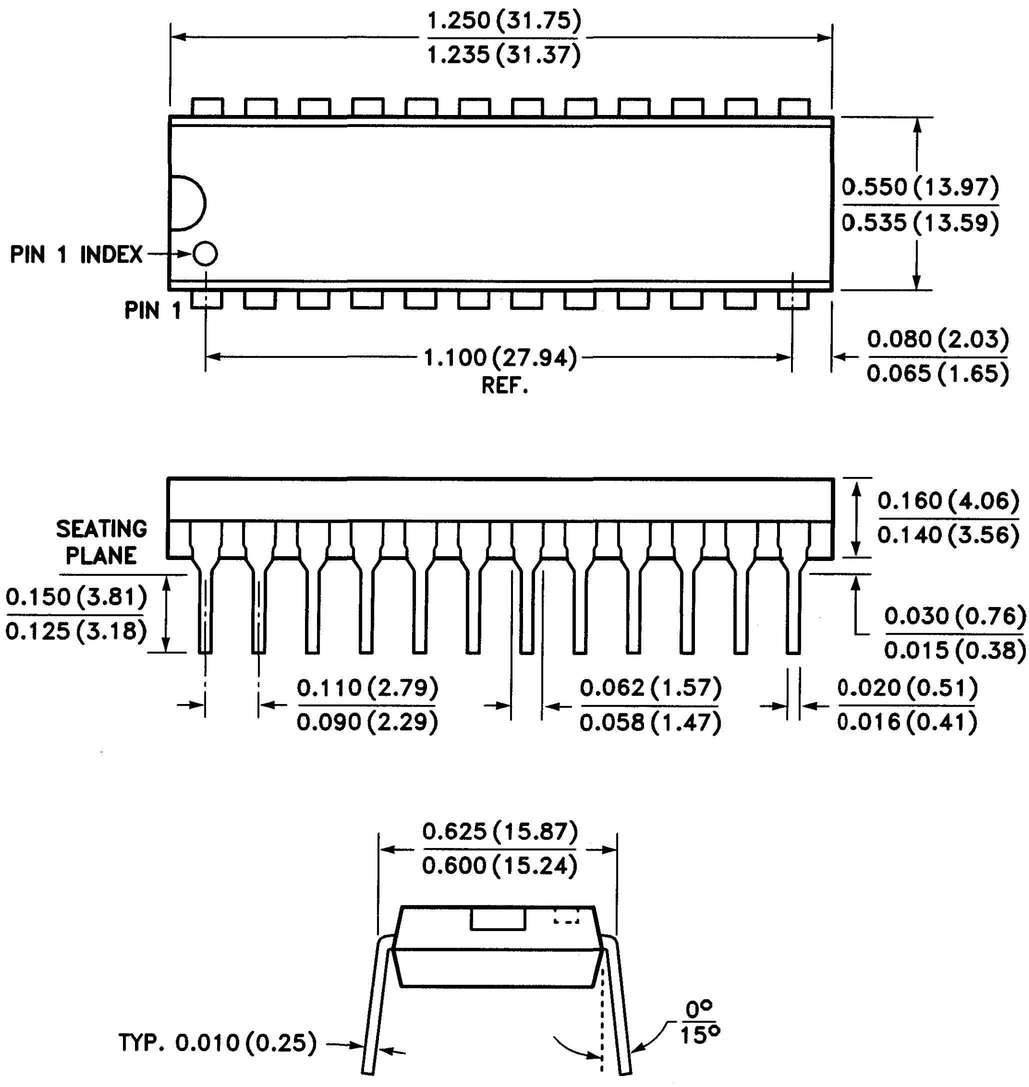
Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = 24-Lead Plastic DIP
D = Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

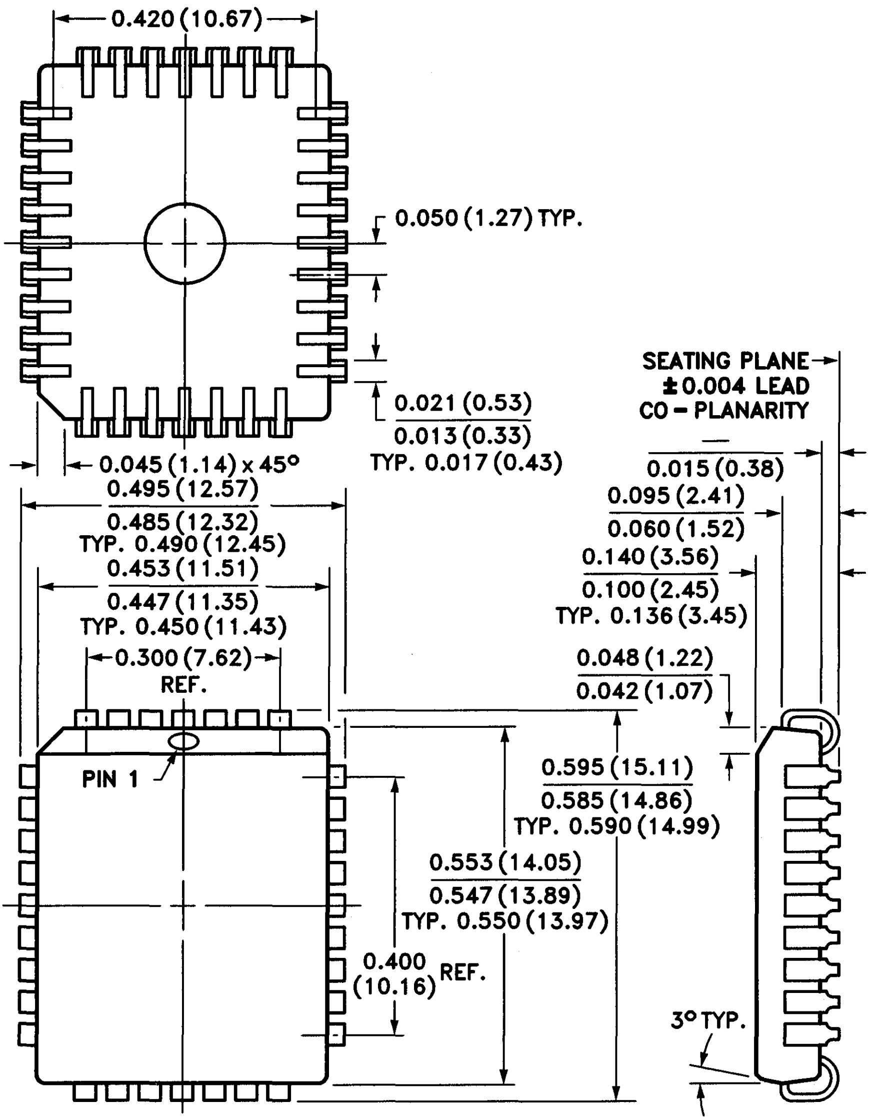
24-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



PJG032

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

NOTES

NOTES

NOTES

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64K | Commercial / Industrial | X2864B / X2864BI | 8192 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **120 ns Access Time**
- **High Performance Scaled NMOS Technology**
- **Fast Write Cycle Times**
  - **—32-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 3 ms Typical**
  - **—Complete Memory Rewrite: 750 ms Typical**
  - **—Effective Byte Write Cycle Time of 95 μs Typical**
- **$\overline{\text{DATA}}$ Polling**
  - **—Allows User to Minimize Write Cycle Time**
- **Simple Byte and Page Write**
  - **—Single TTL Level $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

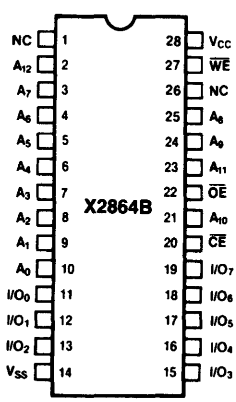
The Xicor X2864B is a 8K x 8 E^2PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864B supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

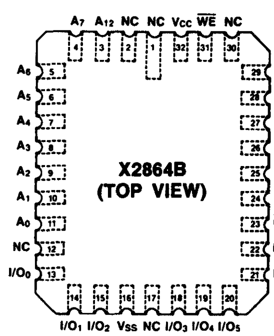
PIN CONFIGURATIONS

PLASTIC
CERDIP
FLAT PACK



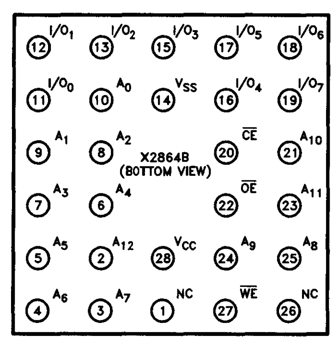
0031-1

PLCC
LCC



0031-2

PGA



0031-11

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X2864B .... $-10°C$ to $+85°C$
X2864BI .... $-65°C$ to $+135°C$
Storage Temperature .... $-65°C$ to $+150°C$
Voltage on any Pin with
Respect to Ground .... $-1.0V$ to $+7V$
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864B $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified.
X2864BI $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	150	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50	80	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	-1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		$V_{CC} + 1.0$	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
C_{IN}(3)	Input Capacitance	6	pF	$V_{IN} = 0V$

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and $C_L = 100$ pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

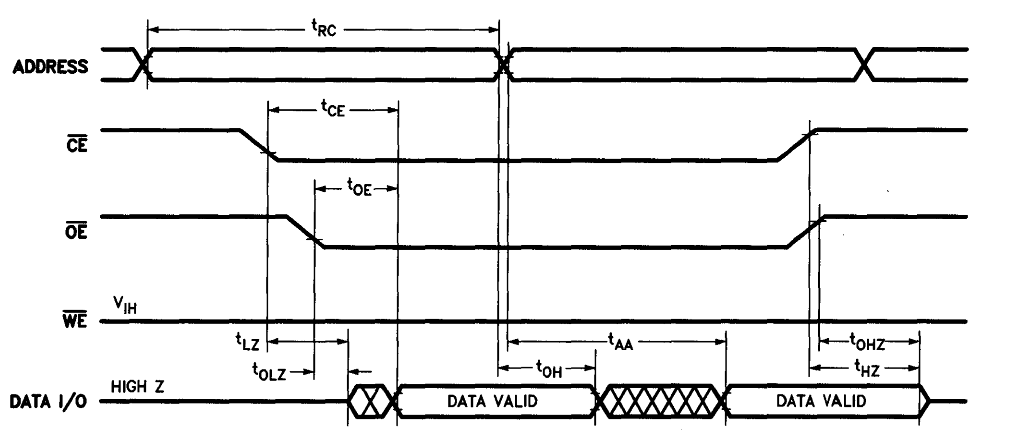
A.C. CHARACTERISTICS

X2864B T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2864B-12 X2864BI-12		X2864B-15 X2864BI-15		X2864B-18 X2864BI-18		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		180		ns
t_{CE}	Chip Enable Access Time		120		150		180	ns
t_{AA}	Address Access Time		120		150		180	ns
t_{OE}	Output Enable Access Time		50		70		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Read Cycle



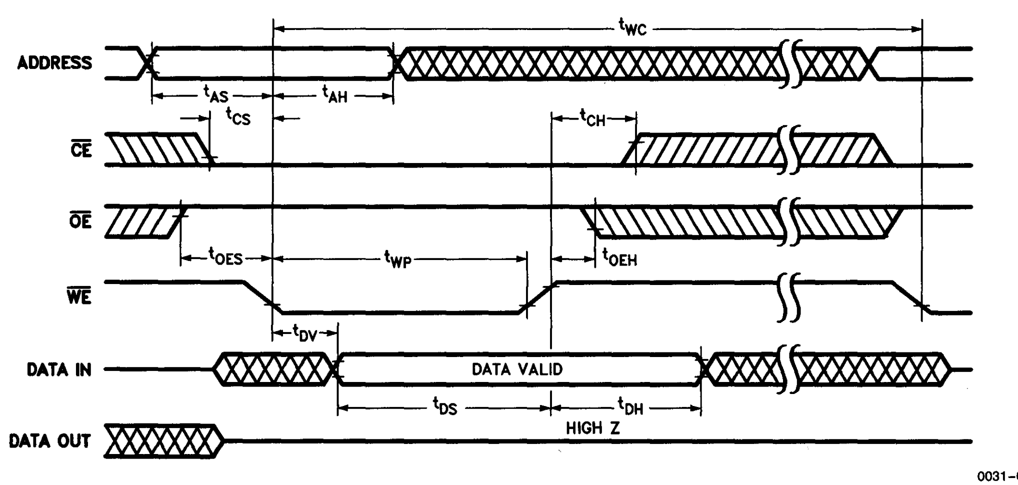
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

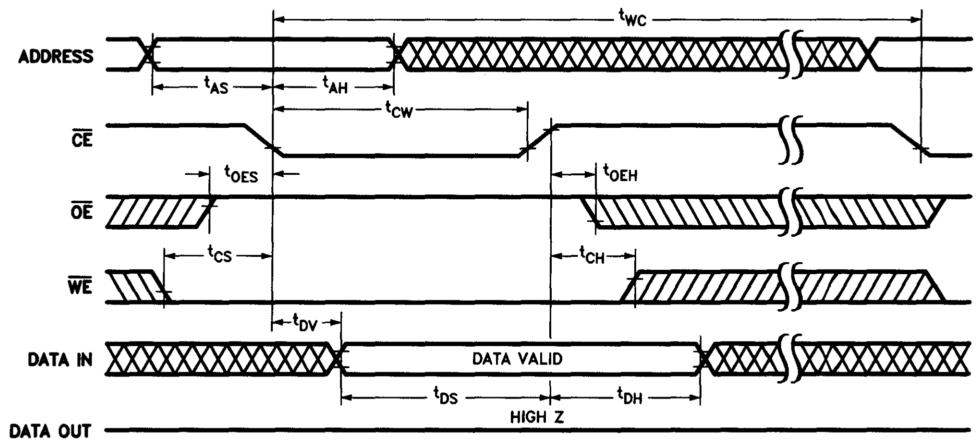
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	5			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	50			ns
t_{DV}	Data Valid			100	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	5			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle



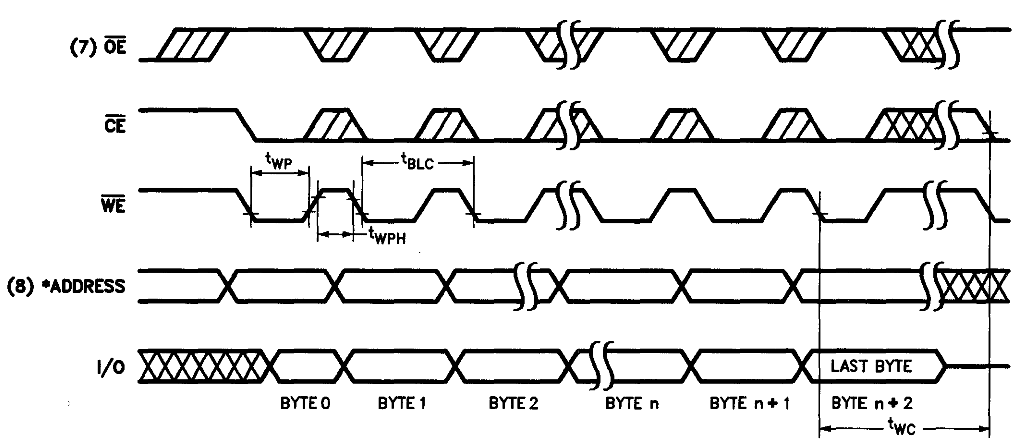
Note: (6) Typical values are for T_A = 25°C and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



0031-7

Page Mode Write Cycle



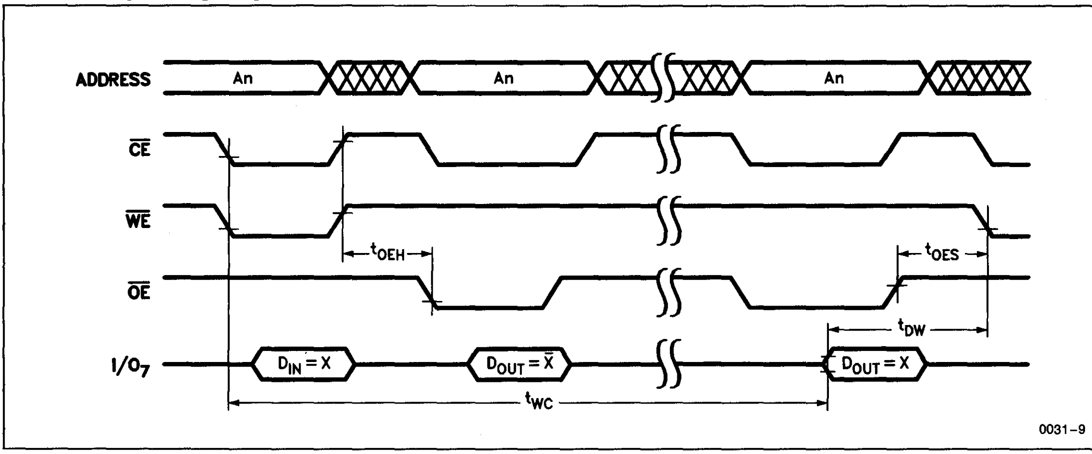
0031-8

*For each successive write within the page write operation, A_5–A_{12} should be the same or writes to an unknown address could occur.

Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g., this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

DATA Polling Timing Diagram(9)



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2864B through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2864B.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864B supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation

The page write feature of the X2864B allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864B prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_5 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide so long as the host continues to access the device within the byte load cycle time of 100 μs.

$\overline{DATA}$ Polling

The X2864B features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are two features that protect the nonvolatile data from inadvertent writes.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3.5V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

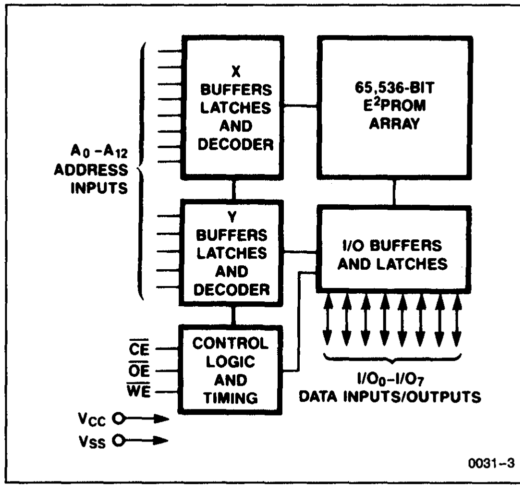
Because the X2864B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

64K E^2PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BP-12	8192 x 8		•									†	120 ns	NMOS	Standard
X2864BP-15	8192 x 8		•									†	150 ns	NMOS	Standard
X2864BP-18	8192 x 8		•									†	180 ns	NMOS	Standard
X2864BPI-12	8192 x 8		•									I	120 ns	NMOS	Standard
X2864BPI-15	8192 x 8		•									I	150 ns	NMOS	Standard
X2864BPI-18	8192 x 8		•									I	180 ns	NMOS	Standard
X2864BD-12	8192 x 8			•								†	120 ns	NMOS	Standard
X2864BD-15	8192 x 8			•								†	150 ns	NMOS	Standard
X2864BD-18	8192 x 8			•								†	180 ns	NMOS	Standard
X2864BDI-12	8192 x 8			•								I	120 ns	NMOS	Standard
X2864BDI-15	8192 x 8			•								I	150 ns	NMOS	Standard
X2864BDI-18	8192 x 8			•								I	180 ns	NMOS	Standard
X2864BF-12	8192 x 8					•						†	120 ns	NMOS	Standard
X2864BF-15	8192 x 8					•						†	150 ns	NMOS	Standard
X2864BF-18	8192 x 8					•						†	180 ns	NMOS	Standard
X2864BFI-12	8192 x 8					•						I	120 ns	NMOS	Standard
X2864BFI-15	8192 x 8					•						I	150 ns	NMOS	Standard
X2864BFI-18	8192 x 8					•						I	180 ns	NMOS	Standard

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BK-12	8192 x 8							•				†	120 ns	NMOS	Standard
X2864BK-15	8192 x 8							•				†	150 ns	NMOS	Standard
X2864BK-18	8192 x 8							•				†	180 ns	NMOS	Standard
X2864BKI-12	8192 x 8							•				I	120 ns	NMOS	Standard
X2864BKI-15	8192 x 8							•				I	150 ns	NMOS	Standard
X2864BKI-18	8192 x 8							•				I	180 ns	NMOS	Standard
X2864BJ-12	8192 x 8								•			†	120 ns	NMOS	Standard
X2864BJ-15	8192 x 8								•			†	150 ns	NMOS	Standard
X2864BJ-18	8192 x 8								•			†	180 ns	NMOS	Standard
X2864BJI-12	8192 x 8								•			I	120 ns	NMOS	Standard
X2864BJI-15	8192 x 8								•			I	150 ns	NMOS	Standard
X2864BJI-18	8192 x 8								•			I	180 ns	NMOS	Standard
X2864BE-12	8192 x 8									•		†	120 ns	NMOS	Standard
X2864BE-15	8192 x 8									•		†	150 ns	NMOS	Standard
X2864BE-18	8192 x 8									•		†	180 ns	NMOS	Standard
X2864BEI-12	8192 x 8									•		I	120 ns	NMOS	Standard
X2864BEI-15	8192 x 8									•		I	150 ns	NMOS	Standard
X2864BEI-18	8192 x 8									•		I	180 ns	NMOS	Standard

Key:

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E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E^{2}PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BG-12	8192 x 8										•	†	120 ns	NMOS	Standard
X2864BG-15	8192 x 8										•	†	150 ns	NMOS	Standard
X2864BG-18	8192 x 8										•	†	180 ns	NMOS	Standard
X2864BGI-12	8192 x 8										•	I	120 ns	NMOS	Standard
X2864BGI-15	8192 x 8										•	I	150 ns	NMOS	Standard
X2864BGI-18	8192 x 8										•	I	180 ns	NMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
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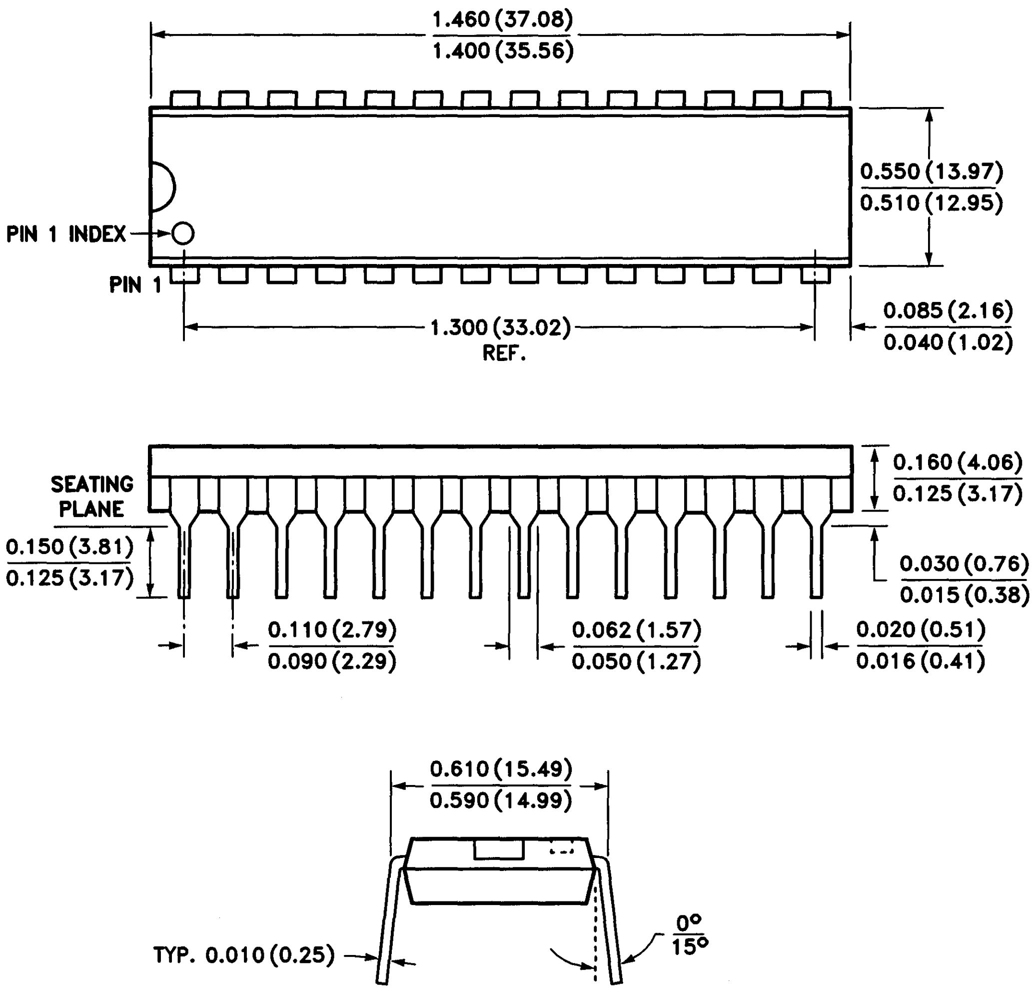
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

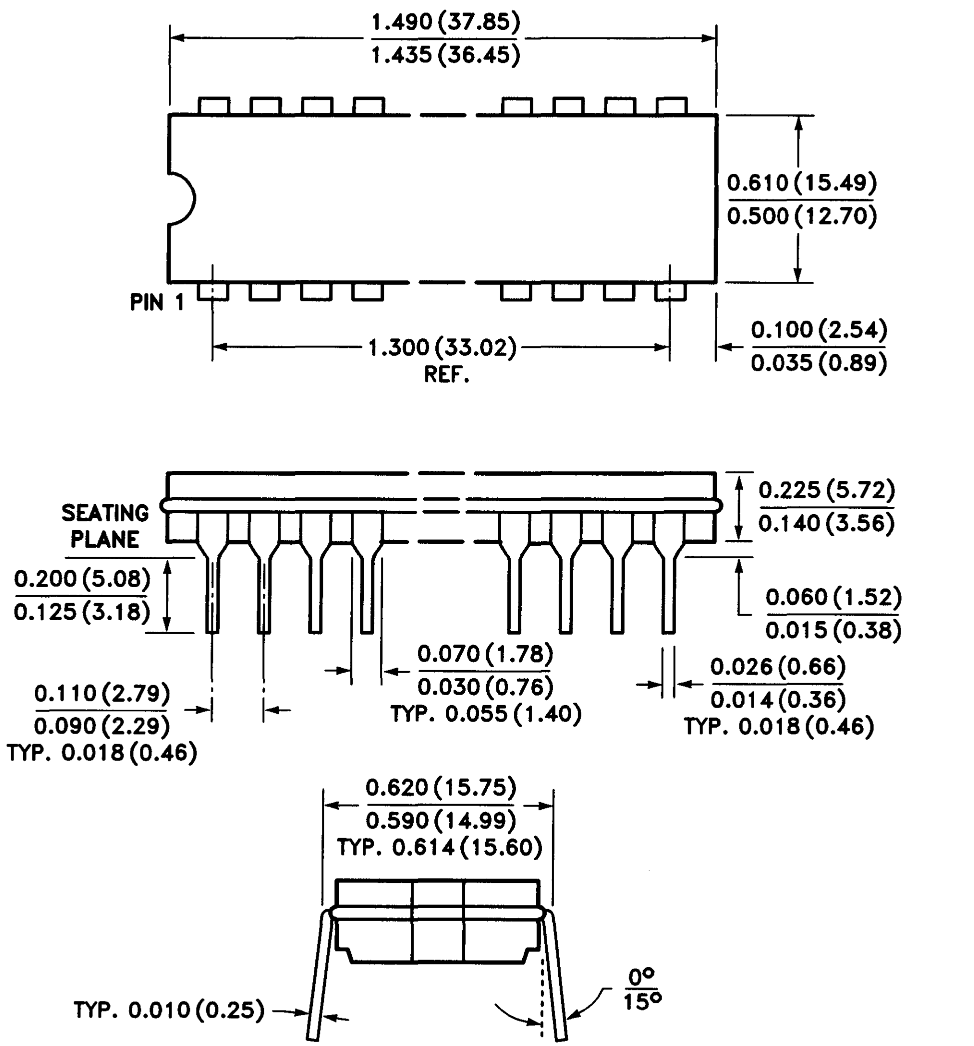
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

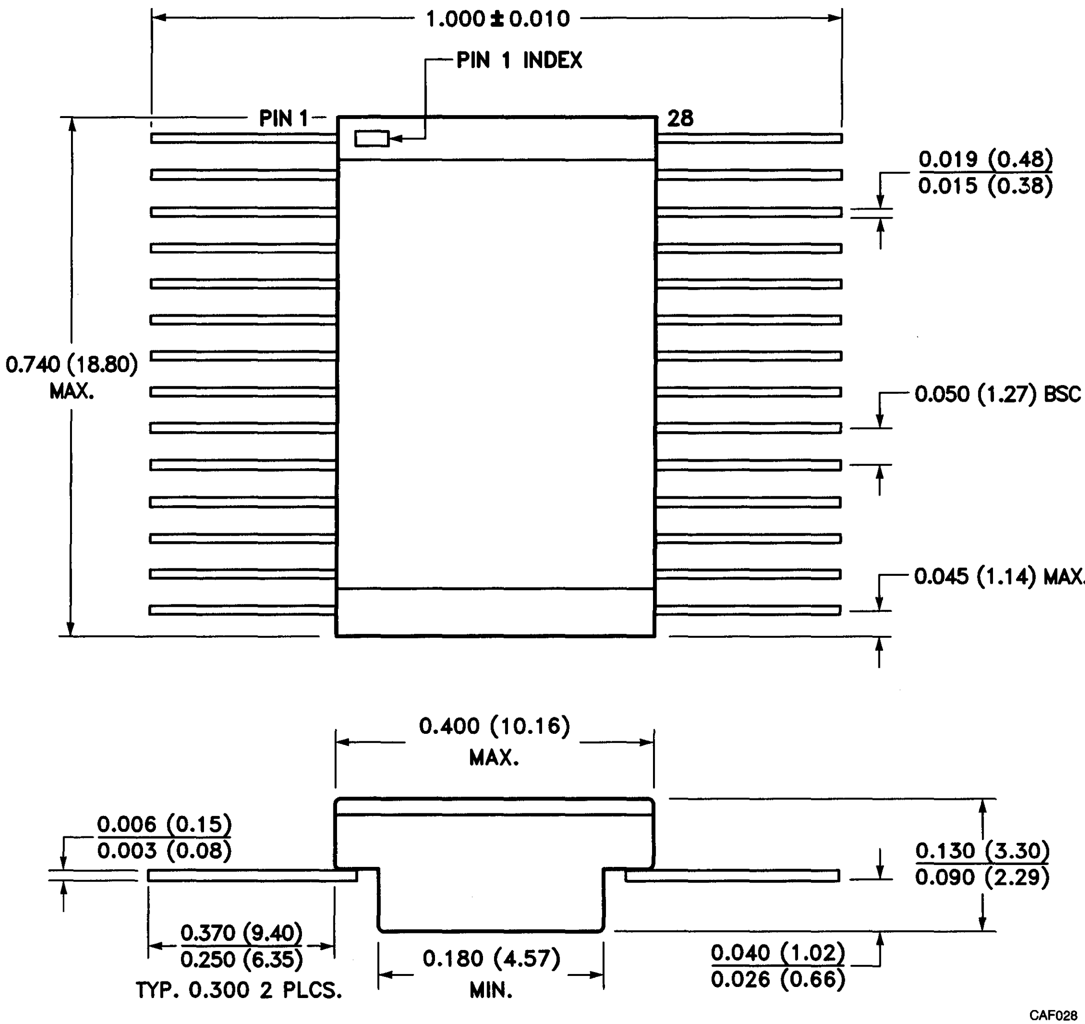
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

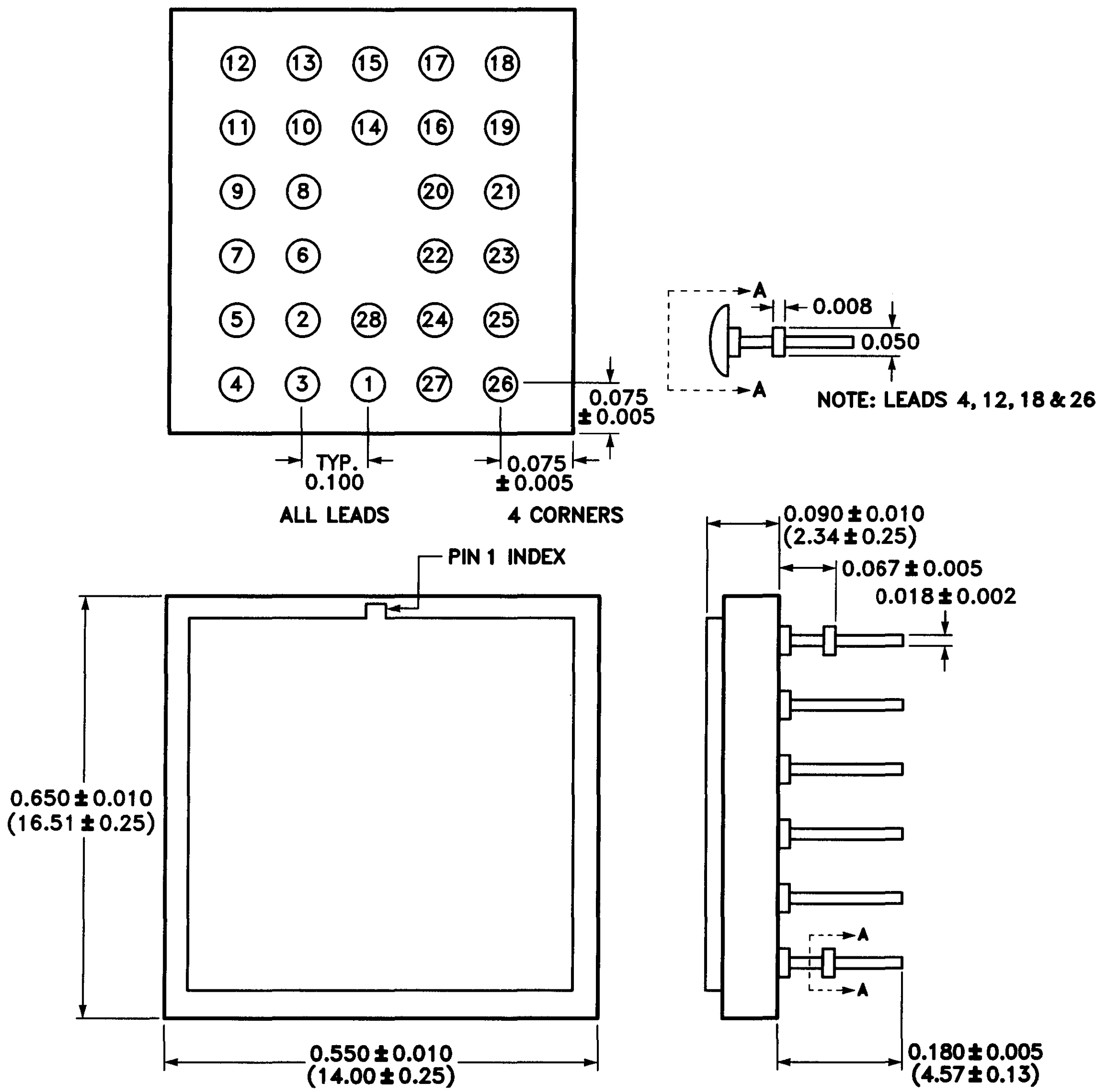
28-LEAD CERAMIC FLAT PACK TYPE F1



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H

PACKAGING INFORMATION

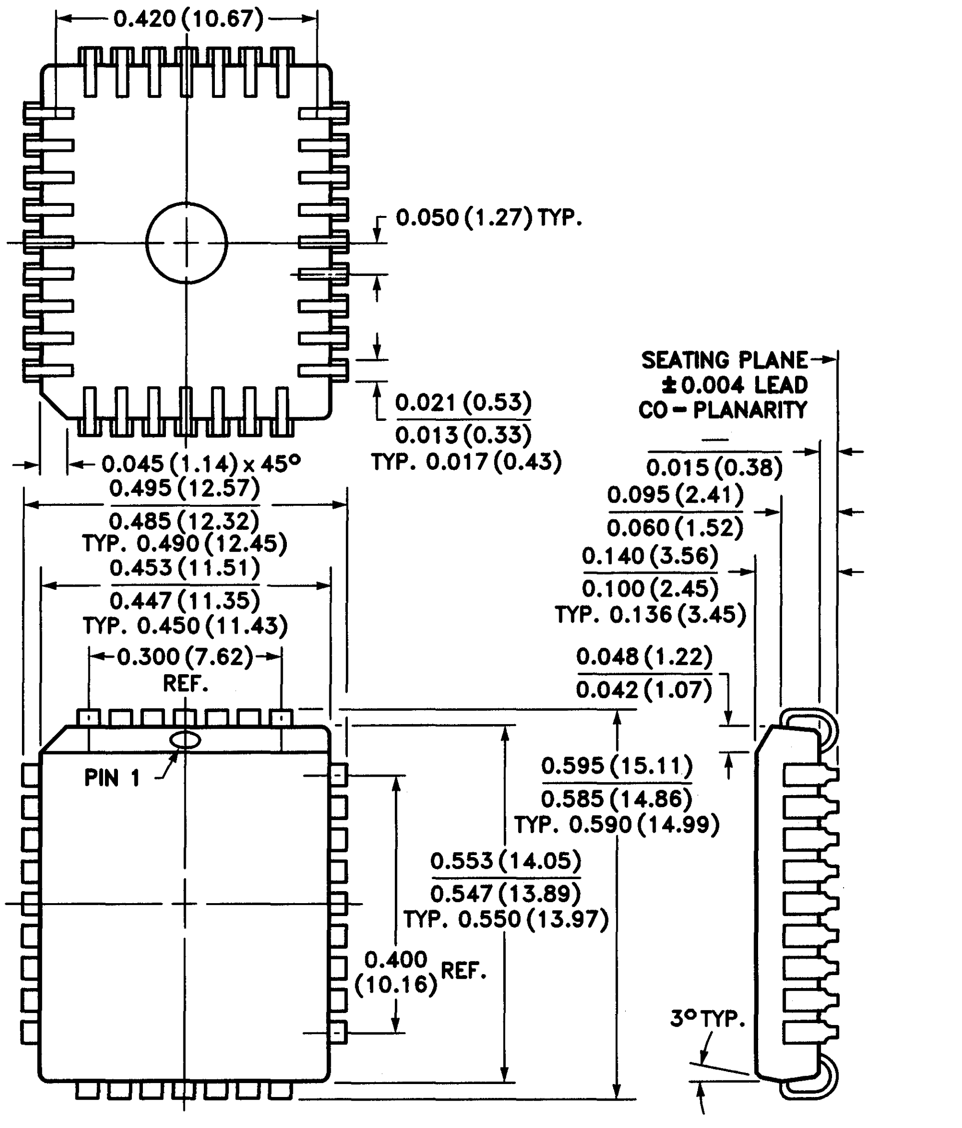
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

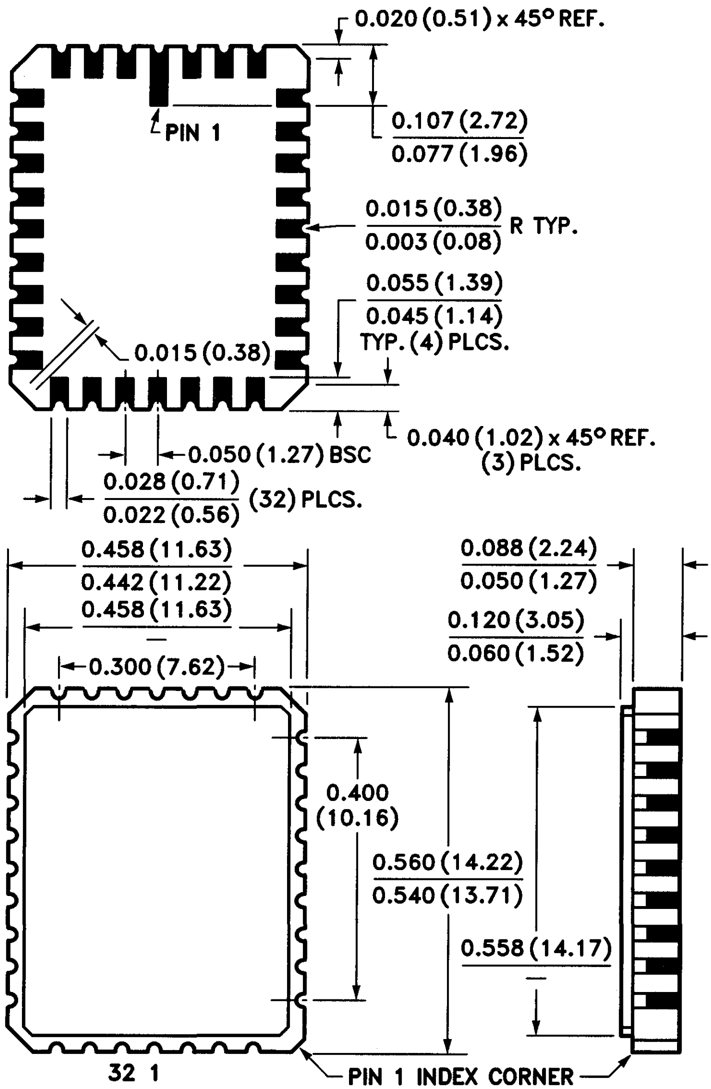
32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

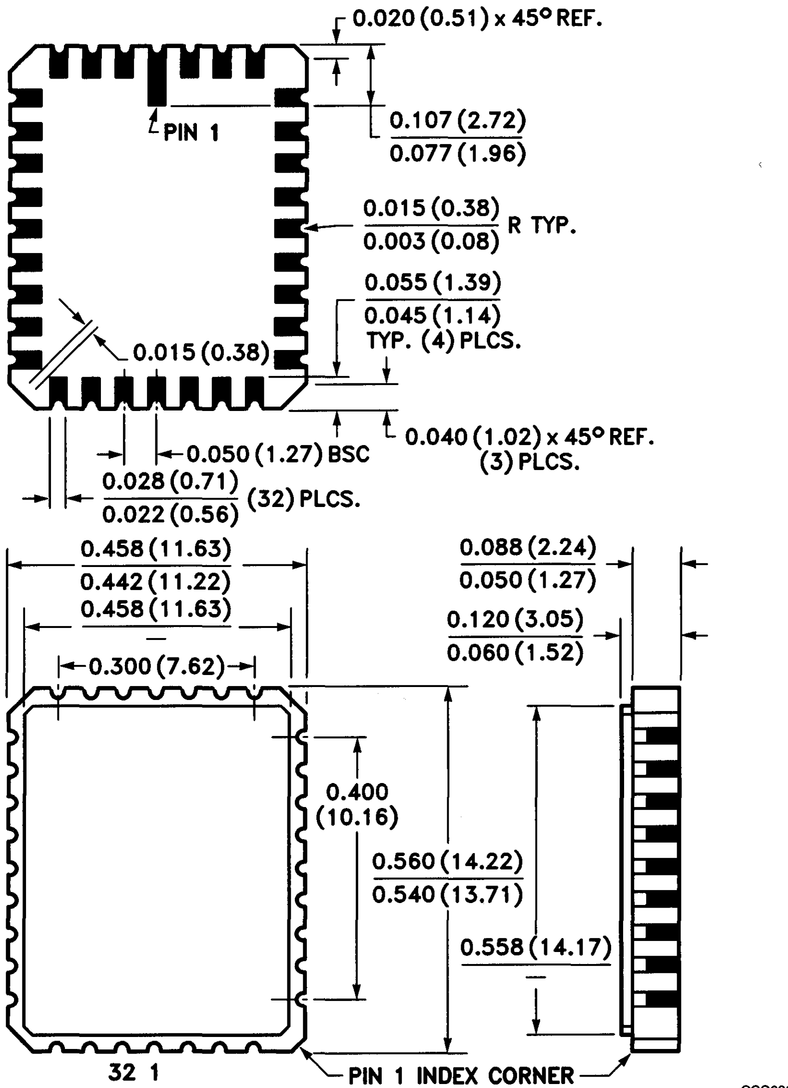


CEG032

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

NOTES

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U.S. Sales Offices

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Fax: 408/432-0640

8/88 Stock No. 200-177

64K Military X2864BM 8192 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **120 ns Access Time**
- **High Performance Scaled NMOS Technology**
- **Fast Write Cycle Times**
  - **—32-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 3 ms Typical**
  - **—Complete Memory Rewrite: 750 ms Typical**
  - **—Effective Byte Write Cycle Time of 95 μs Typical**
- **$\overline{\text{DATA}}$ Polling**
  - **—Allows User to Minimize Write Cycle Time**
- **Simple Byte and Page Write**
  - **—Single TTL Level $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

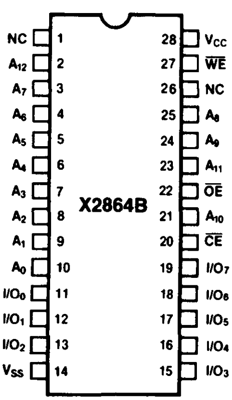
The Xicor X2864B is an 8K x 8 E^2PROM, fabricated with an advanced, high performance N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864B supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

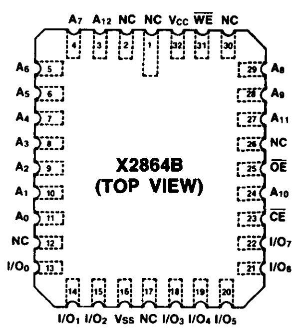
PIN CONFIGURATIONS

CERDIP
FLAT PACK



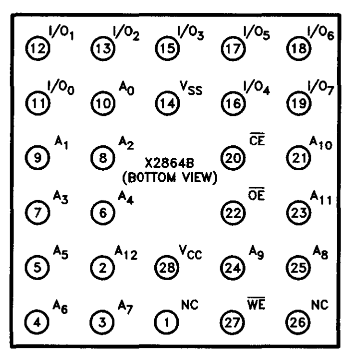
0032-1

LCC



0032-2

PGA



0032-9

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	150	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50	80	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		$V_{CC}+1.0$	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

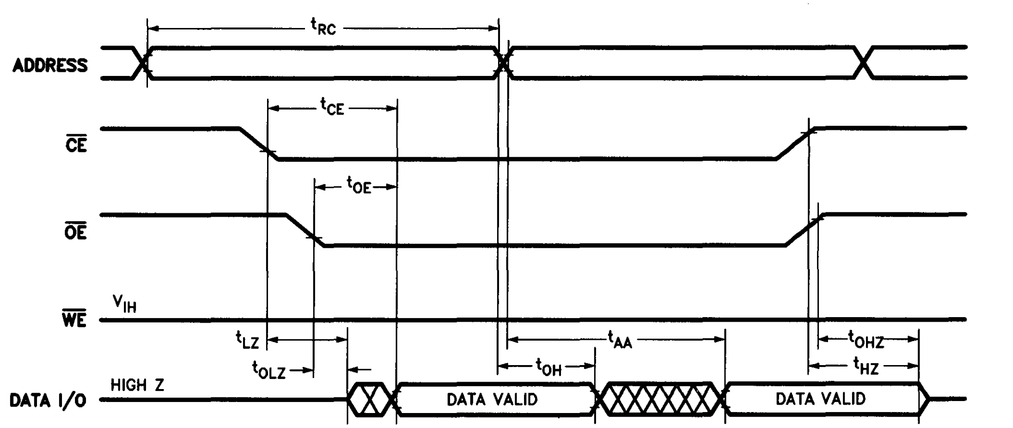
A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2864BM-12		X2864BM-15		X2864BM-18		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	120		150		180		ns
t_{CE}	Chip Enable Access Time		120		150		180	ns
t_{AA}	Address Access Time		120		150		180	ns
t_{OE}	Output Enable Access Time		50		70		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		ns

Read Cycle



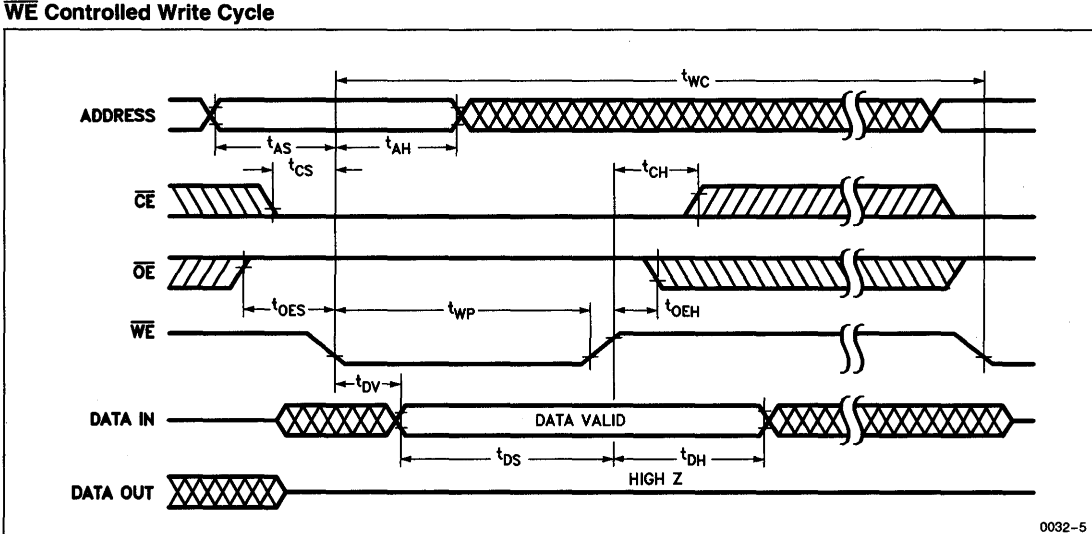
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

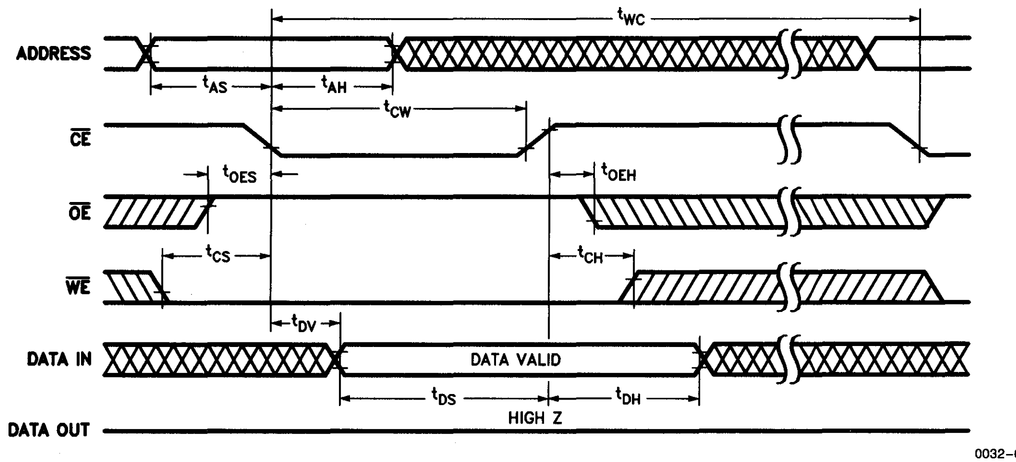
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	5			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	50			ns
t_{DV}	Data Valid			100	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	5			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle

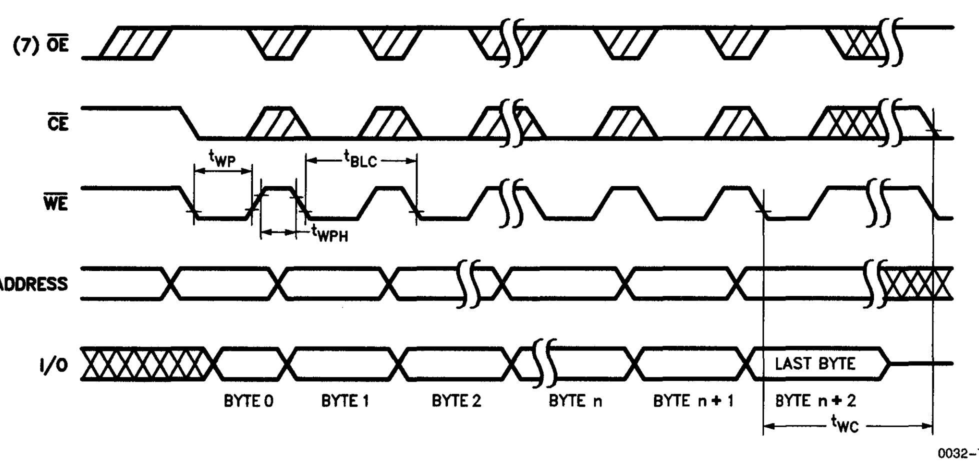


Note: (6) Typical values are for T_A = 25°C and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

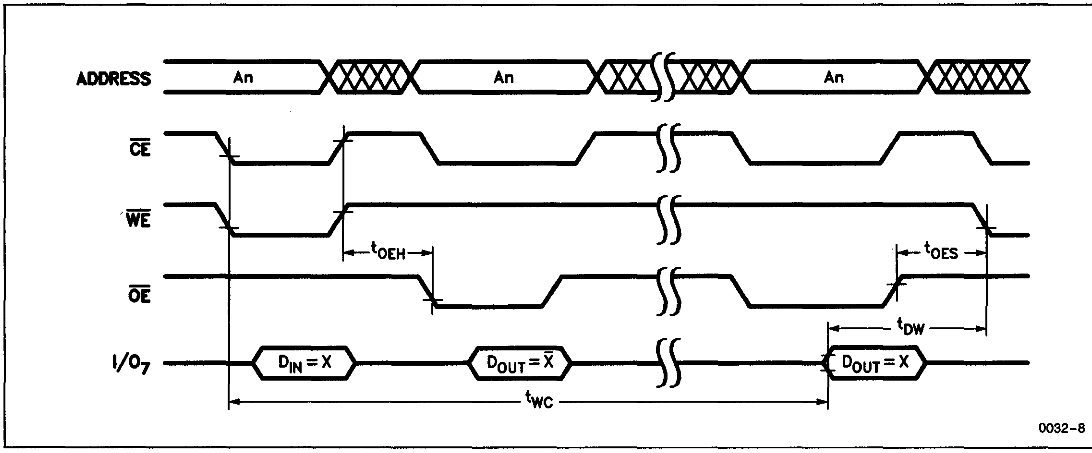


*For each successive write within the page write operation, A_5–A_{12} should be the same or writes to an unknown address could occur.

Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g., this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2864B through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2864B.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864B supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation

The page write feature of the X2864B allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864B prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_5 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. The page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

$\overline{DATA}$ Polling

The X2864B features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are two features that protect the nonvolatile data from inadvertent writes.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3.5V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

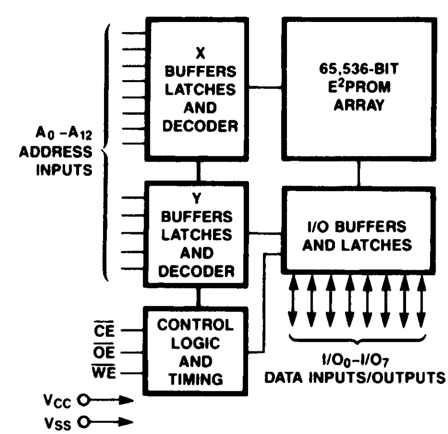
Because the X2864B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



0032-3

ORDERING INFORMATION

64K E²PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BDM-12	8192 x 8			•								M	120 ns	NMOS	Standard
X2864BDM-15	8192 x 8			•								M	150 ns	NMOS	Standard
X2864BDM-18	8192 x 8			•								M	180 ns	NMOS	Standard
X2864BDMB-12	8192 x 8			•								M	120 ns	NMOS	883 Rev. C, Class B
X2864BDMB-15	8192 x 8			•								M	150 ns	NMOS	883 Rev. C, Class B
X2864BDMB-18	8192 x 8			•								M	180 ns	NMOS	883 Rev. C, Class B
X2864BFM-12	8192 x 8					•						M	120 ns	NMOS	Standard
X2864BFM-15	8192 x 8					•						M	150 ns	NMOS	Standard
X2864BFM-18	8192 x 8					•						M	180 ns	NMOS	Standard
X2864BFMB-12	8192 x 8					•						M	120 ns	NMOS	883 Rev. C, Class B
X2864BFMB-15	8192 x 8					•						M	150 ns	NMOS	883 Rev. C, Class B
X2864BFMB-18	8192 x 8					•						M	180 ns	NMOS	883 Rev. C, Class B
X2864BKM-12	8192 x 8							•				M	120 ns	NMOS	Standard
X2864BKM-15	8192 x 8							•				M	150 ns	NMOS	Standard
X2864BKM-18	8192 x 8							•				M	180 ns	NMOS	Standard
X2864BKMB-12	8192 x 8							•				M	120 ns	NMOS	883 Rev. C, Class B
X2864BKMB-15	8192 x 8							•				M	150 ns	NMOS	883 Rev. C, Class B
X2864BKMB-18	8192 x 8							•				M	180 ns	NMOS	883 Rev. C, Class B
X2864BEM-12	8192 x 8									•		M	120 ns	NMOS	Standard
X2864BEM-15	8192 x 8									•		M	150 ns	NMOS	Standard
X2864BEM-18	8192 x 8									•		M	180 ns	NMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864BEMB-12	8192 x 8									•		M	120 ns	NMOS	883 Rev. C, Class B
X2864BEMB-15	8192 x 8									•		M	150 ns	NMOS	883 Rev. C, Class B
X2864BEMB-18	8192 x 8									•		M	180 ns	NMOS	883 Rev. C, Class B
X2864BGM-12	8192 x 8										•	M	120 ns	NMOS	Standard
X2864BGM-15	8192 x 8										•	M	150 ns	NMOS	Standard
X2864BGM-18	8192 x 8										•	M	180 ns	NMOS	Standard
X2864BGMB-12	8192 x 8										•	M	120 ns	NMOS	883 Rev. C, Class B
X2864BGMB-15	8192 x 8										•	M	150 ns	NMOS	883 Rev. C, Class B
X2864BGMB-18	8192 x 8										•	M	180 ns	NMOS	883 Rev. C, Class B

Key:

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I = Industrial = −40°C to +85°C
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F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
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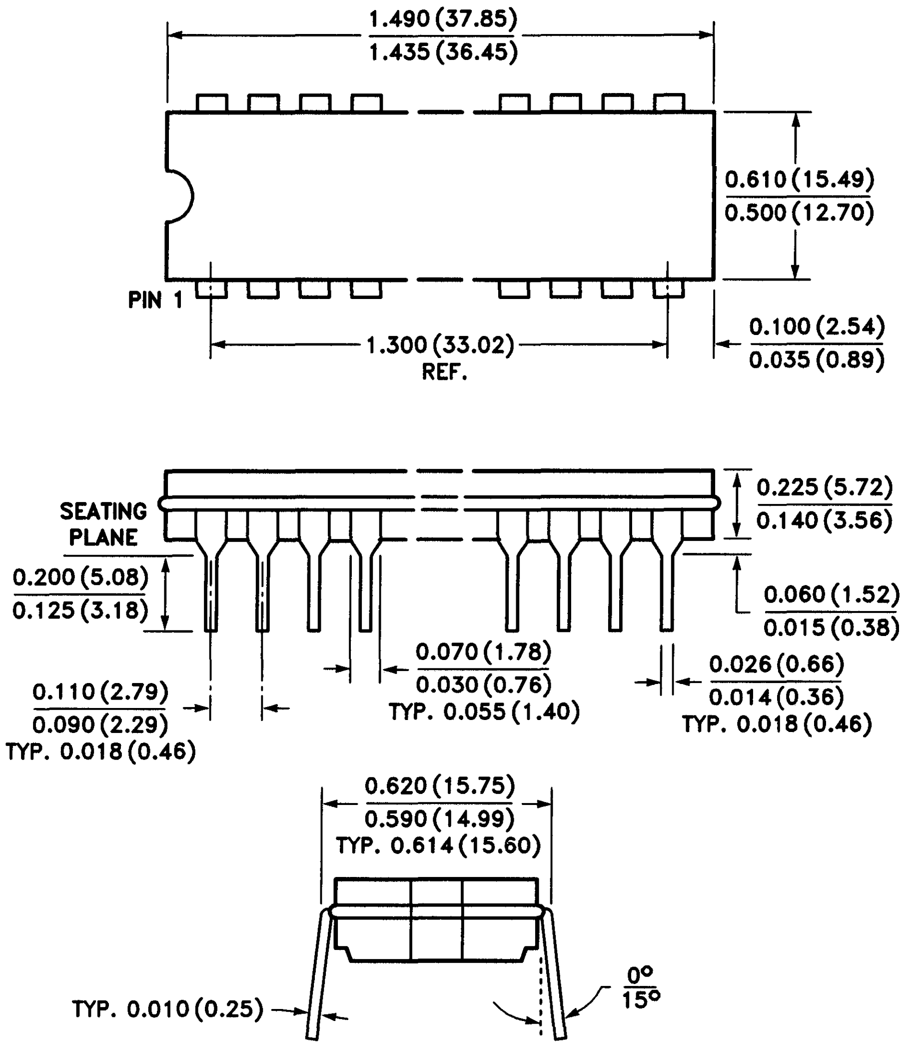
K = 28-Pin Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

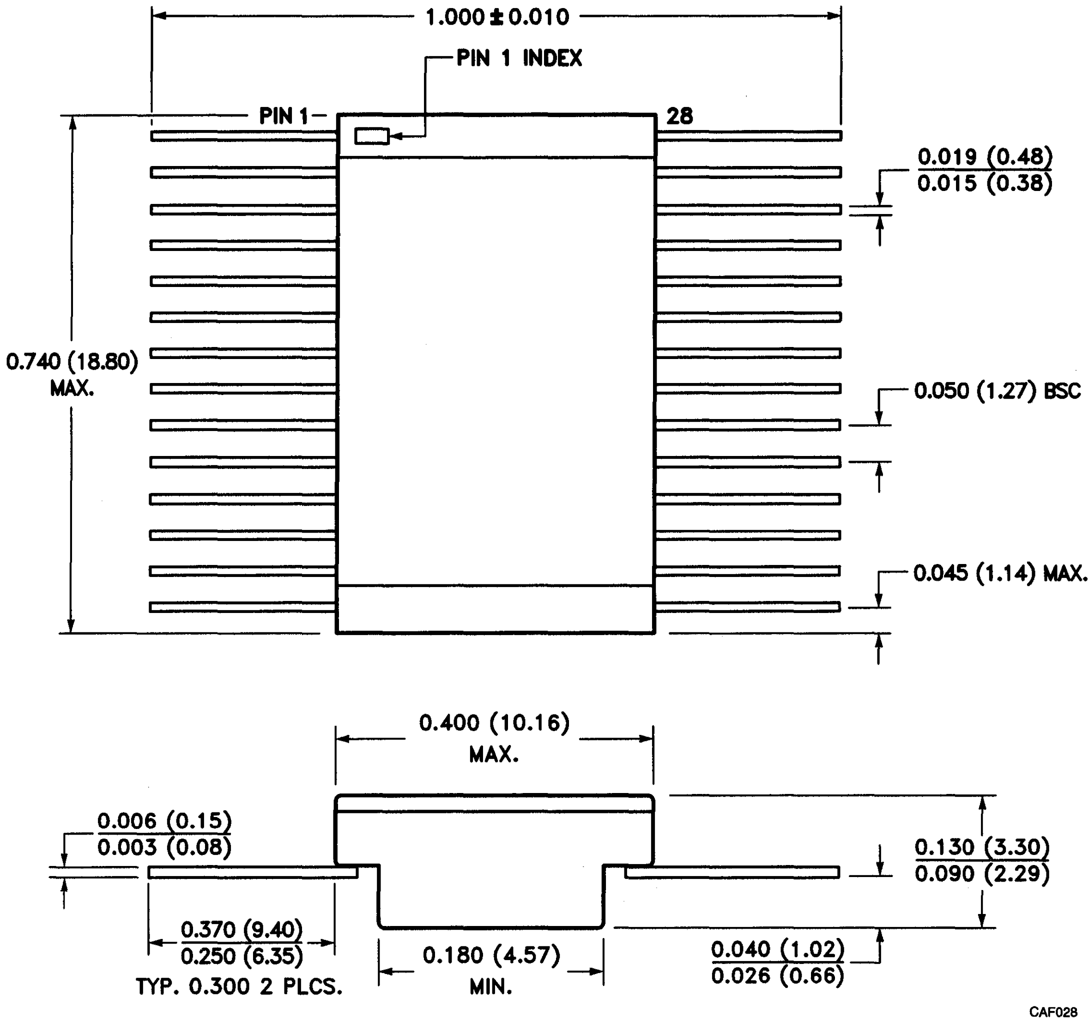
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

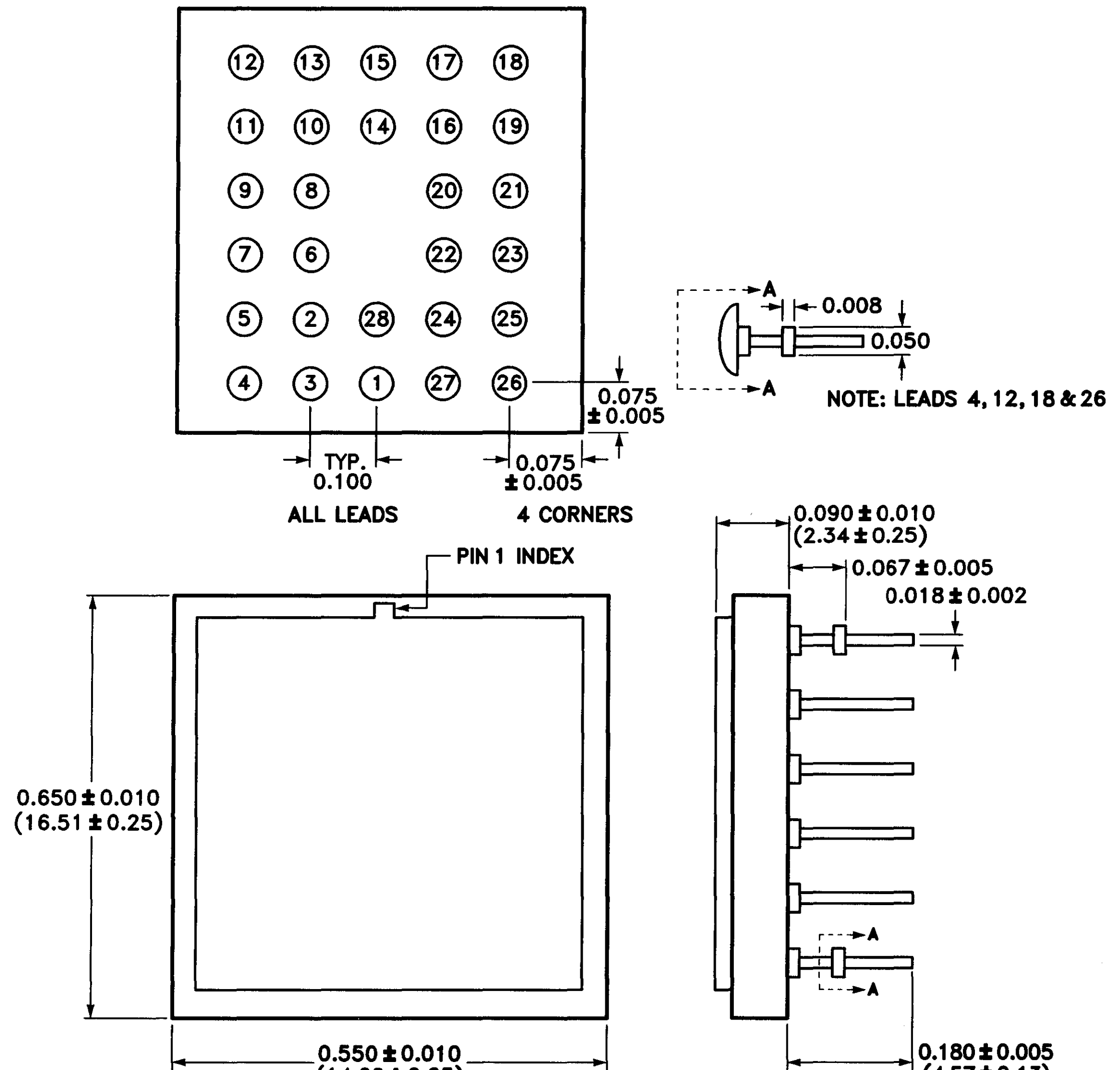
28-LEAD CERAMIC FLAT PACK TYPE F1



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H

PACKAGING INFORMATION

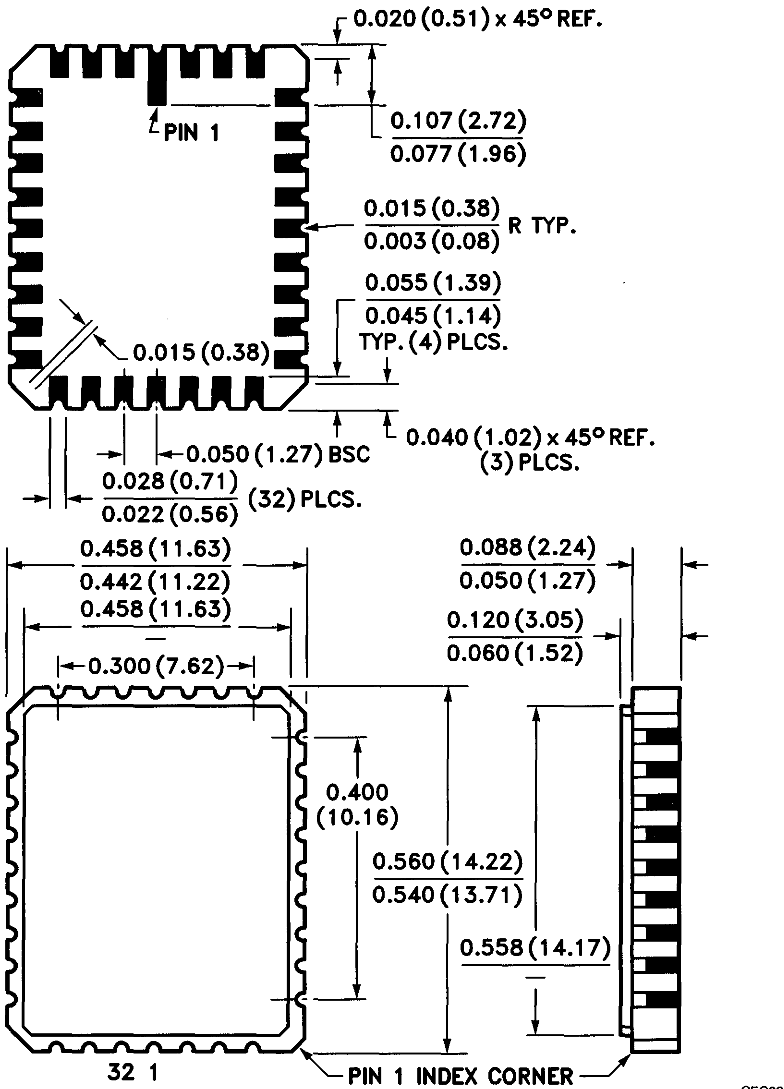
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

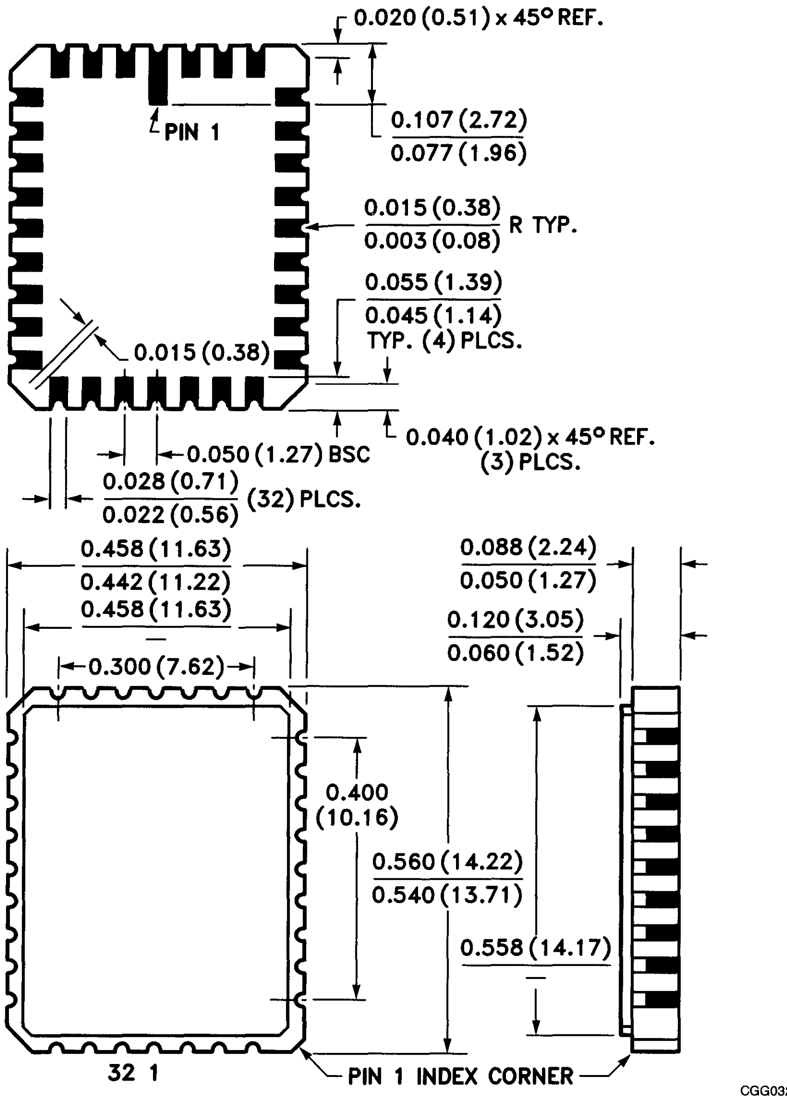


NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

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64K **Commercial Industrial** **X2864H X2864HI** **8192 x 8 Bit**

Electrically Erasable PROM

TYPICAL FEATURES

- **70 ns Access Time**
- **High Performance Scaled NMOS Technology**
- **Fast Write Cycle Times**
  - **—32-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 3 ms Typical**
  - **—Complete Memory Rewrite: 750 ms Typical**
  - **—Effective Byte Write Cycle Time of 95 μs Typical**
- **$\overline{\text{DATA}}$ Polling**
  - **—Allows User to Minimize Write Cycle Time**
- **Simple Byte and Page Write**
  - **—Single TTL Level $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

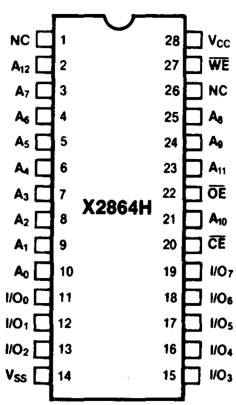
The Xicor X2864H is a high speed 8K x 8 E^{2}PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864H features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs, and EPROMs.

The X2864H supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864H also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

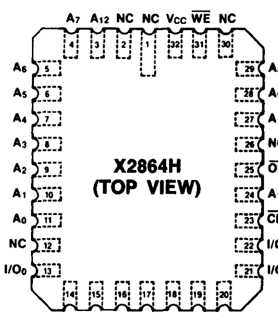
PIN CONFIGURATIONS

PLASTIC CERDIP FLAT PACK



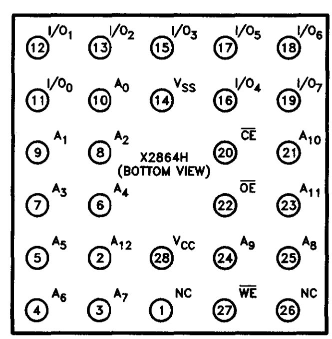
0034-1

PLCC LCC



0034-2

PGA



0034-9

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
- X2864H .... −10°C to +85°C
- X2864HI .... −65°C to +135°C

Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
- Respect to Ground .... −1.0V to +7V

D.C. Output Current .... 5 mA
Lead Temperature
- (Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X2864H T_A = 0°C to +70°C, V_{CC} = +5V ±5%, unless otherwise specified.
X2864HI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	150	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50	80	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L = 30 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

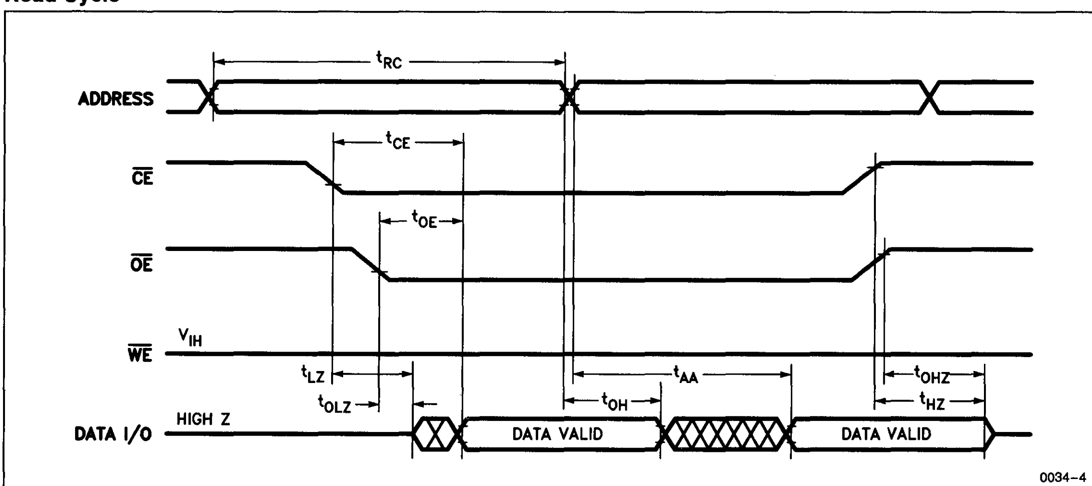
A.C. CHARACTERISTICS

X2864H $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$, unless otherwise specified.
X2864HI $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X2864H-70 X2864HI-70		X2864H-90 X2864HI-90		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	70		90		ns
t_{CE}	Chip Enable Access Time		70		90	ns
t_{AA}	Address Access Time		70		90	ns
t_{OE}	Output Enable Access Time		35		45	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	40	0	40	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	40	0	40	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Read Cycle



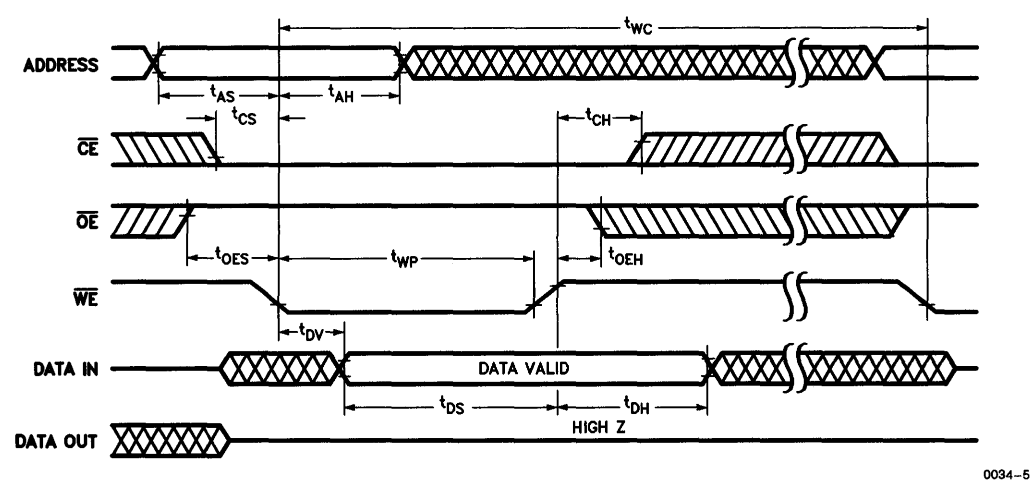
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

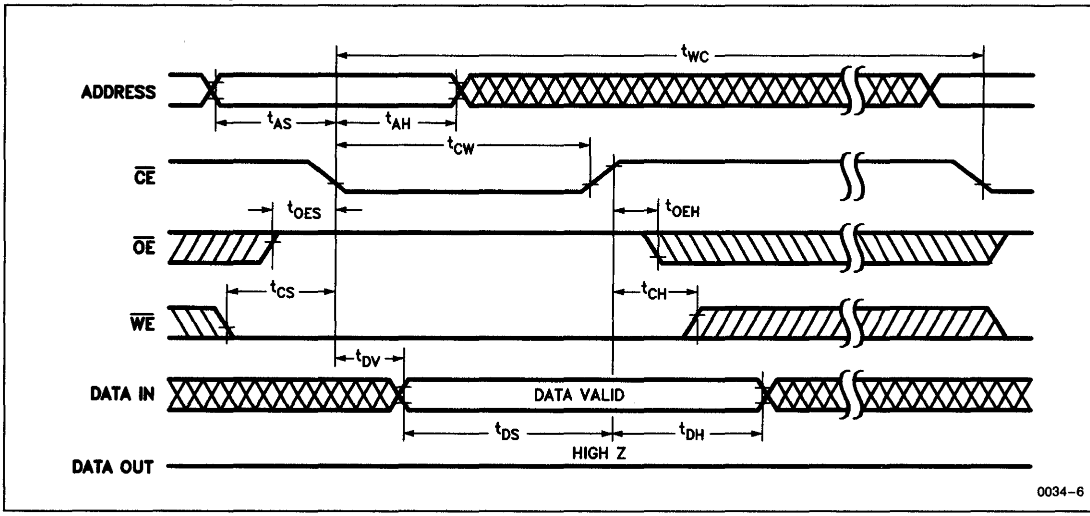
Write Cycle Limits

Symbol	Parameter	X2864H-70 X2864HI-70		X2864H-90 X2864HI-90		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		5		5	ms
t_{AS}	Address Setup Time	5		5		ns
t_{AH}	Address Hold Time	50		50		ns
t_{CS}	Write Setup Time	0		0		ns
t_{CH}	Write Hold Time	0		0		ns
t_{CW}	$\overline{CE}$ Pulse Width	60		80		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	5		5		ns
t_{WP}	$\overline{WE}$ Pulse Width	60		80		ns
t_{WPH}	$\overline{WE}$ High Recovery	50		50		ns
t_{DV}	Data Valid		100		100	µs
t_{DS}	Data Setup	35		35		ns
t_{DH}	Data Hold	5		5		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	1	100	1	100	µs

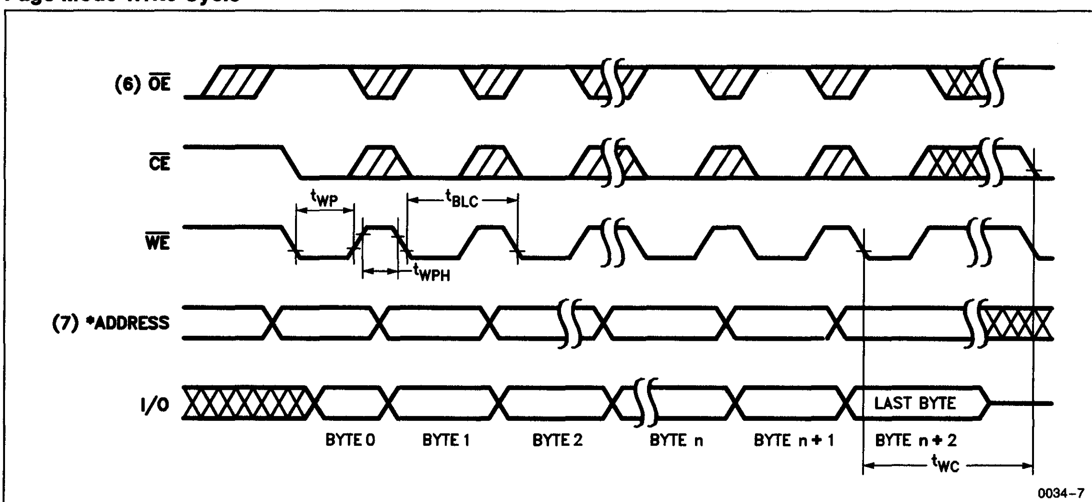
$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

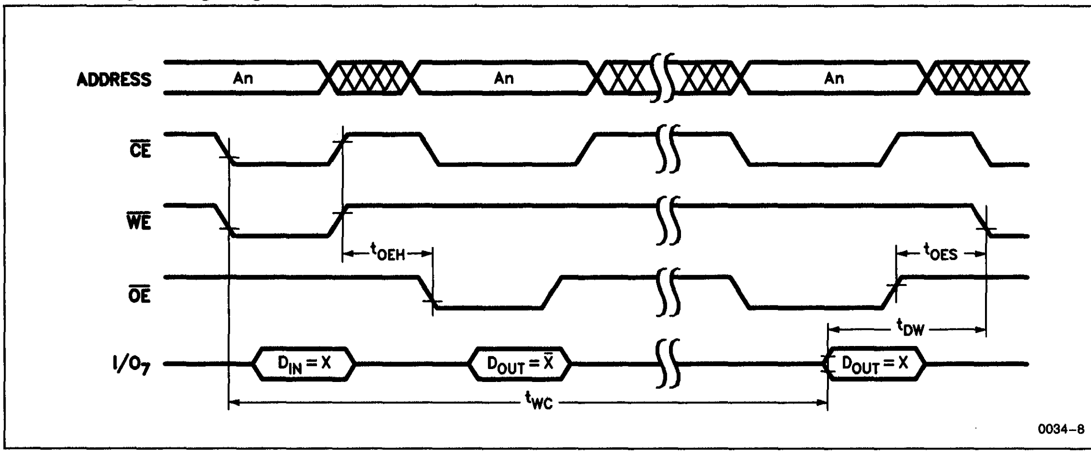


*For each successive write within the page write operation, A_5–A_{12} should be the same or writes to an unknown address could occur.

Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g., this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(8)



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (8) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2864H through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2864H.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864H supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation

The page write feature of the X2864H allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864H prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_5 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the 100 μs byte load cycle time.

$\overline{DATA}$ Polling

The X2864H features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864H, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are two features that protect the nonvolatile data from inadvertent writes.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$4.0V.
- Write Inhibit—Holding $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

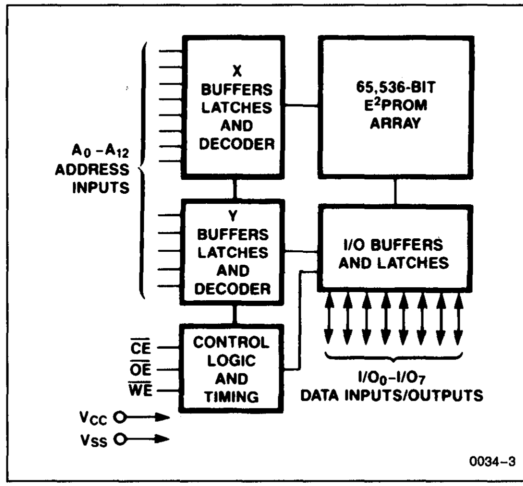
Because the X2864H is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864H has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

64K E²PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864HP-70	8192 x 8		•									†	70 ns	NMOS	Standard
X2864HP-90	8192 x 8		•									†	90 ns	NMOS	Standard
X2864HPI-90	8192 x 8		•									I	90 ns	NMOS	Standard
X2864HD-70	8192 x 8			•								†	70 ns	NMOS	Standard
X2864HD-90	8192 x 8			•								†	90 ns	NMOS	Standard
X2864HDI-90	8192 x 8			•								I	90 ns	NMOS	Standard
X2864HF-70	8192 x 8					•						†	70 ns	NMOS	Standard
X2864HF-90	8192 x 8					•						†	90 ns	NMOS	Standard
X2864HFI-90	8192 x 8					•						I	90 ns	NMOS	Standard
X2864HK-70	8192 x 8							•				†	70 ns	NMOS	Standard
X2864HK-90	8192 x 8							•				†	90 ns	NMOS	Standard
X2864HKI-90	8192 x 8							•				I	90 ns	NMOS	Standard
X2864HJ-70	8192 x 8								•			†	70 ns	NMOS	Standard
X2864HJ-90	8192 x 8								•			†	90 ns	NMOS	Standard
X2864HJI-90	8192 x 8								•			I	90 ns	NMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E^2PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864HE-70	8192 x 8									•		†	70 ns	NMOS	Standard
X2864HE-90	8192 x 8									•		†	90 ns	NMOS	Standard
X2864HEI-90	8192 x 8									•		I	90 ns	NMOS	Standard
X2864HG-70	8192 x 8										•	†	70 ns	NMOS	Standard
X2864HG-90	8192 x 8										•	†	90 ns	NMOS	Standard
X2864HGI-90	8192 x 8										•	I	90 ns	NMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
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F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
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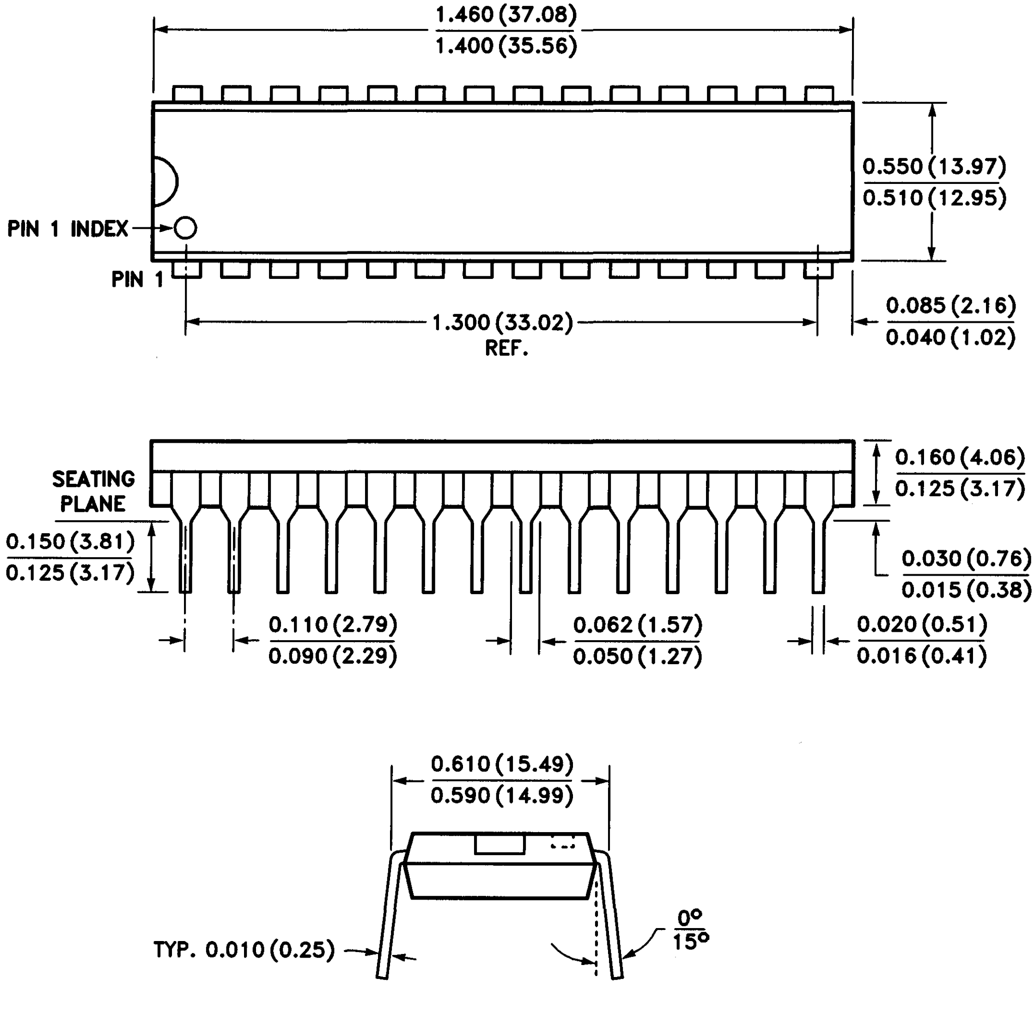
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

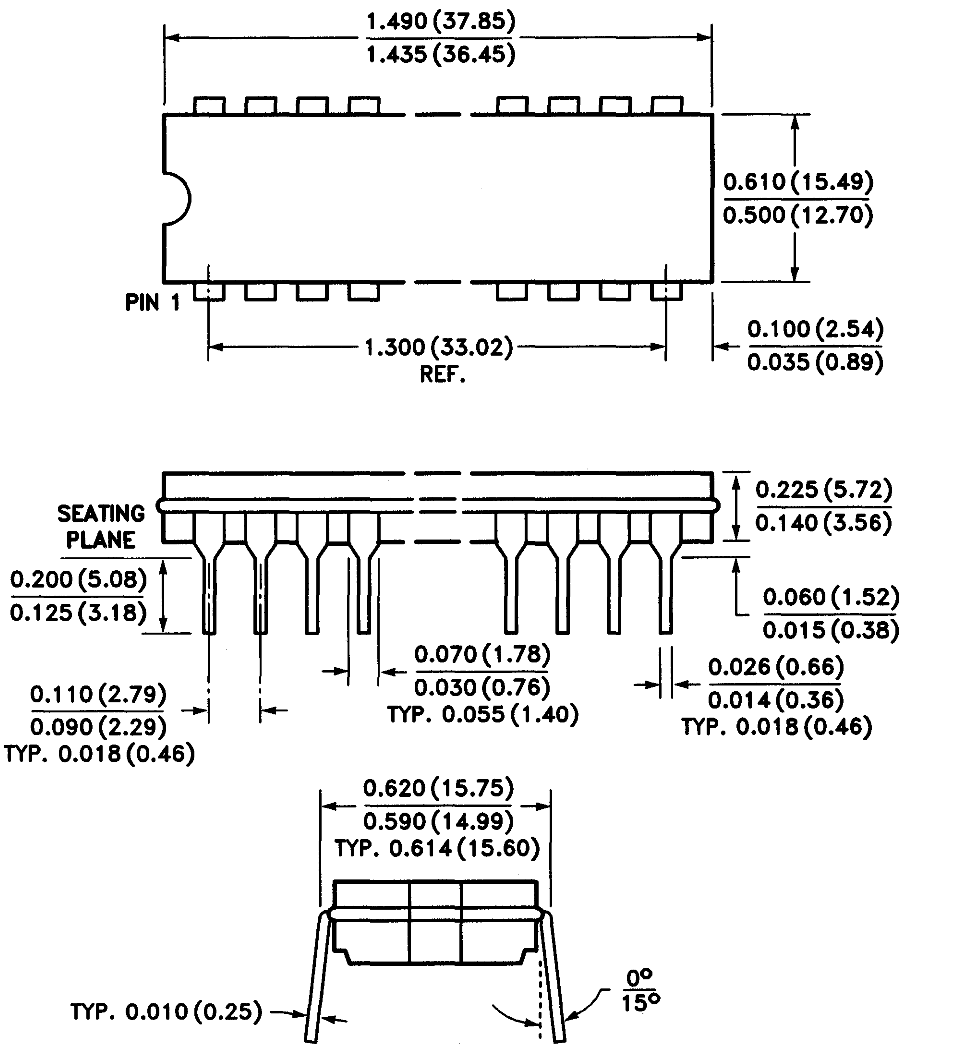
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

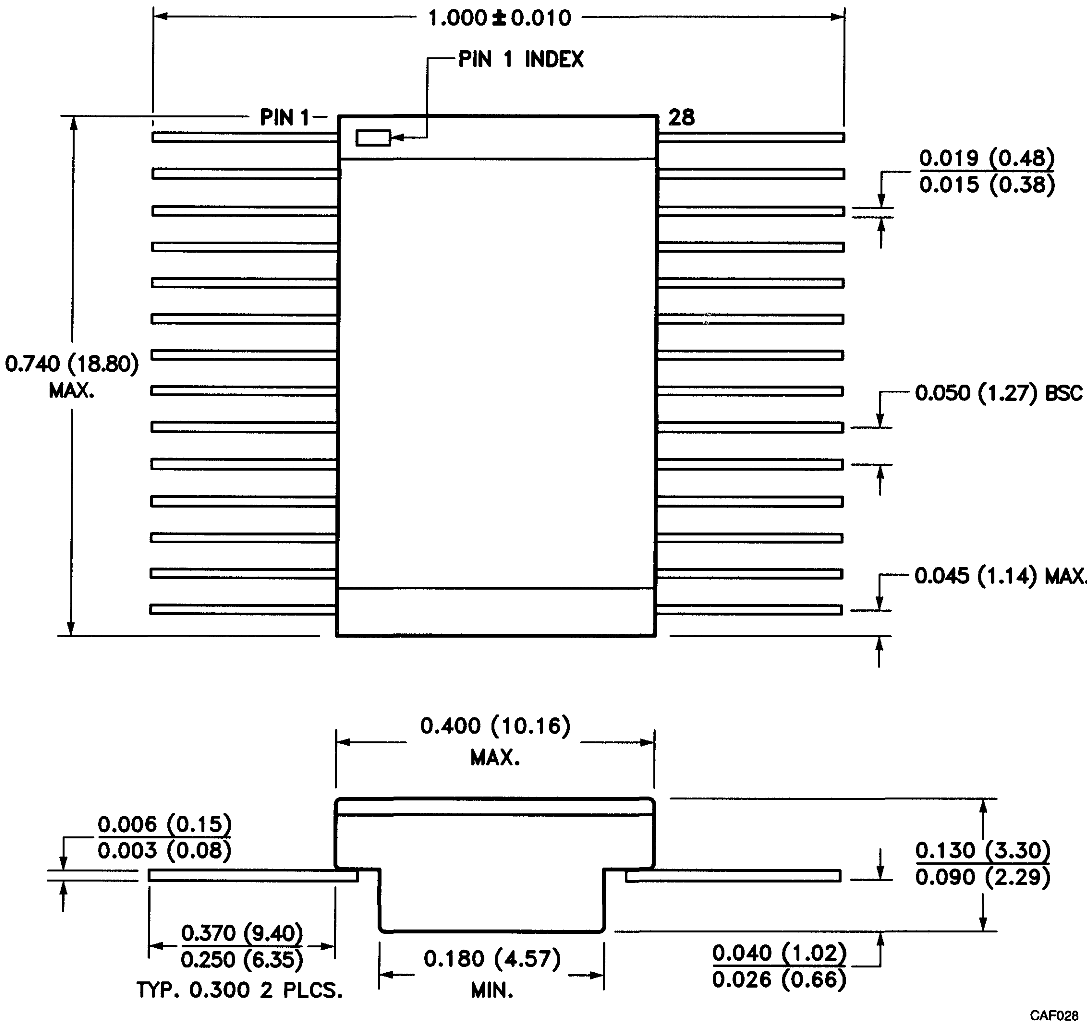
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

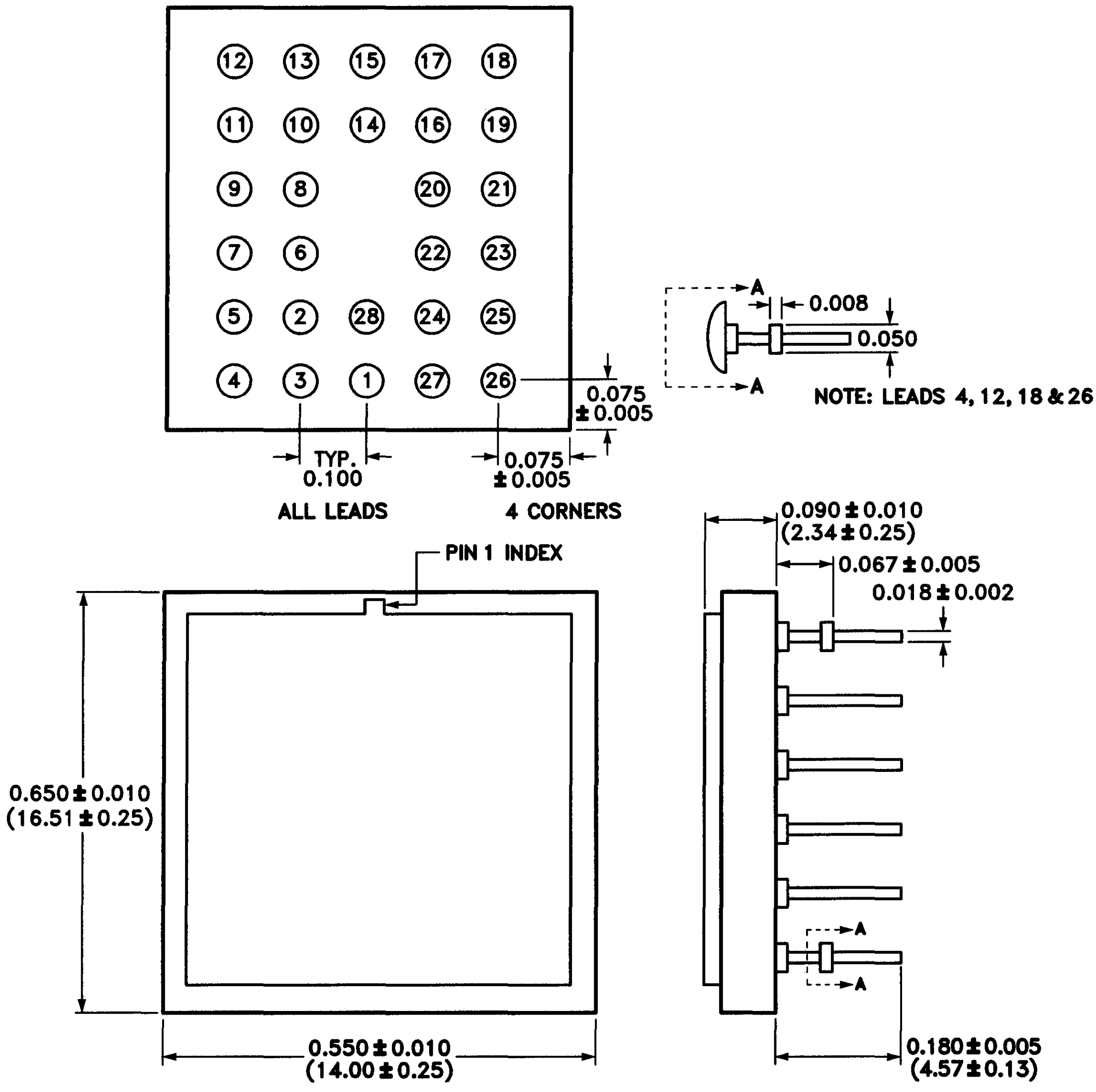
28-LEAD CERAMIC FLAT PACK TYPE F1



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H

PACKAGING INFORMATION

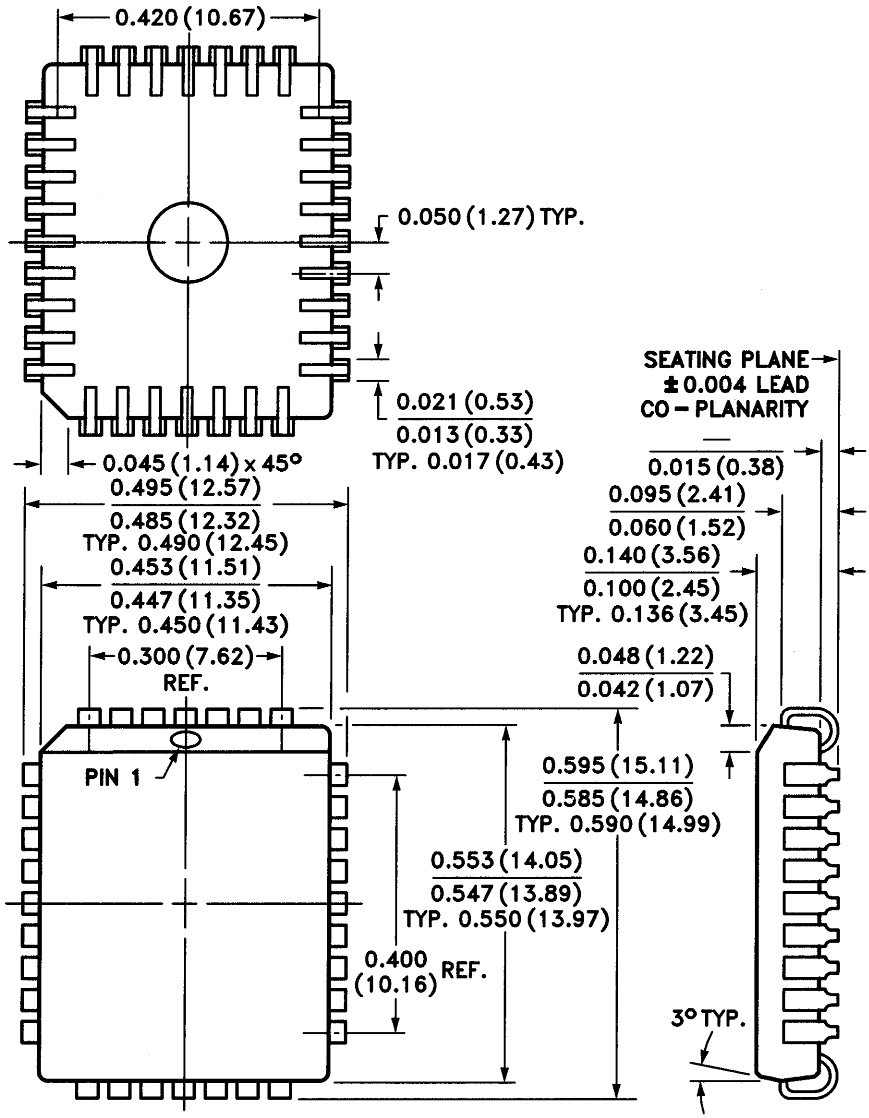
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

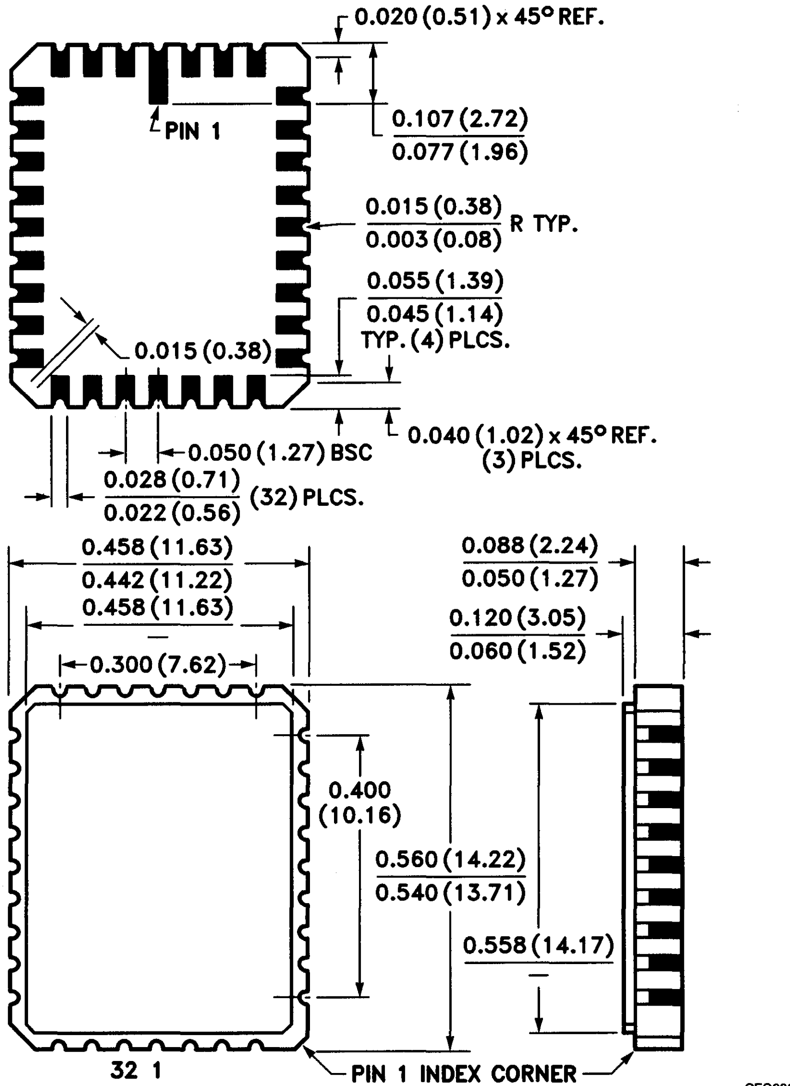


PJG032

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

PACKAGING INFORMATION

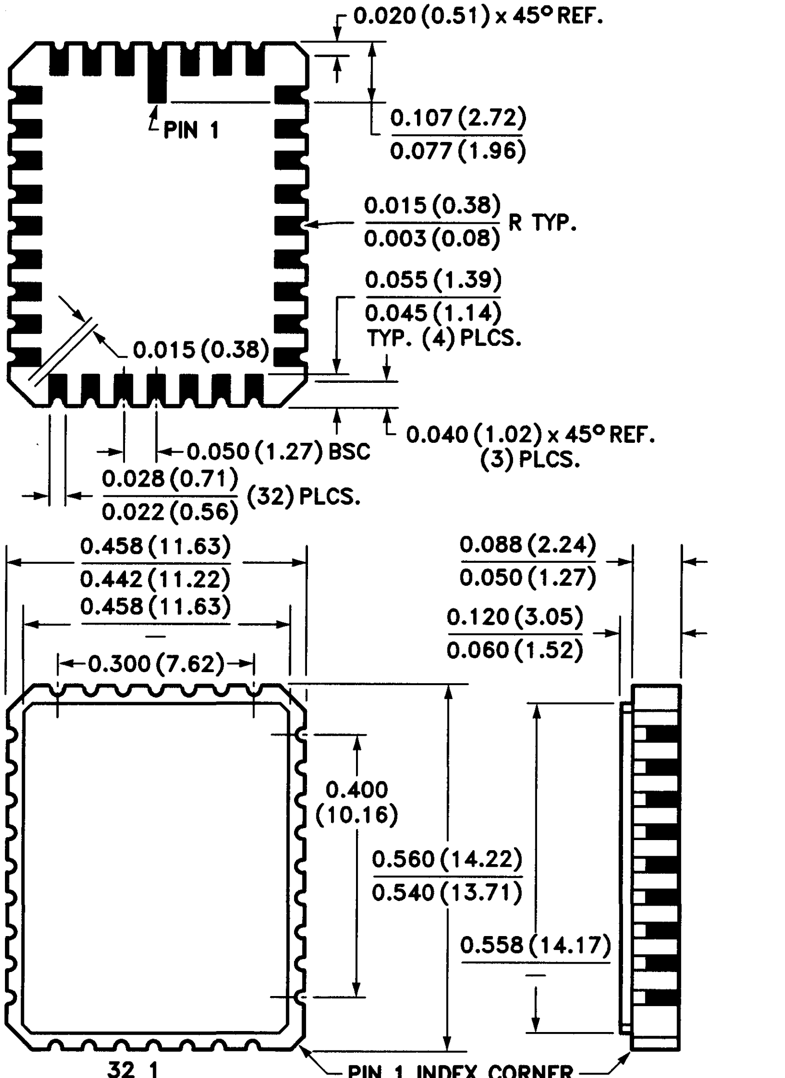
32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

NOTES

NOTES

Sales Offices

U.S. Sales Offices

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Fax: 408/432-0640

64K Military X2864HM 8192 x 8 Bit

Electrically Erasable PROM

TYPICAL FEATURES

- **90 ns Access Time**
- **High Performance Scaled NMOS Technology**
- **Fast Write Cycle Times**
  - **—32-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 3 ms Typical**
  - **—Complete Memory Rewrite: 750 ms Typical**
  - **—Effective Byte Write Cycle Time of 95 μs Typical**
- **$\overline{\text{DATA}}$ Polling**
  - **—Allows User to Minimize Write Cycle Time**
- **Simple Byte and Page Write**
  - **—Single TTL Level $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

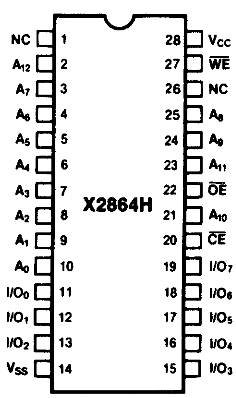
The Xicor X2864H is a high speed 8K x 8 E^2PROM, fabricated with Xicor's proprietary, high performance, N-channel floating gate MOS technology. Like all Xicor programmable nonvolatile memories it is a 5V only device. The X2864H features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs, ROMs and EPROMs.

The X2864H supports a 32-byte page write operation, effectively providing a 95 μs/byte write cycle and enabling the entire memory to be written in less than 750 ms. The X2864H also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

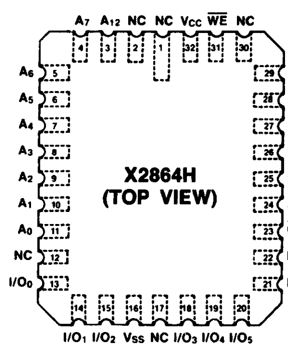
PIN CONFIGURATIONS

CERDIP
FLAT PACK



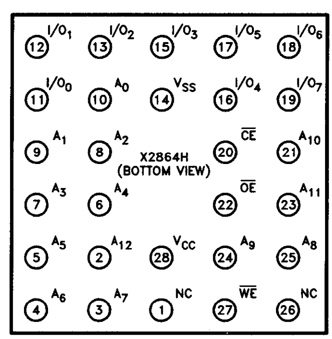
0033-1

LCC



0033-2

PGA



0033-9

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active)		80	150	mA	$\overline{CE} = \overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{SB}	V_{CC} Current (Standby)		50	80	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	1	ms
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL Gate and C_L = 30 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

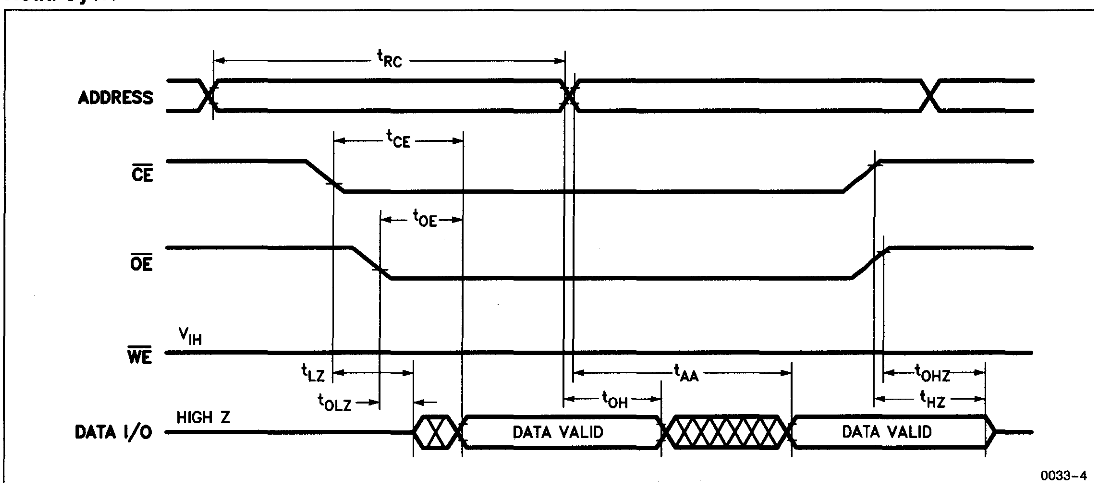
A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	90		ns
t_{CE}	Chip Enable Access Time		90	ns
t_{AA}	Address Access Time		90	ns
t_{OE}	Output Enable Access Time		45	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	40	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	40	ns
t_{OH}	Output Hold from Address Change	0		ns

Read Cycle



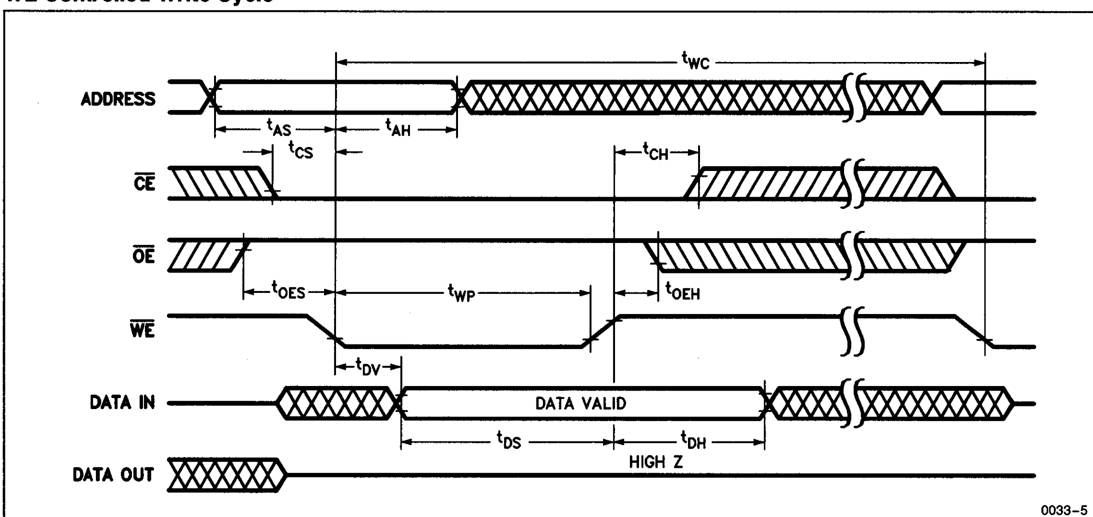
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

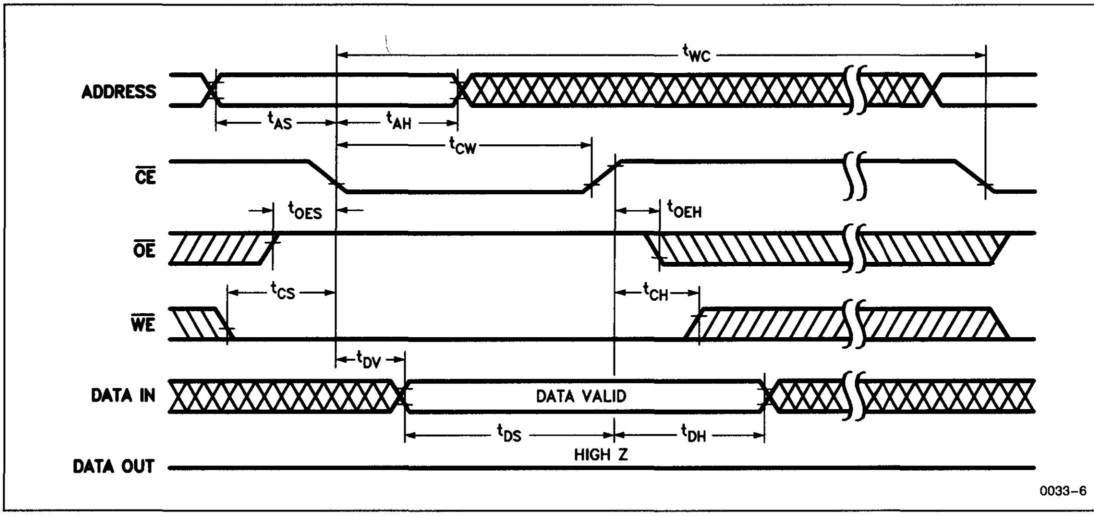
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time		5	ms
t_{AS}	Address Setup Time	5		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	80		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	5		ns
t_{WP}	$\overline{WE}$ Pulse Width	80		ns
t_{WPH}	$\overline{WE}$ High Recovery	50		ns
t_{DV}	Data Valid		100	µs
t_{DS}	Data Setup	35		ns
t_{DH}	Data Hold	5		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	1	100	µs

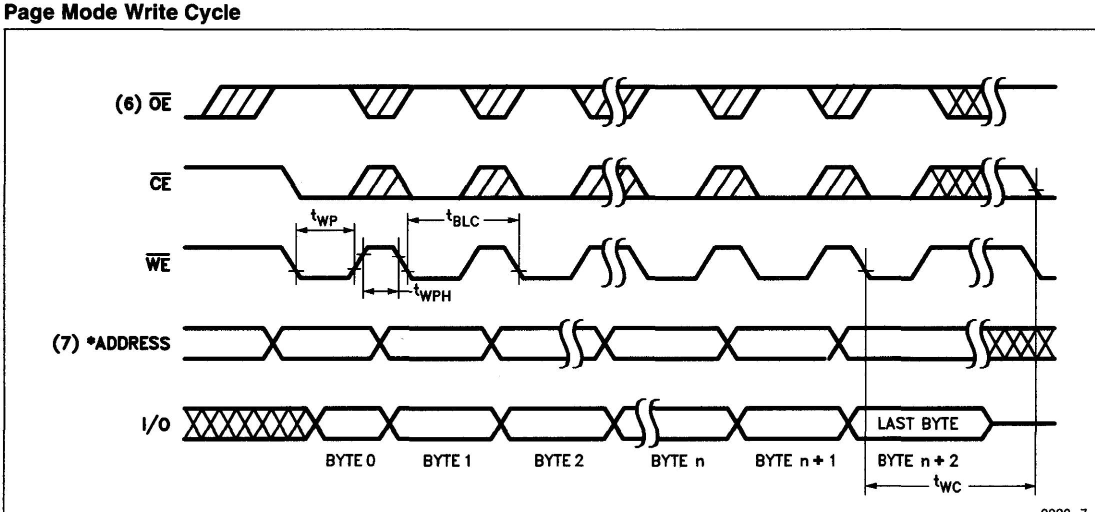
$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



Page Mode Write Cycle

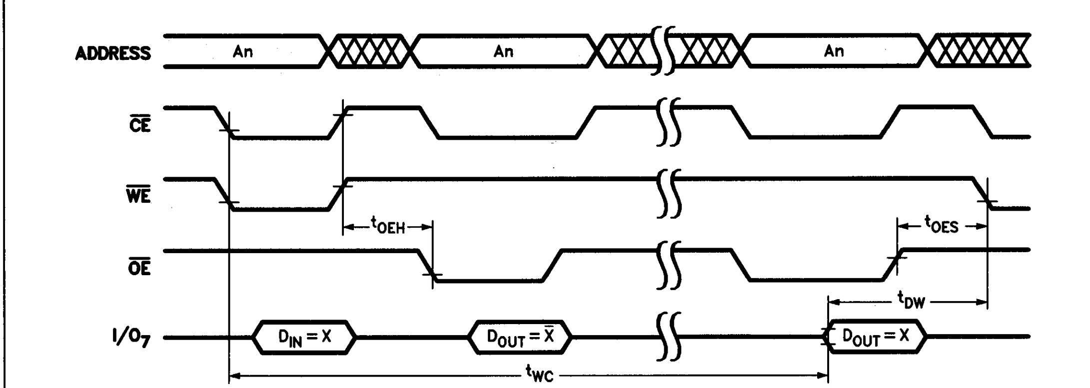


*For each succcessive write within the page write operation, A_5–A_{12} should be the same or writes to an unknown address could occur.

Notes: (6) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW; e.g., this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(7) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(8)



0033-8

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (8) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X2864H through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X2864H.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X2864H supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation

The page write feature of the X2864H allows the entire memory to be written in 750 ms. Page write allows two to thirty-two bytes of data to be consecutively written to the X2864H prior to the commencement of the internal programming cycle. The destination addresses for a page write operation must reside on the same page; that is, A_5 through A_{12} must not change.

The page write mode can be entered during any write operation. Following the initial byte write cycle, the host can write an additional one to thirty-one bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the 100 μs byte load cycle time.

$\overline{DATA}$ Polling

The X2864H features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X2864H, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

WRITE PROTECTION

There are two features that protect the nonvolatile data from inadvertent writes.

- V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$4.0V.
- Write Inhibit—Holding $\overline{OE}$ LOW, $\overline{WE}$ HIGH or $\overline{CE}$ HIGH during power-on and power-off, will inhibit inadvertent writes.

SYSTEM CONSIDERATIONS

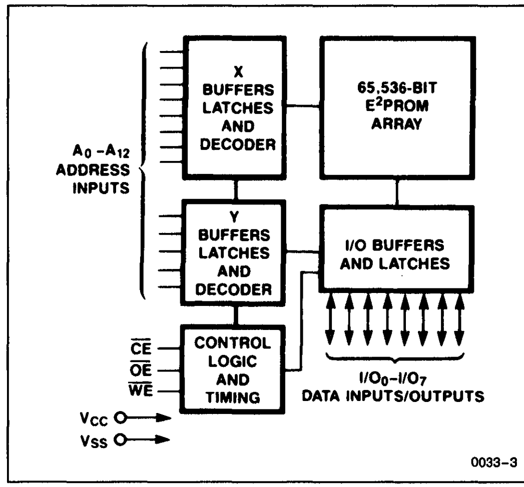
Because the X2864H is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X2864H has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

64K E²PROMs

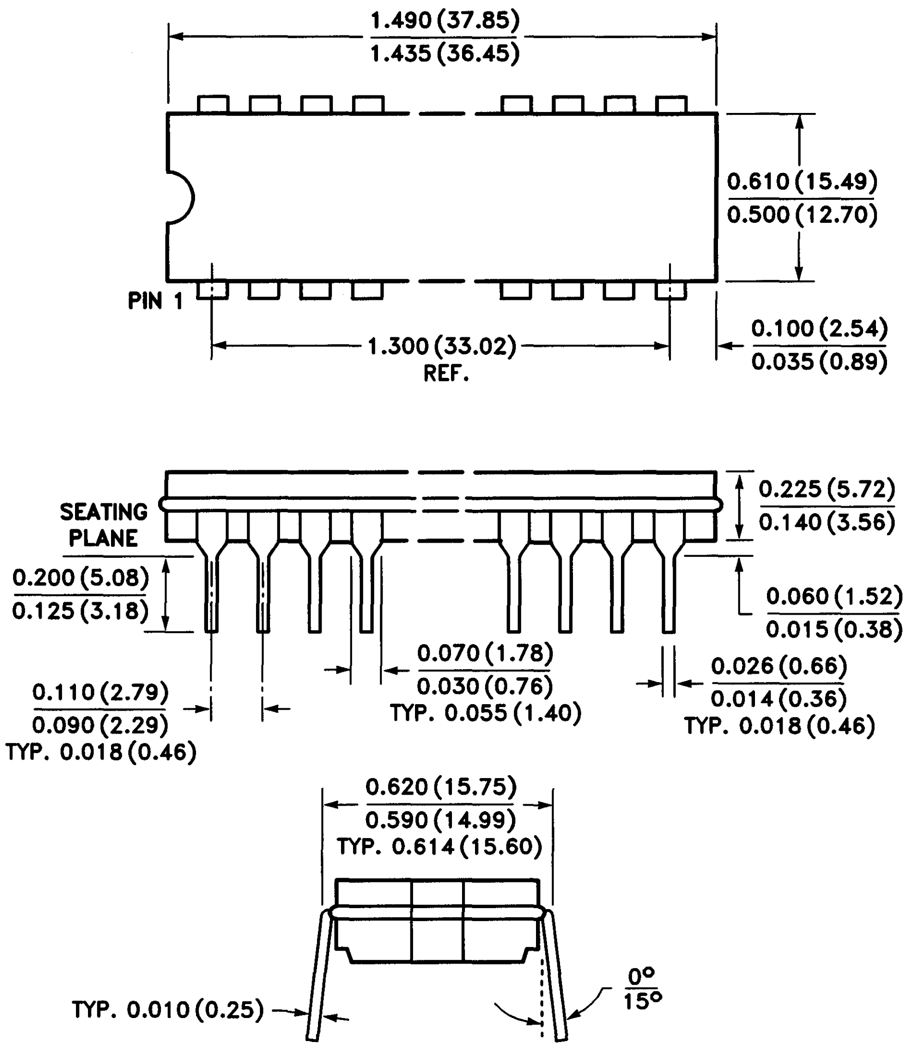
Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X2864HDM-90	8192 x 8			•								M	90 ns	NMOS	Standard
X2864HDMB-90	8192 x 8			•								M	90 ns	NMOS	883 Rev. C, Class B
X2864HFM-90	8192 x 8					•						M	90 ns	NMOS	Standard
X2864HFMB-90	8192 x 8					•						M	90 ns	NMOS	883 Rev. C, Class B
X2864HKM-90	8192 x 8							•				M	90 ns	NMOS	Standard
X2864HKMB-90	8192 x 8							•				M	90 ns	NMOS	883 Rev. C, Class B
X2864HEM-90	8192 x 8									•		M	90 ns	NMOS	Standard
X2864HEMB-90	8192 x 8									•		M	90 ns	NMOS	883 Rev. C, Class B
X2864HGM-90	8192 x 8										•	M	90 ns	NMOS	Standard
X2864HGMB-90	8192 x 8										•	M	90 ns	NMOS	883 Rev. C, Class B

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

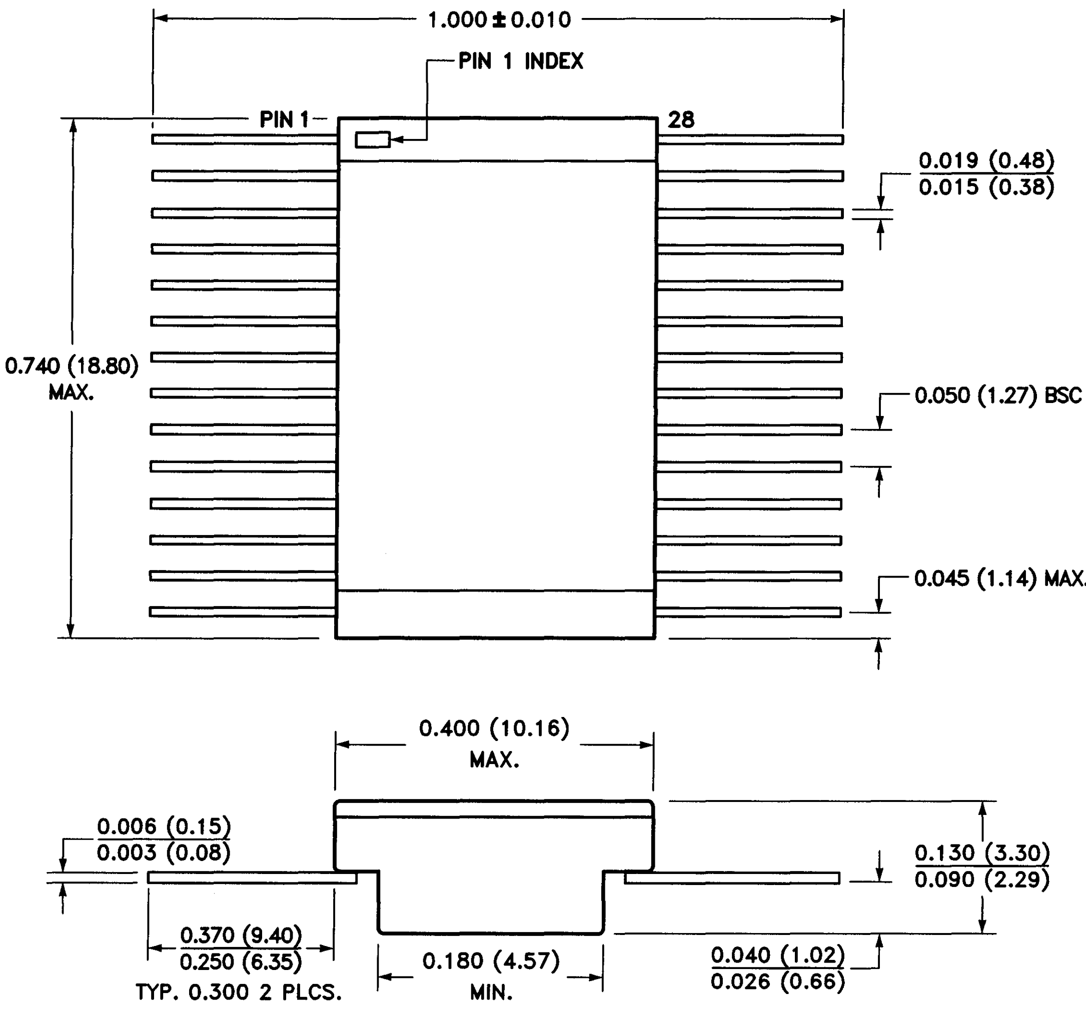
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

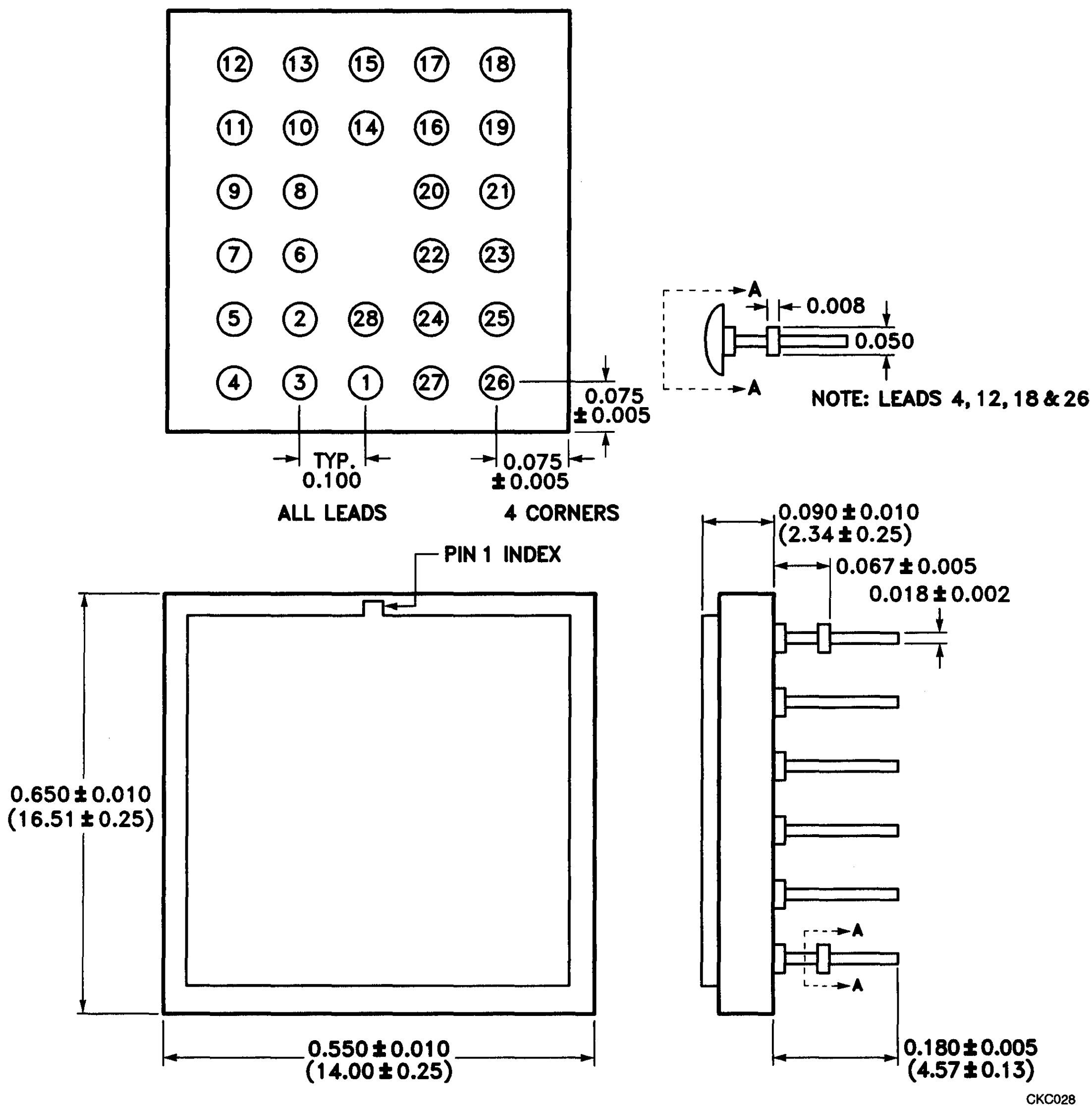
28-LEAD CERAMIC FLAT PACK TYPE F1



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B AND X2864H

PACKAGING INFORMATION

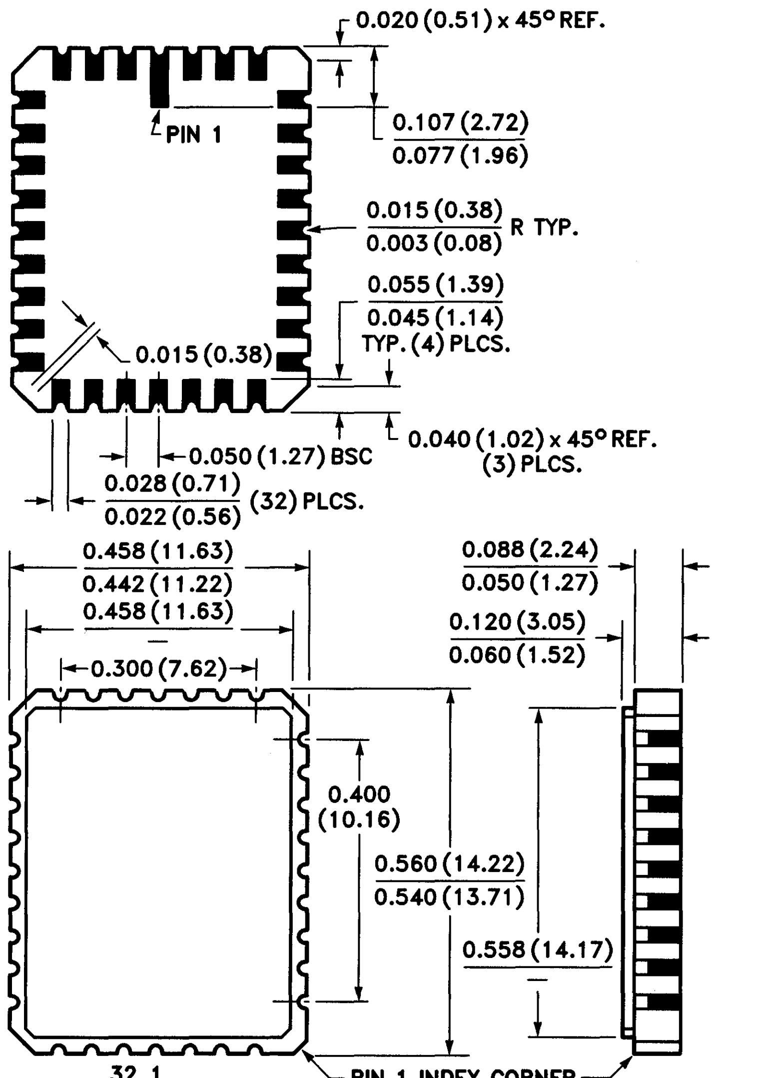
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

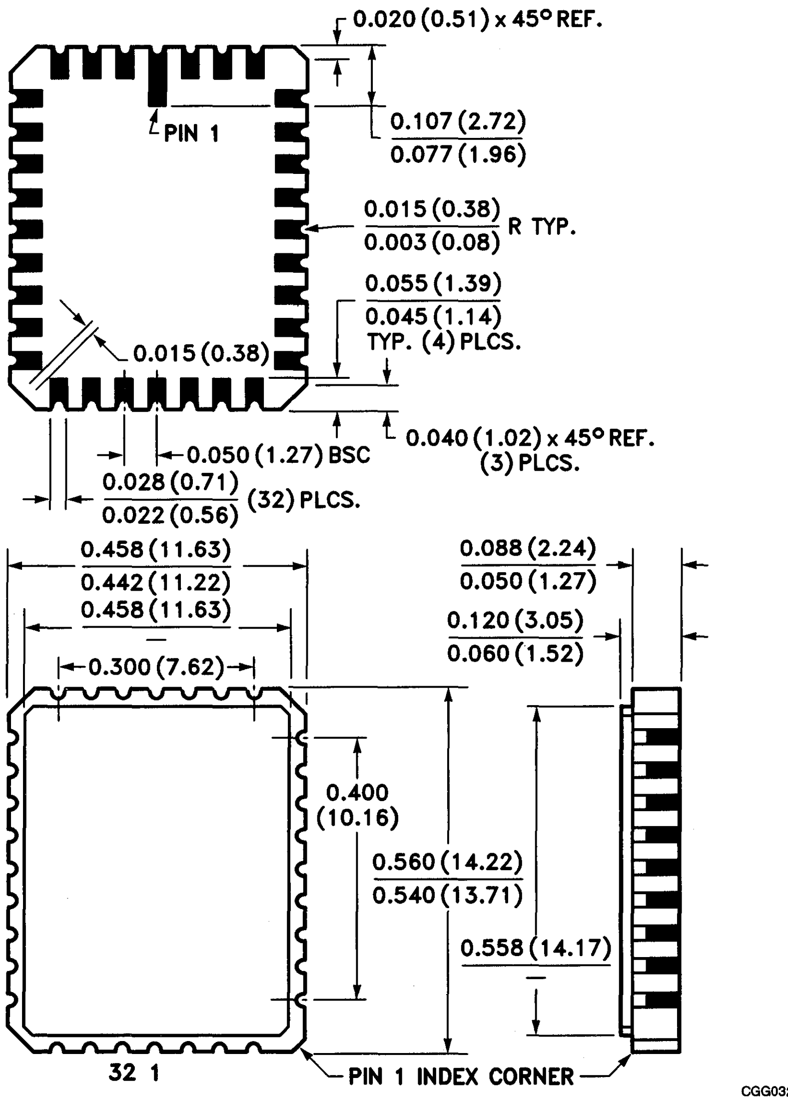
32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

NOTES

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8/88 Stock No. 200-180

ADVANCED INFORMATION

64K	Commercial Industrial	X28C64 X28C64I	8K x 8 Bit

Electrically Erasable PROM

FEATURES

- **LOW Power CMOS**
  - **—60 mA Active Current Max.**
  - **—200 μA Standby Current Max.**
- **Fast Write Cycle Times**
  - **—64-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 5 ms Typical**
  - **—Complete Memory Rewrite: 0.625 Sec. Typical**
  - **—Effective Byte Write Cycle Time: 78 μs Typical**
- **Software Data Protection**
- **End of Write Detection**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit**
- **Simple Byte and Page Write**
  - **—Single TTL Compatible $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

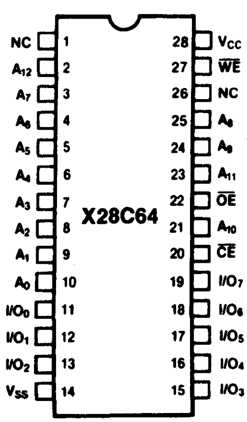
The Xicor X28C64 is a 8K x 8 E^2PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C64 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

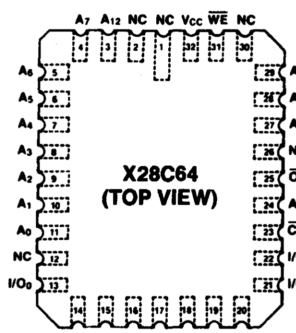
PIN CONFIGURATIONS

PLASTIC
CERDIP
FLAT PACK



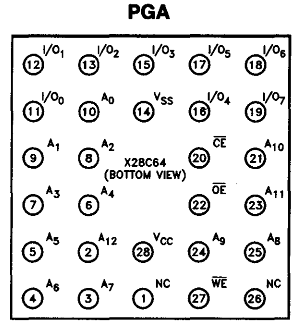
0101-1

PLCC
LCC



0101-2

PGA



0101-3

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
- X28C64 .... −10°C to +85°C
- X28C64I .... −65°C to +135°C

Storage Temperature .... −65°C to +150°C

Voltage on any Pin with
- Respect to Ground .... −1.0V to +7V

D.C. Output Current .... 5 mA

Lead Temperature
- (Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28C64 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C64I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	µA	$\overline{CE} = \overline{WE} = V_{CC} - 0.3V$ All I/O's = Open, Other Inputs = Don't Care
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	100	µs
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

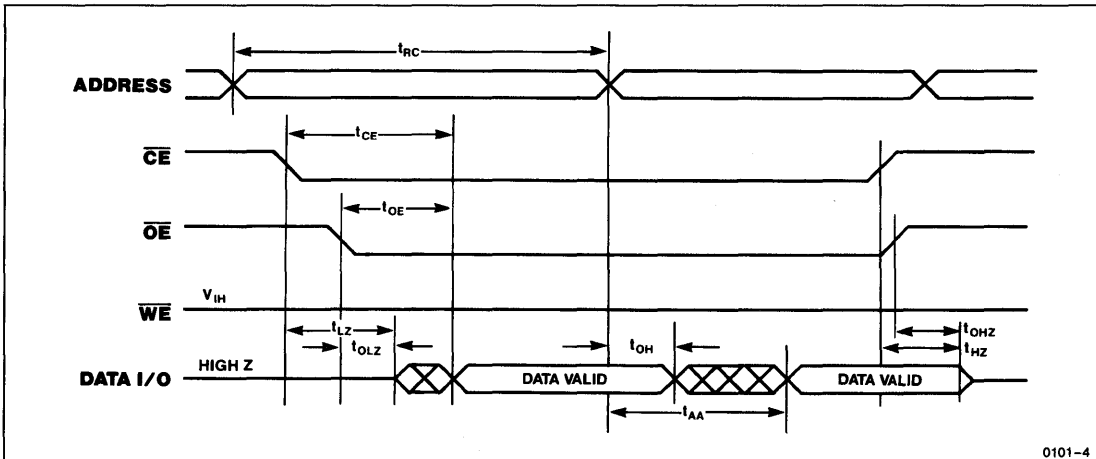
A.C. CHARACTERISTICS

X28C64 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C64I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C64-20 X28C64I-20		X28C64-25 X28C64I-25		X28C64 X28C64I		X28C64-35 X28C64I-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		350		ns
t_{CE}	Chip Enable Access Time		200		250		300		350	ns
t_{AA}	Address Access Time		200		250		300		350	ns
t_{OE}	Output Enable Access Time		80		100		100		100	ns
$t_{LZ}^{(4)}$	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
$t_{OLZ}^{(4)}$	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
$t_{HZ}^{(5)}$	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
$t_{OHZ}^{(5)}$	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



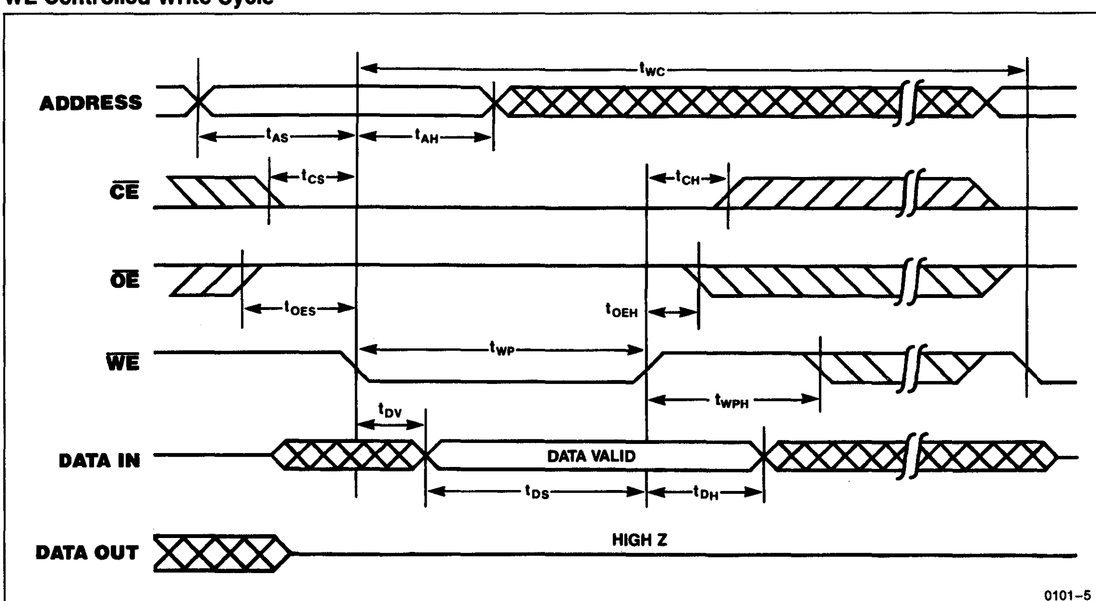
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

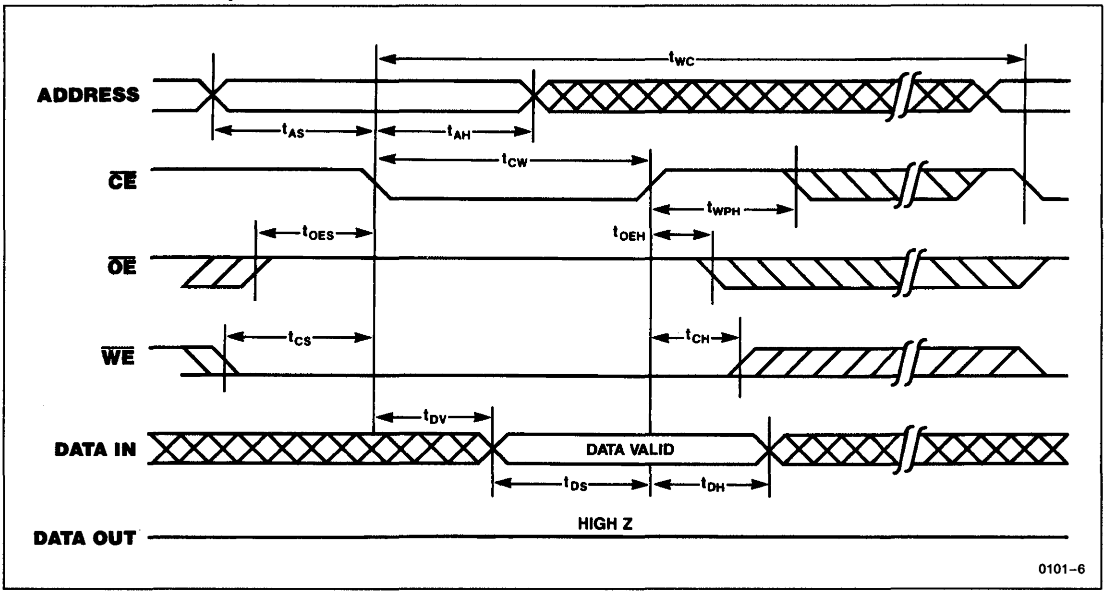
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	200			ns
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle

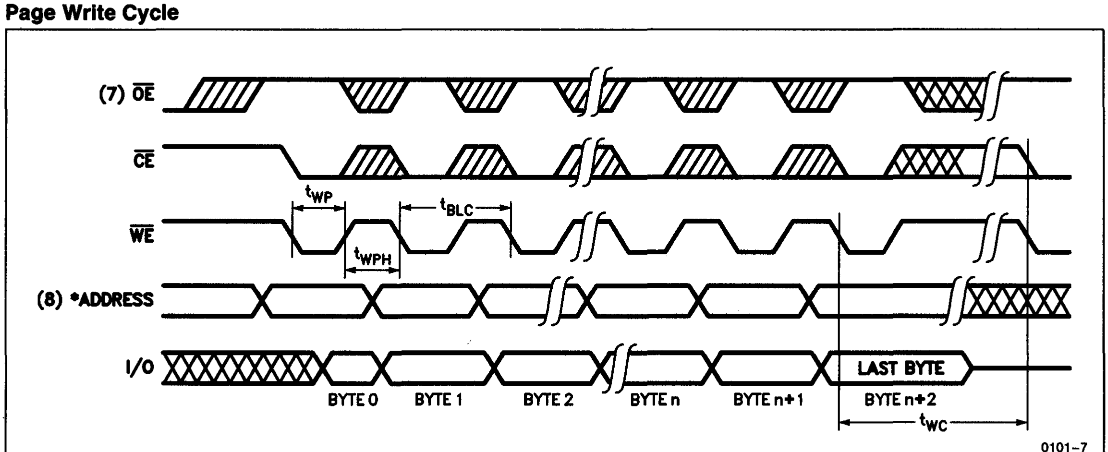


Note: (6) Typical values are for $T_A = 25°C$ and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

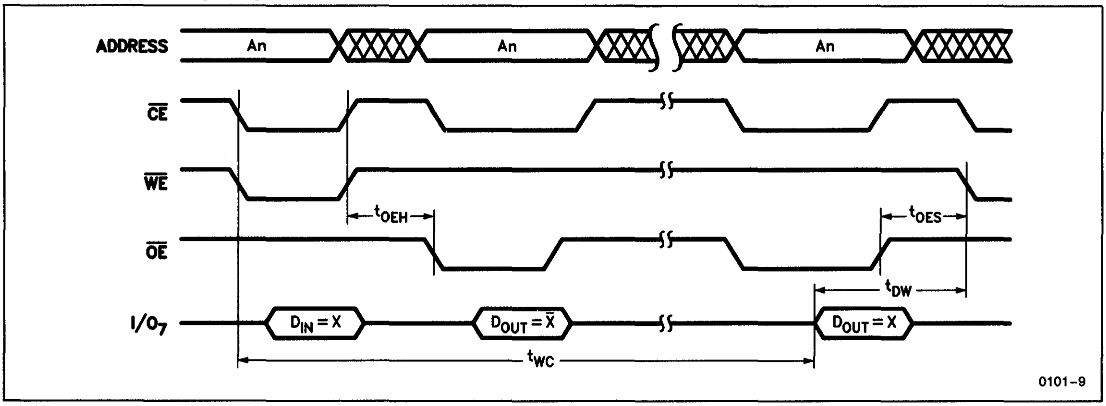


*For each successive write within the page write operation, A_6–A_{12} should be the same or writes to an unknown address could occur.

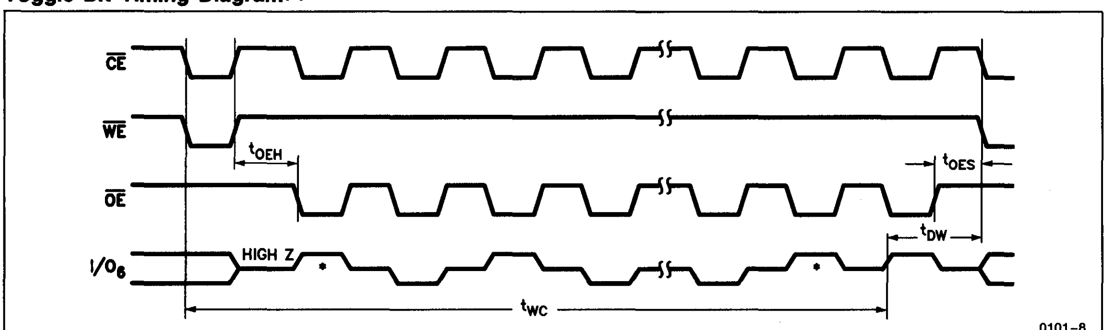
Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)

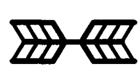


Toggle Bit Timing Diagram(9)



*I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C64 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C64.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

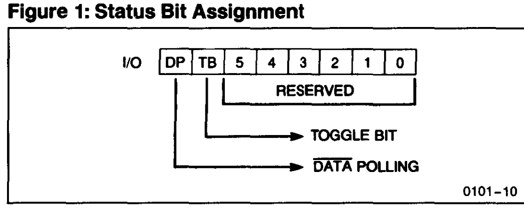
The page write feature of the X28C64 allows the entire memory to be written in 0.625 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C64 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{12}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits

The X28C64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{\text{DATA}}$ Polling (I/O_7)

The X28C64 features $\overline{\text{DATA}}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{\text{DATA}}$ Polling allows a simple bit test operation to determine the status of the X28C64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C64 is in the protected state and an illegal write operation is attempted $\overline{\text{DATA}}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O$_7$

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

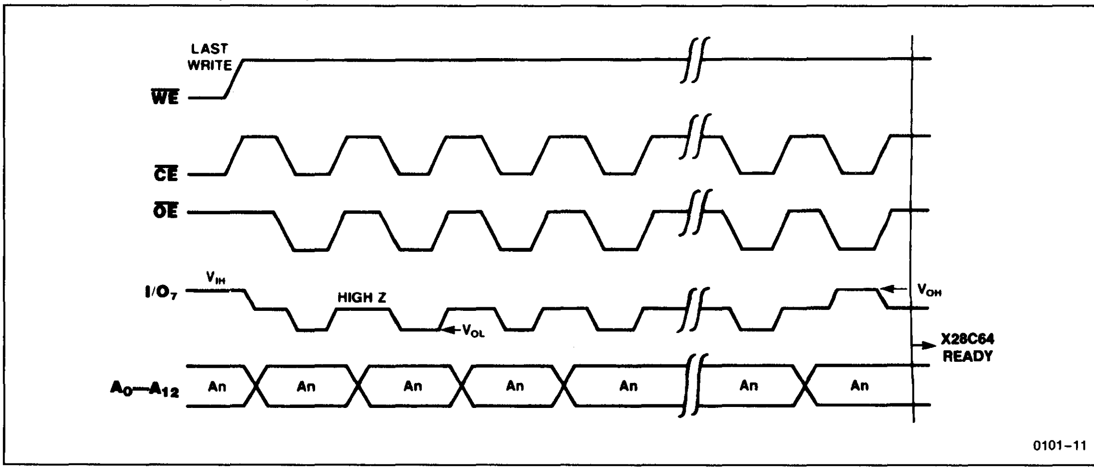
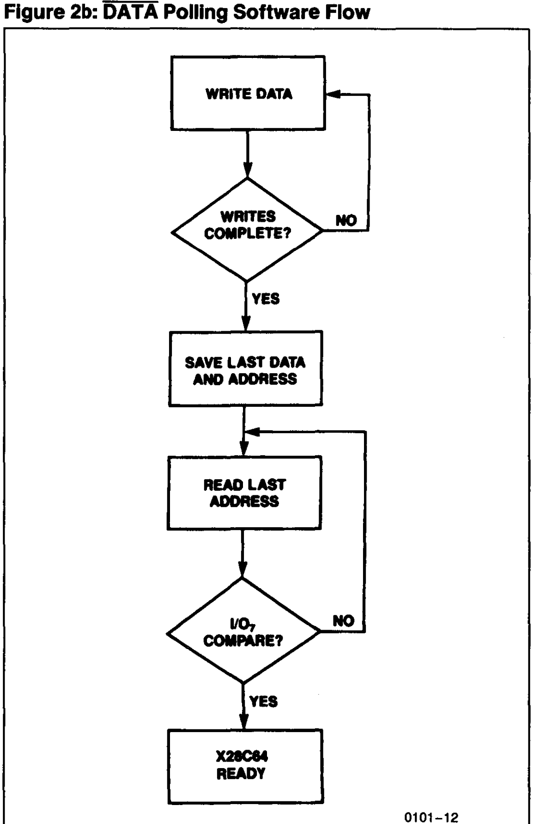


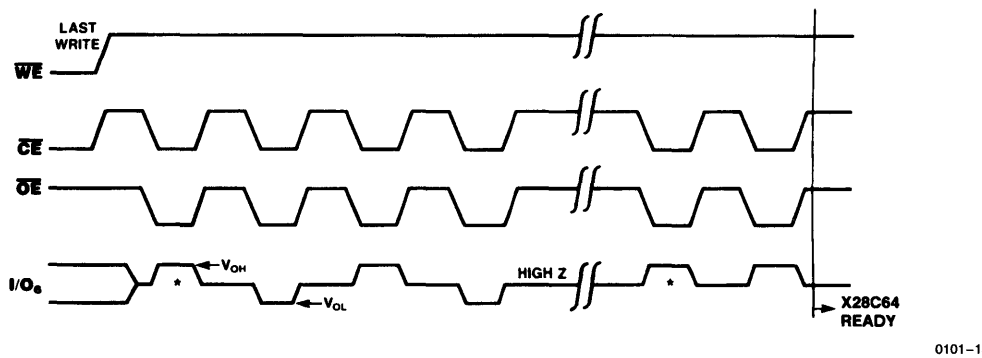
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C64. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

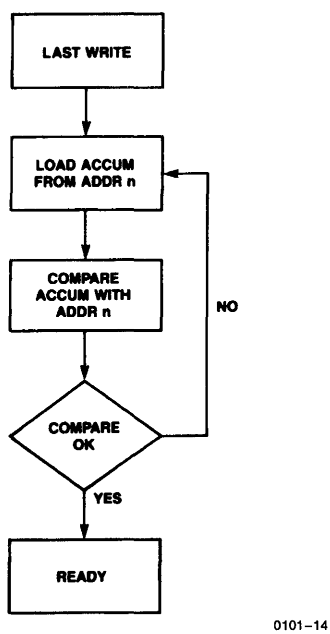
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C64 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C64 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C64 offers a software controlled data protection feature. The X28C64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.(10) Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (10) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

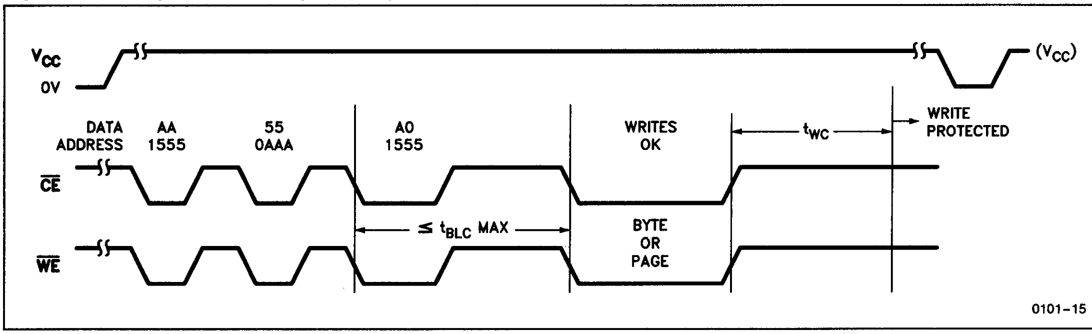
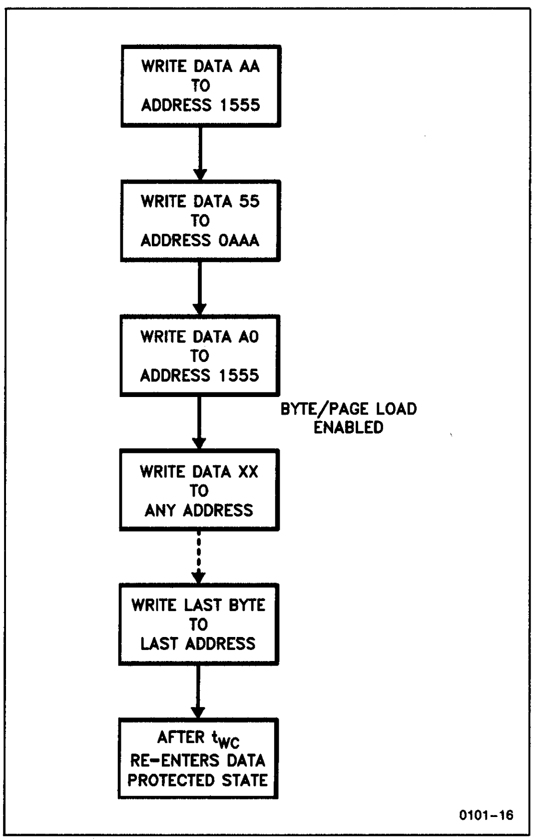


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C64 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

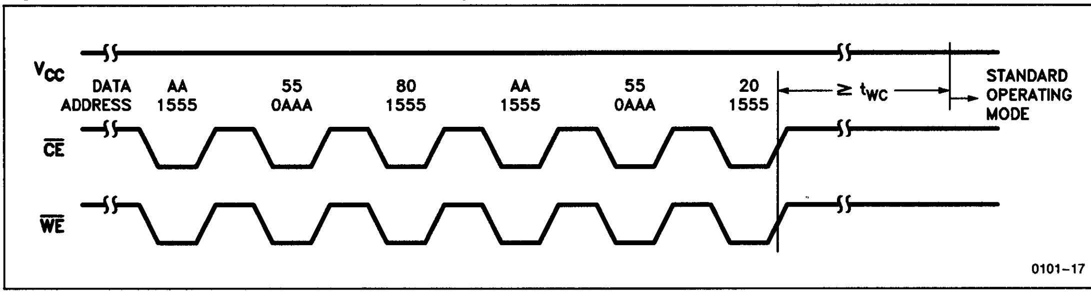
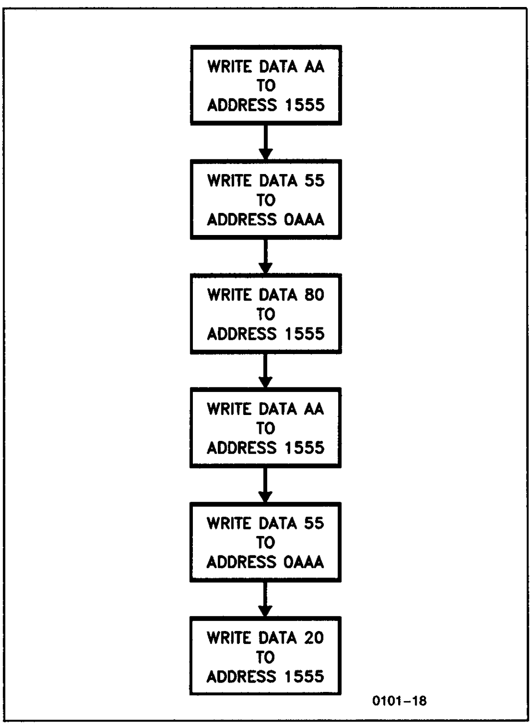


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

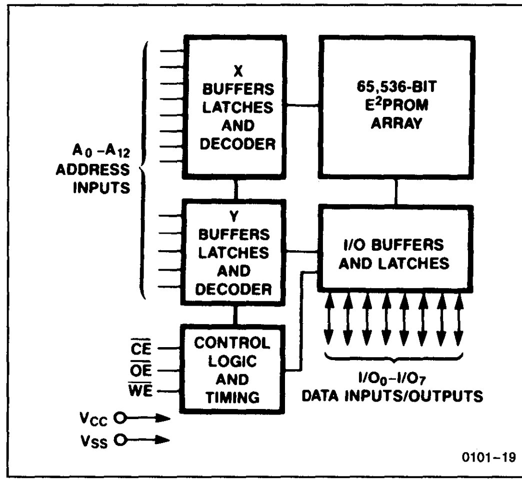
Because the X28C64 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

64K E²PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C64P-20	8192 x 8		•									†	200 ns	CMOS	Standard
X28C64P-25	8192 x 8		•									†	250 ns	CMOS	Standard
X28C64P	8192 x 8		•									†	300 ns	CMOS	Standard
X28C64P-35	8192 x 8		•									†	350 ns	CMOS	Standard
X28C64PI-20	8192 x 8		•									I	200 ns	CMOS	Standard
X28C64PI-25	8192 x 8		•									I	250 ns	CMOS	Standard
X28C64PI	8192 x 8		•									I	300 ns	CMOS	Standard
X28C64PI-35	8192 x 8		•									I	350 ns	CMOS	Standard
X28C64D-20	8192 x 8			•								†	200 ns	CMOS	Standard
X28C64D-25	8192 x 8			•								†	250 ns	CMOS	Standard
X28C64D	8192 x 8			•								†	300 ns	CMOS	Standard
X28C64D-35	8192 x 8			•								†	350 ns	CMOS	Standard
X28C64DI-20	8192 x 8			•								I	200 ns	CMOS	Standard
X28C64DI-25	8192 x 8			•								I	250 ns	CMOS	Standard
X28C64DI	8192 x 8			•								I	300 ns	CMOS	Standard
X28C64DI-35	8192 x 8			•								I	350 ns	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E2PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C64F-20	8192 x 8					•						†	200 ns	CMOS	Standard
X28C64F-25	8192 x 8					•						†	250 ns	CMOS	Standard
X28C64F	8192 x 8					•						†	300 ns	CMOS	Standard
X28C64F-35	8192 x 8					•						†	350 ns	CMOS	Standard
X28C64FI-20	8192 x 8					•						I	200 ns	CMOS	Standard
X28C64FI-25	8192 x 8					•						I	250 ns	CMOS	Standard
X28C64FI	8192 x 8					•						I	300 ns	CMOS	Standard
X28C64FI-35	8192 x 8					•						I	350 ns	CMOS	Standard
X28C64K-20	8192 x 8							•				†	200 ns	CMOS	Standard
X28C64K-25	8192 x 8							•				†	250 ns	CMOS	Standard
X28C64K	8192 x 8							•				†	300 ns	CMOS	Standard
X28C64K-35	8192 x 8							•				†	350 ns	CMOS	Standard
X28C64KI-20	8192 x 8							•				I	200 ns	CMOS	Standard
X28C64KI-25	8192 x 8							•				I	250 ns	CMOS	Standard
X28C64KI	8192 x 8							•				I	300 ns	CMOS	Standard
X28C64KI-35	8192 x 8							•				I	350 ns	CMOS	Standard

Key:

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ORDERING INFORMATION

64K E2PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C64J-20	8192 x 8								•			†	200 ns	CMOS	Standard
X28C64J-25	8192 x 8								•			†	250 ns	CMOS	Standard
X28C64J	8192 x 8								•			†	300 ns	CMOS	Standard
X28C64J-35	8192 x 8								•			†	350 ns	CMOS	Standard
X28C64JI-20	8192 x 8								•			I	200 ns	CMOS	Standard
X28C64JI-25	8192 x 8								•			I	250 ns	CMOS	Standard
X28C64JI	8192 x 8								•			I	300 ns	CMOS	Standard
X28C64JI-35	8192 x 8								•			I	350 ns	CMOS	Standard
X28C64E-20	8192 x 8									•		†	200 ns	CMOS	Standard
X28C64E-25	8192 x 8									•		†	250 ns	CMOS	Standard
X28C64E	8192 x 8									•		†	300 ns	CMOS	Standard
X28C64E-35	8192 x 8									•		†	350 ns	CMOS	Standard
X28C64EI-20	8192 x 8									•		I	200 ns	CMOS	Standard
X28C64EI-25	8192 x 8									•		I	250 ns	CMOS	Standard
X28C64EI	8192 x 8									•		I	300 ns	CMOS	Standard
X28C64EI-35	8192 x 8									•		I	350 ns	CMOS	Standard

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E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E^2PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C64G-20	8192 x 8										•	†	200 ns	CMOS	Standard
X28C64G-25	8192 x 8										•	†	250 ns	CMOS	Standard
X28C64G	8192 x 8										•	†	300 ns	CMOS	Standard
X28C64G-35	8192 x 8										•	†	350 ns	CMOS	Standard
X28C64GI-20	8192 x 8										•	I	200 ns	CMOS	Standard
X28C64GI-25	8192 x 8										•	I	250 ns	CMOS	Standard
X28C64GI	8192 x 8										•	I	300 ns	CMOS	Standard
X28C64GI-35	8192 x 8										•	I	350 ns	CMOS	Standard

Key:

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I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
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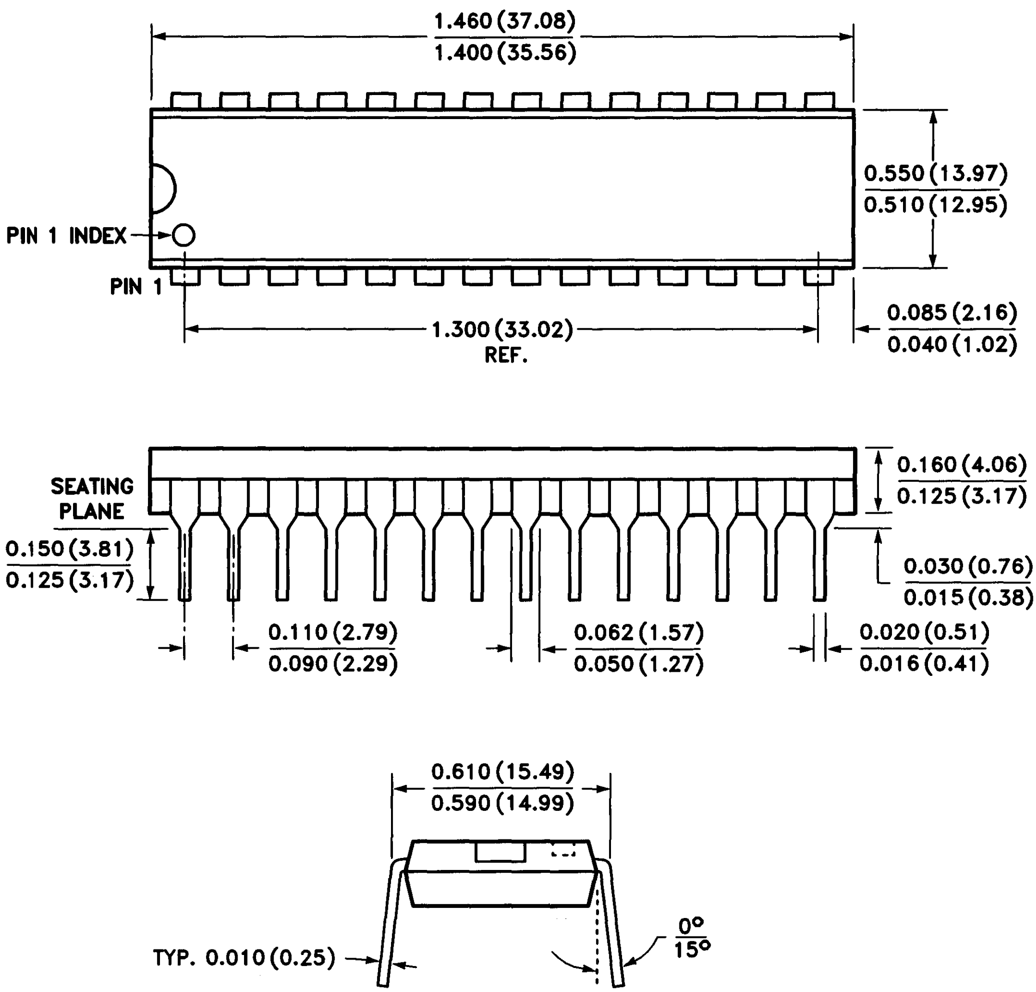
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P

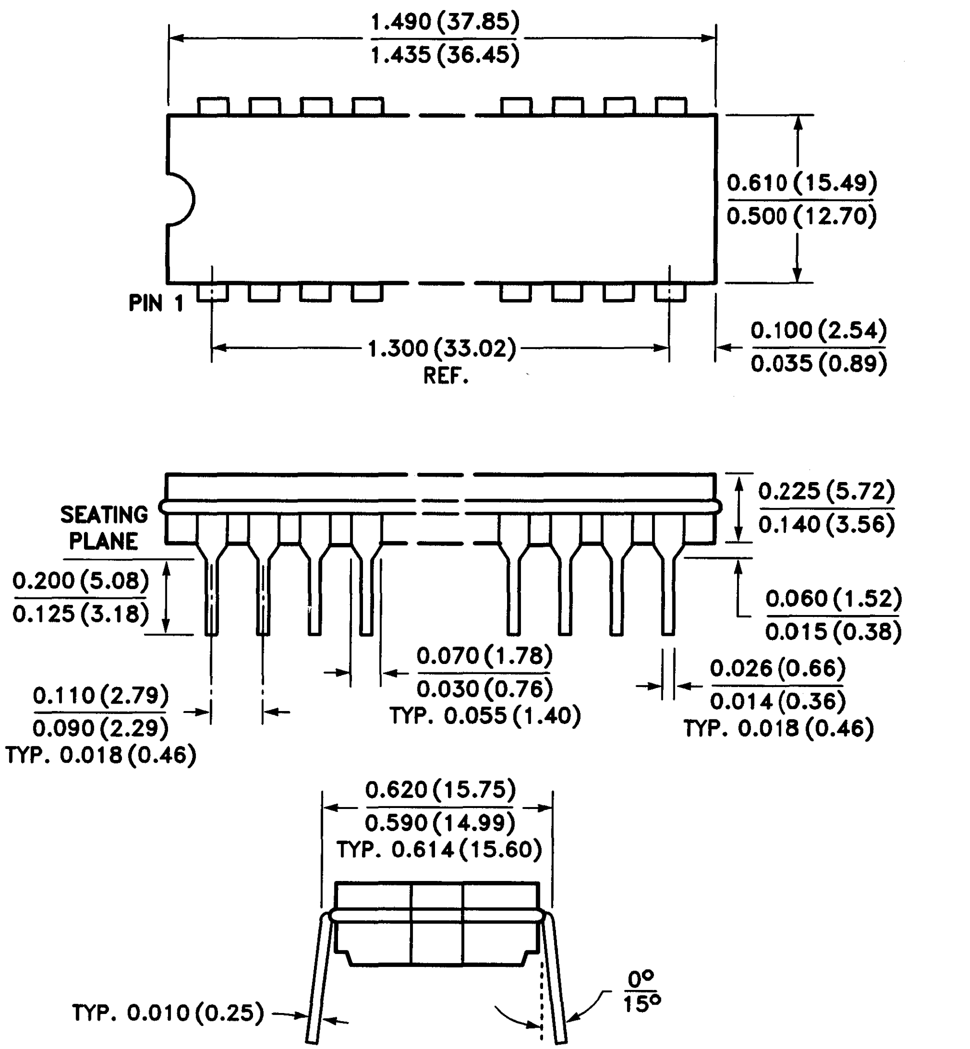


PPI028

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

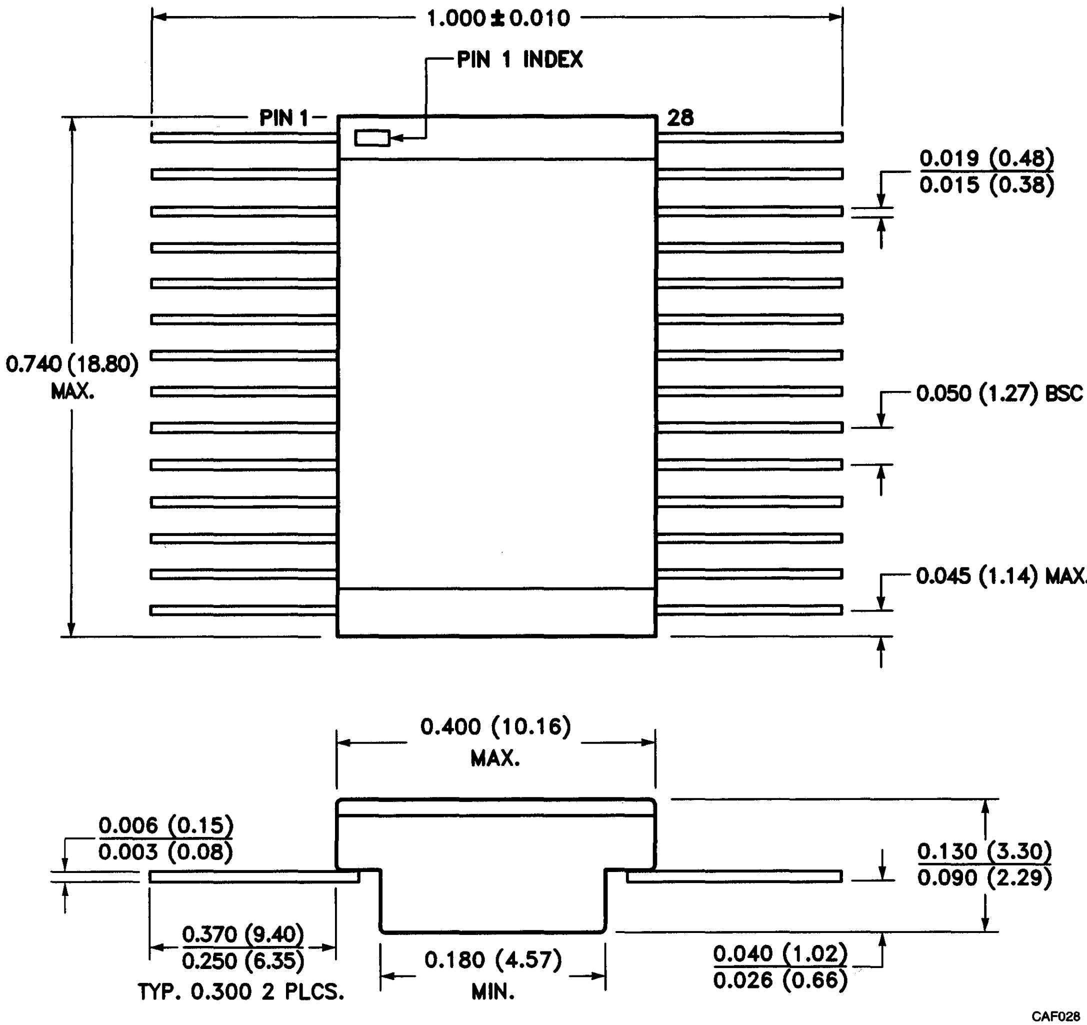
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

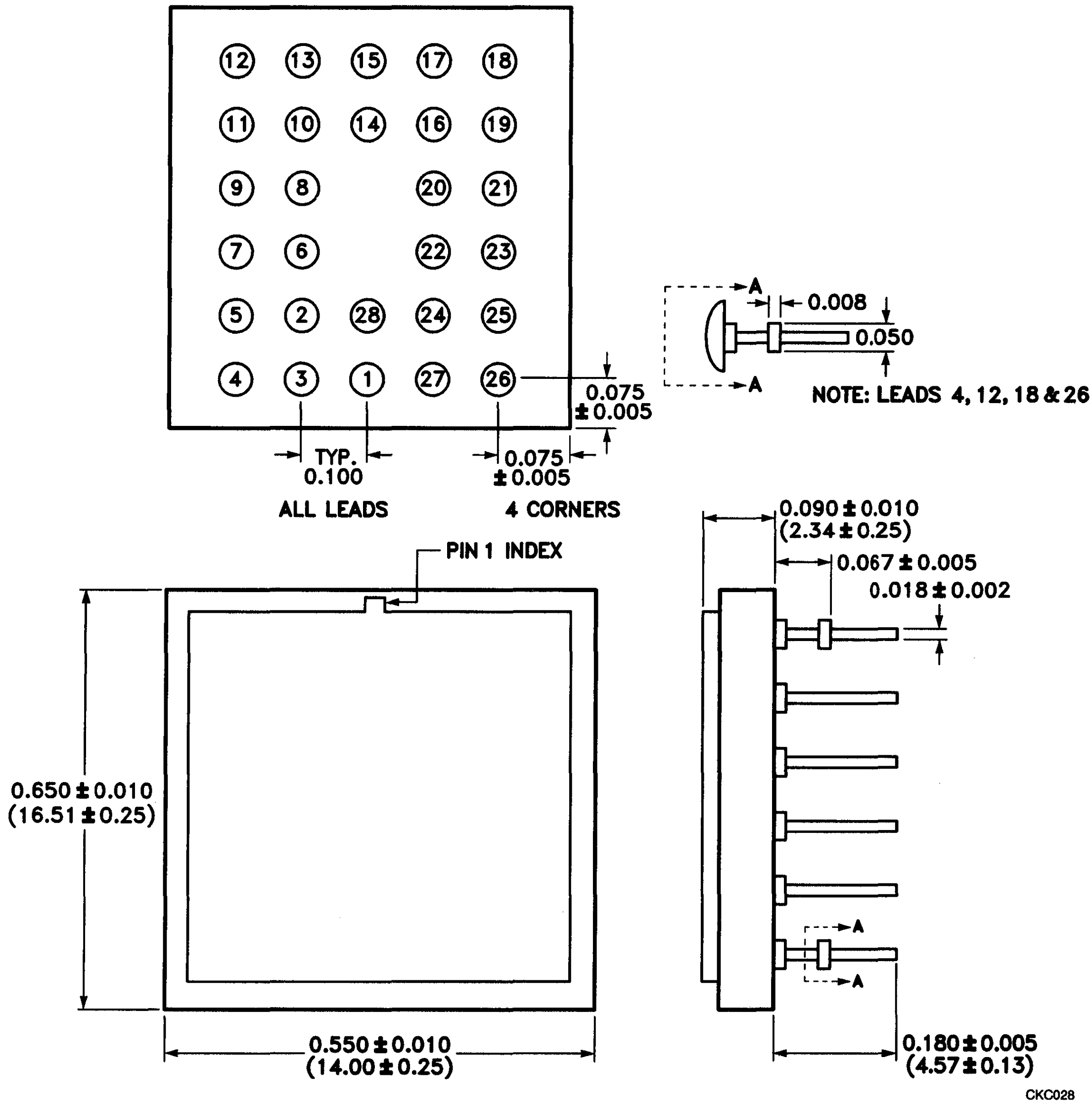
28-LEAD CERAMIC FLAT PACK TYPE F1



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B, X2864H AND X28C64

PACKAGING INFORMATION

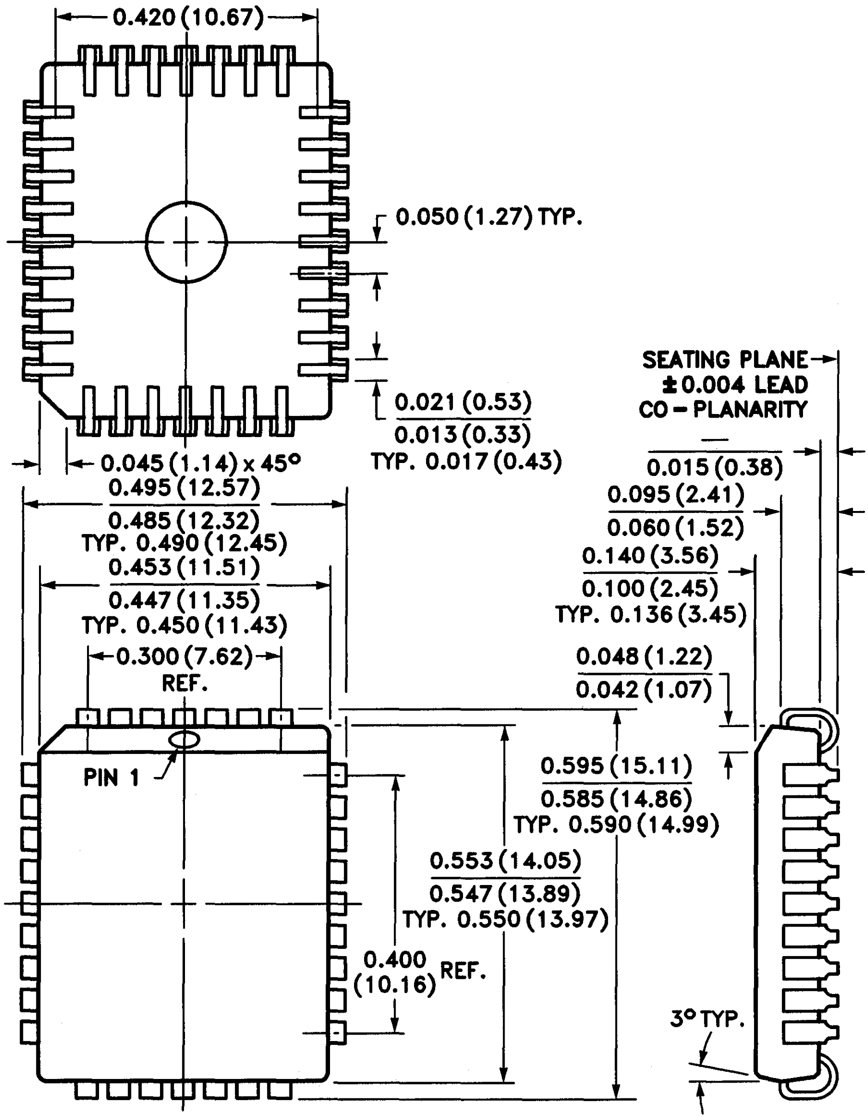
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

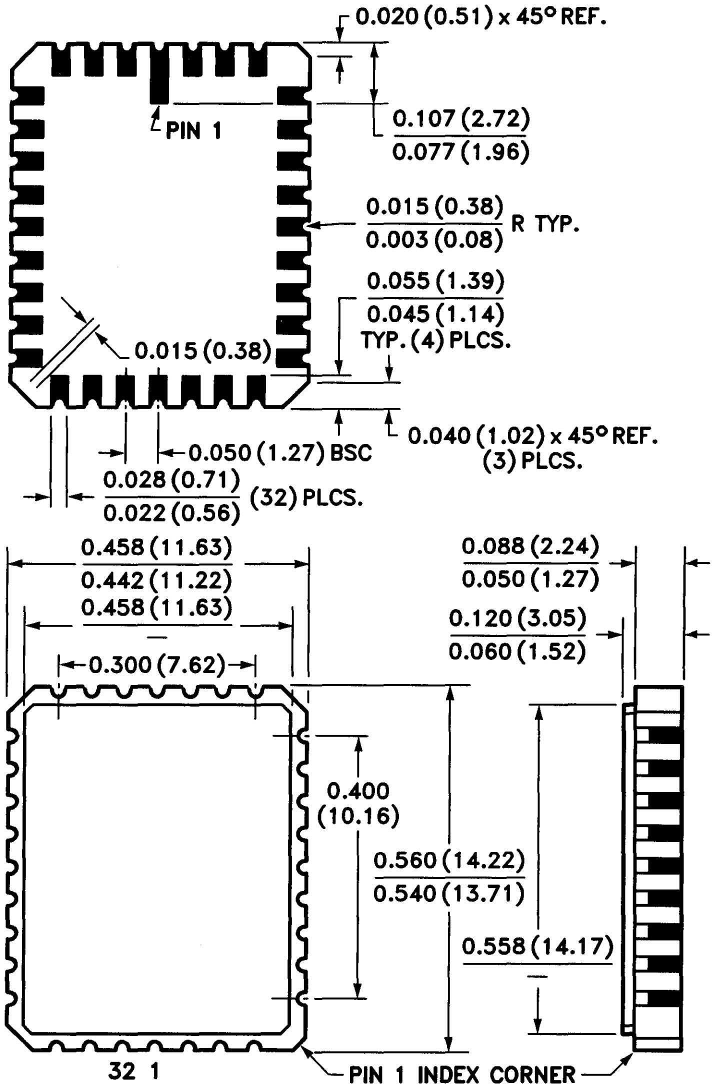
32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



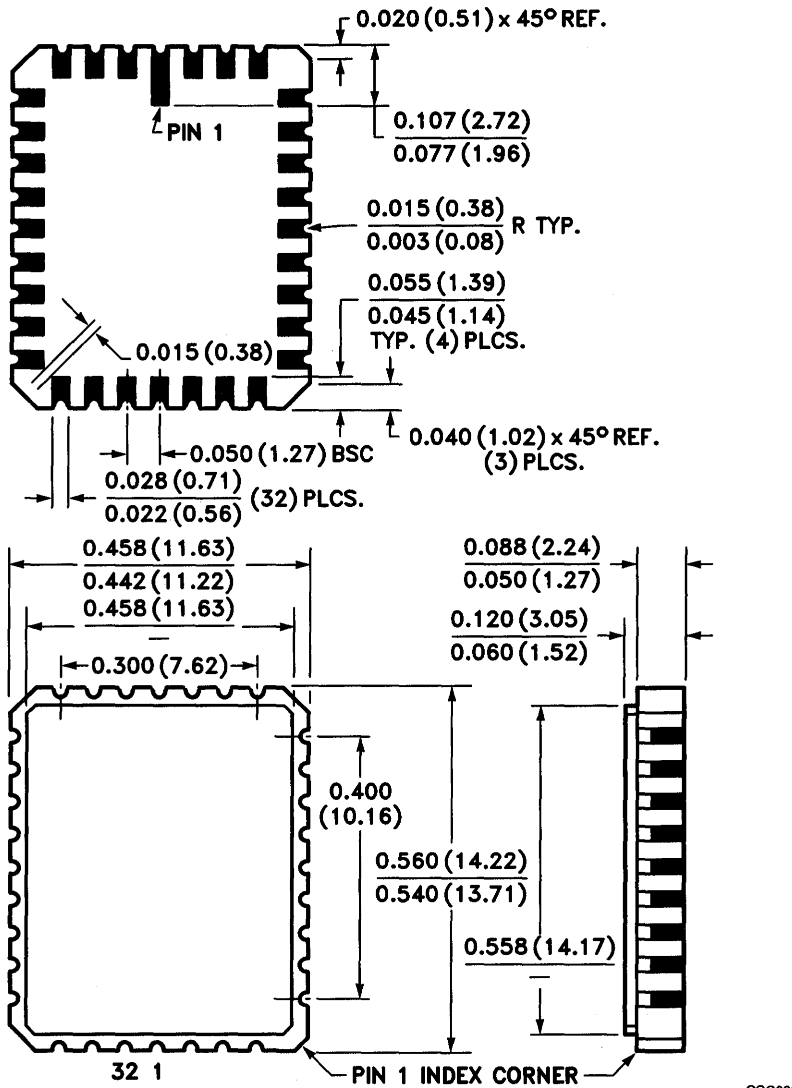
CEG032

NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

NOTES

NOTES

NOTES

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Fax: 312/490-0637

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TWX: 510-101-0110
Fax: 714/752-8634

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TWX: 910-379-0033
Fax: 408/432-0640

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Fax: 44.993.841.029

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Telex: 5213883
Fax: (49) 89/4605472

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USA
Phone: 408/432-8888
TWX: 910-379-0033
Fax: 408/432-0640

64K Military X28C64M 8K x 8 Bit

Electrically Erasable PROM

FEATURES

- LOW Power CMOS
  - —60 mA Active Current Max.
  - —200 μA Standby Current Max.
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 0.625 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

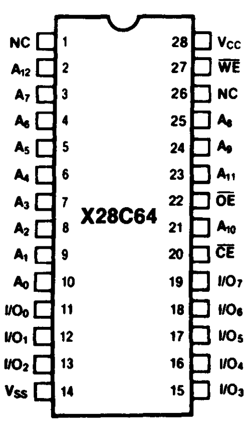
The Xicor X28C64 is a 8K x 8 E^{2}PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C64 is a 5V only device. The X28C64 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C64 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in 0.625 seconds. The X28C64 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C64 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

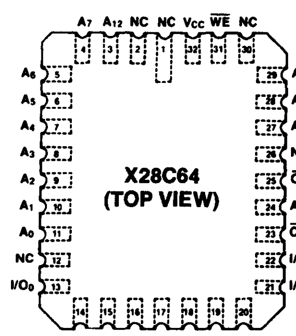
PIN CONFIGURATIONS

CERDIP
FLAT PACK



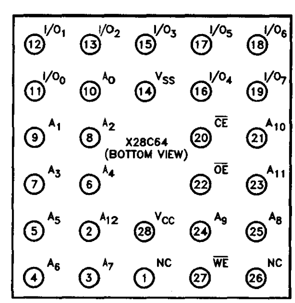
0100-1

LCC



0100-2

PGA



0100-3

PIN NAMES

A_0–A_{12}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	μA	$\overline{CE} = \overline{WE} = V_{CC} - 0.3V$ All I/O's = Open Other Inputs = Don't Care
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(3)	Power-Up to Read Operation	100	μs
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

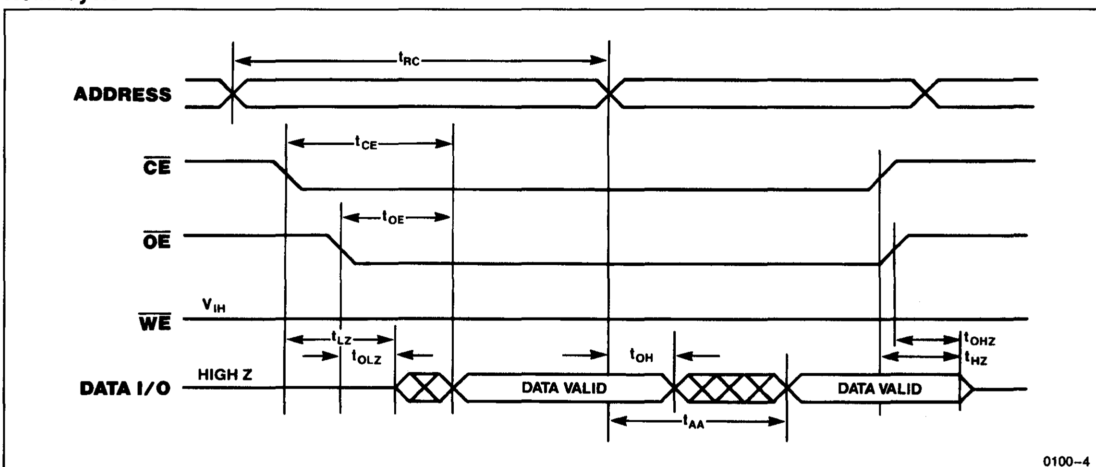
A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C64M-20		X28C64M-25		X28C64M		X28C64M-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		350		ns
t_{CE}	Chip Enable Access Time		200		250		300		350	ns
t_{AA}	Address Access Time		200		250		300		350	ns
t_{OE}	Output Enable Access Time		80		100		100		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



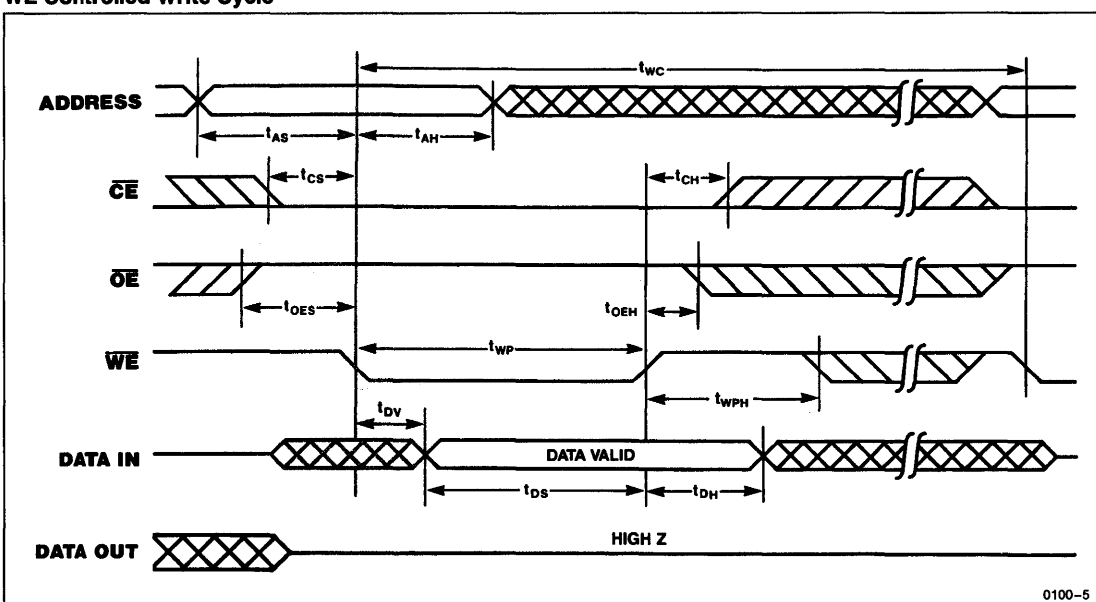
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

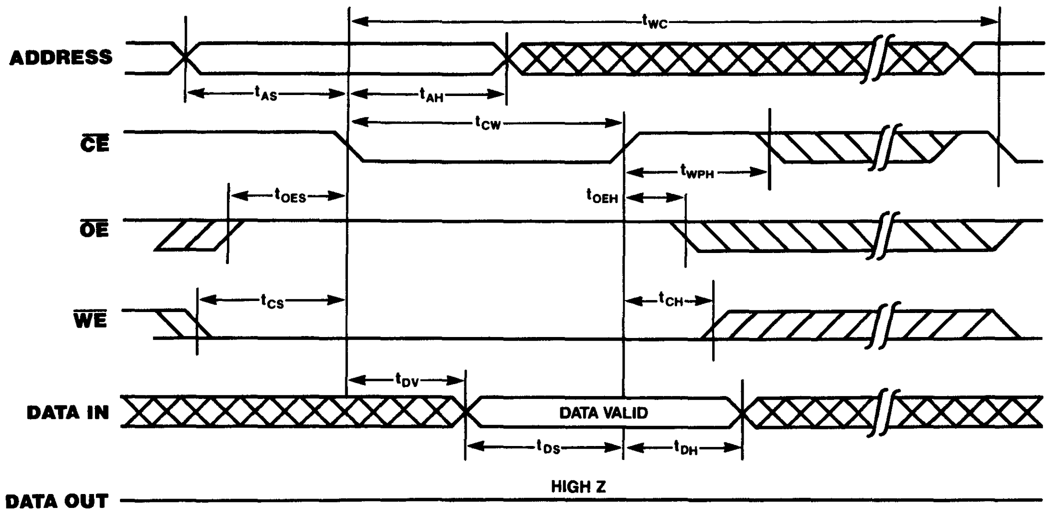
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	200			ns
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle



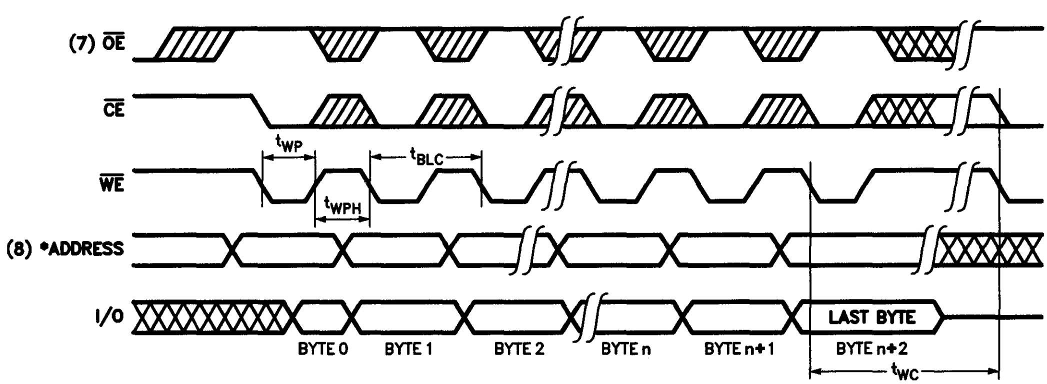
Note: (6) Typical values are for T_A = 25°C and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



0100-6

Page Write Cycle



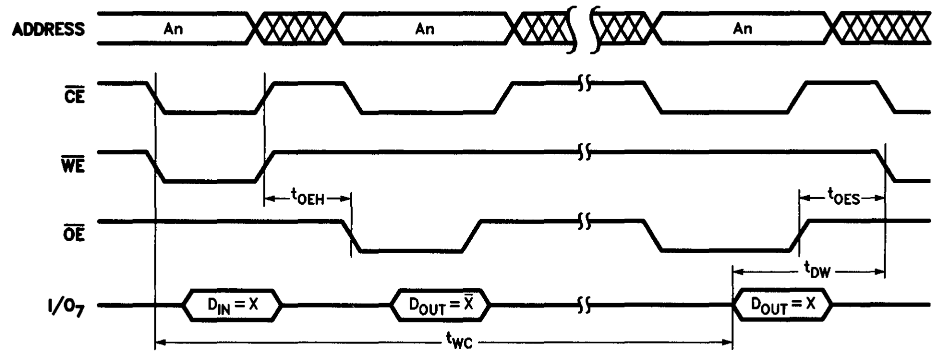
0100-7

*For each successive write within the page write operation, A_6–A_{12} should be the same or writes to an unknown address could occur.

Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

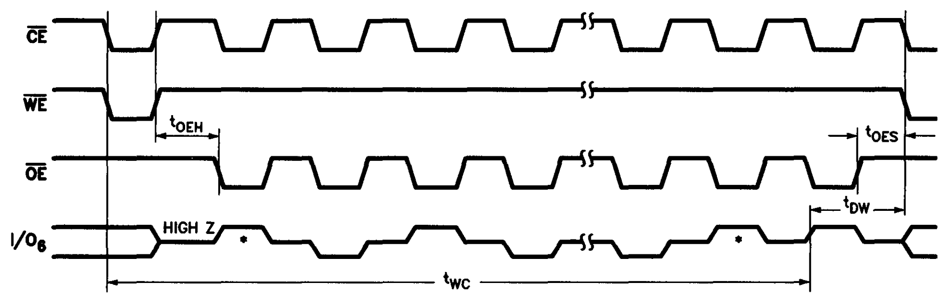
(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)



0100-9

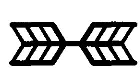
Toggle Bit Timing Diagram(9)



0100-8

* I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C64 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C64.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

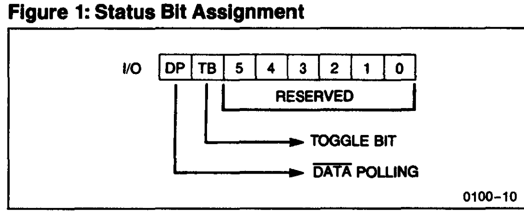
The page write feature of the X28C64 allows the entire memory to be written in 0.625 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C64 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{12}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits

The X28C64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C64 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C64 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O$_7$

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

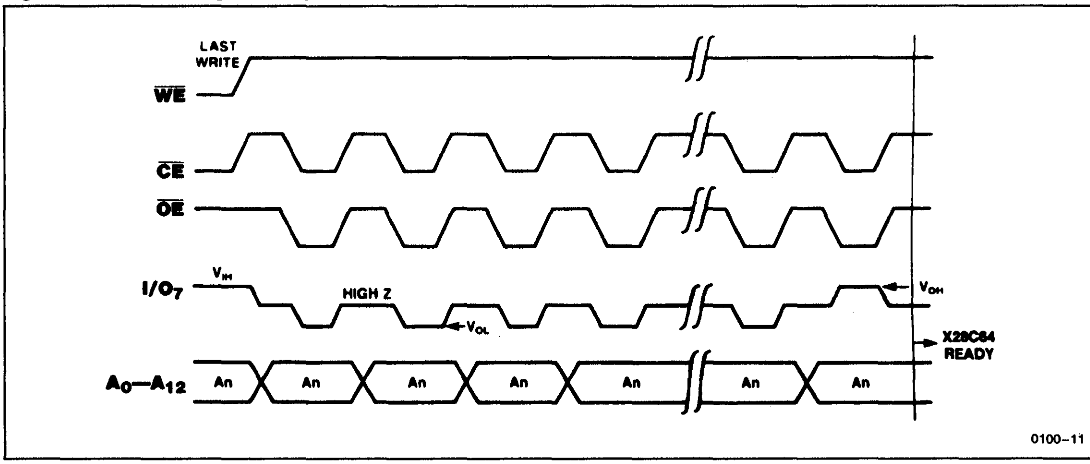
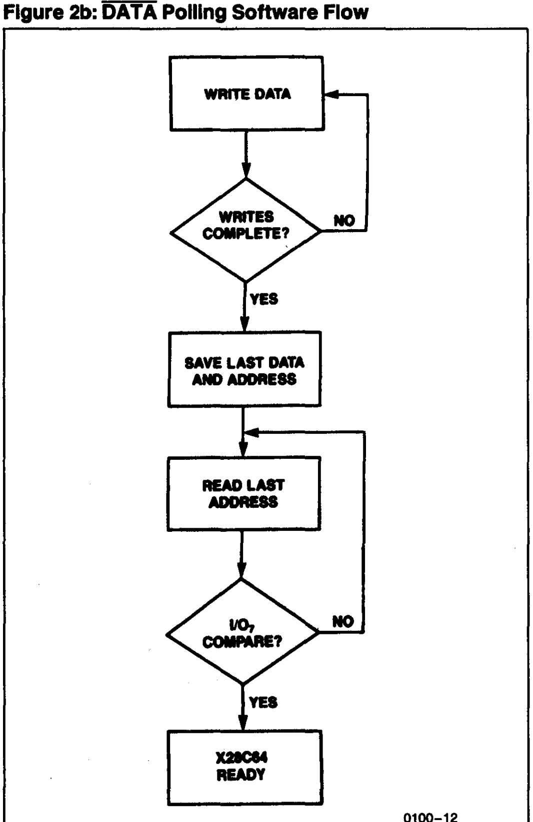


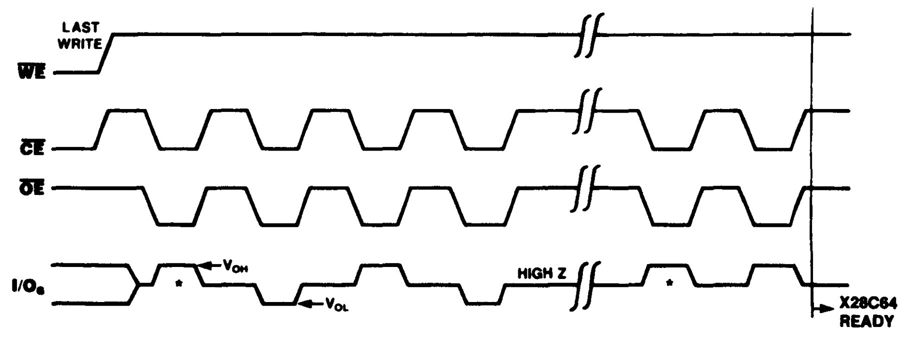
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C64. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

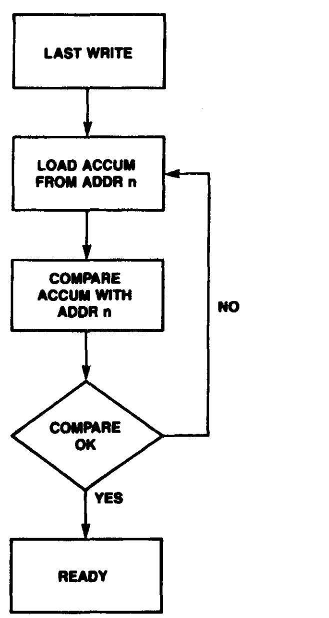
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C64 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C64 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C64 offers a software controlled data protection feature. The X28C64 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C64 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.[10] Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (10) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

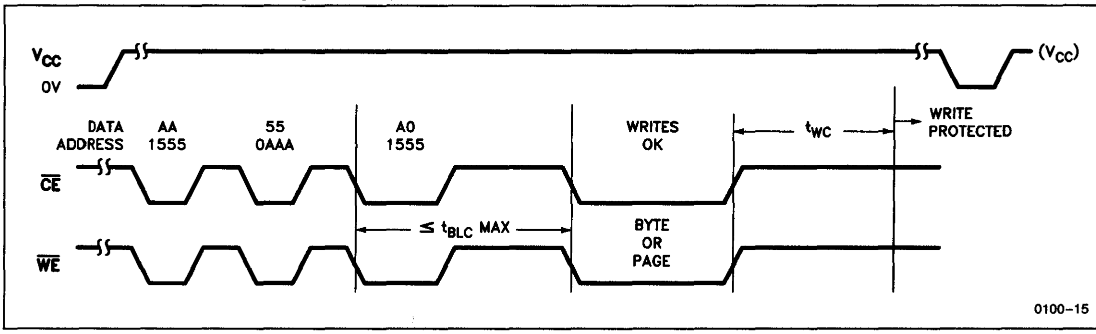
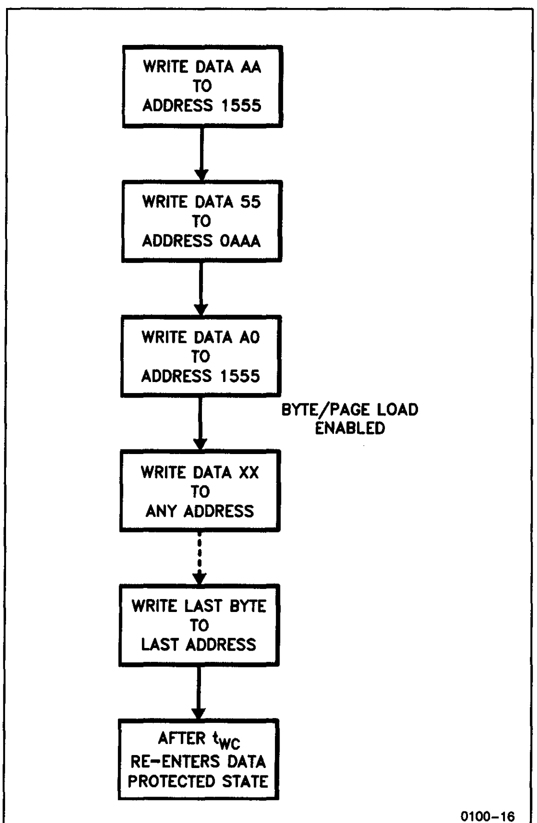


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C64 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

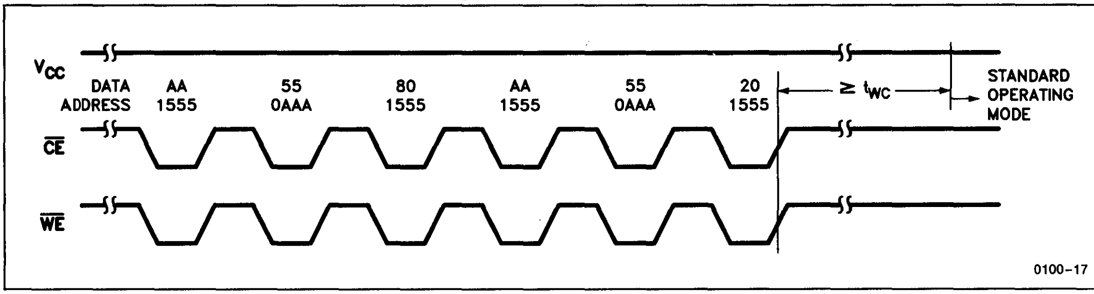
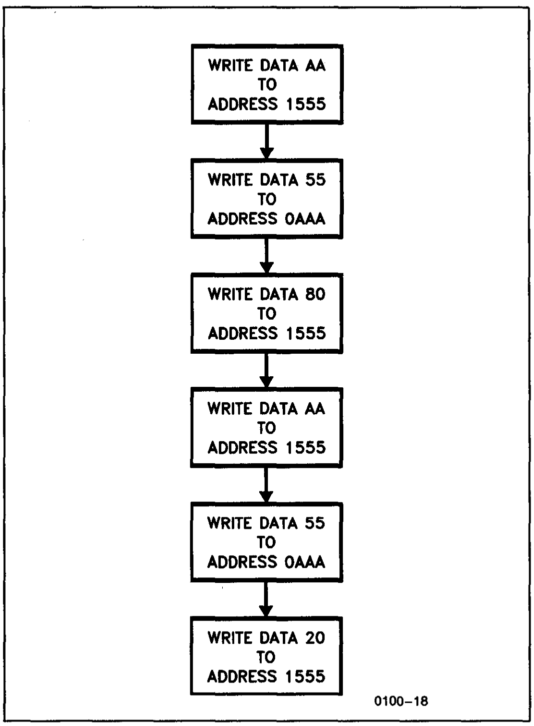


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E[2]PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

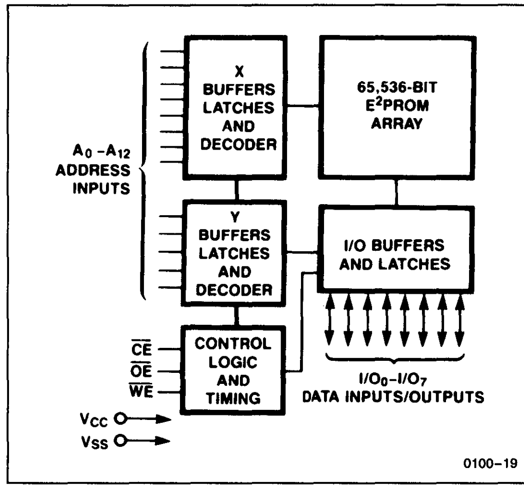
Because the X28C64 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

64K E²PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C64DM-20	8192 x 8			•								M	200 ns	CMOS	Standard
X28C64DM-25	8192 x 8			•								M	250 ns	CMOS	Standard
X28C64DM	8192 x 8			•								M	300 ns	CMOS	Standard
X28C64DM-35	8192 x 8			•								M	350 ns	CMOS	Standard
X28C64DMB-20	8192 x 8			•								M	200 ns	CMOS	883 Rev. C, Class B
X28C64DMB-25	8192 x 8			•								M	250 ns	CMOS	883 Rev. C, Class B
X28C64DMB	8192 x 8			•								M	300 ns	CMOS	883 Rev. C, Class B
X28C64DMB-35	8192 x 8			•								M	350 ns	CMOS	883 Rev. C, Class B
X28C64FM-20	8192 x 8					•						M	200 ns	CMOS	Standard
X28C64FM-25	8192 x 8					•						M	250 ns	CMOS	Standard
X28C64FM	8192 x 8					•						M	300 ns	CMOS	Standard
X28C64FM-35	8192 x 8					•						M	350 ns	CMOS	Standard
X28C64FMB-20	8192 x 8					•						M	200 ns	CMOS	883 Rev. C, Class B
X28C64FMB-25	8192 x 8					•						M	250 ns	CMOS	883 Rev. C, Class B
X28C64FMB	8192 x 8					•						M	300 ns	CMOS	883 Rev. C, Class B
X28C64FMB-35	8192 x 8					•						M	350 ns	CMOS	883 Rev. C, Class B

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C64KM-20	8192 x 8							•				M	200 ns	CMOS	Standard
X28C64KM-25	8192 x 8							•				M	250 ns	CMOS	Standard
X28C64KM	8192 x 8							•				M	300 ns	CMOS	Standard
X28C64KM-35	8192 x 8							•				M	350 ns	CMOS	Standard
X28C64KMB-20	8192 x 8							•				M	200 ns	CMOS	883 Rev. C, Class B
X28C64KMB-25	8192 x 8							•				M	250 ns	CMOS	883 Rev. C, Class B
X28C64KMB	8192 x 8							•				M	300 ns	CMOS	883 Rev. C, Class B
X28C64KMB-35	8192 x 8							•				M	350 ns	CMOS	883 Rev. C, Class B
X28C64EM-20	8192 x 8									•		M	200 ns	CMOS	Standard
X28C64EM-25	8192 x 8									•		M	250 ns	CMOS	Standard
X28C64EM	8192 x 8									•		M	300 ns	CMOS	Standard
X28C64EM-35	8192 x 8									•		M	350 ns	CMOS	Standard
X28C64EMB-20	8192 x 8									•		M	200 ns	CMOS	883 Rev. C, Class B
X28C64EMB-25	8192 x 8									•		M	250 ns	CMOS	883 Rev. C, Class B
X28C64EMB	8192 x 8									•		M	300 ns	CMOS	883 Rev. C, Class B
X28C64EMB-35	8192 x 8									•		M	350 ns	CMOS	883 Rev. C, Class B

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

64K E²PROMs (Continued)

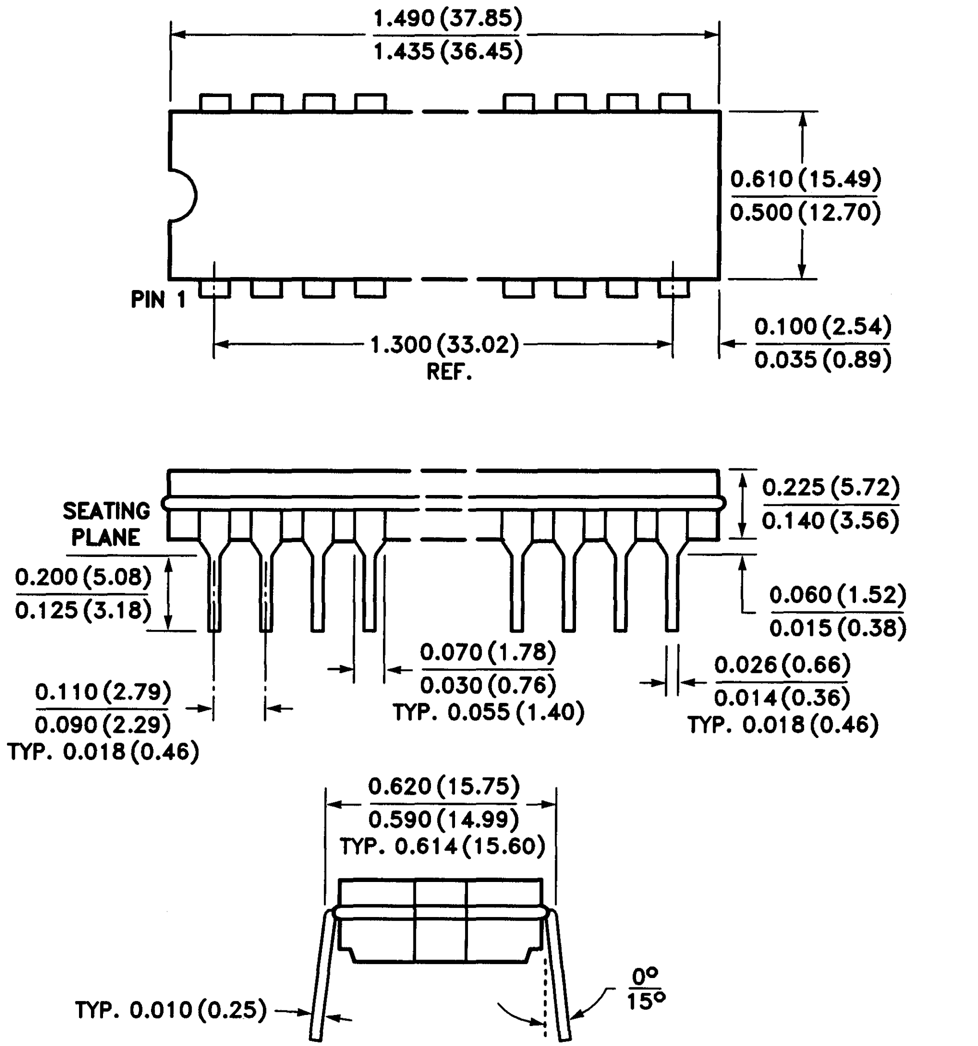
Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C64GM-20	8192 x 8										•	M	200 ns	CMOS	Standard
X28C64GM-25	8192 x 8										•	M	250 ns	CMOS	Standard
X28C64GM	8192 x 8										•	M	300 ns	CMOS	Standard
X28C64GM-35	8192 x 8										•	M	350 ns	CMOS	Standard
X28C64GMB-20	8192 x 8										•	M	200 ns	CMOS	883 Rev. C, Class B
X28C64GMB-25	8192 x 8										•	M	250 ns	CMOS	883 Rev. C, Class B
X28C64GMB	8192 x 8										•	M	300 ns	CMOS	883 Rev. C, Class B
X28C64GMB-35	8192 x 8										•	M	350 ns	CMOS	883 Rev. C, Class B

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = 28-Lead Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

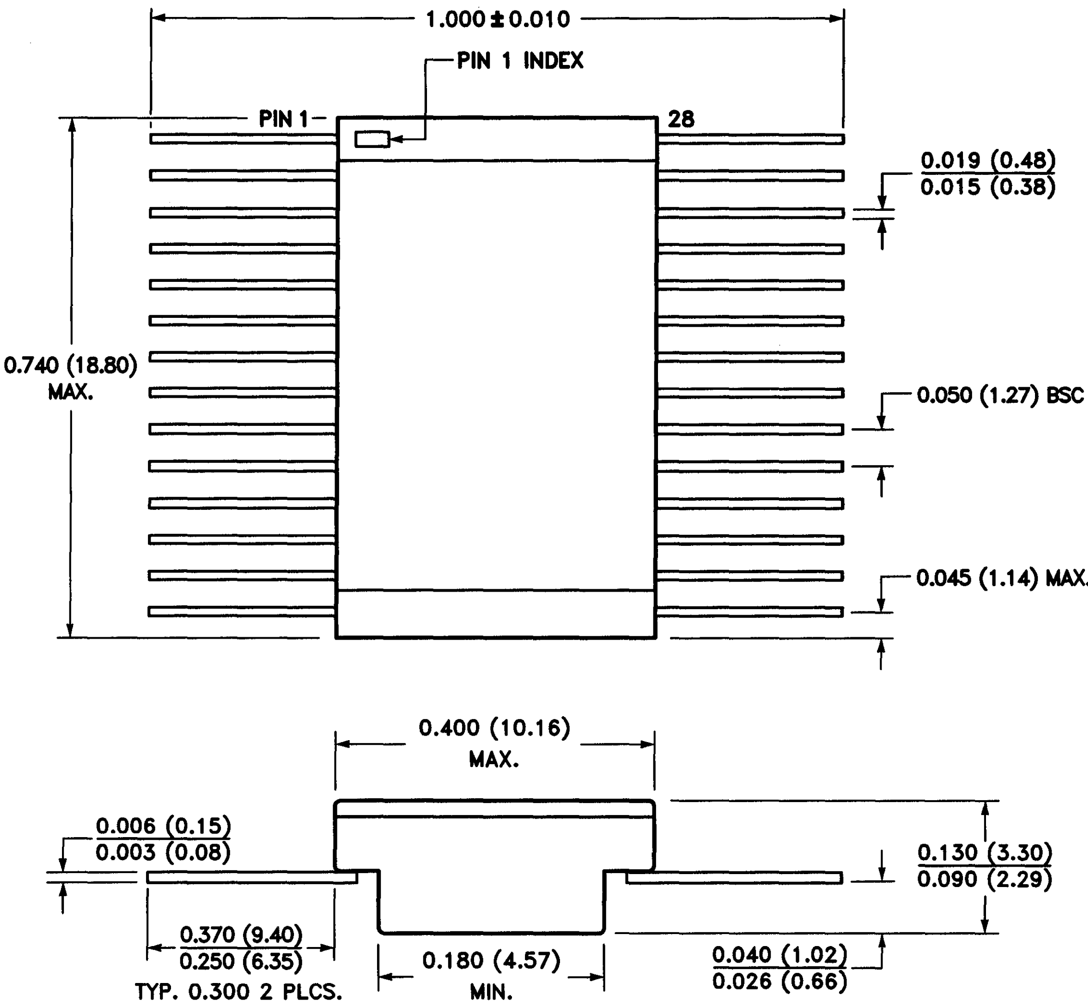
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F1

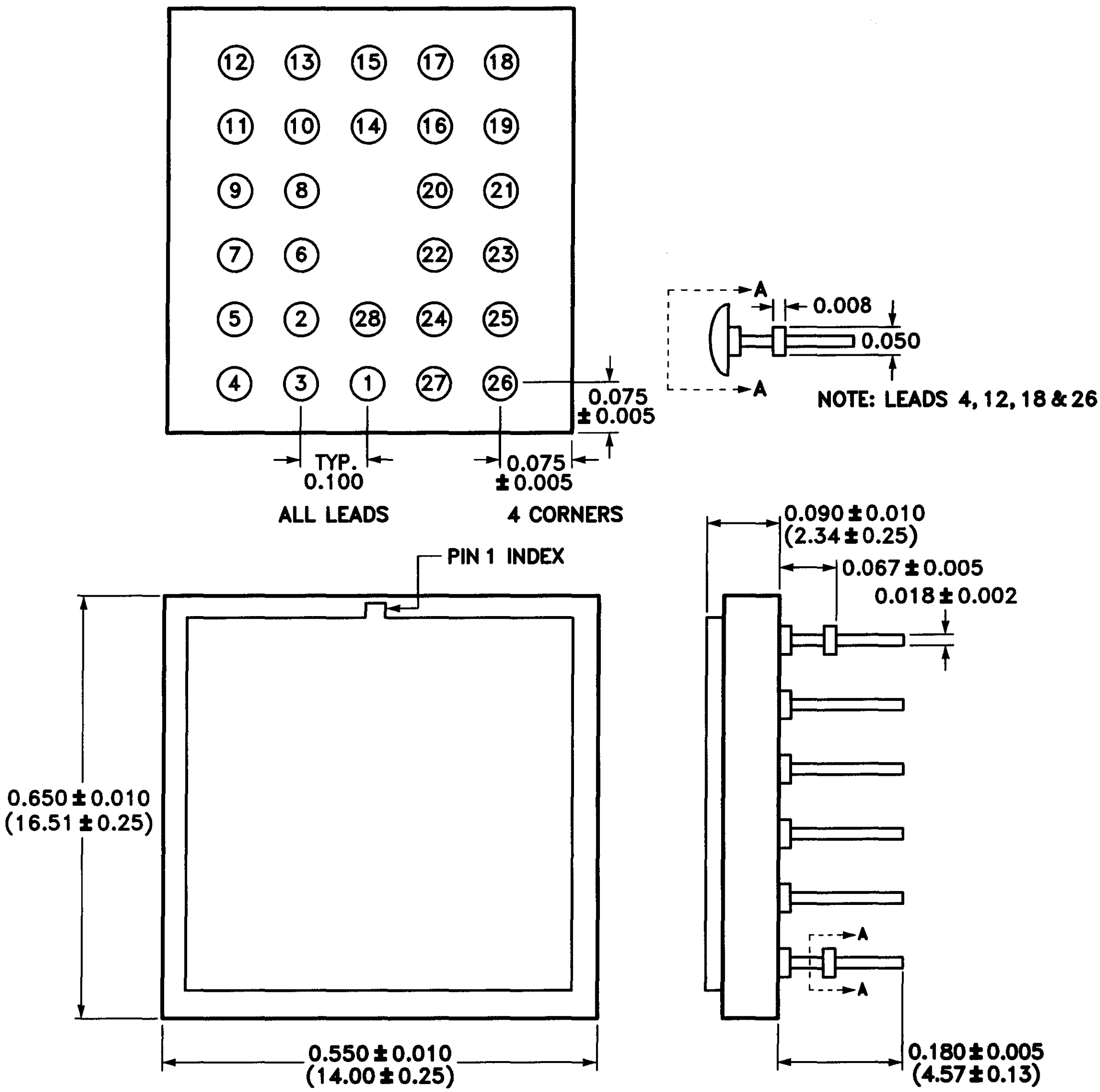


NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X2864A, X2864B, X2864H AND X28C64

PACKAGING INFORMATION

28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K

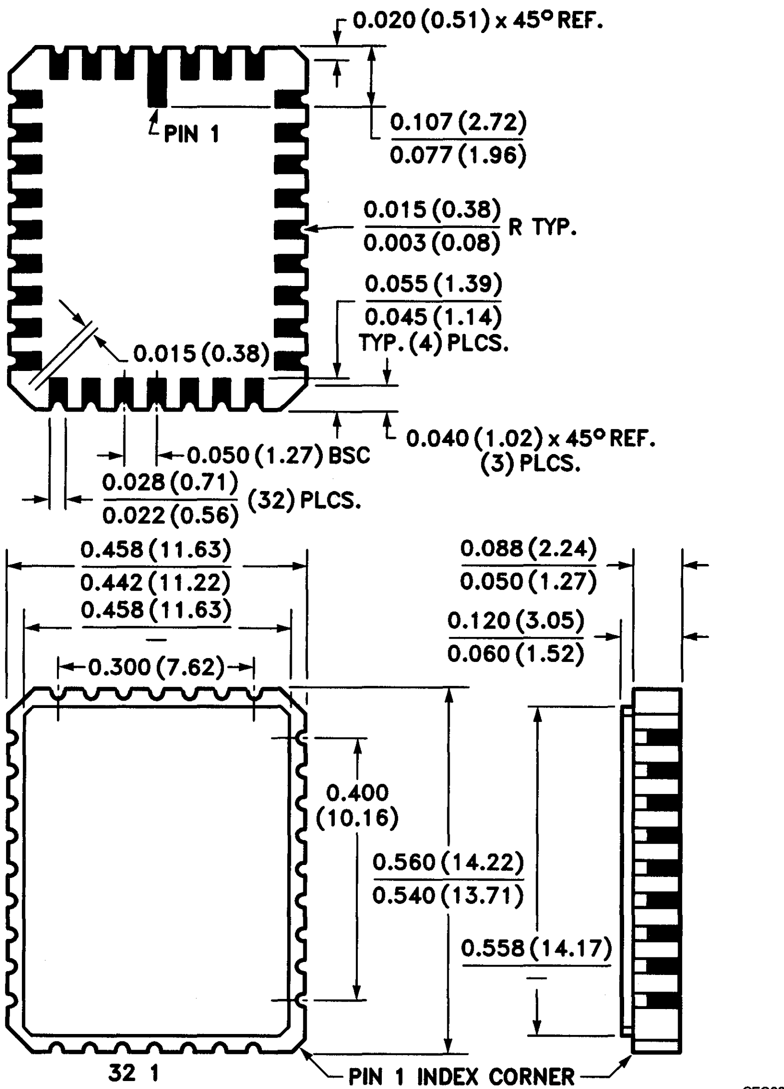


CKC028

NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

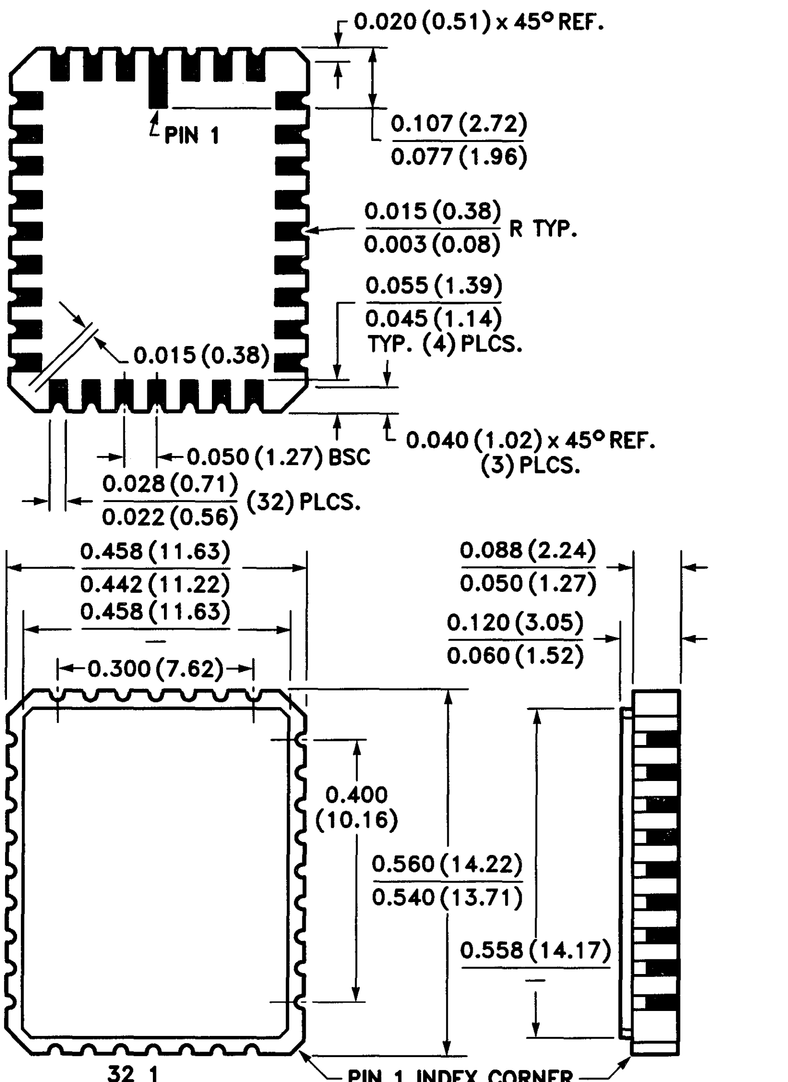


NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

NOTES

NOTES

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U.S. Sales Offices

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Telex: 230853137
Fax: 203/794-9501

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TWX: 910-997-3663
Fax: 312/490-0637

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Telex: 62027057
Fax: 214/644-5835

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Fax: 714/752-8634

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Fax: 408/432-0640

256K	Commercial Industrial	X28C256 X28C256I	32K x 8 Bit

Electrically Erasable PROM

FEATURES

- LOW Power CMOS
  - —60 mA Active Current Max.
  - —200 μA Standby Current Max.
- Fast Write Cycle Times
  - —64-Byte Page Write Operation
  - —Byte or Page Write Cycle: 5 ms Typical
  - —Complete Memory Rewrite: 2.5 Sec. Typical
  - —Effective Byte Write Cycle Time: 78 μs Typical
- Software Data Protection
- End of Write Detection
  - —$\overline{\text{DATA}}$ Polling
  - —Toggle Bit
- Simple Byte and Page Write
  - —Single TTL Compatible $\overline{\text{WE}}$ Signal
  - —Internally Latched Address and Data
  - —Automatic Write Timing
- Upward Compatible with X2864A
- JEDEC Approved Byte-Wide Pinout

DESCRIPTION

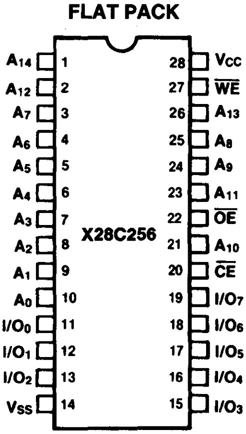
The Xicor X28C256 is a 32K x 8 E²PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E²PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

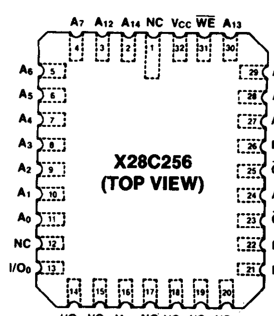
PIN CONFIGURATIONS

PLASTIC
CERDIP
FLAT PACK



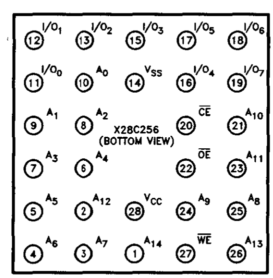
0067-1

PLCC
LCC



0067-2

PGA



0067-21

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
- X28C256 .... −10°C to +85°C
- X28C256I .... −65°C to +135°C

Storage Temperature .... −65°C to +150°C

Voltage on any Pin with Respect to Ground .... −1.0V to +7V

D.C. Output Current .... 5 mA

Lead Temperature (Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28C256 $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.
X28C256I $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	μA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} +1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-Up to Read Operation	100	μs
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, $V_{CC} = 5V$

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O} = 0V$
C_{IN}(3)	Input Capacitance	6	pF	$V_{IN} = 0V$

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for $T_A = 25°C$ and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

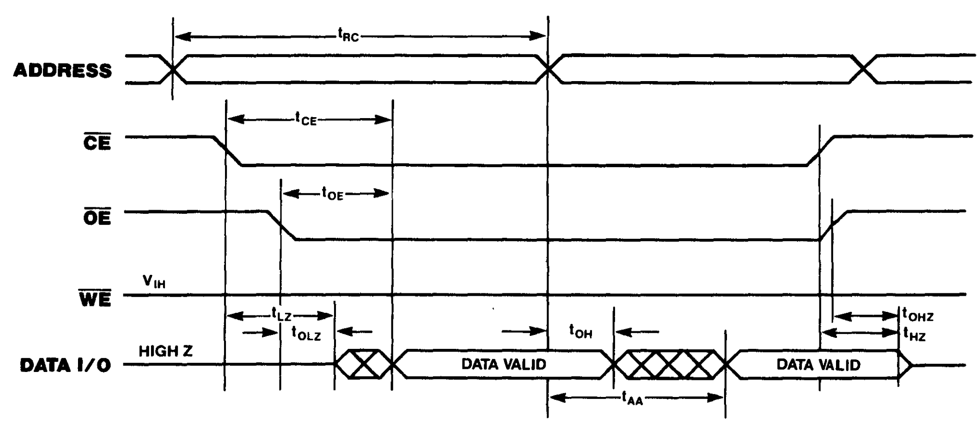
A.C. CHARACTERISTICS

X28C256 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C256I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C256-20 X28C256I-20		X28C256-25 X28C256I-25		X28C256 X28C256I		X28C256-35 X28C256I-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		350		ns
t_{CE}	Chip Enable Access Time		200		250		300		350	ns
t_{AA}	Address Access Time		200		250		300		350	ns
t_{OE}	Output Enable Access Time		80		100		100		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



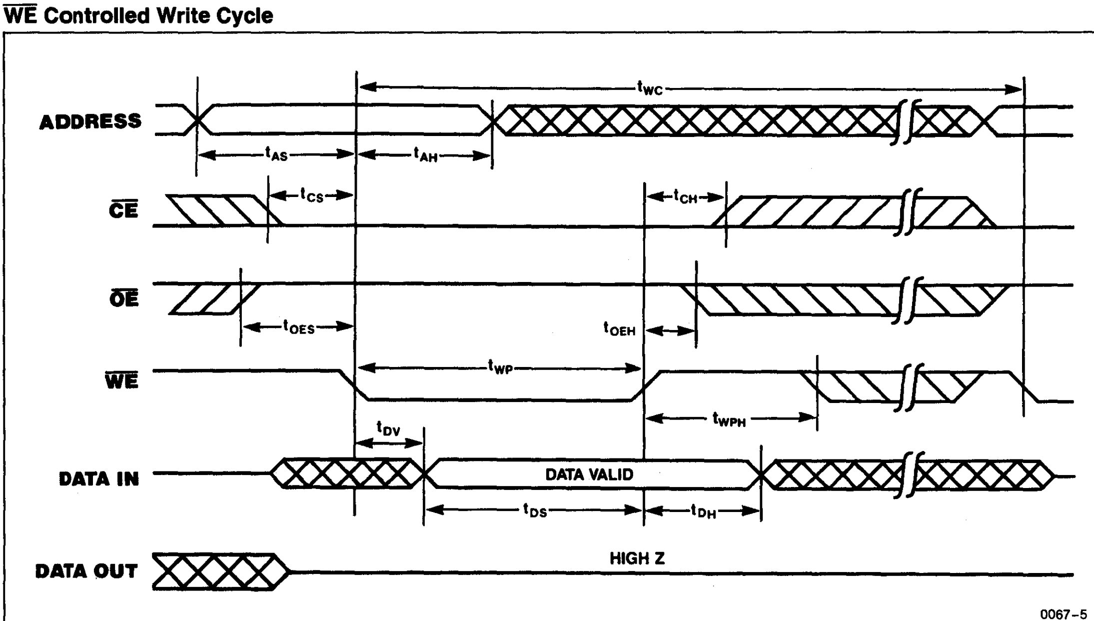
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

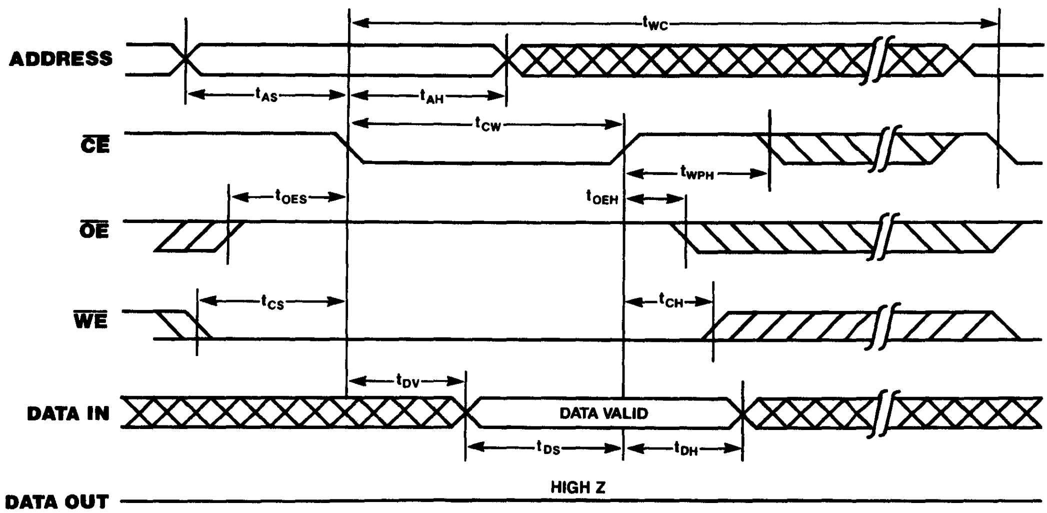
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	200			ns
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle



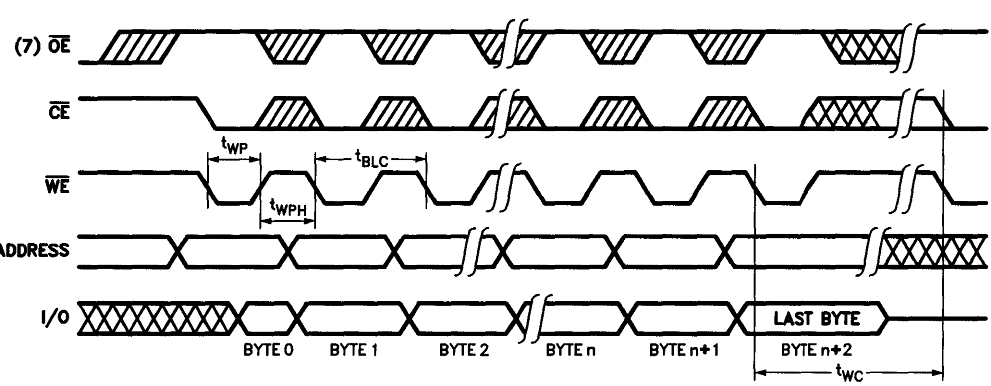
Note: (6) Typical values are for T_A = 25°C and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



0067-6

Page Write Cycle



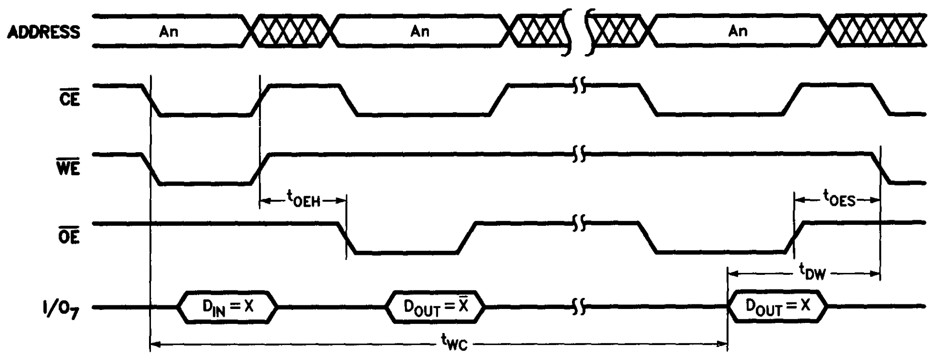
0067-7

*For each successive write within the page write operation, A_6–A_{14} should be the same or writes to an unknown address could occur.

Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

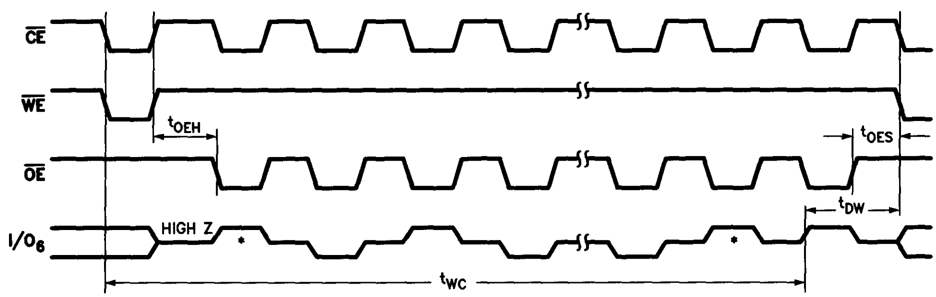
(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram[9]



0067-9

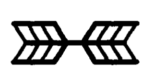
Toggle Bit Timing Diagram



0067-8

*I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C256 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C256.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

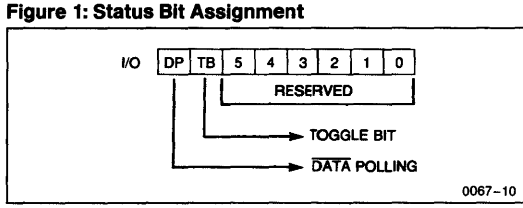
The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits

The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

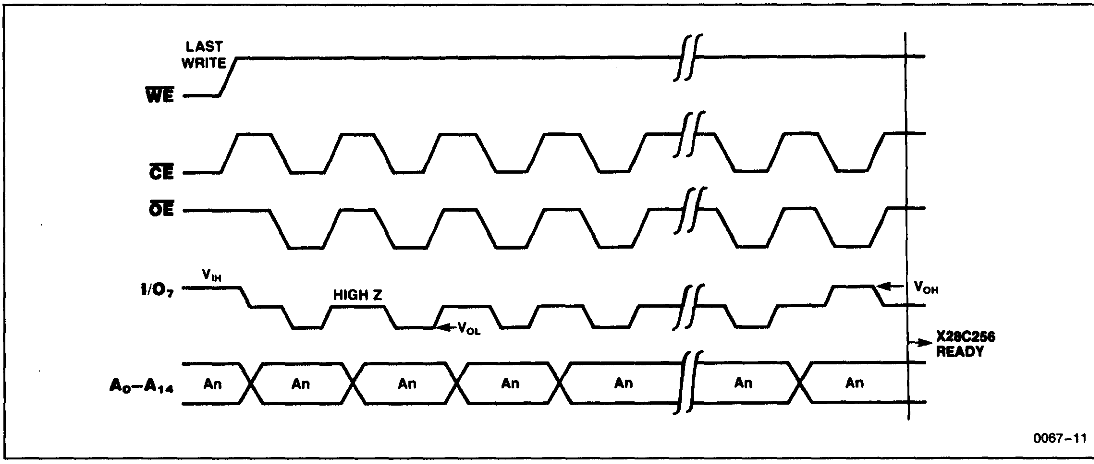
The X28C256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

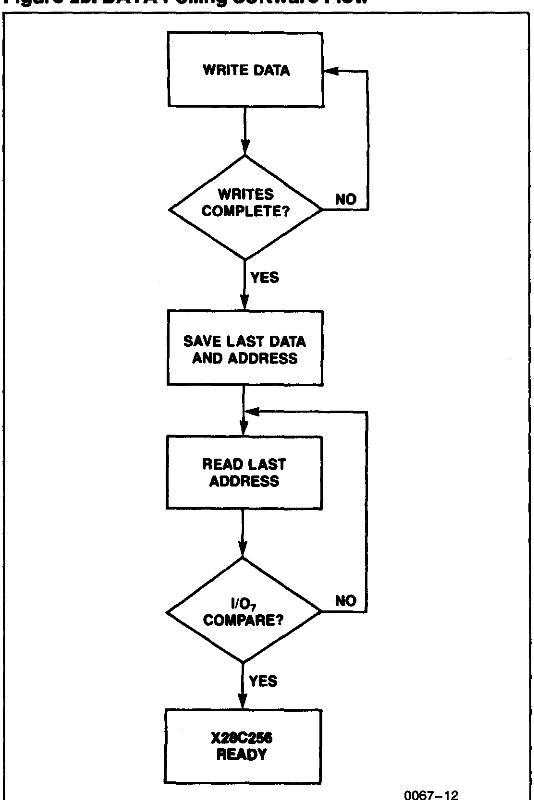
$\overline{\text{DATA}}$ POLLING I/O$_7$

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence



0067-11

Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow

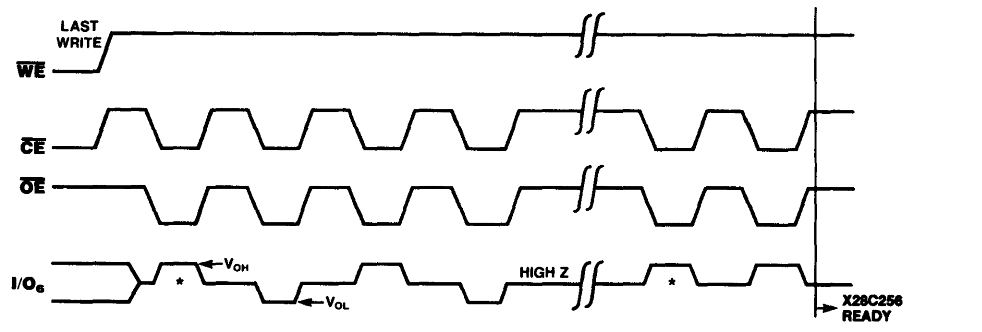


0067-12

$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

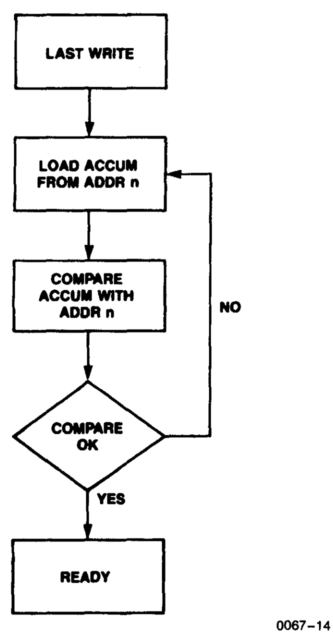
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq 3V$.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

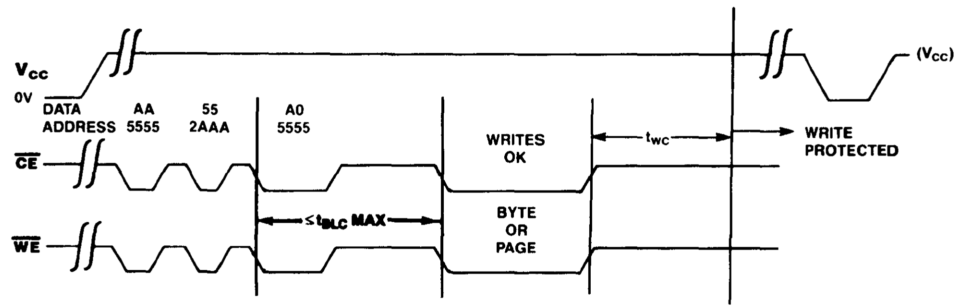
SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.(10) Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (10) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

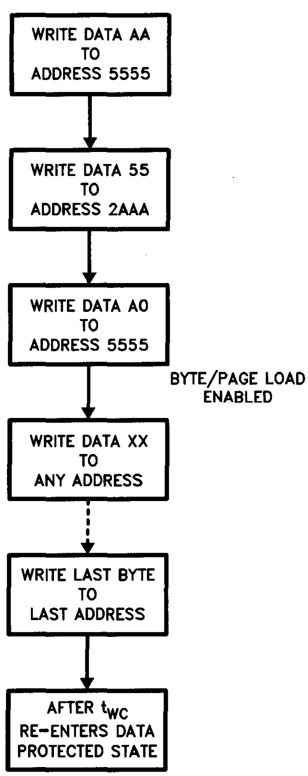
SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write



0067-15

Figure 4b: Write Sequence for Software Data Protection



0067-16

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

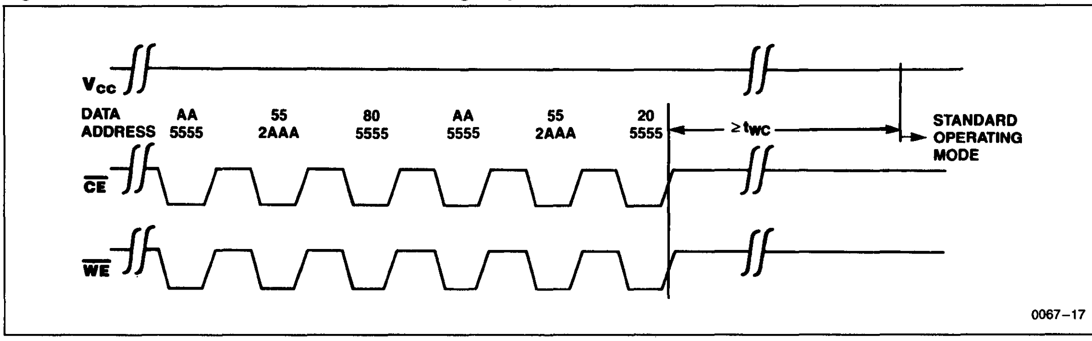
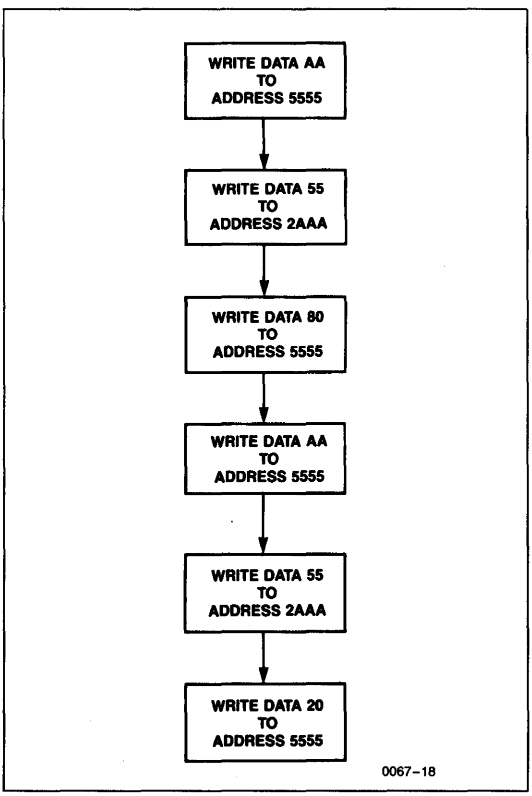


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

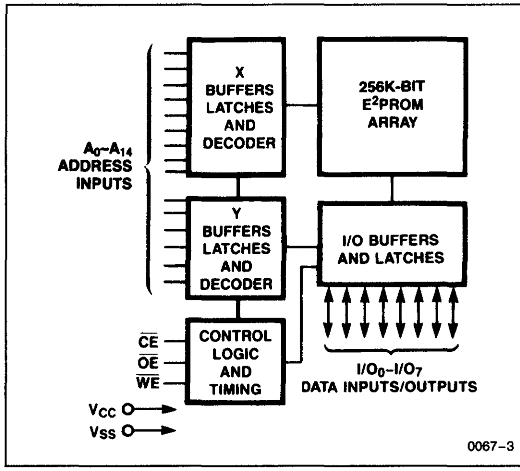
Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

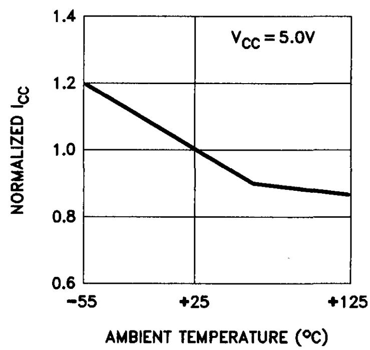
Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM

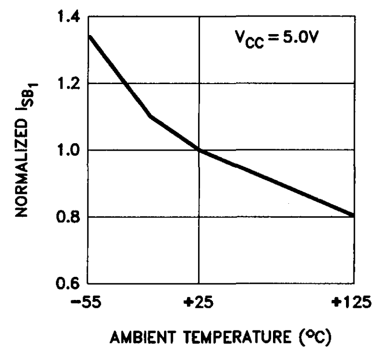


Normalized Active Supply Current vs. Ambient Temperature



0067-19

Normalized Standby Supply Current vs. Ambient Temperature



0067-20

ORDERING INFORMATION

256K E²PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C256P-20	32768 x 8		•									†	200 ns	CMOS	Standard
X28C256P-25	32768 x 8		•									†	250 ns	CMOS	Standard
X28C256P	32768 x 8		•									†	300 ns	CMOS	Standard
X28C256P-35	32768 x 8		•									†	350 ns	CMOS	Standard
X28C256PI-20	32768 x 8		•									I	200 ns	CMOS	Standard
X28C256PI-25	32768 x 8		•									I	250 ns	CMOS	Standard
X28C256PI	32768 x 8		•									I	300 ns	CMOS	Standard
X28C256PI-35	32768 x 8		•									I	350 ns	CMOS	Standard
X28C256D-20	32768 x 8			•								†	200 ns	CMOS	Standard
X28C256D-25	32768 x 8			•								†	250 ns	CMOS	Standard
X28C256D	32768 x 8			•								†	300 ns	CMOS	Standard
X28C256D-35	32768 x 8			•								†	350 ns	CMOS	Standard
X28C256DI-20	32768 x 8			•								I	200 ns	CMOS	Standard
X28C256DI-25	32768 x 8			•								I	250 ns	CMOS	Standard
X28C256DI	32768 x 8			•								I	300 ns	CMOS	Standard
X28C256DI-35	32768 x 8			•								I	350 ns	CMOS	Standard
X28C256F-20	32768 x 8						•					†	200 ns	CMOS	Standard
X28C256F-25	32768 x 8						•					†	250 ns	CMOS	Standard
X28C256F	32768 x 8						•					†	300 ns	CMOS	Standard
X28C256F-35	32768 x 8						•					†	350 ns	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = 28-Lead Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

256K E²PROMs (Continued)

Device Order Number	Organization	Package S	P	D	C	F1	F2	K	J	E	G	Temp. Range	Access Time	Process Technology	Processing Level
X28C256FI-20	32768 x 8						•					I	200 ns	CMOS	Standard
X28C256FI-25	32768 x 8						•					I	250 ns	CMOS	Standard
X28C256FI	32768 x 8						•					I	300 ns	CMOS	Standard
X28C256FI-35	32768 x 8						•					I	350 ns	CMOS	Standard
X28C256K-20	32768 x 8							•				†	200 ns	CMOS	Standard
X28C256K-25	32768 x 8							•				†	250 ns	CMOS	Standard
X28C256K	32768 x 8							•				†	300 ns	CMOS	Standard
X28C256K-35	32768 x 8							•				†	350 ns	CMOS	Standard
X28C256KI-20	32768 x 8							•				I	200 ns	CMOS	Standard
X28C256KI-25	32768 x 8							•				I	250 ns	CMOS	Standard
X28C256KI	32768 x 8							•				I	300 ns	CMOS	Standard
X28C256KI-35	32768 x 8							•				I	350 ns	CMOS	Standard
X28C256J-20	32768 x 8								•			†	200 ns	CMOS	Standard
X28C256J-25	32768 x 8								•			†	250 ns	CMOS	Standard
X28C256J	32768 x 8								•			†	300 ns	CMOS	Standard
X28C256J-35	32768 x 8								•			†	350 ns	CMOS	Standard
X28C256JI-20	32768 x 8								•			I	200 ns	CMOS	Standard
X28C256JI-25	32768 x 8								•			I	250 ns	CMOS	Standard
X28C256JI	32768 x 8								•			I	300 ns	CMOS	Standard
X28C256JI-35	32768 x 8								•			I	350 ns	CMOS	Standard

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

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D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = 28-Lead Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

256K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C256E-20	32768 x 8									•		†	200 ns	CMOS	Standard
X28C256E-25	32768 x 8									•		†	250 ns	CMOS	Standard
X28C256E	32768 x 8									•		†	300 ns	CMOS	Standard
X28C256E-35	32768 x 8									•		†	350 ns	CMOS	Standard
X28C256EI-20	32768 x 8									•		I	200 ns	CMOS	Standard
X28C256EI-25	32768 x 8									•		I	250 ns	CMOS	Standard
X28C256EI	32768 x 8									•		I	300 ns	CMOS	Standard
X28C256EI-35	32768 x 8									•		I	350 ns	CMOS	Standard

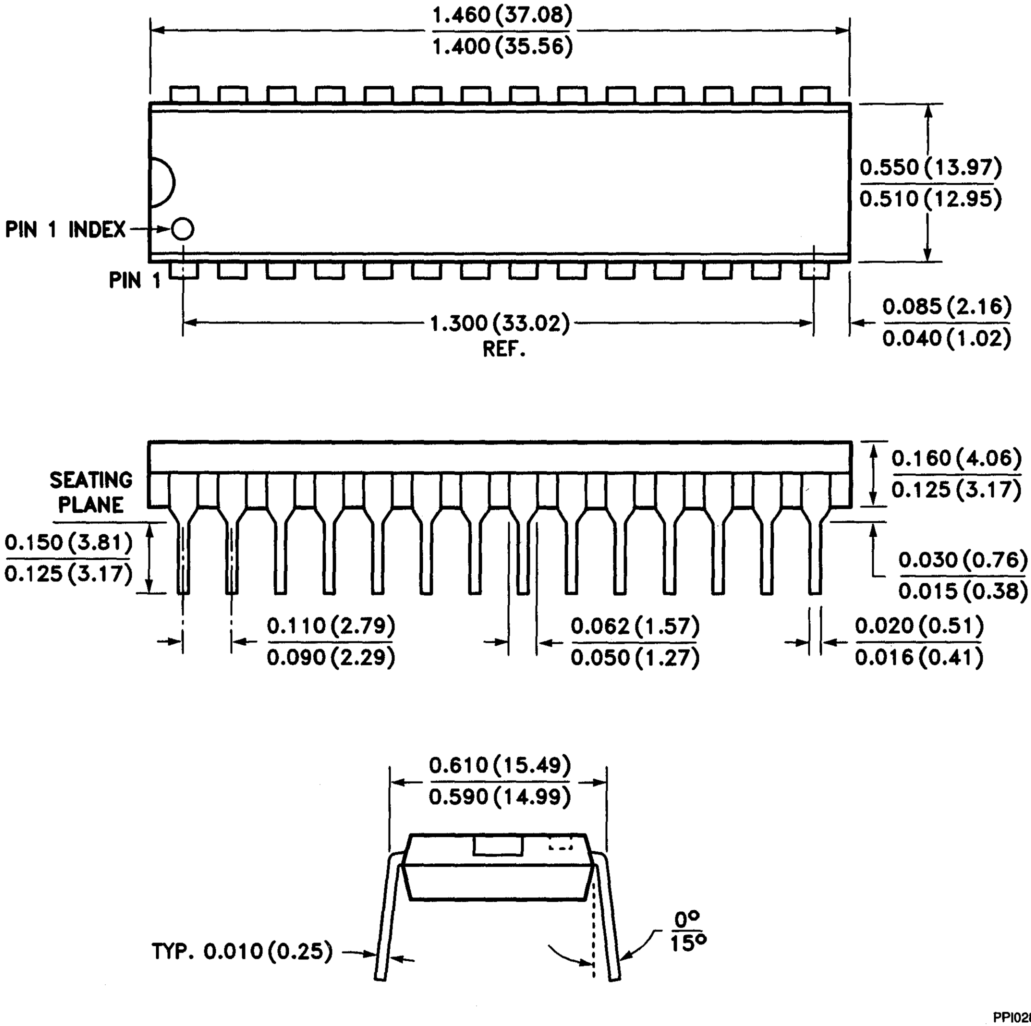
Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = 28-Lead Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

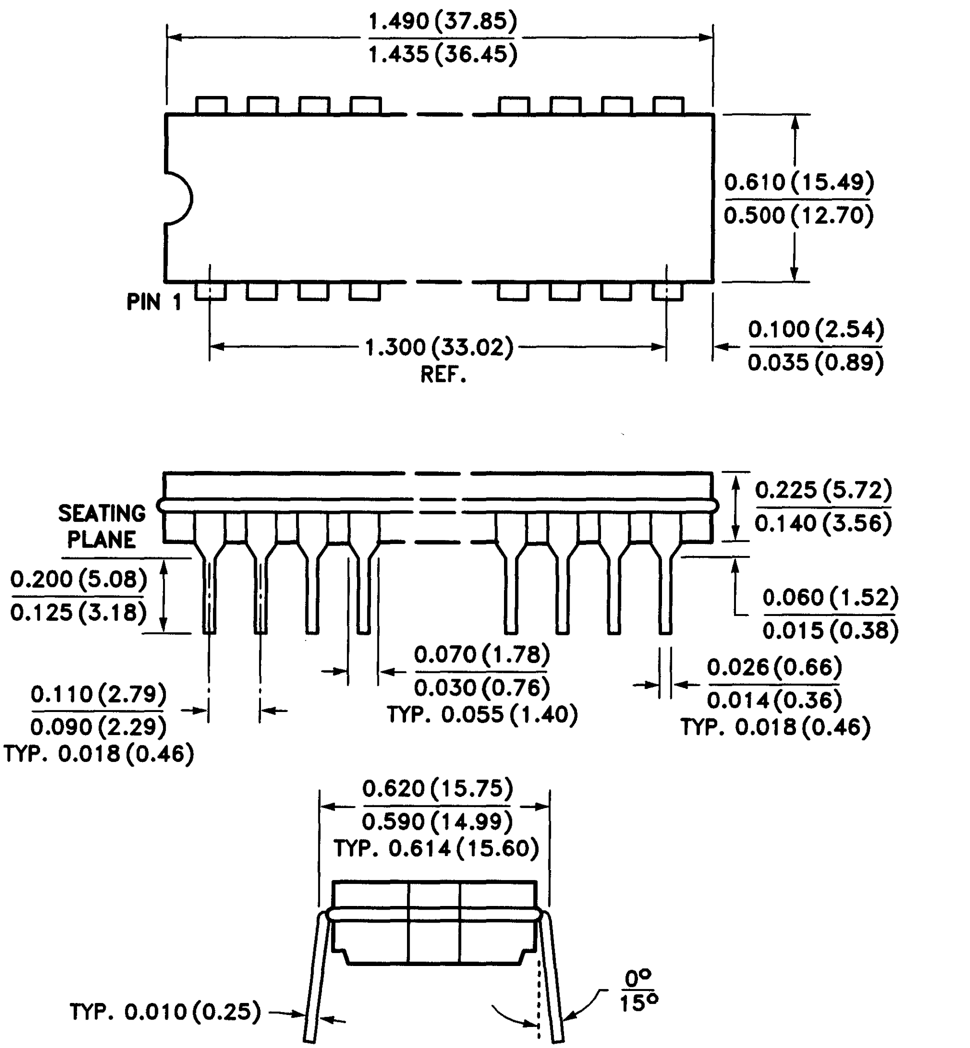
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

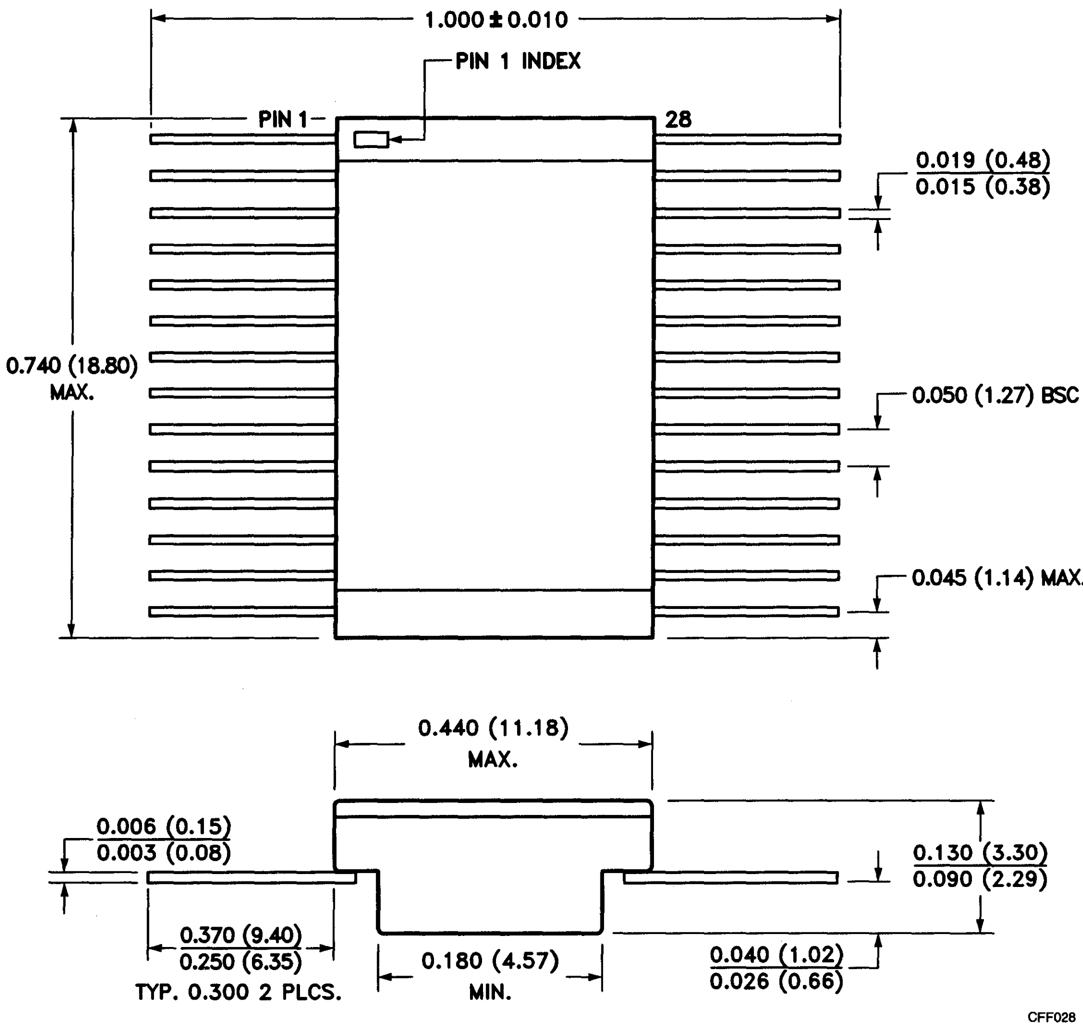
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

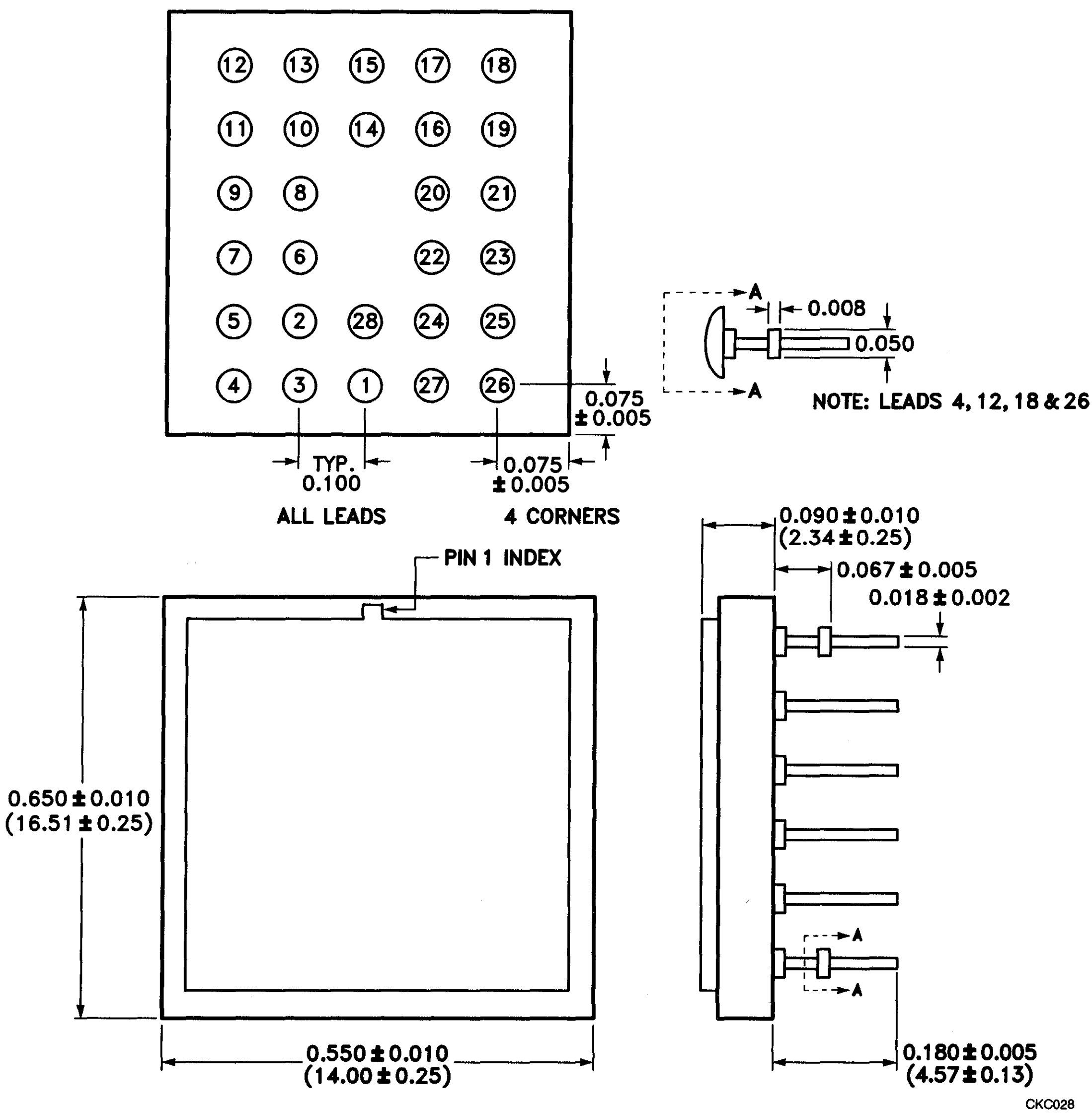
28-LEAD CERAMIC FLAT PACK TYPE F2



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. CASE OUTLINE FOR X28256 AND X28C256

PACKAGING INFORMATION

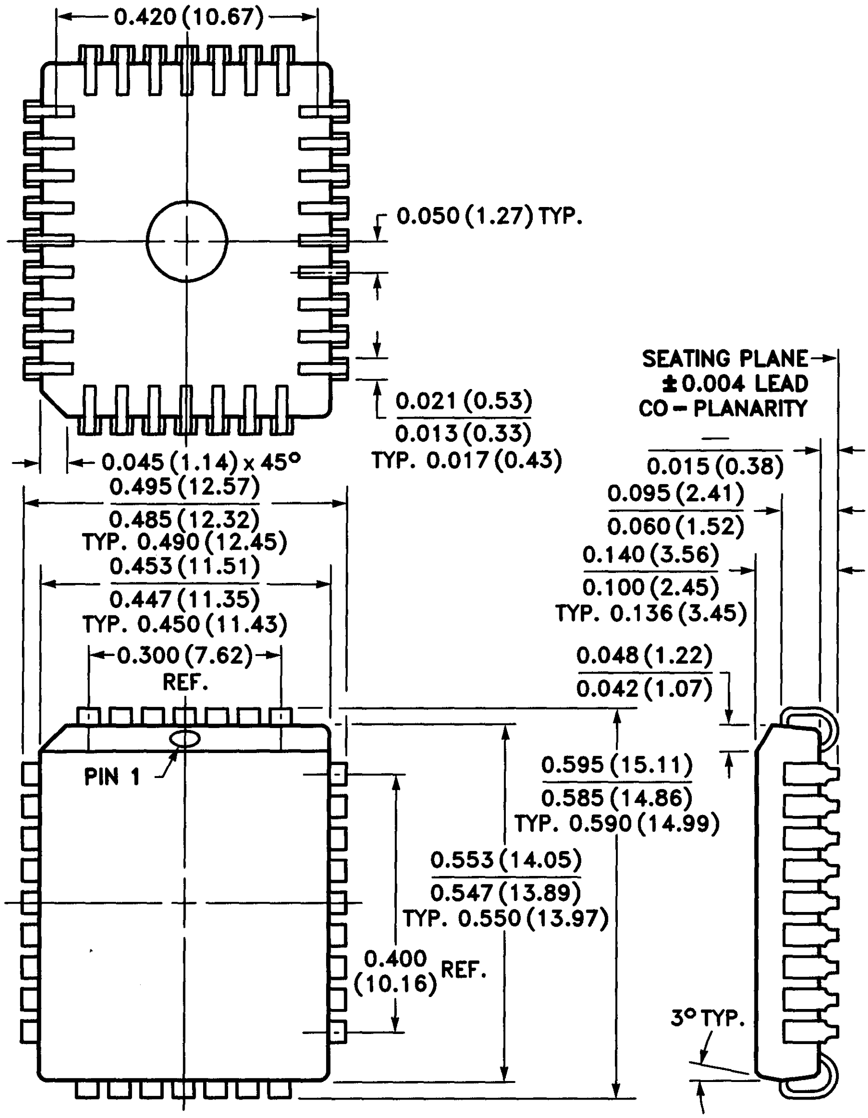
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

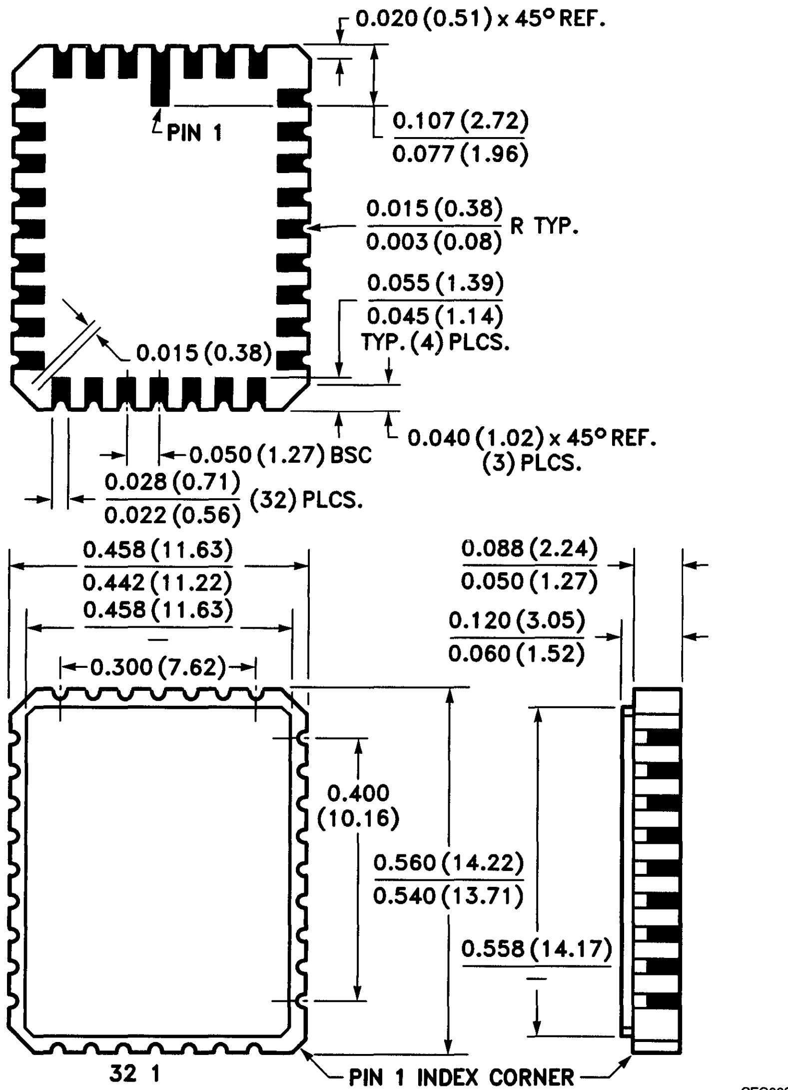
32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)

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TWX: 910-379-0033
Fax: 408/432-0640

256K Military **X28C256M** 32K x 8 Bit

Electrically Erasable PROM

FEATURES

- **LOW Power CMOS**
  - **—60 mA Active Current Max.**
  - **—200 μA Standby Current Max.**
- **Fast Write Cycle Times**
  - **—64-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 5 ms Typical**
  - **—Complete Memory Rewrite: 2.5 Sec. Typical**
  - **—Effective Byte Write Cycle Time: 78 μs Typical**
- **Software Data Protection**
- **End of Write Detection**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit**
- **Simple Byte and Page Write**
  - **—Single TTL Compatible $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **Upward Compatible with X2864A**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

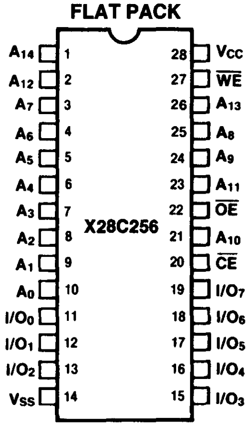
The Xicor X28C256 is a 32K x 8 E^{2}PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable nonvolatile memories the X28C256 is a 5V only device. The X28C256 features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256 supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256 also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256 includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

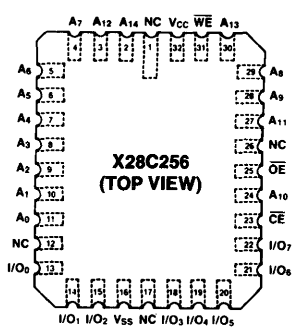
PIN CONFIGURATIONS

CERDIP
FLAT PACK



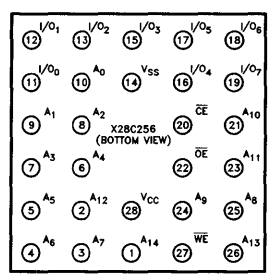
0065-1

LCC



0065-2

PGA



0065-21

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	μA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE} = V_{IL}$ All I/O's = Open Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		$V_{CC} + 1.0$	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 μA

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-Up to Read Operation	100	μs
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE $T_A = 25°C$, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

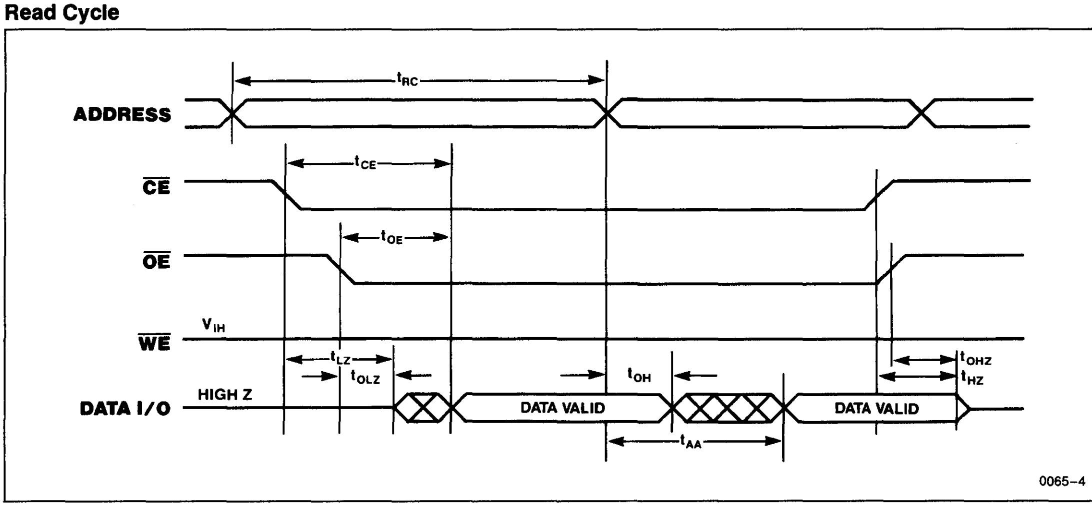
A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C256M-20		X28C256M-25		X28C256M		X28C256M-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		350		ns
t_{CE}	Chip Enable Access Time		200		250		300		350	ns
t_{AA}	Address Access Time		200		250		300		350	ns
t_{OE}	Output Enable Access Time		80		100		100		100	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



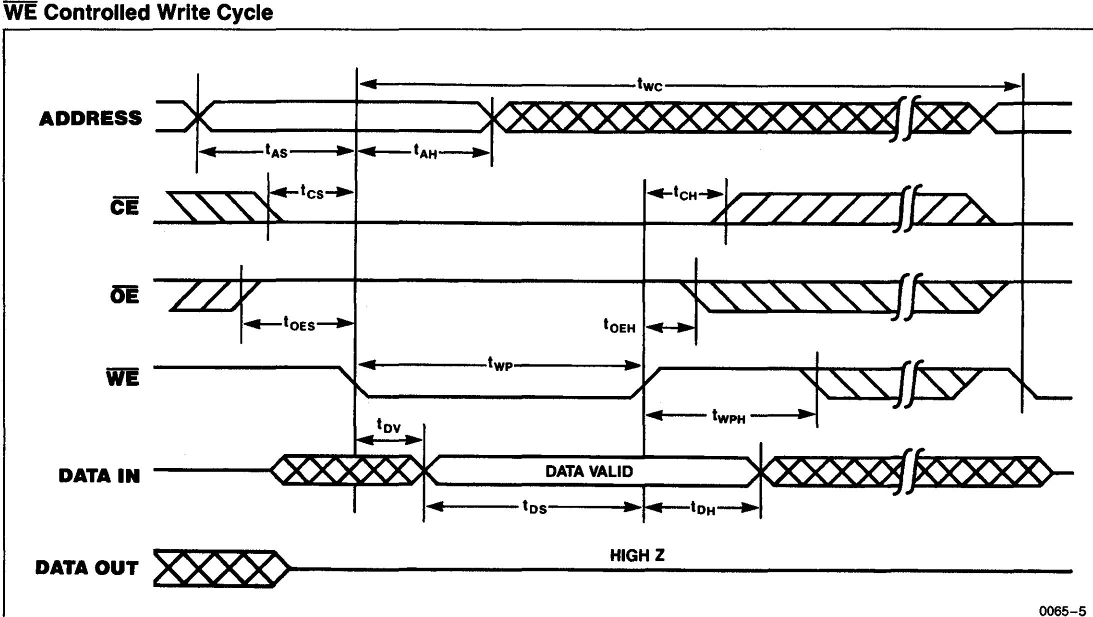
Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

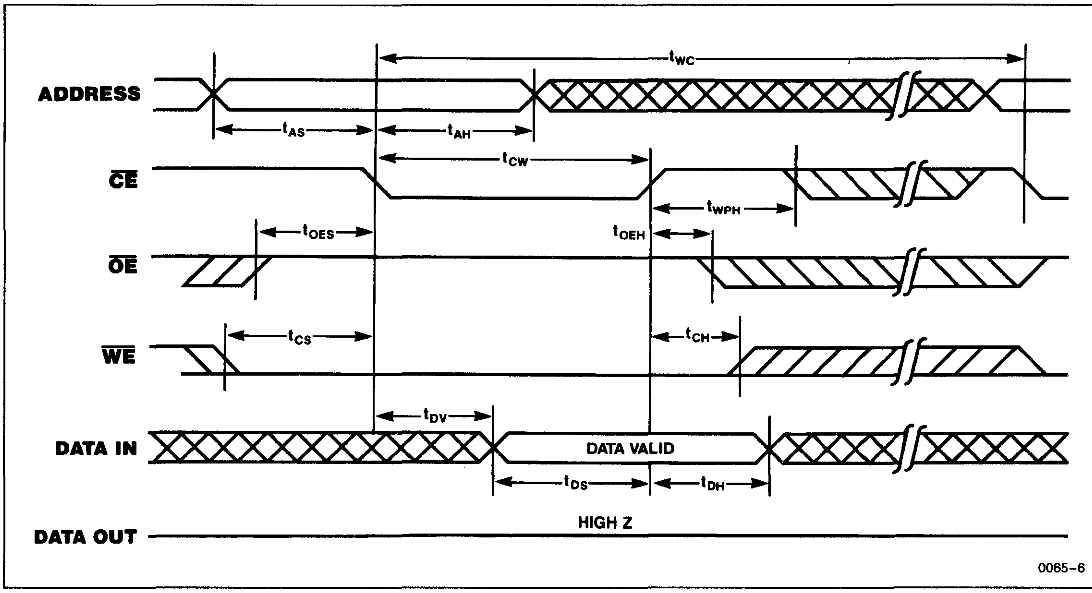
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	200			ns
t_{DV}	Data Valid			1	μs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			μs
t_{BLC}	Byte Load Cycle	1		100	μs

$\overline{WE}$ Controlled Write Cycle

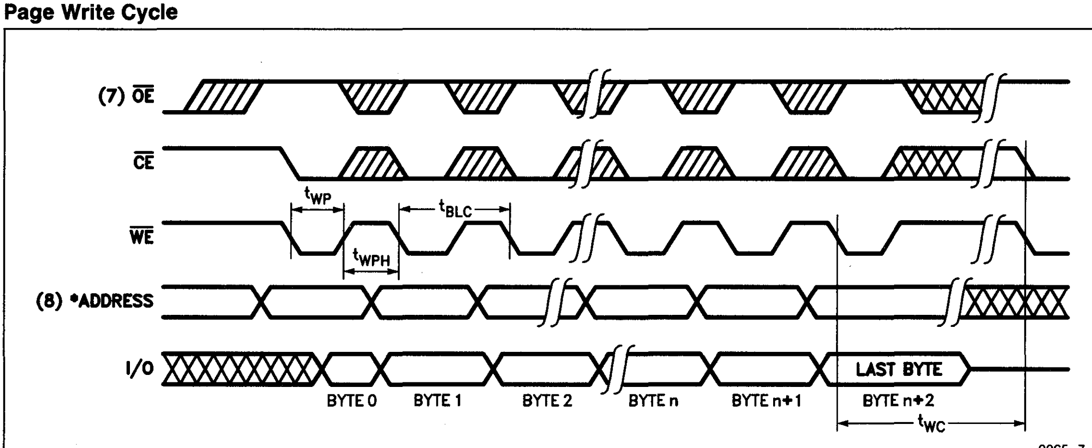


Note: (6) Typical values are for T_A = 25°C and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

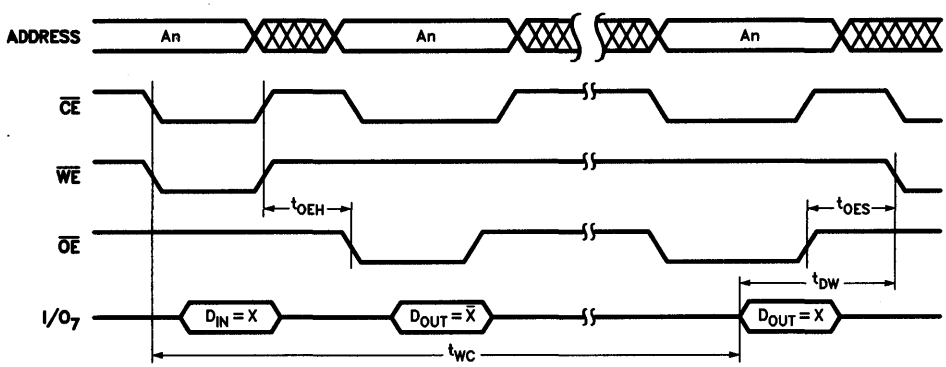


*For each successive write within the page write operation, A_6–A_{14} should be the same or writes to an unknown address could occur.

Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

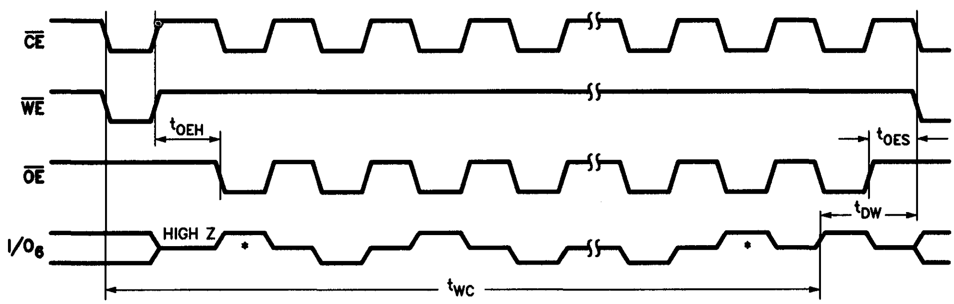
(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)



0065-9

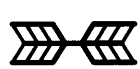
Toggle Bit Timing Diagram



0065-8

* I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C256 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C256.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C256 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

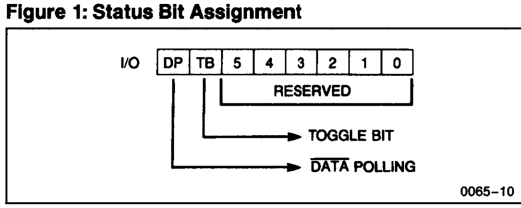
The page write feature of the X28C256 allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits

The X28C256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C256 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C256 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O$_7$

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

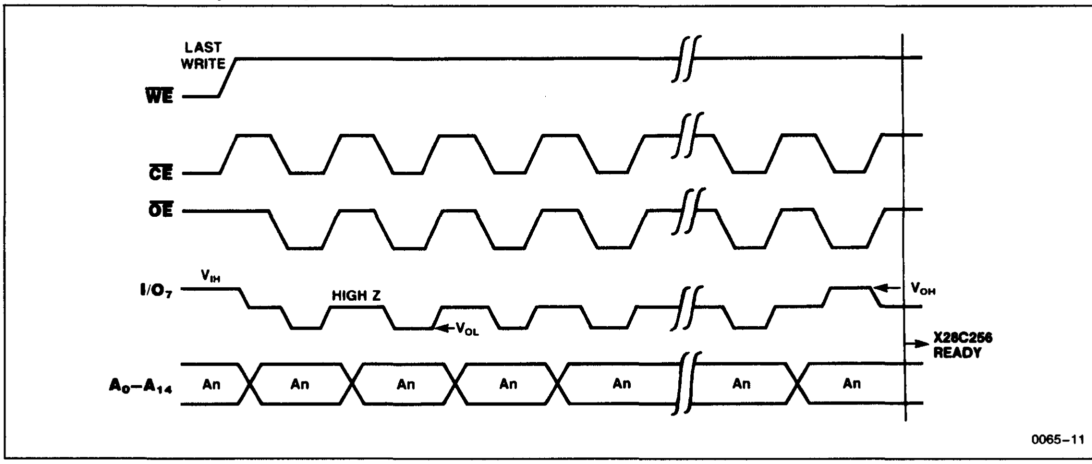
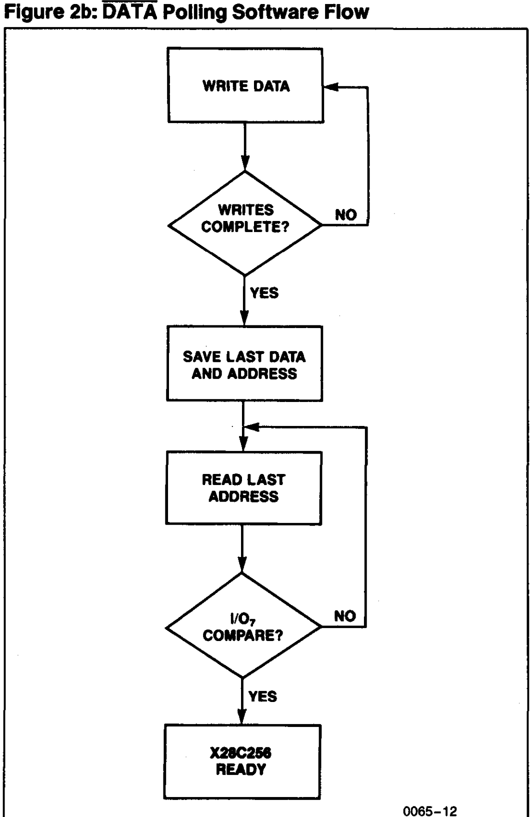


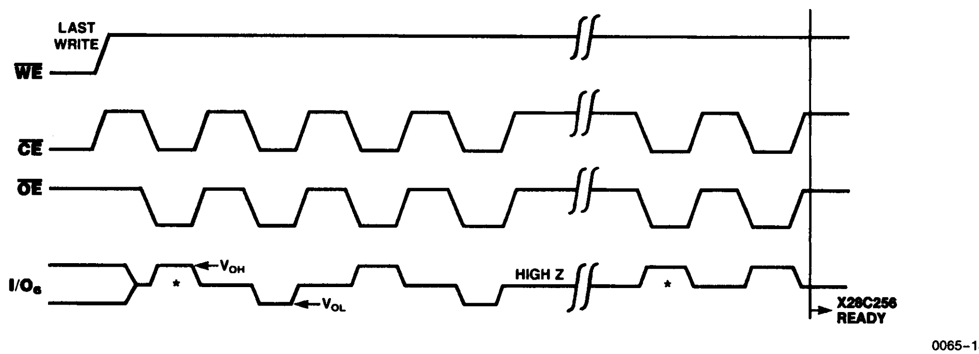
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C256. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

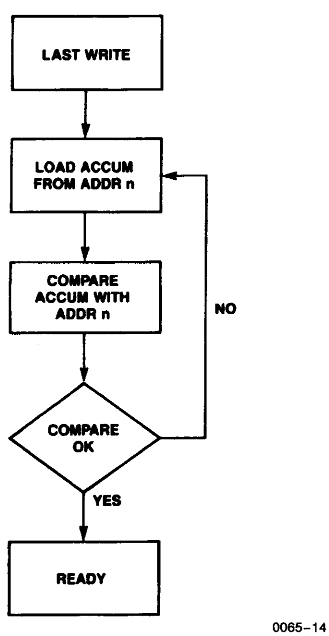
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C256 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C256 provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq 3V$.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C256 offers a software controlled data protection feature. The X28C256 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C256 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

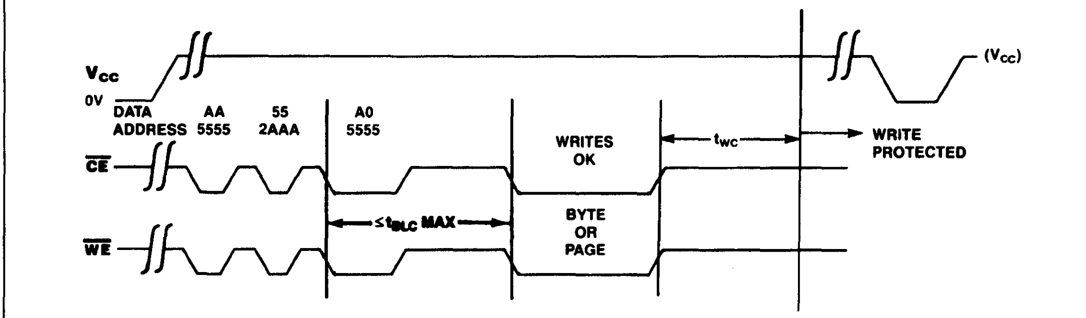
SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.[10] Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (10) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

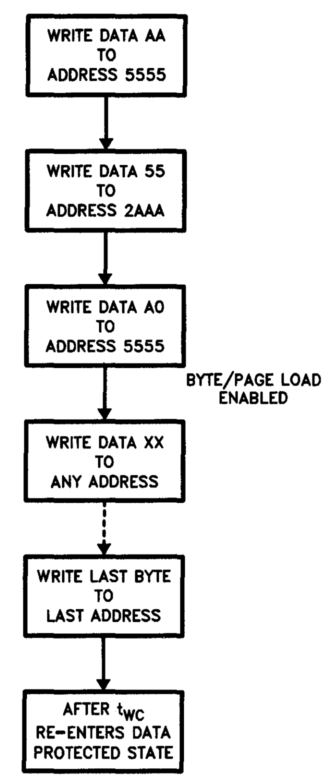
SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write



0065-15

Figure 4b: Write Sequence for Software Data Protection



0065-16

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C256 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

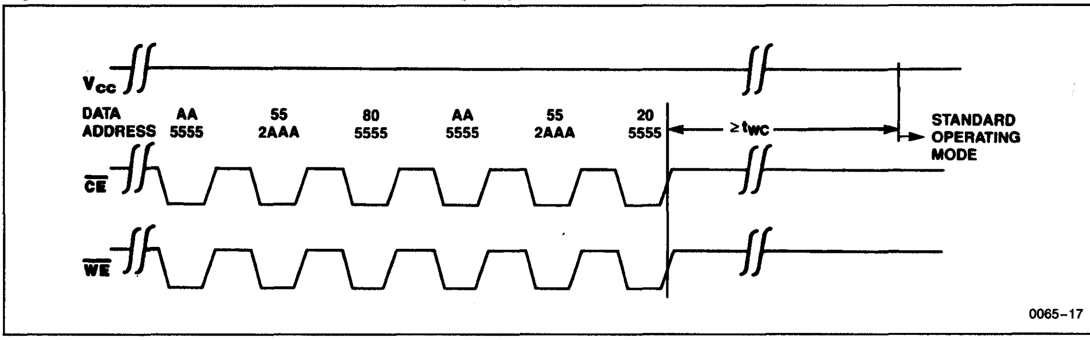
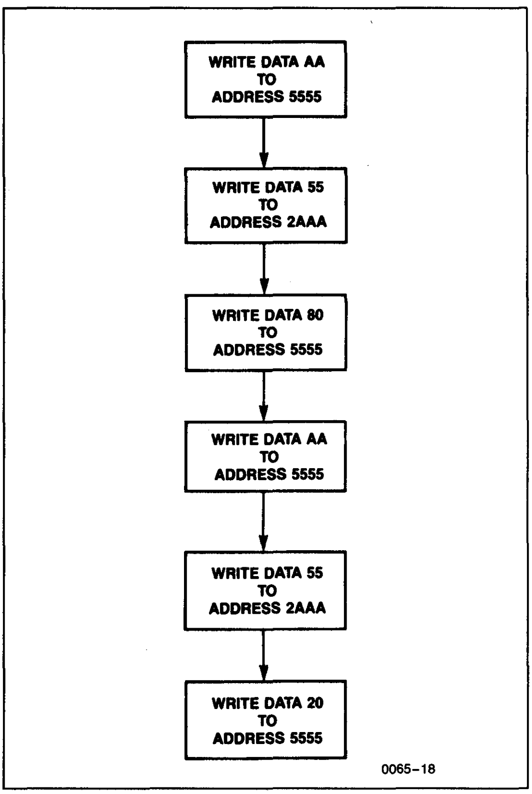


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C256 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

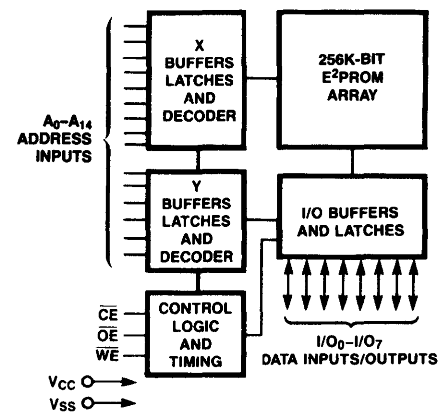
Because the X28C256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

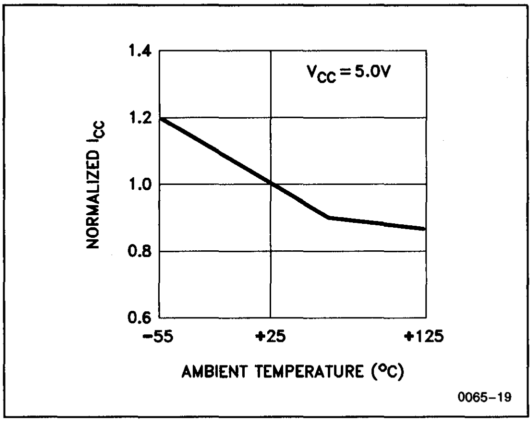
In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM

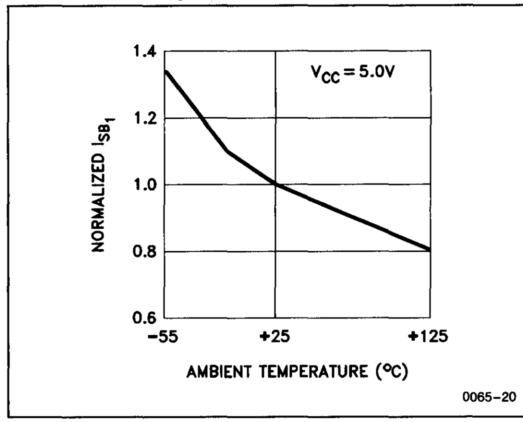


0065-3

Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



ORDERING INFORMATION

256K E^2PROMs

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C256DM-20	32768 x 8			•								M	200 ns	CMOS	Standard
X28C256DM-25	32768 x 8			•								M	250 ns	CMOS	Standard
X28C256DM	32768 x 8			•								M	300 ns	CMOS	Standard
X28C256DM-35	32768 x 8			•								M	350 ns	CMOS	Standard
X28C256DMB-20	32768 x 8			•								M	200 ns	CMOS	883 Rev. C, Class B
X28C256DMB-25	32768 x 8			•								M	250 ns	CMOS	883 Rev. C, Class B
X28C256DMB	32768 x 8			•								M	300 ns	CMOS	883 Rev. C, Class B
X28C256DMB-35	32768 x 8			•								M	350 ns	CMOS	883 Rev. C, Class B
X28C256FM-20	32768 x 8						•					M	200 ns	CMOS	Standard
X28C256FM-25	32768 x 8						•					M	250 ns	CMOS	Standard
X28C256FM	32768 x 8						•					M	300 ns	CMOS	Standard
X28C256FM-35	32768 x 8						•					M	350 ns	CMOS	Standard
X28C256FMB-20	32768 x 8						•					M	200 ns	CMOS	883 Rev. C, Class B
X28C256FMB-25	32768 x 8						•					M	250 ns	CMOS	883 Rev. C, Class B
X28C256FMB	32768 x 8						•					M	300 ns	CMOS	883 Rev. C, Class B
X28C256FMB-35	32768 x 8						•					M	350 ns	CMOS	883 Rev. C, Class B

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = 28-Lead Ceramic Flat Pack for X28256 and X28C256
K = 28-Pin Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

256K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C256KM-20	32768 x 8							•				M	200 ns	CMOS	Standard
X28C256KM-25	32768 x 8							•				M	250 ns	CMOS	Standard
X28C256KM	32768 x 8							•				M	300 ns	CMOS	Standard
X28C256KM-35	32768 x 8							•				M	350 ns	CMOS	Standard
X28C256KMB-20	32768 x 8							•				M	200 ns	CMOS	883 Rev. C, Class B
X28C256KMB-25	32768 x 8							•				M	250 ns	CMOS	883 Rev. C, Class B
X28C256KMB	32768 x 8							•				M	300 ns	CMOS	883 Rev. C, Class B
X28C256KMB-35	32768 x 8							•				M	350 ns	CMOS	883 Rev. C, Class B
X28C256EM-20	32768 x 8									•		M	200 ns	CMOS	Standard
X28C256EM-25	32768 x 8									•		M	250 ns	CMOS	Standard
X28C256EM	32768 x 8									•		M	300 ns	CMOS	Standard
X28C256EM-35	32768 x 8									•		M	350 ns	CMOS	Standard
X28C256EMB-20	32768 x 8									•		M	200 ns	CMOS	883 Rev. C, Class B
X28C256EMB-25	32768 x 8									•		M	250 ns	CMOS	883 Rev. C, Class B
X28C256EMB	32768 x 8									•		M	300 ns	CMOS	883 Rev. C, Class B
X28C256EMB-35	32768 x 8									•		M	350 ns	CMOS	883 Rev. C, Class B

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E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

256K E^2PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C256GM-20	32768 x 8										•	M	200 ns	CMOS	Standard
X28C256GM-25	32768 x 8										•	M	250 ns	CMOS	Standard
X28C256GM	32768 x 8										•	M	300 ns	CMOS	Standard
X28C256GM-35	32768 x 8										•	M	350 ns	CMOS	Standard
X28C256GMB-20	32768 x 8										•	M	200 ns	CMOS	883 Rev. C, Class B
X28C256GMB-25	32768 x 8										•	M	250 ns	CMOS	883 Rev. C, Class B
X28C256GMB	32768 x 8										•	M	300 ns	CMOS	883 Rev. C, Class B
X28C256GMB-35	32768 x 8										•	M	350 ns	CMOS	883 Rev. C, Class B

Key:
† = Blank = Commercial = 0°C to +70°C
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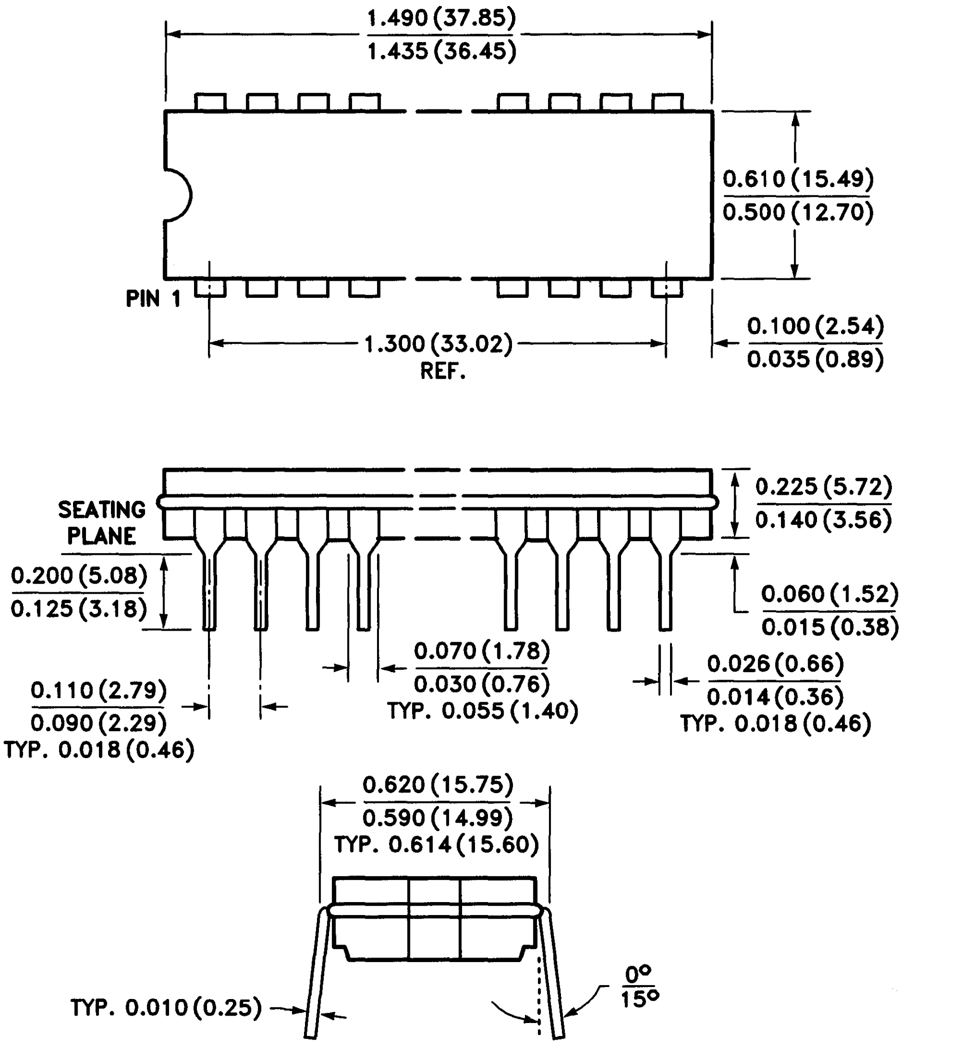
J = J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = 32-Pad Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

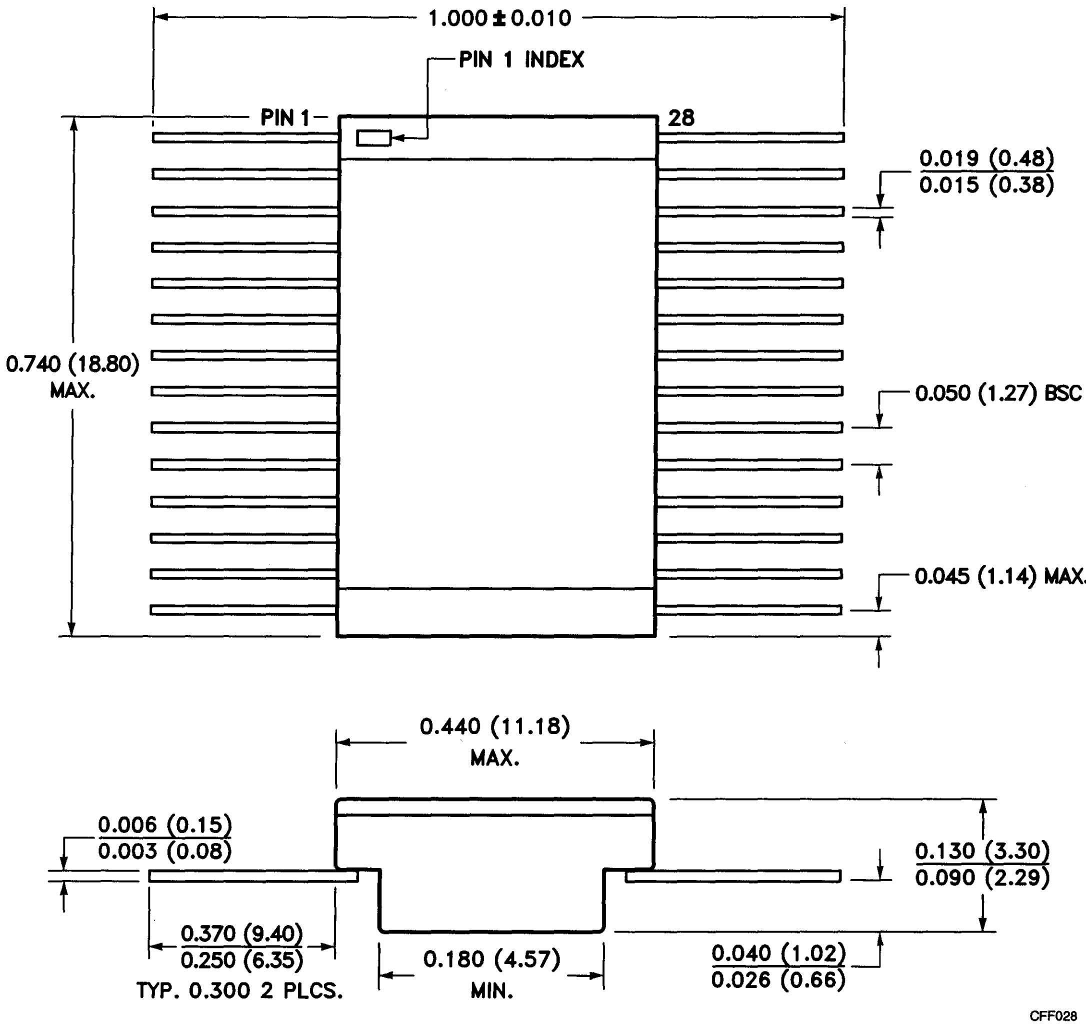
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

28-LEAD CERAMIC FLAT PACK TYPE F2



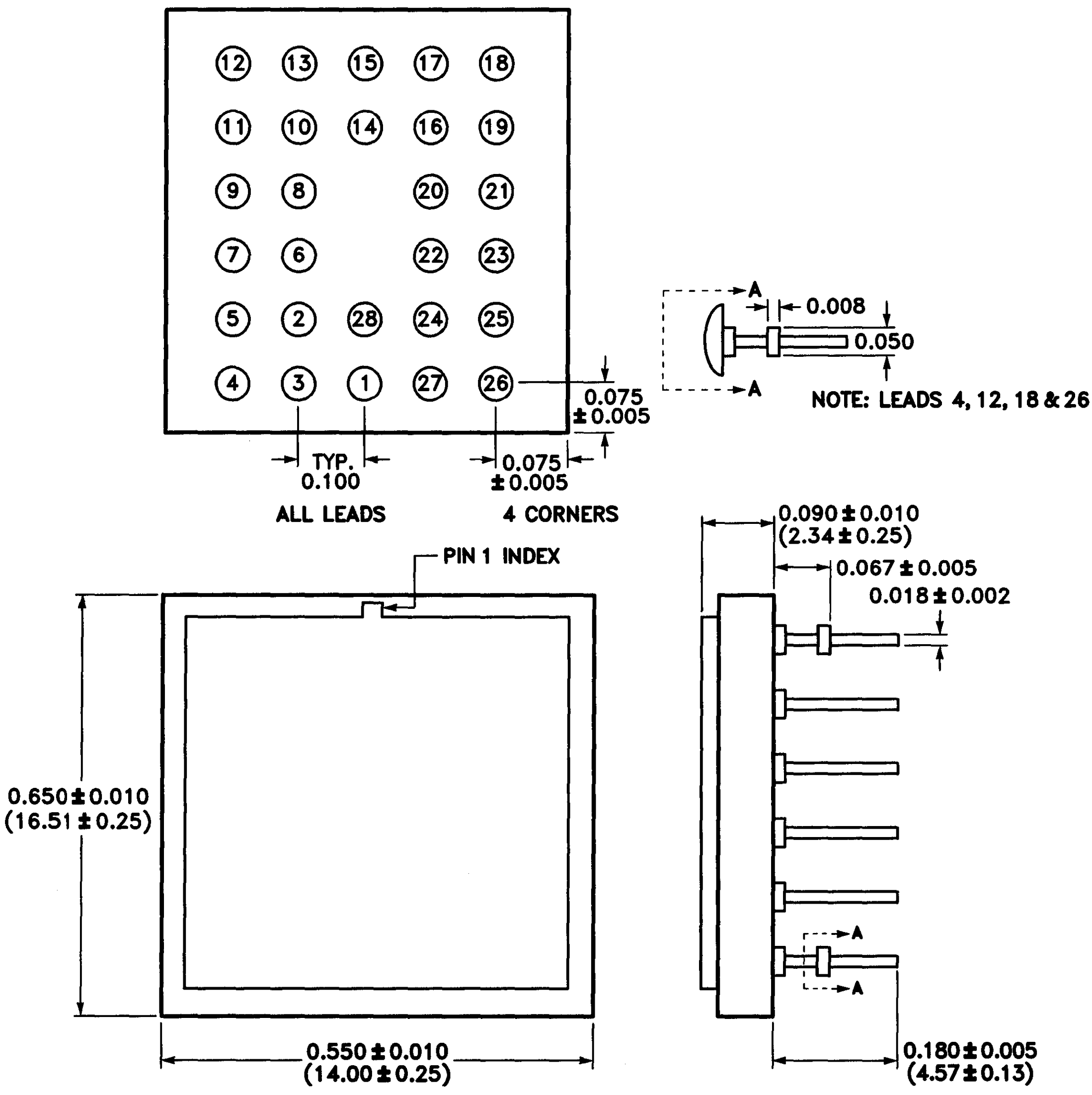
NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

2. CASE OUTLINE FOR X28256 AND X28C256

PACKAGING INFORMATION

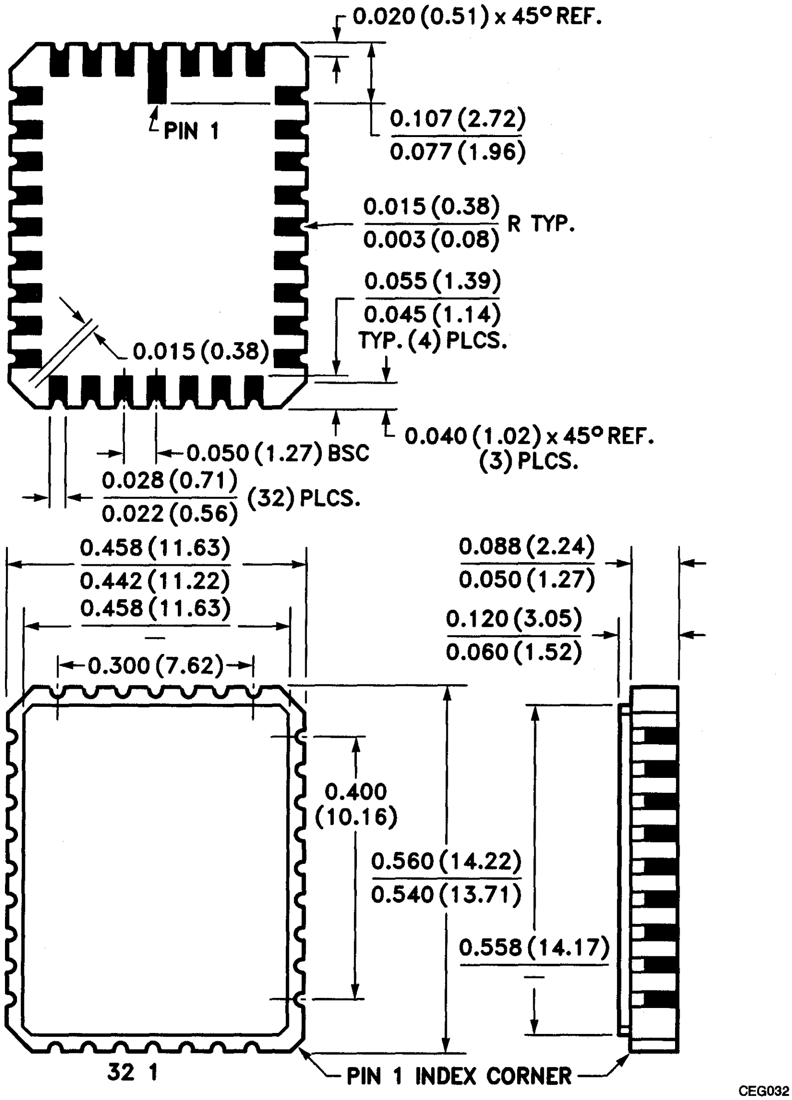
28-PIN CERAMIC PIN GRID ARRAY PACKAGE TYPE K



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E

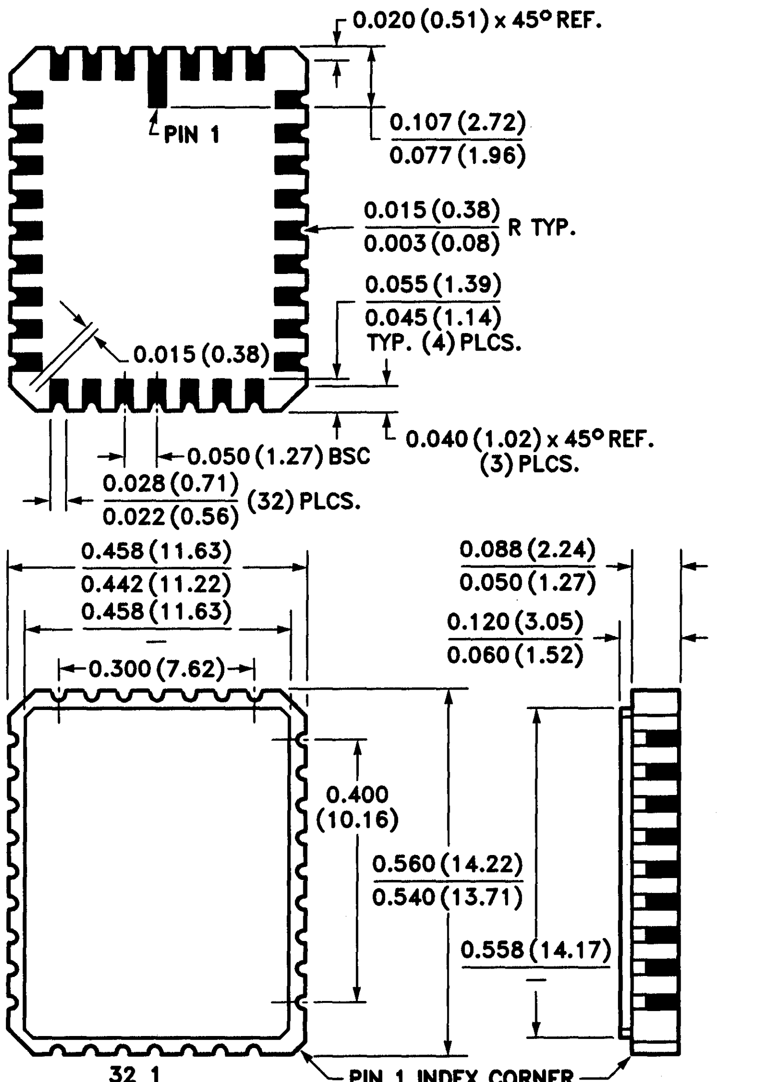


NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER (GLASS FRIT SEAL) PACKAGE TYPE G



NOTES:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ±1% NLT ±0.005 (0.127)
3. FOR EXTENDED STORAGE TEMPERATURE ENVIRONMENTS

NOTES

Sales Offices

U.S. Sales Offices

Northeast Area
Xicor, Inc.
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6/88 Stock No. 200-171

DATA SHEET SUPPLEMENT

256K Mil-Std-883C X28C256MB 32K x 8 Bit

Electrically Erasable PROM

REQUIREMENTS FOR CHIP ERASE

CHIP ERASE FUNCTIONALITY WILL BE GUARANTEED VIA C-SPEC ONLY. ADD C6767 TO XICOR PART NUMBER WHEN ORDERING.

DESCRIPTION

The X28C256MB may be erased (all bits cleared to logic "1") by two different methods. Both erasure methods clear the device within 10 ms. Because both methods employ Fowler-Nordheim Tunneling vs. Avalanche Programming, previously written data is not recoverable; thus, providing a method for maintaining security of proprietary information.

The first method is similar to that employed on earlier generations of E^2PROMs requiring the application of V_{OE} to the $\overline{OE}$ pin. Although a high voltage is applied to the pin, it is not coupled internally into the device. The voltage is sensed as being greater than V_{IH} and in conjunction with $\overline{CE}$ and $\overline{WE}$ LOW initiates an internal erase cycle. The voltages required to perform the actual erase operation are developed and controlled internally.

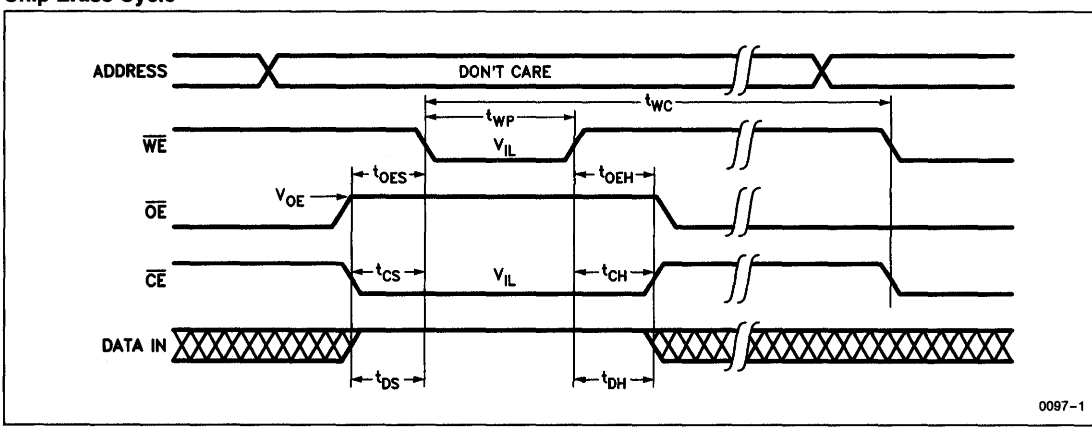
The second method of erasure is an extension of the Software Data Protection command sequence. It is a 5V only operation; thereby, eliminating the need for dual voltages within a system. Once the command sequence is issued by the host, the X28C256MB will automatically complete the erasure of the device within 10 ms.

A.C. CHIP ERASE CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$.

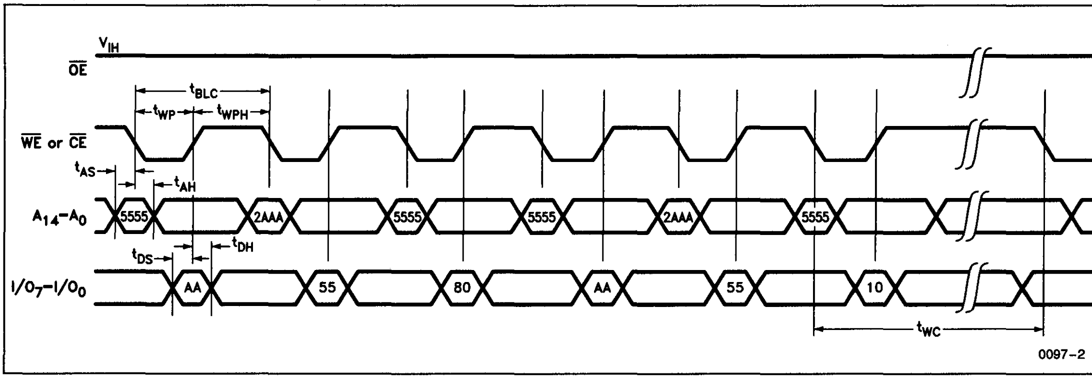
Symbol	Parameter	Limits		Units
		Min.	Max.	
V_{OE}	Output Enable Voltage	+14	+16	V
t_{CS}	$\overline{CE}$ to $\overline{WE}$ Setup Time	20		ns
t_{DS}	Data to $\overline{WE}$ Setup Time	20		ns
t_{DH}	Data Hold after $\overline{WE}$ High	20		ns
t_{WP}	Write Enable Pulse Width	150		ns
t_{CH}	$\overline{WE}$ High to $\overline{CE}$ Hold Time	20		ns
t_{OES}(1)	V_{OE} to $\overline{WE}$ Setup Time	20		ns
t_{OEH}(1)	V_{OE} Hold Time	20		ns
t_{WC}	Erase Cycle Time		10	ms

Chip Erase Cycle

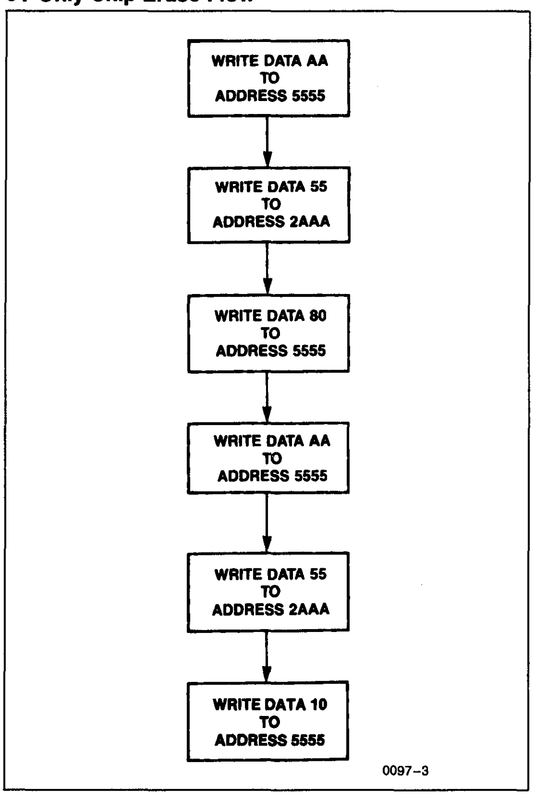


Note: (1) t_{OES} and t_{OEH} guaranteed by design, not 100% tested.

5V Only Chip Erase Timing Diagram



5V Only Chip Erase Flow



Note: 5V only erase function timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go LOW, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go HIGH.

The command sequence must conform to the page write timing.

Refer to the X28C256M data sheet for write timing parameters.

Write protection is set after 5V Only Chip Erase.

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6/88 Stock No. 200-172

PRELIMINARY INFORMATION

256K	Commercial Industrial	X28C256B X28C256BI	32K x 8 Bit

Electrically Erasable PROM

FEATURES

- **150 ns Access Time**
- **LOW Power CMOS**
  - **—60 mA Active Current Max.**
  - **—200 μA Standby Current Max.**
- **Fast Write Cycle Times**
  - **—64-Byte Page Write Operation**
  - **—Byte or Page Write Cycle: 5 ms Typical**
  - **—Complete Memory Rewrite: 2.5 Sec. Typical**
  - **—Effective Byte Write Cycle Time: 78 μs Typical**
- **Software Data Protection**
- **End of Write Detection**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit**
- **Simple Byte and Page Write**
  - **—Single TTL Compatible $\overline{\text{WE}}$ Signal**
  - **—Internally Latched Address and Data**
  - **—Automatic Write Timing**
- **Upward Compatible with X2864A**
- **JEDEC Approved Byte-Wide Pinout**

DESCRIPTION

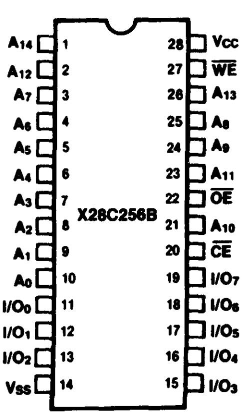
The Xicor X28C256B is a 32K x 8 E^2PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C256B is a 5V only device. The X28C256B features the JEDEC approved pinout for byte-wide memories, compatible with industry standard RAMs.

The X28C256B supports a 64-byte page write operation, effectively providing a 78 μs/byte write cycle and enabling the entire memory to be typically written in less than 2.5 seconds. The X28C256B also features $\overline{\text{DATA}}$ Polling, a system software support scheme used to indicate the early completion of a write cycle. In addition, the X28C256B includes a user-optional software data protection mode that further enhances Xicor's hardware write protect capability.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

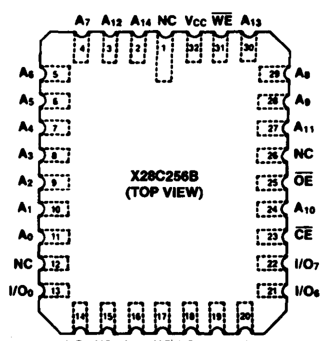
PIN CONFIGURATIONS

PLASTIC
CERDIP



0098-1

PLCC
LCC



0098-2

PIN NAMES

A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X28C256B .... −10°C to +85°C
X28C256BI .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28C256B T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C256BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits Min.	Typ.(1)	Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Active) (TTL Inputs)			60	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)			2	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		100	200	µA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	−1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −400 µA

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-Up to Read Operation	100	µs
t_{PUW}(3)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(3) This parameter is periodically sampled and not 100% tested.

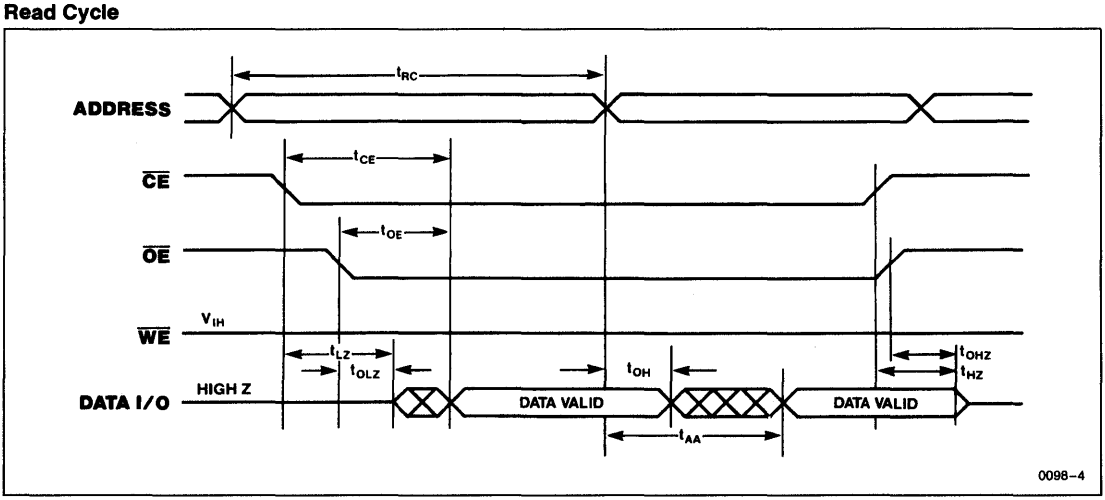
A.C. CHARACTERISTICS

X28C256B T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C256BI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C256B-15 X28C256BI-15		X28C256B-18 X28C256BI-18		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	150		180		ns
t_{CE}	Chip Enable Access Time		150		180	ns
t_{AA}	Address Access Time		150		180	ns
t_{OE}	Output Enable Access Time		50		50	ns
t_{LZ}(4)	$\overline{CE}$ Low to Active Output	0		0		ns
t_{OLZ}(4)	$\overline{OE}$ Low to Active Output	0		0		ns
t_{HZ}(5)	$\overline{CE}$ High to High Z Output	0	50	0	50	ns
t_{OHZ}(5)	$\overline{OE}$ High to High Z Output	0	50	0	50	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Read Cycle

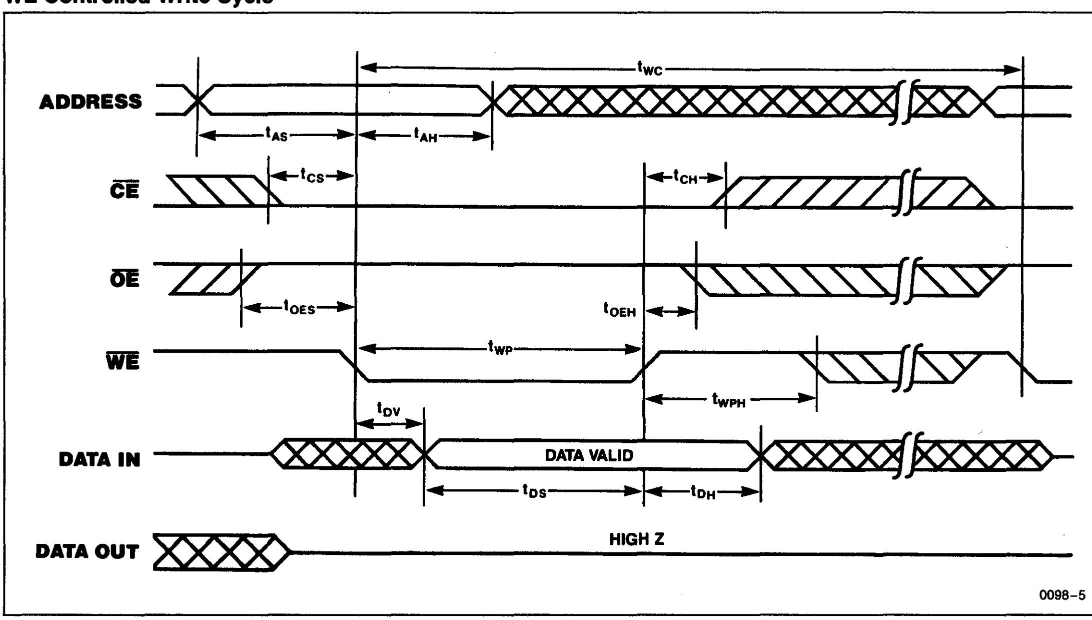


Notes: (4) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.
(5) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven. t_{HZ} min. and t_{OHZ} min. are shown for reference only, they are periodically characterized and are not tested.

Write Cycle Limits

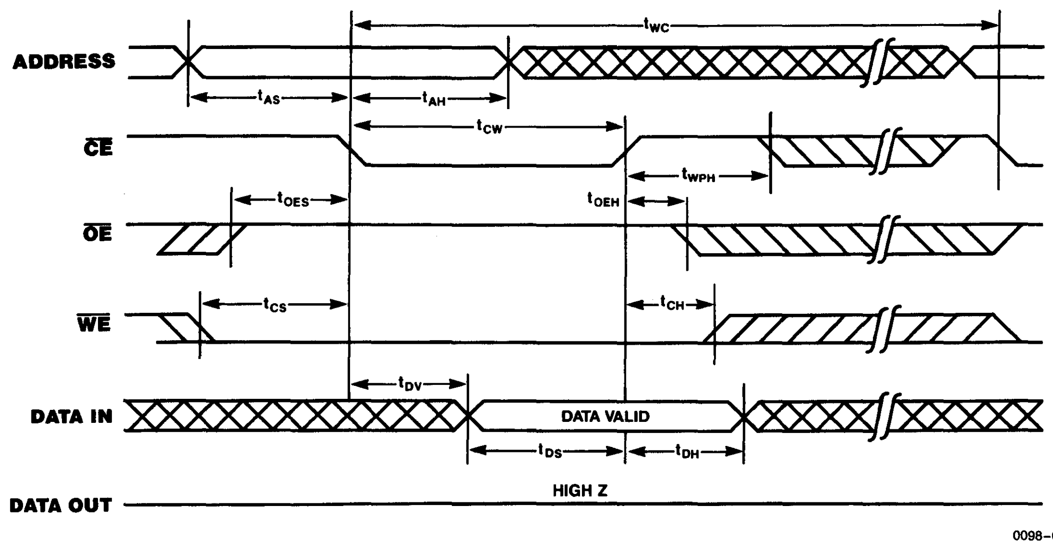
Symbol	Parameter	Min.	Typ.(6)	Max.	Units
t_{WC}	Write Cycle Time		5	10	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	150			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	100			ns
t_{OES}	$\overline{OE}$ High Setup Time	10			ns
t_{OEH}	$\overline{OE}$ High Hold Time	10			ns
t_{WP}	$\overline{WE}$ Pulse Width	100			ns
t_{WPH}	$\overline{WE}$ High Recovery	200			ns
t_{DV}	Data Valid			1	µs
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	10			ns
t_{DW}	Delay to Next Write	10			µs
t_{BLC}	Byte Load Cycle	1		100	µs

$\overline{WE}$ Controlled Write Cycle

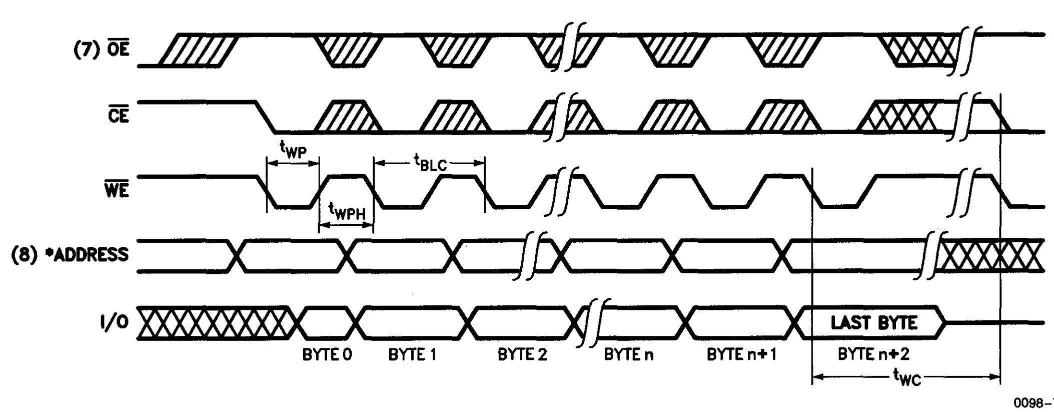


Note: (6) Typical values are for $T_A = 25°C$ and nominal supply voltage.

$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

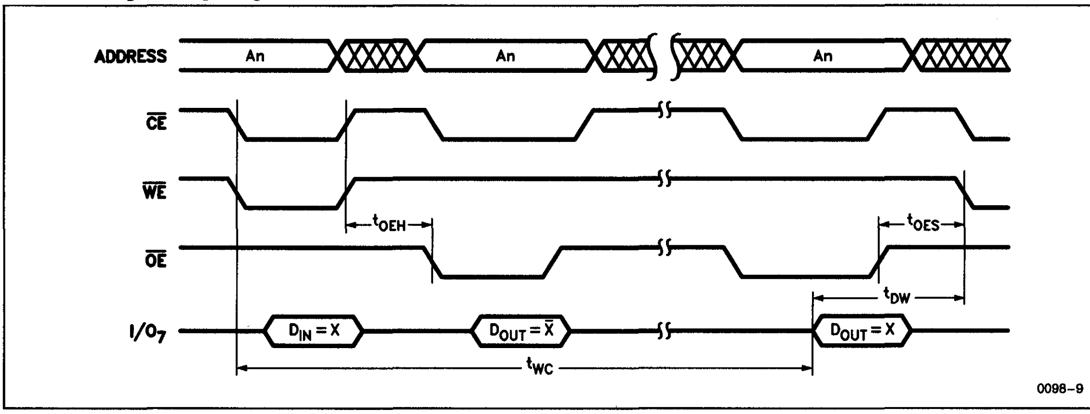


*For each successive write within the page write operation, A_6–A_{14} should be the same or writes to an unknown address could occur.

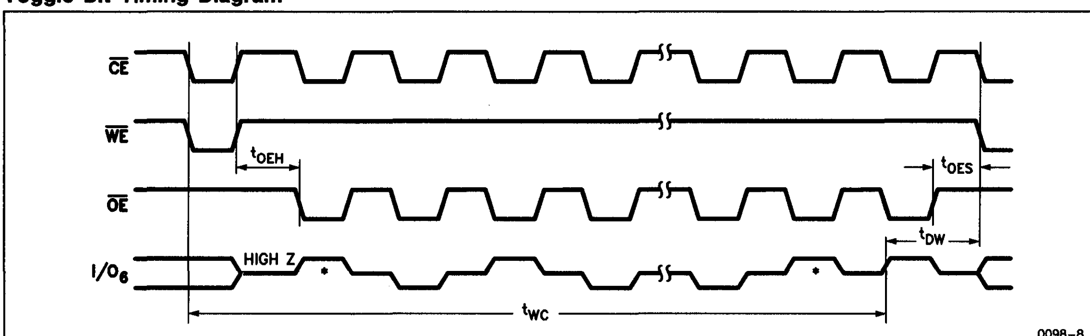
Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)



Toggle Bit Timing Diagram



*I/O6 beginning and ending state will vary, depending upon actual t_{WC}.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C256B through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C256B.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C256B supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

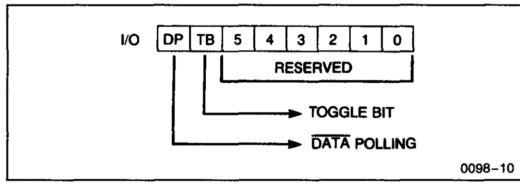
The page write feature of the X28C256B allows the entire memory to be written in 2.5 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28C256B prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits

The X28C256B provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C256B features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C256B, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C256B is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C256B also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O$_7$

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

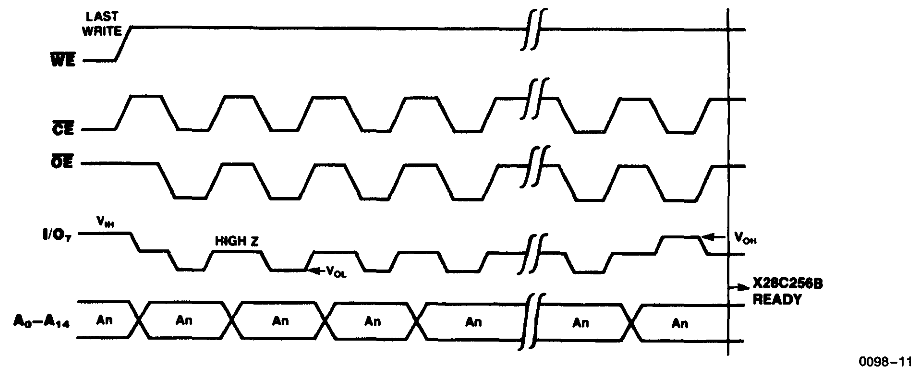
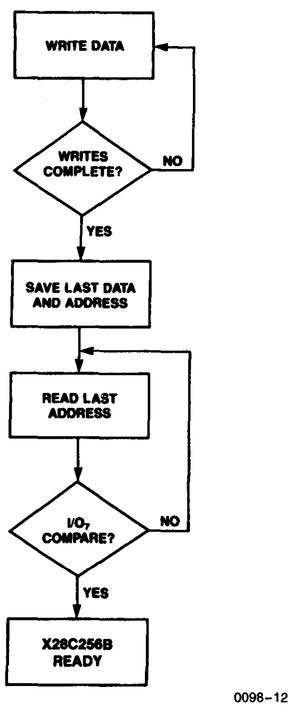


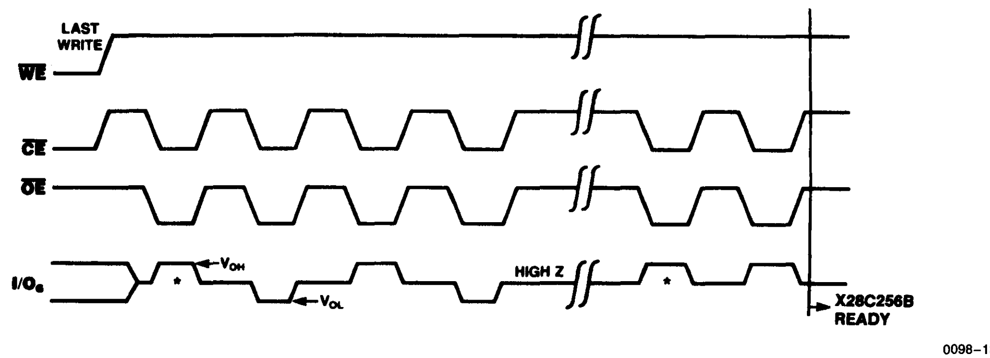
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C256B. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

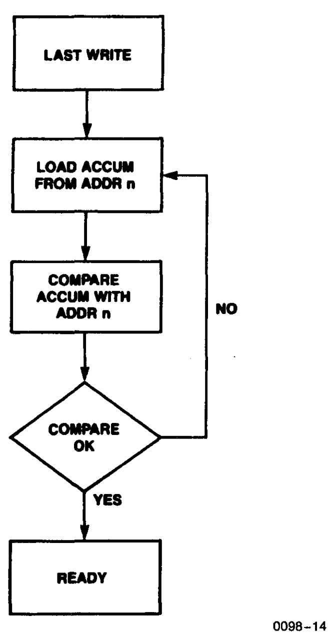
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C256B memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C256B provides three hardware features (compatible with X2864A) that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C256B offers a software controlled data protection feature. The X28C256B is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C256B can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C256B is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data.(10) Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

Note: (10) Once the three byte sequence is issued it must be followed by a valid byte or page write operation.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

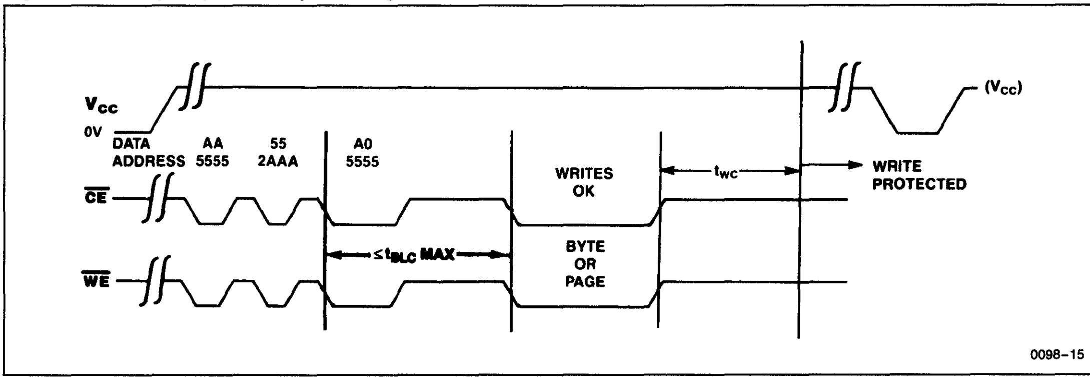
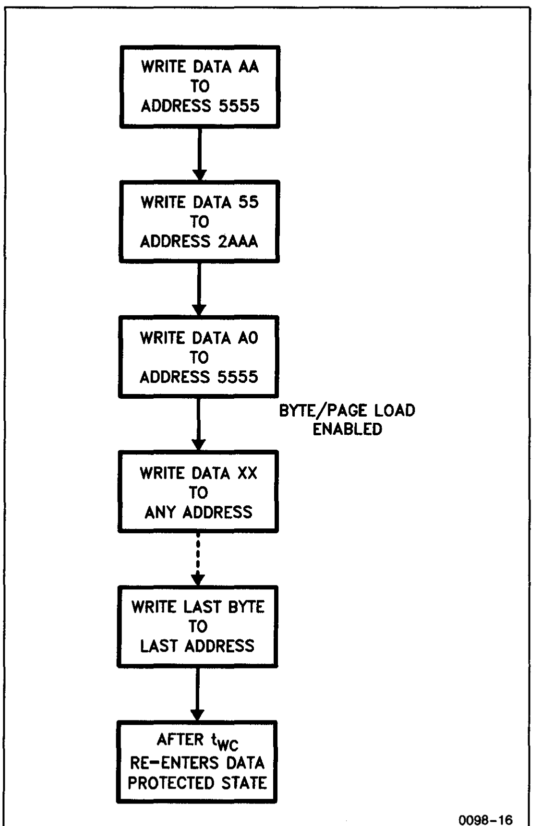


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the X28C256B will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C256B will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

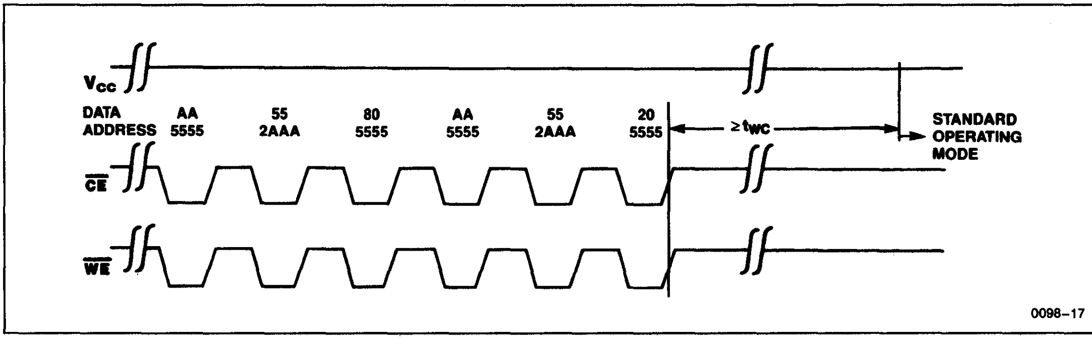
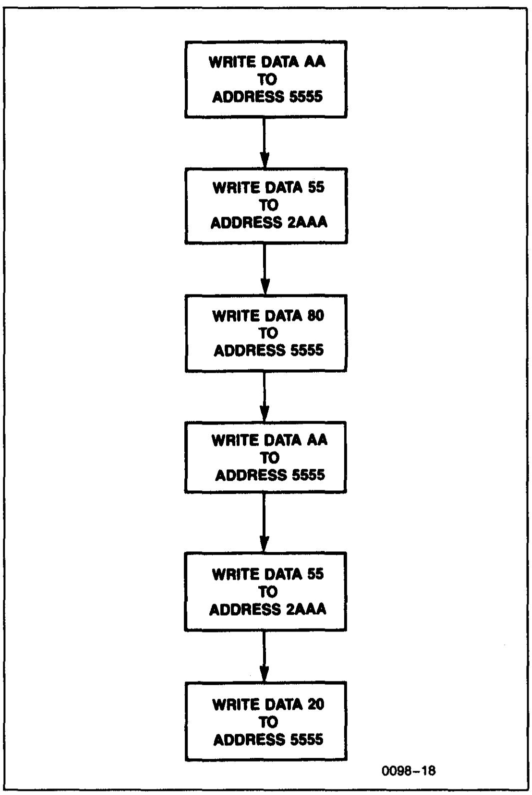


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C256B will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

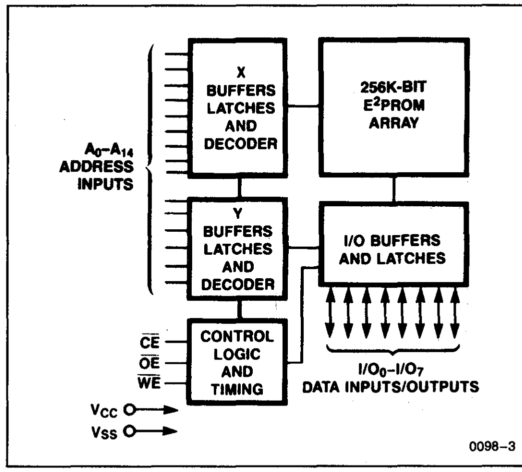
Because the X28C256B is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

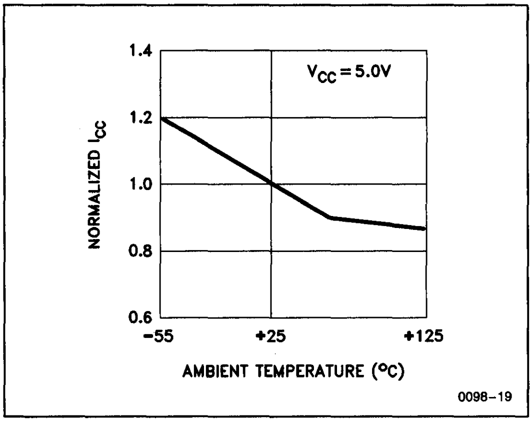
Because the X28C256B has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

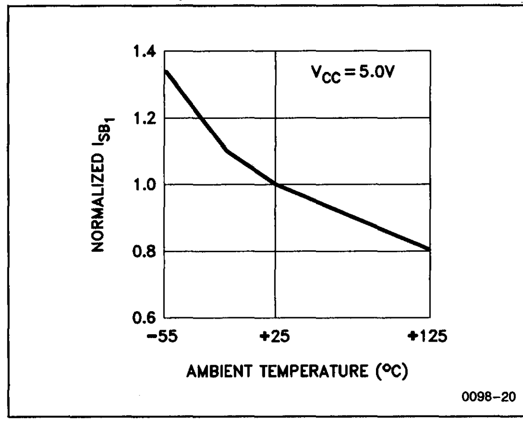
FUNCTIONAL DIAGRAM



Normalized Active Supply Current vs. Ambient Temperature



Normalized Standby Supply Current vs. Ambient Temperature



ORDERING INFORMATION

256K E2PROMs

Device Order Number	Organization	Package S	P	D	C	F1	F2	K	J	E	G	Temp. Range	Access Time	Process Technology	Processing Level
X28C256BP-15	32768 x 8		•									†	150 ns	CMOS	Standard
X28C256BP-18	32768 x 8		•									†	180 ns	CMOS	Standard
X28C256BPI-15	32768 x 8		•									I	150 ns	CMOS	Standard
X28C256BPI-18	32768 x 8		•									I	180 ns	CMOS	Standard
X28C256BD-15	32768 x 8			•								†	150 ns	CMOS	Standard
X28C256BD-18	32768 x 8			•								†	180 ns	CMOS	Standard
X28C256BDI-15	32768 x 8			•								I	150 ns	CMOS	Standard
X28C256BDI-18	32768 x 8			•								I	180 ns	CMOS	Standard
X28C256BJ-15	32768 x 8								•			†	150 ns	CMOS	Standard
X28C256BJ-18	32768 x 8								•			†	180 ns	CMOS	Standard
X28C256BJI-15	32768 x 8								•			I	150 ns	CMOS	Standard
X28C256BJI-18	32768 x 8								•			I	180 ns	CMOS	Standard

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
P = 28-Lead Plastic DIP
D = 28-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B and X2864H
F2 = Ceramic Flat Pack for X28256 and X28C256
K = Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

256K E²PROMs (Continued)

Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C256BE-15	32768 x 8									•		†	150 ns	CMOS	Standard
X28C256BE-18	32768 x 8									•		†	180 ns	CMOS	Standard
X28C256BEI-15	32768 x 8									•		I	150 ns	CMOS	Standard
X28C256BEI-18	32768 x 8									•		I	180 ns	CMOS	Standard

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C
T = Ultra High Temp. = 0°C to +150°C

S = Plastic Small Outline Gull Wing
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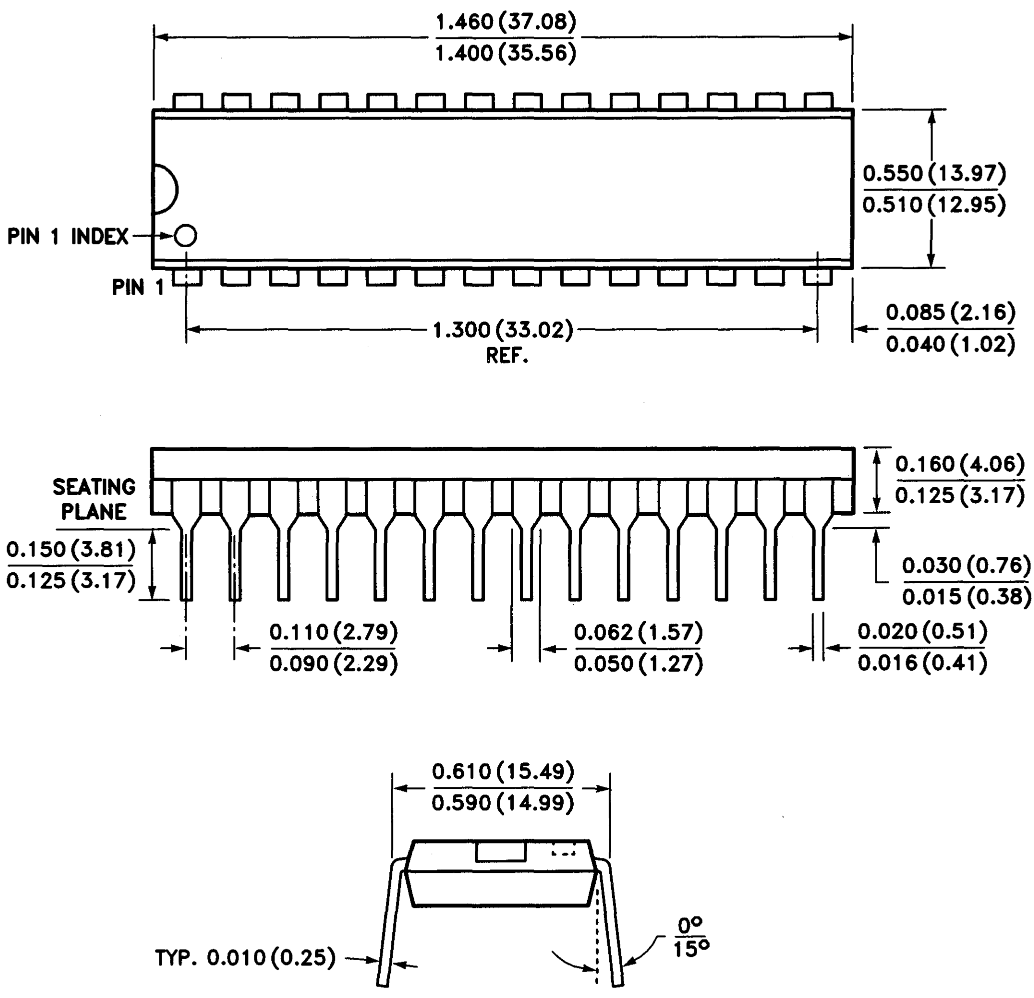
K = Ceramic Pin Grid Array
J = 32-Lead J-Hook Plastic Leaded Chip Carrier
E = 32-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

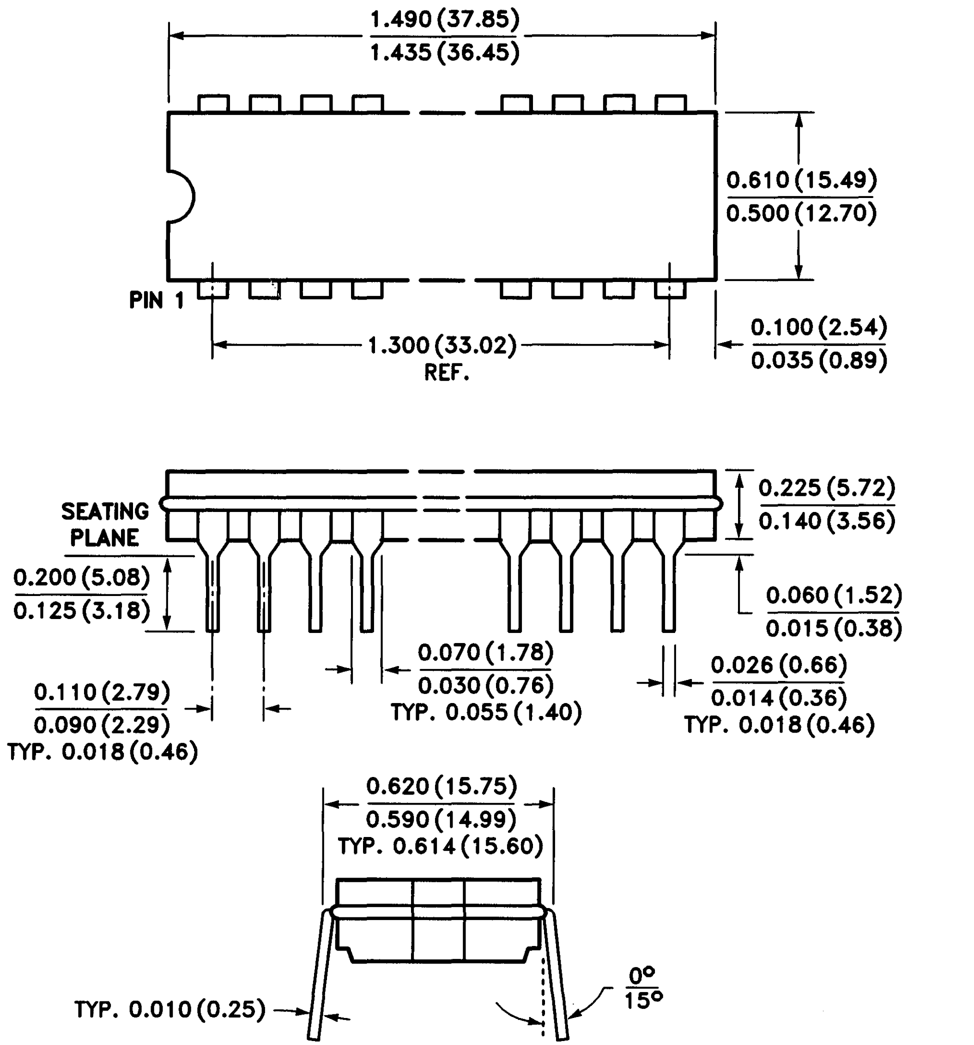
28-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

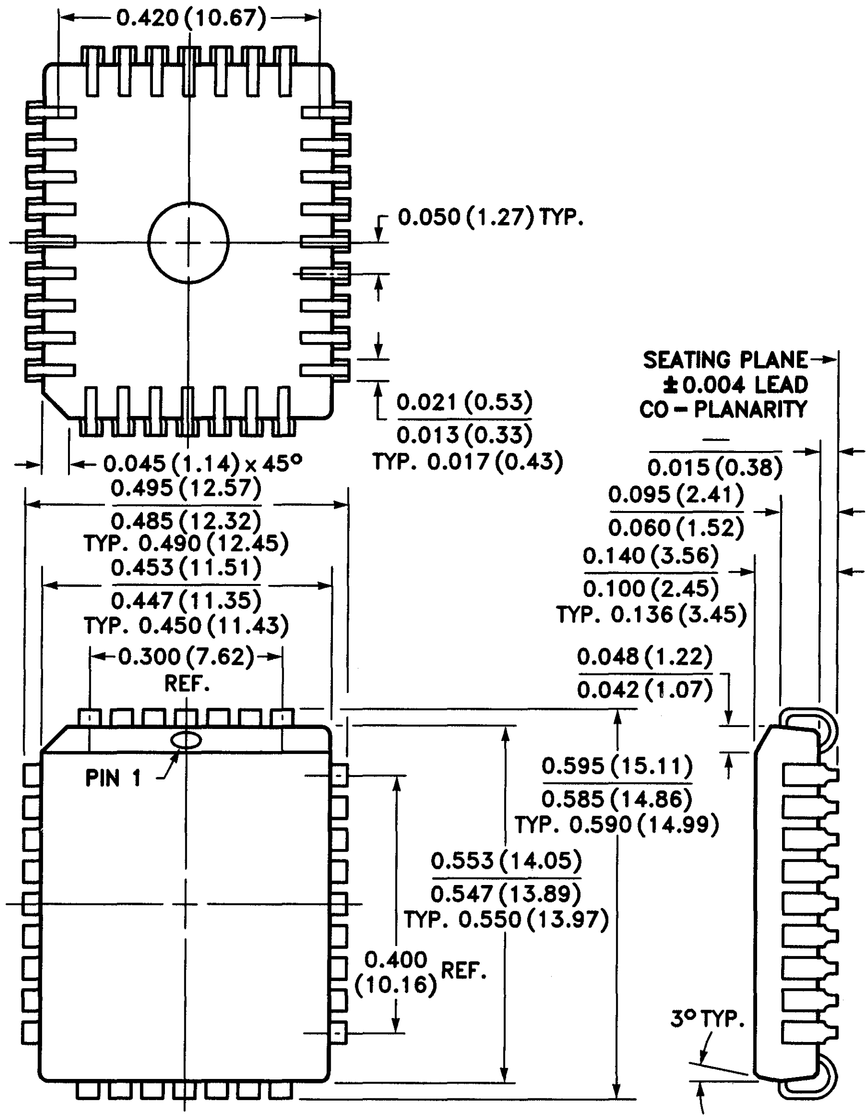
28-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J

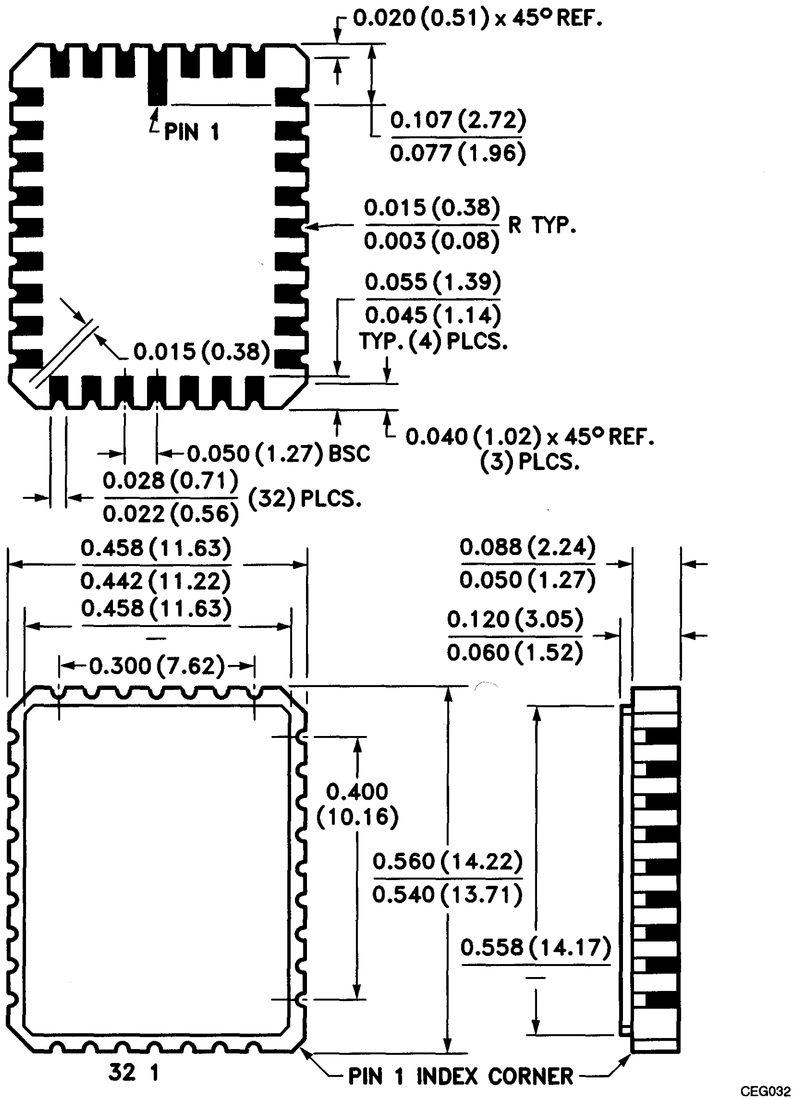


PJG032

NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. TOLERANCE: ± 1% NLT ± 0.005 (0.127)

NOTES

NOTES

NOTES

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U.S. Sales Offices

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TWX: 910-379-0033
Fax: 408/432-0640

7/88 Stock No. 200-176

ADVANCED INFORMATION

1M	Commercial Industrial	X28C010 X28C010I	128K x 8 Bit

Electrically Erasable PROM

FEATURES

- **Low Power CMOS**
  - **—50 mA Active Current Max.**
  - **—500 μA Standby Current Max.**
- **High Speed Page Write Operation**
- **Fast Write Cycle Times**
  - **—256-Byte Page Size**
  - **—Byte or Page Write Cycle: 5 ms Typical**
  - **—Complete Memory Rewrite: 2.5 Sec.**
  - **—Effective Byte Write Cycle Time: 19 μs**
- **End of Write Detection**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit Testing**
    - **—Accommodates Multiprocessor Applications**
- **Software Data Protection**
- **JEDEC Approved Byte-Wide Pinout for DIPs**

DESCRIPTION

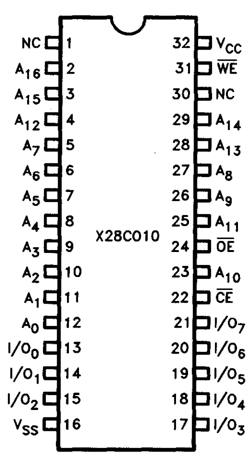
The Xicor X28C010 is a 128K x 8 E^2PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19 μs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C010 also features $\overline{\text{DATA}}$ Polling and Toggle Bit test, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports the Software Data Protection option.

Xicor E^2PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

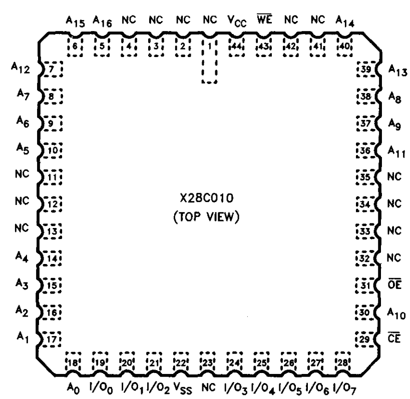
PIN CONFIGURATIONS

SIDE BRAZE



0104-1

LCC



0104-2

PIN NAMES

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias
X28C010 .... −10°C to +85°C
X28C010I.............................. −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground........................ −1.0V to +7V
D.C. Output Current.................................5 mA
Lead Temperature
(Soldering, 10 Seconds) ....300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X28C010 T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X28C010I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		500	μA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input Low Voltage	−1.0	0.8	V	
V_{IH}(1)	Input High Voltage	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to Read Operation	100	μs
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

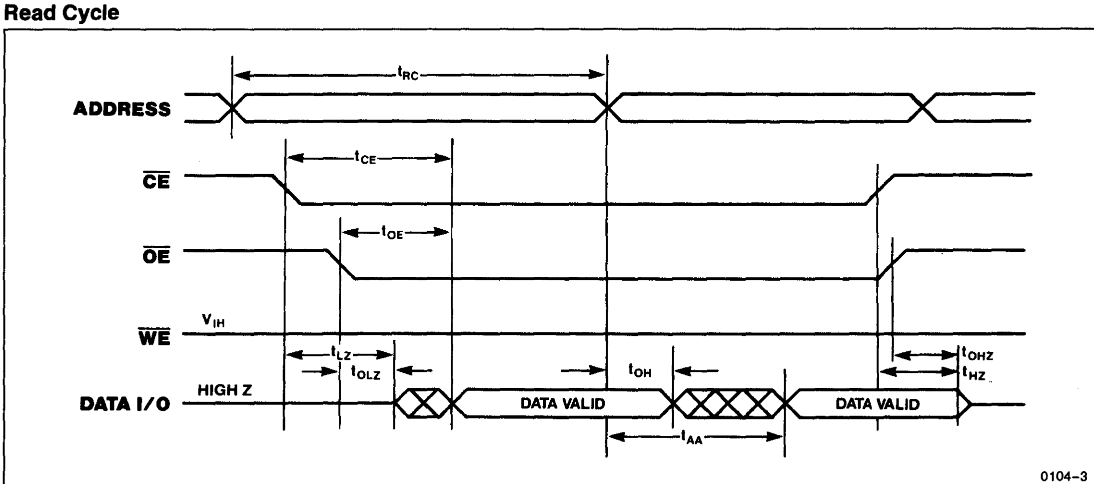
A.C. CHARACTERISTICS

X28C010 $T_A = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.
X28C010I $T_A = -40°C$ to $+85°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C010-20 X28C010I-20		X28C010-25 X28C010I-25		X28C010 X28C010I		X28C010-35 X28C010I-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		350		ns
t_{CE}	Chip Enable Access Time		200		250		300		350	ns
t_{AA}	Address Access Time		200		250		300		350	ns
t_{OE}	Output Enable Access Time		50		50		100		100	ns
t_{LZ}(3)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ High to High Z Output		50		50		50		50	ns
t_{OHZ}(4)	$\overline{OE}$ High to High Z Output		50		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle

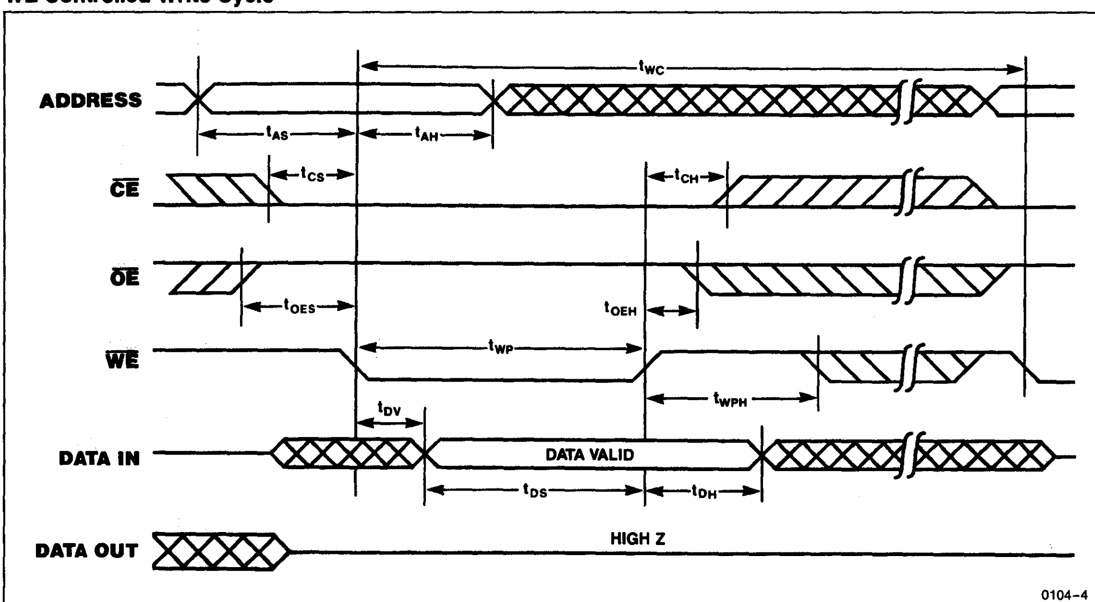


Notes: (3) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.
(4) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

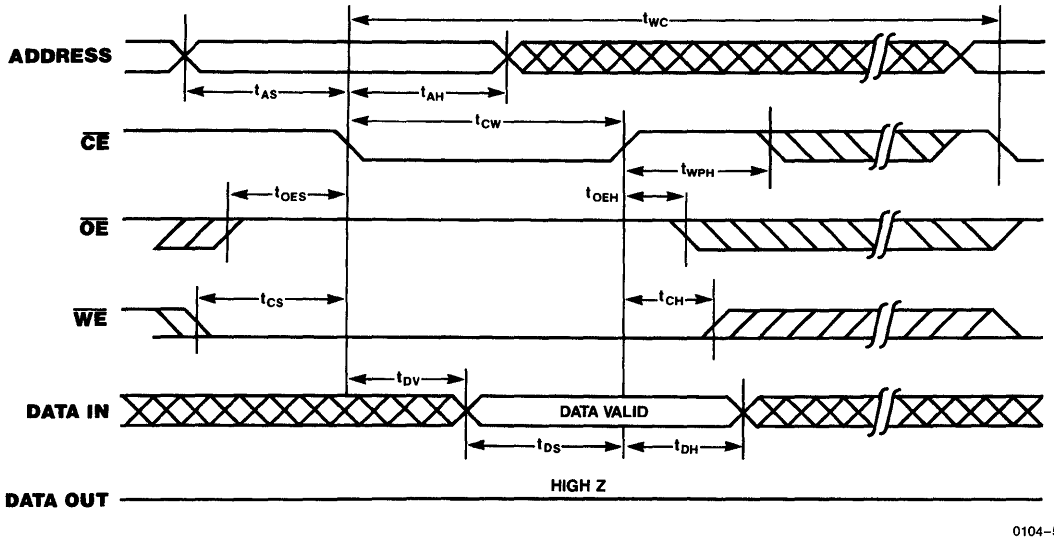
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		ns
t_{DV}	Data Valid		1	μs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		μs
t_{BLC}	Byte Load Cycle	0.20	200	μs

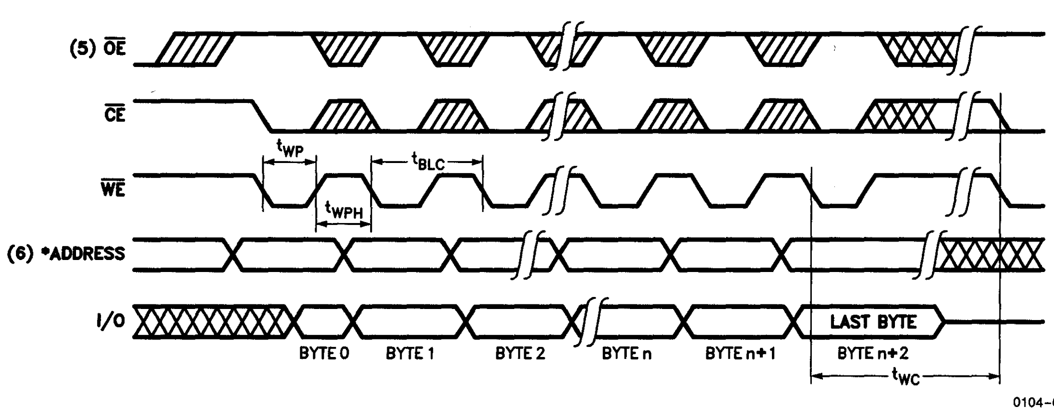
$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

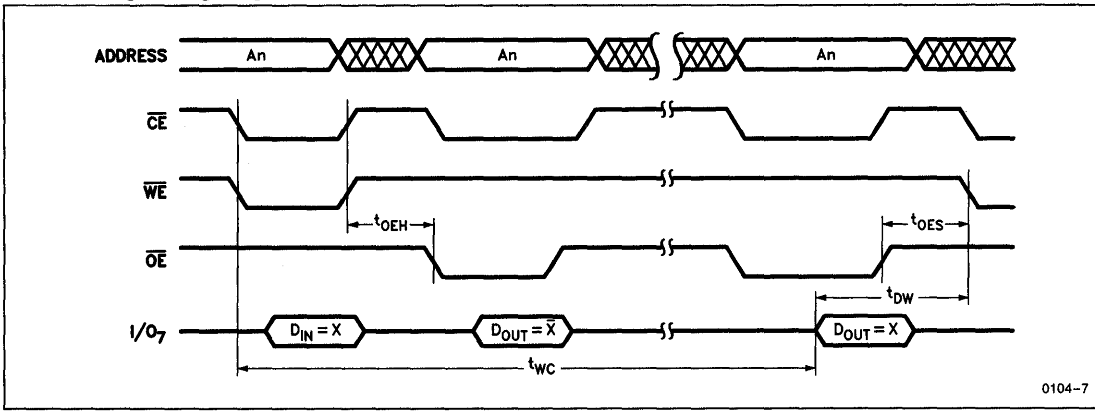


*For each successive write within the page write operation, A_8–A_{16} should be the same or writes to an unknown address could occur.

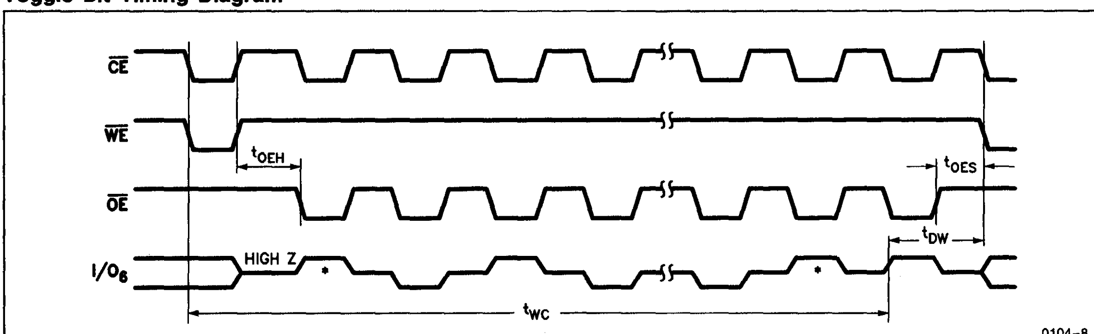
Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(7)

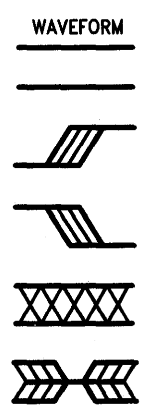


Toggle Bit Timing Diagram



*I/O_6 beginning and ending state will vary.

SYMBOL TABLE



WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C010 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C010.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

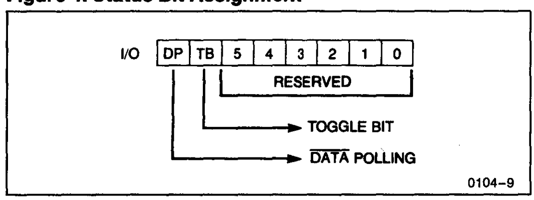
The page write feature of the X28C010 allows the entire memory to be written in 2.5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-five bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 200 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 200 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 200 μs.

Write Operation Status Bits

The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will alternate between one and zero on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O$_7$

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

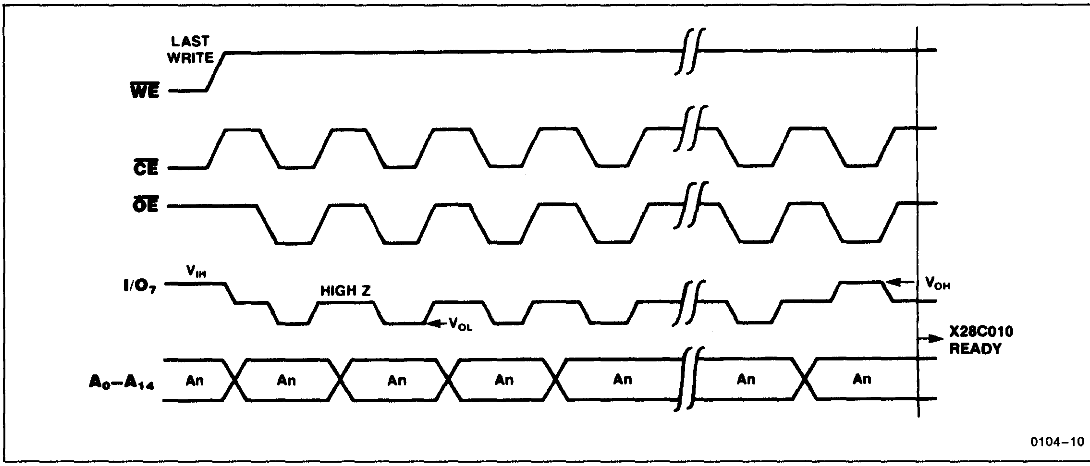
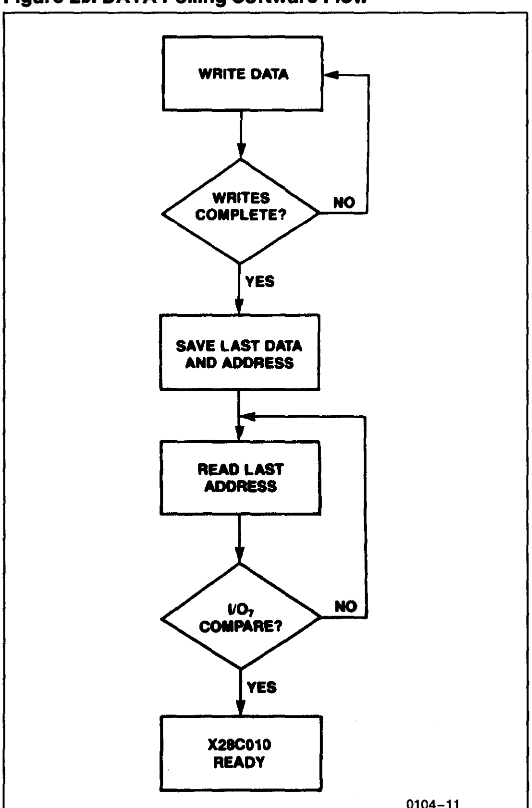


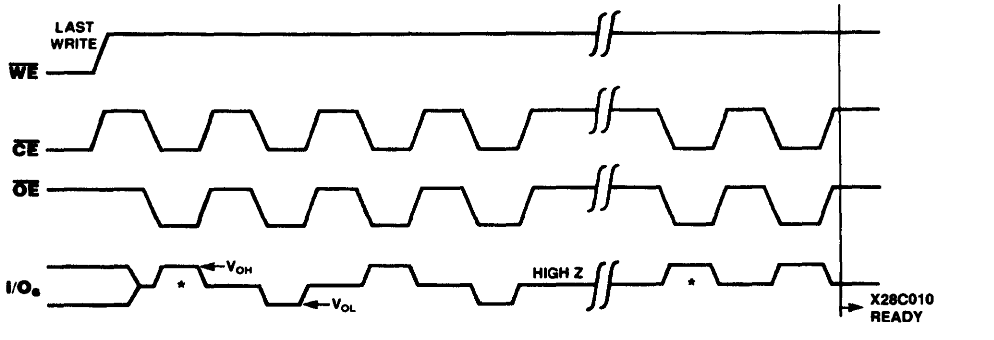
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

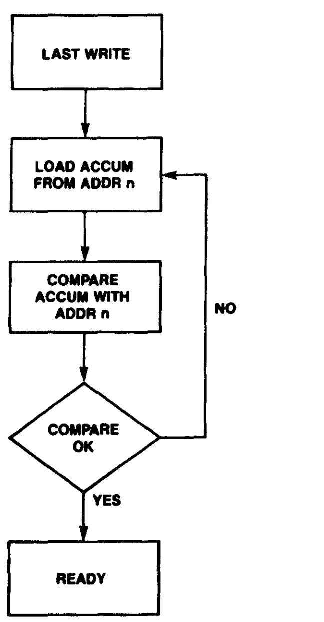
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3.8V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

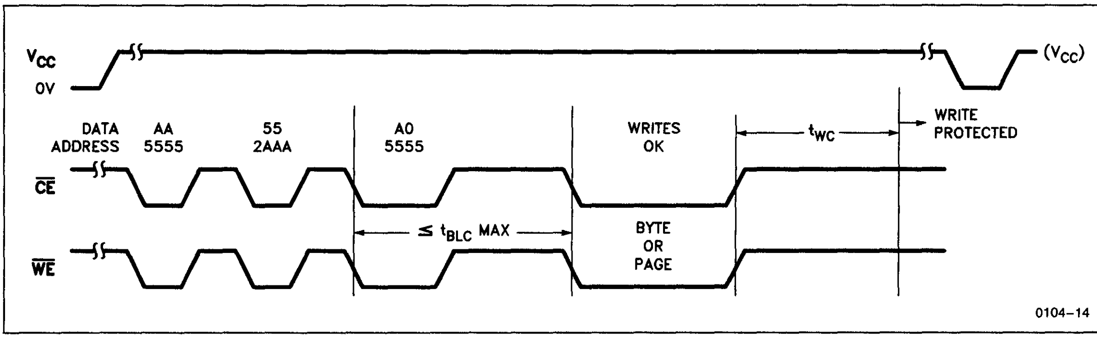
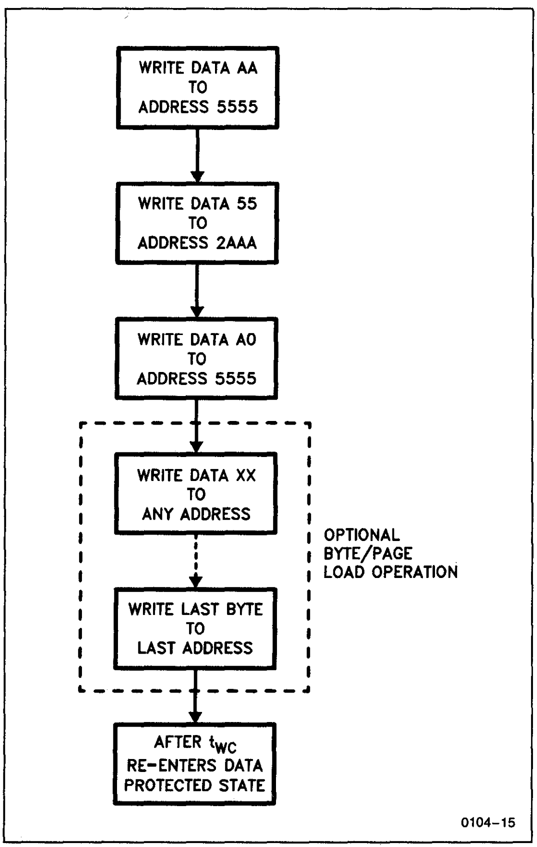


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

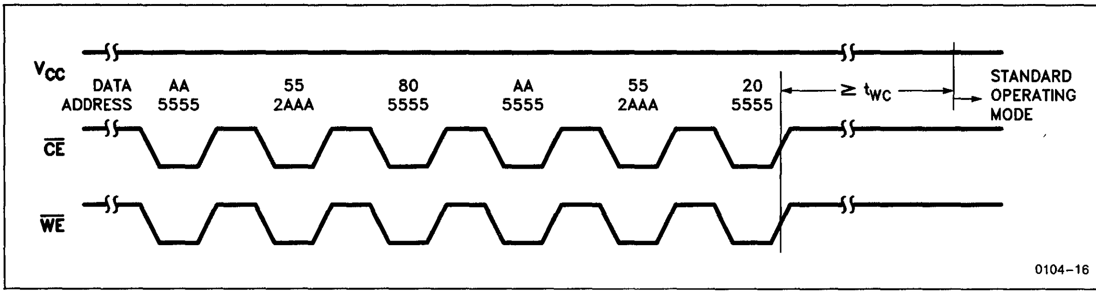
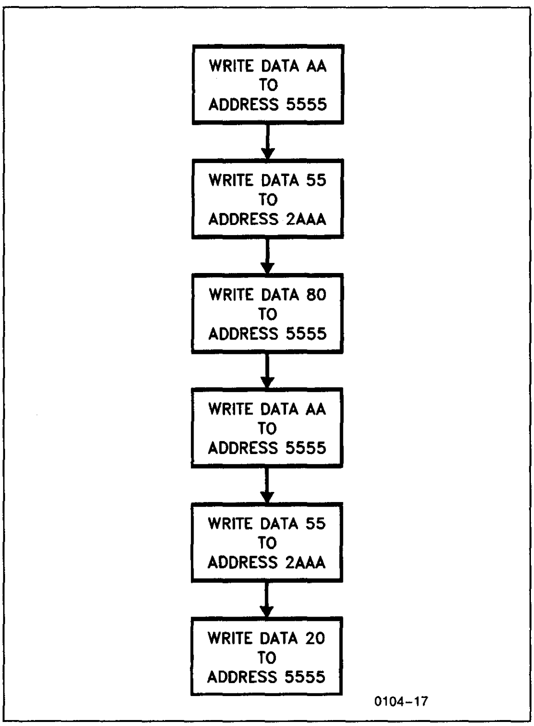


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E²PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

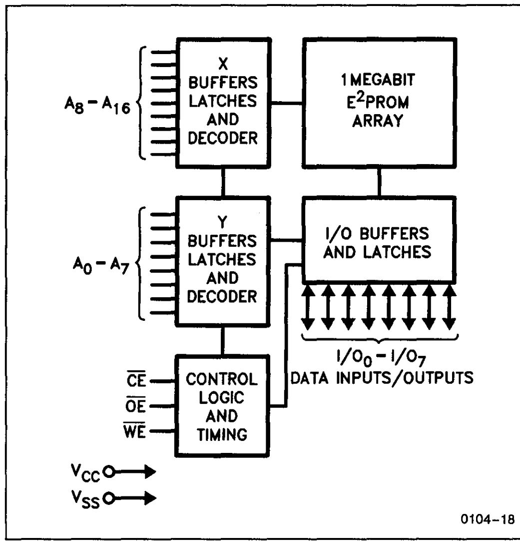
Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

1M E^{2}PROMs

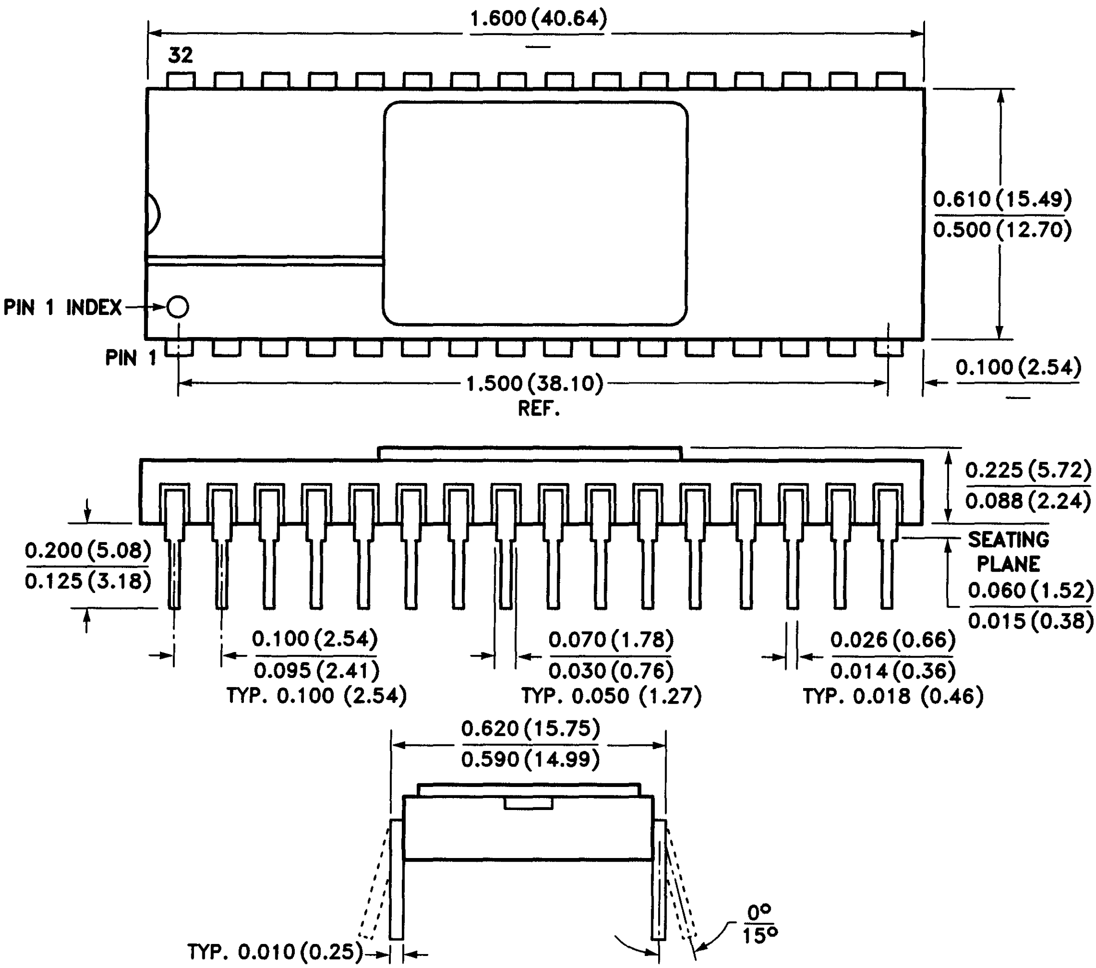
Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C010C-20	131072 x 8				•							†	200 ns	CMOS	Standard
X28C010C-25	131072 x 8				•							†	250 ns	CMOS	Standard
X28C010C	131072 x 8				•							†	300 ns	CMOS	Standard
X28C010C-35	131072 x 8				•							†	350 ns	CMOS	Standard
X28C010CI-20	131072 x 8				•							I	200 ns	CMOS	Standard
X28C010CI-25	131072 x 8				•							I	250 ns	CMOS	Standard
X28C010CI	131072 x 8				•							I	300 ns	CMOS	Standard
X28C010CI-35	131072 x 8				•							I	350 ns	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = Cerdip
C = 32-Lead Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 44-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

32-LEAD SIDE BRAZE PACKAGE TYPE C



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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ADVANCED INFORMATION

1M Military X28C010M 128K x 8 Bit

Electrically Erasable PROM

FEATURES

- **Low Power CMOS**
  - **—50 mA Active Current Max.**
  - **—500 μA Standby Current Max.**
- **High Speed Page Write Operation**
- **Fast Write Cycle Times**
  - **—256-Byte Page Size**
  - **—Byte or Page Write Cycle: 5 ms Typical**
  - **—Complete Memory Rewrite: 2.5 Sec.**
  - **—Effective Byte Write Cycle Time: 19 μs**
- **End of Write Detection**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Bit Testing**
    - **—Accommodates Multiprocessor Applications**
- **Software Data Protection**
- **JEDEC Approved Byte-Wide Pinout for DIPs**

DESCRIPTION

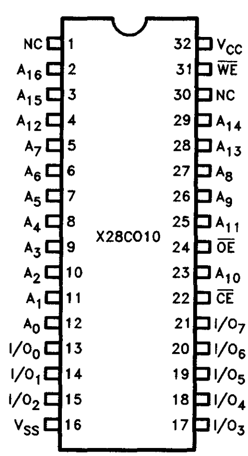
The Xicor X28C010 is a 128K x 8 E^{2}PROM, fabricated with Xicor's proprietary, high performance, floating gate CMOS technology. Like all Xicor programmable non-volatile memories the X28C010 is a 5V only device. The X28C010 features the JEDEC approved pinout for byte-wide memories, compatible with industry EPROMs.

The X28C010 supports a 256-byte page write operation, effectively providing a 19 μs/byte write cycle and enabling the entire memory to be written in less than 2.5 seconds. The X28C010 also features $\overline{\text{DATA}}$ Polling and Toggle Bit test, system software support schemes used to indicate the early completion of a write cycle. In addition, the X28C010 supports the Software Data Protection option.

Xicor E^{2}PROMs are designed and tested for applications requiring extended endurance. Data retention is specified to be greater than 10 years.

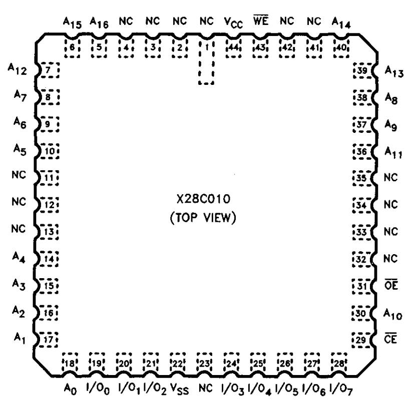
PIN CONFIGURATIONS

SIDE BRAZE



0103-1

LCC



0103-2

PIN NAMES

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{\text{WE}}$	Write Enable
$\overline{\text{CE}}$	Chip Enable
$\overline{\text{OE}}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

T_A = −55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		50	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)		3	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		500	μA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(1)	Input Low Voltage	−1.0	0.8	V	
V_{IH}(1)	Input High Voltage	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(2)	Power-Up to Read Operation	100	μs
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	10	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

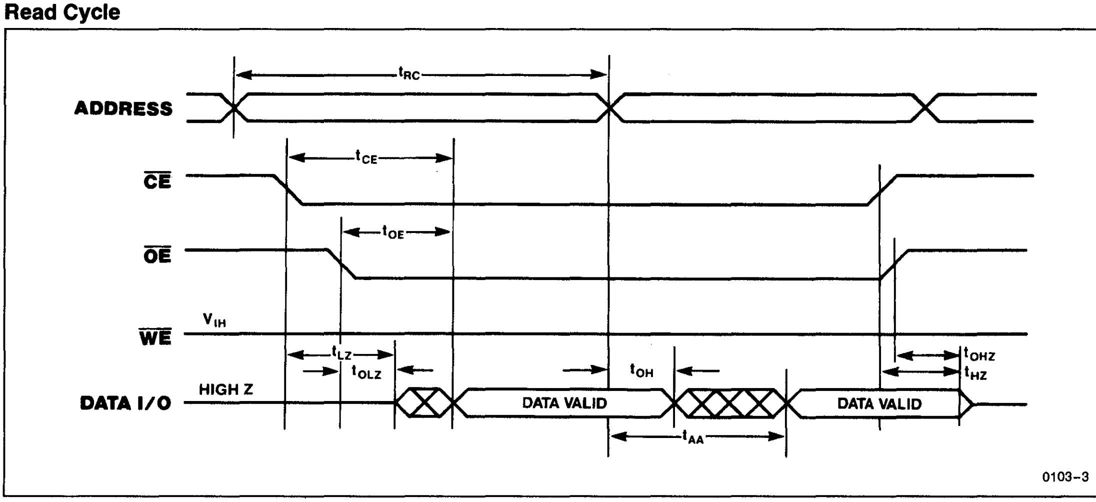
A.C. CHARACTERISTICS

$T_A = -55°C$ to $+125°C$, $V_{CC} = +5V \pm 10\%$, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	X28C010M-20		X28C010M-25		X28C010M		X28C010M-35		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	200		250		300		350		ns
t_{CE}	Chip Enable Access Time		200		250		300		350	ns
t_{AA}	Address Access Time		200		250		300		350	ns
t_{OE}	Output Enable Access Time		50		50		100		100	ns
t_{LZ}(3)	$\overline{CE}$ Low to Active Output	0		0		0		0		ns
t_{OLZ}(3)	$\overline{OE}$ Low to Active Output	0		0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ High to High Z Output		50		50		50		50	ns
t_{OHZ}(4)	$\overline{OE}$ High to High Z Output		50		50		50		50	ns
t_{OH}	Output Hold from Address Change	0		0		0		0		ns

Read Cycle



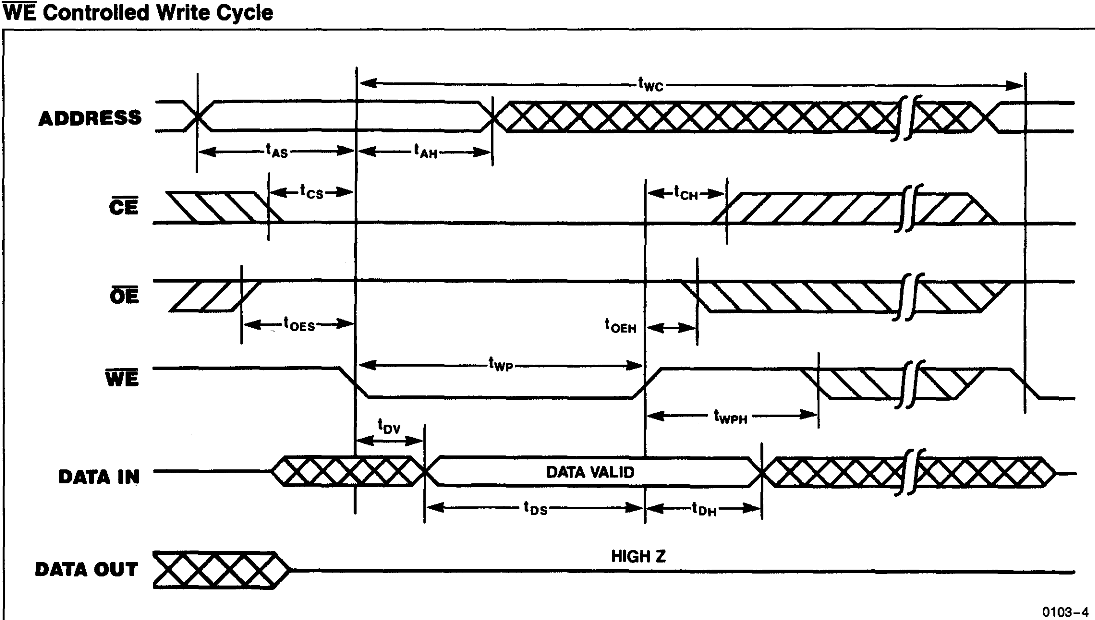
Notes: (3) t_{LZ} min. and t_{OLZ} min. are shown for reference only, they are periodically characterized and are not tested.

(4) t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

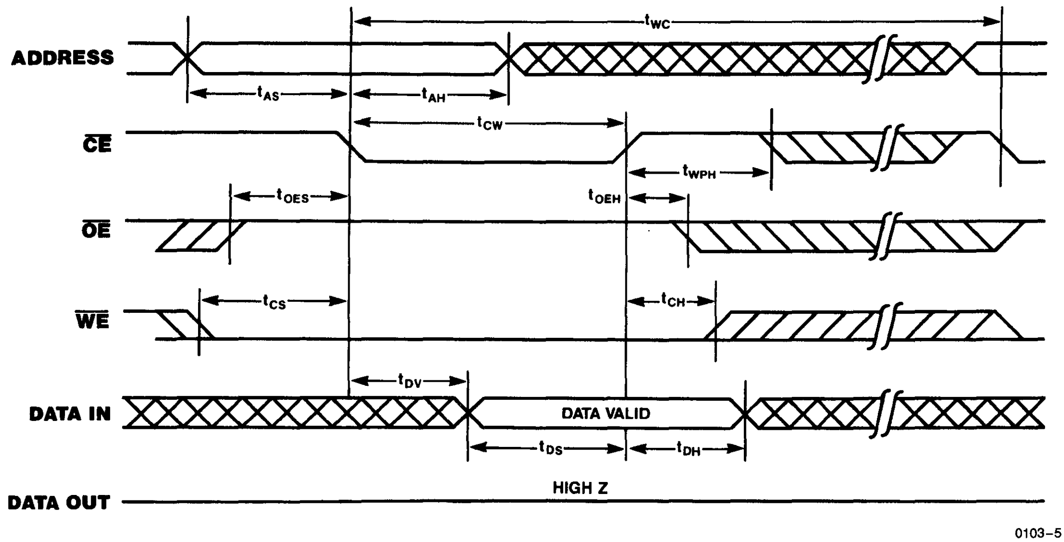
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time		10	ms
t_{AS}	Address Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Write Setup Time	0		ns
t_{CH}	Write Hold Time	0		ns
t_{CW}	$\overline{CE}$ Pulse Width	100		ns
t_{OES}	$\overline{OE}$ High Setup Time	10		ns
t_{OEH}	$\overline{OE}$ High Hold Time	10		ns
t_{WP}	$\overline{WE}$ Pulse Width	100		ns
t_{WPH}	$\overline{WE}$ High Recovery	100		ns
t_{DV}	Data Valid		1	µs
t_{DS}	Data Setup	50		ns
t_{DH}	Data Hold	10		ns
t_{DW}	Delay to Next Write	10		µs
t_{BLC}	Byte Load Cycle	0.20	200	µs

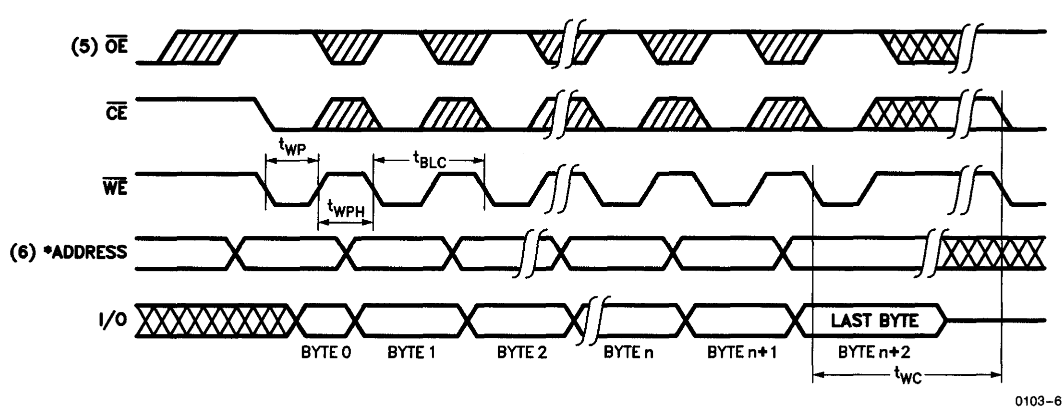
$\overline{WE}$ Controlled Write Cycle



$\overline{CE}$ Controlled Write Cycle



Page Write Cycle

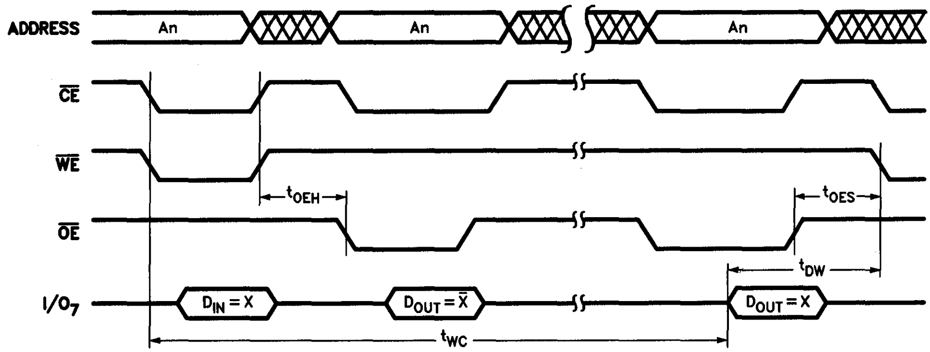


*For each successive write within the page write operation, A_8–A_{16} should be the same or writes to an unknown address could occur.

Notes: (5) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

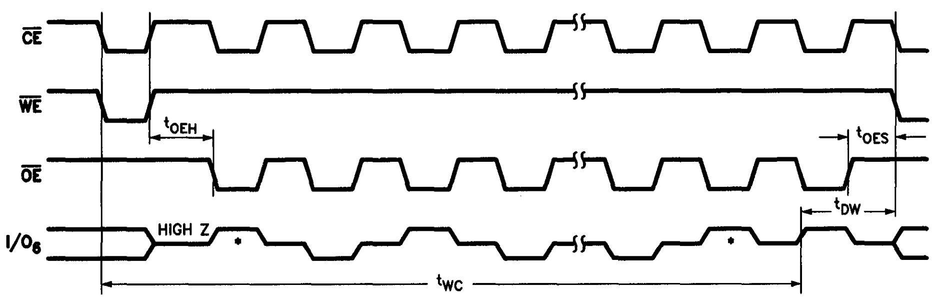
(6) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram[7]



0103-7

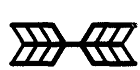
Toggle Bit Timing Diagram



0103-8

*I/O_6 beginning and ending state will vary.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Note: (7) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28C010 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28C010.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The X28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms.

Page Write Operation

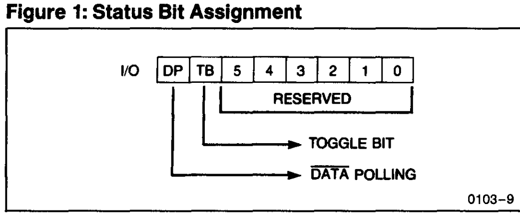
The page write feature of the X28C010 allows the entire memory to be written in 2.5 seconds. Page write allows two to two hundred fifty-six bytes of data to be consecutively written to the X28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_8 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to two hundred fifty-five bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 200 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 200 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 200 μs.

Write Operation Status Bits

The X28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the X28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The X28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will alternate between one and zero on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

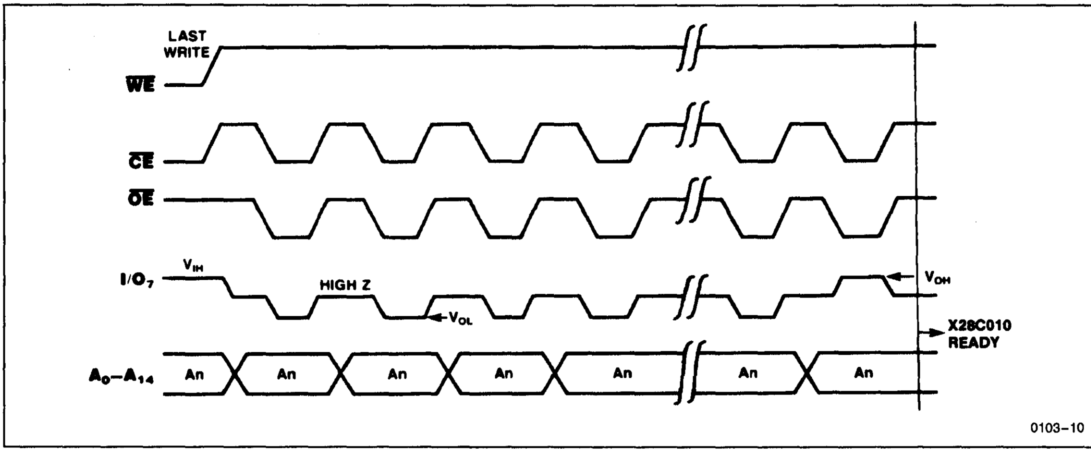
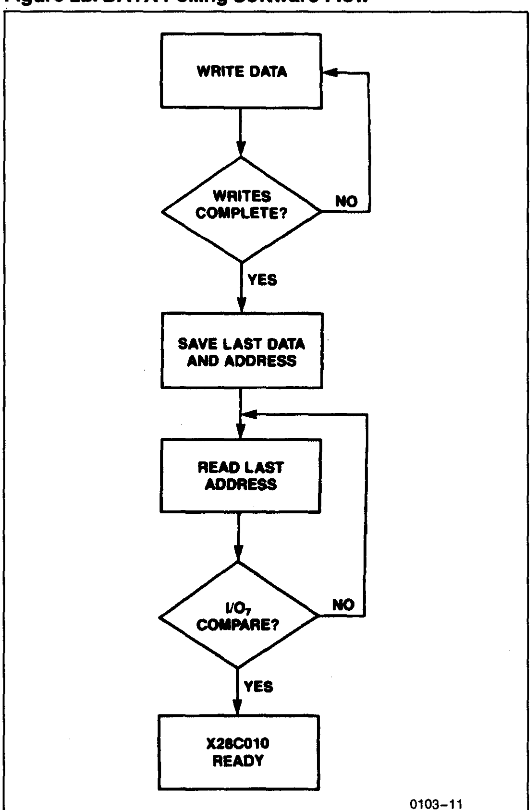


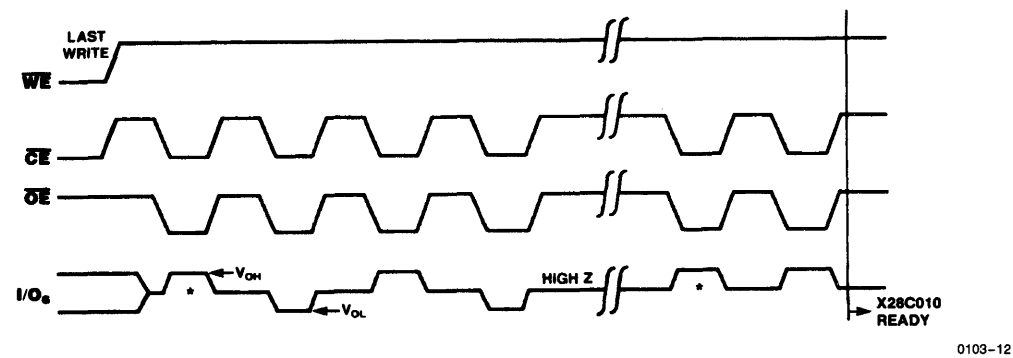
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the X28C010. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

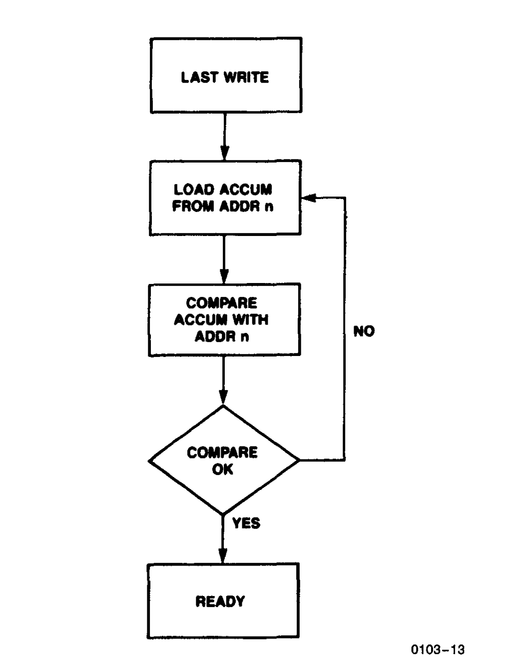
THE TOGGLE BIT I/O_6

Figure 3a: Toggle Bit Bus Sequence



*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple X28C010 memories that is frequently updated. Toggle Bit testing can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 10 ns will not initiate a write cycle.
- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is $\leq$3.8V.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28C010 offers a software controlled data protection feature. The X28C010 is shipped from Xicor with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28C010 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device unless the reset command is issued.

Once the software protection is enabled, the X28C010 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 4a and 4b for the sequence. The three byte sequence opens the page write window enabling the host to write from one to two hundred fifty-six bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

SOFTWARE DATA PROTECTION

Figure 4a: Timing Sequence—Byte or Page Write

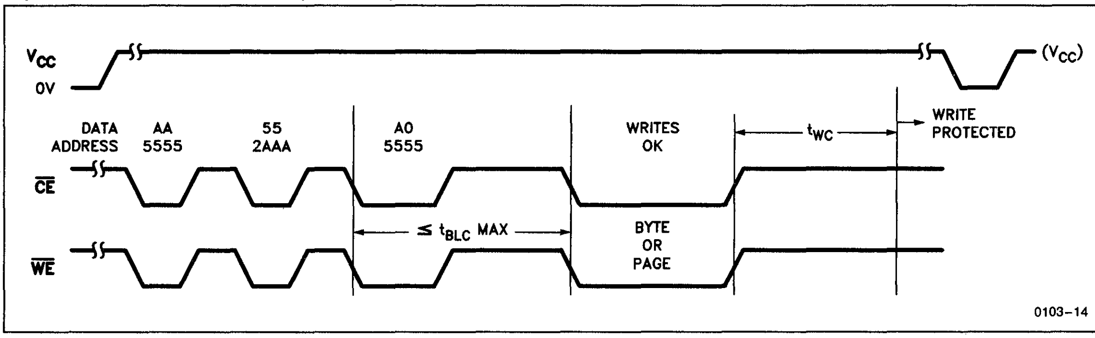
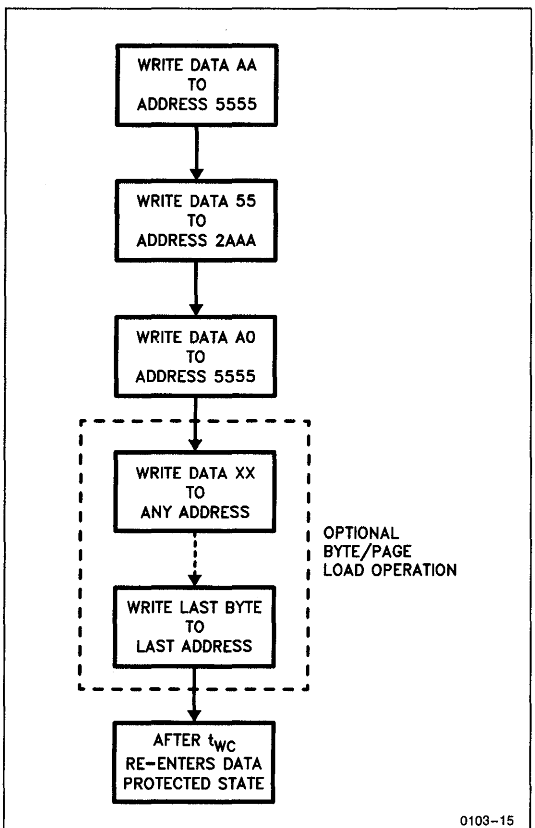


Figure 4b: Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used and data has been written, the X28C010 will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the X28C010 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence

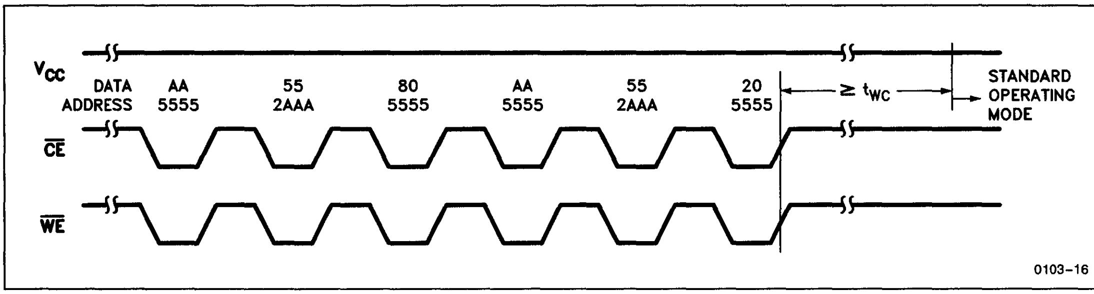
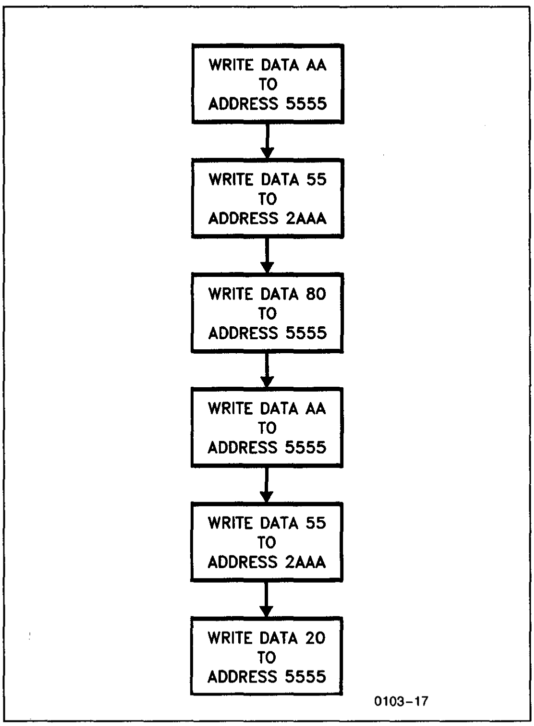


Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E[2]PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28C010 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

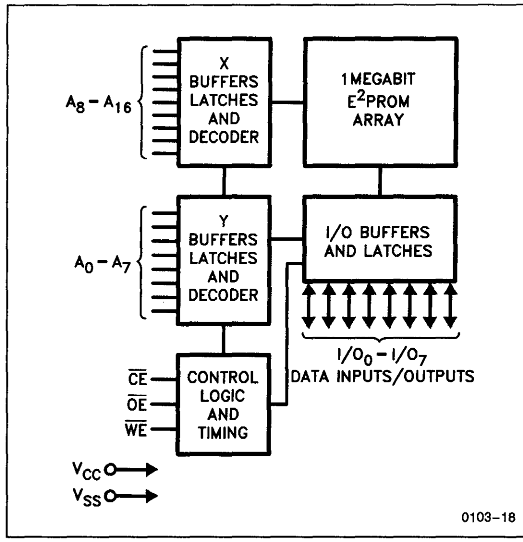
Because the X28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

1M E2PROMs

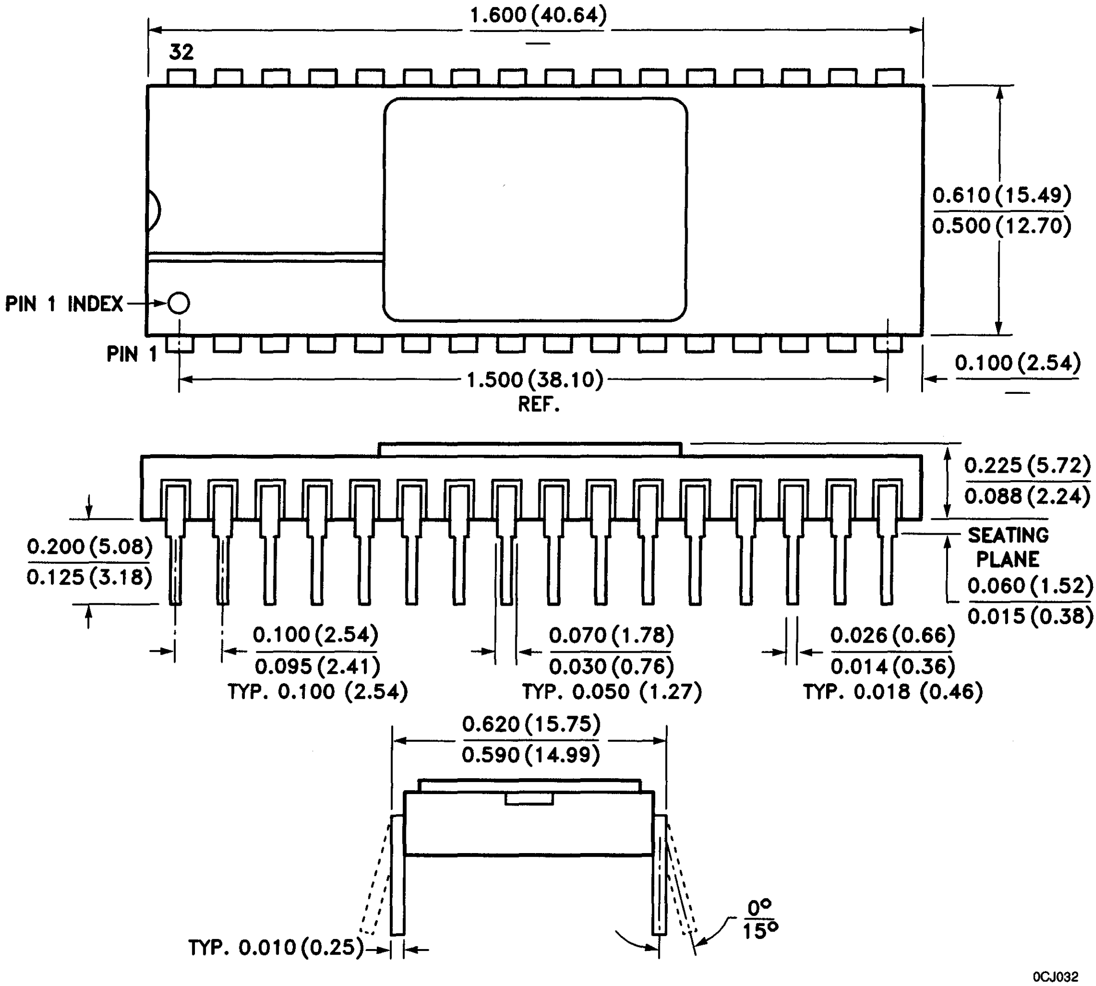
Device Order Number	Organization	Package										Temp. Range	Access Time	Process Technology	Processing Level
		S	P	D	C	F1	F2	K	J	E	G				
X28C010CM-20	131072 x 8				•							M	200 ns	CMOS	Standard
X28C010CM-25	131072 x 8				•							M	250 ns	CMOS	Standard
X28C010CM	131072 x 8				•							M	300 ns	CMOS	Standard
X28C010CM-35	131072 x 8				•							M	350 ns	CMOS	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = Plastic Small Outline Gull Wing
P = Plastic DIP
D = Cerdip
C = 32-Lead Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = 44-Pad Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

32-LEAD SIDE BRAZE PACKAGE TYPE C



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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PRELIMINARY INFORMATION

1Megabit Module XM28C010 128K x 8 Bit

Electrically Erasable PROM

FEATURES

- **High Density 1Megabit (128K x 8) E²PROM Module**
- **Access Time of 250 ns at −55°C to +125°C**
- **Base Memory Component: Xicor CMOS X28C256**
- **JEDEC Standard 32-Pin 600 Mil Wide Ceramic Side Braze Package**
- **Pin Compatible with the X28C010 1Megabit Monolithic CMOS E²PROM**
- **Fast Write Cycle Times Supported by:**
  - **—Internal Program Cycle 10 ms Max.**
  - **—64-Byte Page**
  - **—$\overline{\text{DATA}}$ Polling**
  - **—Toggle Status Bit**
- **High Rel Module Available with:**
  - **—100% MIL-STD-883 Compliant Components**
  - **—100% Screening and MIL-STD-883 Processing of Modules**
- **Software Data Protection**

DESCRIPTION

The XM28C010 is a high density 1Megabit E²PROM comprised of four X28C256 32K x 8 LCCs mounted on a co-fired multilayered ceramic substrate. The XM28C010 is configured 128K x 8 bit and features the JEDEC approved pinout for byte-wide memories, compatible with the monolithic X28C010.

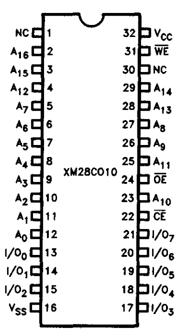
The XM28C010 is available in commercial, industrial and military temperature ranges. The military temperature range module is built with MIL-STD-883 Class B microcircuit components. In addition, after being assembled all High Rel modules undergo 100% screening.

The XM28C010 supports a 64-byte page write operation, this, combined with $\overline{\text{DATA}}$ Polling or Toggle Bit testing, effectively provides a 78 μs/byte write cycle, enabling the module memory array to be rewritten in 10 seconds.

The XM28C010 will also support Software Data Protection, a user-optional method of protecting data during power transitions.

The XM28C010 provides the same high endurance and data retention as the base memory components.

PIN CONFIGURATION

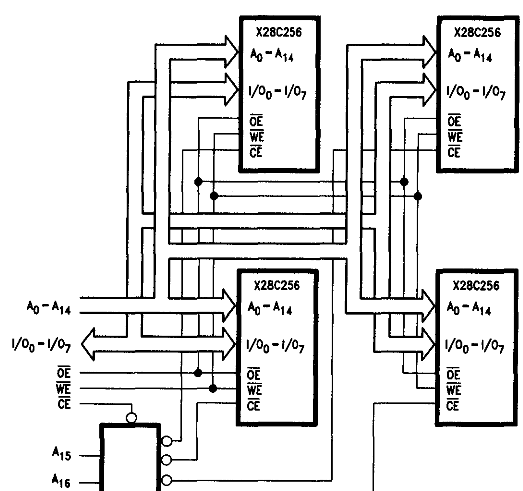


0091-1

PIN NAMES

A_0–A_{16}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

FUNCTIONAL DIAGRAM



0091-2

Characteristics subject to change without notice

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on any Pin with
Respect to Ground .... −1.0V to +7V
D.C. Output Current .... 5 mA
Lead Temperature
(Soldering, 10 Seconds) .... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

XM28C010 T_A = 0°C to +75°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010M T_A = −55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits Min.	Limits Max.	Units	Test Conditions
I_{CC}	V_{CC} Current (Active) (TTL Inputs)		70	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = Open, 1 Device Active Address Inputs = TTL Levels @ f = 5 MHz
I_{SB_1}	V_{CC} Current (Standby) (TTL Inputs)		15	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{IH}
I_{SB_2}	V_{CC} Current (Standby) (CMOS Inputs)		800	μA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = Open, Other Inputs = V_{CC}
I_{LI}	Input Leakage Current		10	μA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	μA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}	Input Low Voltage	−1.0	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA

TYPICAL POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Units
t_{PUR}(2)	Power-Up to Read Operation	100	μs
t_{PUW}(2)	Power-Up to Write Operation	5	ms

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(2)	Input/Output Capacitance	40	pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	24	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	Write Inhibit	—	—
X	X	H	Write Inhibit	—	—

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) This parameter is periodically sampled and not 100% tested.

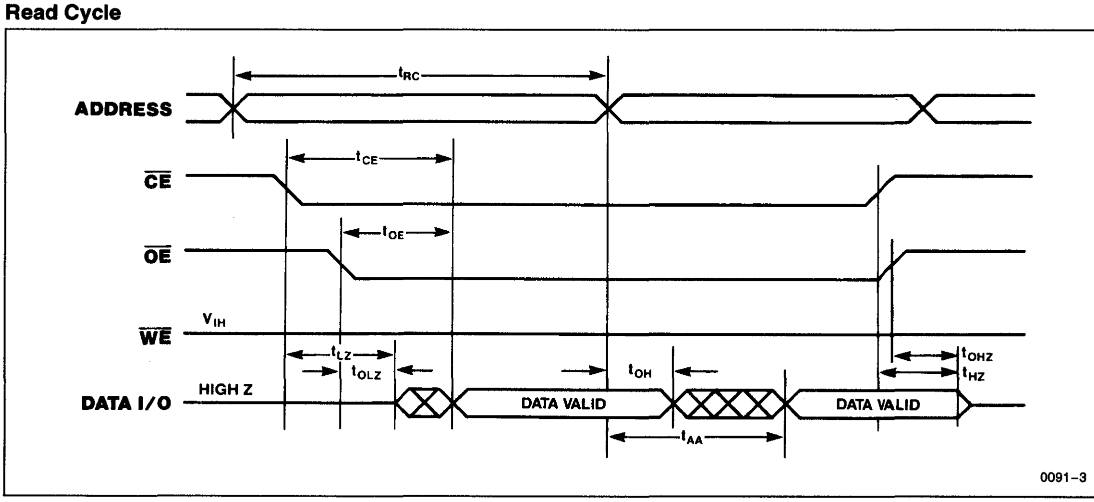
A.C. CHARACTERISTICS

XM28C010 T_A = 0°C to +75°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010I T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.
XM28C010M T_A = −55°C to +125°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	XM28C010-25		XM28C010		Units
		Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	250		300		ns
t_{CE}	Chip Enable Access Time		250		300	ns
t_{AA}	Address Access Time		250		300	ns
t_{OE}	Output Enable Access Time		100		100	ns
t_{LZ}	$\overline{CE}$ Low to Active Output	0		0		ns
t_{OLZ}	$\overline{OE}$ Low to Active Output	0		0		ns
$t_{HZ}^{(3)}$	$\overline{CE}$ High to High Z Output	0	100	0	100	ns
$t_{OHZ}^{(3)}$	$\overline{OE}$ High to High Z Output	0	100	0	100	ns
t_{OH}	Output Hold from Address Change	0		0		ns

Read Cycle

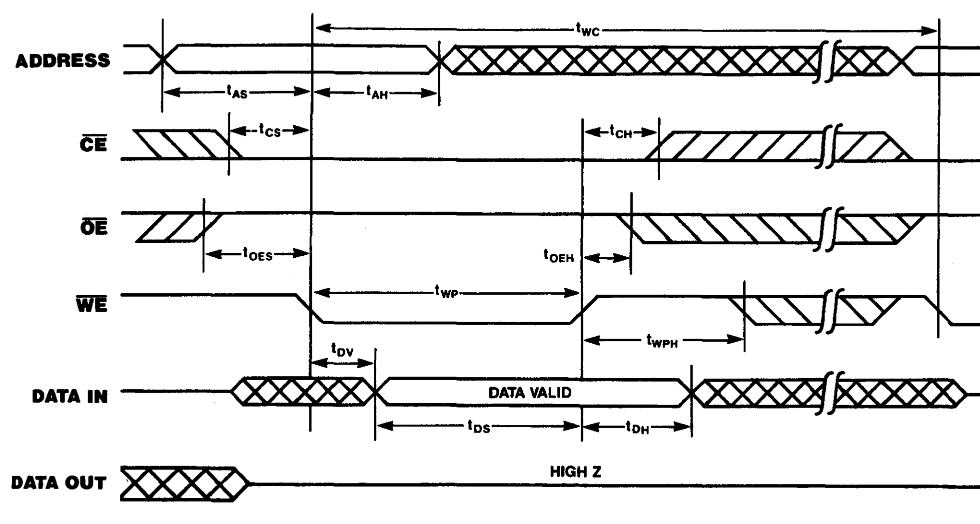


Note: (3) t_{HZ} and t_{OHZ} are measured from the point when $\overline{CE}$ or $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

Write Cycle Limits

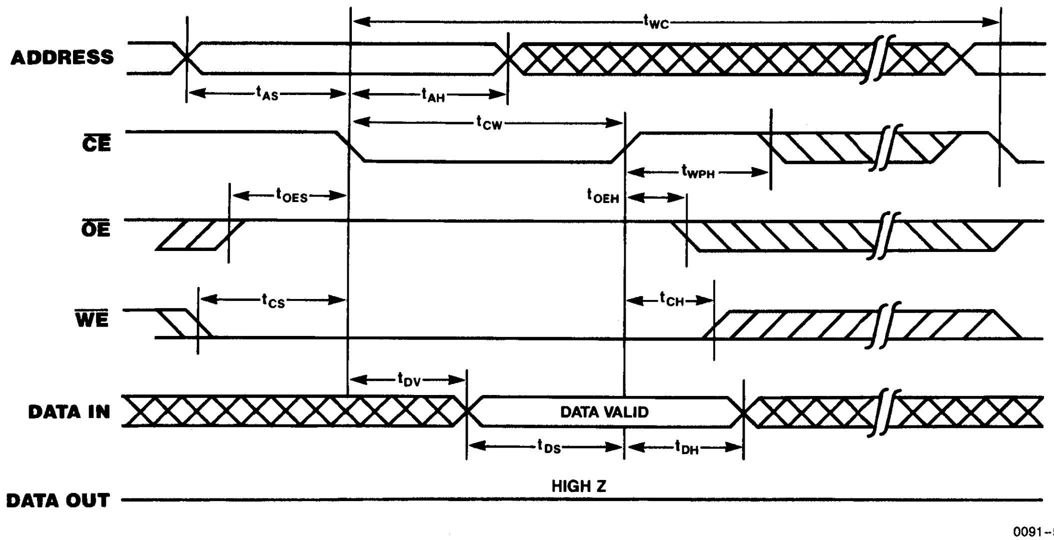
Symbol	Parameter	WE Controlled Write		CE Controlled Write(4)		Units
		Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time		10		10	ms
t_{AS}	Address Setup Time	0		0		ns
t_{AH}	Address Hold Time	150		175		ns
t_{CS}	Write Setup Time	25		0		ns
t_{CH}	Write Hold Time	0		25		ns
t_{CW}	CE Pulse Width	125		100		ns
t_{OES}	OE High Setup Time	10		10		ns
t_{OEH}	OE High Hold Time	10		35		ns
t_{WP}	WE Pulse Width	100		125		ns
t_{WPH}	WE High Recovery	1		1		µs
t_{DV}	Data Valid		1		1	µs
t_{DS}	Data Setup	50		50		ns
t_{DH}	Data Hold	10		35		ns
t_{DW}	Delay to Next Write	10		10		µs
t_{BLC}	Byte Load Cycle	1	100	1	100	µs

WE Controlled Write Cycle

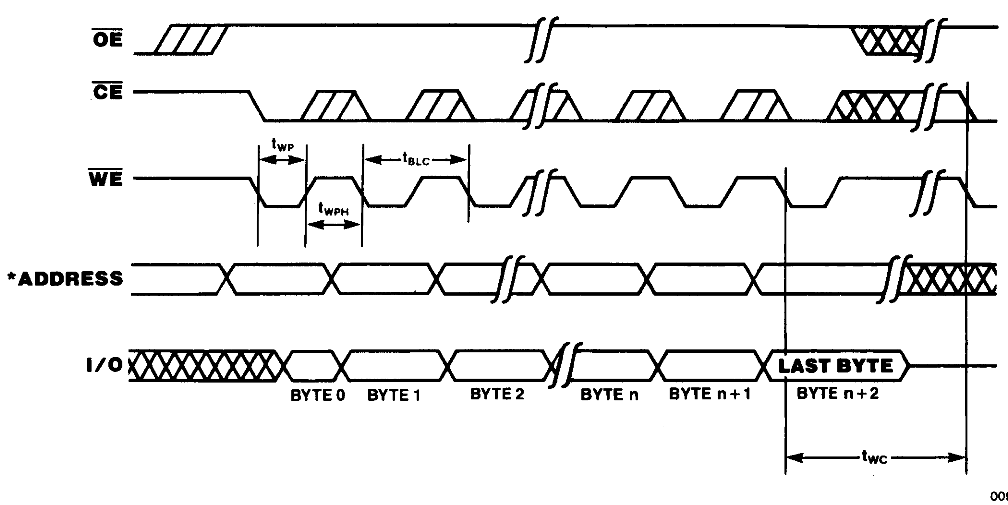


Note: (4) Due to the inclusion of the decoder IC on board the module the WE and CE write controlled timings will vary. When utilizing the CE controlled write operation all the hold timings must be extended by the worst case propagation delay of the decoder. For a WE controlled write operation CE must be a minimum 125 ns to accommodate the additional setup time required.

$\overline{CE}$ Controlled Write Cycle

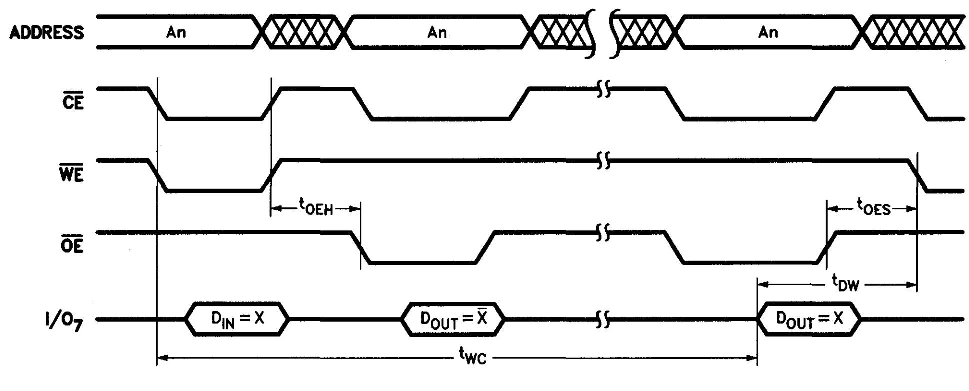


Page Write Cycle

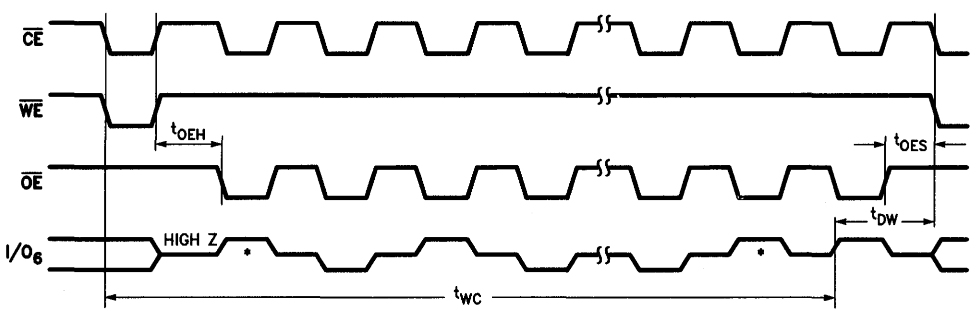


*For each successive write within the page write operation, A_6–A_{16} should be the same or writes to an unknown address could occur.

$\overline{\text{DATA}}$ Polling Timing Diagram



Toggle Bit Timing Diagram



*Starting and ending state of I/O_6 will vary, depending upon actual t_{WC}.

PIN DESCRIPTIONS

Addresses (A_0–A_{16})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced (see Note 4).

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the XM28C010 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the XM28C010.

DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This 2-line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The XM28C010 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 5 ms (see Note 4).

Page Write Operation

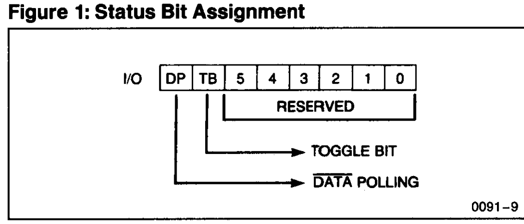
The page write feature of the XM28C010 allows the entire memory to be written in 10 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the XM28C010 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{16}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 μs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 μs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 μs.

Write Operation Status Bits

The XM28C010 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1: Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The XM28C010 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the XM28C010, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data. Note: If the XM28C010 is in the protected state and an illegal write operation is attempted $\overline{DATA}$ Polling will not operate.

Toggle Bit (I/O_6)

The XM28C010 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the last byte written. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{\text{DATA}}$ POLLING I/O_7

Figure 2a: $\overline{\text{DATA}}$ Polling Bus Sequence

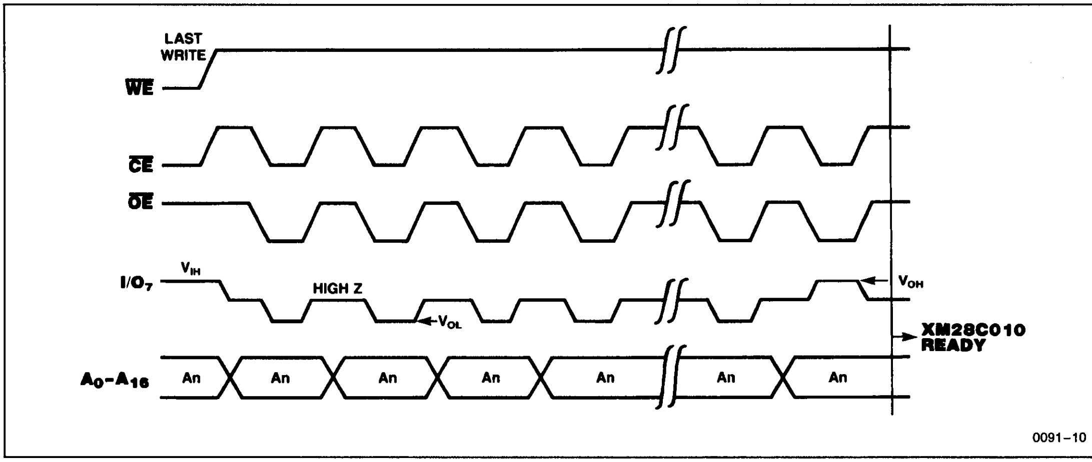
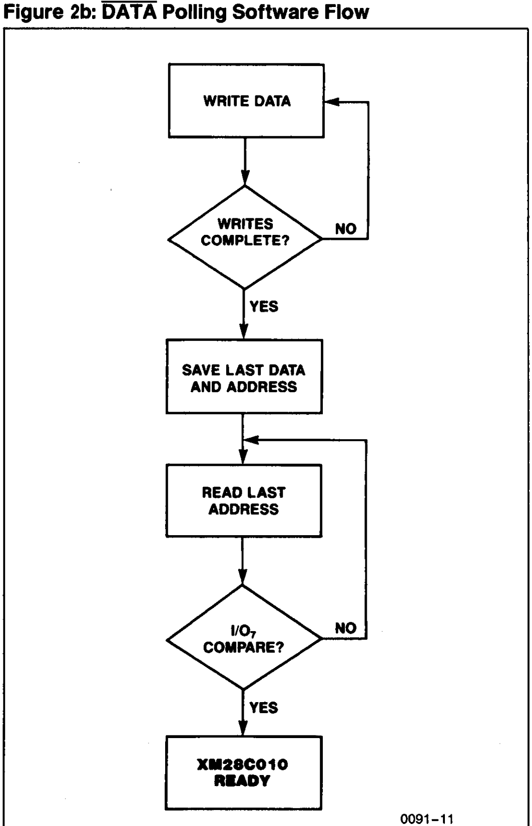


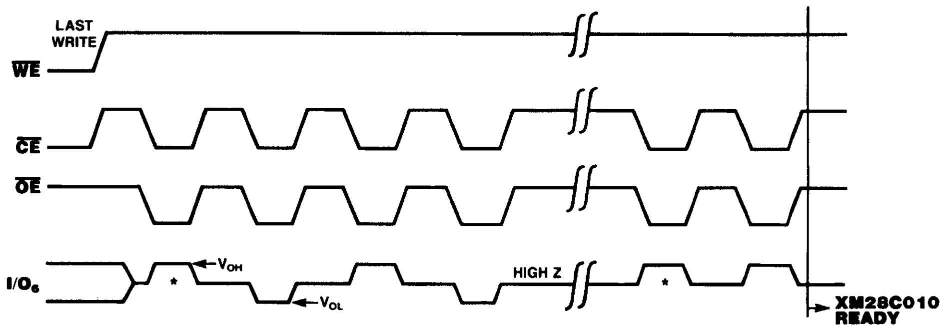
Figure 2b: $\overline{\text{DATA}}$ Polling Software Flow



$\overline{\text{DATA}}$ Polling can effectively halve the time for writing to the XM28C010. The timing diagram in Figure 2a illustrates the sequence of events on the bus. The software flow diagram in Figure 2b illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

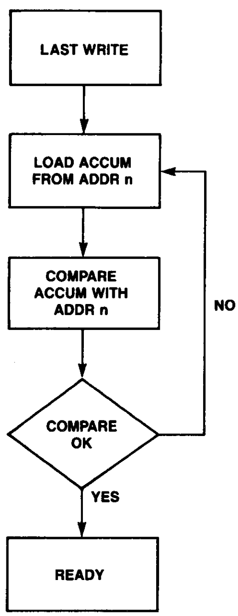
Figure 3a: Toggle Bit Bus Sequence



0091-12

*Beginning and ending state of I/O_6 will vary.

Figure 3b: Toggle Bit Software Flow



0091-13

The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{\text{DATA}}$ Polling. This can be especially helpful in an array comprised of multiple XM28C010 memories that is frequently updated. The timing diagram in Figure 3a illustrates the sequence of events on the bus. The software flow diagram in Figure 3b illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The XM28C010 provides three hardware features that protect nonvolatile data from inadvertent writes.

- Noise Protection—A $\overline{WE}$ pulse less than 20 ns will not initiate a write cycle.
- Default V_{CC} Sense—All functions are inhibited when V_{CC} is $\leq$3V.
- Write Inhibit—Holding $\overline{OE}$ LOW will prevent an inadvertent write cycle during power-on and power-off.

SOFTWARE DATA PROTECTION

The XM28C010 does provide the Software Data Protection (SDP) feature. Because the module is comprised of four discrete X28C256 LCCs, the algorithm will differ from the algorithm employed for the monolithic 1Megabit X28C010.

The module is shipped from Xicor with the Software Data Protect NOT ENABLED; that is, the module will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host system will then have open read and write access of the module once V_{CC} is stable.

The module can be automatically protected during power-up/-down without the need for external circuits by employing the SDP feature. The internal SDP circuit is enabled after the first write operation utilizing the SDP command sequence.

When this feature is employed, it will be easiest to incorporate in the system software if the module is viewed as a subsystem composed of four discrete memory devices with an address decoder (see Functional Diagram). In this manner, system memory mapping will extend onto the module. That is, the discrete memory ICs and decoder should be considered memory board components and SDP can be implemented at the component level as described below.

SOFTWARE COMMAND SEQUENCE

A_{15} and A_{16} are used by the decoder to select one of the four LCCs. Therefore, only one of the four memory devices can be accessed at one time. In order to protect the entire module, the command sequence must be issued separately to each device.

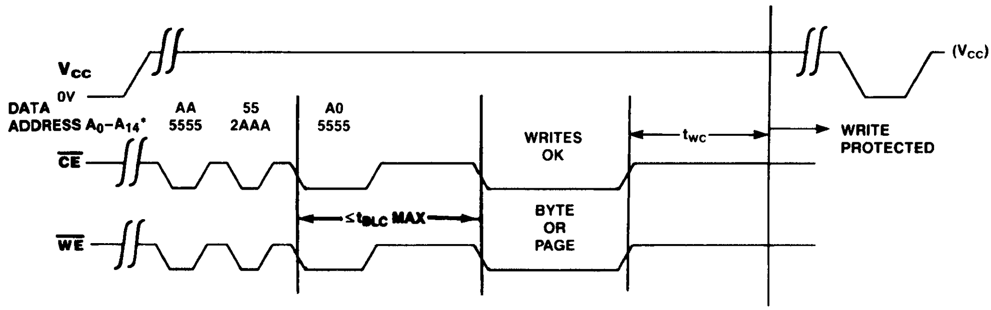
Enabling the software data protection mode requires the host system to issue a series of three write operations: each write operation must conform to the data and address sequence illustrated in Figures 4a and 4b. Because this involves writing to a nonvolatile bit the device will become protected after t_{WC} has elapsed. After this point in time devices will inhibit inadvertent write operations.

Once in the protected mode, authorized writes may be performed by issuing the same command sequence that enables SDP, immediately followed by the address/data combination desired. The command sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the data has been written, the device will automatically be returned to the protected state.

In order to facilitate testing of the devices the SDP mode can be deactivated. This is accomplished by issuing a series of six write operations: each write operation must conform to the data and address sequence illustrated in Figures 5a and 5b. This is a nonvolatile operation, and the host will have to wait a minimum t_{WC} before attempting to write new data.

SOFTWARE DATA PROTECTION

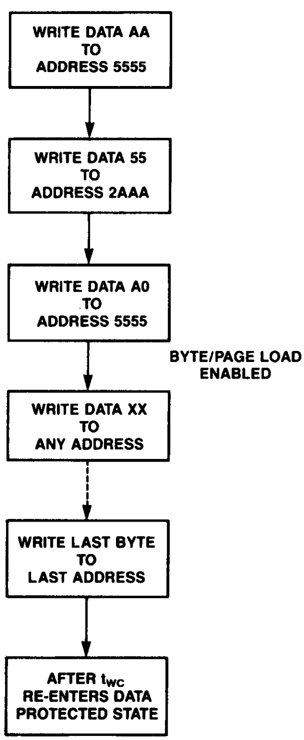
Figure 4a: Timing Sequence—Byte or Page Write



0091-14

*A_{15} & A_{16} select one of four devices on the module.

Figure 4b: Write Sequence for Software Data Protection

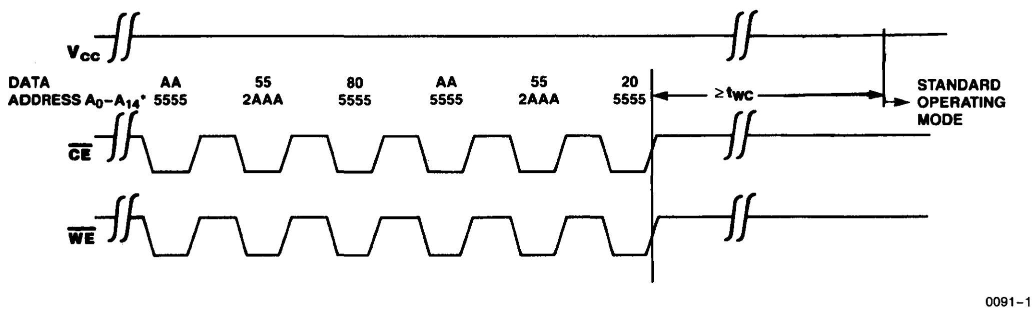


0091-15

Regardless of whether the device has previously been protected or not, once the software data protected algorithm is used and data has been written, the device will automatically disable further writes unless another command is issued to cancel it. If no further commands are issued the device will be write protected during power-down and after any subsequent power-up.

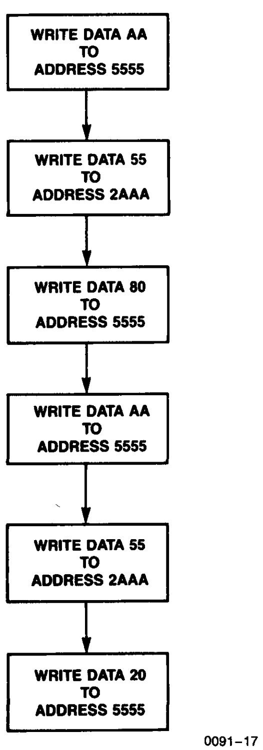
RESETTING SOFTWARE DATA PROTECTION

Figure 5a: Reset Software Data Protection Timing Sequence



*A_{15} & A_{16} select one of four devices on the module.

Figure 5b: Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an E^2PROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the device will be in standard operating mode.

SYSTEM CONSIDERATIONS

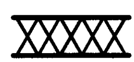
Because the XM28C010 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the XM28C010 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 μF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 μF electrolytic bulk capacitor be placed between V_{CC} and GND for every two modules employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Ordering Information

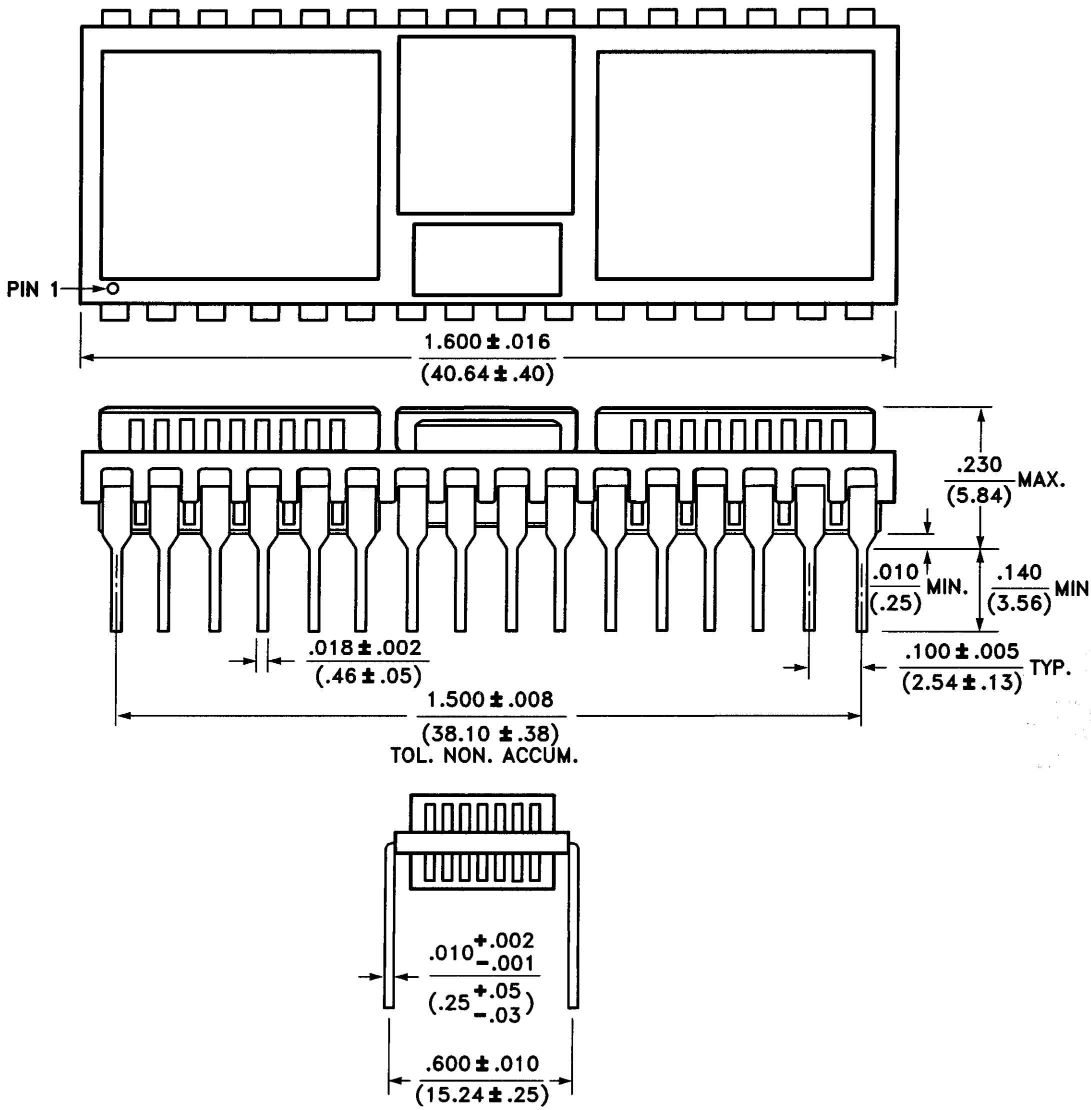
1MEGABIT E^2 MODULES

Device Order Number	Organization	Temp. Range	Access Time	Process Technology	Processing Level
XM28C010-25	131072 x 8	†	250 ns	CMOS	Standard
XM28C010I-25	131072 x 8	I	250 ns	CMOS	Standard
XM28C010M-25	131072 x 8	M	250 ns	CMOS	High Rel
XM28C010	131072 x 8	†	300 ns	CMOS	Standard
XM28C010I	131072 x 8	I	300 ns	CMOS	Standard
XM28C010M	131072 x 8	M	300 ns	CMOS	High Rel

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

Packaging Information

32-PIN DUAL-IN-LINE PACKAGE
CERAMIC LEADLESS CHIP CARRIERS
ON SIDE BRAZED CERAMIC SUBSTRATE



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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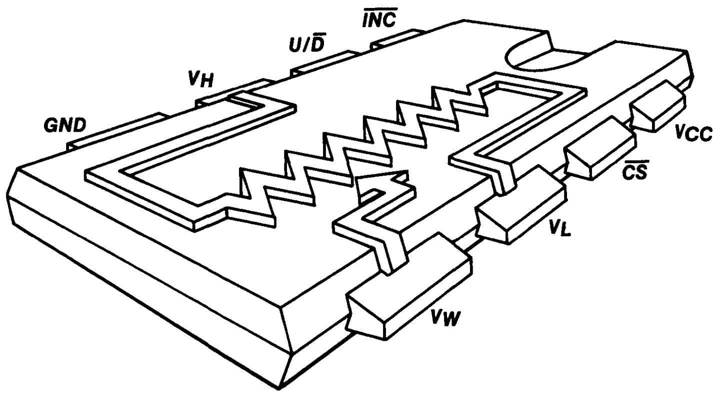
3/88 Stock No. 200-169

THE X9MME



0110-3

Part Number	Maximum Resistance
X9102	1 KΩ
X9103	10 KΩ
X9503	50 KΩ
X9104	100 KΩ

Please use this Xicor Data Book Supplement in conjunction with the Xicor 1988 Data Book, Stock No. 100-080, which contains additional product line information, product reliability reports and application notes.

PRELIMINARY INFORMATION

Commercial	**X9MME**
Industrial	**X9MMEI**

E²POT™ Digitally Controlled Potentiometer

FEATURES

- **Solid State Reliability**
- **Single Chip MOS Implementation**
- **Three Wire TTL Control**
- **Operates From Standard 5V Supply**
- **99 Resistive Elements**
  - **—Temperature Compensated**
  - **—±20% End to End Resistance Range**
- **100 Wiper Tap Points**
  - **—Wiper Position Digitally Controlled**
  - **—Wiper Position Stored in Nonvolatile Memory Then Automatically Recalled on Power-Up**
- **100 Year Wiper Position Retention**
- **8 Pin Mini-DIP Package**
- **14 Pin SOIC Package**

DESCRIPTION

The Xicor X9MME is a solid state nonvolatile potentiometer and is ideal for digitally controlled resistance trimming.

The X9MME is a resistor array composed of 99 resistive elements. Between each element and at either end are tap points accessible to the wiper element. The position of the wiper element on the array is controlled by the $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ inputs. The position of the wiper can be stored in nonvolatile memory and is recalled upon a subsequent power-up.

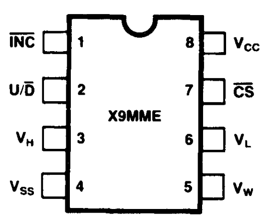
The resolution of the X9MME is equal to the maximum resistance value divided by 99. As an example; for the X9503 (50 KΩ) each tap point represents 505Ω.

Xicor E² products are designed and tested for applications requiring extended endurance. Refer to Xicor reliability reports for further endurance information.

E²POT™ is a trademark of Xicor, Inc.

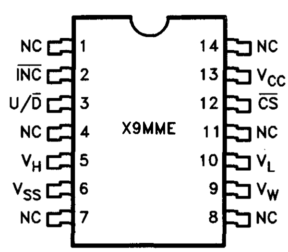
PIN CONFIGURATIONS

PLASTIC



0039–1

SOIC



0039–12

PIN NAMES

V_H	High Terminal of Pot
V_W	Wiper Terminal of Pot
V_L	Low Terminal of Pot
V_{SS}	Ground
V_{CC}	System Power
U/$\overline{D}$	Up/Down Control
$\overline{INC}$	Wiper Movement Control
$\overline{CS}$	Chip Select for Wiper Movement/Storage
NC	No Connect

ANALOG CHARACTERISTICS

Electrical Characteristics

End to End Resistance Tolerance .... ±20%
Power Rating at 25°C
X9102 .... 16 mW
X9103, X9503 and X9104 .... 10 mW
Wiper Current .... ±1 mA Max.
Typical Wiper Resistance .... 40Ω at 1 mA
Typical Noise
X9102 .... < −120 dB/√Hz Ref: 1V
X9103, X9503 and X9104 .... < −95 dB/√Hz Ref: 1V

Resolution

Resistance 1%

Linearity

Absolute Linearity(1) .... ±1.0 MI(2)
Relative Linearity(3) .... ±0.2 MI(2)

Temperature Coefficient

−40°C to +85°C
X9102 .... ±600 ppm/°C Typical
X9103, X9503 and X9104 .... ±300 ppm/°C Typical
Ratiometric Temperature Coefficient .... ±20 ppm

Wiper Adjustability

Unlimited Wiper Adjustment
(Volatile Mode While Chip is Selected)
Nonvolatile Storage of Wiper Position
.... 10,000 Cycles Typical

Environmental Characteristics

Temperature Range
Operating X9MME .... 0°C to +70°C
X9MMEI .... −40°C to +85°C
Storage .... −65°C to +150°C

Physical Characteristics

Marking Includes:
Manufacturer's Trademark
Resistance Value or Code
Date Code

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias .... −65°C to +135°C
Storage Temperature .... −65°C to +150°C
Voltage on $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ and V_{CC}
Referenced to Ground .... −1.0V to +7.0V
Voltage on V_H and V_L
Referenced to Ground .... −8.0V to +8.0V
Lead Temperature (Soldering, 10 Seconds) .... +300°C
Wiper Current .... ±1 mA
$\Delta V = |V_H - V_L|$
X9102 .... 4V
X9103, X9503 and X9104 .... 10V

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

X9MME T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X9MMEI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(4)	Max.		
I_{CC}	Supply Current		25	35	mA	
I_{LI}	Input Leakage Current			±10	µA	V_{IN} = 0V to 5.5V, $\overline{INC}$, U/$\overline{D}$, $\overline{CS}$
V_{IH}	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{IL}	Input Low Voltage	−1.0		0.8	V	
R_W	Wiper Resistance		40	100	Ω	±1 mA
V_{VH}(5)	V_H Voltage	−5.0		+5.0	V	
V_{VL}(5)	V_L Voltage	−5.0		+5.0	V	
C_{IN}(6)	$\overline{CS}$, $\overline{INC}$, U/$\overline{D}$, Input Capacitance			10	pF	

Notes: (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.

Absolute Linearity = $(V_{W(n)}(\text{actual}) - V_{W(n)}(\text{expected}))$ = ±1 MI Max.

(2) 1 MI = $R_{TOT}/99$ or $\frac{V_H - V_L}{99}$ = Minimum Increment.

(3) Relative Linearity is utilized to determine the actual change in voltage between successive tap position when used as a potentiometer. It is a measure of the error in step size.

Relative Linearity = $V_{W(n+1)} - [V_{W(n)} + MI]$ = ±0.2 MI Max.

Typical values of Linearity are shown in Figures 3, 6, 9 and 12.

(4) Typical values are for T_A = 25°C and nominal supply voltage.

(5) ΔV for X9102 = $|V_H - V_L| \leq 4V$. ΔV for X9103, X9503 and X9104 = $|V_H - V_L| \leq 10V$.

(6) This parameter is periodically sampled and not 100% tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input	1.5V

MODE SELECTION

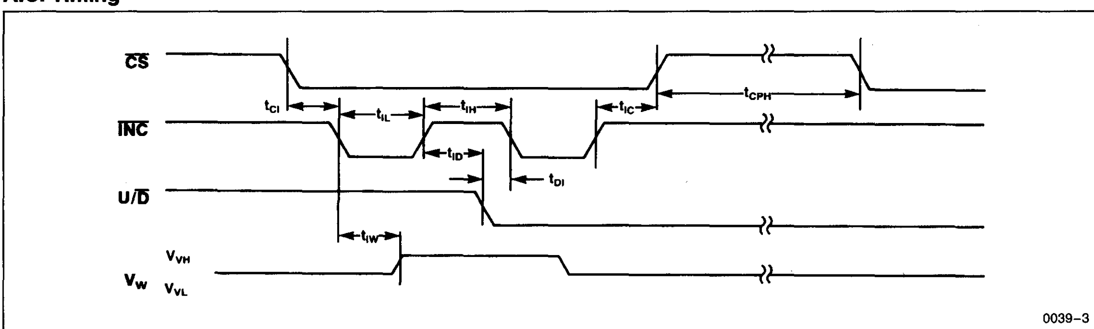
$\overline{CS}$	$\overline{INC}$	U/$\overline{D}$	Mode
L	↘	H	Wiper Up
L	↘	L	Wiper Down
↗	H	X	Store Wiper Position

A.C. CHARACTERISTICS

X9MME T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.
X9MMEI T_A = −40°C to +85°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Units
		Min.	Typ.(7)	Max.	
t_{CI}	$\overline{CS}$ to $\overline{INC}$ Setup	100			ns
t_{ID}	$\overline{INC}$ High to U/$\overline{D}$ Change	100			ns
t_{DI}	U/$\overline{D}$ to $\overline{INC}$ Setup	2.9			µs
t_{IL}	$\overline{INC}$ Low Period	1			µs
t_{IH}	$\overline{INC}$ High Period	3			µs
t_{IC}	$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	1			µs
t_{CPH}	$\overline{CS}$ Deselect Time	20			ms
t_{IW}	$\overline{INC}$ to V_W Change		100	500	µs

A.C. Timing



Note: (7) Typical values are for T_A = 25°C and nominal supply voltage.

PIN DESCRIPTIONS

V_H

The high terminal of the X9MME is capable of handling an input voltage from −5V to +5V.

V_L

The low terminal input is limited from −5V to +5V.

V_W

The wiper terminal series resistance is typically less than 40Ω. The value of the wiper is controlled by the use of U/$\overline{\text{D}}$ and $\overline{\text{INC}}$.

Up/Down (U/$\overline{\text{D}}$)

The U/$\overline{\text{D}}$ input controls the direction of the wiper movement and the value of the nonvolatile counter.

Increment ($\overline{\text{INC}}$)

The $\overline{\text{INC}}$ input is negative-edge triggered. Toggling $\overline{\text{INC}}$ will move the wiper and either increment or decrement the counter in the direction indicated by the logic level on the U/$\overline{\text{D}}$ input.

Chip Select ($\overline{\text{CS}}$)

The device is selected when the $\overline{\text{CS}}$ input is LOW. The current counter value is stored in nonvolatile memory when $\overline{\text{CS}}$ is returned HIGH with $\overline{\text{INC}}$ HIGH.

DEVICE OPERATION

The $\overline{\text{INC}}$, U/$\overline{\text{D}}$ and $\overline{\text{CS}}$ inputs control the movement of the wiper along the resistor array. HIGH to LOW transitions on $\overline{\text{INC}}$, with $\overline{\text{CS}}$ LOW, increment (U/$\overline{\text{D}}$ = HIGH) or decrement (U/$\overline{\text{D}}$ = LOW) an internal counter. The output of the counter is decoded to position the wiper. When $\overline{\text{CS}}$ is brought HIGH the counter value is automatically stored in the nonvolatile memory. Upon power-up the nonvolatile memory contents are restored to the counter.

With the wiper at position 99, additional increments (U/$\overline{\text{D}}$ = HIGH) will not move the wiper. With the wiper at position 0, additional decrements (U/$\overline{\text{D}}$ = LOW) will not move the wiper.

The state of U/$\overline{\text{D}}$ may be changed while $\overline{\text{CS}}$ remains LOW, allowing a gross then fine adjustment during system calibration.

If V_{CC} is removed while $\overline{\text{CS}}$ is LOW the contents of the nonvolatile memory may be lost.

The end to end resistance of the array will fluctuate once V_{CC} is removed.

APPLICATIONS

The combination of a digital interface and nonvolatile memory in a silicon based trimmer pot provides many application opportunities that could not be addressed by either mechanical potentiometers or digital to analog circuits. The X9MME addresses and solves many issues that are of concern to designers of a wide range of equipment.

Consider the possibilities:

Automated assembly line calibration versus mechanical tweaking of potentiometers.

Protection against drift due to vibration or contamination.

Eliminate precise alignment of PWB mounted potentiometers with case access holes.

Eliminate unsightly access holes on otherwise aesthetically pleasing enclosures.

Product enhancements such as keyboard adjustment of volume or brightness control.

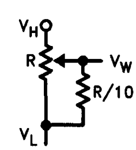
Front panel microprocessor controlled calibration of test instruments.

Remote location calibration via radio, modem or LAN link.

Calibration of hard to reach instruments in aircraft or other confined spaces.

APPLICATION CIRCUITS

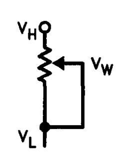
Application Circuit #1



0039-4

Approximating audio trim with external resistor.

Application Circuit #2

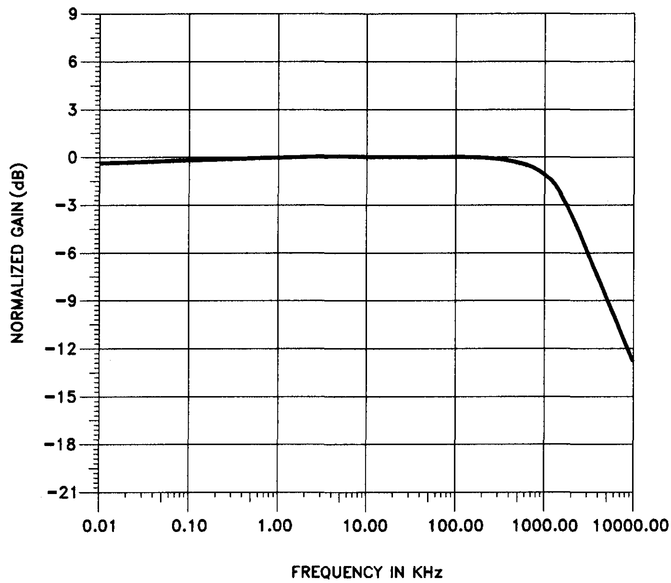


0039-5

Utilizing the X9MME as a variable resistor.

Note: Maximum Wiper Current = 1 mA.

Figure 1: Typical Frequency Response for X9102

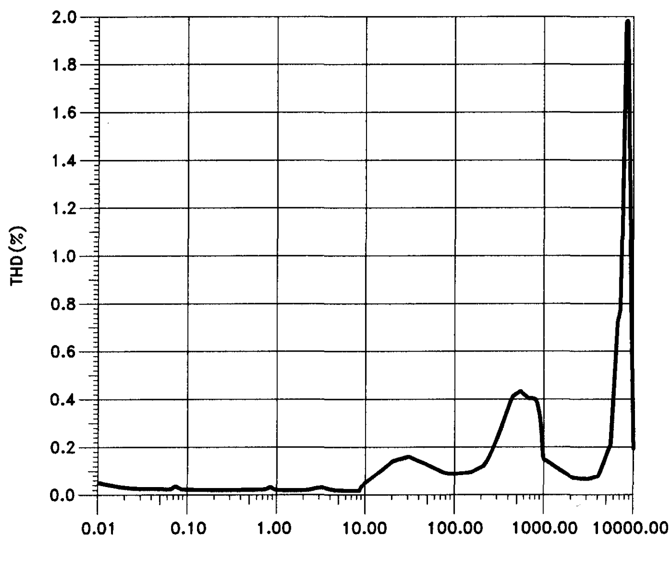


TEST CONDITIONS

V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1

0039-13

Figure 2: Typical Total Harmonic Distortion for X9102

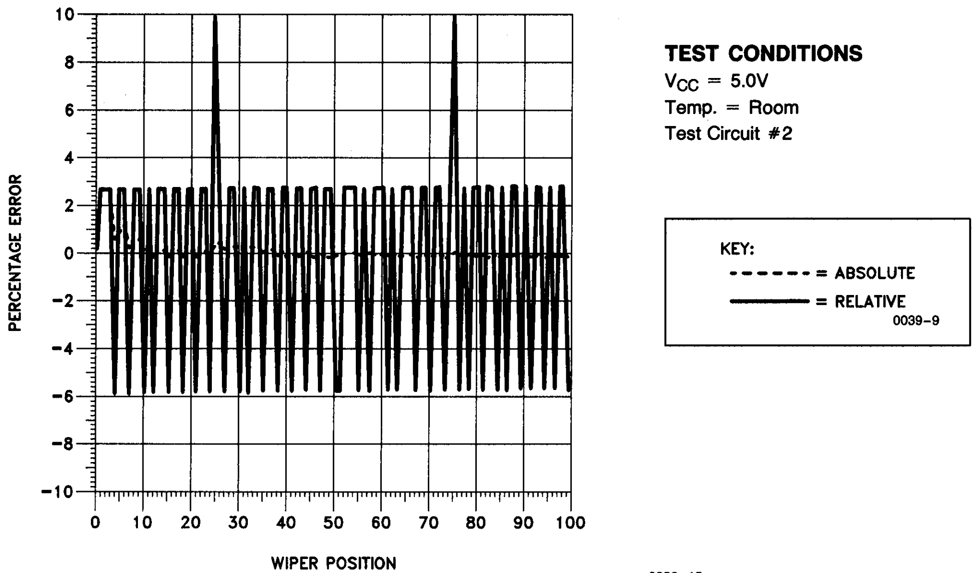


TEST CONDITIONS

V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 2V RMS
Test Circuit #1

0039-14

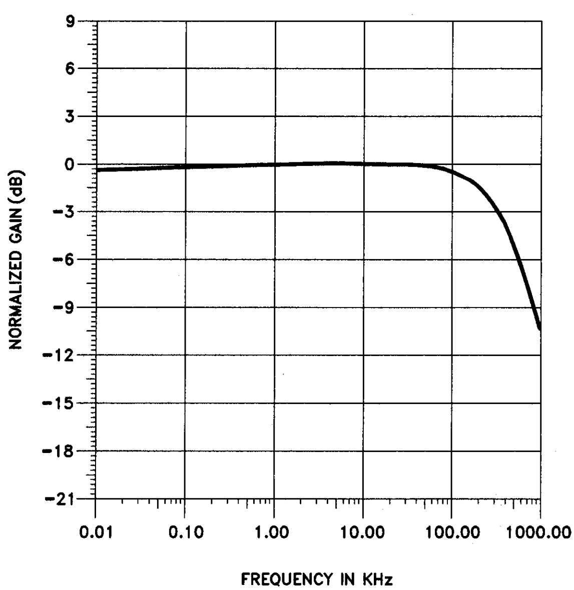
Figure 3: Typical Linearity for X9102



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Test Circuit #2

0039-15

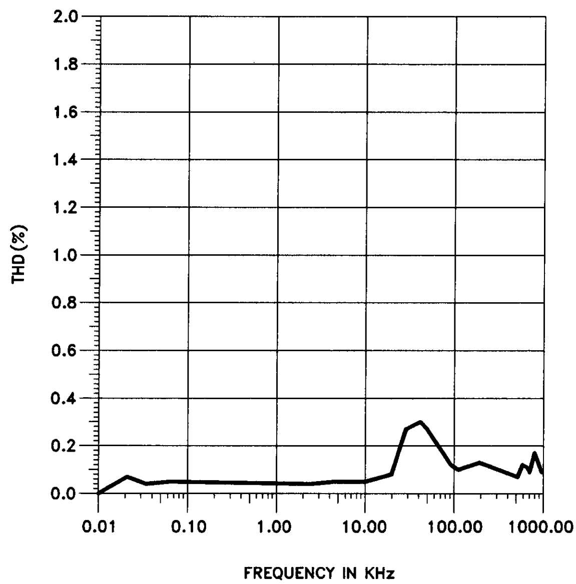
Figure 4: Typical Frequency Response for X9103



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1

0039-6

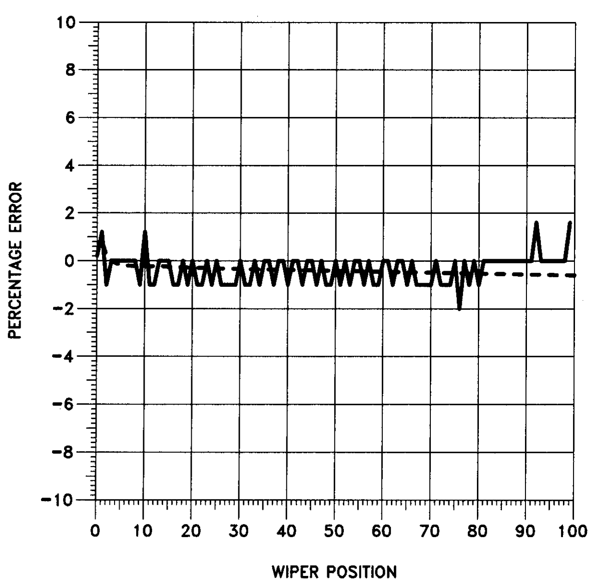
Figure 5: Typical Total Harmonic Distortion for X9103



TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 2V RMS
Test Circuit #1

0039-7

Figure 6: Typical Linearity for X9103

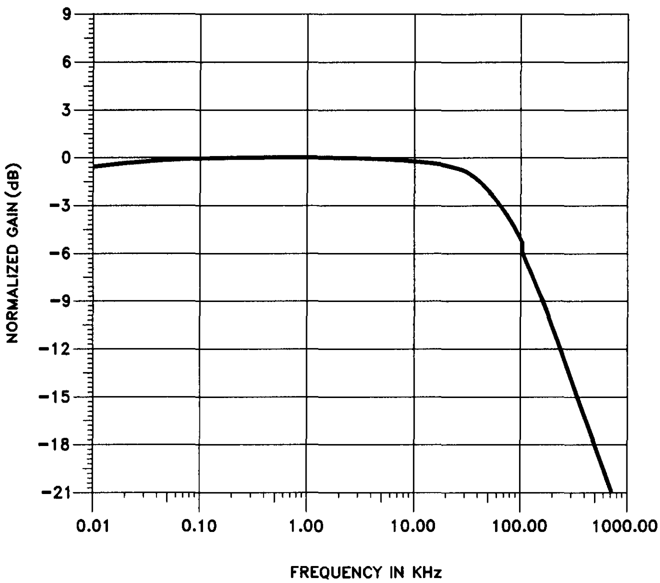


TEST CONDITIONS
V_{CC} = 5.0V
Temp. = Room
Test Circuit #2

KEY:
------ = ABSOLUTE
—— = RELATIVE
0039-9

0039-8

Figure 7: Typical Frequency Response for X9503

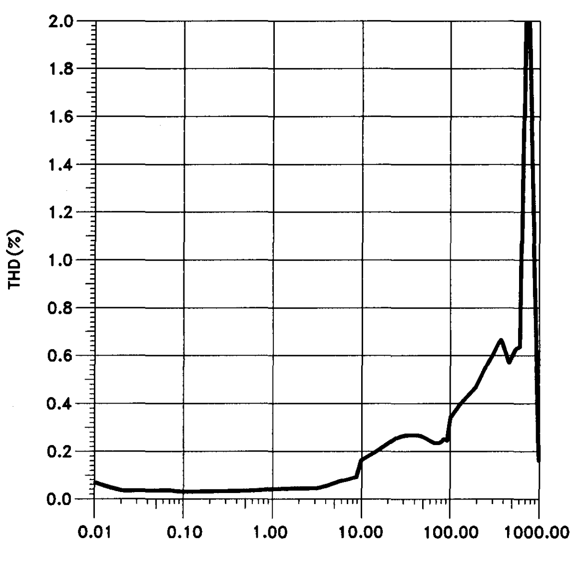


TEST CONDITIONS

V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 0.5V RMS
Normalized (0 dB @ 1 KHz)
Test Circuit #1

0039–16

Figure 8: Typical Total Harmonic Distortion for X9503

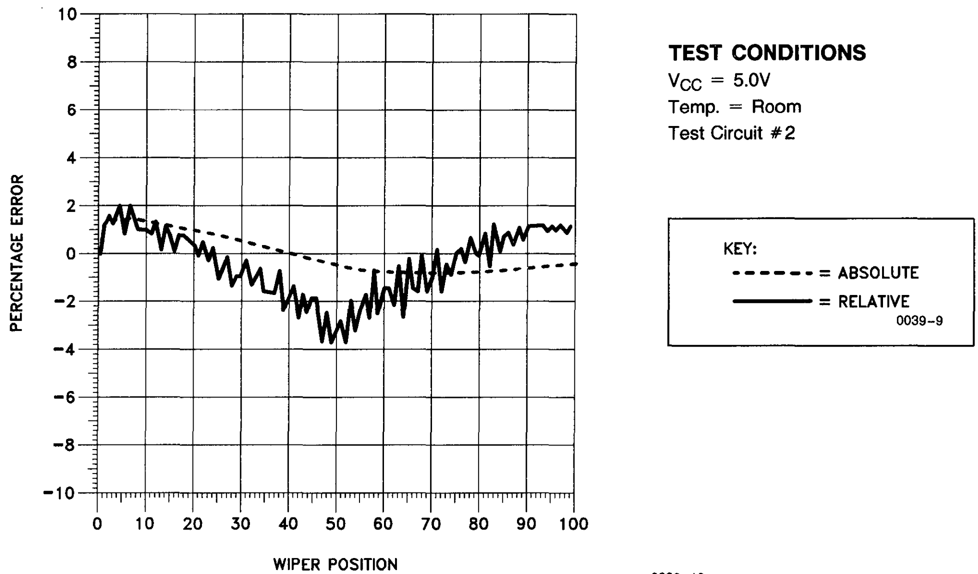


TEST CONDITIONS

V_{CC} = 5.0V
Temp. = Room
Wiper @ Tap 50
V_H = 2V RMS
Test Circuit #1

0039–17

Figure 9: Typical Linearity for X9503



TEST CONDITIONS

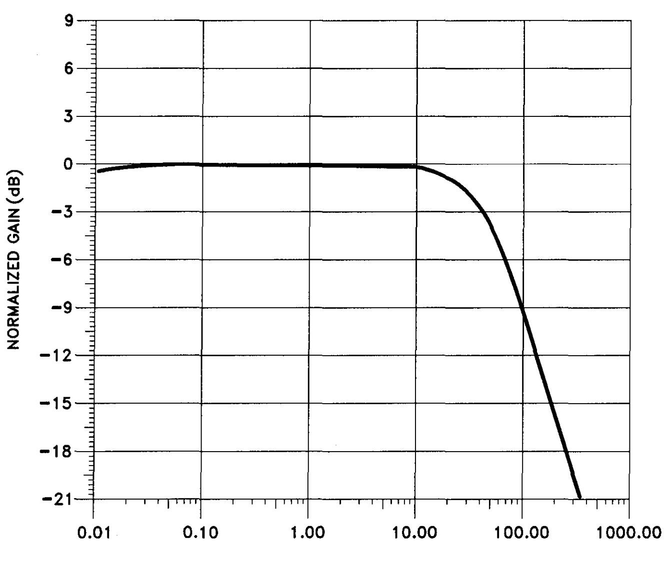
V_{CC} = 5.0V

Temp. = Room

Test Circuit #2

0039-18

Figure 10: Typical Frequency Response for X9104



TEST CONDITIONS

V_{CC} = 5.0V

Temp. = Room

Wiper @ Tap 50

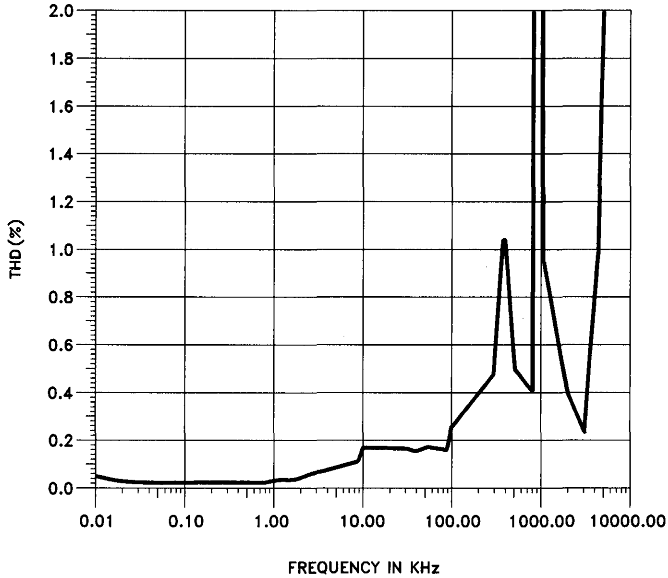
V_H = 0.5V RMS

Normalized (0 dB @ 1 KHz)

Test Circuit #1

0039-19

Figure 11: Typical Total Harmonic Distortion for X9104



TEST CONDITIONS

V_{CC} = 5.0V

Temp. = Room

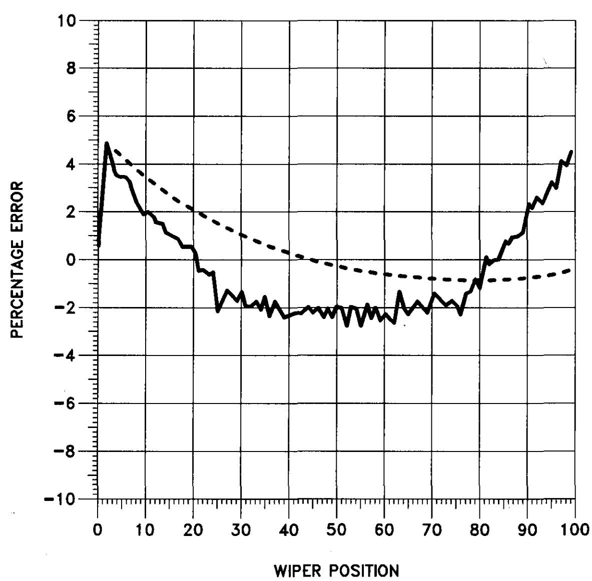
Wiper @ Tap 50

V_H = 2V RMS

Test Circuit #1

0039-20

Figure 12: Typical Linearity for X9104



TEST CONDITIONS

V_{CC} = 5.0V

Temp. = Room

Test Circuit #2

KEY:

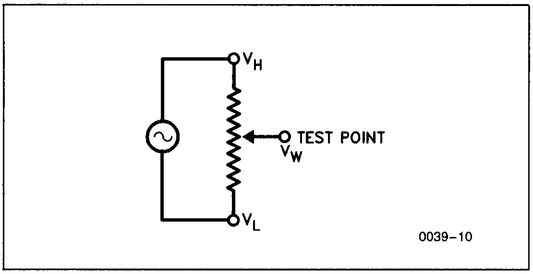
- - - - - - = ABSOLUTE

——— = RELATIVE

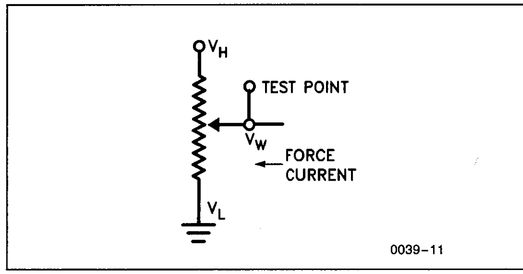
0039-9

0039-21

Test Circuit #1



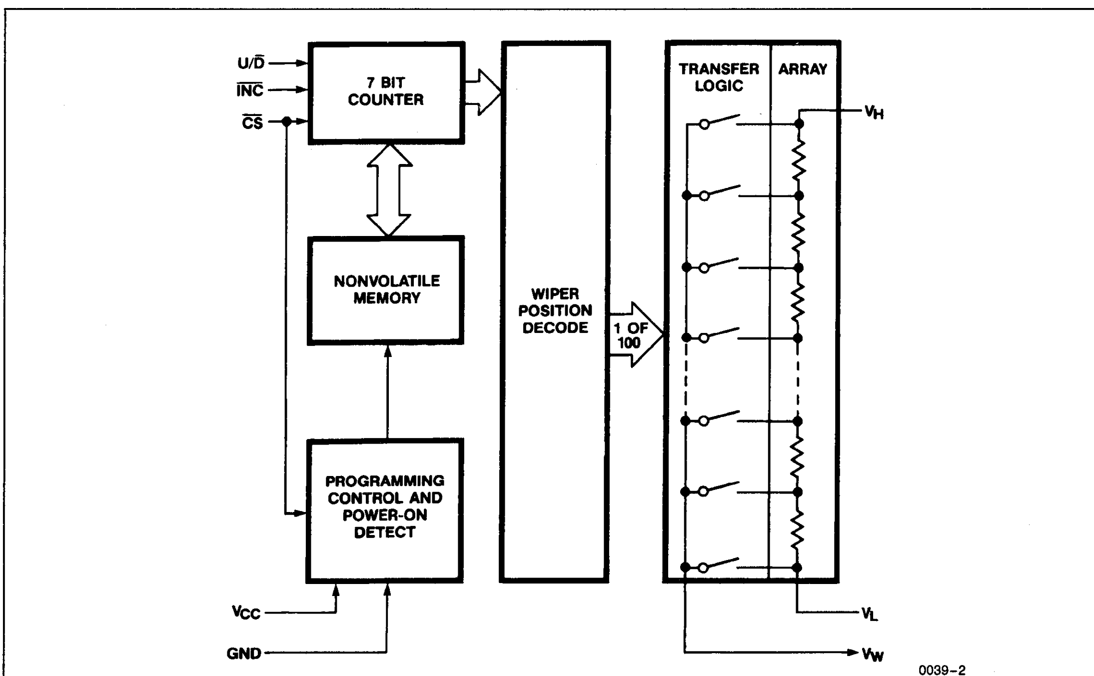
Test Circuit #2



Standard Parts

Minimum Resistance	Wiper Increments	Maximum Resistance	Part Number
40Ω	10.1Ω	1 KΩ	X9102
40Ω	101Ω	10 KΩ	X9103
40Ω	505Ω	50 KΩ	X9503
40Ω	1010Ω	100 KΩ	X9104

FUNCTIONAL DIAGRAM



ORDERING INFORMATION

E2POTENTIOMETERs

Device Order Number	Maximum Resistance	Package										Temp. Range	Processing Level
		S	P	D	C	F1	F2	K	J	E	G		
X9102S	1 KΩ	•										†	Standard
X9103S	10 KΩ	•										†	Standard
X9503S	50 KΩ	•										†	Standard
X9104S	100 KΩ	•										†	Standard
X9102SI	1 KΩ	•										I	Standard
X9103SI	10 KΩ	•										I	Standard
X9503SI	50 KΩ	•										I	Standard
X9104SI	100 KΩ	•										I	Standard
X9102P	1 KΩ		•									†	Standard
X9103P	10 KΩ		•									†	Standard
X9503P	50 KΩ		•									†	Standard
X9104P	100 KΩ		•									†	Standard
X9102PI	1 KΩ		•									I	Standard
X9103PI	10 KΩ		•									I	Standard
X9503PI	50 KΩ		•									I	Standard
X9104PI	100 KΩ		•									I	Standard

Key:

† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 14-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
D = 8-Lead Cerdip
C = Side Braze
F1 = Ceramic Flat Pack for X2864A, X2864B, X2864H and X28C64
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

ORDERING INFORMATION

E²POTENTIOMETERs (Continued)

Device Order Number	Maximum Resistance	Package										Temp. Range	Processing Level
		S	P	D	C	F1	F2	K	J	E	G		
X9102D	1 KΩ			•								†	Standard
X9103D	10 KΩ			•								†	Standard
X9503D	50 KΩ			•								†	Standard
X9104D	100 KΩ			•								†	Standard
X9102DI	1 KΩ			•								I	Standard
X9103DI	10 KΩ			•								I	Standard
X9503DI	50 KΩ			•								I	Standard
X9104DI	100 KΩ			•								I	Standard

Key:
† = Blank = Commercial = 0°C to +70°C
I = Industrial = −40°C to +85°C
M = Military = −55°C to +125°C

S = 14-Lead Plastic Small Outline Gull Wing
P = 8-Lead Plastic DIP
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C = Side Braze
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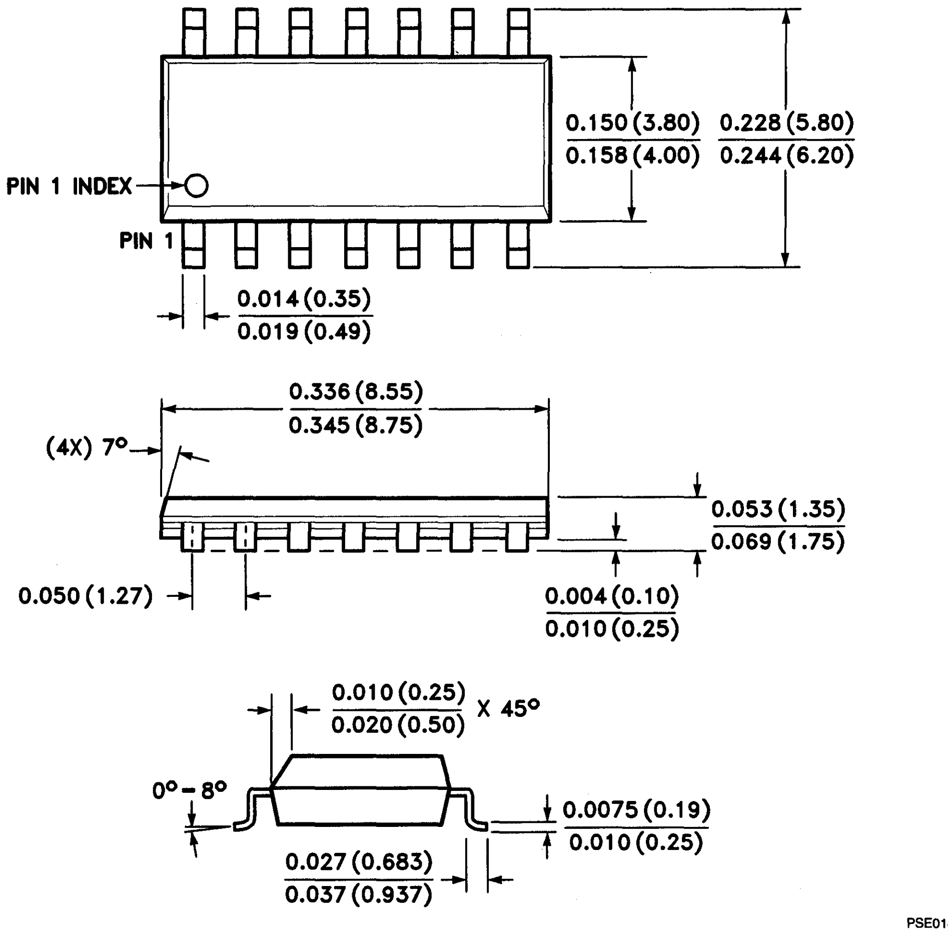
F2 = Ceramic Flat Pack for X28C256 and X28C256B
K = Ceramic Pin Grid Array
J = J-Hook Plastic Leaded Chip Carrier
E = Ceramic Leadless Chip Carrier (Solder Seal)
G = Ceramic Leadless Chip Carrier (Glass Frit Seal)

PACKAGING INFORMATION

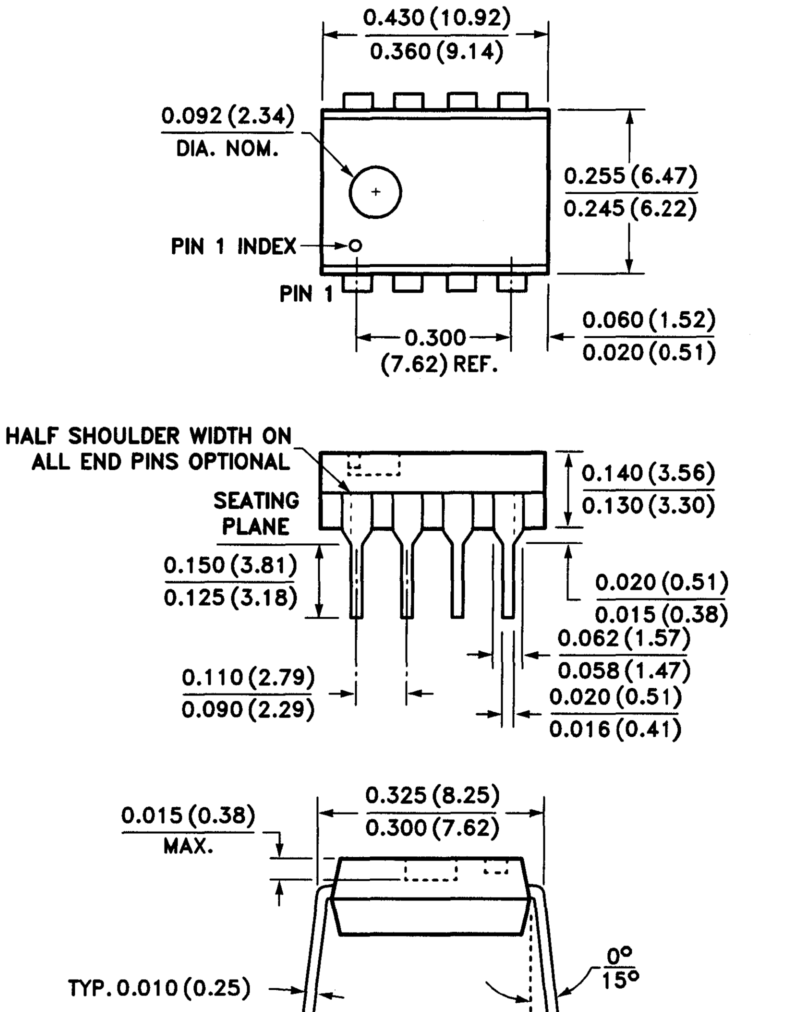
14-LEAD PLASTIC SMALL OUTLINE GULL WING PACKAGE TYPE S



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

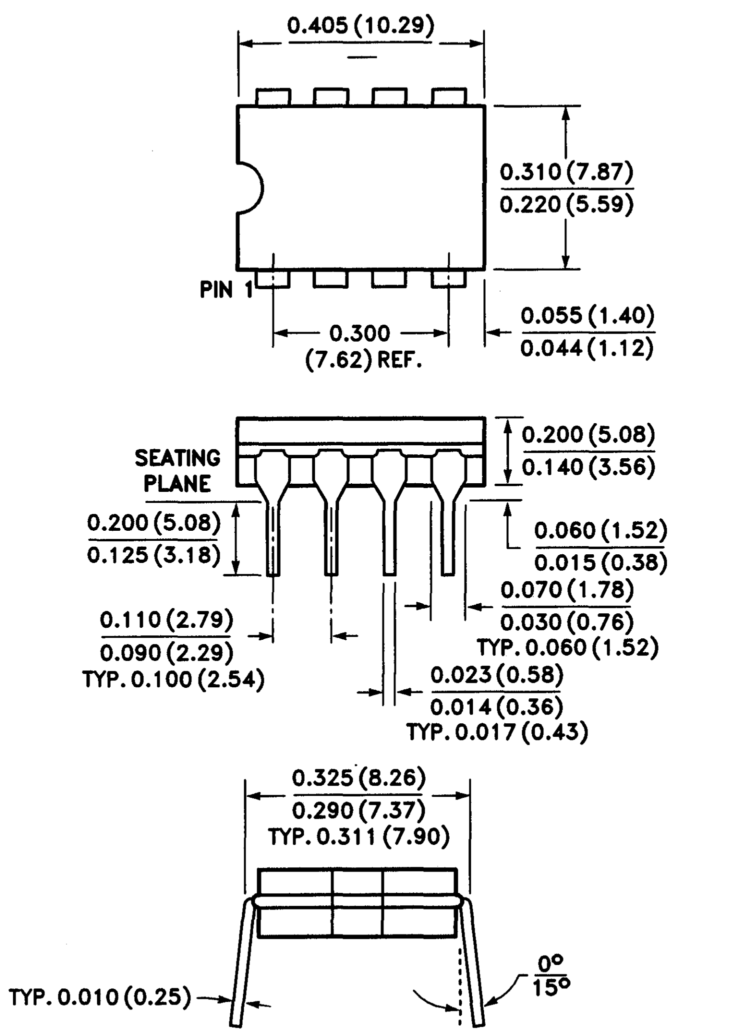
8-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

8-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

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5. 256K E^2PROMs
6. 1M E^2PROMs
7. Serial E^2PROMs
8. E^2 Potentiometers

D. My Primary Technology Interest is:
1. NMOS
2. CMOS

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