XCELL

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XILINX®
The Programmable Logic Company℠

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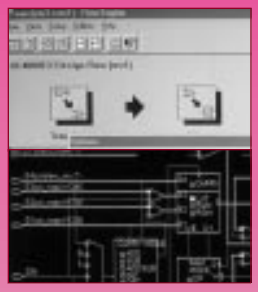

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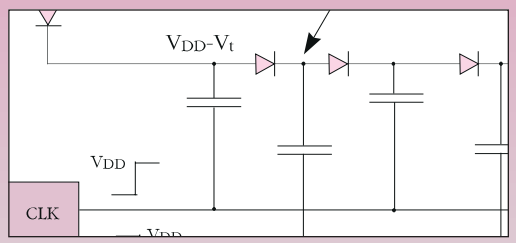

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FPGAs, Power and Packages

By BRADLY FAWCETT ◆ Editor

As programmable logic suppliers accelerate their use of advanced deep-submicron process technologies, the performance and density capabilities of FPGAs continues to increase dramatically. System designers can now take advantage of programmable logic devices exceeding 100,000 logic gates and supporting system clock rates approaching 100 MHz.

In general, the CMOS technology used to produce FPGAs is a low-power technology. However, given the density and performance levels of leading-edge FPGA devices, power consumption issues can no longer be ignored during high-density FPGA design. In the past, the availability of architectural resources (such as logic blocks and interconnect routing) and the inherent delays of the various logic elements and routing switches were almost always the limiting factors in determining device utilization levels and system speed. Now, power consumption can be the limiting factor. In other words, a designer might not be able to use all the available logic blocks and run the design as fast as possible without risking reliability problems due to overheating the devices.

As well as affecting the maximum possible density and performance, the power characteristics of FPGA devices directly affect packaging (and, therefore, component costs) and device reliability. Junction temperatures within a device are a function of power consumption and the thermal resistance of the package (θ_{JA}). Overall device reliability decreases exponentially as junction temperature increases. In general, junction temperatures need to stay below 125° C for plastic packages and 150° C for ceramic packages.

Several factors determine the power consumption within an FPGA, including the supply voltage, the architecture of the device, system performance (switching frequency), and device utilization (the number of interconnects and logic elements used and the percentage of these that switch at a given time).

As with most CMOS devices, the operating power consumption of an FPGA is almost exclusively dynamic, and varies with the square of the supply voltage. Thus, using FPGAs based on the 3.3V power standard, as opposed to the 5V standard, greatly reduces device power requirements. For a given circuit and clock speed, just reducing the supply voltage from 5V to 3.3V decreases operating power consumption by 56%. (The move to lower supply voltages is largely driven by the fact that the ever-shrinking transistors within a submicron device cannot withstand high voltages; however, even if this was not the case, the industry would be driven to lower supply voltages due to device power dissipation issues alone.)

Low-Power Architectures

The architectures of Xilinx high-density FPGAs — specifically the XC4000E, XC4000EX, and XC4000XL families — have been designed to minimize power consumption. For example, the patented segmented-interconnect architecture minimizes the lengths of metal traces, thereby preventing unnecessary interconnect capacitance from slowing device operation and causing extra power dissipation. The extra buffering that was added to the long lines and quad lines when adapting the original XC4000 architecture to create the new XC4000EX and XC4000XL series devices further minimizes interconnect capacitances. As a result, these devices can be fully utilized and operated with high system clock frequencies, even when using plastic packages.

> *"...power consumption issues can no longer be ignored during high-density FPGA design."*

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GUEST EDITORIAL

HardWire ASIC + LogiCORE = Reduced Time-to-Volume

by RICK PADOVANI ◆ Marketing Director

Increasingly, systems designers in fast-moving, competitive markets cannot tolerate the long development cycles required for the successful implementation of conventional mask-programmed gate arrays. Successful gate array development time can range from six to 18 months or more, and often requires additional time for re-spins. In addition, the demand for rapid product enhancements has dramatically shrunk typical product life cycles. As a result, leading-edge designers must look for innovative development approaches to reduce risk, while gaining a time-to-market advantage.

As the performance and density of Field-Programmable Gate Arrays (FPGAs) increase, many traditional mask-programmed gate array designers are taking advantage of the fast development time and flexibility of FPGA technology. Submicron CMOS process technology and architectural enhancements are making die sizes more cost-effective; and price points for FPGAs are declining rapidly. In fact, in the lower complexity ranges, FPGAs have been approaching price parity with mask-programmed gate arrays as die sizes in both technologies have become pad-limited.

In the higher complexity ranges, where the cost difference between FPGAs and masked-programmed devices is still significant, the HardWire ASIC model, pioneered by Xilinx in 1989, has gained broad market acceptance. Xilinx FPGA-to-HardWire ASIC migration provides total life-cycle management of high-volume applications by combining the advantages of FPGA development time and flexibility with the cost-efficiency of masked-programmed devices. The technology enables designers to achieve the fastest possible time-to-market and the lowest overall production cost. While the FPGA is in use, late design changes or system upgrades can be accommodated. Production ramps up much more rapidly than it would with a conventional ASIC approach. When the design is final, the systems vendor has the option of requesting a HardWire conversion from Xilinx, leaving no gap between development completion and high-volume production. This represents a major competitive advantage for our users.

> *"Xilinx FPGA-to-HardWire migration provides total life-cycle management of high-volume applications."*

The efficiency of using pre-verified LogiCORE modules for high-complexity FPGA design really brings the HardWire advantage into focus. The system hardware and software verification process can proceed much more rapidly using FPGAs. Concurrent hardware and software engineering is facilitated by virtue of the FPGA, as opposed to the longer development and prototyping time of conventional mask-programmed gate arrays. Hardware corrections, as well as software corrections, can be implemented at the same time, so designers have the option to make optimal corrections, rather than using software patches to work around hardware bugs. The HardWire conversion process preserves the total functionality and performance of the design, including the LogiCORE module.

For example, user-specific PCI designs can be implemented very cost-effectively for high-volume production using the Xilinx PCI LogiCORE module and HardWire ASIC devices. A fully-compliant PCI core and up to 10,000 gates or more of user-specific logic can be implemented for less than $20 in volume quantities.

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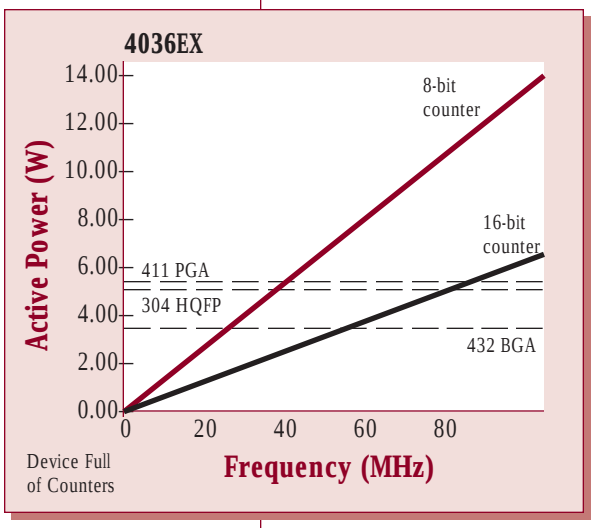
For example, the figure shows the power consumption of an XC4036EX device (a 5V FPGA) when the entire device is filled with 8-bit and 16-bit counters. (In an 8-bit counter, 25% of the flip-flops toggle each clock period, while in a 16-bit counter 12.5% of the flip-flops toggle; thus, the power consumption with the 8-bit counter benchmark is about twice that of the 16-bit counter.) The horizontal lines on the graph correspond to the maximum power dissipation recommended for various package types (without heat sinks or fans). Thus, it is safe to operate the full XC4036EX device in a low-cost HQFP plastic package at speeds up to 70 MHz without requiring heat sinks or fans.

In contrast, some other vendors' high-density FPGAs have interconnect structures based on a multiplicity of long metal traces. The high-speed switching of these long traces, with their inherently larger capacitance, results in considerably higher power consumption. As a result, while the data sheets offered by these vendors boast of high densities and performance rates, these rates can only be reliably sustained by using expensive ceramic packages (and even then often require the further expense of heat sinks and fans). For example, one competitor's device, with a density roughly equivalent to the XC4036EX, was benchmarked using the same methodology as described above. Due to power dissipation limits, it can be run only at speeds below 18 MHz in plastic packages, and at speeds below 35 MHz in ceramic packages; at any higher performance level, heat sinks and fans will be needed.



Thus, users of high-density FPGAs must be careful not to fall victim to "bait and switch" tactics, wherein a designer is enticed to select a high-density FPGA based on performance claims and the price of plastic-packaged parts, only to later discover that power consumption considerations dictate the use of a more expensive package and/or slower speed operation.

Estimating/Minimizing Consumption

Unfortunately, power consumption within an FPGA is design-dependent and can be difficult to calculate prior to implementing the design. Charts provided in Xilinx data sheets provide dynamic power consumption values for typical design elements (for example, the power consumption of one XC4000E CLB flip-flop driving its neighbor and nine lines of interconnect is 0.2mW per million transitions per second); these can be used to derive useful power consumption estimates, but require the designer to estimate the average percentage of nodes in the FPGA design that switch with each clock transition. In any event, it is highly-recommended that users of high-density FPGAs always measure device power consumption (usually by measuring the total I_{CC} current at actual system frequency) upon completion of a design to insure that the right package and cooling methods are being employed.

Some design techniques can be employed to minimize FPGA power consumption *(see* XCell 19, *page 34)*. As mentioned earlier, users of high-density, high-performance devices should strongly consider the use of FPGAs based on the 3.3V supply voltage standard, such as the XC4000XL series. Most power dissipation is produced by external capacitive loads on output buffers, so those loads should be minimized and outputs should be switched as infrequently as possible. Similarly, use clock enables to switch off inactive portions of circuits, preventing internal nodes from toggling unnecessarily. Use the place and route tools to maximize the performance of the design, even if the resulting performance far exceeds requirements. Circuits that are able to run faster can do so because of lower routing capacitance; consequently, they dissipate less power at any given clock frequency. ◆

FPGAs Bring Needed Flexibility to Telecomm Testers

The rapid proliferation of new services and standards complicates the already challenging task of meeting the high-performance needs of the telecommunications equipment market. At **ICT Electronics** (Barcelona, Spain), a leading manufacturer of telecommunications test equipment, the flexibility of SRAM-based FPGA technology plays a key role in meeting that challenge.

Since 1989, designers at ICT Electronics have exploited the reconfigurable nature of Xilinx FPGA technology to create high-performance, cost-effective test equipment. Their systems take advantage of the reconfigurable nature of Xilinx FPGAs in two ways:

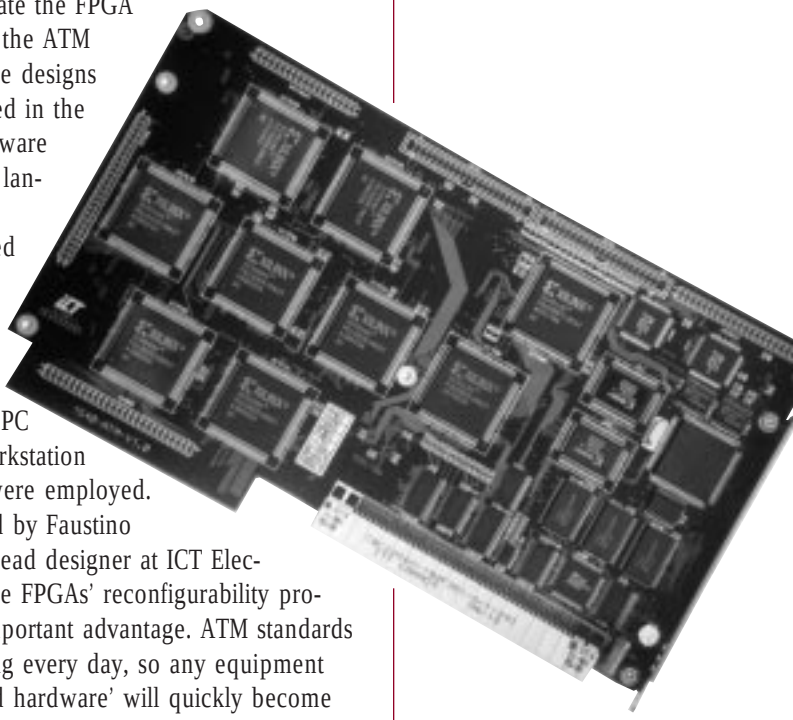
- to implement multiple operations with the minimal amount of logic.
- to enable field upgrades.

Often, multiple potential bitstreams are available for a particular FPGA device, so the FPGA is configured (and reconfigured) dependent on the user's selection of a particular command or operating mode. When the various industry organizations issue new standards or recommendations, systems can be upgraded in the field by supplying new FPGA configuration bitstreams. Typically, the FPGAs are configured using the asynchronous peripheral mode, with the configuration bitstreams stored on a hard or floppy disk within the system. Equipment can be easily updated by sending out new configuration bitstreams via floppy disk or over the Internet.

For example, the new Flexacom Analyzer/Generator for broadband ISDN digital transmission systems contains a mix of about one hundred XC3000 and XC4000 series FPGA devices in a typical system configuration. This powerful instrument allows users to work separately or simultaneously with both the Synchronous and Plesiochronous Digital Hierarchies (SDH and PDH). Optional modules support Jitter and Wander analysis and generation.

The Flexacom system's FPGA-based asynchronous transfer mode (ATM) module, pictured here, is a typical example of the use of FPGAs in the various system modules. This module can act as both an ATM cell simulator and an ATM cell monitor. The majority of the logic on the board is implemented in 11 different FPGAs, ranging from the XC4013E to the XC3042A device. The FPGAs implement a wide variety of logic functions, including finite state machines, counters, register files, multiplexers/demultiplexers, and decoders. The XC4000E architecture's on-chip memory capability is used to efficiently implement large register files and look-up tables used to identify virtual channels. The FPGA's dedicated arithmetic carry logic is key to implementing the large counters needed to simultaneously monitor up to 16 communication channels. Utilization of these devices ranges from about 65% to over 90%, and system clock speeds range from 512 KHz to 40 MHz.

Data I/O's Synario design software was used to create the FPGA designs for the ATM module. The designs were entered in the VHDL hardware description language, and implemented using the Xilinx XACT-Foundry tools. Both PC and HP workstation platforms were employed.



As noted by Faustino Cuadrado, lead designer at ICT Electronics, "The FPGAs' reconfigurability provides an important advantage. ATM standards are changing every day, so any equipment with 'closed hardware' will quickly become obsolete. Flexacom ATM can be updated easily, via floppy or remote control, helping make Flexacom the best solution for B-ISDN networks." ◆

More Enhancements to WebLINX

Several significant enhancements have been added to WebLINX, the Xilinx World Wide Web site (www.xilinx.com). In addition to posting hundreds of new documents, improvements have focused on making technical information easier to find. For example, new capabilities have been added to the *Smart*Search and Agent tools, and "Expert Journals" are now part of the Technical Answers section. A further addition is the "LogiCORE Lounge", designed to provide the latest and most-accurate information on our LogiCORE products, including the new PCI CORE Generator *(see page 14)*.

> *"SmartSearch improvements are intended to produce significantly better results from your search queries."*

*Smart*Search & Agents

WebLINX *Smart*Search lets you quickly find information on the Xilinx site and any of the over 50 PLD-industry sites that we index. Agents automatically notify you of changes to those sites by sending you an e-mail notification whenever new documents are added that match your designated areas of interest. Several recent improvements have increased the utility of these tools.

In an effort to help you find information faster, two new *Smart*Search pages have been added. These pages include checkboxes to help narrow your search to specific topics, such as PCI or DSP, and specific sites (or even areas within those sites!).

Other *Smart*Search improvements are intended to produce significantly better results from your search queries. Searches now include matching to document "keywords." For instance, searching for "install" might find hundreds of documents, while there might only be a dozen documents that really directly address the topic of Install. The use of keywords will ensure that those dozen documents are presented at the top of the search results list. Keywords will be added to the documents on our site over the next few months, so you should see continued improvements in your search results. Searches also can be narrowed to just document titles by clicking an option on the search page. This will significantly reduce the number of matches, and result in locating documents that more closely match your interests.

While over 2,000 visitors to WebLINX have signed up for Agents, only a small percentage have actually created them. To make *Smart*Search Agents even easier to use, Agents for several popular topics now can be created simply by checking a box on the agent sign-up page or the Popular Agents page. These Agents range from alerting you to changes on the Xilinx "What's New" page to keeping you abreast on PCI developments throughout the industry. Furthermore, the format of the e-mail notification has been updated to provide additional information about new documents that have been posted, as well as document revisions. Thus, at a quick glance, you can decide if the information is important to you, without spending a lot of time "surfing" the sites. Remember, you are in complete control, and can start and stop the e-mail activity at any time simply by deleting or creating agents.

Expert Journals

"Expert Journal" pages are a useful recent addition to the "Technical Answers" area of WebLINX. Here, Xilinx Technical Support experts provide the latest installation and "getting started" tips, top solutions, design techniques and software patches for Xilinx Foundation software and Xilinx Alliance interfaces to Cadence, Mentor Graphics, Synopsys and Viewlogic tools.

LogiCORE VIP Lounges

The LogiCORE VIP Lounge is a password-protected area; registered LogiCORE product owners have access. This site is designed to provide the most current information and design files for our LogiCORE products, including product enhancements, design tips, known issues, new releases of design files and much more. If you are a current LogiCORE PCI user, register today.

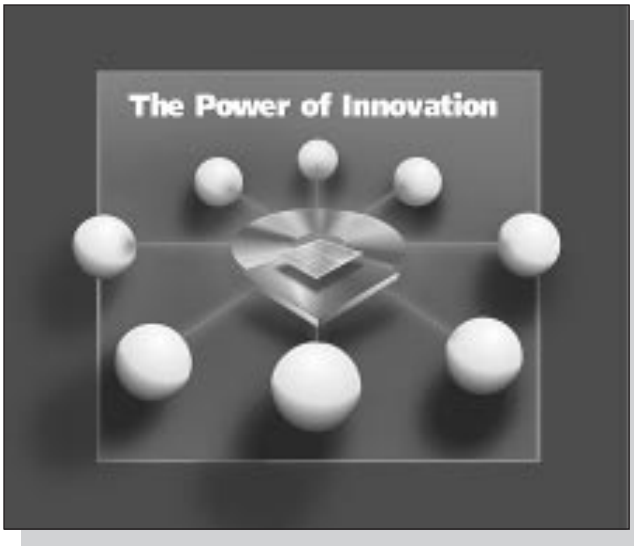
The LogiCORE VIP Lounge also is the site of the first web-based tool for fast FPGA core design, the CORE Generator for PCI *(see page 14)*. The CORE Generator for PCI will be merged with the CORE Generator for DSP later this year to form a generic framework for providing and using both LogiCORE and AllianceCORE products. ◆

"Power of Innovation" Seminars Reach WorldWide

By the time this publication reaches you, the Xilinx seminar series *The Power of Innovation* will be drawing to a close. The seminar discusses programmable logic solutions for digital systems, with an emphasis on new products such as the XC4000XL FPGA family, the XC9500 CPLD family, and the LogiCORE drop-in modules.

During May and June, these one-day seminars are being held at more than 40 locations throughout North America, Europe, and Japan. Seminars are scheduled for several locations in Southeast Asia in late July.

To those of you who attended one of these seminars, our sincere thanks for your time. If you were unable to attend, but would like to receive a copy of the seminar materials or information about new Xilinx products, or to register for an upcoming seminar in Southeast Asia, please contact your local Xilinx sales representative. ◆



TECHNICAL TRAINING UPDATE

XACT*step* Version M1 Training to Debut

With the impending release of the XACT*step* version M1 software *(see page 12)*, the Customer Education Group has focused on the development of new technical education courses that coincide with this new software release.

The three-day XACT*step* version M1 course is organized in a modular manner. Basically, the course is divided into two sections: **low-density design** (one day) and **high-density design** (two days). This method of organization allows the course to focus on the use of all the Xilinx tools, including the specific tools associated with the XACT*step* version M1 software release.

The XACT*step* version M1 course will be complemented by one- and two-day "bolt-on" courses focused on the CAE interfaces supported and sold through Xilinx (e.g., Foundation, FPGA Express, etc.). These bolt-on courses provide the user with an overall better knowledge of how to use the Xilinx tools and devices in conjunction with the various third-party design entry, synthesis and verification tools.

In the same time frame as the XACT*step* version M1 release, a one-day M1 update course will be offered to the Xilinx user community, providing further information and specifics on the new release.

Dates and schedules for both the XACT*step* M1 and XACT*step* M1 Update courses will be disseminated in this publication and on WebLINX (www.xilinx.com).

The 1997 Educational Services Brochure will be updated at mid-year with all of the latest course descriptions and schedule information. This updated brochure will be available at all Xilinx sales offices in July. ◆

New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	NUMBER
Corporate		
Product Overview Brochure	Features & Benefits	#0010130-06
Xilinx Packaging Guide	Technical Data	#100120
AppLINX CD	Technical Data	#106425-04
Software		
Software Quick Reference Card	Technical Data	#0010104-07

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

Design Automation Conference (DAC)
June 9-13
Anaheim, CA

Embedded Computing
June 17
Santa Clara, CA

Embedded Computing
June 19
Irvine, CA

Japan PLD Conference
June 25-27
Tokyo, Japan

Electronic Design Automation and Test Conference (EDA&T)
Aug. 18-19
Shanghai, China

Electronic Design Automation and Test Conference (EDA&T)
Aug, 21-22
Seoul, Korea

Electronic Design Automation and Test Conference (EDA&T)
Aug. 25-26
Hsinchu,Taiwan

International Workshop on Field Programmable Logic and Applications (FPL '97)
Sept. 1-3
London, UK

DSP World Expo
Sept. 15-17
San Diego, CA

PC Card '97
Sept. 17-18
Santa Clara, CA

DSP France
Sept. 17-19
Paris, France

EuroDAC
Sept. 22-26
Dusseldorf, Germany

DSP Germany
Sept. 30-Oct. 1
Munich, Germany

Xilinx Inc. stock is traded on the NASDAQ exchange under symbol XLNX.

FINANCIAL RESULTS

Another Record Fiscal Year

As in every year since Xilinx was founded, the company again established a new annual revenue record for fiscal year 1997 (April 1996 to March 1997). Fiscal 1997 sales revenue totaled $568.1 million, up from $560.8 million in fiscal 1996. Revenues for the fourth quarter (January-March 1997) reached a record $151.8 million, an 11.9% increase from the previous quarter.

While revenue growth for the fourth quarter was strong across all product lines, sales of the flagship XC4000 series FPGA products were particularly robust, increasing by more than 24% sequentially. Development system sales reached an all-time high of about 1,700 new software seats. Earlier this year, Xilinx announced the shipment of its 35,000th software design system.

Looking forward, Chief Executive Officer Wim Roelandts commented, "Fiscal 1998 is shaping up to be an exciting year for Xilinx. Our density and performance leadership coupled with our leading edge software solidifies our position as the premier PLD company. As we continue to engineer more comprehensive solutions for our customers, and aggressively converge on the sweet spot of the gate array market, I am confident in our opportunities for future growth." ◆

Industry's Fastest 5V FPGAs in Production

XC4000E-1 Series Offers 25% Performance Gain

As introduced in *XCell 24*, XC4000E devices featuring the new -1 speed grade are now shipping in production volumes. Based on an optimized 0.5µ three-layer-metal process, the new -1 devices support typical system clock speeds in the 80 MHz range — 20-25% higher performance than the XC4000E-2 FPGAs, previously the fastest devices in the XC4000E family.

Extensive performance analysis using comparable 5V FPGAs from other vendors has confirmed that the XC4000E-1 device is 5-20% faster in end-user applications. The analysis included three different types of benchmarks:

- the actual implementations of representative macro- and core-level functions from key application areas.
- the actual implementations of representative "real-world" system designs of various density and performance levels obtained from systems manufacturers.
- the guaranteed system I/O speed, as measured by adding the clock-to-out and global-clock-setup specifications obtained in product data sheets.

When compared with its closest competitor, the XC4000E-1 FPGA delivers 20% better performance, on average, for the scaled functions, and 12% better performance for the real-world designs. System I/O speed for the XC4000E-1 device is 5% better than the fastest competitive device.

The XC4000E-1 device expands the power of the LogiCORE PCI design solution. This performance improvement extends full PCI compliance to 20,000-gate densities and increases overall design flexibility for PCI interface designs. Other emerging applications such as networking, multimedia, and high-speed telecommunications can benefit from this FPGA family's increased performance capabilities.

The performance leadership of the XC4000 series complements its highly-integrated feature set, including on-chip three-state buffers, dedicated arithmetic carry logic, multiple global clock networks, and on-chip Select-RAM memory. The XC4000E family spans from 237 to 2,432 logic cells (approximately 2,000 to 25,000 logic gates), and is available in a variety of packages.

The Xilinx Foundation and Alliance Series development systems support the new XC4000E-1 speed grade. The Foundation series is a fully-integrated, ready-to-use, Windows-based solution, including support for industry-standard HDLs, synthesis, schematic entry, simulation, and the XACT*step* implementation tools. The Alliance series allows the use of the XACT*step* tools with the industry's most-popular third-party EDA tools; this series of development system products provides open-system benefits with support for industry-standard design methodologies and interfaces, including EDIF, VHDL (VITAL 95), and Verilog/SDF.

Please contact your local Xilinx sales representative for current pricing information. ◆

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XC95288 CPLD Enters Production

Five XC9500 CPLD family members are now in production, including the new 288-macrocell XC95288 device (**Table 1**). The XC9500 family continues to lead the industry with user-proven in-system-programmability and pin-locking capabilities, support for a full suite of IEEE 1149.1 (JTAG) instructions, mixed 3.3V/5V system compatibility, pin-to-pin speeds as fast as 5 ns, and a large variety of density/package combinations. Full footprint-compatibility whenever multiple densities share a common package type facilitates design migrations between family members (**Table 2**). ◆

Table 1: *XC9500 Device Family*

	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288
Macrocells	36	72	108	144	216	288
Usable Gates	800	1,600	2,400	3,200	4,800	6,400
Registers	36	72	108	144	216	288
t_{PD} (ns)	5	7.5	7.5	7.5	10	15
t_{SU} (ns)	4.5	5.5	5.5	5.5	6.5	8.0
t_{CO} (ns)	4.5	5.5	5.5	5.5	6.5	8.0
f_{CNT} (MHz)	100	125	125	125	111	95
f_{SYSTEM} (MHz)	100	83	83	83	67	56
Availability	NOW	NOW	NOW	4Q97	NOW	NOW

Notes: f_{CNT} = *Operating frequency for 16-bit counters*
f_{SYSTEM} = *Internal operating frequency for general purpose system designs spanning multiple FBs.*

Table 2: *Available Packages and Device I/O Pins (not including dedicated JTAG pins)*

	XC9536	XC9572	XC95108	XC95144	XC95216	XC95288
44-Pin VQFP	34					
44-Pin PLCC	34	34				
84-Pin PLCC		69	69			
100-Pin TQFP		72	81			
100-Pin PQFP		72	81	81		
160-Pin PQFP			108	133	133	
208-Pin HQFP					166	168
352-Pin BGA					166	192

GUEST EDITORIAL

Continued from page 3

Customer re-verification of the complex design is not required with the HardWire solution; Xilinx guarantees equivalent functionality and performance. In some cases (depending on the design), speed improvements can be obtained in the HardWire device by eliminating delays associated with programmable interconnects in the FPGA, and because of the shorter routing delays associated with the smaller HardWire die size.

> *"HardWire ASIC devices are available to support each Xilinx FPGA family."*

About HardWire

HardWire technology allows users to "design once" with FPGAs. It uses FPGA-specific gate arrays and libraries, along with a specialized conversion methodology patented by Xilinx that uses the circuit and physical layout data of the routed and verified FPGA netlist to generate a similar physical mapping of equivalent logic cells in the mask-programmed HardWire device. This ensures circuit equivalence and timing compatibility. Risks associated with design re-targeting and verification are virtually eliminated.

HardWire conversion is superior to conventional gate array conversions because the HardWire conversion is based on "design mapping" at the physical level, rather than common gate array "re-targeting" that begins at the design capture level. Gate array re-targeting actually requires a second complete design cycle after the FPGA development; re-targeting techniques alter the netlist and require significant re-verification effort (and high risk!). The HardWire process reduces the user's expense of time and engineering resources, while offering guaranteed "socket compatibility" and very low risk. Furthermore, the production test program for the HardWire device is developed by Xilinx using a scan path insertion and ATPG (automatic test pattern generation) methodology. No vectors are required from the user and >95% fault coverage of the user's logic is provided.

HardWire ASIC devices are available to support each Xilinx FPGA family. ◆

XC4085XL FPGA Sets New Density Standard

This May, Xilinx began shipping sample quantities of the new XC4085XL FPGA. The XC4085XL device is now the largest member of the XC4000XL family (a position previously held by the XC4062XL device). It is the industry's leading high-performance 3.3V FPGA solution, with 7,448 logic cells (3,136 CLBs) and 448 I/O blocks.

With the introduction of the high-density XC4062XL and XC4085XL devices, FPGA technology can now effectively address new, high-density markets such as telecommunications, data processing and industrial applications. As FPGA costs decline and densities increase, all gate array designers who are currently using devices with up to 100,000 gates can now secure the convenience and time-to-market benefits of FPGA technology.

The development system software for the XC4000XL family, available now, is included as part of the new XACT*step* version M1 design environment. The additional routing available in the XC4000XL family architecture, along with improved routing algorithms in the new M1 release, result in dramatically-reduced software compilation times for these high-density FPGAs.

The XC4085XL device is available in 560-pin super ball grid array and 559-pin pin grid array packages. Please contact your local Xilinx sales representative for the latest price and availability information. ◆

Extends Density of XC4000XL FPGA Family by 40%

XC6264 Added to XC6200 Family of RPUs

Xilinx recently announced the addition of the 64,000-gate XC6264 device to the XC6200 family of reconfigurable processing units (RPUs). The XC6264 and XC6216 RPUs are the only programmable logic devices that have been optimized for reconfigurable logic applications such as real-time adaptive filtering and algorithm acceleration.

While FPGAs traditionally have been used to implement individual logic designs, RPUs are intended to support multiple designs in a single piece of silicon — either by "swapping out" unnecessary pieces of a design to save silicon space or by changing logic on-the-fly to increase performance.

Innovative XC6200 features such as fast partial reconfiguration, a built-in microprocessor interface and an open bitstream format make RPUs the component of choice for system designers exploring or using dynamic hardware designs.

Xilinx Delivers Next Generation

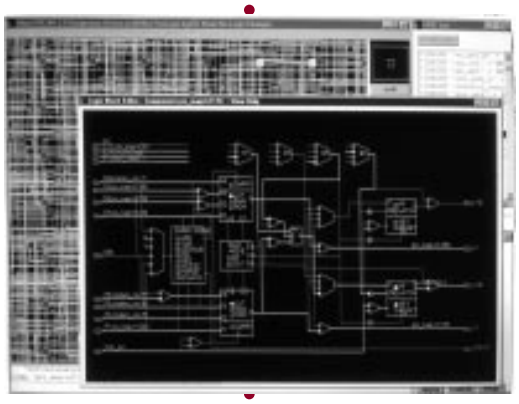
New XACT*step* M1 Places and Routes 1,000 Gates per Minute With a 25% Performance Increase

The new XACT*step* version M1 software technology enables users at every design level to increase design performance, leverage standards-based, high-level design methodologies, and quickly receive future software updates and device support for Xilinx FPGA and CPLD solutions.

Version M1.2 is available now for the PC and for UNIX workstations, including Sparc-compatible SunOS 4.1.3 and Solaris 2.3, HP-UX and IBM RS6000 platforms. Current users of XACT*step* 5.2/6.0 with an active support or maintenance plan will receive a free upgrade to XACT*step* M1.3; upgrades are scheduled to start shipping in mid-summer.

XACT*step* version M1, developed as a result of the Xilinx merger with NeoCAD, Inc., dramatically improves design performance using advanced placement and routing algorithms, powerful "auto-interactive" tools that deliver the choice between a push-button or manually-directed design methodology, and support for industry standard-based design flows, including EDIF, SDF, VHDL (Vital) and Verilog support.

Version M1's design flow engine.



Schematic editing an XC4028 device in a BG352 package.

XACT*step* M1 User Benefits

Maximum Design Performance — Version M1 software enables maximum design performance by providing a unique combination of advanced algorithms and interactive tools. Designer productivity is greatly enhanced with its simple, push-button flows and optional auto-interactive tools. User testing has shown that version M1 software used with XC4000XL devices results in 70 percent shorter run times, up to a 25 percent performance improvement, and the ability to place and route devices with up to 100 percent utilization with a push-button flow.

Modular Software System — The modular architecture of the M1 system will allow Xilinx to rapidly deliver incremental technologies, new features, device support and new versions of its leading software product families. New feature sets can now be released independently; as a result, users can quickly complete designs without having to re-learn new tools as enhancements are made. The investment Xilinx has made in the M1 technology ensures that the continuous delivery of innovative device architectures and improved software solutions can be accomplished more rapidly and more predictably.

Methodology Flexibility — High-level design methodologies are becoming the methodology choice for the design of complex programmable logic. Version M1 software delivers programmable logic specific high-level flows. The flows provide high-quality, high-performance and optimized results, and allow fast, flexible design changes and iterations, matching the way that engineers design. Xilinx users often employ a mixture of graphical and language-based design entry methods to design their products. The flow is built to complement existing schematic-based design methods while providing an easy-to-learn environment for Hardware Description Language (HDL) based design. Xilinx recognizes that design environments are variant and, therefore, has created a flexible system, enabling the user to choose the best methodology for the environment and design challenge.

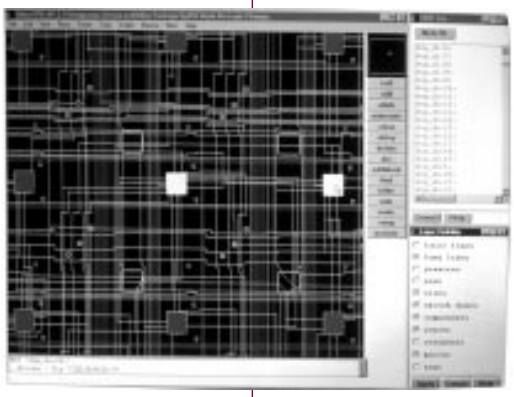
XILINX®

Software Platform

Product Configurations

XACT*step* version M1 software delivers all these benefits through both the XACT*step* Foundation and Alliance Series software solutions. The Foundation Series features a complete, front-to-back design solution based on industry-standard HDLs and push-button design flows. The Alliance Series focuses on open systems integration, with the industry's most extensive set of third-party EDA vendor integration.

Please contact your local Xilinx sales representative for the latest availability and pricing information. Inquiries regarding the status of software maintenance contracts should be directed to Xilinx Customer Service. ◆



The logic block editor.

Xilinx Now Shipping Cadence Interface Kit

To provide the best possible support to our users, Xilinx and Cadence Design Systems have mutually agreed to have Xilinx take over development, sales and support of the interface kit for using Cadence design entry and simulation tools with the Xilinx XACT*step* system. Cadence has discontinued sale and support of their Xilinx interface kit; the last Cadence version of that kit is the 97A release.

A new Cadence interface kit is available directly from Xilinx. The currently-released beta version is for the XACT*step* version M1.2 release — full production will start in conjunction with the introduction of M1.3, scheduled for mid-summer. This new interface kit has superior schematic and HDL support for all Xilinx architectures, including the XC4000EX/XL FPGA families. The new release supports EDIF netlist entry, VHDL- and Verilog-based design, as well as both functional and timing simulation. The VITAL libraries in XACT*step* M1 will work with the Cadence Leapfrog VHDL simulator. (The EDIF netlister is available from Cadence on its ftp site.)

Xilinx is committed to fully support our Cadence users, including the timely introduction of schematic and HDL libraries for new component architectures. Resources in engineering and software quality assurance are now dedicated to developing and testing Concept and Verilog libraries; dedicated Cadence experts have been added to the technical support organization. Xilinx has developed detailed documentation on the design flow, including a new guide for users migrating from XACT*step* v5.2.1 to M1.

Cadence will continue to sell and support its HDL synthesis solution for Xilinx components. Synergy synthesis libraries for the XC4000EX family will be available on the Cadence ftp site by early summer. *(For more information on the availability of synthesis libraries, please contact the Cadence support organization in your area.)*

Cadence discontinued sales of Xilinx place and route tools in November 1996 — version 9604 was the last release. All in-warranty owners of these tools can receive the latest XACT*step* package by calling Xilinx customer service.

If you are currently a Cadence Design Systems customer and are using Xilinx tools purchased from Cadence, please fax a copy of the following information to the Xilinx Customer Service group (408-559-0115) — company name, user name, mailing address, telephone number, fax number and e-mail address. ◆

CORE Generator for PCI:

MEMBER PCI LOCAL BUS SPECIAL INTEREST GROUP

The First Web-Based Development Tool for FPGA Design

This spring, Xilinx introduced an innovative, web-based tool that radically simplifies the use of cores for FPGA design. The new, on-line CORE Generator tool facilitates core usage by enabling designers to instantly access, customize, and download core designs using WebLINX (www.xilinx.com).

It features an intuitive graphical interface, thereby shortening the learning curve for logic designers. Initially designed to support users of the LogiCORE PCI module, the CORE Generator will be extended to support other Xilinx LogiCORE and third-party AllianceCORE products later this year.

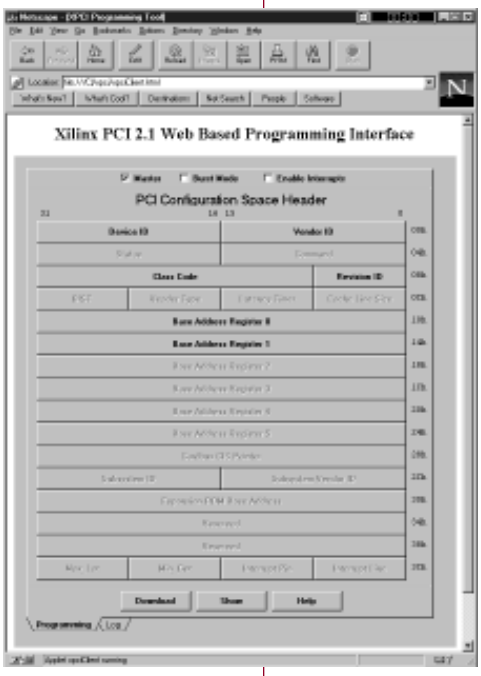


Figure 1: *CORE Generator tool for PCI, main menu*

The CORE Generator tool for PCI introduces a new methodology for acquiring and using cores with FPGAs. Since the tool executes on the web, LogiCORE PCI users always have access to the latest versions of the cores (as well as the latest product information). "Customized" cores are created by the CORE Generator based on user-defined parameters, allowing designers to easily create and download their unique versions of the core netlist, regardless of the design tools and methodologies used for design entry and simulation.

Using CORE Generator

To create a PCI core netlist using the CORE Generator, designers enter their system's parameters by using the program's graphical user interface (GUI). The GUI mirrors the already-familiar PCI Specification Standard table. For example, the GUI includes a copy of the configuration space header from the PCI specification (**Figure 1**); the user simply enters the parameters by selecting the appropriate values in pre-defined menus. The GUI prevents designers from entering invalid parameters. On-line help is available, as well as application notes describing the complete design flow from core configuration to implementation.

The CORE Generator allows the designer to integrate the LogiCORE PCI module using any chosen tool environment, including VHDL, Verilog, or schematic-based design. (Previously, Viewlogic schematic entry tools were required to modify and customize the design.) The CORE Generator creates all the files needed to integrate the PCI core within the FPGA design and verify the results, including:

1) a netlist with constraints that ensure that timing is met without any manual tuning.
2) a "wrapper" used to instantiate the core in a VHDL, Verilog or schematic-based design.
3) a VHDL/Verilog simulation model for functional verification.

These files are then downloaded over the web to the designer's development platform.

The PCI cores created by the CORE Generator are "firm" cores, with relative placement and timing constraints embedded in the netlist to ensure that the performance of the implemented design meets the requirements of the PCI specification. Thus, PCI timing can be met without any manual tuning of the core, and, as a result, engineering resources can be focused on the system-level design, potentially saving months of development time.

Figure 2 compares typical development times and costs for designing a PCI interface from scratch using a generic, synthesizable core and using a proven LogiCORE PCI core.

Visit the VIP Lounge

To access the tool, use a Java-enabled web browser such as Netscape 3.0 or Microsoft Explorer 3.0 to visit WebLINX (www.xilinx.com). The CORE Generator is part of the new "LogiCORE VIP lounge" site that holds useful

Continued on page 22

The Xilinx DSP CORE Generator

Automated Tool Generates Parameterized DSP Designs Optimized for FPGAs

Today's FPGAs offer an attractive solution for the computationally-intensive functions found in digital signal processing (DSP) applications. By combining the flexibility of a general-purpose, programmable digital signal processor with the speed and density of a custom-hardware implementation, FPGAs can provide increased DSP system performance at a reduced system cost.

However, to achieve this high level of FPGA-based DSP performance, you must craft the DSP algorithm into the architecture of the FPGA. Ironically, many DSP designers, while well-versed in the algorithmic approaches used when programming conventional DSP processors, are not familiar with distributed arithmetic and similar techniques applicable to the highly-parallel structures of FPGA-based solutions.

Rather than learning all the details of these approaches and their implementations, Xilinx users can take advantage of the new DSP CORE Generator. With the DSP CORE Generator, complex parameterized DSP building blocks, optimized for the target FPGA architecture, can be implemented automatically and integrated into Xilinx FPGA designs.

The DSP CORE Generator accepts parameters from a dialog box (Figure 1), and outputs a completed design in the form of a netlist, complete with the appropriate relative-placement constraints. The tool also produces a symbol for the module suitable for use with a schematic editor, VHDL / Verilog instantiation code, and behavioral models. Thus, the CORE Generator meshes smoothly with any combination of HDL and schematic-based design methodologies.

The user interface for the DSP CORE Generator delivers all of the parameterized cores, fixed cores, and the DSP Toolbox Library of parameterized base building blocks, as well as all of the data sheets and documentation, through a hierarchical, expandable tree structure similar to Windows 95 Explorer (Figure 2).

The initial release, currently available, contains support for the generation of serial distributed arithmetic FIR filters, one-dimensional ROM- or RAM-based correlators, Comb filters, integrators, delay elements, and high-speed area-efficient parallel multipliers. Support for Comb and Integrator filter functions facilitate the implementation of Hogenauer filters.

This first release (Alpha 1.0) supports Windows 95 (PC only), and can be obtained through any of the Xilinx DSP FAEs in the US and Europe, or through DSP marketing for Japan and Asia. This release requires Foundation software, since it accesses the Metamor synthesis tools.

The next release, scheduled for mid-summer, will add support for additional functions, including parallel FIR filters, IIR filters (biquads), Fast Fourier Transforms, and FIFO buffers. The summer release also will include support for workstation platforms, and will work with all the XACT*step* packages, eliminating the requirement for Foundation software only. ◆

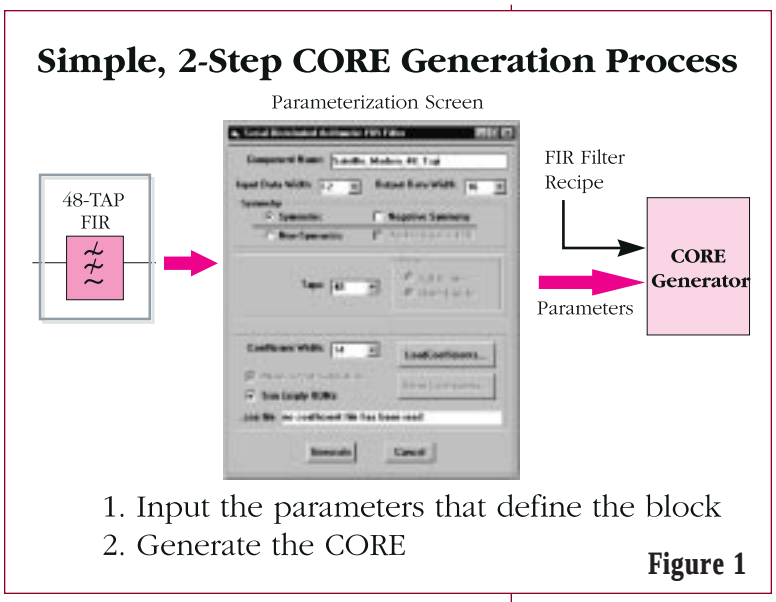
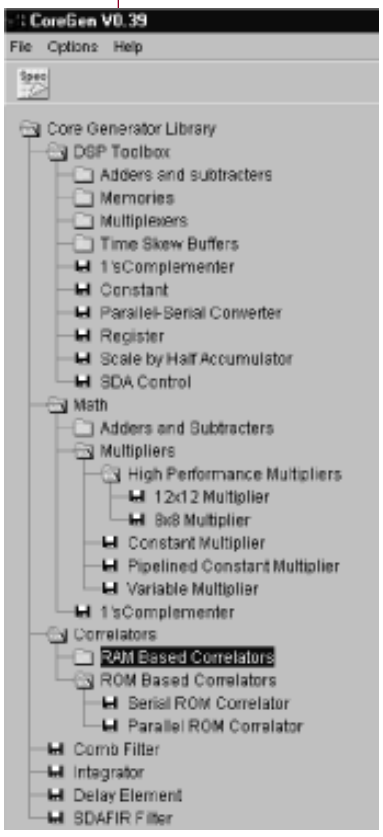


Figure 1

Figure 2: *DSP Design Explorer Tree*



Some Simple XC9500 Prog

In-system-programmable (ISP) CPLDs provide remarkable capabilities for logic design. They permit the development of non-volatile designs without the aid of a device programmer.

In essence, this capability is obtained by incorporating the device programmer within the CPLD device itself. Internal circuitry takes the user-provided pattern and sets the internal storage cells automatically. The circuits involved include a programming state machine and a charge pump.

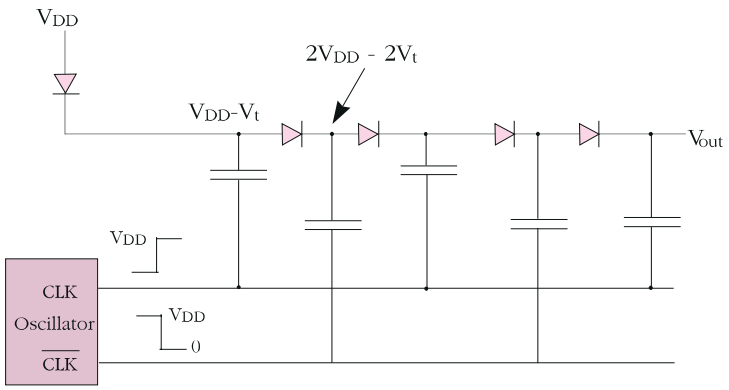


Figure 1: *Simplified Charge Pump Diagram*

For the Xilinx XC9500 family, the state machine is driven by extended JTAG instructions, and uses the same 4-pin set used by the IEEE 1149.1 test commands, thereby minimizing the chip overhead needed to provide ISP capability. Coming from the JTAG controller, the bits are delivered to the ISP controller, which forwards them to the target locations, where the charge pump programs them into the appropriate bit locations.

To take advantage of ISP, *some simple guidelines must be followed*. These guidelines are straightforward — but some users overlook them and become frustrated. As usual, frustration is avoided by planning.

Charge pumps (**Figure 1**) derive their internal "supervoltages" by pumping the external voltage provided at the V_{CC} pin(s). Charge pumps are designed to be robust, but they do require simple care. The various stages of the pump are mathematically related to the V_{CC} level, so it is critical that V_{CC} be within the specified range for the pump to achieve its correct internal voltage. With the XC9500 family, this range is between 4.5 and 5.5 volts.

While this sounds simple, it can be difficult to ensure in practice. V_{CC} voltage can be measured at the card edge or, preferably, right at the CPLD device's pins, but noise on the V_{CC} signal due to the dynamic behavior of the PC board while the system is running can be difficult to detect and quantify. However, as described above, it is critical that the ISP circuitry be provided a stable V_{CC} so the charge pumps can function properly. The usual solution is to attach decoupling capacitors right at the CPLD V_{CC} and V_{CCIO} pins terminating directly to the nearest ground plane.

The stability of the board signals that drive CPLD devices' JTAG circuitry is of equal importance. The JTAG specification dictates that the TMS and TDI signals be "pulled up" to the system power supply, but does not include the specific resistance value required. This creates an interesting quandary, particularly for long JTAG ISP chains across multiple vendor chips (**Figure 2**).

Figure 2a shows a mix of JTAG chips, attached in a standard format. Figure 2b shows that each chip may provide an internal pullup resistor of a different value at each site; in Figure 2b, the pull-up resistors

"To take advantage of ISP, some simple guidelines must be followed. These guidelines are straightforward..."

gramming Guidelines

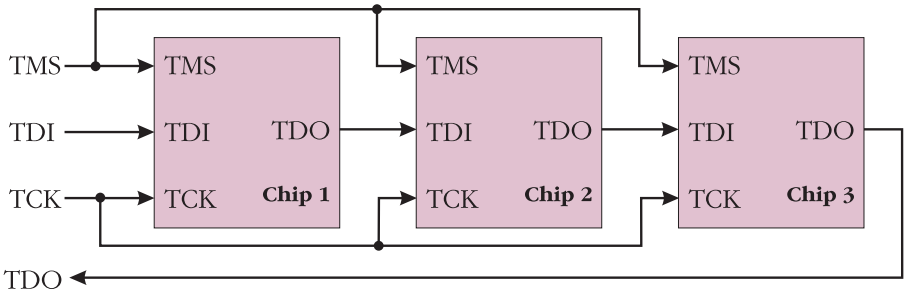


Figure 2a: *Ideal JTAG Chain*

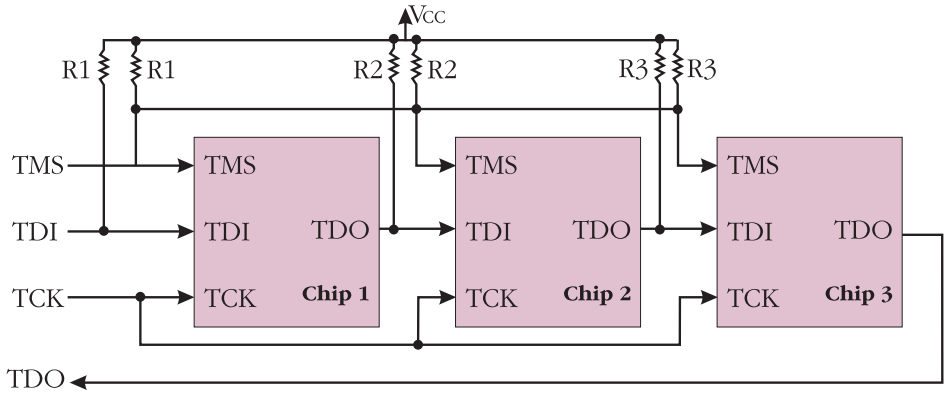


Figure 2b: *More "real" JTAG Chain*

are shown external to the chips, but in reality, they are contained inside the respective chip — and are out of the designer's control. Luckily, most JTAG TCK speeds are well below 10 MHz, minimizing transmission line effects.

Recommendations that will aid in trouble-shooting problems caused by impedance mismatches on the JTAG signal lines include the following:

- For long JTAG chains (greater than 5 or 6 chips) include a buffer site. This is a point where the external cable may be isolated from the rest of the chain.
- Consider including sites where series or parallel termination resistance can be attached. This will have to be determined experimentally.
- If prototype difficulty persists, consider breaking up the on-board JTAG chain with additional buffers.

Finally, continuing improvements to the software protocols are increasing the reliability of in-system programming. The new XACT*step* M1 JTAG download software includes the latest ISP protocols to best manage the actual delivery of bits into the end system. Patches and updated releases are made available at WebLINX (www.xilinx.com). ◆

Viewlogic

How do I select the correct Xilinx libraries for an M1 design within Workview Office?

The file %WVOFFICE%\STANDARD\LIBS.LST defines the library listings for Workview Office. The LIBS.LST file that is shipped with current versions of Workview Office contains Xilinx libraries for XACT*step* v6.0.1. To update this file for version M1, you will need to download a file from our FTP site to replace the current LIBS.LST. The file, called M1LIBS.ZIP, can be found at ftp://ftp.xilinx.com/pub/swhelp/viewlogic.

Hundreds of warnings/errors about "Unexpanded Blocks," "No Driver/Load," and "Multiple Drivers" appear when running NGDBUILD. What causes this, and how can it be prevented?

The flow for a Viewlogic-Xilinx M1 design includes writing out an EDIF file from the Viewlogic design environment. The Viewlogic program EDIFNETO is responsible for this, but it must be run with a Xilinx option. When using the Workview Office or Powerview GUI to run EDIFNETO, enter the word "xilinx" in the Level field. The command line equivalent for this option is:

```
edifneto -l xilinx design
```

It stops the EDIF netlister at Xilinx primitives.

Mentor Graphics

When running PLD_EDIF2TIM in the M1 simulation flow, what causes the following error:

```
// Error: Cannot find library
  specified "/home/salma/dsprdo/
  SIMPRIMS" (from: Synthesis/EDIF
  Interface/Miscellaneous 15)
// Error: View "view_1" was not
  created successfully;
// thus cannot instantiate "AND0".
  (from: Synthesis/EDIF Interface/
  Miscellaneous 1C)
// Note: Finding part "SIMPRIMS/
  x_and2" (from: Synthesis/EDIF
  Interface/Eddm Interface 81)
// Error: Could not find the
  External part "SIMPRIMS/x_and2".
  (from: Synthesis/EDIF Interface/
  Miscellaneous 25)
```

Timing simulations in XACT*step* version M1 use the simprim (simulation primitive) library to model routed designs. For Mentor Graphics, these simulation models are located in the $SIMPRIMS library. The $SIMPRIMS variable typically is set to $LCA/simprims.

The EDIF file that PLD_EDIF2TIM is processing should reference this simulation library as "$SIMPRIMS". However, in this situation, the library is referenced as simply "SIMPRIMS" (without the dollar sign). This causes ENRead, the Mentor EDIF reader used by PLD_EDIF2TIM, to look in the current directory for a SIMPRIMS subdirectory, where it expects to find the libraries.

To correct this, the EDIF file must be rewritten to reference the simprim library as $SIMPRIMS. This is done using the vendor option in the NGD2EDIF command line:

```
ngd2edif -v mentor
  filename.nga
```

Optionally, if using the Xilinx Design Manager/Flow Engine, go to the Implementation Options Template. Under the Interface panel, change the Simulation Data Options: Vendor setting to "Mentor". Rerun the Timing stage of the Flow Engine and reprocess the EDN file through PLD_EDIF2TIM.

***Need technical help right now?* Here's where to start:**

1. **Find us on the Internet at www.xilinx.com** — We update our **"Answers"** Web tool daily with the latest application notes, data sheets, patches and solutions to your technical questions. Get immediate answers 24 hours per day!

If you don't have access to the Web or can't locate an answer via step #1, then...

2. **Contact your nearest Customer Support Hotline**

NORTH AMERICA

(Mon, Tues, Wed, Fri 6:30am-5pm, Thur 6:30am - 4:00pm Pacific Time)
Hotline: 800 255 7778
or 408 879 5199
Fax: 408 879 4442
BBS: 408 559 9327
Email: hotline@xilinx.com

UNITED KINGDOM

(Mon, Tues, Wed, Thur 9:00am-12:00pm, 1:00-5:30pm, Fri 9:00am-12:00pm, 1:00-3:30pm)
Hotline: (44) 1932 820821
Fax: (44) 1932 828522
Email: ukhelp@xilinx.com

FRANCE

(Monday-Friday 9:30am-12:30pm, 2:00-5:30pm)
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Fax: (33) 1 3463 0959
Email: frhelp@xilinx.com

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Fax: (49) 89 904 4748
Email: dlhelp@xilinx.com

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Increased Design Portability with XACT*step* Version M1

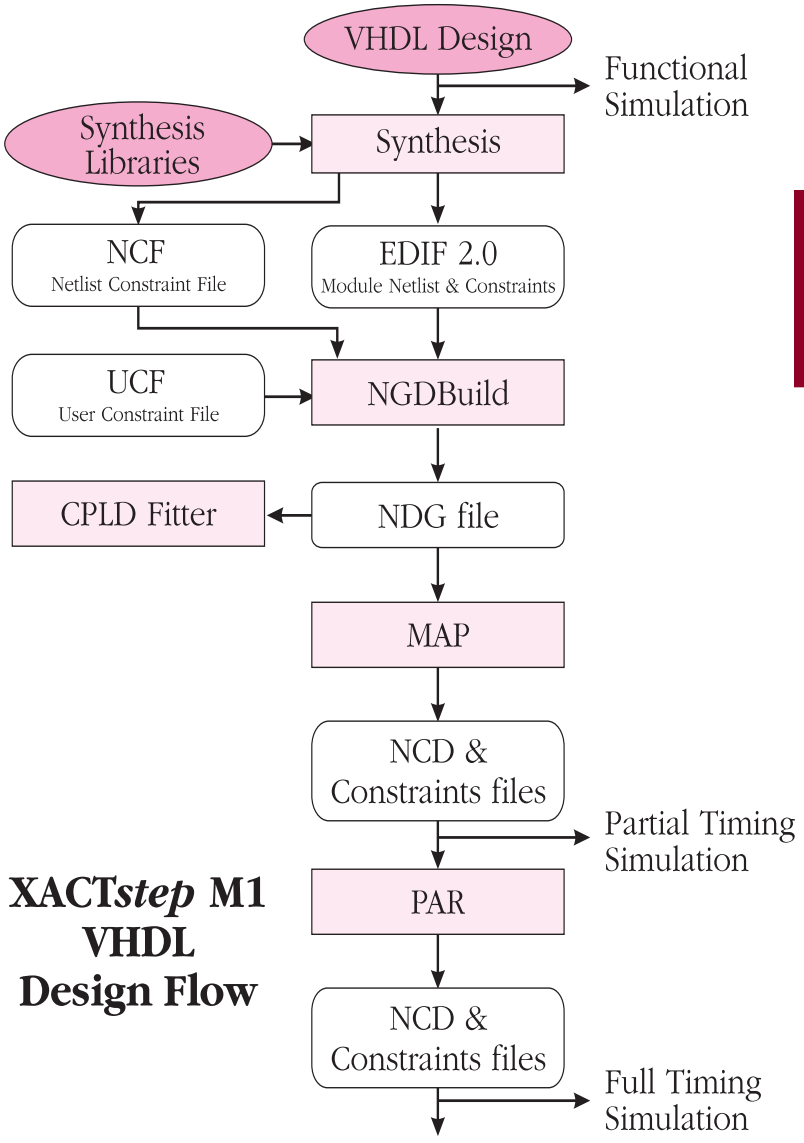
The Xilinx XACT*step* version M1 software technology enables users at every design level to increase optimization, manage design changes, and quickly complete designs with the entire spectrum of Xilinx FPGA and CPLD devices. For example, the version M1 tools are designed to support multiple device architectures using the same core physical implementation (i.e., map, place and route) software. To implement this capability, a new program has been introduced into the design flow: **NGDBuild**.

NGDBuild is responsible for two functions during the design implementation process. First, the design's elements are brought together into a single database so that subsequent operations, such as map, place and route, may be applied to the entire design at once. Second, NGDBuild re-expresses the design as a netlist of "technology-less" primitives that are common to all CPLDs and FPGAs. The components in this technology-independent library are known as "SimPrims."

NGDBuild's impact on the design is to make it instantly "re-targetable" between any of the Xilinx device architectures supported by the core software. Thus, a design's performance may be investigated in any Xilinx architecture, with little or no design rework required.

The core implementation tools (map, place and route) receive a netlist from NGDBuild that expresses the design as a netlist of SimPrims, and it's these technology-independent cells that are implemented within the target device. Consequently, the back-annotation process (that is the creation of a post-Map or post-PAR netlist describing the design's physical implementation) results in a netlist of SimPrims annotated with the appropriate block and net delay data that arises from the place and route process.

As a result of this strategy, different simulation libraries are needed to support simulation before and after NGDBuild has been applied to a design. Prior to NGDBuild, designs will be expressed as netlists containing Unified Library components. After NGDBuild, designs will be expressed as netlists consisting of SimPrims. ◆



XACT*step* M1 VHDL Design Flow

Programmable Logic in Mixed Voltage Applications

The use of advanced, deep-submicron IC fabrication processes is resulting in rapidly increasing density and performance for programmable logic devices. However, as device geometries shrink below 0.5 microns, the smallest transistors cannot withstand 5 volts without damage. Thus, the largest and fastest new devices are based on lower supply voltages. For example, the new XC4000XL FPGA family, featuring the industry's highest-capacity, high-performance FPGAs, is based on the 3.3V standard.

To reap the benefits of advanced process technology — including increased performance, increased density, lower power consumption, and lower price — many programmable logic users are making the transition from the 5V standard to lower voltages. This transition affects not only the supply voltage, but also I/O signaling levels. Xilinx is actively taking the lead in working with programmable logic users to plan an orderly transition to a lower voltage standard.

Xilinx introduced the Zero+ product line, the industry's first 3.3V FPGAs, in 1993. Since then, the number of 3.3V product offerings has increased dramatically. However, many other system components remain available in 5V versions only. Thus, mixed-voltage systems employing a mix of 5V and 3.3V components are likely to be the rule rather than the exception in the immediate future.

Xilinx products have been designed with this mixed-voltage environment in mind. 5V input tolerance has been designed into many Xilinx 3.3V devices; these devices accept 5V signals on all I/Os and can drive TTL levels into any 5V device, eliminating all interface issues. Many Xilinx 5V components can directly interface with 3.3V devices. Table 1 lists the Xilinx component product families that can be employed in mixed-voltage systems. All Xilinx device inputs maintain their excellent protection against electrostatic discharge (ESD), even in mixed-voltage applications.

"Xilinx introduced the Zero+ product line, the industry's first 3.3V FPGAs, in 1993. Since then, the number of 3.3V product offerings has increased dramatically."

Mixing 5V and 3.3V Devices

When mixing 3.3V and 5V devices on the same board, I/O signaling levels compatible with both types of components are needed on all signals lines connecting the two types of components. Since both types of supply share a common ground, there are no problems interfacing logic Low levels in either direction, but there are compatibility issues for the logic High levels.

3.3V Devices Driving Inputs on 5V Devices

The lowest output High voltage (V_{OH}) of the 3.3 device must exceed the V_{IH} requirements of the 5V device. Minimum V_{OH} for all Xilinx 3.3V devices is 2.4V, well above the 2.0V minimum High level for TTL signaling. (This includes the XC3000L, XC3100L, XC5200L, and XC4000XL FPGA families and the XC7300 and XC9500 CPLD families when V_{CCIO} = 3.3V.) Thus, all Xilinx 3.3V devices can drive inputs to devices with TTL-compatible input thresholds, including all 5V Xilinx devices. (Note: Some Xilinx 5V devices can be programmed for TTL or CMOS input thresholds; these devices must be configured for TTL-compatible inputs to be directly driven from a 3.3V device.)

5V Devices Driving Inputs on 3.3V Devices

The highest 5V device output voltage must not force excessive current into the input of the 3.3V device. The input structures of Xilinx 3.3V FPGAs include input protection circuits. These protection circuits in the XC3000L and

	Device Family	Accepts 3.3V Compatible Inputs[1]	Drives 3.3V Devices	Key Features
Single Supply V_{CC} = 5V	XC3000A	Yes	With limiting resistor	Low quiescent current
	XC3100A	Yes	With limiting resistor	High performance
	XC4000E/EX	Yes	Yes	Highest density and performance
	XC5200	Yes	With limiting resistor	Cost-effective
	XC7300	Yes	With limiting resistor	5 ns T_{PD}, 100% utilization
	XC9500	Yes	With limiting resistor	5V in-system-programmable, pin locking

	Device Family	Accepts 5V Compatible Inputs	Drives 5V Devices	Key Features
Single Supply V_{CC} = 3.3V	XC3000L	With limiting resistor	Yes	Very low powerdown & quiescent current
	XC3100L	With limiting resistor	Yes	High performance
	XC4000XL	Yes	Yes	Highest density & performance
	XC5200L	With limiting resistor	Yes	Cost-effective

	Device Family	Accepts 5V Compatible Inputs	Drives 5V Devices	Key Features
Dual Supply	XC5200L	Yes	Yes	Cost-effective
V_{CC} = 5V	XC7300	Yes	Yes	Mixed-voltage system capable
V_{CCIO}/V_{TT} = 3.3V	XC9500	Yes	Yes	Mixed-voltage system capable

Table 1: *Xilinx products and supply voltage options*

Note: (1) Inputs must be configured for TTL thresholds

XC3100L devices are designed for 3.3V inputs. However, the protection circuits in the XC4000XL and XC5000L devices are designed to withstand 5V levels.

Most 5V devices have complementary CMOS outputs where V_{OH} can reach the 5V rail. (All Xilinx 5V FPGAs and CPLDs, except the XC4000 series devices, have complementary CMOS outputs.) When driving XC3000L and XC3100L inputs (and most other 3.3V devices) from such a 5V device, then the input current must be limited by a series resistor of no less than 150Ω. This guarantees an input current below 10mA, flowing through the ESD input protection diode backwards into the 3.3V supply. That amount of input current is generally considered safe, causing neither metal migration nor latch-up problems. Care must be taken to avoid forcing the nominally 3.3V supply voltage above its 3.6V maximum whenever a large number of active High inputs drive the 3.3V device, potentially causing the 3.3V supply current to reverse direction. The 3.3V V_{CC} power should be on before driving the device inputs from a 5V device.

The I/O structures of the XC4000XL FPGAs have been designed to tolerate being driven to a 5V rail by a low-impedance source. These 3.3V FPGAs can be directly driven by 5V devices with either TTL or CMOS outputs. Power supply sequencing is not a problem; the inputs can be driven to 5V either before or after the 3.3V V_{CC} power is supplied without risking damage to the devices.

In mixed voltage systems, the XC7300 and XC9500 CPLDs can be driven directly by 5V inputs when set up for 3.3V I/O operation (i.e., V_{CCIO} = 3.3V). The input protection diodes in these CPLDs are always connected to the 5V V_{CC} power line, allowing them to tolerate 5V inputs without the need for current-limiting resistors.

Similarly, the XC5000L FPGAs can be used in mixed-voltage systems by connecting the V_{TT} pin to 5V. The input protection circuits are connected to the V_{TT} line, allowing these 3.3V FPGAs to tolerate 5V inputs without the need for current-limiting resistors.

If the 5V device has "totem-pole" n-channel-only outputs (as in the XC4000E/EX FPGA series), V_{OH} is reduced by one threshold and the series resistor can be eliminated, provided the nominally 5V supply does not exceed 5.25. Thus, the XC4000E and XC4000EX FPGAs can directly drive any 3.3V device without the need for current-limiting resistors. ◆

Integrating XC9500 ISP With Manufacturing

In-system programming (ISP) allows the programming and reprogramming of logic devices already soldered on a system board. ISP capability provides many advantages, including facilitating design changes during prototyping, remote system upgrades, and manufacturing flows.

The XC9500 CPLD family supports the in-system programming of its FLASH configuration memory using the IEEE 1149.1 (JTAG) test access port (TAP), and without requiring externally applied "supervoltages" (i.e., voltages greater than 5V). This allows the use of automatic test equipment (ATE) that supports the JTAG TAP to program XC9500 family devices. Thus, CPLD device programming can be integrated with board testing in a single manufacturing step.

The Genrad GR228X series of board test systems are examples of such ATE platforms. This series includes the following Genrad testers: the GR2287L, GR2286i, GR2287i, GR2283i, GR2284i, GR2281i, and GR2280i systems. The tester must be running version 3.2 (or higher) of the Genrad software. (Deep vector memory is not required.) Creating the appropriate "test program" for a GR228X system requires the Xilinx EZTag software and a Xilinx-supplied vector translation tool (svf2dts), as described below.

Using EZTag to generate an SVF file

EZTag can generate a serial vector format (SVF) file from the JEDEC programming file of the target design. The SVF file is in ASCII format and describes 1149.1 TAP operations; the file encodes the entire programming algorithm for the selected device in the system as a series of JTAG TAP instructions.

The XC9500 programming operation includes a built-in verification step. However, in developing a new ATE ISP flow, a separate readback/verify step may be used as an ATE ISP process verification step.

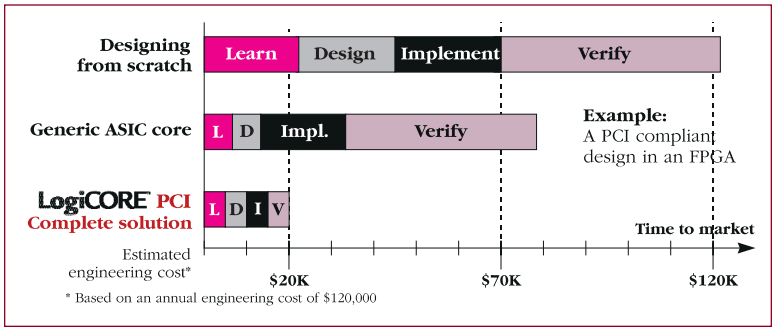
EZTag can generate an SVF file for erasure, programming, or readback verification, using the following steps:

CORE Generator

Continued from page 14

information and design files for registered LogiCORE product owners; all users with a valid maintenance agreement can log onto the new LogiCORE lounges and register for access to the CORE Generator. The CORE Generator tool is password protected so that only LogiCORE PCI owners have access to the core.

Figure 2: *Proven LogiCORE PCI core cut development time*



For now, even WebLINX visitors without a valid maintenance agreement can access a *demonstration* version of the PCI CORE Generator, allowing the evaluation of the GUI and an examination of the various options available for the PCI interface core. In the future, all visitors will be allowed to create functional simulation models for LogiCORE PCI designs, allowing users to create and download the model, instantiate it into a custom design, and perform complete system functional verification, all prior to purchasing the core.

Further information, including the demonstration version of the CORE Generator, can be found at www.xilinx.com/products/logicore/logicore.htm. ◆

Test on the GR228X

1. Create the XC9500 design using XABEL-CPLD or any compatible third-party design entry tool.
2. Fit the design and save it as a JEDEC output file.
3. Invoke the EZTag software from the XACT command line using the following command:

   ```
   eztag -svf
   ```

   The following message appears:

   ```
   Xilinx (R) EZTAG XC9500-CPLD-6.0.5
    - JTAG Boundary-Scan Download
   Copyright (C) Xilinx Inc. 1991-
   1996. All Rights Reserved.
   ____________________________

   SVF GENERATION MODE.
   EZTAG?
   ```

4. At this prompt, type the following command:

   ```
   part deviceType1:designName1 …
    deviceTypeN:designNameN
   ```

   where designName is the name of the design to translate into SVF, and deviceTypeN is the type of device in the nth position in the JTAG device chain (beginning with the first device to receive TDI and ending with the last device to output TDO). For any non-XC9500 part in the JTAG chain, the BSDL file for the specified part must be available along the XACT path and is called deviceType.bsd (e.g., 4003pc84.bsd for a XC4003 in the PC84 package).

5. Enter any one of the following commands:

   ```
   erase designName
   ```

   generates an SVF file that specifies the bit sequence to erase the device.

   ```
   program [-b] designName [-j
    jedecFileName]
   ```

   generates an SVF file that specifies the bit sequence to erase and program the specified part from a JEDEC file named designName.jed (or alternately, the JEDEC file name specified after the "-j"). Use the -b option to skip the erase.

   ```
   verify designName [-j
    jedecFileName]
   ```

   generates an SVF file that specifies the bit sequence to read back the device contents and compares it against the contents of the specified JEDEC file.

6. Exit EZTag by entering the quit command

The SVF file contains all data and commands necessary to perform the specified function. The SVF file will be named designName.svf, and will be created in the current working directory (the directory in which EZTAG is being run). Consecutive operations on the same designName file will overwrite the SVF file each time.

Generating a Genrad GR228X ISP Program

The svf2dts program translates SVF files to GR228X stimulus files. The svf2dts software and accompanying documentation is available via WebLINX (www.xilinx.com), and the associated Xilinx ftp site. The svf2dts translation tool is supported on DOS, Windows 95, DOS window on SCO UNIX, and Windows NT platforms.

The svf2dts program is run on the computer that is the controller for the GR228X tester. On the tester's controller, make a directory called "svf" and copy all the SVF files into this directory. The svf2dts program performs the SVF to DTS conversion, where DTS (digital test source) is the GR228X stimulus description language. The DTS file is partitioned into "bursts" of 15K vectors. Invoke the "svf2dts" program with the name of SVF program file as follows:

```
svf2dts <SVF file>
```

A copyright notification appears; enter return to clear this display. The program now takes you through a series of questions about file names, TAP pin numbers, and similar information.

Once all the questions have been answered, the program executes after printing the start time. A running total of the SVF records processed is given. When the svf2dts program finishes processing the records, it writes the .DTS file. The resulting DTS file can be used to program the device on the Genrad GR228X tester, as part of an integrated device program and board test operation.

> *"CPLD device programming can be integrated with board testing in a single manufacturing step."*

For further information, or to download the svf2dts program, visit WebLINX at www.xilinx.com/apps/epld.htm. ◆

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E	XC4028EX	XC4036EX	XC4005XL	XC4010XL	XC4013XL	XC4020XL	XC4028XL	XC4036XL	XC4044XL	XC4052XL
44	PLASTIC LCC	PC44		◆												◆																						
	PLASTIC QFP	PQ44																																				
	PLASTIC VQFP	VQ44																																				
	CERAMIC LCC	WC44																																				
64	PLASTIC VQFP	VQ64		◆					◆							◆																						
68	PLASTIC LCC	PC68	◆	◆											◆	◆																						
	CERAMIC LCC	WC68																																				
84	PLASTIC LCC	PC84	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆						◆	◆						
	CERAMIC LCC	WC84																																				
	CERAMIC PGA	PG84	◆	◆	◆										◆	◆	◆																					
100	PLASTIC PQFP	PQ100	◆	◆	◆										◆	◆	◆				◆	◆									◆	◆						
	PLASTIC TQFP	TQ100														◆	◆																					
	PLASTIC VQFP	VQ100		◆	◆				◆	◆			◆			◆	◆				◆																	
	TOP BRZ. CQFP	CB100	◆		◆										◆	◆	◆																					
120	CERAMIC PGA	PG120																			◆																	
132	PLASTIC PGA	PP132			◆	◆											◆	◆																				
	CERAMIC PGA	PG132			◆	◆											◆	◆																				
144	PLASTIC TQFP	TQ144			◆	◆	◆			◆	◆	◆	◆	◆			◆	◆				◆	◆															
	CERAMIC PGA	PG144																																				
156	CERAMIC PGA	PG156																				◆	◆															
160	PLASTIC PQFP	PQ160				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆					◆	◆	◆	◆				
164	TOP BRZ. CQFP	CB164					◆												◆	◆		◆															
175	PLASTIC PGA	PP175					◆												◆	◆																	
	CERAMIC PGA	PG175					◆												◆	◆																	
176	PLASTIC TQFP	TQ176					◆					◆		◆					◆																		
191	CERAMIC PGA	PG191																						◆	◆												
196	TOP BRZ. CQFP	CB196																							◆												
208	PLASTIC PQFP	PQ208					◆												◆	◆		◆	◆	◆	◆	◆					◆	◆	◆	◆				
	HI-PERF QFP	HQ208																							◆	◆	◆		◆					◆	◆		
223	CERAMIC PGA	PG223																		◆						◆	◆	◆					◆				
225	PLASTIC BGA	BG225																							◆	◆											
228	TOP BRZ. CQFP	CB228																								◆		◆									
240	PLASTIC PQFP	PQ240																								◆							◆	◆			
	HI-PERF QFP	HQ240																								◆	◆	◆	◆	◆					◆	◆	◆	◆
256	PLASTIC BGA	BG256																														◆	◆	◆				
299	CERAMIC PGA	PG299																										◆	◆					◆				
304	HI-PERF. QFP	HQ304																										◆	◆	◆				◆	◆			
352	SUPER BGA	BG352																											◆	◆				◆	◆	◆		
411	CERAMIC PGA	PG411																												◆					◆	◆	◆	
432	SUPER BGA	BG432																												◆					◆	◆	◆	
475	CERAMIC PGA	PG475																																				
559	CERAMIC PGA	PG559																																				
560	SUPER BGA	BG560																																				◆

MAY 1997

PINS	TYPE	CODE	XC4062XL	XC4085XL	XC4005L	XC4010L	XC4013L	XC5202	XC5204	XC5206	XC5210	XC5215	XC6216	XC6264	XC7236A	XC7272A	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144	XC9536	XC9572	XC95108	XC95216	XC95288
44	PLASTIC LCC	PC44													◆		◆	◆	◆	◆				◆	❖			
	PLASTIC QFP	PQ44															◆	◆	◆									
	PLASTIC VQFP	VQ44																◆				◆						
	CERAMIC LCC	WC44													◆			◆	◆	◆								
64	PLASTIC VQFP	VQ64																										
68	PLASTIC LCC	PC68														◆				◆	◆							
	CERAMIC LCC	WC68														◆				◆	◆							
84	PLASTIC LCC	PC84			◆	◆		◆	◆	◆	◆					◆					◆	◆			◆	◆		
	CERAMIC LCC	WC84														◆					◆	◆						
	CERAMIC PGA	PG84														◆												
100	PLASTIC PQFP	PQ100						◆	◆	◆											◆	◆			◆	◆		
	PLASTIC TQFP	TQ100																							◆	◆		
	PLASTIC VQFP	VQ100						◆	◆	◆																		
	TOP BRZ. CQFP	CB100																										
120	CERAMIC PGA	PG120																										
132	PLASTIC PGA	PP132																										
	CERAMIC PGA	PG132																										
144	PLASTIC TQFP	TQ144						◆	◆	◆	◆		◆															
	CERAMIC PGA	PG144																				◆						
156	CERAMIC PGA	PG156						◆	◆																			
160	PLASTIC PQFP	PQ160							◆	◆	◆	◆										◆	◆			◆	◆	
164	TOP BRZ. CQFP	CB164																										
175	PLASTIC PGA	PP175																										
	CERAMIC PGA	PG175																										
176	PLASTIC TQFP	TQ176				◆				◆	◆																	
191	CERAMIC PGA	PG191							◆																			
196	TOP BRZ. CQFP	CB196																										
208	PLASTIC PQFP	PQ208			◆	◆	◆			◆	◆																	
	HI-PERF QFP	HQ208										◆															◆	◆
223	CERAMIC PGA	PG223									◆																	
225	PLASTIC BGA	BG225					◆				◆	◆	◆							◆	◆							
228	TOP BRZ. CQFP	CB228																										
240	PLASTIC PQFP	PQ240					◆				◆																	
	HI-PERF QFP	HQ240	◆									◆	◆	❖														
256	PLASTIC BGA	BG256																										
299	CERAMIC PGA	PG299										◆	◆															
304	HI-PERF. QFP	HQ304										◆	◆															
352	PLASTIC BGA	BG352										◆		❖													◆	◆
411	CERAMIC PGA	PG411												❖														
432	PLASTIC BGA	BG432	◆																									
475	CERAMIC PGA	PG475	◆																									
559	CERAMIC PGA	PG559	◆	❖																								
560	PLASTIC BGA	BG560	◆	❖																								

◆ = Product currently shipping or planned

❖ = New since last issue of *XCell*

Programmer Support For Xilinx XC7200/XC7300 CPLDS — May 1997

MANUFACTURER	MODEL	7236A	7272A	7318	7336	7336Q	7354	7372	73108	73144
ADVANTECH	PC-UPROG LABTOOL-48				DISQUALIFIED			NS	NS	
ADVIN SYSTEMS	PILOT-U40 PILOT-U84	10.84B 10.84B	10.84B	10.86B 10.86B	10.86B 10.86B	10.84B 10.84B	10.84B 10.84B	10.84B	10.84B	10.84B
AMERICAN RELIANCE, INC.	SPECTRUM-48				DISQUALIFIED					
B&C MICROSYSTEMS, INC.	Proteus	Jun-97	Jun-97	Jun-97	Jun-97	Jun-97	Jun-97	Jun-97	Jun-97	Jun-97
BP MICROSYSTEMS	BP-1200 BP-1400 BP-2100 BP-2200	V3.15 V3.15 V3.15 V3.15	V3.15 V3.15 V3.15 V3.15	V3.15 V3.15 V3.15 V3.15	V3.18 V3.18 V3.18 V3.18	V3.15 V3.15 V3.15 V3.15	V3.15 V3.15 V3.15 V3.15	V3.15 V3.15 V3.15 V3.15	V3.15 V3.15 V3.15 V3.15	
BYTEK	CHIPBURNER-40		1.0a	1.0a	1.0a		1.0a	1.0a	1.0a	1.0a
DATAMAN	DATAMAN-48	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	
DATA I/O	2900 3900/AutoSite UniSite			V5.3 V5.3 V5.3	V5.3 V5.3 V5.3	V5.3 V5.3 V5.3	V5.3 V5.3 V5.3	 V5.3 V5.3	 V5.3 V5.3	
DEUS EX MACHINA ENGINEERING	XPGM	V1.60	V1.60	V1.60	V1.60	V1.60	V1.60	V1.60	V1.60	V1.60
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ MEGAMAX	V2.4U V1.1E	V2.4U V1.1E	V2.5i V2.1x	V2.5i V2.1x	V2.4U V1.1E	V2.4U V1.1E	V2.4U V1.1E	V2.4U V1.1E	
ELAN	6000 APS				DISQUALIFIED					
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V3.1 V3.1 V3.1 V3.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1
LEAP ELECTRONIC CO., LTD.	LEAPER-10 LP U4	V3.2 V2.1	V3.2 V2.1	V3.2 V3.0	V3.2 V3.0	V3.2 V2.1	V3.2 V2.1	V3.2 V2.1	V3.2 V2.1	
LOGICAL DEVICES	ALLPRO-88 ALLPRO-88XR ALLPRO-96 Chipmaster 2000 Chipmaster 6000 XPRO-1	6.4.26 V2.4U V1.31A	6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	
MICROPROSS	ROM9000	V3.85	Jun-97							
MQP ELECTRONICS	SYSTEM 2000 PIN-MASTER 48	V1.25	V1.25	V1.25	V1.25	V1.25	V1.25	V1.25	V1.25	V1.25
NEEDHAM'S ELECTRONICS	EMP20	V3.10	V3.10	V3.39	V3.39	V3.10	V3.10	V3.10	V3.10	
SMS	EXPERT OPTIMA				DISQUALIFIED DISQUALIFIED					
STAG	ECLIPSE	6.4.26	6.4.26	6.12.11	6.12.11	6.4.26	6.4.26	6.4.26	6.4.26	6.8.9
SUNRISE	T-10 UDP T-10 ULC				DISQUALIFIED DISQUALIFIED					
SUNSHINE	POWER-100 EXPRO-60/80	V8.40 V8.40	V8.40 V8.40	V8.40 V8.40	V8.40 V8.40		V8.40 V8.40	V8.40 V8.40	V8.40 V8.40	
SYSTEM GENERAL	TURPRO-1/FX MULTI-APRO	V2.30 V3.02	V2.30 V3.02	V2.31 V3.02	V2.31 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02
TRIBAL MICROSYSTEMS	Flex-700 TUP-300 TUP-400	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09	
XELTEK	SUPERPRO SUPERPRO II SUPERPRO II/P	2.4B 2.4B	2.4B 2.4B	2.5B 2.5B	2.5B 2.5B	2.5B 2.5B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B
XILINX	HW-130	V2.04	V2.04	V4.00	V4.00	V4.00	V4.00	V4.00	V4.00	V4.00

Programmer Support For XC9500 CPLDs — May 1997

MANUFACTURER	MODEL	9536	9536F	9572	9572F	95108	95108F	95216
ADVANTECH	LABTOOL-48	May-97	May-97	Jun-97	Jun-97	May-97	May-97	
BP MICROSYSTEMS	BP-1200 BP-1400 BP-2100 BP-2200	V3.21 V3.21 V3.21 V3.21	V3.21 V3.21 V3.21 V3.21	V3.24 V3.24 V3.24 V3.24	V3.24 V3.24 V3.24 V3.24	V3.21 V3.21 V3.21 V3.21	V3.21 V3.21 V3.21 V3.21	
DATA I/O	2900 3900/AutoSite UniSite	V5.4 V5.4 V5.4	V5.4 V5.4 V5.4	 V5.4 V5.4	 V5.4 V5.4	 V5.4 V5.4	 V5.4 V5.4	
HI-LO SYSTEMS RESEARCH	All-07	V3.02	V3.02	V3.02	V3.02	V3.02	V3.02	
LOGICAL DEVICES	ALLPRO-88 ALLPRO-96	May-97 V7.3.27	May-97 V7.3.27	Jun-97 Jun-97	Jun-97 Jun-97	May-97 V7.3.27	May-97 V7.3.27	
SMS	EXPERT OPTIMA	May-97 May-97	May-97 May-97	Jun-97 Jun-97	Jun-97 Jun-97	May-97 May-97	May-97 May-97	
STAG	ECLIPSE	V7.1.30	V7.1.30	Jun-97	Jun-97	V7.1.30	V7.1.30	
SYSTEM GENERAL	MULTI-APRO	May-97	May-97	Jun-97	Jun-97	May-97	May-97	
TRIBAL MICROSYSTEMS	Flex-700	V3.02	V3.02	V3.02	V3.02	V3.02	V3.02	
XILINX	HW-130*	V4.00	V4.00	V4.10	V4.10	V4.00	V4.00	V4.10

Changes since last issue are noted in color.

**** NOTE**: Reflects the version of the Host Software.*

Programmer Support For Xilinx XC1700 Serial Proms - May 1997

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
ADVANTECH	PC-UPROG				
	LABTOOL-48		DISQUALIFIED		
ADVIN	PILOT-U24	10.84B		10.84B	
	PILOT-U28	10.84B		10.84B	
	PILOT-U32	10.84B		10.84B	
	PILOT-U40	10.84B		10.84B	
	PILOT-U84	10.84B		10.84B	
	PILOT-142	10.84B		10.84B	
	PILOT-143	10.84B		10.84B	
	PILOT-144	10.84B		10.84B	
	PILOT-145	10.84B		10.84B	
AMERICAN RELIANCE, iNC.	SPECTRUM-48				
B&C MICROSYSTEMS INC.	PROTEUS-UP40	3.7Q		3.7Q	
BP MICROSYSTEMS	CP-1128				
	EP-1140				
	BP-1200	V3.15	V3.15	V3.15	
	BP-1400	V3.15	V3.15	V3.15	
	BP-2100	V3.15	V3.15	V3.15	
	BP-2200	V3.15	V3.15	V3.15	
BYTEK	135H-FT/U	8E	8E	8E	8E
	MTK-1000	8E	8E	8E	8E
	MTK-2000	8E	8E	8E	8E
	MTK-4000	8E	8E	8E	8E
	FIREMAN-8M	8E	8E	8E	8E
	FIREMAN-8X	8E	8E	8E	8E
	CHIPBURNER-40	1.0a	1.0a	1.0a	1.0a
DATAMAN	DATAMAN-48	V1.30		V1.30	
DATA I/O	UniSite	V5.4	V5.4	V5.4	BBS
	2900	V5.4	V5.4	V5.4	BBS
	3900	V5.4	V5.4	V5.4	BBS
	AutoSite	V5.4	V5.4	V5.4	BBS
	ChipLab	V5.4	V5.4	V5.4	BBS
	2700	V5.4	V5.4	V5.4	BBS
DEUS EX MACHINA	XPGM	V1.60	V1.60	V1.60	V1.60
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+	V2.4U	V2.4U	V2.4U	
	MEGAMAX	V1.1E	V1.1E	V1.1E	
ELAN DIGITAL SYSTEMS	3000-145				
	5000-145				
	6000 APS		DISQUALIFIED		
HI-LO SYSTEMS RESEARCH	All-03A	V3.19	V3.19	V3.19	V3.19
	All-07	V3.19	V3.19	V3.19	V3.19
ICE TECHNOLOGY LTD	Micromaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Speedmaster 1000/E	V3.17	V3.17	V3.17	V3.17
	Micromaster LV	V3.17	V3.17	V3.17	V3.17
	LV40 Portable	V3.17	V3.17	V3.17	V3.17
	Speedmaster LV	V3.17	V3.17	V3.17	V3.17

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
LEAP ELECTRONICS	LEAPER-10	V2.0		V2.0	
	LP U4	V2.0		V2.0	
LINK COMPUTER GRAPHICS	CLK-3100	V5.61		V5.61	
LOGICAL DEVICES	ALLPRO-40				
	ALLPRO-88	V2.7		V2.7	
	ALLPRO-88XR	V2.7		V2.7	
	ALLPRO-96	6.5.10	6.5.10	6.5.10	6.5.10
	CHIPMASTER 2000	V2.4U		V2.4U	
	CHIPMASTER 6000	V1.31A		V1.31A	
	XPRO-1	SPROM.310		SPROM.310	
MICRO PROSS	ROM 5000 B	V1.94		V1.94	
	ROM 3000 U	V3.84		V3.84	
	ROM9000				
MQP ELECTRONICS	MODEL 200	6.46	6.46	6.46	
	SYSTEM 2000	2.25	2.25	2.25	
	PIN-MASTER 48	V1.25	V1.25	V1.25	V1.25
NEEDHAM'S ELECTRONICS	EMP20	V3.10		V3.10	
RED SQUARE	IQ-180		DISQUALIFIED		
	IQ-280		DISQUALIFIED		
	Uniwriter 40		DISQUALIFIED		
	Chipmaster 5000		DISQUALIFIED		
SMS	Expert		DISQUALIFIED		
	Optima		DISQUALIFIED		
	Multisyte		DISQUALIFIED		
	Sprint Plus48		DISQUALIFIED		
STAG	Eclipse	6.5.10	6.5.10	6.5.10	6.5.10
	Quasar				
SUNRISE	T-10 UDP		DISQUALIFIED		
	T-10 ULC		DISQUALIFIED		
SUNSHINE	POWER-100	V8.40		V8.40	
	EXPRO-60/80	V8.40		V8.40	
SYSTEM GENERAL	TURPRO-1	V2.26H	V2.26H	V2.26H	V2.26H
	TURPRO-1 F/X	V2.26H	V2.26H	V2.26H	V2.26H
	TURPRO-1 T/X				
	APRO	V1.24			
	MULTI-APRO	V1.16	V1.16	V1.16	V1.16
TRIBAL MICROSYSTEMS	TUP-300	V3.19	V3.19	V3.19	V3.19
	TUP-400	V3.19	V3.19	V3.19	V3.19
	FLEX-700	V3.19	V3.19	V3.19	V3.19
XELTEK	SuperPRO				
	SuperPRO II	2.4B		2.4B	
	SuperPRO II/P	2.4B		2.4B	
XILINX	HW-112*		New algorithms in progress		
	HW-130*	V2.03	V2.03	V2.03	V2.03

**NOTE: Reflects the version of the host software*

Changes since last issue printed in color

Xilinx Alliance-EDA Companies & Products - May 1997 - 1 of 2

	Company Name	Product Name	Version	Function	3K/ 4K	XC 5200	CPLD 7K9K	Uni Lib	PLATFORMS PC	Sun	RS6000	HP7
DIAMOND	Aldec	Active-CAD	2.2	Schematic Entry, State Machine & HDL Editor, FPGA Synthesis & Simulation	✓	✓	✓	✓	✓			
	Cadence	Verilog	97A	Simulation	✓	✓	7k	✓		✓	✓	✓
		Concept	97A	Schematic Entry	✓		7k	✓		✓	✓	✓
		FPGA Designer	97A	Topdown FPGA Synthesis	✓	✓	7k	✓		✓	✓	✓
		Synergy	97A	FPGA Synthesis	✓	✓	7k	✓		✓	✓	✓
		Composer	97A	Schematic Entry	✓		7k	✓		✓	✓	✓
	Mentor Graphics	Design Architect	B.x	Schematic Entry	✓	✓	7k	✓		✓	✓	✓
		Galileo	3.2.5	Synthesis/Timing Analysis	✓	✓	✓	✓		✓	✓	✓
		Leonardo	4.0.3	Synthesis/Timing Analysis	✓	✓	✓	✓		✓	✓	✓
		QuickSim II	B.x	Simulation	✓	✓	7k	✓		✓	✓	✓
		QuickHDL	B.x	Simulation	✓	✓	7k	✓		✓	✓	✓
	Synario Design Automation	ABEL	6.3	Synthesis, Simulation			✓	✓	✓			
		Synario	2.3	Schematic Entry, Synthesis & Simulation	✓	✓	✓	✓	✓			
	Synopsys	FPGA Express	1.1	Synthesis	✓	✓	9k		✓			
		FPGA Compiler	97.01	Synthesis	✓	✓	✓	✓		✓	✓	✓
		Design Compiler	97.01	Synthesis	✓	✓	✓	✓		✓	✓	✓
		VSS	97.01	Simulation	✓	✓	✓	✓		✓	✓	✓
	Viewlogic	WorkView Office	7.1.2/7.2	Schem/Sim/Synth	✓	✓	✓	✓	✓			
		PowerView	6.0	Schem/Sim/Synth/Timing Analysis	✓	✓	✓	✓		✓	✓	✓
RUBY	Capilano Computing	Design Works	3.1	Schematic Entry/Sim	✓			✓	✓			
	Compass Design Automation	ASIC Navigator		Schematic Entry	✓	✓	7k			✓		✓
		X-Syn		Synthesis	✓					✓		✓
		QSim		Simulation	✓	✓	7k			✓		✓
	Escalade	DesignBook	2.0	Design Entry	✓			✓	✓	✓		
	Exemplar Logic	Galileo	3.2.5	Synthesis/Timing Analysis Simulation	✓	✓	✓	✓	✓	✓		✓
		Leonardo	4.0.3	Synthesis/Timing Analysis	✓	✓	✓	✓		✓	✓	✓
	IK Technology Co.	Ishizue Professionals	1.06	Schematic Entry/Simulation	✓	4Q			✓	✓		✓
	IKOS Systems	Voyager	2.31	Simulation	✓	✓				✓		✓
		Gemini	1.21	Simulation	✓	✓				✓		✓
	INCASES Engineering GmbH	Theda	5.0	Design Entry	✓				✓	✓	✓	✓
	ISDATA	LOG/iC2	5.0	Synthesis Simulation	✓	✓	7k	✓	✓	✓		✓
	Logic Modeling Corp. (Synopsis Division)	Smart Model		Simulation Models	✓	✓	7k,9k		✓	✓	✓	✓
		LM1200		Hardware Modeler	✓		7k,9k		✓	✓	✓	
	Model Technology	V-System/VHDL	4.4j (PC) / 4.6a (WS)	Simulation	✓			✓	✓	✓	✓	✓
	OrCAD	Capture (Win)	7.0	Schematic Entry	✓	✓	✓	✓	✓			
		Simulate (Win)	6.10	Simulation	✓	✓	✓	✓	✓			
		VST 386+ (DOS)	1.2	Simulation	✓			✓	✓			
		SDT 386+ (DOS)	1.2	Schematic Entry	✓			✓	✓			
		PLD 386+ (DOS)	2.0	Synthesis	✓			✓	✓			
	Protel Technology	Advanced Schematic	3.2	Schematic Entry	✓	✓	7k	✓	✓			
		Advanced PLD	3	PLD/FPGA Design & Simulation	✓	✓	7k		✓			
	Quad Design Technology	Motive	4.3	Timing Analysis	✓				✓	✓	✓	✓
	SimuCad	Silos III	96.1	Schematic Entry & Simulation	✓	✓		✓	✓			
	Sophia Sys & Tech	Vanguard	5.31	Schematic Entry	✓		✓		✓	✓		✓
	Summit Design Corp.	Visual HDL	3.0	Graphical Design Entry/ Simulation/Debug	✓	✓	✓	✓	✓	✓	✓	✓
	Synplicity, Inc.	Synplify-Lite	2.6c	Synthesis	✓	✓	9k	✓	✓	✓		✓
		Synplify	2.6c	Synthesis	✓	✓	9k	✓	✓	✓		✓
	TopDown Design Solutions	V-BAK	1.1	XNF to VHDL translator	✓	✓		✓	✓	✓	✓	

Xilinx Alliance-EDA Companies & Products - May 1997 - 2 of 2

	Company Name	Product Name	Version	Function	3K/ 4K	XC 5200	CPLD 7K9K	Uni Lib	Platforms PC	Sun	RS6000	HP7
RUBY	Veda Design Automation Inc	Vulcan	4.5	Simulation	✓					✓		✓
	Veribest	Veribest VHDL	14.0	Schematic Entry	3k,4k			✓	✓	✓		✓
		Veribest Verilog	14.0	Simulation	3k,4k			✓	✓	✓		✓
		VeriBest Simulator	14.0	Simulation	3k,4k	✓		✓	✓	✓		✓
		DMM	14.x	Design Management	3k,4k	✓		✓	✓	✓		✓
		VeriBest Synthesis	14.0	Synthesis	3k,4k	✓		✓	✓	✓		✓
		Synovation	12.2	Synthesis	3k,4k			✓	✓	✓		✓
		PLDSyn	12.0	Design Entry Synthesis	✓		7k		✓	✓		✓
		VerBest Design Capture	14.x	Design Capture	3k,4k	✓		✓	✓	✓		✓
EMERALD	Accolade Design Automation	Peak VHDL	3.2	Simulation	✓	✓	✓	✓	✓			
		Peak FPGA	3.20	Synthesis	✓	✓	✓	✓	✓			
	ACEO Technology, Inc.	Asyn	4.1	Synthesis	✓	✓		✓	✓	✓	✓	✓
		Softwire	3.3	Multi-FPGA Partitioning	✓	✓		✓	✓	✓	✓	✓
		Gatran	3.3	ASIC to FPGA Netlist Mapping	✓	✓		✓	✓	✓	✓	✓
	Acugen Software, Inc.	Sharpeye	2.60	Testability Analysis	✓	✓	7k		✓	✓		✓
		ATGEN	2.60	Automatic Test Generation	✓	✓	7k		✓	✓		✓
		AAF-SIM	2.60	Fault Simulation	✓	✓	7k		✓	✓		✓
		PROGBSDL	2.63	BSDL Customization	✓	✓	7k		✓	✓		✓
		TESTBSDL	2.63	Boundary Scan ATG	✓	✓	7k		✓	✓		✓
	ALPS LSI Technologies	Edway Design Systems		Synthesis/Simlulation	✓		✓		✓			
	Aptix Corporation	System Explorer	3.1	System Emulation	✓	✓	✓			✓		✓
		ASIC Explorer	2.3	ASIC Emulation	4K	✓		✓				
	Aster Ingenierie S.A.	XILLAS	4.2	LASAR model generation	✓		7k		✓	✓		✓
	Auspy Development Co.	APS	1.3.3	Multi-FPGA Partitioning	✓	✓			✓	✓		
	Chronology Corporation	TimingDesigner	3.0	Timing Specification and Analysis	✓	✓	7k,9k	✓	✓	✓		✓
		QuickBench	1.0	Visual Test Bench Generator	✓	✓	7k,9k	✓	✓	✓		✓
	CINA-Computer Integrated Network Analysis	SmartViewer	1.0e	Schematic Generation	✓		7k		✓			
	Epsilon Design Systems	Logic Compressor		Synthesis optimization	✓	✓			✓	✓	✓	✓
	Flynn Systems	Probe	3.0	Testability Analysis	✓	✓	7k		✓			
		FS-ATG	3.0	Test Vector Generation	✓	✓	7k		✓			
		CKTSIM	3.0	Logic Analysis	✓	✓	7k		✓			
		FS-SIM	3.0	Simulation	✓	✓	7k		✓			
	Fujitsu LSI	PROVERD		Top-Down Design System	3k,4k				✓			
	Harmonix Corporation	PARTHENON	2.3	Synthesis	4k		7k		✓	✓		
	Logical Devices	Total Designer	4.7	Simulation & Synthesis	✓	✓	✓	✓	✓			
		Ulysa	1.0	VHDL Synthesis	✓	✓	✓	✓	✓			
	MicroSim	MicroSim Design Lab		Schematic, Simulation	✓	✓		✓	✓			
	MINC	PLDesigner-XL/PL-Synthesizer	3.3/3.2.2	Synthesis	✓				✓	✓		✓
	Teradyne	Lasar	6	Simulation	✓					✓		✓
	Tokyo Electron Limited	ViewCAD	1.2	FLDL to XNF translator	✓							
	Trans EDA Limited	TransPRO	1.2	Synthesis	✓					✓		✓
	Visual Software Solutions	Statecad	3.0	Grph. Design Entry, Sim., Debug	✓	✓	✓	✓	✓	✓		✓
	Zuken	Tsutsuji		Synthesis/Simulation	3k,4k					✓	✓	✓
	Zycad	Paradigm RP		Rapid Prototyping	✓					✓		✓
		Paradigm XP		Gate-level Sim	✓					✓		✓

Items that have changed since the last issue (XCell 24) are in color.

Diamond: These partners have strong strategic relationships with Xilinx and have a direct impact on our releases. Typically, Xilinx is directly involved in the development and testing of the interface to XACT*step* software for these products.

Ruby: These partners have a high degree of compatibility and have repeatedly shown themselves to be significant contributors to our users' development solutions.

Emerald: Proven Xilinx compatibility

XILINX ALLIANCE-EDA CONTACTS - MAY 1997

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Changes since last issue (*XCell* 24) printed in color.

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XILINX ALLIANCECORE PARTNERS - MAY 1997

Additional information is available on WebLINX, starting at: http://www.xilinx.com/products/logicore/alliance/tblpart.htm

PARTNER NAME	PHONE	EMAIL/WEB URL	EXPERTISE
ARM Semiconductor (USA), Inc. 1095 E. Duane Ave., Suite 211 Sunnyvale, CA 94086 (USA)	Tel: 408-733-3344 Fax: 408-733-9922	armsemi@netcom.com	Microprocessors, microcontrollers, peripherals, communications
Comit Systems 1250 Oakmead Pkwy, Suite 210 Sunnyvale, CA 94088 (USA)	Tel: 408-988-2988 Fax: 408-988-2133	preeth@comit.com www.comit.com	Base functions, communications
CoreEL Microsystems 46750 Fremont Blvd #208 Fremont, CA 94538 (USA)	Tel: 510-770-2277 Fax: 510-770-2288	sales@coreel.com www.coreel.com	ATM, communications
Digital Objects 3550 Mowry Ave., Suite 101 Fremont, CA 94538 (USA)	Tel: 510-795-2212 Fax: 510-795-2219	sales@digitalobjects.com www.digitalobjects.com	PCMCIA, CardBus
Eureka Technology 4962 El Camino Real, #108 Los Altos, CA 94022 (USA)	Tel: 415-960-3800 Fax: 415-960-3805	info@eurekatech.com	PCI, PowerPC peripherals
Integrated Silicon Systems, Ltd. 29 Chlorine Gardens Belfast, BT9 5DL (North. Ireland)	Tel: +44-1232-664664 Fax: +44-1232-669664	info@iss-dsp.com www.iss-dsp.com	DSP functions
Inventra/Mentor 1001 Ridder Park Drive, San Jose, CA 95131-2314 (USA)	Tel: 503-685-8000 Fax: 408-451-5690	info@mentorg.com www.mentorg.com/inventra	USB, PCI, DSP, telecom, microprocessor peripherals
Logic Innovations 6205 Lusk Boulevard San Diego, CA 92121 (USA)	Tel: 619-455-7200 Fax: 619-455-7273	fpga@logici.com www.logici.com	PCI, MPEG-2, ATM, communications
Memec Design Services 1819 S. Dobson Rd., Suite 203, Mesa, AZ 85202 (USA)	Tel: 602-491-4311 Fax: 602-491-4907	info@memecdesign.com www.memecdesign.com	Microprocessor peripherals, base functions, Xilinx design services
NMI Electronics, Ltd., Fountain House, Great Cornbow, Halesowen, West Midlands, B63 3BL (UK)	Tel: +44 121 585 5979 Fax: +44 121 585 5764	ip@nmi.co.uk www.nmi.co.uk	Design services and base-level functions for the XC9500
Phoenix Technologies/Virtual Chips 411 E. Plumeria Drive, San Jose, CA 95134 (USA)	Tel: 408-570-1000 Fax: 408-452-0952	virtualchips-info@phoenix.com www.phoenix.com	PCI, USB, CardBus, ATM
Rice Electronics PO Box 741 Florissant, MO 63032 (USA)	Tel: 314-838-2942 Fax: 314-838-2942	ricedsp@aol.com	DSP
SAND Microelectronics 3350 Scott Blvd., #24, Santa Clara, CA 95131 (USA)	Tel: 408-235-8600 Fax: 408-235-8601	sales@sandmicro.com www.sandmicro.com	PCI, USB
SICAN Microeletronics Corp. 400 Oyster Point Blvd., #512, So. San Francisco, CA 94080 (USA)	Tel: 415-871-1494 Fax: 415-871-1504	infor@sican-micro.com www.sican-micro.com	CAN bus, DSP, communications
VAutomation 20 Trafalgar Square Suite 443 (4th Floor) Nashua, NH 03063 (USA)	Tel: 603-882-2282 Fax: 603-882-1587	sales@vautomation.com www.vautomation.com	Microprocessors, microcontrollers, communications

XILINX RELEASED SOFTWARE STATUS - MAY 1997

XILINX INDIVIDUAL PRODUCTS

KEY	PRODUCT CATEGORY	PRODUCT DESCRIPTION	PRODUCT FUNCTION	XILINX PART REFERENCE NUMBER	CURRENT VERSION BY PLATFORM PC1 *6.2*	SN2 *4.1.x*	HP7 *9.01*	LAST UPDT COMP	PREVIOUS VERSION RELEASE	NOTES/ FEATURES
U	CORE XEPLD	XC7K Support	Core Implementation	DS-550-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	PC update by request only
U*	XABEL-CPLD	XC7K, XC9500 Support	Entry/Simulation/Core	DS-571-PC1	6.1.2			11/96	6.1.1	New version w/Win 95 to 3.11, update by request
*	XACT-CPLD	XC7K, XC9500 Support	Core + Interface	DS-560-xxx	6.0.1	6.0.1	6.0.1	7/96	6.0	
	Mentor	8.4=A.4	Interface and Libraries	DS-344-xxx		5.2.1	5.2.1	7/96	5.20	
	OrCAD		Interface and Libraries	DS-35-PC1	6.0.1			7/96	6.0	Support for SDT+, VST+ v1.2
	Synopsys		Interface and Libraries	DS-401-xxx		5.2.1	5.2.1	7/96	5.20	DA1 platform remains at v5.2
	Viewlogic	PROcapture	Interface and Libraries	DS-390-PC1	6.0.1			7/96	5.2/6.0	Includes PRO Series 6.1
	Viewlogic	PROsim	Interface and Libraries	DS-290-PC1	6.0.1			7/96	6.0	Includes PRO Series 6.1
	Viewlogic		Interface and Libraries	DS-391-xxx	6.0.1	5.2.1	5.2.1	7/96	6.0	
	XABEL		Entry,Simulation,Lib, Optimizer	DS-371-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	Now available on HP7
	XBLOX		Module Generator & Optimizer	DS-380-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	
E	Verilog	2K,3K,4K,4KE,5K Lib.	Models & XNF Translator	ES-VERILOG-xxx		1.00	1.00	na	na	Sun and HP

XILINX PACKAGES

		SILICON SUPPORT 2K	3K	4K/E	5K	7K	9K						
	Cadence	X	X	X	X	X	X	DS-CDN-STD-xxx		5.2.1	5.2.1	7/96	5.20	
	Mentor	X	X	X	X	X	X	DS-MN8-STD-xxx		5.2.1	5.2.1	7/96	5.20	No AP1 update
	Mentor	X	X	X	X	X	X	DS-MN8-ADV-xxx		7.00	7.00	na	na	
U	OrCAD	X	X	X	X	X	X	DS-OR-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	OrCAD	X	X	X	X	X	X	DS-OR-STD-PC1	6.0.1			7/96	6.0	
	Synopsys		X	X	X	X	X	DS-SY-STD-xxx		5.2.1	5.2.1	7/96	5.20	Includes DS-401 v5.2
	Synopsys		X	X	X	X	X	DS-SY-ADV-xxx		7.00	7.00	na	na	Includes DS-401 v5.2
U	Viewlogic	X	X	X	X	X	X	DS-VL-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	Viewlogic	X	X	X	X	X	X	DS-VL-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.26.0	DA1 platform remains at v6.0
	Viewlogic	X	X	X	X	X	X	DS-VL-ADV-xxx	7.00	7.00	7.00	na	na	
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-BAS-PC1	6.0.1			7/96	6.0	Currently updating in-warranty cust. w/WVO
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-STD-PC1	6.0.1			7/96	6.0	Currently updating in-warranty cust. w/WVO
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-EXT-PC1	6.0.1			7/96	6.0	Currently updating in-warranty cust. w/WVO
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-ADV-PC1	7.00			na	na	
U	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-BAS-xxx	6.0.1			7/96	na	Customer w/v6.0 will receive v6.0.1 update
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	Includes 502/550/380
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-ADV-xxx	7.00	7.00	7.00	na	na	Includes 502/550/380 & Foundry
	Foundation Series	X	X	X	X	X	X	DS-FND-BAS-PC1	6.0.2			2/97	6.0.1	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-BSV-PC1	6.0.2			2/97	6.0.1	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STD-PC1	6.0.2			2/97	6.0.1	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STV-PC1	6.0.2			2/97	6.0.1	Includes support for XC4000E and XC9500
	LogiCore-PCI Slave			X				LC-DI-PCIS-C	1.10	1.10	1.10	na	na	Requires signed license agreement
	LogiCore-PCI Master			X				LC-DI-PCIM-C	1.10	1.10	1.10	na	na	Requires signed license agreement
	Evaluation	X	X	X	X	X	X	DS-EVAL-XXX-C	2.00	2.00	2.00	4/96	01/04	PC, Sun, HP kits with v5.2.1 and v6.0.1

KEY: *N=New Product E= Engineering software for in-warranty users by request only U= Update by request only * = Check BBS or FTP site for most current revision of EZTAG programming software..*

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