ACS NEWSLETTER

MEMORY ISSUE

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MEMBERSHIP

A letter about the ACS in the January IEEE Spectrum (page 129) has brought a fresh flow of inquiries about membership. The ACS now has members in 20 states, plus Canada, Italy and Switzerland.

WHAT TO DO WITH CORES OF UNKNOWN ORIGIN, by Sal Zuccaro

(Sal has been in memory design for 10 years, and has patents in core-diode logic.)

The used and surplus planes I've seen on the market are real antiques. I tested one originally made by Univac and found the switching time to be about two microseconds. A memory using this 80-mil core wouldn't be able to go faster than a five-microsecond cycle time. The size also would be excessively large.

There are several possible reasons for core planes being in the reject bin. One is that too many cores in the matrix need to be replaced. Another is that too many were replaced to pass the quality-control requirements of some given project. One more is trouble in the manufacturing process where the magnet wires are corroding for some reason. In like manner, a batch of cores could be too weak or brittle and thus subject to breakage.

Sometimes a bunch of cores will have a shifting loop; that is, they have a magnetic bias. Cores in this category used to get well into production before someone discovered the defect. Mechanical damage, such as lifted pads, etc., is a frequent cause for rejects.

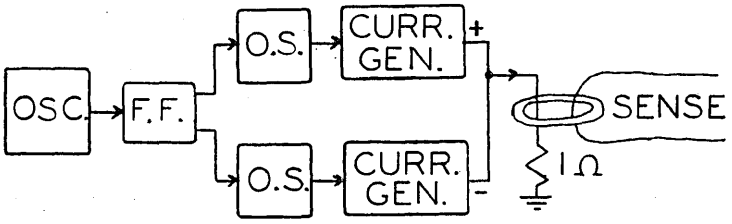
Happily, however, the reject bin also gets good usable frames, from several causes.

Because every computer manufacturer uses a different size memory with any of a number of different cores, any event that stops a large production run in the middle, puts good matrixes into the scrap bin. Nobody wants anybody else's design.

Cores are not going out of style; in fact, the demand is increasing. As for speed, our fast cores are turning over in 75 to 80 nanoseconds. Down in this region, the transition time of the signal along a wire is quite significant. [In one nanosecond, a pulse travels along some 9 inches of wire.]

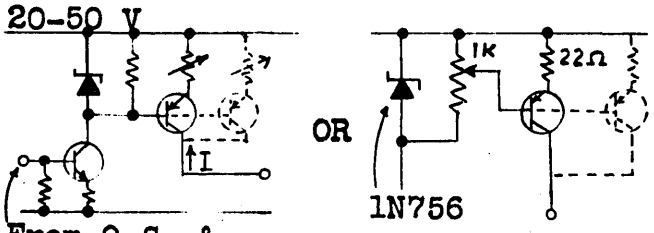
Here is an outline of a few steps to take with a core of unknown origin. You need a bidirectional constant current source, so you can turn the core first in one direction and then in the other.

The simplest setup would be:

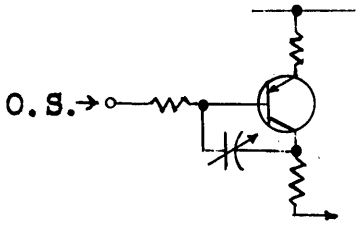


The amplitude of the current is monitored across the one-ohm resistor with an oscilloscope.

Some of the simplest forms of current generators are shown at the top of the next page. Parallel the output transistors as needed to get the required current.

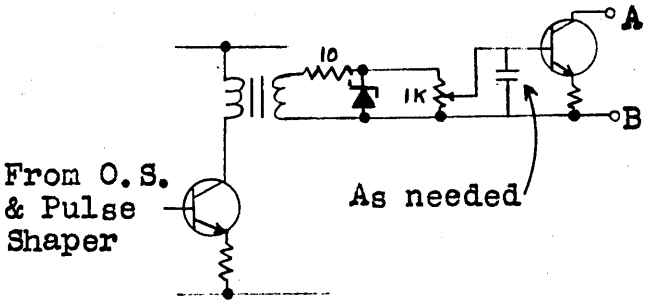


The pulse shaper can be just a Miller circuit:



For the negative, just replace NPN's with PNP's, and invert voltages.

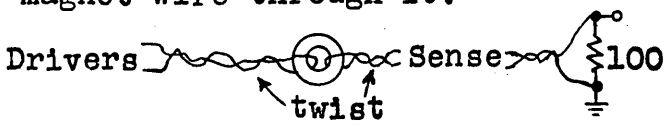
A little simpler system is:



This circuit has the advantage that it can pass a constant current from either the positive or negative voltages. For positive, A goes to a positive voltage and B is the output. For negative, B goes to a negative and A is the output. Any number can be connected to the same output terminal.

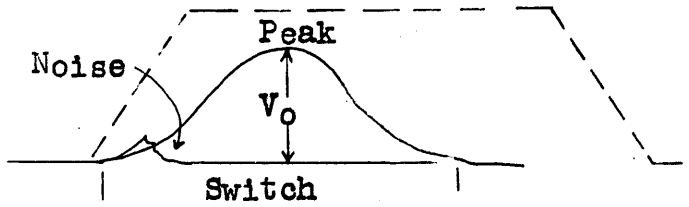
Pulse widths should be around five microseconds. Rise and fall times, around 0.2 microseconds.

To check out a core, put a small magnet wire through it:



This can be done even while it's in the matrix.

Set one pulse around one amp, and sync the scope to the beginning of this pulse. Now, starting at near-zero current, advance the other current until an output is just ready to form on the sense line. This should be the knee. A turn-over signal looks like:



The value of current which, when increased, produces an output (first appearing at the noise position), is the value of the knee.

This, divided by 0.6, should be equal to the maximum current needed to operate the core. This current divided by 2 is what goes down the X and Y lines. A core that has a knee lower than 0.6 is rather shaky. Some have knees much higher. In such a case the second pulse, called the write pulse, is increased to the point where the size of the output signal does not increase.

If you compare this value with the knee, you will get the true value of the disturb ratio.

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Another member, Jon Lax, stresses the need to go to 50- and 30-mil cores. This is because, although 80-mil cores are inexpensive, they are more trouble than they are worth, considering size, heat and drive currents.

Jon says that 80-mil cores take about three times the space, twice the current and about 2½ times the cooling as 50- and 30-mil cores.

Also, they are about half as fast. What with the new, very fast logic available, and trends toward miniaturization and the least upkeep possible, it is possible that you can sacrifice certain parts of the design rather than save a few dollars by using the cheaper planes. It all depends on how you design your machine.

Jon is president of a company, made up of high-school seniors, that sells cores, planes, stacks and magnetic-tape loops, to help finance the computer they're building. The cores sell for $10 to $80 per thousand, up to 10,000, and for $10 to $40 per thousand over 10,000. IBM-style buffer planes, 160 cores each, are sold at cost, $8.50 each. For details:

Jonathan R. Lax, President
The Information Organization
121 Gill Road
Haddonfield, New Jersey 08033

Jon figures that the cost of a core memory ranges from 15¢ to 90¢ a bit, depending on the ingenuity of the designer. The big difference is whether you use transistor or core sensing. The best source of schematics is textbooks, such as "Solid State Magnetic & Dielectric Devices" by Katz and "Information Storage and Retrieval" by Becker and Hayes, both published by Wiley.

The best source of cores is the manufacturers, says Jon. However, if anyone is willing to forego perfect specs, his company can provide cores from their revolving stock of rejects which they obtain from various of the larger houses. Many who do not need the ultimate in uniformity have been able to use them in the past, he adds.

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Pete Showman says that the amount of sophistication needed in a core-memory system seems to depend strongly on the physical size of the memory stack and on the threshold current of the cores. If the memory is small, diode decoding with drivers at each end of the line can be used. Some useful articles on such systems are "Designing a Small Core Memory ..., " by Jimerson, in Solid State Design, April 1964, pages 31-34, a word-select system with partial driver schematics; "A Versatile Magnetic Core Store Driving and Detection System," by J.A. Borrie, Electronic Engineering (British), Jan. 1963, pages 28-31.

When a core stack is big enough to have reflection problems, things get messy. Such memories must be treated as transmission lines, which 1) makes bidirectional drive harder, and 2) means large driver voltage swing: since Z_o is 100 ohms or so, and the half select current for typical surplus cores is $\geqslant \pm 600$ ma, ± 60 volts are required. Transistors that can handle that much power in 100 nsec are far out of the amateur's price range. The best solution Pete has seen is the load-sharing matrix switch. This multi-turn transformer array allows several (10, for example) smaller transistors to combine their outputs, and to send the pulse to any of several (16, for example) output lines. An article with good references is "Magnetic Core Access Switches," by Minnick and Haynes, EC-11 IRE Trans., June 1962, pp 352-368. The articles referenced are mainly mathematical theory, not schematics, but are useful if given a little study. Although the matrix switch is expensive, it can reduce overall system cost, since epoxy-cased transistors like the 2N3643 can be used as drivers.

Pete isn't sure where the dividing line between "large" and "small" memories is. The only way to find out is to try a diode-select system

and see if errors occur, he says, adding that a wrong guess could be expensive.

Pete estimates the cost of the electronics for a 16K by 13-bit memory using a load-sharing matrix to be about $800, or about 0.4¢ per bit. The stack is extra, of course. Because cost increases slowly with the number of bits, a 4K system would probably cost $500 or so. A very small memory gets simpler, but diodes with the required rating might be fairly expensive, too.

There are several articles on the gory details of sense-amplifier design, but Pete is not convinced that all the trouble is necessary in coincident-current systems (word-select memories evidently have greater noise problems). So far Pete has had good results with a well-balanced differential amplifier.

In a previous letter, Pete said: In the real world, drum and disk memories are of course the cheapest, but hard to fix if damaged, and hard to find in good condition. Old core planes seem to be numerous, but about six identical ones is the practical minimum for an efficient stack. I estimate minimum driver costs at $1.35 per driver, and sense amplifiers at $3-5. Thus a 1024 by 13-bit memory would be $160, or an effective 8192 by 2 by 13 bits would be $425, both excluding cores and decoding logic.

COMMENTS, ANYONE?

A few comments have been received, all saying they like the ACS Newsletter. Nice to get that kind, but more helpful would be comments on what you don't like about the Newsletter. What should there be more of, or less of?

STANDARD AMATEUR COMPUTER KIT

Amateur computer builders are now much like the early radio amateurs. There's a lot of home-brew equipment, much patchwork, and most commercial stuff is just too expensive.

The ACS can help advance the state of the amateur computer art by designing a standard amateur computer, or at least setting up the specs for one. Although the mere idea of a standard computer makes the true-blue home-brew types shudder, the fact is that amateur radio would not be where it is today without the kits and the off-the-shelf equipment available.

For those who don't believe in conformity, the computer kit can be a jumping-off place, a basic machine on which to build their own variations and special add-ons.

I propose a basic philosophy for the standard machine: it should be designed on the "bit-slice" principle, so that the basic kit can be bought with a minimum word length. Then, as the builder can afford, he buys bit-units, each containing all the cards for adding one bit to the word length throughout the machine. A bare minimum of registers would be used in the bit-slice stages, with further registers to be added on later, one by one (if this is feasible).

Possible optional add-ons might include a printer, character generator, X-Y plotter, card punch, card reader, additional core memory, drum memory, maybe even a Teletype.

Many problems exist; here are some:

1. What is the minimum number of registers for it? Maximum?
2. What should be the price for the basic machine? $500 too much?
3. What should be the maximum word length? And the minimum?

4. What options should be made available for add-ons?
5. Should the basic machine have more than manual input and lamp output? If so, what?
6. Should the contents of all registers be visible on the console? Or should one set of lamps do for all?
7. For the stage after manual input and lamp output, is paper tape okay? Or should we go directly to tape? Or drum?
8. How much assembly work should the kit-builder have to do? Could he solder in the ICs without burning them up, or should sockets be used?

It may be possible to get some kit or IC manufacturer interested in putting the standard amateur computer kit (SACK for short) on the market, if there are enough prospective kit builders so he would not be left holding the bag.

Please give SACK some thought, and let me know what you think about it. A standard amateur computer will probably be on the market by 1970, whether or not we do anything about it. There's no reason why we can't steer the inevitable in the direction we think best.

BOOKS AND MAGAZINES

"Sense Amplifier Fits Any Memory," Electronics, Sept. 5, 1966, pages 89-94, by a Sylvania engineer. New general-purpose amplifier can be used with most coincident-current memories. Designed to be compatible with the Sylvania high-level (SUHL) logic family, for use with Sylvania's MSP-24 microcircuit computer (Electronics, Oct. 18, 1965, page 72).

(There are two models of this sense amplifier, the SA-10, with high fanout, and the SA-11, with a lower fanout. Prices are:

	1	25	100
SA-10	$35.90	28.60	24.20
SA-11	26.10	20.80	17.60

Not cheap, but neither is the SUHL line, in which the cheapest flip-flop costs $5.90 for 1 to 24. However, that's a 20-Mc J-K flip-flop.)

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"Linear Pulse Transformers in Core Memory Design," W.G. Rumble (Lockheed), Computer Design, Feb. 1967, pages 48 to 60.

Although pulse transformers are bulky and expensive, and are not amenable to IC techniques, there are some advantages. This survey article discusses the major design problems in four types of memory configurations, without going into the finer details of circuit design; 28 figures, no component values.

* * * * *

Small Computer Handbook, 544 pages, free from Digital Equipment Corp., 146 Main St., Maynard, Mass. 01754. Discusses in detail, from a user's viewpoint, the PDP-8, PDP-8/S and the LINC-8 (PDP-8 and LINC combination). Chapters on computer basics, programming, I/O devices, operation. Almost 100 pages on interface and installation, a variety of basic schematics illustrating programmed data transfers, data break transfers and digital logic circuits. Combines three separate, larger handbooks in one small, 5½ by 8 format. DEC describes it as a "sourcebook of basic computer technology for the computer user and the student."

COMPUTER SCHEMATICS

Build-it-yourself books on the LINC computer are available:

Vols. 1-11, $63. Manufacturing Description (wiring tables, parts list for DEC cards required, etc.)
Vol. 12, $12. Logic Diagrams and

The Amateur Computer Society is open to all who are interested in building and operating a digital computer that can at least perform automatic multiplication and division, or is of a comparative complexity.

For membership in the ACS, and a subscription of at least eight issues of the Newsletter, send $3 (or a check made out to me):

Stephen B. Gray
Amateur Computer Society
219 West 81 St
New York, N.Y. 10024

The Newsletter will appear about every two months.

Timing Diagrams. (This alone is not enough; you need the wiring tables, too.)

Vols. 13-14. Theory of Operation. (Not yet written).

Vol. 15, $8. Assembly and Test Procedures.

The set of 13 available volumes weights about 35 pounds, will be sent postage collect. Send your check to:

Norman Kinch
Computer Research Laboratory
Washington University
700 S. Euclid Avenue
St. Louis, Missouri 63110

LINC is a computer designed to control experiments and to collect and analyze data in biomedical and environmental science research. A single-address, fixed word length, parallel computer, using 12-bit binary arithmetic, LINC contains a crt display, an analog-to-digital converter, a relay register, and dual magnetic tapes (DECtapes, 3½-inch reels, transfer rate 6000 words a second). DEC combines LINC with a PDP-8, so the two share a 4096-word core memory. A LINC costs about $30,000 assembled. Parts can be bought from DEC: cards, cages.

INTEGRATED CIRCUITS IN QUANTITY

Pete Showman reports that only one ACS member has responded to his offer to take charge of buying ICs in quantity (Issue 2, page 5). However, by finding another purchaser outside the ACS, he was able to persuade Fairchild to give the quantity price on 2400 pieces. Pete hopes to place a second order around May.

Anyone interested in ordering at least 50 of the Fairchild RTL ICs, please write to

Peter S. Showman
403 School St.
Watertown, Mass. 02172

Pete notes that using ICs would allow a 2-Mc clock, and figures the cost at about $2.27-2.60 per stage of an "average" arithmetic register, depending on purchase quantities. (Pete's typical register can shift two ways and load in parallel from another register.)

PROBLEMS FOR THIS ISSUE

4-1. A member who bought a Skybolt computer welcomes any information available on this item, especially the core memory. Information sent to the ACS will be forwarded.

4-2. Another member could use a good solution to hardware floating point. Responses will be forwarded.

4-3. A member is looking for a supplier for used or rebuilt electric typewriters with electrical inputs for computer I/O use. Any help?

YOUR ANSWERS TO THESE PROBLEMS WILL APPEAR IN THE NEXT ISSUE. Please look through past issues for unsolved problems and send in your answers.

NEXT ISSUE will be about how and where to look up articles and books on computer subjects of interest to amateurs, including some sources you may not have heard of, such as depositories.

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