MASS CORE STORAGE

A multi-million bit ferrite core memory system is seen to fill the speed gap between the extremes of nanoseconds-per-access and milliseconds-per-average access.

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The recent installation of a Fabri-Tek MT mass core storage system at the Massachusetts Institute of Technology points up a significant development in computer memory usage techniques. Ten years ago, a capacity of several hundred thousand bits of high-speed main memory was sufficient for most computer systems. Neither hardware nor software was sophisticated enough that more capacity was economically feasible. During the past decade this has changed rapidly. First, the cost of basic storage elements has been reduced. Second, manufacturing and testing techniques and procedures have been improved greatly. Third, there has been an improvement in semiconductors and their cost is much lower. Fourth, new organizational innovations have been devised. Fifth, and probably most important, system designers and programmers have been demanding additional memory at an economical price.

The results of these demands are various. Planar thin-film and plated-wire memories show hope as the primary devices for very high-speed main memories. However, for small storage requirements, integrated circuits are making inroads. Moreover, the ever-present ferrite core is proving a worthwhile element even in the 500 nanosecond cycle time range of operation. High-speed memories are still quite costly when compared to the storage media used for the other extreme of the cost/speed spectrum where demands are for billions of bits at significantly lower costs. At this end of the spectrum, advanced drum and disc systems have been developed.

A third concern is with memories that accommodate the speed gap between the extremes of nanoseconds-per-access and milliseconds-per-average access. Here, Fabri-Tek foresaw a need in mid-1964. The industry had slow memories that were about 10^4 times cheaper than the fastest memories available; however, these devices had an average access time of 10^5 times slower. What was needed were capacities of up to 20 or 30 million bits of storage, operating at one quarter to half as fast as main memory, but at a sufficiently lower cost. Just what is this cost, and, is the economically-required cost of the device technically feasible? Fabri-Tek believed at that time that such a memory could be built and sold for two to three cents per bit and that a market existed at that price. Experience showed that the ferrite core was a satisfactory memory element and that production techniques were enough advanced to attain these goals. The development program at Fabri-Tek has proved this to be true. A 65,536 word by 20 bit prototype, operating at 5.5 microseconds per cycle, resulted from initial development efforts. Discrete components were used throughout the electronics and the stack was constructed of 30 mil O.D. ferrite cores. The memory was two-wire, 2½D in organization which proved to be economical to produce in very large arrays. The system was described in the April 1966 issue of *Computer Design*.

An order for a 262,144 word by 40 bit mass core store was received in the fall of 1965 and this memory is now installed and operational at MIT (see Fig. 1). During the acceptance testing period this memory was available to the customer 98.9 percent of the time (measured over a 30-day period). The full-cycle time of this memory is 2.75 microseconds. To meet the speed requirement, fast switching complementary transistor integrated circuits are used for a majority of the logic functions of the memory. Also, integrated circuits are used for the final sense amplifiers. All drive circuits consist of integrated circuit decoding inputs and discrete transistor high-current drivers.

This particular memory is designed to interface as an extension of main memory with Digital Equipment Corp.'s PDP-6 computer. However, the basic design of the memory is such that the interface is easily redesigned for use with other families of computers. The design of the MT series allows for several word capacity and word length configurations. Memories are available with word lengths from 20 to 120 bits and total bit capacities from 2.5 to 20 million.

Just what comparative advantages mass core storage has over other bulk storage devices is not entirely known as yet. The factors that are most evident are the absence of latency and addressability at either the word or byte level. However, what must really be considered is: What possible improvements (lower costs and faster, more efficient computer system operation) result from incorporating an intermediate speed memory with main memory and peripheral bulk

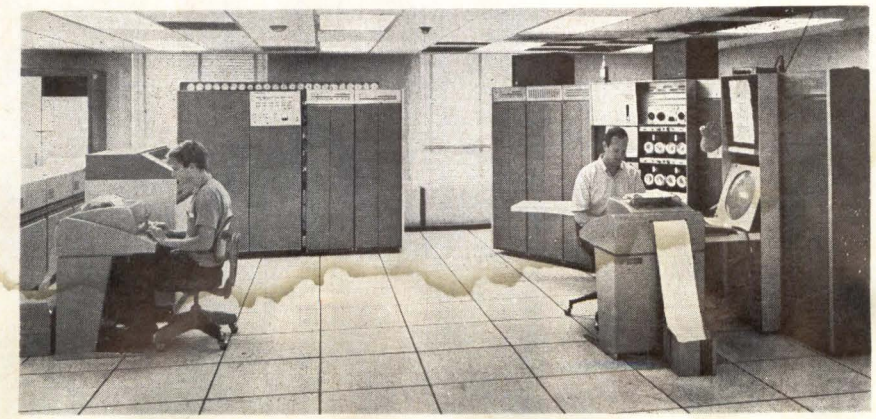


Fig. 1. Fabri-Tek's MT Mass Core Memory is shown in the left background as it relates to the total system configuration of the PDP-8 computer at M. I. T.

storage? According to computer systems designers, main memory need only be large enough to feed the central processor continually with instructions and data. Entwined in making an evaluation of how much memory is needed are considerations of the rate at which main memory is accessed (the execution rate) and how fast main memory information can be exchanged with peripheral memory information.

Computer systems designers are beginning to believe that the real answer for cost/speed/performance optimization is the creation of a memory hierarchy. Fabri-Tek feels its MT mass core memory system is the tool that allows the "tailoring" of this hierarchy for a number of large data processing configurations. The MT will eventually establish itself as a specific product, much the same as tape decks and rotating devices have. Systems designers will incorporate mass core storage in a number of ways resulting in the optimum solution for various data processing applications. Fabri-Tek's optimism is based on success in making cost reductions, and on the encouraging results of several experiments using mass core memories with two different large computer systems. These experiments project probable job time savings of from 30 percent to 60 percent in large job stack situations. The savings are largest when job priorities are well defined and when a large variety of data handling requirements exist. Job priority is dependent on frequency of use and urgency.

The mass core store can be used to extend the computing power of a large system. By relating the expected job loading profile to cost and speed, the configurations giving the desired performance can be determined. These configurations may use mass core storage for extension of main memory, block transfer interchange of main memory information, data collection and distribution for small remote processors, sharing of storage for multiple processors, or data buffering between main memory and peripheral bulk storage devices. Furthermore, one system may even use several combinations of these configurations. Several large time sharing computer installations have done this. A number of additional features are possible through logic design. For example, interleaving of several mass core memories and multiple-word read-out, and sophisticated priority schemes such as first-come-first-served, ordered priority, and automatic assignment of priority allow considerable increases in throughput. These features can be designed into the memory controller which may, in some cases, be only a re-design of an existing I/O controller.

Most advances in ferrite core and thin-film technology have been directed towards increasing the operational speed of memories. When the need arose for low per-bit costs, some of the same technological improvements could be employed. In addition, a new memory organization and very large magnetics module configurations were required to achieve the desired cost goals. However, these requirements result in operation at slower speeds because of increased back voltages, increased stack delays, and more sophisticated sense amplification and strobing. The design objective of the mass core storage system was to make the trade-off between memory cycle time and per-bit cost which would most satisfactorily fit the needs that are developing in the speed gap between very high-speed main memories and the very slow rotating peripheral memories.

Third generation medium-to-large computers have normally from one to 20 million bits of internal main storage. Cycle times are from 0.5 to 2.0 microseconds per cycle. Maximum module size is in the order of 65,536 words by 72 bits (approximately 5×10^6 bits). From these guidelines, a minimum mass core memory of 2.5×10^6 bits was chosen as the lower size limit. With cycle times of two to eight microseconds as a goal (a speed differential of one quarter to one half as fast as main storage units), the maximum low-cost single memory unit feasible was 20×10^6 bits (262,144 words by 80 bits). Units of this size appeared to fit the market that was developing. Since the initiation of this development program, the practical speed of operation of the resulting Fabri-Tek mass core memory has increased to two to three microseconds per cycle

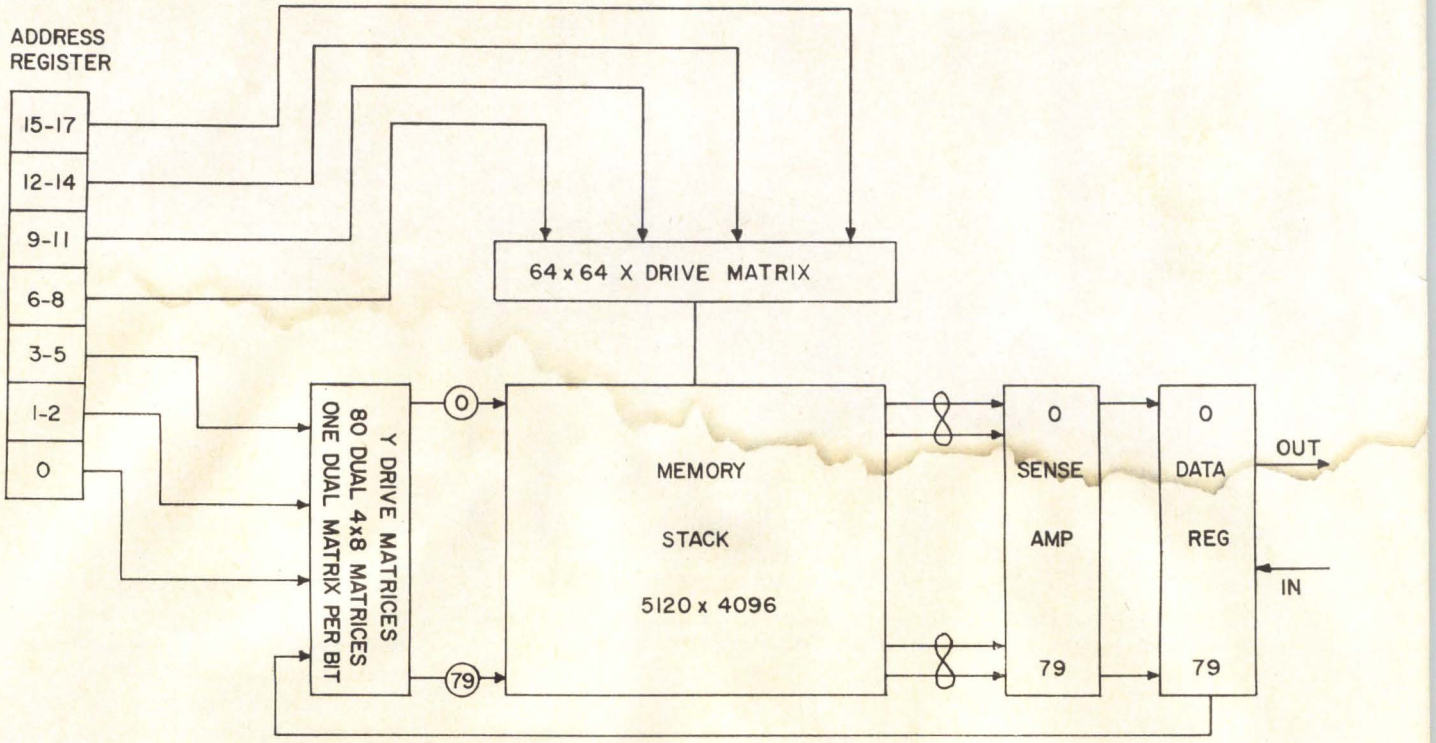


Fig. 2. Block diagram of Fabri-Tek's mass core memory.

TABLE 1

GENERAL SPECIFICATION OF THE MIT MASS CORE MEMORY

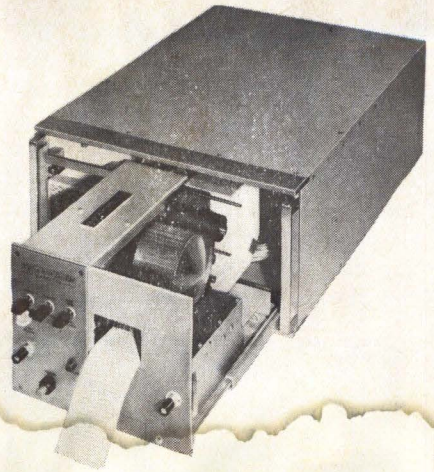
MEMORY TYPE	COINCIDENT CURRENT, FERRITE CORE 2½D SELECTION.
CAPACITY	262,144 WORDS AT 40 BITS PER WORD.
MEMORY CAPABILITIES	FULL CYCLE, RANDOM ACCESS DURING NORMAL OPERATION. SEQUENTIAL ACCESS DURING SELF-TEST.
MEMORY CYCLES	CLEAR-WRITE (FULL CYCLE LOAD) READ-RESTORE (FULL CYCLE UNLOAD) READ-PAUSE-WRITE (FULL CYCLE MODIFY)
CYCLE TIME	CLEAR-WRITE 2.75 USEC MAX. READ-RESTORE 2.75 USEC MAX. READ-PAUSE-WRITE 2.75 USEC PLUS MODIFY TIME.
ACCESS TIME	65% OF CYCLE TIME
OPERATING TEMPERATURE	60°F TO 90°F
STORAGE TEMPERATURE	−20°C TO +65°C
RELATIVE HUMIDITY	10 TO 90 % WITHOUT CONDENSATION
DIMENSIONS	LENGTH — 50 INCHES HEIGHT — 69¼ INCHES WIDTH — 26¼ INCHES
WEIGHT	1500 POUNDS

at no cost increase over original design goals.

From an analysis of four-wire coincident current memories, it can be shown that a majority of the costs are in the core stacks. At very large sizes (10^7 bits and above), core stacks account for about 80 percent of the total cost. It became evident that stack costs must be reduced to obtain any significant cost improvement. Thus, an organization which allows a trade-off between stack costs and circuitry costs would be beneficial.

Therefore, the Fabri-Tek mass core design approach, first developed in 1964, employs a two-wire stack design and a 2½D electronics organization capable of sensing, as well as current driving, on one of the two wires. A cost breakdown of a memory shows that four major criteria are involved, and the two-wire design using a large memory plane allows cost reductions in three of these criteria:

• Ferrite Core — since the memory speed is relaxed, core peaking time and switching time are not as critical. The elimination of the inhibiting function improves current margins and, hence, relaxes delta noise requirements. Each of the above-mentioned factors improves core yield and, hence, reduces core cost.



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812D-6	6	12	√	
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812D-10	10	12	√	
1200	12	20	√	
1600	16	20	√	
1600	16	30	√	
1600	16	40	√	
2200	22	20	√	
2200	22	30	√	
2200	22	40	√	
2200	22	20		√
3200	32	20	√	
3200	32	30	√	
3200	32	40	√	
3200	32	20		√

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• Wire Stringing and Terminating — because only two wires are used rather than four, and because the first two wires are easier to place than the last two, a reduction of greater than 50 percent is obtained in stringing cost. The use of large planes reduces the number of connections, or wire terminations, per bit. For example, a plane of 256 x 1280 would have about 10 connections per 1000 cores, but a 64 x 64 array would have about 62 per 1000. The economic advantage of large planes is evident.

• Test and Rework — testing can be automated quite readily. There is benefit with larger planes in reducing testing costs, because the time needed to install the plane in the tester, measured on a per-bit basis, is reduced. With larger planes, rework tends to be increased, somewhat. However, the simplicity of the two-wire scheme and the good margins obtained, as mentioned above, greatly alleviate the need for substantial rework. Memory system testing for 2½D organization is very similar to that of 3D memory systems.

• System Organization — the system organization used in Fabri-Tek's mass core memory allows for a simplified memory stack at some increase in circuitry cost. However, in a large-capacity memory, the circuitry cost-per-bit attained is still quite low. The principal reason for this is that the 2½D selection scheme allows the use of an efficient near-square stack array and yet takes advantage of the economies of coincident current read selection. This technique, combined with a sensing design which allows one sense amplifier and data register to serve up to 262,144 bits, makes the design of a 20-million bit memory practical. The block diagram shown in Fig. 2 is an organizational breakdown of a full-sized Fabri-Tek MT mass core memory. The memory contains 262,144 words of 80 bits. Table 1 lists the general specifications for the 262,144 word by 40 bit memory which is in operation at MIT.

This discussion does not cover all of the possible applications for a mass core memory. Fabri-Tek believes that computer system designers will be finding many applications and new configurations for which a mass core memory will prove to be the best storage device available.

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