

SIGDA NEWSLETTER

SPECIAL INTEREST GROUP ON DESIGN AUTOMATION

VOLUME 4 NUMBER 1 JANUARY 1974

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ADDRESSES

CHAIRMAN:

Charles E. Radke
IBM Corporation (B99/951)
P. O. Box 390
Poughkeepsie, New York 12602
(914) 485-7775

VICE-CHAIRMAN:

David W. Hightower
Bell Labs 2B312A
Holmdel, New Jersey 07733
(201) 949-6549

SECRETARY/TREASURER:

Lorna Capodanno
Bell Labs 2C169
Murray Hill, New Jersey 07974
(201) 582-6909

EDITOR:

Stephen P. Krosner
IBM Corporation (96N/002)
P. O. Box 1328
Boca Raton, Florida 33432
(305) 391-0500 (4052)

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Department of Elec. Eng.
University of Texas
Austin, Texas 78712
(512) 471-7365

Donald J. Humcke
Bell Labs 2C-318
Holmdel, New Jersey 07733
(201) 949-6253

Larry Margol
Micro Electronics Division
Rockwell Instruments
D/734-057
Box 3669
Anaheim, California 92803
(714) 632-8565

Charles W. Rose
Computing & Information Sci.
Case Western Reserve Univ.
Cleveland, Ohio 44106
(216) 368-2800

MEMBERSHIP

SIGDA dues are \$3.00 for ACM members and \$5.00 for non-ACM members. Checks should be made payable to the ACM and may be mailed to the SIGDA Secretary/Treasurer listed above, or to SIGDA, ACM Headquarters, 1133 Avenue of Americas, New York, N. Y. 10036. Please enclose your preferred mailing address and ACM Number (if ACM member).

SIG/SIC FUNCTIONS

Information processing comprises many fields, and continually evolves new subsectors. Within ACM these receive appropriate attention through Special Interest Groups (SIGs) and Special Interest Committees (SICs) that function as centralizing bodies for those of like technical interests ... arranging meetings, issuing bulletins, and acting as both repositories and clearing houses. The SIGs and SICs operate cohesively for the development and advancement of the group purposes, and optimal coordination with other activities. ACM members may, of course, join more than one special interest body. The existence of SIGs and SICs offers the individual member all the advantages of a homogeneous narrower-purpose group within a large cross-field society.

ACTIVITIES

- 1) Informal technical meetings at SJSS and FJCC.
- 2) Formal meeting during National ACM meeting + DA Workshop.
- 3) Joint sponsorship of annual Design Automation Workshop.
- 4) Quarterly newsletter.
- 5) Panel and/or technical sessions at other National meetings.

FIELD OF INTEREST OF SIGDA MEMBERS

Theoretic, analytic, and heuristic methods for:

- 1) performing design tasks,
- 2) assisting in design tasks,
- 3) optimizing designs through the use of computer techniques, algorithms and programs to:
 - 1) facilitate communications between designers and design tasks,
 - 2) provide design documentation,
 - 3) evaluate design through simulation,
 - 4) control manufacturing processes.

CHAIRMAN'S MESSAGE

Role of SIGDA

On Monday evening, June 25th at the 10th DA Workshop in Portland, Oregon, a joint meeting of the DA Technical Committee (IEEE) and SIGDA (ACM) was held. The theme of the meeting was "the role of professional societies in the design automation areas. Some thoughts which I presented during the meeting might be of value to all of the membership:

- R . Develop design automation as a discipline
- O . Provide direct and timely exchange of information on DA
- L . Provide a thriving organization which can serve as a focal point for those of similar interests
- E . Provide an environment for lively interaction with fellow DA professionals (not just other members)
- S . Provide interfaces with professional groups which relate to the DA interest
- . Provide members with awareness of related activities in DA

The employer gains through advancement of the individual in the profession. Further, the industrial community can gain through activities involving standards and educational programs.

There are certain constraints placed in each role. For example:

- . Develop DA as a discipline -- because of resource limitations, we must act as a catalyst. One could not expect to have the organization or resources to do otherwise.
- . Direct exchange of information. Companies treat DA as highly proprietary and, hence, there are often severe restrictions placed on what the members can and cannot publish, especially as concerns the timeliness of the information. We do have the direct exchange and should within these constraints strive to improve the timeliness of the exchange.

CHAIRMAN'S MESSAGE

One must remember that most professional groups depend strongly upon volunteers. These groups must operate in a catalyst mode.

The roles of "focal point and environment for lively interaction" are further restricted by a geographical barrier, as is the interfacing with other professional groups. Within ACM, one can organize local special interest groups. For example, in the Washington, D.C. area, there is a very active SIG on Graphics. However, today DA members do not appear to be distributed in terms of large clusters.

Finally, a very strong controlling factor must be added - that is, the level of interest and level of dedication of the members to have the organization play their roles.

What is the future direction with DA as a discipline and with a separate professional subgroup, in our case, SIGDA?

An array is often used to describe DA. Along one axis are the functions such as simulation, analysis, testing, data base, etc., and along the other axis are the applications areas, e. g., computer design, mechanical design, architecture, aerospace, etc. We find our backgrounds quite diverse. It might be Engineering in a particular field, programming or computer science, mathematics, architects, etc.

Today we see application areas. We do not have a distinct and separable discipline. I feel we must work toward developing DA as a discipline or we have no professional society. I predict this will come to pass. The differences in DA systems independent of application modules will continue to disappear.

My crystal ball is a little cloudy, however, if primitives which are used in in design are sufficiently reduced, the programs themselves and even design languages can merge. We have seen this in the merging of Engineering disciplines and in DA systems to handle flow type problems. However, we certainly are bounded by the fact that the application areas are so prominent.

Because of this boundary, industrial users treat their DA activity as a very proprietary area. Therefore, the degree to which communication can take place is restricted. I feel this present restriction is being relieved somewhat by several factors:

- The increase in the number of manufacturers of hardware which fit into a design center, e. g., graphic tablets, vector oriented terminals, raster displays, raster plotters, plotters, and digitizers. Attempts will be made to sell them as a system with programming support.

CHAIRMAN'S MESSAGE

- . The increase in the number of areas (applications) utilizing terminals, computers, and program in their design process. Hence, the number of individuals in the DA area will increase.
- . The tendency to integrate specific functions into a total system and, hence, make the application more general. There will then be less reflection on the specific application.
- . The tendency to include more function in the system, including an output to manufacturing. Hence, a broader distribution of the system takes place.
- . Finally, certain manufacturers will want to publicize a job, DA system, well done.

I claim, therefore, that the boundaries which now separate the applications will decrease and are, in fact, somewhat artificial. They exist because we have been too narrow and not general enough. Universities have not developed appropriate generalizations. Also, we have not felt that we could gain enough by cross communications with other application groups.

Within DA, regardless of application, the objectives are the same: "to reduce the time from product specification to delivery to the builder of the product at a reduced cost with assured performance".

Finally, I am convinced that the professional organization, at least SIGDA, will grow and the relationship of SIGDA with other groups of common or overlapping interest will be strengthened.

Briefly, again the six roles are:

- . Develop discipline of DA
- . Direct and timely exchange of information
- . Provide a thriving organization to serve as focal point
- . Provide an environment for lively interaction
- . Provide interfaces with other professional groups
- . Provide members with awareness of related activities

CHAIRMAN'S MESSAGE

The members gain directly if the professional organization is able to fulfill its roles. "One gets out of the organization what one puts into it" is valid.

Although the three dollars to SIGDA constitutes an initial effort, the real effort required is your personal involvement.

Dr. Harlow Freitag, Chairman of the DA Technical Committee of IEEE, also presented his views on the topic. A lively discussion followed with a large percentage of the almost eighty people participating. If I may generalize, I netted out three major points raised in the discussions:

- 1) Why are there two (or more) DA groups and computer groups in general? How can they work together better and closer? What are their differences?
- 2) Definitely there is a need for a professional society or sub-group in the area of design automation or if you prefer, computer applications in the area of Engineering design.
- 3) We should include various disciplines in the SIGDA Newsletter and workshops, not just computer design. Further, the newsletter should be published on a set schedule and all should be encouraged to make it the focal point for communications in the DA area.

Your comments and inputs would be appreciated.

C. E. Radke
Chairman, SIGDA

CER/ca

SPECIAL NOTICE:

INFORMAL MEETING AT NCC (NATIONAL COMPUTER CONFERENCE) MAY 6 - 10, 1974

Subject for discussion; providing flexibility in DA systems to allow for changing technologies.

For more information; check in the ACM Communications of the ACM, check ACM Meeting Schedules at the NCC, or contact Dave Hightower (see inside cover for address).

STANDARDS

During the 1973 DA Workshop, the subject of standards was brought up several times in relationship to DA. Bob Dunn, present Chairman of SIGGRAPH, was also in attendance at the workshop and indicated the needs for standards in the area of graphics (e. g. , hardware interfaces, data formats, and application/command language). Sergio Bernstein, at the software session, stressed the need for portability of application modules. Others expressed concern about information provided for input to logic delay simulations and for delay calculations. Concern was also expressed concerning standardized design languages and package terminology.

Within ACM, there is a standing committee on standards:

J. A. N. Lee
University of Massachusetts
Department of Computer Sciences
Amherst, Massachusetts 01002
(413) 545-2744

ACM representatives on the American National Standards Group of interest to SIGDA are as follows:

X-3, Computers and Information Processing
J. A. N. Lee (principal)

Y-32, Graphic Symbols and Designations
P. G. Skelly (principal)
Honeywell Information Systems, Inc.
13430 North Black Canyon
Phoenix, Arizona 85029
(602) 993-3000

I have put one person in contact with one of the committees. SIGGRAPH has appointed several members to assist ACM and review those standards which affect graphics (one person hardware interface, one person software).

Unless I receive additional input concerning standards relative to DA, I don't intend at this time to take further action. I do request that if you do have standard concerns, that you let me know.

C. E. Radke

CER/ca

OBJECTIVES OF THE SIGDA TECHNICAL COMMITTEE

One of the current objectives of the SIGDA Technical Committee is to increase the activity of SIGDA in all areas of Design Automation. We would like to act as a platform for the exchange of ideas on Design Automation in any field where a computer program is used as a design tool. For example, in such fields as ship and highway design.

To meet that objective we presently are planning technical sessions at the 1974 ACM conference to cover broad areas of interest. One of these will be devoted to DA at the university, and the other will be on the Total Data Base concept. We hope these topics will serve the objective of widening the traditional meaning of design automation which, heretofore has meant design of circuits.

We would also like to have a technical session at the next National Computer Conference. A possible topic would be "New Applications of Design Automation."

Another goal of the Technical Committee is to develop a comprehensive bibliography of DA literature. To that end, starting with the next issue of the SIGDA Newsletter, we will begin a series of bibliographies of articles and books related to Design Automation. The bibliography to appear in the next issue is entitled "Algorithms for Shortest Path, Shortest Spanning Tree, and Related Circuit Routing Problems (1957-1973)" and was prepared by A. R. Pierce at Bell Labs. Other bibliographies will follow. To keep our bibliographies current we strongly suggest that if you run across an interesting article related to Design Automation, please drop Steve Krosner a card with the necessary information on it. If you have ever needed to know if an idea has been published, you know the value of a complete bibliography. If the members of SIGDA will help we can develop a complete bibliography that will be of great value to anyone working in the field.

Another goal of the Technical Committee is to strengthen the technical content of the SIGDA Newsletter. In addition to bibliographies, the newsletter needs current technical papers. We understand the problems of having papers cleared by your company. The feeling seems to be that if an author goes to the trouble of getting a paper cleared, then he might as well send it to a major publication. However, the author's ideas may be sound but either not fully

developed or too narrow in scope to warrant appearing in a major publication. In this case he should send the paper to Steve Krosner, and when it is printed he will find out if the ideas are sound when he hears from SIGDA Newsletter readers.

Besides being a medium for publishing papers, the SIGDA Newsletter can serve as a sounding board for ideas that the author would like reactions to. Just a note or abstract could be enough to provoke substantive discussions with people in other companies interested in similar problems. We understand the proprietary nature of the work done in Design Automation and are not advising you to violate company proprietary policies but we are suggesting that if you can clear up any proprietary problems, then you will benefit from the exchange of ideas that is certain to result from an informal presentation of ideas.

In summary, the Technical Committee would like to broaden the sphere of activity of the SIGDA and would like to encourage more participation on the part of the members by asking them to submit papers or ideas for publication, and to submit names of papers that should go into our bibliography.

I believe that with the cooperation of the SIGDA membership we can continue to improve the utility of SIGDA and can make the Newsletter into an important publication.

DAVID W. HIGHTOWER
Chairman
SIGDA Technical Committee

AUTOMATING THE DESIGN PROCESS

I highly recommend for reading a paper by Richard R. Heldenfels, NASA Langley Research Center (AIAA Paper No. 73-410) presented at the AIAA/ASME/SAE 14th Structures, Structural Dynamics, and Materials Conference, Williamsburg, Virginia, March 20-22, 1973. Note: AIAA (American Institute of Aeronautics and Astronautics), ASME (American Society of Mechanical Engineers), SAE (Society of Automotive Engineers). Abstract:

The design process of large aerospace vehicles is discussed, with particular emphasis on structural design. Problems with current procedures are identified. Then, the contributions possible from automating the design process (defined as the best combination of men and computers) are considered. Progress toward automated design in the aerospace and other communities is reviewed, including NASA studies of the potential development of Integrated Programs for Aerospace-Vehicle Design (IPAD). The need for and suggested directions of future research on the design process, both technical and social, are discussed. Although much progress has been made to exploit the computer in design, it is concluded that technology is available to begin using the computer to speed communications and management as well as calculations in the design process and thus build man-computer teams that can design better, faster and cheaper.

Consider for the thought for the quarter, one of Mr. Heldenfel's statements: "Providing greater depth of analysis sooner is one of the important potential contributions of automation".

C. E. Radke

CER/ca



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NOVEMBER 11-13, 1974 • COMMUNITY CONCOURSE

ASSOCIATION FOR COMPUTING MACHINERY

P. O. BOX 9366 • SAN DIEGO, CALIFORNIA 92109

Next year's annual conference takes place November 11 through 13 in beautiful San Diego, "The Unconventional City". Plans are being made right now to integrate a strong, balanced technical program with the many attractions of San Diego's recreational facilities and historical points of interest. An outstanding convention complex coupled with some of the best weather in Southern California (almost legendary) should contribute immeasurably to the success of the conference and comfort of the attendees.

Be sure to be on the lookout for the Call For Papers announcement which will appear in ACM Communications and other publications later this year. In the meantime, contact Dave Bulman, Technical Program Chairman, ACM '74, P. O. Box 9366, San Diego, California 92109 for further information about submitting papers.

San Diego abounds with excellent restaurants, serving food ranging from seafood and steaks to the mexican variety (ole!), and also offers a wide selection of entertainment. Located in the immediate vicinity are numerous computer centers, such as the Navy Electronics Laboratory, U. S. Customs, University of California at San Diego, General Dynamics/Convair, and Rohr, which offer the latest in technological advances.

Convention Headquarters will be located at the Sheraton-Airport, situated on Harbor Island on San Diego Bay.

So, why not enjoy yourself, relax a little, renew old acquaintances, meet some new friends, and participate in some stimulating technical sessions.

See you in San Diego for ACM '74!!

CALL FOR PAPERS - For SIGDA Session of ACM '74 (November 11-13, 1974), San Diego, California

SIGDA is planning to have two sessions at the ACM '74.

1) Data Based Systems for Design Support

Types of papers desired:

- . Data Based Systems used for Computer-Aided Design Support
- . Design Automation Systems

Organizer: C. E. Radke

2) Computer-Aided Design Development in the University

Types of papers desired:

- . Computer-Aided Design Activity in the University
- . Design Automation as a discipline in the University

Organizer: D. W. Hightower

Consult official call for papers or contact session organizers for information. Addresses for the session organizers may be found at the front of the Newsletter.

ON TIME SHARING SYSTEMS' PERFORMANCE...

Premise: "Evaluating the performance of a time sharing system is difficult."

Harry jumped up from his terminal, slammed the receiver back in its cradle after twenty unanswered rings, and stormed out of the office, cursing. Harry had been doing a lot of that recently, Joe thought. Well, a cup of coffee usually puts him back in a better humor...we'll see. Maybe that new time sharing service Harry raved about and started to use also went...no, it couldn't be. Could it really have gone bankrupt, too? And Harry there with that deadline? No wonder he was so angry. Oh well... we'll see...we'll see.

Joe dialed his time sharing company, hoping he could get some work done. "FRIENDLY T/S COMPANY AT YOUR SERVICE...PLEASE LOG IN." Ahhh... happiness is finding that your computer is up! Joe went to work.

Some time later, Harry walked back in, a long sheet of paper in one hand and a cup of coffee in the other. He seemed more pensive than irate now. "I wonder," he said. "I really wonder what in the name of 'down time' does it all mean, Joe. Is any of it MEANINGFUL?"

"What, Harry? That time sharing company gone bankrupt, or has the friendly phone company screwed up again?"

"Never mind that. I was thinking about response time...disk access time...memory cycle time...you know. What does it all mean, Joe? What

ON TIME SHARING SYSTEMS' PERFORMANCE

does all this stuff really MEAN?"

Joe could feel Harry's despair. He tried to find soothing words, but he knew he couldn't. Life is the way ~~it~~ **is**, and kind words sometimes do not apply, even if some can be found!

He took the paper from Harry's hand and looked it over. He pulled in a deep breath, sighed, and said, "I don't know, Harry. I really don't know. All I DO know is what these numbers come out to be. No more, no less. What they mean is not for me to say or to judge. I try to stick to the facts. God knows that's hard enough! The pundits and computer experts can come out and try to make a name for themselves, trying to tell us what it MEANS...but not me, buddy, not me. I just stick to the facts, Harry, and there they are. Take 'em or leave 'em. I'm not getting into any messy arguments with anybody! You wanted a quick evaluation of some time sharing systems, something quick and dirty which we could try while the salesman wasn't looking...some simple FORTRAN test which was sure to run on every machine. So here it is, Harry. It's a test. Just a simple test...so don't give me any of that 'meaningful' stuff!

"Really, Harry, could YOU come up with something MEANINGFUL in ten lines of code? Or even a hundred lines, for that matter? If the results depend on the time of day or how many users are on the system, I really can't help it. After all, it's REASONABLE to assume that we have to work during the day sometimes, and not only after six p.m.!

"So here it is, old buddy...here it is. I'll give it to you straight. Just the facts, the way I got them from every time sharing system I could

ON TIME SHARING SYSTEMS' PERFORMANCE...

lay my hands on. You tell ME what it means...what it REALLY means."

MORAL: "It is better to run a single test than to curse all time sharing systems."

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EPILOGUE:

The results presented may be strongly dependent on the choice of program, since each machine may use a different exponentiation algorithm.

Exponentiation was chosen since it was the easiest function to program in order to have a test which was "compute bound".

Thus, irate voices will be heard (hopefully...we shall get some feedback!) objecting to the validity of this "test" .

WE hope so! We want to encourage commentary on this, and other subjects. If we can find, determine, design, standardize, or otherwise come up with a simple test to check price/performance of a Time Sharing System, then our goal in writing this little note will have been reached--- let us hear from you, please.

Sergio Bernstein
Berne Electronics
28 Havilands Lane
White Plains, NY.
10605

Tel: 914 946-7950
=====

MACHINE TYPE :	WORD SIZE	CPU secs. Singl.Pr.	CPU secs. Doubl.Pr.	ELAPSED Minutes	Num.of Users:	COST for CPU Only	C O M M E N T S :
PDP-10	36	21.5	280.0	2.1/5.5	4/4	2.15/28.00	CPU Charges: 10¢ for 2K Core 23¢ for 20K Core
Sigma-7	32	27.0	46.0	1.0/2.25	5/5	2.70/4.60	
CDC-3300	48	39.0	--	0.8	???	4.68	Dual processor configuration
CDC-3500	48	30.0	--	0.6	6	4.50	
CDC-6400	60	33.5	--	2.33	29	6.70	
B - 5500	48	62.0	79.0	3.8/11.0	8	6.00/8.00	
U - 1108	36	17.5	60.0	? /?	???	4.50/16.00	
GE - 635	36	49.5	--	3.0	???	???	
IBM 360/67	32	29.3	44.4	1.0/2.25	30/30	11.00/16.50	

Notes: All 48-Bit machines specified use 24-Bits for integer words, 48-Bits for Real words, and upwards of 70-Bits for double precision real words.

The following FORTRAN Program was used for running time tests, after compilation and loading:

```

C      DOUBLE PRECISION A,B,C
C      ABOVE USED FOR DOUBLE PRECISION TIMINGS
C.
      A = 2.
      B = 3.
      READ(5,100) N
100    FORMAT(I6)
C
      DO 200 J = 1, N
      C =(A + J)**B
200    CONTINUE
      WRITE(6,300) C
300    FORMAT(1x,E20.5)
      STOP
      END

```

Note: The FORTRAN Device numbers
are changed for each system
when required.

A Bibliography For Computer Aided Interconnection And Placement

David C. Wilson and Robert J. Smith, II
Southern Methodist University
Dallas, Texas 75275

Introduction

This list emphasizes the area of digital design automation concerned with geographic placement of elements on or within a specific environment (e.g., flatpacks on a printed circuit board), and, to a certain extent, the routing of conductor paths which interconnect various points in the environment. Although similar problems are found in civil engineering, sociology, operations research and other disciplines, the accumulation of comprehensive bibliographies in these related fields was deemed impractical by the authors.

Since much of the recent routing and placement work has not been described in the open literature, readers are cautioned not to consider this list a reflection of current state-of-the-art in this field.

The list is intended to provide a comprehensive coverage of the routing and placement problems as related to the design of electronic equipment; complete listings for related fields were not accumulated, but an attempt was made to cite representative introductory sources in each of these disciplines.

Content

The bibliography was originally assembled for a research project in computer aided placement techniques. Additional entries were made as new material was discovered. The list of entries below is being maintained at Southern Methodist University in machine-readable form; the authors would appreciate receiving copies of past or future work which should be included in the bibliography, as well as citations which may have been overlooked.

Organization

The first section provides a classification of the works cited based on 12 categories. Each reference was assigned to one major and up to 3 minor areas; classification decisions reflect the evaluations made by the authors. Section two of the bibliography lists in numbered alphabetical order all references suitable for inclusion as of September 1973.

DESIGN AUTOMATION SURVEYS

35	36	373	375
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DESIGN AUTOMATION SYSTEMS GENERAL

29	32	37	47	53	83	87
167	170	226	227	243	251	252
254	280	295	302	306	327	334
347	375					

PRINTED CIRCUIT

10	87	88	100	131	151	155
170	226	227	295	327		

MICROCIRCUIT

7	95	224	251	252	256	264
295						

BACKPLANE

110

HISTORICAL

9	44	136	189	196	255
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BACKGROUND

GRAPH THEORY

1	8	21	49	82	86	126
129	139	152	167	176	178	242
250	322	384				

OPERATIONS RESEARCH TECHNIQUES

15	18	19	28	38	66	67
68	69	70	78	79	85	86
104	107	162	191	210	229	230
244	268	291				

WIRE ROUTING

GENERAL

0	1	7	8	29	35	36
37	39	53	72	88	95	100
110	125	131	139	151	152	155
165	167	178	184	195	225	232
239	243	247	252	256	259	264
269	281	283	284	295	298	306
314	319	333	334	337	338	339
344	347	368				

ORDERING OF WIRES

0	1	162	167
---	---	-----	-----

LAYERING

1	125	167	339
---	-----	-----	-----

MAZE RUNNING

0	5	10	72	110	125	165
171	232	258	259	269	276	284
314	368					

HEURISTICS

10	153	171	225	258	268
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TRAVELING SALESMAN

15	79	104	195	242
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MULTILAYER

262	338
-----	-----

ASSIGNMENT

GENERAL

2	7	28	29	32	35	36
37	39	53	64	65	81	88
92	95	100	111	128	129	141
142	151	154	155	181	184	206
207	213	219	224	228	231	234
243	252	257	260	267	272	279
285	286	290	295	333	334	342
343	344	347	348	350	352	354
358	360	365				

CLUSTERING

2	92	154	228	231	250	257
260	272	285	342	344	349	350
352	354					

MONTE CARLO

64	285
----	-----

MATHEMATICAL PROGRAMMING

38	39	128	365
----	----	-----	-----

VECTOR RELAXATION

141	348
-----	-----

SPACE PLANNING

2	33	234
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QUADRATIC ASSIGNMENT

82	129	142	229
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GRAPH THEORETIC

82	260	333	365
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TRANSPORTATION

28	66	68	69	70	107	142
191	206	267	279			

TRAVELING SALESMAN

18	162	210	244	267	291
----	-----	-----	-----	-----	-----

- ABEL, L.C.
ON THE ORDERING OF CONNECTIONS FOR AUTOMATIC WIRE ROUTING
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-21 (NOVEMBER 1972), PGS. 1227-1233
ALSO COORDINATED SCIENCE LABORATORY REPORT R-537, UNIVERSITY OF ILLINOIS,
URBANA, 1971
- 1 ABEL, L.C.
ON THE AUTOMATED LAYOUT OF MULTILAYER PLANAR WIRING AND A RELATED GRAPH
COLORING PROBLEM
ILLINOIS UNIVERSITY, AD 737151, JANUARY 1972, 159 PAGES
COORDINATED SCIENCE LABORATORY REPORT R-546, UNIVERSITY OF ILLINOIS, JANUARY
1972
 - 2 ADAMOWICZ, M. AND ALBANO, A.
A TWO-STAGE SOLUTION OF THE CUTTING-STOCK PROBLEM
PROCEEDINGS OF THE IFIPS, 1971, PGS. 1086-1091
 - 3 ADSHEAD, H.G.
OPTIMIZING AUTOMATIC TRACKING OF MULTILAYER BOARDS
AGARD CONFERENCE, COMPUTER AIDED DESIGN FOR ELECTRONIC CIRCUITS,
COPENHAGEN, MAY 1973
 - 4 AKERS, S.R.
SOME PROBLEMS AND TECHNIQUES OF AUTOMATIC WIRE LAYOUT
DIGEST OF THE FIRST ANNUAL IEEE COMPUTER CONFERENCE (SEPTEMBER, 1967),
PGS. 135-136.
 - 5 AKERS, S.R.
A MODIFICATION OF LEES PATH CONNECTION ALGORITHM
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME EC-16, NUMBER 1
(FEBRUARY 1967), PGS. 97-98
 - 6 AKERS, S.R.
ROUTING
CHAPTER 6, PGS. 283-333, IN DESIGN AUTOMATION OF DIGITAL SYSTEMS, M.A. BREUER,
EDITOR, PRENTICE HALL, ENGLEWOOD CLIFFS, N.J., 1972
 - 7 AKERS, S.R., GEYER, J.M., AND ROBERTS, D.L.
IC MASK LAYOUT WITH A SINGLE CONDUCTOR LAYER
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 22-25,
1970, SAN FRANCISCO, PGS. 7-16.
 - 8 AKERS, S.R., AND HADLOCK, F.O.
GRAPH THEORY MODELS OF ELECTRICAL NETWORKS AND THEIR MINIMUM CROSSOVER LAYOUTS
UNIVERSITY OF THE WEST INDIES CONFERENCE ON GRAPH THEORY AND COMPUTING,
JANUARY, 1969.
 - 9 ALTMAN, G.W., DECAMPO, L.A., AND WARBURTON, C.R.
AUTOMATION OF COMPUTER PANEL WIRING
TRANSACTIONS OF THE AIEE, VOLUME 79, PART 1 (MAY 1960), PGS. 118-125
 - 10 ARAMAKI, I., KAWABATA, T., AND ARIMOTO, K.
AUTOMATION OF ETCHING PATTERN LAYOUT
COMMUNICATIONS OF THE ACM, VOLUME 4, NUMBER 11 (NOVEMBER 1971), PGS. 720-730
 - 11 ARBABI, M. AND HOROWITZ, H.M.
TRANSPORTATION PROBLEM APPLICATION TO SCHEDULE MULTI-COMMODITIES WITH
PREDETERMINED PRIORITIES USING SHORTEST PATH TECHNIQUES
IBM TECHNICAL REPORT TR 48.67.002, GAITHERSBURG, MD., NOV. 28, 1967.
 - 12 AUSLANDER, L. AND TRENT, H.M.
ON THE TOPOLOGY OF PRINTED CIRCUITS
TRANSACTIONS OF THE IRE, VOLUME CT-8, NUMBER 4, 1959
 - 13 BEARDSLEY, C.W.
SPECIAL APPLICATIONS REPORT 1 COMPUTER AIDS FOR IC DESIGN, ARTWORK, AND MASK
GENERATION
IEEE SPECTRUM, SEPTEMBER 1971, PG. 63
 - 14 REELITZ, H.R., LINHARDT, R.J., AND MULLER, H.S.
PARTITIONING FOR LARGE SCALE INTEGRATION
IN PROCEEDINGS OF THE 1967 INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE,
FEBRUARY 12-16, 1967, PGS. 50-51

- 15 BELLMAN, R.
ON A ROUTING PROBLEM
QUARTERLY JOURNAL OF APPLIED MATHEMATICS, VOLUME 16, NUMBER 1 (APRIL 1958),
PGS. 87-90
- 16 BELLMAN, R.E. AND DREYFUS, S.
APPLIED DYNAMIC PROGRAMMING
PRINCETON UNIVERSITY PRESS, PRINCETON, N.J., 1962, PGS. 229-231
- 17 BELLMAN, R.E. AND KALABA, R.
ON K-TH BEST POLICIES
JOURNAL OF THE SIAM, VOLUME 8 (1960), PGS. 582-588
- 18 BELLMORE, M., AND MALONE, J.C.
PATHOLOGY OF TRAVELING SALESMAN ALGORITHMS
JOHN HOPKINS REPORT, 1969
- 19 BELLMORE, M. AND NEMHAUSER, G.L.
THE TRAVELING SALESMAN PROBLEM : A SURVEY
JOURNAL OF OPERATIONS RESEARCH, VOLUME 16 (1968), PGS. 538-558
- 20 RENNIER, D.J., AND O DONNELL, C.K.
PRINTED CIRCUITS ETCHED WIRING GUIDE
W.R.E. TECHNICAL MEMORANDUM EC3, 1963.
- 21 BERGE, C.
THE THEORY OF GRAPHS AND ITS APPLICATIONS
JOHN WILEY AND SONS, NEW YORK, NEW YORK, 1962
- 22 BERGE, C. AND GHOUILA-HOURI, A.
PROGRAMMING GAMES AND TRANSPORTATION NETWORKS
JOHN WILEY AND SONS, NEW YORK, NEW YORK, 1962, PG. 179
- 23 RILDE, O. AND KRARUP, J.
A MODIFIED ALGORITHM FOR SHORTEST PATHS
TRA, VOLUME 8 (1969), PGS. 231-241
- 24 RINDSCHEDLER, A.E. AND MOORE, J.M.
OPTIMUM LOCATION OF NEW MACHINES IN EXISTING PLANT LAYOUTS
JOURNAL OF INDUSTRIAL ENGINEERING, VOLUME 12 (1961), PGS. 41-48
- 25 RITTMER, B. AND ULRICH, U.
A METHOD FOR IMPROVING THE LOCATION OF CONNECTING PATHS FOR CIRCUIT CARD
WIRING
REPORT FROM THE THOMAS BEDE FOUNDATION
IEEE COMPUTER SOCIETY REPOSITORY R-68-128
- 26 ROESCH, F.T.
PROPERTIES OF THE DISTANCE MATRIX OF A TREE
QUARTERLY JOURNAL OF APPLIED MATHEMATICS, VOLUME 26 (1969), PGS. 607-609
- 27 RONNER, R.E.
ON SOME CLUSTERING TECHNIQUES
IBM JOURNAL OF RESEARCH AND DEVELOPMENT, VOLUME 8, PAGES 22-32
- 28 ROUGEOTIS, F. AND LASSALE, J.
AN EXTENSION OF THE MUNKRES ALGORITHM FOR THE ASSIGNMENT PROBLEM TO
RECTANGULAR MATRICES
COMMUNICATIONS OF THE ACM, VOLUME 14, NUMBER 12 (DECEMBER 1971), PGS. 802-806
- 29 ROWDON, E.
DIGITAL NETWORK DESIGN AIDS-AN INTEGRATED APPROACH
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 22-25,
1970, SAN FRANCISCO, PGS. 220-225
- 30 ROWDON, E.K. AND BRUCE, R.
COMPUTER AIDS FOR DIGITAL NETWORK DESIGN : INTERIM REPORT
COLLINS RADIO COMPANY, WORKING PAPER NO. 954, SEPTEMBER, 1967, 45 PAGES
- 31 ROWICK, J.W. ET AL
NEW HELP FOR PRINTED CIRCUIT DESIGNERS
TELESIS, MAY 1970, PGS. 249-254

- 32 BRACCHI, G.
ON THE GENERATION OF SYSTEM PARTITIONS FOR LARGE SCALE INTEGRATION
IEEE TRANSACTIONS ON SYSTEMS, MAN, AND CYBERNETICS, VOLUME SMC1, OCTOBER 1971,
PGS. 325-330
- 33 BRACCHI, G. AND FERRARI, D.
A LANGUAGE FOR TREATING GEOMETRICAL PATTERNS IN A TWO DIMENSIONAL SPACE
COMMUNICATIONS OF THE ACM, JANUARY, 1971, PGS. 26-32
- 34 BRECKON, T.J.
DETERMINING PARTITION ELEMENTS WITH FEEDBACK CONSTRAINTS
NAVAL POSTGRADUATE SCHOOL, AD 709910, JUNE 1970, 76 PAGES
- 35 BREUER, M.A.
DESIGN AUTOMATION OF DIGITAL SYSTEMS, VOLUME 1 THEORY AND TECHNIQUES
PRENTICE HALL, ENGLEWOOD CLIFFS, N.J., 1972
- 36 BREUER, M.A.
GENERAL SURVEY OF DESIGN AUTOMATION OF DIGITAL COMPUTERS
PROCEEDINGS OF THE IEEE, VOLUME 54, NUMBER 12 (DECEMBER 1966), PGS. 1708-1721
- 37 BREUER, M.A.
RECENT DEVELOPMENTS IN DESIGN AUTOMATION
COMPUTER, MAY-JUNE 1972, PGS. 23-25
- 38 BREUER, M.A.
THE APPLICATION OF INTEGER PROGRAMMING IN DESIGN AUTOMATION
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1966
- 39 BREUER, M.A.
THE FORMULATION OF SOME ALLOCATION AND CONNECTION PROBLEMS AS INTEGER PROGRAMS
NAVAL RESEARCH LOGISTICS QUARTERLY, VOLUME 13 (MARCH 1966), PGS. 83-95
- 40 BROFFITT, J.D., MORGAN, H.L., AND SODEN, J.V.
ON SOME CLUSTERING TECHNIQUES FOR INFORMATION RETRIEVAL
REPORT ISR-11 TO THE NATIONAL SCIENCE FOUNDATION, SECTION IX, CORNELL
UNIVERSITY, JUNE 1966
- 41 BROWN, E.A.
GENERATION OF ALL SHORTEST PATHS OF A DIRECTED NETWORK
IBM RESEARCH REPORT RC-283, YORKTOWN HEIGHTS, N.Y., JULY 7, 1960
- 42 BROWN, F.M.
THE DETERMINATION OF THE MAXIMUM COMPATIBILITY CLASSES
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME 19 (1970), PG. 459
- 43 BROWN, J.A., CESA, L.J., AND SAWTICKI, J.J.
DESIGN AUTOMATION AND THE WRAP SYSTEM
PROCEEDINGS OF THE DESIGN AUTOMATION WORKSHOP, 1968, PGS. 19-1 TO 19-30
- 44 BROWN, R.R. AND PUTNAM, G.F.
THE AUTOMATION OF TOPOLOGICAL LAYOUT
AIEE TRANSACTIONS, PART 1, 1962, PGS. 136-139
- 45 BRUNO, J., STEIGLITZ, K., AND WEINBERG, L.
A NEW PLANARITY TEST BASED ON 3-CONNECTIVITY
IEEE TRANSACTIONS ON CIRCUIT THEORY, VOLUME 17 (1970), PGS. 197-206
- 46 BRYANT, P.R.
THE ALGEBRA AND TOPOLOGY OF ELECTRICAL NETWORKS
PROCEEDINGS OF THE IEEE, VOLUME 61, 8, PAGES 215-229, 1961
- 47 RUELOW, F.K., HARTMAN, F.B., WILLETTE, E.L., AND ZASIO, J.J.
A CIRCUIT PACKAGING MODEL FOR HIGH SPEED COMPUTER TECHNOLOGY
IBM JOURNAL OF RESEARCH AND DEVELOPMENT, VOLUME 7 (JULY 1963), PGS. 182-189
- 48 BURNS, J.A. AND EFTANG, G.
A NEW RELIABLE PRINTED WIRING BOARD THROUGH CONNECTION
IN ADVANCES IN ELECTRONIC CIRCUIT PACKAGING, VOLUME 6, ROGERS PUBLICATIONS,
1965, PGS. 6-1 TO 6-18

- 49 RUSACKER, R.G. AND SATTY, T.L.
FINITE GRAPHS AND NETWORKS
MCGRAW-HILL BOOK COMPANY, NEW YORK, 1965.
- 50 RUTAS, L.F.
A DIRECTIONALLY ORIENTED SHORTEST PATH ALGORITHM
TRANSPORTATION RESEARCH, VOLUME 5 (1968), PGS. 253-263
- 51 CALDWELL, T.
ON FINDING MINIMUM ROUTES IN A NETWORK WITH TURN PENALTIES
COMMUNICATIONS OF THE ACM, VOLUME 4 (1961), PGS. 107-108
- 52 CAMPAGNA, R.
COMPUTER LAYOUT OF DENSE PRINTED CIRCUIT BOARDS
ELECTRONICS, VOLUME 44 (MAY 10 1971), PGS. 76-79
- 53 CASE, P.W., GRAFF, H.H., GRIFFITH, L.E., LECLERCQ, A.P., MURLEY, W.B., AND
SPENCE, T.M.
SOLID LOGIC DESIGN AUTOMATION FOR IBM SYSTEM/360
IBM JOURNAL OF RESEARCH AND DEVELOPMENT, VOLUME 8 (APRIL, 1964), PGS. 127-140
- 54 CHAN, K.H.
ARTWORK PRODUCTION FOR MULTI-LAYER PRINTED CIRCUIT BOARDS BY COMPUTER
COMPUTER AIDED DESIGN, VOLUME 2 (1970), PGS. 31-32
- 55 CHARNES, A. AND COOPER, W.W.
THE STEPPING STONE METHOD OF EXPLAINING LINEAR PROGRAMMING CALCULATIONS IN
TRANSPORTATION PROBLEMS
MANAGEMENT SCIENCE, VOLUME 1 (1954), PGS. 49-69
- 56 CHARNEY, H.R. AND PLATO, D.L.
EFFICIENT PARTITIONING OF COMPONENTS
PROCEEDINGS OF THE 5TH ANNUAL DESIGN AUTOMATION WORKSHOP, JULY 15-18, 1968,
PGS. 16-0 TO 16-21
- 57 CHING, S.W. AND KEENAN, W.F.
A NOTE ON THE CARD ASSIGNMENT PROBLEM
BURROUGHS CORPORATION, JUNE 6, 1964, UNPUBLISHED
- 58 CHOUDHURY, A.K., BASU, A.K., AND DESARKAR, S.C.
ON THE DETERMINATION OF THE MAXIMUM COMPATIBILITY CLASSES
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME 18 (1969), PG. 665
- 59 CLARK, R.L.
A TECHNIQUE FOR IMPROVING WIRABILITY IN AUTOMATED CIRCUIT CARD PLACEMENT
RAND CORPORATION REPORT R-4049, AUGUST, 1969
- 60 CLARKE, S., KRIKORIAN, A., AND RAUSEN, J.
COMPUTING THE N BEST LOOPLESS PATHS IN A NETWORK
JOURNAL OF THE SIAM, VOLUME 11 (1963), PGS. 1096-1102
- 61 COMMUNICATIONS SYSTEMS, INC.
CONNECTIVITY AND CAPACITY COMPUTER PROGRAM WITH CIRCUIT AND ROUTING LOGIC
COMMUNICATIONS SYSTEMS, INC., PARAMUS, N.J., JULY 30, 1965, CFSTI AD 469 378
- 62 COOK, P.W., DONATH, W.E., LAMKE, G.A., AND BRENNEMAN, A.F.
AUTOMATIC NETWORK GENERATION FOR LARGE SCALE INTEGRATION
IEEE JOURNAL OF SOLID STATE CIRCUITS, VOLUME SC 2, NUMBER 4, PGS. 190-196
- 63 COOKE, K.L. AND HALSEY, E.
THE SHORTEST ROUTE THROUGH A NETWORK WITH TIME-DEPENDENT INTERNODAL TRANSIT
TIMES
JOURNAL OF MATHEMATICAL ANALYSIS AND APPLICATIONS, VOLUME 14 (1966), PGS. 493-
498
- 64 COOPER, J.F.
MONTE CARLO POSITIONING OF CONNECTED ELEMENTS ON A CARRIER
IBM REPORT 64-520-005, JUNE 29, 1964
- 65 COOPER, J.F. AND BROWN, J.A.
AUTOMATED PARTITIONING AND PLACEMENT IN THE WRAP SYSTEM
PROCEEDINGS OF THE TECHNICAL PROGRAM, NATIONAL ELECTRONICS PACKAGING AND
PRODUCTION CONFERENCE, JANUARY 1968, PGS. 85-93

- 66 COOPER, L.
LOCATION-ALLOCATION PROBLEMS
OPERATIONS RESEARCH, VOLUME 11, NUMBER 3 (MAY-JUNE 1963), PGS. 331-343
- 67 COOPER, L.
HEURISTIC METHODS FOR LOCATION ALLOCATION PROBLEMS
SIAM REVIEW, VOLUME 6 (JANUARY 1964), PGS. 37-53.
- 68 COOPER, L.
SOLUTIONS OF GENERALIZED LOCATIONAL EQUILIBRIUM MODELS
JOURNAL OF REGIONAL SCIENCE, VOLUME 7, NUMBER 1, 1967, PGS. 1-18
- 69 COOPER, L.
AN EXTENSION OF THE GENERALIZED WEFER PROBLEM
JOURNAL OF REGIONAL SCIENCE, VOLUME 8, NUMBER 2, 1968, PGS. 182-197
- 70 COOPER, L.
A RANDOM LOCATIONAL EQUILIBRIUM PROBLEM
TECHNICAL REPORT CP 74020, DEPARTMENT OF COMPUTER SCIENCE AND OPERATIONS
ALSO ACCEPTED FOR PUBLICATION, JOURNAL OF REGIONAL SCIENCE
- 71 COURANT, R. AND ROBBINS, H.
WHAT IS MATHEMATICS
OXFORD UNIVERSITY PRESS, LONDON AND NEW YORK, 1941
- 72 CRANE, R.A.
PATH FINDING WITH ASSOCIATIVE MEMORY
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-17 (JULY 1968), PGS. 691-693
- 73 CROCKETT, F.D. ET ALL
COMPUTER AIDED SYSTEM DESIGN
PROCEEDINGS OF THE FUCC, VOLUME 37 (1970), PGS. 287-296
- 74 CROUCH, D.
CLUSTERING
PH.D. THESIS, SOUTHERN METHODIST UNIVERSITY
- 75 CROW, R.A.
A GRAPH THEORETICAL APPROACH TO CLUSTERING
AFOSR 69-0912 TR, OCTOBER 1968, AFSTI AD 688 227
- 76 DANTZIG, G.B.
DISCRETE VARIABLE EXTREMUM PROBLEMS
OPERATIONS RESEARCH, VOLUME 5 (1957), PGS. 266-277
- 77 DANTZIG, G.B.
ON THE SHORTEST ROUTE THROUGH A NETWORK
RAND PAPER P-1345, 1958 ; ALSO MANAGEMENT SCIENCE, VOLUME 6 (1960), PGS. 187-190
- 78 DANTZIG, G.
LINEAR PROGRAMMING AND EXTENSIONS
PRINCETON UNIVERSITY PRESS, PRINCETON, NEW JERSEY, 1963
- 79 DANTZIG, G., FULKERSON, D. AND JOHNSON, S.
SOLUTIONS OF A LARGE SCALE TRAVELING SALESMAN PROBLEM
JOURNAL OF OPERATIONS RESEARCH, VOLUME 2 (1954), PGS. 393-410
- 80 DAWSON, D.F., KUO, F.F., AND MAGNUSON, W.G.
COMPUTER AIDED DESIGN OF ELECTRONIC CIRCUITS - A USERS VIEWPOINT
PROCEEDINGS OF THE IEEE, VOLUME 55 (1967), PGS. 1946-1954
- 81 DECKER, C.A. AND DECKER, L.N.
TOWARDS A COMPLETELY AUTOMATIC LAYOUT DESIGNER
VIRGINIA UNIVERSITY, AD 723064, SEPTEMBER 1970, 57 PAGES
- 82 DONATH, W.E.
STATISTICAL PROPERTIES OF THE PLACEMENT OF A GRAPH
SIAM JOURNAL ON APPLIED MATHEMATICS, VOLUME 16, NUMBER 2 (MARCH 1968), PGS. 439-457

- 83 DONATH, W.E.
HARDWARE IMPLEMENTATION
PROCEEDINGS IFIPS FALL JOINT COMPUTER CONFERENCE, 1968, PG. 1502
- 84 DONATH, W.E.
ALGORITHM AND AVERAGE-VALUE BOUNDS FOR ASSIGNMENT PROBLEMS
IBM JOURNAL OF RESEARCH AND DEVELOPMENT, VOLUME 13 (1969), PGS. 380-386
- 85 DREYFUS, S.E.
AN APPRAISAL OF SOME SHORTEST-PATH ALGORITHMS
IN PERSPECTIVES ON OPTIMIZATION, EDITED BY A.M. GEFFRION, ADDISON-WESLEY
PUBLISHING COMPANY, READING, MASSACHUSETTS, 1972
OPERATIONS RESEARCH, VOLUME 17 (1969), PGS. 395-412
- 86 DULMAGE, A.P. AND MENDELSON, N.S.
REMARKS ON SOLUTION OF THE OPTIMAL ASSIGNMENT PROBLEM
JOURNAL OF THE SIAM, VOLUME 11 (DECEMBER 1963), PGS. 1103-1109
- 87 DUNNE, G.V.
THE DESIGN OF PRINTED CIRCUIT LAYOUTS BY COMPUTER
PROCEEDINGS OF THE THIRD AUSTRALIAN COMPUTER CONFERENCE, CANBERRA, AUSTRALIA,
(1967), PGS. 419-423
- 88 FARDLEY, D.B. AND BERGGREN, J.L.
A MULTILAYER PRINTED CIRCUIT CARD FOR NANOSECOND CIRCUITS
IBM JOURNAL OF RESEARCH AND DEVELOPMENT
- 89 ERMOLEV, Y.M.
SHORTEST ADMISSIBLE PATHS
CYBERNETICS, VOLUME 2 (MAY 1966), PGS. 74-79
- 90 ERNESTO, C. AND LINDGREN, S.
PROPOSED SOLUTION FOR THE MINIMUM PATH PROBLEM
HARVARD UNIVERSITY LABORATORY FOR COMPUTER GRAPHICS, PAPER NUMBER 4, OCTOBER
14, 1967, CFSTI AD-660193
- 91 ESTRIN, G.
MAZE STRUCTURE AND INFORMATION RETRIEVAL
INTERNATIONAL CONFERENCE ON SCIENTIFIC INFORMATION, NATIONAL ACADEMY OF
SCIENCE, WASHINGTON, D.C., 1958, PGS. 1383-1416
- 92 EVANS, D.H.
MODULAR DESIGN A SPECIAL CASE IN NONLINEAR PROGRAMMING
JOURNAL OPERATION RESEARCH SOCIETY OF AMERICA, VOLUME 11 (JULY-AUGUST 1963),
PGS. 637-647
- 93 EVANS, G.C. AND GRIBBLE, M.W.
AUTOMATIC INTERCONNECTION SYSTEM FOR ELECTRONIC COMPONENTS
PROCEEDINGS OF THE IEE, VOLUME 116 (DECEMBER 1969), PGS. 1992-2000
- 94 FARBEY, B.A., HAND, A.H., AND MURCHLAND, J.D.
THE CASCADE ALGORITHM FOR FINDING ALL SHORTEST DISTANCES IN A DIRECTED GRAPH
MANAGEMENT SCIENCE, VOLUME 14 (1967), PGS. 19-28
- 95 FARLOW, C.
MACHINE AIDS TO THE DESIGN OF CERAMIC SUBSTRATES CONTAINING INTEGRATED CIRCUIT
CHIPS
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 22-25,
1970, SAN FRANCISCO, PGS. 274-285
- 96 FERRARI, D. AND MEZZALANA, L.
A COMPUTER AIDED APPROACH TO INTEGRATED CIRCUIT LAYOUT DESIGN
COMPUTER-AIDED DESIGN, VOLUME 2 (WINTER 1970), PGS. 19-23
- 97 FERRARI, D. AND SAMI, M.
AN ALGORITHM FOR PARTITIONING NETWORKS INTO LIMITED SETS OF DIFFERENT
SUBNETWORKS
IN DIGEST OF THE 1969 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUIT THEORY
- 98 FIELDING, G.F.
AUTOMATICALLY PROCESSED WIRE LISTS
WESTERN ELECTRONIC NEWS, JUNE, 1962, PG. 22

- 99 FISK, C.J., CASKEY, D.L. AND WEST, L.E.
TOPOGRAPHIC SIMULATION AS AN AID TO PRINTED CIRCUIT DESIGN
PROCEEDINGS OF THE SHARE DESIGN AUTOMATION WORKSHOP, VOLUME 4 (1967), PGS.
17-1 TO 17-23
- 100 FISK, C.J., CASKEY, D.L., AND WEST, L.L.
ACCEL : AUTOMATED CIRCUIT CARD ETCHING LAYOUT
PROCEEDINGS IEEE, VOLUME 55, NUMBER 11 (1967), PGS. 1971-1982
ALSO SANDIA LAB REPORT SC-R-67-1208
- 101 FISK, C.J. AND ISETT, D.D.
ACCEL : AUTOMATED CIRCUIT CARD ETCHING LAYOUT
SM-TM-65-544, SANDIA LABORATORY, ALBUQUERQUE, N.M.
- 102 FISK, C.J., CASKEY, D.L. AND WEST, L.E.
ACCEL-AUTOMATED CIRCUIT CARD ETCHING LAYOUT
PROCEEDINGS OF THE HAWAII INTERNATIONAL CONFERENCE ON SYSTEM SCIENCE,
UNIVERSITY OF HAWAII PRESS, HONOLULU, 1968, PGS. 107-108
- 103 FISK, C. AND ISETT, D.
ACCEL AUTOMATED CIRCUIT CARD ETCHING LAYOUT
PROCEEDINGS OF THE DESIGN AUTOMATION WORKSHOP, 1965, PGS. 5-32
- 104 FLOOD, M.
THE TRAVELING SALESMAN PROBLEM
JOURNAL OF OPERATIONS RESEARCH, VOLUME 4, NUMBER 1 (FEBRUARY 1956), PGS. 61-75
- 105 FLOYD, R.W.
ALGORITHM 97 : SHORTEST PATH
COMMUNICATIONS OF THE ACM, VOLUME 5 (1962), PG. 345
- 106 FLYNN, M.J. AND SNOW, W.
MULTI-PLANAR SELF-RESTRICTING MAZES : SOME RESULTS AND SYSTEMS APPLICATIONS
HAWAII INTERNATIONAL CONFERENCE ON SYSTEM SCIENCE, VOLUME 3 (1970),
UNIVERSITY OF HAWAII PRESS, PGS. 564-567
- 107 FORD, L.R. AND FULKERSON, D.R.
SOLVING THE TRANSPORTATION PROBLEM
MANAGEMENT SCIENCE III, OCTOBER, 1956, PGS. 24-32
- 108 FORD, L.R. AND FULKERSON, D.R.
A SIMPLE ALGORITHM FOR FINDING MAXIMAL NETWORK FLOWS AND AN APPLICATION TO THE
HITCHCOCK PROBLEM
RAND CORPORATION, REPORT P-743, SEPTEMBER 26, 1955, SANTA MONICA, CALIFORNIA
- 109 FORD, L.R. AND FULKERSON, D.R.
FLOWS IN NETWORKS
PRINCETON UNIVERSITY PRESS, PRINCETON, NEW JERSEY, 1962
- 110 FOSTER, J.C.
A ROUTER FOR MULTILAYER PRINTED WIRING BACK PLANES
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973,
PGS. 44-49
- 111 FRANCIS, R.L.
A NOTE ON THE OPTIMUM LOCATION OF NEW MACHINES IN EXISTING PLANT LAYOUTS
THE JOURNAL OF INDUSTRIAL ENGINEERING, VOLUME 14 (1963), PGS. 57-59
- 112 FRANQUY, R.
AUTOMATION OF MLR INTERCONNECTION LAYOUT
TECHNICAL MEMORANDUM 343-04-04, DATA SYSTEMS DIVISION, AUTONETICS, ANAHEIM,
CALIFORNIA
- 113 FREEMAN, M., GINSBERG, G., RESNICK, M. AND WHITLEY, E.
MULTILAYER PRINTED WIRING - COMPUTER AIDED DESIGN
PROCEEDINGS OF THE SHARE / ACM DESIGN AUTOMATION WORKSHOP, 1967, LOS ANGELES
PGS. 16-1 TO 16-28
- 114 FREEMAN, M. AND RESNICK, M.
GENDA - A GENERALIZED DESIGN AUTOMATION SYSTEM FOR MODULAR HARDWARE
PROCEEDINGS OF THE 5TH SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1968,
PGS. 2.1 - 2.21

- 115 FREITAG, H.
DESIGN AUTOMATION FOR LARGE SCALE INTEGRATION
IBM WATSON RESEARCH CENTER, YORKTOWN HEIGHTS, NEW YORK. PRESENTED AT THE
WESTERN ELECTRONIC SHOW AND CONVENTION, AUGUST 22-26, 1966
- 116 FREITAG, H. AND DONATH, W.E.
AUTOMATIC MASK GENERATION AND WIRING PATTERN RECOGNITION
NASA ERC COMPUTER AIDED DESIGN SYMPOSIUM, APRIL 1967
- 117 FREITAG, H. AND HANAN, M.
A PLACEMENT ALGORITHM
IBM INTERNAL REPORT, NOVEMBER, 1966
- 118 FRIEDMAN, J. AND MARKS, H.
WIRE PATH STRATEGIES FOR SIGNAL HARNESS
INTERNAL MEMO, DIGITAL TECHNOLOGY PROJECTS, DEPARTMENT OF ELECTRICAL
ENGINEERING, UNIVERSITY OF CALIFORNIA, LOS ANGELES, JANUARY, 1965
- 119 GAMBLIN, R.L., JACOBS, M.O., AND TUNIS, C.J.
AUTOMATIC PACKAGING OF MINIALIZED CIRCUITS
IN ADVANCES IN ELECTRONIC CIRCUIT PACKAGING, G.A. WALKER, ED., VOLUME 2,
PLENUM PRESS, NEW YORK, 1962, PGS. 219-232
- 120 GARDNER, M.
MATHEMATICAL GAMES
SCIENTIFIC AMERICAN, NOVEMBER, 1963
- 121 GARSIDE, R.G. AND NICHOLSON, T.A.
PERMUTATION PROCEDURE FOR THE BACKBOARD WIRING PROBLEM
PROCEEDINGS OF THE IEE (JANUARY 1968), PGS. 27-30
- 122 GASCHUTZ, G.K. AND AHRENS, J.H.
SUBOPTIMAL ALGORITHMS FOR THE QUADRATIC ASSIGNMENT PROBLEM
NAVAL RESEARCH LOGISTICS QUARTERLY, VOLUME 15, NUMBER 1 (MARCH 1968)
- 123 GASKILL, R.A.
A GENERAL TREE SEARCH ALGORITHM FOR A CLASS OF COMBINATORIAL PROBLEMS
INVOLVING DIRECTED GRAPHS
DOCTORAL DISSERTATION, CASE WESTERN RESERVE UNIVERSITY, 1969
- 124 GESINK, D.L.
AN APPROACH TO PLACEMENT AND ROUTING APPLICATIONS ON AN IBM
IBM MANUAL Z77-8149, WHITE PLAINS, N.Y., DEC. 11, 1968
- 125 GEYER, J.M.
CONNECTION ROUTING ALGORITHM FOR PRINTED CIRCUIT BOARDS
IEEE TRANSACTIONS ON CIRCUIT THEORY, VOLUME C-20 (JANUARY 1971), PGS. 95-100
- 126 GILBERT, E.N. AND POLLAK, H.O.
STEINER MINIMAL TREES
SIAM JOURNAL ON APPLIED MATHEMATICS, VOLUME 16 (1968), PGS. 1-29
- 127 GILL, S.
THE USE OF COMPUTERS IN DESIGNING COMPUTERS
INDUSTRIAL RESEARCH (LONDON), VOLUME 15 (1962), PGS. 159-163
- 128 GILMORE, P.C.
A SOLUTION TO THE MODULE PLACEMENT PROBLEM
IBM REPORT RC-430, APRIL 26, 1961
- 129 GILMORE, P.C.
OPTIMAL AND SUBOPTIMAL ALGORITHMS FOR THE QUADRATIC ASSIGNMENT PROBLEM
JOURNAL OF THE SIAM, VOLUME 10, NUMBER 2 (JUNE 1962), PGS. 305-313
- 130 GILMORE, P.C.
SOLUTION OF A WIRE LAYOUT PROBLEM
IBM RESEARCH NOTE RC-183, YORKTOWN HEIGHTS, NEW YORK, DECEMBER 17, 1962
- 131 GINSBERG, G.L., MAURER, C.R., AND WHITLEY, E.H.
AN UPDATED MULTILAYER PRINTED WIRING C-A-D CAPABILITY
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 8-12,
1969, MIAMI BEACH, FLORIDA, PGS. 145-154

- 132 GLASER, R.H.
A QUASI-SIMPLEX METHOD FOR DESIGNING SUBOPTIMAL PACKAGES FOR ELECTRONIC BUILDING BLOCKS
PROCEEDINGS 1959 COMPUTER APPLICATIONS SYMPOSIUM AT ARMOUR RESEARCH FOUNDATION ILLINOIS INSTITUTE OF TECHNOLOGY, PGS. 100-111
- 133 GOLDBERG, M.J.
ON-LINE OPERATION OF CADIC-COMPUTER AIDED DESIGN OF INTEGRATED CIRCUITS
NORDEN DIVISION, UNITED AIRCRAFT CORPORATION, NORWALK, CONN.
- 134 GRAVES, G.W. AND WHINSTON, A.B.
AN ALGORITHM FOR THE QUADRATIC ASSIGNMENT PROBLEM
MANAGEMENT SCIENCE, VOLUME 17, NUMBER 7 (MARCH 1970)
- 135 GREENBERG, H. AND HEGERICH, R.L.
A BRANCH SEARCH ALGORITHM FOR THE KNAPSACK PROBLEM
MANAGEMENT SCIENCE, VOLUME 16, NUMBER 5 (JANUARY 1970)
- 136 GRIM, R.K. AND BROUWER, D.P.
WIRING TERMINAL PANNELS BY MACHINE
CONTROL ENGINEERING, VOLUME 8, NUMBER 8 (AUGUST 1961), PGS. 77-81
- 137 GRIMMER, R.C.
INTERCONNECTING HIGH-SPEED INTEGRATED CIRCUITS WITH MULTILAYER BOARDS
COMPUTER DESIGN, VOLUME 6 (FEBRUARY 1967), PGS. 36-40
- 138 HABAYER, A.R.
SYSTEM DECOMPOSITION, PARTITIONING, AND INTEGRATION FOR MICROELECTRONICS
IEEE TRANSACTIONS ON SYSTEMS SCIENCE AND CYBERNETICS, VOL. SSC-4, NUMBER 2 (JULY 1968), PGS. 164-172
- 139 HANAN, M.
ON STEINERS PROBLEM WITH RECTILINEAR DISTANCE
SIAM JOURNAL OF APPLIED MATHEMATICS, VOLUME 14 (1966), PGS. 255-265
- 140 HANAN, M.
NET WIRING FOR LARGE SCALE INTEGRATED CIRCUITS
IBM REPORT RC-1375, FEBRUARY 1965
- 141 HANAN, M. AND KURTZBERG, J.M.
FORCE-VECTOR PLACEMENT TECHNIQUES
IBM REPORT RC-2843, APRIL, 1970
- 142 HANAN, M. AND KURTZBERG, J.M.
A REVIEW OF THE PLACEMENT AND QUADRATIC ASSIGNMENT PROBLEMS
SIAM REVIEW, VOLUME 14, NUMBER 2 (APRIL 1972)
ALSO PREPRINTED AS IBM REPORT RC-3046, 20 APRIL 1970
- 143 HANAN, M. AND KURTZBERG, J.M.
PLACEMENT TECHNIQUES
CHAPTER 5, PGS. 213-282, IN DESIGN AUTOMATION OF DIGITAL SYSTEMS, M.A. BREUER, EDITOR, PRENTICE HALL, ENGLEWOOD CLIFFS, N.J., 1972
- 144 HANAN, M. AND ODEN, P.H.
A WIRING PROBLEM FOR LARGE SCALE INTEGRATED CIRCUITS
IBM REPORT RC-1615, MAY 1966
- 145 HANNE, J.R.
AUTOMATED INTERCONNECTION SCHEMES AT TEXAS INSTRUMENTS
7TH INTERNATIONAL ELECTRONICS PACKAGING SYMPOSIUM, PRESENTED AT THE WESTERN ELECTRONICS SHOW AND CONVENTION, CALIFORNIA
- 146 HAPP, W.W.
COMPUTER AIDED DESIGN IN THE USA
DESIGN ELECTRONICS, VOLUME 4 (1967), PGS. 42-44
- 147 HARARY, F.
GRAPH THEORY AND ELECTRICAL NETWORKS
THE TRANSACTIONS ON CIRCUIT THEORY, VOLUME CT-6, 1959, PGS. 95-109

- 148 HARARY, F.
GRAPH THEORY
ADDISON-WESLEY PUBLISHING COMPANY, READING, MASS., 1969
- 149 HARDGRAVE, W. AND NEMHAUSER, G.L.
ON THE RELATIONSHIP BETWEEN THE TRAVELING SALESMAN AND LONGEST PATH PROBLEMS
BELL SYSTEM MONOGRAPH NUMBER 4336
ALSO OPERATIONS RESEARCH, VOLUME 10 (1962), PGS. 647-657
- 150 HART, P., NILSSON, N., AND RAPHAEL, B.
A FORMAL BASIS FOR THE HEURISTIC DETERMINATION OF MINIMUM COST PATHS
IEEE TRANSACTIONS ON SYSTEM SCIENCE AND CYBERNETICS, VOLUME SSC-4, NUMBER 2,
(JULY 1968), PGS. 100-107
- 151 HARVEY, J.G.
AUTOMATED BOARD LAYOUT
PROCEEDINGS OF THE ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 26-28, 1972,
DALLAS, PGS. 264-271
- 152 HASHIMOTO, A. AND NOSHITA, K.
A PROPERTY OF N-GRAPHS
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-20 (JANUARY 1971), PGS. 95-97
- 153 HASHIMOTO, A. AND STEVENS, J.
WIRE ROUTING BY OPTIMIZING CHANNEL ASSIGNMENT WITHIN LARGE APERTURES
THE EIGHT DESIGN AUTOMATION WORKSHOP PROCEEDINGS, 1971, PGS. 155-169
- 154 HASPEL, C.H.
THE AUTOMATIC PACKAGING OF COMPUTER CIRCUITRY
IEEE INTERNATIONAL CONVENTION RECORD, VOLUME 13, PART 3 (1965), PGS. 4-20
- 155 HAYASHI, T.
FACOM 230-SERIES COMPUTER DESIGN AUTOMATION SYSTEM
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 22-25,
1970, SAN FRANCISCO, PGS. 230-242
- 156 HAZLETT, L.H. AND BEEMILLER, G.V.
AUTOMATIC ARTWORK GENERATION FOR INTEGRATED CIRCUITS
IN COMPUTER ORIENTED CIRCUIT DESIGN, PRENTICE-HALL, 1969
- 157 HEAP, R.R.
PERMUTATIONS BY INTERCHANGES
COMPUTER JOURNAL, VOLUME 6 (OCTOBER 1963), PGS. 293-294
- 158 HEIDER, C.H.
AN N-STEP 2 VARIABLE SEARCH ALGORITHM FOR THE COMPONENT PLACEMENT PROBLEM
CENTER FOR NAVAL ANALYSIS, PROFESSIONAL PAPER NUMBER 90, OCTOBER 1972,
CFSTI AD 756 502
- 159 HEIDER, C.H.
A COMPUTATIONALLY SIMPLIFIED PAIR-EXCHANGE ALGORITHM FOR THE QUADRATIC
ASSIGNMENT PROBLEM
CENTER FOR NAVAL ANALYSIS, PROFESSIONAL PAPER NUMBER 101, NOVEMBER 1972,
CFSTI AD 756 503
- 160 HEIDER, C.H.
A DECOMPOSITION PROCEDURE FOR THE QUADRATIC ASSIGNMENT PROBLEM
CENTER FOR NAVAL ANALYSIS, PROFESSIONAL PAPER NUMBER 100, NOVEMBER 1972,
CFSTI AD 751 215
- 161 HEISS, S.
A PATH CONNECTING ALGORITHM FOR MULTILAYER BOARDS
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1968,
PGS 6-0 TO 6-14
- 162 HELD, M. AND KARP, R.
A DYNAMIC PROGRAMMING APPROACH TO SEQUENCING PROBLEMS
JOURNAL OF THE SIAM, VOLUME 10, NUMBER 1 (MARCH 1962), PGS. 196-210
- 163 HERBST, R.T.
DESIGNING EQUIPMENT WITH COMPUTERS
BELL LABORATORY RECORD, VOLUME 44 (APRIL 1966), PGS. 129-134

- 164 HICKS, D.M.
COMPUTER-AIDED DIGITAL DESIGN
ROEING REPORT D2-90831-1
- 165 HIGHTOWER, D.W.
A SOLUTION TO LINE ROUTING PROBLEMS ON THE CONTINUOUS PLANE
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 8-12,
1969, MIAMI BEACH, FLORIDA, PGS. 1-24
- 166 HIGHTOWER, D.W.
INTERCONNECTION TECHNIQUES
PROCEEDINGS OF THE 1972 INTERNATIONAL SEMINAR ON DESIGN AUTOMATION, ILTAM,
JERUSALEM, ISRAEL
- 167 HIGHTOWER, D.W.
INTERCONNECTION TECHNIQUES
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973,
PGS. 1-21
- 168 HIGHTOWER, D. AND UNGER, R.
A METHOD FOR RAPID TESTING OF RFAM CROSSOVER CIRCUITS
PROCEEDINGS OF THE ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1972, PGS. 144-156
- 169 HILLIER, F.S. AND CONNORS, M.M.
QUADRATIC ASSIGNMENT PROBLEM ALGORITHMS AND THE LOCATIONS OF INDIVISIBLE
FACILITIES
MANAGEMENT SCIENCE, VOLUME 13, NUMBER 1 (SEPTEMBER 1966), PGS. 42-57
- 170 HIRAKAWA, K. AND HIRANO, T.
COMPUTER-AIDED DESIGN SYSTEM FOR LOGIC EQUIPMENT APPLIED TO DESIGN OF
ELECTRONIC SWITCHING EQUIPMENT
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973,
PGS. 205-209
- 171 HITCHCOCK, R.R.
CELLULAR WIRING AND THE CELLULAR MODELING TECHNIQUE
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 8-12,
MIAMI BEACH, FLORIDA, 1969, PGS. 25-41
- 172 HITCHNER, L.E.
A COMPARATIVE INVESTIGATION OF THE COMPUTATIONAL EFFICIENCY OF SHORTEST PATH
ALGORITHMS
OPERATIONS RESEARCH CENTER REPORT ORC 68-25, UNIVERSITY OF CALIFORNIA-BERKELEY
BERKELEY, CALIFORNIA, NOVEMBER 1968
- 173 HOFFMAN, A.J. AND MARKOWITZ, H.M.
A NOTE ON SHORTEST PATH, ASSIGNMENT, AND TRANSPORTATION PROBLEMS
NAVAL RESEARCH LOGISTICAL QUARTERLY, VOLUME 10 (1963), PGS. 375-379
- 174 HOFFMAN, W. AND PAVLEY, R.
A METHOD FOR THE SOLUTION OF THE N-TH BEST PATH PROBLEM
JOURNAL OF THE ACM, VOLUME 6 (1959), PGS. 506-514
- 175 HOLSTEIN, D.
ARE YOU READY FOR COMPUTER AIDED DESIGN
PRODUCT ENGINEERING, VOLUME 35 (NOVEMBER 1964), PGS. 66-76
- 176 HOPE, A.K.
A PLANAR GRAPH DRAWING PROGRAM
SOFTWARE-PRACTICE AND EXPERIENCE, VOLUME 1 (JANUARY-MARCH 1971), PGS. 83-91
- 177 HORN, W.A.
MINIMUM LENGTH COVERING BY INTERSECTING INTERVALS
JOURNAL OF RESEARCH, NATIONAL BUREAU OF STANDARDS, 73B(1969), PGS. 49-51
- 178 HU, T.C.
REVISED MATRIX ALGORITHMS FOR SHORTEST PATHS
SIAM JOURNAL, VOLUME 15 (1967), PGS. 207-218
ALSO IRM RESEARCH REPORT RC-1478, SEPTEMBER 28, 1965

- 179 HU, T.C.
A DECOMPOSITION ALGORITHM FOR SHORTEST PATHS IN A NETWORK
OPERATIONS RESEARCH, VOLUME 16 (1968), PGS. 91-102
ALSO IBM RESEARCH REPORT RC-1562, FEBRUARY 1966
- 180 HU, T.C. AND TORRES, W.T.
SHORTCUT IN THE DECOMPOSITION ALGORITHM FOR SHORTEST PATHS IN A NETWORK
IBM JOURNAL OF RESEARCH AND DEVELOPMENT, VOLUME 13 (1969), PGS. 387-390
ALSO MATHEMATICAL RESEARCH CENTER, U.S. ARMY REPORT 882, UNIVERSITY OF
WISCONSIN, MADISON, JULY 1968, CESTI AD679 936
- 181 HUGHES, J.S. AND LALLIER, K.W.
AUTOMATED COMPONENT PLACEMENT AND PIN ASSIGNMENT
IBM REPORT 65-825-1422, FEBRUARY, 1965
- 182 HURST, R. AND ROSENSTEIN, A.
INTEGRATED COMPUTER AIDED DESIGN SYSTEMS
PROCEEDINGS OF THE FJCC, 1970, PGS. 297-314
- 183 HUTTLY, N.A.
AUTOMATED PRODUCTION OF WIRING SCHEDULES AND PRINTED CIRCUIT LAYOUTS
MARCONI REVIEW, VOLUME 30 (1968), PGS. 20-31
- 184 IBM
THREE DIMENSIONAL PLACEMENT AND ROUTING
IBM DATA PROCESSING APPLICATION MANUAL E20-0119-0, 84 PAGES
- 185 ILTAM, JERUSALEM, ISRAEL
PROCEEDINGS OF THE 1972 INTERNATIONAL SEMINAR ON DESIGN AUTOMATION OF DIGITAL
SYSTEMS
ILTAM, JERUSALEM, ISRAEL
- 186 JAMISON, J.F.
USERS MANUAL : UCARDS, UNION CARBIDE AUTOMATIC ROUTING AND DESIGN SYSTEM
FOR PRINTED CIRCUIT BOARDS
UNION CARBIDE CORP. NUCLEAR DIVISION REPORT K-1736, OAK RIDGE GASEOUS
DIFFUSION PLANT, OAK RIDGE, TENN., JANUARY 25, 1968, STAR N69-33691, VOLUME 7,
NUMBER 19, PG. 544
- 187 JARVIS, J.F.
THE DESIGN OF INTERACTIVE GRAPHICS AIDS TO MASK LAYOUT
PROCEEDINGS OF THE IEEE, VOLUME 60, PG. 35 (1972)
- 188 JOKSCH, H.C.
THE SHORTEST ROUTE PROBLEM WITH CONSTRAINTS
JOURNAL OF MATHEMATICAL ANALYSIS AND APPLICATIONS, VOLUME 14 (1966), PGS 191-
197
- 189 KALLAS, J.L.
COMPUTER AIDED WIRING DESIGNS
BELL LABS RECORD, VOLUME 42 (NOVEMBER 1964), PGS. 343-349
- 190 KARP, R.M.
REDUCIBILITY AMONG COMBINATORIAL PROBLEMS
UNIVERSITY OF CALIFORNIA BERKELEY, COMPUTER SCIENCE TECHNICAL REPORT 3, 1972
- 191 KATZ, I.N. AND COOPER, L.
AN ALWAYS CONVERGENT NUMERICAL SCHEME FOR A RANDOM LOCATIONAL EQUILIBRIUM
PROBLEM
TECHNICAL REPORT CP72021, DEPARTMENT OF COMPUTER SCIENCE AND OPERATIONS
RESEARCH, SOUTHERN METHODIST UNIVERSITY, DALLAS, 1972
ALSO ACCEPTED FOR PUBLICATION IN THE SIAM JOURNAL OF NUMERICAL ANALYSIS
- 192 KAWAKATSU, F., TAKAHASHI, H. AND HYODO, T.
A NEW ALGORITHM OF PATH CONNECTION FOR SAVING DIGITS
DIGEST OF THE IEEE SOLID-STATE CIRCUITS CONFERENCE, VOLUME 11 (1968), PGS. 72
-73
- 193 KEENAN, W.F. AND CHING, S.W.
A NOTE ON THE CARD ASSIGNMENT PROBLEM
BURROUGHS CORPORATION, JUNE 6, 1964, UNPUBLISHED

- 194 KERNIGHAN, R.W. AND LIN, S.
AN EFFICIENT HEURISTIC PROCEDURE FOR PARTITIONING GRAPHS
BELL SYSTEM TECHNICAL JOURNAL, VOLUME 49 (FEBRUARY 1970), PGS. 291-308
U.S. PATENT NUMBER 3,617,714
- 195 KERNIGHAN, R.W., SCHWEIKERT, D.G. AND PERSKY, G.
AN OPTIMUM CHANNEL ROUTING ALGORITHM FOR POLYCELL LAYOUTS OF INTEGRATED
CIRCUITS
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973,
PGS. 50-59
- 196 KIRBY, D.R. AND ROSENTHAL, C.W.
COMPUTER PROGRAM FOR PREPARING WIRING DIAGRAMS
TRANSACTIONS AIEE, PART 1, VOLUME 80 (1961), PGS. 509-513
- 197 KIRBY, R.F. AND POTTS, R.R.
THE MINIMUM ROUTE PROBLEM FOR NETWORKS WITH TURN PENALTIES AND PROHIBITIONS
TRANSPORTATION RESEARCH, VOLUME 3 (1969), PGS. 397-408
- 198 KLEE, V.
A STRING ALGORITHM FOR SHORTEST PATH IN A DIRECTED NETWORK
OPERATIONS RESEARCH, VOLUME 12 (1964), PGS. 428-432
- 199 KLEMETSMO, R.R., MINTURN, G.A., AND WRIGHT, A.I.
GRAPHIC DISPLAY TECHNIQUES IN THE AUTOMATED INTERCONNECTION PROCESS
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1968,
PGS. 20-1 TO 20-17
- 200 KODRES, U.R.
FORMULATION AND SOLUTION OF CIRCUIT CARD DESIGN PROBLEMS THROUGH USE OF GRAPH
METHODS
IN ADVANCES IN ELECTRONICS CIRCUIT PACKAGING, VOLUME 2, G.A.WALKER, ED.,
PLENUM PRESS, NEW YORK, 1962, PGS. 121-142
ALSO IBM TECHNICAL REPORT 00.796, 1961
- 201 KODRES, U.R.
GEOMETRICAL POSITIONING OF CIRCUIT ELEMENTS IN A COMPUTER
AIEE PUBLICATION NUMBER CP 59-1172 (OCTOBER 1959), FALL 1959 AIEE MEETINGS
- 202 KODRES, U.R. AND LIPPMAN, H.E.
SLT BOARD LAYOUT
IBM TECHNICAL REPORT TR00.1010, REVISED MARCH 10, 1964
- 203 KODRES, U.R.
SYSTEMATIC METHODS FOR COMPUTER AIDED DESIGN OF COMPUTERS
U.S. NAVAL POSTGRADUATE SCHOOL LECTURE NOTES, MARCH 19-22, 1968
- 204 KODRES, U.R.
LOGIC CIRCUIT LAYOUT
PROCEEDINGS OF THE JOINT CONFERENCE ON MATHEMATICAL AND COMPUTER AIDS TO
DESIGN, 1969, PGS. 165-191
- 205 KODRES, U.R.
PARTITIONING AND CARD SELECTION
CHAPTER 4, PGS. 173-212, IN DESIGN AUTOMATION OF DIGITAL SYSTEMS, M.A. BREUER,
EDITOR, PRENTICE HALL, ENGLEWOOD CLIFFS, N.J., 1972
- 206 KOOPMANS, T.C. AND BECKMAN, M.
ASSIGNMENT PROBLEMS AND THE LOCATION OF ECONOMIC ACTIVITIES
ECONOMETRICA, VOLUME 25 (1957), PGS. 53-76
- 207 KOREN, NORMAN
PIN ASSIGNMENT IN AUTOMATED PRINTED CIRCUIT BOARD DESIGN
PROCEEDINGS OF THE ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1972, DALLAS,
PGS. 72-79
- 208 KOZAKA, T. ET AL
BLOCK AND TRACK METHOD FOR AUTOMATED LAYOUT GENERATION OF MOS/LSI ARRAYS
1972 IEEE SOLID-STATE CIRCUITS CONFERENCE DIGEST, PGS. 62-63

- 209 KRARUP, JAKOB
A BRANCH-BOUND ALGORITHM FOR A WIRING PROBLEM
BIT, VOLUME 9, NUMBER 2 (1969), PGS. 133-156
- 210 KROLAK, P. AND MARBLE, G.
A MAN-MACHINE APPROACH TOWARDS SOLVING THE TRAVELING SALESMAN PROBLEM.
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1970,
SAN FRANCISCO, PGS. 250-264
- 211 KRUSKAL, J.B.
ON THE SHORTEST SPANNING SUBTREE OF A GRAPH AND THE TRAVELING SALESMAN PROBLEM
PROCEEDINGS OF THE AMERICAN MATHEMATICAL SOCIETY, VOLUME 7 (1956), PGS. 48-50
- 212 KU, Y.H. AND REDROSIAN, S.A.
ON TOPOLOGICAL APPROACHES TO NETWORK THEORY
JOURNAL OF THE FRANKLIN INSTITUTE, JANUARY 1965, PG. 279
- 213 KUHN, H.W.
THE HUNGARIAN METHOD FOR THE ASSIGNMENT PROBLEM
NAVAL RESEARCH LOGISTICAL QUARTERLY, VOLUME 2, NUMBER 1 (MARCH-JUNE 1955),
PGS. 83-97
- 214 KUO, FF. AND MAGNUSON, W.G., EDITORS
COMPUTER ORIENTED CIRCUIT DESIGN
PRENTICE HALL, ENGLEWOOD, N.J., 1968, CHAPTER 12
- 215 KURTZBERG, J.M.
APPROXIMATION METHODS FOR SOLUTION OF LARGE SCALE ASSIGNMENT PROBLEMS
BURROUGHS TECHNICAL REPORT TR 60-32, JUNE 10, 1964
- 216 KURTZBERG, J.M.
BACKBOARD WIRING ALGORITHMS FOR THE PLACEMENT AND CONNECTION ORDER PROBLEMS
BURROUGHS TECHNICAL REPORT TR 60-40, JUNE 28, 1960
- 217 KURTZBERG, J.M.
ALGORITHMS FOR BACKPLANE FORMATION
IN MICROELECTRONICS IN LARGE SYSTEMS, SPARTAN BOOKS, 1965, PGS. 51-76
- 218 KURTZBERG, J.M.
COMPUTER MECHANIZATION OF DESIGN PROCEDURES
PROCEEDINGS OF THE SIXTH ANNUAL AIEE CONFERENCE, DETROIT, MICHIGAN, OCTOBER,
1964
- 219 KURTZBERG, J.M.
ON APPROXIMATION METHODS FOR THE ASSIGNMENT PROBLEM
JOURNAL OF THE ACM, VOLUME 9, NUMBER 4 (OCTOBER 1962), PGS. 419-439
- 220 KURTZBERG, J.M. AND ESTES, B.
INITIAL CARD PLACEMENT ALGORITHMS : AN EVALUATION
BURROUGHS TECHNICAL REPORT TR 61-44, AUGUST 21, 1961
- 221 KURTZBERG, J.M. AND SEWARD, J.
PROGRAM FOR STAR CLUSTER WIRING OF BACKPLANE
BURROUGHS INTERNAL REPORT, JANUARY, 1964
- 222 LANDAU, I.Y.
USING ETSVM (ELECTRONIC DIGITAL COMPUTERS) TO DESIGN ETSVM
FOREIGN TECHNOLOGY DIVISION, WRIGHT-PATTERSON AFB, OHIO, JULY, 1968,
CFSTI AD-682176
- 223 LANDMAN, B.S. AND RUSSO, R.L.
ON A PIN VERSUS BLOCK RELATIONSHIP FOR PARTITIONS OF LOGIC GRAPHS
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-20, (DECEMBER 1971), PGS. 1469-1479
- 224 LARSEN, R.P.
COMPUTER AIDED PRELIMINARY LAYOUT DESIGN OF CUSTOMIZED MOS ARRAYS
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-20, NUMBER 5 (MAY 1971), PGS. 512-
- 225 LASS, S.E.
AUTOMATED PRINTED CIRCUIT ROUTING WITH A STEPPING APERTURE
COMMUNICATIONS OF THE ACM, VOLUME 2, NUMBER 5 (MAY 1969)

- 226 LAVERING, F.B. AND COREY, P.J.
AUTOMATED PRINTED CIRCUIT BOARD DESIGN
THE BOEING COMPANY, MAY, 1964, UNPUBLISHED.
- 227 LAVERING, F.B., LYONS, J.J. AND COREY, P.J.
AUTOMATED PRINTED CIRCUIT BOARD DESIGN
PROCEEDINGS OF THE SHARE DESIGN AUTOMATION WORKSHOP, JUNE 24-26, 1964
- 228 LAWLER, E.L.
ELECTRICAL ASSEMBLIES WITH A MINIMUM NUMBER OF INTERCONNECTIONS
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME EC-11 (FEBRUARY 1962),
PGS. 84-88
- 229 LAWLER, E.L.
THE QUADRATIC ASSIGNMENT PROBLEM
MANAGEMENT SCIENCE, VOLUME 9 (1963), PGS. 586-599
- 230 LAWLER, E.L. AND WOOD, D.E.
BRANCH AND BOUND METHODS: A SURVEY
JOURNAL OF OPERATIONS RESEARCH, VOLUME 14 (1966), PGS. 699-719
- 231 LAWLER, E.L., LEVITT, K.N. AND TURNER, J.
MODULE CLUSTERING TO MINIMIZE DELAY IN DIGITAL NETWORKS
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME C-18 (JANUARY 1969),
PGS. 47-57
- 232 LEE, C.Y.
AN ALGORITHM FOR PATH CONNECTIONS AND ITS APPLICATIONS
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME EC-10, NUMBER 3
(SEPTEMBER 1961), PGS. 346-365
- 233 LEE, C.Y.
A NOTE ON THE N-TH SHORTEST PATH PROBLEM
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME 11 (1962), PGS. 572-573
- 234 LEE, R.C. AND MOORE, T.M.
CORELAP - COMPUTERIZED RELATIONSHIP LAYOUT PLANNING
JOURNAL OF INDUSTRIAL ENGINEERING, VOLUME 18, NUMBER 3 (MARCH 1967), PGS. 195-
200
- 235 LEEVERS, D.F.A.
THE USE OF A GRAPHICAL DISPLAY IN THE AUTOMATIC DESIGN OF PRINTED CIRCUIT
BOARDS
INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN, IEE, 1969, PGS. 11-20
- 236 LEINER, A.L., WEINBERGER, A., COLEMAN, C., AND LOBERMAN, H.
USING DIGITAL COMPUTERS IN THE DESIGN AND MAINTENANCE OF NEW COMPUTERS
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME 10 (1961), PGS. 680-690
- 237 LERDA, F. AND MAJORANI, E.
AN ALGORITHM FOR CONNECTING N POINTS WITH A MINIMUM NUMBER OF CROSSINGS
CALCOLO 1 (1964), PGS. 257-264
- 238 LEVI, G. AND LUCCIO, F.
A WEIGHTED GRAPH EMBEDDING TECHNIQUE AND ITS APPLICATION TO AUTOMATIC CIRCUIT
LAYOUT
CALCOLO, VOLUME 8 (JANUARY-JUNE 1971), PGS. 47-60
- 239 LEVIN, B.M. AND HEDETNIEMI, S.
DETERMINING FASTEST ROUTES USING FIXED SCHEDULES
AFIPS PROCEEDINGS OF THE SPRING JOINT COMPUTER CONFERENCE, 1963, PGS. 1-5
- 240 LEVITT, K.N. AND KAUTZ, W.H.
CELLULAR ARRAYS FOR THE SOLUTION OF GRAPH PROBLEMS
COMMUNICATIONS OF THE ACM, VOLUME 15, NUMBER 9 (SEPTEMBER 1972), PGS. 789-801
- 241 LEWALLEN, D.R.
MOS LSI COMPUTER AIDED DESIGN SYSTEM
PROCEEDINGS OF THE 6TH SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1969,
PGS. 91-101

- 242 LIN, S.
COMPUTER SOLUTIONS OF THE TRAVELING SALESMAN PROBLEM
BELL SYSTEM TECHNICAL JOURNAL, VOLUME 44 (1965), PGS. 2245-2269
- 243 LINDERS, J.G. AND VANCLEEMPUT, W.M.
AN INTERACTIVE SYSTEM FOR COMPUTER AIDED DESIGN OF PRINTED CIRCUIT BOARDS
PROCEEDINGS OF THE ACM ANNUAL CONFERENCE, 1972, BOSTON
- 244 LITTLE, J.D.C., MURTY, K.G., SWEENEY, D.W., AND KAREL, C.
AN ALGORITHM FOR THE TRAVELING SALESMAN PROBLEM
JOURNAL OF OPERATIONS RESEARCH, VOLUME 11 (NOVEMBER 1963), PGS. 972-989
- 245 LIU, C.L.
INTRODUCTION TO COMBINATORIAL MATHEMATICS
MCGRAW HILL BOOK COMPANY, NEW YORK, 1968
- 246 LLEWELLYN, R.W.
OPTIMUM ROUTES THROUGH NETWORKS
IN LINEAR PROGRAMMING, HOLT, RINEHARD, AND WINSTON, N.Y., 1964, PGS. 335-340
- 247 LOBERMAN, H. AND WEINBERGER, A.
FORMAL PROCEDURES FOR CONNECTING TERMINALS WITH A MINIMUM TOTAL WIRE LENGTH
JOURNAL OF THE ACM, VOLUME 4 (OCTOBER 1957), PGS. 428-437
- 248 LODATO, V.A.
THE MINIMISATION OF DISTANCE IN PLACEMENT ALGORITHMS
COMPUTER JOURNAL, VOLUME 14 (1971), PGS. 206-262
- 249 LUCCIO, F.
ON SOME ITERATIVE METHODS FOR THE DETERMINATION OF OPTIMAL PATHS THROUGH
A NETWORK
CALCOLO, VOLUME 3 (1966), PGS. 31-48
- 250 LUCCIO, F. AND SAMI, M.
ON THE DECOMPOSITION OF NETWORKS IN MINIMALLY INTERCONNECTED NETWORKS
IEEE TRANSACTIONS ON CIRCUIT THEORY, VOLUME CT-16, NUMBER 2 (MAY 1969),
PGS. 184-189
- 251 LYNN, D.K.
COMPUTER AIDED DESIGN FOR LARGE-SCALE INTEGRATED CIRCUITS
COMPUTER, MAY-JUNE 1972, PGS. 36-45
- 252 LYNN, D.K.
COMPUTER AIDED LAYOUT SYSTEM FOR INTEGRATED CIRCUITS
IEEE TRANSACTIONS ON CIRCUIT THEORY, VOLUME CT-18, NUMBER 1, (JANUARY 1971),
PGS. 128-139
- 253 LYSKITT, V.S.
ALGORITHMIC DESIGN OF DIGITAL COMPUTING DEVICES
BOOK PUBLISHED IN THE SERIES SPOORSHTENIA PO BYCHISLITELNOI TEHNIKI BY THE
COMPUTING CENTRE OF THE ACADEMY OF SCIENCES OF THE UNION OF SSR, MOSCOW,
1963, VYPUK 2
- 254 MCGINNIS, D.J.
AUTOCHECK PROGRAM, PROGRAM TO CHECK VALIDITY OF PRINTED CIRCUIT CARDS AND
CIRCUIT USAGE
PROCEEDINGS OF THE ACM ANNUAL CONFERENCE, 1972, BOSTON
- 255 MCLEAN, M.E.
AUTODESIGN AUTOMATED WIRING DESIGN SYSTEM
PROCEEDINGS OF THE ACM 15TH NATIONAL MEETING, AUGUST, 1960
- 256 MACKINTOSH, I.M. AND GREEN, D.
PROGRAMMED INTERCONNECTIONS-A RELEASE FROM TYRANNY
PROCEEDINGS OF THE IEEE, VOLUME 52 (1964), PGS. 1448-1450
- 257 MAH, L. AND STEINBERG, L.
TECHNIQUES OF GATE ASSIGNMENT
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1972,
DALLAS, PGS. 63-67

- 258 MAH, L. AND STEINBERG, L.
TOPOLOGICAL CLASS ROUTING FOR PRINTED CIRCUIT BOARDS
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1972,
DALLAS, PGS. 80-93
- 259 MAJORANI, E.
SIMPLIFICATION OF LEES ALGORITHM FOR SPECIAL PROBLEMS
CALCOLO, VOLUME 1 (1964), PGS. 247-256
- 260 MAMELAK, J.S.
THE PLACEMENT OF COMPUTER LOGIC MODULES
JOURNAL OF THE ACM, VOLUME 13 (OCTOBER 1966), PGS. 615-629
- 261 MARCH, C.D.
AUTOMATION OF THE DESIGN AND MANUFACTURE OF A LARGE DIGITAL COMPUTER
ELECTRONICS AND POWER, OCTOBER 1970
- 262 MARKOVITZ, W.D.
MULTILAYER BOARDS BY COMPUTER
ELECTRONIC PRODUCTS, VOLUME 9 (1967), PGS. 92-96
- 263 MARTIN, L.C.
COMPUTER AIDED CIRCUIT LAYOUT AND DESIGN
PROCEEDINGS OF THE 5TH SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1968,
PGS. 7.1-7.16
- 264 MATTISON, R.L.
A HIGH QUALITY, LOW COST ROUTER FOR MOS-LSI
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1972,
DALLAS, PGS 94-103
- 265 MEADE, R.M. AND GELLER, H.
SYSTEM 360 INFLUENCE ON THE DESIGN OF SOLID LOGIC TECHNOLOGY
SOLID STATE DESIGN, VOLUME 6 (JULY 1965), PGS. 21-27
- 266 MELZAK, Z.A.
ON THE PROBLEM OF STEINER
CANADIAN MATHEMATICAL BULLETIN, VOLUME 4 (1961), PGS. 143-148
- 267 MICHIE, D., FLEMING, J.G., AND OLDFIELD, J.V.
A COMPARISON OF HEURISTIC, INTERACTIVE, AND UNAIDED METHODS OF SOLVING A
SHORTEST-ROUTE PROBLEM
MACHINE INTELLIGENCE, AMERICAN ELSEVIER, NEW YORK, 1968, PG. 245
- 268 MIEHLE, W.
LINK LENGTH MINIMIZATION IN NETWORKS
JOURNAL OF OPERATIONS RESEARCH, VOLUME 6 (1958), PGS. 232-243
- 269 MIKAMI, K. AND TABUCHI, K.
A COMPUTER PROGRAM FOR OPTIMAL ROUTING OF PRINTED CIRCUIT CONNECTORS
IFIPS PROCEEDINGS VOLUME H47, 1968 (VOLUME 2, PAGE 1475)
INFORMATION PROCESSING 68, PGS. 1475-1478
- 270 MILLS, G.
A DECOMPOSITION ALGORITHM FOR THE SHORTEST ROUTE PROBLEM
OPERATIONS RESEARCH, VOLUME 14 (1966), PGS. 279-291
- 271 MILLS, G.
A HEURISTIC APPROACH TO SOME SHORTEST ROUTE PROBLEMS
JOURNAL OF THE CANADIAN OPERATIONS RESEARCH SOCIETY, VOLUME 6 (1968), PGS. 20-
25
- 272 MILNE, M.A.
CLUSTER : A PROGRAM FOR STRUCTURING DESIGN PROBLEMS
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1971,
PGS. 242-249
- 273 MINNICK, R.C.
OUTPOINT CELLULAR LOGIC
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME EC-13 (1964), PG. 685

- 274 MINTY, G.J.
A COMMENT ON THE SHORTEST ROUTE PROBLEM
OPERATIONS RESEARCH, VOLUME 5 (1957), PG. 724
- 275 MINTY, G.J.
A VARIANT ON THE SHORTEST ROUTE PROBLEM
OPERATIONS RESEARCH, VOLUME 6 (1958), PGS. 882-883
- 276 MOORE, E.F.
SHORTEST PATH THROUGH A MAZE
ANNALS OF THE COMPUTATION LABORATORY OF HARVARD UNIVERSITY, HARVARD
UNIVERSITY PRESS, CAMBRIDGE, MASS., VOLUME 30 (1959), PGS. 285-292
ALSO BELL SYSTEM MONOGRAPH NUMBER 3523
- 277 MOORE, R.C.
COMPUTER AIDED LAYOUT OF MINISTICK ARTWORK
TECHNICAL MEMO TG-889, JOHNS HOPKINS UNIVERSITY, SILVER SPRINGS, MARYLAND,
FEBRUARY, 1969, ALSO CFSTI AD 648724, 140 PAGES
- 278 MORI, M. AND NISHIMURA, T.
SOLUTION OF THE ROUTING PROBLEM THROUGH A NETWORK BY A MATRIX METHOD WITH
AUXILIARY NODES
TRANSPORTATION RESEARCH, VOLUME 1 (1967), PGS. 165-180
- 279 MUNKRES, J.
ALGORITHMS FOR THE ASSIGNMENT AND TRANSPORTATION PROBLEMS
JOURNAL SIAM, VOLUME 9 (1957), PGS. 32-38
- 280 MURA, A. AND TOMLIJANOVICH, M.
AN INTERACTIVE SYSTEM FOR SEMI-AUTOMATIC ARTWORK GENERATION OF PRINTED CIRCUIT
BOARDS
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973,
PG. 60
- 281 NAKAHARA, H.
COMPUTER AIDED INTERCONNECTION ROUTING
NETWORKS, VOLUME 2, NUMBER 2 (1972), PGS 167-183
- 282 NEMHAUSER, G.L.
A GENERALIZED PERMANENT LABEL SETTING ALGORITHM FOR THE SHORTEST PATH BETWEEN
SPECIFIED NODES
JOURNAL OF MATHEMATICAL ANALYSIS AND APPLICATIONS, VOLUME 38, 1972
- 283 NEWELL, R.G.
AN INTERACTIVE APPROACH TO PIPE ROUTING IN PROCESS PLANTS
PROCEEDINGS OF THE IFIPS, 1971, PGS. 1080-1085
- 284 NICHOLSON, T.A.J.
FINDING THE SHORTEST ROUTE BETWEEN TWO POINTS IN A NETWORK
COMPUTER JOURNAL, VOLUME 9, NUMBER 3 (NOVEMBER 1966), PGS. 275-280
- 285 NICHOLSON, T.A.J.
PERMUTATION PROCEDURE FOR MINIMIZING THE NUMBER OF CROSSINGS IN A NETWORK
PROCEEDINGS OF THE IEE (LONDON), VOLUME 115 (JANUARY 1968), PGS. 21-26
- 286 NIDECKER, H.A. AND SIMON, W.F.
LOGIC PARTITIONING - COMPONENT ASSIGNMENT
PROCEEDINGS OF THE 1968 ACM NATIONAL CONFERENCE, PGS. 211-221
- 287 NINOMIYA, S.
COMPUTER AIDED DESIGN FOR IC COMPUTERS
FUJITSU SCIENTIFIC AND TECHNICAL JOURNAL, VOLUME 5, NUMBER 1 (MARCH 1969)
- 288 NOTZ, W.A. ET AL
LARGE SCALE INTEGRATION : BENEFITTING THE SYSTEMS DESIGNER
ELECTRONICS, FEBRUARY 20, 1967, PGS. 130-141
- 289 NOUR, M.E.
A NEW LINEAR PROGRAMMING TECHNIQUE FOR THE SHORTEST ROUTE PROBLEMS
DOCTORAL DISSERTATION, UNIVERSITY OF PITTSBURGH, 1968

- 290 NUGENT, C.E., VOLLMAN, T.E., AND RUMI, J.
AN EXPERIMENTAL COMPARISON OF TECHNIQUES FOR THE ASSIGNMENT OF FACILITIES TO LOCATIONS
JOURNAL OF OPERATIONS RESEARCH, VOLUME 16 (1968), PGS. 150-173
- 291 OBERUC, R.E.
A PRACTICAL ALGORITHM FOR FINDING SOLUTIONS TO THE TRAVELING SALESMAN PROBLEM
PRESENTED AT THE OPERATIONS RESEARCH SOCIETY OF AMERICA THIRTY-FOURTH NATIONAL MEETING, DENVER, NOVEMBER, 1968
- 292 OESTREICHER, D.
AUTOMATIC PRINTED CIRCUIT BOARD DESIGN
UNIVERSITY OF UTAH COMPUTER SCIENCE DIVISION, UTEC-CSC-72-119, JUNE 1972
- 293 ORE, O.
THE FOUR COLOR PROBLEM
ACADEMIC PRESS, NEW YORK, 1967
- 294 ORE, O.
THEORY OF GRAPHS
AMERICAN MATHEMATICAL SOCIETY, PROVIDENCE, R.I., 1962
- 295 ORR, W.K.
COMPUTER-AIDED DESIGN FOR CUSTOM INTEGRATED SYSTEMS
PROCEEDINGS OF THE FALL JOINT COMPUTER CONFERENCE, 1969, PGS. 599-611
- 296 OUALLINE, C.M. AND JENNINGS, R.M.
PLACEMENT AND INTERCONNECTION OF THINGS SO PLACED
UNIVERSITY OF MICHIGAN SHORT COURSE, APPLICATION OF COMPUTERS TO AUTOMATED DESIGN, JULY 22-24, 1968
- 297 OWENS, A.R.
GRAPH AND PRINTED CIRCUIT IMBEDDINGS-A SURVEY AND BIBLIOGRAPHY
NRL BIBLIOGRAPHY 33, NAVAL RESEARCH LABORATORY, WASHINGTON, D.C., MAY 1, 1969, CFSTI AD-704843
- 298 PALERMO, F.P.
A NETWORK MINIMIZATION PROBLEM
IBM JOURNAL OF RESEARCH AND DEVELOPMENT, VOLUME 5 (1961), PGS. 335-337
- 299 PEARCE, N.
PRINTED CIRCUIT BOARD LAYOUT USING AN INTERACTIVE GRAPHICS TERMINAL
COMPUTER AIDED DESIGN, VOLUME 2 (1970), PGS. 9-18
- 300 PEART, R.M., RANDOLPH, P.H., AND BARTLETT, T.E.
THE SHORTEST ROUTE PROBLEM
OPERATIONS RESEARCH, VOLUME 8 (1960), PGS. 866-868
- 301 PERKO, A.
SOME COMPUTATIONAL NOTES ON THE SHORTEST ROUTE PROBLEM
COMPUTER JOURNAL, VOLUME 8 (1965), PGS. 19-20
- 302 PERSKY, G. AND GUMMEL, H.K.
GRAPHOS - A SYMBOLIC ROUTING LANGUAGE
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973, PGS. 173-181
- 303 PETEANU, V.
AN ALGEBRA OF THE OPTIMAL PATH IN NETWORKS
MATHEMATICA, VOLUME 9 (1967), PGS. 335-342
- 304 PETEANU, V.
OPTIMAL PATHS IN NETWORKS AND GENERALIZATIONS
MATHEMATICA, VOLUME 11 (1969), PGS. 311-327
- 305 PICKRELL, W.E.
A LAMINATE DESIGN SYSTEM
PROCEEDINGS OF THE 2ND SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1965, PGS. 1-10

- 306 PICKRELL, W.E.
AN AUTOMATED INTERCONNECT DESIGN SYSTEM
PROCEEDINGS OF THE FALL JOINT COMPUTER CONFERENCE, 1965, PGS. 1087-1092
- 307 PIERCE, J.F. AND CROWSTON, W.B.
TREE SEARCH ALGORITHMS FOR QUADRATIC ASSIGNMENT PROBLEMS
NAVAL RESEARCH LOGISTICS QUARTERLY, VOLUME 18, NUMBER 1 (MARCH 1971)
- 308 POHL, T.S.
RIDIRECTIONAL AND HEURISTIC SEARCH IN PATH PROBLEMS
DOCTORAL DISSERTATION, STANFORD UNIVERSITY, 1969
- 309 POHL, T.S.
A THEORY OF BI-DIRECTIONAL SEARCH IN PATH PROBLEMS
IBM RESEARCH REPORT RC-2713, DECEMBER 1, 1969
- 310 POHL, T.S.
HEURISTIC SEARCH VIEWED AS A PATH PROBLEM
IBM RESEARCH REPORT RC-2770, JANUARY 26, 1970
- 311 POHL, T.S.
FIRST RESULTS ON THE EFFECT OF ERROR IN HEURISTIC SEARCH
IN MACHINE INTELLIGENCE, VOLUME 5, UNIVERSITY OF EDINBURGH PRESS, EDINBURGH,
1970, PGS. 219-236
- 312 POLLACK, M.
SOLUTIONS OF THE K-TH BEST ROUTE THROUGH A NETWORK-A REVIEW
JOURNAL OF MATHEMATICAL ANALYSIS AND APPLICATIONS, VOLUME 3 (1961), PGS. 547-559
- 313 POLLACK, M.
THE K-TH BEST ROUTE THROUGH A NETWORK
OPERATIONS RESEARCH, VOLUME 9 (1961), PGS. 578-580
- 314 POLLACK, M. AND WIERENSON, W.
SOLUTIONS OF THE SHORTEST-ROUTE PROBLEM - A REVIEW
OPERATIONS RESEARCH, VOLUME 8, PGS. 224-230 (MARCH-APRIL 1960)
- 315 PONENTALE, T.
AN ALGORITHM FOR MINIMIZING BACKBOARD WIRING FUNCTIONS
COMMUNICATIONS OF THE ACM, VOLUME 8, NUMBER 11 (NOVEMBER 1965), PGS. 699-703
- 316 PONENTALE, T.
THE MINIMIZATION OF BACKBOARD WIRING FUNCTIONS
SIAM REVIEW, VOLUME 9, NUMBER 3 (JULY 1967), PGS. 564-568
- 317 PONSTEIN, J.
SELF-AVOIDING PATHS AND THE ADJACENCY MATRIX OF A GRAPH
JOURNAL OF THE SIAM, VOLUME 14 (1966), PGS. 600-609
- 318 PREISS, R.J.
DESIGN AUTOMATION SURVEY
IBM TECHNICAL NOTE TN 00.480, 1960
- 319 PRIM, R.C.
SHORTEST CONNECTION NETWORKS AND SOME GENERALIZATIONS
BELL SYSTEM TECHNICAL JOURNAL, VOLUME 36 (NOVEMBER 1957), PGS. 1389-1401
- 320 PRINCE, M.D.
MAN-COMPUTER GRAPHICS FOR COMPUTER-AIDED DESIGN
PROCEEDINGS OF THE IEEE, VOLUME 54 (1966), PGS. 1698-1708
- 321 RADLEY, P.E.
THE AUTOMATIC DESIGN OF INTERCONNECTION PATTERNS FOR LARGE SCALE INTEGRATION
INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN, INSTITUTION OF ELECTRICAL ENGINEERS, 1969, PGS. 114-121
- 322 RAMAMOORTHY, C.V.
ANALYSIS OF GRAPHS BY CONNECTIVITY CONSIDERATIONS
JOURNAL OF THE ACM, VOLUME 13 (APRIL 1966), PGS. 211-222

- 323 RAMAMOORTHY, C.V.
A STRUCTURAL THEORY OF MACHINE DIAGNOSIS
PROCEEDINGS AFIPS SPRING JOINT COMPUTER CONFERENCE, 1967, PGS. 743-756
- 324 RAO, M.R.
CLUSTER ANALYSIS AND MATHEMATICAL PROGRAMMING
CFSTI AD 697 267
- 325 READ, R.C.
GRAPH THEORY ALGORITHMS
IN GRAPH THEORY AND ITS APPLICATIONS, ACADEMIC PRESS, N.Y., 1970, PGS. 51-78
- 326 REITER, S. AND SHERMAN, G.
DISCRETE OPTIMIZING
JOURNAL OF THE SIAM, VOLUME 13 (SEPTEMBER 1965), PGS. 864-889
- 327 RICE, R.
SYSTEMATIC PROCEDURES FOR DIGITAL SYSTEM REALIZATION FROM LOGIC DESIGN TO PRODUCTION
PROCEEDINGS OF THE IEEE, VOLUME 52 (1964), PG. 1691
- 328 RICHARDS, D.L.
SWAP : A PROGRAMMING SYSTEM FOR AUTOMATIC SIMULATION, WIRING, AND PLACEMENT OF LOGICAL EQUATIONS
PRESENTED AT THE 1967 SHARE DESIGN AUTOMATION WORKSHOP
- 329 RICHARDSON, F.K.
AN INTERACTIVE GRAPHICAL SYSTEM FOR THE DESIGN OF PHOTOMASKS
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1972, PG. 34
- 330 ROCCHIO, J.J.
DOCUMENT RETRIEVAL SYSTEMS-OPTIMIZATION AND EVALUATION
HARVARD UNIVERSITY, PH.D. THESIS, ALSO NSF REPORT ISR-10, CHAPTER 4, HARVARD COMPUTATION LABORATORY, MARCH 1966
- 331 ROCKET, F.A.
A SYSTEMATIC METHOD FOR COMPUTER SIMPLIFICATION OF LOGIC DIAGRAMS
IRE CONVENTION RECORD, PART 2, 1967, PGS. 217-223
- 332 ROSE, N.A.
COMPUTER AIDED DESIGN OF PRINTED WIRING BOARDS
PH.D. THESIS, UNIVERSITY OF EDINBURGH, APRIL 1970
- 333 ROSE, N. AND OLDFIELD, J.V.
PRINTED WIRING BOARD LAYOUT BY COMPUTER
ELECTRONICS AND POWER, OCTOBER 1971, PGS. 376-379
- 334 ROSENTHAL, C.W.
COMPUTING MACHINE AIDS TO A DEVELOPMENT PROJECT
IEEE TRANSACTIONS ON ELECTRONIC COMPUTERS, VOLUME EC-10 (SEPTEMBER 1961), PGS. 400-406
- 335 ROSS, D.T. AND RODRIGUEZ, J.E.
THEORETICAL FOUNDATIONS FOR THE COMPUTER-AIDED DESIGN SYSTEMS
AFIPS CONFERENCE PROCEEDINGS, VOLUME 23 (1963), PGS. 305-322
- 336 ROSSMAN, M.J. AND TWERY, R.J.
COMBINATORIAL PROGRAMMING
ABSTRACT JOURNAL OF THE OPERATIONS SOCIETY OF AMERICA, 6TH ANNUAL MEETING
- 337 ROZENBERG, D.P. AND RUPP, J.S.
THE AUTOMATIC ROUTING OF MULTIPLE PLACE WIRING
IBM REPORT NUMBER 64-825-1159, FEDERAL SYSTEMS DIVISION, 1964
IBM SPACE GUIDANCE CENTER, REPORT 64-825-1159, OWEGO, N.Y., SEPTEMBER 1964
- 338 RUBIN, F.
PRINTED WIRE ROUTING FOR MULTILAYER CIRCUIT BOARDS
DOCTORAL DISSERTATION, SYRACUSE UNIVERSITY, JUNE 1972
- 339 RUBIN, F.
ASSIGNING WIRES TO LAYERS OF A PRINTED CIRCUIT BOARD
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973, PGS. 22-32

- 340 RUSSELL, S.
ALGORITHMIC CONCEPTS FOR CIRCUIT LAYOUT BY DIGITAL COMPUTER
PRESENTED AT THE 1963 IBM WORKSHOP ON ROUTING AND PLACEMENT
- 341 RUSSO, R.L.
ON THE TRADEOFF BETWEEN LOGIC PERFORMANCE AND CIRCUIT TO PIN RATIO FOR LST
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-21, (FEBRUARY 1972), PGS. 147-153
- 342 RUSSO, R.L., ODEN, P.H., AND WOLFF, P.K.
A HEURISTIC PROCEDURE FOR THE PARTITIONING AND MAPPING OF COMPUTER LOGIC
GRAPHS
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-20, NUMBER 12 (DECEMBER 1971)
- 343 RUSSO, R.L. AND WOLFF, P.K.
ALMS : AUTOMATED LOGIC MAPPING SYSTEM
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1971,
PGS. 118-130
- 344 RUTMAN, R.A.
AN ALGORITHM FOR PLACEMENT OF INTERCONNECTED ELEMENTS BASED ON MINIMUM WIRE
LENGTH
PROCEEDINGS OF THE SPRING JOINT COMPUTER CONFERENCE, 1964, PGS. 477-491
- 345 SAKAROVITCH, M.
THE K SHORTEST ROUTES AND K SHORTEST CHAINS IN A GRAPH
OPERATIONS RESEARCH CENTER REPORT ORC 66-32, UNIVERSITY OF CALIFORNIA,
BERKELEY, OCTOBER 1966, CFSTI AD-642823
- 346 SAKSENA, J.P. AND KUMAR, S.
THE ROUTING PROBLEM WITH K SPECIFIED NODES
OPERATIONS RESEARCH, VOLUME 14 (1966), PGS. 909-913
- 347 SASS, W. AND KROSNER, S.
AN 1130-BASED LOGIC, LAYOUT AND EVALUATION SYSTEM
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 22-25,
1970, SAN FRANCISCO, PGS. 64-70
- 348 SCANLON, F.T.
AUTOMATED PLACEMENT OF MULTITERMINAL COMPONENTS
PROCEEDINGS OF THE SHARE / ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1971
- 349 SCHULER, D.M.
THE CLUSTERING OF INTERCONNECTED NODES
GENERAL TELEPHONE AND ELECTRONICS LABORATORIES TECHNICAL MEMORANDUM 70-468.1,
DECEMBER, 1970
- 350 SCHULER, D.M. AND ULRICH, E.G.
CLUSTERING AND LINEAR PLACEMENT
PROCEEDINGS OF THE ACM / IEEE DESIGN AUTOMATION WORKSHOP, JUNE 26-28, 1972,
DALLAS, PGS. 50-56
- 351 SCHUSTER, N. AND REIMAN, W.
MULTILAYER ETCHED LAMINATES IN HIGH DENSITY ELECTRONIC EQUIPMENT
LITTON INDUSTRIES, PRESENTED AT THE ELECTRONIC CIRCUIT PACKAGING SYMPOSIUM,
UNIVERSITY OF COLORADO, AUGUST 18-19, 1960, PGS. 437-471
- 352 SCHWEIKERT, D.G. AND KERNIGHAN, R.W.
A PROPER MODEL FOR THE PARTITIONING OF ELECTRICAL CIRCUITS
PROCEEDINGS OF THE ACM / IEEE DESIGN AUTOMATION WORKSHOP, 1972, PGS. 57-62
- 353 SCOTT, A.J.
THE OPTIMAL NETWORK PROBLEM : SOME COMPUTATIONAL PROCEDURES
TRANSPORTATION RESEARCH, VOLUME 3 (1969), PGS. 201-210
- 354 SHAFER, O.B.
REDUCING WIRING LENGTHS
ELECTRO TECHNOLOGY, OCTOBER, 1962, PGS. 92-95
- 355 SHANNON, C.E.
PRESENTATION OF THE MAZE-SOLVING MACHINE
TRANSACTIONS OF THE 8TH CYBERNETICS CONFERENCE, JOSIAH MACY, JR., FOUNDATION,
NEW YORK, 1952, PGS. 173-180

- 356 SHAPIRO, D.
ALGORITHMS FOR THE SOLUTION OF THE OPTIMAL COST TRAVELING SALESMAN PROBLEM
SC. D. THESIS, WASHINGTON UNIVERSITY, 1966
- 357 SHEPERD, W.
MAZES AND LABYRINTHS
DOVER, NEW YORK, 1961
- 358 SILVER, R.
AN ALGORITHM FOR THE ASSIGNMENT PROBLEM
COMMUNICATIONS OF THE ACM, VOLUME 3 (NOVEMBER 1960), PGS. 605-606
- 359 SMIDT, R.M. AND REIS, I.L.
SYMBOLIC LOGIC AND PLANT LOCATION
JOURNAL OF INDUSTRIAL ENGINEERING, VOLUME 14 (1956), PGS. 59-66
- 360 SO, H.C.
PIN ASSIGNMENT OF CIRCUIT CARDS AND THE ROUTABILITY OF MULTILAYER PRINTED
WIRING BACKPLANES
PROCEEDINGS OF THE 10TH DESIGN AUTOMATION WORKSHOP, JUNE 1973,
PGS. 33-43
- 361 SOLOMON, E.W.
A COMPREHENSIVE PROGRAM FOR NETWORK PROBLEMS
COMPUTER JOURNAL, VOLUME 3 (1960), PGS. 89-97
- 362 SPANDORFER, L.J. AND MURPHY, J.V.
SYNTHESIS OF LOGIC FUNCTIONS ON AN ARRAY OF INTEGRATED CIRCUITS
UNIVAC ENGINEERING CENTER SCIENTIFIC REPORT NUMBER 1, OCTOBER 31, 1963
ALSO U.S. DEPARTMENT OF COMMERCE, GOVERNMENT REPORT AD 431017
- 363 SPITALNY, A.J. AND GOLDBERG, M.J.
ON-LINE GRAPHICS APPLIED TO LAYOUT DESIGN OF INTEGRATED CIRCUITS
PROCEEDINGS OF THE IEEE, VOLUME 55 (1967), PGS. 1982-1988
- 364 STEIGLITZ, K. AND WEINER, P.
SOME IMPROVED ALGORITHMS FOR COMPUTER SOLUTION OF THE TRAVELING SALESMAN
PROBLEM
PROCEEDINGS OF THE 6TH ANNUAL ALLERTON CONFERENCE, OCTOBER 1968, PGS. A14-A21
- 365 STEINBERG, L.
THE BACKBOARD WIRING PROBLEM : A PLACEMENT ALGORITHM
SIAM REVIEW, VOLUME 3, NUMBER 1 (JANUARY 1961), PGS. 37-50
- 366 STEVENS, J.E.
FAST HEURISTIC TECHNIQUES FOR PLACING AND WIRING PRINTED CIRCUIT BOARDS
PH.D. THESIS, COMPUTER SCIENCE DEPARTMENT, UNIVERSITY OF ILLINOIS, 1972
- 367 STONE, A.J.
PARTITIONING OF LOGIC INTO PHYSICAL ENTITIES
PROCEEDINGS OF THE SHARE DESIGN AUTOMATION WORKSHOP, 1966
- 368 SUTHERLAND, I.E.
A METHOD FOR SOLVING ARBITRARY WALL MAZES BY COMPUTER
IEEE TRANSACTIONS ON COMPUTERS, VOLUME C-18, NUMBER 12 (DECEMBER 1969),
PGS. 1092-1097
- 369 SWEN, G.E.
DEVELOPMENT OF THE SPANNING TREE CONCEPT WITH APPLICATIONS TO THE SHORTEST
ROUTE PROBLEM
DOCTORAL DISSERTATION, UNIVERSITY OF PITTSBURGH, 1968
- 370 THOMPSON, S.A.
CAD GRAPHICS : CIRCUITS MADE TO ORDER
THE ELECTRONICS ENGINEER, AUGUST, 1969
- 371 THORELLI, L.
AN ALGORITHM FOR COMPUTING ALL PATHS IN A GRAPH
BIT, VOLUME 6 (1966), PGS. 347-349

- 372 TIGHE, M.F.
MAZE SEARCH : A PROGRAM THAT SOLVES N DIMENSIONAL MAZES
COMPUTERS AND AUTOMATION, VOLUME 19 (FEBRUARY 1970), PGS. 22-24
- 373 TRIER, P.E.
COMPUTER AIDED DESIGN IN ELECTRONICS
PROCEEDINGS OF THE IEE, VOLUME 119 (JANUARY 1972), PGS. 17-27
- 374 UHLIK, R.J.
GRAPHIC UPDATE OF AUTOMATED LOGIC DIAGRAMS
IBM TECHNICAL REPORT TR 00.1747, POUGHKEEPSIE, NEW YORK, JUNE 12, 1968
- 375 URBAN, S.
EFFECTIVE USE OF A COMPUTER AIDED DESIGN SYSTEM
PROCEEDINGS OF THE SHARE / ACM / IFEE DESIGN AUTOMATION WORKSHOP, JUNE 22-25, 1970, SAN FRANCISCO, PGS. 243-249
- 376 VAJDA, S.
MATHEMATICAL PROGRAMMING
ADDISON-WESLEY PUBLISHING COMPANY, READING, MASS, 1961
- 377 VERBLUNSKY, S.
ON THE SHORTEST PATH THROUGH A NUMBER OF POINTS
PROCEEDINGS OF THE AMERICAN MATHEMATICAL SOCIETY, VOLUME 2 (1951), PGS. 904-913
- 378 WALKER, A., EDITOR
ADVANCES IN ELECTRONIC CIRCUIT PACKAGING
PLENUM PRESS
- 379 WALLACE, P.A.
THE MAZE SOLVING COMPUTER
PROCEEDINGS ACM ANNUAL MEETING, PITTSBURGH, 1952, PGS. 119-125
- 380 WARSHAWSKY, E.H.
OPTIMIZATION PROBLEMS
PROCEEDINGS OF THE DESIGN AUTOMATION SEMINAR, SPONSORED BY MESA SCIENTIFIC CORPORATION, 2930 WEST IMPERIAL HIGHWAY, INGLEWOOD, CALIFORNIA, 1964, PGS. 69-105
- 381 WARBURTON, C.R.
AUTOMATION OF LOGIC PAGE PRINTING
PRESENTED AT THE 1961 AIEE SUMMER GENERAL MEETING, PAPER CP61-726
- 382 WEIMER, D.L.
A SERIAL TECHNIQUE TO DETERMINE MINIMUM PATHS
COMMUNICATIONS OF THE ACM, VOLUME 4 (1963), PGS. 664-666
- 383 WEINBERG, L.
MICROELECTRONICS AND PRINTED CIRCUITS : PROBLEMS AND THEIR SOLUTIONS
PROCEEDINGS OF THE SHARE / ACM / IFEE DESIGN AUTOMATION WORKSHOP, WASHINGTON, 1968
- 384 WEINBERGER, A. AND LOBERMAN, H.
SYMBOLIC DESIGNATIONS FOR ELECTRICAL CONNECTIONS
JOURNAL OF THE ACM, VOLUME 4 (OCTOBER 1957), PGS. 420-437
- 385 WEINDLING, M.N.
A COMPUTER SYSTEM FOR THE AUTOMATIC OPTIMAL DESIGN OF AN ELECTRONIC SYSTEM
DOUGLAS MISSILE AND SPACE SYSTEMS DIVISION, SANTA MONICA, CALIFORNIA, PAPER 1822
- 386 WEINDLING, M.N.
A METHOD FOR BEST PLACEMENT OF UNITS ON A PLANE
PROCEEDINGS OF THE SHARE DESIGN AUTOMATION WORKSHOP, 1964
ALSO DOUGLAS AIRCRAFT COMPANY PAPER 3109, DOUGLAS AIRCRAFT COMPANY, SANTA MONICA, CALIFORNIA
(OR PAPER 3108)
- 387 WEINDLING, M.N. AND GOLOMB, S.W.
MULTILAMINAR GRAPHS
DOUGLAS MISSILE AND SPACE SYSTEMS DIVISION, PAPER NUMBER 3594, SEPTEMBER, 1965

- 388 WEISSMAN, J.
BOOLEAN ALGEBRA, MAP COLORING, AND INTERCONNECTIONS
AMERICAN MATHEMATICAL MONTHLY, VOLUME 69 (1962), PGS. 608-613
- 389 WEISSMAN, J.
BOOLEAN ALGEBRA, MAP COLORING, AND INTERCONNECTIONS
AUTONETICS DEPARTMENT 3341-51, ANAHEIM, CALIFORNIA
- 390 WEISSMAN, J.
THE MATHEMATICAL BASIS OF THE AUTONETICS ETCHED INTERCONNECTION DESIGN PROGRAM
PAPER NUMBER 7, DEPARTMENT 3341-51, AUTONETICS, ANAHEIM, CALIFORNIA
- 391 WEST, L.E. AND CASKEY, D.L.
TOPOGRAPHIC SIMULATION AS AN AID TO PRINTED CIRCUIT BOARD DESIGN
HAIDE 5TH ANNUAL MEETING, 1966, PGS. III-1 TO III-30
- 392 WHITING, P.D. AND HILLIER, J.A.
A METHOD FOR FINDING THE SHORTEST ROUTE THROUGH A ROAD NETWORK
OPERATIONAL RESEARCH QUARTERLY, VOLUME 11 (1960), PGS. 37-40
- 393 WILBER, D.A. AND ZANE, R.
PUZZLE ! A PROGRAM FOR COMPUTER AIDED DESIGN OF PRINTED CIRCUIT ARTWORK
UCRL 17814, SEPTEMBER 12, 1967
ALSO HAWAII INTERNATIONAL CONFERENCE ON SCIENCE, HONOLULU, JANUARY 29-31, 1968
- 394 WING, OMAR
ALGORITHM TO FIND THE MOST RELIABLE PATH IN A NETWORK
IBM RESEARCH REPORT RC-300, YORKTOWN HEIGHTS, N.Y., AUGUST 8, 1960
- 395 WISE, D.J.K.
LIDO-AN INTEGRATED SYSTEM FOR COMPUTER LAYOUT AND DOCUMENTATION OF DIGITAL ELECTRONICS
INTERNATIONAL CONFERENCE ON COMPUTER AIDED DESIGN, IEEE, 1969, PGS. 72-81
- 396 WISEMAN, N.E.
APPLICATION OF LIST PROCESSING METHODS TO THE DESIGN OF INTERCONNECTIONS FOR A FAST LOGIC SYSTEM
COMPUTER JOURNAL, VOLUME 6 (1964), PG. 321
- 397 WOLLMER, R.
REMOVING ARCS FROM A NETWORK
OPERATIONS RESEARCH, VOLUME 12 (1964), PGS. 934-940
- 398 YAMADA, H.
COMPUTER APPLICATION TO THE DESIGN OF ELECTRONIC CONTROL EQUIPMENT
FUJITSU SCIENTIFIC AND TECHNICAL JOURNAL, VOLUME 3, NUMBER 1 (MARCH 1967)
- 399 YEN, J.Y.
SOME ALGORITHMS FOR FINDING THE SHORTEST ROUTES THROUGH THE GENERAL NETWORKS
IN COMPUTING METHODS IN OPTIMIZATION PROBLEMS, VOLUME 2, ACADEMIC PRESS,
NEW YORK, 1968, PGS. 377-388
- 400 YEN, J.Y.
AN ALGORITHM FOR FINDING SHORTEST ROUTES FROM ALL SOURCES TO A GIVEN
DESTINATION IN GENERAL NETWORKS
QUARTERLY JOURNAL OF APPLIED MATHEMATICS, VOLUME 27 (1970), PGS. 526-530
- 401 YOUNG, S.P. AND ECKBERG, A.E.
SURVEY OF LITERATURE ON INTERCONNECTION, COMPONENT PLACEMENT, AND LOGIC
PARTITIONING
RAYTHEON MISSILE SYSTEMS, DIGITAL SYSTEMS DEPARTMENT, MEMO SY-3-69, APRIL 4,
1969

THE CURRENT STATUS AND FUTURE WORK
OF DESIGN AUTOMATION IN JAPAN

BY

Stephen Y. H. Su, Staff Consultant
Design Automation
UNIVAC
P. O. Box 500
Blue Bell, Penna. 19422

The Japanese computer industry is very active and has done a great deal of work in the Design Automation area. The author has had the opportunity to talk to some of the people working for the leading Japanese computer manufacturers.

The purpose of this article is to provide the readers with information about the recent Design Automation activities and future trend of work in this area in Japan.

I. PRESENT STATUS

(1) Design Language:

As of July, 1973 there existed no design language for automated logic and system design in the Japanese computer industry. Professor T. Motooka of the University of Tokyo has initiated some research in the design language area.

(2) Design Language Translator (hardware compiler)

As of July, 1973 there was no working hardware compiler in Japan.

(3) System and Logic Level Simulator

As far as can be determined, there is no working System Simulator in Japan. Most of the companies have logic level simulators capable of performing parallel simulation.

(4) Logic design automation system

To my knowledge, no program exists for automated logic synthesis using multiple-level NAND networks with fan-in, fan-out constraints (1) or a library of IC chips (2).

(5) Test generation

Most of the manufacturers have computer programs for generating tests for detecting and locating single stuck-type (stuck-at-1 and stuck-at-0) failure in a combinational or a sequential network. The tests for the last few percentages of faults are being done by hand in most of the companies. No program for detecting multiple faults has been reported. D-algorithm is being used by some companies.

(6) Card Design

- a. Partitioning, for the most part, is still being done manually.
- b. Packaging is being done automatically by most of computer manufacturers. It consists of the placement of IC modules, the assignment of IC pins and the assignment of package terminal.
- c. Routing and artwork generation are being done automatically.

II. APPLICATION OF DESIGN AUTOMATION SYSTEMS IN JAPAN

- a) As a result of a high speed and high density requirement of the logic equipments, there is a growing trend to increase the phases of the design cycle where computer aided design techniques can make the most significant impact in the computer design area.
- b) Experience has dictated the following requirements for a Design Automation System:
 - (1) Automation of the logic and system design aspects of computer design.
 - (2) D.A. System should follow technical innovations in hardware design.
 - (3) Simplicity of usage of D.A. Systems is a must.

- (4) The design engineer must be able to devote his efforts to the creative work in the systems design area leaving the tedious calculations and routine design efforts to the computer.
- (5) Minimization of quantity of documents produced by a D.A. System is a necessity; however, the documents should be self explanatory.
- (6) Maximum utilization of man-machine interfaces by the D.A. System should be encouraged.
- (7) Adaptability of the design automation system to allow for changes in the physical design techniques.

III. FUTURE WORK - Design Automation areas in which the Japanese computer industry is expected to concentrate its efforts are:

1. Computer-aided logic and system design

This is one of the most popular subjects of common interest among Japan computer manufacturers and universities. This work includes investigation of design languages and hardware compilers for the design languages.

2. Microprogramming D.A.
3. Automated Partitioning
4. MSI and LSI oriented packaging techniques
5. (a) General purpose data base optimal host language
(b) PL/I has not been but will be used
6. Interactive design via graphical terminals and teletypes
7. Efficient System Simulation and evaluation techniques
8. New, efficient logic synthesis algorithm
9. Data base: data structure and data description language

IV. COMMENTS

The current trend is toward the automation of high level design (system and logic design). In other words, the goal is to generate the system and logic diagrams with minimum amounts of human intervention. Such observation is obtained mainly from two sources: (1) After the author of this paper presented the paper, "An Interactive Design Automation System" (A system for computer-aided analysis and logic design of digital networks) at the 10th Annual Design Automation Workshop on June 27, 1973, many people from various countries expressed their interests in this area and requested more detailed information and (2) It was pointed out in the final Panel Discussion

Session (consisting of all Session Chairmen and the D.A. Workshop Committee) that computer-aided logic and system design is an important goal to achieve. Clearly, it is a gap to be bridged in order to obtain a total design automation system.

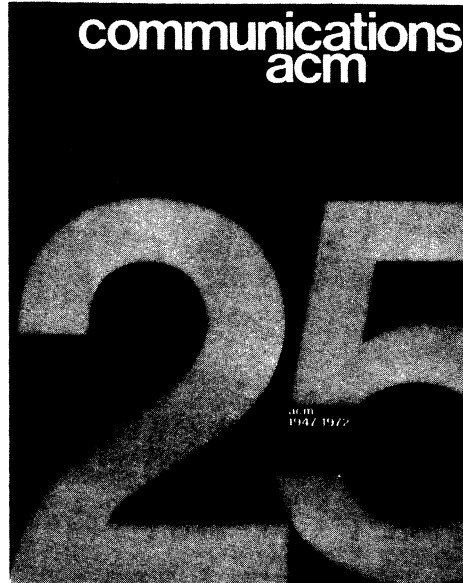
One of the biggest problems in computer design is the mismatch between software and hardware. Therefore, future design automation systems should emphasize integrated hardware, software and firmware design. Our goal is to have a design automation system which is capable of modeling and generating not only hardware but also software and firmware. A multi-level modeling philosophy and design language has been presented in (3). A system is considered to have a control part and a structure part. The designer can specify his design in any level of detail he wants. The language is relatively simple and is suitable for an interactive environment. The language, in its present form, is for logic and system hardware design. Future work includes using basically the same modeling philosophy for modeling and generation of firmware and software.

References

1. S. Y. H. Su and C. W. Nam, "Computer-aided Synthesis of Multiple Output Multi-level NAND Networks with Fan-in and Fan-out Constraints," IEEE Transactions on Computers, Vol. C-21, pp. 1445-1455, December, 1971.
2. P. R. Schneider and D. L. Dietmeyer, "An Algorithm for Synthesis of Multiple-output Combinational Logic," IEEE Transactions on Computers, Vol. C-17, pp. 117-128, February, 1968.
3. M. B. Baray and S. Y. H. Su, "A Digital System Modeling Philosophy and Design Language," Proceedings of the 8th Annual Design Automation Workshop, pp. 1-22, 1971.

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