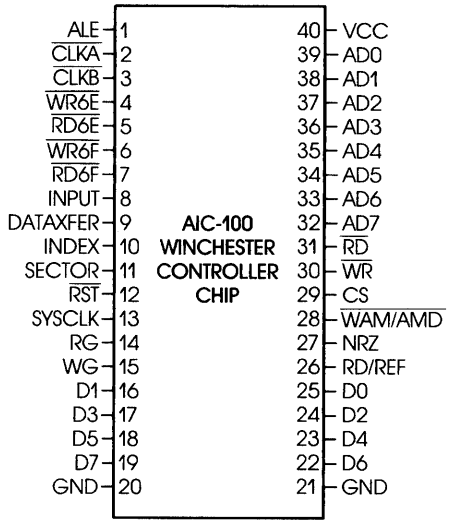
Winchester Disk Controller

AIC-100 & AIC-100-10

PRELIMINARY

- Controls ST506/412, SA1000, ST412HP, ESDI and SMD, Interface Drives
- 32-bit ECC Internal Polynomial
- 5 Mbits/sec and 10 Mbits/sec Transfer Rate Versions
- Soft or Hard Sector Drives
- Multiple Sector Transfer
- Sector Level Defect Handling
- Non-interleaved Operation
- Sector Lengths in Multiples of 128 Bytes
- High Speed Search Capability
- Single +5V Power



DESCRIPTION

The Adaptec AIC-100 Winchester Disk Controller is a LSI component that provides the major portion of hardware necessary to build a Winchester disk controller. The chip is capable of supporting most drive interfaces including, but not limited to, ST506/412, ESDI, SMD, SA1000, and ST412-HP.

The AIC-100 forms the nucleus of a three chip set comprised of the AIC-100, AIC-250 and the AIC-300. These chips along with a data separator, driver/receivers, and a microprocessor chip provide all that is required to implement a full-featured, high performance disk controller. Typically, most implementations are able to read or write a full track in one revolution, run commonly available drives at their performance limits and, in fact, tend to put the performance bottleneck within the limitations of the system, as opposed to those of the controller.

The AIC-100 performs the basic read/write functions for a disk drive. For this purpose, the chip provides the necessary serialization/deserialization, formatting, ECC generation and correction functions. In addition, the AIC-100 also has search and verify capabilities.

The AIC-250 provides the write precompensation, write address mark/address mark detect and NRZ to MFM conversion functions required in ST506/412 type of drive interface applications.

The AIC-300 provides a dual-ported buffer controller function in systems whose available bus bandwidth requires the use of a buffer between the host bus and the controller.

Figure 1 shows a simplified block diagram of an ST412/506 controller using the three chip set.

The AIC-100 is designed to work with either a local processor or the host processor. This choice is up to the designer and is a function of the host system's available bus bandwidth and board space design considerations. Accordingly the microcode for the control of the AIC- 100 will be present in the system ram or a local (ep) rom.

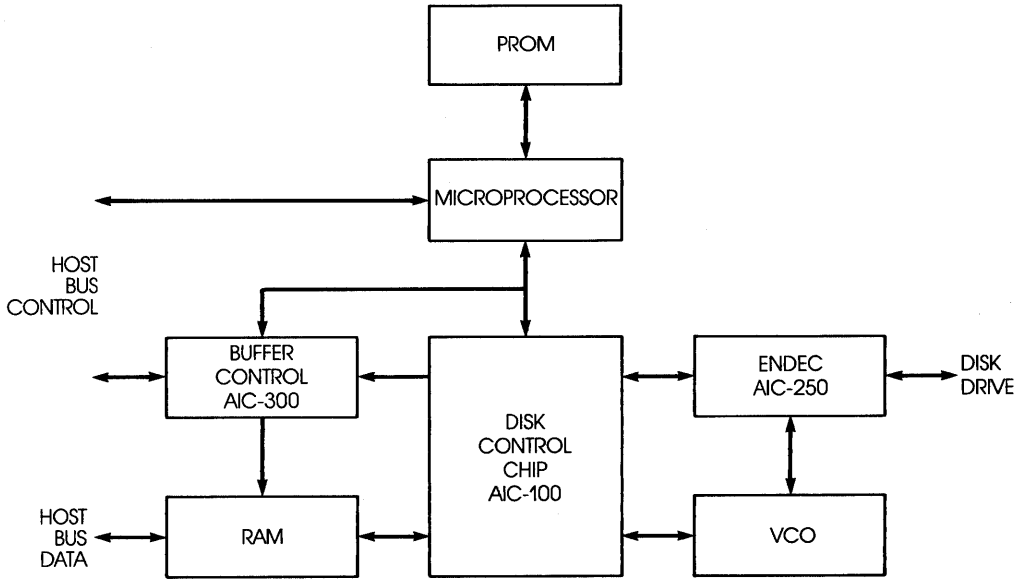


FIGURE 1. SIMPLIFIED WINCHESTER DISK CONTROLLER BLOCK DIAGRAM

AIC-100 PIN DESCRIPTION

SYMBOL	PIN	TYPE	NAME AND FUNCTION
ALE	1	IN	ADDRESS LATCH ENABLE: Signal used to latch the address from the multiplexed address/data bus.
$\overline{\text{CLKA}}$	2	OUT	CLOCK A: During a read or write operation, the output of this signal is equal to the input RD/REF CLK (pin 26)divided by 2. Otherwise, it is equal to the input SYSCLK (pin 13). An additional divide by 2 of RD/REF CLK is invoked when Register 7F is set with FF. The switch between RD/REF and SYSCLK is glitch free.
$\overline{\text{CLKB}}$	3	OUT	CLOCK B: A pulse which overlaps the negative edge of $\overline{\text{CLKA}}$, and occurs whenever a byte is transferred to/from Data Bus pins DO–D7.
$\overline{\text{WR6E}}$	4	OUT	WRITE TO REGISTER 6E: Active while WR is active, providing address 6E is latched internally and the chip is selected.
$\overline{\text{RD6E}}$	5	OUT	READ FROM REGISTER 6E: Active while RD is active, providing address 6E is latched internally and the chip is selected.
$\overline{\text{WR6F}}$	6	OUT	WRITE TO REGISTER 6F: Active while WR is active, providing address 6F is latched internally and the chip is selected.

AIC-100 PIN DESCRIPTION (Continued)

SYMBOL	PIN	TYPE	NAME AND FUNCTION
$\overline{RD6F}$	7	OUT	READ FROM REGISTER 6F: Active while RD is active, providing address 6F is latched internally and the chip is selected.
INPUT	8	IN	INPUT PIN: The state of this pin is sampled by reading Register 7E, bit 4.
DATAXFER	9	OUT	DATA TRANSFER: Active during data transfer on lines DO - D7. Also bit 6 in status Register R79.
INDEX	10	IN	INDEX: Input for the index pulse received from the disk drive. Must be a minimum of 9 RD/REF cycles.
SECTOR	11	IN	SECTOR: Input for the sector pulse received from drives that are hard-sectored. Must be a minimum of 9 RD/REF cycles.
$\overline{RST}$	12	IN	RESET: A low input sets an internal reset latch that stops all operations within the chip and drops RG, WG, WAM and NRZ outputs. Registers 71 through 7E are reset.
SYSCLK	13	IN	SYSCLK: A 1.5 to 2.5 MHz clock input which becomes Clock A output when not reading or writing data.
RG	14	OUT	READ GATE: Enables the external phaselock loop to lock onto the read data stream coming from the drive.
WG	15	OUT	WRITE GATE: Is used to enable or gate the writing of NRZ data out to the disk drive.
DO-D7	16-19 22-25	IN/OUT	DATA BUS: Byte parallel data lines to/from the buffer.
GND	20-21		GROUND
RD/REF CLK	26	IN	READ REFERENCE CLOCK: A multiplexed input sourced from the VFO during read gate, otherwise from the write oscillator. This is the primary clock for the AIC-100.
NRZ	27	IN/OUT	NRZ: Read data input from the disk when RG is active; write data to the disk when WG is active.
$\overline{WAM/AMD}$	28	IN/OUT	WRITE ADDRESS MARK/ADDRESS MARK DETECT: A one bit wide pulse is output when write gate is active and an address mark is to be written. When read gate is active, a low level input indicates address mark detect.
CS	29	IN	CHIP SELECT: Active during processor bus cycles to/from the chip.
$\overline{WR}$	30	IN	WRITE: Signal from the microprocessor to latch data into a specified register.
$\overline{RD}$	31	IN	READ: Signal from the microprocessor to enable data from a specified register out onto the bus.
AD0-AD7	32-39	IN/OUT	Multiplexed address/data lines interfacing to the control processor.
V_{CC}	40		+5 Volts.

FUNCTIONAL DESCRIPTION

Internal to the controller chip are three functional blocks:

- ☐ Microprocessor Interface Decoder
- ☐ Sector Format Sequencer
- ☐ Data Flow

MICROPROCESSOR INTERFACE DECODER: The microprocessor interface is an eight-bit multiplexed bus such as is found on the Intel 8085 family of processors. Other microprocessors such as the Z80 can be utilized by multiplexing their address and data lines, and generating the necessary control lines. There are 19 registers that provide for operation control, ECC control, drive interface and format control. The device architecture is structured to allow the firmware of an NMOS processor to determine what functions are to be incorporated in the control unit design.

SECTOR FORMAT SEQUENCER: The sector format sequencer performs the basic read/write functions for a disk drive which include:

- ☐ Read ID
- ☐ Read ID and Read Data
- ☐ Read ID and Write Data

These functions can be modified to perform the search data and verify data functions.

The track format is the same as that recommended by several disk manufacturers except for the addition of a flag byte in the ID field, providing defect flagging at the sector level, and 4 bytes of ECC rather than 2 CRC bytes. The addition of these bytes in ID and data fields is accommodated by a corresponding decrease in the VFO sync fields. A 256-byte data field requires a total of 315 bytes per sector.

The Winchester controller chip interfaces with the bidirectional data bus which is connected to an external RAM buffer. The CS, WE, and address increment signals required for the sector buffer are derived from the Clock A and Clock B outputs.

DATA FLOW: The data flow portion of the controller chip is composed of a 32-bit ECC and a serializer/deserializer. Data to be written to the disk enters the device in 8-bit parallel format. It is serialized, and run through a 32-bit ECC generator. The controller chip outputs NRZ serial data followed by 4 bytes of ECC check burst.

The 32-bit ECC polynomial is optimized for sector lengths between 256 and 2048 bytes and provides greater data integrity than the traditional "fire code" polynomials. Adaptec's polynomial will correct 8-bit single burst errors with an extremely low probability of miscorrection and a lower probability of undetected errors. This polynomial will also detect double burst errors.

Figure 2 is a block diagram of the AIC-100 controller chip, and identifies the different blocks.

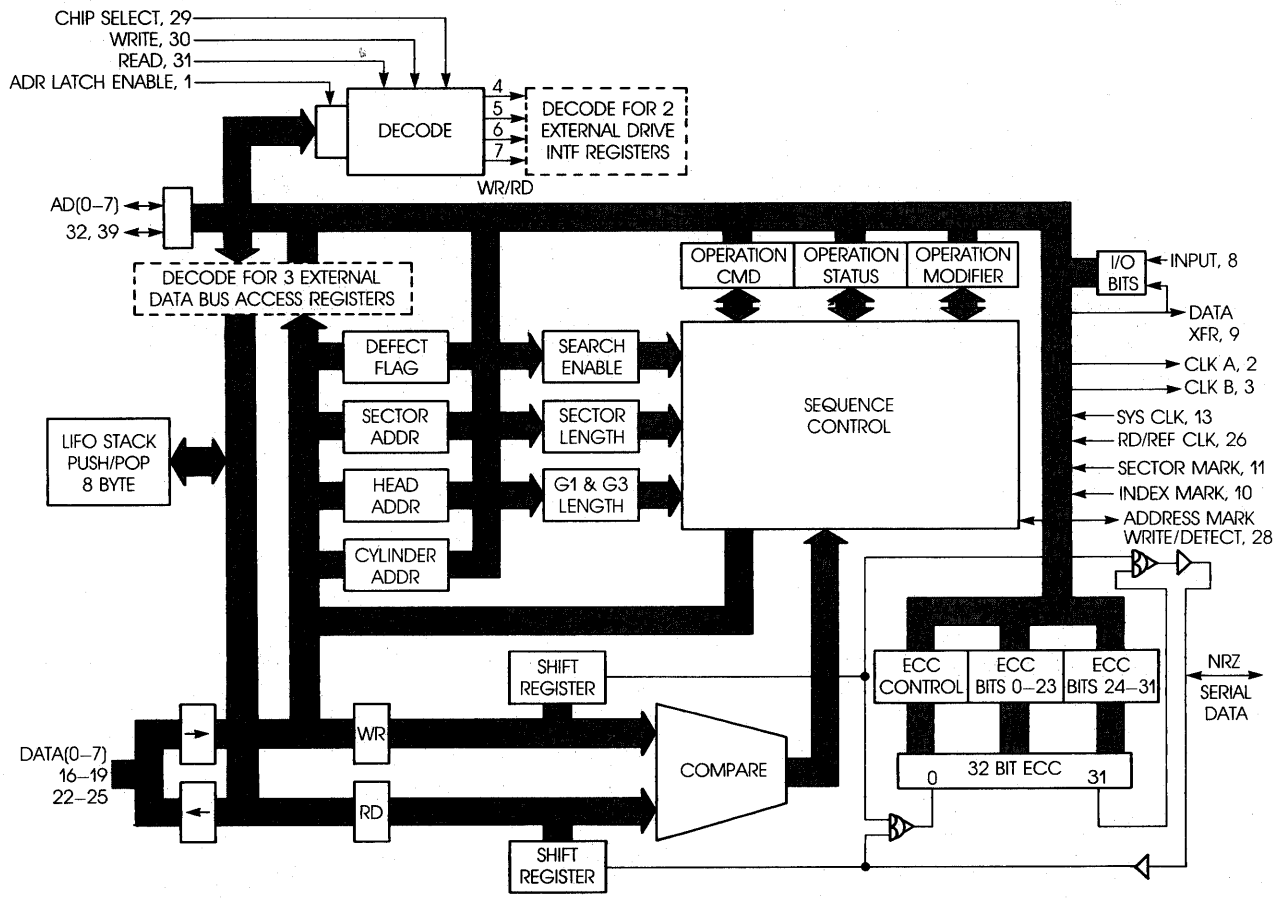


FIGURE 2. AIC-100 BLOCK DIAGRAM

FUNCTIONAL OPERATION

The Winchester controller chip is designed to be used with a low-cost microprocessor rather than the high-speed-bit slice designs required for controllers in the past. This NMOS processor is used to maintain "loose" synchronization with the real time on the disk through the OP Command (R78) and Sequencer Status (R79) registers. The Winchester controller chip in return maintains the "close" synchronization of data to and from the disk and provides the signals necessary to control this path. With this device, a lower total part count can be achieved with the same or greater performance than that of a bit slice processor design.

Because the Winchester controller chip controls primarily the high speed signals associated with the Winchester disk, the designer is free to choose which type of drive to interface, e.g., ST506, SMD, etc. Each of these interfaces can be accommodated with the 4 signal pins RD6E, WR6E, RD6F, and WR6F. The AIC-100 chip simplifies the external logic needed, by internally decoding addresses 6EH and 6FH, and providing signals to read and write ports at these locations.

An example of an ST412 application is shown in Figure 3. These 4 signals are used to read or write drive control lines.

The basic read/write and format sequences are described in the following pages. Note that for the read or write operations a match between the cylinder, head, and sector registers and ID field being read must occur before the operation continues. If a match does not occur, the operation will stop and must be restarted until the desired sector is found. In either case, the last ID field read may be "popped" from the stack (R7F).

If an ECC error is detected after a read data operation, the syndrome is saved in the ECC register and will not be reset until a new read OP is started. By employing Registers 71, 72 and 73, the microprocessor can determine if the error is correctable, and if so, the error pattern and displacement from the beginning of the sector. The ECC polynomial is a computer selected code that will correct 8 bit single burst errors. After the error pattern is determined, it is EXORed with the data byte (bytes) in the RAM buffer.

CLKA, CLKB, and DATAXFER outputs are used to control the external RAM buffer address counter. CLKB should be interpreted as the beginning of a controller chip memory access with a Clock A period equal to the RAM access time +200 ns. The D(0-7) pins will contain valid data during that time of the cycle when CLKA is high. This is shown in the reference timing diagram.

The operation of the chip revolves around the command register, Register 78; and the status/execution register, Register 79. The registers can be grouped by function as follows:

- ☐ Stored Value Registers
- ☐ Command Set-up Registers
- ☐ Command Register, Register 78
- ☐ Status/Execution Register, Register 79
- ☐ External Registers

The table shows the registers in each group and their function. A more detailed graphical breakdown of the registers follows.

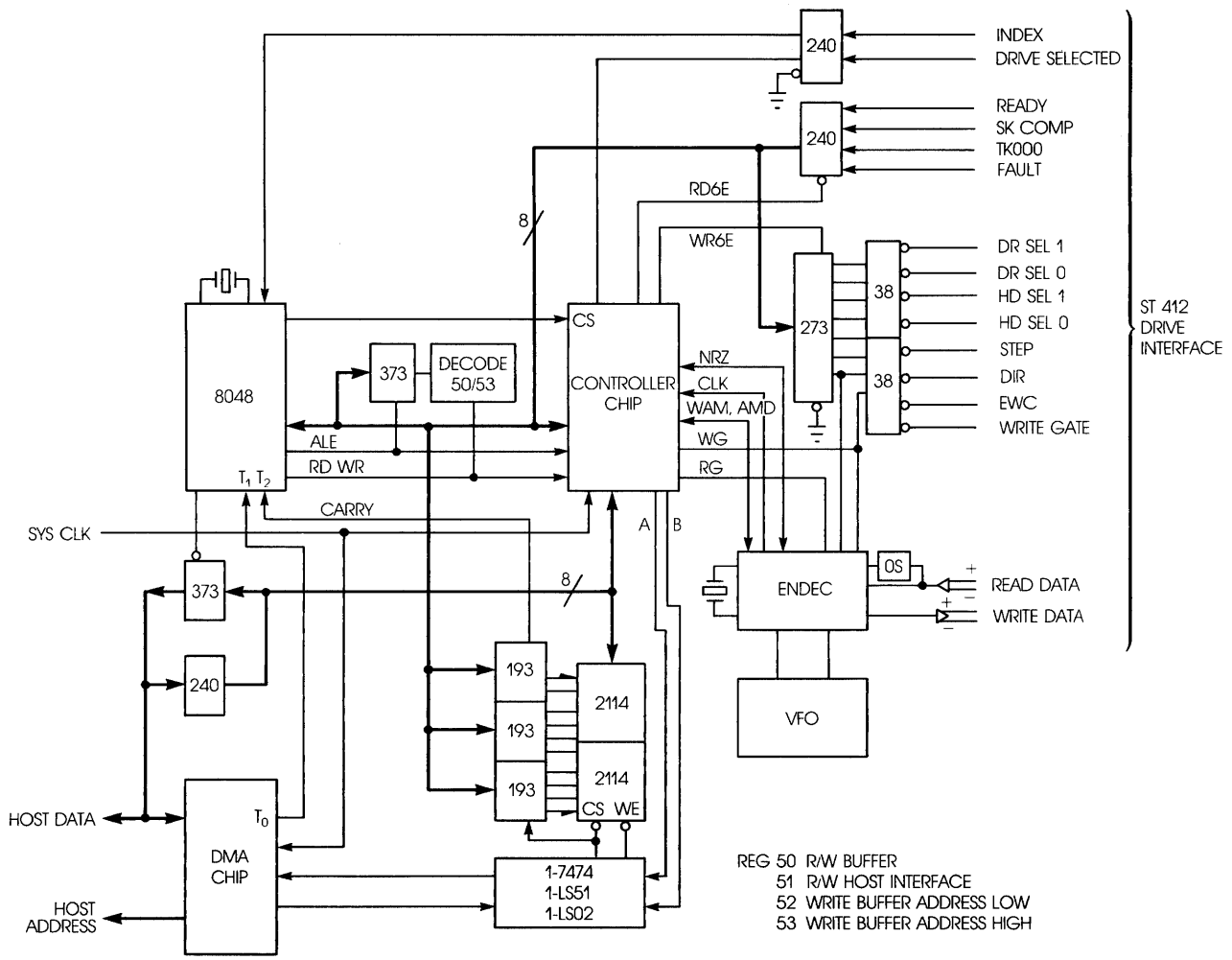


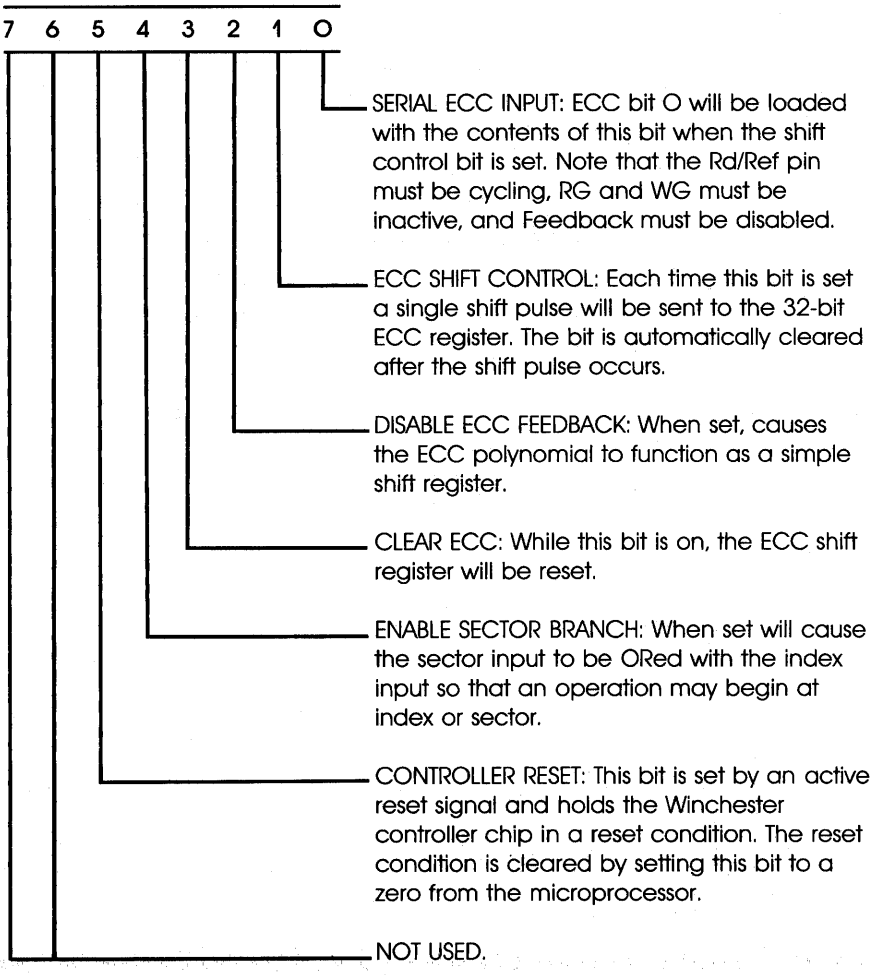
FIGURE 3. AIC-100 ST412 APPLICATION

AIC-100 REGISTER TABLE

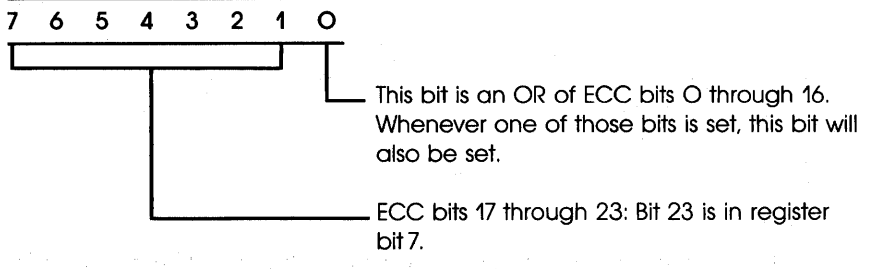
REG	TITLE	R=READ/ W=WRITE	FUNCTION
STORED VALUE REGISTERS			
72	ECC BITS 0-16 "OR"ED, and 17-23	R	SYNDROME BITS
73	ECC BITS 24-31	R	ERROR BITS
D0	GAP LENGTH	W	BIT CONTROL
E0	CYLINDER BYTE	R/W	ID FIELD BYTE
E1	HEAD BYTE	R/W	ID FIELD BYTE
E2	SECTOR BYTE	R/W	ID FIELD BYTE
E3	FLAG BYTE	R/W	ID FIELD BYTE
COMMAND SET-UP REGISTERS			
71	ECC CONTROL	W	CORRECTION CONTROL
74	ECC POLYNOMIAL	W	LOW ORDER BITS
77	ECC POLYNOMIAL	W	HIGH ORDER BITS
7A	OPERATION MODIFIER	R/W	OPERATION CONTROL
7E	SPECIAL I/O	R	INPUT and DATA XFER BITS
7F	POP STACK	R	LIFO STACK READ
7F	CLOCK CONTROL	W	CLKA CONTROL
A4	SEARCH BIT	W	ENABLES SEARCH
C4	SECTOR LENGTH	W	SECTOR DATA FIELD LENGTH
COMMAND REGISTER			
78	OPERATION COMMAND	W	CONTROLS THE SEQUENCING OF THE CONTROLLER CHIP
STATUS/EXECUTION REGISTER			
79	CHIP STATUS	R	MONITOR CHIP STATUS
79	START EXECUTION	W	STARTS CHIP EXECUTION
EXTERNAL REGISTERS			
50	HOST DATA TRANSFER	R/W	ALLOWS PROCESSOR TO R/W DATA DIRECTLY FROM THE HOST.
51	HOST DATA TRANSFER	R/W	EXACTLY LIKE REG 50.
70	BUFFER DATA TRANSFER	R/W	ALLOWS PROCESSOR TO R/W DATA DIRECTLY FROM THE BUFFER.
6E	EXTERNAL LINE CONTROL	R/W	CAUSES THE PINS DESIGNATED RD6E & WR6E TO BE ACTIVATED BY PROCESSOR.
6F	EXTERNAL LINE CONTROL	R/W	SAME AS ABOVE, BUT FOR PINS RD6F AND WR6F.

Internal Register Description

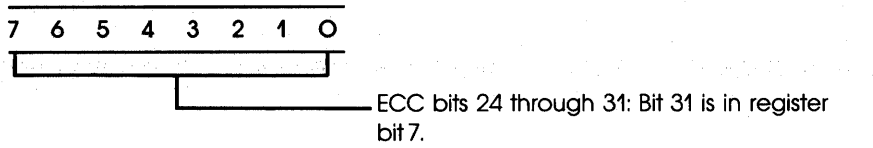
71 ECC CONTROL (WRITE ONLY)



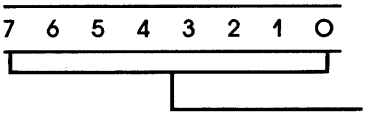
72 ECC (O-23) (READ ONLY)



73 ECC (24-31) (READ ONLY)

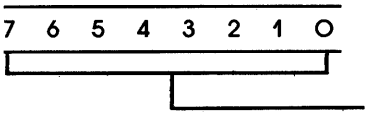


74 ECC POLYNOMIAL (Bits O-7)



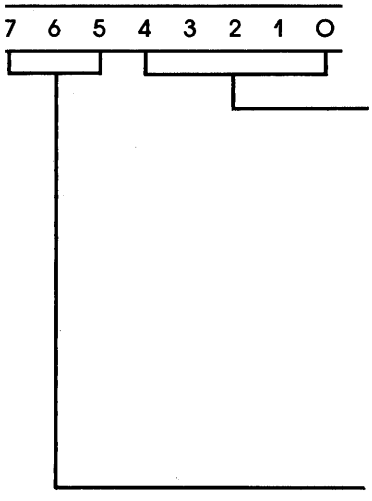
4O = Forward Polynomial
OO = Reciprocal Polynomial

77 ECC POLYNOMIAL (Bits 24-31)



OO = Forward Polynomial
O1 = Reciprocal Polynomial

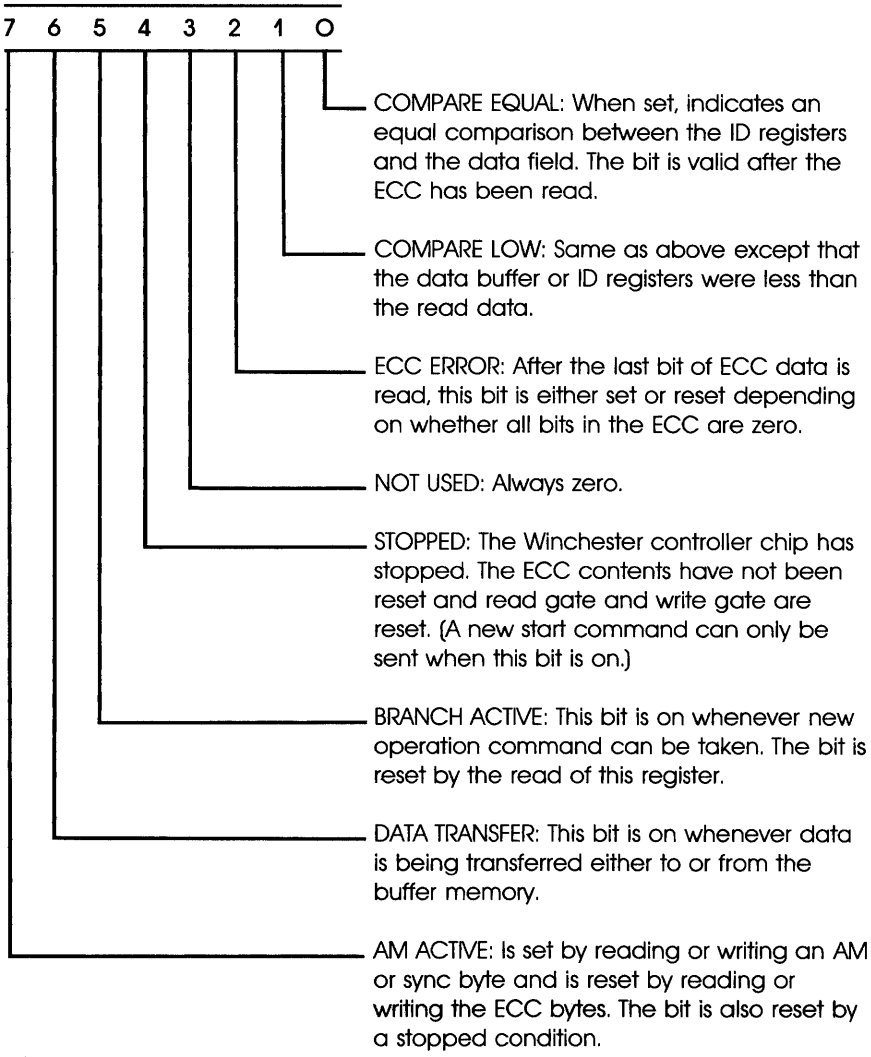
78 OPERATION COMMAND (WRITE ONLY)



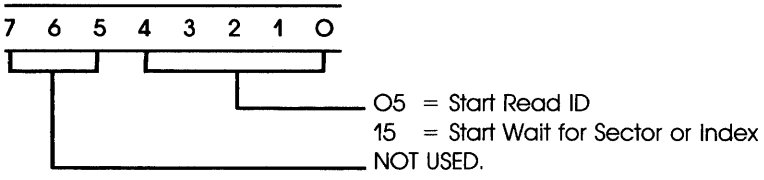
O5 = Read and Compare ID.
O8 = Read Data.
O9 = Write Data.
1O = Write Gap 1 (4E) and 1st ID Field.
11 = Format Write Data Field.
12 = Format Write ID Field after Data Field.
13 = At End of Format Data Field Write 4E until Index.
14 = End Read Data or End Write Data.
15 = At End of Format Data Field Write OO until Index or Sector Mark. Start Wait for Index or Sector Mark if Write Gate is Off.
18 = Stop at Next Branch.
NOT USED.

See OP Command sequence for proper timing as to when these registers are loaded.

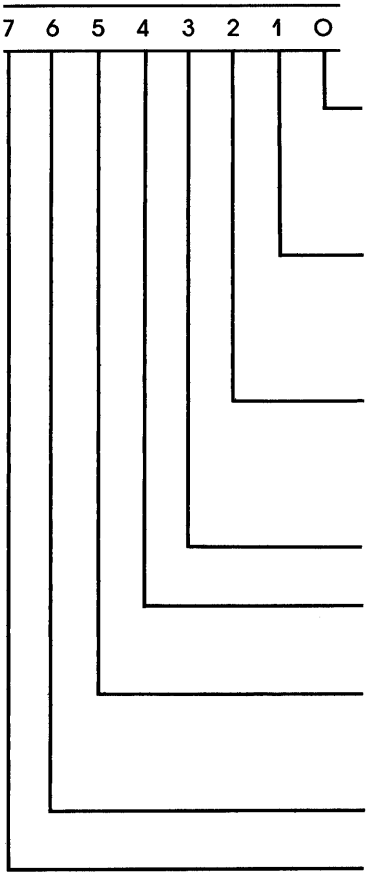
79 CONTROLLER CHIP STATUS (READ/WRITE) READ



REG 79 WRITE

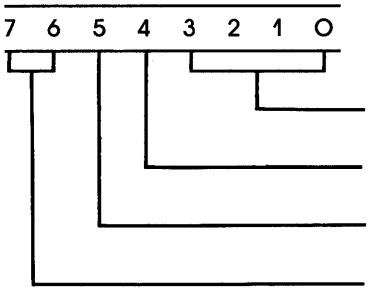


7A OPERATION CONTROL (READ/WRITE)



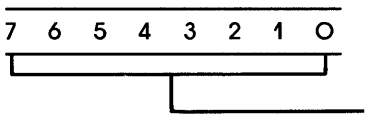
- INDEX PAST: Index point from the device has been detected since the last time this register was accessed. (READ ONLY) This bit is reset when read.
- SECTOR PAST: Sector pulse has been received from the device since the last access of this register. (READ ONLY) This bit is reset when read.
- NRZ DATA IN: An input of "1" on the NRZ data pin while read gate was on has occurred since the last time this register was accessed. (READ ONLY) This bit is reset when read.
- NOT USED.
- SEARCH OPERATION: This bit must be set whenever a data field compare is required.
- SUPPRESS TRANSFER: CLKB will not be generated when this bit is on. Also during WG the data field will be written with 6C.
- NOT USED.
- INHIBIT DATA FIELD CARRY: When set the carry/load of the counter for the data field will be inhibited causing an additional 256 bytes of data to be read or written. After a carry has occurred this bit will be reset.

7E I/O BITS (READ ONLY)



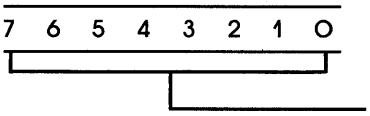
- NOT USED.
- INPUT: When set the input pin is high.
- DATA XFER: Same as R79, bit 6.
- NOT USED.

7F STACK (READ)



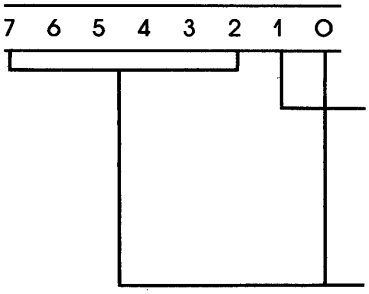
- Every time an ID field is read from the disk it is pushed on to the stack. A read of the LIFO stack will pop the flag, sector, head and cylinder bytes of the last ID field read, whether it is matched or not.

7F CLOCK CONTROL (WRITE)



OO = CLKA is RD/REF CLK/2 during data transfer, SYSCLK at other times.
FF = CLKA is RD/REF CLK/4 during data transfer, SYSCLK at other times.

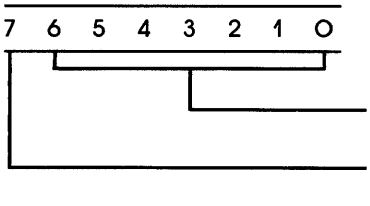
A4 SEARCH ENABLE (WRITE ONLY)



SEARCH ENABLE: This will, along with the search bit in register 7A, cause a byte for byte comparison of the addressed sector data with the data bus (0-7) input from the external sector buffer.

NOT USED.

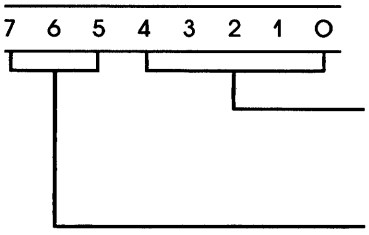
C4 DATA LENGTH (WRITE ONLY)



NOT USED.

1 = 256-byte or greater sectors.
0 = 128-byte sectors.

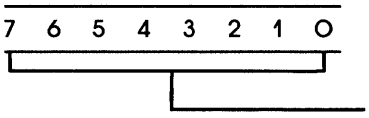
D0 GAP 1 & 3 LENGTH (WRITE ONLY)



GAP LENGTH: The 5 bit length value determines the Gap 1 and Gap 3 length during a format operations.

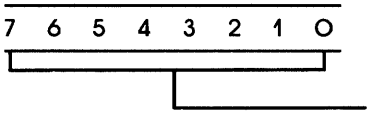
NOT USED.

E0 CYLINDER BYTE (READ/WRITE)

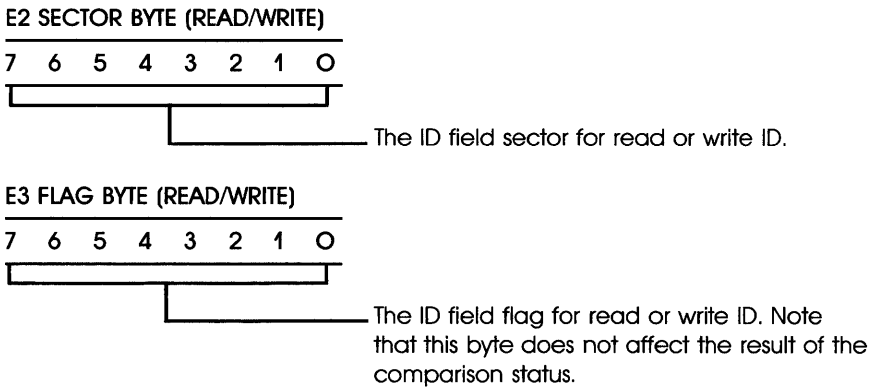


The ID field cylinder for read or write ID.

E1 HEAD BYTE (READ/WRITE)



The ID field head for read or write ID.



External Registers

The Winchester controller chip has five registers decoded that do not exist within the device. Their purpose is to provide versatile control unit design capability.

Registers 5O, 51, and 7O, when decoded, provide for a bidirectional connection of the microprocessor data bus with the buffer data bus through the Winchester controller chip on read or write. By designing Register 5O or 51 as a HOST INTERFACE REGISTER and Register 7O as the SECTOR BUFFER ACCESS REGISTER, some external components are not necessary.

Register 6E and 6F are decoded and a read or write to one of these addresses will generate a negative pulse on one of four pins. These signals are then used to enable a 74LS244 onto the microprocessor bus or to latch the bus into a 74LS373. In this manner the drive interface to several types of drives can be accommodated.

An example of the usage of Registers 6E and 6F decode is shown below in Figure 4.

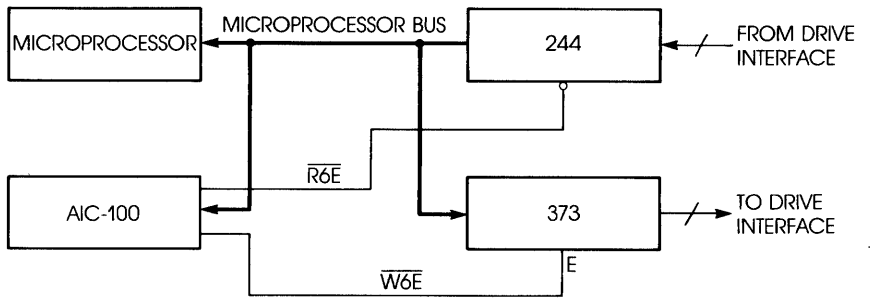


FIGURE 4. AIC-100 REGISTERS 6E AND 6F USAGE

OP COMMAND SEQUENCES

Fundamentally, any operation of the AIC-100 revolves around the following sequence of events:

- ☐ Initialize the chip (once after every power on reset).
- ☐ Place stored values in the appropriate registers.
- ☐ Place command parameters in the appropriate registers.
- ☐ Place actual command in Register 78.
- ☐ Read status/execute the command using Register 79.
- ☐ Repeat until command execution is complete.

At this point, there are five fundamental operations that should be looked at. These are as follows:

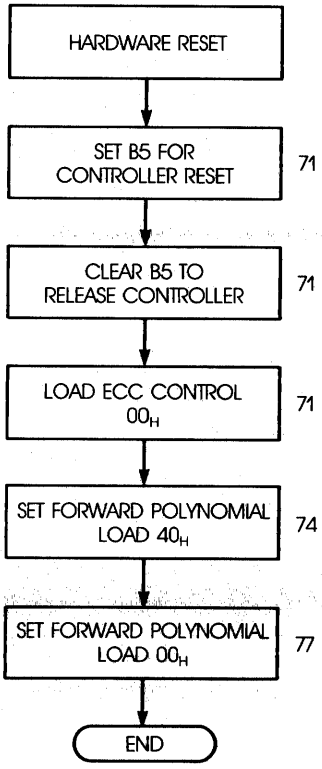
- ☐ Power on initialization
- ☐ Soft sector format
- ☐ Soft sector read/write
- ☐ Hard sector format
- ☐ Hard sector read/write

The flow charts show the recommended steps to be followed in order to execute the above operations.

Controller Chip Power On Initialization

Following a hardware reset of the controller chip, before attempting to use it to execute commands, a software initialization is necessary to properly set up the chip. The command sequence is as follows:

1. Set bit 5 in Register 71.
2. Reset bit 5 in Register 71.
3. Set contents of Register 71 to 00_H.
4. Set contents of Register 74 to 40_H. This sets a forward ECC polynomial.
5. Set contents of Register 77 to 00_H. This sets a forward polynomial.
6. Exit this routine.

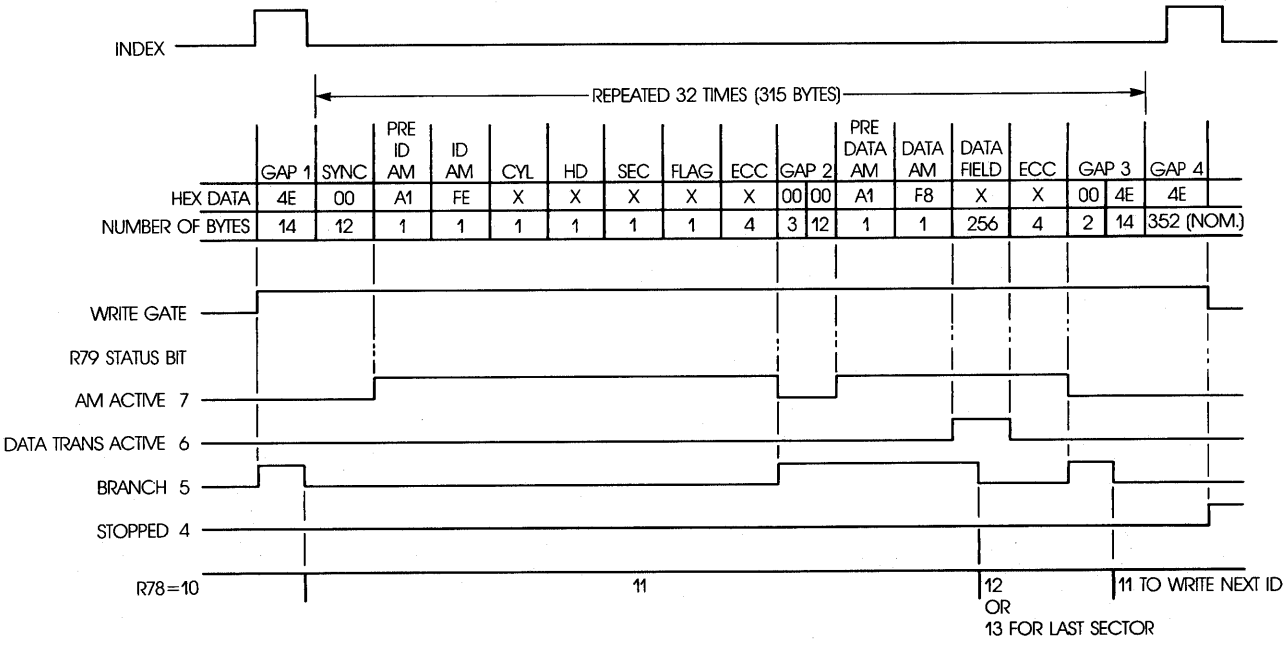


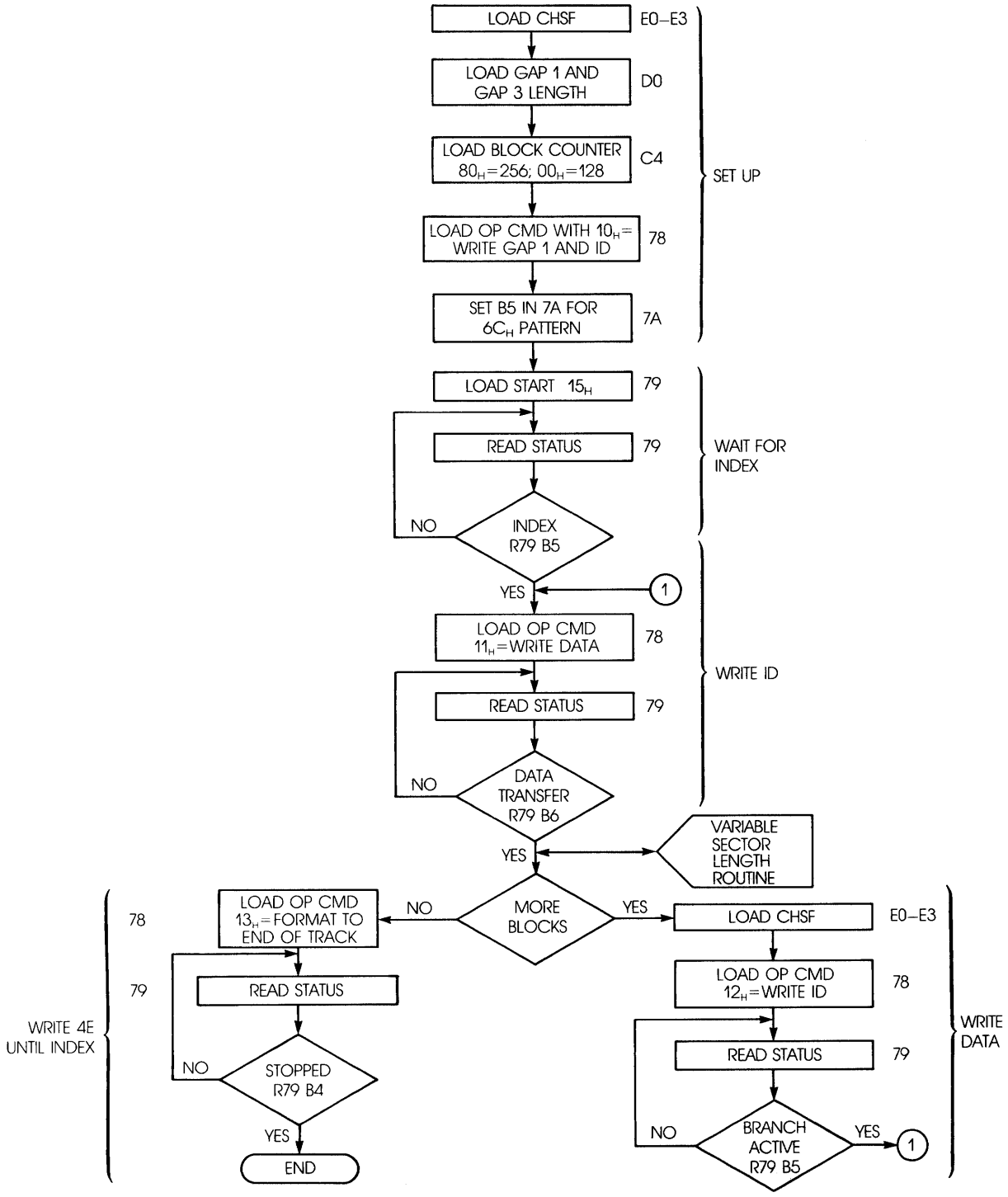
Soft Sector Format

A standard Winchester soft sector format employs 256 byte sectors and MFM encoding. This format yields 32 sectors per track. Any sector size which is a multiple of 128 may be employed (discussed later).

The format track command sequence is as follows:

1. Set Registers EO, E1, E2, and E3 with the first sector ID (cylinder, head, sector and flag respectively).
2. Set Register DO with Gap 1 and Gap 3 length.
3. Set Register C4 with either $8O_H$ (256 byte count) or OO_H (128 byte count).
4. Set Register 78 (command register) with $1O_H$. This will format Gap 1 after index.
5. Set bit 5 in Register 7A for a $6C_H$ data pattern. Otherwise contents of the sector buffer will be used during write to the data field.
6. Set Register 79 with 15_H. This will start the format operation. The Winchester controller chip waits for index, after which Gap 1 will be written.
7. Read status from Register 79. If BRANCH ACTIVE (bit 5 is set) it means that index is past and Gap 1 is being written. After this the first ID will be written.
8. Set Register 78 with 11_H. This will cause the data to be written next.
9. Read status from Register 79. If bit 6 is set, the data field is now being written.
10. If there are no more sectors to be written, load Register 78 with 13_H, check Register 79 and wait for the controller to stop (bit 4 is set).
11. Otherwise set Register 78 with 12_H and update Register EO through E3 with the next ID field to be written.
12. Wait for BRANCH ACTIVE by monitoring Register 79, bit 5. Gap 3 is being written.
13. Repeat steps 8, 9, 10, 11 and 12 for 31 times or the number of sectors to be formatted.



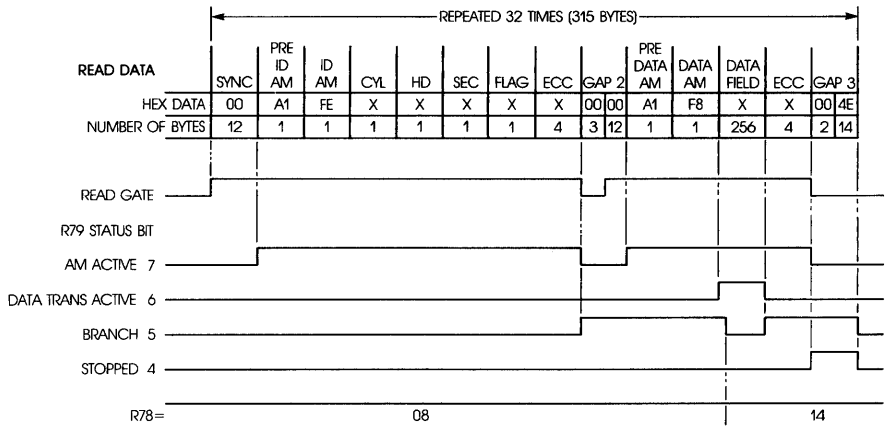

LOAD CHSF
E0–E3
LOAD GAP 1 AND GAP 3 LENGTH
D0
LOAD BLOCK COUNTER 80_H=256; 00_H=128
C4
SET UP
LOAD OP CMD WITH 10_H= WRITE GAP 1 AND ID
78
SET B5 IN 7A FOR $6C_H$ PATTERN
7A
LOAD START 15_H
79
READ STATUS
79
WAIT FOR INDEX
NO
INDEX R79 B5
YES
1
LOAD OP CMD 11_H=WRITE DATA
78
WRITE ID
READ STATUS
79
NO
DATA TRANSFER R79 B6
YES
VARIABLE SECTOR LENGTH ROUTINE
MORE BLOCKS
NO
YES
78
LOAD OP CMD 13_H=FORMAT TO END OF TRACK
79
READ STATUS
WRITE 4E UNTIL INDEX
NO
STOPPED R79 B4
YES
END
LOAD CHSF
E0–E3
LOAD OP CMD 12_H=WRITE ID
78
READ STATUS
79
WRITE DATA
NO
BRANCH ACTIVE R79 B5
YES
1

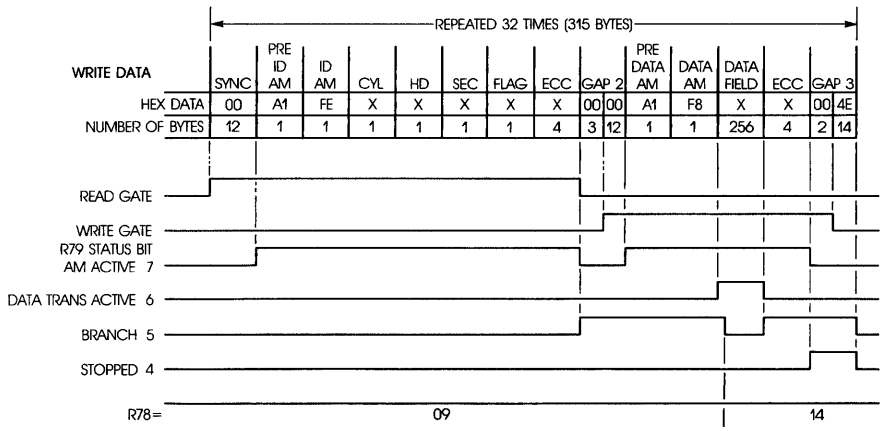
Soft Sector Read/Write

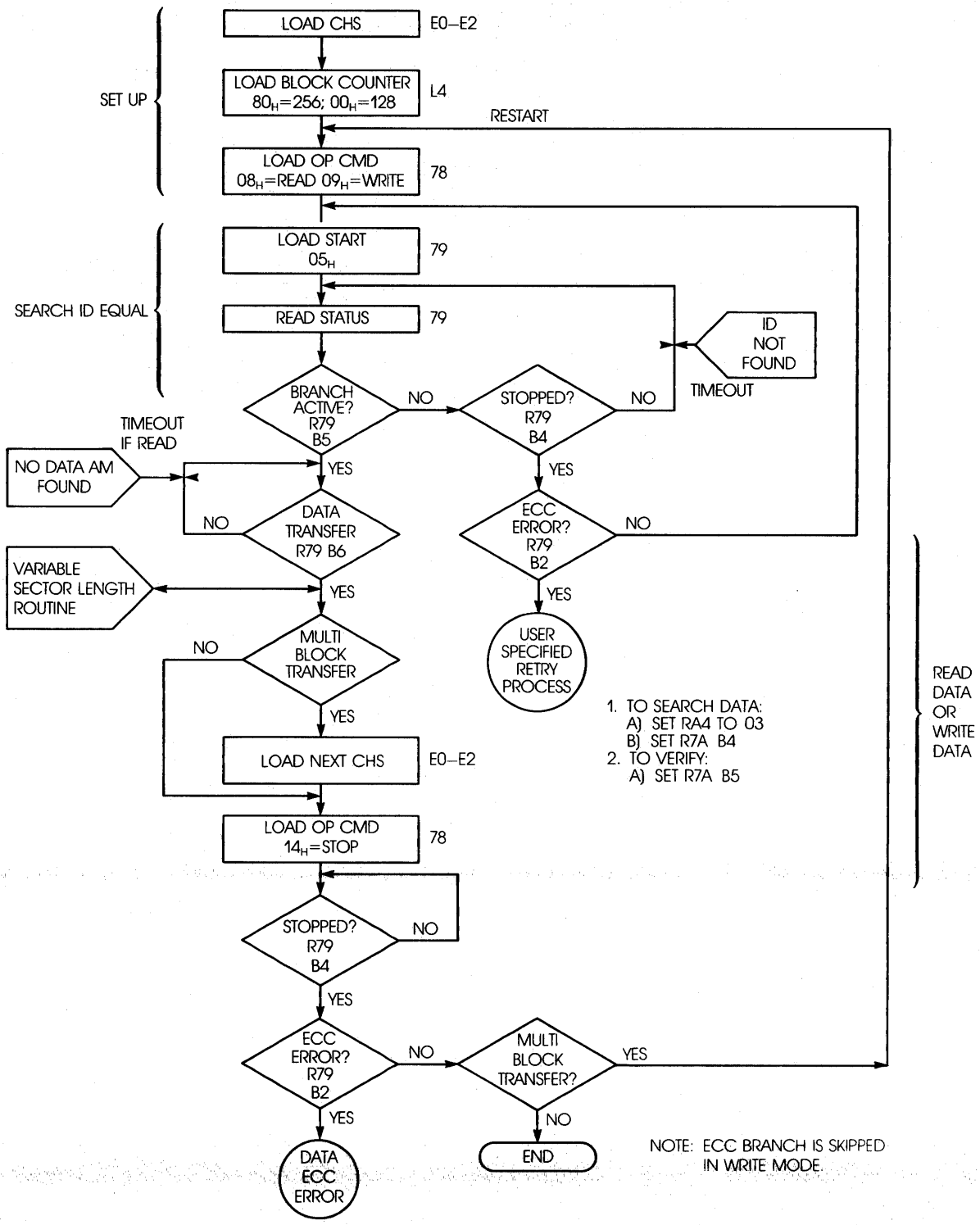
In order to read or write data, the heads have to first be positioned over the appropriate cylinder, and the relevant head must be selected. The following steps assume that the correct track has been reached.

The operation is performed as follows:

1. Set REO, E1 and E2 with the desired sector ID.
2. Set C4 with either OO (128 byte counter) or 8O (256 byte counter).
3. Set OP command (R78) with O8, the read data command, or with O9, the write command.
4. Set Start Reg (R79) with O5. This will turn on Read Gate and enable the VFO to look for an address mark.
5. Wait for BRANCH ACTIVE (R79, bit 5). If the correct ID field was read, the Winchester controller chip will continue on to read the data field. If an ID ECC error or incorrect sector was encountered, the stopped bit in R79 will be set. If so, go back to Step 4.
6. Wait for DATA TRANSFER (R79 bit 6). Read data is now being transferred to the sector buffer, or write data from the buffer.
7. If this is a multiblock transfer, update EO-E2 with next sector ID while data is being transferred.
8. Set OP command (R78) with 14. This will stop the Winchester controller chip at the end of the data field ECC.
9. Wait for STOPPED (R79 bit 4).
10. If it is a read command, test ECC ERROR (R79, bit 2). If it is set, go to the error correction routine. If not, continue on to read the next sector (Step 3) or end.






SET UP
LOAD CHS
E0–E2
LOAD BLOCK COUNTER
80H=256; 00H=128
L4
RESTART
LOAD OP CMD
08H=READ 09H=WRITE
78
SEARCH ID EQUAL
LOAD START
05H
79
READ STATUS
79
ID
NOT
FOUND
TIMEOUT
BRANCH
ACTIVE?
R79
B5
NO
STOPPED?
R79
B4
NO
TIMEOUT
IF READ
NO DATA AM
FOUND
YES
YES
NO
DATA
TRANSFER
R79 B6
ECC
ERROR?
R79
B2
NO
VARIABLE
SECTOR LENGTH
ROUTINE
YES
YES
NO
MULTI
BLOCK
TRANSFER
USER
SPECIFIED
RETRY
PROCESS
YES
1. TO SEARCH DATA:
A) SET RA4 TO 03
B) SET R7A B4
2. TO VERIFY:
A) SET R7A B5
LOAD NEXT CHS
E0–E2
LOAD OP CMD
14H=STOP
78
STOPPED?
R79
B4
NO
YES
ECC
ERROR?
R79
B2
NO
MULTI
BLOCK
TRANSFER?
YES
YES
NO
DATA
ECC
ERROR
END
NOTE: ECC BRANCH IS SKIPPED
IN WRITE MODE.
READ
DATA
OR
WRITE
DATA

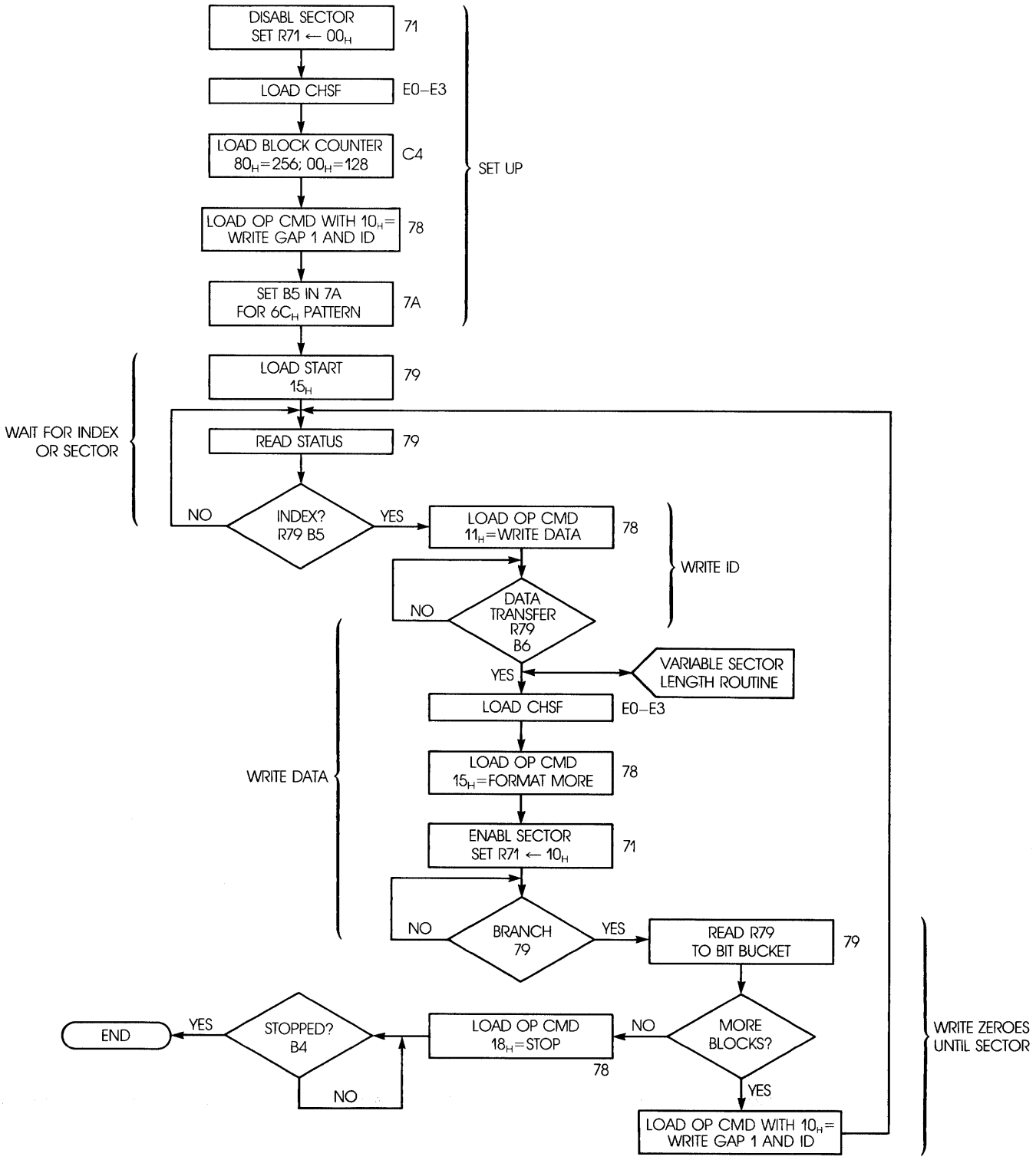
Hard Sector Format

As mentioned earlier, the AIC-100 controller chip is capable of supporting hard sectored drives. Hard sector drives differ from soft sector drives in that, between every adjacent sector on a track, there is a sector mark, and this is used to identify the beginning of a sector.

A hard sectored format operation is performed as follows:

1. Disable sector mark by setting Register 71 to 00_H. Thus the controller chip will wait for the index mark before writing out Gap 1.
2. Load Registers E0-E3 with the sector ID (cylinder, head, sector and flag).
3. Load Register C4 with the data length (80_H =256, 00_H =128).
4. Load Register 78 with 10_H. This will cause Gap 1 to be written after index.
5. Set bit 5 in Register 7A for $6C_H$ data pattern. Otherwise sector buffer is used.
6. Load Register 79 with 15_H to start formatting.
7. Read status from Register 79. If bit 5 is set, then Gap 1 is being written. After this the ID is written.
8. Load Register 78 with 11_H. This tells the controller to write the data next.
9. Read status from Register 79. If bit 6 is set, then data is being transferred.
10. Update Registers E0-E3 with the next sector ID. This has to be done before even checking if there are more blocks, since, on a hard sector drive, the timing is more critical.
11. Load Register 78 with 15_H. This tells the controller to write zeros until the next sector mark is encountered.
12. Enable sector branch by setting Register 71 to 10_H.
13. Read status from Register 79 and branch when active (bit 5 is set). This means that a sector mark was encountered.
14. Read status from Register 79 and discard contents. This guarantees a reset.
15. Check to see if any more blocks have to be written. If there is no more to be done, then load Register 78 with 18_H. This tells the controller to stop. Monitor Register 79 bit 4 (stop bit) before leaving the routine.
16. If more blocks have to be written, then load Register 78 with 10_H and repeat steps 7 through 15.

NOTE: It is suggested that Gap 1 length be kept to zero. Thus, during format, after the sector mark is encountered, the controller will write out the Sync for ID field. Inter record separation is provided by the controller writing 00 from end of data field to next sector mark.

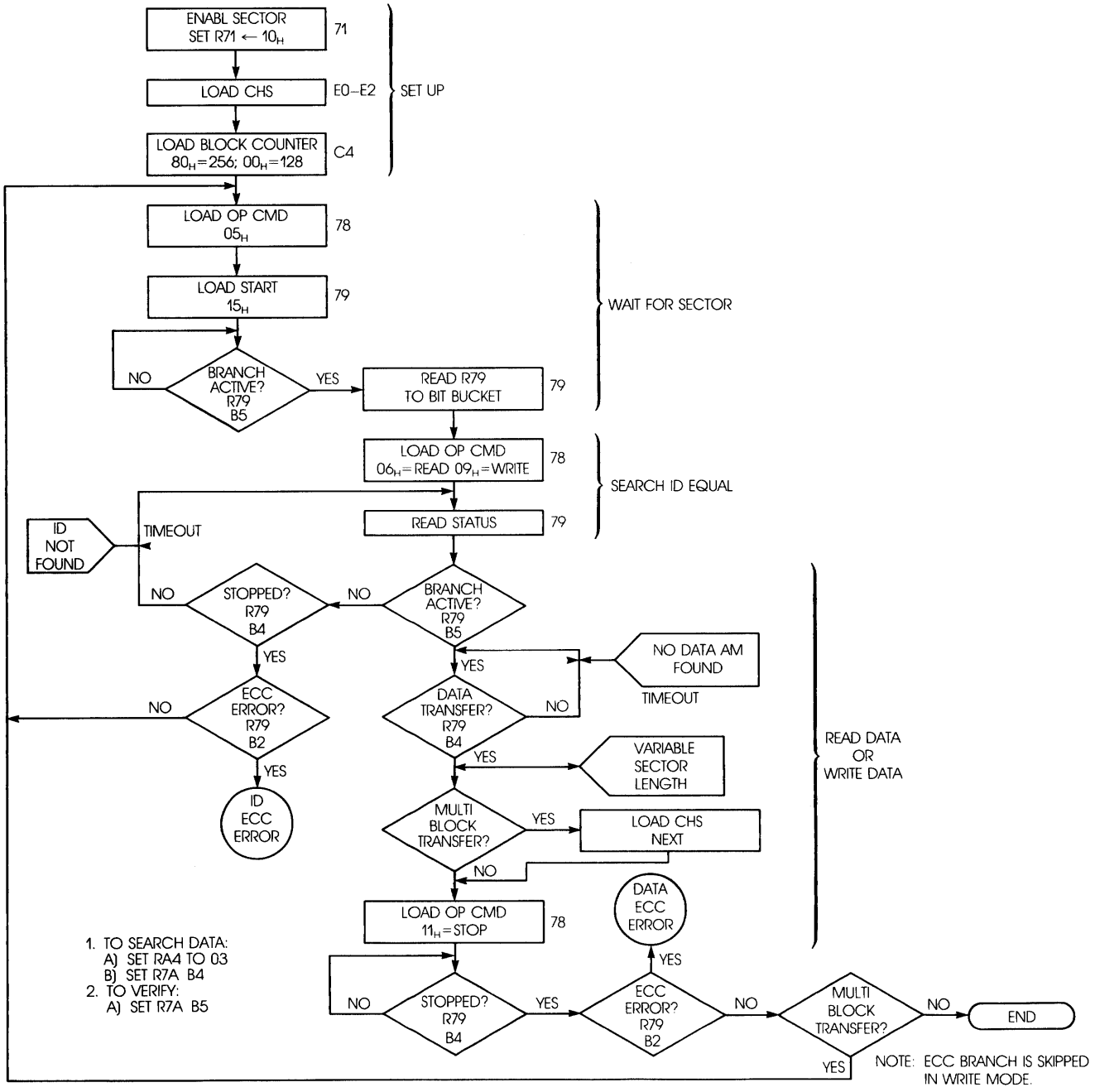

DISABL SECTOR
SET R71 ← 00H
71
LOAD CHSF
E0–E3
LOAD BLOCK COUNTER
80H=256; 00H=128
C4
LOAD OP CMD WITH 10H=
WRITE GAP 1 AND ID
78
SET B5 IN 7A
FOR 6CH PATTERN
7A
SET UP
LOAD START
15H
79
WAIT FOR INDEX
OR SECTOR
READ STATUS
79
NO
INDEX?
R79 B5
YES
LOAD OP CMD
11H=WRITE DATA
78
WRITE ID
NO
DATA
TRANSFER
R79
B6
YES
VARIABLE SECTOR
LENGTH ROUTINE
LOAD CHSF
E0–E3
WRITE DATA
LOAD OP CMD
15H=FORMAT MORE
78
ENABL SECTOR
SET R71 ← 10H
71
NO
BRANCH
79
YES
READ R79
TO BIT BUCKET
79
END
YES
STOPPED?
B4
NO
LOAD OP CMD
18H=STOP
78
NO
MORE
BLOCKS?
YES
LOAD OP CMD WITH 10H=
WRITE GAP 1 AND ID
WRITE ZEROES
UNTIL SECTOR

Hard Sector Read/Write

As mentioned earlier, a hard sector drive has a sector mark between adjacent sectors. Thus the controller starts reading the ID field after the next sector mark is encountered.

The read and write operations differ in that after a write operation, no ECC test is necessary. The read or write data operation is performed as follows:

1. Enable branch on sector mark by setting Register 71 to $1O_H$.
2. Set Registers EO, E1 and E2 with the desired sector ID.
3. Set C4 with either OO (128 byte counter) or 8O (256 byte counter).
4. Load Register 78 with $O5_H$, the read ID command. The VFO will look for a SYNC of A1 after read gate is turned on.
5. Load Register 79 with 15_H. The controller will wait for index or the next sector mark (since R71 was set to $1O_H$) and read the ID field.
6. Wait for BRANCH ACTIVE (R79, bit 5). This means that the next sector mark or index has been encountered. The read gate will not be turned on.
7. Read and discard Register 79 to ensure reset.
8. Load Register 78 with O8, the read command or a O9 for a write command.
9. Wait for BRANCH ACTIVE (R79 bit 5). If the correct ID field was read, the Winchester controller chip will continue on to read the data field. If an ID ECC error or incorrect sector was encountered, the stopped bit in Register 79 will be set. If so, go back to Step 4.
10. Wait for DATA TRANSFER (R79, bit 6). Read data is now being transferred to the sector buffer, or from the buffer in the case of a write.
11. If this is a multi-block transfer, update EO-E2 with next sector ID while data is being transferred.
12. Set Register 78 with 14_H (STOP command). This will stop the controller chip at the end of the data field ECC.
13. Wait for STOPPED (R79, bit 4).
14. Test ECC ERROR (R79, bit 2). If it is set, go to the error correction routine. If not, continue on to the next sector (Step 4) or end.


ENABL SECTOR
SET R71 ← 10H
71
LOAD CHS
E0–E2
LOAD BLOCK COUNTER
80H=256; 00H=128
C4
SET UP
LOAD OP CMD
05H
78
LOAD START
15H
79
WAIT FOR SECTOR
NO
BRANCH ACTIVE? R79 B5
YES
READ R79 TO BIT BUCKET
79
LOAD OP CMD
06H=READ 09H=WRITE
78
SEARCH ID EQUAL
READ STATUS
79
ID NOT FOUND
TIMEOUT
NO
STOPPED? R79 B4
NO
BRANCH ACTIVE? R79 B5
YES
NO DATA AM FOUND
TIMEOUT
YES
NO
ECC ERROR? R79 B2
DATA TRANSFER? R79 B4
NO
YES
VARIABLE SECTOR LENGTH
YES
ID ECC ERROR
MULTI BLOCK TRANSFER?
YES
LOAD CHS NEXT
NO
READ DATA OR WRITE DATA
LOAD OP CMD
11H=STOP
78
DATA ECC ERROR
YES
1. TO SEARCH DATA:
A) SET RA4 TO 03
B) SET R7A B4
2. TO VERIFY:
A) SET R7A B5
NO
STOPPED? R79 B4
YES
ECC ERROR? R79 B2
NO
MULTI BLOCK TRANSFER?
NO
END
YES
NOTE: ECC BRANCH IS SKIPPED IN WRITE MODE.

Multi-Sector Read or Write

Multi-sector reads or writes are accomplished by loading the next sector address to be found while DATA TRANSFER is active (Reg 79, Bit 6) for the present sector and restarting the read or write at Step 3 immediately after the stopped bit is set.

Verify Sector

A Verify Sector is accomplished by setting the SUPPRESS TRANSFER in the OP Modifier Register (Reg 7A, bit 5) and then performing the read data command sequence. This will verify that the ECC is good for the data field without generating a CLKB.

Search Sector Data

A search of the data field is performed by setting OP Modifier Register, (7A, bit 4) and the Search Enable Register (Reg A4, bit 2) then entering the read data sequence. The contents of the sector buffer will be compared, byte for byte, with the data read from the disk. The result of this comparison is latched into the Status Register (79, bits O and 1). Be sure to reset both Reg 7A, bit 4, and Reg A4, bit 2, after completion of search.

Variable Sector Size

The Winchester controller chip has an 8-bit data field length counter. The most significant bit of this counter is programmable by setting or resetting Data Length Register (C4, bit 7). O in this bit will cause 128 bytes and a 1 will cause 256 bytes to be read or written.

For multiples of 128- or 256-byte record lengths, bit 7 of the OP Modifier (7A) Register must be employed.

By setting this bit during DATA TRANSFER before the first 128/256 byte count has expired, the Winchester controller chip will be inhibited from going on to ECC and another 256 bytes of data will be transferred. OP Modifier bit 7 (7A, bit 7) will be automatically reset whenever the counter overflows. By testing this bit, a count of 256 byte segments may be accomplished.

PROGRAMMING 8-BIT ECC CORRECTION

After each read data operation a read error may have occurred. This may be determined by reading Register 79. If bit 2 is set, an error did occur and the following procedure is employed to determine if the error is correctable. Note that the majority of read errors are soft (i.e., caused by noise) and that the correction algorithm is time consuming. It is recommended that the record be re-read before attempting correction.

The general flow of the algorithm for 8 bit correction is as follows:

1. Off-load the 32-bit syndrome into local RAM.
2. Shift the syndrome back into the ECC register in reverse order, swapping the syndrome end for end.
3. Change the ECC polynomial from forward to reciprocal.
4. Shift the ECC until all bits except the high order (24-31) bits are zero (correctable) or the number of shifts are greater than the number of bits in the record (uncorrectable).
5. If correctable, the number of shifts represent the displacement of the error from the end of the record (the last bit of the ECC). The error pattern is located in bits 24-31 of the ECC register. This pattern is exclusive ORed with the appropriate bits in memory to correct the error.

Detailed Programming Steps

1. After a read error is detected, disable feedback by setting R71=04_H.
2. Store contents of R73 in RAM (x).
3. Shift ECC 8 times by setting R71=06_H eight times.
4. Store contents of R73 in RAM (x+1).
5. Shift ECC 8 times by setting R71=06_H eight times.
6. Store contents of R73 in RAM (x+2).
7. Shift ECC 8 times by setting R71=06_H eight times.
8. Store contents of R73 in RAM (x+3).
9. Clear ECC and disable feedback by setting R71 to 08 and then 04.
10. Right rotate location RAM (x+3) and test if carry is set: (i.e., test bit 0) if set, then load R71=07_H if not set, then load R71=06_H repeat operation 7 more times to load entire byte.
11. Repeat step 10 for RAM locations x+2, x+1, and x until all 32 bits of the syndrome are loaded into the ECC in reverse order.
12. Load R74=00_H and R77=01_H to enable the reciprocal polynomial and disable the forward polynomial.
13. Compute record length in bits: # of bits per data field=ECC+Data+AM and SYNC for a 256 byte record length in bits =4*8+256*8+2*8=2096.
14. Enable feedback by setting R71=00_H.
15. Shift ECC once by setting R71=02_H and increment a software counter.
16. Test to see if the software counter is greater than the record length; if yes, the error is uncorrectable, re-enable the forward polynomial and end operation.
17. Test to see if R72=00_H; if yes, go to Step 18 if no, go to Step 15.
18. Subtract hardware offset of 7 from the shift count. If a correctable error is located within the ECC or the SYNC & AM bytes (the shift count <=32), the data field is good and no further action is required. Subtract 32 from the shift count.
19. The bit displacement (shift count) must now be converted to a byte offset by right shifting the count 3 times. The value of the shift count equals the bit displacement from end of the record.
20. R73 is the mirror image of the error pattern. Form the error mask data (2 bytes) by concatenating R73 with a zero byte.
21. Get the shift count (E) for error mask data by extracting the lower 3 bits from the shift count obtained in Step 18.
22. Right shift the error mask data with MSB (bit 15) set to zero. Repeat E-1 times more.
23. Mirror the error mask data byte by byte.
24. The 2 byte error mask data may now be EXORed with the data in memory to correct the error. The byte offset obtained in Step 19 is low order byte offset.

NOTES:

1) For 5-bit ECC correction, the following modification is necessary.
   Step 17: Test to see if R72=OO_H and R73 bits O, 1, 2 are zero; if yes, go to Step 18. if no, go to Step 15.
   Step 18: R73 bits 3-7 are the mirror image of the error pattern. (O-7 for 8 bit ECC)
2) In Step 23, say, if the original error mask data is 5C 9A, after mirroring the data is 3A 59.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to 150°C
Voltage on Any Pin with Respect to Ground ..... −0.5 to 7 volts
Power Dissipation ..... 1 watt
Power Supply Voltage ..... 4.75 to 5.25 volts

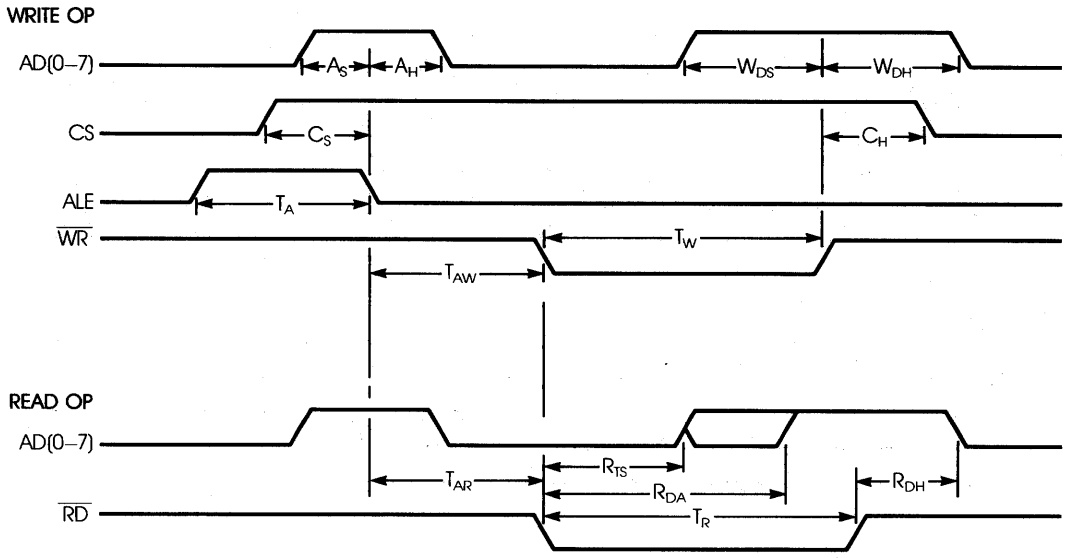
NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage (NRZ, RD/REF, WAM/AMD)	−0.5	0.5	V	
V_{IL}	Input Low Voltage (All Other)	−0.5	0.3	V	
V_{IH}	Input High Voltage	3.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA*
V_{OH}	Output High Voltage	2.2			I_{OH} = 400 µA
I_{CC}	Supply Current		200	mA	
I_{IL}	Input Leakage	−10	10	µA	$0 < V_{IN} < V_{CC}$
I_{OL}	Output Leakage Off State	−100	100	µA	$0.45 < V_{OUT} < V_{CC}$
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		30	pF	

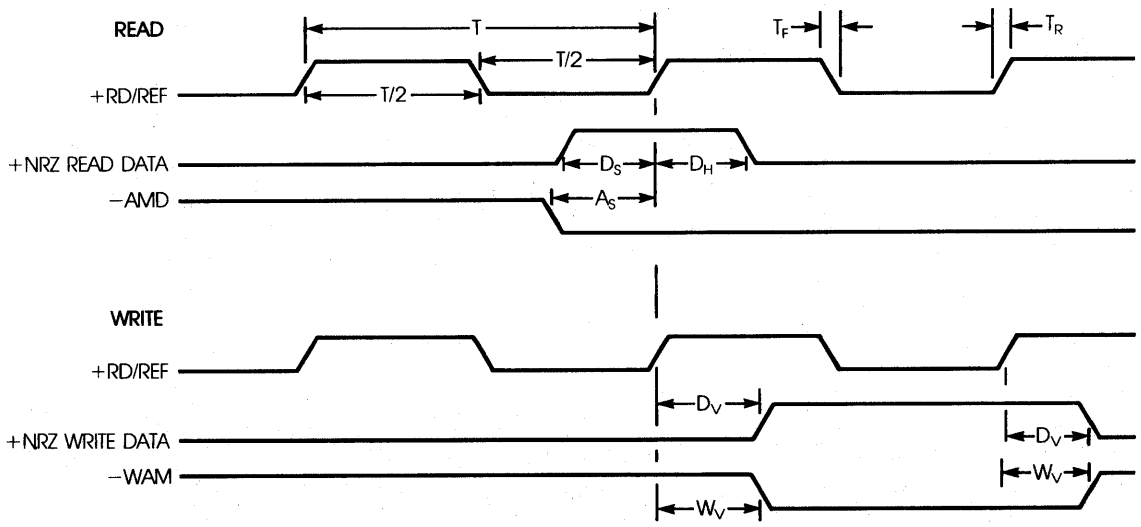
NOTE: For RG and WG, I_{OL} = 5 mA.

AIC-100 MICROPROCESSOR INTERFACE TIMING



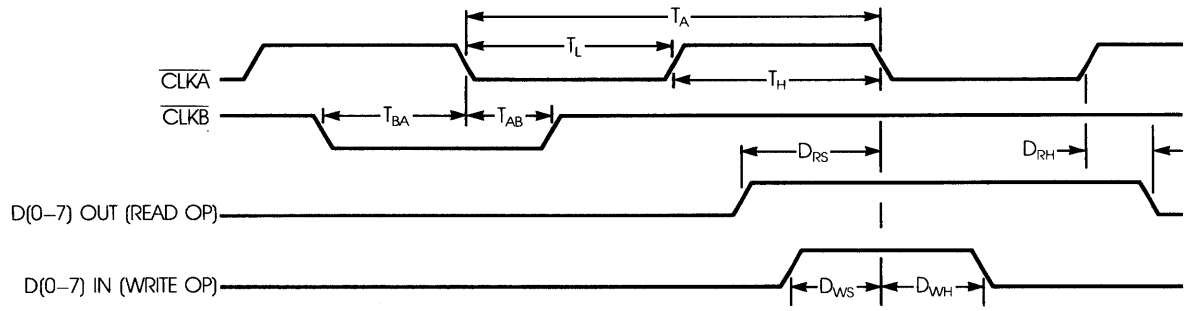
SYMBOL	PARAMETER	MIN	MAX	UNITS
T_A	ALE Width	45		ns
T_{AW}	ALE ↓ to $\overline{WR}$ ↓	60		ns
T_{AR}	ALE ↓ to $\overline{RD}$ ↓	60		ns
T_W	$\overline{WR}$ Width	200		ns
T_R	$\overline{RD}$ Width	230		ns
A_S	ADRS Valid to ALE ↓	25		ns
A_H	ALE ↓ to ADRS $\overline{Valid}$	20		ns
C_S	CS Valid to ALE ↓	25		ns
C_H	$\overline{RD}$ or $\overline{WR}$ ↑ to CS ↓	0		ns
W_{DS}	Write Data Valid to $\overline{WR}$ ↑	40		ns
W_{DH}	$\overline{WR}$ ↑ to Write Data $\overline{Valid}$	0		ns
R_{TS}	$\overline{RD}$ ↓ to AD (0-7) Active	40		ns
R_{DA1}	$\overline{RD}$ ↓ to Data Valid (Regs 71-7F)		150	
R_{DS2}	$\overline{RD}$ ↓ to Data Valid (All Other Regs)		230	ns
R_{DH}	$\overline{RD}$ ↑ to Data $\overline{Valid}$	80	130	ns

AIC-100 DISK READ/WRITE TIMING



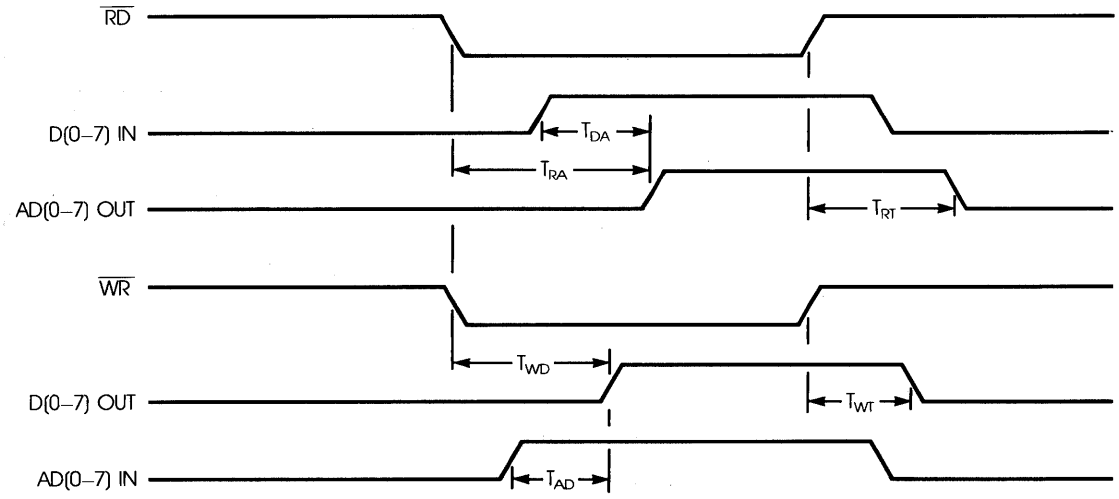
SYMBOL	PARAMETER	AIC-100 MIN	AIC-100 MAX	AIC-100-10 MIN	AIC-100-10 MAX	UNITS
T	RD/REF Period	180	5000	100	5000	ns
T/2	RD/REF Period ÷ 2	85		45		ns
T_R	RD/REF Rise Time		20		10	ns
T_F	RD/REF Fall Time		20		10	ns
D_S	Data In Valid to RD/REF ↑	50		20		ns
D_H	RD/REF ↑ to Data In $\overline{\text{Valid}}$	10		50		ns
A_S	AMD Valid to RD/REF ↑	50		20		ns
D_V	RD/REF ↑ to Data Out	15	100	10	60	ns
W_V	RD/REF ↑ to W_{AM} Out	15	100	10	60	ns

AIC-100 READ/WRITE DATA BUS TIMING



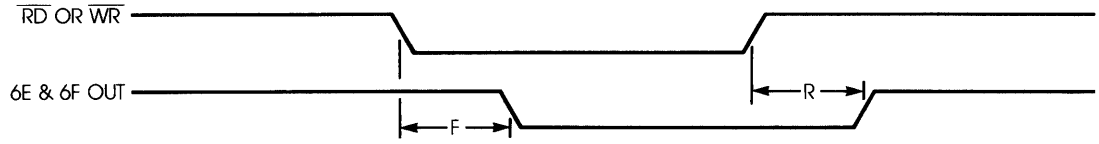
SYMBOL	PARAMETER	MIN	MAX	UNITS
T_A	$\overline{CLKA}$ Period	200		ns
$T_H=T_L$	$\overline{CLKA}$ Low or High Time	95		ns
T_{BA}	$\overline{CLKB}$ ↓ to CLKA ↓	90		ns
T_{AB}	$\overline{CLKA}$ ↓ to $\overline{CLKB}$ ↑	100		ns
D_{RS}	D(0-7) In Valid to $\overline{CLKA}$ ↓	60		ns
D_{RH}	$\overline{CLKA}$ ↑ to D(0-7) Out $\overline{Valid}$	20	80	ns
D_{WS}	D(0-7) In Valid to $\overline{CLKA}$ ↓	50		ns
D_{WH}	$\overline{CLKA}$ ↓ to D(0-7) In $\overline{Valid}$	20		ns

AIC-100 REG 50, 51 AND 70 TIMING



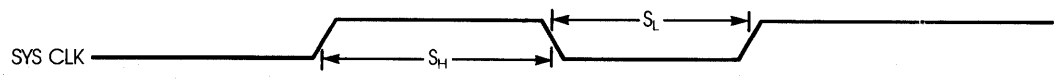
SYMBOL	PARAMETER	MIN	MAX	UNITS
T_{DA}	D(0-7) In Valid to AD(0-7) Out Valid		115	ns
T_{RA}	$\overline{RD}$ ↓ to AD(0-7) Out Valid		160	ns
T_{RT}	$\overline{RD}$ ↑ to AD(0-7) Out Tri State	35	100	ns
T_{WD}	$\overline{WR}$ ↓ to D(0-7) Out Valid		120	ns
T_{WT}	$\overline{WR}$ ↑ to D(0-7) Out Tri State	40	130	ns
T_{AD}	AD(0-7) In Valid to D(0-7) Out Valid		95	ns

AIC-100 REG 6E AND 6F TIMING



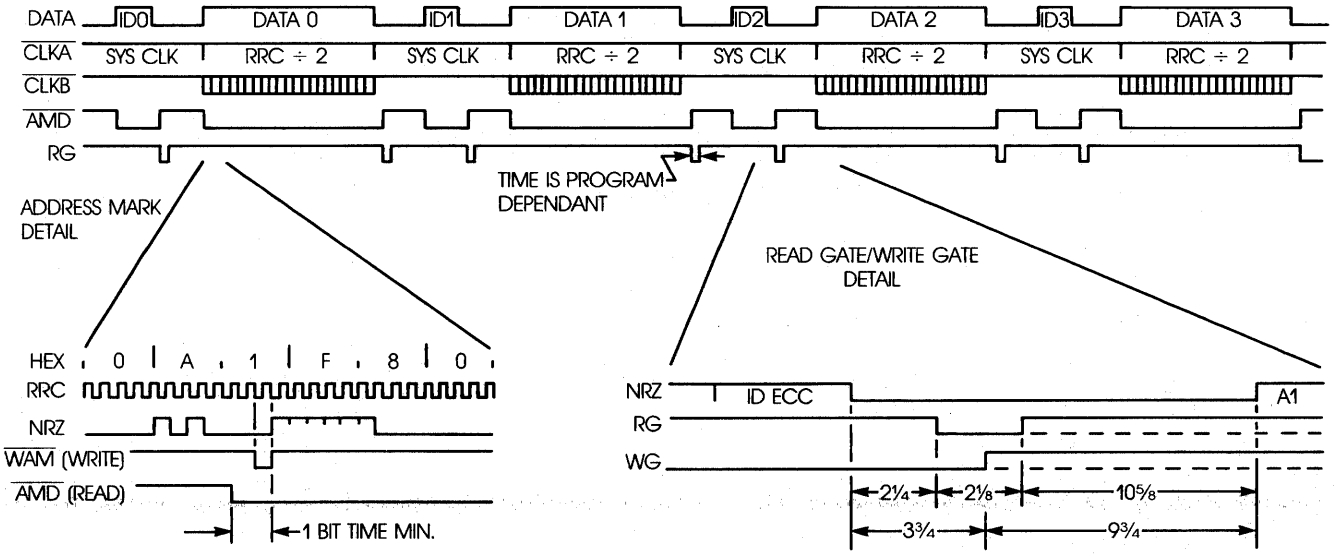
SYMBOL	PARAMETER	MIN	MAX	UNITS
F	$\overline{RD}$ or $\overline{WR}$ ↓ to 6E or 6F ↓		130	ns
R	$\overline{RD}$ or $\overline{WR}$ ↑ to 6E or 6F ↑	45	140	ns

AIC-100 SYSCLK TIMING



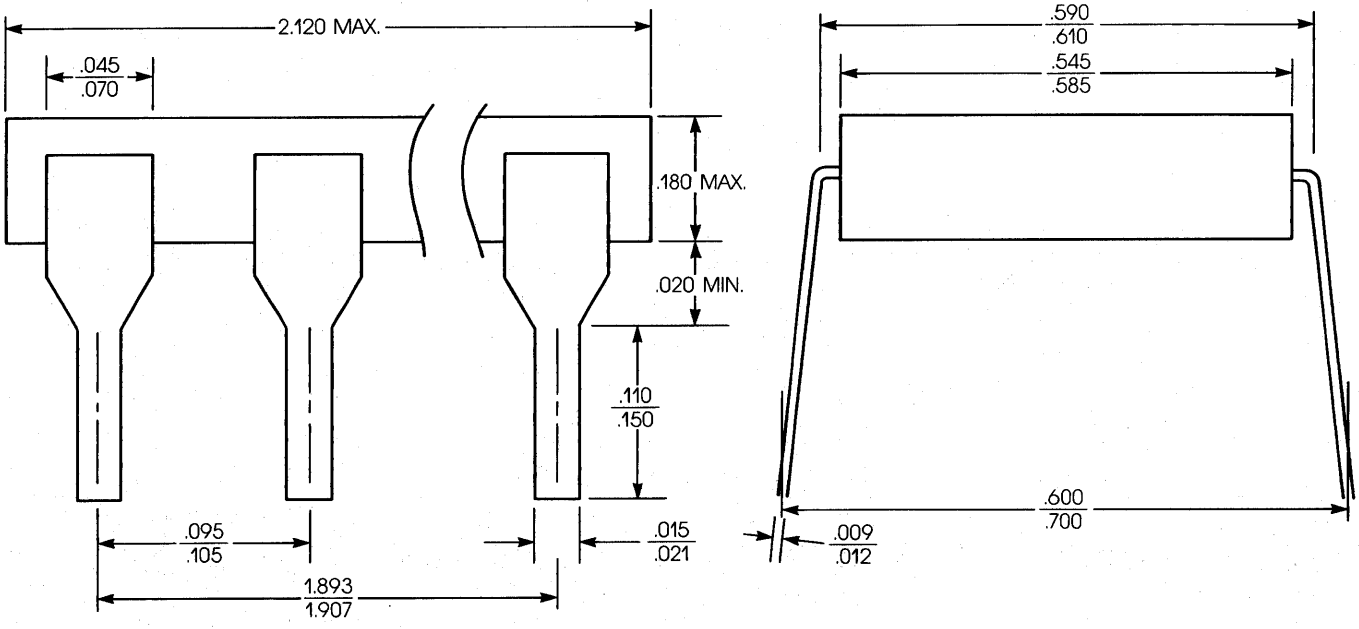
SYMBOL	PARAMETER	MIN	MAX	UNITS
S_H	SYSCLK High	60		ns
S_L	SYSCLK Low	60		ns

REFERENCE TIMING DIAGRAM



NOTE: NUMBERS ARE GIVEN IN BYTE TIMES. NOTICE THAT THE SUM OF RG TIMES IS 1.5 BYTES LONGER THAN THE SUM OF WG TIMES DUE TO 1 BYTE DATA DELAY IN THE AIC-100 AND ½ BYTE DELAY IN THE ENCODER.

PACKAGING INFORMATION



40-Lead Plastic Dual-in-line Package

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STOCK NO: 500001-00
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