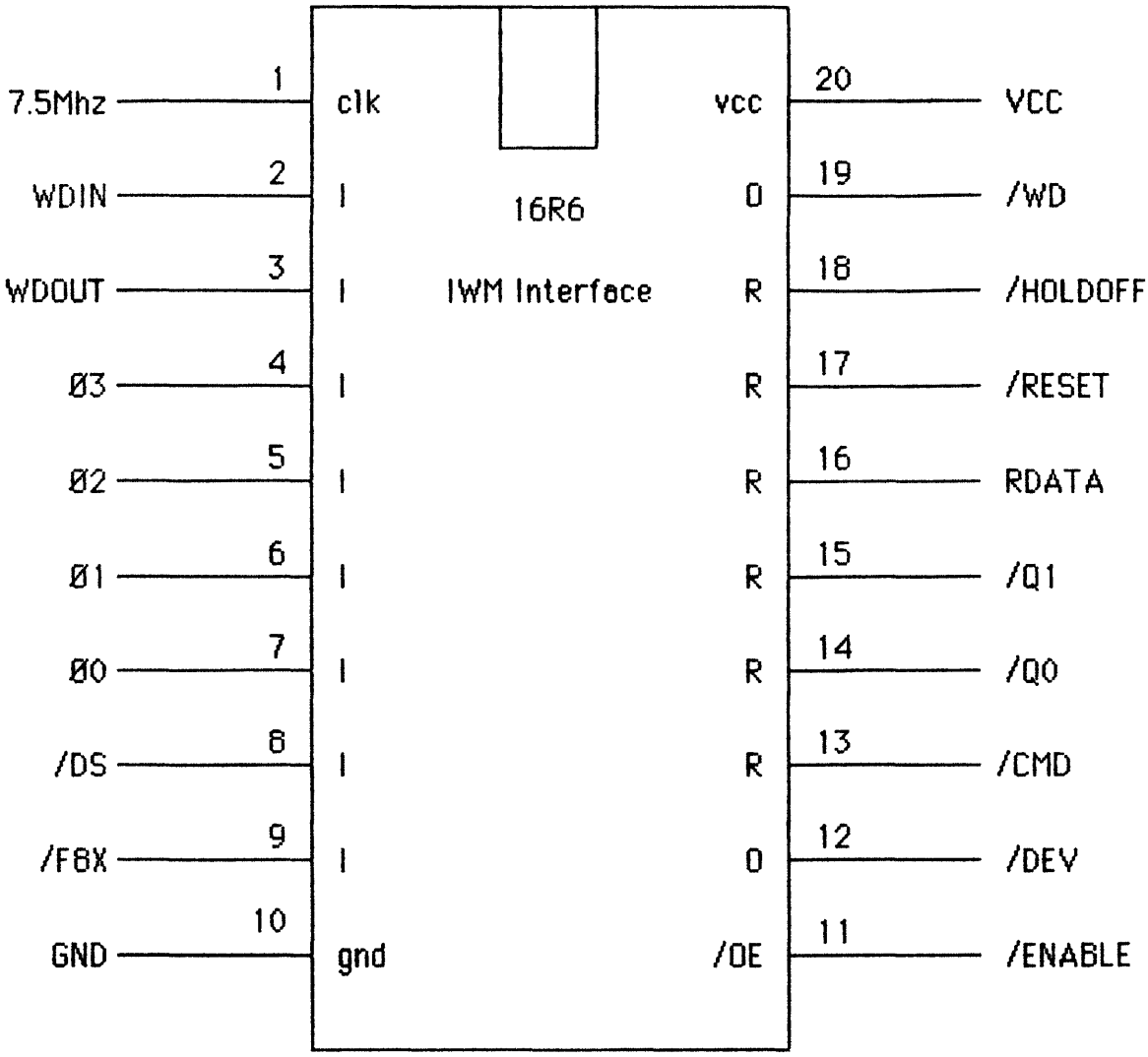

7.5Mhz
1
clk
WDIN
2
I
WDOUT
3
I
Ø3
4
I
Ø2
5
I
Ø1
6
I
Ø0
7
I
/DS
8
I
/F8X
9
I
GND
10
gnd
16R6
IWM Interface
vcc
20
VCC
O
19
/WD
R
18
/HOLDOFF
R
17
/RESET
R
16
RDATA
R
15
/Q1
R
14
/Q0
R
13
/CMD
O
12
/DEV
/OE
11
/ENABLE

Notes on IWM interface:

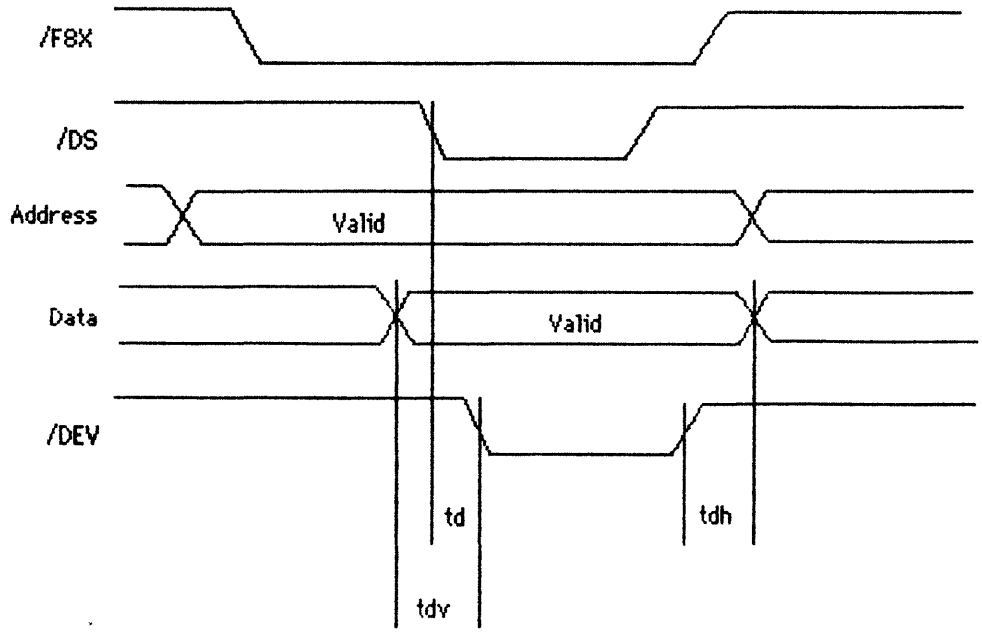
The IWM interface is a PAL which has several functions. It monitors the write data lines of the IWM's of both the host and Nisha. It also monitors the state of the phase lines coming from the host IWM. It produces read data pulses based on the phase lines' state and based on transitions seen on either of the write data lines. The PAL also produces controller reset and two handshaking lines: CMD and HOLDOFF.

In order to produce read data pulses, the PAL sees the transitions on the write data lines and outputs a high going pulse of a duration of two clock periods. This pulse is output on the read data line. Read data is enabled when the signal /ENABLE is asserted low. The read data line is held high unless the phase lines are in the following states:

Ø3	Ø2	Ø1	Ø0	read data level
1	0	X	X	read data
0	1	0	1	0

In order to read data the phase lines must be in the correct state (as indicated above-10XX).

The PAL produces the signal /DEV when both /DS and /F8X are asserted. Thus /DEV follows /DS when the correct address (F8X) is asserted on the address bus. Shown below is timing for a write to the IWM:



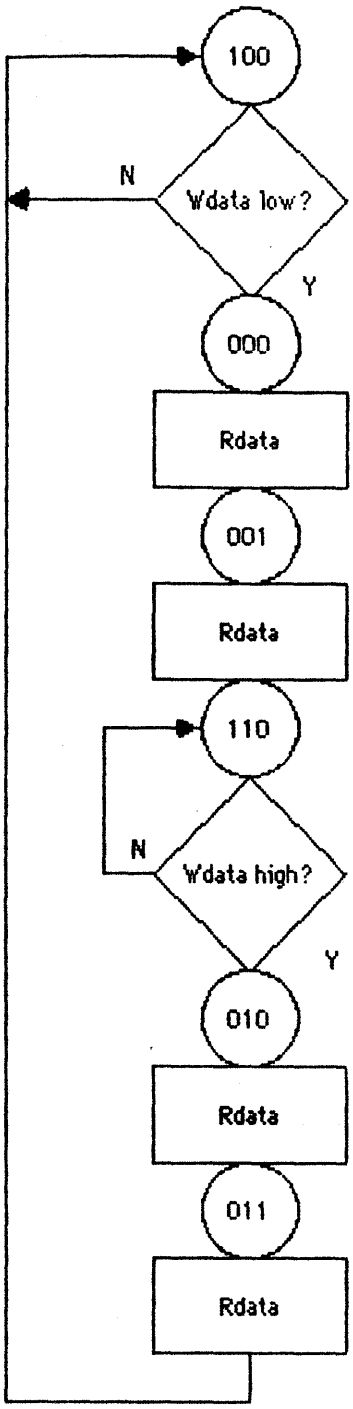
td (/DS to /DEV delay time) = 10 ns
tdh (/DEV to write data not valid delay) = 60 ns
tdv (write data valid to /DEV) = 60 ns

The signal /RESET is asserted low when the phase lines are 1100 and the signal /ENABLE is asserted low.

The signal /CMD is asserted low when the phase lines are 10X1 and the signal /ENABLE is asserted low.

The signal /HOLDOFF is asserted low when the phase lines are 101X and the signal /ENABLE is asserted low.

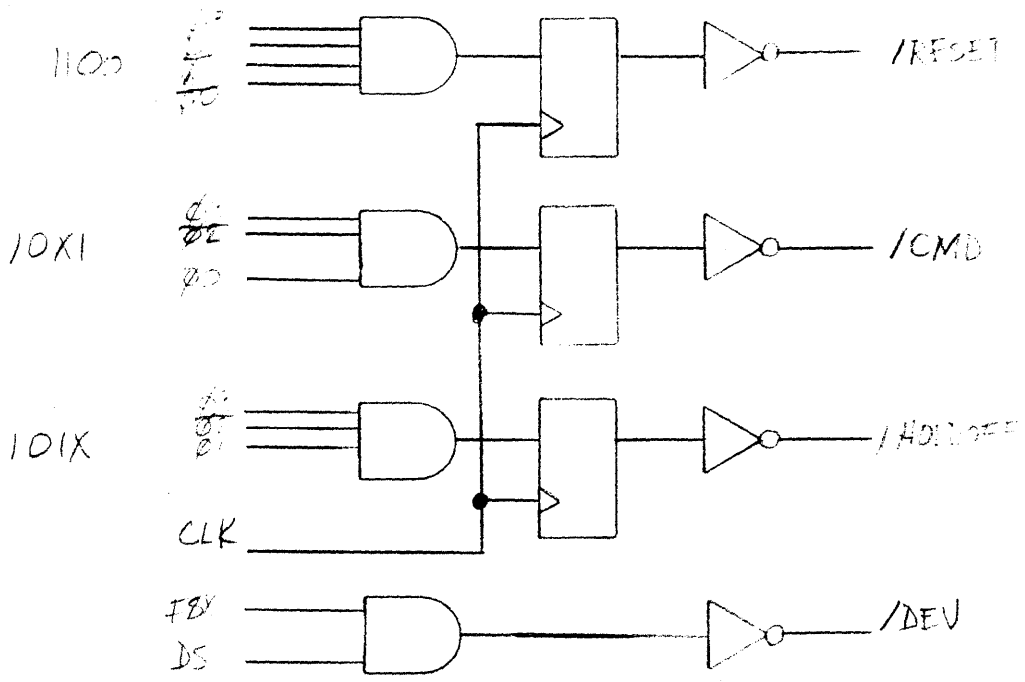
Because /RESET, /CMD, and /HOLDOFF are signals which are gated through flip-flops internally within the PAL, they are synchronized with the clock.

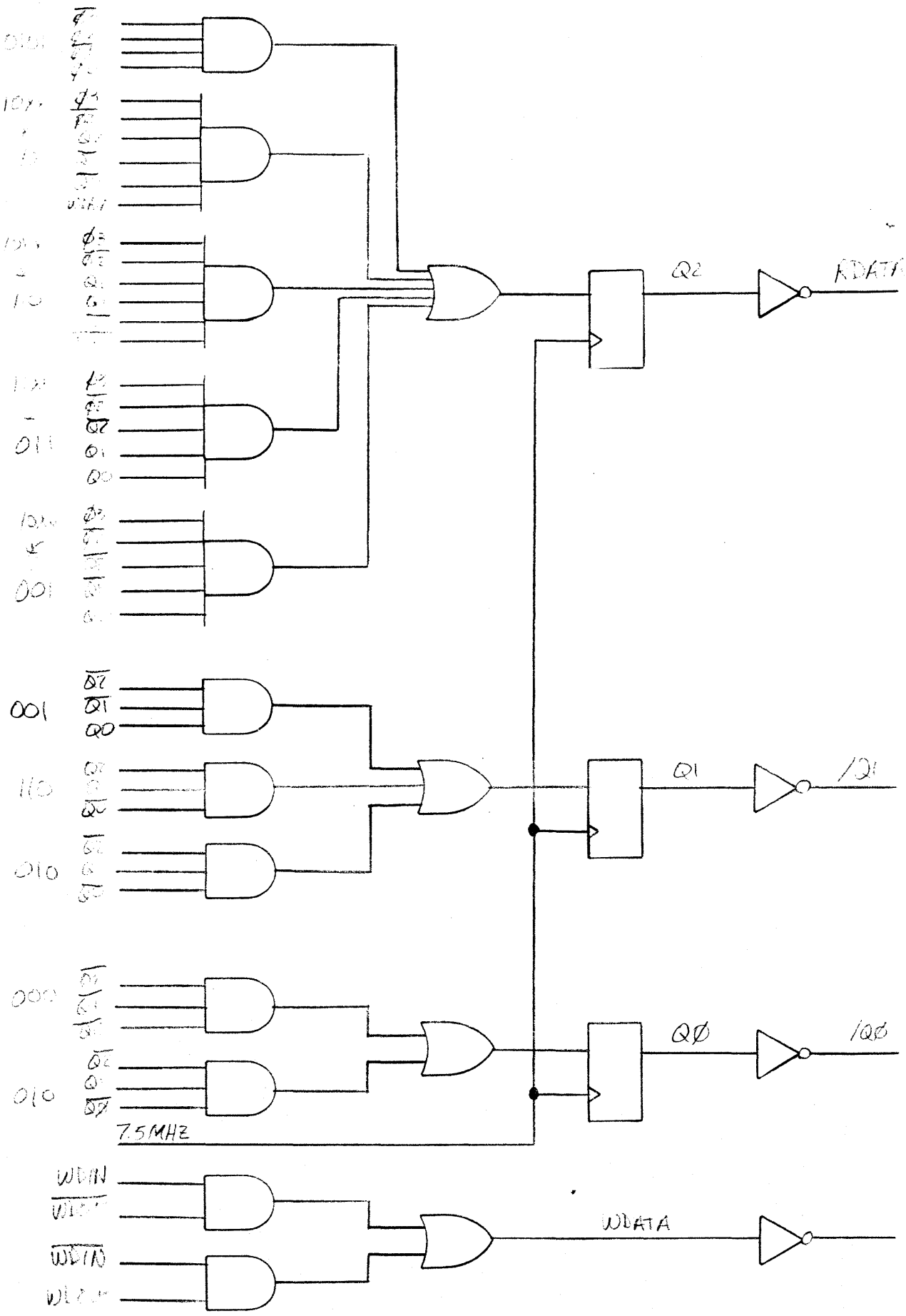


	00 01	11 10
0	0 1	3 2
1	4 5	7 6

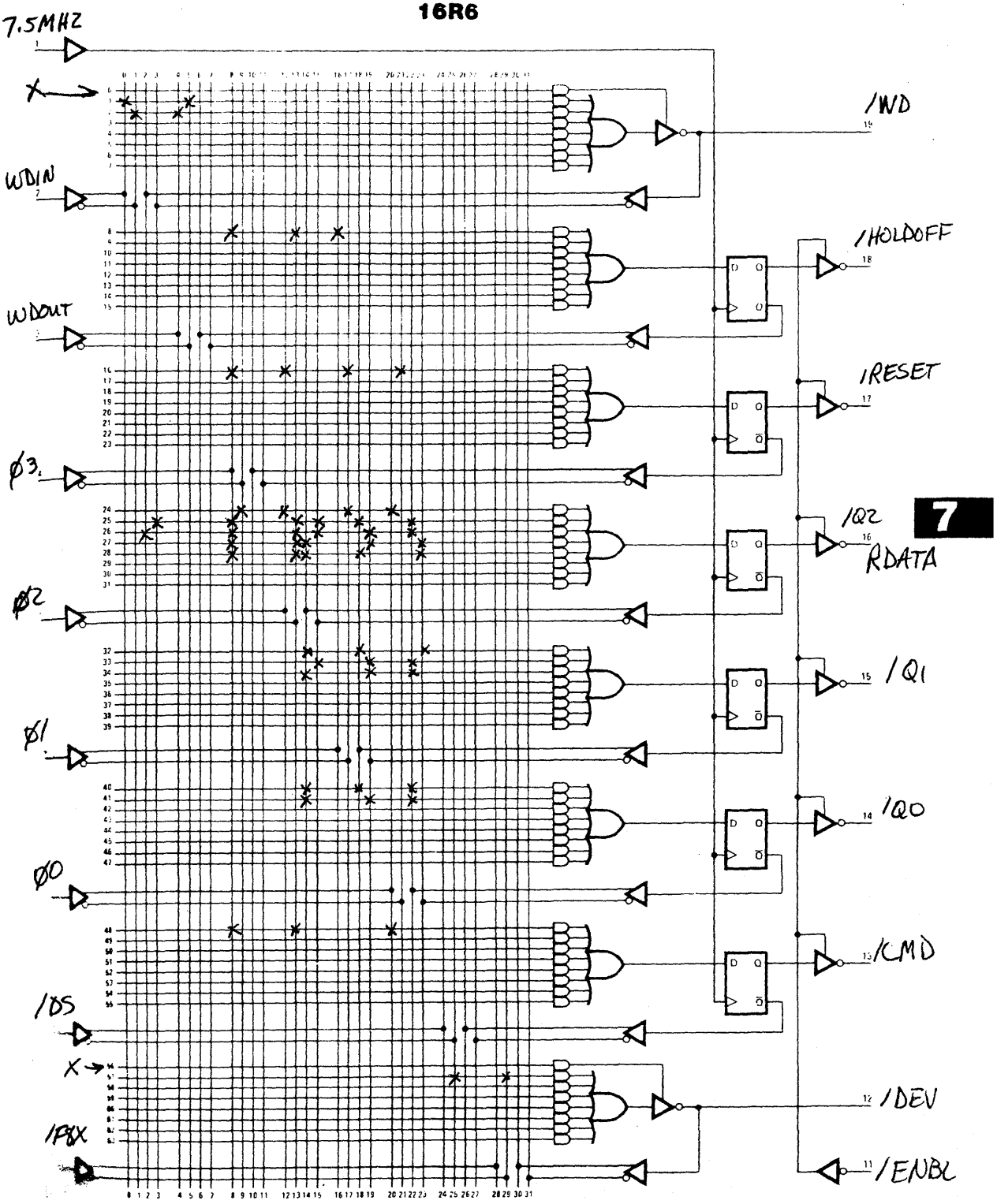
Phase Line Control for Renee

Mac to PAL				PAL to Z8			PAL to Mac
Phase3	Phase2	Phase1	Phase0	Reset	HoldOff	Host	Data to Host
1	0	0	0	0	0	0	
1	0	0	1	0	0	1	
1	0	1	0	0	1	0	
1	0	1	1	0	1	1	
1	1	0	0	1	0	0	
0	1	0	1				0
0	1	1	0				1
0	1	1	1				1


1100
/RESET
10X1
/CMD
101X
CLK
FBY
DS
/DEV


Q2
Q1
Q0
7.5MHZ
WDATA

16R6


7.5MHZ
WDIN
WDOUT
Ø3
Ø2
Ø1
Ø0
/DS
/PSX
/WD
/HOLDOFF
/RESET
/Q2
RDATA
/Q1
/Q0
/CMD
/DEV
/ENBL

7

```
 PAL16R6
IWM INTERFACE
NISHA
12/13/84
7 SCLK WDIN WDOUT PH3 PH2 PH1 PH0 /DS /F8X GND
/ENBL /DEV /CMD /Q0 /Q1 /Q2 /RESET /HOLDOFF /WD VCC

RESET:= PH3*PH2*/PH1*/PH0                    ; 1100 -PHASE LINES

CMD:= PH3*/PH2*PH0                           ; 10X1

HOLDOFF:= PH3*/PH2*PH1                       ; 101X

DEV = F8X*DS                                 ; MAKE DEVICE EN

WD = WDIN*/WDOUT                             ; A*/B +
   + /WDIN*WDOUT                             ; /A*B = EXOR!

Q2:= /PH3*PH2*/PH1*PH0                       ; 0101 -PHASE LINES
        + PH3*/PH2*Q2*/Q1*/Q0*WD             ; 100 = STATE NO.
        + PH3*/PH2*Q2*Q1*/Q0*/WD             ; 110
        + PH3*/PH2*/Q2*Q1*Q0                 ; 011
        + PH3*/PH2*/Q2*/Q1*Q0                ; 001

Q1:= /Q2*/Q1*Q0                              ; 001
   + Q2*Q1*/Q0                               ; 110
   + /Q2*Q1*/Q0                              ; 010

Q0:= /Q2*/Q1*/Q0                             ; 000
   + /Q2*Q1*/Q0                              ; 010

DESCRIPTION
THIS PAL HANDLES READ DATA EXTRACTION AND GENERATES CMD, HOLDOFF, AND RESET.

END
```