PRODUCT SPEC DISTRIBUTION

PS No. *1989 9368*   Title: *B4900 I/o Subsystem*

Revision: *B*   Release Date: *4/27/83*

PASADENA - CSG
6005	R. Bernstein	(2)
6002	R. Cole	(3)
7615	D. Edlin	(2)
6300	M. Emm	(1)
6210	N. Fleming	(2)
6210	D. Forbes	(1)
6800	B. Gaither	(1)
6900	A. Johnson	(1)
6004	E. Keeley	(1)
5400	D. Keene	(1)
5200	P. Lucey	(1)
5410	K. Smith	(1)
6600	R. Solt	(1)
6830	D. Speers	(1)
7607	T. Sternal	(1)
6004	J. Swensson	(1)
6620	H. Townsend	(1)
6810	L. Wasserman	(1)

WORLD HEADQUARTERS
J. M. Harris	(1)	2D96
W. Lapinsky	(1)	420
S. Offman	(1)	3A80
G. Piddington	(1)	4F76
J. Raker	(1)	3A97
D. Simmons	(1)	5A66
F. Vukmanic	(1)	2A16

LIEGE - CSG

J. Wery (1)

PISCATAWAY - CSG

J. McMahon (1)

PLG DIST SERV - LIVONIA

C. Muscillo (2)

SANTA BARBARA - CSG

K. De La Torre (1)

MISSION VIEJO - CSG

M. P. Feeney (1)
S. Samman   (1)

ED DEV CTR - EL MONTE

R. Tierney (2)

McLEAN, VA - F&SSG

R. Brochu (1)
M. Gaffney (1)

PAOLI - GVL

G. Smolnik (1)

TREDYFFRIN - CSG

A. Works   (1)

ATLANTA - DISG

C. Fillingim
T. Niesgoda

PLG DIST SERV - SEFDC

G. Onderbeke

PLG DIST SERV - NEFDC

L. T. Hardy

ATLANTA - PPD

C. Hammer
J. Stossel

NOTE: For changes to this list, advise N. Fleming;
      Engineering Operations (6210), Pasadena, CA 91109.

COMPANY CONFIDENTIAL

PRODUCT SPECIFICATION

REVISIONS

REV LTR	REVISION ISSUE DATE	PAGES REVISED, ADDED, DELETED OR CHANGE OF CLASSIFICATION	PREPARED BY	APPROVED BY
A	12/08/82	Initial Issue ECN 47960	L. Simpson D. Leslie	D. Simpson M. Rooke S. Davis N. Ruddick P. Lamson J. Swensson
B	4/27/83	Updated I/O Descriptors, Section 3.5.5 per REE 91224. ECN 48343	L. Simpson D. Leslie	D. Simpson N. Ruddick J. Swensson R. Cole

PAS 1968   REV. 8-73

PS76

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page   1

TABLE OF CONTENTS

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page   2

1   INTRODUCTION

1.1   PREFACE

This specification describes the functional requirements for
an I/O subsystem used in the B4900 system. The major
functional units are the I/O Processor, the Data Link
Processors (DLP's), and the DLP Base Modules. Functions
common to DLP's are briefly described. Details of cabinets
and physical location of the modules within the subsystem are
described in the applicable System Product Specifications.

1.2   RELATED SPECIFICATIONS

The information contained in the following documents is
pertinent to this specification.

P.S. NO.	NAME
1987 1037	B4900 Central System
1984 0263	B4900 Processor

S.D.S. NO.	NAME
2323 7399	Message Level Interface (UIO)
2323 7381	DLP Subsystem (UIO)
2360 1016	DLP Test Bus on Universal Console
1970 9922	Shared System Processor Subsystem

STD. NO.	NAME
1284 9097	Burroughs EBCDIC/ASCII

1.3   PRODUCT IDENTIFICATION

M&E numbers for orderable units are specified in the B4900
System Index.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B Page 3

2   GENERAL DESCRIPTION

The I/O Subsystem provides interface for peripheral
controllers called Data Link Processors (DLP's). LCP's used
in the B4800 are not compatible. I/O operations are
described by formatted data fields in main memory called I/O
Descriptors.

Each DLP communicates with its connected device in a manner
unique to that device.

Adapters which provide the required interface to each type of
DLP must be installed in the DLP base when that type of
peripheral is used.

2.1   I/O CHANNEL USAGE

Programmatically a peripheral unit communicates with the
system via an I/O channel. Each I/O channel is provided with
channel scratchpad memory, an area of main memory for Result
Descriptor storage, and a channel number. The I/O channel
responds to the IIO (OP 94) and RAD (OP 92) processor
instruction.

Use of channel 08 is restricted to the IOP to facilitate
execution of certain operations and it is not included in
channel configuration/allocation.

The system configuration allows one or two IOP's. Each IOP is
allocated 32 channels.

2.2   DLP INTERFACE

The DLP's interface to main memory and the processor via the
I/O Processor (IOP). The IOP transforms a "DLP set" of I/O
Descriptors into Command Messages (C/M's) which are acted
upon by the DLP's. The DLP's accept these instructions,
control the operation of the peripheral device and report
results. Both the DLP's and the IOP can return result status
messages which are stored in reserved locations in main
memory.

The DLP subsystem includes up to four DLP Base Modules
connected to each IOP, and up to eight DLP's in each Base
Module. A maximum configuration contains 64 DLP's.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 4

2.3   PROCESSOR INTERFACE

The IOP interfaces to the Processor via two state toggles
contained in the Read/Write module. The processor partially
validates the Instruction and Descriptor before notifying the
IOP. The IOP then completes Descriptor accesses and
validation followed by communication to the selected DLP (I/O
Channel).

The first state toggle is I/O Descriptor Ready. It is set by
the processor after an I/O Descriptor is ready. The selected
IOP will reset it after obtaining its descriptor.

The second state toggle is I/O Complete Interrupt. An IOP
will set it whenever an I/O completes. The processor will
reset it.

2.4   MEMORY ACCESS BANDWIDTH

The B4900 I/O Subsystem has a maximum bandwidth of 16.0
megabytes per second (peak) when DLP Interface Cables do not
exceed 50 feet in length.

Access to main memory is shared by the IOP's and the
Processor; highest priority is allocated to the IOP's. IOP
#2 has a higher priority than IOP #1. The Processor uses
memory cycles available on a lowest priority basis.

2.5   SHARED SYSTEMS

The Shared System Processor (SSP) will appear to the user as
a replacement of the File Protect Memory 2 (FPM2). The SSP
provides limited system-to-system communication by the MCP
and user programs via disk block-level locking and unlocking
capabilities. The SSP is a four-card storage device
(residing in a UIO DLP base) which can be accessed by up to
four Medium Systems 800/900 Series Computer Systems when
sharing one or more disk file subsystems or disk pack
subsystems. See Product Specification 1970 9922, Shared
System Processor

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

```
                                    +------------+
                                    |   1989 9368
          +-------------------------+
          |
          |              B4900 I/O SUBSYSTEM
          |
          +----------------------------------------
COMPANY CONFIDENTIAL        PRODUCT SPECIFICATION  Rev. B  Page  5
```

FIGURE 2-1 B4900 CENTRAL SYSTEM MAJOR FUNCTIONS
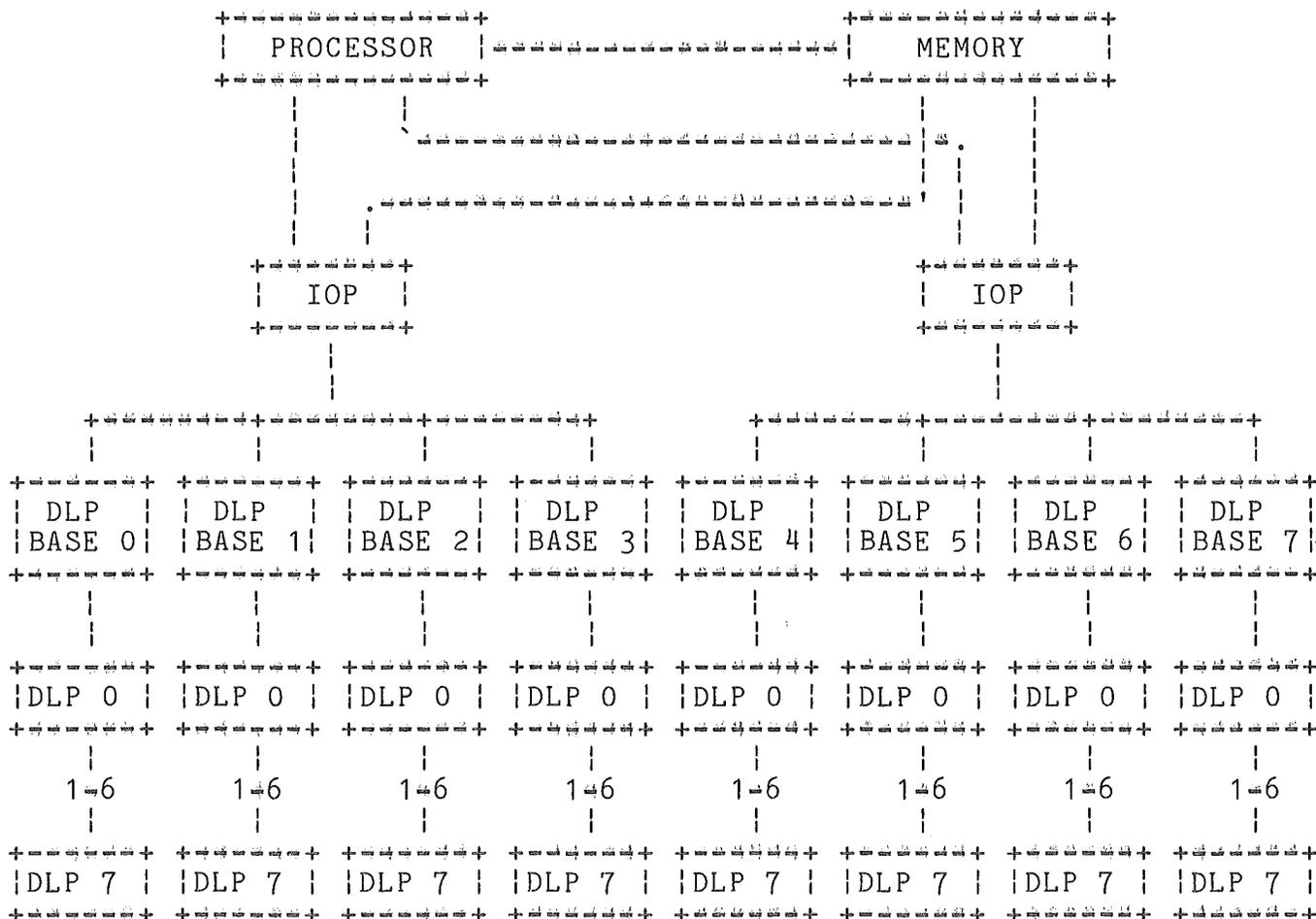
```
      +------------------+                   +--------------+
      |   PROCESSOR      |-------------------|   MEMORY     |
      +------------------+                   +--------------+
               |      |                            |     |
               |      `----------------------------| ..  |
               |                                    |  .  |
               |      .-----------------------------'  |  |
               |      |                                 |  |
               |      |                                 |  |
      +---------+                            +----------+
      |   IOP    |                           |   IOP    |
      +---------+                            +----------+
               |                                  |
               |                                  |
   +-----------+-----------+-----------+   +---------+---------+---------+
   |           |           |           |   |         |         |         |
+-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+
| DLP   |  | DLP   |  | DLP   |  | DLP   |  | DLP   |  | DLP   |  | DLP   |  | DLP   |
|BASE 0 |  |BASE 1 |  |BASE 2 |  |BASE 3 |  |BASE 4 |  |BASE 5 |  |BASE 6 |  |BASE 7 |
+-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+
   |          |          |          |          |          |          |          |
   |          |          |          |          |          |          |          |
+-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+
|DLP 0  |  |DLP 0  |  |DLP 0  |  |DLP 0  |  |DLP 0  |  |DLP 0  |  |DLP 0  |  |DLP 0  |
+-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+
   |          |          |          |          |          |          |          |
  1-6        1-6        1-6        1-6        1-6        1-6        1-6        1-6
   |          |          |          |          |          |          |          |
+-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+
|DLP 7  |  |DLP 7  |  |DLP 7  |  |DLP 7  |  |DLP 7  |  |DLP 7  |  |DLP 7  |  |DLP 7  |
+-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+  +-------+
```

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page   6

3   OPERATION

An I/O request is an Initiate I/O instruction specifying the
address in main memory of the appropriate I/O Descriptor and
the channel for which it is intended.

The I/O Descriptor contains the OP code and variants for the
DLP and the beginning and ending main memory address (A and B
address) of the information buffer and an optional device
dependent C address, e.g. disk address.

The processor accesses the descriptor and performs all
invalid I/O tests. If the IIO is valid, it will store the
channel and descriptor in memory at the IOP scratchpad
location for the IOP channel.

The IOP reads this descriptor and sends the OP code and
variants to the selected DLP. The DLP and IOP validate the
OP code and accept or reject the request.

The IOP puts the A and B addresses into channel scratchpad
memory. The A address is the low order (or beginning) address
and the B address is the high order (or ending) address
delineating a main memory buffer area.

Note: IOP channel scratchpad is located in sub MCP-base
      memory and is not part of the addressing space of the
      operating system or user programs.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 7

3.1   OP 94 -IIO (INITIATE I/O)

3.1.1   IIO Instruction Format

         This is a privileged instruction executed by the Processor.
         Refer to B4900 Processor Product Specification.

         The address of the descriptor may be indexed, 8-digit
         extended or 6-digit non-extended and must specify unsigned
         numeric or indirect.   If indirect address is specified, the
         final address must specify unsigned 4-bit format. The I/O
         Descriptor must start at an even address.

         The format for the Initiate I/O Instruction is shown here for
         reference:

```
            +--------+--------+-------+----------+
            |  OP    |  AF    |  BF   |  A----A   |
            +--------+--------+-------+----------+
```

                OP = 94
                AF = Not used by IOP
                BF = I/O Channel number that is to
                     receive the I/O Descriptor
                     (00-77 octal) or (08)
                     BF may contain an Indirect Field
                     number to reference an I/O Channel
                     number stored at locations 00
                     through 38 (BF = C0 - F8).
         A----A = Address of the I/O Descriptor

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page   8

3.1.2   I/O Descriptor Format

The information in the I/O Descriptor (See Table 3-1) is as follows:

1. Type of I/O operation (2 digits)

2. Variants (4 digits)

3. Begin Address (absolute) when present

4. End Address (absolute) when present

5. Disk address or additional variants when present

The IOP sends a converted OP code and variants to the designated channel. If a "C" address is present it is also sent to the channel.

The begin and end addresses, if present, are placed in the reserved locations of the channel's address memory. The begin address and the end address must be even. The B address must be greater than the A address. Neither address may contain undigits.

The Processor writes an Invalid I/O Result Descriptor (Processor R/D bits 1,2, and 4) and sets the Interrupt Flip Flop if:

1. The channel is busy.

2. The channel designated is invalid.

3. The Descriptor address is not even.

4. The OP code is not 40 or greater, but less than 80.

3.1.2   I/O Descriptor Format (Continued)

I/O Descriptor Format


```
+-----------+-----------+-----------+-----------+-----------+
¦    OP     ¦  Variants ¦ A-Address ¦ B-Address ¦ C-Address ¦
¦           ¦           ¦  (Begin)  ¦   (End)   ¦           ¦
+-----------+-----------+-----------+-----------+-----------+
¦           ¦           ¦           ¦           ¦           ¦
¦<-2 digits->¦<-4 digits->¦ <-6 digits-> ¦ <-6 digits-> ¦ <-6 digits-> ¦
¦           ¦           ¦    or     ¦    or     ¦    or     ¦
¦           ¦           ¦ <-8 digits->¦ <-8 digits->¦ <-8 digits->¦
```


6-digit Address Format


```
+---+---+---+---+---+---+
¦ 6 ¦ 5 ¦ 4 ¦ 3 ¦ 2 ¦ 1 ¦
+---+---+---+---+---+---+
¦                       ¦
¦<-- All digits = 0-9-->¦
```


8-digit Address Format (A-Address or B-Address only)

        (8-digit format flag = C)
                ¦
                v

```
+---+---+---+---+---+---+---+---+
¦ C ¦ 7 ¦ 6 ¦ 5 ¦ 4 ¦ 3 ¦ 2 ¦ 1 ¦
```


8-digit Address Format (C-Address only)

```
+---+---+---+---+---+---+---+---+
¦ 8 ¦ 7 ¦ 6 ¦ 5 ¦ 4 ¦ 3 ¦ 2 ¦ 1 ¦
```

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 10

3.2   CHANNEL NUMBERS

When a DLP is installed, it is assigned a unique number
called its "Channel Number". This number appears in the
Initiate I/O or RAD instruction BF Field.

DLP's get their Channel Number from a strap setting within
each DLP and are numbered with decimal values of 0-7.

DLP Channels assigned to IOP #1 are numbered from 00-07 in
the first Base Module, 10-17 in the second Base Module, 20-27
in the third Base Module, and 30-37 in the fourth Base
Module.

DLP channels assigned to IOP #2 are numbered 40-47 in the
first base module, 50-57 in the second base module, 60-67 in
the third base module, and 70-77 in the fourth base module.

3.2.1   Channel Scratchpad Memory

Channel Scratchpad Memory (also called a Channel Scratchpad
Entry) locations are used to contain the Begin and End
addresses for I/O memory transfer operations. Each
Scratchpad Entry corresponds to a Channel Number.

Channel Scratchpad Memory for all DLP's is wholly contained
in main memory.

3.2.2   IOP Channel 08

For certain I/O Descriptors (see Table 3-1; OP 71, 72, 73)
the IOP must perform the operation independent of the DLP.
The IIO Instruction specifies "Channel 08" in those cases to
facilitate proper performance of the operation by the IOP.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 11

3.3   RESULT DESCRIPTOR STORAGE

Result Descriptors are stored in reserved main memory
locations. The location for a specific I/O Channel is
calculated by multiplying the Channel Number by 20 and adding
100.

When a DLP sends a Result Descriptor (also called a result
status message) to the IOP, the IOP accesses main memory
directly to store the first word. The possible remaining
words are stored in IOP scratchpad and may be accessed with a
"Read Extended R/D (OP=70) or with a RAD with AF=22.

3.4   DATA TRANSLATION (EBCDIC/ASCII)

If data translation is required for the DLP Subsystem,
BCL/EBCDIC translation is performed by the DLP and
ASCII/EBCDIC translation is performed by the IOP. See
Appendix A for EBCDIC/ ASCII Translation Table and Appendix B
for ASCII/EBCDIC Translation.

Because of the diversity of interpretation possible by the
various peripheral devices in use, the graphic symbols
associated with the bit patterns shown are those most
commonly encountered by Burroughs users.

This translation follows standard Burroughs EBCDIC/ASCII
translation (see Standard No. 1284 9097 "Burroughs
EBCDIC/ASCII Code Translation").

3.5   SUBSYSTEM DESCRIPTION

3.5.1   Base Module Configuration

A Base Module contains up to eight DLP's, a Distribution Card
(or cards), two Terminator Cards, and one Maintenance Card.

3.5.1.1 Distribution Card

A DLP connects to the IOP via a Distribution Card. The
algorithms for establishing connection between a DLP and the
system are implemented on the Distribution Card. A system
initiated request for connection is designated "Poll Test"
and a DLP initiated connection is designated "Poll Request".

3.5.1.2 Maintenance Card

Each DLP Base Module contains one non-optional Maintenance
Card which has the capability of exercising a selected DLP
for maintenance and diagnostic purposes.

Control of the maintenance features is provided by the
Maintenance Processor I/O Test Bus which is connected to each
DLP Base Module. The Test Bus has facilities for thoroughly
exercising any DLP on that Base. See the DLP Subsystem
System Design Specification, the DLP Test Bus System Design
Specification and the individual DLP Product Specifications
for a description of the Maintenance Processor Test Bus and
its functions.

3.5.1.3 DLP Address Designation

The address designation of a DLP in a Base Module is
determined by jumpers on one card of each DLP. This address
is independent of the DLP's position within the Base Module.
Its Channel Number is determined by a combination of base
number and address within the base.

3.5.2   I/O Processor

The IOP transforms system I/O Descriptors into the
appropriate operational messages relevant to each DLP.
Result messages from the DLP in the form of result
descriptors are not translated by the IOP but are stored in
memory as transmitted by the DLP's. The IOP performs all
information transfers between the DLP's and main memory
necessary to support the I/O capability.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 13

3.5.2.1   IOP to DLP Communication

The IOP receives I/O Descriptors from main memory.   The IOP
then connects to the requested DLP (indicated by the Channel
Number) and sends it the descriptor information in message
format.   The IOP then becomes DLP Status driven. This means
that the IOP responds to the various DLP States (including
memory requirements) as indicated via the control lines
between the DLP and IOP.

The IOP controls the transfer of information between main
memory and the DLP's. The DLPs' memory requirements drive
the IOP for all data transfers except initiation.

Only the IOP can initiate connection. The IOP initiates a
connection by performing an algorithm called a "Poll Test".
The DLP requests a connection by performing an algorithm
called a "Poll Request". A Poll Request is only performed by
the DLP in response to a Poll Test previously performed by
the IOP. While the DLP is connected to the IOP it indicates
its status via control lines.   A DLP initiating a Poll
Request must compete with the other DLP's in the system for
connection. Connection is granted on a priority basis (see
Section 3.5.4).

During an operation a DLP may indicate to the IOP that the
DLP wishes to disconnect. The IOP then disconnects from the
DLP, and may service other DLP's at this time.   When the
original DLP wishes to reconnect for further use of main
memory, or to send a Result Status Message, it again performs
the Poll Request algorithm.

Communication between the IOP and DLP's is accomplished by a
standard flow discipline common to all DLP's (see the DLP
Subsystem System Design Specification for details).

Data and Control Messages are transmitted in 16 bit words
with a vertical odd parity bit. The last word of the message
is a longitudinal odd parity word with its vertical odd
parity bit.

Vertical and longitudinal parity is checked by both the IOP
and the DLP. If a parity error is detected by the DLP, the
DLP reports this in its result information transmission and
halts the operation. If the IOP detects a parity error, an
indication of this condition is inserted in the IOP Result
Descriptor.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 14

3.5.3   DLP Functions

The DLP accepts a control message (OP code and variants) and buffers it. The control message consists of from one to three message transmissions from the IOP. The number of transmissions is DLP dependent. The first transmission always contains one digit of OP code and three variant digits. The optional second and third transmissions contain the "C" address (see Section 3.5.5 and Table 3-1).

The DLP performs the operation specified by the control message, and, at the completion of the operation, generates a result status message which reports status and error conditions.

See the individual DLP product specifications for functional details concerning DLP and peripheral device dependencies.

3.5.4   Priority Resolution

Only one DLP may be connected to memory at a time through each IOP and all DLP's may request connection simultaneously. The decision as to which DLP is connected is based on the DLP's designated priority. Priority is only used to arbitrate DLP connection to the system; it is not needed for system connection to a DLP. Priority is usually based upon the access needs of the device which the DLP controls (speed, stream mode, etc.). Priority designations are of two types. The first type is the priority of the DLP within its Base Module (Base Priority). The second type (highest) is the priority of the DLP within the I/O Subsystem (Global Priority).

3.5.4.1 Base Priority

There are eight priority positions (one for each possible DLP) on the Distribution Card for specifying Base Priority. The DLP is assigned to one of these positions when it is installed. No two DLP's have the same Base Priority within a DLP Base Module.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 15

3.5.4.2   Global Priority

There are seven levels of Global Priority within the I/O
Subsystem.   One of these levels is assigned to each DLP via
its Distribution Card (or Cards).   Two or more DLP's may have
the same Global Priority. Usually the DLP with the highest
Base Priority is assigned the highest Global Priority.   If
two DLP's of the same Global Priority are located in
different bases and are simultaneously requesting access,   it
will be granted on a basis determined by the IOP.   More than
one DLP may have the same Global Priority within a   DLP   Base
Module.

A level of highest Global Priority is also provided and is
designated as an Emergency Request.   An Emergency Request is
defined to be a condition in which lack of immediate memory
access will necessitate difficult error recovery or operator
intervention.

When the IOP is in an Idle state, all the Emergency Request
and Interrupt Request signals are tested. The selected base
is determined by global priority.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

+------------------------------------+
| |
| B4900 I/O SUBSYSTEM |
| |

| 1989 9368

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 16

3.5.5   I/O Descriptors

The DLP Subsystem I/O Descriptors are of two types. The
first type, General Descriptors, are READ, WRITE, TEST and
ECHO. This type requires a minimum of IOP initiated
intervention in the I/O operation. The second type, Special
Descriptors, are DISCONTINUE, CONDITIONAL CANCEL and
UNCONDITIONAL CANCEL. This type requires substantial IOP
initiated intervention in the operation.

The I/O Descriptors sent to the IOP are shown in Table 3-1.
Operation (OP) codes 40 thru 54 are translated into a DLP OP
code digit (digit A). The "V" digits in the variant field
carry information used in the DLP OP code variant digits
(digits B, C & D) of the 4 digit descriptor information sent
to the DLP. The "I" digit is used by the IOP as shown in the
table.

The descriptor information sent to the DLP may also include
the C-address field. If the DLP requests this information,
and the I/O descriptor is not a 3-address OP code, the DLP
stops in an unknown, unspecified state. The C-address error
in DLP result Descriptor (Bit D1) is set. An Unconditional
Cancel descriptor to IOP channel 8 (7200 CC) is required to
place the DLP in the proper idle state.

If the I/O descriptor is a 3-address OP code, and the DLP
does not require the C-address information, the C-address
information is ignored.

3.5.5   I/O Descriptors (Continued)

TABLE 3-1   I/O Descriptors (as received by the IOP)

Description	OP Code	Vari- ants	A Address	B Address	C Address
READ					
Forward (2-byte)	40	IVVV	A----A	B----B	
Forward (5-byte)	50	IVVV	A----A	B----B	CCCCCC
Forward (6-byte)	60	IVVV	A----A	B----B	CCCCCCCC
Backward	41	IVVV	A----A	B----B	
WRITE					
Forward (2-byte)	42	IVVV	A----A	B----B	
Forward (5-byte)	52	IVVV	A----A	B----B	CCCCCC
Forward (6-byte)	62	IVVV	A----A	B----B	CCCCCCCC
TEST					
(2-byte)	44	IVVV			
(5-byte)	54	IVVV	A----A	B----B	CCCCCC
(6-byte)	64	IVVV	A----A	B----B	CCCCCCCC
ECHO					
(Maint) (2-address)	48	IVVV	A----A	B----B	
SPECIAL					
Conditional cancel	71	uvcc	(generates TEST OP = 28uv)		
Unconditional cancel	72	00cc	(generates Selective Clear)		
Test Discontinue	73	uvcc	(DISCONTINUE OP = 2Auv)		

NOTES:

Addresses

A----A = Low-order address of memory buffer (6 or 8 digits)
B----B = High-order address of memory buffer (6 or 8 digits)
C----C = Peripheral Device Information (6 or 8 digits)

Variants

I = Variants used by the IOP
    Bit 8 = Inhibit data transfer to memory
    Bit 4 = 0 (OMEGA)
    Bit 2 = ASCII translation
    Bit 1 = Real time...
VVV = DLP variants sent unmodified to DLP
CC = DLP Channel designation (00 - 77)
u = Unit Number
v = Variant

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 18

3.5.5   I/O Descriptors (Continued)

OP Codes

4x, 5x, 6x are converted to DLP OP Codes
              Read   : OP = 8
              Write : OP = 4
              Test   : OP = 2
              Echo   : OP = 1
71 is converted by IOP to DLP OP, Variants = 28uv
  72 is converted by IOP to DLP selective clear
     (terminate).
73 is converted by IOP to DLP OP, Variants = 2Auv

(71, 72 and 73 are sent channel 8--IOP channel).

Not compatible with DL-2 PE Mag Tape DLP.

3.5.5.1   Forward Operations

The A address is used as the beginning address and the B
address as the ending address. The A address is incremented
the appropriate amount each time data is stored or read. The
B address remains unchanged.

3.5.5.2   Backward Operations

The B address is used as the beginning address and the A
address as the ending address. The B address is decremented
the appropriate amount each time data is stored.   The A
address remains unchanged.   Data is effectively read in
reverse order between the A and B addresses.

3.5.5.3   Test Operations

Test operations are those wherein no data transfer occurs
between the DLP and the area of system main memory specified
by the A and B addresses.

An application for a test operation would be one in which the
system interrogates a particular DLP to determine the status
of that DLP's attached peripheral or to cause the attached
peripheral to take some action not otherwise requiring data
from the system (e.g. printer channel skip).

| | 1989 9368 |

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION Rev. B Page 19

3.5.5.4 Echo Operations

An echo operation is one wherein a complete message buffer is transmitted from the system, beginning at the "A" address, to a DLP.

The DLP, when its buffer area is full, indicates to the system that it wishes to disconnect. After disconnection, the DLP performs the Poll Request algorithm and, when reconnected, transmits the same (except where translation is involved) buffer message to the system, reporting Result Status when completed.

Individual DLP buffer sizes are peripheral device dependent (see individual DLP product specifications for sizes). The buffer area in main memory must be twice the size of the DLP buffer. The first half of the system main memory buffer is to contain the message to be "echoed". When the DLP returns the message it will be stored in the last half of the system buffer.

The echo operation will not cause peripheral device participation. It is meant to provide a means of programmatic verification of the data paths between the system and a DLP. The buffer size must be correct or proper system operation may be affected.

3.5.5.5 Extended Result Descriptor Store

This instruction is used to obtain additional Result Descriptor words sent by DLP's but not stored by the IOP.

The IOP accepts up to three words of Result Descriptor from a DLP.

The first word is stored with the IOP Channel Result Descriptor word which contains one bit to signify that the DLP's complete Result Status Message has not been stored.

The remaining word(s) are stored in IOP channel scratchpad. These extra words remain intact until the next Read, Write, Test or Echo operation is performed.

To retrieve this extra information, the Extended Result Descriptor Store operation is sent to the appropriate channel. The A address must be modulo four.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION Rev. B Page 20

3.5.5.5 Extended Result Descriptor Store (Continued)

An Extended Result Descriptor Store operation may only be
issued to a non-busy channel. Variant digits must be zero.
No communication actually takes place with the addressed DLP.

> NOTE: A RAD with AF=22 may also be used to retrieve
>   Extended Result Descriptors.

3.5.5.6 Cancel Operations

These operations must be sent to channel 8 with the variant
digits specifying which busy channel is to receive the
cancel.

Only one cancel can be pending at any given time. Issuing a
Cancel (Conditional or Unconditional) while one is already
pending will cause inconsistent and unreliable results.

A Cancel is considered pending from the time it is initiated
until a Result Descriptor providing the result status
information for that cancel is stored in the Channel 8
location address 260.

Conditional Cancel

A Conditional Cancel is converted by the IOP to a Test
operation with a "28uv" descriptor. This Test OP is then
passed to the specified busy DLP channel.

If the DLP is not busy or will not accept the cancel or some
other error condition occurs, the IOP stores a result
descriptor for channel 8 with Bit C2 set true and other
applicable error bits also set true.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 21

3.5.5.6   Cancel Operations   (Continued)

If the Cancel OP is successfully accepted by the DLP, the IOP
stores an OP-Complete-No-Exception result descriptor for
channel 8. The cancelled channel also returns a result
descriptor in its channel location in memory.

Unconditional Cancel
────────────────────

An Unconditional Cancel attempts a connection with the
specified DLP and, if successful, generates a Selective Clear
for that DLP.

If the DLP responds by clearing itself, the IOP stores an
Operation-Complete-No-Exception result descriptor in the
Channel 8 result descriptor area and no result descriptor
occurs for the DLP channel.

If the IOP cannot make a connection or the DLP does not clear
before a Timeout period expired, the IOP stores a result
descriptor for Channel 8 with Bit C2 set true and other
applicable error bits also set true.

A DLP that will not Clear when Unconditionally Cancelled is
failing.

Discontinue
───────────

A Discontinue is converted by the IOP to a Test operation
with a "2Auv" descriptor. This Test OP is then passed to the
specified busy DLP channel.

If the DLP is not busy or will not accept the discontinue or
some other error condition occurs, the IOP stores a result
descriptor for channel 8 with Bit C2 set true and other
applicable error bits also set true.

If the Discontinue is successfully accepted by the DLP, the
IOP stores an OP-Complete-No-Exception result descriptor for
channel 8. The discontinued channel also returns a result
descriptor in its channel location in memory.

| | 1989 9368 |

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION Rev. B Page 22

3.5.6   Result Descriptors

Result Descriptors for all Channels are stored at memory
locations determined by multiplying the Channel Number by 20
and adding the value 100.

The first four digits of the Channel Result Descriptor
contains status information for the Channel as reported by
the IOP.

The second four digits are used by the Processor only.

The third four digits contain the first Result Descriptor
word as sent by the DLP.   This word contains specific
information about the operation status of the DLP portion of
the operation.

If a DLP sends more than one Result Descriptor word and the
second or third word is non-zero, the first word is stored as
described above, the Extended Result Descriptor bit is set
TRUE and the extra DLP Result Descriptor words are held in
IOP Scratchpad for that channel.   These words may   be
retrieved by requesting an Extended Result Descriptor Store
operation or a RAD.

The first four bits of the first DLP Result Descriptor word
are usually common to all DLP's, the remaining bits are
unique to the DLP and are defined in the   product
specifications for those DLP's (see Sec. 3.5.6.2).

3.5.6.1 IOP Portion Of The Channel Result Descriptor

        Bit   Bit

        A8: Operation Complete   C8: Extended Result Desc. Present
        A4: Exception Condition   C4: DLP Address Word Parity Error
        A2: DLP Timeout   C2: Unable to Perform OP
        A1: DLP Illegal Status   C1: MLI Vertical Parity Error

        B8: DLP Not Present   D8: MLI Longitudinal Parity Error
        B4: Memory Parity Error   D4: Result Descriptor Parity Error
        B2: Op Buffer Full (Not used)   D2: A or B Address Error
        B1: Base Port Busy   D1: C-Address Error

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL

PRODUCT SPECIFICATION   Rev. B   Page 23

3.5.6.1 IOP Portion Of The Channel Result Descriptor (Continued)

A8 Operation Complete

This bit is set TRUE at the completion of an operation on that Channel.

A4 Exception Condition

This bit is set TRUE if any condition bits are set in the IOP or DLP portion of the Channel Result Descriptor.

A2 DLP Timeout

A DLP response to an IOP strobe was not received within 56 uSEC.

A1 DLP Illegal Status

The connected DLP generated an illegal sequence of Status as defined by the general MLI flow.

B8 DLP Not Present

When attempting connection to the specified DLP, this bit indicates that the Base or the DLP is not present or is off-line.

B4 Memory Parity Error

A memory parity error was detected during data transfer.

B2 OP Buffer Full (not used)

There was no room in the buffer to hold the operation initiated on this Channel.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION Rev. B Page 24

3.5.6.1 IOP Portion Of The Channel Result Descriptor (Continued)

B1   Base Port Busy (shared system).

A Poll Test was denied because the Base requested was
busy (being used by another system).

C8   Extended Result Descriptor Present

The DLP presented more than one word of Result
Descriptor information and words other than the first
were non-zero. The remaining words are held by the
IOP.

C4   DLP Address Word Parity Error

A Poll Test was denied because the address presented
to the Distribution Card contained even parity (odd
parity is required).

C2   Unable To Perform OP

This bit is set if the I/O Descriptor OP code is
invalid per Table 3-1. This bit is also set in the
Channel 8 Result Descriptor if the IOP could not
successfully conclude a Cancel operation (Conditional
or Unconditional).

C1   MLI Vertical Parity Error

Data sent to the IOP over the Message Level Interface
contained even parity (odd parity is required).

D8   MLI Longitudinal Parity Error

The longitudinal check word received by the IOP at
the end of the block of data did not compare equal to
the one generated by the IOP.

D4   Result Descriptor Parity Error

The Result Descriptor received from the DLP contained
incorrect vertical and/or longitudinal parity, as
indicated by bit C1 and D8 of the Result Descriptor.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION Rev. B Page 25

3.5.6.1 IOP Portion Of The Channel Result Descriptor (Continued)

D2   A or B Address Error

A word oriented DLP was given a modulo 2 buffer
(modulo 4 is required) and the DLP attempted to Read
or Write one character past the ending address. When
this error terminates an operation the A address may
be greater than the B address.

This bit is also set if B address is not greater than
A address in the I/O descriptor.

D1   C Address Error

The DLP requested additional C address descriptor
information that was not supplied in the I/O
descriptor.

3.5.6.2 DLP Portion Of The Channel Result Descriptor

A8   Not Ready

The unit is in a condition other than power on and
and ready

A4   Descriptor Error

A parity error was detected on the Op-code, variants
or descriptor link

Or an invalid Op-code was given

A2   Vertical Parity Error (system interface)

The vertical parity detected on the system interface
was even

A1   Longitudinal Parity Error (system interface)

The longitudinal parity word from the system did not
compare with the one generated by the DLP

B8-D1

Unique to each DLP and are defined in the relevent
product specifications.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

| 1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 26

3.5.7   IOP Address Memory Handling

For purposes of discussion, assume the A≠address (beginning address) and the B≠address (ending address) in the I/O Descriptor are A≠≠≠A and B≠≠≠B respectively. For either forward and backward operations, the A≠address is loaded into the "A" Scratchpad Memory and the B≠address is loaded into the "B" Scratchpad Memory. The contents of the "A" Scratchpad Memory are incremented during forward operation until all information is transferred, or until equal to the contents of the "B" Scratchpad Memory.

For backward read operation, the contents of the "B" Scratchpad Memory are decremented during operation until all information has been transferred or until equal to the contents of the "A" Scratchpad Memory.

	FORWARD OPERATION		BACKWARD OPERATION	
BEGINNING OF OPERATION	| A≠≠≠A |	"A" SCRATCHPAD	| A≠≠≠A |	"A" SCRATCHPAD
	| B≠≠≠B |	"B" SCRATCHPAD	| B≠≠≠B |	"B" SCRATCHPAD
END OF OPERATION	| B≠≠≠B |	"A" SCRATCHPAD	| A≠≠≠A |	"A" SCRATCHPAD
	| B≠≠≠B |	"B" SCRATCHPAD	| A≠≠≠A |	"B" SCRATCHPAD

In order to obtain the address of the last memory location into which data was transferred during forward operations, a RAD instruction with the variant set to zero is required. For backward read operation the variant must be set to one.

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 27

APPENDIX A   (See Section 3.4)

EBCDIC/ASCII TRANSLATION TABLE

EBC	ASC	GRF	EBC	ASC	GRF	EBC	ASC	GRF	EBC	ASC	GRF	EBC	ASC	GRF
00	00	NULL	27	1B	ESC	4D	28	(	73	BD		99	72	r
01	01	SOH	28	88		4E	2B	+	74	BE		9A	CB	
02	02	STX	29	89		4F	21	!	75	BF		9B	CC	
03	03	ETX	2A	8A		50	26	&	76	C0		9C	CD	
04	9C		2B	8B		51	A9		77	C1		9D	CE	
05	09	HT	2C	8C		52	AA		78	C2		9E	CF	
06	86		2D	05	ENQ	53	AB		79	60	CNTR DOT	9F	D0	
07	7F	DEL	2E	06	ACK	54	AC					A0	D1	
08	97		2F	07	BEL	55	AD		7A	3A	:	A1	7E	tilde
09	8D		30	90		56	AE		7B	23	#	A2	73	s
0A	8E		31	91		57	AF		7C	40	@	A3	74	t
0B	0B	VT	32	16	SYN	58	B0		7D	27	'	A4	75	u
0C	0C	FF	33	93		59	B1		7E	3D	=	A5	76	v
0D	0D	CR	34	94		5A	5D	]	7F	22	"	A6	77	w
0E	0E	SO	35	95		5B	24	$	80	C3		A7	78	x
0F	0F	SI	36	96		5C	2A	*	81	61	a	A8	79	y
10	10	DLE	37	04	EOT	5D	29	)	82	62	b	A9	7A	z
11	11	DC1	38	98		5E	3B	;	83	63	c	AA	D2	
12	12	DC2	39	99		5F	5E	(NEQ)	84	64	d	AB	D3	
13	13	DC3	3A	9A		60	2D	-	85	65	e	AC	D4	
14	9D		3B	9B		61	2F	/	86	66	f	AD	D5	
15	85	NL	3C	14	DC4	62	B2		87	67	g	AE	D6	
16	08	BS	3D	15	NAK	63	B3		88	68	h	AF	D7	
17	87		3E	9E		64	B4		89	69	i	B0	D8	
18	18	CAN	3F	1A	SUB	65	B5		8A	C4		B1	D9	
19	19	EM	40	20	SPACE	66	B6		8B	C5		B2	DA	
1A	92		41	A0		67	B7		8C	C6		B3	DB	
1B	8F		42	A1		68	B8		8D	C7		B4	DC	
1C	1C	FS	43	A2		69	B9		8E	C8		B5	DD	
1D	1D	GS	44	A3		6A	7C			8F	C9		B6	DE	
1E	1E	RS	45	A4		6B	2C	,	90	CA		B7	DF	
1F	1F	US	46	A5		6C	25	%	91	6A	j	B8	E0	
20	80		47	A6		6D	5F	UNDRSCORE	92	6B	k	B9	E1	
21	81		48	A7		6E	3E	>	93	6C	l	BA	E2	
22	82		49	A8		6F	3F	?	94	6D	m	BB	E3	
23	83		4A	5B	[	70	BA		95	6E	n	BC	E4	
24	84		4B	2E	(period)	71	BB		96	6F	o	BD	E5	
25	0A	LF				72	BC		97	70	p	BE	E6	
26	17	ETB	4C	3C	<				98	71	q	BF	E7	

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 28

APPENDIX A   (See Section 3.4)   (Continued)

EBCDIC/ASCII TRANSLATION TABLE   (Continued)

EBC	ASC	GRF	EBC	ASC	GRF	EBC	ASC	GRF	EBC	ASC	GRF	EBC	ASC	GRF
C0	7B	(	CD	EB		DA	EE		E7	58	X	F4	34	4
C1	41	A	CE	EC		DB	EF		E8	59	Y	F5	35	5
C2	42	B	CF	ED		DC	F0		E9	5A	Z	F6	36	6
C3	43	C	D0	7D	(MZ)	DD	F1		EA	F4		F7	37	7
C4	44	D	D1	4A	J	DE	F2		EB	F5		F8	38	8
C5	45	E	D2	4B	K	DF	F3		EC	F6		F9	39	9
C6	46	F	D3	4C	L	E0	5C		ED	F7		FA	FA	
C7	47	G	D4	4D	M	E1	9F		EE	F8		FB	FB	
C8	48	H	D5	4E	N	E2	53	S	EF	F9		FC	FC	
C9	49	I	D6	4F	O	E3	54	T	F0	30	0	FD	FD	
CA	E8		D7	50	P	E4	55	U	F1	31	1	FE	FE	
CB	E9		D8	51	Q	E5	56	V	F2	32	2	FF	FF	
CC	EA		D9	52	R	E6	57	W	F3	33	3			

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 29

APPENDIX B   (See Section 3.4)

ASCII/EBCDIC TRANSLATION TABLE

ASC	EBC	GRF	ASC	EBC	GRF	ASC	EBC	GRF	ASC	EBC	GRF	ASC	EBC	GRF
00	00	NULL	27	7D	'	4D	D4	M	72	99	r	99	39	
01	01	SOH	28	4D	(	4E	D5	N	73	A2	s	9A	3A	
02	02	STX	29	5D	)	4F	D6	O	74	A3	t	9B	3B	
03	03	ETX	2A	5C	*	50	D7	P	75	A4	u	9C	04	
04	37	EOT	2B	4E	+	51	D8	Q	76	A5	v	9D	14	
05	2D	ENQ	2C	6B	,	52	D9	R	77	A6	w	9E	3E	
06	2E	ACK	2D	60	-	53	E2	S	78	A7	x	9F	E1	
07	2F	BEL	2E	4B	.	54	E3	T	79	A8	y	A0	41	
08	16	BS			(period)	55	E4	U	7A	A9	z	A1	42	
09	05	HT	2F	61	/	56	E5	V	7B	C0	(	A2	43	
0A	25	LF	30	F0	0	57	E6	W	7C	6A	|	A3	44	
0B	0B	VT	31	F1	1	58	E7	X	7D	D0	(MZ)	A4	45	
0C	0C	FF	32	F2	2	59	E8	Y	7E	A1	tilde	A5	46	
0D	0D	CR	33	F3	3	5A	E9	Z	7F	07	DEL	A6	47	
0E	0E	SO	34	F4	4	5B	4A	[	80	20		A7	48	
0F	0F	SI	35	F5	5	5C	E0		81	21		A8	49	
10	10	DLE	36	F6	6	5D	5A	]	82	22		A9	51	
11	11	DC1	37	F7	7	5E	5F	(NEQ)	83	23		AA	52	
12	12	DC2	38	F8	8	5F	6D		84	24		AB	53	
13	13	DC3	39	F9	9		UNDRSCORE		85	15	NL	AC	54	
14	3C	DC4	3A	7A	:	60	79	CNTR	o6	06		AD	55	
15	3D	NAK	3B	5E	;			DOT	87	17		AE	56	
16	32	SYN	3C	4C	<	61	81	a	88	28		AF	57	
17	26	ETB	3D	7E	=	62	82	b	89	29		B0	58	
18	18	CAN	3E	6E	>	63	83	c	8A	2A		B1	59	
19	19	EM	3F	6F	?	64	84	d	8B	2B		B2	62	
1A	3F	SUB	40	7C	@	65	85	e	8C	2C		B3	63	
1B	27	ESC	41	C1	A	66	86	f	8D	09		B4	64	
1C	1C	FS	42	C2	B	67	87	g	8E	0A		B5	65	
1D	1D	GS	43	C3	C	68	88	h	8F	1B		B6	66	
1E	1E	RS	44	C4	D	69	89	i	90	30		B7	67	
1F	1F	US	45	C5	E	6A	91	j	91	31		B8	68	
20	40	SPACE	46	C6	F	6B	92	k	92	1A		B9	69	
21	4F	|	47	C7	G	6C	93	l	93	33		BA	70	
22	7F	"	48	C8	H	6D	94	m	94	34		BB	71	
23	7B	#	49	C9	I	6E	95	n	95	35		BC	72	
24	5B	$	4A	D1	J	6F	96	o	96	36		BD	73	
25	6C	%	4B	D2	K	70	97	p	97	08		BE	74	
26	50	&	4C	D3	L	71	98	q	98	38		BF	75	

BURROUGHS CORPORATION
SYSTEMS DEVELOPMENT GROUP
PASADENA PLANT

1989 9368

B4900 I/O SUBSYSTEM

COMPANY CONFIDENTIAL   PRODUCT SPECIFICATION   Rev. B   Page 30

APPENDIX B   (See Section 3.4)   (Continued)

ASCII/EBCDIC TRANSLATION TABLE   (Continued)

ASC	EBC	GRF	ASC	EBC	GRF	ASC	EBC	GRF	ASC	EBC	GRF	ASC	EBC	GRF
C0	76		CD	9C		DA	B2		E7	BF		F4	EA	
C1	77		CE	9D		DB	B3		E8	CA		F5	EB	
C2	78		CF	9E		DC	B4		E9	CB		F6	EC	
C3	80		D0	9F		DD	B5		EA	CC		F7	ED	
C4	8A		D1	A0		DE	B6		EB	CD		F8	EE	
C5	8B		D2	AA		DF	B7		EC	CE		F9	EF	
C6	8C		D3	AB		E0	B8		ED	CF		FA	FA	
C7	8D		D4	AC		E1	B9		EE	DA		FB	FB	
C8	8E		D5	AD		E2	BA		EF	DB		FC	FC	
C9	8F		D6	AE		E3	BB		F0	DC		FD	FD	
CA	90		D7	AF		E4	BC		F1	DD		FE	FE	
CB	9A		D8	B0		E5	BD		F2	DE		FF	FF	
CC	9B		D9	B1		E6	BE		F3	DF				