L9000 ADJUSTMENTS

PRINT HEAD CABLE ADJUSTMENT

With upper carrier assembly G, Fig. IV-20, advanced and print head cable A visually centered with retractor E and channel B there should be .20" to .30" total free play in cable A approximately mid-way between points H and I.

NOTE: With the cable in its normal relaxed position, but bowed toward wall F of the lower carrier assembly, there should be no rubbing of the cable with wall F when the upper carrier assy is advanced or retracted.

To Adjust:

Loosen both screws C on clamp D and with cable A positioned as required, gently pull cable at clamp end snugly against retractor E to remove any excessive slack. Tighten screws C.

Reason:

To avoid tension and prevent rubbing at the flexing portion of the cable.

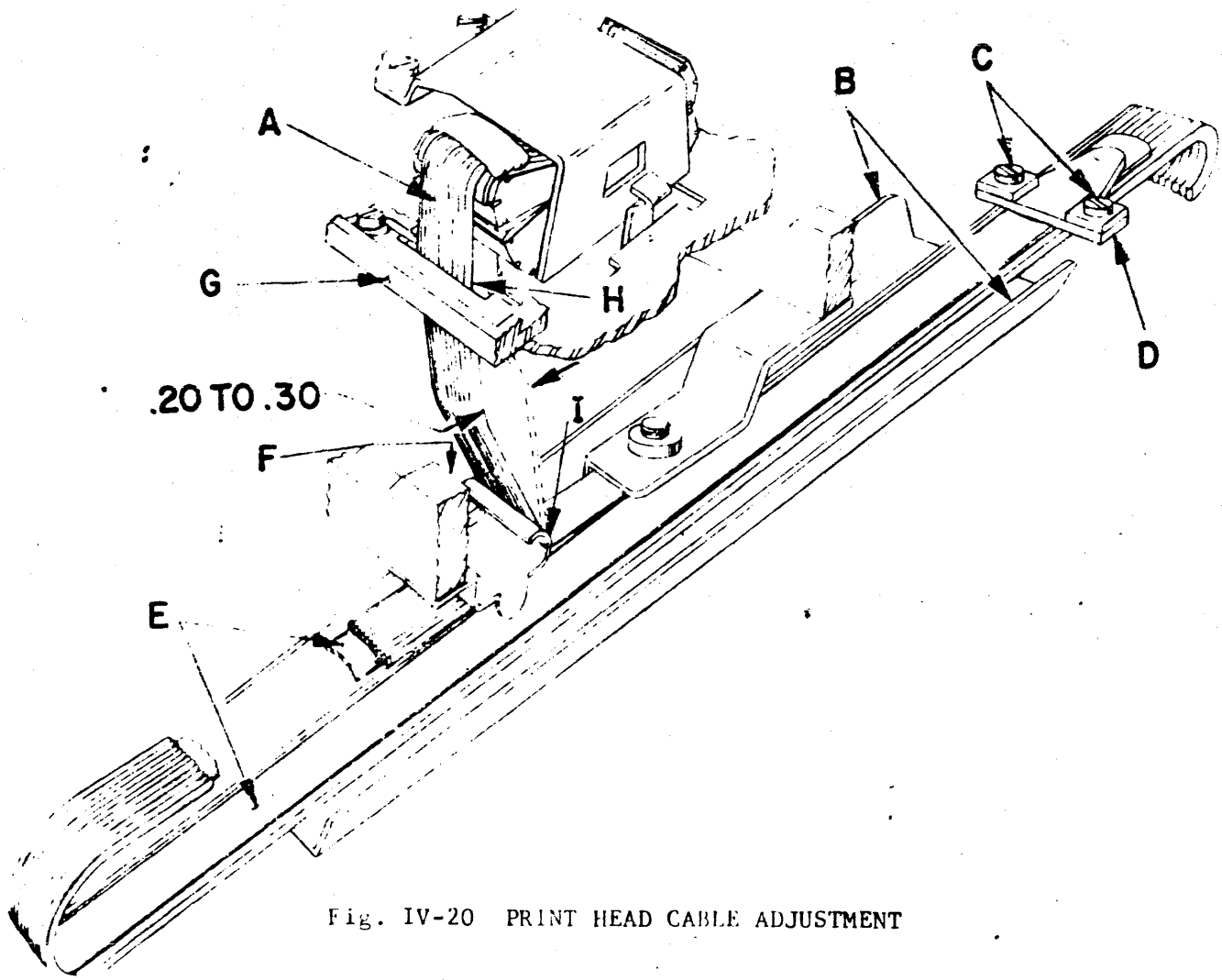


Fig. IV-20 PRINT HEAD CABLE ADJUSTMENT

CARRIER ASSEMBLY

With the carrier assembly positioned on rails C and G of Fig. IV-21:

A) There should be clearance not to exceed .002" between eccentric B and rail C.

B) There should be clearance not to exceed .0015" between link D and high points of rail G.

To Adjust:

A) Loosen screw A, rotate eccentric B as required. Tighten screw A.

B) Turn both screws E as required. Tighten both nuts F.

NOTE: Check for free carrier travel across entire length of rails C and G.

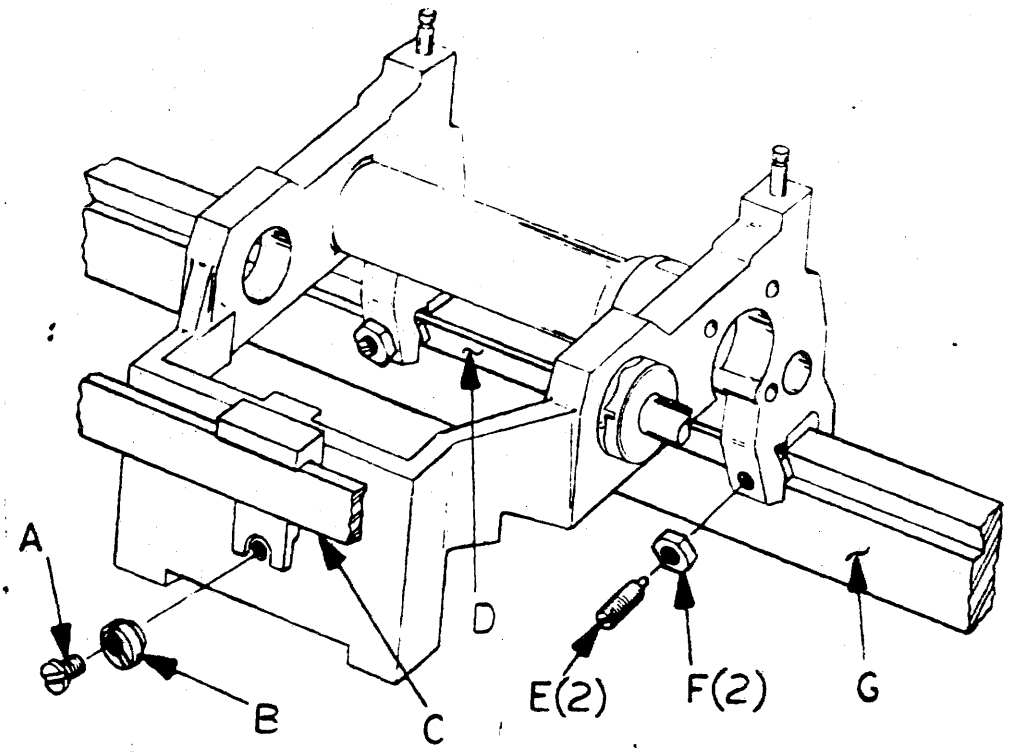


Fig. IV-21 CARRIER ASSEMBLY ADJUSTMENT

PLATEN-PRINT HEAD

With upper carrier assembly H advanced, Fig. IV-22, roller G limiting on cam F, and with the carrier in any print position, there should be:

A. 1.0960" $\pm$ .0015" between top of platen E and top of upper carrier casting H.

B. .016" $\pm$ .001" clearance between platen E and the four sled faces D.

C. .030" $\pm$ .001" clearance between print head nose A and platen E, and the print head nose should be central to ribbon guide posts C within .006".

To Adjust:

The carriage must be securely tied down with screws T.

1. With carrier H in its leftmost position, adjust platen E to its proper height using screw R, then adjust the platen to sled B gap using screw J.

2. With carrier H in its right most position, adjust platen E to its proper height using screw P, then adjust the platen to sled gap using eccentric N. Tighten screws M and O and bring up screw L just enough to support the rear of the carriage.

3. Recheck adjustments. Fine tune, if necessary, to meet the requirements of tests A and B. Tighten locknuts Q.

4. Perform CARRIAGE DRIVE BELT TENSION ADJUSTMENT (60 CPS) as outlined elsewhere in this section.

5. Perform CARRIAGE TIMING ADJUSTMENT (60 CPS) as outlined elsewhere in this section.

6. Loosen nuts I, position print head A as required. Tighten nuts I with 7 to 8 in. - lbs of torque each.

Reason:

To achieve optimum print quality within a limited pin travel, over a .020" maximum document thickness differential.

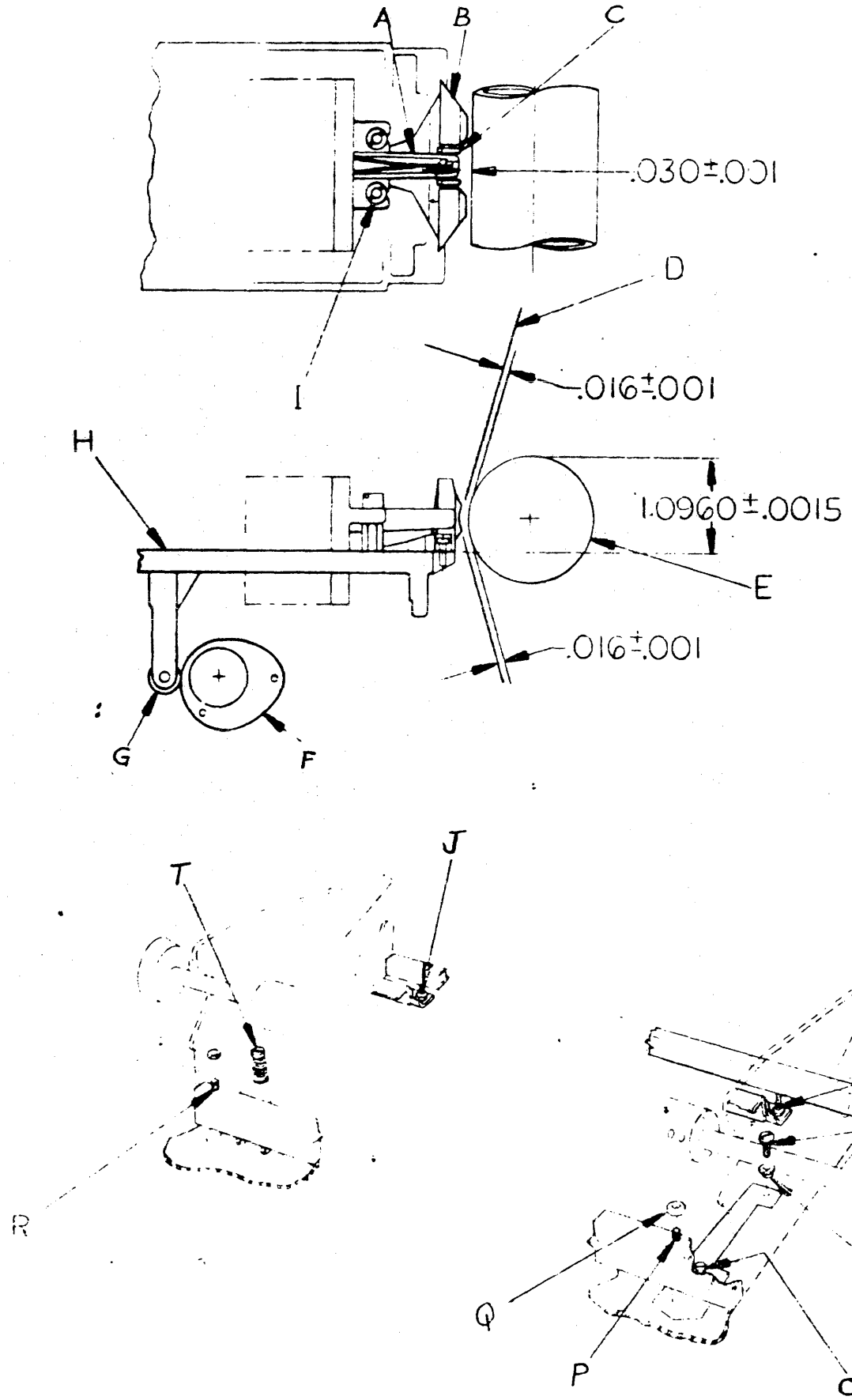


Fig. IV-22 PLATEN-PRINTHEAD ADJUSTMENTS

CARRIAGE DRIVE BELT TENSION (60 CPS)

With a 16 oz. load applied at the center of the long span of belt B, Fig. IV-23, belt B should deflect .2".

To Adjust:

Loosen screws A and position idler C as required. Tighten screws A.

Reason:

To provide proper belt tension.

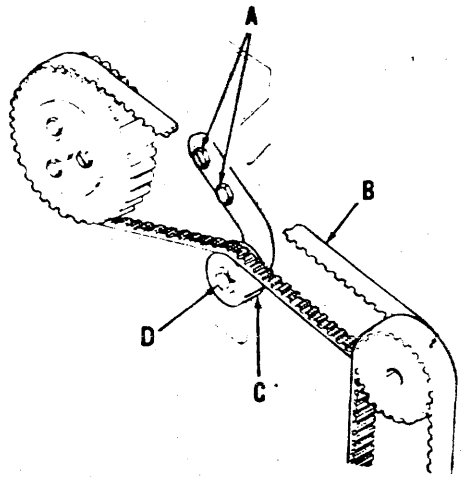


Fig. IV-23 60 CPS CARRIAGE DRIVE BELT TENSION ADJUSTMENT

PRINT SHAFT BELT TENSION (60 CPS)

With a force of 16 oz. applied at the center of the long span of belt C, Fig. IV-24, belt C should be deflected .120" to .140".

To Adjust:

Loosen screws B and locate idler pulley bracket A as required. Tighten screws B.

Reason:

To prevent belt slippage and minimize belt noise and bearing wear.

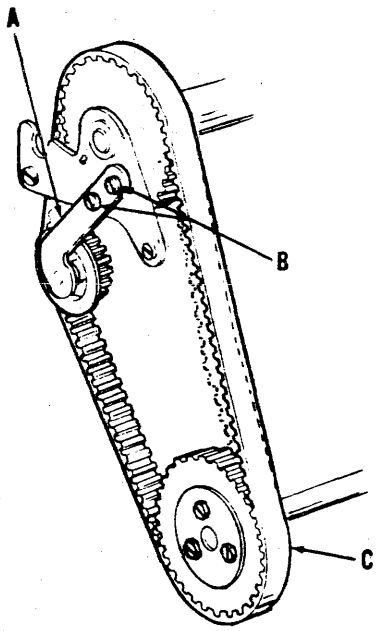


Fig. IV-24 60 CPS PRINT SHAFT BELT TENSION

PULSE GENERATOR BELT TENSION (60 CPS)

There should be 8 oz. tension in belt A, Fig. IV-25.

To Adjust:

Loosen screws B. While applying a 16 oz. $\pm$ 1 oz. load to tab C, tighten screws B.

Reason:

To ensure minimum bearing wear and proper pulse generator operation.

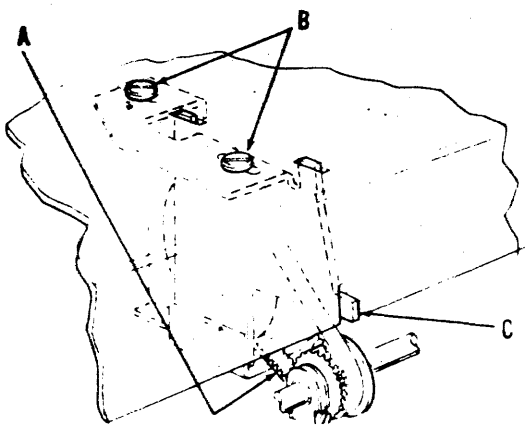


Fig. IV-25 30 CPS PULSE GENERATOR BELT TENSION

PRINT TIMING ADJUSTMENT (60 CPS)

NOTE: The PRINT SHAFT BELT TENSION (60 CPS) and the PULSE GENERATOR BELT TENSION (60 CPS) adjustments must be completed prior to performing this adjustment.

Print shaft F and jack shaft O, Fig. IV-26, should be synchronized with pulse generator disc H.

To Adjust:

Loosen three (3) screws T in pulley S, and one (1) screw R on clamp Q. Insert timing pin N in hole in side frame M. Rotate jackshaft O until timing pin N enters the hole in cam L. Rotate pulley P until the hole in disc H is aligned with the slot in plate G. Insert timing pin J and tighten screw R on clamp Q. Manually trip latch FF, Fig. IV-26, and rotate clutch driver BB counter clockwise until clutch dog CC drops into notch on clutch driver BB. Apply clockwise torque to clutch driver BB to ensure that clutch stop DD is in contact with pawl EE. Tighten screws T in pulley S. Remove all timing pins and restore insert/retract clutch to the latched position.

Rotate jackshaft O to see that belt K tracks in the approximate center of pulley P. If not, again insert timing pins N and J and reposition pulley P along jackshaft O as required. Remove all timing pins.

Reason:

To provide proper printer timing.

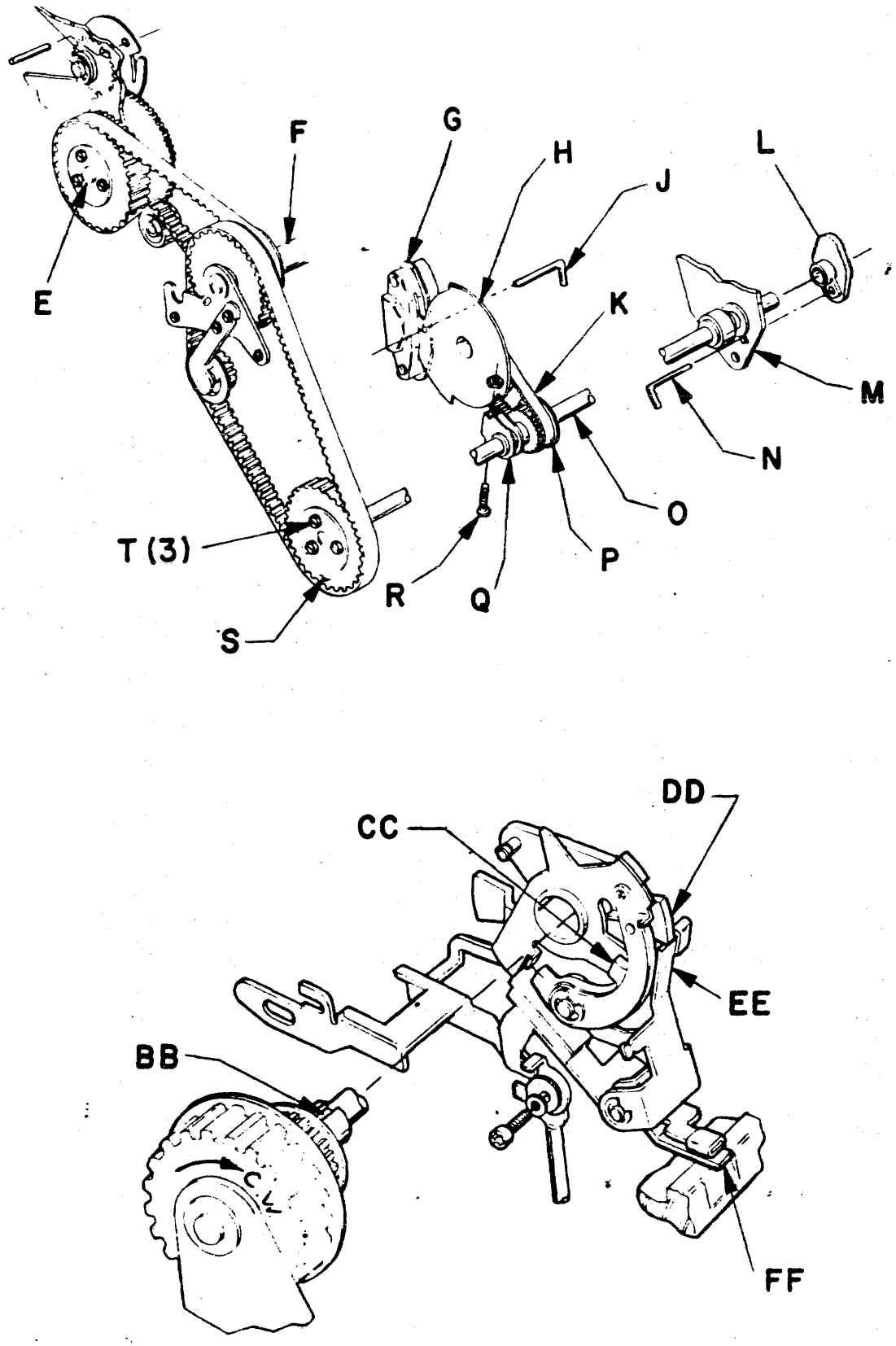


Fig. IV-26 PRINT TIMING ADJUSTMENTS

CARRIAGE TIMING

NOTE: The following adjustments must be completed prior to performing this adjustment:

PLATEN-PRINT HEAD ADJUSTMENT, PRINT SHAFT BELT TENSION ADJUSTMENT, CARRIAGE DRIVE BELT TENSION ADJUSTMENT, PULSE GENERATOR BELT TENSION ADJUSTMENT AND PRINTER TIMING (60 CPS) ADJUSTMENT

The carriage drive jackshaft E, Fig. IV-27 should be synchronized with the print shaft F and jackshaft O.

To Adjust:

Manually turn the carriage drive jackshaft E counter clockwise to actuate the carriage drive to place the forms spacing camshaft AA in the "zero" position. The "zero" position is set by inserting pin A (.093" dia.) through hole Z of side-frame B and through the corresponding hole D in forms spacing clutch release cam C. The axis of the .093" dia. pin A must be square with the surface of side frame B. Loosen (3) screws X in pulley Y to free pulley from drive hub. Rotate jackshaft) until the holes in disc H and plate G are in alignment. Insert timing pin J. Tighten three screws X in pulley Y. Remove timing pin J and timing fixture.

Reason:

To provide proper carriage synchronization.

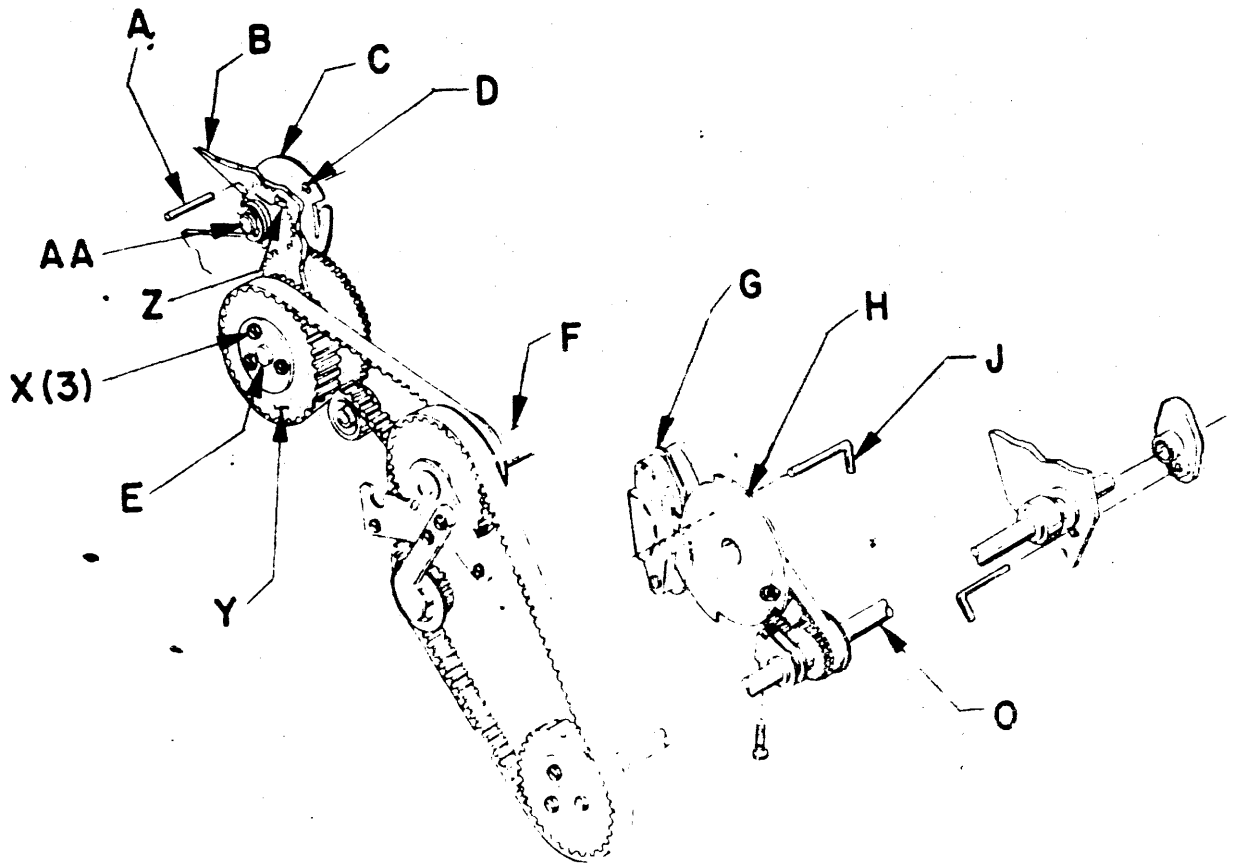


Fig. IV-27 CARRIAGE TIMING ADJUSTMENT

STATE SWITCH TIMING AND LUBRICATION

The State switch cam "D" , Fig. IV-28, should be synchronized with the "insert/retract" clutch.
To Adjust:

Loosen setscrew A in hub B as shown in Fig. IV-28. Ensure that the "insert/retract" clutch is latched with the print head in the inserted position. When the print head is fully inserted, slide C should be in the full down position. This position is set by placing aligning pin E (.093" dia) in the hole in cam D and rotating the cam until pin E enters the slot in slot slide C. While holding pin E perpendicular to the face of cam D, a .005" shim should be inserted between hub B and bearing F. With a force P applied to cam face to push the cam and hub against the shim, tighten set screw A to 9±1 in. lbs torque. Remove pin E.

With slide C still in the full down position, there should be .015± .005" clearance between tab G on slide C and the top of switch H. Bend tab G as required.

Reason:

To provide proper state switch timing and cam hub running clearance.

Lubricate the points indicated in Fig. IV-28 with a small amount of Alvania No. 1 grease (1624 9369).

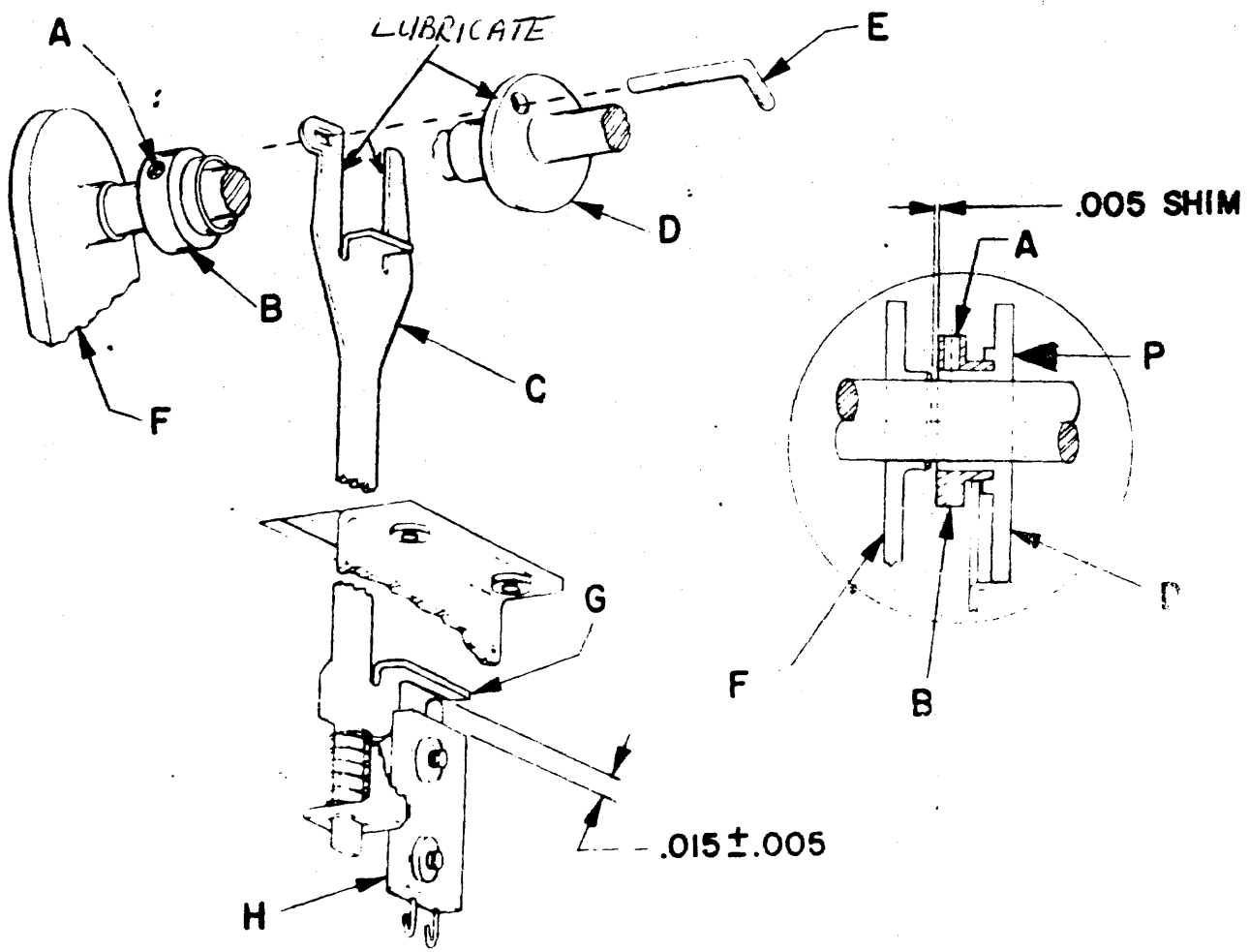


Fig. IV-28 STATE SWITCH TIMING ADJUSTMENT

CARRIER POSITION READOUT (60 CPS)

The Readout disc assembly A, Fig. IV-29, should be centered in the lamp and sensor assembly slot C within .005". Slot C is formed by housing F and printed wiring board assembly G. With the Carrier Position Escape Mechanism latched, any one of the twelve slots in the readout disc should be centered on the LED and photo-transistor axis.

To Adjust:

Loosen screw B. Insert timing pin D (.046" dia.) in timing hole E. Rotate readout disc assembly A (in direction shown by arrow) until the timing pin can enter one of the twelve slots in the disc assembly. Continue rotating readout disc until the slot limits on the timing pin. Holding this contact point, position readout disc assembly A within the lamp and sensor assembly slot C to provide the centered condition shown. (Equal within .005"). Tighten screw B and remove timing pin D.

Reason:

To provide proper readout disc operation.

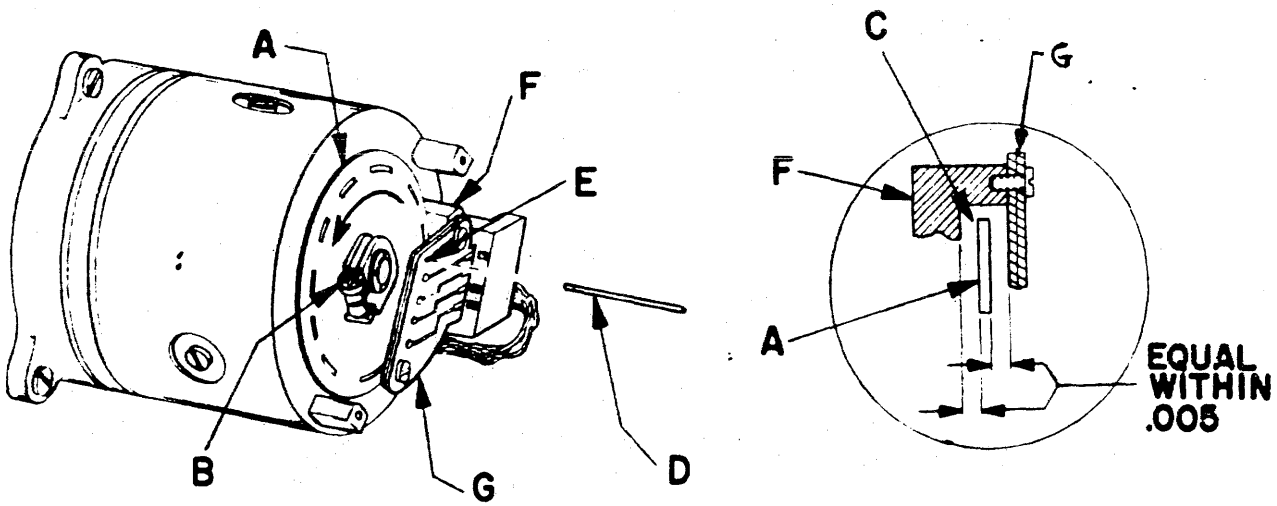


Fig. IV-29 CARRIER POSITION READOUT ADJUSTMENT

RIBBON DRIVE LUBRICATION

Remove the ribbon cartridge. Remove the three screws holding the cover plate over the stepper motor gear assembly and remove plate.

Lubricate gears A and B, Fig. IV-30, with a small amount of Alvania No. 1 grease (1624 9369). Replace cover plate, screws and ribbon.

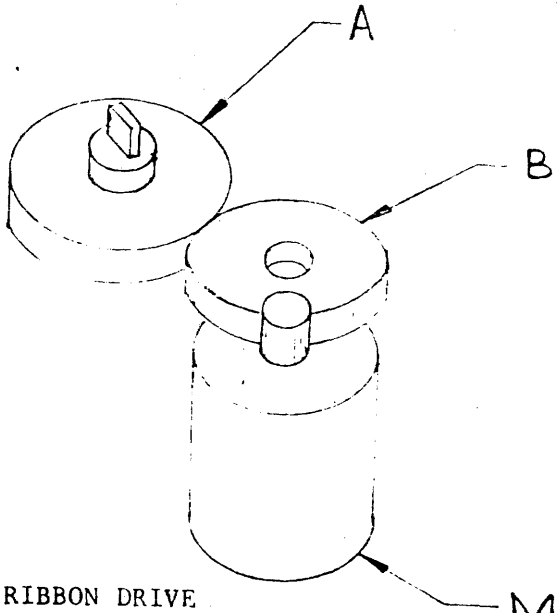


Fig. IV-30 RIBBON DRIVE

L9000 - 60 CHARACTER PER SECOND

The 60 CPS printer used on the L9000 series machines is an enhancement to the existing L8000 product line. The 60 CPS printer currently utilizes a seven pin solenoid activated print head capable of producing five legible copies of printing and one original at a maximum speed of 60 characters per second. Unlike the L8000 there is no red ribbon capability on the L9000's. This section describes the functional detail of the 60 CPS console via the universal front end.

The Printer-Carrier-Forms (PCF) logic of L9000 60 CPS machines is different than that of either the 20 CPS or 30 CPS L8000 style machines. The 60 CPS PCF logic uses a TPU (Terminal Processor Unit) micro processor consisting of a TPU LSIC and 1K of 12-bit Program ROM and associated logic to control the PCF functions of the console.

From a mechanical standpoint the print ball, with its tilt and rotate bands and associated motors or decoder, has been replaced by a seven pin solenoid actuated print head mounted on the carrier.

There is an operational difference between the L9000 60 CPS printer and the L8000 ball printer. The 60 CPS pin printer prints in between detent positions, where as the L8000 ball printer escapes and then prints on the detent position after escapement. Considering the following code sequence: PRTRT, A; PRTLT, B

The ball printer will print the characters BA in contiguous print positions; whereas, the 60 CPS L9000 pin printer, executing the same code sequence, will first print the A as the print head moves to the right. The character B will print right on top of the A as the print head moves to the left.

Firmware takes into consideration the overprint mentioned in the above example to insure this will not occur. Existing L8000 firmware sets are compatible with the L9000 hardware.

Unlike the L8000 ball printer firmware, the L9000 firmware has the capability of printing bi-directionally, i.e., printing is possible in both directions, left and right on the same line. This is accomplished by the L9000 character generator logic which is capable of formatting the correct dot pattern for each character irrespective of the direction of carrier movement.

When the carrier moves to the right, printing of each character occurs serially from left to right. When the carrier moves to the left, printing of each character occurs serially from right to left.

L9000 CARD ASSIGNMENTS.

The card assignments for the 60 CPS machine are shown in Fig. IIC-91. The various machine styles will have different combinations of the console mechanism and controls depending on machine configurations, e.g., 15", 26"with or without MMR. The console interface requirements for the 60 CPS printer are the same and the 60 CPS Printer-Carrier-Forms logic and mechanics are the same for MMR as well as non-MMR machines.

MMR, however, shares the use of the forms control mechanism in its ledger handling operations. There is a certain amount of interaction between the console and MMR operations which firmware takes into consideration to control either one or the other.

The L9000 configuration chart, Fig. IIC-92, illustrates the various combinations of features in each of the L9000 series machine styles including MMR.

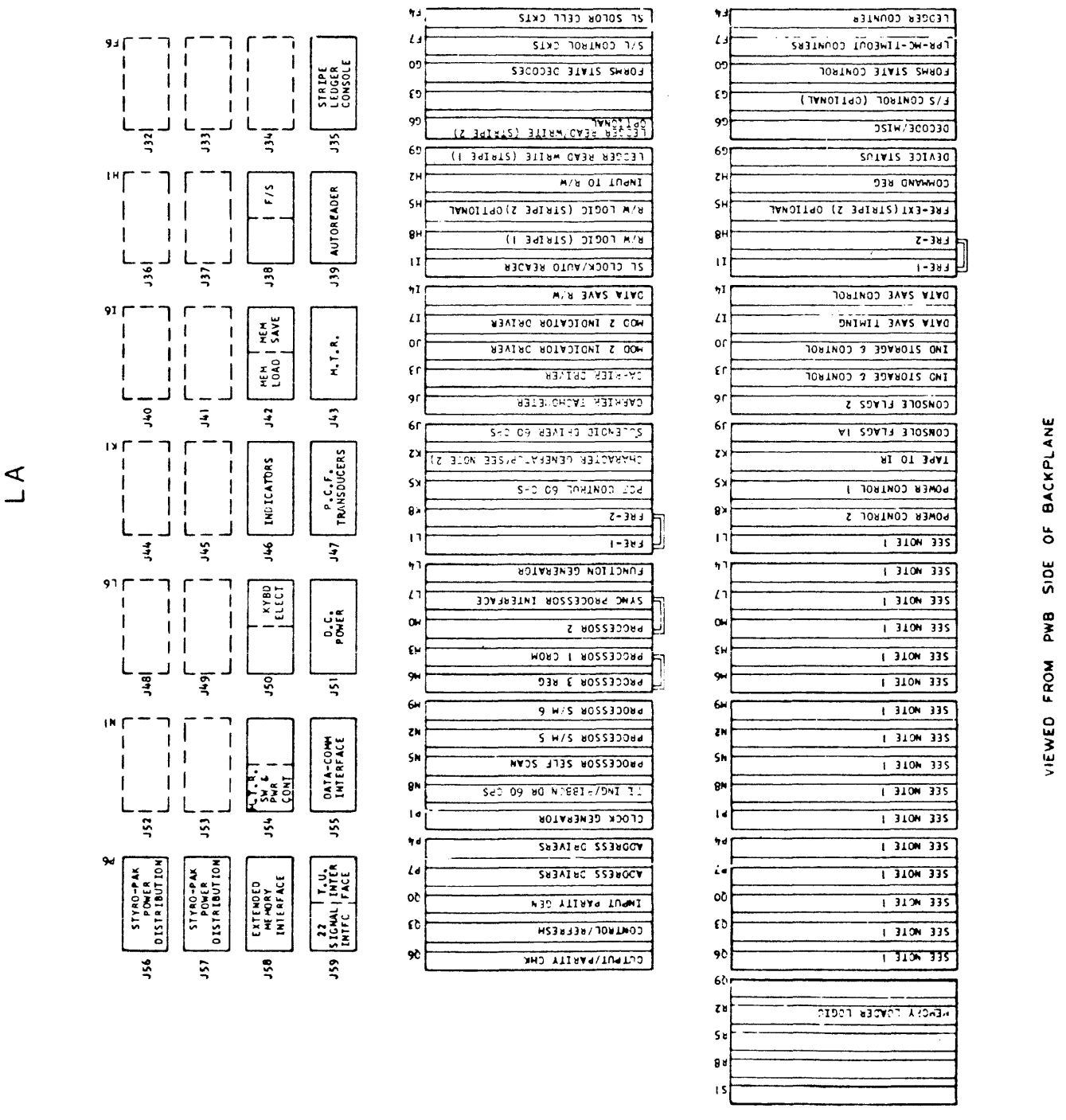


FIG. IIC-91 CARD LOCATION DIGRAM

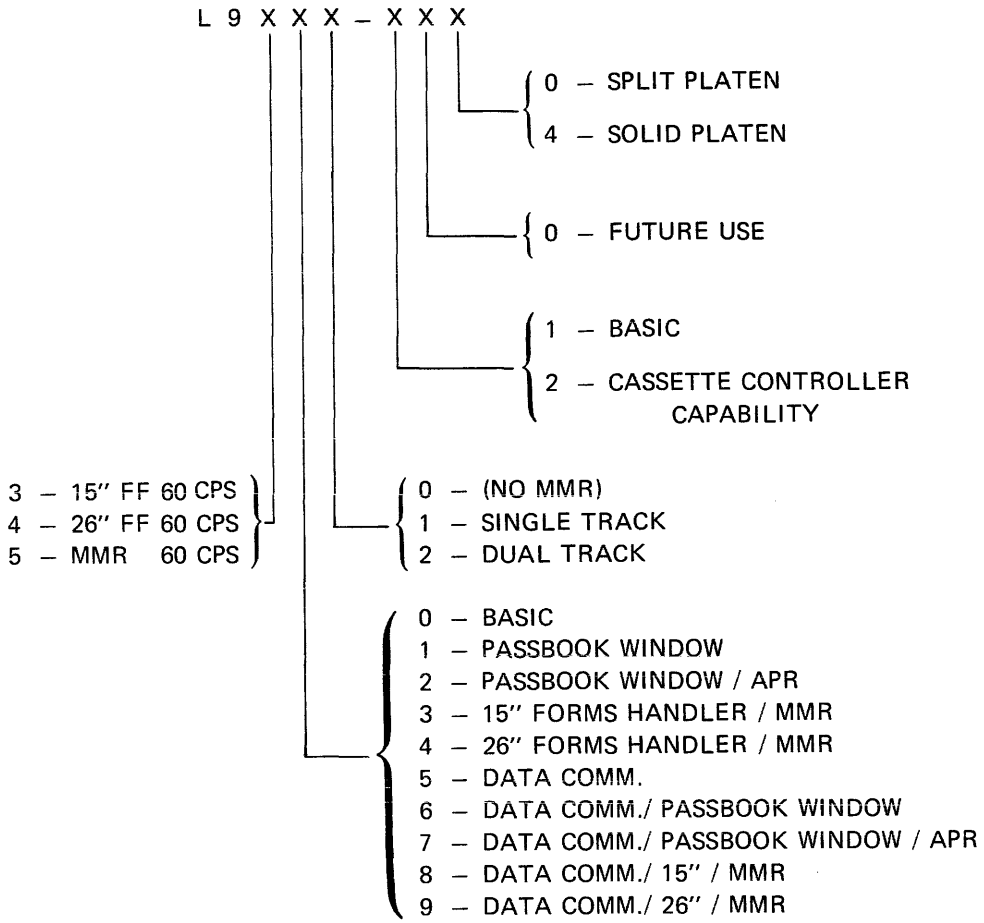


FIG. IIC-92 L9000 STYLE CONFIGURATOR

L9000 (60 CPS) CONSOLE PRINTER CARRIER FORMS.

The L9000 (60 CPS) Console Printer Carrier Forms mechanism, like the L8000 (20 CPS and 30 CPS) console mechanism, is controlled by the basic processor through a set of codes which specifies the control and its parameter, and the characters to be printed. These codes are loaded by the basic processor into an output buffer, where they are retrieved and interpreted by the TPU microprocessor to perform the specified operation. Fig. IIC-93 is a generalized block diagram of the L9000 PCF mechanism.

Printer Carrier Forms Code Set

The code set for the control of the L9000 printer carrier forms consists of 8-bit codes, which can be divided into three groups: control codes, print codes, and no-op codes.

Control Codes — The control codes are used to control printing format, forms handling, carrier positioning, as well as print head retraction and engagement. These control codes appear in ASCII 0 and 1, and are described in Fig. IIC-94.

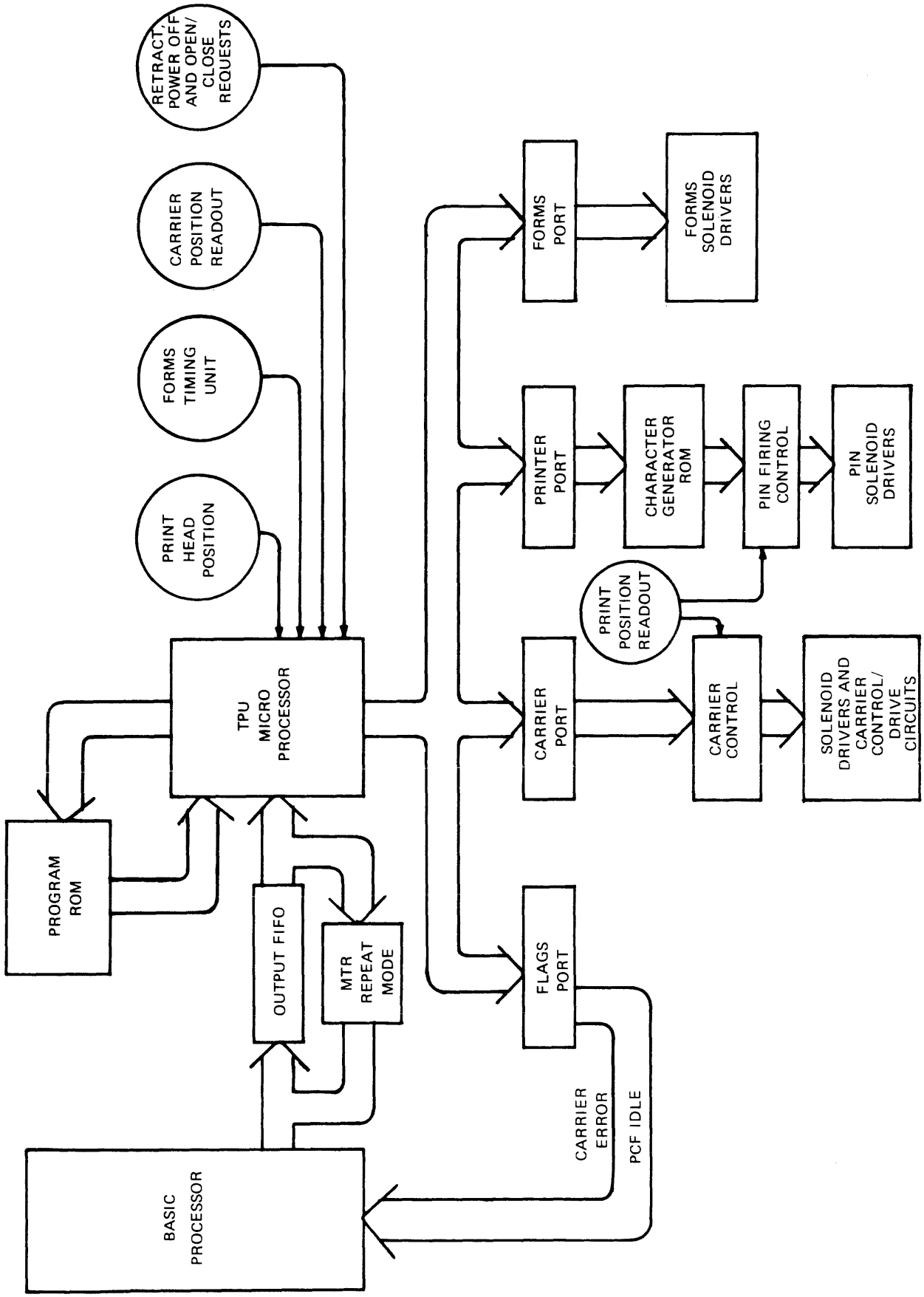


FIG. IIC-93 L9000 SIMPLIFIED BLOCK DIAGRAM

CONTROL CODES CODE	NAME	CONTROL FUNCTION	REMARKS
0-1	PIP	PRINT-IN-PLACE	MODIFY THE NEXT PERIOD OR COMMA TO PRINT IN BETWEEN PRINT POSITIONS.
0-4	PRTLT	PRINT DIRECTION	PRINT TO THE LEFT
0-5	PRTRT		PRINT TO THE RIGHT
0-6	PRTLT		PRINT TO THE LEFT
0-7	PRTRT		PRINT TO THE RIGHT
0-8	OPN	PLATEN OPEN/CLOSE	OPEN PLATEN
0-9	CLOS		CLOSE PLATEN
0-A	O/C		COMPLEMENT PLATEN IF THE PRINTHEAD IS ENGAGED AGAINST THE PLATEN, AN OPEN PLATEN OPERATION IS ALWAYS PRECEDED BY A HARDWARE INITIATED HEAD RETRACT
0-C	SHLT	CARRIER POSITIONING	MOVE CARRIER N POSITIONS TO THE LEFT (SHLT) OR RIGHT (SHRT). N IS THE 8-BIT BINARY NUMBER IN THE OUTPUT FIFO IMMEDIATELY FOLLOWING SHLT OR SHRT. N = 0 NO MOVEMENT N = 1 ONE POSITION ETC. SHLT SETS PRINT DIRECTION TO THE LEFT. SHRT SETS PRINT DIRECTION TO THE RIGHT
0-D	SHRT		
0-E	LNLT	CARRIER POSITIONING	UNASSIGNED CODE NOT USED BY L9000
0-F	LNRT		
1-0	ALARM	ALARM	SOUNDS AUDIBLE ALARM
1-1	POFF	POWER OFF	RETRACTS THE PRINTHEAD (IF IT HAS NOT BEEN RETRACTED) AND WAITS UNTIL P-C-F IS IN THE IDLE STATE, THEN CAUSES MACHINE TO GO ON STANDBY POWER.

CONTROL CODES CODE	NAME	CONTROL FUNCTION	REMARKS
1-2	PMOF	AC MOTOR OFF	RETRACTS THE PRINTHEAD (IF IT HAS NOT BEEN RETRACTED) AND WAITS UNTIL P-C-F IS IN THE IDLE STATE, THEN TURNS THE AC MOTOR OFF.
1-3	ENGG	ENGAGE PRINTHEAD	CLOSES THE PLATEN (IF IT IS OPEN) AND THEN ENGAGE THE PRINTHEAD AGAINST THE PLATEN ROLLER READY FOR PRINTING.
1-4	RTRCT	RETRACT PRINTHEAD	WILL RETRACT THE PRINTHEAD.
1-5	BKSP	HORIZONTAL SPACING	WILL POSITION ONE SPACE OPPOSITE THE DIRECTION PRESENTLY SPECIFIED. DOES NOT CHANGE SPECIFIED DIRECTION, EXCEPT TO ACCOMPLISH BACKSPACE.
1-6	ENUND	ENABLE UNDERLINE	WILL MODIFY SUBSEQUENT PRINT CHARACTERS (INCLUDING SPACES) BY UNDERLINING THEM. THIS IS IN EFFECT UNTIL SUCH TIME A DSUND CODE IS RECEIVED.
1-7	DSUND	DISABLE UNDERLINE	WILL DISABLE UNDERLINING OF PRINT CHARACTERS CAUSED BY THE CODE. HAS NO EFFECT ON THE UNDER-SCORE CODE (5-F)
1-8	ALT	VERTICAL FORMS MOVEMENT	ADVANCE LEFT PLATEN (ALT), ADVANCE RIGHT PLATEN (ART), OR BOTH RIGHT AND LEFT PLATENS (ARL) N LINES. N IS THE 8-BIT BINARY NUMBER IN THE OUTPUT FIFO IMMEDIATELY FOLLOWING THE ADVANCE CODE.
1-9	ART		
1-A	ARL		
1-C	SKHDL	VERTICAL FORMS MOVEMENT	ADVANCE LEFT (SKHDL) OR RIGHT (SKHDR) PLATEN TO TOP OF FORM. IN PRESENT L9000 DESIGN, WILL ADVANCE SPECIFIED PLATEN ONE LINE.
1-D	SKHDR		
1-E	INLT	CARRIER MOVEMENT	MOVES CARRIER TO LEFT (INLT) OR RIGHT (INRT)BUMPER AT ESCAPE VELOCITY (6"/SEC). INLT SETS PRINT DIRECTION TO THE RIGHT. INRT SETS PRINT DIRECTION TO THE LEFT.
1-F	INRT		

FIG. IIC-94 L9000 CONTROL CODES

Print Codes and No-op Codes

The print codes and No-op codes used in the L9000 are shown in Fig. IIC-95 . Unlike the L8000 machines the ASCII print codes do not require any conversion into tilt or rotate coding as the L9000 pin printer contains no tilt or rotate mechanics. Instead, the ASCII print code, under TPU microprocessor control, is fed into a character generator ROM which formats the character as the print head moves across the platen.

The No-Op codes, as shown in Fig. IIC-95 , may be classified into 2 types.

Regular No-ops.

0-0, 0 B, 1-B and all ASCII stick 8 and 9 codes are regular no-ops that time out within 300 microseconds after they are loaded into the output buffer by the basic processor. After this maximum time delay, the TPU microprocessor is ready to service the next code (if any) in the output buffer.

No-ops with Delay.

0-2 and 0-3 are no-ops that provide a delay of 100-150 MS before the TPU microprocessor returns to service the next code (if any) in the output buffer.

The P-C-F idle status bit will indicate "busy" during the delay when any of these no-ops codes are processed by the TPU microprocessor.

P-C-F INITIALIZATION

The P-C-F control program in the TPUmicroprocessor will be initialized to the idle state by any one of the following:

A. Machine full operational power is turned on.
B. The manual reset button is depressed, or a "No memory card" error occurs.
C. A "Reset Port and Clear Buffers" IOCTL command is issued to the console port.

The initialization will turn the AC motor on, retract the printhead, open the carriage, and set the print direction to the right. Any other forms or carrier movement must be initiated programmatically.

Initialization will also clear the carrier velocity error flag.

PRINT-IN-PLACE

All codes, except 2-0, that are preceded by the PIP control code 0-1, will print one of two symbols: PIP Comma, or PIP Period.

Specific code assignments are shown as follows:

CODES	SYMBOLS
2-B, 2-C 2-F, 3-C	COMMA
2-7, 2-E 3-E	PERIOD

B8 →					0	0	0	0	0	0	0	0
B7 →					0	0	0	0	1	1	1	1
B6 →					0	0	1	1	0	0	1	1
B5 →					0	1	0	1	0	1	0	1
BITS B4	B3	B2	B1	ROW↓ COL→	0	1	2	3	4	5	6	7
0	0	0	0	0	NO-OP	ALARM	SPACE	0	@	P	`	p
0	0	0	1	1	PIP	POFF	!	1	A	Q	a	q
0	0	1	0	2	NO-OP[2]	MOF	"	2	B	R	b	r
0	0	1	1	3	NO-OP[2]	ENGG	#	3	C	S	c	s
0	1	0	0	4	PRTLT	RTRCT	$	4	D	T	d	t
0	1	0	1	5	PRTRT	BKSP	%	5	E	U	e	u
0	1	1	0	6	PRTLT	ENUND	&	6	F	V	f	v
0	1	1	1	7	PRTRT	DSUND	'	7	G	W	g	w
1	0	0	0	8	OPN	ALT[1]	(	8	H	X	h	x
1	0	0	1	9	CLOS	ART[1]	)	9	I	Y	i	y
1	0	1	0	10	O/C	ARL[1]	*	:	J	Z	j	z
1	0	1	1	11	NO-OP	NO-OP	+	;	K	[	k	{
1	1	0	0	12	SHLT[1]	SKHDL	,	<	L	\	l	|
1	1	0	1	13	SHRT[1]	SKHDR	-	=	M	]	m	}
1	1	1	0	14	LNLT[1]	INLT	.	>	N	^	n	~
1	1	1	1	15	LNRT[1]	INRT	/	?	O	_	o	BLANK

1 - MUST BE FOLLOWED BY A COUNT
2 - NO-OP WITH DELAY OF 50-100 ms

FIG. IIC-95 L9000 94 CHARACTER INTERNAL CODES

The space code (2-0) will cause a space to be "printed-in-place," instead of a PIP punctuation.

All other codes will be mapped into either a comma or period.

The print-in-place punctuation is printed while the print-head is moving over a detent position (between character positions). This requires that the printhead be in a state of continuous motion both prior to and after the PIP punctuation if printed. The type of carrier motion on either or both sides of the PIP punctuation can be either a carrier positioning sequence, a printable character, a space code, or any combination of these. They must all be in the same direction (right or left) as the PIP printing.

If the PIP control code is issued when the printhead is not in a state of motion, or, if a command is not immediately issued after the PIP punctuation to keep the printhead in a state of continuous motion, certain carrier maneuvers are to be performed by hardware to ensure that the above mentioned requirement is met. Essentially, the printhead has to be backspaced once, before being moved forward to print the PIP punctuation. After the PIP punctuation is printed, the printhead will move one space beyond, before being backspaced to its intended detent position.

Attempts to print the PIP punctuation on either the left-most or right-most detent position will result in a carrier error condition.

UNDERLINE.

The underline function shown in Fig. IIC-96 can be done only by a printhead that has 9 needles. This may be done by one of two ways:

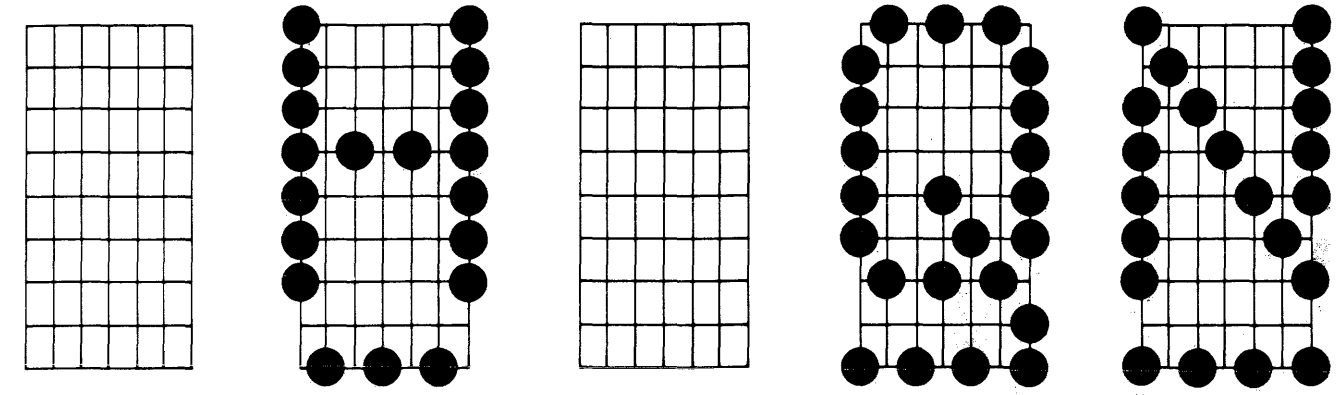
The underscore code (ASCII 5-F) is loaded into the output buffer, and then used to address the character generator ROM to print a 4-dot underscore. Note that this method is not valid for certain non-domestic character generator ROM's whose 5-F code does not address the underscore character.

An enable underline code, ENUND, (1-6) is issued, which will modify subsequent print characters (including the space code, 2-0) by underlining them. This will be in effect for all subsequent print characters until a disable underline code, DSUND (1-7) is issued. It will have no effect on the BKSP code, 1-5.

This mode of underscore operation required only one pass of the printhead motion at the same time as the characters to be underlined, are being printed. This is a 5 dot/character underline, except for the first and last character of a print field.

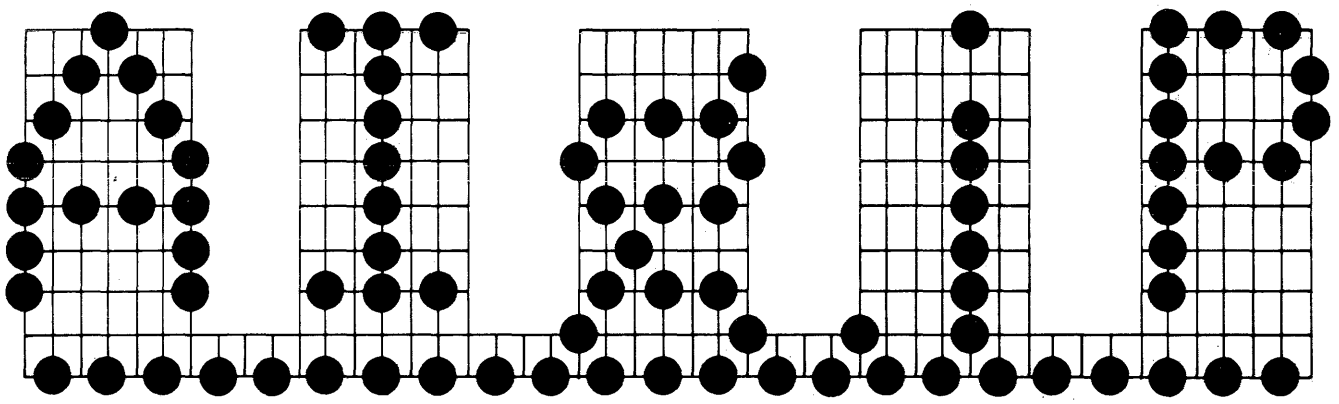
Both types of underline operations should not be attempted simultaneously, because each of their dot constructions does not coincide with the other. Doing so will result in firing the 9th head solenoid in consecutive print positions.

Therefore, firmware should replace the underscore code with a space code in print fields where underline has been enabled by the ENUND code (1-6). In this case, the 4-dot underscore will be replaced by the 5-dot underline, modifying the space character.



SINGLE CHARACTER
WITH UNDERLINE ENABLED

UNDERLINING WITH UNDERSCORE CODE



MULTIPLE CHARACTERS WITH UNDERLINE ENABLED

FIG. IIC-96 UNDERLINE & UNDERSCORE

AC MOTOR ON/OFF CONTROL OPTION.

On-off control of the AC motor is an optional feature, and not part of standard construction.

With this option installed, the AC motor can be turned off programmatically by the motor off control code (MOF). There is also an optional motor off timer, such that if the printer-carrier-forms are idle continuously for approximately 13 seconds, the AC motor will automatically turn off.

The printhead is always retracted by hardware logic before the motor is turned off.

Any code, including no-op codes, will turn the motor back on, except the 0-0, 1-1, or 1-2 codes.

In striped ledger machines, a ledger line advance command to the striped ledger port will also turn the motor back on.

The O/CKY line to the TPU processor, when activated, will also turn the motor on.

CAUTION

After the AC motor is turned off, the TPU processor control program is in its idle loop. If the head engage clutch is activated to trip the printhead state switch, the control program will react by turning on the AC motor to attempt to perform a head retraction. Anyone servicing the mechanical parts in that vicinity must take extra precaution to prevent injury.

PRINTHEAD ENGAGEMENT AND RETRACTION.

The printhead is retracted by the following:

A RTRCT code (1-4).

The printer-carrier-forms are idle for a time period of 1.6 seconds. This time period is field alterable in increments of 400 ms starting at a minimum of 400 ms, up to a maximum of 6 seconds.

The printhead is always retracted prior to AC motor off or power off.

An open platen operation is always preceded by a head retraction to avoid mechanical interference.

The printhead is engaged by the following:

An ENGG code (1-3)

Any code in sticks 2 through 7 (except the space code, 2-0) or any codes in sticks 10 through 15, will close the carriage, and engage the printhead against the platen to print the underline.

INTERFACE WITH MMR.

MMR shares the use of the forms control mechanism in its ledger handling operations. There are certain interaction between the console and MMR operation that firmware has to take into consideration to control one or the other.

FIRMWARE INTERLOCKING OF CONSOLE AND STRIPED LEDGER.

Firmware should not perform any striped ledger operation until the "Console Printer, Forms and Carrier Quiet and Print Buffer Empty" condition is indicated by the console. Once ledger command execution begins, the "Console/SL Interlock Required" flag will be set to 1 and firmware should not perform any print buffer operations that might cause mechanical interference between the console and ledger mechanism until the console/SL interlock required flag is reset to 0.

With the flag "Console/SL Interlock Required" =1, the following console operations can be performed:

a. Power off, audible alarm, all indicators.

b. Carrier positioning.

c. Advance left platen on a split platen console.

d. Print to the left of the left ledger margin.

Note that in case of a console carrier stall or overspeed condition, the flag "Console Printer, Forms and Carrier Quiet and Print Buffer Empty" will be in a state to inhibit SL operations until the stall or overspeed condition is cleared.

CONSOLE OPERATIONS WHEN A MMR JAM CONDITION EXISTS

The console operations that can be performed while a S.L. jam condition is present are:

a. Power Off; Audible Alarm; All Indicators.
b. Open or close platen.
c. Carrier positioning.
d. Advance left platen on a split platen console.
e. Print to the left of the left ledger margin.

STRIPED LEDGER STATUS ON CONSOLE PORT

Two striped ledger status bits will be included as the console port device status:

a. Ledger positioned: This bit is 1 if and only if the ledger positioned transducer at the gripper jaws indicates a ledger is positioned.

b. Console/SL interlock required: This bit, when set, indicates that certain console operations should not be performed programmatically in order to avoid mechanical interference between SL and console mechanisms.

   Those console operations that should not be performed when this bit is 1 are listed below:

   Printing on the ledger.

   Open or close the platen.

   Advance right platen on a split platen machine or advance left platen on a solid platen machine.

   All console operations not listed above may be performed when this bit is 1.

INTERFACE WITH APR.

The APR is part of the console port. It shares the universal front end with the console device control.

The APR Address is IOAR=10000

The processor can control the enabling and inhibiting of the console output FIFO extend line that goes into the TPU microprocessor, by issuing proper IOCTL commands to the APR control logic. APR uses the console port output FIFO in the serial output mode. Consequently, when APR is output active, APR logic can inhibit erroneous operation of the P-C-F control logic by inhibiting the FIFO extend line to the TPU microprocessor. This P-C-F inhibit applies only to P-C-F operations initiated by control codes and print codes passing through the FIFO. Other P-C-F operations that are not issued through the FIFO, can still be performed, such as:

a. Alarm IOCTL

b. Power off IOCTL

c. O/CKY line remains active

d. The timer that controls head retraction and AC motor off remains active.

The keyboard can remain enabled. APR has its own input FIFO and does not inhibit keyboard operation.

FRONT END STATUS BYTE.

The front end status bytes are defined in the L8000 I/O and device control logic. They are listed below, with those unique to the console further defined.

NOTE

Any front end status bit that is set (condition present) will appear as a zero in the AR, whereas device status bits will appear as a one in the AR if the condition is present.

TROUBLE.

This bit will be a one if any of the following conditions occur:

a. Out-of-paper detected.
b. Carrier velocity error.
c. Invalid keyboard entry flag set.

XFF.

This flip-flop will be set when the ready switch is depressed. It is reset via an IOCTL command to the console port. A minimum of at least two milliseconds should be allowed for contact bounce before resetting XFF.

Refer to the L8000 I/O and device control logic for a description of the following bits:

a. Trouble.

b. Input buffer extend (at least one byte in the input FIFO).

c. Output buffer empty.

d. Output buffer almost empty.

e. Input buffer full.

f. Input buffer almost full.

CONSOLE FLAGS.

Flags and status bits for the console device control consist of three bytes of device status as defined in the L8000 I/O logic. These status bytes are read when addressing the console device control, address 00000. The first device status byte contains console device control general status bits. The second device status byte contains TC1700 window machine flags. The third device status byte contains processor-oriented flags. The device status bytes are defined below.

If a particular option that is the source of a status bit is not present in a machine, then that bit will always be 0 (except in the DC140, PCF IDLE=1.)

Figs. IIC-97, 98 and 99 list the device status bits.

BIT	B8	B7	B6	B5	B4	B3	B2	B1	
AR	ZONE				NUMERIC				
	Z8F	Z4F	Z2	Z1F	N8F	N4F	N2F	N1F	
	CVER	OPD	0	0	PCFI	IKE	LP	C/SLI	DEVICE STATUS BYTE 1

B1=C/SLI CONSOLE/STRIPED LEDGER INTERLOCK REQUIRED
B2=LP LEDGER POSITIONED
B3=IKE INVALID KEYBOARD ENTRY
B4=PCFI PRINTER-CARRIER-FORMS IDLE
B5=0
B6=0
B7=OPD OUT-OF-PAPER DETECTED
B8=CVER CARRIER VELOCITY ERROR

FIG. IIC-97 DEVICE STATUS BYTE 1 BIT ASSIGNMENTS

BIT	B8	B7	B6	B5	B4	B3	B2	B1	
AR		ZONE				NUMERIC			
	SVOL	TBL	TAL	0	0	PBLL	PSOF	PBFL	DEVICE STATUS BYTE 2

B1=PBFL PASSBOOK FIRST LINE
B2=PSOF PASSBOOK SPACE OVER FOLD
B3=PBLL PASSBOOK LAST LINE
B4=NOT USED ALWAYS ZERO
B5=NOT USED ALWAYS ZERO
B6=TAL TELLER A LOCK
B7=TBL TELLER B LOCK
B8=SVOL SUPERVISORY OVERRIDE LOCK

FIG. IIC-98 DEVICE STATUS BYTE 2 BIT ASSIGNMENTS
WINDOW MACHINE FLAGS

BIT	B8	B7	B6	B5	B4	B3	B2	B1	
AR		ZONE				NUMERIC			
	LLVF	Ø	Ø	BTEN	0	MRPE	NMC	BTON	DEVICE STATUS BYTE 3

B1=BTON BATTERY ON
B2=NMC NO MEMORY CARD
B3=MRPE MEMORY READ PARITY ERROR
B4=0
B5=BTEN BATTERY ENABLED
B6=NOT USED
B7=NOT USED
B8=LLVF LOW LINE VOLTAGE FLAG

FIG. IIC-99 DEVICE STATUS BYTE 3 BIT ASSIGNMENTS

DEVICE STATUS BYTE 1.

CONSOLE/STRIPED LEDGER INTERLOCK REQUIRED (B1 IN AR)

This bit, when set, indicates that certain console operations should not be performed programmatically in order to avoid mechanical interference between SL and console mechanisms. Those console operations that should not be performed when this bit is 1 are:

a. Printing on the ledger.

b. Open or close platen.

c. Advance right platen on a split platen machine or advance left platen on a solid platen machine.

All other console operations may be performed when this bit is 1.

LEDGER POSITIONED (B2 IN AR):

This bit is 1 if and only if the ledger position transducer at the gripper jaws indicates a ledger is present.

INVALID KEYBOARD ENTRY (B3 IN AR):

This flag is a 1 if a keyboard depression has occurred while the keyboard was inhibited. It can also be set by an IOCTL command from the processor. It can be reset by an IOCTL command from the processor or by initializing the console port.

FIG. IIC-100 defines the IOCTL commands for setting and resetting this flag, as well as other console device IOCTL commands.

PRINTER-CARRIER-FORMS IDLE (B4 IN AR)

This bit is set when the console printer, carrier, and forms are idle and the console output buffer is empty. The console output buffer will appear empty to the TPU microprocessor if the command to inhibit console output buffer is issued prior to any APR operations. This signal is also hard-wired to the MMR.

Note that if the console output buffer is not empty, the PCF IDLE bit will be 0. Therefore, any no-op, PIP, PRTLT, PRTRT, ENUND, or DSUND codes, that are sent to the output buffer will cause the PCF IDLE bit to be 0, until the TPU microprocessor can retrieve and finish processing them.

OUT-OF-PAPER (B7 IN AR)

This bit is a direct function of the out-of-paper detector. If set (1), it indicates the out-of-paper detector is active (no paper). If reset (0), then the out-of-paper detector is not active (paper present). No programmatic set/reset of this bit is available.

CARRIER VELOCITY ERROR (B8 IN AR)

This bit is set under any of the following conditions:

Carrier overspeed is detected by hardware when the hold solenoid is about to be de-energized.

Carrier underspeed

The printhead cannot be engaged due to a malfunction, when printing is initiated.

The carrier velocity error bit can be reset by initializing the consol port. If the carrier velocity error bit is set, the PCF IDLE bit will be 0, no further printer-carrier-forms operations can occur, except sounding the audible alarm via an IOCTL command to the Universal Front End.

BIT	B8	B7	B6	B5	B4	B3	B2	B1			DC140
	ZONE 8F	ZONE 4F	ZONE 2F	ZONE 1F	NUMERIC 8F	NUMERIC 4F	NUMERIC 2F	NUMERIC 1F	HEX		
	0	0	0	0	1	0	0	1	0-9	RESET XFF (READY SWITCH)	Y
	0	0	0	1	1	1	0	1	1-D	SET OUTBUFF INHIBIT FF	N
	0	0	0	1	0	1	0	1	1-5	RESET OUTBUFF INHIBIT FF	N
	0	0	1	1	0	0	0	1	3-1	IOC31 (AUDIBLE ALARM BYPASS)	N
	0	0	1	1	1	1	0	1	3-D	SET GEN FF (POWER OFF BYPASS)	Y
	0	0	0	1	0	0	0	1	1-1	RESET OUTBUFF CALL FF	N
	0	0	0	1	1	0	0	1	1-9	SET OUTBUFF CALL FF	N
	0	0	1	1	1	1	0	0	3-C	SELECT INDICATOR GROUP "S"	Y
	0	1	0	0	1	1	0	0	4-C	SELECT INDICATOR GROUP "A"	Y
	0	1	0	1	1	1	0	0	5-C	SELECT INDICATOR GROUP "B"	N
	0	1	1	0	1	1	0	0	6-C	SELECT INDICATOR GROUP "C"	N
	0	1	1	1	1	1	0	0	7-C	SELECT INDICATOR GROUP "D"	Y
	0	0	0	0	0	0	1	1	0-3	KEYBOARD ENABLE	Y
	0	0	1	0	0	0	1	1	2-3	LOADER ENABLE	Y
	0	1	0	0	0	0	1	1	4-3	SET INVALID KEYBOARD ENTRY FF	N
	0	1	1	0	0	0	1	1	6-3	RESET INVALID KYBD ENTRY FF	N
	1	0	0	0	0	0	1	1	8-3	SET BATTERY ENABLE FF	Y
	1	0	1	0	0	0	1	1	A-3	SET KEYBOARD INHIBIT	N

(SEVERAL OF THESE COMMANDS ARE DEFINED IN THE UNIVERSAL FRONT END SPECIFICATION, AS ARE ADDITIONAL FRONT END-SENSITIVE CODES.)

FIG. IIC-100 L8000 CONSOLE DEVICE CONTROL IOCTL COMMANDS

DEVICE STATUS BYTE 2.

This byte is the second device status byte and is made available after reading the first device status byte. It consists of the window machine flags for the TC1700. If the window machine option is not installed, all bits will be zero. The bit designations are listed below:

a. Passbook first line (B1 in AR).

b. Passbook space over fold (B2 in AR).

c. Passbook last line (B3 in AR).

d. Teller A lock (B6 in AR).

e. Teller B lock (B7 in AR).

f. Supervisory override lock (B8 in AR).

DEVICE STATUS BYTE 3.

This status byte is reserved for processor-oriented flags. It is made available after reading device status byte 2.

In the standby power or battery mode the console will have all power removed except for the device status byte 3 flags. To make status byte 3 available in the battery mode, the processor must set IOAR to 0 and do three read microinstructions, disregarding the data loaded into the AR as a result of these three read's. The next slow read command (must be a slow read, 1-0, because TR will be high - fast read will not load AR) will load device status byte 3 into the AR. Neither the "No Memory Card" nor "Parity Error" flag will be reset by reading device status byte 3 when in the battery mode. If set, these two flags will remain set (battery mode only).

BATTERY ON FLAG (B1 IN AR).

This flag is reset by hardware when power is turned on from a full power off condition. The flag will be set if an under-voltage condition occurs such that it may be necessary to perform a memory dump operation.

Firmware can cause the machine to go to either full power off or standby power when this flag is set. If memory dump is not addressed (DSAF=0) a modified IOCTL instruction, 971F, will cause a transfer to the standby power mode. The same modified IOCTL instruction will cause a full power off condition if memory dump is addressed.

NO MEMORY CARD FLAG (B2 IN AR).

(Normal operation: Memory dump is not addressed: DSAF=0.)

This flag is reset by hardware when power is turned on from a full power off condition. It is set if an attempt is made to access (read or write) an area of memory for which there is no printed circuit board present. When "No Memory Card" is detected, the machine is initialized to FFFF.

"No Memory Card" flag is reset when the processor does a read of device status byte 3. (INTIO will not reset this flag.)

Refer to "L8000 Firmware Control of Data Save Hardware" for no memory card errors when data save is addressed.

MEMORY READ PARITY ERROR FLAG (B3 IN AR).

The memory control circuits generate odd parity when data is written into the R/W memory. The parity bit is a ninth bit associated with each 8-bit memory location and is not accessible to the processor logic. The memory control circuits check parity when a R/W memory location is read. If a memory parity error occurs, the "Memory Read Parity Error" flag will be set.

There are two conditions that will cause the memory parity error flag to be set. They are:

a. A parity error is detected when a valid R/W memory location is read and a ligitimate parity error occurs.

b. A parity error is detected when reading a R/W memory location that is physically not present, although the printed circuit board that contains a position for that location is present. (e.g., on a 2048-byte R/W PCB, only 1024 bytes are assembled and an attempt is made to read a location in the missing 1024 bytes.)

The "Memory Read Parity Error" flag will be reset when power is turned on from a full power off condition. It will also be reset when the processor does a read of device status byte 3. (INTIO will not reset this flag.)

The Memory Read Parity Error flag can be interrogated by firmware when data save is not addressed, by a 3F (SKIP) instruction, as follows:

```
                                                    .
                                                    .
                                                    .
                                                (DSAF=0)
                                                    .
                                                    .
                                                    .
PARITY ERROR FLAG=1                              3-F    TXRC
                                                 D-N    BRU
                                                 P-Q    PARITY ERROR FLAG=0
                                                 Z-N
```

If the parity error flag is set, it can only be reset by firmware by reading device status byte 3. The skip micro does not reset it.

If memory dump is addressed (DSAF=1), the 3F skip microinstruction will test the no memory card flag.

BATTERY ENABLE FLAG (B5 in AR).

This flag is reset by hardware when power is turned on from a full power off condition. It can only be set by programmatically issuing the appropriate IOCTL command to the console port 0. It should be set by the processor following a successful memory load, after which any DC undervoltage condition will cause hardware to switch in the battery. If "Battery Enable" is not set, a DC undervoltage condition will cause the machine to go to a full power off state. Fig. IIC-100 defines the IOCTL to set this flag.

LOW LINE VOLTAGE FLAG (B8 IN AR).

This flag is sampled by firmware when the power control circuits detect a D.C. undervoltage condition and initialize the machine. As a result of sampling the flag, firmware decides if a memory dump operation is required, or if the machine should go to the standby power mode.

CHARACTER GENERATOR ROMS.

There is provision made in the L9000 character generator hardware to accomodate two character generator ROM's: One that is addressed by print codes in ASCII columns 2 through 7, and another one that is addressed by print codes in ASCII columns 10 through 15.

There is another hardware configuration available wherein bit 8 of the print codes will be ignored, so that codes in ASCII columns 10 through 15 will be mapped into those in columns 2 through 7, thereby controlling printing from only one character generator ROM.

There is no hardware provision, however, to map ASCII columns 6 or 7 codes onto columns 4 or 5. These codes will directly address the character generator, and whatever is defined in the character generator ROM at that location will be printed. Note that this implies that, if such mapping is desired, a printer code translation table must be employed by firmware.

CONSOLE MTR FUNCTIONS.

Console MTR functions for the L9000 are identical to those defined for the L8/TC.

L9000 LOGIC CIRCUITS

The following describes the basic logic elements as well as the packaging used for each logic element. The basic logic element is the NAND gate. There are also a number of unique logic elements used to control specific PCF functions. These include Flip-flops, DMV's, binary counter and shift register devices as well as some unique LSIC and ROM chips. The individual devices are explained in detail here to provide a better understanding of how each device operates.

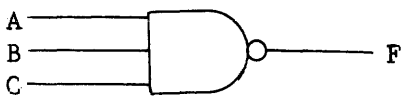
L9000 LOGIC LEVELS

The L9000 PCF logic deals primarily with two state devices. The two physical states on each signal line can be referred to as the high state and low state. Generally, the high state will be the active state and the low state will be the inactive state. There are exceptions when the low state will be the active state.

The L9000 PCF logic uses both positive logic and Negative MOS logic. The TPU LSIC and the two Micro Program ROMs use Negative MOS logic levels. It is only necessary to think of these outputs as active low. Reference to input or output signals for the negative active devices will be referred to as big or low which indicates that the voltage level is either high or low.

NAND GATE

The symbol shown in Fig. IIC-101 represents one version of the NAND function. From the accompanying truth table it can be seen that any low input clamps the output high. The output goes low, its active condition, only when all inputs are high.

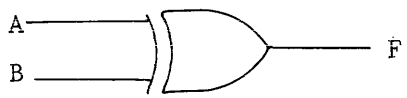


INPUT			OUTPUT
A	B	C	F
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

FIG. IIC-101 NAND GATE

2 INPUT EXCLUSIVE OR

The symbol shown in Fig. IIC-102 represents the EXCLUSIVE OR function. As seen in the accompanying truth table the output is high, active condition, only when the two inputs are dissimilar. If both inputs are high or low at the same time, the output of the EXCLUSIVE OR will be low.



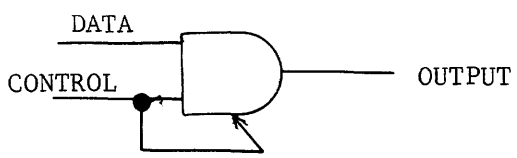
INPUT		
A	B	F=
L	L	L
L	H	H
H	L	H
H	H	L

A (H) and B (L) or B (H) and A (L)

FIG. IIC-102 EXCLUSIVE OR

TRI-STATE BUFFER

Fig. IIC-103 indicates the symbol for a TRI-STATE BUFFER. As shown in the truth table, three states



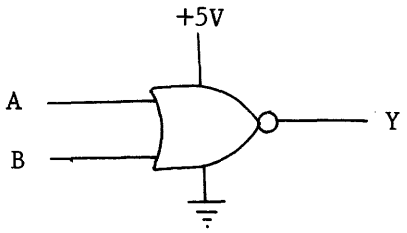
DATA	CONTROL	OUTPUT
H	H	H
L	H	L
L	L	HIGH IMPEDANCE
H	L	HIGH IMPEDANCE

FIG. IIC-103 TRI-STATE BUFFER

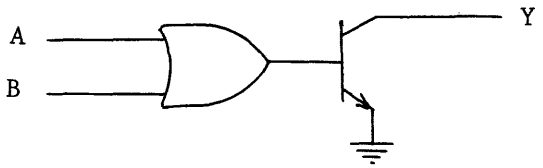
are possible. The state of the data input, either high or low, will be reflected on the output whenever the control input is high. With the control input low, and, irrespective of the state of the data input, the output line will appear as a high impedance to the next input device. This high impedance is in the megohms and is effectively an open to subsequent logic.

POSITIVE NOR PERIPHERAL DRIVER

FIG.IIC-104 indicates the symbol for a POSITIVE NOR PERIPHERAL DRIVER. It is a NOR gate with a driver transistor attached. The Emitter is grounded and the collector is open receiving collector voltage from the load to which it is attached. The POSITIVE NOR PERIPHERAL DRIVER provides fast and positive switching.

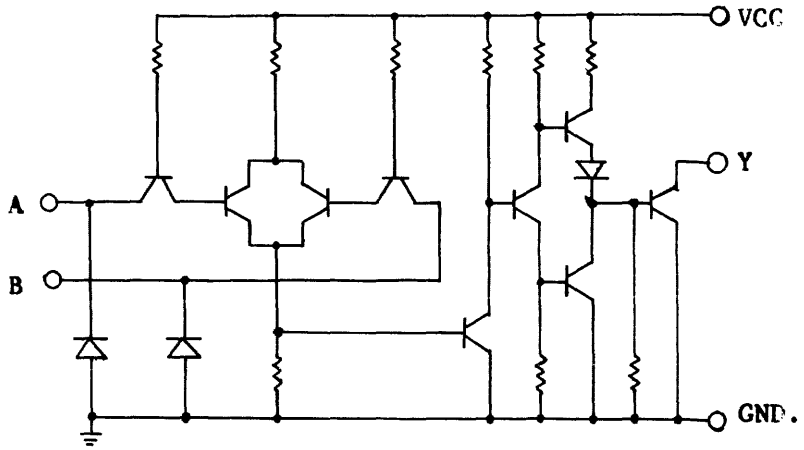


SYMBOL



EQUIVALENT CIRCUIT

EQUIVALENT CIRCUIT (Each Driver)



TRUTH TABLE

A	B	Y	
L	L	H	(OFF STATE)
L	H	L	(ON STATE)
H	L	L	(ON STATE)
H	H	L	(ON STATE)

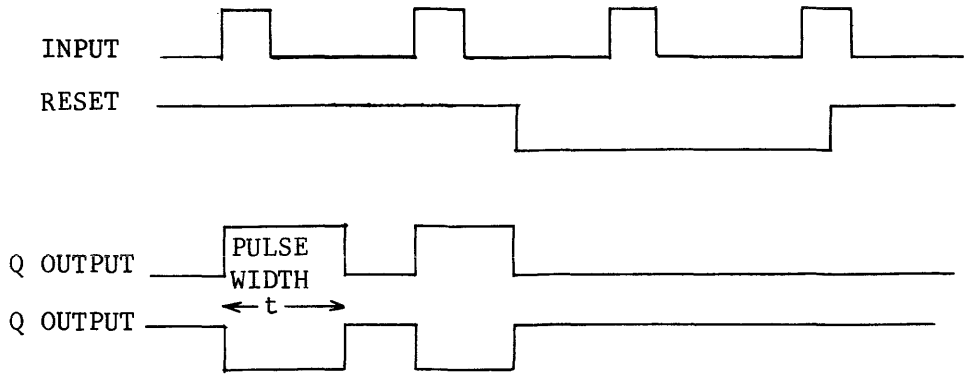
H= HIGH LEVEL LOW = LOW LEVEL

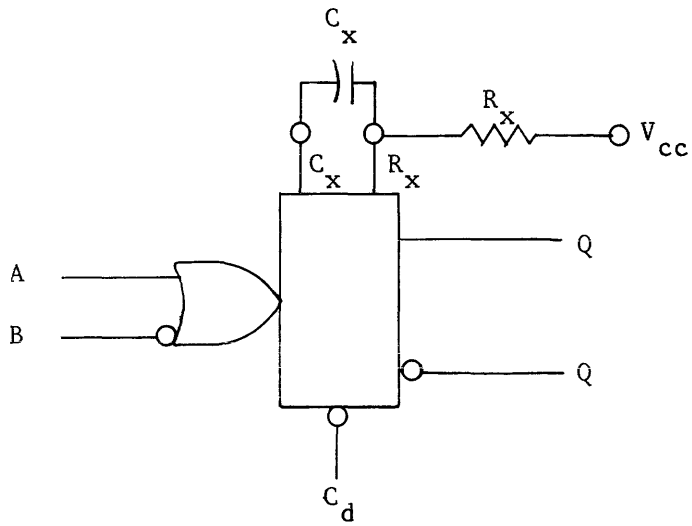
FIG. IIC-104 DUAL POSITIVE-NOR PERIPHERAL DRIVER

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

The multivibrator shown in Fig.IIC-105 provides an output pulse whose duration and accuracy is a function of the externally mounted timing components (capacitor Cx and resistor Rx).

Reset Operation - An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.





(1/2 OF DIVICE SHOWN)

PIN NO'S			OPERATION
B	A	Cd	
H → L	L	H	TRIGGER
H	L → H	H	TRIGGER
X	X	L	RESET

H = HIGH VOLTAGE LEVEL

L = LOW VOLTAGE LEVEL

H → L = HIGH TO LOW VOLTAGE LEVEL TRANSITION.

L → H = LOW TO HIGH VOLTAGE LEVEL TRANSITION.

X = DO NOT CARE

FIG. IIC-105 LOGIC DIAGRAM AND TRIGGERING TRUTH TABLE

ONE OF TEN DECODER

The ONE OF TEN DECODER IC is shown in Fig. IIC-106. The device accepts four inputs (A_0 - A_3) and provides ten mutually exclusive outputs. This device is used to generate the port addresses by decoding the 4 input addresses (XAD0 - XAD3). The active output of the decoder is a low logic level as shown in the truth table.

	A_0	A_1	A_2	A_3	0/	1/	2/	3/	4/	5/	6/	7/	8/	9/
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	H	L	L	L	H	L	H	H	H	H	H	H	H	H
2	L	H	L	L	H	H	L	H	H	H	H	H	H	H
3	H	H	L	L	H	H	H	L	H	H	H	H	H	H
4	L	L	H	L	H	H	H	H	L	H	H	H	H	H
5	H	L	H	L	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	H	H	H	L	H	H	H	H	H	H	H	L	H	H
8	L	L	L	H	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
10	L	H	L	H	H	H	H	H	H	H	H	H	H	H
11	H	H	L	H	H	H	H	H	H	H	H	H	H	H
12	L	L	H	H	H	H	H	H	H	H	H	H	H	H
13	H	L	H	H	H	H	H	H	H	H	H	H	H	H
14	L	H	H	H	H	H	H	H	H	H	H	H	H	H
15	H	H	H	H	H	H	H	H	H	H	H	H	H	H

1 Address Input A_2
2 Address Input A_3
3 Output 5/
4 Output 6/
5 Output 7/
6 Output 8/
7 Output 9/
8 Ground
9 Output 4/
10 Output 3/
11 Output 2/
12 Output 1/
13 Output 0/
14 Address Input A_1
15 Address Input A_0

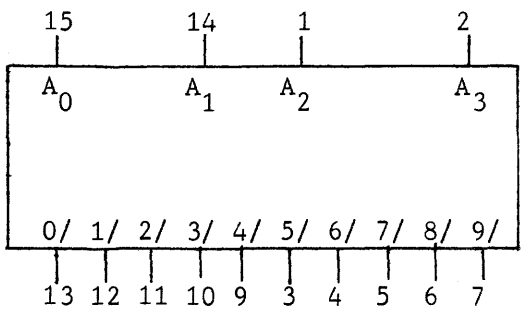


FIG. IIC-106 ONE OF TEN DECODER

ROM CHIPS

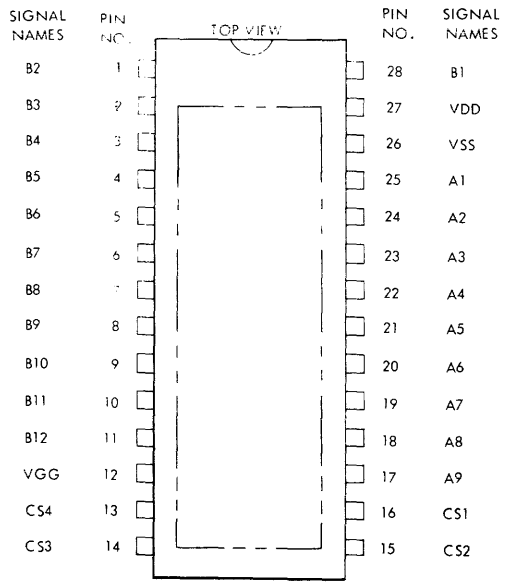
There are three different type MOS ROMs used in the L9000 TPU Micro processor logic. These are the two TPU Micro Program ROMs, the Character Generator ROMs and the PIP ROM. The chip configuration for these three ROMs is shown in Fig. IIC-107.

The ROM chips as well as the TPU LSIC inputs and outputs are all Negative MOS Logic Levels. With Negative MOS Logic Levels a 0 is a more positive voltage (+5 volts) and a 1 is a more negative voltage (0 volts).

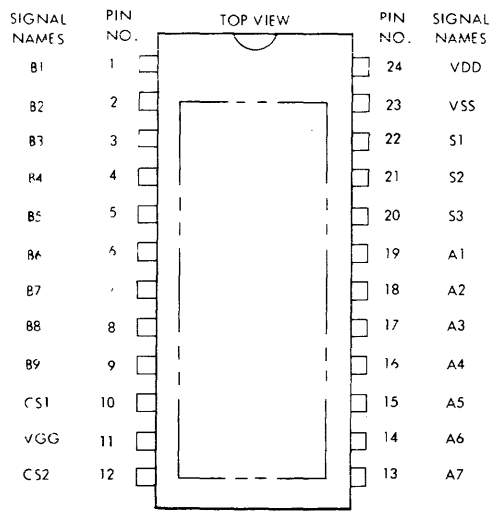
The TPU Micro Program ROMs consist of 512 characters of 12 bit wide data (B1-B12) and is referred to as a 512 X 12 ROM. The active state of the ROM inputs and outputs is 0 volts and is said to be low active.

The Character Generator ROMs are 96 X 7 X 9 which means that there are a total of 96 9 bit characters (B1-B9 outputs) which are counted out in serial fashion by counting the S1-S2 scanning line inputs from 1 to 7 for each 8 bit address into the chip (A1-A7).

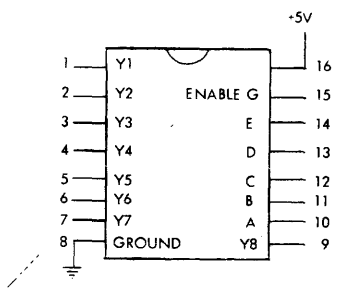
The PIP ROM is a 32 X 8 ROM. It contains 32 characters of 8 bit data selected by the 8 address line inputs enabled by the ENABLE signal.



TPU ROM (512 X 12)



CHARACTER GENERATOR ROM (96 X 7 X 9)

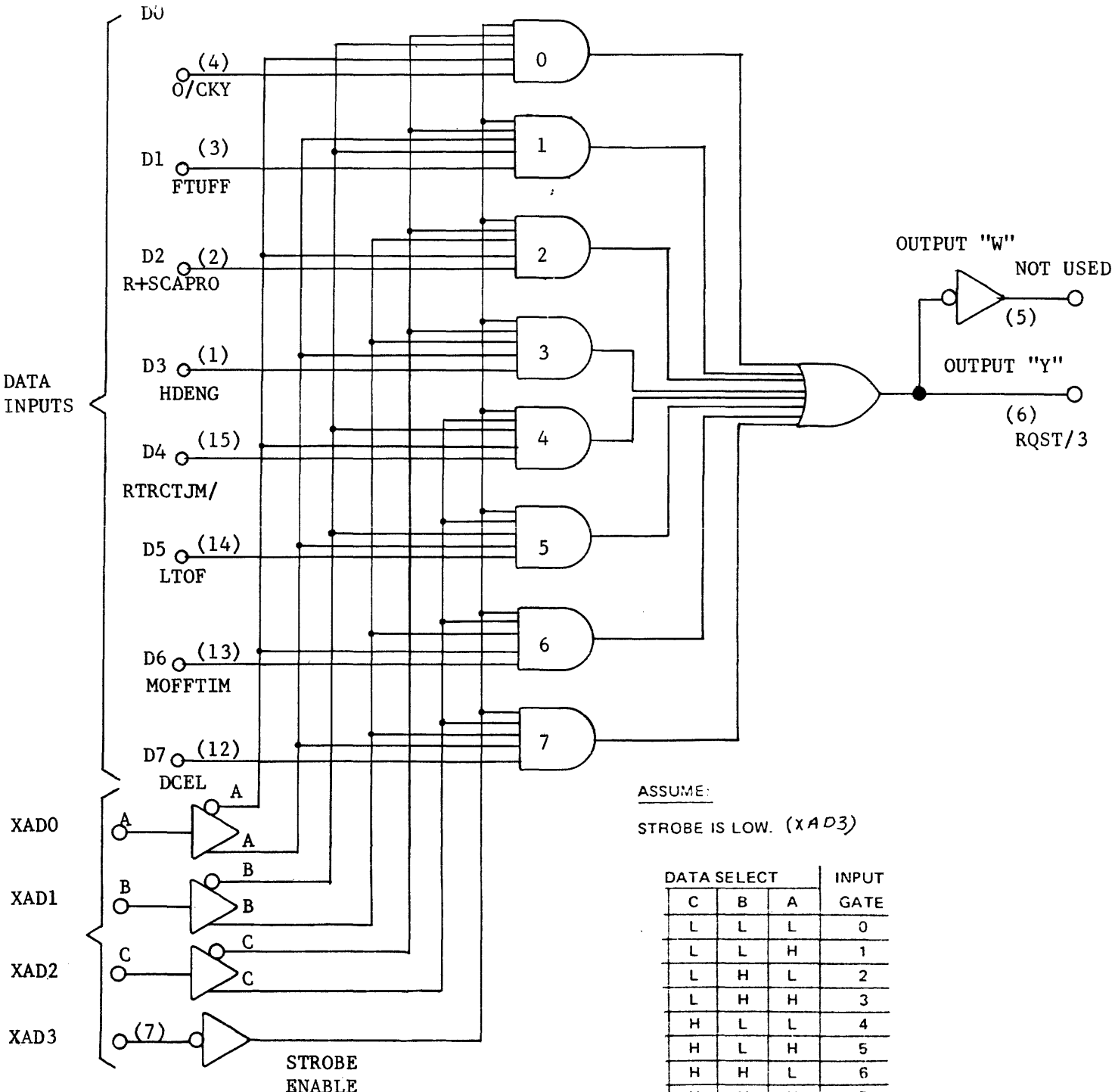


PIP ROM (32 X 8)

FIG. IIC-107 L9000 ROMS

DATA SELECTOR MULTIPLEXER

The Data Selector Multiplexer shown in Fig. IIC-108 is used to reflect the status of various PCF functions to the TPU Microprocessor as defined by the data input signals. As seen in the accompanying truth table the data select inputs A, B, and C will determine which input gate 0-7 will be selected. The A, B, and C data select inputs are the TPU Microprocessor address lines XAD0-XAD3 respectively. XAD3/ is the strobe enable signal and must be low to enable data selection. The output of the chip RQST/-B will be set to the same condition as the data input to the selected input gate.



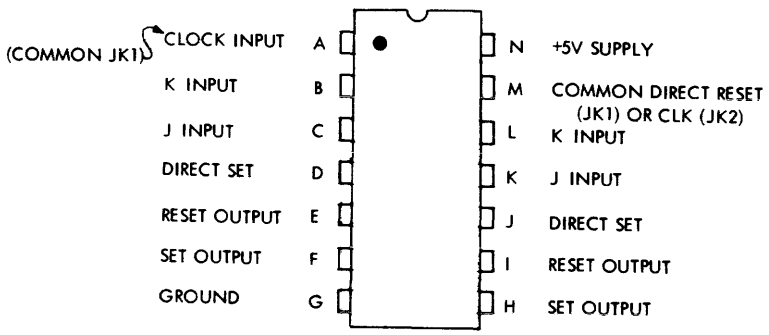
DATA SELECT			INPUT
C	B	A	GATE
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

FIG. IIC-108 DATA SELECTOR MULTIPLEXER

JK FLIP-FLOPS

There are two types of JK Flip-flops used in the L9000. They are designated JK1 or JK2. Fig. IIC-109 shows the layout of the two types. The JK1 chip has two flip-flops sharing a common clock input and a common direct reset input. The JK2 chip has a seperate clock input for both flip-flops but no direct reset for either.

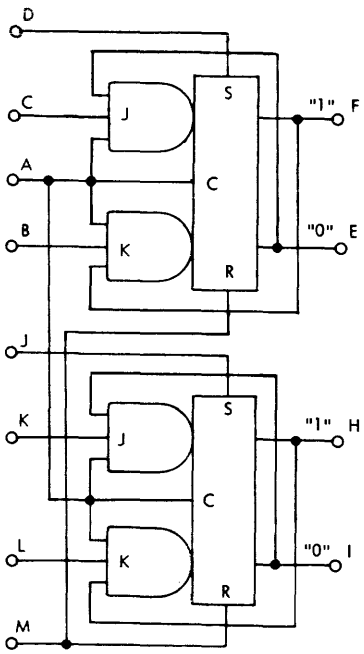
Both the JK1 and JK2 flip-flops function as shown in the accompanying truth table.



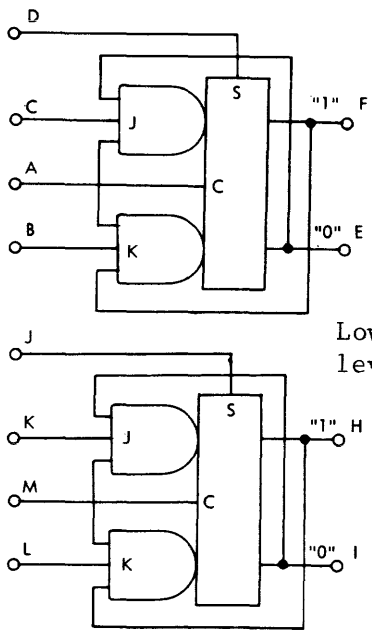
DUAL JK FLIP-FLOP PACKAGE
PIN LETTERING, NUMBERING, AND USES

TRUTH TABLE		
t_n		t_n+1
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

NOTES: A. t_n = Bit time before clock pulse.
B. t_n+1 = Bit time after clock pulse.



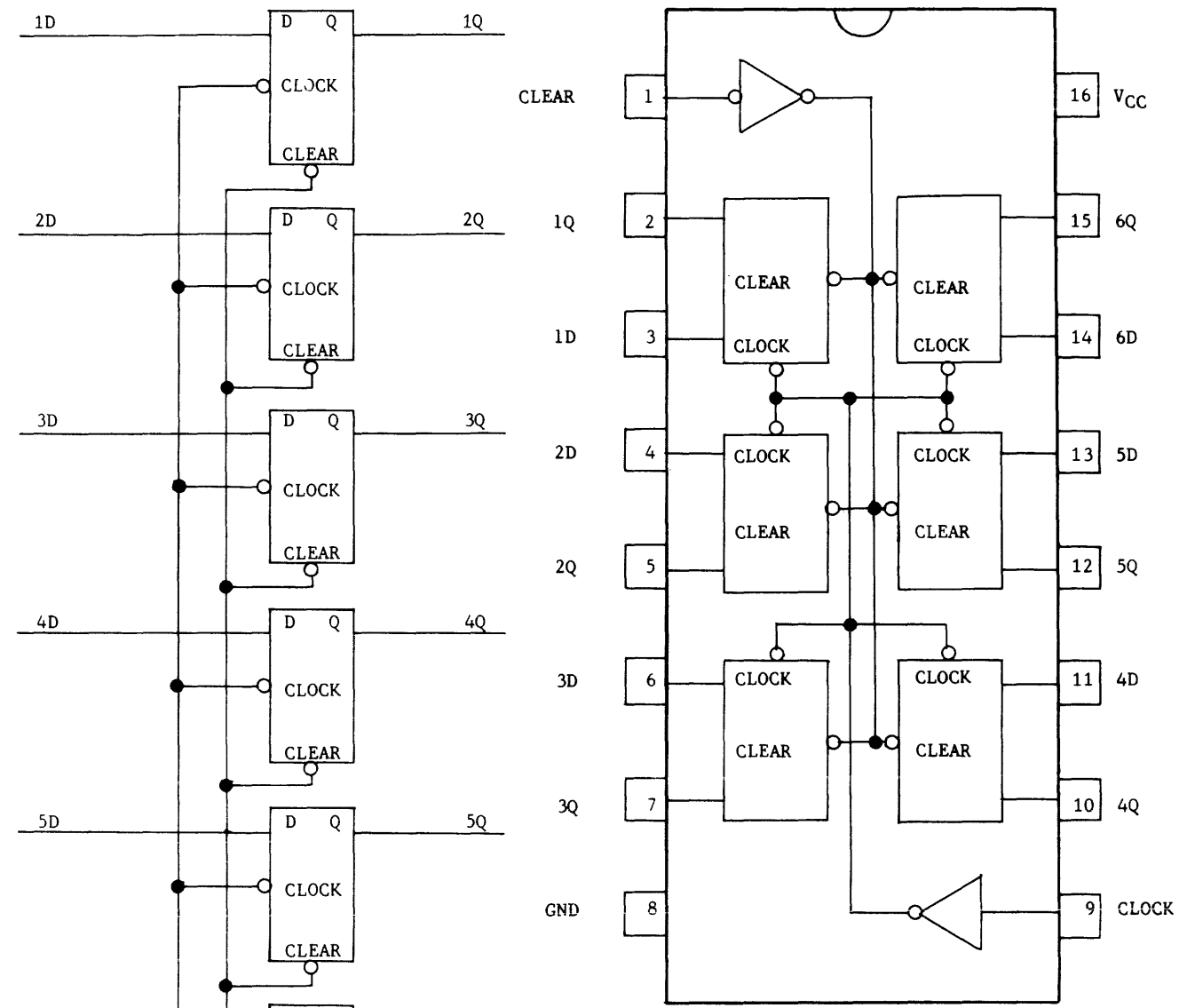
JK1 FF'S
COMMON CLOCK INPUT.
COMMON DIRECT RESET.



JK2 FF'S
INDIVIDUAL CLOCK INPUTS.
NO DIRECT RESET.

Low input to preset sets Q to high level. Preset is independent of clock.

Fig. IIC-109 J-K FLIP-FLOPS



TRUTH TABLE

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	QO

H = HIGH LEVEL VOLTAGE
L = LOW LEVEL VOLTAGE
X = IRREVALENT
↑ = TRANSITION FROM LOW TO HIGH LEVEL
QO = LEVEL OF Q BEFORE THE INDICATED STEADY STATE INPUT CONDITIONS WERE ESTABLISHED

FIG. IIC-110 D-TYPE FLIP-FLOP

D-TYPE FLIP FLOP

The D-Type Flip flop shown in Fig. IIC-110 consists of six flip flops with a common clock input and a common clear line. Input data is transferred from the D inputs to the Q outputs on the positive-going edge of the clock pulse.

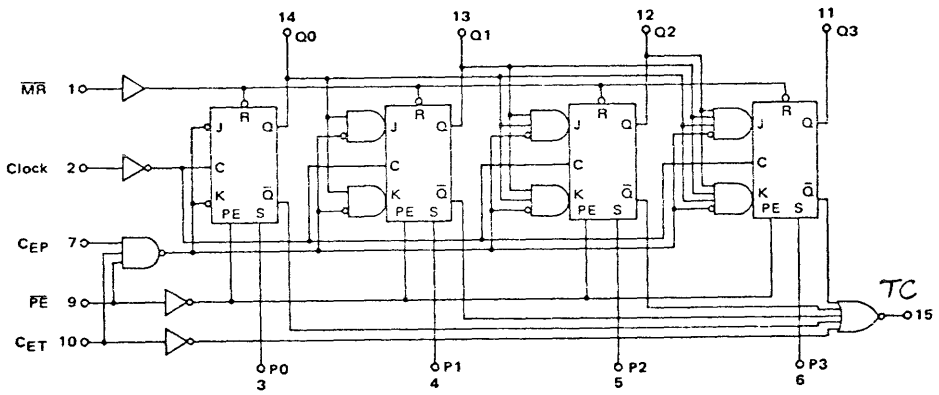
FOUR BIT BINARY COUNTER

The four Bit Binary Counter is shown in Fig.IIC-111 and has two modes of operation in the L9000. The counter may be operated as a straight binary counter counting from 0 to a maximum count of 15 (TC output). The counter may also be preset via its PE/ line to a specific count which appears on the P0-P3 lines.

In most instances in the L9000 this counter will first be preset to a specific count, then counted up to a desired count. Several Counters may be cascaded to achieve counts greater than 15 where required. This is done by hooking the TC output of one stage to the CET input of the next stage to clock the second stage once for every 15 counts in the first stage.

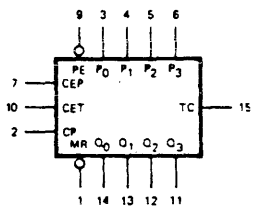
Referring to Fig.IIC-111 when the MR/ line goes low all four Flip-flops will be reset. To allow operation of the counter, MR/ must be high. Each Flip-flop has a binary weight as shown in the schematic respresentation.

When PE/ goes low, the Flip-flops will be preset to a count between 0-15 by the condition on the P0-P3 inputs. In the count up mode, counting will begin from 0 or the preset value. The first counter Flip-flop is enabled and compliments on each clock pulse. As each Flip-flop sets, the next one is enabled to set as shown in the timing diagram.



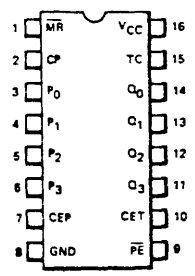
V_{CC} = Pin 16
GND = Pin 8

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAMS
DIP (TOP VIEW)



MODE SELECTION

$\overline{PE}$	CEP	CET	MODE
L	L	L	Preset
L	L	H	Preset
L	H	L	Preset
L	H	H	Preset
H	L	L	No Change
H	L	H	No Change
H	H	L	No Change
H	H	H	Count

($\overline{MR}$ = HIGH)

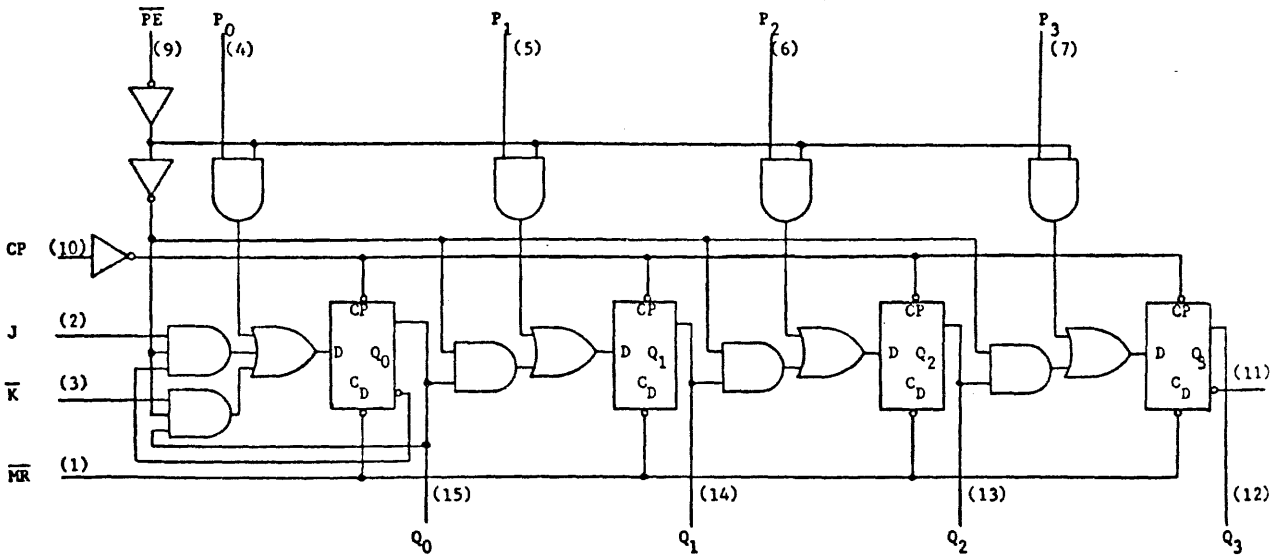
PIN NAMES

$\overline{PE}$	Parallel Enable (Active LOW) Input
P_0, P_1, P_2, P_3	Parallel Inputs
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock (Active HIGH Going Edge) Input
$\overline{MR}$	Master Reset (Active LOW) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
TC	Terminal Count Outputs

FIG. IIC-111 FOUR BIT BINARY COUNTER

FOUR BIT SHIFT REGISTER

The Four Bit Shift Register is shown in Fig. IIC-112. The register may be used to synchronously shift data appearing at the J or K inputs with application of a clock pulse. However, the Four Bit Shift Register is used as a 4 bit latch in the L9000. This is accomplished by permanently enabling the PE/ input of the chip, i.e. grounding the PE/ line. This causes data appearing on the P0-P3 input lines to be loaded into its associated flip-flop and appear at the Q0-Q3 outputs respectively. In this case the J and K inputs are not used and the data transfer from parallel input (P0-P3) to the Q0-Q3 outputs occurs after the positive transition of the clock pulse. The MR/input, when low, causes the Q0-Q3 outputs to reset.



Notes:
1. Terminal 16 = V_{CC}; terminal 8 = ground.
2. Input/output terminal number is given in parentheses adjacent to the input/output.

Terminal	Name
$\overline{PE}$	Parallel Enable (Active Low) Input
P_0, P_1, P_2, P_3	Parallel Inputs
J	First Stage J (Active High) Input
$\overline{K}$	First Stage K (Active Low) Input
CP	Clock (Active High) Going Edge Input
$\overline{MR}$	Master Reset (Active Low) Input
Q_0, Q_1, Q_2, Q_3	Parallel Outputs
$\overline{Q}_3$	Complementary Last Stage Output

FIG. IIC-112 FOUR BIT SHIFT REGISTER

TWO PHASE MOS CLOCK DRIVER

The Two Phase MOS Clock Driver shown in Fig. IIC-113 consists of 2 seperate inverting drivers used to supply the PH1/ and PH2/ clocks to the TPU LSIC. The output of each clock driver uses an external pull up resistor to +5 volts. The drivers provide negative going clock pulses into the TPU LSIC. The level of the clock pulses will swing from +5 volts to -12 volts.

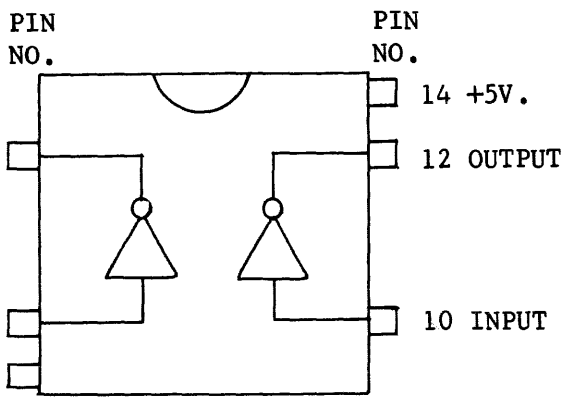


FIG. IIC-113 TWO PHASE MOS CLOCK DRIVER

UP-DOWN COUNTER

The four bit UP-DOWN counter shown in Fig.IIC-114 is similar in operation to the four bit binary counter. The UP-DOWN counter has two seperate clock inputs, one for count up (CPU) and one for count down (CPD).

Negative going clock pulses into CPU with CPD held high will cause the counter to count up. Likewise negative clock pulses into CPD with CPU held high causes the counter to count down. The timing for both the count up and count down modes is illustrated in the timing diagram.

As used in the L9000, the UP-DOWN counter is first preset to the count on the PA-PD inputs when PL/ goes low. The counter will then count up or down. In the L9000 the up down counter is loaded to the value of CRGR and PIB, then counted up or down as determined by CRGR to change the scanning address lines of the character generator ROM or PIP ROM as printing occurs.

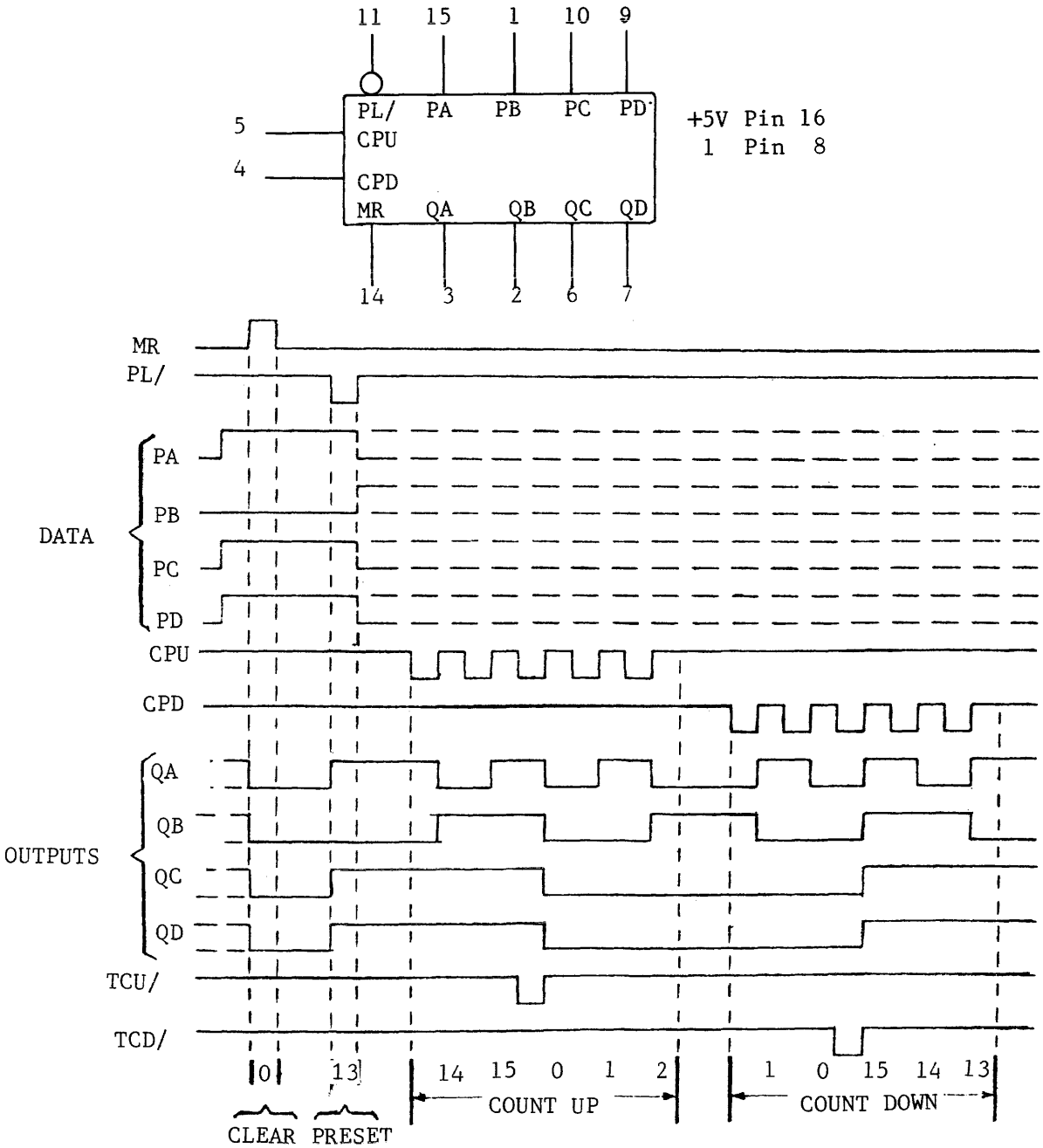


FIG. IIC-114 UP-DOWN COUNTER

HALF-DUPLEX TRANSMITTER RECEIVER

The Half-Duplex Transmitter Receiver chip shown in Fig. IIC-115 is used to control data transfer to and from the TPU LSIC in the L9000. Each chip is capable of controlling two data lines. Since there are 8 data lines, OBD1C-OBD8C, a total of four Half-Duplex Transmitter Receiver chips are used in the L9000.

Data Transfer through the chip will be from pin 4 to pin 1 and from pin 10 to pin 13 when WRITE/ (pin 3) is high and WRITE-1 (pin 11) is low. When the conditions of WRITE/ and WRITE-1 are reversed, ie. WRITE/ is low, WRITE-1 is high, data transfer will be from pin 1 to pin 6 and from pin 13 to pin 8.

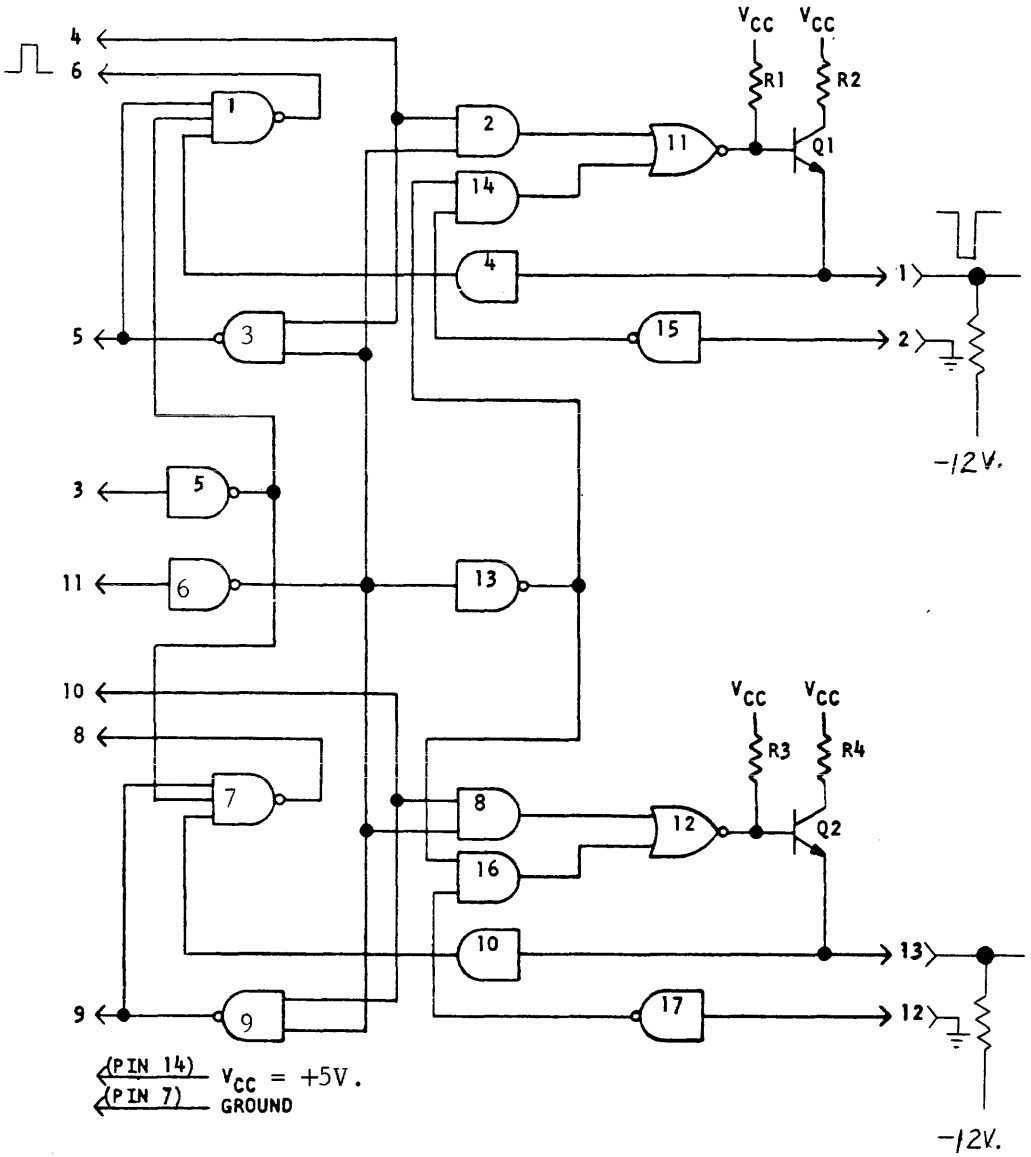
Since there are two identical circuits in each chip with a common control, an explanation of only the upper portion will be given here. It should be understood that both circuits function identically and simultaneously.

Front End Data to TPU.

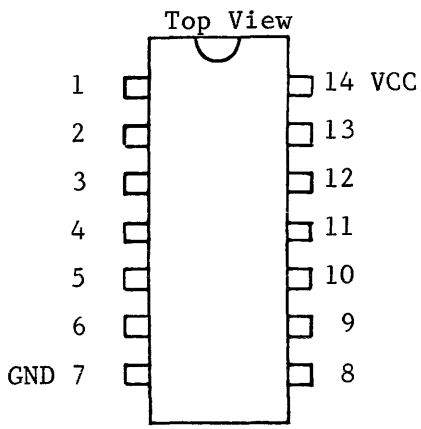
When pin 3 is high the low out of gate 5 disables gate 1 causing pin 6 to go high. The low on pin 11 causes gate 6 to go high enabling gate 2. The positive going data pulses on pin 4 appear on the upper input of NOR gate 11 through AND gate 2. Pin 2 of the chip is permanently grounded causing gate 15 to output a high into AND gate 14. The high from gate 6 is inverted through gate 13 making the upper input of gate 14 low. The lower input of NOR gate 11 is now low. The positive going pulse on the upper input of NOR gate 11 appears as a negative pulse on the base of Q1. Q1 is cut off and pin 1 is pulled down to -12 by the externally connected pull down resistor. Q1 conducts during the positive duration of the pulse on Q1 causing pin 1 to go to +5V. The negative pulse at pin 1 under goes a transition from +5 Volts to -12 Volts.

TPU Data to Ports.

With pin 3 low, the output of gate 5 is high causing the center input of gate 1 to be high. Pin 11 is high and gate 6 makes the lower input of gate 3 low. Gate 3's output makes the top input of gate 1 high. The negative TPU data pulse on pin 1 appears on the lower input of gate 1 after buffering through AND gate 4. The pulse at pin 1 under goes a transition from +5 Volts to -12 Volts. AND gate 4 changes this level to +5 volts and ground. The output of gate 1 at pin 6 will be a positive pulse in response to the negative input pulse at pin 1.



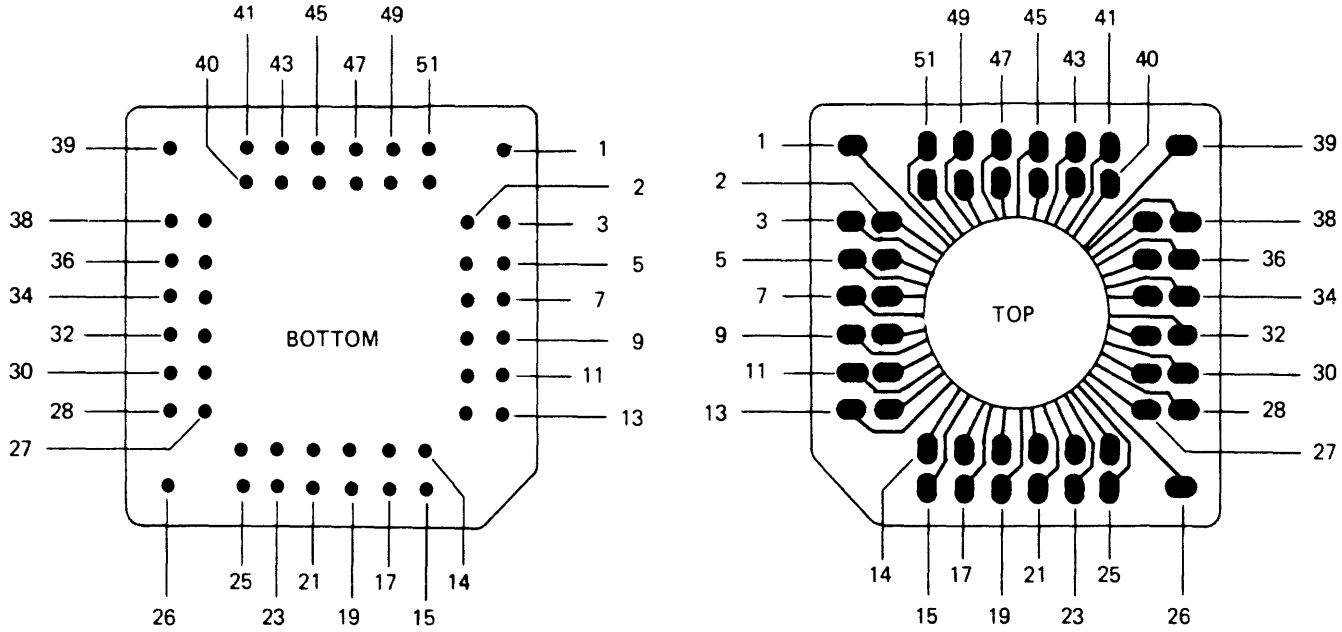
DATA IN	CONTROL		DATA TRANSFER	
	WRITE/	WRITE-1		
PINS 4 & 10	H	L	PIN 4 TO 1	PIN 10 TO 13
PINS 1 & 13	L	H	PIN 1 TO 6	PIN 13 TO 8



TTL MSI HALF DUPLEX TRANS/REC CHIP

FIG. IIC-115 HALF DUPLEX TRANSMITTER/RECEIVER

Fig. IIC-116 illustrates the pin identification layout of an LSIC. Pins 13 and 15 are located closest to the double-edged side of the LSIC. All input/output signals are accessible for probing on the top surface of the chip.



TPU LSIC Inputs and Outputs

All TPU LSIC inputs and outputs (FigureIIC-116) are Negative MOS Logic Levels. A logic "1" = 0V and a logic "0" = +5V.

Pin No.	Signal Name	Function	Pin No.	Signal Name	Function
1	VSS	+5 VOLTS	27	TPUD6/-M	IN/OUT
2	CTL	OUTPUT	28	TPUD5/-M	IN/OUT
3	DIR	OUTPUT	29	TPUD4/-M	IN/OUT
4	PAD 0/	OUTPUT	30	TPUD3/-M	IN/OUT
5	PAD 1/	OUTPUT	31	TPUD2/-M	IN/OUT
6	PAD 2/	NOT USED	32	TPUD1/-M	IN/OUT
7	XAD 0/	OUTPUT	33	ROM 9/	INPUT
8	XAD 1/	OUTPUT	34	ROM 8/	INPUT
9	XAD 2/	OUTPUT	35	ROM A/	INPUT
10	XAD 3/	OUTPUT	36	ROM B/	INPUT
11	RQST	INPUT	37	ROM 7/	INPUT
12	IOX/	OUTPUT	38	ROM 6/	INPUT
13	ADD7/	OUTPUT	39	VD	-3 VOLTS
14	ADD6/	OUTPUT	40	ROM 5/	INPUT
15	ADD5/	OUTPUT	41	ROM 4/	INPUT
16	ADD4/	OUTPUT	42	Ø2	CLOCK INPUT
17	ADD3/	OUTPUT	43	Ø1	CLOCK INPUT
18	ADD2/	OUTPUT	44	INIT/	INPUT
19	ADD1/	OUTPUT	45	ROM 3/	INPUT
20	ADD0/	OUTPUT	46	ROM 0/	INPUT
21	FETCH	OUTPUT	47	ROM 1/	INPUT
22	T4	NOT USED	48	ROM 2/	INPUT
23	TFLAG	NOT USED	49	INTRPT/	NOT USED
24	TPUD8/-M	IN/OUT	50	R/W	NOT USED
25	TPUD7/-M	IN/OUT	51	RM	NOT USED
26	VDD	-12 VOLTS			

FIG. IIC-116 TPU LSIC INPUTS & OUTPUTS

L9000 TPU MICRO-PROCESSOR

The PCF functions of the L9000 are controlled by a TPU Micro-processor consisting of a single TPU LSIC in conjunction with 1K X 12 of ROM program memory and other associated logic found on the PCF Control, 60 CPS P.C. card. The TPU Micro-processor receives PCF control and data characters from the basic processor via the Front End output FIFO, processes this data, and sends instructions to the PCF ports for execution. A brief description of all the elements of the L9000 TPU Micro-processor follows; reference should be made to the block diagram shown in Fig. IIC-117.

TPU LSIC

The TPU LSIC is a complete micro processor contained within a standard 51 pin LSIC package. The TPU LSIC is shown in block diagram form in Fig. IIC-118 and consists of an instruction register, a number of seperate storage registers (A, B, X, Y and Q), an arithmetic logic unit (ALU), a decoder and state machine along with other internal logic which together form a complete processor. The TPU LSIC contains no internal micro instruction set. All micro instructions required for the TPU LSIC to cycle and control PCF functions in the L9000 are contained in two externally connected micro program ROM chips.

MICRO PROGRAM ROMS

There are two (512 X 12) ROM chips which contain 1024 12 bit wide micro instructions required to cycle the TPU LSIC micro processor. The implementation of these micro instructions in the TPU LSIC allows the TPU micro processor to act upon the PCF control codes. The PCF control codes, both control characters and data characters, are sent to the TPU micro processor from the console through the Front End output FIFO. The TPU LSIC micro processor, acting upin the PCF control codes, directs the operation of the PCF mechanics and electronics and reports back the execution of the PCF control codes to the console via the TPU microprocessor Flags port.

The inputs and outputs of both ROM chips are wired in parallel, however, only one ROM chip will output a 12 bit wide micro instruction at a time. This is accomplished by the PAD1/ signal into both ROMS. One ROM will be enabled when PAD1/ goes high while the other ROM will be enabled when PAD1/ goes low.

TPU MICRO PROCESSOR PORTS

The TPU Micro-processor controls four ports which cause PCF functions to occur as directed by the TPU Micro-processor. These ports are the carrier port, flags port, forms port and the printer port. Each of these ports performs a specific PCF function when addressed by the TPU Micro-processor. The TPU Micro-processor generates 4 address lines (XAD0 - XAD3) which are decoded into a specific port address (PORT0-PORT15) , which in conjunction with the TPU WRITE-1 command, cause TPU data (TPUD1/-M - TPUD8/-M) to load the specific PCF function into the addressed port for execution. The TPU data lines (TPUD1/-M - TPUD8/-M) are sent to the addressed port through the four Half-Duplex Xmitter/Receiver chips when the WRITE-1 control line is high. The condition of the TPUD1/-M - TPUD8/-M are inverted in the

Half-Duplex Xmitter/Receiver chip and are routed to the ports as the TPUD1 - TPUD8 signals. All four ports receive the TPUD1 - TPUD8 signals, but only the addressed port will load and execute the TPU command.

The addressed port will now execute the TPU command. The TPU Micro-processor waits until the present TPU command is executed. The completion of the command by the addressed port is signaled to the TPU Micro-processor via it's RQST line. RQST is a multiplexed signal consisting of selected feedback signals from the four ports used to signal the performance or completion of a PCF command to the TPU Micro-processor. The RQST line may also be brought high prior to the performance of a PCF function to insure correct timing prior to performing the function. To illustrate, the TPU Micro-processor will look at the O/CKY state at prot 0 time prior to loading data into the printer port at prot 4 time to insure that the carriage is closed before printing occurs. If the carriage is open and printing is to take place, the TPU Micro-processor will first ensure that it is closed before printing can take plae. Likewise certain forms functions must be done in time with the forms timing unit and RQST would signal the TPU Micro-processor prior to loading the forms port at Port 1 time.

TPU MICRO-PROCESSOR FUNCTIONAL DETAIL

The TPU Micro-processor, under ROM program firmware control, causes the 8 bit (byte) PCF control code to be read into the TPU LSIC via the Front End Output FIFO. The TPU Micro-processor decodes the PCF code and writes the proper instructions into the four PCF ports via the TPU address lines for execution of the PCF function.

The reading of data into the TPU and the subsequent writing of instructions and print codes to the ports is controlled by three internally generated signals from the TPU. These signals are CTL (Control), IOX/ (Input Output Exchange) and DIR (Direction). These three signals are decoded on the PCF Control 60 cps P.C. card by a series of gates to generate the signals WRITE, WRITE/, WRITE-1 and ODC/ (Output Dump Command).

The condition of these signals determines the mode of operation of the TPU Micro-processor and are summerized below.

FUNCTION	CTL	IOX/	DIR	WRITE	WRITE/	WRITE-1	ODC/
READ	L	L	L	L	H	L	L
WRITE	L	L	H	H	L	H	H

READ - With the READ function enabled ODC/ causes the next byte from the Front End Output FIFO to appear on the OBD1L - OBD8L lines as inputs to the Half-Duplex Xmitter/Receiver chips. WRITE/ and WRITE-1 are the controling inputs to the Half-Duplex Xmitter/Receiver and cause the OBD1L - OBD8L lines to be read into the TPU LSIC via the TPUDX/-M lines out of the Half-Duplex Xmitter/Receiver.

WRITE - With WRITE-1 and WRITE/ controlling the Half-Duplex Xmitter/Receiver TPU Data on the TPUDX/-M lines will be transferred through the Half-Duplex Xmitter/Receiver to the TPUDX lines. TPUDX along with WRITE will cause this TPU data to be written to the port addressed by the TPU.

The TPU Micro-processor continues to cycle, reading the micro program ROM's and writing TPU data to the ports at selected addresses until the PCF function is complete.

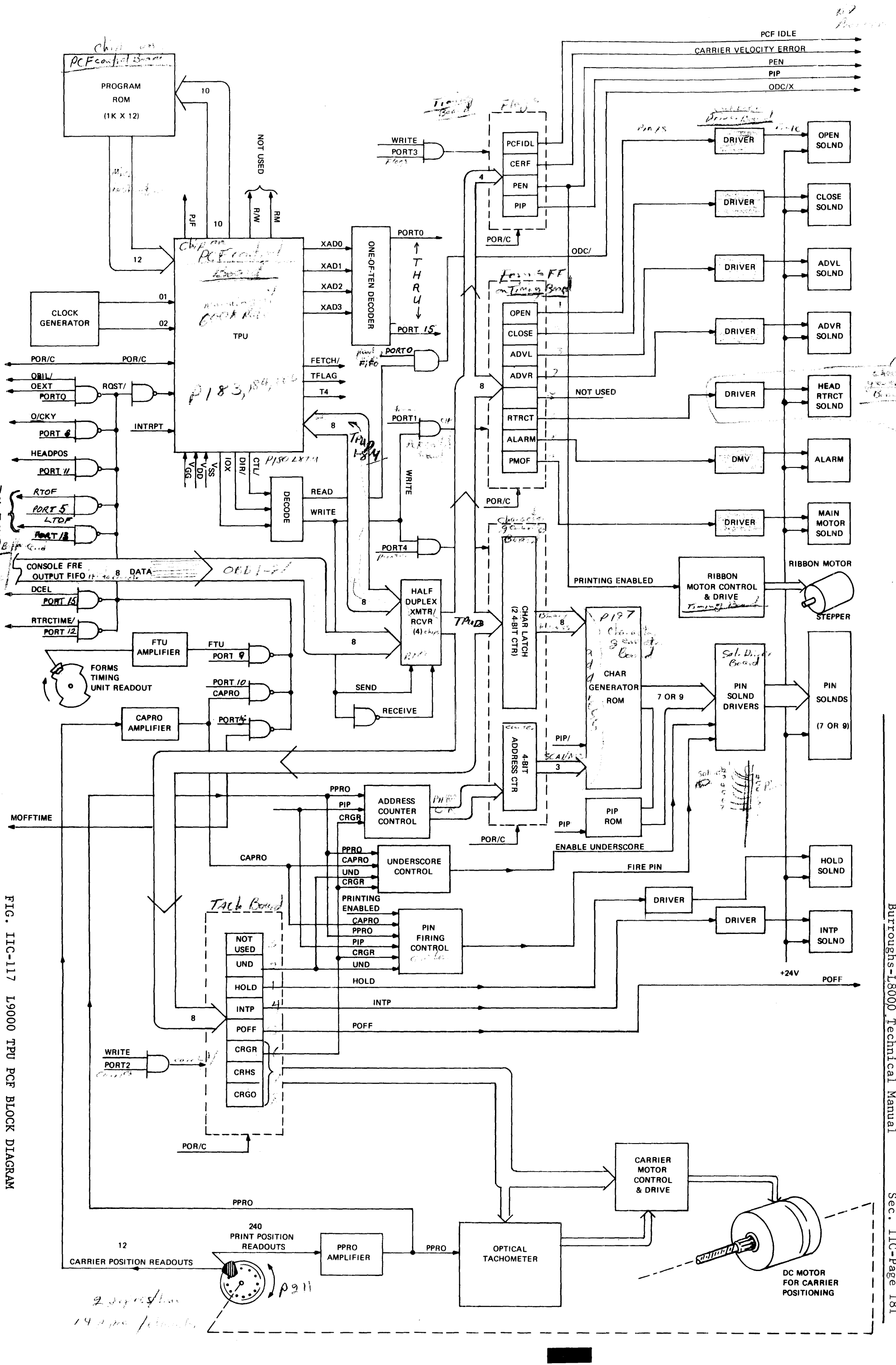


FIG. IIC-117 L9000 TPU PCF BLOCK DIAGRAM

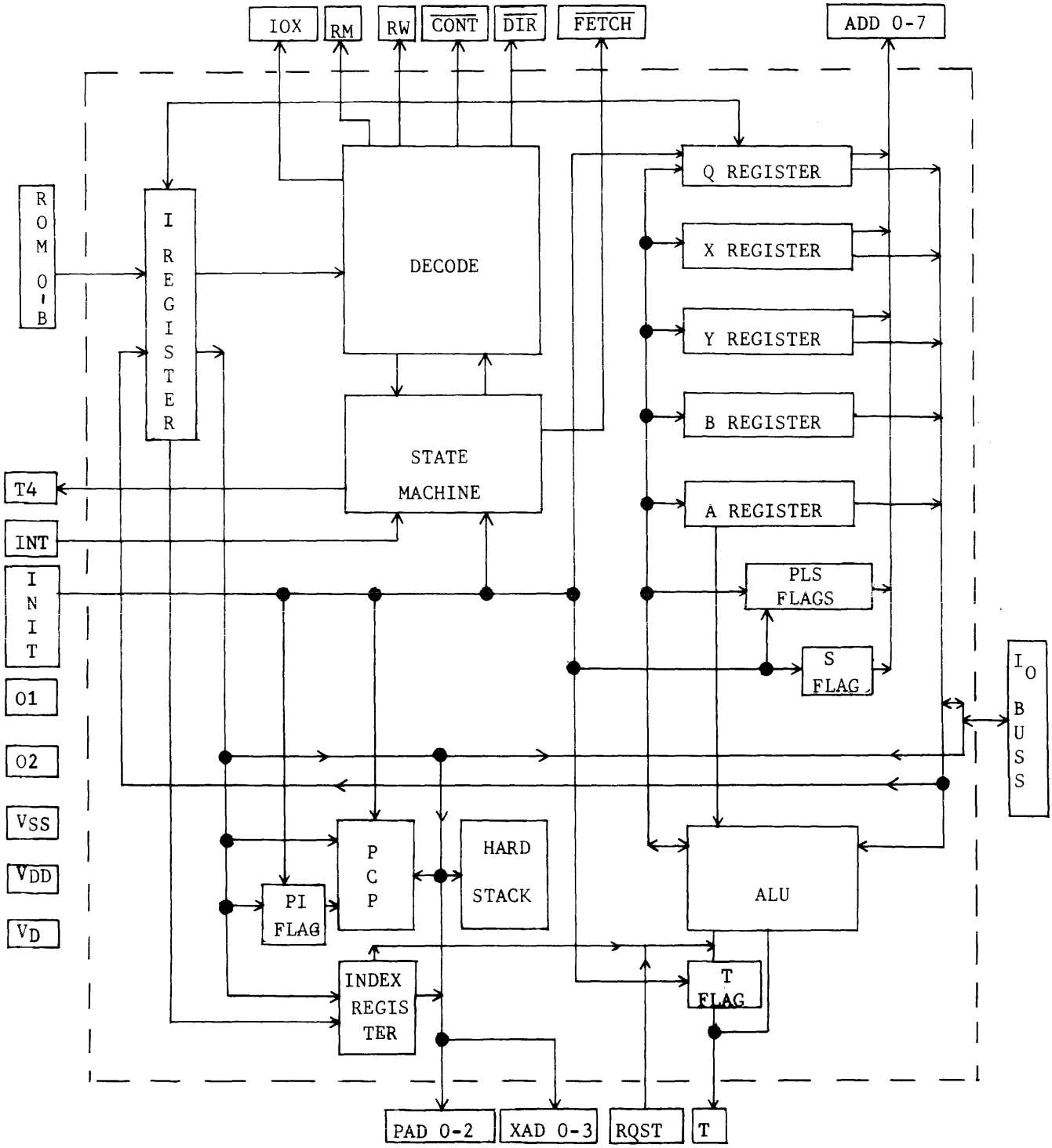


FIG. IIC-118 BLOCK DIAGRAM TPU LSIC

PORT ADDRESS GENERATION

The TPU Micro-processor generates 16 active addresses (0-15), used to load the four PCF ports and interrogate the status of the PCF mechanisms via the RQST/-B signal. Fig. IIC-120 shows the port load functions when the port addresses 0-4 are active. Port addresses 5-15, when active, will bring up the RQST/-B line. The TPU monitors the RQST line at these times as the TPU Micro-processor must know the status of the PCF mechanics so that loading of the four ports, and, execution of the commands loaded will occur at the correct time in relation to the mechanics. Referring to the TPU program flow shown in Fig. IIC- it can be seen that the TPU interrogates the Forms Timing Unit (FTU) for every decoded PCF function. The status of the FTU is interrogated at the TPU port 9 address time. Since there are 4 TPU generated address lines, XAD0-XAD3, it can be seen that port address 9 consists of:

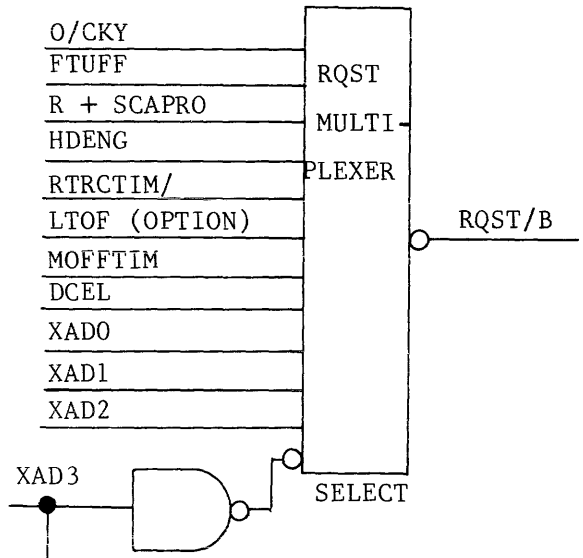
	XAD0	XAD1	XAD2	XAD3
Binary Value	1	2	4	8
	1	0	0	1

These four address lines are inputs to both the 1 of 10 Decoder as well as the RQST Multiplexer as shown in Fig. IIC-120. The 1 of 10 Decoder generates the PORT9/ signal, however, this signal is not used and merely serves as a test point. There are only five active addresses out of the 1 of 10 decoder which are actually used. These are Port 0 - Port 4. Their functions are shown in Fig. IIC-120.

XAD0 - XAD3 are also inputs to the RQST Multiplexer. XAD3 is inverted and acts as the select or enable line to the Multiplexer. Whenever XAD3 is set, addresses 8-15, the RQST Multiplexer will be enabled to reflect the status of the control inputs, O/CRY - DCEL, onto the RQST/-B output as shown in Fig. IIC-120.

The generation of the port addresses 8-15 is a function of the RQST Multiplexer with XAD3, TPU address of 8, required to enable the Multiplexer.

The Port 8 - Port 15 addresses are valid TPU generated addresses decoded internally by the RQST Multiplexer. With exception of PORT8/ and PORT9/ signals out of the 1 of 10 Decoder no signal line is provided showing the Port 10 - Port 15 addresses. The Port 10 - Port 15 address, however, are used internally by the RQST Multiplexer to develop RQST/-B.



PORT ADDRESS	RQST INPUT TO TPU
5	RTOF (RIGHT TOP OF FORMS)*
6 & 7	NOT USED
8	O/CKY OPEN/CLOSE KEY
9	FTUFF (FORMS TIMING UNIT FF)
10	CAPRO (CARRIER POSITION READOUT)
11	HDENG (HEAD ENGAGED)
12	RETRCTIM/ (HEAD RETRACT TIME)
13	LTOF (LEFT TOP OF FORMS)*
14	MOFFTIM (MOTOR OFF TIME)
15	DCEL (DECELERATE CARRIER)

PORT ADDRESS	PORT FUNCTION
0	ODC/ READ OUTPUT OEXT FIFO TO TPU
1	LOAD FORMS PORT
2	LOAD CARRIER PORT
3	LOAD FLAGS PORT
4	LOAD PRINTER PORT

* INPUTS AVAILABLE BUT NOT USED. RESERVED FOR FTURE USE.

Fig. IIC-119 PORT ADDRESS GENERATION AND FUNCTIONS

Fig. IIC-120 summerizes the port assignments by the specific TPU generated addresses 0-15 and describes the functions performed at these addresses. The Port output bit assignments are also shown as well as the X-register internal to the TPU LSIC.

OUTPUT PORT
BIT ASSIGNMENTS:

CARRRIER

CRGO	CRHS	CRGR	POFF	INTP		UND	HOLD

FORMS

ALRM	ADVR	HEAD		MOF	ADVL	CLO	OPN

FLAGS

				PIP	PEN	CER	IDLE

INTERNAL REGISTERS
BIT ASSIGNMENTS:

X REG

	UND	O/C	L/R				

FORMS OPERATION TIMER
0 = PRINT RIGHT
1 = PRINT LEFT
0 = PLATEN CLOSED
1 = PLATEN OPENED
1 = UNDERSCORE ENABLED
GENERAL WORK FLAGS

Y, A & B REG ARE USED AS GENERAL WORKING REGISTERS

FIG. IIC-120 PORT ASSIGNMENT SUMMARY

PORT ASSIGNMENTS:

PORT NAME	PORT #	REMARKS
PRINTER	4	OUTPUT PORT INTO WHICH THE COMPLEMENT OF THE PRINT CODE IS LOADED
CARRIER	2	OUTPUT PORT FOR CARRIER CONTROL
FORMS	1	OUTPUT PORT FOR FORMS CONTROL
FLAGS	3	OUTPUT FLAGS PORT
FIFO	0	INPUT PORT FROM WHICH THE PCF CODES ARE LOADED INTO THE TPU
OEXT	0	REQUEST STATUS OF FIFO EXTEND LINE
LTOF	13	REQUEST STATUS OF LEFT TOP OF FORM
MOFF	14	MOTOR OFF REQUEST
RTRCTC	12	RETRACT PRINTHEAD REQUESTED IF RTRCTIM/ = 0
DCEL	15	DROP HOLD SOLENOID ONLY IF DCEL = 0, WHICH IMPLIES THAT THE CARRIER HAS DECELERATED TO A SAFE SPEED FOR STOPPING
O/CKY	8	COMPLEMENT PLATEN REQUEST
FTU	9	FORMS TIMING UNIT SIGNAL
CAPRO	10	CARRIER POSITION READOUT; AT A DETENTED POSITION, CAPRO=1
HEAD	11	PRINTHEAD POSITION; WHEN THE PRINTHEAD IS ENGAGED, HDENG=1
RTOF	5	REQUEST STATUS OF RIGHT TOP OF FORM
CTRFLD	6	PASSBOOK CENTERFOLD MAY INTERFERE WITH PRINT HEAD IF CTRFLD=1

FORMS PORT

The forms port logic is contained on the Timing/Ribbon Driver 60 CPS P.C. card and consists of two 4 bit shift registers. When the TPU Micro-processor determines that a forms function is to occur the TPU LSIC will write the specific forms functions required to the forms port. PE/ of both 4 bit shift registers is permanently enabled. The TPU data signals TPUD1 - TPUD8, which contain the forms instructions, are connected to the P0-P3 inputs of the two 4 bit shift registers. The signal WRITE/ and WRITE-1 cause TPU data to written from the TPU LSIC to the TPUD1-TPUD8 lines and consequently to the P0-P3 inputs. The signal WRITE along with the TPU PORT 1 address and the PH1 clock pulse (all high) generate the FMSLD/ signal which clocks the TPU data from the P0-P3 inputs to the Q0-Q3/ outputs of the two 4 bit shift register.

The outputs of the 4 bit shift registers are routed to the Carrier Driver P.C. card which cause the respective forms solenoids to be picked.

The relationship between the TPU data lines and their respective forms function are shown below.

FORMS PORT INPUT FROM TPU	FORMS PORT SIGNALS	FUNCTION
TPUD1	OPNDR	H PICKS FORMS OPEN SOLENOID
TPUD2	CLODR	H PICKS FORMS CLOSE SOLENOID
TPUD3	AVDLDRA	H PICKS LEFT FORMS ADVANCE SOLENOID
TPUD4	MONDR	H PICKS MOTOR ON DRIVER SOLENOID
TPUD5	NOT USED	
TPUD6	RTRCTDR	H PICKS RETRACT SOLENOID
TPUD7	ADVRDRA	H PICKS RIGHT FORMS ADVANCE SOLENOID
TPUD8	ALARM DR/	L RESETS ALARM SOLENOID DMV WHICH PICKS ALARM SOLENOID

FLAGS PORT

The flags port logic consists of one 4 bit shift register used to latch TPU data and generate flags port signals. It is located on the Timing/Ribbon Driver 60 CPS P.C. card. The flags port is written to from the TPU at port 3 time upon the WRITE command. TPUD1 - TPUD4 lines are latched into the flags port and generate the signals as shown below.

FLAGS PORT INPUT FROM TPU	FLAGS PORT SIGNAL	FUNCTION
TPUD1	PCFBUSY/	L INDICATES PCF FUNCTION BEING PERFORMED
TPUD2	CERF	H INDICATES CARRIER ERROR CONDITION
TPUD3	PEN	H ENABLE SIGNAL TO PRINTER, ALSO ENABLES RIBBON STEPPER MOTOR
TPUD4	PIB	H INHIBITS NORMAL PRINT, ENABLES PIP

RIBBON STEPPER MOTOR DRIVE LOGIC

The ribbon stepper motor logic is located on the Timing/Ribbon Driver card. The ribbon motor advances pulling the ribbon in front of the print head only when the carrier moves with the PCF busy and with printing enabled. There are three control signals used to control a four bit counter chip which initiates the basic timing for the ribbon stepper motor driver. CEP of the counter is the PEN signal from the flags port which indicates printing is enabled. CET of the counter is PPROEDG which occurs only when the carrier is in motion and occurs from movement of the readout disk on the carrier. The Clock pulse into the counter is PH1/. With CEP and CET enabled, the clock pulses will cause the four bit counter to count. The PE/ and P0-P2 parallel inputs are wired such that when the counter reaches 7 (Q0* Q1*Q2), the Q2 output is inverted and enables PE/ which resets Q0-Q2 to 0 since the corresponding P0-P2 inputs are grounded. The counter will again count to 7. This cycle continues as long as PEN, PPROEDG, and PH1 occur.

The Q2 output of the four bit counter will be a symmetrical square wave as shown in Fig. IIC-121. Q2 clocks two cross-coupled JK Flip-flops to provide two outputs JK1 Q1 and JK2 Q2 and their compliments. The Q1 and Q2 outputs are phase shifted 90° as shown in Fig. IIC-121. This 90° phase shift is required to produce rotation of the stepper motor which has a phase angle of 90°.

The Q1 and Q1/ outputs are inverted and drive the RB1A-RB1B winding in the stepper motor through two driver stages. Q2 and Q2/ are inverted and drive the RB2A-RB2B through two driver stages.

PFIDLE is gated with the Q1, Q1/, Q2 and Q2/ signals as a control to allow these signals to activate the ribbon stepper motor only when the PCF is busy, e.g. PCFIDLE=0.

The driver stages will alternately change the polarity on the stepper motor windings from +24 V. to ground. This causes current reversals of 90° to occur between the two winding of the stepper motor as shown in Fig. IIC-121.

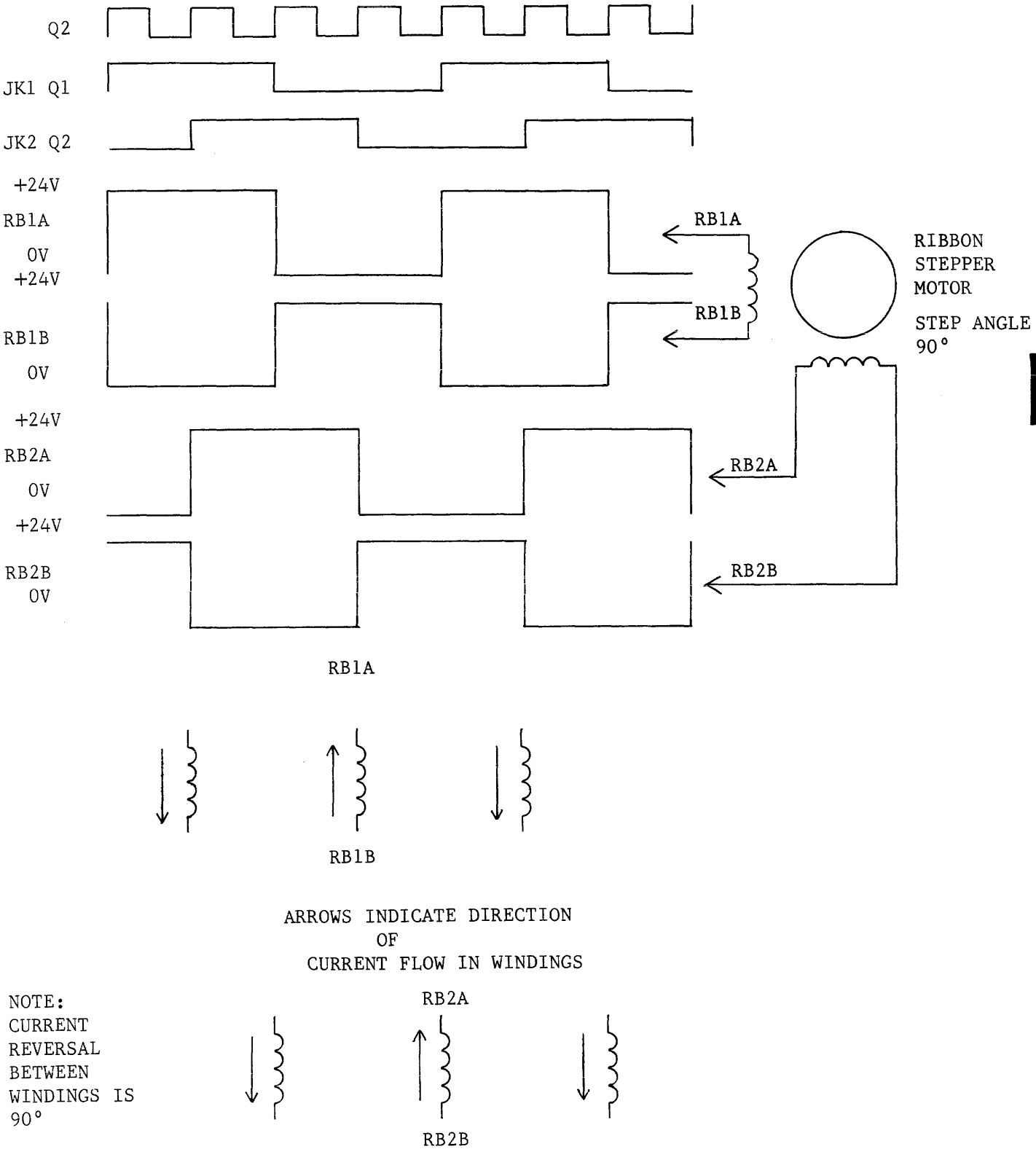


FIG. IIC-121 RIBBON STEPPER MOTOR CONTROL TIMING

SOLENOID DRIVER CIRCUITS

Four types of solenoid driver circuits are described in the following text. The first type of driver circuit is located on the Solenoid Driver 60 CPS PCB and is used for the firing of the printer pins.

Statically, the input, in this example, FP1 (Figure IIC-122) is high (+5 volts) keeping transistor A cut off. The base of transistor A is also held at a positive potential by 5VPINSD through resistors R1 and R2. The base of transistor B is statically at ground potential through resistor R5. One end of the Pin 1 Solenoid on the printer is tied to +24 volts, the other end is tied to the collector of transistor B. Thus, the Pin 1 Solenoid is de-energized.

When FP1/ goes low (0 volts) the base of transistor A is forward-biased placing the transistor into conduction. Conduction of transistor A places a positive voltage on the base of transistor B placing it into conduction. Transistor B's collector goes to ground completing the current path for energizing the Pin 1 Solenoid. When FP1/ goes high, transistor A is cut off, it in turn cuts off transistor B. The collapsing field of the solenoid coil discharges through diode CR1 which is used for transient suppression and protection of transistor B. Paralled resistors R3 and R4 are current limiting resistors which are used to protect transistor A should transistor B short out.

The second type of solenoid driver circuit is located on the Carrier Driver PCB and is used for energizing the Alarm Solenoid. The circuit consists primarily of a Dual Retriggerable 1 Shot Multivibrator (IC2 in Figure IIC-123) and a Dual Positive Nor Peripheral Driver (IC3) which is used for current gain. Either the signal SET * APBF going high or ALRAM DR/ going low will cause IC2 to produce a 25 milli-second pulse whose time duration is determined by C2 and R3. SET * APBF is only 3 micro-seconds in duration thus the Alarm Solenoid would never pick. The high output of IC2 is gated into IC3 which causes the output of IC3 to go low providing a ground path through IC3 for energizing of the Alarm Solenoid. CR1 is used for transient suppression.

The third type of solenoid driver circuit is located on the Carrier Driver PCB and is used for energizing the Advance Right Solenoid and the Advance Left Solenoid. The circuit consists of two Dual Positive NOR Peripheral Drivers (IC3 of Fig. IIC-124).

Operation of the Advance Right Solenoid is discussed. Two signals, ADVRDR (stripe ledger machines) and ADVRDRA (forms port advance) are parallel inputs to both drivers. Pull-down resistor R1 is used to keep the Advance Right Solenoid from energizing in non-stripe ledger machines, (energization would occur because the ADVRDR line would be floating (high) thus energizing the Advance Right Solenoid. When either ADVRDR or ADVRDRA go high, ground is applied to the Advance Right Solenoid through IC3.

The last type of solenoid driver circuit is also located on the Carrier Driver PCB and is used for energizing the Carriage Open, Carriage Close, Retract, Interposer, and Hold solenoids. The Retract Solenoid driver circuit is explained. The circuit consists of a Dual Positive Non Peripheral Driver (IC3 in Figure IIC-125) and a diode (CR1). When the signal RTRCTDR goes high; the output of IC3 goes low, providing a path to ground through IC3 for energizing the Retract Solenoid. CR1 is used for transient suppression.

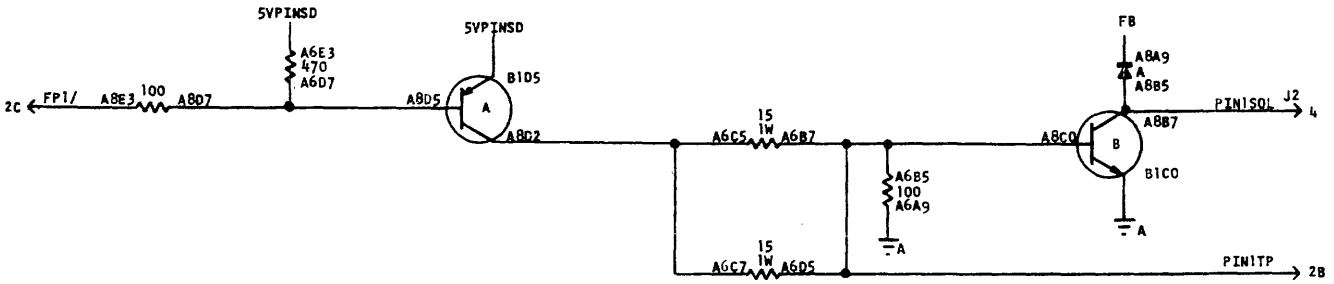


FIG. IIC-122 PIN SOLENOID DRIVER

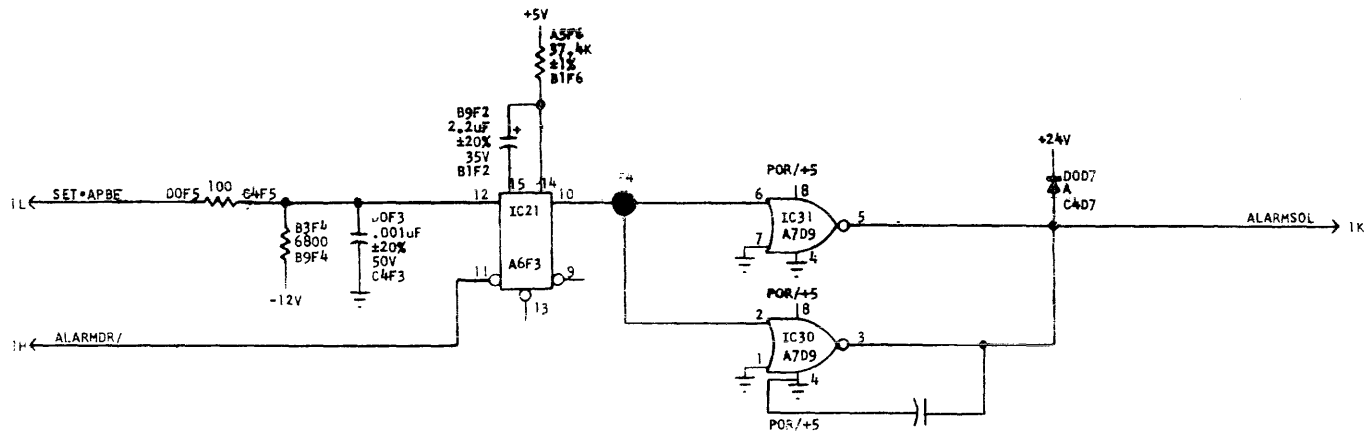


FIG. IIC-123 ALARM SOLENOID DRIVER

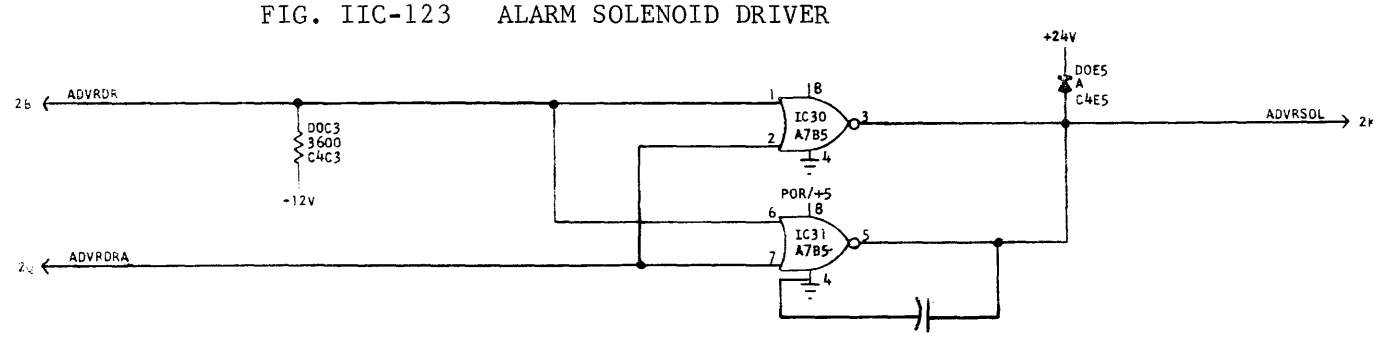


FIG. IIC-124 ADVANCE RIGHT & LEFT SOLENOID DRIVER

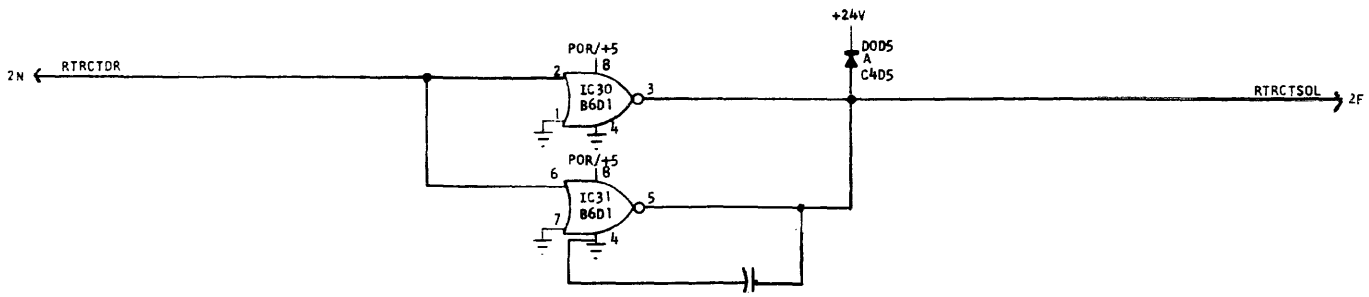


FIG. IIC-125 RETRACT SOLENOID DRIVER

PRINTER PORT

The printer port consists of two 4-bit shift registers, the character generator ROM's and other associated logic used for printing and is located on the Character Generator P.C. card. Unlike the control codes used for other PCF functions, the TPU micro-processor does not manipulate the print codes but writes the compliment of the print code received from the front end to the printer port. Writing to the printer port occurs at port four time upon the WRITE command. The gating for loading the printer port (PRTLD/) is located on the PCF Control 60 CPS P.C. card.

It is necessary for the TPU to output the compliment of the print code to the printer port since the outputs of the printer port will serve as address inputs to the Character Generator ROM. This ROM is a Negative MOS device whose active input is a 0. Each print code compliment loaded into the printer port addresses a portion of the ROM which defines which pins in the printhead are to be fired to print the character specified.

The relationship between the TPU data lines, which contain the print code compliments, and the Character Generator ROM address lines is shown below:

PRINTER PORT INPUT FROM TPU	CHARACTER GENERATOR ROM ADDRESS INPUTS
TPUD1	A1 ADDRESS INPUT TO ROM
TPUD2	A2 ADDRESS INPUT TO ROM
TPUD3	A3 ADDRESS INPUT TO ROM
TPUD4	A4 ADDRESS INPUT TO ROM
TPUD5	A5 ADDRESS INPUT TO ROM
TPUD6	A6 ADDRESS INPUT TO ROM
TPUD6/	A7 ADDRESS INPUT TO ROM
TPUD7	A7 ADDRESS INPUT TO ROM
TPUD7/	A6 ADDRESS INPUT TO ROM
TPUD8	CS1 CHIP SELECT ENABLE TO ROM

The character Generator P.C. card is arranged to accomodate either a 7-pin or 9-pin print head, different character sets, as well as PIP.

The TPUD6 and TPUD7 lines are inverted in the printer port and are cross coupled to the A7 and A6 address inputs. Jumpers are provided to enable this cross coupling to provide for some character code translation where required. Figure IIC-126 illustrates the character code sets possible and their respective ASCII codes. Included are the jumpers required to insure proper operation depending on the character generator ROM used as well as the number of needles used in the print head. These are shown for reference only and are subject to change.

CHARACTER GENERATOR FUNCTIONAL DESCRIPTION

The character generator ROM stores the bit patterns required to print the codes sent to it from the TPU. The character to be printed will be in the form of a 7 x 7 dot matrix when a 7-pin print head is used on a 9 x 7 dot matrix when a 9-pin print head is used.

Figure IIC-127 illustrates the character generator addressing and output coding for the upper case K. The print code for the K is ASCII 4/B sent to the TPU.

It should be noted that the TPU sends the compliment of the ASCII 4/B code to the printer port which addresses A1-A7 of the Character Generator ROM as shown below:

	Zone			Numeric			
ADDRESS INPUTS	A7	A6	A5	A4	A3	A2	A1
BINARY WEIGHT	512	256	128	64	32	16	8
4/B (K)	0	1	1	0	1	0	0

DECIMAL ADDRESS = 512 + 64 + 16 + 8 = 600

In addition to the A1-A7 addresses, three scanning address inputs are used (S1-S3) which together form the 10-bit address for the character to be printed. The A1-A7 address lines plus the three scanning address lines will address decimal address 601 of the ROM for the character K as shown in Fig.IIC-127.

The Character Generator ROM is an MOS device whose active inputs and outputs are 0, i.e., 0 = +5V. The inputs and outputs of the Character Generator ROM are shown as 0 active in Fig.IIC-127.

The bit patterns required for the printing of the character K reside in the ROM at addresses 601 through 607. The scanning address lines will be counted either up or down depending on the direction of carrier movement. It is necessary to change the scanning addresses seven times. This enables the seven sets of B1-B9 output codes which fire the correct pin solenoids at the seven horizontal matrix positions as the carrier moves to the right. The print head consists of either seven or nine vertically placed solenoid actuated pins which are fired to push the ribbon against the paper to produce the dots required to form a character. A 0 at B1 will enable the pin 1 solenoid driver which causes the uppermost dot to be printed. Likewise, a 0 at B7 or B9 will cause the lower most dot of the character to print depending on whether a 7-pin or 9-pin print head is used.

The three scanning addresses (S1-S3) are loaded into the character generator ROM at the same time as the A1-A7 addresses. Since the scanning lines must be changed as the carrier moves to insure the proper bit patterns out of the ROM, the logic shown in Figure IIC-128 is used.

Figure IIC-128 shows the UP-DOWN counter. The outputs of the chip are S1-S3. The PRTLD/ signal (which loads the printer port to the A1-A7 address) loads a preset count into the up/down counter on PA-PC. The preset counter is 1011 or 13 if CRGR is high or 0000=0 if CRGR is low. The state of CRGR determines the direction of

CHARACTER GENERATOR ROMS

96 CHAR STANDARD

Bits B4 B3 B2 B1	COL/ROW	2	3	4	5	6	7
0 0 0 0	0	Sp	0	@	P	`	p
0 0 0 1	1	!	1	A	Q	a	q
0 0 1 0	2	"	2	B	R	b	r
0 0 1 1	3	#	3	C	S	c	s
0 1 0 0	4	$	4	D	T	d	t
0 1 0 1	5	%	5	E	U	e	u
0 1 1 0	6	&	6	F	V	f	v
0 1 1 1	7	'	7	G	W	g	w
1 0 0 0	8	(	8	H	X	h	x
1 0 0 1	9	)	9	I	Y	i	y
1 0 1 0	10	*	:	J	Z	j	z
1 0 1 1	11	+	;	K	[	k	{
1 1 0 0	12	,	<	L	\	l	|
1 1 0 1	13	-	=	M	]	m	}
1 1 1 0	14	.	>	N	^	n	~
1 1 1 1	15	/	?	O	_	o	Sp

64 CHAR STANDARD/NATIONALISTIC

Bits B4 B3 B2 B1	COL/ROW	2	3	4	5	6	7
0 0 0 0	0	Sp	0	@	P	Ä	0
0 0 0 1	1	!	1	A	Q	Õ	1
0 0 1 0	2	"	2	B	R	Æ	2
0 0 1 1	3	#	3	C	S	Ć	3
0 1 0 0	4	$	4	D	T	Ö	4
0 1 0 1	5	%	5	E	U	Ç	5
0 1 1 0	6	&	6	F	V	Ñ	6
0 1 1 1	7	'	7	G	W	Ø	7
1 0 0 0	8	(	8	H	X	Č	8
1 0 0 1	9	)	9	I	Y	£	9
1 0 1 0	10	*	:	J	Z	ß	¹
1 0 1 1	11	+	;	K	[	Ü	{
1 1 0 0	12	,	<	L	/	Ā	|
1 1 0 1	13	-	=	M	]	Å	}
1 1 1 0	14	.	>	N	^	$	~
1 1 1 1	15	/	?	O	_	Ž	Sp

96 CHAR NATIONALISTIC (LOWER CASE)

Bits B4 B3 B2 B1	COL/ROW	2	3	4	5	6	7
0 0 0 0	0	—				´	p
0 0 0 1	1	ä				a	q
0 0 1 0	2	ö				b	r
0 0 1 1	3	ü				c	s
0 1 0 0	4	ō				d	t
0 1 0 1	5	ç				e	u
0 1 1 0	6	ā				f	v
0 1 1 1	7	n̄				g	w
1 0 0 0	8	æ				h	x
1 0 0 1	9	ā				i	y
1 0 1 0	10	ø				j	z
1 0 1 1	11	ć				k	{
1 1 0 0	12	č				l	|
1 1 0 1	13	š				m	}
1 1 1 0	14	ž				n	~
1 1 1 1	15	ß				o	Sp

96 CHAR KAWASE

Bits B4 B3 B2 B1	COL/ROW	2	3	4	5	6	7
0 0 0 0	0	Sp	0	ケ	P	ソ	マ
0 0 0 1	1	⌐	1	A	Q	タ	ミ
0 0 1 0	2	゙	2	B	R	チ	ム
0 0 1 1	3	⌐	3	C	S	ツ	メ
0 1 0 0	4	°	4	D	T	テ	モ
0 1 0 1	5	¥	5	E	U	ト	ヤ
0 1 1 0	6	ア	6	F	V	ナ	ユ
0 1 1 1	7	イ	7	G	W	ニ	ヨ
1 0 0 0	8	ウ	8	H	X	ヌ	ラ
1 0 0 1	9	エ	9	I	Y	ネ	リ
1 0 1 0	10	オ	カ	J	Z	ノ	ル
1 0 1 1	11	+	キ	K	ヨ	ハ	レ
1 1 0 0	12	,	(	L	サ	ヒ	ロ
1 1 0 1	13	−	=	M	シ	フ	ワ
1 1 1 0	14	.	)	N	ス	ヘ	ソ
1 1 1 1	15	/	ク	O	セ	ホ	Sp

LOCATION OF ROM ON THE CHAR GEN PCB

FIRMWARE LOOK-UP TABLE & THE REQUIRED HARDWARE JUMPERS ON THE CHAR GEN PCB

LOC. E2B1 — 96 CHAR DOMESTIC 9-NEEDLE PRINTHEAD

VERSION	ASCII CODE	FIRMWARE TABLE LOOK-UP OUTPUT	REMARKS
1A	COLUMN 2	COLUMN 2	JUMPER: D6E2-E2E2
	3	3	
	4	4	
	5	5	
	6	6	
	7	7	

LOC. E2B1 — 64 CHAR DOMESTIC 7-NEEDLE PRINTHEAD

VERSION	ASCII CODE	FIRMWARE TABLE LOOK-UP OUTPUT	REMARKS
1	COLUMN 2	COLUMN 2	JUMPERS: E2E4-D6E4 E9B9-F5B9
	3	3	
	4	4	
	5	5	
	6	4	
	7	5	
	7-14	7-14 ~	

E2B1 — 64 CHAR NATIONALISTIC 7-NEEDLE PRINTHEAD

VERSION	ASCII CODE	FIRMWARE TABLE LOOK-UP OUTPUT	REMARKS
2-10	FIRMWARE LOOK-UP TABLE IS IDENTICAL TO THAT USED FOR THE 64 CHAR DOMESTIC SET, WITH THE FOLLOWING EXCEPTIONS:		
2,3,4	2-3	6-9 £	JUMPERS: E2E4-D6E4 E9B9-F5B9
5	2-3	6-9 £	
	4-0	6-10 §	
	5-11	6-0 Ä	
	5-12	6-4 Ö	
	5-13	6-11 Ü	
6	5-11	6-1 Ø	
	5-12	6-5 Ç	
	5-13	6-12 Å	
7	5-12	6-6 Ñ	
8	2-3	6-9 £	
	4-0	6-4 Ö	
	5-11	6-2 Æ	
	5-12	6-7 Ø	
	5-13	6-13 Å	
	5-14	6-11 Ü	
	5-15	6-0 Ä	
9	2-3	6-9 £	
	4-0	6-10 §	
	5-11	6-3 Ç	
	5-12	6-8 Ñ	
	5-13	6-14 $	
	5-14	6-15 Ž	
10,	2-3	6-9 £	
	5-11	6-0 Ä	
	5-12	6-4 Ö	
	5-13	6-13 Å	
	5-14	6-11 Ü	

E2B1 — 96 CHAR NATIONALISTIC 9-NEEDLE PRINTHEAD

VERSION	ASCII CODE	FIRMWARE TABLE LOOK-UP OUTPUT	REMARKS
2-10	FIRMWARE LOOK-UP TABLE IS IDENTICAL TO THAT USED FOR THE 64 CHAR NATIONALISTIC SET WITH THE FOLLOWING EXCEPTIONS:		
	COLUMN 6 7 3-0 thru 3-9	COLUMN 14 15 7-0 thru 7-9	WITH FURTHER VARIATIONS WITHIN EACH VERSION AS LISTED.
2,3,4	7-14	10-0 —	JUMPERS: D6E2-E2E2 E9D8-F5D8
5	7-11	10-1 ä	
	7-12	10-2 ö	
	7-13	10-3 ü	
	7-14	10-15 ß	
6	7-11	10-4 ā	
	7-12	10-5 ç	
	7-13	10-6 æ	
	7-14	10-0 —	
7	7-12	10-7 ñ	
	7-14	10-0 —	
8	6-0	10-2 ö	
	7-11	10-8 æ	
	7-12	10-10 ø	
	7-13	10-9 å	
	7-14	10-3 ü	
9	7-11	10-11 ć	
	7-12	10-12 č	
	7-13	10-13 š	
	7-14	10-14 ž	
10	7-11	10-1 ä	
	7-12	10-2 ö	
	7-13	10-9 å	
	7-14	10-3 ü	ABN

LOC. D6E0 / LOC E2B1 — KATAKANA 7-NEEDLE PRINTHEAD

VERSION	ASCII CODE	FIRMWARE TABLE LOOK-UP OUTPUT	REMARKS
11	FIRMWARE LOOK-UP TABLE IS IDENTICAL TO THAT USED FOR THE 96 CHAR DOMESTIC SET, EXCEPT FOR THE FOLLOWING TRANSLATION:		
	2-1	10-10 *	JUMPERS: E2E4-D6E4 E9B9-F5B9 E9D8-F5D8
	2-3	10-3 #	
	3-0 thru 3-9	11-0 thru 11-9	

FIG. IIC-126 CHARACTER GENERATOR CODE SETS

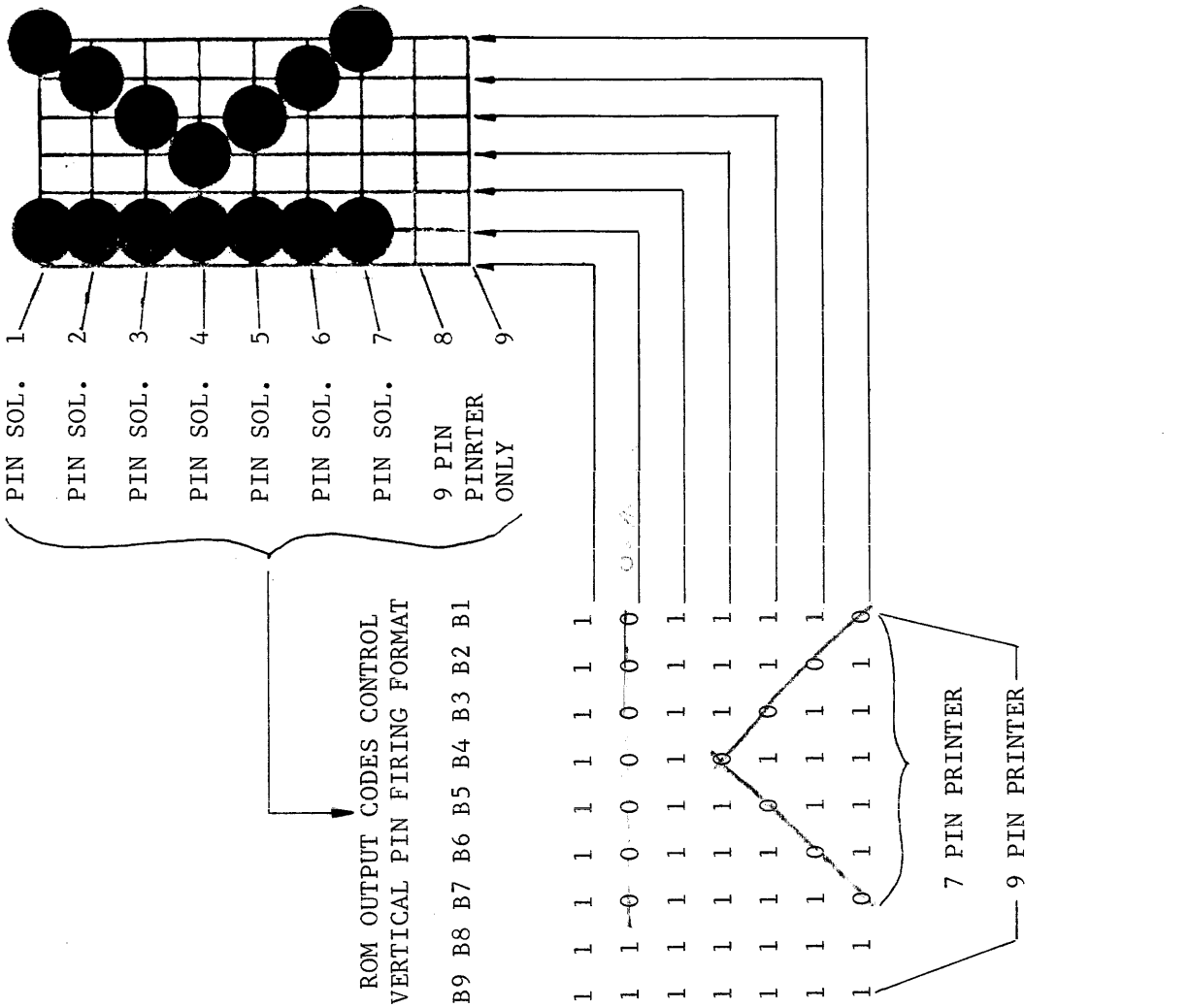


FIG. IIC-127 PRINTING AS FUNCTION OF CHARACTER GENERATOR ROM

DECIMAL ADDRESS	BINARY ADDRESS A7	A6	A5	A4	A3	A2	A1	BINARY ADDRESS CORRESPONDS TO THE ASCII PRINT CODE 4/B 4/B = K
601	0	1	1	0	1	0	0	
603	0	1	1	0	1	0	0	
602	0	1	1	0	1	0	0	
604	0	1	1	0	1	0	0	
605	0	1	1	0	1	0	0	
607	0	1	1	0	1	0	0	
606	0	1	1	0	1	0	0	

FIG. IIC-127 CHARACTER GENERATOR INPUTS & OUTPUTS

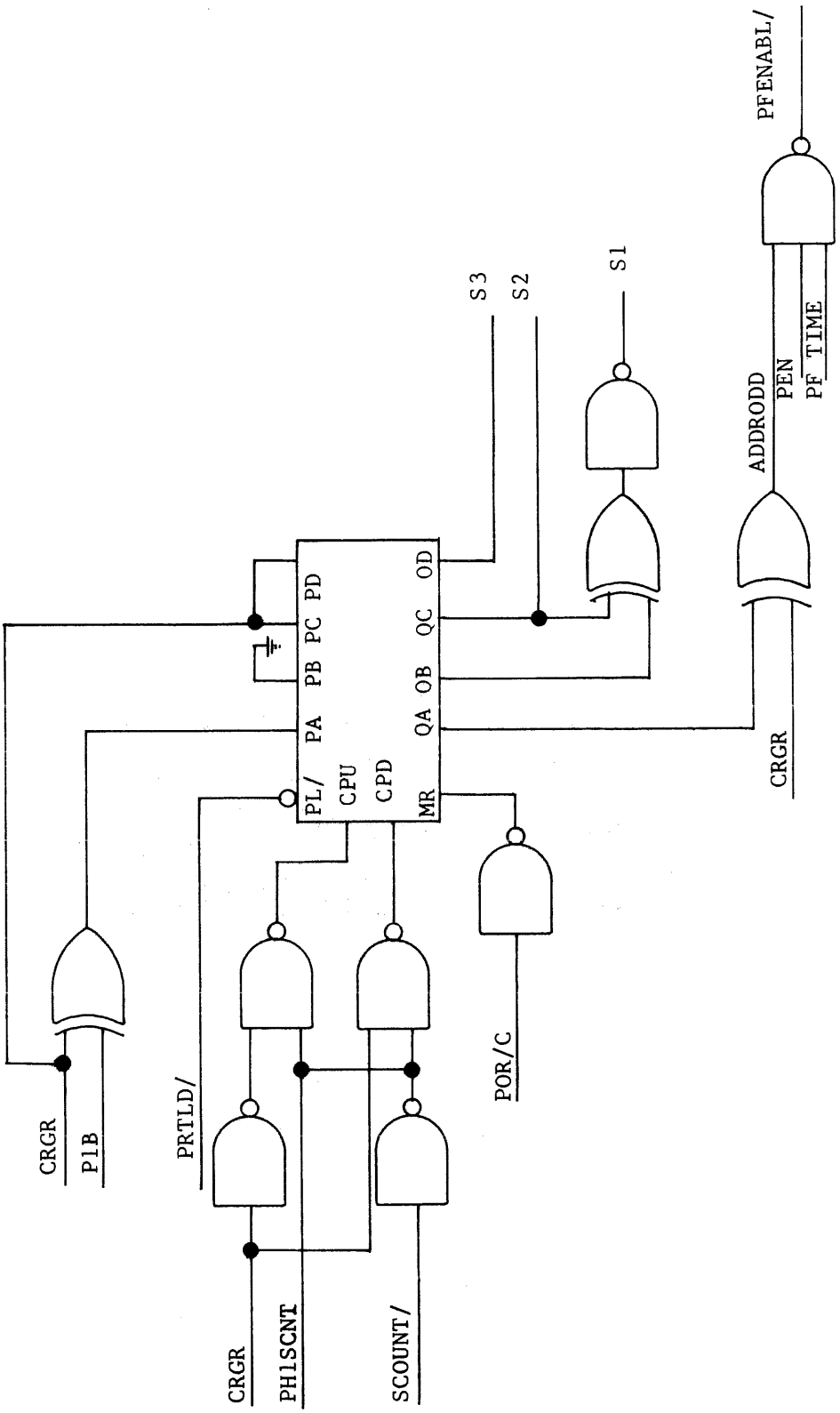
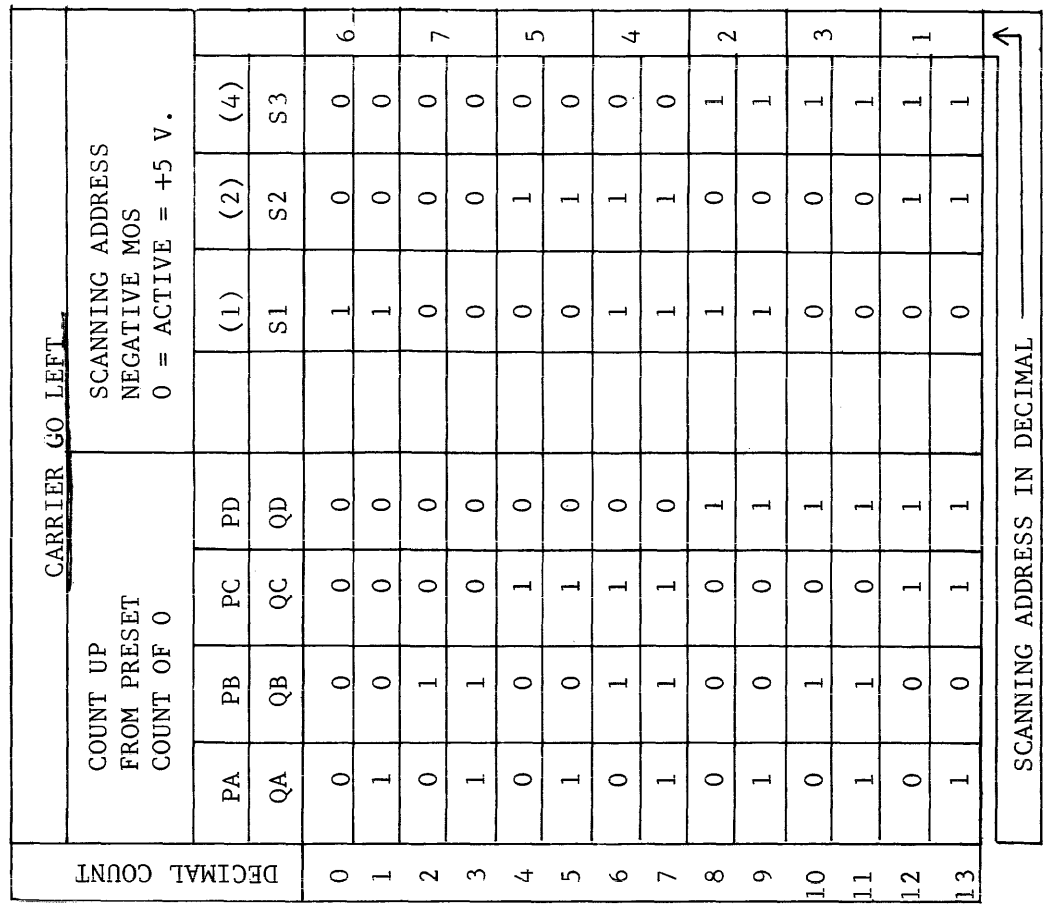


FIG. IIC-128 UP-DOWN COUNTER & S1-S3 GENERATION



CARRIER GO LEFT

DECIMAL COUNT	COUNT UP FROM PRESET COUNT OF 0 PA	PB	PC	PD	SCANNING ADDRESS NEGATIVE MOS 0 = ACTIVE = +5 V. (1)	(2)	(4)	
	QA	QB	QC	QD	S1	S2	S3	
0	0	0	0	0	1	0	0	6
1	1	0	0	0	1	0	0	
2	0	1	0	0	0	0	0	7
3	1	1	0	0	0	0	0	
4	0	0	1	0	0	1	0	5
5	1	0	1	0	0	1	0	
6	0	1	1	0	1	1	0	4
7	1	1	1	0	1	1	0	
8	0	0	0	1	1	0	1	2
9	1	0	0	1	1	0	1	
10	0	1	0	1	0	0	1	3
11	1	1	0	1	0	0	1	
12	0	0	1	1	0	1	1	1
13	1	0	1	1	0	1	1	

SCANNING ADDRESS IN DECIMAL

CARRIER GO RIGHT

DECIMAL COUNT	COUNT DOWN FROM PRESET COUNT OF 13 PA	PB	PC	PD	SCANNING ADDRESS NEGATIVE MOS 0 = ACTIVE = +5 V. (1)	(2)	(4)	
	QA	QB	QC	QC	S1	S2	S3	
13	1	0	1	1	0	1	1	1
12	0	0	1	1	0	1	1	
11	1	1	0	1	0	0	1	3
10	0	1	0	1	0	0	1	
9	1	0	0	1	1	0	1	2
8	0	0	0	1	1	0	1	
7	1	1	1	0	1	1	0	4
6	0	1	1	0	1	1	0	
5	1	0	1	0	0	1	0	5
4	0	0	1	0	0	1	0	
3	1	1	0	0	0	0	0	7
2	0	1	0	0	0	0	0	
1	1	0	0	0	1	0	0	6
0	0	0	0	0	1	0	0	

SCANNING ADDRESS IN DECIMAL

FIG. IIC-129 UP-DOWN COUNTER COUNTING SEQUENCE

carrier movement. If carrier movement is to the right, 13 is loaded into the counter. Carrier movement to the left loads the counter to 0. The state of CRGR also determines if the counter will count up (CPU) or down (CPD). The SCOUNT/ pluses from the Carrier Tachometer PC card, synchronized with the PH1 clock (PH1SCNT), will then count the counter down from 13 to 0 for right carrier movement or up from 0 to 13 for left carrier movement as shown in Figure IIC-129.

Note: The PA-PD inputs to the UP-DOWN counter are shown as positive logic levels while the S1-S3 outputs are shown 0 active.

S1-S3 are outputs from the counter. Note that S1 is an exclusive OR of QB and QC from the counter outputs which cause the S1-S3 count to be modified to count 1, 3, 2, 4, 5, 7, and 6 for a right carrier movement or 6, 7, 5, 4, 2, 3, and 1 for left carrier movement. Notice that S1-S3 are shown as negative or 0 active MOS levels, i.e., 0 = +5 volts. A count of

S1	S2	S3	
1	0	0	
(1)	(2)	(4)	BINARY VALUE

is equal to six as far as the character generator ROM is concerned. To avoid confusion between positive and negative MOS logic levels, it should be remembered that for printing a character with right carrier movement, 13 is preset into the UP-DOWN counter which counts down causing the S1-S3 lines to be counted down.

PIB PRINT

There are several important differences between normal print and PIB print. PIB means Print In Between meaning that the PIB period or comma will print in between characters. This is analogous to the PIP on a ball printer. The differences between normal print and PIB are outlined below, the logic responsible will be examined in detail.

Normal Print

1. The UP-DOWN counter is initially preset to 13 or 0, depending on direction of carrier movement.

2. The UP-DOWN counter generates the S1-S3 addresses to the Character Generator ROM. These S1-S3 addresses will change 7 times during printing of the character.

3. The UP-DOWN counter must count once (either up or down) before generating ADDRODD which occurs on a count of 12 or 1 and every other count thereafter for 7 times.

4. The output of the Character Generator ROM fires the pins in the print head seven times to produce a character.

The Character Generator ROM is arranged such that no needle fires consecutively.

PIB Print

1. The UP-DOWN counter is initially preset to 12 or 1 depending on direction of carrier movement.

2. The UP-DOWN counter generates the S1-S3 addresses to the PIB ROM. These addresses will change only twice during the PIB print of period or comma.

3. The UP-DOWN counter generates ADDRODD on the Preset of 12 or 1 and again when the counter reaches 10 or 3.

4. The output of the PIB ROM fires the pins in the print head only twice to produce the PIB period or comma. The PIB ROM is arranged such that consecutive needle firing is permitted.

It should be understood that the PIB period and comma differ in appearance from the normal period and comma due to different formatting in the PIB ROM as compared to the Character Generator ROM. These differences are shown in Fig. IIC-130. These differences are for 7 pin print head only.

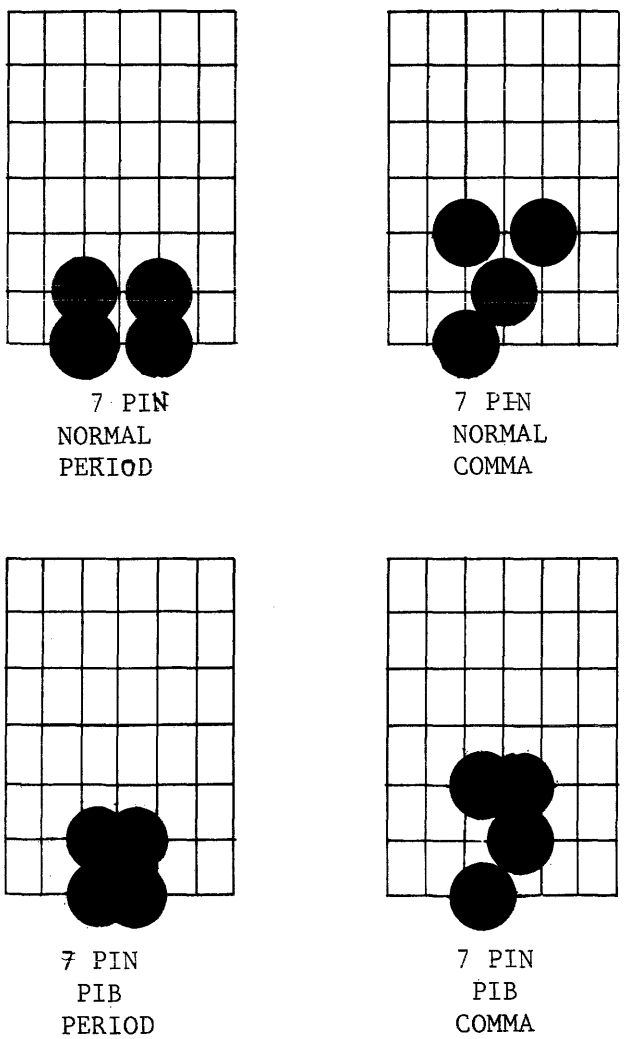


FIG. IIC-130 7 PIN PRINT HEAD PERIODS & COMMAS

MODIFIED COUNT FOR PIB

Setting of the PIB function by the TPU micro-processor modifies the count preset into the UP-DOWN counter. As seen in Fig. IIC-128 CRGR and PIB are exclusive OR'ed and control the PA input of the UP-DOWN counter. CRGR also controls both the PC and PD inputs directly. During non-PIB print CRGR and PIB, which is low, presets the counter to either 13 or 0 depending on carrier direction as defined by the state of CRGR. During PIB, however, the exclusive OR of CRGR and PIB, which is now high, causes the UP-DOWN counter to be preset to a count of 12 for PIB with right carrier movement or to a count of 1 for PIB with left carrier movement.

The UP-DOWN counter will now count either up or down as the CPU or CPD clock pulses are received. The scanning address lines S1-S3 and TPUD1 will address the PIB ROM.

The QA output of the UP-DOWN counter is exclusive OR'ed with CRGR to generate the signal ADDRODD. ADDRODD will occur only once per every two PPRO pulses as there are 14 PPRO pulses and only seven vertical print positions. ADDRODD allows printing on odd SCOUNT/ pulses. SCOUNT/ is a function of PPRO. During normal or non-PIB print, the UP-DOWN counter is preset to 13 or 0. In either case, the first ADDRODD occurs on a count of 12 or 1. ADDRODD at this time, along with PEN and PFTIME, generates PFENABL/ which allow the print head to fire pins as directed by the output codes of the character generator ROM.

During PIB, however, ADDRODD occurs on the preset of 12 or 1. This difference is significant in that the PIB character must print in between normal character positions. Under PIB, ADDRODD occurs ½ count earlier than in normal print. ADDRODD is required to generate the signal PFENABL/ which allows the PIB (or Character Generator) ROM outputs to fire the pins in the printhead as shown in Fig. IIC-131.
During PIB, the print head fires only twice to produce the compacted period or comma shown in Fig. IIC-130. The S1-S3 address lines into the PIB ROM need be incremented or decremented only once after the preset of the counter to enable the proper pins to fire to produce the period or comma. The carrier however, is still in motion producing SCOUNT/ clock pulses into the UP-DOWN counter.

After the two pin fires produce the PIB punctuation, a means of stopping the UP-DOWN counter is required after the PIB character prints. This is done by the PRTLD/ signal from the TPU Micro-processor which loads the next character to be printed into the printer port and simultaneously presets the UP-DOWN counter to either 13 or 0 for proper scanning of the Character Generator address lines. If a character does not follow the PIB punctuation, 0's are loaded into the printer port.

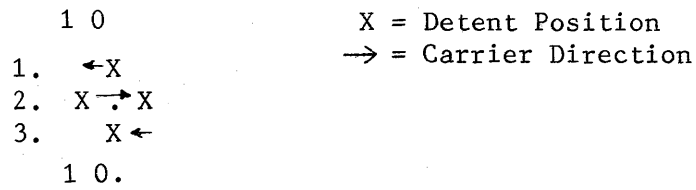
PIB OPERATION

The normal period or comma as shown in Fig.IIC-130 besides being physically wider than the PIB period or comma, also prints in a character position, i.e. between two consecutive detent positions. The PIB period or comma prints on the detent position, i.e. between two character positions.

The following explanation clarifies the carrier movements relative to the different ways in which the PIB punctuation is printed.

Assuming that 10 had been printed and the carrier is detented after the 0. To print the PIB period in the detent position or after the 0 requires some carrier manipulation provided by the TPU micro-processor to print the PIB punctuation. It should be remembered that the pin printer must be in motion before printing can take place. The TPU Micro-processor would cause the hold and interposer solenoids to pick and the carrier would reverse direction and move one character position to the left and be detented as shown in 1 below.

Carrier direction is reversed, the hold and interposer solenoids pick, and the carrier moves to the right. As the carrier moves the PIB period is printed in the original detent position as shown in 2. The carrier continues to advance and detents one character position to the right of the PIB period. Carrier direction is again reversed, and escapement to the original detent position takes place with the carrier being detented at its original detent position. This is shown in 3. The carrier remains detented here with the PIB period printed in this detent position. The TPU Micro-processor establishes the original print direction to insure printing of subsequent characters in the proper direction.

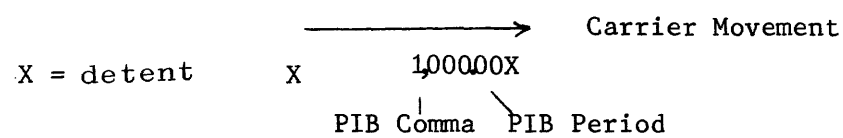


The only limitation to PIB is that if the carrier is positioned at either bumper the carrier would hit the bumper and flag Carrier error when attempting to backspace relative to direction of carrier movement.

If, during the previous example, additional characters were to be printed besides the PIB period, i.e., OEXT = 1 after the PIB period is printed, the TPU micro processor would not detent as in 2 or backspace as in 3, but would continue to print characters in 2.

Normally the PIB punctuation will be included within a group of characters printed from the Front End buffer.

In this case the PIB character will be treated as a normal character as far as the carrier is concerned, i.e. The aforementioned carrier manipulations will not be performed. The PIB character will be printed in the normal detent position with a single carrier escapement as shown below:



When the TPU Micro-processor receives the PIB code (0/1) the micro processor will branch to the PIB routine in which the next character in the FIFO will be printed as a PIB period or comma.

The TPU Micro-processor signals PIB by writing TPUD4 to the flags port at port 3 time (TPUD4=PIB). PIB going high disables the character generator ROM and enables the PIB ROM via ENABLEG as shown in Fig. IIC- PIB also disables the pin 1 print solenoid by inhibiting the FP1/ output gate.

The PIP ROM outputs PD2-PD9 control the firing of pin solenoid 2 through 9 and will output the correct print pattern, either period or comma, as formatted by the PIP ROM.

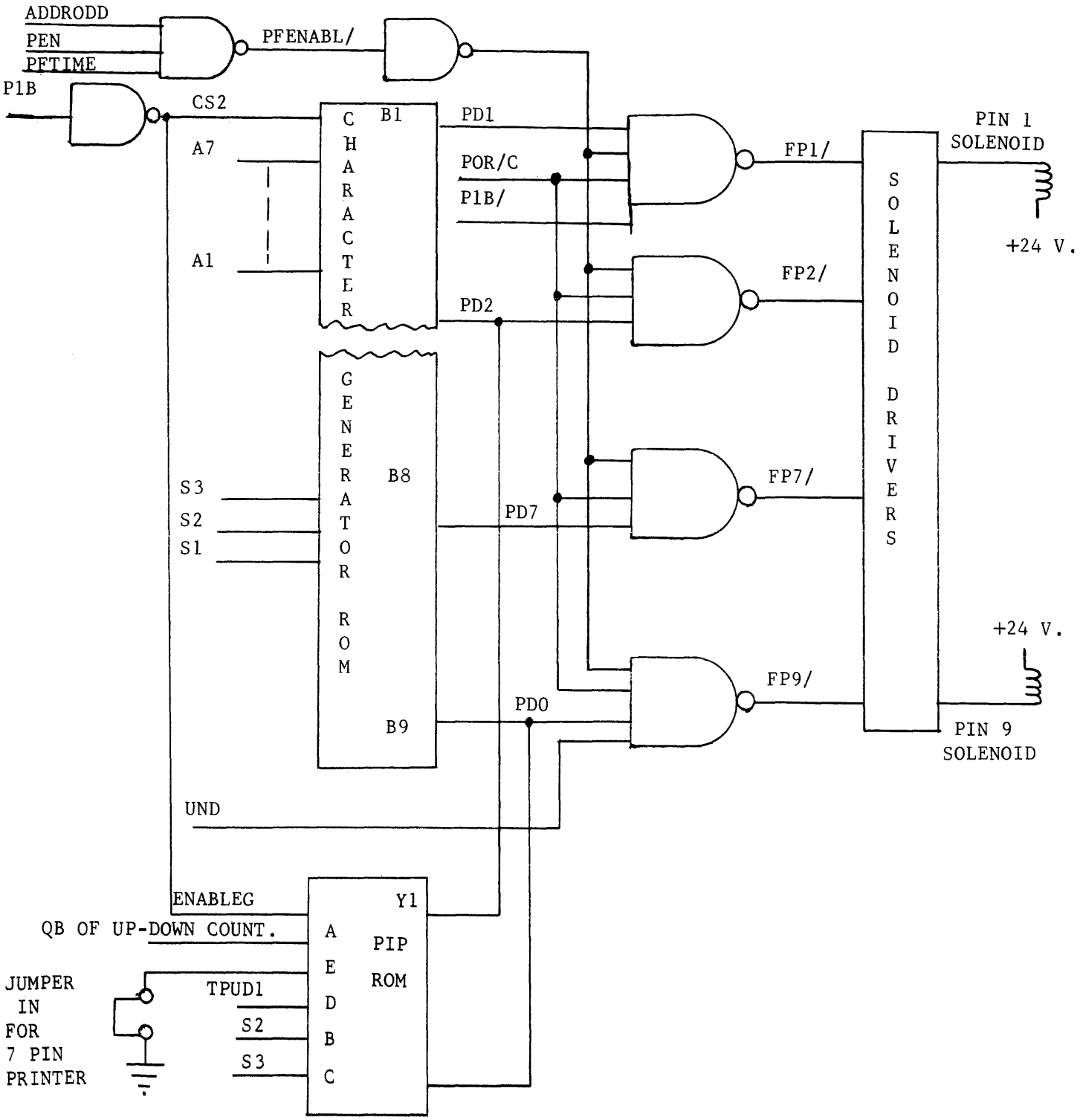


FIG. IIC-133 PRINT FIRE ENABLE GATING & PIP LOGIC

The PIB ROM outputs the compacted period or comma by action of the UP-DOWN counter which counts the TPUD1, S2 and S3 scanning address lines.

The actual addressing of the PIB ROM as well as the firing of the pins in the print head (PFENABL/) must occur sooner than during printing of a non PIB character. This is required to position the PIB punctuation between two characters. The PIB ROM is addressed sooner than the character generator by the preset loaded into the UP-DOWN counter.

The TPU Micro-processor monitors the R+S CAPRO (Real or Simulated Capro) signal via it's RQST multiplexer. The TPU uses this signal to determine when to load the printable character to the printer port. During normal character print, printing occurs on the negative excursion of the CAPRO signal as shown in Fig. IIC-131. Notice that pin firing occurs on the odd PPRO pulses as a result of ADDRODD such that the seventh or last pin fire for a normal character occurs on the 13th PPRO pulse. To position the PIB punctuation in the detent position (between characters) the TPU Micro-processor requires that pin fire for the PIB occur on the positive transition of the CAPRO signal on two even PPRO pulses. To enable the proper positioning of the PIB punctuation the CAPRO signal must make its transition from low to high sooner, or must be simulated five milliseconds before the actual transition occurs. This 5 millisecond acceleration of CAPRO is required so the TPU Micro processor can decode the PIB (0/1) code and write the PIB function to the printer port. The UP-DOWN counter is preset, the PIB Rom is scanned and PFENABL/ allows the PIB character to be printed on the next two even PPRO pulses (16 and 18) as shown in Fig. IIC-132.

The CAPRO simulator logic is located on the Timing/Ribbon Driver P.C. card and consists of 1 four bit counter chip and associated logic as shown in Fig. IIC-131. The CAPRO simulator functions as follows. PO, CET, and MR are held high (+5V) all the time. CAPRO/ on the PE/ input controls the preset into the counter. When CAPRO is high, PE/ goes low presetting 1000 into the counter. CAPRO goes low and PPROEDG/ clocks the four bit counter. 14 PPROEDG/ pulses are counted, on the next PPROEDG/ TC goes high. TC/ and CAPRO/ are gated to produce the simulated high transition of CAPRO 5 milliseconds before the actual transition of CAPRO. The next two PPROEDG/ pulses after the simulated CAPRO cause the PIB punctuation to print.

PRINT SOLENOID FIRING

Figure IIC-133 illustrates the output enable gating used to cause pin firing to occur during printing. PFENABL/ (Print Firing Enable) is generated on the Carrier Tachometer P.C. card and consists of ADDRODD (Address Odd), PEN (Print Enable) and PFTIME (Print Firing Time). ADDRODD consists of an exclusive OR of CRGR and QA of the UP-DOWN counter. There are a total of 14 PPRO pulse possible between CAPRO pulses due to the physical construction of the Carrier Readout assembly. These 14 PPRO pulses define the print positions of the non PIB characters.

Since there are 14 PPRO pulses for each print position, and since there are only seven horizontal print positions, ADDROD insures that the pin printer solenoids fire only seven times on the odd PPRO pulses. PEN is a function of the TPU micro-processor via the flags port indicating that printing is now enabled. PFTIME is a function of the Carrier Tachometer logic indicating the carrier is up to speed and positioned properly for printing. All condition being met by these signals, PFENABL/ goes low enabling the PD1-PD9 character generator ROM print driver lines to fire their respective pins through the solenoid drivers as directed by the character generator ROM output codes.

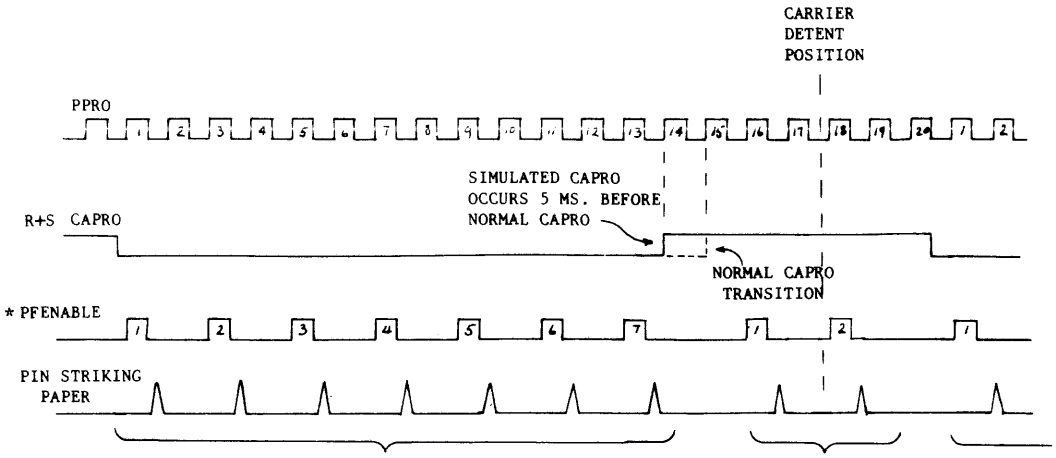


FIG. IIC-132 PIB PRINT POSITION TIMING

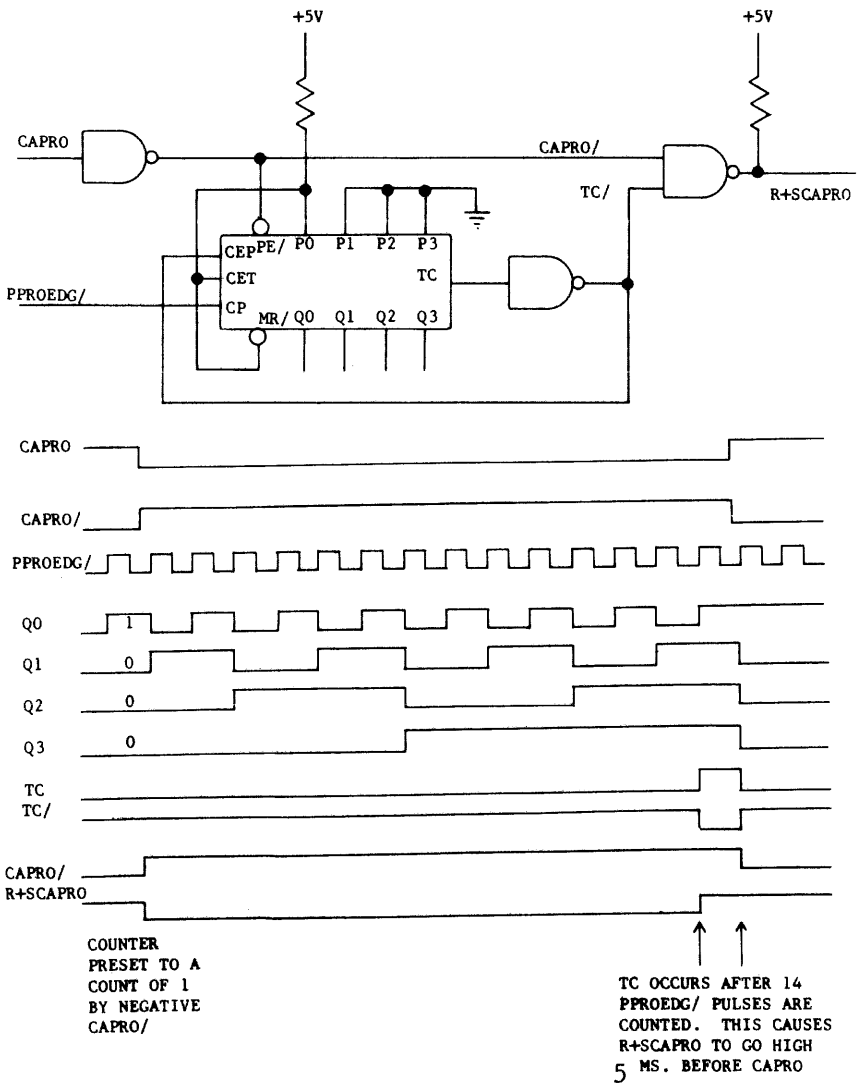


FIG. IIC-133 CAPRO SIMULATION FOR PIB

PRINT HEAD ENGAGEMENT AND RETRACTION

Print head engagement is a mechanical printer function. The print head, if retracted, will engage when the insert/retract solenoid (L4) is activated prior to printing. Activation of the insert/retract solenoid rotates the print shaft 180° to position cam A as shown in Fig. IIC- 134 allowing the spring loaded printer sled to engage print head for printing. Note that the only function of the print shaft in the L9000 is to engage or retract the print head. This shaft does not rotate during printing as with ball printers.

Print head retraction occurs when the insert/retract solenoid picks with the head engaged. The print shaft now rotates cam A 180° so it's away from the platten. This allows the printed characters to be read by the operator.

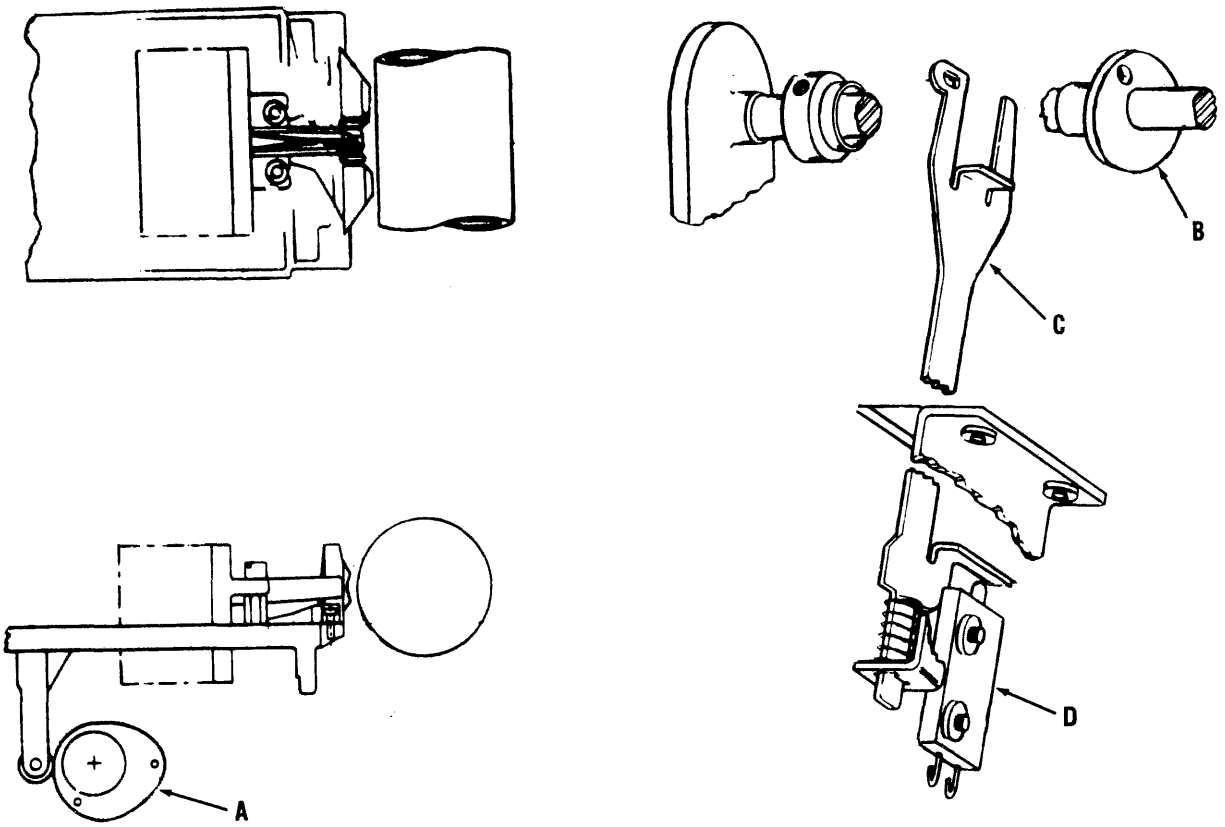
The state of the print head (engaged or retracted) is controlled by state switch D, Fig. IIC- 134. When the print head is engaged cam B on the print shaft pushes down slide C making state switch D. With the print head retracted, state switch D is open. The TPU Micro-processor monitors the state of the print head via the condition of the state switch. When printing is to occur, the TPU Micro-processor interrogates the condition of the state switch via the RQST line. If the print head is retracted (state switch open) the TPU Micro-processor will cause the insert/retract solenoid to pick engaging the head. The state switch is wired to the RQST multiplexer as the HDENG input which the TPU Micro-processor interrogates at PORT address 11.

After printing occurs, the TPU Micro-processor interrogates the RTRCTIM/ input of the RQST multiplexer at port address 12. When RTRCTIM/ goes low, the TPU will pick the insert/retract solenoid retracting the head. RTRCTIM/ is generated on the Character Generator PC card. The logic used is shown in Fig. IIC- 135. Two 4-bit binary counters are cascaded and will count FTUFF (Forms Timing Unit Flip-flop) pulses when the MR/ inputs to the counters go high. This occurs when either PCFIDLE occurs from the TPU or ILC/KB (Initiate Load Keyboard) occurs. Under either of these conditions, no printing is possible so the head is retracted. The outputs of the counters are gated together to generate the RTRCTIM/ signal. Jumpers are provided to delay the RTRCTIM signal from .6 seconds to 6 seconds. The jumper shown enabled provides a nominal delay of approximately 1.6 seconds.

MOTOR OFF TIMER

The same timer logic is used for the Motor Off timer option (if used, remove jumper to ground on MOFFTIM) with the addition of control logic required to turn the printer motor off when desired.

MOFFTIM is multiplexed to generate the TPU RQST signal at port address 14 to enable the TPU Micro-processor to turn the motor off.



PRINT HEAD ENGAGED

STATE SWITCH
DETERMINES IF
HEAD IS ENGAGED
OR
RETRACTED

FIG. IIC-134 PRINT HEAD ENGAGE/RETRACT MECHANICS

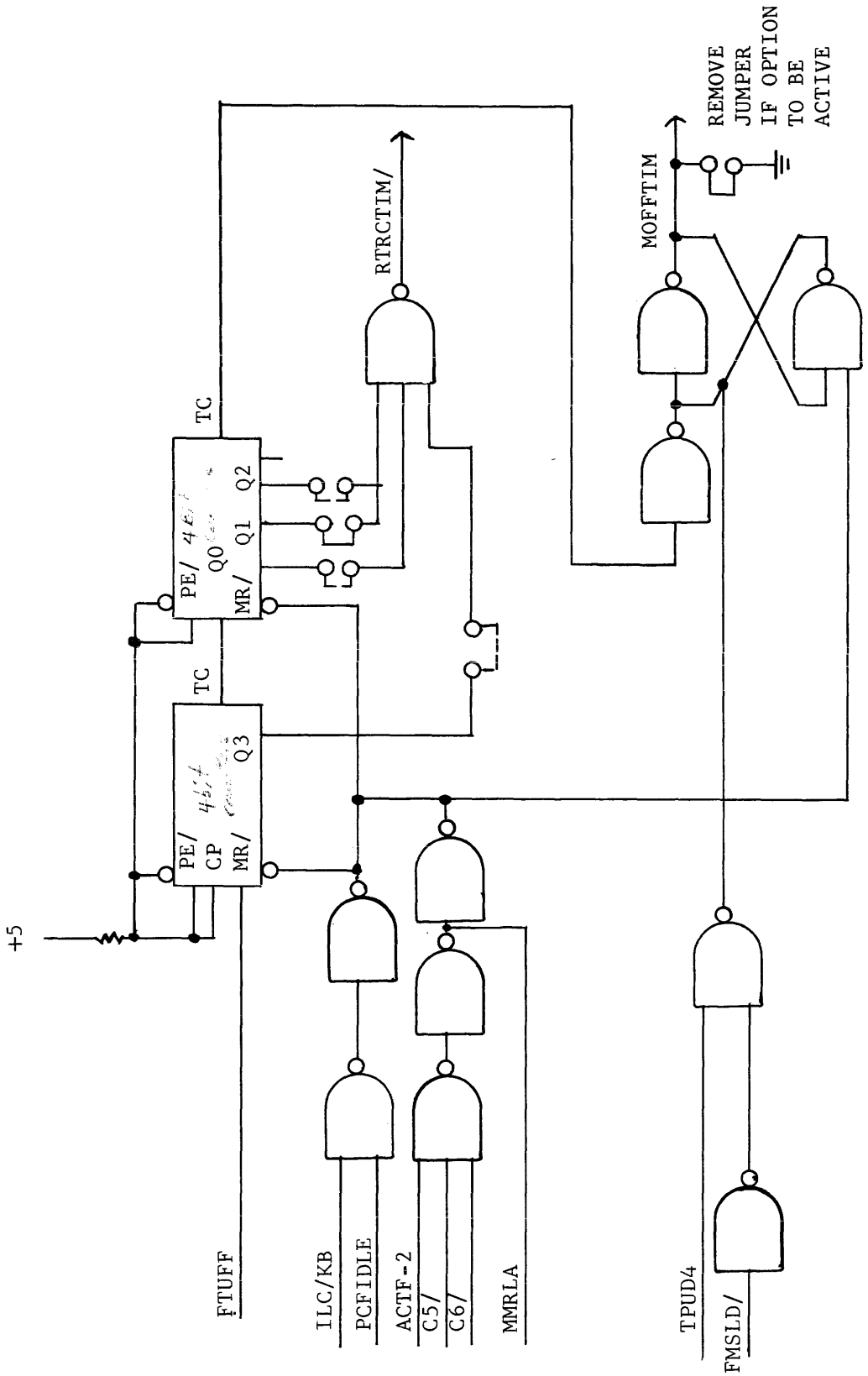


FIG. IIC-135 HEAD RETRACT TIMER LOGIC & MOTOR OFF TIMER LOGIC

CARRIER PORT

The Carrier Port is located on the Carrier Tachometer PC card and consists of two 4-bit shift registers. The signal CARRLD/ loads TPU data bits 1-8 into the carrier port upon the TPU generated PORT 2 address and the WRITE signal. CARRLD/ is generated on the Timing/Ribbon Driver PC card. The TPUD1-D8 signals once loaded into the carrier port perform the carrier functions shown below.

Carrier (Port 2) Input From TPU	Carrier Port Signals	Carrier Port Functions
TPUD1	Q3/ CRHICUR/	L ENABLES HIGH CURRENT TO CARRIER MOTOR
	Q3 HOLDDR	H PICKS HOLD SOLENOID
TPUD2	UND (9 PIN PRINTER ONLY)	H ENABLES PIN SOLENOID 9 FOR UNDERLINE
TPUD3	TP	TEST POINT
TPUD4	INTPDR	H PICKS INTERPOSER SOL.
TPUD5	POFF	H MACHINE GOES TO STANDBY
TPUD6	CRGR	H CARRIER GO RIGHT
TPUD7	CRHS	H CARRIER HIGH SPEED
TPUD8	CRGO	H ENABLES CARRIER TO GO

CARRIER READOUT WHEEL

The carrier readout wheel mounted on the end of the carrier motor consists of two sets of timing windows used to control carrier positioning and print timing in relation to carrier positioning. Fig. IIC-136 illustrates a 30° segment of the carrier readout which corresponds to one character position of the 60 CPS printer. The carrier readout wheel contains 240 print position windows equally spaced around the outer periphery of the wheel. Along the inner periphery of the wheel are 12 longer carrier position windows. The arrangements of the two sets of windows are such that for every 20 print position windows one carrier position window will occur. As seen in Fig. IIC-136 one character position (30° rotation) is defined by 20 print position windows. Fourteen of the print position windows define the print area of one character, and the remaining six, which occur during the carrier position window, define the spacing between characters and the detent position.

Besides defining print position, the 240 print position windows are also used by the Optical Tachometer logic as a feed back for determining whether the carrier speed is under or over a predetermined reference.

The print position windows and the carrier position windows are counted through the use of a 2-separate LED and photo-transistor assemblies which are mounted on the carrier readout wheel. The output of the photo-transistor transistors are routed to separate amplifier circuits on the 60 CPS Solenoid Driver PC card to produce the PPRO (Print Position Read Out) and CAPRO (Carrier Position Read Out) signals. PPRO and CAPRO are shown in Fig. IIC-137 in relationship to the carrier readout windows and the pin firing timing used in the printing of a character.
NOTE: Printing occurs between CAPRO windows,that is, when CAPRO goes low as shown in Fig. IIC-137. During PIB character printing, printing occurs on the positive transition of CAPRO as shown in Fig. IIC-132.

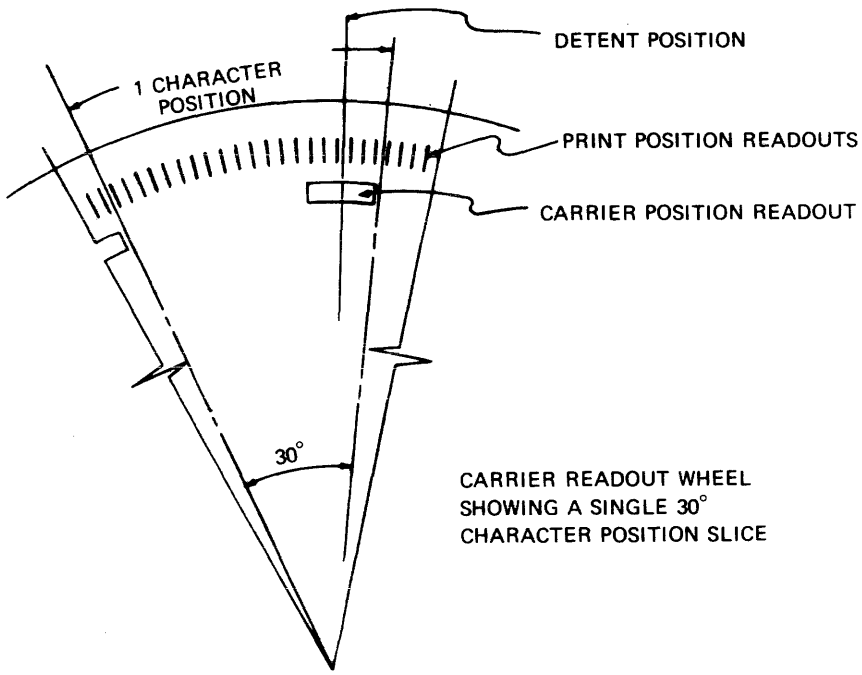


FIG. IIC-136 RELATION OF CAPRO AND PPRO ON CARRIER READOUT ASSEMBLY

Fig. IIC-137 illustrates the timing relationship between the CAPRO and PPRO pulses with the firing of the pins in the printhead.

Fig. IIC-138 illustrates the timing of the carrier port solenoids for both single and successive character print. The FTU (Forms Timing Unit) signal is shown since the TPU Micro-processor monitors the FTU timing flag to insure that loading and execution of carrier solenoid instructions occurs at the proper time.

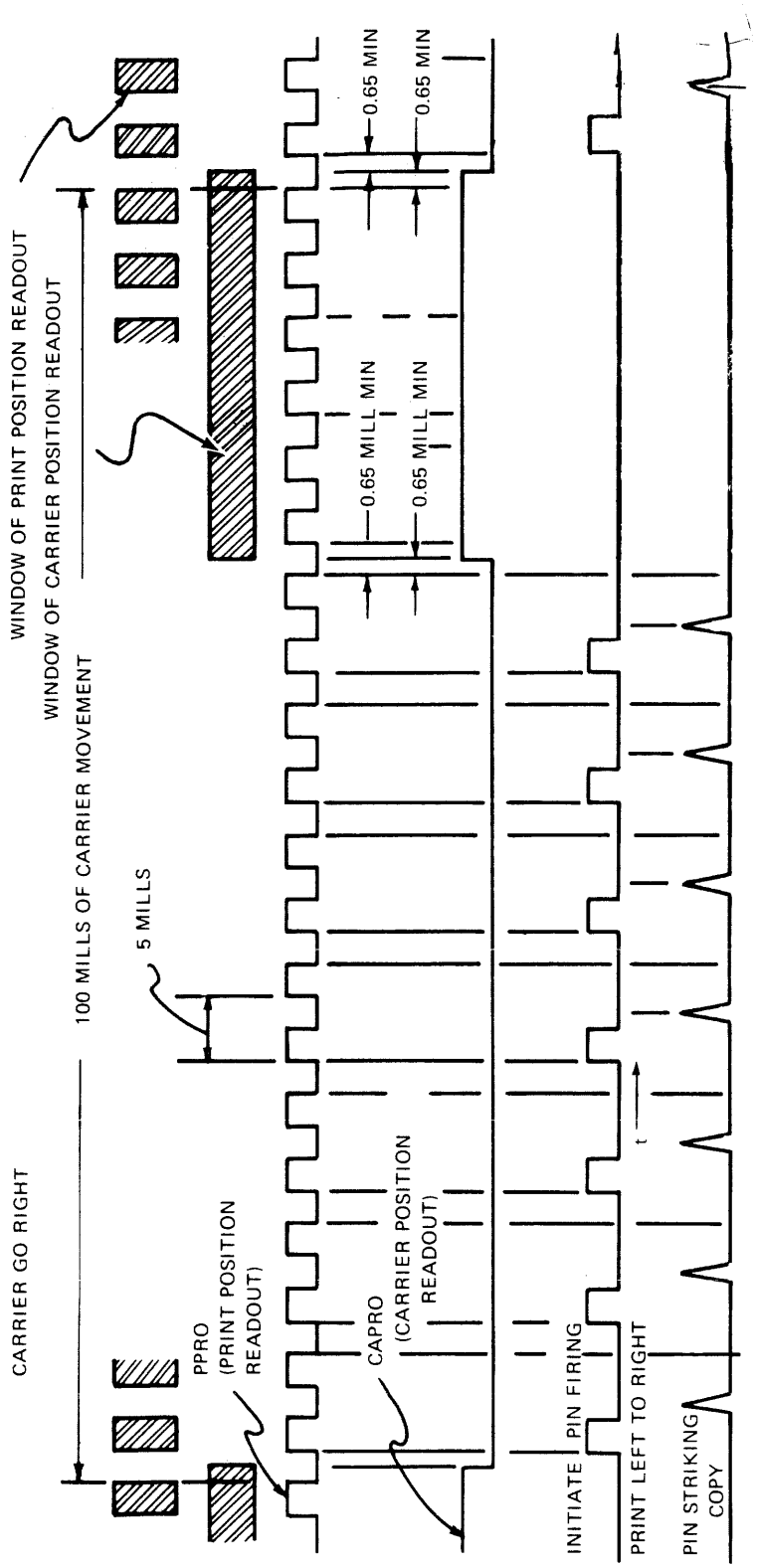


FIG. IIC-137 RELATION OF CAPRO & PPRO TO PRINTING

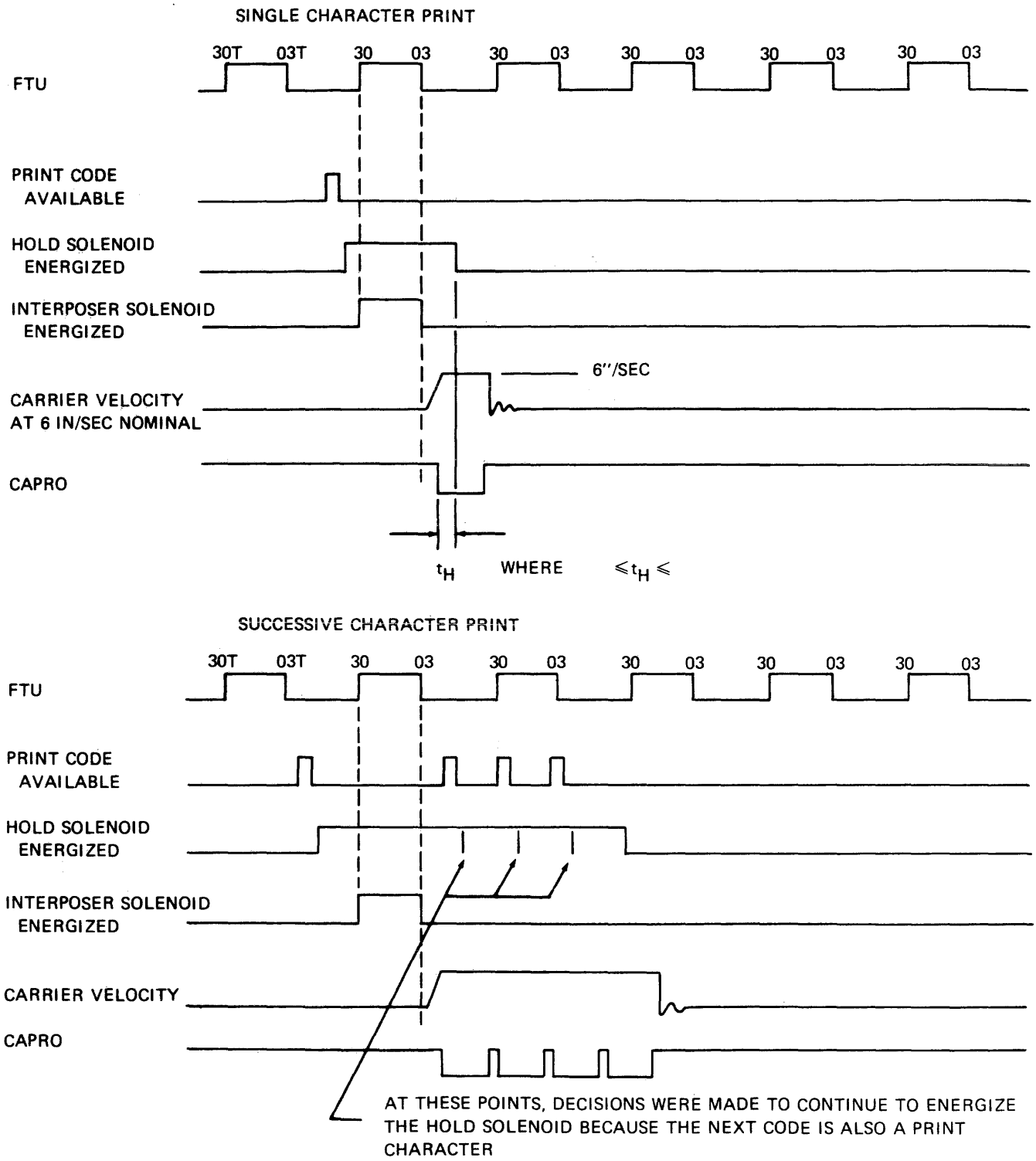


FIG. IIC-138 RELATION OF CARRIER PORT SOLENOIDS TO FTU DURING PRINTING

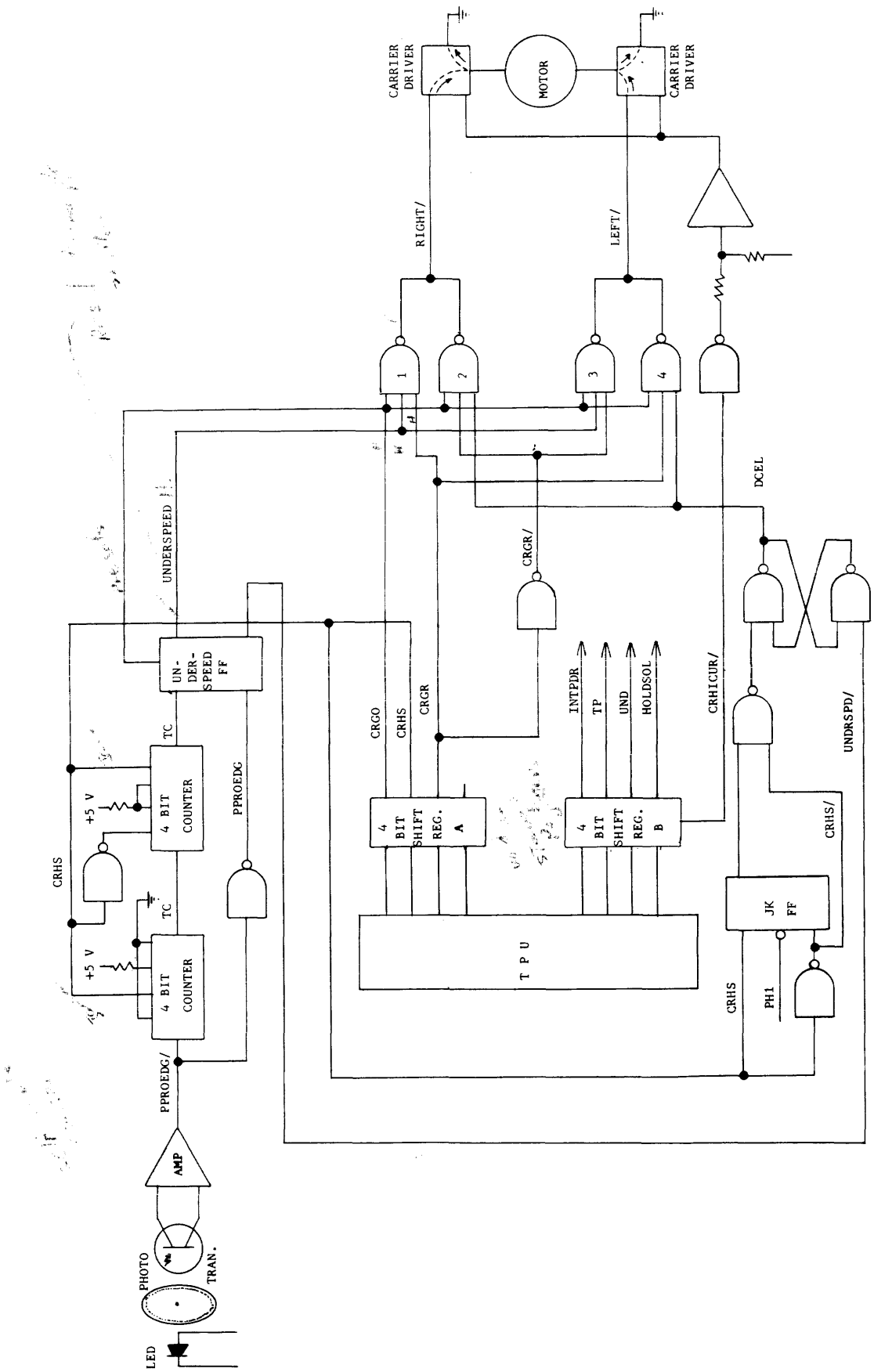


FIG. IIC-139 CARRIER CONTROL & ELECTRONIC TACHOMETER BLOCK DIAGRAM

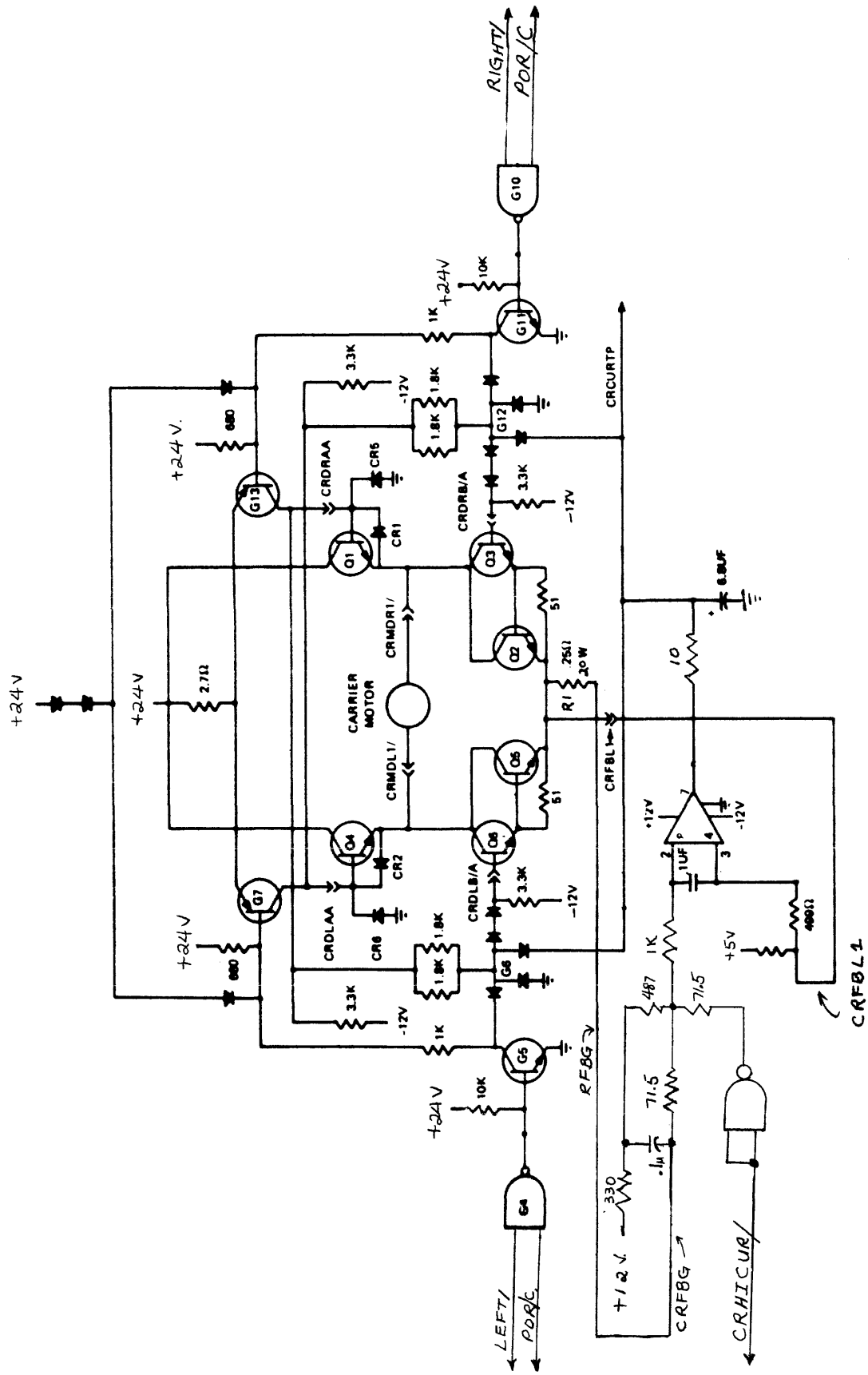


FIG. IIC-140 CARRIER MOTOR DRIVER SCHEMATIC 60 CPS L9000

60 CPS TIMING

The PH1 and PH2 clocks used by the TPU Micro-processor and associated PCF logic in the L9000 are generated on the Carrier Tachometer P.C. card. As shown in Fig. IIC-141 the basic processor clock, P, clocks a JK Flip flops whose inputs are permanently wired to +5V. P is a symetrical clock 3 us. long which causes the outputs of the Flip-flop to compliment on alternate P clock pulses. The outputs of the Flip-flop are gated with P to produce the PH1/ and PH2/ clocks as shown in the timing diagram in Fig. IIC-141.

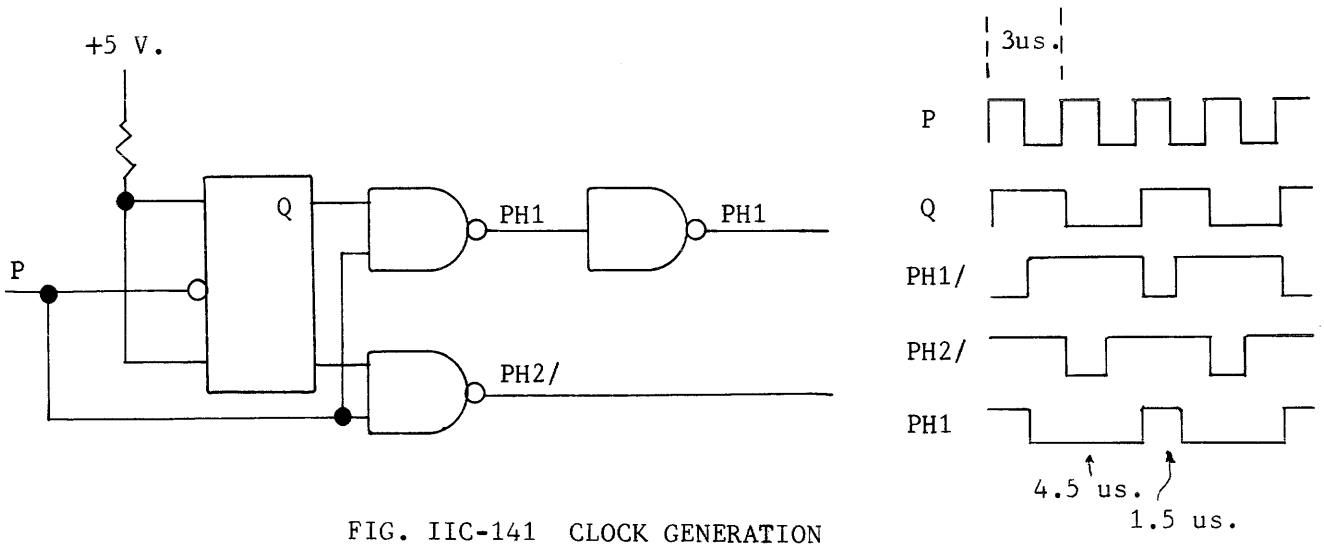


FIG. IIC-141 CLOCK GENERATION

FORMS TIMING UNIT TIMING

The Forms Timing Unit consists of a lamp and photo-transistor assembly with a rotating flag between driven off the jackshaft. The signal FTUC from the collector of the photo-transistor is amplified and inverted on the Clock Generator P.C. card to form FTU/. FTU/ is a symetrical square wave with a period of 50 ms. for one cycle as determined by the construction of the flag assembly and the speed of rotation of the flag.

FTU/ is synchronized with the PH1 clock on the Timing/Ribbon Driver P.C. card through a D-type Flip-flop with PH1/ as the clock pulse. Refer to Fig. IIC-142.

The output of this Flip-flop is inverted and appears as FTUFF. FTUFF is an input to the RQST Multiplexer on the PCF Control P.C. card and its condition will be monitored by the TPU at PORT9. FTUFF is also used on the Character Generator P.C. card to clock the Retract Timer logic which generates the RTRCTIM/ pulse to retract the print head in the absence of printing. FTUFF also controls the motor off time if this option is used.

FTU/, after syncronization with PH1/through one D-type Flip-flop, is delayed by 12 us. through the use of two more D-type Flip-flops. Each Flip-flop is clocked by PH1/ which has a period of 6 us. The output of the second Flip-flop (FTU delayed by 12 us.) is inverted and gated with FTUFF to produce the signal T30. T30 is a 12 us. wide positive pulse which is used by the APR logic on the Decode/Misc P.C. card.

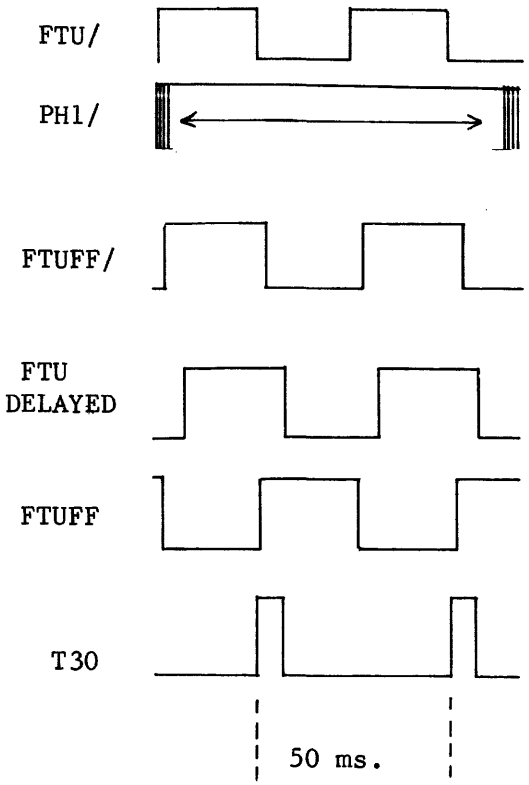


FIG. IIC-142 FTU & T30 GENERATION

GLOSSARY

ALARMDR/	Alarm Driver
ALARMSOL	Alarm Solenoid
CAPRO	Carrier Position Readout
CAPROC	Carrier Position Readout
CAPROC	Carrier Position Readout Collector
CAPROE	Carrier Position Readout Emitter
CAPROG	Carrier Position Readout Ground
CARRLD/	Carrier Load
CER	Carrier Error
CGEOPN	Carriage Open
CLODR	Close Driver
CLOSOL	Close Solenoid
CRDLA	Carrier Drive Left A
CRDLB/	Carrier Drive Left B/
CRDLC/	Carrier Drive Left C/
CRDRA	Carrier Drive Right A
CRDRB/	Carrier Drive Right B/
CRDRC/	Carrier Drive Left C/
CRFBG	Carrier Feed Back Ground
CRFBL1	Carrier Feed Back Level 1
CRFBL2.	Carrier Feed Back Level 2
CRGR	Carrier Go Right
CRH1CUR/	Carrier High Current/
CTL	Control Line to TPU

DCEL	Decelerate (Carrier)
DIR	Direct Line to TPU
FLGSLD/	Flags Load
FMSLD/	Forms Load
FP1/-FP9/	Fire Pin 1 - Fire Pin 9
FTU	Forms Timing Unit
FTUC	Forms Timing Unit Collector
FTUFF	Forms Timing Unit Flip-flop
FTULAMP	Forms Timing Unit Lamp
HDENG	Head Engaged
HDENGSW	Head Engage Switch
INTPSOL	Interposer Solenoid
INTRPT/	Interrupt Line to TPU (Not Used)
IOX	Input Output Exchange (TPU)
LEFT/	Left Carrier
MOFFTIM	Motor Off Timer Output
MONDR	Motor On Driver
O/CKY	Open/Close Key
ODC	Output Dump Command
OEXT	Output Extend
P	Basic PCF Clock
PAD0/	Page Address 0 Selects TPU ROM
PAD1/	Page Address 1 Selects TPU ROM
PCFBUSY	Printer Carrier Forms Busy
PCFIDLE	Printer Carrier Forms Idle
PEN	Printing Enabled
PFENABL/	Print Fire Enable
PH1	Phase 1 Clock
PH2	Phase 2 Clock
PIB	Print In Between
PPRO	Print Position Read Out
PPROC	Print Position Read Out Collector
PPROEDG/	Print Position Readout Edge
PPROG	Print Position Readout Ground
PORT1-PORT5	TPU PCF PORTS 1-5
PRTRLD	Printer Load
RB1A-RB1B	Ribbon Motor Phase 1 Driver
RB2A-RB2B	Ribbon Motor Phase 2 Driver
RIGHT/	Right Carrier
ROM0/-ROMB/	TPU ROM Output Lines
RQST	Request Line to TPU
R+SCAPRO	Real or Simulated Carrier Position Readout
RTRCTIM/	Retract Timer Output
TPUD1-TPUD8	TPU Data Lines 1-8
WRITE	TPU Write Line
XAD0-XAD3	TPU Address Lines

CARRIER CONTROL

The 60 CPS L9000 Carrier Control is contained on the Carrier Tachometer P.C. card. The Carrier Driver P.C. card contains the carrier driver logic. Fig. IIC-139 illustrates a simplified block diagram of the logic control used for the carrier. The upper portion of the diagram shows the electronic tachometer. The TPU and the carrier port are shown as they relate to generation of the carrier control signals.

Prior to a print operation or a carrier excursion the TPU Micro-processor, under ROM firmware control, loads the carrier port consisting of shift register A and B by the CARLD/signal. The outputs from the carrier port are the required carrier control signals for the carrier excursion. The signal CRHS is a preset input to the two 4 bit counter chips which form the electronic tachometer. The gating of the TPU output signals produce the drive signals RIGHT/ and LEFT/.

The carrier control functions as follows, assuming the TPU causes right carrier movement. The TPU ROM program causes the TPU to output the signals hold solenoid, interposer, carrier high speed,carrier go right and carrier go. This causes the output of gates 1 and 2 to give a low active RIGHT/ to the motor drive circuit. The inversion of the HOLDDR signal is CRHICUR/ which modifies the carrier drive logic causing immediate carrier drive after the interposer solenoid pulls down the detents. CRHICUR/ is required to get the carrier up to speed to print the first character.

The first PPROEDG signal from the read out disk as the carrier starts to move is used to preset the two four bit counters in the electronic tachometer to the value created by the signal CRHS and the permanently wired inputs, which is 0110 0111. The signal CRGO directly sets the Underspeed Flip-flop which enables gate 1. CRGR is high and along with CRGO and the Underspeed Flip-flop causes RIGHT/ to go low activating the carrier motor drivers to cause right carrier movement. If the second and consecutive PPROEDG do not occur before the terminal count, the carrier is not up to speed and TC goes high to keep the drive on.

However, when the carrier is up to speed or above, the PPROEDG will occur before TC. This signal is inverted, and resets the Underspeed Flip-flop and via gate 1 shuts off the drive. When the carrier speed falls, TC will occur before the next PPROEDG signal presets the counter causing the Underspeed Flip-flop to set turning the drive back on.

When the carrier is 5 positions from home the TPU lowers the CRHS signal causing a low pulse out of JK flip flop G and its associated TTL gate. This in turn sets the cross coupled latch to generate DCEL which through gate 4 and CRGR going low produces a LEFT/ drive signal to brake the motor.

Under control of the TPU a low speed drive right is then initiated. The counter now counts up from a value of 0010 1110 to produce TC to control the speed as before at position 0. The TPU Rom program de-energises the hold solenoids and after a 50 msec delay, turns off the CRGO signal causing the carrier to coast into the detents.

The same sequence applies for left travel and in slow speed when printing.

Fig. IIC-140 illustrates the carrier motor driver logic located on the Carrier Driver P.C. card. The signals RIGHT/, LEFT/, and CRHICUR/ are generated on the Carrier Electronic Tachometer P.C. card as previously discussed.