B 1800/B 1700

DISK PACK CONTROL II

TECHNICAL MANUAL

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INTRODUCTION

The B 1800/B 1700 Disk Pack Control II (DPC-II) is part of the B 1800/B 1700 Disk Pack Subsystem. This subsystem also includes a disk pack electronics controller (DPEC) and one to eight disk pack drives (DPD), as diagrammed in figure 1-1.

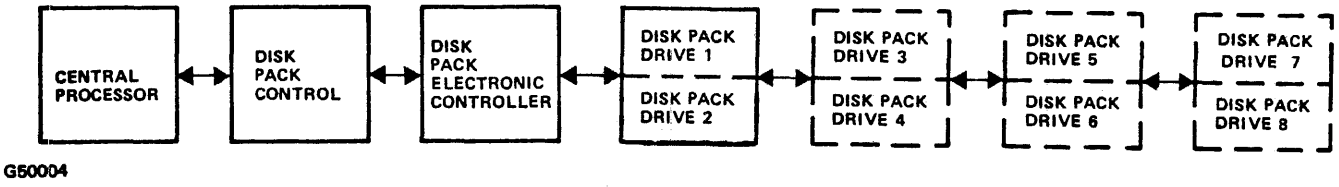

Figure 1-1. Disk Pack Subsystem

DISK PACK CONTROL II

GENERAL INFORMATION

The B 1800/B 1700 Disk Pack Control II consists of two B 1700-size logic cards. These logic cards must be installed in a two-card location in an I/O base or I/O base extension.

The DPC-II performs the following functions:

a. Provides an interface between the central processor and the DPEC

b. Provides data storage for three sectors of disk pack information

c. Decodes and interprets the operation (OP) code from the central processor to the DPEC

d. Assembles a result descriptor based on information received from the DPEC

The DPC-II receives the I/O descriptor operators that are fetched by the I/O driver from main memory, interprets the operation specified by the descriptor operator and its variants, and initiates the required action in the DPEC. At the completion of the operation, the DPC generates a result descriptor using information received from the DPEC. The I/O driver stores the result descriptor in the result status (RS) field of the I/O descriptor. The I/O driver also returns an interrupt message if requested.

I/O DESCRIPTOR

The I/O descriptor consists of seven 24-bit fields as shown in figure 1-2. The following is a detailed description of the functions and usage of each field.

E	ENDING ADDRESS.
RS	RESULT STATUS (ALSO LOCATION OF RESULT DESCRIPTOR).
L	LINK ADDRESS.
OP	OP, VARIANTS AND UNIT NUMBER.
A	START ADDRESS OF DATA
B	END PLUS ONE, ADDRESS OF DATA.
C	START ADDRESS OF DATA(FILE ADDRESS).

G50005

Figure 1-2. DPC I/O Descriptor

E Field

After an operation, the I/O driver stores the final incremented A address in the E field. The address in this field points to the memory location where the next bit of data normally would be stored. For read, write, and search operations, the E field address is normally equal to the B address unless the operation is terminated because of a "not-ready", address error, time-out, command transmission error, write lock-out (write operation only), or the end of the search table or entry (search operation only). The E field is not defined after a test operation or stop operation.

During some operations, the E field is used by the I/O driver to save the incremented A address between buffer loads to the DPC.

RS Field

After completion of an operation and after the actual ending address has been stored in the E field, the I/O driver exchanges the result status information in the result status field with the interrupt control information.

Prior to and during an operation, the first 15 bits of the RS field are used to store temporary flags for the I/O driver. The last nine bits are used to indicate dynamic interrupt information.

L Field

After storing the result status information and after returning any requested interrupt message, the I/O driver normally fetches the Link address from the L field. The Link address is a 24-bit address pointing to the RS field of the next I/O descriptor to be executed.

OP Code, Variant(s) and Unit Number

The OP code, variant(s) and unit number are contained in a 24-bit field. The leftmost three bits are used to designate the majority of operator codes; the rightmost four bits are used to designate the unit. (Operator codes extending beyond three bits are indicated by 111 in the first three bit positions.) The remaining bits are then used for variants (explained under the description of the individual operators). All bits remaining unassigned are reserved bits; they must be zeros.

A and B Fields

For most operators, the A and B fields are 24-bit fields containing the beginning and ending memory bit addresses, respectively, for a given operation. These addresses normally define the number of bits to be transferred. If the value in A equals the value in B, no data is transferred. For the Test descriptor, the A-field and B-field addresses are not used.

C Field (File Address)

The File Address, a binary sequential address contained in a 24-bit field, is used to designate a particular sector on a disk pack as the starting point for all operations except Test and Stop.

For full-capacity type 225 disk pack drives, the maximum binary file address is 485,169 corresponding to a maximum capacity of 87,330,600 eight-bit bytes for each removable disk pack. For half-capacity type 225 disk pack drives, the corresponding figures are 242,584, and 43,665,300 bytes, respectively. The disk cartridge track format for a type 225 disk drive is shown in figure 1-3.

For type 206 disk pack drives, the maximum binary file address is 362,229, corresponding to a maximum capacity of 65,201,400 eight-bit bytes per removable disk pack. For half-capacity type 206 (type 205) disk pack drives, the corresponding figures are 181,114, and 32,600,700 bytes, respectively. The disk cartridge track format for a type 206 disk drive is shown in figure 1-4.

For type 225 disk drives, the binary sequential file address corresponds to contiguous or adjacent sectors (excluding spares and sectors which have been relocated) that begin on head 0, cylinder 0 and continue through the pack by head and cylinder (in that order). On each surface (except the first) there are sixty sectors. The order of the sectors following index is 0, 1, 2, ..., 57, 58, 59. On the first surface (head 0) five spare sectors occupy the positions normally occupied by sectors 55 through 59. These spare sectors are not addressable in the address continuum (unless they have been assigned by relocation).

For type 206 disk drives, the binary sequential file address corresponds to interlaced sectors (excluding spares and sectors which have been relocated) that begin on head 0, cylinder 0 and continue through the pack by head and cylinder (in that order). On each surface except the fifth one, there are 90 sectors. The order of the sectors following index is 45, 0, 46, 1, 47, 2, ..., 89, 44. On the fifth surface (head 4) five spare sectors occupy the position normally occupied by sectors 85 through 89. These spare sectors are not addressable in the address continuum (unless they have been assigned by relocation).

For type 205/206 disk drives, a reserved cylinder is used for maintenance purposes. Sectors on this reserved cylinder are addressed with addresses 362,230 through 362,679.

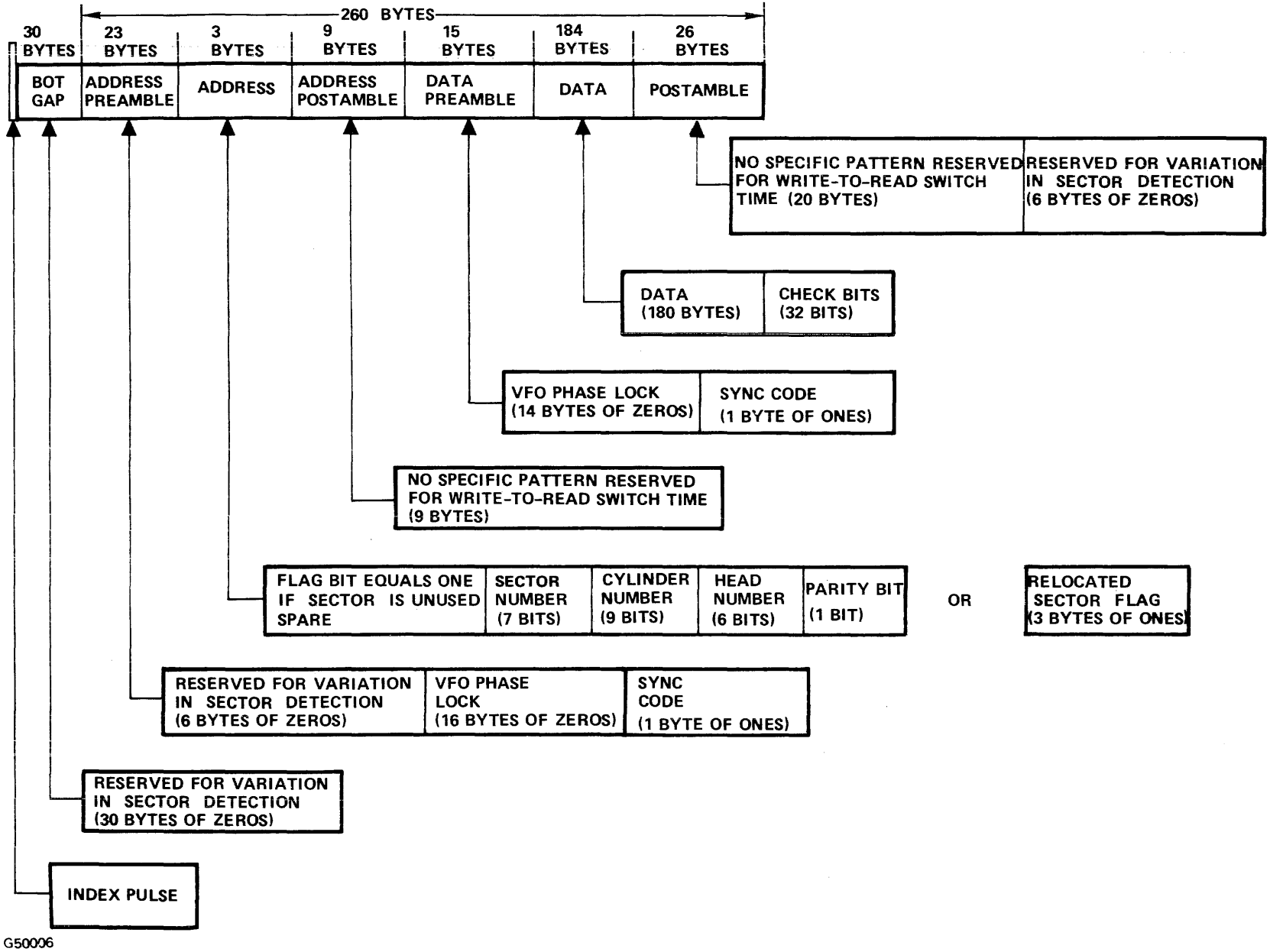

Figure 1-3. Type 225 Disk Pack Track Format

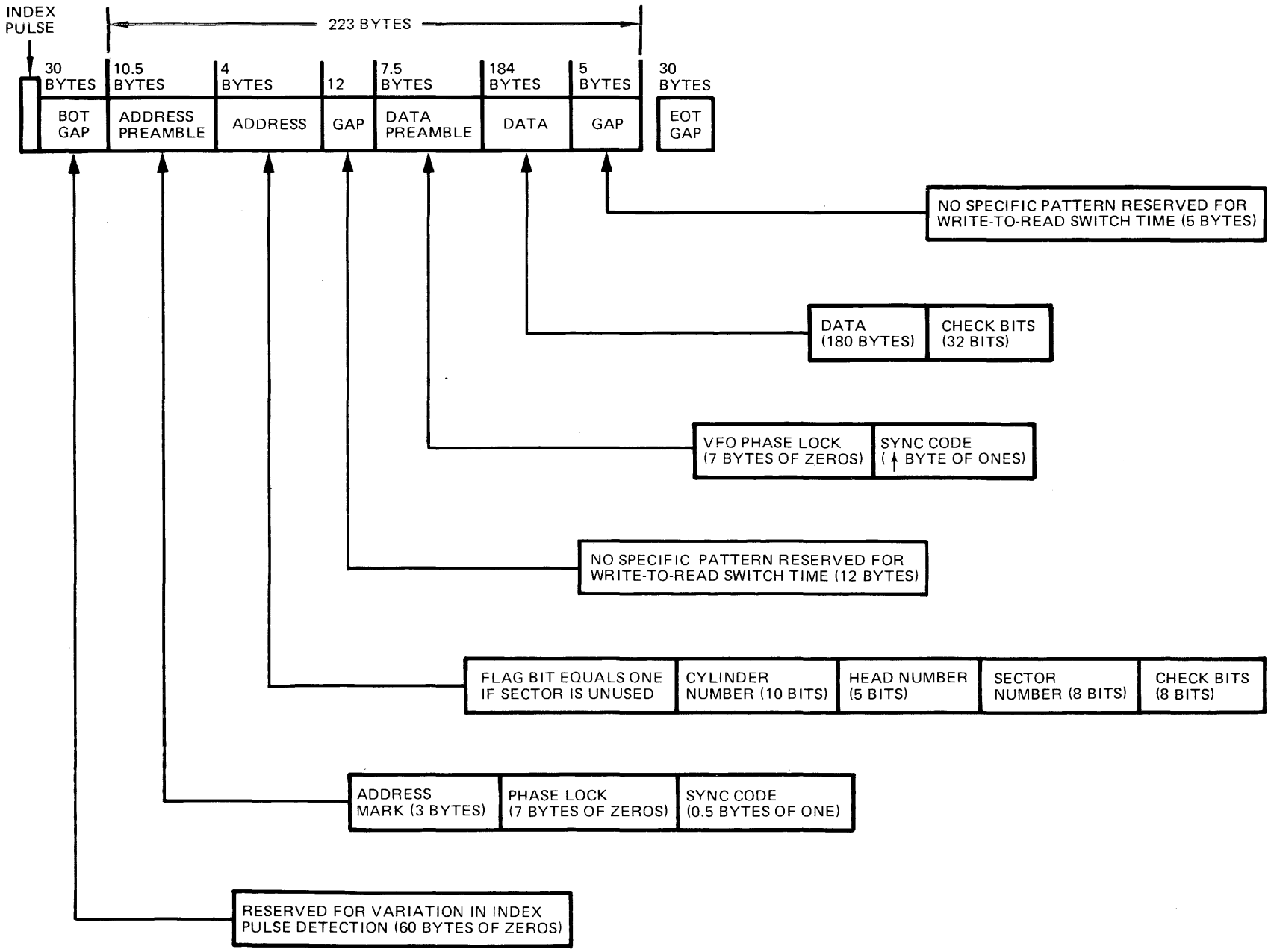

Figure 1-4. Type 206 Disk Pack Track Format

I/O OPERATORS

The following are all I/O operators for DPC-II:

a. Read

b. Write

c. Initialize

d. Relocate

e. Test

f. Pause

g. Stop

Each I/O operator consists of a 24-bit field. The first three-bit positions (leftmost three-bit positions as displayed on the console) are reserved for the type of operation. The last four-bit positions are reserved for unit number; remaining positions are reserved for variants.

Read Operator

The read operator (refer to figure 1-5) provides the capability to read data from the disk pack, starting at the given file address (C field), into ascending memory locations that begin at the location specified by the A address and end at the location specified by the B address (minus one). A complete segment does not need to be stored but can be parity-checked. The DPEC transmits a total of 90 sixteen-bit data words and two error-code words to the DPC for each sector read. In addition, one 16-bit result status word reflecting the accumulation status of the entire operation up to that point is transmitted immediately following error-code words for each sector. Only data bits are stored, unless otherwise specified by variant E − 1 or M = 1.

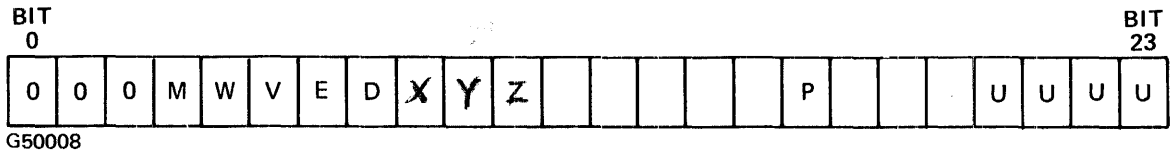

Figure 1-5. Read Operator

Functions of the Read operator variants follow:

Variant	Control Function
MEDP = 0E00	Read data as described under "Read Operator," above. The Read operator and VXYZ variants are sent to the DPEC. VXYZ variants are decoded as follows:
	VXYZ = 0000 — Normal Read
	VXYZ = 10Y0 — Enable strobe; Y denotes direction, 0 = −, 1 = +, type 206 only.
	VXYZ = 0X01 — Enable offset; X denotes direction, 0 = −, 1 = +, types 206 and 225 DL2 only
	VXYZ = 1XY1 — Enable strobe and offset; XY denotes direction, type 206 only
	V = 1 — Disable automatic restore after a seek error, type 225 only
	Y = 1 — Not permitted on type 225 (See D = 1, following)
	XZ = 10 — Not defined
	VY = 01 — Not defined
MEDP = 0E01	Read data (see paragraph entitled Read Operator). The verify operator and the VXYZ variants are sent to the DPEC. XYZ equal to 000 indicates normal sectors while XYZ equal to 001 through 101 indicates the spare sector on the designated cylinder. If a spare sector is designated, only one sector is read. Designation of a spare sector is not permitted if the specified spare sector has been assigned. Variant MD must equal 00. For type 206, variant V also must equal 0. For type 225, V equal to 1 disables automatic restore after a seek error.
E = 1	Read data as described under "Read Operator," where P can be equal to 0 or 1 but, in addition to the data bits, can return the 32-bit error check code and the 16-bit result word from the DPEC for each segment read. Return the final DPC result for the operation with bits 17-22-23-24 = 0001. Variant MD must equal 00.
M = 1	Read the sync code, the address (and whenever possible) the data, the data check bits, and the postamble as recorded at the designated segment. In addition return the 16-bit result from the DPEC. If the sector is relocated, the sync code and the address field returned then contains all "ones." Neither parity error nor wrong address terminates the operation at this time. The position of the sector is obtained in the DPEC by counting from the index. All other variants except WV must equal 0. For type 206, variant V must equal 0.

Variant	Control Function
D = 1	Read extended status data from the DPEC. The DPC treats this operation identically to a read operation except for data length. Presently, data transfer from DPEC is terminated by DPEC after 64 bits occur. The data transfer from the control, if not terminated earlier by the system, is terminated after 264 bytes. The excess data is not defined. For type 225 DL2, the normal read operation (with Y equal to 1 variant) is sent to the DPEC. For type 206, the diagnostic read operation with the Y variant equal to 1 is sent to the DPEC. All other variants (except W) must equal 0. This D = 1 operation is not permitted for type 225 DL1 drive.
W = 0	Do not wait on a busy exchange. If the interface line "Exchange Busy" is true, terminate the operation and return the final result status with bits 0, 1 (with 16 equal to 110).
W = 1	Wait on busy exchange.

NOTE
There is no exchange for the disk pack subsystem at this writing.

UUUU = 0....15	Unit number (spindle).

Write Operator

The write operator (see figure 1-6) provides the capability to write data to the disk pack starting at a given file address (C field) from ascending memory locations beginning at the location specified by the A address and ending at the location specified by the B address (minus one). Zero-fill bits are written to complete the last segment. The DPC transmits to DPEC 90 sixteen-bit data words per sector. In addition, DPC sends two dummy words at the end of each sector, during which time the DPEC is writing an error code on the disk.

The functions of the Write operator variants follow:

Variants	Control Function
W = 0	Do not wait if a busy exchange condition exists. If the interface line "exchange busy" is true, terminate the operation and return the final result status with bits 0, 1, and 16 equal to 110.
W = 1	Wait if a busy exchange condition exists
V = 0	Enables automatic restore after a seek error
V = 1	Disables automatic restore after a seek error
UUUU = 0....15	Unit number (spindle)

NOTE
There is no exchange for the disk pack subsystem at the present time. Only eight spindles are permitted for each I/O control.

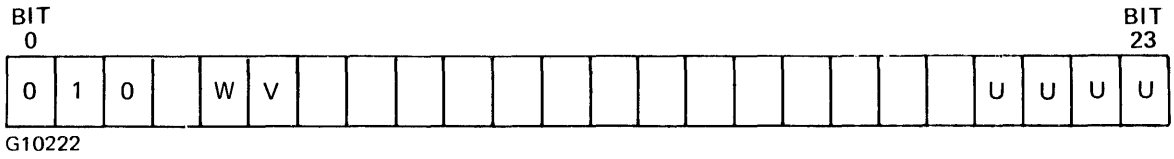

Figure 1-6. Write Operator

Initialize Operator

The Initialize operator (figure 1-7) provides the capability to write all format bits in all tracks starting after the index pulse on the track decoded from the given file address (C field) and continuing through the entire track or pack. Spare sectors are also initialized. The data pattern consists of the sync code (eight ones) and the actual sector address (repeated 45 times for each sector). The DPC treats this operation exactly as if it were a Write operation. However, the DPEC normally does not accept more than one 16-bit data transfer.

The functions of the initialize operator variants follow:

Variants	Control Function
P = 1	Initializes the entire disk pack
P = 0	Initializes one track only
V = 0	Enables automatic restore after a seek error
V = 1	Disables automatic restore after a seek error
S = 0	The data fields are written with the sync byte (8 1's). The actual sector address is repeated 45 times (type 225)
S = 0	The data fields are written with the actual sector address and EPL repeated 45 times (type 206).
S = 1	The data fields are written with the first 16 bits of data received from system repeated 90 times
UUUU = 0...15	Unit number (spindle)

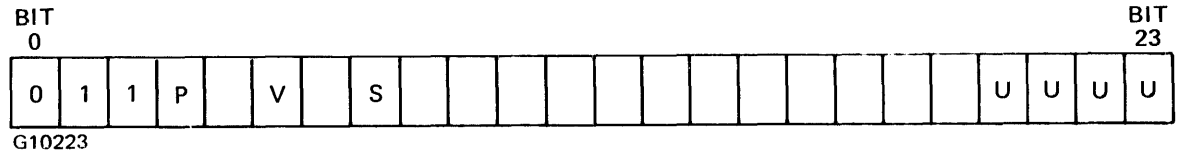

Figure 1-7. Initialize Operator

Relocate Operator

The relocate operator (see figure 1-8) provides the capability to flag the address field of the sector designated by the given file address (C field) with a relocated address flag pattern. In addition the relocate operator writes the spare sector on the track specified by NNN with the address of the relocated sector and with a data pattern. This portion consists of the sync code (eight 1's) and the sector address of the relocated sector is repeated 45 times. Both the original sector and the relocated sector are located by counting from the index; other sectors are unaffected. Spare sectors are to be allocated in reverse order, that is, N = 5 first. N = 5 designates the last physical sector on the track.

The DPC treats this operation exactly as if it were a write operation. However, the DPEC normally does not accept more than one 16-bit data transfer.

The functions of the Relocate operator follow:

Variants	Control Function
V = 0	Enables automatic restore after a control function/description seek error
V = 1	Disables automatic restore after a seek error (type 225)
S = 0	The data field is written with the sync byte (8 1's) and the sector address of the relocated sector repeated 45 times (type 225)
S = 0	The data is written with the sector address and EPL of the relocated sector requested 45 times (type 206)
S = 1	The data field is written with the first sequence of 16 data bits received from the system repeated 90 times
NNN = 1 – 5	Indicates the spare sector on the designated cylinder
UUUU = 0...15	Unit number (spindle)

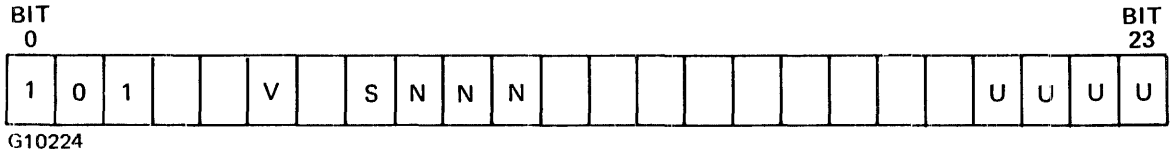

Figure 1-8. Relocate Operator

Test Operator

The test operator (see figure 1-9) examines a selected disk drive and returns a result descriptor containing the following information:

a. The "ready" status of the disk drive

b. Disk drive identification (ID)

c. Whether or not the disk drive has a write-lockout condition

d. The disk drive exchange configuration

e. Whether or not the disk drive is in a seek status

f. Whether or not the disk drive has occurred a transmission error

g. The DPC identification

h. The seek-status flip-flop state

The functions of the test operator variants follow:

Variants	Control Function
VV = 00	Return result as previously described
VV = 10	Store a result only if the disk drive is present, ready, and not seeking; otherwise unlock and fetch the next descriptor
VV = 01	Store a result only if the disk drive is not present or not ready; otherwise unlock and fetch the next descriptor
VV = 11	Undefined
R = 1	Place the disk drive off-line for disk pack removal if the drive is present and available; variant VVP must equal 000
P = 1	A pause of 1 to 2 ms is effected before a service request (SR) is returned to the I/O driver. Bit 16 of the result descriptor is suppressed. Variant VVRC must equal 0000
C = 1	Clear the seek status flip-flop
UUUU = 0...15	Unit number (spindle)

NOTE

The control determines whether or not the result can be stored in accordance with the variant bit VV. In all cases, the control returns the result immediately. If the result is to be stored, result descriptor bit 16 is equal to one. If the result is not to be stored, result descriptor bit 16 is equal to zero.

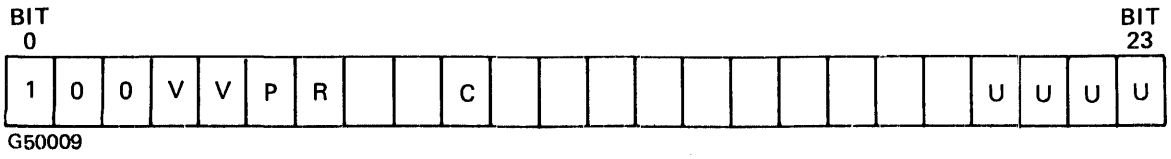

Figure 1-9. Test Operator

Pause Operator

The pause operator (see figure 1-10) provides capability for the control to pause 1 to 2 ms before a service request (SR) is returned to the system. Bit 16 of the result descriptor is suppressed to indicate that the result is not to be stored.

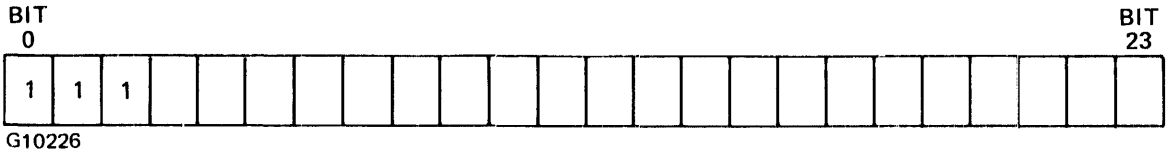

Figure 1-10. Pause Operator

Stop Operator

The stop operator (see figure 1-11) provides capability for the control to idle after returning a result. If requested, it can generate an interrupt. The stop operator is interpreted by the I/O driver and is not sent to the control.

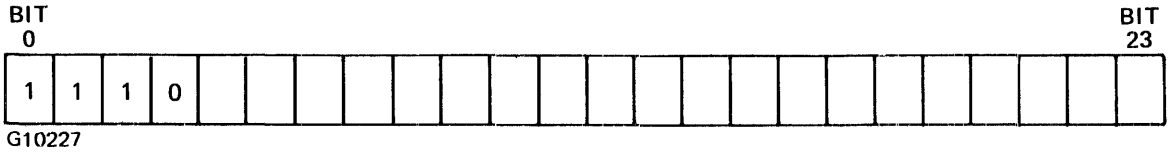

Figure 1-11. Stop Operator

RESULT STATUS (RESULT DESCRIPTOR)

The end of a disk pack operation occurs when either the DPC or the DPEC terminates. The DPEC terminates by "dropping" the ready line; the DPC terminates by "dropping" the select line. Whichever device terminates, another device also then terminates by "dropping" the applicable line. At termination, the DPEC places the 16-bit DPEC result descriptor on the information lines between the DPEC and the DPC, generating a clock pulse. The functions of the 16-bit DPEC result descriptor are listed in table 1-1.

The DPEC result descriptor is used by the DPC to produce a 24-bit result descriptor that is stored in the RS field at the completion of an operation.

The bit structure and usage of the 24-bit result descriptor used by the B 1800/B 1700 processor are listed in table 1-2 and described in following paragraphs.

Table 1-1. DPEC 16-bit Result Descriptor

Information Line (Bit)	Result Descriptor Bit Functions
0	Read data error (Fire Code error)
1	Write-lockout
2	Seek status flip-flop
3	Drive not ready (positioner not settled)
4	Drive off-line
5	Drive unsafe
6	Address parity or sync-code error
7	Sector address error
8	Seek timeout
9	Drive not present
10	Not used
11	Not used
12	Not used
13	OP complete in local (type 225 DL2 only)
14	Transmission parity error
15	Try Diagnostic routine

Operation Complete

Bit 0 and bit 16 are always set in the RS field to indicate operation complete.

In some special cases, bit 16 is suppressed in order to indicate to the I/O driver that no result is to be stored. These cases occur during:

a. Pause completion

b. Test VV = 10 and unit is not ready, seeking, or not present

c. Test VV = 01 and unit is ready

d. Read, write, or relocate operation; and unit is seeking or a seek is initiated

e. Read, write, relocate, or initiate operation; and when unit is busy and W = 0 (do not wait)

f. Read, write, or relocate operation (with the seek status flip-flop set) and when the address is indicated for another cylinder

In other types of special cases, bit 16 is suppressed and special flags are returned to indicate to the I/O driver that special action is required. In these cases, the I/O driver sets bit 16 in the RS field. The cases where special action is required are:

a. Read operation with E = 1 (special flag bits 21, 22, 23 = 001 are also returned)

b. Read, write, relocate, or initialize operation (if special flag bits 21, 22, 23 = 011 are returned)

Whether or not bit 16 is suppressed in these cases, all bits returned by the control are valid unless bit 16 = 1.

NOTE
Bit 15 can take precedence over bit 16 suppression if bit 15 = 1 or bit 16 is not suppressed.

Table 1-2. DPC 24-bit Result Descriptor

Bit	Significance	Test	Relocate	Initialize	Write	Read
0	Operation complete	X	X	X	X	X
1	Exception condition (3, 4, 5, 7, 10, 11, 12, 13, 15, 16, or 23 set) (3, 7, 13, 15 or 16 set)	X	X	X	X 	 X
2	Not ready	X	X	X	X	X
3	Read Data error	X				
4	Attention	X	X	X	X	
5	Reserved					
6	Write lockout		X	X	X	X
7	Slip occurred	X	X			
7,8,9	Unit ID (field changeable) 000 not present 001 type 225 — half capacity (M223) 010 type 225 — full capacity (M225) 011 reserved 100 reserved 101 type 206 — half capacity (M205) 110 type 206 — full capacity (M206) 111 reserved					X
9	Address parity or sync-code error	X	X			
10	Sector address error	X	X		X	
11	Timeout	X	X	X	X	
10,11	Configuration (field changeable) 00 no exchange 01 exchange 1 10 exchange 2 11 exchange 3					X
12	Seeking					X
13	Reserved					
14	Seek status flip-flop set	X	X		X	X
15	Transmission parity error	X	X	X	X	X
16	Operation completed (See Operation Complete in text)	X	X	X	X	X
17 — 23	ID = 0011110					X
21, 22, 23	Special flags 001 Read OP E variant=1 011 DPEC attention	 X X	 X	 X	 X	

X = This bit is set in the returned result descriptor

Exception Condition

Bit 1, indicating an exception condition, is set if (on any operation) one or more of bits 2, 3, 4, 6, 9, 10, 11, 12, 14, 15, or 22 are set.

Exceptions are:

a. When bit 1 is set only for test purposes (if one or more of bits 2, 6, 12, 14, or 15 are set.

b. When bit 1 = and bit 16 = 0, they are returned (and no result is stored); if set on read W = 0, a busy exchange is then encountered.

NOTE
An exception condition is not reported for a sector if the data associated with the sector is not requested by the system.

Not Ready

If at the start of or during any operation the selected DPEC or disk pack is or goes not ready (drive unsafe), the operation is terminated and bit 2 is set. Also, if a drive is not present, not ready is reported. (Exception: see test operator VV = 10)

Read Parity Error

During a read operation, the 32-bit error check code following each 180 bytes of data is checked by the DPEC for correctness. If any error is detected, it is reported by DPEC to DPC (which will set bit 3 in the RS field after the operation is completed). (Exception: on a read operation with E = 1, bit 3 is not set)

The error check code provides for detection of any single error burst of 32 bits or less, detection of virtually all error bursts greater than 32 bits in length, and correction of any single error burst of 11 or fewer bits.

Correction of any error is performed by software utilizing the error check bits (see read operator E = 1).

DPE/Drive Failure

Bit 4 is set (if a failure indicated by a DPEC attention is reported to the control).

Write Lockout

If at the start of a write, initialize or relocate operation the pack is in a write lockout state the operation is terminated immediately and bit 6 is set. A write lockout condition is also reported on a test operation for type 225 only if the condition is true.

Slip Occurred

If a slip occurs, bit 7 is set in the result after the operation is completed. Bit 1 is not set.

Unit Identification

Bits 7, 8, and 9 are set appropriately as a result of a test operation to indicate presence and type of the designated unit. The assignment of ID bits for each unit (spindle 0 through 15) is set by the Field Engineer and is subject to the following restrictions:

Dual Drives	Spindles
0 & 4	0, 1, 8 & 9 must be same type
1 & 5	2, 3, 10 & 11 must be same type
2 & 6	4, 5, 12 & 13 must be same type
3 & 7	6, 7, 14 & 15 must be same type

Bit significance is as follows:

Bit: 7	8	9	
0	0	0	Not Present
0	0	1	60 sector — 203 cylinder — 20 surfaces
0	1	0	60 sector — 406 cylinder — 20 surfaces
0	1	1	Reserved
1	0	0	Reserved
1	0	1	90 sector — 407 cylinder — 5 surfaces
1	1	0	90 sector — 814 cylinder — 5 surfaces
1	1	1	Reserved

Address Parity Error

If, during any operation, an address parity error is detected after the initial sector is encontered, the operation is terminated immediately and bit 9 is set. If the starting sector cannot be found and an address parity error was detected, bit 9 is also set and the operation terminated. An address parity error in a sector prior to the starting sector is not reported.

If a data sync error is detected during a read operation, the operation is terminated and bit 9 is set.

On type 225, if there is a failure to detect sector pulses, the operation is terminated and bits 4, 9, 10, 11, 22 and 23 are set.

On type 225, if there is a failure to detect read data from the drive, bits 9, 10 and 11 are set.

On type 206, if the address cannot be found bit 9 is set.

Sector Address Error (type 225 only)

On type 225 (during a read, write, or relocate operation), if all address fields are read with correct parity and all cylinder and head address fields indicate that those heads are positioned correctly and there exists a failure to find the requested sector on a given track (track 0 if relocated), the operation is terminated immediately and bit 10 is set.

On type 225, if read data is overlapping into the next sector, bit 10 is set.

Timeout

During a read, write, or relocate operation, if clocks are not received for 1.0 second, the operation is terminated and bit 11 is then reported.

A read, write, initialize, or relocate operation is terminated immediately if the drive is in or goes into a seek-timeout condition. Bit 11 is set.

On type 225, if the DPEC is unable to decode cylinder or head address or if there is a failure to detect an address sync, bit 11 is set.

I/O Subsystem Configuration

Bits 10 and 11 are also set appropriately as a result of a test operation in order to indicate the configuration of the I/O subsystem.

Bit: 11	12	
0	0	Direct connection to DPEC
0	1	DPC connected to exchange 1
1	0	DPC connected to exchange 2
1	1	DPC connected to exchange 3

Seeking

If the interrogated unit is found to be in a seeking status, during a test operation, bit 12 is set immediately.

If the unit is seeking at the start of a read, write, or relocate operation, a result with bit 12 set and bit 16 suppressed is returned immediately. If an address field is read at the start of a read, write or relocate operation with correct parity, and the cylinder address read indicates that the heads are positioned incorrectly and if the seek status flip-flop is off, then a "seek" to the correct cylinder is indicated and a result (with bit 12 set and bit 16 suppressed) is returned.

Bit 16 suppressed indicates to the I/O driver that no result is to be stored.

Seek Status Flip-Flop Set

If the interrogated unit is not seeking during a test operation, and the seek status flip-flop is set, bit 14 is set immediately. The seek complete status of the unit remains unchanged. If the interrogated unit is found during a read, write, or relocate operation to be "not seeking" and the seek status flip-flop is set, but the address calls for another cylinder, then bit 14 is returned and bit 16 is suppressed. No result is stored; no seek is initiated.

Transmission Error

Transfer of information (OP code, file address, data, and result) between the DPC and the DPEC is parity-checked. Even parity constitutes an error. Any detected error is reported in the RS field by setting bit 15. In addition, bit 16 is always reported by the control and is not suppressed at all (in this case).

If a parity error is detected during the initiate phase between the DPC and DPEC, bit 15 is set immediately and the operation is not performed. If a parity error is detected after the initiate phase, bit 15 is set at the end of the operation.

NOTE

Should the error occur during the result status transfer from the DPEC, only bit 0, 1, 7, 15, and 16 are valid; bits 7, 8, 9, 10, 11, 17, 18, 19, 20, 21, 22, 23 are valid only during a test operation.

Control Type

Bits 17 through 23 are set as a result of a test operation to indicate the type of control.

17	18	19	20	21	22	23
0	0	1	1	1	1	0

Special Flags

Bit 21, 22, 23 = 011 are returned representing special flags to the I/O driver on all operations (except test) to indicate that extended status information is available in the DPEC. (Bit 16 is suppressed in this case.)

Bit 21, 22, 23 = 001 are returned as special flags to the I/O driver on the read E = 1 operation. (Bit 16 is suppressed in this case.)

NOTE

An extended status report takes precedence over special flags for read (with E = 1 variant).

SECTION 4

MAINTENANCE TECHNIQUES

DIAGNOSTIC READ

GENERAL INFORMATION

A diagnostic read operation is accomplished by using the read operator D variant. The diagnostic read operation provides 64 bits that indicate the DPEC/DPD. These 64 bits are an extension of the error indications contained in the 16-bit DPEC result descriptor. The relationships of these extended information bits to the 16-bit DPEC result descriptor are listed in table 4-1.

Tables 4-2 through 4-4 and the associated notes list the use of these extended result descriptor bits for both type 225 and type 206 disk pack drives.

TYPE 225 DRIVES — NOTES

a. Only bits 41, 42, 43, 45, 46, 47, and 49 through 64 cause a DPEC attention to be returned to the system

b. Bits 33 through 48 are generated by the DPEC

c. Bits 49 through 62 are generated by the DL-2 Drive (for DL-1 Drives these bits are equal to zero)

d. Only bits 41, 42, 43, 45, 46, and 49 through 62 terminate an operation

e. The extended status register (bits 33 through 64) is cleared only by a read extended status operation

f. The DPEC inhibits all operations (directed to a spindle) and reports DPEC-attention to the system (if the extended status register contains a fault associated with that spindle). If the operation is directed to a spindle that is not in fault, the operation is not inhibited and no attention is reported

g. If a second spindle reports an attention prior to the register in the DPEC being cleared, the DPEC then reports that attention to the DPC, but it does not change the information in the extended status register

TYPE 206 DRIVES — NOTES

a. A status register error report is returned if any bits SR06 through SR21 or SR23 or SR24 are true

b. A requested operation is executed only in the case indicated by bit SR22

c. All bits are reset when the drive reports the exception to the DPEC (except where noted in table 6 (SR bits 5, 9, 10, 14, 16, 22, 23))

d. The drive is powered down in cases indicated by bit SR16, SR21, and SR23

e. The DPEC performs an automatic restore if bit SR9, SR10 or SR14 are reported

f. The status register in DPEC can be cleared only by a read status command

g. If a read extended status operation is sent to DPEC and no extended status information is available in the DPEC, the DPC result reports OP complete, no exception, and no data will be transferred

h. A control message error report is returned for the following conditions/reasons:

1. A control message parity error

2. If two or more read, write or continue bits are true in the same control message

3. If no End bit in control message

Table 4-1. Relationship of DPEC and DPC Extended Status Results

Result DPEC	Result DPC	M225 Extended Result	M206 Extended Result
1. Read data error	4	–	–
2. Write lockout	7	–	–
3. Seek status FF set	15	–	–
4. Drive not ready (positioner not settled)	13	–	–
5. Drive off-line	3	–	–
6. Drive unsafe	3	38, 43, 49, thru 62	SR16, SR21, SR23
7. Address parity or sync code error	10	34, 38, 41	–
8. Sector address error (M225)	11	38, 41	–
9. Seek timeout	12	33, 35, 36, 41, 43	SR14
10. Drive not present	3	—	–
11. Not used	—	—	—
12. Not used	—	—	—
13. Not used	—	—	—
14. OP complete in local (DL-2 225)	[illegible]	—	—
15. Transmission or parity error or illegal command	[illegible]	41, 42, 43, 45, 46,	33 through 38, 63
16. Attention (not possible with DL-1 M225 DPEC)	5, 23, 24	47, and 49 thru 62	SR05 through SR21, SR23, SR24

Table 4-2. Diagnostic Read Bit Functions (Type 225 DPEC)

Bit	Significance	Bit	Significance
1	"0"	33	Add. sync start fault
2	Cylinder 256 address decode	34	Data sync start fault
3	Cylinder 128 address decode	35	Head equal fault
4	Cylinder 64 address decode	36	Cylinder equal fault
5	Cylinder 32 address decode	37	Forced head to zero
6	Cylinder 16 address decode	38	Read data not received
7	Cylinder 8 address decode	39	Spare
8	Cylinder 4 address decode	40	Spare
9	Cylinder 2 address decode	41	Missing sector pulse
10	Cylinder 1 address decode	42	Drive write data not present
11	Head 16 address decode	43	Seek incomplete
12	Head 8 address decode	44	Sequence count = 1 — 9
13	Head 4 address decode	45	Missing R/W clock
14	Head 2 address decode	46	DPEC fan blower failure
15	Head 1 address decode	47	Data skew
16	"0"	48	Not used
17	Sector 32 address decode	49	Speed error
18	Sector 16 address decode	50	DC unsafe
19	Sector 8 address decode	51	Off rack error
20	Sector 4 address decode	52	DC low
21	Sector 2 address decode	53	Read/write error
22	Sector 1 address decode	54	Write current error
23	OP code 1	55	Write/erase current error
24	OP code 2	56	Erase current error
25	OP code 3	57	Read current error
26	Unit 4	58	Head select error
27	Unit 2	59	Air pressure error
28	Unit 1	60	First seek error
29	Old Cylinder not equal to new one	61	End of Cylinder
30	Variant N1 (X)	62	Illegal cylinder
31	Variant N2 (Y)(D)	*63	Sequence count = 10
32	Variant N3 (Z)	*64	External seek

*Bits 63	64	
0	0	Bit 41 to 64 valid; bit 1 to 32 valid for previous OP if bit 44 is TRUE
0	1	Bits 1 — 32 & 41 — 64 valid
1	1	All bits valid

Table 4-3. Diagnostic Read Bit Functions (Type 206 DPEC)

Bit	Significance
1	Cylinder 512 address decode
2	Cylinder 256 address decode
3	Cylinder 128 address decode
4	Cylinder 64 address decode
5	Cylinder 32 address decode
6	Cylinder 16 address decode
7	Cylinder 8 address decode
8	Cylinder 4 address decode
9	Cylinder 2 address decode
10	Cylinder 1 address decode
11	"0"
12	"0"
13	Head 4 address decode
14	Head 2 address decode
15	Head 1 address decode
16	Sector 64 address decode
17	Sector 32 address decode
18	Sector 16 address decode
19	Sector 8 address decode
20	Sector 2 address decode
21	Sector 2 address decode
22	Sector 1 address decode
23	OP code 1
24	OP code 2
25	OP code 3
26	Unit 4
27	Unit 2
28	Unit 1
29	Variant NO (Y)
30	Variant N1 (X)
31	Variant N2 (Y) (D)
32	Variant N3 (Z)

Bit	Significance
33	DPEC blower fan failure
34	Missing read-write clock
35	Missing sector pulse (Address mark)
36	Read data not received
37	"0"
38	Bit 38, if true, indicates a control message error, in which case bit 39 through 62 contain the last CM* sent to the drive. If bit 38 is false, then bit 39 through 62 contain the contents of the drive's status register (SR01 through SR24)
39 • • • 62	See table 4-4
63	Bad DM response
64	Spare "0"

*CM = Control Message

Table 4-4. Control Messages (Type 206 Drive; Bits 39 through 62)

Bit	Type 1	Type 2	Type 3	Type 4
39 01	"0"	Mark	Mark	Mark
02	"0"	Write/	Write/	Write/
03	"0"	Read/	Read/	Read/
04	"0"	Address/	Address/	Address/
05	"0"	Parity (even)	Parity (even)	Parity (even)
06	"0" 0	Continue 1	Continue 1	Continue 1
07	"0" 0	Control/ 0	Head or cylinder 1	Head or cylinder 1
08	"0"	Offset on	Cylinder/ 0	Head 1
09	"0"	Offset in	Cylinder address (LSB)	Head address (LSB)
10	"0"	PLO early indicators	Cylinder address	Head address
11	"0"	PLO late	Cylinder address indicators	Head address
12	"0"	Power up	Cylinder address	Head address
13	"0"	Power down	Cylinder address	Head address (MSB)
14	"0"	Restore	Cylinder address	Spindle address (LSB)
15	"0"	Read status	Cylinder address	Spindle address
16	"0"	Find index	Cylinder address	Spindle address
17	"0"	"0"	Cylinder address	Spindle address
18	"0"	"0"	Cylinder address (MSB)	Spindle address
19	Mark	Reset maintenance	"0"	Spindle address
20	Write/	Set maintenance	"0"	Spindle address
21	Read/	Set write enable	"0"	Spindle address (MSB)
22	Address/	"0"	"0"	"0"
23	Parity (even)	Parity (even)	Parity (even)	Parity (even)
62 24	End/	End/	End/	End/

Note: The indicators following the control messages for bits 6, 7, and 8 determine the type of control message as follows:

Bit 6=0	Type 1
Bit 6=1, Bit 7=0	Type 2
Bit 6=1, Bit 7=1, Bit 8=0	Type 3
Bit 6=1, Bit 7=1, Bit 8=1	Type 4

SECTION 5

THEORY OF OPERATION

INTRODUCTION

The primary function of the B 1800/B 1700 Disk Pack Control II (DPC-II) is data routing from the central processor to the disk pack electronics controller (DPEC) or from the DPEC to the processor. DPC-II accepts commands and operators from the processor and translates them into useful information for the DPEC. DPC-II also accepts a result from the DPEC and translates it into useful information for the processor.

Data is transferred between the processor and the DPC 24 bits at a time, but only 16 bits at a time between the DPC and DPEC. Data is stored in the RAM 8 bits at a time; therefore, three RAM accesses are required in a system memory cycle and two accesses for a disk cycle. DPC-II has the capacity to buffer five sectors (900 bytes) of data. The DPC keeps track of how much buffering is available at all times and puts the DPEC in the slip mode as required.

When the DPC is not in communication with the system, it goes into a polling mode searching for a drive that is in Seek-Complete status. If such a drive is found the DPC interrupts the processor.

The DPC contains a timeout counter that reports to the processor if communication has been unexpectedly lost with the DPEC for more than 1 second.

LOGIC FUNCTIONS

DPC-II consists of two logic cards, one primarily for data functions, the other for control functions. The logic blocks that comprise each card are listed in table 5-1.

Table 5-1. Logic Blocks in DPC-II

Data Card Logic Blocks	Control Card Logic Blocks
Input register	Status counter
Output register	Load and dump counters
RAM memory	Buffers full counter
Memory address counters	Control flip-flops
Memory request selection	Operation register
Memory control	Channel recognition circuitry
Memory write enable generation	Command and command variant registers
Interface clock logic	Result descriptor gating
Interface drivers and receivers	Sequence decoder
Parity logic	Diagnostic logic
File address register	

Paragraphs following contain descriptive data on logic blocks with many of their interfacing relationships with one another.

INPUT REGISTER

The input register consists of an electronic control input register and an exchange input register (EC IR). (See figures 5-1 and 5-2.) The EC IR is made up of six CTL LFAN chips arranged as three 8-bit bytes. The EC IR is made up of four CTL LFAN chips arranged as two bytes. The five bytes are wire-ored at the output of the LFANs and drive the eight data inputs of the RAM memory. The enables of the LFANs are controlled by the memory control. The EC IR is loaded with the reference address with CA, XFROTA, and STC07, STC08, or STC09. It is loaded with data with RC and XFROTB. The EC IR is loaded with data from the EC with ECRQW.

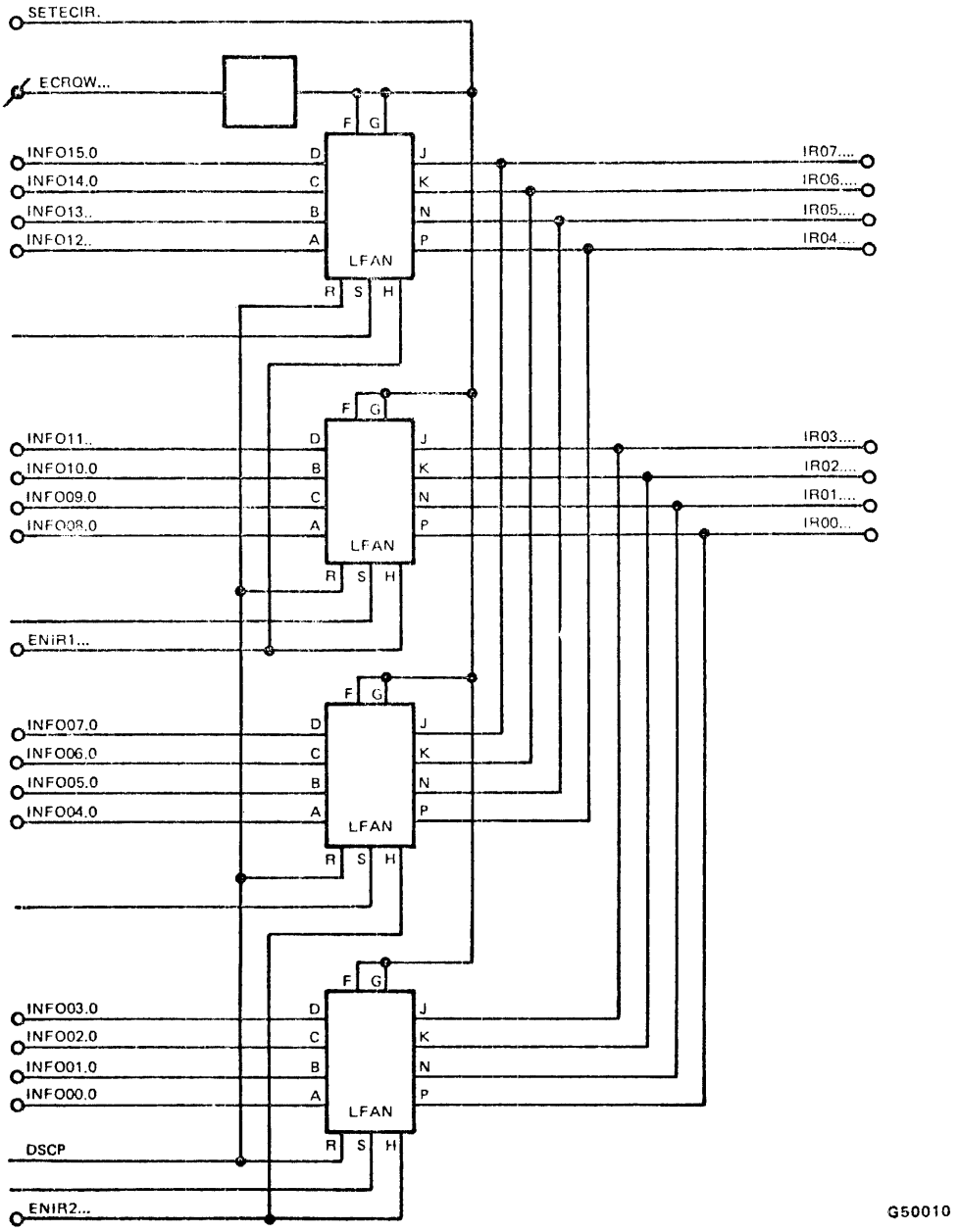

Figure 5-1. Electronic Control Input Register (ECIR)

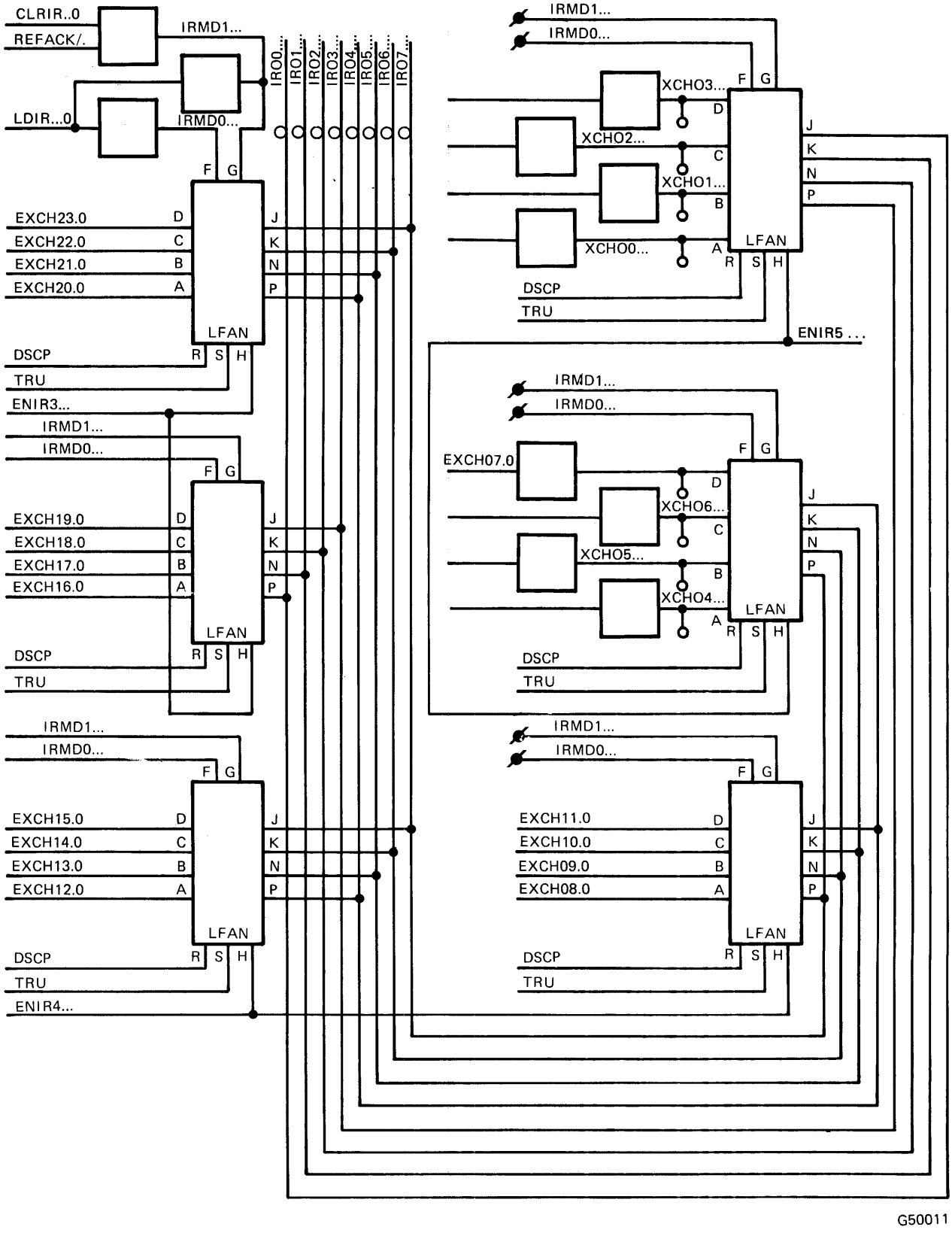

Figure 5-2. Exchange Input Register (Exchange IR)

OUTPUT REGISTER

The output register (OR) consists of an exchange OR and an electronic control OR. (See figure 5-3 and 5-4.) The exchange OR is made up of six CTL LFAN chips arranged as three bytes. The EC OR is made of eight CTL LFAN chips arranged as two 16-bit registers in series (EC OR1 and EC OR2), each of which consists of two 8-bit bytes. The exchange OR and EC OR1 are driven by the data outputs of the RAM memory. EC OR2 is driven by the output of EC OR1. The loading of the exchange OR and EC OR1 is controlled by the memory control. EC OR2 is loaded with ECRQR. The output of the exchange OR drives the exchange lines and is enabled with a XFRIN command in STC07, STC08, STC09, or STC15. The output of EC OR2 drives the information bus during the data phase of read operation.

RAM STORAGE

The RAM storage, figure 5-5, consists of eight RW06 chips (1024 bits) arranged as 1024 eight-bit words. This allows storage for five sectors of data and the reference address. It is driven by the input register and drives the output register.

RAM ADDRESS COUNTERS

The memory address counter consists of four separate counters whose outputs go through a 4-1 multiplexor (S4-N) to the address lines of the RAM memory. The four counters are the reference address counter, the system address counter, the electronic control (EC) address counter, and the initialize address counter.

The reference address counter, figure 5-6, is a single CR4N chip. It is preset to one, counts by one up to three, and from three is reset to one. This allows for three memory addresses to store the reference address. They are 00 0000 0001 through 00 0000 0011. The counter is incremented by the memory control.

The system address counter, figure 5-6, is made of three CR4N chips. It is preset to 00 0101 1110, incremented by ones to value 11 1111 1111, and resets to 00 0101 1110. This gives 930 storage locations or five sectors (5 x186=930) of storage. On read operations buffer n+5 will be stored in the same memory location as buffer n. Since only 180 bytes are stored per sector on a write op, the bytes for buffer n +5 will be stored 30 addresses before the corresponding bytes in buffer n.

The EC address counter, figure 5-6, has the same characteristics as the system address counter. However, the EC address counter is selected when accesses are being made by the EC.

The initialize address counter, figure 5-7, also consists of three CR4Ns. It is used to count through all memory locations during a clear cycle on the card tester to clear the RAM. It also doubles as a 1-sec timeout timer. If the DPC ever remains in STC10 on a non-initialize op for more than one sec, the timer times out and the control exits.

MEMORY REQUEST SELECTION

There are six types of memory requests listed below (in order of priority):

1) REFROR — reference address request for read

2) REFRQW — reference address request for write

3) ECROR — electronic control request for read

4) ECROW — electronic control request for write

5) SYRQR — system request for read

6) SYRQW — system request for write

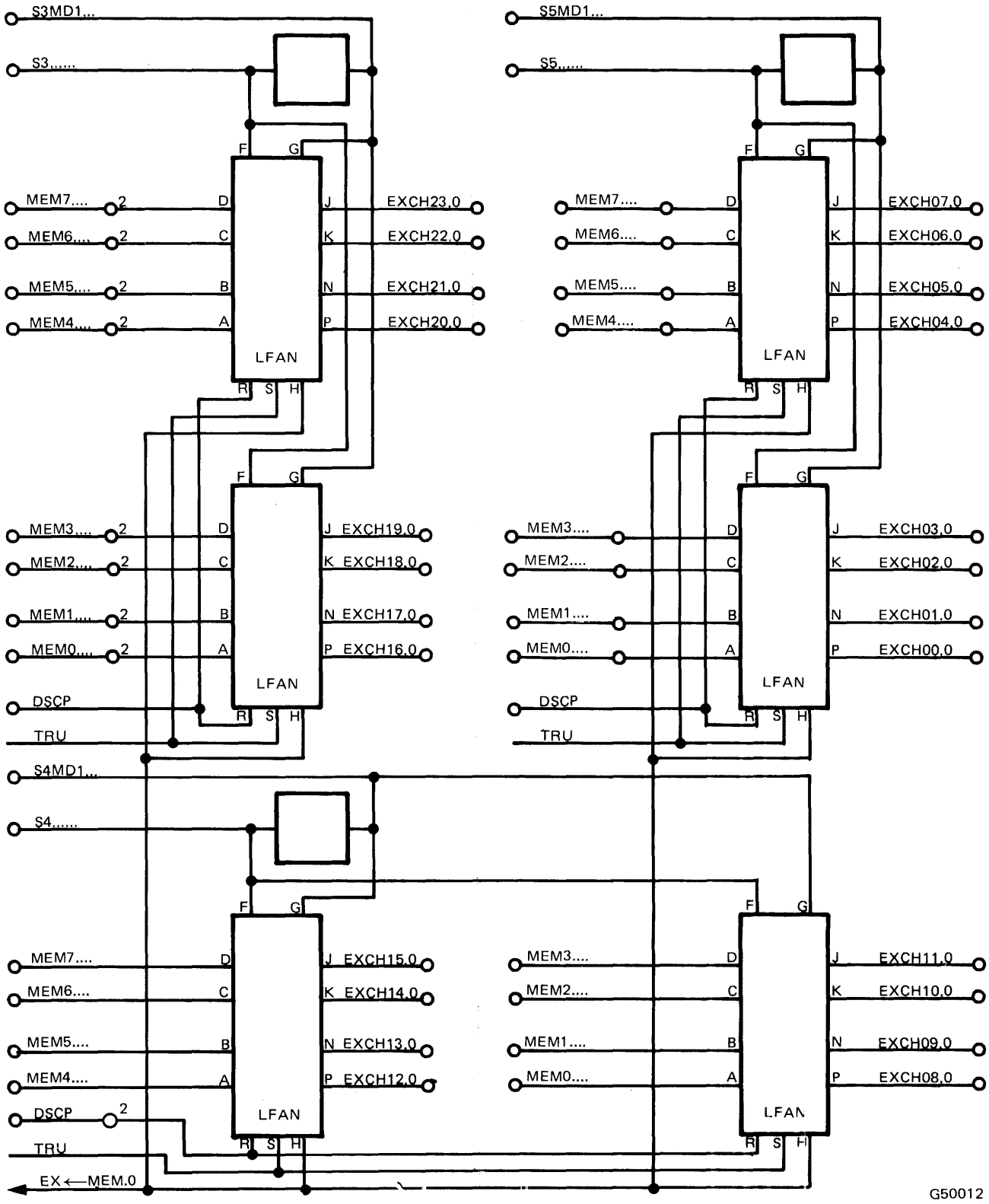

Figure 5-3. Exchange Output Register (Exchange OR)

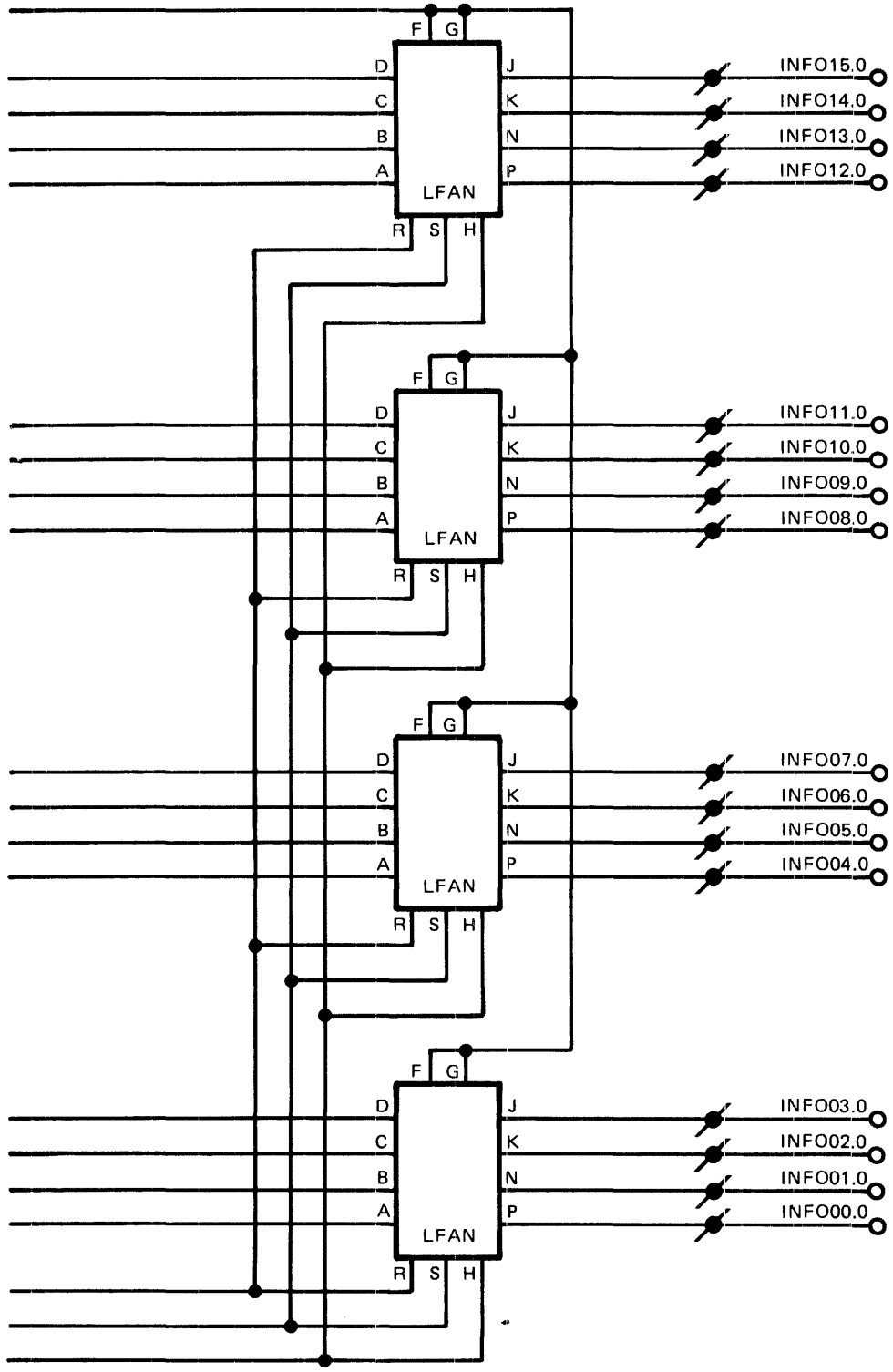

Figure 5-4. Electronic Control Output Registers 1 and 2 (ECOR1, ECOR2)

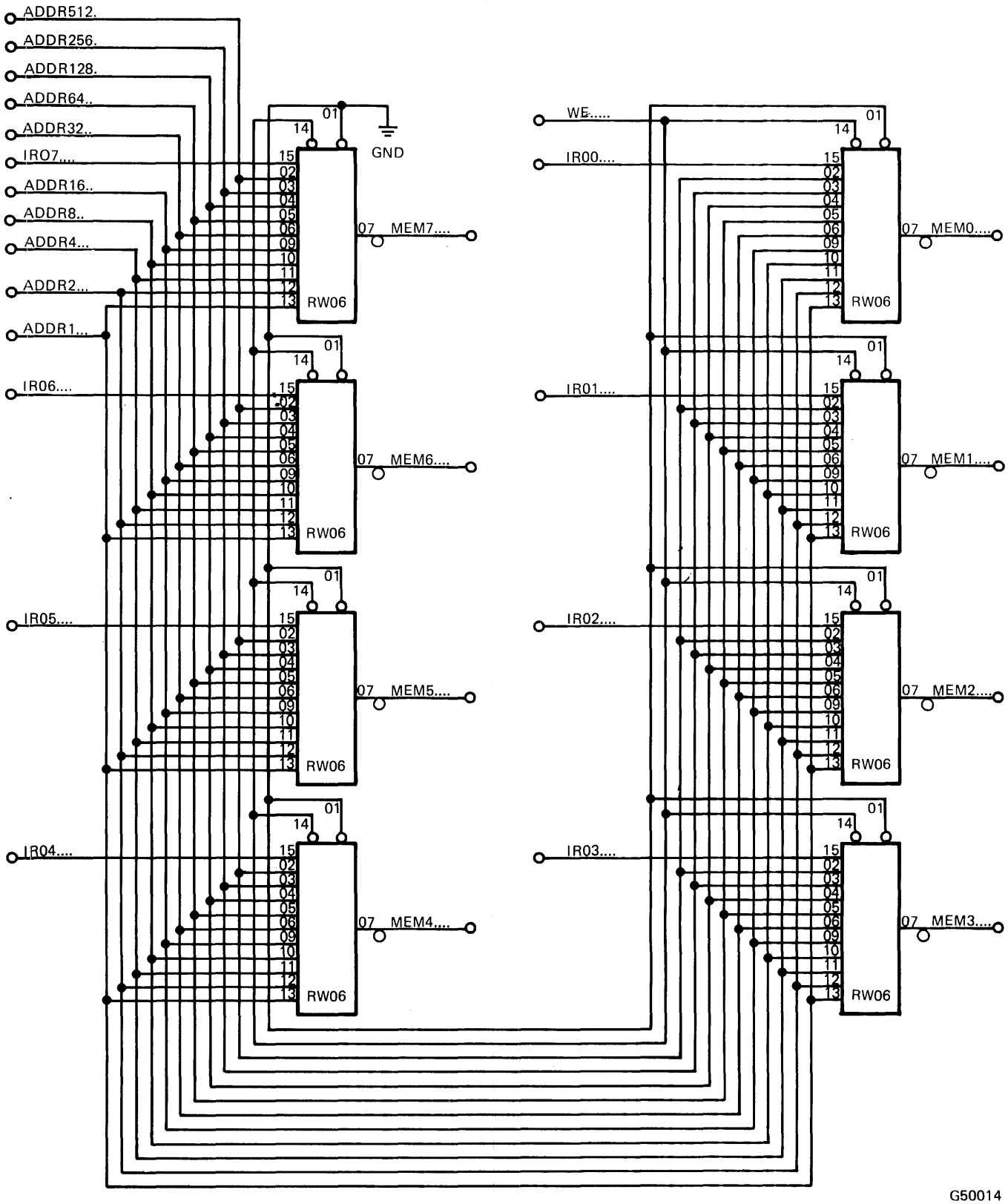

Figure 5-5. RAM Storage DPC-II

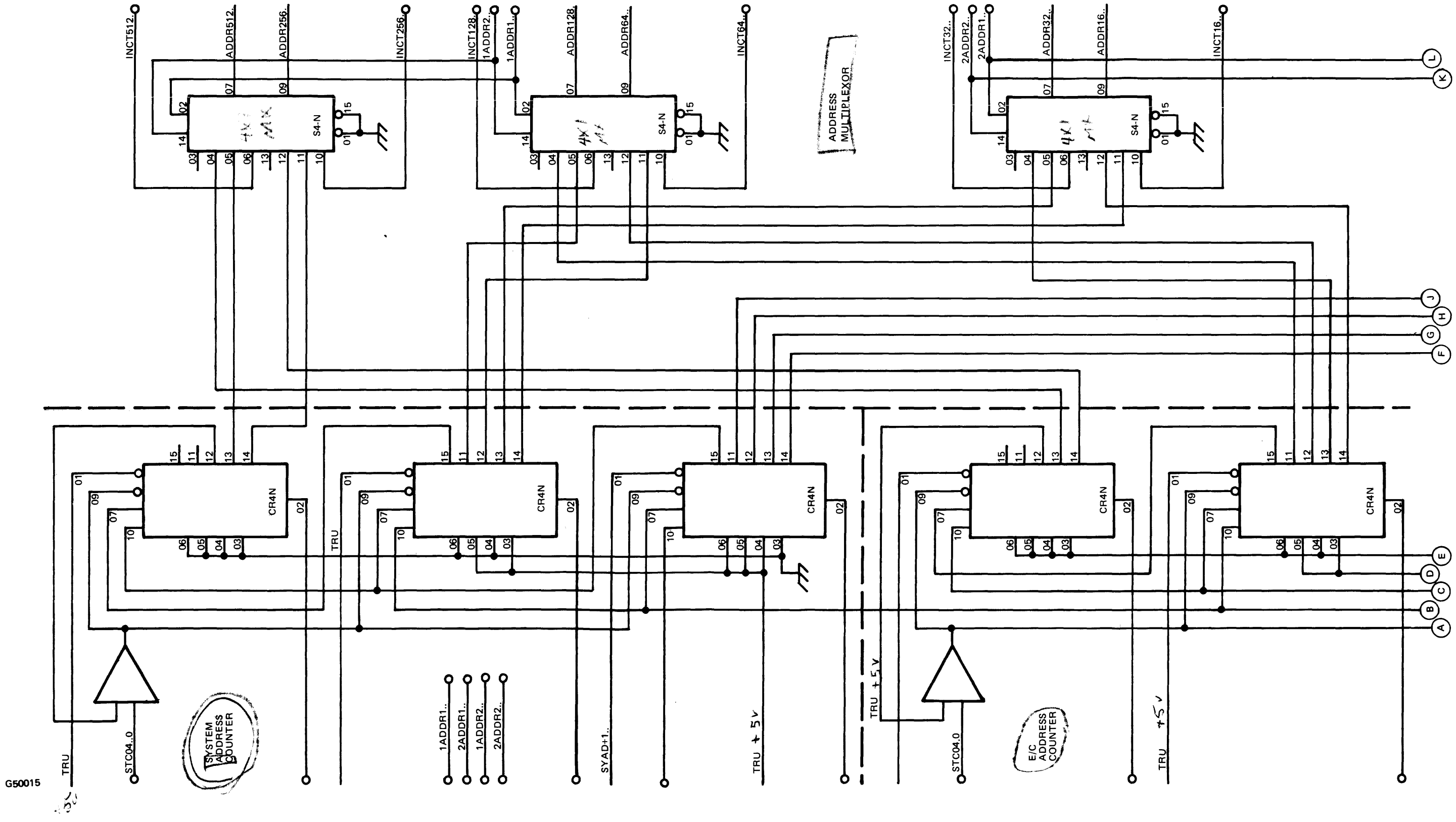

Figure 5-6. System, Electronic Control, and Reference Address Counters (Sheet 1 of 2)

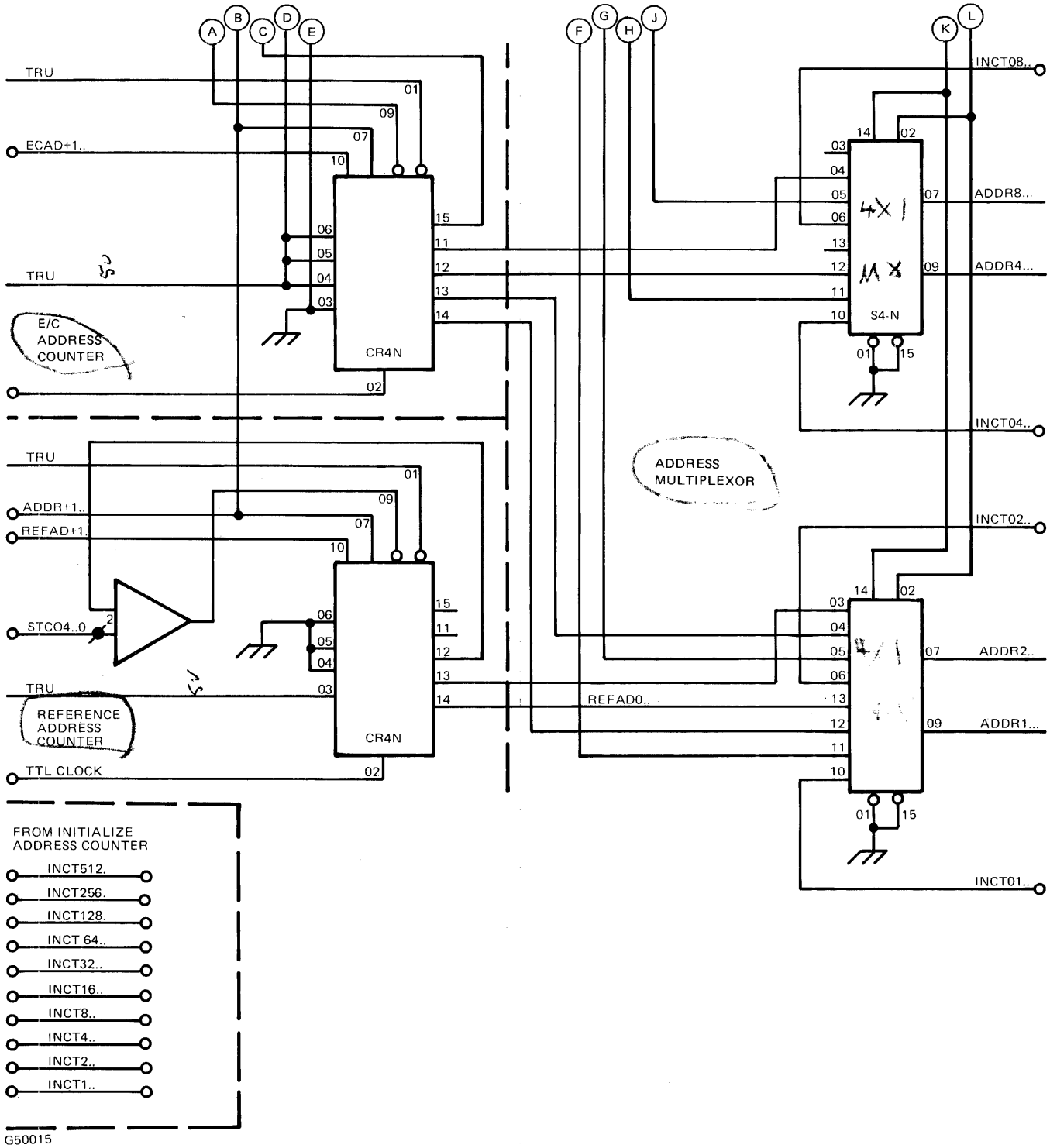

Figure 5-6. System, Electronic Control, and Reference Address Counters (Sheet 2 of 2)

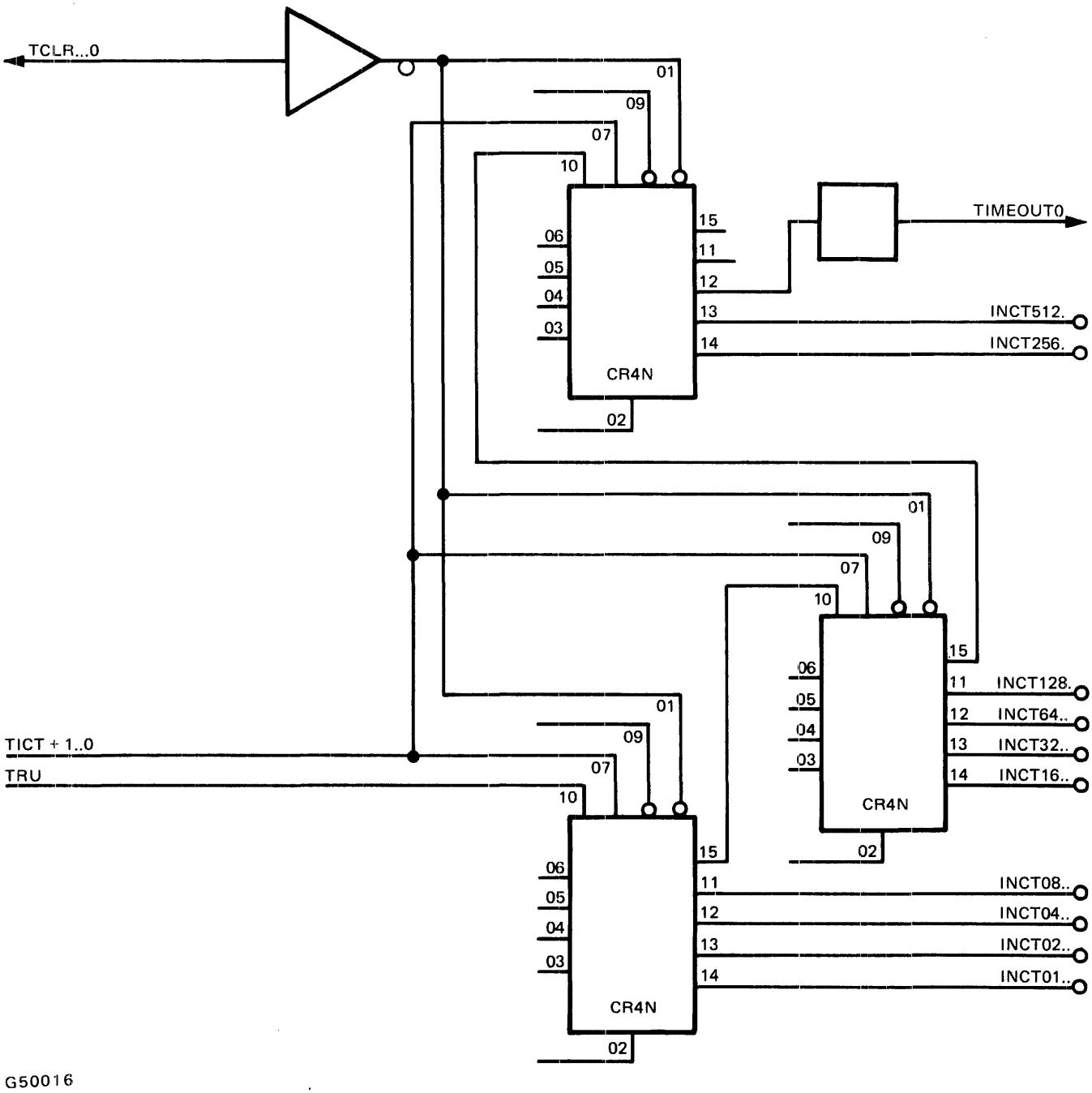

Figure 5-7. Initialize Address Counter

These six requests are stored in six separate flip-flops that have outputs that go to a priority encoder (EFAN) which resolves their order of priority. The flip-flops are reset with an appropriate acknowledgeable signal from memory control. (See figure 5-8.)

MEMORY CONTROL

General

The memory control consists of a request register, a PROM, a state register and two decoders. The request register is loaded when the control memory is idle with the outputs of the request encoder. The outputs of the request register select the appropriate memory address counter and addresses the 32 x 8 P002 PROM. This "PROM" generates IDLE, ACK, and WE signals along with the next state. The state register is an RFBN whose outputs are the WE pulse and address to the PROM. The RFBN outputs also go to two decoders (DFANs) that generate the IR and OR load and enable signals. (See figure 5-9.)

The priority encoder outputs RQ1, RQ2, and RQ3 define the memory access requests as shown in table 5-2 below.

Table 5-2. Definition of Memory (RAM) Access Requests from Priority Encoder Outputs

States			
RQ1	RQ2	RQ3	Definition of Memory (RAM) Access Request
1	1	1	Reference address read
0	1	1	Reference address write
1	0	1	EC read
6	0	1	EC write
0	1	0	System write
1	1	0	System read

Terms RQ1, RQ2, RQ3 are used by memory control to develop terms MS0, MS1, S1 through S5, ENIR1 through ENIR5, and the various memory address counter-enabling terms. These control terms provide the DPC-II with both the 3-byte to 2-byte transfer conversion and the 2-byte to 3-byte data transfer conversion necessary to interface the B 1700 or B 1800 system with DPEC. These terms also permit the input and output register gating and memory addressing necessary to store and retrieve reference addresses in the DPC-II RAM.

Reference Address Write

During status counts 4, 5, and 6 each one-byte of reference address data are provided to the control on exchange lines zero through seven. These three bytes of the reference address are stored one byte at a time into the DPC-II RAM at address 1, 2 and 3 as directed by the Reference Address counter and Memory Control. (See figure 5-10.) The write sequence depicted in figure 5-11 would be repeated once for each status count 4, 5 and 6.

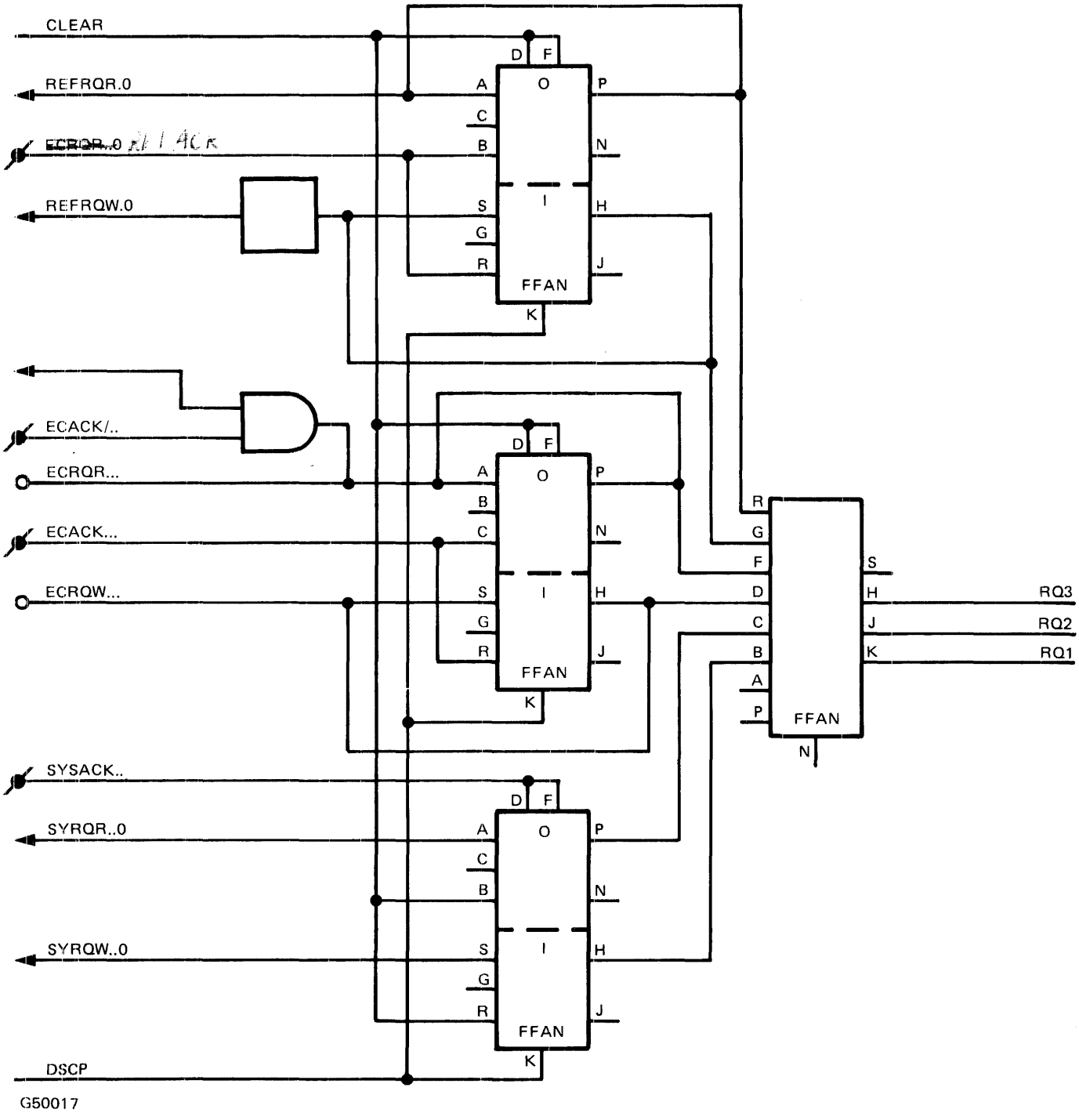

Figure 5-8. Memory Request Flip-flops and Priority Encoder

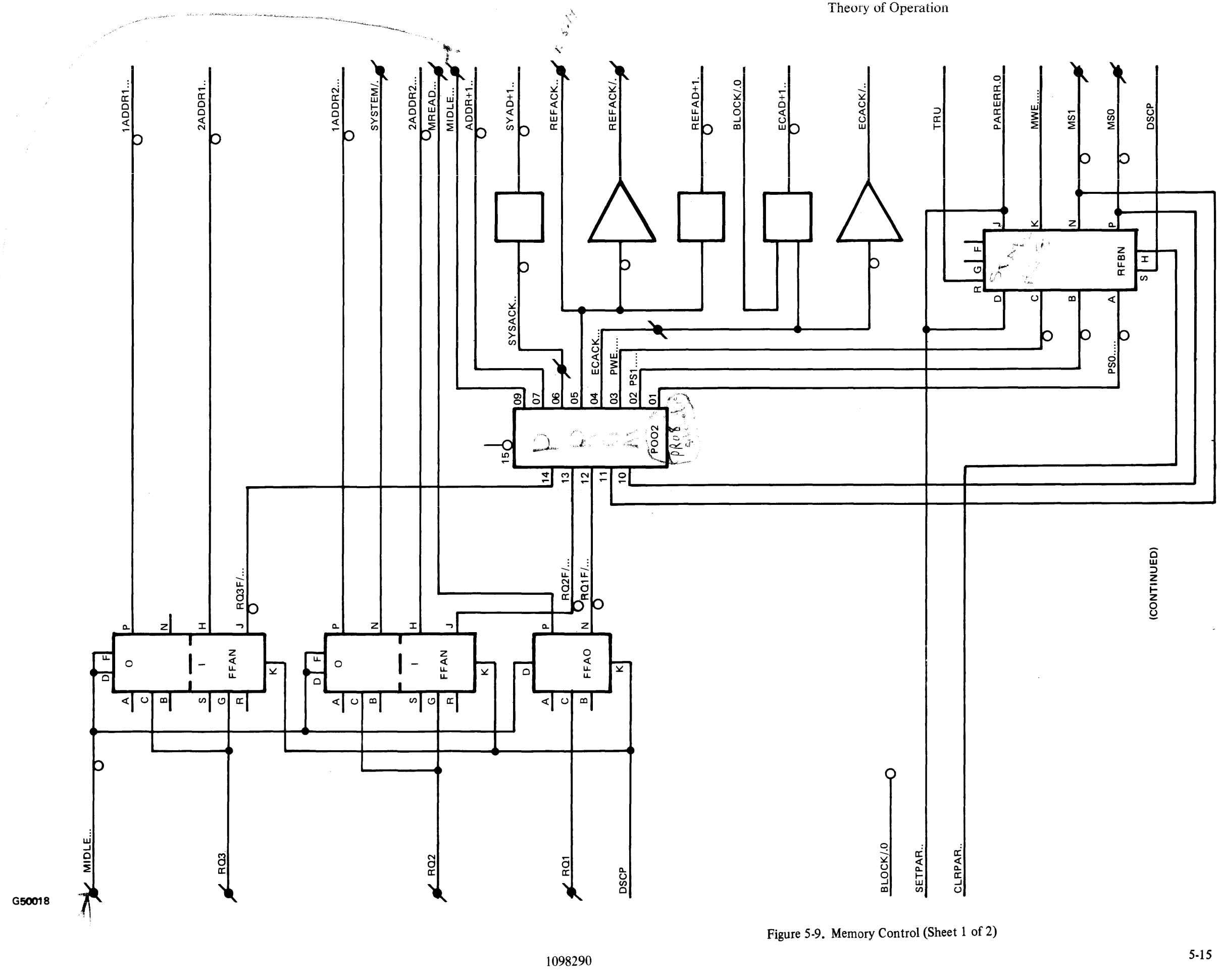

Figure 5-9. Memory Control (Sheet 1 of 2)

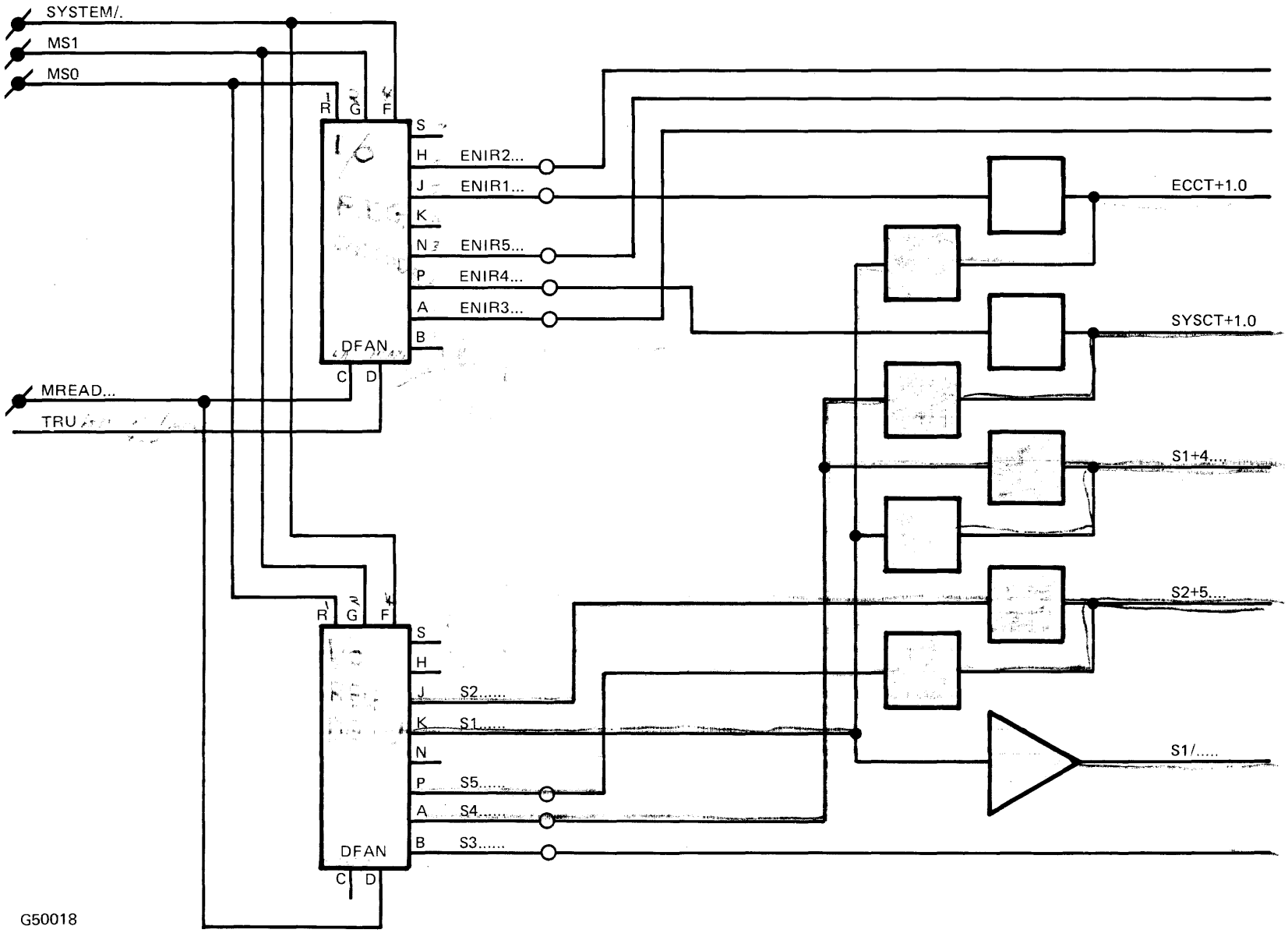

Figure 5-9. Memory Control (Sheet 2 of 2)

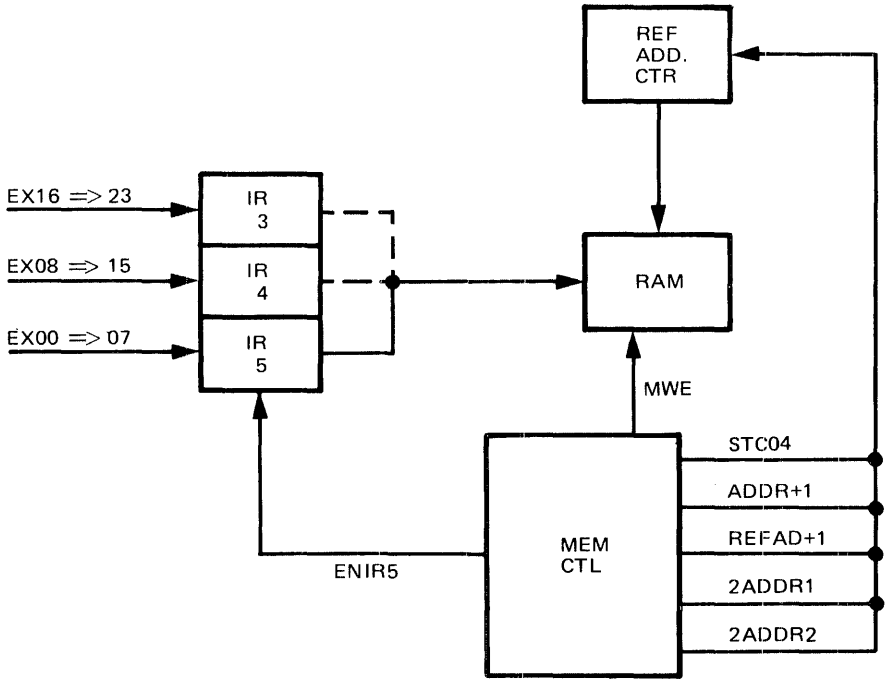

Figure 5-10. Reference Address Write Data Flow Diagram

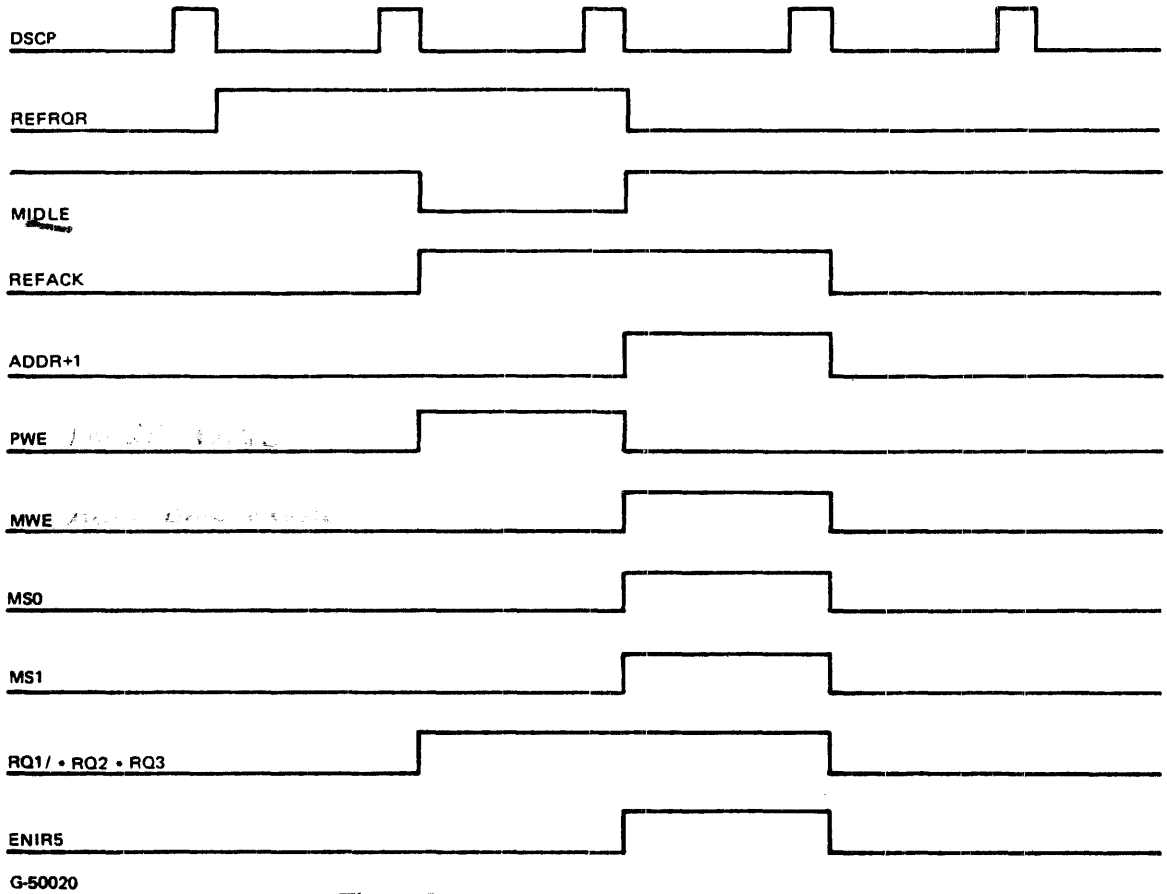

Figure 5-11. RAM Reference Address Write

Reference Address Read

Three bytes of reference address data must be returned to the system during status counts 11, 12 and 13; or 18, 19 and 20, depending upon the operation code and relative items within the flow of that operation code. Only one byte of Reference Address is transferred from the RAM at each status count through output register S5 to exchange lines 00 through 07 as shown in figure 5-12. The reference address read sequence shown in figure 5-13 will be repeated once for each of the aforementioned status counts.

Electronic Control (EC) Write

The RAM EC write sequence shown in figure 5-14 depicts relationship of the nets necessary to accomplish a data write to the RAM from the INFO lines within DPC-II. These lines may receive data from the DPEC during a Read operation (figure 5-16) or the File Address register during a Diagnostic Read operation (figure 5-17). This timing series will be repeated once for every two bytes of data to be written into the RAM. Data latched into the input register two bytes at a time will be written into the RAM one byte at a time, alternating between IR1 and IR2 as determined by Memory Control and the EC Address Counter.

System Read

The RAM system read sequence shown in figure 5-15 depicts the relationships between the nets necessary to accomplish a data read from the RAM to the exchange lines. The data read from the RAM one byte at a time is loaded into the exchange output registers S3, S4 and S5 alternately as determined by Memory Control and the exchange address counter. Three RAM read operations will occur for every data transfer to the system. Therefore, after each completion of the system read timing sequence, the exchange output register will have received one byte of data into each S3, S4 and S5 which are then transferred (all three bytes parallel) to the central system.

The complete EC write-system read cycle accomplishes the 2-byte to 3-byte data conversion. The 3-byte to 2-byte data transfer conversion necessary for a disk write operation utilizes the system write and EC read of the DPC-II RAM.

Figures 5-16 and 5-17 show, respectively, the Read and Diagnostic Read data flows.

System Write

Figure 5-18 shows the relationships of the system write terms. Data, three bytes parallel, is loaded into the exchange input register, IR3, IR4 and IR5 as shown in figure 5-19 for a write operation and figure 5-20 for a Diagnostic Write operation. The data is then written alternately one byte at a time from IR3, IR4 and IR5 as determined by Memory Control, into the RAM addresses determined by the system address counter. The system write timing sequence will be repeated once for each system-to DPC-II data transfer.

Electronic Control Read

Figure 5-21 depicts the RAM EC read timing sequence. The EC address counter selects the addresses to be read from the RAM. Memory control alternately loads the EC output registers S1 and S2 providing data 2 bytes high for transfer to the DPEC. Note that the DPC-II incorporates two levels of EC output buffers, the second of which is loaded from the first by the term ECRQR (EC request for read). [Text continues on page 5-22.]

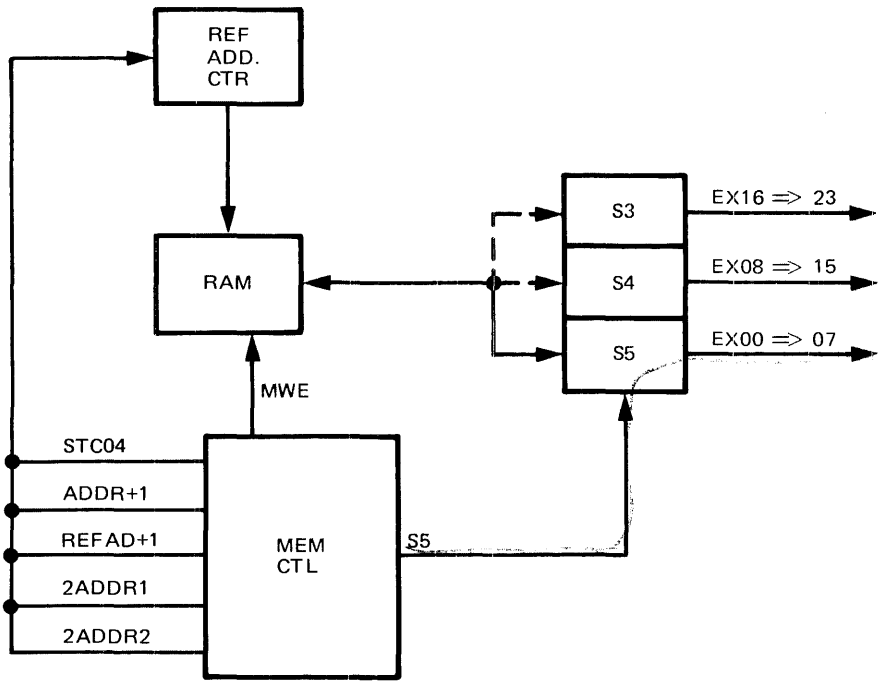

Figure 5-12. Reference Address Read Data Flow Diagram

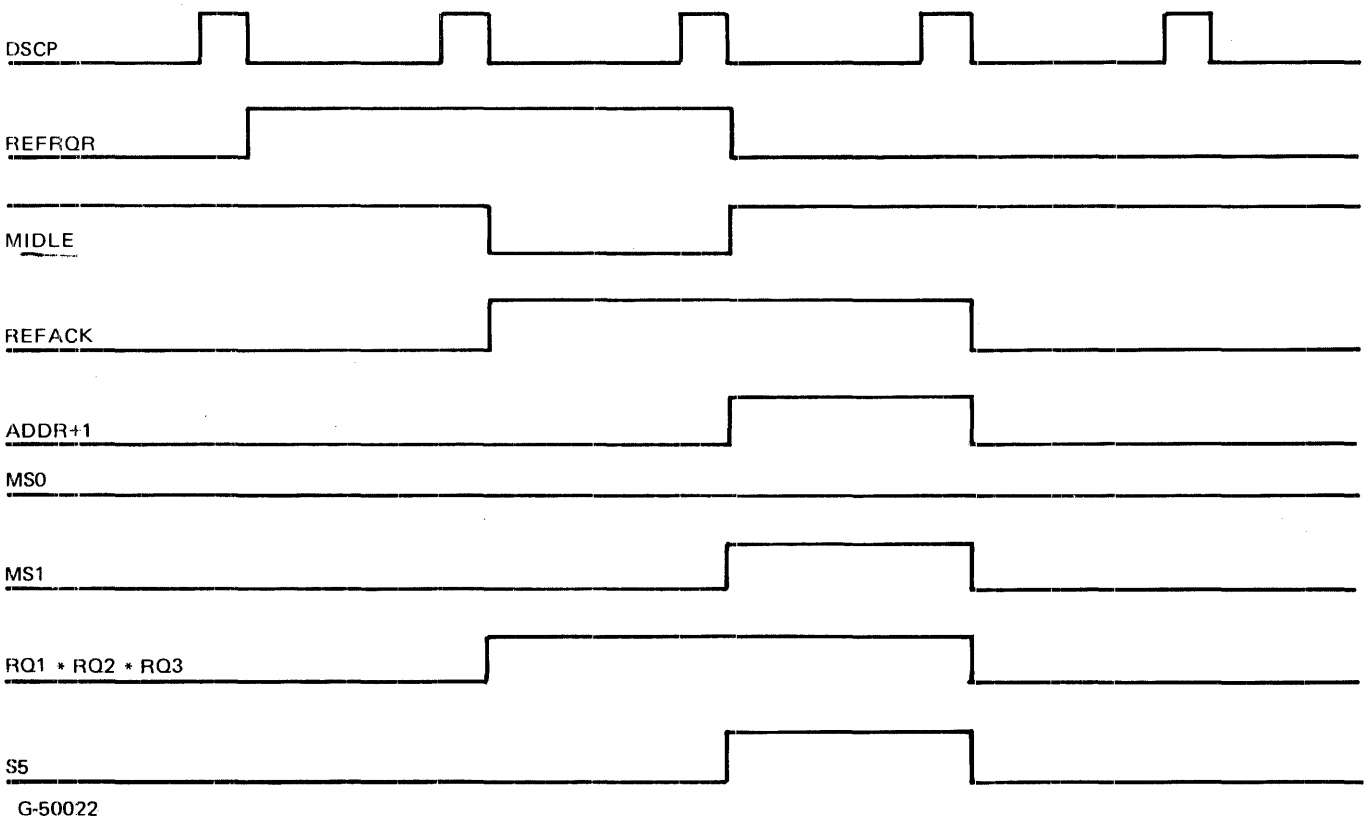

Figure 5-13. RAM Reference Address Read

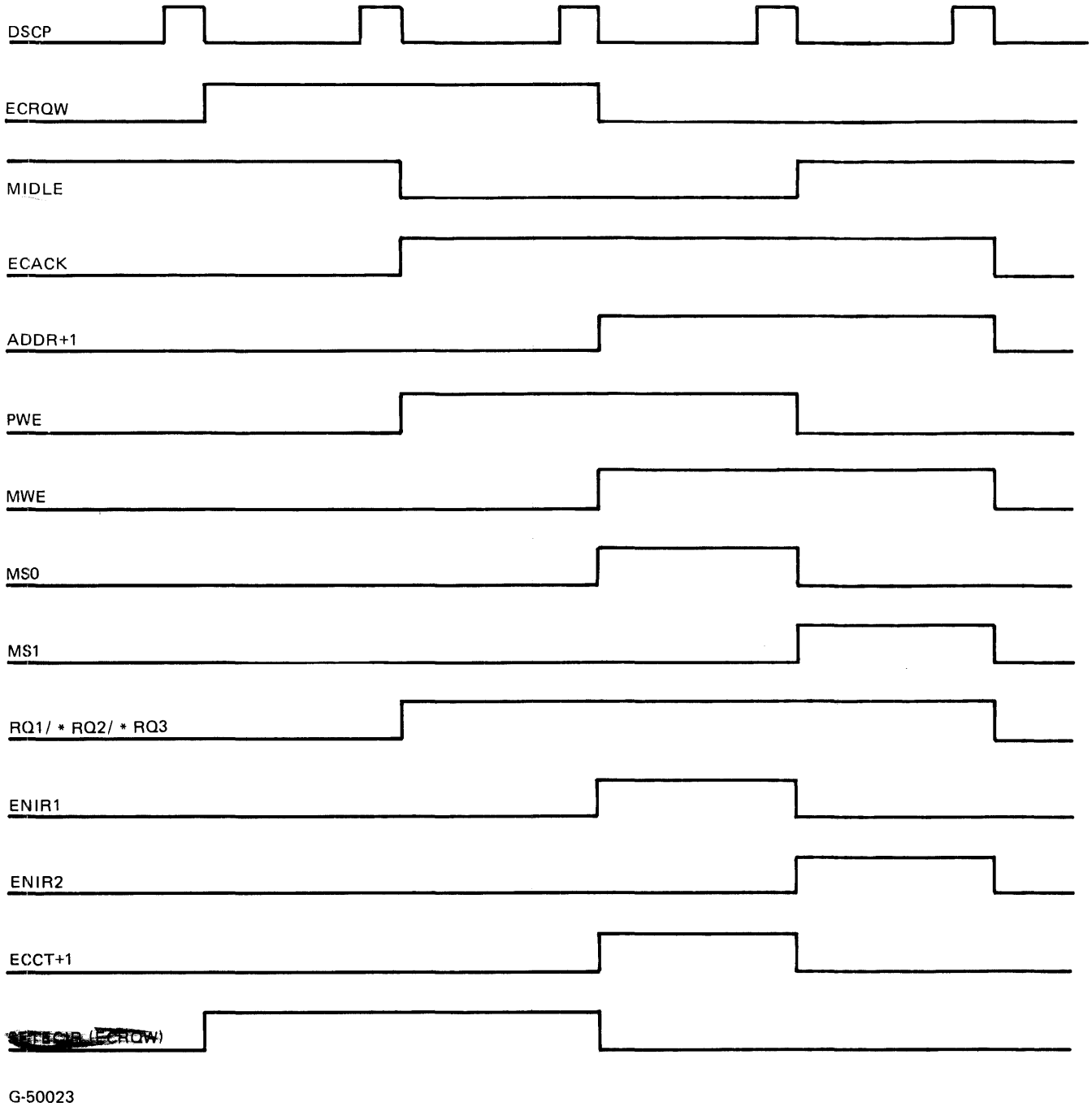

Figure 5-14. RAM EC Write

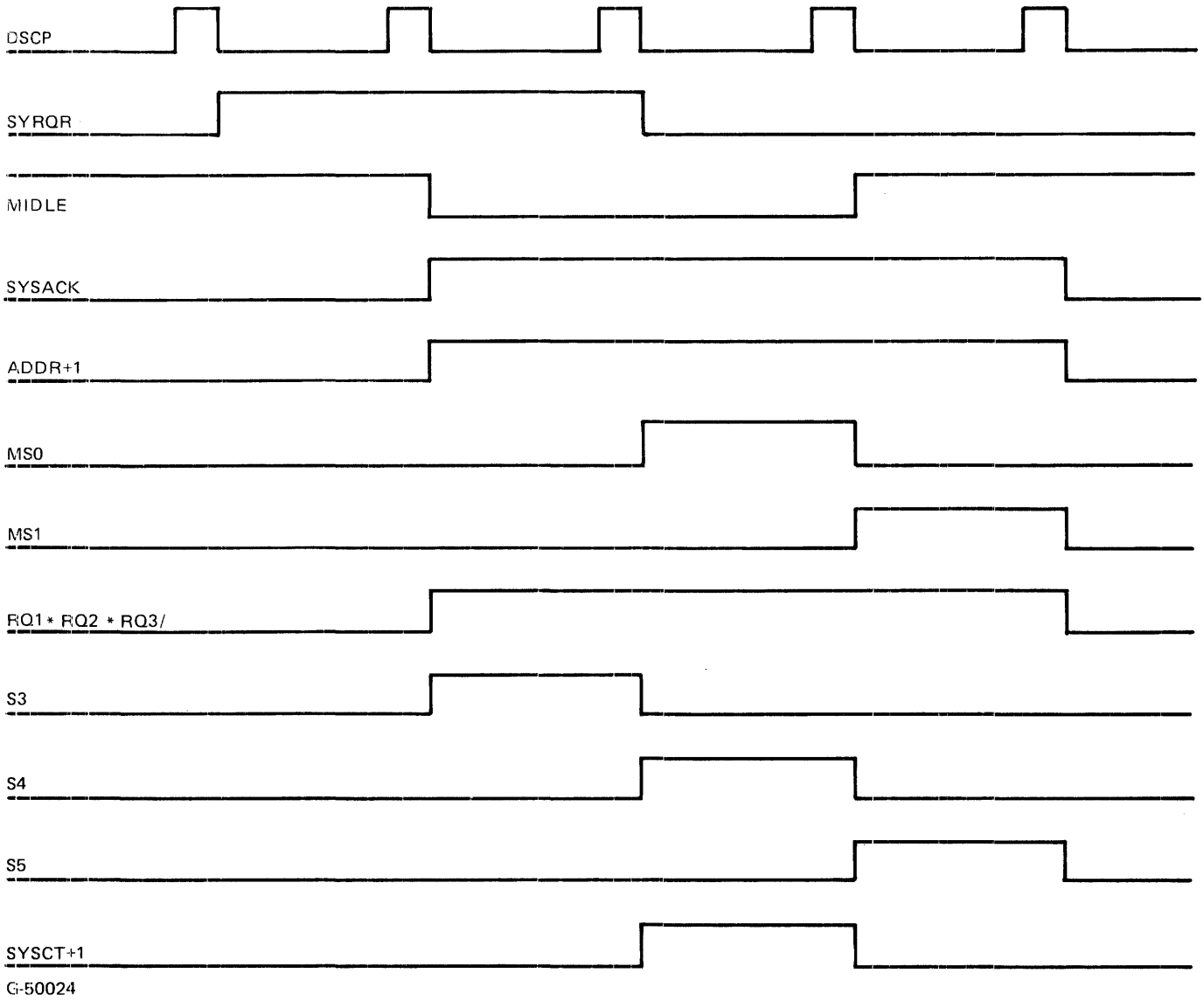

Figure 5-15. RAM System Read

Note that in figure 5-20 (during a diagnostic write operation) data, rather than being transferred to the DPEC, is gated back onto the exchange lines.

The diagnostic RAM test data path, shown in figure 5-22, provides for the write and read of the DPC-II RAM without transferring data to or from the DPEC.

MEMORY WRITE ENABLE GENERATION

The write enable pulses to the RAM are generated through the use of two delay lines. The outputs go to a jumper chip to allow the timing to be adjusted as needed. (See figure 5-23.) Refer to the DPC-II FT&R documents for adjustment procedures.

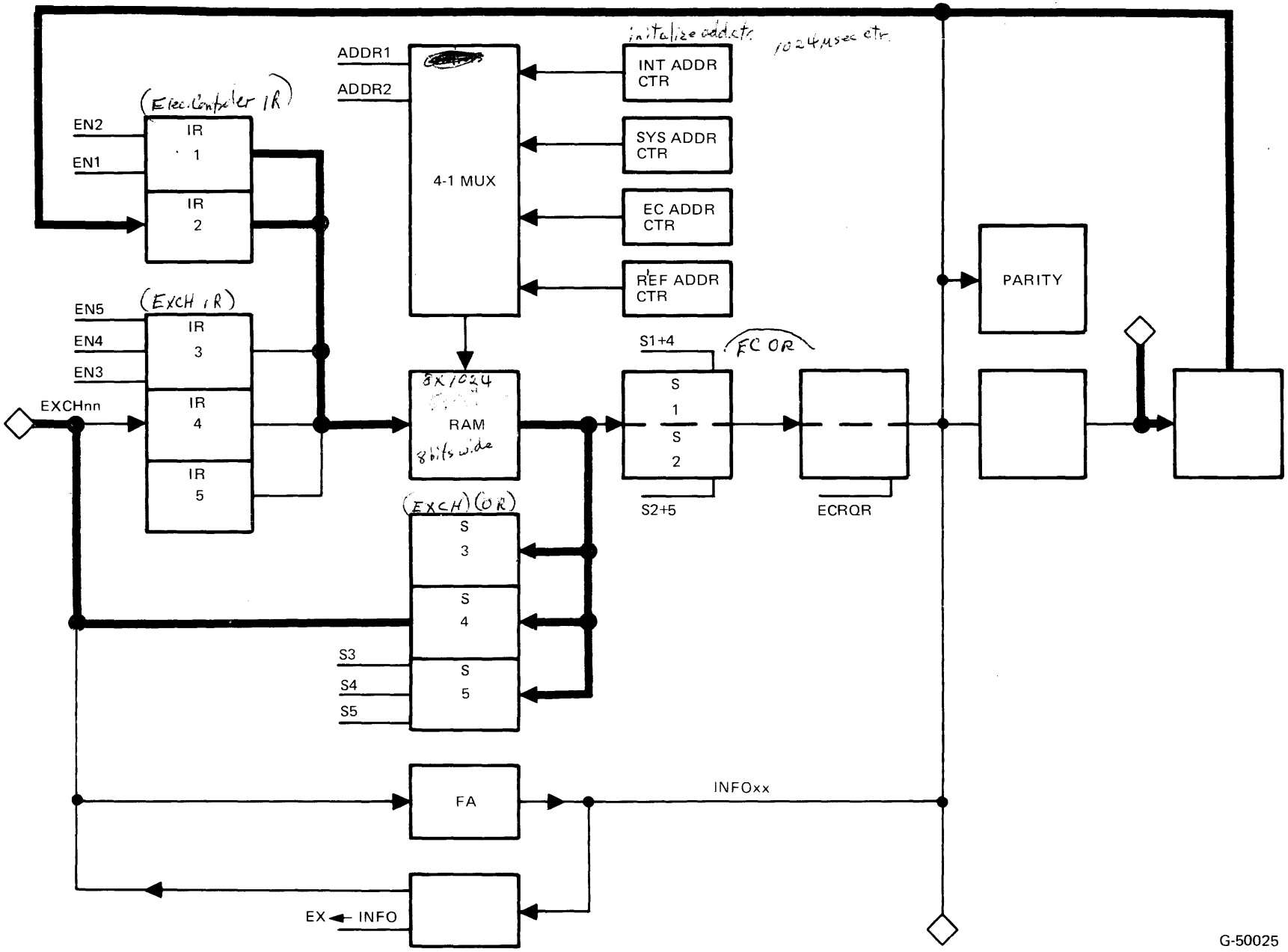

Figure 5-16. Read Data Path

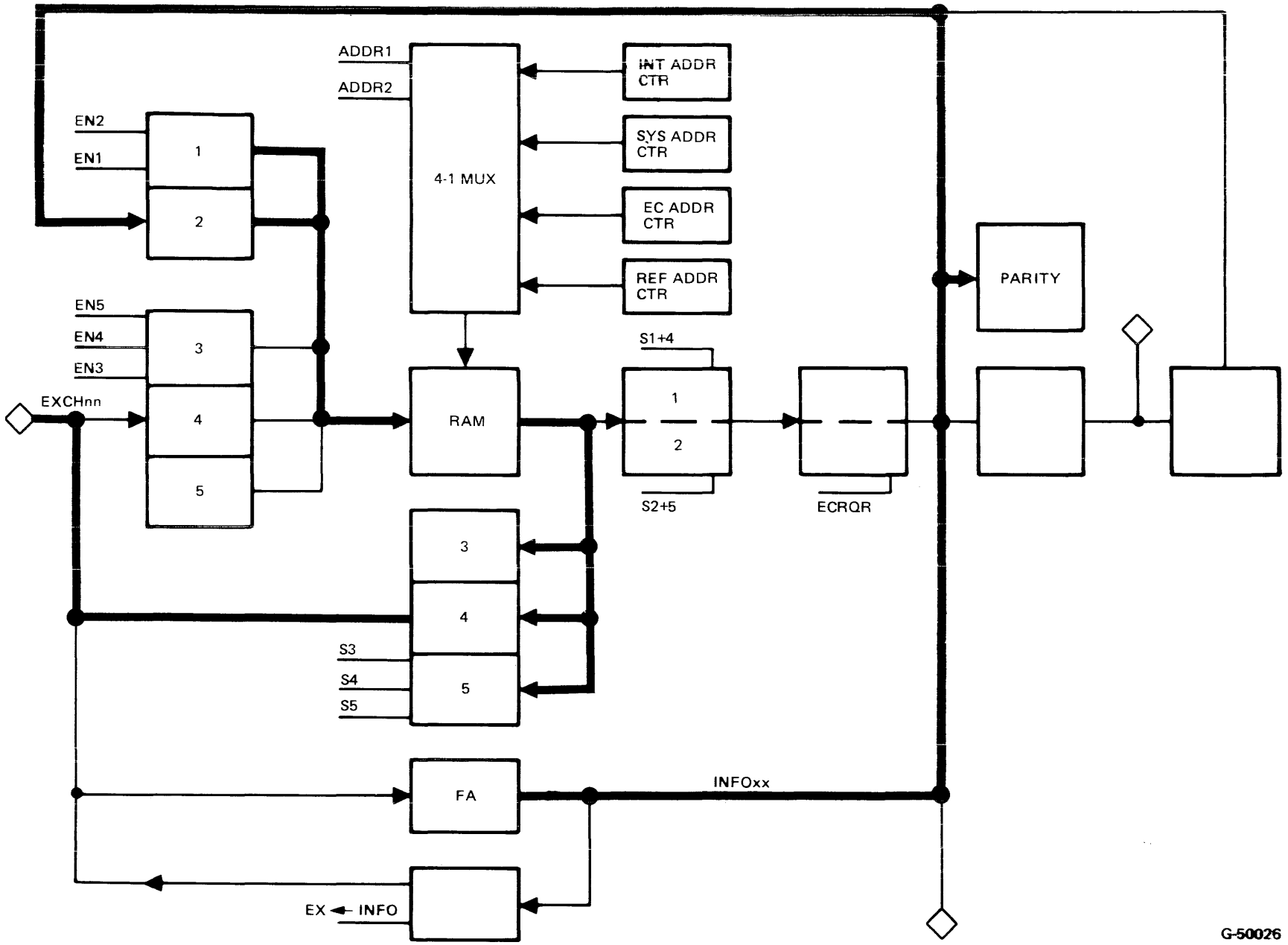

Figure 5-17. Diagnostic Read Data Path

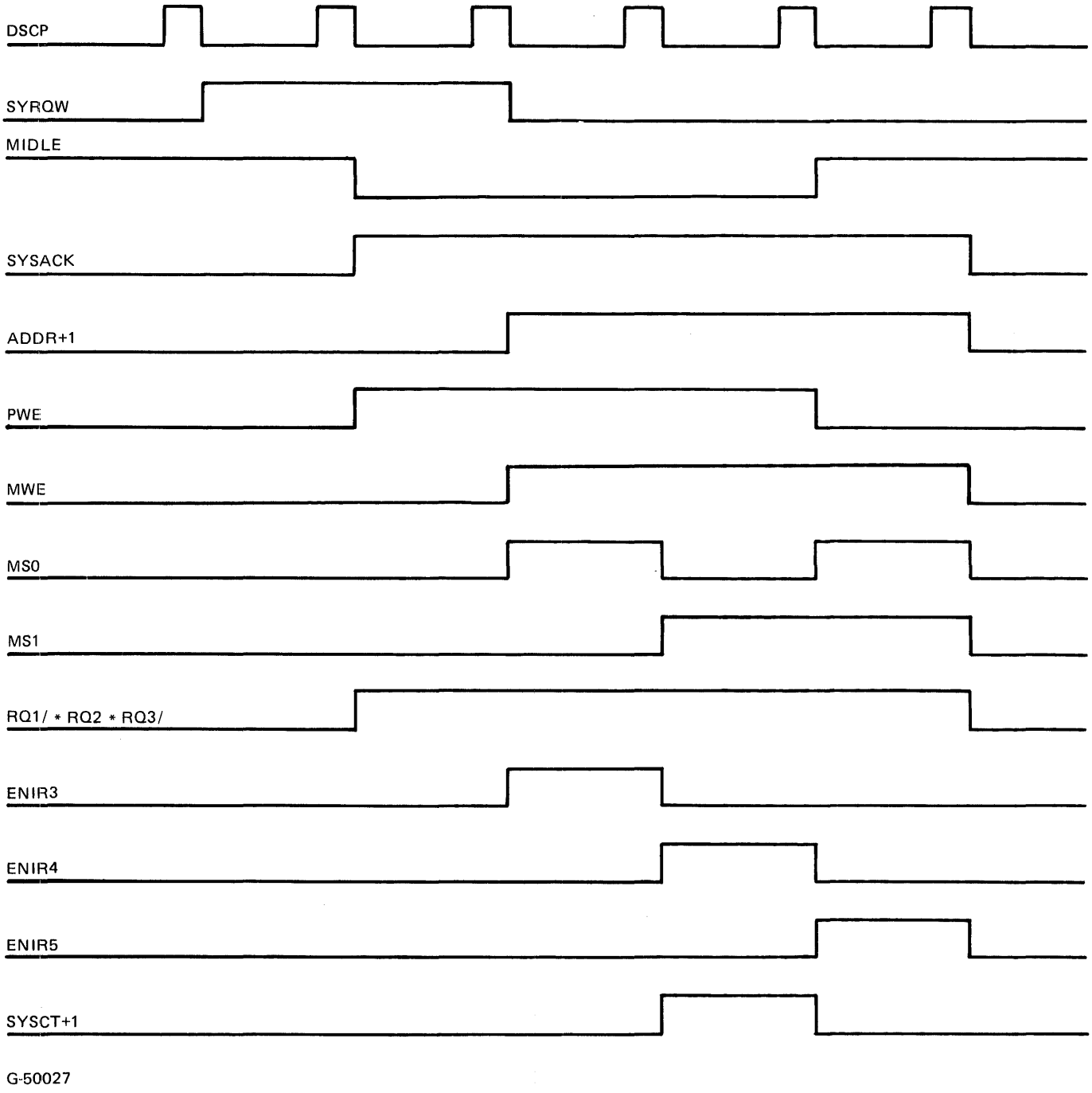

Figure 5-18. RAM System Write

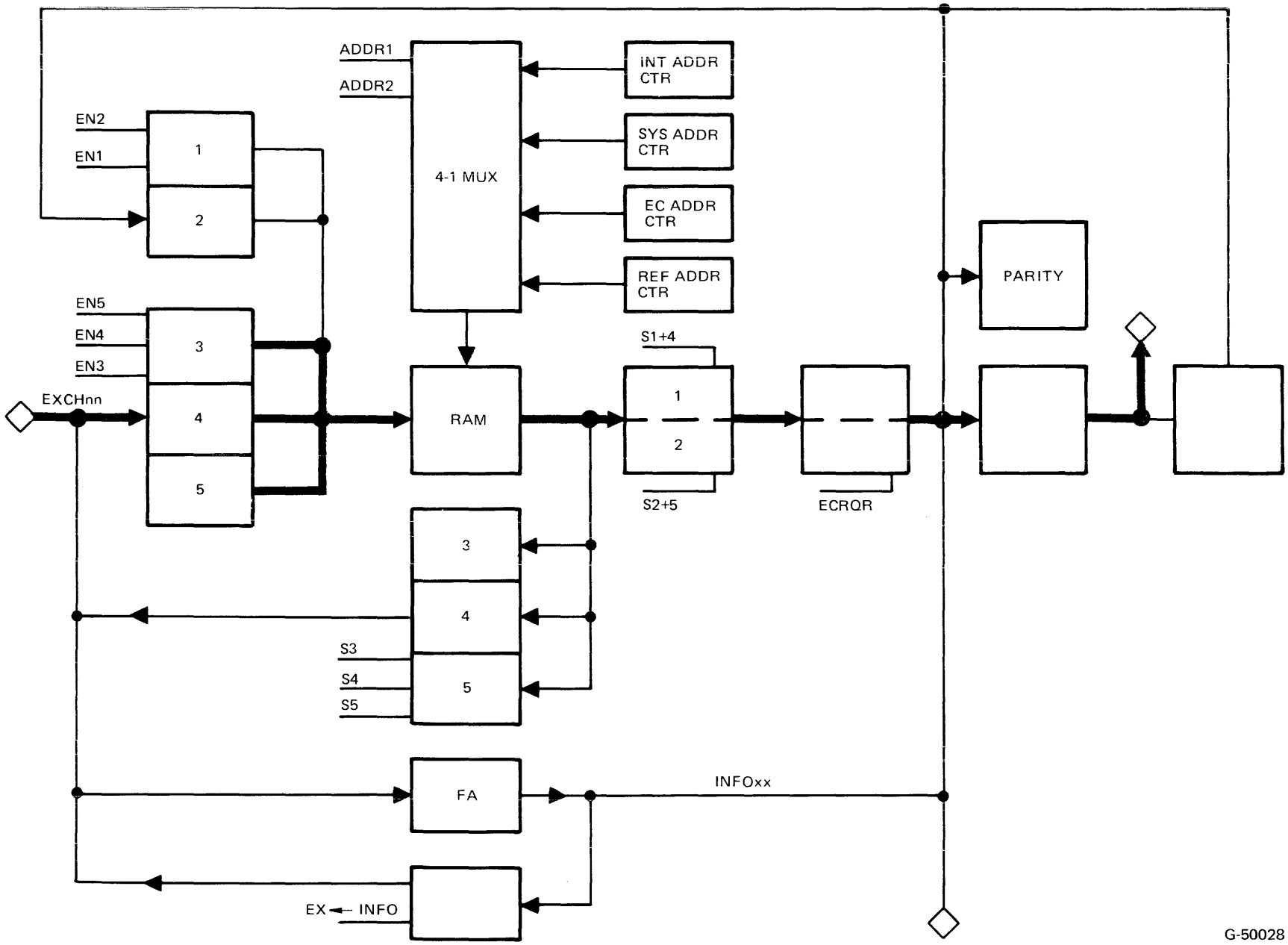

Figure 5-19. Write Data Path

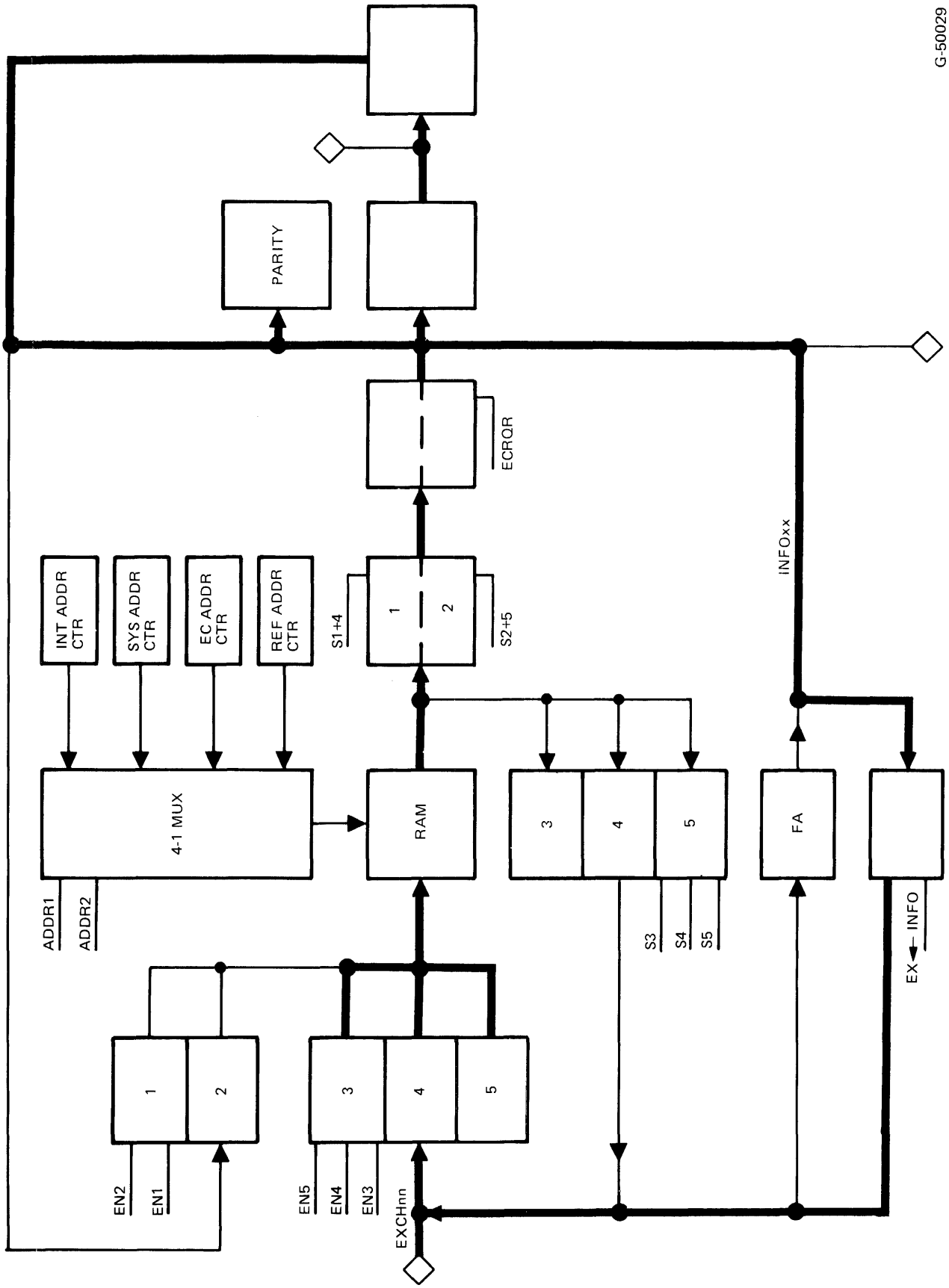

Figure 5-20. Diagnostic Write Data Path

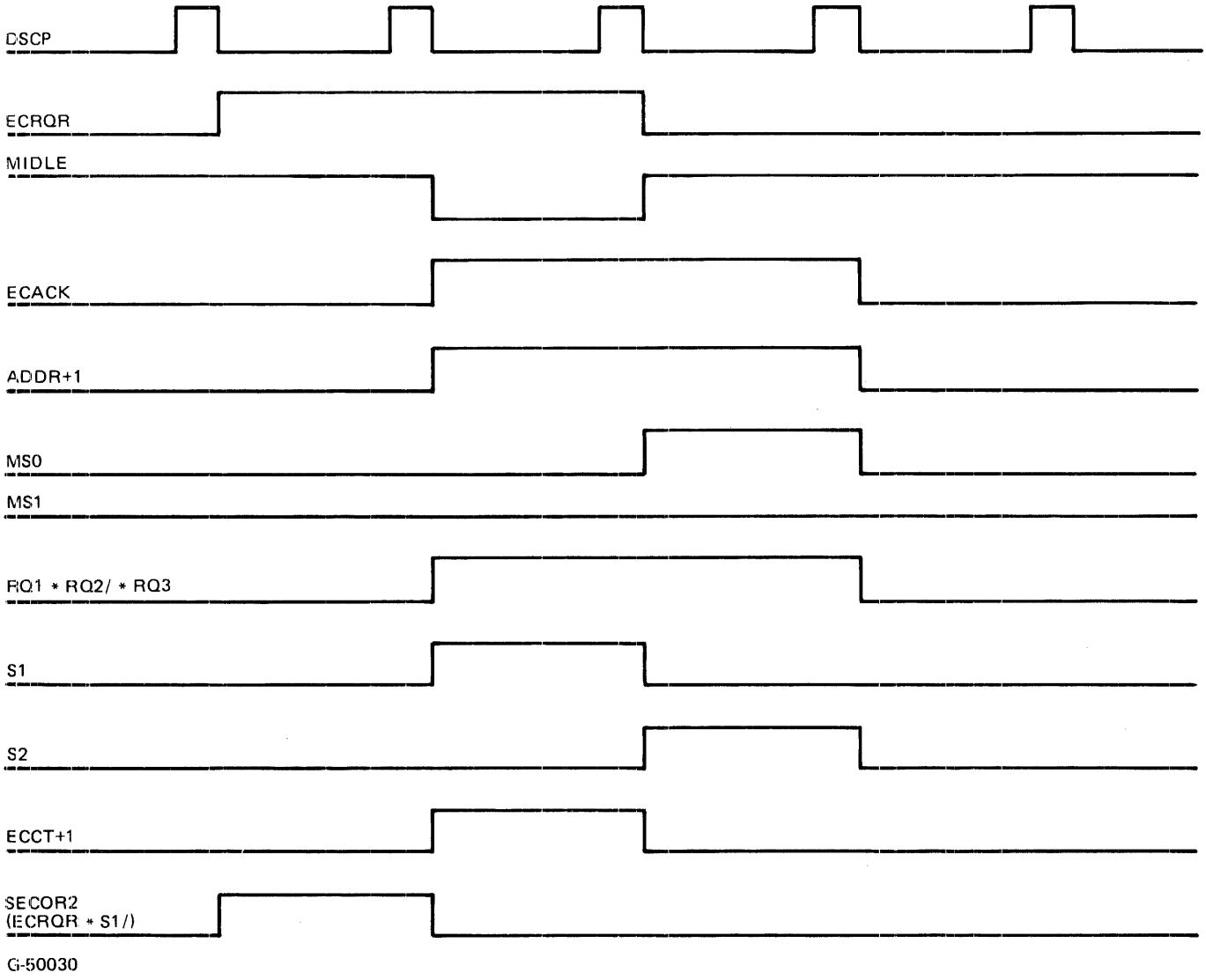

Figure 5-21. RAM EC Read

INTERFACE CLOCK LOGIC

The EC clock is synchronized to the system through the use of two flip-flops connected in series. FF1 and FF2/ give a one system-clock-wide pulse for each EC clock. The unsynchronized EC clock is used directly to strobe data into the LFAN receivers (figure 5-24).

INTERFACE DRIVERS AND RECEIVERS

The interface drivers are eight dual BG-Ns. The receivers are four LFANs which are D-set with each EC clock (figure 5-25).

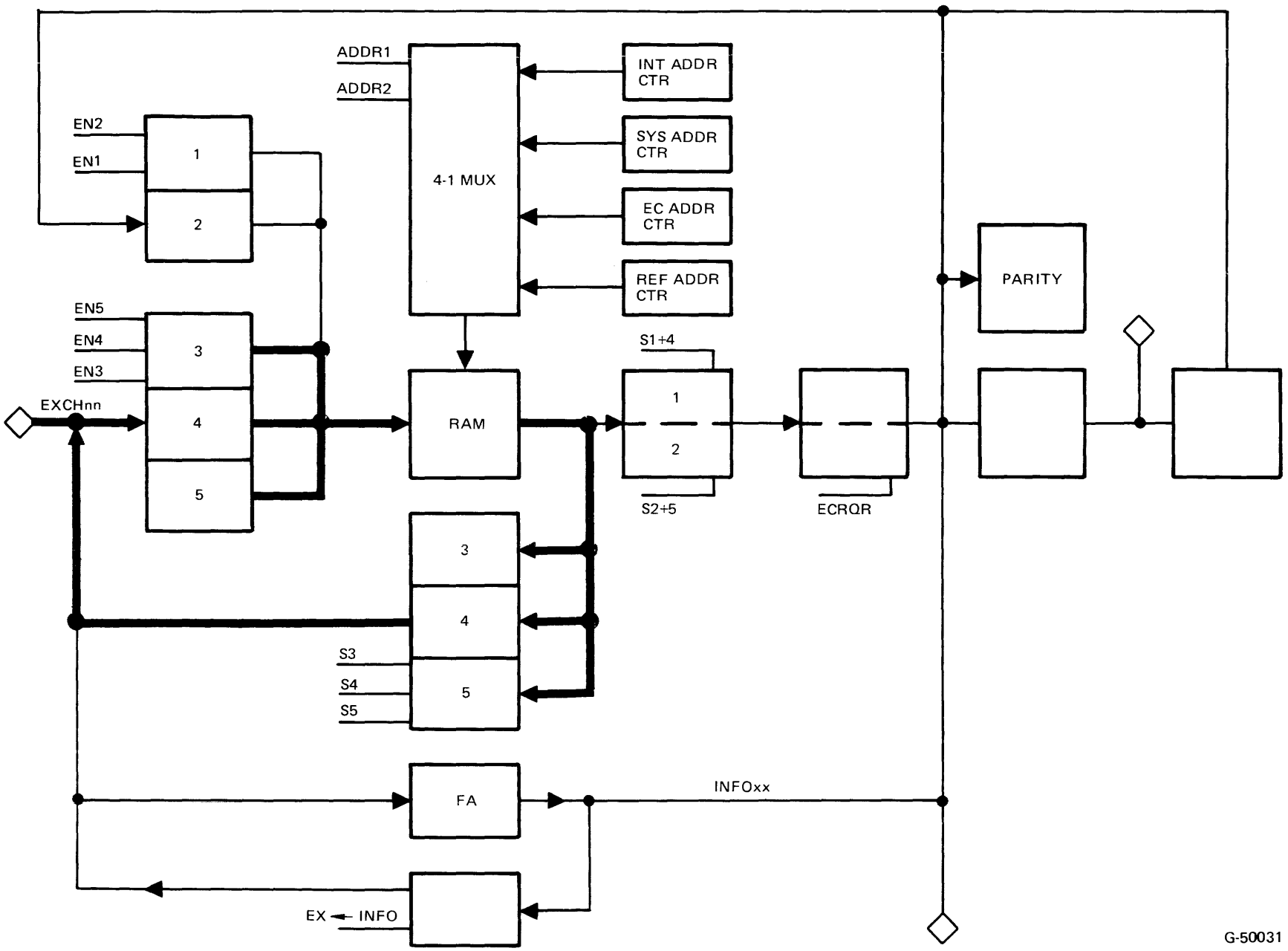

Figure 5-22. Diagnostic RAM Test Data Path

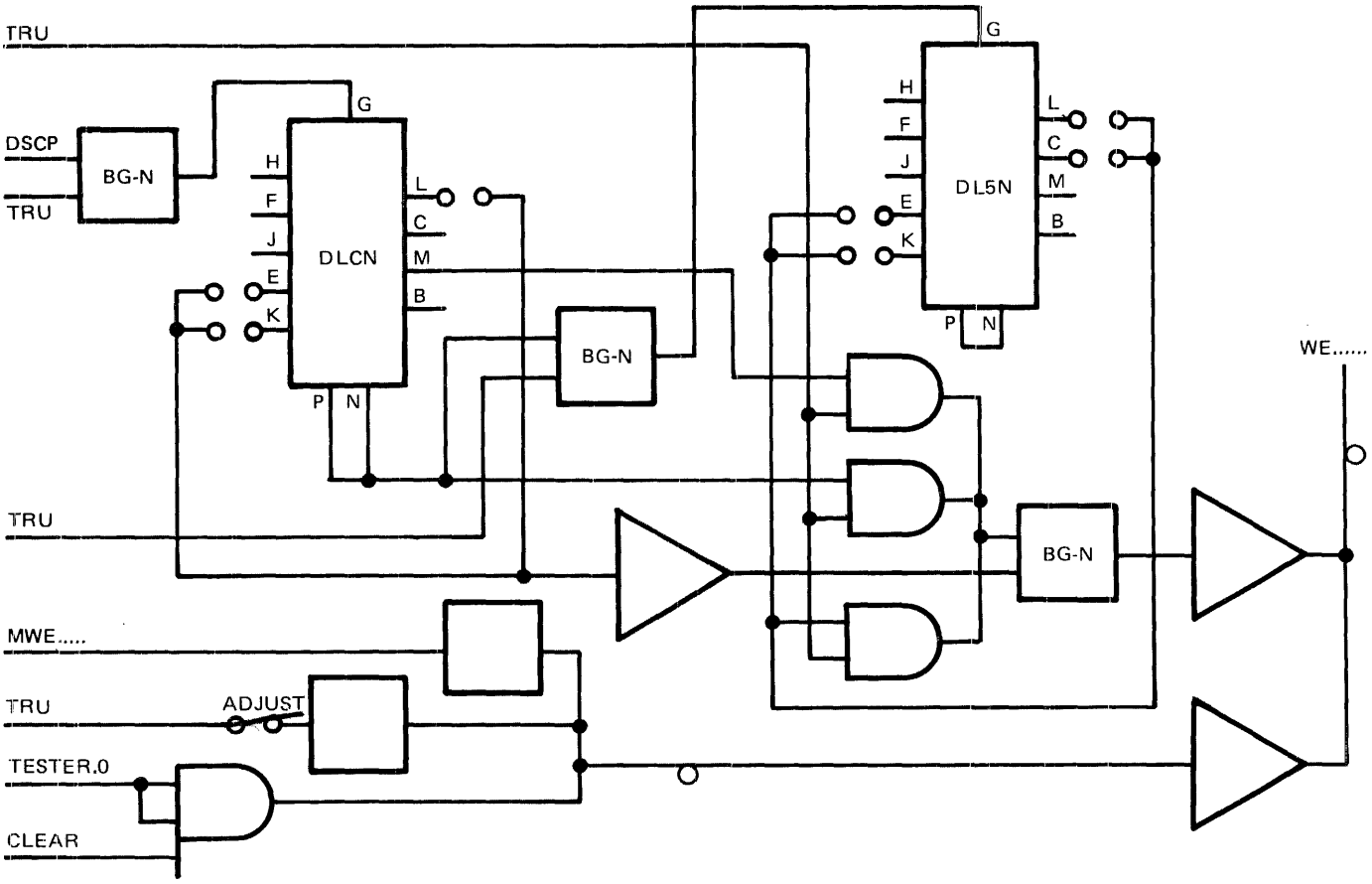

Figure 5-23. Memory Write Enable Generation

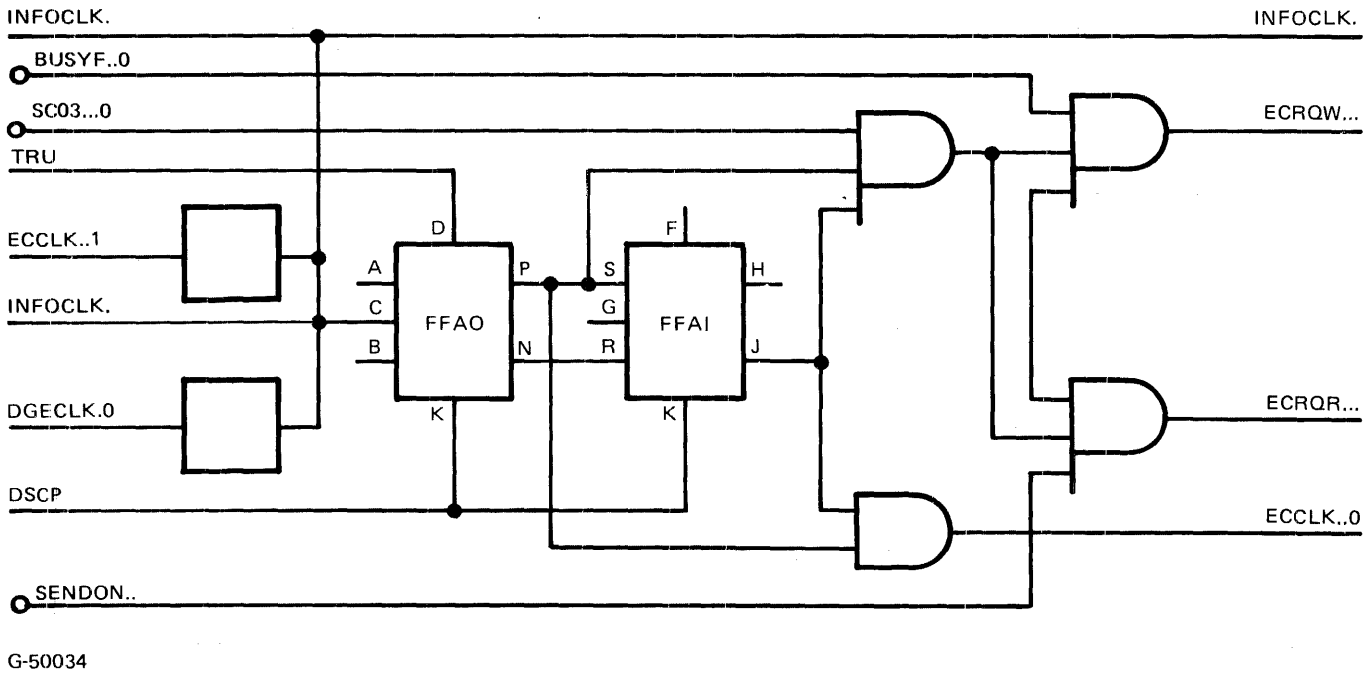

Figure 5-24. Interface Clock Logic

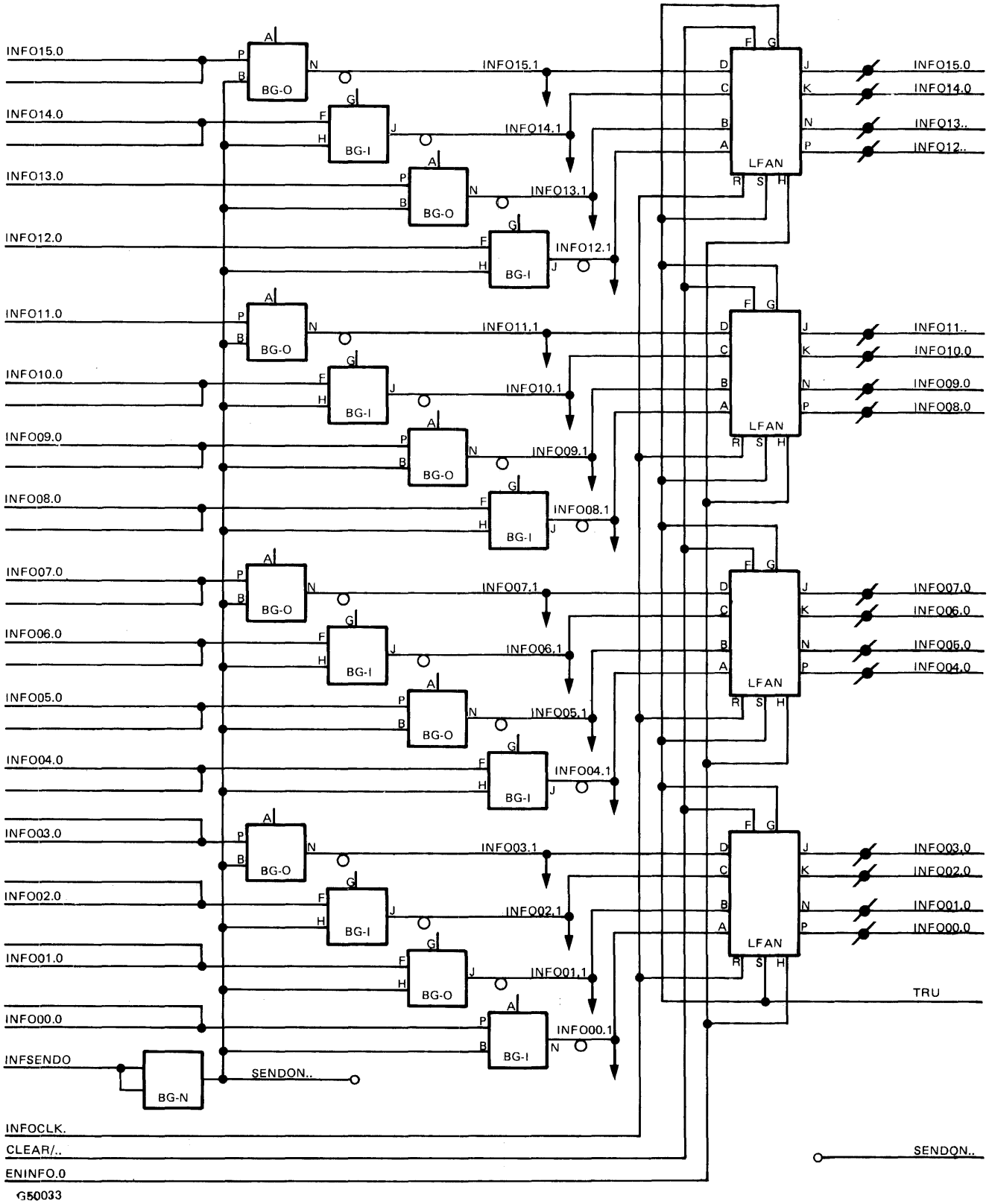

Figure 5-25. Interface Drivers and Receivers

STATUS COUNTER

General

The status counter is composed of two RFANs (counter portion), three DFANs (decode portion) and various CTL gates, buffers, and inverters (control portion). The counter can increment by 1 or 8 or it can D-set to 7. Functions such as STC+2 or STC+3 are accomplished by 2 or 3 STC+1 in succession. As overall status count flow block diagram for DPC-II is shown in figure 5-26.

The status counter (STC00 through STC23) is primarily used to control the flow of data and information between the DPC and the central processor (I/O driver). The function of each status count is described in subsequent paragraphs below.

STC01, 02, 03

If DPC-II has not been initiated by the processor, that is, if it is still in STC01, it goes into a polling mode. It sequentially sends Test operators to each drive connected to the DPEC, looking for a drive in a Seek-Complete status. It continues in this mode until either a drive in a Seek-Complete status is found or an Initiate from the processor is received. If a Seek-Complete status is true the DPC-II raises its service request flip-flop. In response to a TSR, and DPC-II will report what drive is in the seek-complete status.

If an initiate is received from the processor, DPC-II will end the polling sequence by setting the Start FF. DPC-II receives the OP code in STC01, STC02, and STC03.

STC04, 05, 06

DPC-II then receives a file address in STC04, STC05, and STC06. (It goes through the motions of receiving file address even if the OP does not call for one.)

STC07, 08, 09

DPC-II then receives the reference address in STC07, STC08, and STC09 before going to STC10. STC07 also provides logic to set STC64F to 1, if the status counter is not in step with the I/O driver. The out-of-step condition will be indicated in the Test Status phase of the I/O driver.

STC10

Once the DPC is in STC10, the OP code is checked and the control goes to an appropriate sequence count. Except for a Pause OP, the DPC waits for the DPEC to be in an idle state before going to a sequence count. For a Pause OP, the DPC sets the BLOC+PFF when the 1024-usec clock is true and stays in STC10 and SC01 until the next 1024-usec clock. At this time SRF is set and the DPC goes to STC18.

For a Test OP, the DPC goes to SC02. It initiates the DPEC with a Test OP to the drive specified by the OP code and waits for a result. Upon receiving the result, the DPC sets SRF and goes to STC18.

For a Read OP, the DPC goes to SC03, initiates the DPEC and waits for data. If the DPEC must seek, it goes to the result phase and sends a result indicating the seek. The DPC gets this result, sets SRF and goes to STC18. If no seek is needed, the DPEC finds the address and starts sending data to the DPC, which receives it 16 bits at a time and writes it 8 bits at a time to the RAM. After 93 sixteen-bit-transfers (90 data, 2 firecode, 1 result), DPC increments the Buffer Full Counter by one and starts unloading data while continuing to receive data from the DPEC. To unload, the DPC goes to STC15 and transfers 24 bits per RC to the processor. (For Read-Maintenance or Read Diagnostic, the DPC receives all data before transferring any to the processor.)

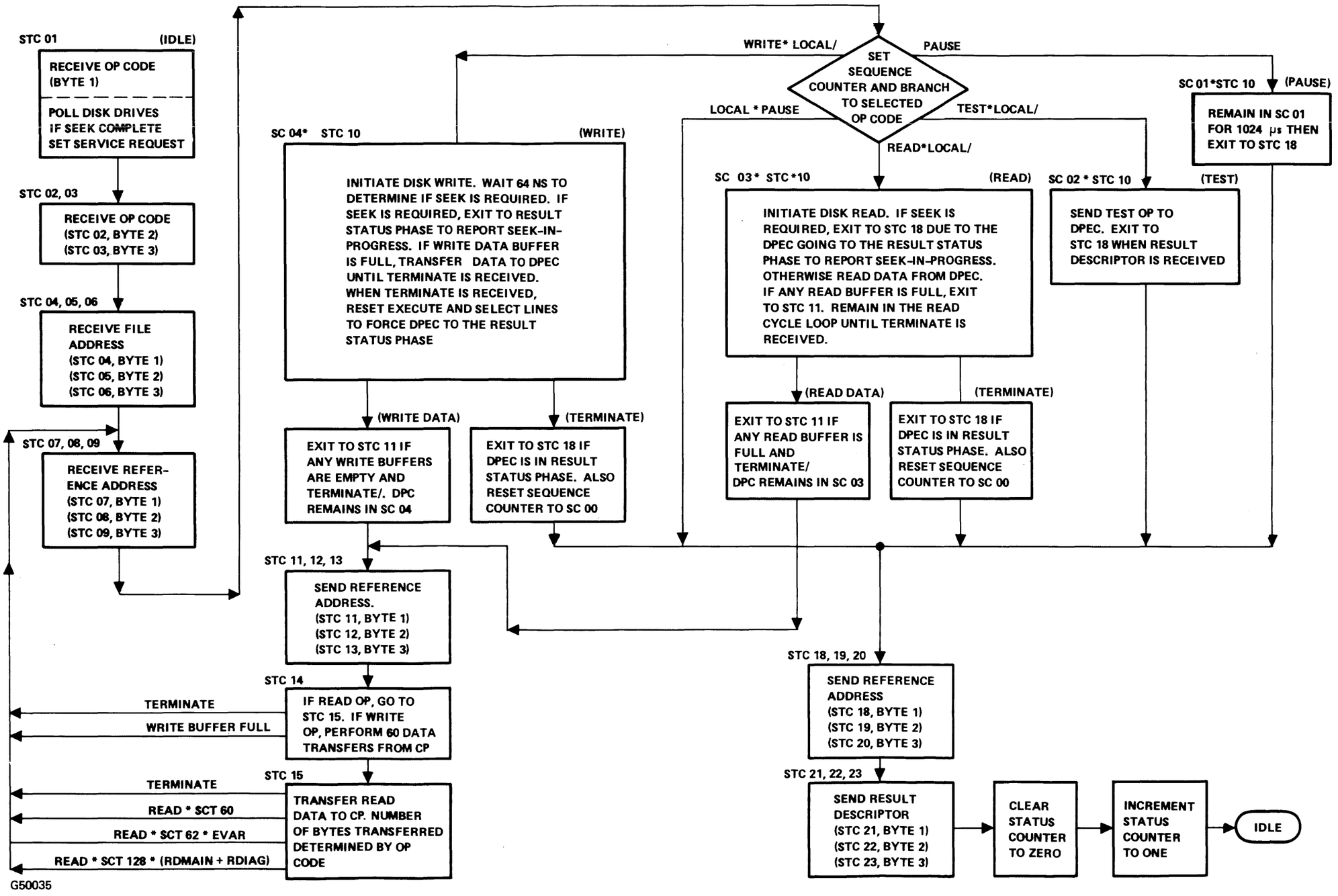

Figure 5-26. Disk Pack Control-II Flow (Detailed)

After making the required number of transfers (Read, 60; Read with E=1, 62; Read Maintenance or Read-Diagnostic, 128 or until terminated), the DPC returns to STC10 and decrements the Buffer Full Counter. If another sector has been loaded from the DPEC and the current OP has not terminated, the DPC returns to STC15 and sends the other sector to the processor. This procedure continues until a terminate is received from the processor.

If the RAM ever fills up, the DPC drops the Execute line and goes into the slip mode where it remains until the RAM empties.

When terminate is received, DPC goes to STC10, does system memory reads until the address counter is pointed at the result associated with the terminated section, and goes to STC18.

The DPC goes to SC04 for an initialize, Relocate, or Write OP. It receives the OP codes, field address and reference address as for a Read OP. Once in STC10, it waits for the DPEC to go idle before going to SC04. In SC04, it initiates the DPEC with the appropriate OP code and starts a timer. If the DPEC has not gone to the result phase after 64 microseconds, a seek is not required and the DPC goes on to STC14 to receive data from the processor. Data is received 24 bits per RC until 60 transfers or terminate. The DPC increments the Buffer Full counter, then returns to STC10 and begins sending data to the DPEC.

While sending, the DPC returns to STC14 to receive another sector. (On Initialize or Relocate, the DPC stays in STC10 until the DPEC terminates the OP.) This loop continues until the processor terminates the OP. If the RAM empties, the DPC drops the Execute line and goes into slip mode until another sector of data is loaded into the RAM.

When the processor terminates the OP, the DPC finishes unloading the RAM to the DPEC, gets a result from the DPEC, goes to STC18, and returns the reference address and result descriptor to the processor.

STC11, 12, 13

The DPC returns three bytes of the reference address to the processor.

STC14

The DPC receives up to 90 bytes (one sector) of write data from the processor. During a write operation, STC14 is used only to provide STC+1 to go to STC15.

STC15

The DPC sends up to 180 bytes of data to the processor for a normal read OP, 186 bytes of data for a read OP with E-variant equal to 1 or 384 bytes for a read diagnostic OP.

STC18, 19, 20

The DPC returns three bytes of the reference address to the processor.

STC21, 22, 23

The DPC returns three bytes of result status information to the processor.

SEQUENCE DECODER

The Sequence Decoder (SC00 through SC04) is used to provide the necessary logic for the flow of information and data between the DPC and the DPEC. The function of each of the sequence counts is described below:

Sequence Count	Function
SC00	Used as the Idle state for the sequence counter
SC01	Provides a 1024-*m*s delay for a Pause operation. At the end of this delay the sequence counter is set to SC00, the status counter is set to STC18 and the service request flip-flop is set to one
SC02	The test operator is transferred from the DCP to the DPEC. When the test operator result descriptor is received from the DPEC, the sequence decoder is set to SC00 and the status counter is set to STC18
SC03	Used for a read operation. The operations that occur during SC03 are described in the following paragraphs: a. The first time that the DPC is at STC10*SC03 for any read operation, the OP code and file address are transferred from the DPC to the DPEC. b. If a seek operation is required, the DPEC goes to the result status phase. The result status phase consists of the following DPEC logic: (SELECT*BUSY*READY/). The DPEC then transfers a 2-byte result descriptor to the DPC. Upon receipt of the DPEC result descriptor, the DPC sets the status counter to STC18 and the sequence decoder to SC00. c. The first time that the DPC is at STC10*SC03 for a read operation and the seek operation is completed, the OP code and file address are transferred from the DPC to the DPEC. The DPC then waits for read data to be transferred from the DPD through the DPEC to the read buffers d. If any read buffer becomes full while the DPC is at STC10*SC03, the status counter is incremented to STC11. In addition, a service request flag is set (SRF ◄- 1) indicating to the I/O driver that a buffer full of read data is available for transfer to the I/O driver. The status count, however, remains at SC03 to provide Read gating between the DPEC and the DPC e. Read data, transferred from the DPEC in two-byte (16-bit) increments, must be stored in the DPC's RAM in 1-byte (8-bit) increments. The Read data conversion and shifting from the DPEC to the DPC is controlled by the memory address counters, memory address selection, memory control logic, memory write enable generation logic, and the system-synchronized EC clock f. When a terminate signal is received in the DPC, it sets the terminate flip-flop (TERMF). The terminate flip-flop is used to notify the DPEC to go into the result status phase by setting the select signal false. During the result status phase, the DPEC transfers a two-byte result descriptor to the DPC. Upon receipt of the DPEC result descriptor, the DPC sets the status counter to STC18 and the sequence counter to SC00. The terminate signal is normally used to end a read operation g. During SC03, if all three read buffers are full, the DPEC goes into a slip mode operation

Sequence Count	Function
SC04	Used for a write operation. The operations that occur during SC04 are: a. The first time that the DPC is at STC10*SC04 for any Write operation, the OP code and file address are transferred from the DPC to the DPEC (initiate word one and initiate word two). When initiate word two is transferred from the DPC to the DPEC, a 64-microsecond timer (TIMERF) is set. b. If a seek operation is required, the DPEC goes to the result status phase. The DPEC then transfers a two-byte result descriptor to the DPC. Upon receipt of the two-byte DPEC result descriptor, the DPC does the following: sets the status counter to STC18, sets the sequence decoder to SC00, resets TIMERF, and sets the service request flip-flop to 1. c. The first time that the DPC is at STC10*SC04 for a Write operation, and the Seek operation is complete, the operation code and file address are transferred from the DPC to the DPEC. When the last 14 bits of the file address are transferred from the DPC to the DPEC, the 64-microsecond timer (TIMERF) is set. When TIMERF times out, the status counter is incremented to STC11. However, the sequence counter remains at SC04 to provide write gating between the DPC-II and the DPEC. d. The Write buffers are filled with write data during STC14. As soon as any write buffer is filled with write data, write gating is enabled. The write data is transferred from the write buffers through the DPEC to the selected DPD. e. Write data is transferred from the write buffers in one-byte increments. Write data to the DPEC, however, must be provided in two-byte increments. The write data shifting and converting from one-byte to two-byte increments is provided by the associated logics used in SC03 for a read OP. f. If any write buffer is empty while the DPC is at STC10*SC04, the status counter is incremented to STC11. However, the sequence counter remains at SC04 to provide write gating between the DPC and the DPEC. g. When a terminate signal is received in the DPC, it sets the terminate flip-flop (TERMF). The terminate flip-flop is used to notify the DPEC to go into the result status phase. During the result status phase, the DPEC transfers a two-byte result descriptor to the DPC-II. Upon receipt of the DPEC result descriptor, the DPC-II sets the status counter to STC18 and the sequence decoder to SC00. The terminate signal is normally used to end a Write operation. h. During SC04, if all of the write buffers are empty, the DPEC goes into slip mode of operation.

Entering the slip mode is accomplished by the DPC setting the execute level false. This occurs under the following conditons:

a. If the DPC is executing a read operation and all three read buffers are full

b. If the DPC is executing a write operation and all three write buffers are empty

When the necessary transfers between these buffers and I/O driver occur, the DPC sets the Execute level true. The first address coincidence in the DPEC with select, busy, ready, and execute true provides the logic to exit the slip mode and resumes reading or writing.

PARITY LOGIC

Odd parity is generated and checked through the use of four CTL AFANs. Bad parity can be generated by setting exchange line 4 with a diagnostic command (figure 5-27).

FILE ADDRESS REGISTER

The file address register consists of LFANs and FFs. It is set in STC04, STC05, and STC06. It is enabled during the initiate phase to the DPEC (figure 5-27).

SYSTEM AND EC COUNTERS

The system and EC counters (figure 5-28) consist of CR4Ns and gates. The system counter is used to determine when a sector of data has been transferred between the system and RAM, and it is incremented by one with each system request for a read or write. Since data is transferred three bytes at a time, its maximum count is 62. The EC counter is used to determine when a sector of data has been transferred between the EC and RAM. The maximum count of the EC counter is 94. The EC counter is also used as a timer to determine whether or not a seek is going to be done by the drive on a write OP. If (after 64US from initiation) the DPEC has not terminated the OP, the DPC requests write data from the processor.

BUFFERS FULL COUNTER

The buffers full counter (figure 5-28) is composed of a RFAN and DFAN. It is incremented whenever the system or EC counters indicate a sector of data has been entered into the RAM and is decremented whenever the counters indicate a sector of data has been unloaded from the RAM. It counts up to five buffers and is used to determine when slip is required and when all data has been transferred.

OPERATION REGISTER

The operation register holds the basic OP code, variants and unit selection. It consists of LFANs and a RFAN for unit selection. The LFANs are loaded in STC01, STC02, and STC03. The unit selection RFAN is also used in the polling of the drives for seek complete.

COMMAND AND COMMAND VARIANT REGISTERS

Both the command and command variant registers consist of one RFAN and one DFAN. The commands recognized are XFROTA, XFROTB, XFRIN, and XFRINC. The variants are TERM, TSTCLR, TESTS, and TSR.

DIAGNOSTIC LOGIC

The diagnostic logic consists of a diagnostic mask register and a diagnostic variant register. There are also four LFANs for enabling the information bus onto the exchange lines.

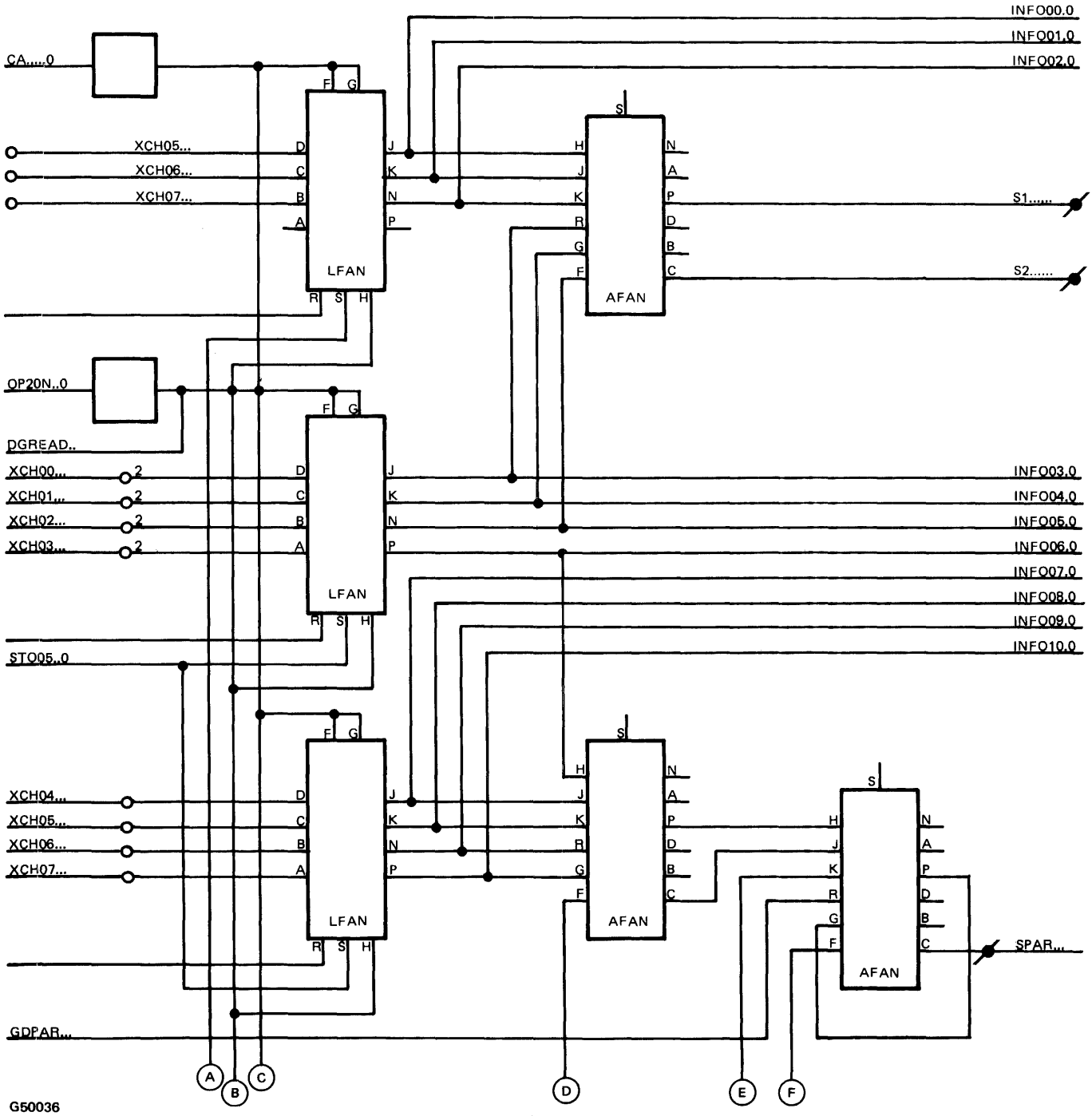

Figure 5-27. Parity Logic and File Address Register (Sheet 1 of 2)

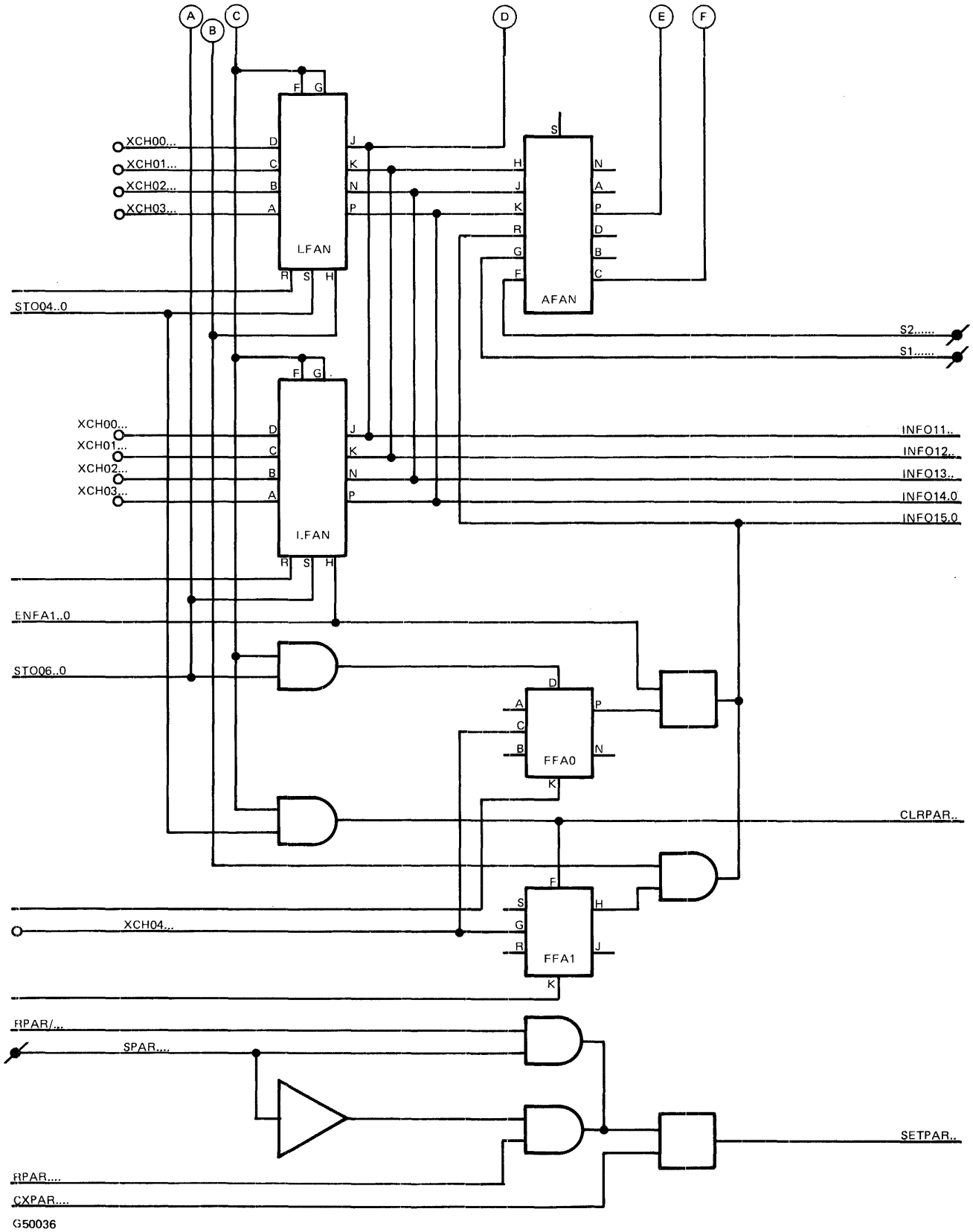

Figure 5-27. Parity Logic and File Address Register (Sheet 2 of 2)

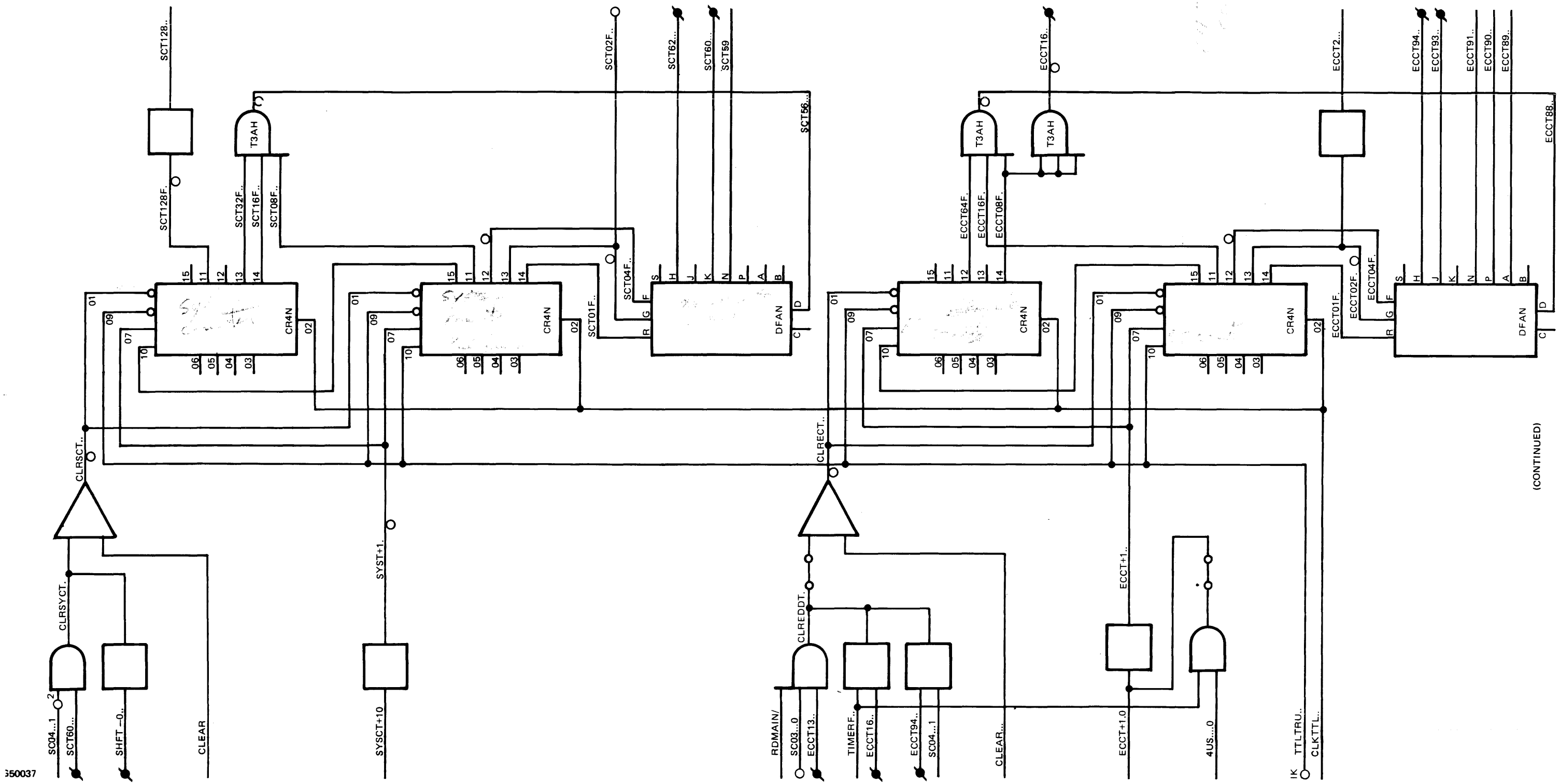

Figure 5-28. System, Buffer Full, and EC Counters (Sheet 1 of 2)

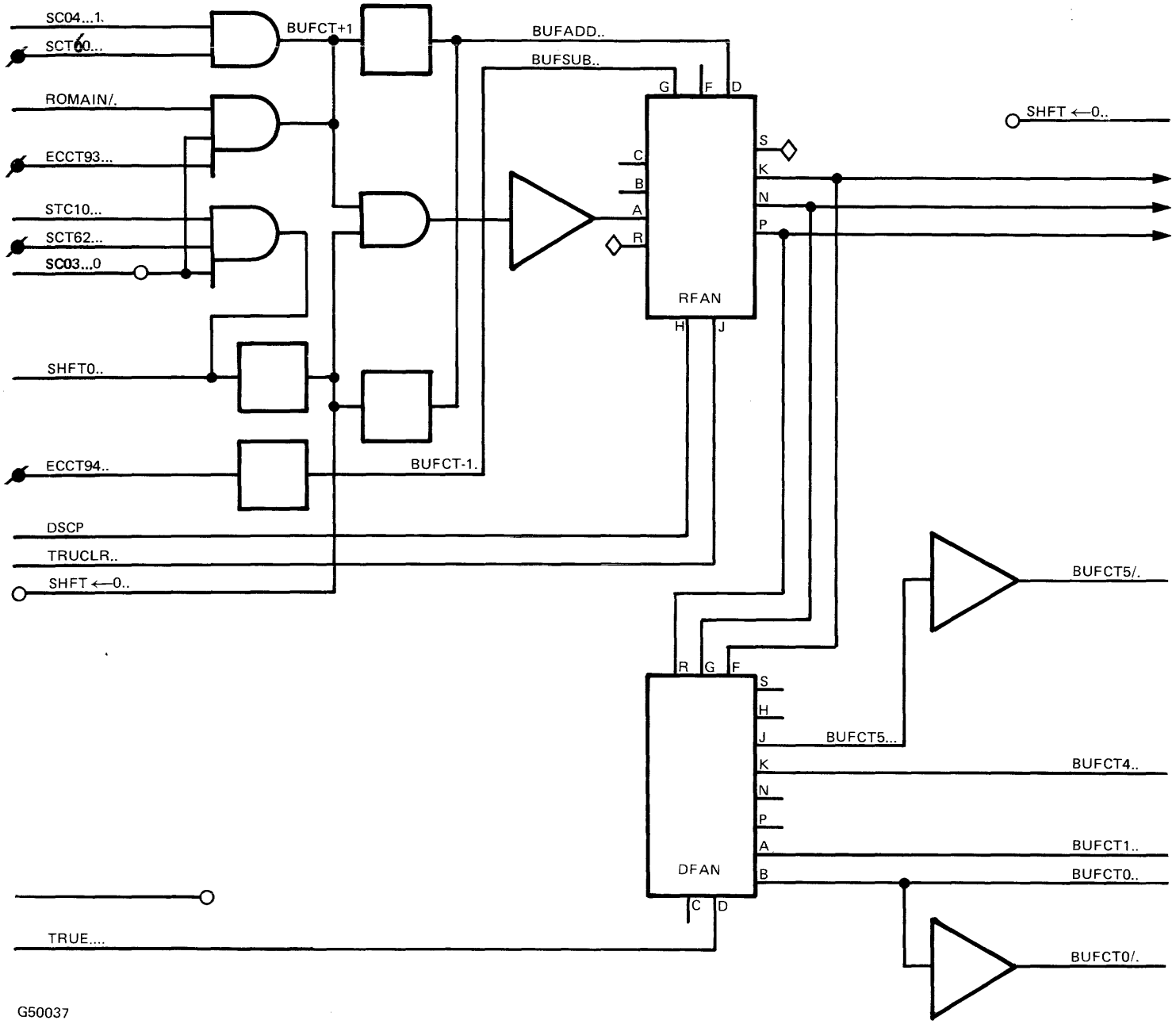

Figure 5-28. System, Buffer Full, and EC Counters (Sheet 2 of 2)

The available diagnostic commands are those listed below:

BASIC COMMAND

EXCH 22	EXCH 21	EXCH 20	
0	0	0	DIAGNOSTIC COMMAND

DIAGNOSTIC MASK

EX.7	EX.6	EX.5	EX.4	
X	X	X	1	BAD PARITY
X	X	1	X	DIAGNOSTIC READY
X	1	X	X	DIAGNOSTIC READ
1	X	X	X	DIAGNOSTIC MODE

X = Don't care — 1, or all may be set

DIAGNOSTIC VARIANT

EX.2	EX.1	EX.0	
0	0	0	DIAGNOSTIC ECCLK
0	0	1	ENINFO
0	1	0	INF ◄— MEM
1	1	0	EX ◄— MEM
1	1	1	DG LOAD

ENINFO enables the EC receiving register onto the information bus and places the information bus onto the exchange lines. INF ◄— MEM places the contents of ECOR2 onto the information bus and the information bus onto the exchange. EX ◄— MEM places the contents of exchange OR onto the exchange. At RC time, a SYROR is issued. DGLOAD loads the IR and issue a SYNRQW at RC time.

CONTROL FLIP-FLOPS

A list and description of the control flip-flops follows:

CAL — CA latch flip-flop. Active for one clock following CA. If active in STC15 with XFRIN it clears command register. Used to terminate multiple RC loop.

DATAF — Set with any ECCLK in data mode. Used to determine whether or not data transfer took place.

EXITF — Set with ECCLK in result phase. Tells the control that a result has been received and it can exit to STC10.

SLIPF	—	Set when EXECUTE dropped.
SLIPR/D	—	Set when EXECUTE turned on and SLIPF has already set. Indicates a slip has occurred.
STARTF	—	Set with first XFROTA command. Stops polling sequence.
TIMERF	—	Used in 64-*m*sec timeout to determine if write OP is to be done.
BLOC+P	—	Blocks incrementing of EC memory address counter while EC is writing firecode. Also used in pause OP.
OKTOEXC	—	Used to get data set into ECOR1 and ECOR2 at beginning of each write sector. OKTOEXC and ECCT2 sets EXECTE.

DPC-II

MEMORY CONTROL