SERIES B9480/81-12

DISK CARTRIDGE DRIVE

TECHNICAL MANUAL

THIS MANUAL REPLACES ALL PREVIOUS ISSUES OF FORM NO 1054392

Burroughs

FIELD ENGINEERING

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INTRODUCTION AND OPERATION

INTRODUCTION

This manual contains the theory of operation for both the model 9480-12 (100 t.p.i.) and 9481-12 (200 t.p.i.). The theory in this manual refers to both models, unless specific exceptions are stated. The differences in the two drives are as follows(see figure 1-1):

A/B 9480-12	Two spindles per cabinet 100 tracks-per-inch 203 tracks per surface Storage Capacity 2.339 megabytes per drive module
A/B 9481-12	Two spindles per cabinet 200 tracks per inch 406 tracks per surface Storage Capacity 4.677 megabytes per drive module

SCOPE

This manual is intended to serve mainly as a reference for customer service engineers, but may also be used by other technical personnel requiring knowledge of the 9480/81-12 operation.

DESCRIPTION

The 9480/81-12 Disk Cartridge Drive consists of a single cabinet containing two separate random access drive modules, a Common Electronics Module, and a common power supply.(See figures 1–2 and 1–3.)

The recording medium is a magnetic oxide-coated disk, mounted inside a plastic container to prevent contamination by dirt or dust. This complete assembly, known as a 'cartridge', is completely demountable and any number can be stored off-line for use as desired.

Storage and retrieval of information recorded on the disk is by means of two read/write heads in each drive module. These fly on an air bearing, formed by a stream of air arising from the rotation of the disk, in very close proximity to the oxide recording surface.

Due to the random access property of the disk cartridge drive, information on the disk is stored in discrete, logical entities known as sectors.

Sectors are arranged in serial form in 203 (9480-12) or 406 (9481-12) evenly-spaced tracks on each disk surface. When a head is stationary over one track, each revolution of the disk therefore brings each sector in that track sequentially under the read/write heads. The heads are rigidly attached to a moving carriage, and accurately aligned to each other, such that if the upper head is, for example, located over track 100, then the lower head will also be located over track 100 on the lower disk surface. Because of this, the heads are often said to be positioned to a 'cylinder', this being the combination of the track addressed on both upper and lower disk surfaces. There

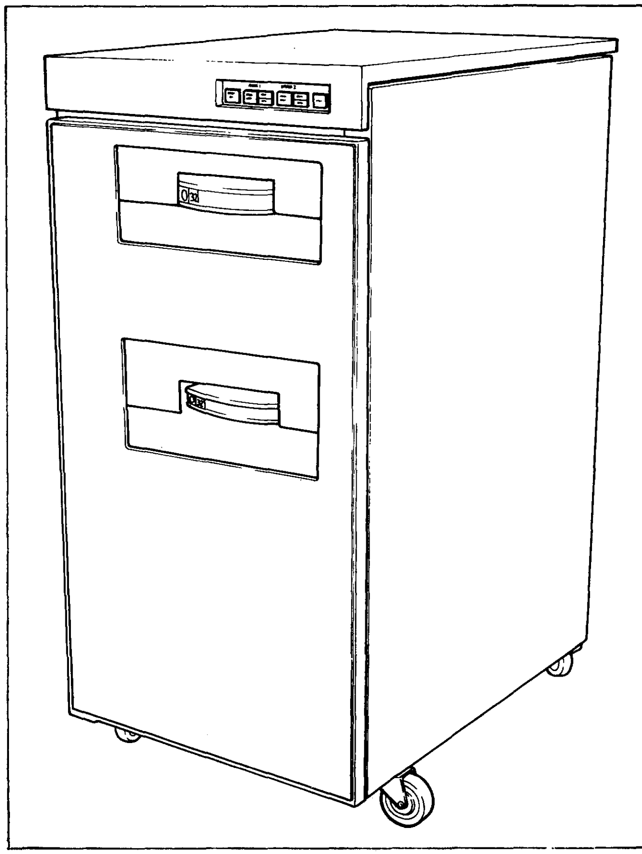


Figure 1–1. Burroughs 9480/81–12 Disk Cartridge Drive

are 32 sectors in each track, defined by slots physically cut into the rim of the disk hub, and each sector can store 180 bytes (1 byte = 8 bits) of information.

Movement of the heads and carriage from one cylinder to another is performed by a servo-positioning system, which consists of a coil to which the carriage is attached, moving in a permanent magnet under the control of the drive electronics, and traversing a guide. Coarse position information is provided by a linear potentiometer (or 'Markite Strip'), and fine position information by an optical detent assembly.

The location of an individual sector address is, however, the function of the host system, in response to timing pulses provided by the drive from the sector slots cut into the disk hub.

Cartridges are inserted into, and removed from the drive by means of a receiver assembly and handle. When inserted into the drive, a magnetic chuck on the drive spindle clamps the disk into place and a spring-loaded bail arm automatically opens the cartridge door to allow access from the heads onto the disk. Safety interlocks are provided to prevent the cartridge being inserted or removed whilst the spindle motor is rotating or the heads positioned over the disk surfaces. A further interlock detects the position of a plug in the cartridge housing, which can be used to prevent the drive from writing on disks which contain irreplaceable information. ('Write Lockout' plug).

A smoked-glass door covers the frontal drive area, and this can be opened by an operator-controlled button. A.C. and D.C. power for both drive modules is provided from a power supply located in the base of the cabinet.

Also located in the base of the cabinet is a clean air unit, the purpose of which is to force a stream of finely-filtered air to both drive modules and thence over the disk/head surfaces.

A clean air unit can also be fitted as an option to earlier 9480-12 models. (See Reliability Improvement Notice No. R4392-028 Revised).

The electronics and logic are packaged onto printed circuit boards, which are as follows:

Mounted in the base of the cabinet, and common to both drive modules:

- Common Electronics Module
- Power Supply

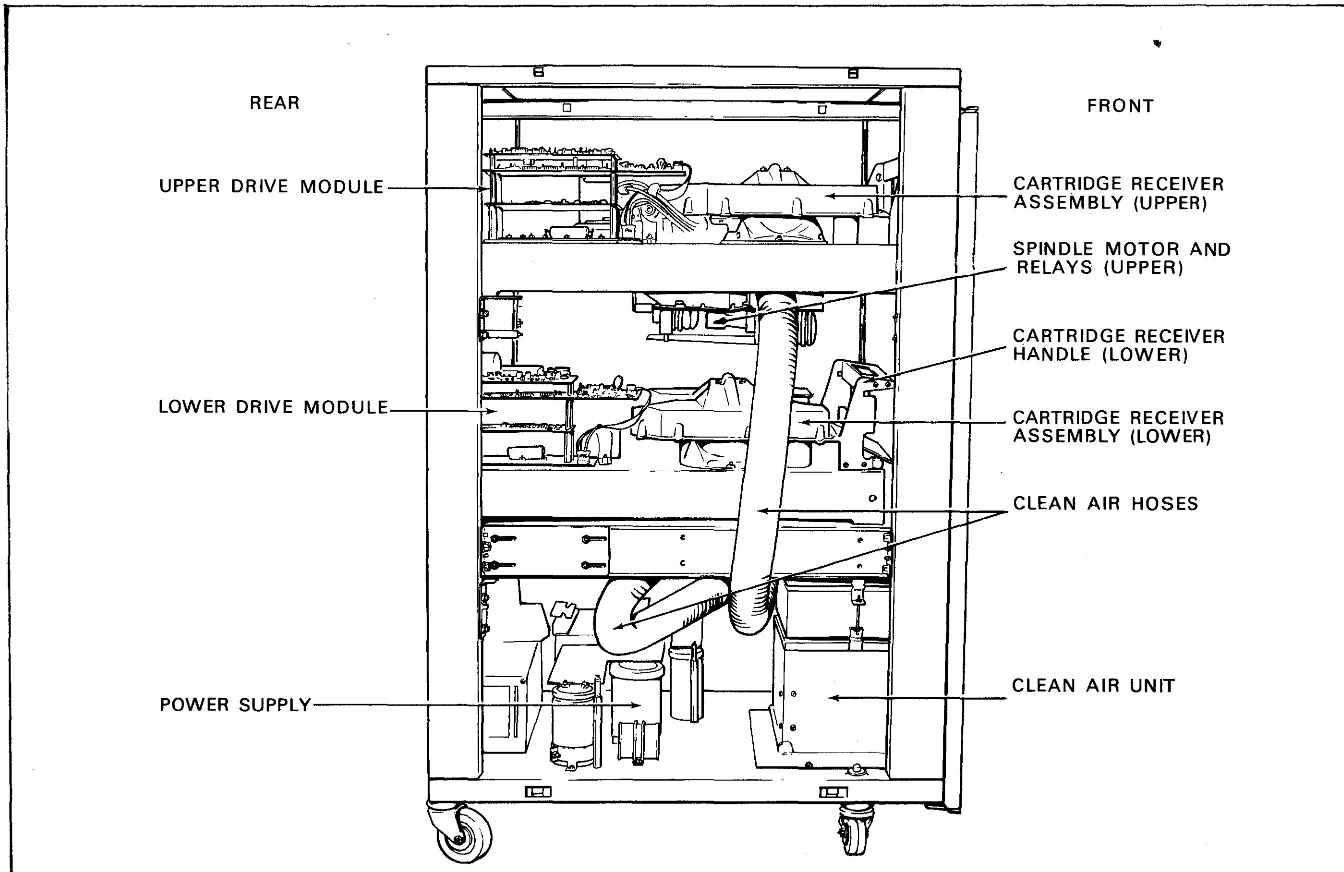


Figure 1-2. Side View of Drive Cabinet (Panel Removed)

Mounted on individual drive modules:

9480-12	Read/Write Amplifier Servo Control Module Power Amplifier Module
9481-12	Read/Write Amplifier Servo Control Module 1 Servo Control Module 2 Power Amplifier Module Temperature Compensation

BASIC OPERATION

From the foregoing description, it can be seen that before information can be stored on or retrieved from the disk, an operation must be performed to move the heads to the desired cylinder. This operation is called a 'seek', and a typical sequence of events in an on-line condition would be as follows:

1. The host system selects the correct drive module in the cabinet, and issues a seek command together with the binary cylinder address (see figure 1-17).
2. Under the control of the positioning system, the heads will move until located at the desired cylinder.
3. The drive informs the host system that the heads are correctly positioned at the desired cylinder.
4. The host system selects the relevant disk surface by enabling one or other of the read/write heads.
5. The host system issues a read command to locate the required sector on the track just selected.
6. When the desired sector is found, the host system will either:

   Continue with the read command and the drive will send the information required, or

   Issue a write command, and send to the drive the information to be written.

APPLICATIONS

The most common application is memory expansion in small scale computers. A typical system would use dual drives with one disk being used to provide

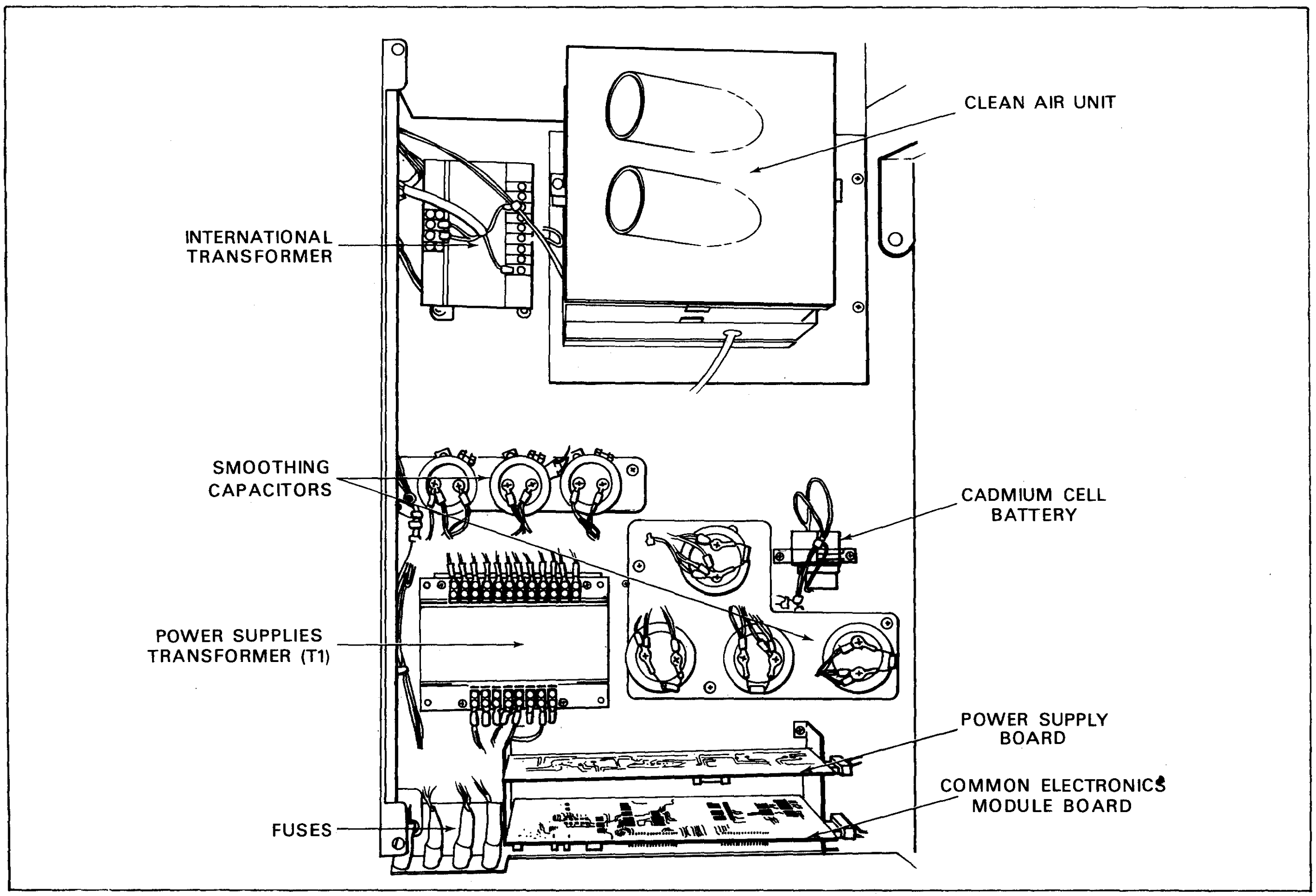


Figure 1-3. Plan View of Power Supply Area

the system with software and user programs; the remaining drives could then be used to contain working files such as inventory, payroll, sales etc. In this application, the software cartridge is a semi-permanent fixture, while the user would select the data cartridges according to the programs he wishes to run.

The main advantage of random access processing is the ability to access any record within a file without having to read the entire file. This is made possible by the fact that each sector has an address and is located at a unique position on the disk. When a system requires to read or write a sector, the controller will instruct the disk unit to position the heads over the correct track, locate the desired sector within that track, and perform the read or write operation.

NOTE

Only a complete sector of information may be written or read. If insufficient data is present in a record to completely fill a sector, then the remainder of that sector is filled with zeroes.

PHYSICAL CHARACTERISTICS

Height (including castors)	44 inches (112 cm)
Width	22 inches (56 cm.)
Depth	30 inches (76.1 cm.)
Weight	363 lbs. (161 kg.)
Shipping Weight	384 lbs. (171 kg.)

POWER SUPPLY

International units are provided with a multi-tap transformer, which provides selection of the following voltages:
100, 110, 115, 125, 200, 220, 230, 240, 250.

This transformer also supplies A.C power to the clean air unit and drive motors.

U.S. Domestic machines do not have this transformer, and only one input voltage is provided for 120V.

A step-down transformer is provided in all units for use in the generation of D.C. voltages via rectifier and regulation circuits.

POWER REQUIREMENTS

	U.S. Domestic	International
Frequency	50/60 Hz	50/60 Hz
Line Voltage	120V ± 10%	100-250V
Line Current	5A	3-5A
Phase	Single	Single
Number of Wires	2 plus ground	2 plus ground
Frequency tolerance	±1%	±1%

OPERATING CHARACTERISTICS

Access Motion Time (including settle time)

	9480-12	9481-12
Track-to-track	13mS	37mS
Average Random	60mS	82mS
Maximum Access	85mS	105mS
Average Latency Time	20mS	20mS

Maximum Packing Density	2200 bits per inch
Disk Rotational Speed	1500 r.p.m.
Bit Transfer Rate	1.55 MHz

Operating Environment:

Temperature	50° F-100° F
Humidity	10%-85%
	R.H. = 85% max net bulb

TOP UNIT NUMBERS

9480-12

2155 1841	60 Hz U.S. Domestic
2155 1866	50 Hz International
2155 1858	60 Hz International

9481-12

2158 8439	60 Hz U.S. Domestic
2158 8454	50 Hz International
2158 8447	60 Hz International

MEDIA (DISK CARTRIDGES)

The storage medium utilized is a disk cartridge (figures 1-4 and 1-5). The disk cartridge is composed of a single, 14 inch diameter aluminum disk which is permanently enclosed in a polycarbonate housing. The disk is a rigid, aluminum substrate coated with an iron oxide formulation designed for compatibility with the read/write heads.

To record information on the disk, the cartridge is placed into a receiver assembly (figures 1-6 and 1-7). This action opens the head access door and releases a spring-loaded spacer from the disk adapter, allowing the disk to rotate freely. Closing the receiver handle simultaneously positions the disk adapter on the drive spindle, figure 1-8, and forces the disk away from the adapter supports. This magnetically locks the adapter to the drive spindle.

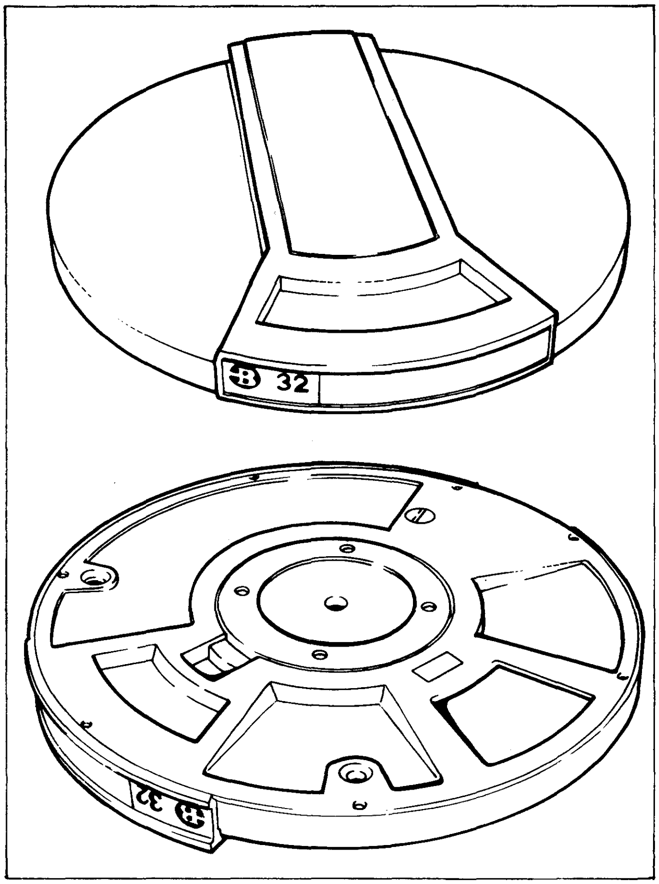


Figure 1-4. Disk Cartridge

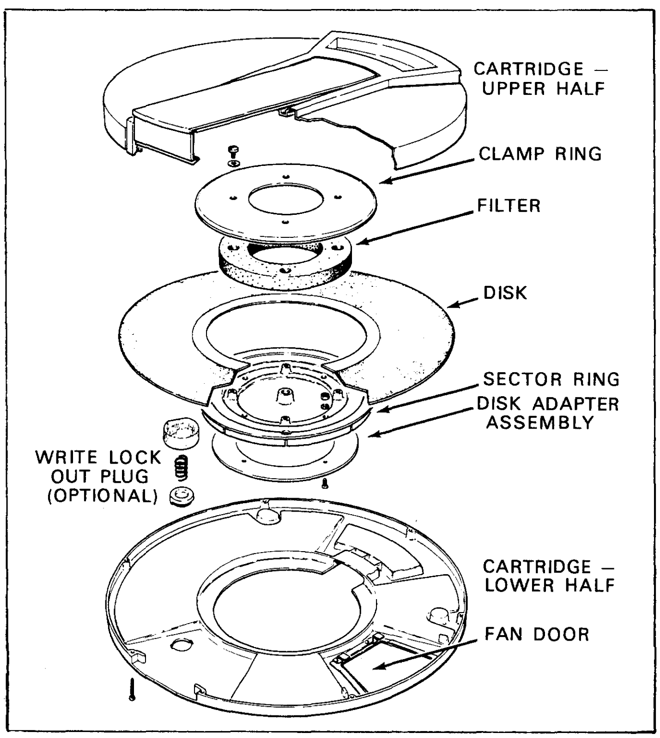


Figure 1-5. Disk Cartridge (Exploded View)

Data is recorded serial-by-bit on concentric tracks of the oxide-coated disk by two non-contact, flying heads which magnetize discrete areas of the disk. These heads float on a film of air, (approximately 100 micro-inches thick) generated by the spinning disk. The data recording surface of the disk is 2.04 inches wide, measured on the radius. The outer radius measures 6.520 inches, whereas the inner radius measures 4.480 inches.

DISK CONTAMINATION

Sites which perform large numbers of cartridge changes, and which have drives installed without clean air units, may over a period of time experience some contamination of the disk surfaces. This is due to an accumulation of particles of oxide, and dust and grease from the surroundings.

If steps are not taken to limit such contamination, it can rapidly spread from one cartridge to another, until the entire site library is affected.

An early indication of disk contamination is intermittent read errors, without any fault being found on the cartridge drives.

Due to the widely varying conditions under which different sites operate, precise guidelines cannot be laid down as to whether or not a particular site is likely to experience a disk contamination problem.

Field engineers should therefore carefully read the information which follows, and then use their own judgement and local knowledge to decide on a regular program of cleaning and inspecting disks.

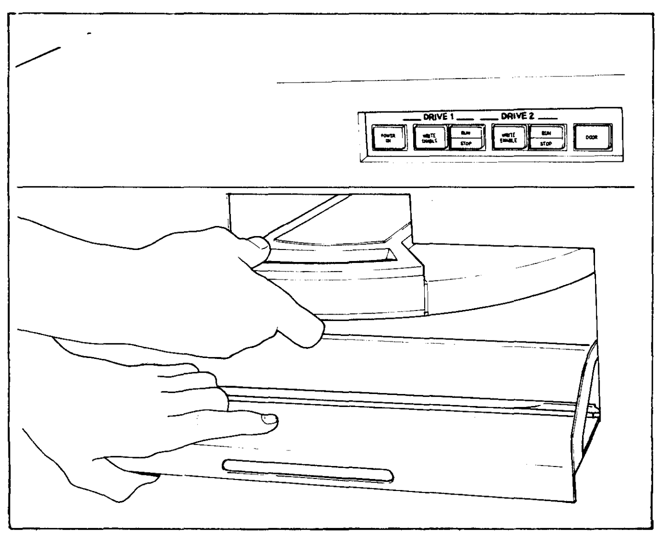


Figure 1-6. Inserting a Disk Cartridge into the Receiver (Upper Drive Module)

CAUTION
MEDIA SHOULD ALWAYS BE CONSIDERED AS AN INTEGRAL PART OF THE DRIVE. POOR QUALITY, DIRTY, OR MIS-HANDLED MEDIA CAN BE JUST AS DETRIMENTAL TO SITE PERFORMANCE AS A SERIOUS MALFUNCTION OF THE DRIVE.

CONDITIONS WHICH CONTRIBUTE TO CONTAMINATION

ENVIRONMENT

If contaminants, such as dust, smoke particles, etc., are present in the computer room, this can obviously spread to the cartridge drives. Drives which have clean air units are much less vulnerable to environmental contamination than those without.

CARTRIDGE CHANGES

Each time a cartridge is inserted into the drive, dust is stirred up from the surroundings and fine particles of oxide dislodged in the vicinity of the heads. As a rough guide, if a site performs more than about 20 cartridge changes per day, this should be considered as a strong contributory factor to disk contamination.

CARTRIDGE QUALITY

If scratches or blemishes are present on the disk surface, this can cause the flying heads to touch occasionally. The oxide so removed may accumulate in ring-like formations which can later be transported to other parts of the disk by head movement. It should be noted that scratches can themselves be caused by contamination, thus compounding the problem.

HEAD QUALITY

Heads that have been damaged, or are very dirty, will almost certainly cause oxide removal, probably resulting eventually in the destruction of the disk. ('Head crash'). If a site has a history of damaged heads, or head crashes, particular attention should be paid to eliminating the resultant contamination.

Any one or more of the above factors can contribute to disk contamination. If contamination is suspected, then with the customer's approval, obtain two or three cartridges from the library, and carefully dismantle them. Inspect the disk surfaces in an oblique light for:

Oxide scratches and indentations.
Dark, ring-like deposits of oxide.
Smears or other oil-like stains.

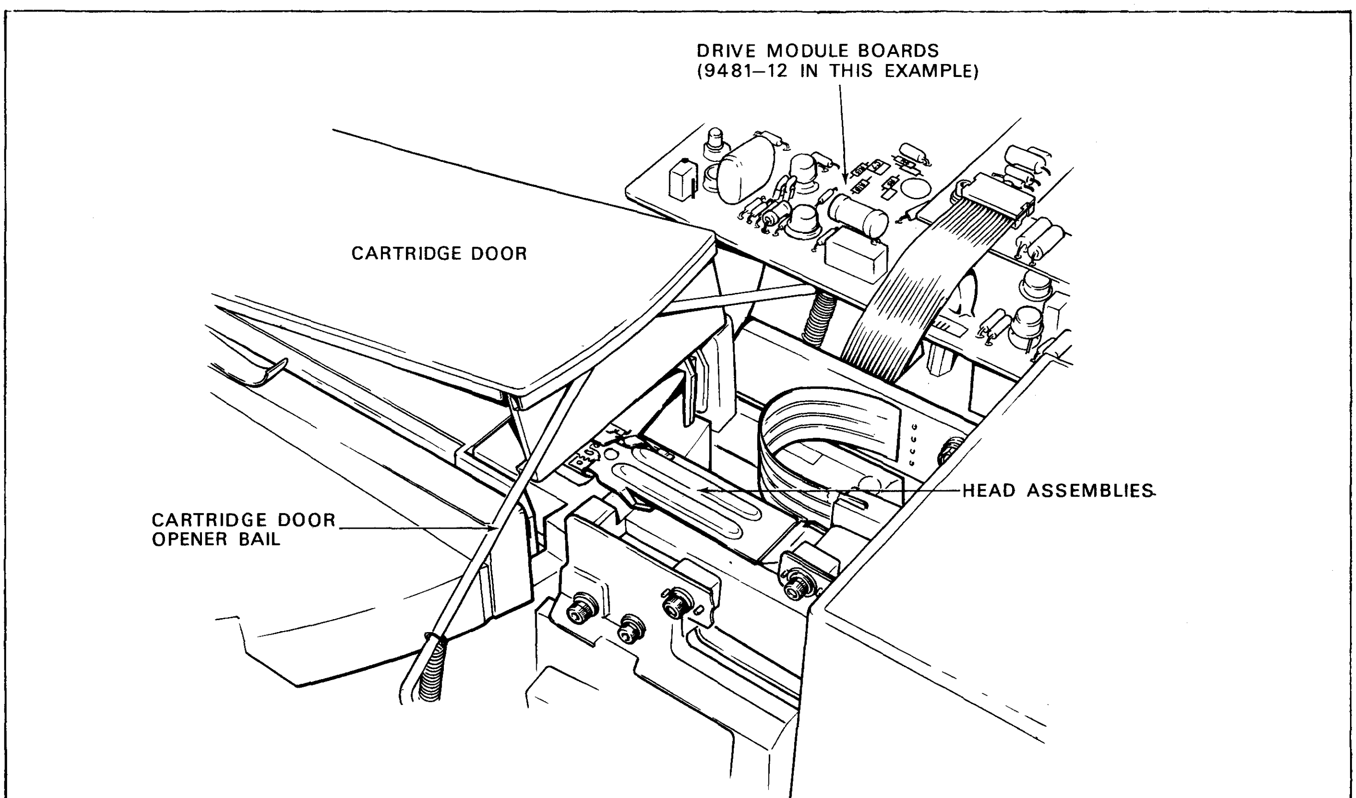


Figure 1-7. Disk Cartridge in Place in Drive Module

CARTRIDGE CLEANING

If contamination is evident, it is recommended that the entire site library be cleaned using the Burroughs BU 5000/BU 5500 Disk Cartridge Cleaner (see figure 1-8).

It is also recommended that any site with a library of more than about 30 cartridges should consider purchasing one of these machines, and use it to clean all cartridges on a regular basis. The actual frequency of cleaning will depend on the degree of usage, but as a rough guide, 6 months may be considered as an average figure.

PREVENTION OF CONTAMINATION

Prevention is always better than cure. The probability of contamination can be much reduced by observing the following guidelines:

1. If the computer room is dusty or contaminated, then fit a clean air unit (RIN R4392-028 rev.)
2. Never use cartridges from an unqualified source. Cartridges of Burroughs approved quality are available through your local Field Engineering Sales office, and are the only ones recommended for use on the 9480/81-12 disk cartridge drives.
3. Always take the utmost care in cleaning and handling of read/write heads, by observing the procedures in the 'Maintenance' section of this manual ('Handling and Cleaning of Read/Write Heads').
4. Encourage the customer to keep an 'Error log'. This would list the different drives on the site and the errors occurring on each of them, on a daily basis. The cartridges on which the errors occur should always be recorded as well. By this means, an early indication can be obtained of a contamination problem, and rectifying action taken quickly before it becomes serious. In particular, excessive read errors on individual cartridges should be quickly investigated.
5. On heavy-usage sites, consideration should be given to regular cleaning with the BU 5000/ BU 5500 Disk Cleaner. Details of this machine can be obtained from your local Field Engineering Sales Office.
6. Carefully read the information which follows, 'Handling and Storage of Disk Cartridges'.

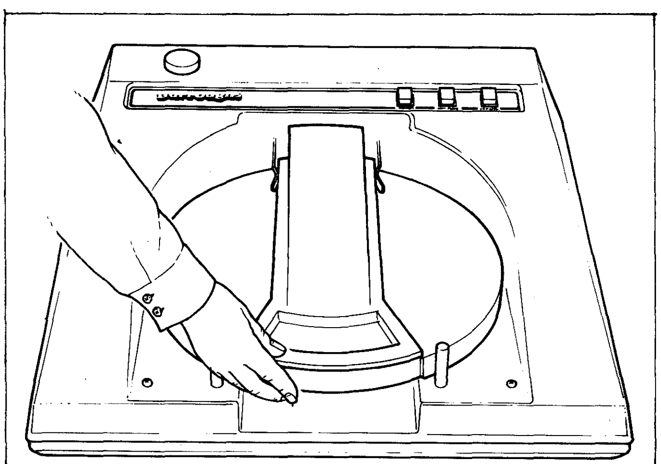


Figure 1-8. Burroughs BU 5000/BU 5500 Disk Cartridge Cleaner

STORAGE AND HANDLING OF DISK CARTRIDGES

HANDLING PROCEDURES

Disk cartridges are precision instruments. Tolerances are small as a few millionths of an inch are common in the usable product. It should, therefore, be realized by data processing personnel at all levels that:

They are dealing with a precision instrument.

Precaution in the handling and storage of the product can save literally thousands of dollars in system re-run time.

The value of the data recorded on a disk cartridge warrants the extra care required.

It is with this in mind that the following procedures are recommended to maintain the quality and lengthen the life of the disk cartridge:

1. Clean the protective covers periodically to remove any buildup of dust. Use a soft lint-free cloth or paper wipe.
2. Keep hands, pencils, or other objects off the disk surfaces. The disk surfaces can be distorted or damaged through impact or excessive pressure or abrasion. Should a disk be suspected of damage, have it inspected by a Burroughs Field Engineer before attempting to use it.
3. Coffee or other beverages spilled on the cartridge and/or covers may require that the cartridge be reconditioned. Keep beverages off the drive and away from the pack storage area.
4. Ashes and tobacco are a prime source of disk cartridge contamination. Tobacco and all smoking accessories should be kept away from areas where disk cartridges are in use or disk drives in operation.
5. Vacuum or wet-mop the machine room daily. Do not raise dust with such cleaning implements as brooms or feather dusters.

STORING THE DISK CARTRIDGE

SHORT-TERM STORAGE

Disk cartridges that are in frequent use are best stored in the computer room or similar environment. The ideal environments for storage are given in the following paragraphs.

Cabinets that are clean and free of dust and made of metal or other fire-resistant material provide the best storage medium. Such a cabinet should have metal doors to provide better protection.

Disk cartridges should never be stored in direct sunlight. Also they should never be exposed to intense magnetic fields, (high-current bus bars, cables, welding transformers, etc.). A field intensity of more than 50 gauss may cause loss of information. The Burroughs Field Engineer should be consulted if high-intensity fields are suspected.

Disk cartridges in shipping containers may be stacked on top of one another up to eight high, but should not be stacked on top of one another otherwise. They may be stored on edge in cabinets especially designed to support them in this position, but should not otherwise be stored on edge.

LONG-TERM STORAGE

For long-term storage the disk cartridges are best stored in the original shipping containers. When stored in this manner, they may be stored on top of each other.

The temperature for long-term storage must remain within the following limits: 40° F to 150° F (4° C to 66° C).

HIGH-SECURITY STORAGE

Vitally important data or duplicate master records should be stored in fire-resistant cabinets or in a separate storeroom that provides protection against catastrophic damage. The storage facilities provided should be insulated in such a manner that the internal temperature of the room or cabinet cannot rise above 150° in case of fire.

A sprinkler system is recommended as additional fire protection. If a sprinkler system is used, it should be of the pre-action type, which guards against the possibility of accidental head seal breakage.

DISK CARTRIDGE STORAGE AND SHIPPING SPECIFICATIONS

DISK WITH COVER

Weight	4 lbs. (1.871 kg.)
Diameter	15.0ins. (38.1 cm.)
Height	1.5ins. (3.8 cm.)

SHIPPING CONTAINER

Length	19.9ins (50.5 cm.)
Width	19.9ins (50.5 cm.)
Height	6.5ins (16.5 cm.)

TEMPERATURE RANGE

Shipping or Long Storage	40° F to 150° F (4° C to 66° C)
Operating or Short Storage	50° F to 105° F (10° C to 42° C)

RELATIVE HUMIDITY

8% to 80%.

RECEIVING AND SHIPPING THE DISK CARTRIDGE

Upon receiving the disk cartridge, examine each shipping carton for possible damage. If the container shows damage, the cartridge must be inspected prior to use. A typical example of gross transit damage is a crushed corner on the carton. Because the area of impact was small, the resulting shock forces may have been sufficient to bend the disk surfaces. Or, if the force did not render the surface unusable due to bending, it may have been sufficient to cause cartridge imbalance which will cause wobble or vibration when rotated on the disk drive.

Another example is holes in the shipping carton. This is again indicative of a large force coming into contact with a small area. Bent disks and/or cartridge imbalance may be the result.

The disk cartridge is shipped in a specially designed packaging assembly. This shipping container provides double protection for the disk cartridge to assure safe arrival to the customer.

The disk cartridge is secured in its two-piece cover. Although the cover is a positive dust proof seal, the disk could become contaminated with dust from the cover, when the cover is removed. Therefore, the cartridge is enclosed in a polyethylene bag. The disk cartridge is then placed in a corrugated folder. Polyurethane foam packing material is attached directly to the folder to protect the cartridge from freight handling or shipping damage. The disk cartridge thus packaged, is then placed in a corrugated carton and scaled for shipment to the customer.

But, even with the precaution of good packaging, transit damage can and does occur. To inspect a disk cartridge for mechanical stability, the following steps are recommended:

- Remove the disk cartridge from the shipping container and protective plastic bag.
- Remove the bottom cover.
- Turn the cartridge upside down in the top cover and examine the sector disk for gross scratches and dents.
- Place the cartridge on a disk drive and remove the top cover.

Look for any separation between the bottom disk and the sector disk.
Turn the drive on and immediately turn it off. This is time enough for the pack to attain a few revolutions. While the disk is spinning, observe it for any abnormal up and down motion.

Should the disk be vibrating or making excessive noise remove the cartridge from the drive, place the cartridge in its original shipping container, and make no further attempt to use it.

Do not under any circumstances attempt to use a cartridge which is suspect for physical damage.

These same procedures should be followed when it is suspected that a cartridge has been damaged in use. It cannot be stressed too strongly that any condition which creates doubt as to the mechanical performance of a disk should be reported immediately. If an operator were to drop a cartridge and then attempt to put that cartridge in use, it could result in gross damage to the disk drive, causing hours of down-time. It would cost must less to recreate the file on a functional cartridge.

When a disk cartridge is to be shipped from one location to another, it is advisable to re-use the original shipping container. The cartridge should be sealed in a plastic envelope prior to placing in the shipping carton. Improper packaging may cause severe damage to the cartridge during shipping. If the original packaging assembly is lost or damaged, replacements can be purchased through your Burroughs Field Engineer.

DISK CARTRIDGE HANDLING PRECAUTIONS

1. **A disk should never be handled without its cover.**
2. **Care must be exercised in installing the disk cartridge.**
   If the hub of the disk storage drive receives a sharp impact from the disk cartridge, the contour of the hub and/or the disk can be altered and cause misalignment of the disk surfaces to the read/write heads.
3. Foreign objects must never be placed where they can fall or be pushed against the disk surfaces.
4. **The operator should check the cartridge door to make sure that it is closed.** If it is open, slight manual pressure will prove sufficient to close the door and thus provide a dust seal.
5. The disk cartridge must always be placed on a table, flat surface, or disk cabinet designed for vertical storage that is free of other objects.

GENERAL OPERATING PROCEDURES

Before a disk cartridge is used, it should be conditioned to the computer-room temperature for at least **two hours** prior to use. The ideal environment for disk cartridges is the **same** as that recommended for the computer room, that is, a temperature of 60-90° F (15.6-32.2° C) and a relative humidity of 10-80%. The conditioning time is required to ensure correct track registration and data recording and retrieval.

Inspect the cartridge cover and remove any dirt or dust before installing the cartridge on the machine. On the drive, the disk cartridge is supplied with air that is taken from the room and filtered at the intake of the drive unit. The glass door of the disk drive should always be kept closed while the drive is in operation, to keep dust from by-passing the filters.

DISK CARTRIDGE INSTALLATION AND REMOVAL

Inserting the Disk Cartridge into the Drive

To install the cartridge,
1. Open the glass door by pressing the illuminated 'DOOR' switch.
2. Pull down the interlock handle on the drive. This clears the opening into which the cartridge is to be inserted.
3. Pick up the cartridge at the handle-like front edge, in such a manner that the cartridge is facing up and pointing away from your hand. The letters embossed on the handle should be to the left of your hand and right-side up.
4. Ensure that the cartridge door is free to move. Do not attempt to insert the cartridge unless it is.
5. Slide in the cartridge like a desk drawer.
6. Close the interlock handle, press the 'RUN/STOP' switch.
7. Press shut the glass door.

Removing the Disk Cartridge from the Drive
1. Press the 'RUN/STOP' button.
2. After about 30 seconds, 'STOP' will be illuminated. Do not attempt to remove cartridge before this time.
3. Press the 'DOOR' switch to open the glass door.
4. Pull down the interlock handle.
5. Take hold of the cartridge handle and pull out the cartridge.
6. Close the cartridge door to seal out dust and immobilise the disk inside.
7. Press shut the glass door.

Note:
1. The 'POWER ON' switch should not be used in lieu of the 'RUN/STOP' switch in the cartridge removal procedure.
2. Do not attempt to operate the interlock handle when no A.C. power is present. The interlock circuitry requires the pressure of mains power.

MECHANICAL COMPONENTS

GENERAL

The Magnetic Disk uses a removable cartridge for data storage. Data storage/retrieval is accomplished by positioning the flying heads over the surfaces of the disk within the cartridge. The major mechanical parts are described in this section.

BASEPLATE CASTING

The baseplate is a rib-reinforced aluminum casting. The functional surfaces are machined to critical tolerances. The servo positioner motor, carriage rail, position transducer, detent assembly, spindle, spindle drive motor, cartridge index locking pins, electronic modules, interlocks, cartridge receiver and cartridge air supply systems are mounted on the baseplate.

SERVO POSITIONER MOTOR

The servo positioner motor is a permanent magnet with a movable bobbin (armature). A precision cast aluminum carriage and head/arm assemblies are attached to the armature.

CARRIAGE AND GUIDE RAIL

The function of the carriage is to position the upper and lower head assemblies over the disk surface. The carriage assembly is a unitized casting that rides on two sets of opposed ball bearings and one ball bearing opposed by two floating ball bearings. The ball bearings ride the guide rail which is mounted onto the baseplate.

POSITION TRANSDUCER

The position transducer is mounted on the guide rail.

HEAD/ARM ASSEMBLY

The head/arm assembly is mounted onto the carriage. The flying head pad is attached to the access arm by a gimbal. Leaf springs are an integral part of the head assembly. These springs provide constant loading force on the flying heads so that the proper flying height is maintained. Gimbal mounting of head core assembly provides two degrees of movement (pitch and roll) in the horizontal axis. A ramp transmits the loading force onto the shoe. As the disk rotates, the gimbal action allows the head shoe to attain the proper aero-dynamic attitude when flying over the disk surface. Two bleed holes symmetrically spaced about the head core axis stabilize the head. These bleed-holes permit the heads to fly at the proper height.

HEAD LOADING

Head loading is achieved through the preformed, precision leaf springs. At the home position of the carriage the leaf springs are maintained in the unloaded position by a self-lubricating ramp. Forward motion of the carriage allows the leaf spring to be activated by sliding off the ramp. The ramp geometry controls the unloaded head to disk spacing, while ramp position controls the area on the disk at which the heads load and unload.

CARTRIDGE INSERTION

Cartridge insertion is accomplished in the receiver, figures 1-6 and 1-7, which functions as a carrier to locate the disk onto the spindle. Lowering the front cover and pulling the receiver handle down allows the user to insert the cartridge. Moving the handle upward settles the cartridge onto the index-lock pins. The disk is located on the spindle by action of the magnetic chuck assembly. The proper seating of the cartridge activates an interlock which allows the spindle motor to be energized. The spindle drive motor is manually turned on from a control on the front of the drive. The receiver handle is mechanically interlocked until the drive spindle is at a complete stop. The cartridge receiver handle cannot be pulled down until 30 seconds after the spindle drive motor has been turned off, or if A.C. power is turned off.

SPINDLE DRIVE ASSEMBLY

The spindle drive assembly, accurately positions and holds the disk in place as the disk is rotated. The spindle is driven by a belt attached to the spindle drive motor pulley and the spindle pulley. No braking of either the drive motor or spindle is used. The disk is held in position by the disk adapter and the spindle chuck. The spindle chuck consists of a magnetic ring and pole piece. When the disk cartridge is mounted on the spindle chuck, a magnetic path is completed to retain the disk securely on the spindle. The 1/12 horsepower induction-type motor attains operating speed within a few seconds after turn-on.

AIR VENTING (EARLY UNITS)

Positive air pressure is maintained in the disk cartridge by a fan that forces filtered air into the cartridge. The fan bonnet opens the air vent trap door in the bottom of the cartridge. When the cartridge is in its operating position, a replaceable nylon mesh screen filters the air prior to its entry into the disk cartridge. The nylon screen is removable, and should be changed as required by environmental operating conditions.

AIR VENTING (LATER UNITS)

Positive air pressure is maintained in the disk cartridge by a fan which drives air through a 0.3 micro filter, and thence through ducting to each drive module. The filters are removable and should be replaced when the air flow reduces to an unacceptable level.

OPERATOR CONTROLS AND INDICATORS

POWER ON

Depression of this switch applies the A.C. line voltage to the power supplies. D.C. power is thus available to the drive electronics and indicators, and A.C. power is available to the drive motor relay. Depression of the switch a second time removes the A.C. line voltage.

WRITE ENABLE

This is an indicator only. If the write lockout plug on the cartridge is not depressed and locked, WRITE INHIBIT is false and the lamp is lit.

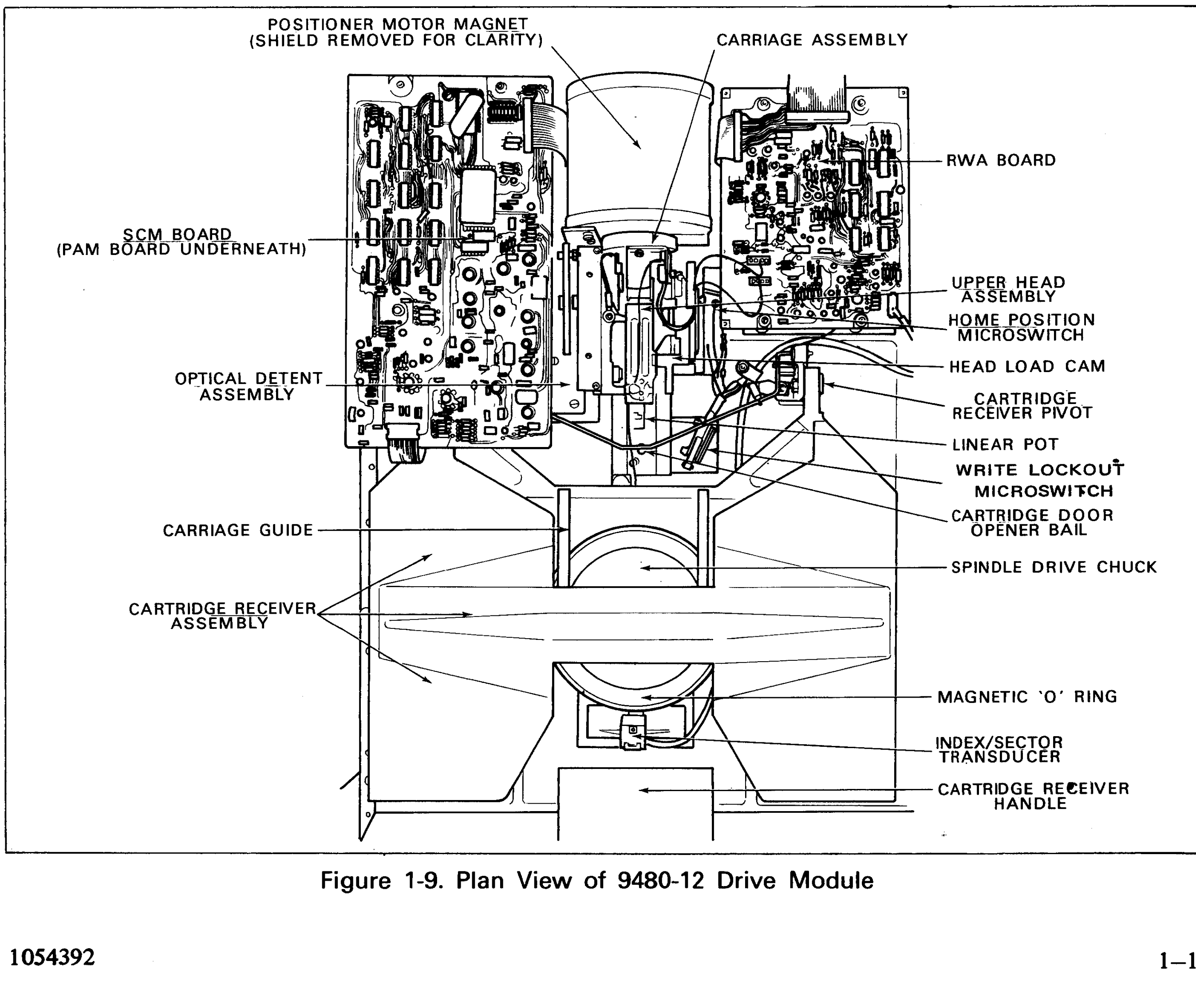


Figure 1-9. Plan View of 9480-12 Drive Module

RUN/STOP

The receiver handle may only be operated if the red 'STOP' light is on. If, after inserting a cartridge, this button is depressed, the following occurs:

1. The disk will be run up to speed.
2. The receiver handle will be locked.
3. The 'RUN' indicator will be lit.
4. The appropriate blue 'DRIVE' indicator will be lit on the modesty panel.
5. After 4 seconds, the positioning system will load the heads on to track 00.

The drive is now ready for use.

If the switch is now depressed a second time, the followng sequence occurs:

1. A.C. power is removed from the disk motor, which therefore slows down.
2. After a few seconds, the positioning system will retract the heads onto the head load ramp.
3. Both 'RUN' and 'STOP' lamps will be extinguished.
4. The appropriate blue 'DRIVE' lamp on the modesty panel will be extinguished.
5. After 30 seconds, the receiver handle is unlocked and the 'STOP' lamp illuminated.

The cartridge can now be removed from the drive.

NOTE

When no A.C. power is present to the power supply, the receiver is kept locked as a precaution in case of a mains power failure.

DOOR

The door is normally kept closed by a magnetic latch. Depression of this switch operates a solenoid which overcomes the magnetic latch and pushes the door open.

RECORDING PRINCIPLES

A read/write head is essentially an electromagnet that can concentrate a high magnetising force over a very small area of the disk coating. When writing, the

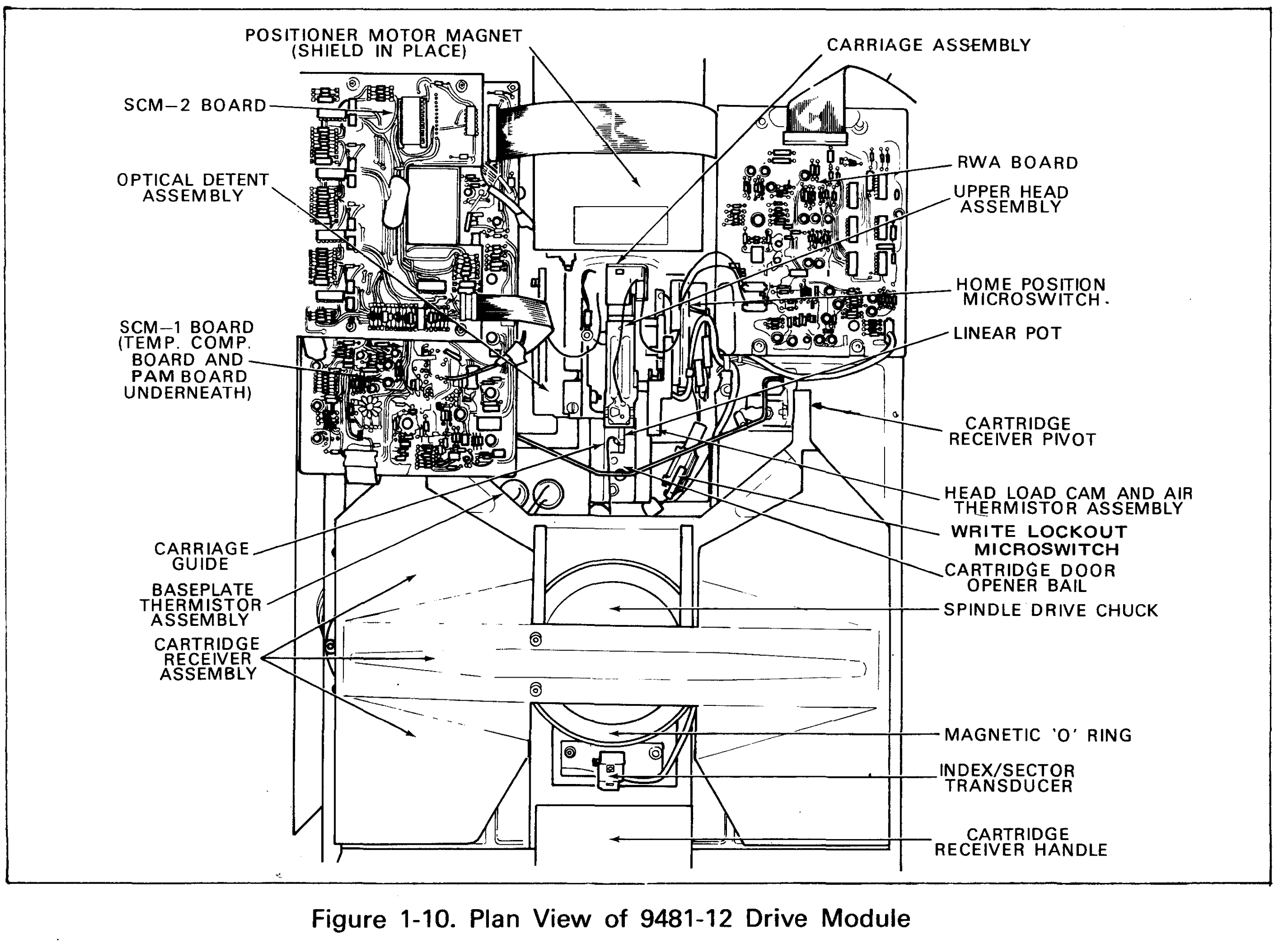


Figure 1-10. Plan View of 9481-12 Drive Module

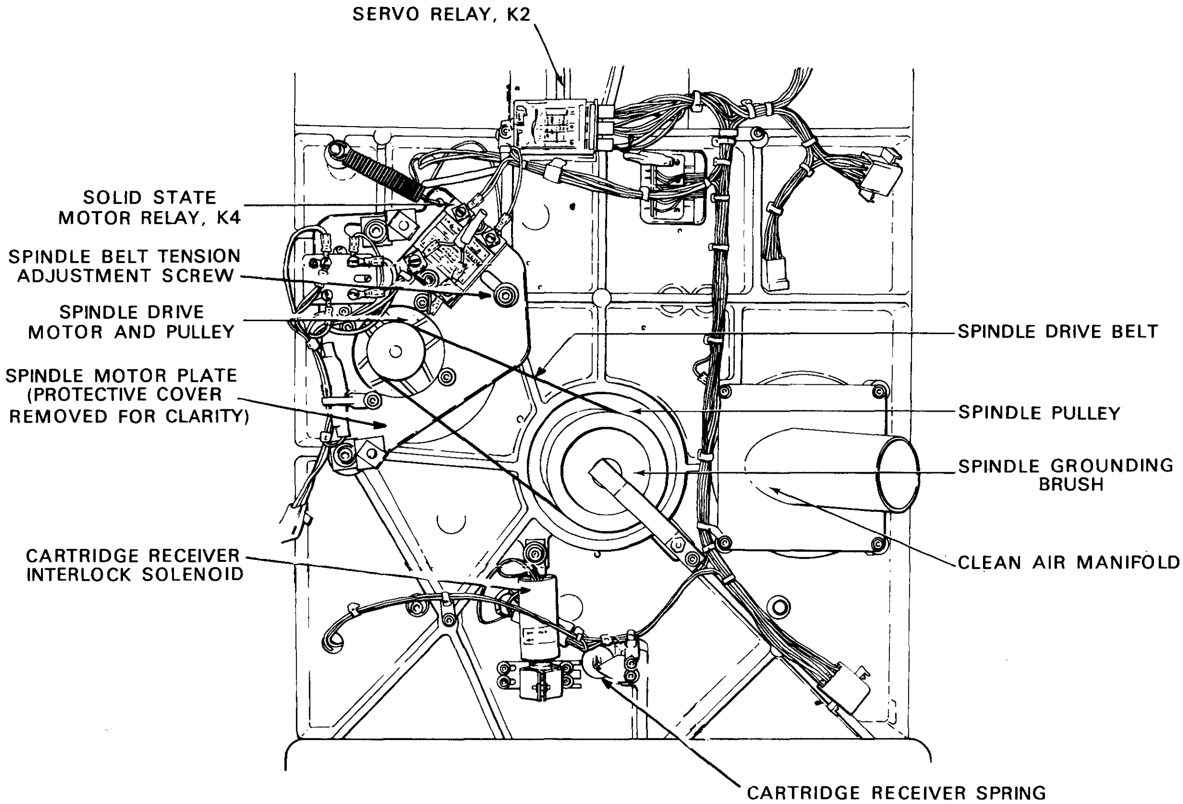


Figure 1-11. Bottom View of Drive Module

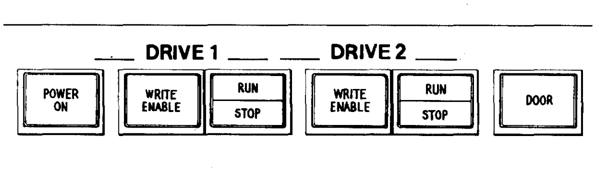


Figure 1-12. Operator Controls and Indicators

field strength is alternated to magnetise the disk with the desired bit pattern. Each read/write head also contains a 'straddle-erase' electromagnet, the function of which is to erase the edges of the data track just written. The width of each track is narrowed to the following approximate dimensions by this erase method, to minimise noise pick-up between adjacent tracks.

Model	Track Width	Track-to-Track Spacing
9480-12	0.007	0.010
9481-12	0.0036	0.005

When reading data, the read/write head operates as a sensor. A flux reversal in the disk coating induces a voltage across the electromagnet coils, which can be amplified and conditioned to recover the original data.

RECORDING FORMAT

In order to obtain optimum packing density and eliminate the need for an extra clock track a form of phase encoding is employed, known as double frequency recording (DFM).

By reference to figure 1-14 it can be seen that this consists of providing 2 flux reversals per 'bit-cell time' for a '1' bit, and 1 flux reversal per 'bit-cell time' for a '0' bit.

TRACK FORMAT

Each track is divided into 32 sectors (see below for sector format), defined by 32 evenly-spaced slots (SECTOR) cut into the disk hub, plus 1 extra slot (INDEX) used as a tacho-generator and for synchronisation.

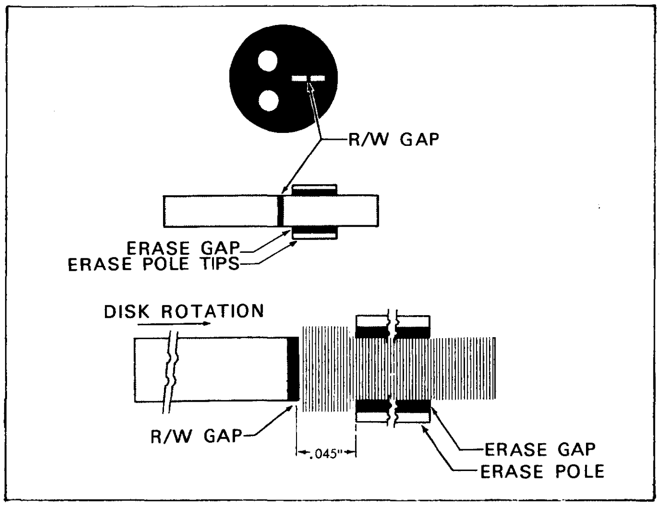


Figure 1-13. Head Recording Principles

All the hub slots are sensed by an optical transducer, and amplified and shaped by the drive electronics. The SECTOR pulse is then passed to the controller to provide indication of the sector boundary, whilst the INDEX pulse is used to monitor the speed of the disk. Should the disk slow down for any reason, the increased time lapse between INDEX pulses will be sensed and the heads retracted automatically.

SECTOR FORMAT

A sector of a track does not just contain the information sent to it by the host system, but has the following format: (Ref. figure 1-15).

A 32 byte preamble of all zeroes to enable read clock synchronisation.
2 synchronous bytes to enable controller synchronisation.
2 bytes containing the track and head address for error checking, and the unique address of the sector.
180 bytes of user data.
1 byte contained a parity error check character.
A postamble of 25 bytes, which allows for slight variations in switching and other timing.

INITIALISATION AND VERIFICATION

In order for the disk to be satisfactory for use by the customer's software, it must first have pre-recorded in each sector the unique address of that sector. In addition, due to the nature of the oxide coating of the disk, blemishes and pin-holes can occasionally be present, and these must be located and rendered unusable by the system software.

This process of initialisation and verification is the function of a system software utility and consists of the following:

—The track and head address and the unique sector address is written in each sector for the entire disk, and a suitable data pattern (preferably a 'worst-case' pattern) in the data field.
—Each address and the data field is then read back and checked for accuracy.
—If any sector fails to be read back correctly, this is assumed to be due to some local abnormality of the disk. The failing sector is then either relocated to a spare track (reserved on the disk for just that purpose), or recorded in a 'look-up' table as an unusable sector.

It is emphasised that the above process is purely a software function, and may vary in detail according to the host system used.

However, if an initialisation and verification run reports a large number of bad sectors, this does not necessarily mean the disk is at fault. The drive should be carefully checked out for faults before discarding a disk due to excessive bad sectors. In particular, any problem in the read-back circuits can cause this indication, and the routine should be run on a known, good, disk to ascertain the cause of the failures.

Another cause of excessive bad sectors is contamination of the disk surfaces.

OPERATION

For logical purposes, the drive operation may be divided into four areas, as under:

The Input/Output Interface
The Positioning System
The Read/Write System.
Miscellaneous Functions

INPUT/OUTPUT INTERFACE

The drive unit itself can only control the basic functions of power supply and certain types of error detection, since it has no in-built controller.

The process of head positioning, reading and writing, must be initiated either by on-line control from the host system, or by a suitable off-line simulating device such as the Model 900 Exerciser.

The input/output interface is the section of logic which passes control signals to the drive, and drive status information to the controller. It must also synchronise the controller to the drive, to enable properly timed data to be transferred during read or write operations.

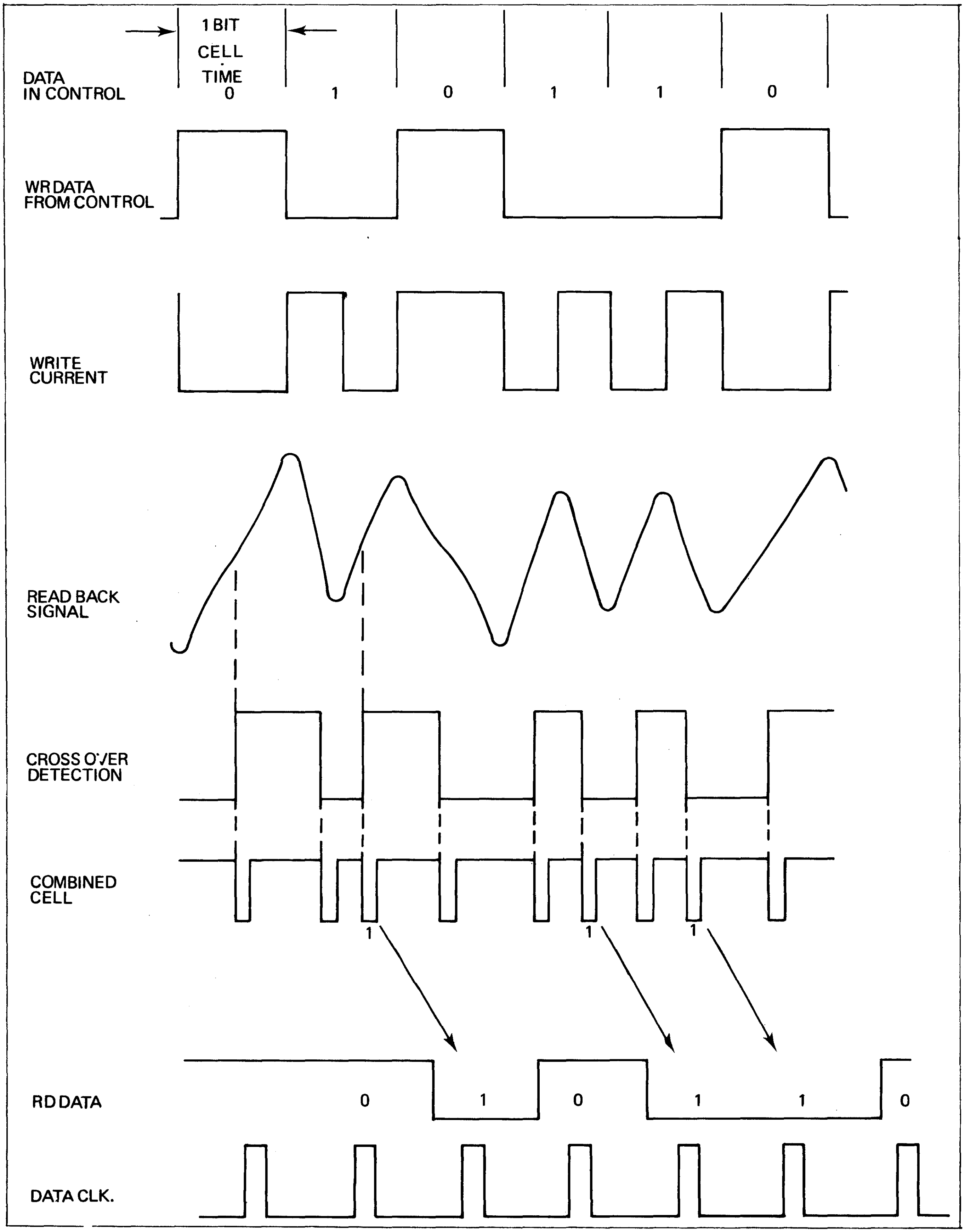


Figure 1-14. Double Frequency Recording

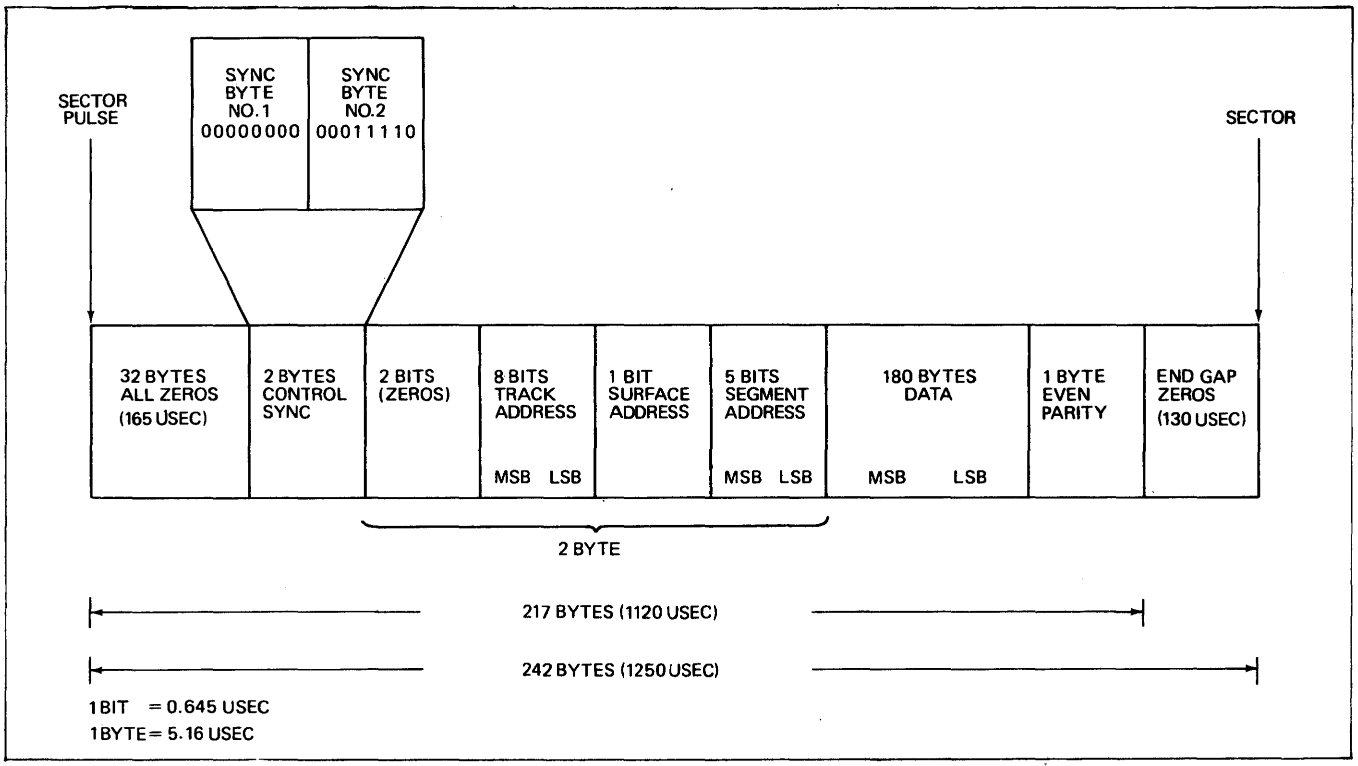


Figure 1-15. Burroughs DCD 2200 BPI 180 Byte Format

Figure 1-16 shows the signals which are transferred by the input/output interface. These are detailed as under.

CYLINDER ADDRESS

This consists of 8 lines (9480-12) or 9 lines (9481-12) and transmits in binary form the address of the cylinder to be accessed. These lines are strobed into the Cylinder Address Register by the SEEK pulse. The address is then decoded and the heads move automatically under the control of the Positioning System. (See figure 1-17).

UNIT SELECT

Unit Select consists of one line. When in the true state the functions applicable to access, control, and data transmission of one drive are selected. When in the false state the functions applicable to access, control and data transmission of the other drive are selected.

SEEK

This line provides a pulse that strobes the address information into the Cylinder Address Register in the drive unit. This pulse also causes the positioning system to initiate a seek operation.

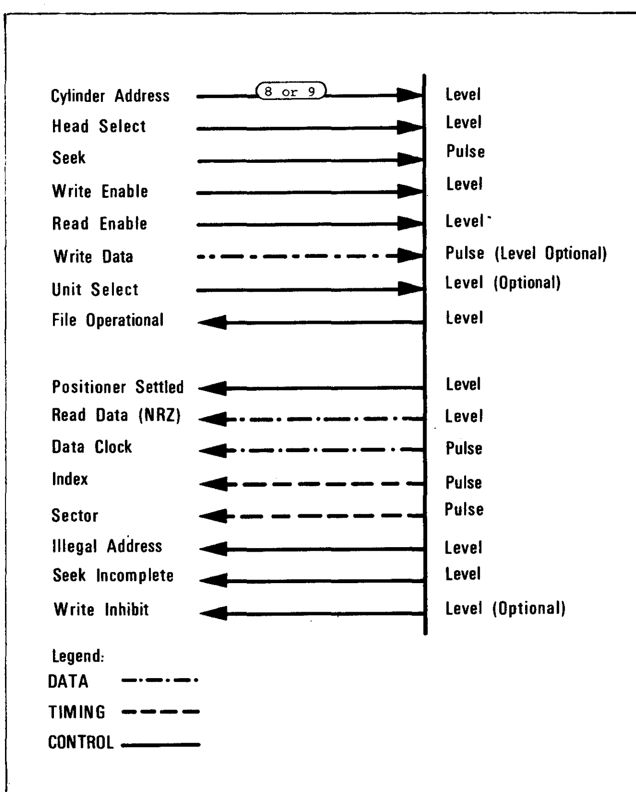


Figure 1-16. I/O Interface

	Decimal Cylinder	Binary Address
9480-12 1	000	00 000 000
	001	00 000 001
	002	00 000 010
	•	•
	•	•
	•	•
	200	11 001 000
	201	11 001 001
	202	11 001 010
9481-12 1	000	000 000 000
	001	000 000 001
	002	000 000 010
	•	•
	•	•
	•	•
	403	110 010 011
	404	110 010 100
	405	110 010 101

Figure 1-17. Binary Notation of Cylinder Address

HEAD SELECT

This line selects the top disk surface when in the false state and the bottom disk surface when in the true state.

WRITE DATA

The Write Data line carries the serial-by-bit NRZ write data from the controller.

WRITE ENABLE

This line turns on the write amplifiers and edge erase. The line must go false after the write operation has been completed.

READ ENABLE

This line enables the read discriminator circuits. When the line is in the true state, the discriminator output will be placed on the Read Data and Clock lines.

FILE OPERATIONAL

This line indicates to the user that the Disk Drive is ready for operation. When the Drive has achieved operational speed, all interlocks and safety circuits are satisfied, and the line goes to a true level.

POSITION SETTLED

This line supplies a level to the user indicating that the heads are positioned and stabilized. The Drive is then ready to accept read or write commands.

READ DATA

The Read Data line transmits serial-by-bit NRZ read data to the controller. The level of this line is maintained for the entire bit period.

DATA CLOCK

This line transmits the 1.55 MHz write or read clock for the data. The clock output is used by the controller to strobe the data.

INDEX

The Index line supplies a pulse for the index reference point on the disk. The index pulse is normally utilized to synchronize the controller's sector counter.

SECTOR

This line supplies a pulse at the beginning of each sector.

ILLEGAL ADDRESS

This line supplies a level when the cylinder address is greater than 202 (9480-12) or 405 (9481-12) during a SEEK command. A valid address and a new SEEK pulse will reset the ILLEGAL ADDRESS line.

POSITION ERROR

This line supplies a true level if POSITION SETTLED has not occurred 200 milliseconds after a SEEK command, thus indicating that the address has not been accessed by the positioning system. This line will be reset by the next SEEK pulse.

POSITIONING SYSTEM (Refer to figures 1-18, 1-19 and 1-20)

The operation of any moving-head disk drive depends upon an accurate, high-speed method of locating the flying heads over the correct track on the disk.

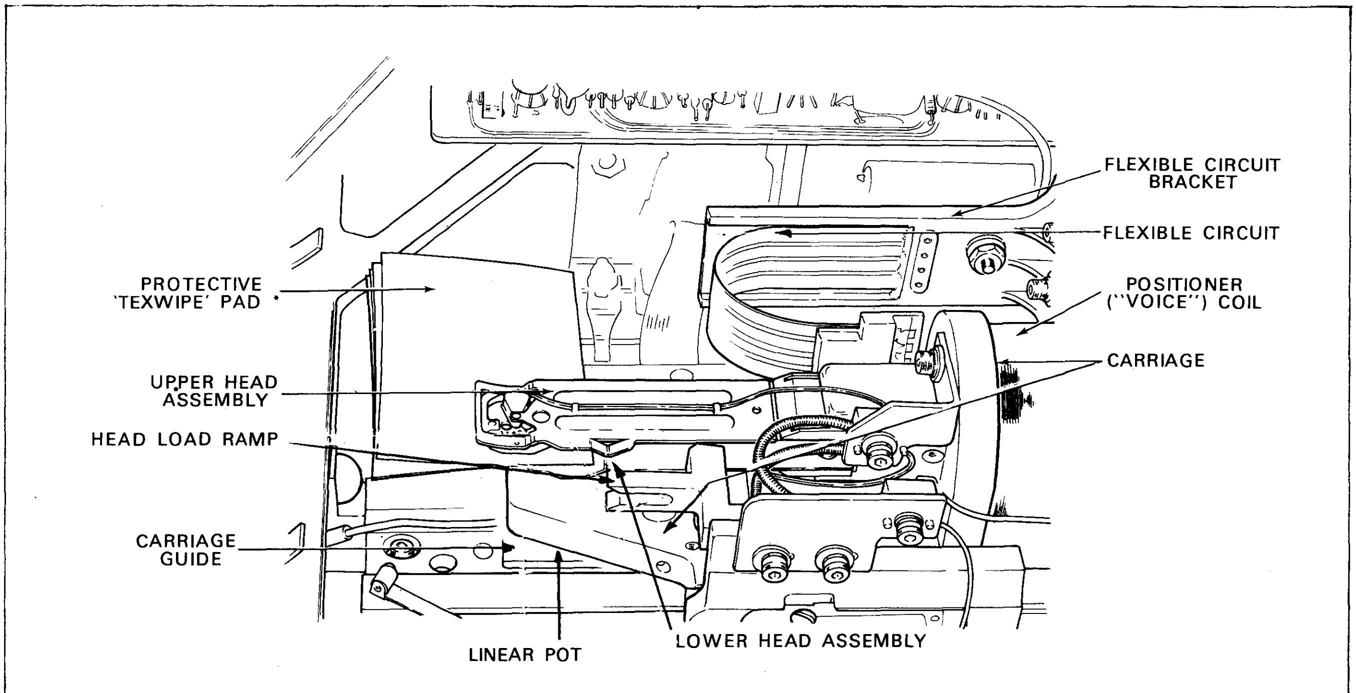


Figure 1-18. Positioner Mechanism (with protective pad in place between heads)

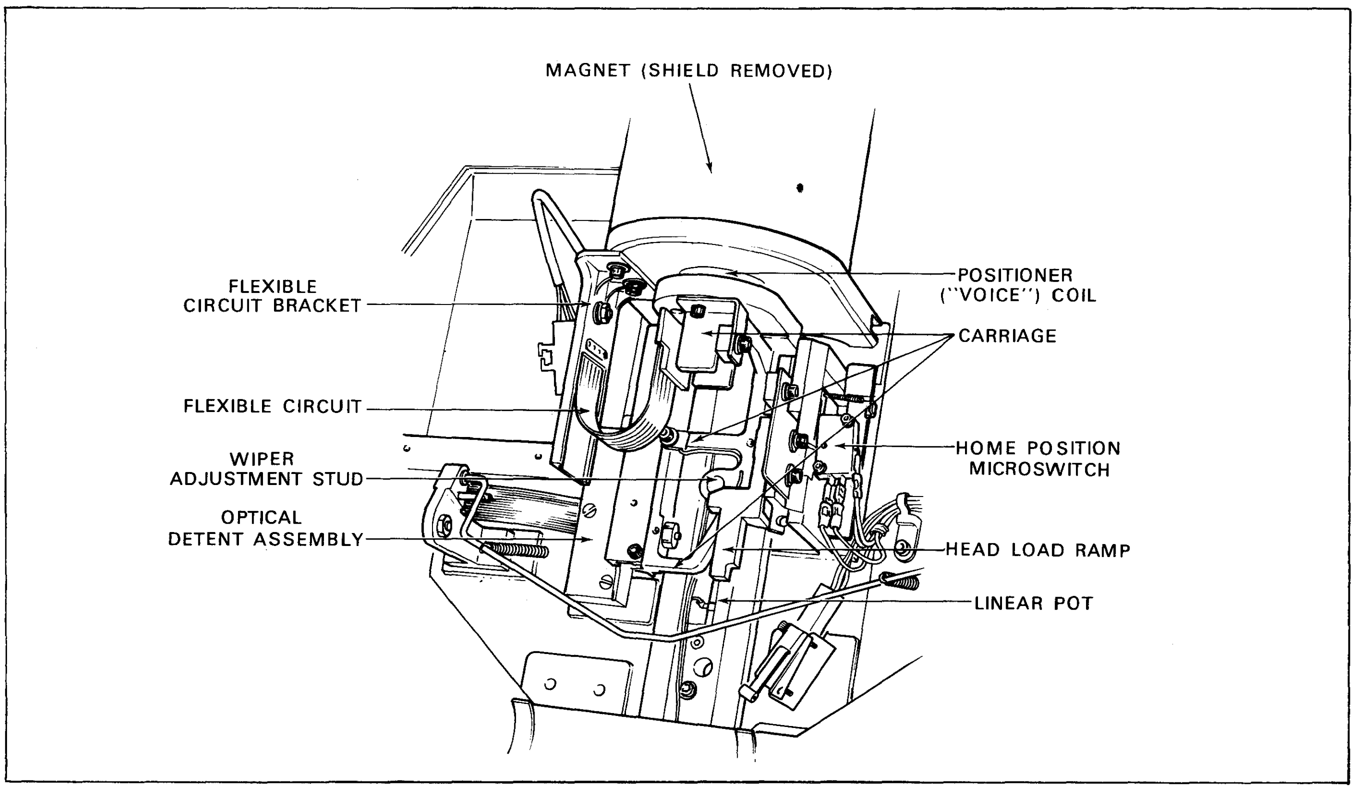


Figure 1-19. Positioning System Components (Heads and Boards Removed for Clarity)

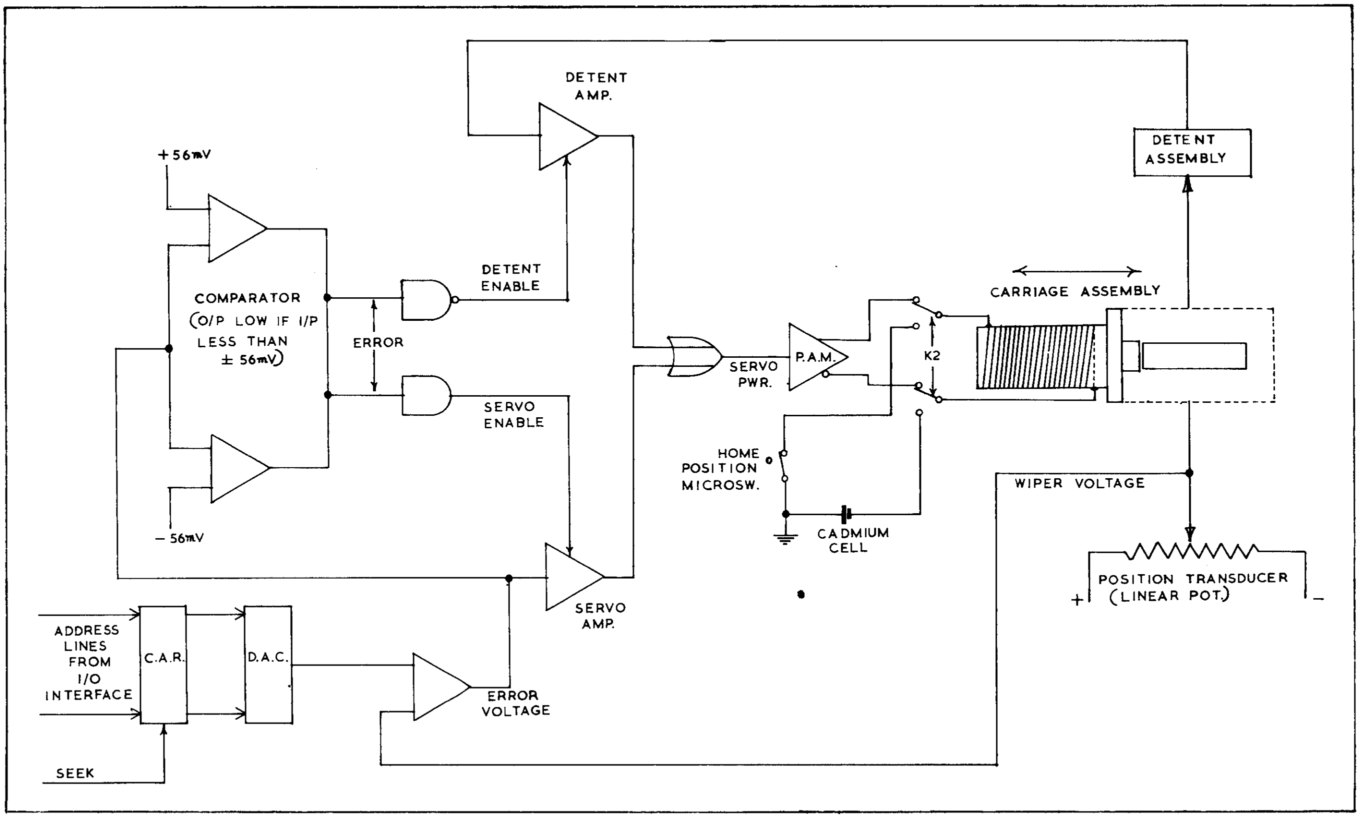


Figure 1-20. Positioning System – Coarse and Fine Servo Loops – Simplified Functional Block Diagram

In the case of the 9480/81, this is achieved by using a 'voice coil' attached to a moving carriage traversing a guide. The heads are fixed to the carriage.

The voice coil is free to move within a large, powerful permanent magnet fixed to the baseplate. In order to move the carriage assembly, a magnetic field is induced in the coil, which interacts with the field from the permanent magnet, thus causing a force which will tend to move the carriage forwards or backwards, depending on the strength and polarity of the current in the coil.

COARSE AND FINE SERVO LOOPS

The position of the carriage is sensed by a wiper traversing a resistive strip which has a voltage gradient from one end to the other. The voltage present at the wiper thus varies according to the position of the carriage. (Linear pot or 'Markite' strip).

Upon receipt of a cylinder address from the I/O interface, the positioning system will convert this from a binary number to a D.C. voltage by means of a digital-to-analog converter (DAC). The voltage from the DAC is compared to the voltage from the linear pot, and if a difference exists, an error voltage is developed. This error voltage is amplified and passed to the voice coil, thus causing the carriage to move until the wiper voltage is approximately equal to the DAC voltage.

The process just described constitutes the coarse servo system, and is not accurate enough to maintain the heads within fine tolerance on the desired track.

The fine servo system is brought into operation when the error voltage reduces below a nominal value (56mV), thus indicating that the heads are in close proximity to the desired track. It consists of an electronically operated optical system incorporating a detent assembly and a carriage mounted mask assembly.

The operation of the fine servo varies in detail for the two styles of drive, due to the differing track densities.

9480-12 FINE SERVO

The detent assembly contains four photo-electric cells, two lamps, a fixed mask, a terminal board, and a combination detent cover and mounting bracket. Four critically spaced groups of grid lines are etched on the mask in positions immediately overlying the four photo-electric cells. This arrangement allows the groups to be divided into two sets that provide selection of either an odd or even track address. When the servo control system attempts to position the read/write heads to an addressed track location, the grid lines on the two masks tend to superimpose. When the heads arrive at the exact addressed track location, the masks align so that the signal outputs from the two responding photo-electric cells are equal and opposite, resulting in a null signal to the servo system. However, if the heads do not arrive at the location, the resulting mask misalignment permits increased output from one photo-electric cell which is provided to the servo control system as an error correction signal. The servo control system will then attempt to reposition the read/write heads until a null condition is indicated.

9481-12 FINE SERVO

The detent assembly contains four pairs of photo-electric cells, one lamp, a fixed mask, a terminal board, and a combination detent cover and mounting bracket. Eight critically spaced groups of grid lines are etched on the mask in positions immediately overlying the four photo-electric cell pairs. This arrangement allows the groups to be divided into four sets that provide selection of either an odd or even track address. When the servo control system attempts to position the Read/Write heads to an addressed track location, the grid lines on the two masks tend to superimpose. When the heads arrive at the exact addressed track location, the masks align so that the signal outputs from the two responding photo-electric cells are equal and opposite, resulting in a null signal to the servo system. However, if the heads do not arrive at the location, the resulting mask misalignment permits increased output from one photo-electric cell which is provided to the servo control system as an error correction signal. The servo control system will then attempt to reposition the Read/Write heads until a null condition is indicated.

When the carriage is correctly positioned by the fine servo, that is, there is no correction voltage being input to the servo amplifier, then the system is said to be in detent. After a short, fixed, delay (to allow the damping of any small carriage vibrations), the signal POSITION SETTLED will be developed for transmission to the controller, and the drive is now ready to accept read or write commands.

SEEK ERROR CONDITIONS (Refer to figure 1-21)

The positioning system can provide ndications of two types of error arising during a SEEK command from the controller. These are:

1. POSITION ERROR. Failure of the carriage to detent 200ms after receipt of a SEEK pulse.
2. ILLEGAL ADDRESS. Receipt of a cylinder address greater than 202 (9480-12) or 405 (9481-12), during the execution of a SEEK pulse.

In each case:
POSITION SETTLED is inhibited.
ILLEGAL ADDRESS or POSITION ERROR is sent to the controller instead to flag the error.

EMERGENCY HEAD RETRACTION

The positioning system will unconditionally retract the heads from the disk surfaces in the event of certain failures in the drive. These are:

1. No current flowing in detent assembly lamps. If any detent lamp is extinguished the servo cannot function correctly whilst in detent.
2. Failure of +20V or −20V. These are the supply voltages for the operational amplifiers in the drive, failure of which could cause serious malfunction of the servo.
3. Failure of +5V. This is the logic supply voltage.
4. Failure to achieve POSITION SETTLED 4 seconds after the receipt of a SEEK command. This indicates a malfunction of the positioning system.
5. Primary A.C. failure. This in turn, will cause either of the conditions in 1 through 4 above.

HEAD LOADING AND RETRACTION

When the drive is not in use, the heads are positioned away from the disk area on the head load ramp. At this point there is no voltage being input to the servo coil.

If a cartridge is inserted and the drive powered up, then after a delay of 4 seconds, a relay (K2) will provide a path from the servo to the coil and the heads will move forward off the head load ramp until positioned over track 00.

When the drive is powered off, operation of the RUN/STOP switch will first return the heads to track 00. When the disk has slowed down sufficiently, relay K2 switches in a battery which provides a reverse voltage to the coil, drawing the heads off the disk and onto the head load ramp. Once on the ramp, the head load cam will depress the home position microswitch, thus disabling the battery.

It should be noted that all head retractions are brought about by switching in the battery, providing a safety factor in the event of servo failure, or a mains voltage failure, etc.

READ/WRITE SYSTEM (Refer to figure 1-22)

When the positioning system has located the heads over the correct track, the host system will then commence reading the pre-recorded addresses in order to locate the one sector at which the read or write operation is to commence.

In response to the SECTOR pulses, each address is read and passed to the host system where it is compared with the desired address until coincidence occurs. It is only then that the actual reading or writing of the user's data can commence.

From this it can be seen that both read and write operations must always be preceded by a read operation in order to locate the desired sector.

In addition, most operating systems incorporate a check for validity of the track and head address, in case of a positioning error. Should the track or head address read from the disk not compare with the address transmitted to the positioning system, a 'seek error' is usually flagged by the host system.

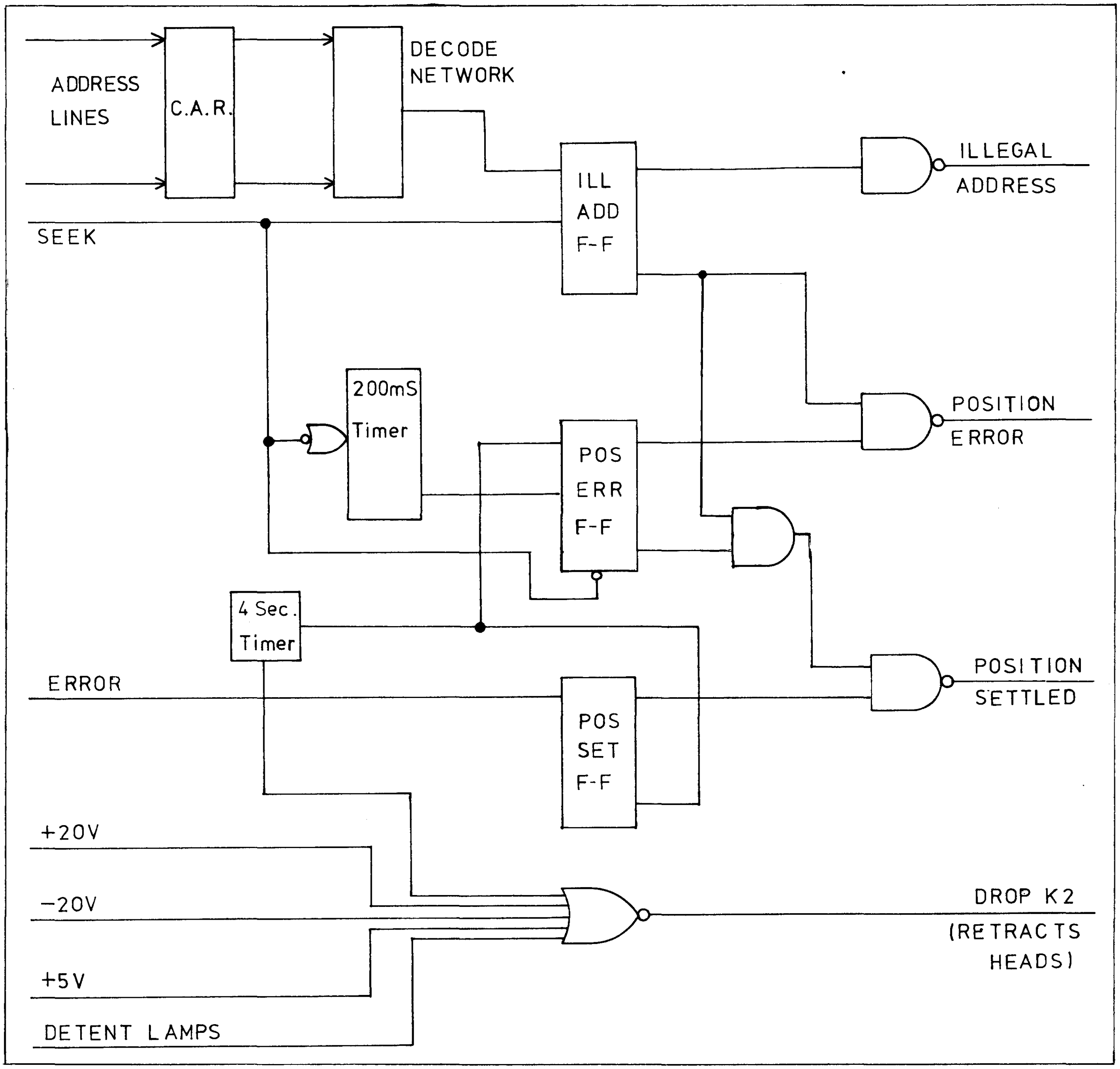


Figure 1-21. Positioning System – Control and Error Detection Logic Block Diagram

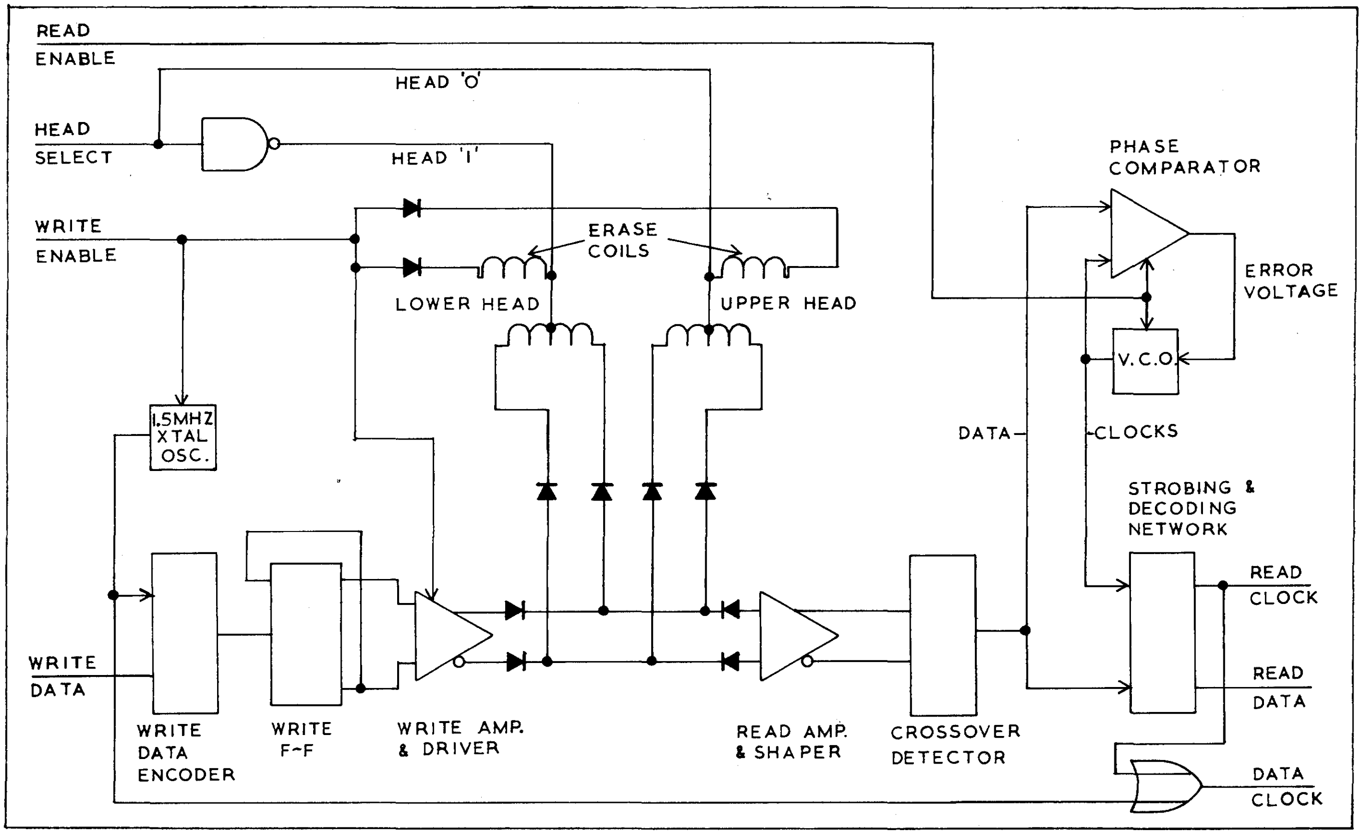


Figure 1-22. Read-Write System – Simplified Functional Block Diagram

It should always be borne in mind, therefore, that any malfunction in the read circuits can also result in seek or address errors during a write operation as well.

(For format of track and sector address see section on Sector Format).

NOTE

The Model 900 Exerciser only reads or writes one address at the beginning of each track, and must therefore never be considered as a full operational check of a drive or cartridge.

Operation of the read/write system is controlled by the signals READ ENABLE, WRITE ENABLE and HEAD SELECT. The reader is referred to the block diagram in figure 1-22.

For a read/write head to be active:

- The read/write coil center-tap must be enabled for the relevant head. Head selection is controlled by HEAD SELECT, which if low will activate head 0 center tap and if high will activate head 1 center tap.
- The read/write coil circuit path must be completed by enabling either the write amplifier or the read amplifier, depending on the state of WRITE ENABLE or READ ENABLE respectively.
- In addition, during a write operation, WRITE ENABLE will turn on the current to the straddle erase coil on the head selected.

When the circuit path has been completed by enabling a head center-tap plus the read or write amplifier, as appropriate, either:

- Current is driven through the head to magnetise the disk in the desired bit pattern,

— or —

- Changes in magnetic flux on the disk will induce a fluctuating voltage in the head, which can be processed by the read circuits.

The diodes in the head circuits are for isolation purposes, and prevent crosstalk and interference between the two heads.

READ OPERATIONS

All mechanical rotating memories, such as the disk cartridge drive, are prone to minor variations in data recording frequency over small local areas of the disk. These are brought about by:

- Variations in rotational speed due to mains voltage

fluctuations, or slight differences in pulley dimensions.
- Vibration of the disk, caused for example, by imperfect bearings.
- Peak shifting due to variations in the magnetic properties of the oxide coating.
- Positioning system tolerances which can cause slight head mis-alignment.
- Temperature fluctuations which can bring about changes in mechanical dimensions. (The 9481-12 has a Temperature Compensation Network to minimise this effect).

The high data recording frequency, in conjunction with the above variations, necessitates a read system which can efficiently adapt itself to local changes of frequency from one sector of information to another.

The purpose of the 32 bytes of preamble at the beginning of each sector is to provide a local reference frequency for that sector. By this means, the read clock can be subjected to fine frequency adjustments to enable accurate strobing of the addresses and data.

Before a read operation can commence:
- The drive must be powered up and rotating above minimum speed. (1200 r.p.m.).
- The positioning system must be in detent and the heads located over the correct track.
- The signal READ ENABLE must be active from the controller.
- The signal UNIT SELECT must be active for the drive which is to perform the read operation.

When the above conditions are met, analog data pulses coming from the read/write head are first amplified and shaped, then passed through a crossover detector which provides a standard width pulse corresponding to each peak of magnetic flux on the disk.

The crossover pulses then enter the data discriminator, which consists of:
- A voltage controlled oscillator (VCO) from which the read clocks are derived (RD CLK).
- A phase comparator which compares the frequency of the VCO with the incoming data pulses.
- A network which develops the correct relationship between clocks and data and converts double frequency code back to NRZ information. (RD DATA).

Operation of the data discriminator is intimately dependent on the controller timing. 65-95 µS after the receipt of a SECTOR pulse, the controller must raise READ ENABLE, this timing being such that the data discriminator will commence operating in the 32 byte preamble of '0's. The phase comparator compares the incoming data frequency with the clock (VCO) frequency, and if a difference exists, an error voltage is developed and passed to the VCO, which then increases or decreases frequency to compensate. The phase comparator and VCO thus form a phase locked loop which is used to synchronise the read clock (VCO) to the local frequency of the incoming data.

The crossover pulses are also passed to a strobing and decoding network. This uses the VCO output to establish the proper relationship between clocks and data and then decodes the data from double frequency code to NRZ for transmission to the controller. The data, however, will not be accepted by the host system until a period of time has elapsed to allow the phase locked loop to 'lock on' to the preamble frequency. By the time the 2 synchronous bytes are reached, it is assumed that the PLL has stabilized and the controller now accepts the following 2 bytes as the track, head and sector address.

The track and head address are checked for a seek error, and the sector address compared for that required to start the read operation. If address coincidence has not occurred, the controller will ignore all further data and remain inactive until the receipt of another SECTOR pulse, when the process repeats itself. If, however, the correct address has been found, the controller will synchronize itself to accept the data field from the sector as the 180 bytes of data required. When the 180 bytes have been counted the controller ignores all further data and remains inactive until the next SECTOR pulse.

Synchronisation of data read from the disk is maintained by the READ CLOCK, which is transmitted to the controller over the DATA CLOCK line.

WRITE OPERATION

As has been seen, before a write operation can commence, the host system must first read the address field to locate the required sector.

A write operation is therefore the same as for a read operation, except that once the correct address has been located the signal WRITE ENABLE will be activated.

In addition, before writing can commence, the write lockout plug on the cartridge must be fully extended to de-activate the write lockout microswitch.

When the above conditions have been met, 1.55 MHz clock pulses from a crystal oscillator on the CEM board are sent to the controller over the DATA CLOCK line to synchronise the incoming data. WRITE ENABLE turns on the write amplifier and driver. The NRZ information sent by the controller over the WRITE DATA line is encoded into double frequency code on the CEM board, and can now be written onto the disk in the desired bit pattern.

At the same time, WRITE ENABLE also turns on the current to the erase coil, which will clip the data just recorded to the correct track width.

When the 180 bytes of information have been written into the sector, the controller must turn off WRITE ENABLE to prevent the addresses and preamble from being overwritten in the next sector.

MISCELLANEOUS FUNCTIONS

These are:
INDEX and SECTOR
Receiver Interlock
Temperature Compensation (9481-12 only)
D.C. Power Supplies.

INDEX AND SECTOR

The purpose of SECTOR pulses is to supply the controller with timing pulses corresponding to the boundary of each sector of information.

The purpose of the INDEX pulse is:
– To inform the controller that the next sector pulse is the first sector on that track.
– To provide the drive electronics with an indication of the rotational speed of the disk.

There are 32 sector slots and 1 index slot cut into the hub of the disk. When the disk is rotating at 1500 r.p.m., SECTOR pulses will be 1250 uS apart, and INDEX pulses 40mS apart. The INDEX slot is cut between the 32nd and 1st SECTOR slots. The rim of the hub into which the slots are cut is seated into a recess of the sector transducer, when the cartridge is fully inserted into the drive. On one side of the recess is a light source and on the other a photo-electric cell and as the disk rotates, light can therefore fall on the photo-cell only when a slot is in the recess. The impulses so induced in the sector transducer are amplified and shaped by the drive electronics, which discriminates between INDEX and SECTOR pulses. It also measures the time period between INDEX pulses, and should this increase to about 50mS (indicating that the disk has slowed down), relay K2 will be dropped causing the battery to retract the heads. In addition, the reverse sequence occurs as the disk runs up to speed; that is, as the period between INDEX pulses decreases to less than 50mS, K2 will be picked and the positioning system will load the heads onto the disk.

RECEIVER INTERLOCK

This is a safety device to prevent accidental insertion or removal of the cartridge whilst the spindle is rotating, since this could result in damage to the disk and heads.

The receiver interlock solenoid is of 'fail safe' design – it must be picked to release the receiver handle. It will be unpicked (locked), under the following conditions:
– No A.C. power available to the drive. If A.C. power is removed for any reason, an attempt could be made to remove the cartridge before the spindle stopped rotating.
– Normal operating conditions, when the drive is powered up and the disk rotating.
30 seconds after the RUN/STOP switch is used to power down the drive, to provide sufficient time for the spindle to come to rest.
– If motor relay K4 develops a short, thus failing to turn off the motor when the RUN/STOP switch is depressed.

TEMPERATURE COMPENSATION NETWORK (9481-12 only)(Refer to figure 1-23)

The track density used on the 9481-12 style drive is double that of the 9480-12, and positioning of the heads is therefore more critical. Changes in temperature can cause the mechanical components of the positioning system and disk to expand or contract causing an unacceptable mis-alignment of the heads.

The purpose of the Temperature Compensation Network is to measure these changes in temperature and to inject a compensating voltage to the positioning system to restore the heads to accurate alignment.

The temp comp module generates a voltage which is a function of three thermistor resistors and an input voltage from the D/A converter.

Of the three thermistors, two are located in a bracket on the baseplate of the drive, out of the way of air flows and the third is located inside the head load cam, which directly measures temperatures of air inside the cartridge. The D/A converter represents the cylinder address.

The voltage generated by temp comp is used by the servo positioning motor while it is in the detent mode and serves to offset the heads by moving them in a specified direction and distance to compensate for the difference in temperature.

D.C. POWER SUPPLIES

The disk cartridge drive uses the following D.C. voltages:

Voltage	Purpose
+36V –36V	Linear Motor Power
+20V –20V	Operational amplifier, transistors and D.A.C.
+ 5V	Logic Supply Voltage (clips)
+12V	Relays and Solenoids

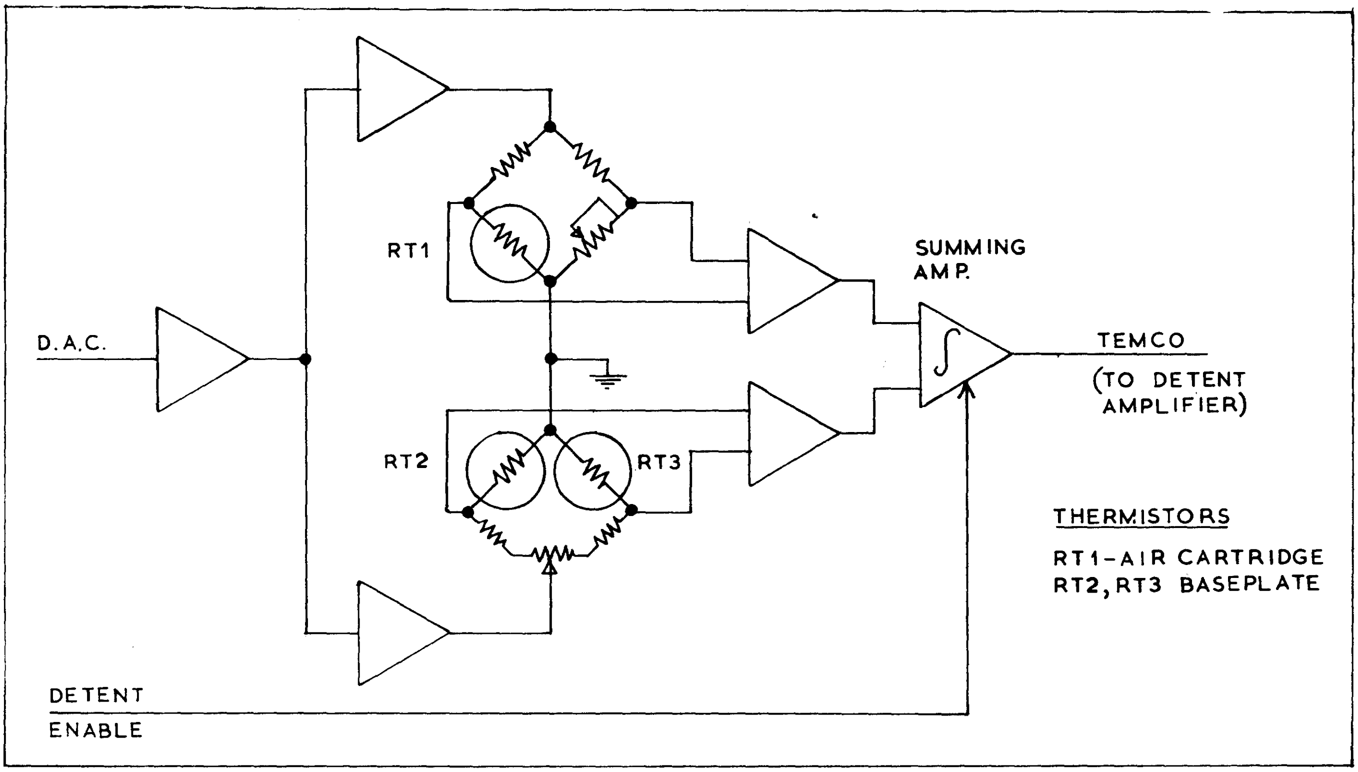


Figure 1-23. Temperature Compensation Network – Block Diagram

All the D.C. voltages are obtained by rectifying the outputs of step-down transformer T1. The input A.C. line voltage to T1 is 120V, and international units must therefore be fitted with a further transformer to step the local line voltage down to 120V.

The +36V,–36V and +12V supplies are unregulated, but the +5V, +20V and –20V supplies use integrated circuit regulators and series pass transistors.

The +5V supply is monitored by an over-voltage 'crowbar' thyristor, SCR-1. This provides protection to the integrated circuits in the event of failure of the +5V regulator.

PRINTED CIRCUIT BOARDS (Refer to figures 1-24 and 1-25).

The following boards are common to both styles of drive:

Common Electronics Module (CEM)
Read/Write Amplifier (RWA)
Power Amplifier Module (PAM)
Power Supply Module (PSM)

The remaining boards are as follows:

9480-12

Servo Control Module (SCM)

9481-12

Servo Control Module 1 (SCM-1)
Servo Control Module 2 (SCM-2)
Temperature Compensation (Temp. Comp)

BOARD FUNCTIONS

COMMON ELECTRONICS MODULE

The CEM board performs the functions which are common to both drives, and there is therefore only one board per drive cabinet.

By means of the signal UNIT SELECT, the CEM board must ensure that commands and information are routed and processed for the correct drive.

The following areas of operation are located on this board:

I/O Interface
Drive Selection
Read Pulse Shaping Circuits
Data Discriminator and Read Clock Generator
Write Clock Generator (1.55 MHz crystal oscillator)
Write Data Encoder.

READ/WRITE AMPLIFIER

There is one RWA board for each drive module, containing the following areas of operation:

Read Data Amplifier
Write Data Amplifier
Write Driver
Erase Current Driver
Head Selection
SECTOR and INDEX.

POWER AMPLIFIER MODULE

There is one PAM board for each drive module. It has mounted on it the power transistors and associated elements, needed to amplify the output from the servo to drive the positioner coil.

POWER SUPPLY MODULE

There is one PS board per drive cabinet. It performs the functions of monitoring and regulating the power supply voltages.

SERVO CONTROL MODULES (9480-12 and 9481-12)

Both the SCM and SCM-1 boards contain the electronics for the coarse and fine servo loops. The track address and control signals form the inputs, the output being the servo control voltage (SVO PWR) and servo status signals. There is one SCM or SCM-1 board for each drive module.

SERVO CONTROL MODULE 2 (9481-12 only)

The SCM-2 board is used solely on the 200 t.p.i. model, to accommodate the extra detent amplication circuitry. There is one board for each drive module.

TEMPERATURE COMPENSATION (9481-12 only)

Contains the temperature compensation network for the 200 t.p.i. model. There is one Temp. Comp board per drive module.

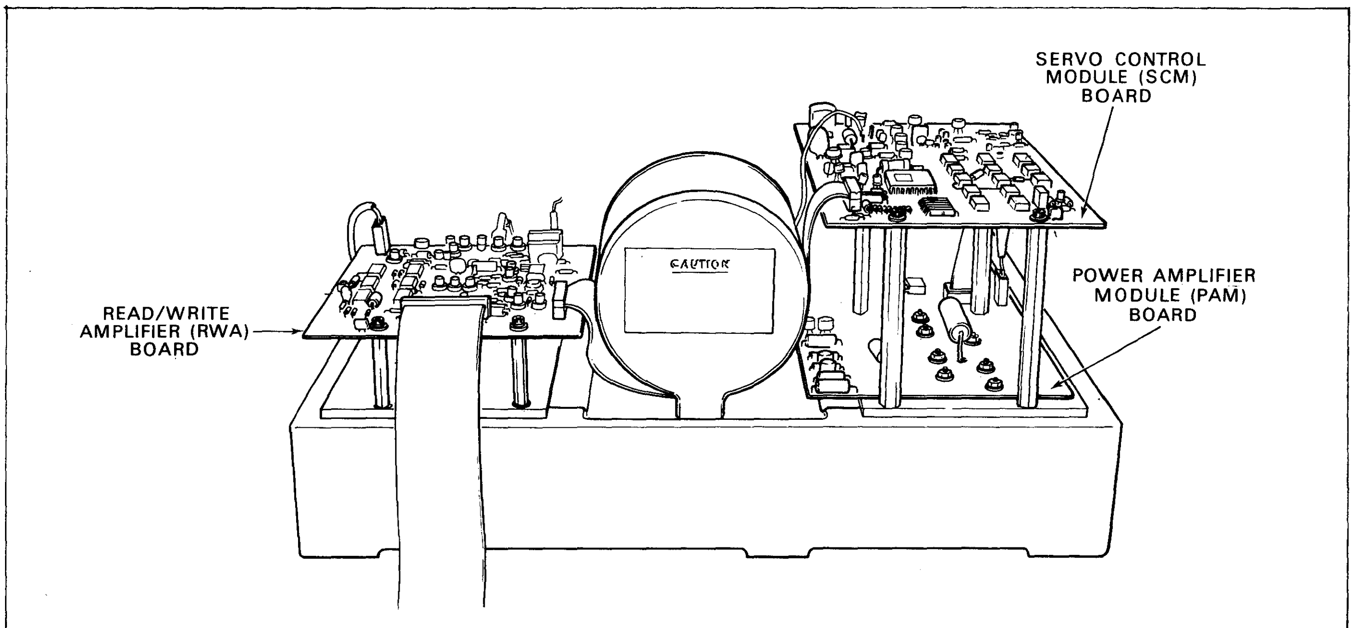


Figure 1-24. Rear View of Module Showing Boards (9480-12)

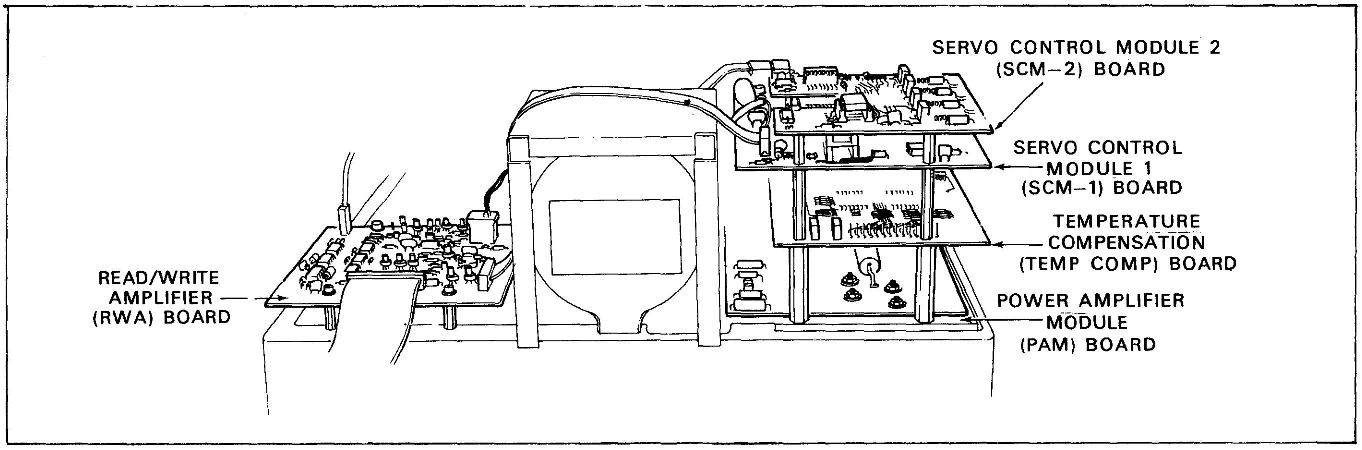


Figure 1-25. Rear View of Module Showing Boards (9481-12)

SECTION 2
FUNCTIONAL DETAIL

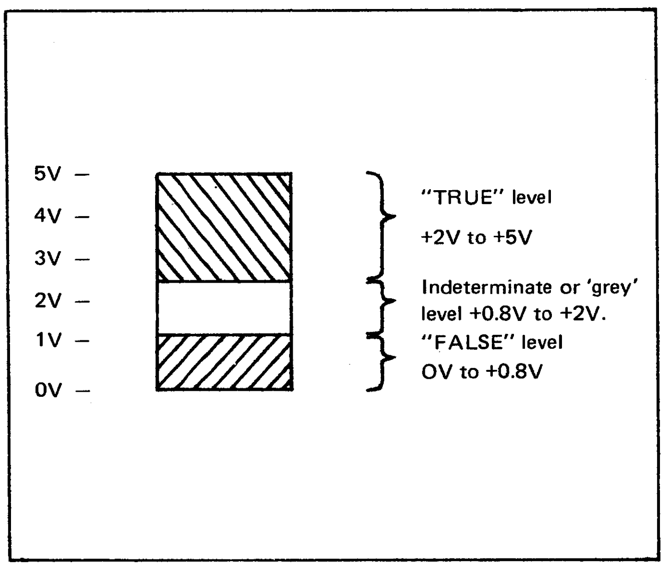
LOGIC ELEMENTS

This section describes the types of integrated circuits (chips) used in the 9480/81-12 disk cartridge drives.

LOGIC TYPES

The type of logic mainly used is TTL (transistor-transistor logic), with one or two exceptions, which are described individually.

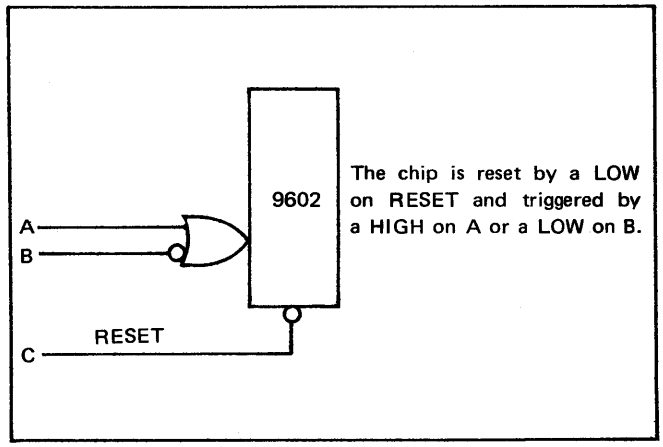
The true and false levels are as follows:

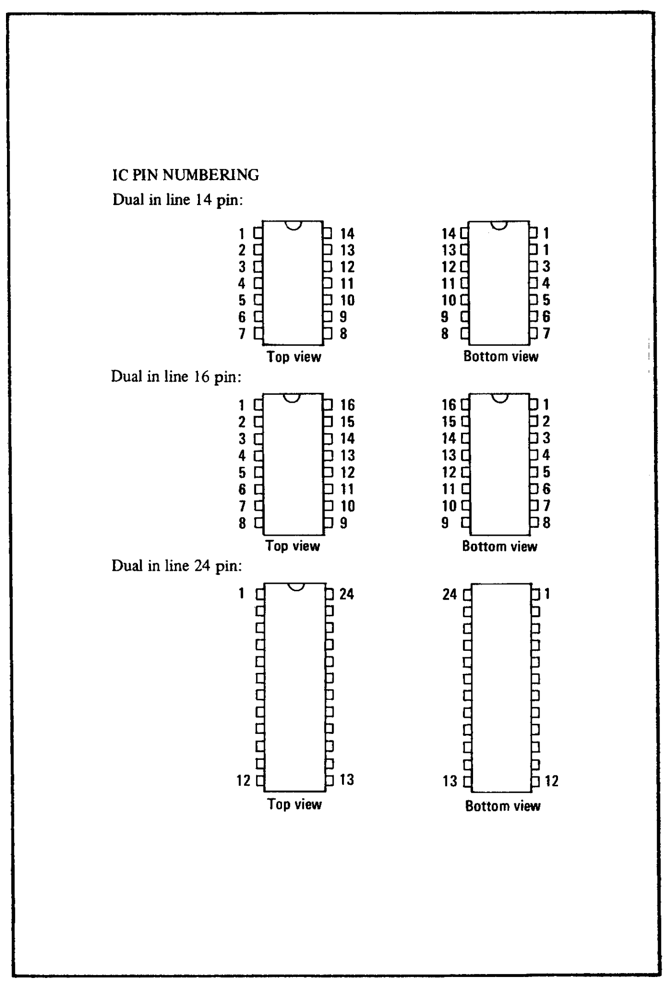


In general, a TRUE is considered as "HIGH" and FALSE is considered "LOW", but there are some exceptions on interface lines and inter-board signals. A PLUS (+) or MINUS (–) sign next to a signal name indicates the active state of the signal, for example:

SEEK (–) Indicates that when the signal SEEK is LOW, a seek operation will be initiated.

In addition, on printed circuit board logic diagrams, a negation symbol (o) is used to indicate that a function is active when low, for example:



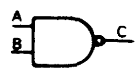


INDEX OF LOGIC ELEMENTS

MANUFACTURER'S IDENTIFICATION(S) : SN7400

TITLE : QUAD 2 INPUT NAND GATE

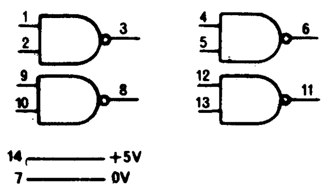
LOGIC SYMBOL :



TRUTH TABLE :

A	B	C
HI	HI	LO
HI	LO	HI
LO	HI	HI
LO	LO	HI

PIN DESIGNATION :



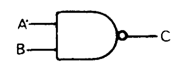
PACKAGE :

14 pin Dual in line.

MANUFACTURER'S IDENTIFICATION(S) : SN7403

TITLE : QUAD 2 INPUT NAND GATE WITH OPEN COLLECTOR OUTPUT.

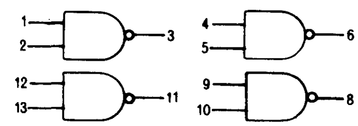
LOGIC SYMBOL :



TRUTH TABLE :

A	B	C
LO	HI	HI
HI	LO	HI
LO	HI	HI
HI	HI	LO

PIN DESIGNATION :



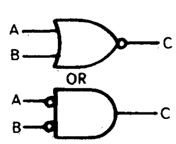
PACKAGE :

Dual in line 14 pin

MANUFACTURER'S IDENTIFICATION(S): SN7402

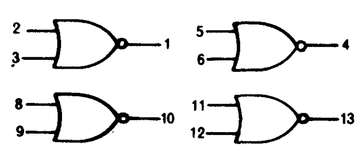
TITLE : QUAD 2 – INPUT NOR GATE

LOGIC SYMBOL :



A	B	C
LO	LO	HI
HI	LO	LO
LO	HI	LO
HI	HI	LO

PIN DESIGNATION :



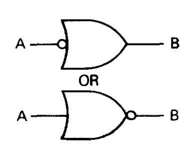
PACKAGE :

Dual in line 14 pin

MANUFACTURER'S IDENTIFICATION : SN7404

TITLE : HEX INVERTER

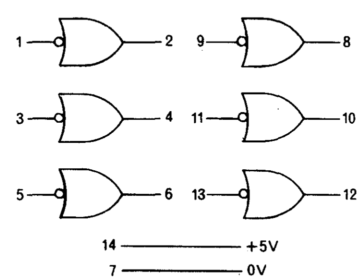
LOGIC SYMBOLS:



TRUTH TABLE:

A	B
HI	LO
LO	HI

PIN DESIGNATION



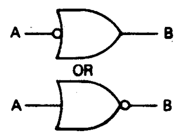
PACKAGE :

14 pin dual-in-line.

MANUFACTURER'S IDENTIFICATION : SN7405

TITLE : HEX INVERTER (WITH OPEN COLLECTOR OUTPUT)

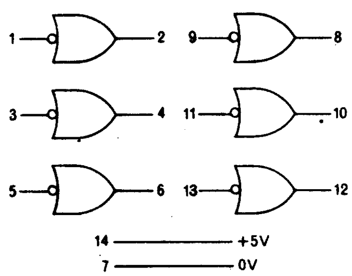
LOGIC SYMBOLS:



TRUTH TABLE:

A	B
HI	LO
LO	HI

PIN DESIGNATION



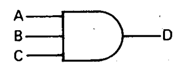
PACKAGE :

14 pin dual-in-line.

MANUFACTURER'S IDENTIFICATION : SN7411

TITLE: TRIPLE 3 INPUT 'AND' GATE

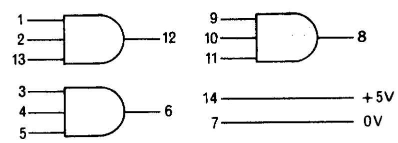
LOGIC SYMBOL:



TRUTH TABLE:

A	B	C	D
LO	LO	LO	LO
HI	LO	LO	LO
LO	HI	LO	LO
HI	HI	LO	LO
LO	LO	HI	LO
HI	LO	HI	LO
LO	HI	HI	LO
HI	HI	HI	HI

PIN DESIGNATION



PACKAGE:

14 pin dual-in-line

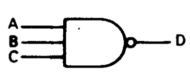
DESCRIPTION:

The output is only high if all inputs are high.

MANUFACTURER'S IDENTIFICATION(S) : SN7410

TITLE : TRIPLE 3 – INPUT NAND GATE.

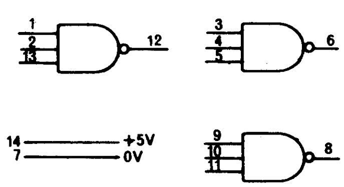
LOGIC SYMBOL :



TRUTH TABLE :

A	B	C	D
HI	HI	HI	LO
LO	HI	HI	HI
HI	LO	HI	HI
HI	HI	LO	HI
LO	LO	LO	HI

PIN DESIGNATION :



PACKAGE :

14 pin Dual in line.

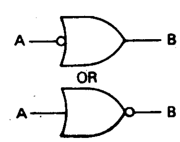
DESCRIPTION:

All highs give a low
Any low gives a high.

MANUFACTURER'S IDENTIFICATION : SN7416

TITLE : HEX INVERTER

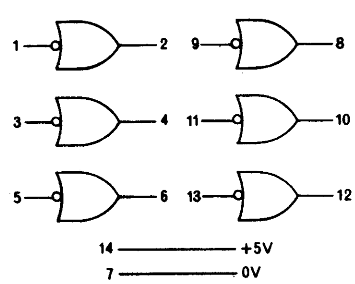
LOGIC SYMBOLS:



TRUTH TABLE:

A	B
HI	LO
LO	HI

PIN DESIGNATION



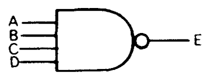
PACKAGE :

14 pin dual-in-line.

MANUFACTURER'S IDENTIFICATION(S) : SN7420 (TTL)

TITLE : DUAL 4 – INPUT NAND GATE.

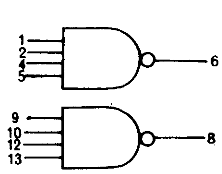
LOGIC SYMBOL :



TRUTH TABLE :

A	B	C	D	E
LO	LO	LO	LO	HI
HI	LO	LO	LO	HI
LO	HI	LO	LO	HI
LO	LO	HI	LO	HI
LO	LO	LO	HI	HI
HI	HI	HI	HI	LO

PIN DESIGNATION :



14 ——— +5 V
7 ——— 0 V

PACKAGE :

Dual in line 14 pin.

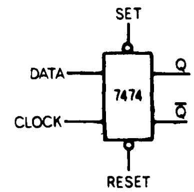
DESCRIPTION:

Any low gives a high.
All high gives a low.

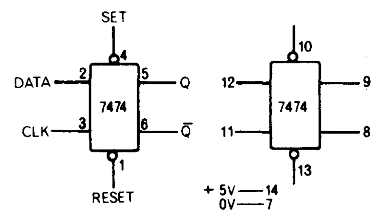
MANUFACTURER'S IDENTIFICATION(S) : SN7474

TITLE : DUAL D–TYPE FLIP–FLOP.

LOGIC SYMBOL :



PIN DESIGNATION :



PACKAGE :
14 pin Dual in Line.

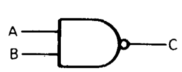
DESCRIPTION:

A low "set" will set the F.F.
A low "reset" will reset the F.F.
Triggering occurs on the leading edge of the clock (going high), setting if Data is high, resetting if Data is low.

MANUFACTURER'S IDENTIFICATION(S) : SN7426

TITLE : •QUAD 2 INPUT HIGH VOLTAGE INTERFACE NAND GATE

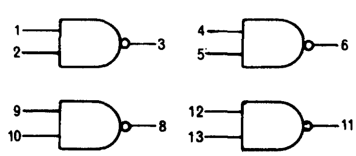
LOGIC SYMBOL :



TRUTH TABLE :

A	B	C
LO	LO	HI
HI	LO	HI
LO	HI	HI
HI	HI	LO

PIN DESIGNATION :



PACKAGE :

14 pin Dual in line.

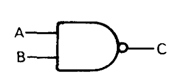
DESCRIPTION:

The 7426 is an open collector NAND gate for use with input voltages up to 15V.

MANUFACTURER'S IDENTIFICATION(S) : 9158 or 958

TITLE : QUAD 2 INPUT NAND GATE, OPEN COLLECTOR OUTPUT

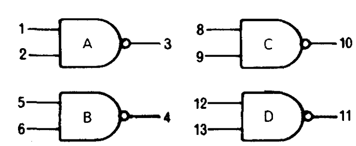
LOGIC SYMBOL :



TRUTH TABLE :

A	B	C
LO	LO	HI
HI	LO	HI
LO	HI	HI
HI	HI	LO

PIN DESIGNATION :



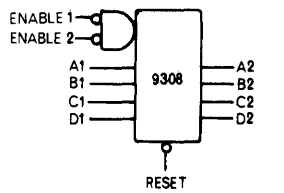
PACKAGE :

14 pin Dual in line.

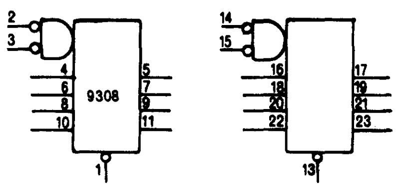
MANUFACTURER'S IDENTIFICATION(S) : 9308

TITLE : DUAL 4 – BIT LATCH

LOGIC SYMBOL :



PIN DESIGNATION :



PACKAGE :

Dual in line 24 pin.

DESCRIPTION:

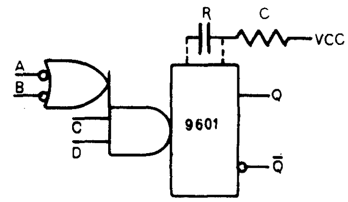
Both "Enables" must go low in order to latch the outputs 2 to the inputs 1. If either "Enable" goes high, the outputs will be unaffected by the inputs.

A low on "Reset" will reset the 4 latches to low.

MANUFACTURER'S IDENTIFICATION(S) : 9601

TITLE : RETRIGGERABLE MONOSTABLE MULTIVIBRATOR.

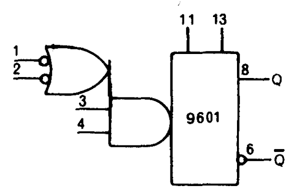
LOGIC SYMBOL :



TRUTH TABLE :

TRIGGER = (A + B) * C * D

PIN DESIGNATION :



DESCRIPTION:

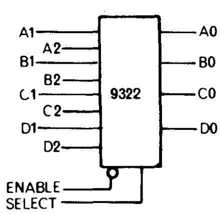
If the input conditions are met, the timer is triggered and a pulse at Q (high) and Q (low) lasts for a period of time depending on R and C.

If the input conditions are met again before the pulse has timer out, the timer retriggers to give the full period pulse from the time of the trigger. This may be disabled by connecting Q to C or D to disable the input gate.

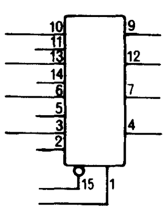
MANUFACTURER'S IDENTIFICATION(S) : 9322 (TTL)

TITLE : QUAD 2 – INPUT MULTIPLEXOR

LOGIC SYMBOL :



PIN DESIGNATION :



PACKAGE :

16 Pin Dual In Line

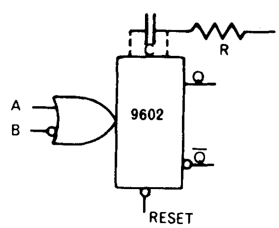
DESCRIPTION:

If ENABLE goes low, inputs 1 OR inputs 2 may be gated to the outputs 0, depending on the select line. High select gates the 1 inputs. Low select gates the 2 inputs.

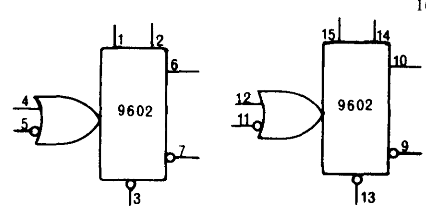
MANUFACTURER'S IDENTIFICATION(S) : 9602 (TTL)

TITLE : DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR.

LOGIC SYMBOL :



PIN DESIGNATION :



PACKAGE :

16 pin Dual in line.

+5V —— 16

0V —— 8

DESCRIPTION:

A leading edge on A or a trailing edge on B will cause High pulse on Q and a low pulse on Q for a period of time depending on R.C.

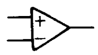
An input pulse occurring before the pulse has timer out, will reset the timer to time out the full period again.

The timer may be cut short at any time by applying a low to "RESET".

MANUFACTURER'S IDENTIFICATION(S) : LM 399

TITLE : QUAD COMPARATOR

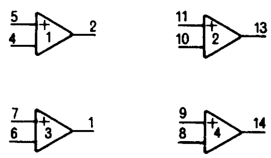
LOGIC SYMBOL :



TRUTH TABLE :

N/A

PIN DESIGNATION :



PACKAGE :

Dual in line 14 pin.

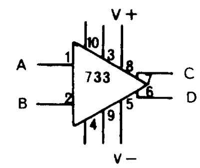
DESCRIPTION:

The LM 399 contains 4 comparators which operate from a single power source. Applications include limit comparators, analog to digital conversion etc.

MANUFACTURER'S IDENTIFICATION(S) : UA 733

TITLE : DIFFERENTIAL AMPLIFIER.

LOGIC SYMBOL :



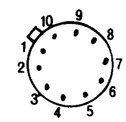
TRUTH TABLE :

N/A

PIN DESIGNATION :

See Above

PACKAGE :



TOP VIEW

DESCRIPTION:

Differences between the voltages AB are amplified and appear at C and D. Gains between 10 and 400 are possible by selecting resistances to be connected between pins 4 and 9, and 10 and 3.

MANUFACTURER'S IDENTIFICATION(S) : 723C

TITLE : VOLTAGE REGULATOR.

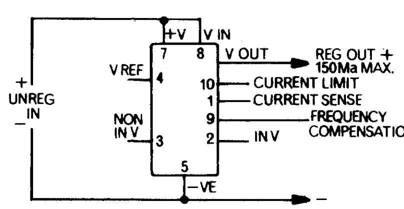
LOGIC SYMBOL :

N/A

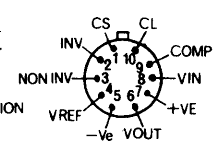
TRUTH TABLE :

N/A

PIN DESIGNATION :



PACKAGE :



DESCRIPTION:

The 723 C consists of:

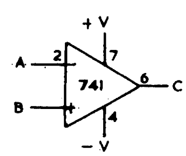
1. A voltage reference source.
2. An error amplifier with inverting and non inverting inputs.
3. A current sense circuit to reduce the output to 0V when overcurrent is sensed.
4. Frequency compensation.

Normally the reference voltage is applied to the non inverting input and the output voltage is applied to the inverting input in order to regulate. Current limit and current sense are applied across a low value series resistor to sense an over current.

MANUFACTURER'S IDENTIFICATION(S) : UA 741C

TITLE : OPERATIONAL AMPLIFIER.

LOGIC SYMBOL :



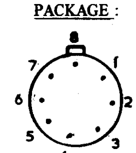
TRUTH TABLE :

N/A

PIN DESIGNATION :

As above

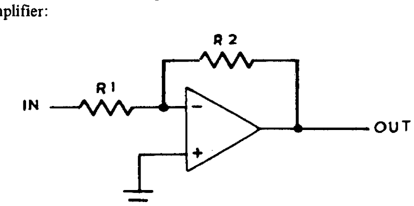
PACKAGE :



TOP VIEW

DESCRIPTION:

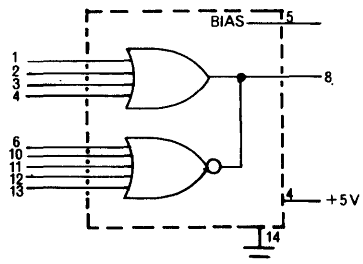
If B goes more positive than A, C goes high.
If A goes more positive than B, C goes low.
Straight amplifier:



MANUFACTURER'S IDENTIFICATION(S) : MC 1218

TITLE : MECL TO TTL LEVEL TRANSLATOR.

LOGIC SYMBOL :



TRUTH TABLE :

N/A

PIN DESIGNATION :

As above

PACKAGE :

14 pin Dual in line.

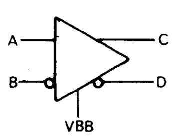
DESCRIPTION:

Pin 5 produces a reference bias. If pin 4 is connected to the bias, the chip is used as a 5 input NOR Gate. If pin 6 is connected to pin 5, the chip can be used as a 4 input OR Gate.

MANUFACTURER'S IDENTIFICATION(S) : MC 1235

TITLE : TRIPLE LINE RECEIVER/DIFFERENTIAL AMPLIFIER.

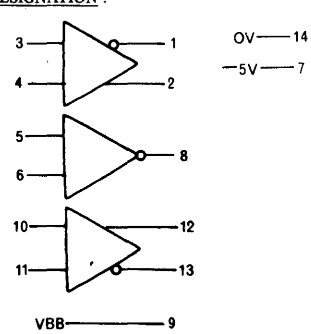
LOGIC SYMBOL :



TRUTH TABLE :

A	B	C	D
1	VBB	1	0
0	VBB	0	1
VBB	1	0	1
VBB	0	1	0

PIN DESIGNATION :



PACKAGE :

Dual in line 14 pin

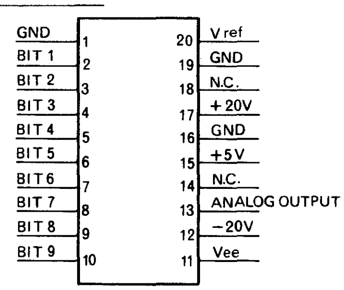
DESCRIPTION:

This change is used to convert low amplitude, analog signals to fast switching square waves suitable for triggering gates, flip-flops etc.

MANUFACTURER'S IDENTIFICATION : CS 1020–9 (CYCON)
UHM–500 (HYBRID SYSTEMS)
Z50212 (ZELTEX)

TITLE **9-Bit Hybrid Digital-to-Analog Converter.**

LOGIC SYMBOL:



TRUTH TABLE

N/A

PIN DESIGNATION

As above

PACKAGE:

Non-standard, 20-pin Dual-in-line.
(2.2" x 1.5" x 0.4")

DESCRIPTION:

The device is a 9-bit digital-to-analog converter using ladder network techniques. The separate circuit elements are combined in a single, encapsulated, hybrid module.

CIRCUIT DESCRIPTION

INPUT/OUTPUT INTERFACE

The I/O Interface, figure 2-1, is part of the CEM board. Input signals from the controller are received by the inverter gates of IC's 6, 7 and 9 which perform the function of buffering and level restoration. Some of the outputs from these gates are sent direct to the drive modules, while others must be gated with UNIT SELECT.

The signals that are applied directly to the drive module are all ADDRESS lines and HEAD SELECT.

The signals that are gated with UNIT SELECT and then routed to relevant drive module are the READ ENABLE, SEEK, WRITE DATA (via write data encoder), and WRITE ENABLE.

Output signals from the drive modules first enter IC's 10 and 11, which are multiplexor chips. These select the relevant set of signals from the drive module according to the state of UNIT SELECT. The selected set of signals is then passed to the NAND gates of IC's 4 and 5, which function as line drivers. The READ DATA line does not pass through the multiplexor chips, but is transmitted direct to the controller by a low impedance transistor driver, Q9. The DATA CLOCK is also sent by means of a low impedance transistor driver, Q10, but is first selected from the relevant drive module by multiplexor IC10.

A list of mnemonic signal terms is as follows:

Mnemonic	Signal Name
UNIT SEL	Unit Select
ADD - 1 ADD 256	Address Lines (9 of)
HEAD SEL	Head Select
SEEK	Cylinder Seek Execute
RD EN	Read Enable
WRT EN	Write Enable
WRT DATA	Write Data
FILE OP	File Operational
POS SET	Position Settled
RD DATA	Read Data
DATA CLK	Data Clocks
INDEX	Index Pulse
SECTOR	Sector Pulse
ILL ADD	Illegal Address
POS ERR	Position Error
WIH	Write Inhibit

POSITIONING SYSTEM

POWER UP AND FIRST SEEK

Refer to figures 2-2, 2-3 and 2-4.

If the POWER ON switch is depressed, ac power is applied through an R.F. line filter to the following (see figure 2-3):

dc Power Supplies (+36V, −36V, +20V, −20V, +12V, +5V)

Clean Air Unit (if present).

Solid State Motor Relay K4.

With dc present to the SCM/SCM-1 board, and the RUN/STOP switch in the STOP position, the MOTOR ON signal will be LOW and CART DOOR EN signal HIGH (floating).

Transistor Q15 (SCM/SCM-1) is a unijunction transistor with an R-C network to provide a timing period of 30 seconds, but is at this stage disabled by MOTOR ON being LOW. Flip-flop IC22A remains reset and ENERGISE SOL is HIGH, turning on transistor Q2 on the PAM board. This picks the receiver solenoid and unlocks the handle.

Insertion of a cartridge will activate the cartridge switch, S1, which places +12V onto relay K4, pin 3 (motor), and K2, pin A (servo). If the RUN/STOP switch is now depressed the N.O. contacts ground K4 pin 4, 115 VAC is applied to the motor drive, and the disk commences to rotate. At the same time, the other set of contacts will cause MOTOR ON to float and Q6 unconditionally sets IC22A. The set output of IC22A is inverted by IC27C. ENERGISE SOL is therefore low to transistor Q2 base on the PAM board. Transistor Q2 turns off, the receiver solenoid is dropped and the receiver is now locked.

The components transistors Q7, Q8, Q9 and IC's 26A/26B and IC's 20A/20B form a timer circuit which will enable the servo 4 seconds after the disk is up to speed.

When the disk reaches 1200 rpm, the INDEX pulses will cause UP SPEED to be generated from the Read/Write Amplifier. UP SPEED is gated with the reset side of IC26B, turning off transistor Q7 causing the unijunction transistor network around transistor Q8 to start timing out. When 4 seconds have elapsed, transistor Q8 switches off, turning off transistor Q9 which clocks IC26A to the set state if UP SPEED is still high.

The set output of IC26A is gated with POS SET/ from IC15A, and ERROR, which is HIGH when the error voltage from the servo is greater than ±56mV, indicating that the positioning system is not in detent. When the above conditions are met, IC25B and IC16B cause SVO EN to go HIGH to enable the coarse servo loop.

After a further 4 seconds, transistor Q8 will again cause transistor Q9 to output a high, and this clocks IC26B to the set state. The set output of IC26B is gated with POS SET/ to turn on transistor Q7, which deactivates the timer circuit around transistor Q8.

When IC26A sets 4 seconds after UP SPEED, the set output is gated through IC17D and IC23C to pro-

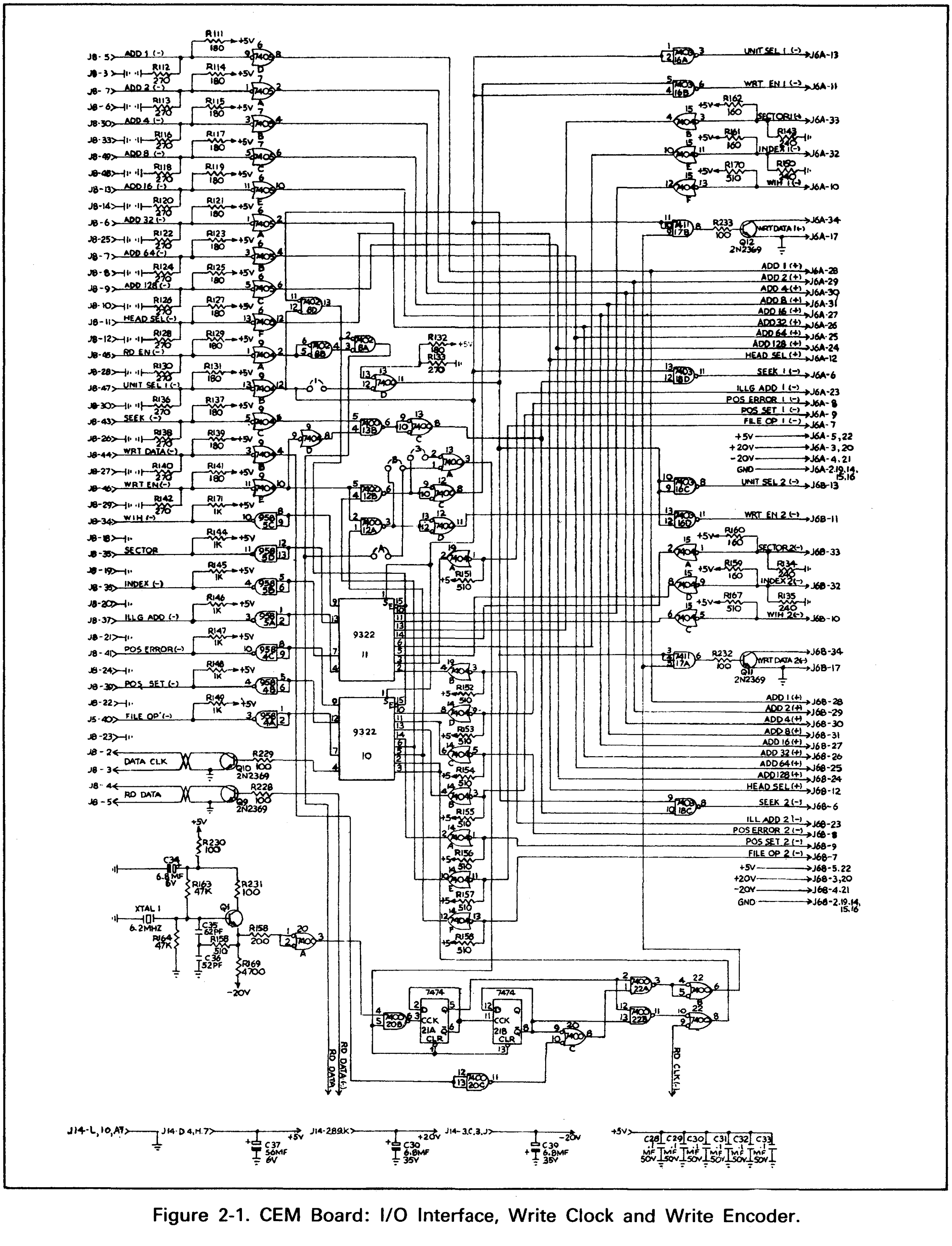


Figure 2-1. CEM Board: I/O Interface, Write Clock and Write Encoder.

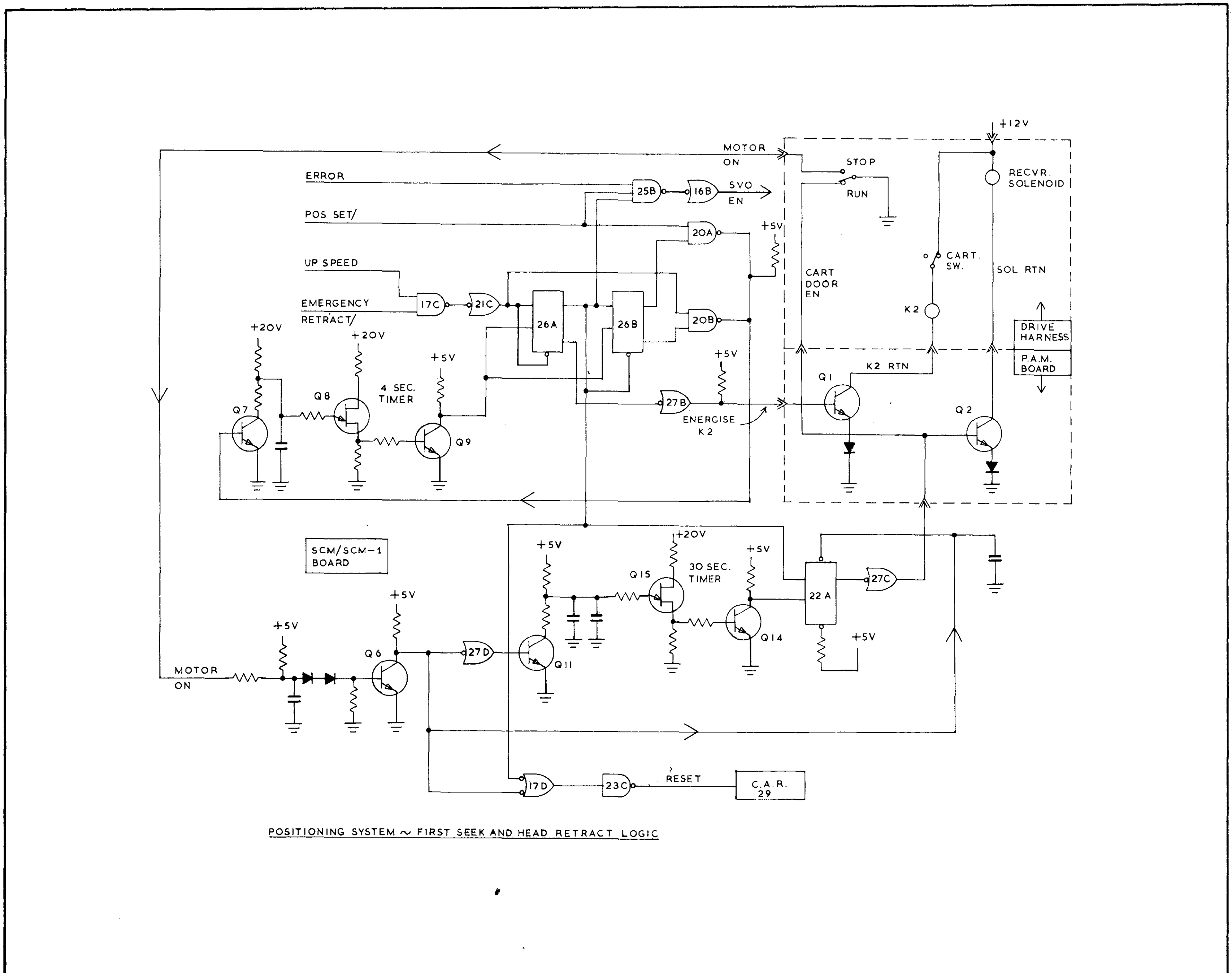


Figure 2-2. Positioning System First Seek And Head Retract Logic

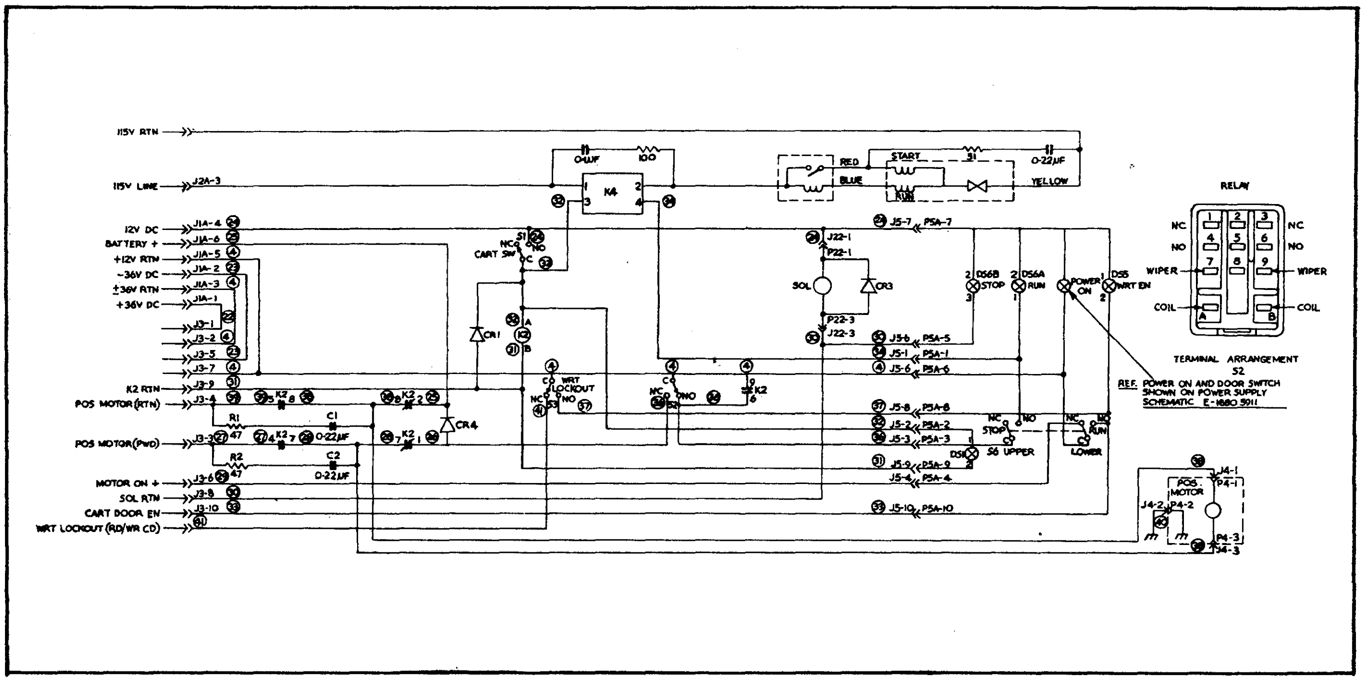


Figure 2-3. Main Harnesses, Switches And Relays.

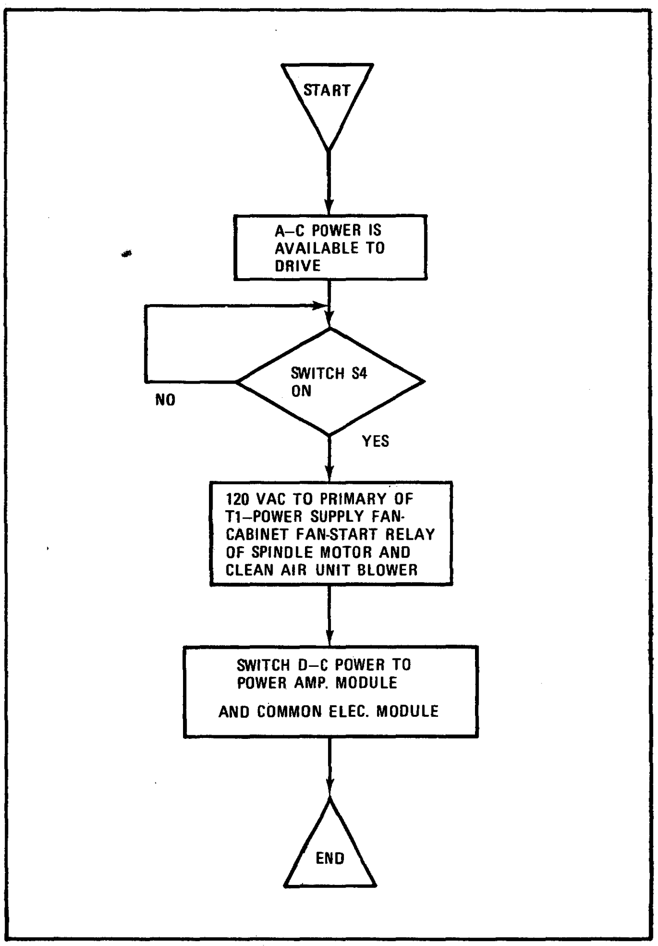


Figure 2-4. Power-Up Flow Chart

vide RESET which will clear the Cylinder Address Register to 000. In addition the reset side is inverted to give ENERGISE K2, which is applied to transistor Q1 base on the PAM board. Transistor Q1 turns on, and relay K2 picks, providing a path through contacts 4/7 and 5/8 from the servo to the positioner coil.

Since the heads are not positioned at track 00, the voltage from the linear potentiometer wiper will not equal the voltage from the DAC, and an error voltage is therefore developed, causing the heads to move off the head load ramp until positioned over track 000.

The system enters into detent, and after the settle delay, POS SET will be applied to the CEM board for transmission to the controller.

NOTE

A detailed description of the coarse and fine servo loops is given in PROGRAM SEEK.

POWER DOWN AND HEAD RETRACTION

Depression of the RUN/STOP button a second time removes the ground from relay K4 pin 4, 115 VAC is no longer available to the motor, and the disk slows down.

The other set of contacts on the RUN/STOP switch ground MOTOR ON, which turns on transistor Q6 and develops RESET (via gates IC21D, IC17D and IC23C) to clear the Cylinder Address Register to 000. If the heads are not already at track 000, ERROR will go HIGH causing the servo to return the

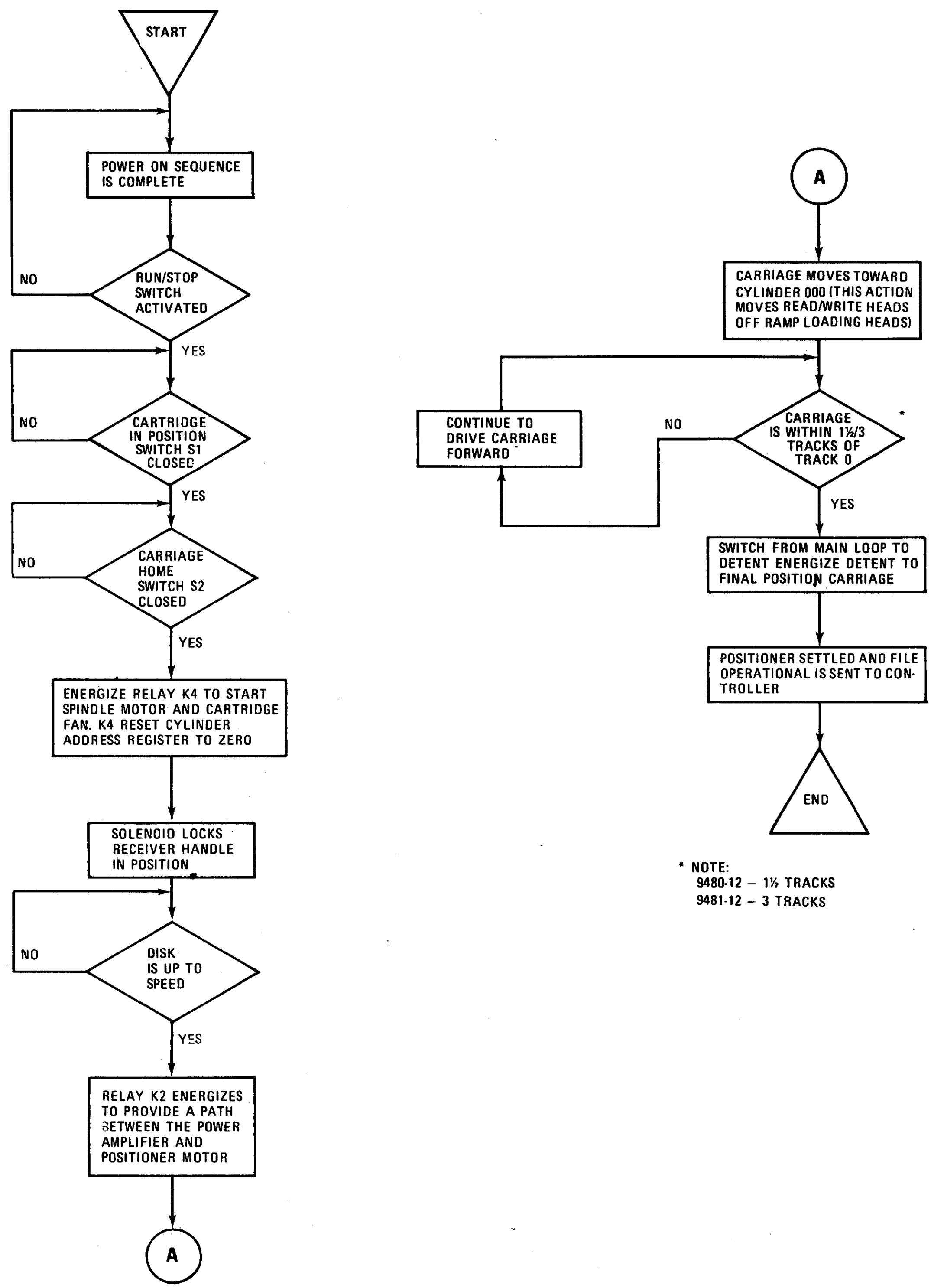


Figure 2-5. First Seek Flow Chart

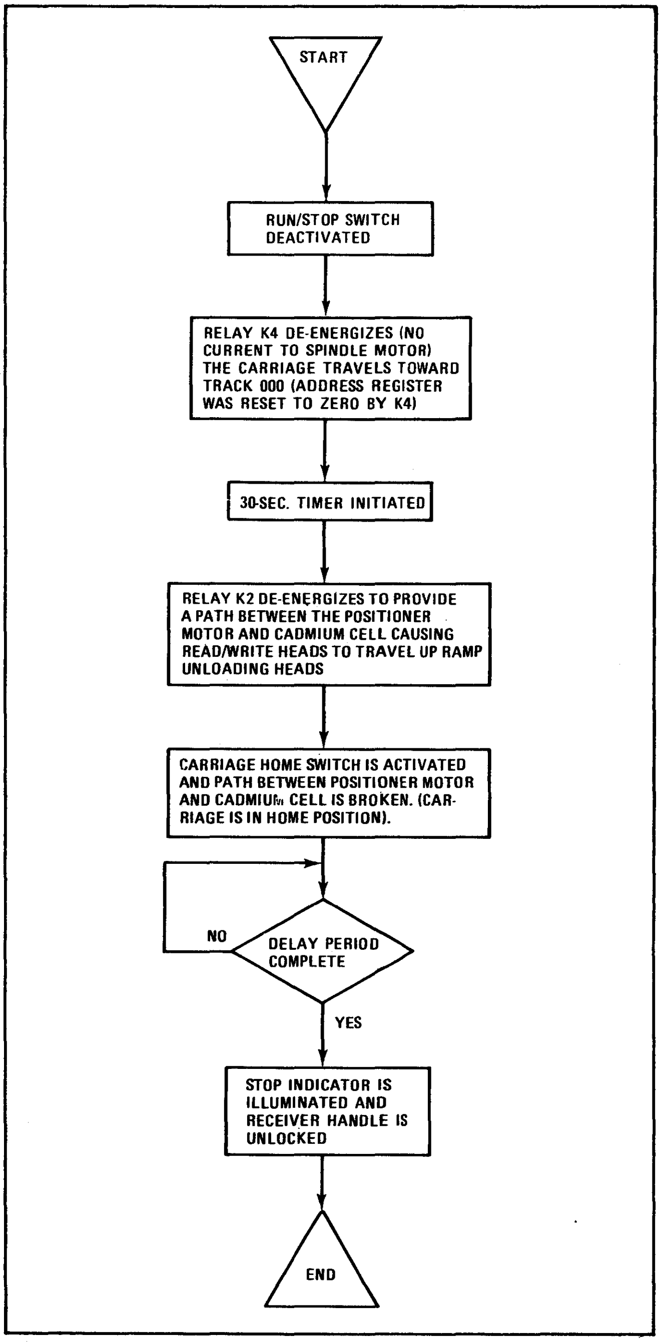


Figure 2-6. Power-Down And Head Retraction Flow Chart

heads to track 000. At the same time, the RUN/STOP switch floats CART DOOR EN, which partially enables transistor Q2 (PAM).

When the disk slows to 1200 rpm, the INDEX pulses will cause UP SPEED to go low from the Read/Write Amp. This unconditionally clears IC26A, and the reset side will turn off transistor Q1 on the PAM board, thus dropping relay K2. Contacts 17 and 28 of relay K2 now enable the battery voltage to the positioner coil, retracting the heads from the disk and on to the head load ramp. Once in the home position, the Home Position switch breaks the path to the battery.

MOTOR ON LOW signal turns on transistor Q15 and after 30 seconds will turn off and clock the reset side of IC26A (now LOW) into IC22A, which therefore resets. The set output is now LOW and is inverted and passed to transistor Q2 (PAM) which can now turn on. SOL RTN goes LOW, the receiver solenoid is picked, and the receiver handle unlocked.

PROGRAM SEEK

COARSE AND FINE SERVO LOOPS

Refer to figures 2-7, 2-8 and 2-9.

Upon receipt of a SEEK pulse, whatever is present on the ADD lines will be strobed into the Cylinder Address Register (CAR). As there is no output gating, the CAR value is immediately converted by the DAC to an equivalent voltage, emerging on pin 13.

The terminal wiper voltage (from the linear potentiometer), is input to IC9, which is a voltage follower. The purpose of IC9 is to buffer the wiper voltage, and by means of resistor R47 the output voltage can be adjusted to 0 volts when the heads are at track 00. (Whereas the input is −85mV). Transistor Q2 and associated components form a current source.

The buffered wiper voltage from IC9 is compared with the DAC voltage by IC10 and IC11:

The error signal resulting from IC10 is amplified by IC12 and passed to the source of field effect transistor (FET) Q5. When the gate of FET Q5 is turned on by SVO EN, the error voltage will be further amplified by IC13 and used to drive the positioner coil via the PAM board. Resistor R66 defines the gain of IC12, and is used to adjust the speed at which the heads move under the control of the coarse servo. (This is referred to as the 'long servo gate' in the Test and Adjustment Procedure).

The error signal resulting from IC11 is monitored by the differential comparators of IC8.

The purpose of IC8 is to detect when the heads are not in close proximity to the desired track. If the inputs to IC8 are more positive than +56mV or more negative than −56mV, the comparator will trigger causing the ERROR signal to go HIGH. This resets the POS SET flip-flop and initiates the coarse servo loop.

With the ERROR signal HIGH, POS SET/ and IC26A set (from first seek), the output of IC25B will go low.

The output of IC25B is inverted by IC15B to give SVO EN.

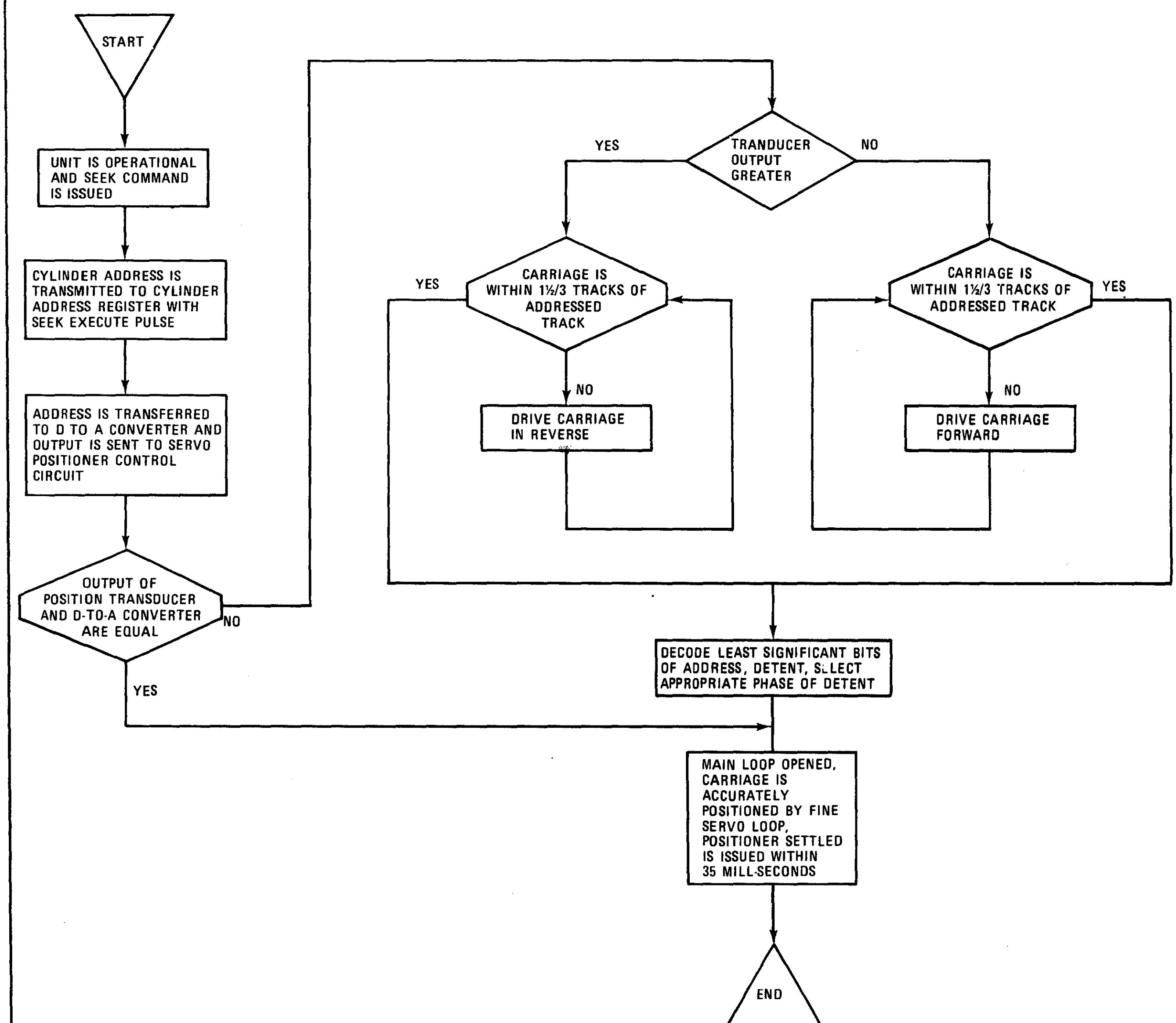


Figure 2-7. Operational Flow Chart Programmed Seek

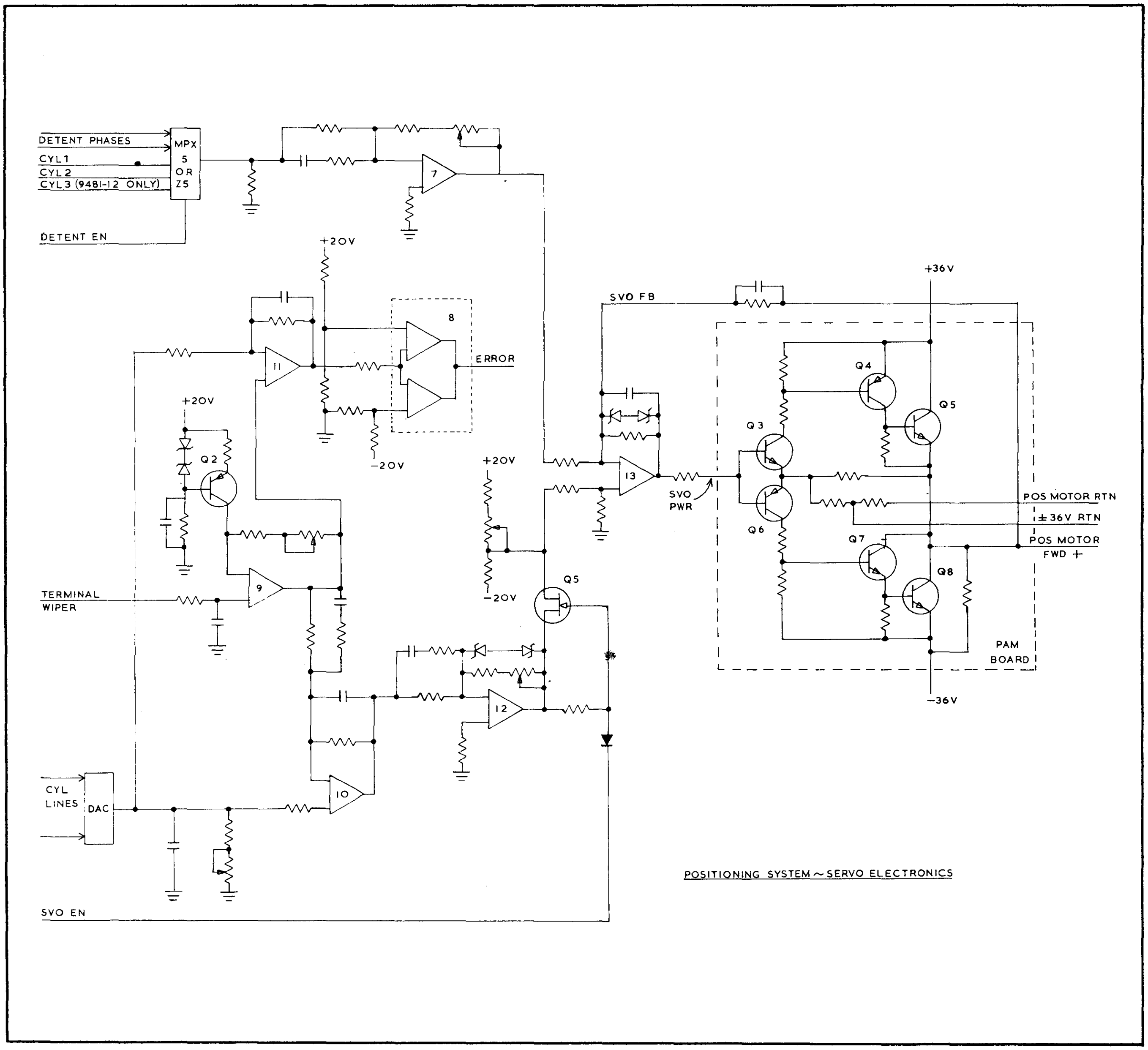


Figure 2-8. Positioning System Servo Electronics

SVO EN is amplified by transistors Q3 and Q4 and turns on the gate of FET Q5.

The output of IC12 is now enabled through Q5 to IC13.

IC13 now amplifies the resultant error voltage from the wiper and DAC, to give SVO PWR.

SVO PWR is transmitted to the PAM board, which provides power amplification to drive the positioner coil.

The carriage starts to move along the guide towards the desired track. If SVO PWR is positive, the carriage moves forward. If SVO PWR is negative, the carriage moves backward.

The servo cannot enter into detent due to the high inputs to IC16A. Pin 2 is high from ERROR, via IC21F and IC17A; pin 1 is high due to POS SET flip-flop being reset.

As the carriage moves along the guide, the wiper voltage approaches the DAC voltage. The error voltage output from IC11 therefore approaches zero. When it is within ±56mV of zero, IC8 will trigger and ERROR goes LOW. This happens when the heads are within 1½ tracks (9480) or 3 tracks (9481) of the desired address.

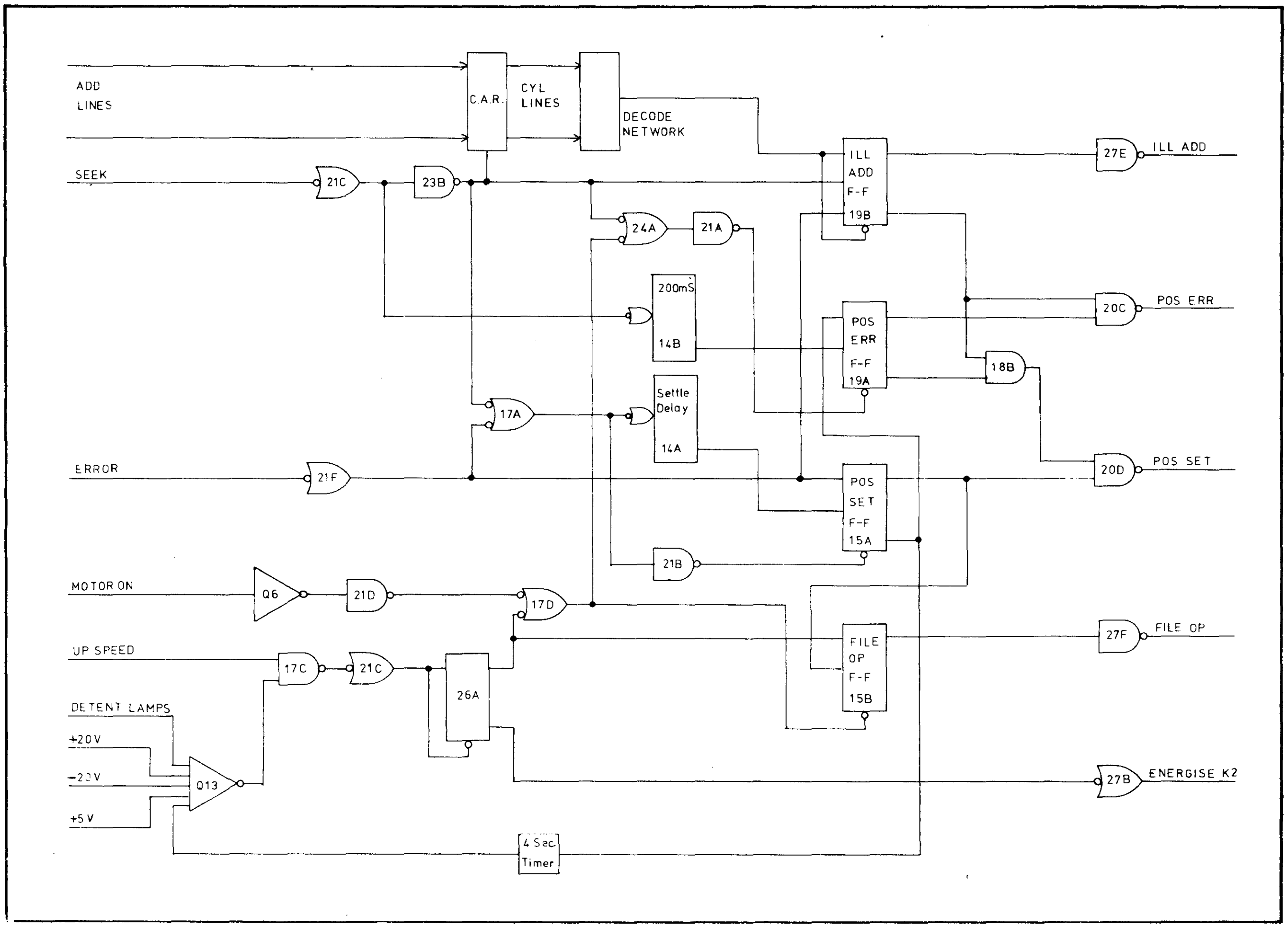


Figure 2-9. Positioning System. Control And Error Detection Logic.

With the ERROR signal LOW, the servo must now go into detent as follows:

IC21F will place a HIGH on the 'D' input to POS SET flip-flop IC15A.

IC21F and IC17A trigger IC14A timer. The purpose of the timer is to allow damping of carriage oscillation before sending POS SET to the controller. The period of this settle delay can be adjusted by resistor R133. (It is referred to as the 'short servo gate' in the Test and Adjustment Procedure).

IC21F and IC17A also input a LOW to IC15A causing DETENT EN to go high.

The output from IC17A also disables IC25B. SVO EN is now LOW and FET Q5 turns off.

This removes the error voltage from IC13, and there is no longer any current from the coarse servo loop to drive the positioner coil.

DETENT EN enables multiplexor chips IC5 (9480) or ICZ5 (9481).

Although the detent circuitry differs in detail for the 2 styles of drive, the principle is the same. The multiplexor chip IC5 (or ICZ5) selects the correct phase from the detent amplifiers, by decoding the 2 (9480) or 3 (9481) least significant bits from the CAR. (See 'Detent Circuit Details').

The selected detent phase is input to IC7 and amplified, then applied to IC13. Resistor R23 defines the gain of the servo while in detent, and is used to adjust the response as the heads come to a stop over the desired track. (This is referred to as 'Servo Settle Time' in the Test and Adjustment Procedure).

The PAM board now provides power input to the positioner coil under the control of the detent amplifiers.

After the settle delay timer IC14A has timed out, the reset output goes low, and inputs a clock pulse to IC15A (POS SET).

IC15A sets, and POS SET is transmitted to the I/O interface.

The drive is now ready for read and write commands.

DETENT CIRCUIT DETAILS

The detent amplifier networks are different for the two styles of drive, and are therefore described separately.

9480-12 DETENT

With the DETENT EN signal high the multiplexor chip IC5 will be enabled. This decodes the two least significant bits CYL1 and CYL2 from the CAR into one out of four possible states. The resultant signal is gated with one of the outputs from the four detent phase amplifiers IC's 1, 2, 3 and 4.

9480-12 OPTICAL DETENT SYSTEM

The optical or electronic detent assembly consists of two glass gratings, one fixed to the baseplate casting and the other attached to the carriage frame allowing it to move, thus forming a vernier scale. Two light sources, A lamp and B lamp, illuminate, through the glass plates, two separate pairs of photocells. One pair giving the A output and the other pair giving the B output.

Figure 2-10 is the schematic diagram for the A output pair of photocells. The glass vernier scale will allow only 3 different combinations of light bias on the photocell pair.

1. Equal amount of light allowed to enter each photocell. This will saturate both A1 and A2 resulting in a 0 volt output at A.

2. Light allowed to enter photocell A1 and light not allowed to enter photocell A2. This will result in A1 being saturated and A2 will be cut off, therefore the output at A will be maximum Negative.

3. Light not allowed to enter A1 and light allowed to enter A2. This will cut off A1 and saturate A2 giving an output at A of maximum Positive.

These three conditions are essential in positioning the heads in the desired position. Once the Fine Positioning circuit is activated and the proper detent phase has been selected, then the output of the detent circuit is used in one of three ways.

1. Head is on top of desired track. In this position the detent output will be 0 volts. This will maintain the positioner in this position.

2. Head is beyond the desired track. Here we need a Negative voltage from the detent output to cause the positioner to back up to the desired track.

3. Head is short of the desired track. Here we need a Positive voltage from the detent output to push the positioner forward to the desired track.

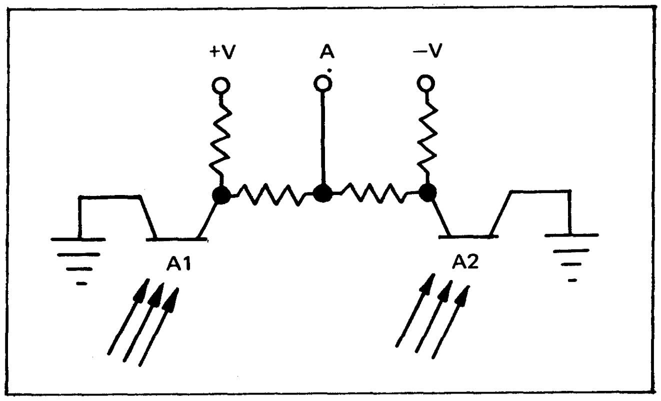


Figure 2-10. Photocell Pair

The detent assembly is not used until the Coarse Positioning has placed the head within 1 1/2 cylinders of the desired address, and the multiplexor chip will use the two low order address bits to select the proper detent output phase.

Referring to figure 2-11a, assume the head is settled on cylinder N. This will show that the venier is positioned to give equal light to A1 and A2 photocells yielding 0 volts out at A. If we increase the address one more cylinder (N+1), figure 2-11b, will indicate the position of the venier thus allowing equal amount of light to B1 and B2 photocells giving 0 volts out of B. Advancing the head one more address (cylinder N+2), figure 2-11c, A1 and A2 photocells will have equal light on them giving 0 volts out at A. The last different position will show by advancing the head one more cylinder (N+3), figure 2-11d. Here B1 and B2 photocells will have equal amount of light on them producing 0 volts out of B.

Figure 2-11e shows the signal phase relationship at the output of the photocells. The B photocell will lag the A photocell by 90° and each NOT photocell will lag its compliment by 180° (for example, A lags A by 180°). Therefore, there are four outputs each 90° apart.

9481-12 DETENT

In the case of the 200 t.p.i. model, an extra board is provided to accommodate the detent amplifiers (SCM-2 board). This is 'piggy-backed' onto the SCM-1 board, and plug connectors carry the inter-board signals.

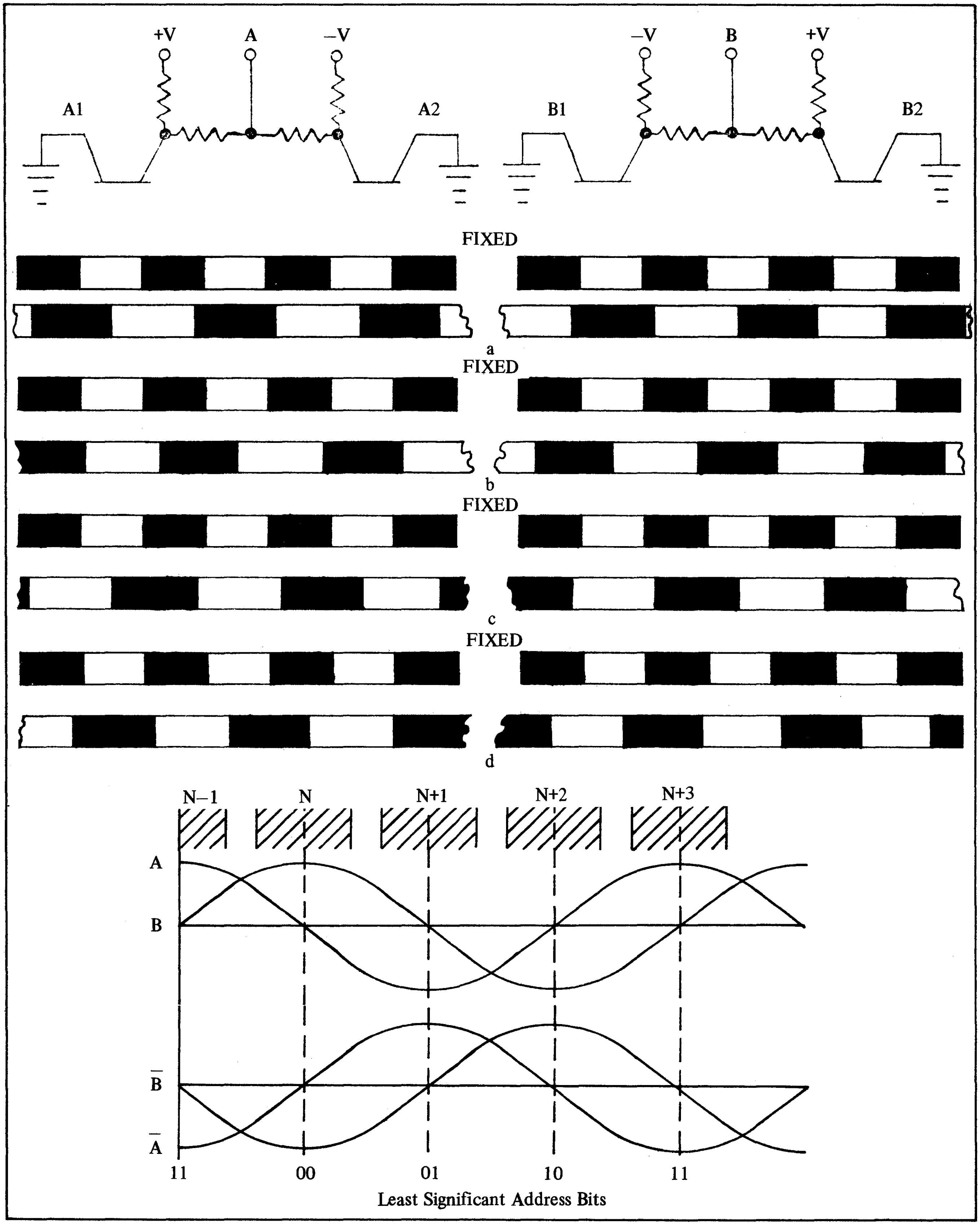


Figure 2-11. 9480-12 Optical Detent

The cylinder address register and multiplexor chip (ICZ5) are mounted on the SCM-2, instead of the SCM-1 board, and an extra flip-flop is used to store bit 9 of the cylinder address (ICZ6).

The DETENT EN signal HIGH enables multiplexor ICZ5. This decodes the three least significant bits, CYL1, CYL2 and CYL3, from the CAR into one out of eight possible states. The resultant signal is gated with one of the outputs from the eight detent phase amplifiers, ICZ1A through ICZ4B.

9481-12 OPTICAL DETENT SYSTEM

The optical or electronic detent assembly consists of two glass gratings, one fixed to the baseplate casting and the other attached to the carriage frame allowing it to move, thus forming a venier scale. One light source illuminates through the glass plates, four separate pairs of photocells. One pair giving the A output, one pair giving the B output, one pair giving C output and the last pair giving D output.

Figure 2-12 is the schematic diagram for the A output pair of photocells. The glass venier scale will allow only 3 different combinations of light bias on the photocell pair.

1. Equal amount of light allowed to enter each photocell. This will saturate both A1 and A2, resulting in a 0 volt output at A.
2. Light allowed to enter photocell A1 and light not allowed to enter photocell A2. This will result in A1 being saturated and A2 will be cut off, therefore, the output at A will be maximum Negative.
3. Light not allowed to enter A1 and light allowed to enter A2. This will cut off A1 and saturate A2 giving an output at A of maximum Positive.

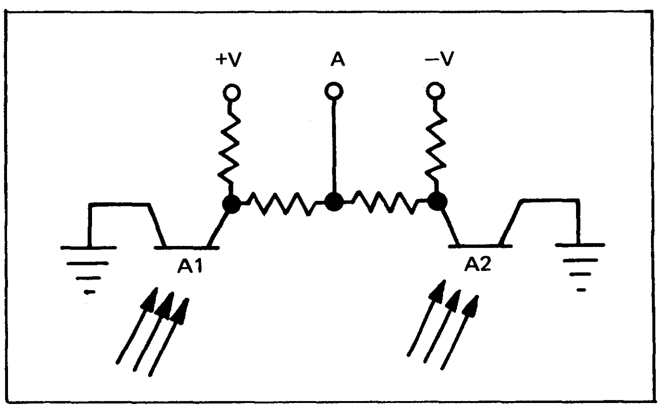


Figure 2-12. Photocell Pair

These three conditions are essential in positioning the heads in the desired position. Once the Fine Positioning circuit is activated and the proper detent phase has been selected, then the output of the detent circuit is used in one of three ways.

1. Head is on top of desired track. In this position, the detent output will be 0 volts. This will maintain the positioner in this position.
2. Head is beyond the desired track. Here we need a Negative voltage from the detent output to cause the positioner to back up to the desired track.
3. Head is short of the desired track. Here we need a Positive voltage from the detent output to push the positioner forward to the desired track.

The detent assembly is not used until the Coarse Positioning has placed the head within 3 cylinders of the desired address. Also, the multiplexor chip will use the three low order address bits to select the proper detent output phase.

Referring to figure 2-13a assume the head is settled on cylinder N. This will show that the venier is positioned to give equal light to A1 and A2 photocells yielding 0 volts out at A. If the address is increased one more cylinder (N+1), then figure 2-13b will indicate the position of the venier thus allowing equal amount of light to B1 and B2 photocells giving 0 volts out of B. Advancing the head one more address (cylinder N+2), figure 2-13c, A1 and A2 photocells will have equal light on them giving 0 volts out at A. By advancing the head one more cylinder (N+3), figure 2-13d, B1 and B2 photocells will have equal amount of light on them producing 0 volts out of B.

Figure 2-13e shows the signal phase relationship at the output of the photocells. The C photocell will lag the A photocell by 45° and each NOT photocell will lag its compliment by 180° (for example, A lags A by 180°). Therefore, there are eight outputs each 45° apart. Figure 2-14 is a chart showing which photocell is used for the address indicated.

POWER AMPLIFIER MODULE (Refer to figure 2-8).

This provides power drive to the positioner coil in response to the value of SVO PWR (+ = FWD) from IC13 on the SCM/SCM-1 board.

If SVO PWR is positive, Q3, Q4 and Q5 will turn on and drive a positive voltage up to +36V to the coil via POS MOTOR FWD+.

If SVO PWR is negative, Q6, Q7 and Q8 will turn on and drive a negative voltage down to −36V to the coil via POS MOTOR FWD+.

The output to the coil, POS MOTOR FWD+ is also fed back as an input to IC13 on the SCM/SCM-

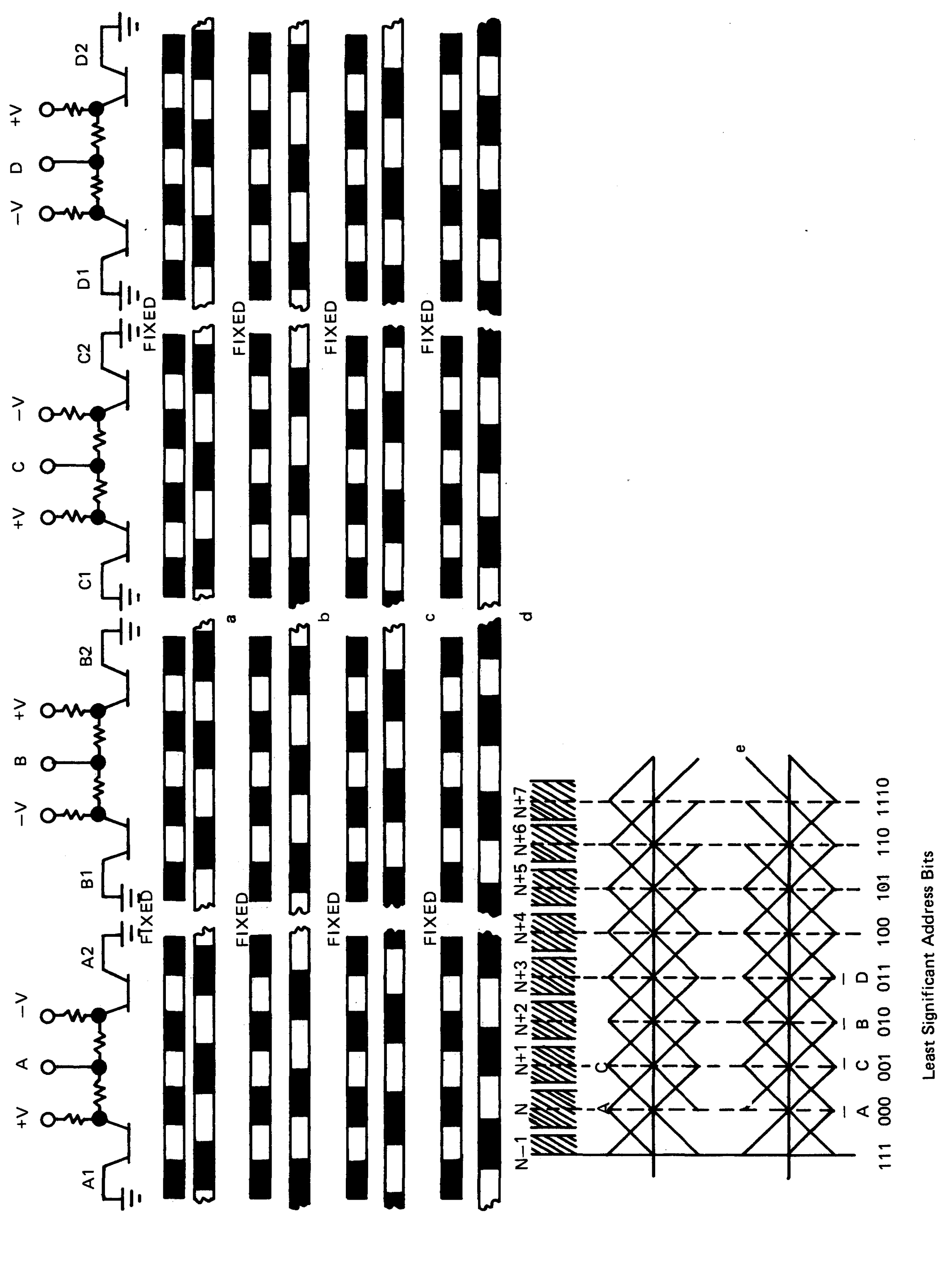


Figure 2-13. 9481-12 Optical Detent

Photocell Output for Cylinder

$\overline{A}$	HD	$\overline{C}$	HD	$\overline{B}$	HD	$\overline{D}$	HD	A	HD	C	HD	B	HD	D	HD
0		1		2		3		4		5		6		7	
8		9		10		11		12		13		14		15	
16		17		18		19		20		21		22		23	
24		25		26		27		28		29		30		31	
32		33		34		35		36		37		38		39	
40		41		42		43		44		45		46		47	
48		49		50		51		52		53		54		55	
56		57		58		59		60		61		62		63	
64		65		66		67		68		69		70		71	
72		73		74		75		76X		77		78		79	
80		81		82		83		84		85		86		87	
88		89		90		91		92X		93		94		95	
96		97		98		99		100X		101		102		103	
104		105		106		107		108		109		110		111	
112		113		114		115		116		117		118		119	
120X		121		122		123		124		125		126		127	
128		129		130		131		132		133		134		135	
136		137		138		139		140X		141		142		143	
144		145		146		147		148		149		150		151	
152		153		154		155		156		157		158		159	
160		161		162		163		164		165		166		167	
168		169		170		171		172		173		174		175	
176		177		178		179		180		181		182		183	
184		185		186		187		188		189		190		191	
192		193		194		195		196		197		198		199	
200		201		202		203		204		205		206		207	
208		209		210		211		212		213		214		215	
216		217		218		219		220		221		222		223	
224		225		226		227		228		229		230		231	
232		233		234		235		236		237		238		239	
240		241		242		243		244		245		246		247	
248		249		250		251		252		253		254		255	
256		257		258		259		260		261		262		263	
264		265		266		267		268		269		270		271	
272		273		274		275		276		277		278		279	
280		281		282		283		284		285		286		287	
288		289		290		291		292		293		294		295	
296		297		298		299		300		301		302		303	
304		305		306		307		308		309		310		311	
312		313		314		315		316		317		318		319	
320		321		322		323		324		325		326		327	
328		329		330		331		332		333		334		335	
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376		377		378		379		380		381		382		383	
384		385		386		387		388		389		390		391	
392		393		394		395		396		397		398		399	
400		401		402		403		404		405					

NOTE: ◯ Indicates tracks used for alignment

Figure 2-14. 9481-12 Detent Phase Table

1 board, (SVO FB). This provides negative feedback to control the stability of the positioner motor.

FAILURE DETECTION CIRCUITRY (EMERGENCY HEAD RETRACT)

Refer to figure 2-15, part of SCM/SCM-1 board.

Diodes CR18 through CR21 form a 4-input 'OR' gate. If any diode is forward biased, Q13 will turn on and input a low to IC17C. The output of IC17C is inverted by IC21C, which clears IC26A unconditionally. The reset output of IC26A is inverted by IC27B and turns off the current to relay K2, thus causing the battery to retract the heads. At the same time, IC26A set output clears IC26B. This inputs a low to IC25C and IC22B sets. The output of IC22B is inverted by IC27A which forward biases CR18 and permanently latches Q13 in the 'ON' state.

The conditions which will cause this are:

1. Failure of detent lamp. If no current is flowing in the detent lamp, Q10 will turn off and forward bias CR19.
2. Failure of −20V. This will forward bias CR20.
3. Failure of +20V. Q12 turns off and CR21 is forward biased.
4. Failure to achieve POSITION SETTLED 4 seconds after a SEEK command. Each time a seek is initiated, POS SET/ and IC26B cause IC20A to trigger the 4 second timer (Q7, Q8 and Q9). If POS SET/ fails to go low before the 4 seconds have timed out, a low will be input to IC25C. IC22B sets, CR18 is forward biased, and Q13 turns on to initiate head retraction.

In the event of an uncommanded head retract, it should be noted that the cause may be deduced by finding out which diodes (CR18 through CR21) are forward biased.

If CR18 only is forward biased, then the servo has failed to detent 4 seconds after a SEEK command. (The usual cause of this is servo oscillation).

If CR19 and CR18 are both forward biased, then the detent lamp has failed.

If CR20 and CR18 are both forward biased, then −20V has failed.

If +5V fails, then there will be no power to IC27B. ENERGISE K2 will therefore be low causing the heads to retract.

ERROR DETECTION

POSITION ERROR

Refer to figure 2-16, part of SCM/SCM-1 board.

After a SEEK command has been issued, the SEEK Pulse activates the positioner error timing network IC14B and clears the IC19A F/F. If, after 200 milliseconds, the SEEK operation is not completed, the IC19A POS E F/F (Position Error) will SET. Under normal conditions, the IC19A POS E F/F is inhibited to SET by IC15A POS SET F/F.

ILLEGAL ADDRESS

Refer to figure 2-17, part of SCM board.

The illegal address circuit consists of 3 NAND gates (IC24C, IC24D, and IC18C), 2 NOR gates (IC24B and IC25A) and six inverters (IC23A, B, C, D, E, F and IC27E). These are arranged in a decoding network such that a summed address at IC18C in excess of cylinder 202 (9480-12) or 405 (9481-12) will set the Illegal Address flip-flop IC19B, using the trailing edge of the SEEK pulse. The carriage is prevented from seeking the illegal address by disabling CYL128 (9480-12) or CYL256 (9481-12). However, the carriage will still seek to the address represented by the remaining bits of the CAR.

READ/WRITE SYSTEM

WRITE OPERATION

The write circuitry is contained partly on the CEM board and partly on the RWA board.

WRITE ENCODING

Refer to figure 2-18, part of CEM board.

In order to write the data received from the CPU, the unit must convert the data format and WRT EN (Write Enable) must be present. The data is received in NRZ (Non-Return to Zero) format and converted into Double Frequency format. A crystal controlled oscillator circuit consisting of XTAL 1 and transistor Q1 establishes the basic clock frequency of 6.2 MHz. The output of the crystal oscillator is inverted by IC20A and then inputs to one leg IC20B. The other leg of IC20B is WRT EN. When WRT EN is OFF, IC9E inverts it to a LOW which disables IC20B and CLEARS F/F's 21A and 21B. When WRT EN is ON IC9E inverts it to a HIGH enabling IC20B. The output of IC20B triggers F/F21A which will output a 3.2 MHz signal. The 'Q' output of F/F21A hs two signal paths. The first path inputs one leg of IC22A and the second path inputs one leg of IC22D. The 'Q' output of F/F21A also has two paths. It feeds the 'D' input of itself and supplies the clock for F/F21B. F/F21B outputs a 1.55 MHz signal. The 'Q' output of F/F21B has three signal paths. The first is to the 'D' input of itself, the second is to one leg of IC22C and the third

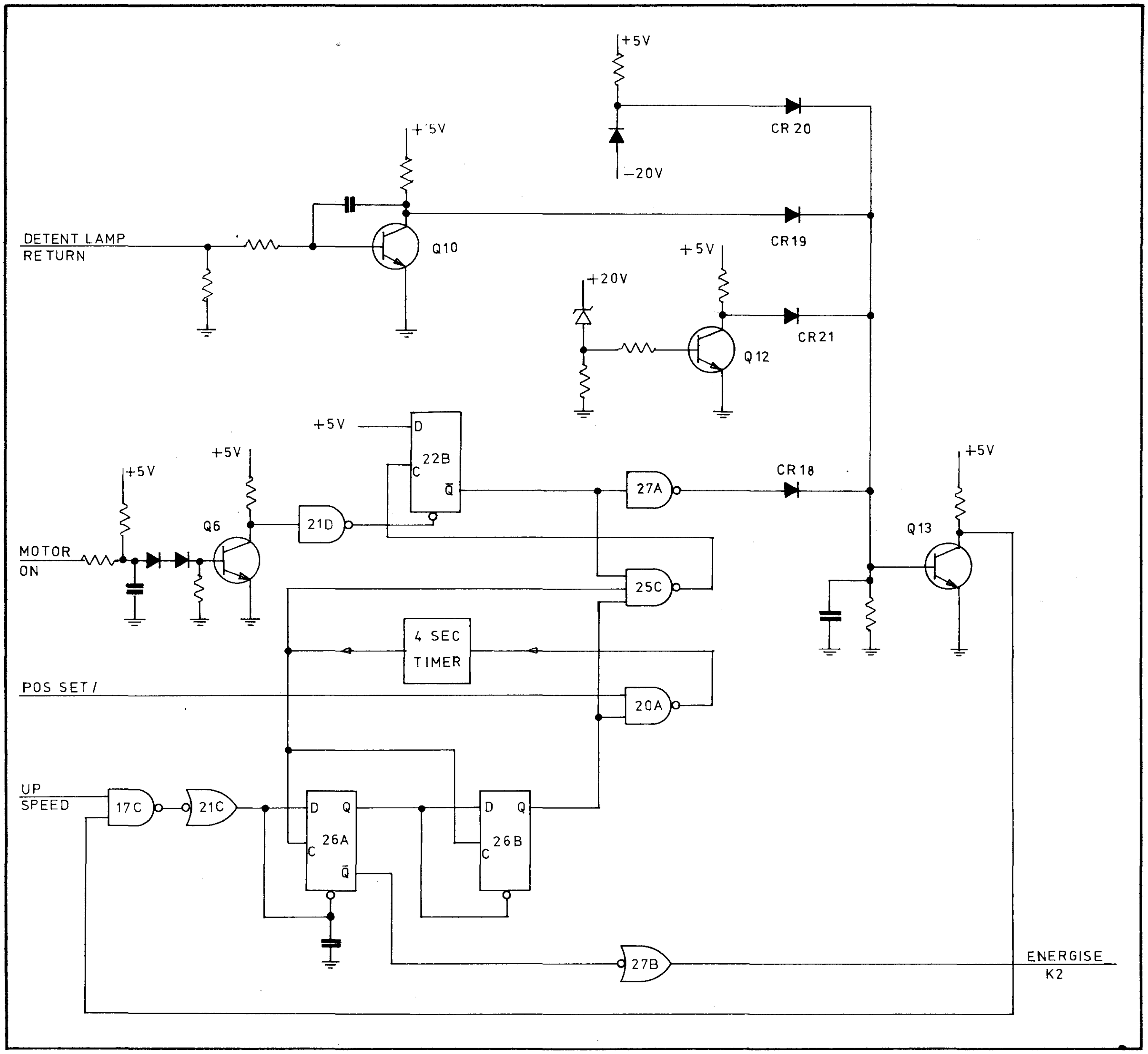

Figure 2-15. Failure Detection Circuitry.

is to the other leg of IC22D. IC22D inputs to IC22C, of which the other input is RD CLK (-) (read clock). Since RD CLK is HIGH at this time the combination of IC22D and IC22C will act as an AND gate, outputting a HIGH when both inputs are HIGH.

One input leg is a 3.1 MHz signal and the other input is a 1.55 MHz signal. The output will be the HIGH portion of the 3.1 MHz signal at a 1.55 MHz frequency. This signal will then go through IC10 to transistor Q10 where it is sent to the controller as DATA CLK (data clock) to strobe WRT DATA back to the unit.

WRT DATA enters the unit and is inverted by IC9B, then inverted by IC20D to input one leg of IC20C. IC20C is a NOR gate which combines WRT DATA with the 1.55 MHz signal from IC21B. If WRT DATA input is a ONE, then IC20C will output a HIGH. If WRT DATA input is a ZERO then IC20C will output a 1.55 MHz pulse. IC20C feeds one leg of IC22A, which in turn, feeds IC22B. The combination of IC22A and IC22B will act like an AND gate. The other input to IC22A is a 3.1 MHz pulse from F/F21A. If IC20C outputs a data ONE (HIGH) then IC22B will output two pulses at 3.1

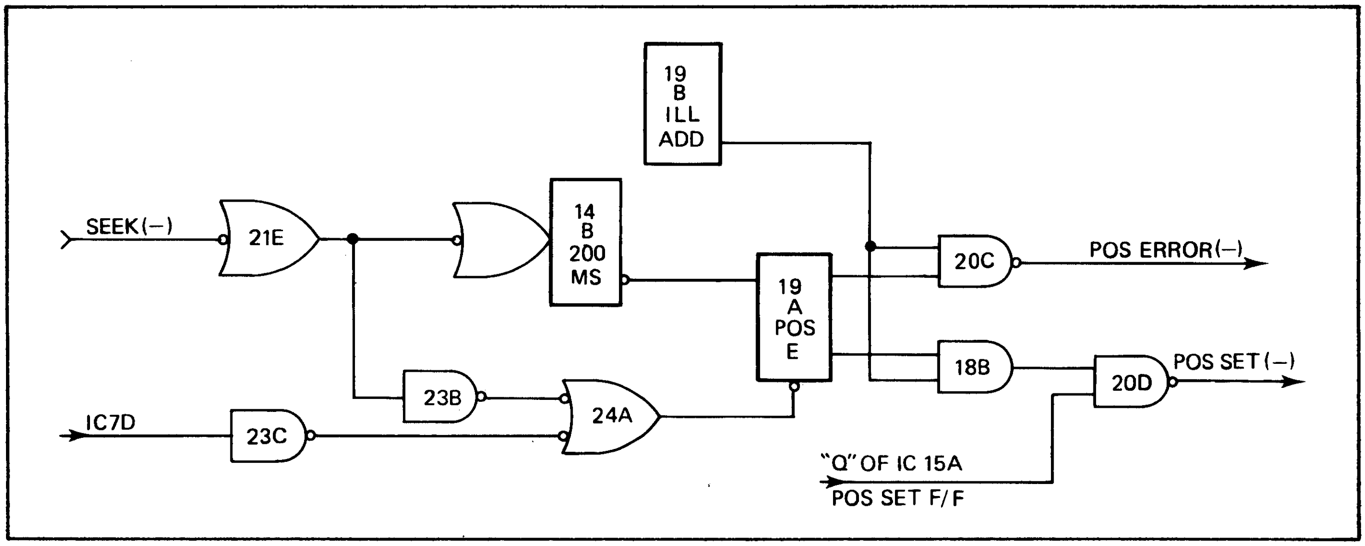

Figure 2-16. Position Error Detection.

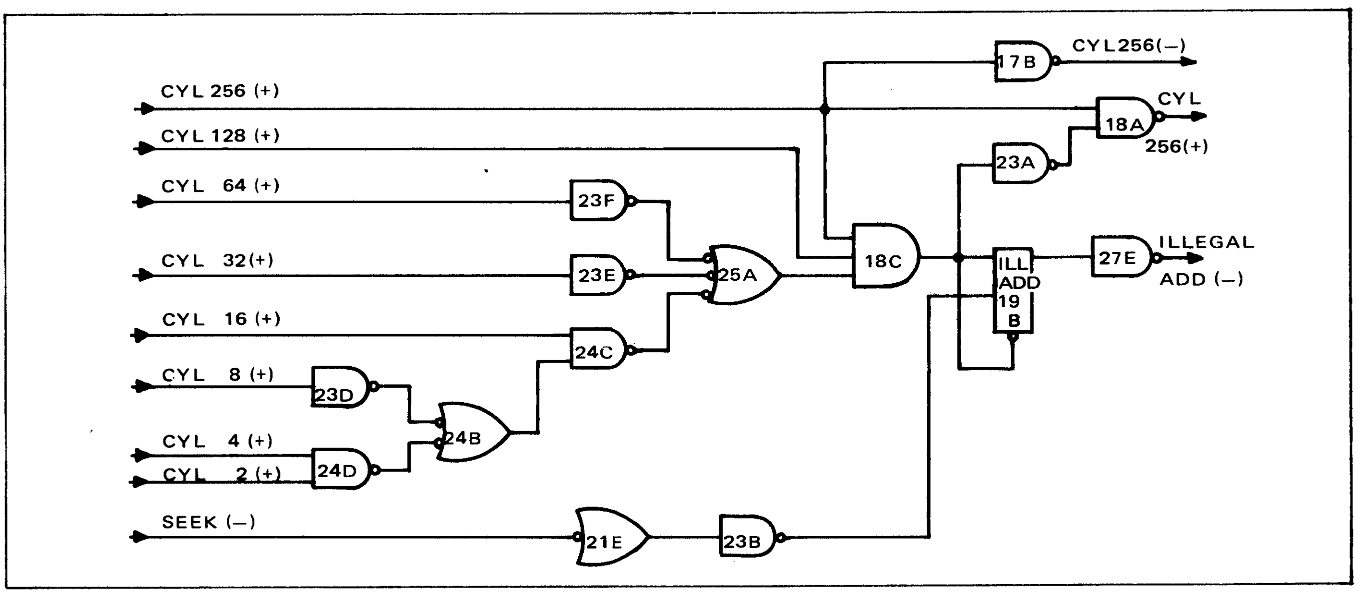

Figure 2-17. Illegal Address Detection (9481-12)

MHz. If IC20C outputs a data ZERO (1.55 MHz pulse) then IC22B will output one 3.1 MHz pulse. This output will feed IC17A and IC17B to be gated by UNIT SEL (unit select) to go to the selected Drive Module's Read/Write Amplifier to be written on the cartridge.

WRITE AMPLIFIER AND DRIVERS

Refer to figure 2-19 part of RWA board.

Writing is controlled by the signals HEAD SEL, WRT DATA, WRT EN and TERMINAL WIH.

HEAD SEL will enable head 0 center tap if LOW or head 1 center tap if HIGH. WRITE EN will turn on transistor Q9 if TERMINAL WIH is high. If TERMINAL WIH is LOW, then the drive is write locked out, and no current can be supplied to the write drivers.

With transistor Q9 turned on the Write current source transistor Q8 turns on and transistors Q10 and Q11 turn on and enable erase current source transistor Q5.

Q8 enables the write driver transistors Q3 and Q4. Current can now be driven through the read/write coils in response to the WRT DATA bit pattern. At the same time, Q5 drives current through the erase coil to clip the data just recorded.

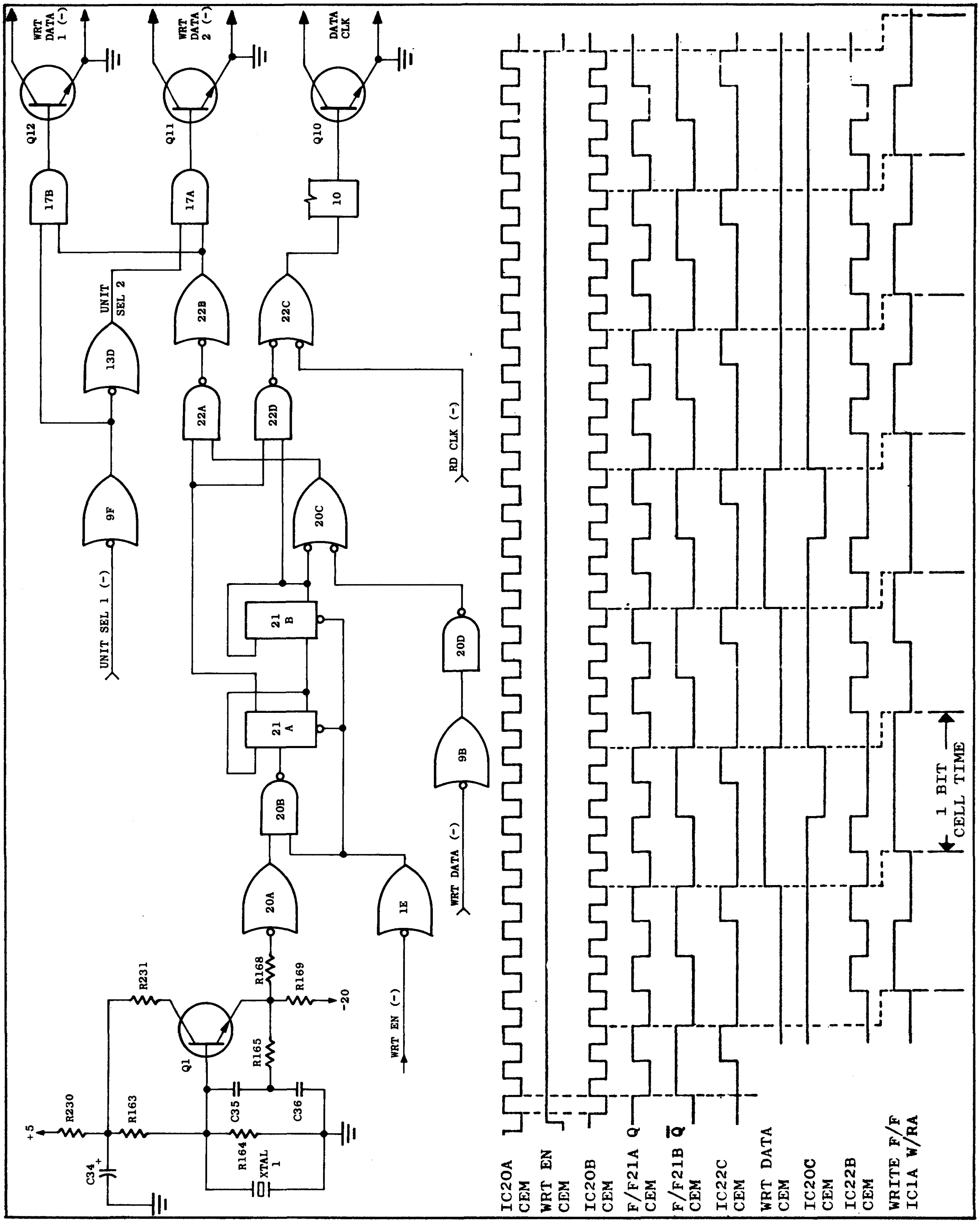

Figure 2-18. Write Data Encoder Part of CEM

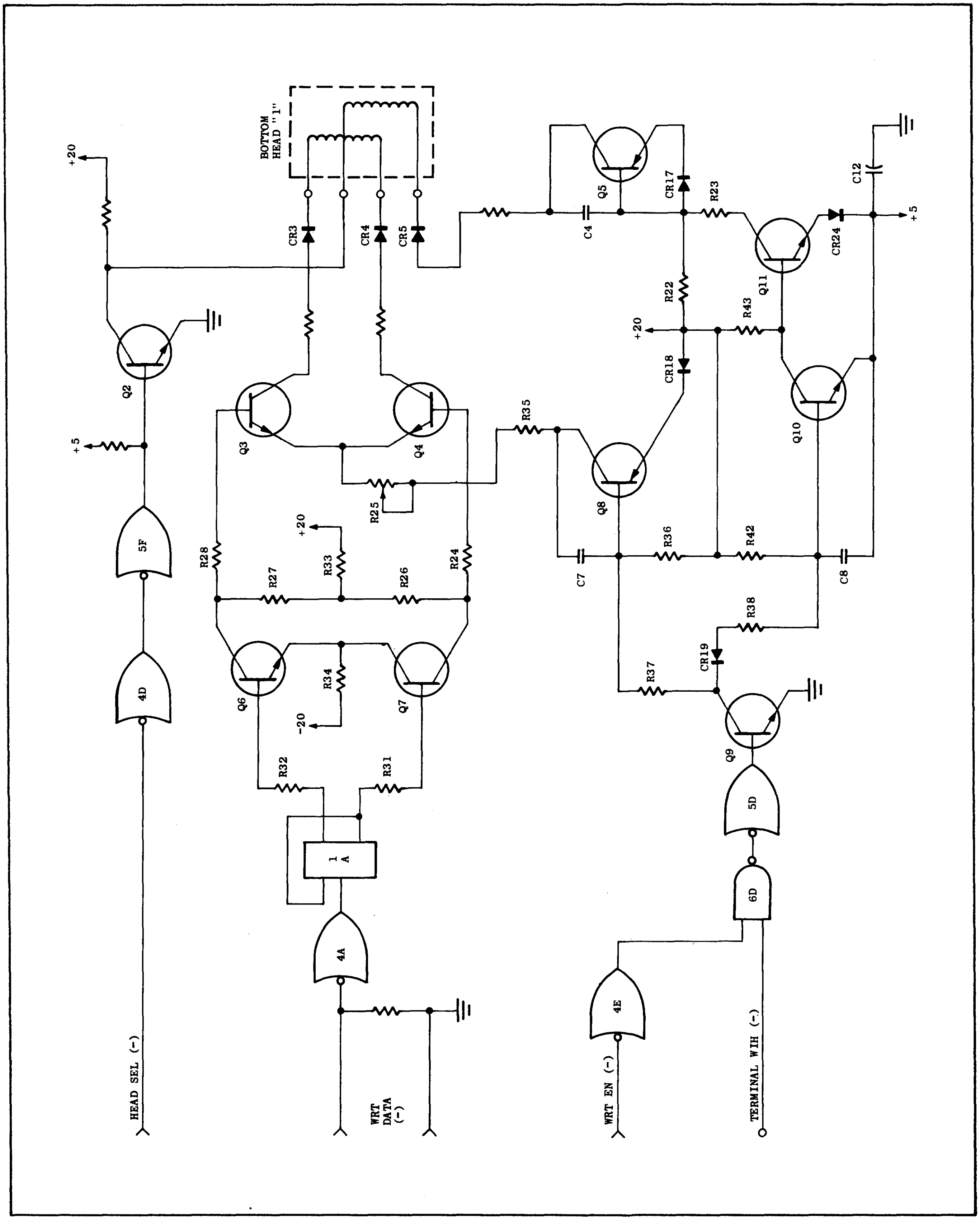

Figure 2-19. Write Amplifiers and Drivers.

READ OPERATION

The read circuitry is contained partly on the RWA board and partly on the CEM board.

HEAD CIRCUITS

Refer to figure 2-20, part of RWA board.

The Flux Lines emanating from the disk surface will induce a current in the Read/Write Head windings. This induced current passes through isolation transformer T1 and is applied to preamplifier IC8. The output of IC8 is fed to Line Driver transistor Q17 and Q18. When the Line Driver is enabled by UNIT SEL from the CEM via IC5C and transistors Q20 and Q19, the read signals are sent to the CEM as a HLA (High Level Analog) signal.

HEAD SIGNAL DISCRIMINATOR

Refer to figure 2-21.

The purpose of this circuit is to accept the HLA signals from the RWA board, and output a properly shaped digital signal for processing by the data discriminator.

HLA signals enter the differential amplifier of Q2 and Q3, which have a delay line connected across the outputs. This has the effect of changing the timing such that the digitized signal emerging from IC1A has a zero-crossing corresponding to each peak of the original HLA signal. Gates IC1B, IC2A and IC2B speed up the switching times of the digital signal, which is then differentiated by capacitors C45 and C46. ECL-to-TTL gate IC3 NOR's together the differentiated signals, and outputs a standard width pulse for each zero crossing of the delayed analog signal at transistors Q2/Q3 collectors. The output of IC3 therefore corresponds to a pulse each bit cell time plus an additional pulse in the center of any bit cells containing a "1".

DATA DISCRIMINATOR

Refer to figure 2-22, part of CEM board.

This consists of a Voltage Controlled Oscillator (VCO), a Phase Comparator, and a strobing and decoding network.

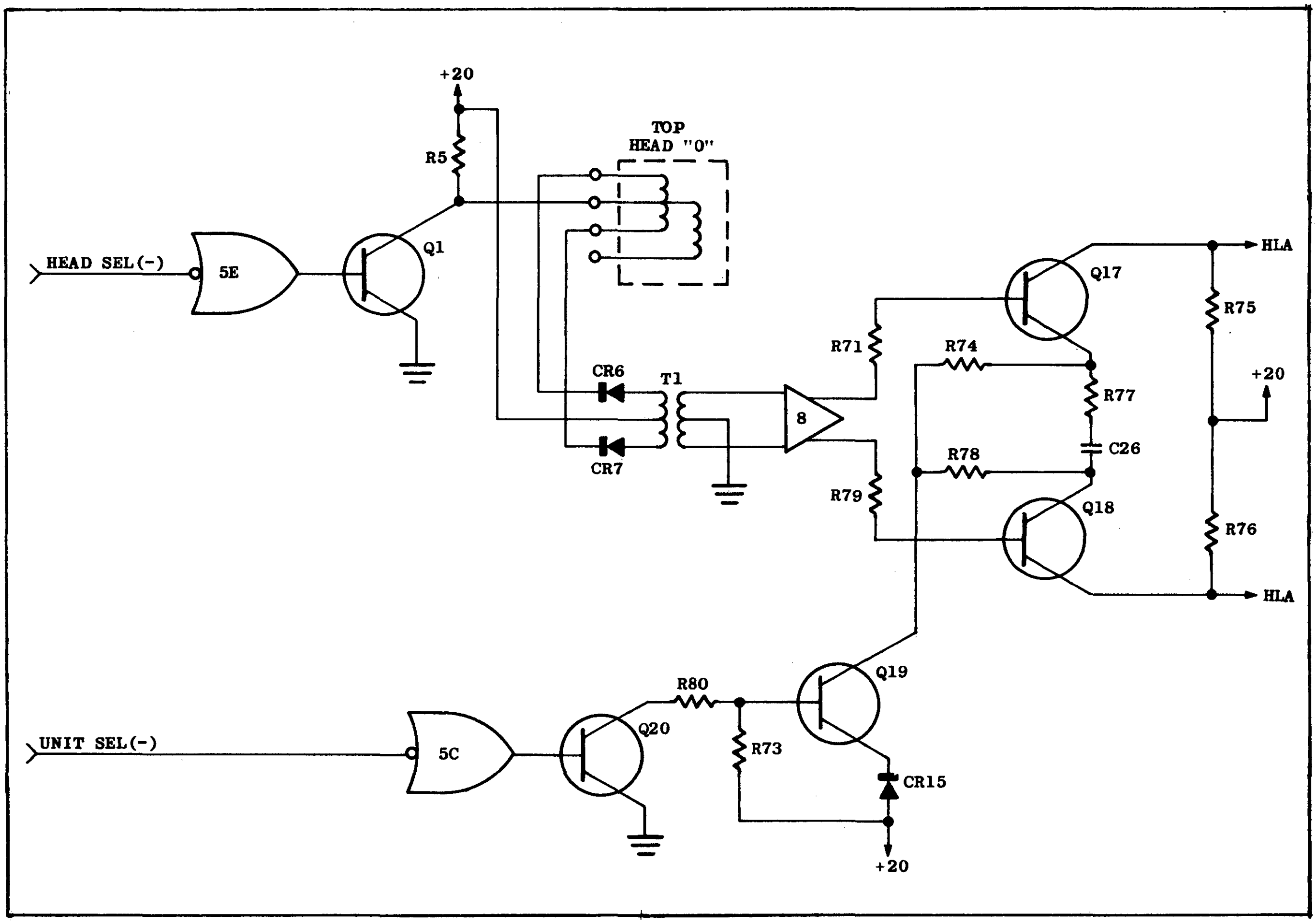

Figure 2-20. Read Part of R/WA

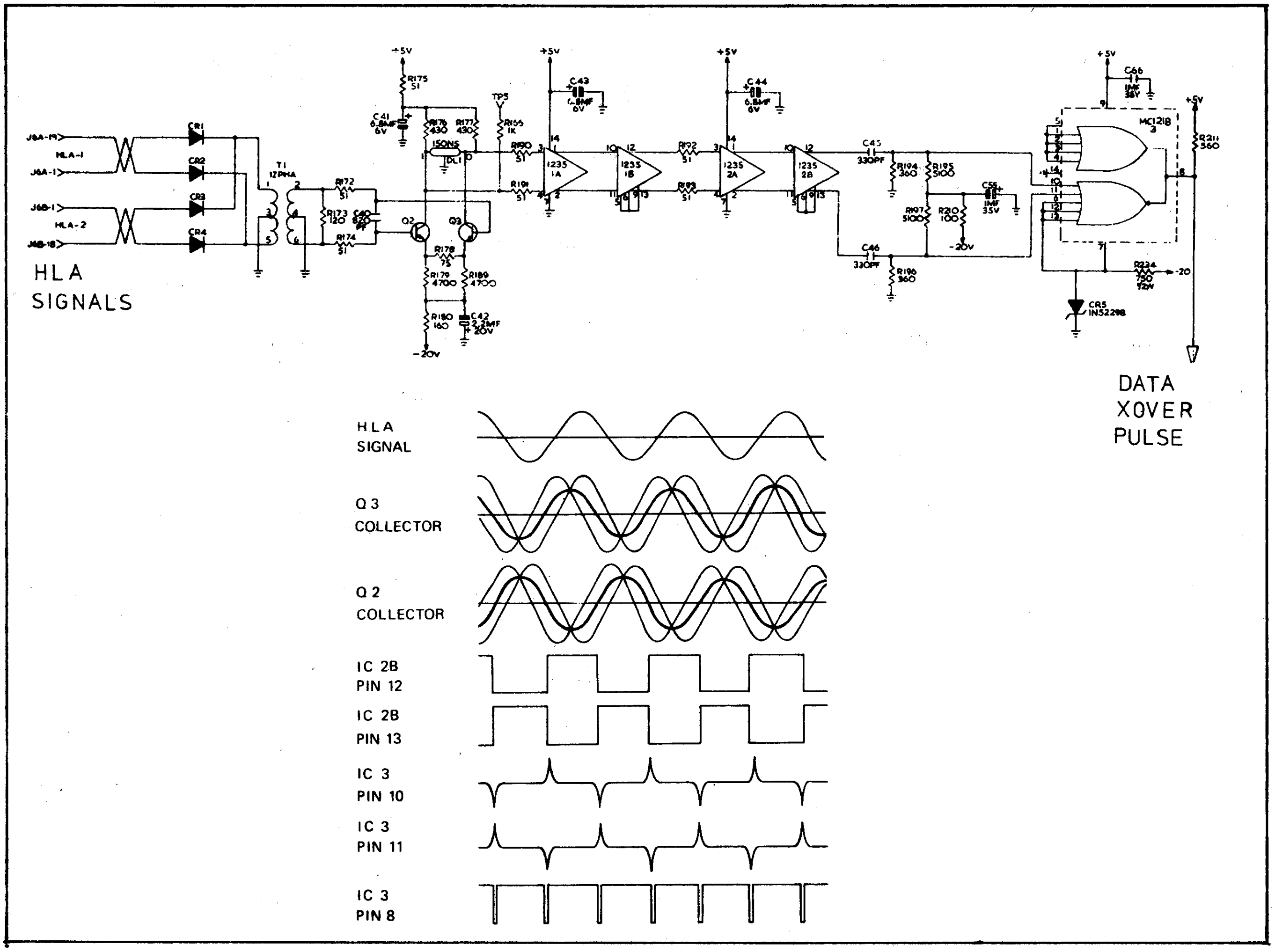

Figure 2-21. Head Signal Discriminator (Part of CEM Board)

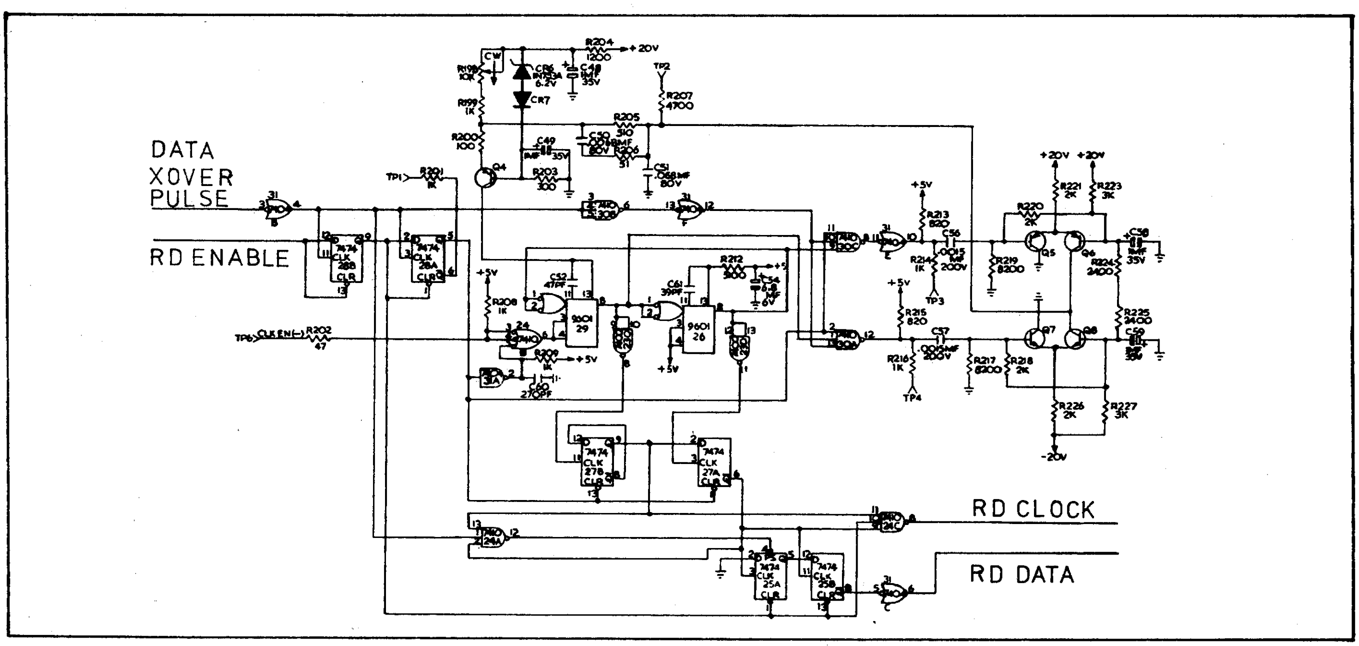

Figure 2-22. Data Discriminator and Phase Locked Loop (Part of CEM Board)

Phase-Locked Loop (PLL)

The VCO and Phase Comparator form a phase-locked loop. The purpose of this is to synchronize the read clock (VCO) to the incoming data frequency.

The VCO consists of 2 monostable multivibrators, IC26 and IC29 which oscillate at a basic frequency of 3.1 MHz. A fine adjustment is effected by altering the charging current through transistor Q4.

The phase comparator consists of transistors Q5, Q6, Q7, Q8, IC30A, IC30C and IC31E. The output of this circuit is an error voltage (T.P.2) which is used to alter the current flowing in transistor Q4 to control the VCO frequency.

Detailed circuit operation of the PLL is illustrated in figures 2-21, 2-23, 2-24 and 2-25.

IC28A and IC28B synchronize the second data pulse from IC31B to the very first clock pulse when RD ENABLE goes HIGH. The 'Q' output of IC28A clears monostable multivibrator IC29 and IC29 inputs a LOW to IC26, which sets for the period defined by its R-C network.

When IC26 times out, its 'Q' output goes low, and sets IC29 for the period defined by the R-C network around transistor Q4. This is, in turn, controlled by the error voltage fed back from the phase comparator.

When IC29 times out, the process repeats itself. IC29 and IC26 therefore oscillate to provide a 3.1 MHz read clock, which can be fine adjusted by the output from the phase comparator. IC30A, IC30C and IC31E NAND the data and clocks and output a stream of pulses. The pulses are integrated by capacitors C56 and C57, and combined together by transistors Q5, Q6, Q7 and Q8 to develop the error voltage used to control the VCO.

The PLL may be thought of as operating in 3 different modes:

Data frequency = VCO frequency

The pulses emerging from capacitors C56 and C57 are of equal width and amplitude, and there is no error voltage input to transistor Q4.

Data frequency > VCO frequency (disk rotating faster)

The pulses from capacitor C56 will be of greater width and amplitude than those at capacitor C57. The error voltage input to transistor Q4 will be more positive, and IC29/IC26 oscillate at a higher frequency.

Data frequency < VCO frequency (disk rotating slower)

The pulses from capacitor C56 will be of lesser width and amplitude than these at capacitor C57. The error voltage input to transistor Q4 will be

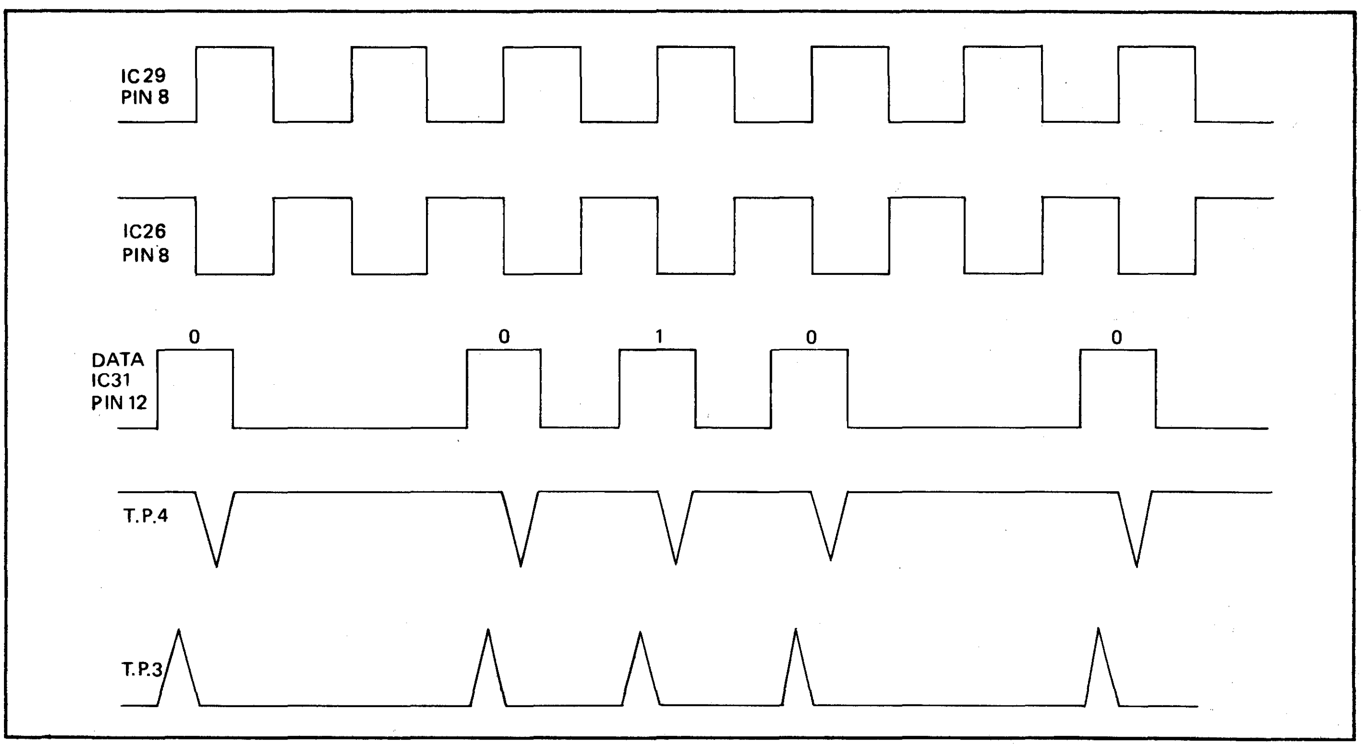

Figure 2-23. Phase-Locked Loop Timing Chart Data And Clocks Synchronized

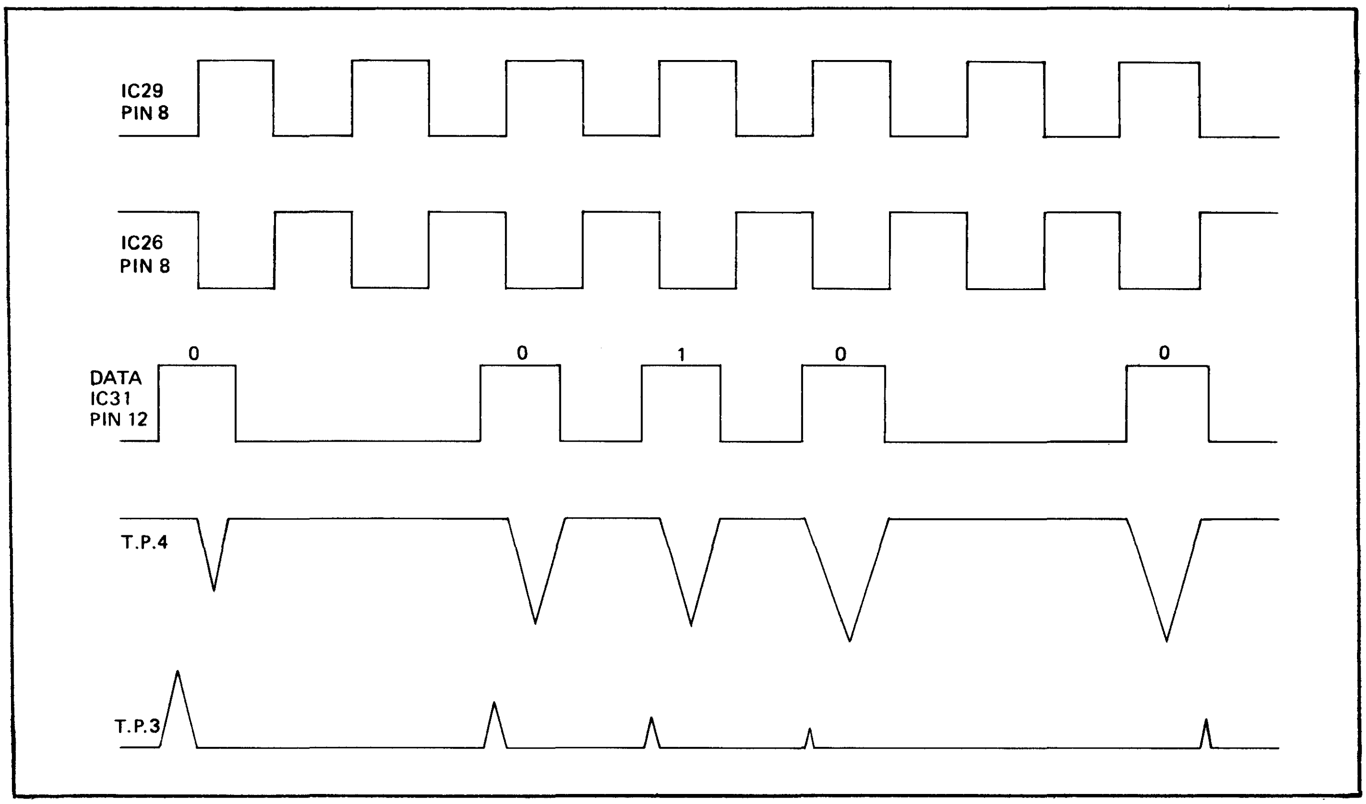

Figure 2-24. Phase-Locked Loop Timing Chart Data Frequency Too Low (Disk Rotating Slower)

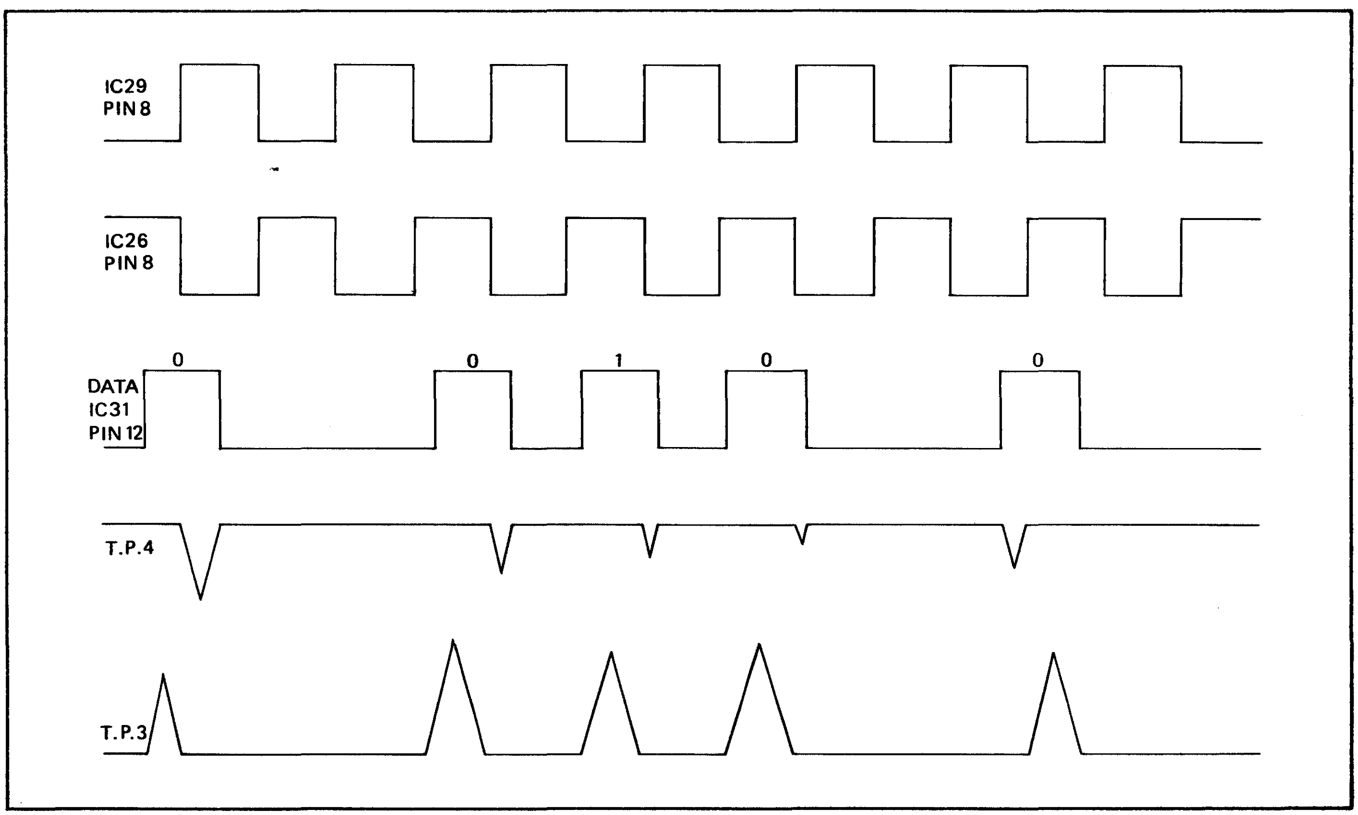

Figure 2-25. Phase-Locked Loop Timing Chart Data Frequency Too High (Disk Rotating Faster)

more negative, and IC29/IC26 oscillate at lower frequency.

Figures 2-23, 2-24 and 2-25 illustrate the preceeding examples.

STROBING AND DECODING

Refer to figures 2-26 and 2-27.

The 2 phases output from the VCO enter flip-flops IC27A and IC27B. These have the effect of dividing the basic clock frequency by 2. The output is overlapping signals at 1.55 MHz.

The purpose of these two signals is to generate a data 'window', from which RD CLOCK is directly derived by IC24C for transmission to the I/O interface.

At the same time, IC24A will be enabled for the window period, and 'looks' for a data '1' bit occurring in the window. The combined action of IC27A, IC24A and IC25A decodes DFM data into NRZ data, as follows:

If a '0' bit is found in the window, there will be no output from IC24A. IC27A clock therefore resets IC25A.

If a '1' bit is found in the window, IC24A will direct set IC25A, which remains set until the next clock pulse from IC27A.

IC25B changes the timing, such that it can only set or reset for 1 complete period of IC27A clock (1 bit cell time).
Therefore, RD DATA will be high or low for 1 bit cell time, according to whether a '1' or a '0' occurred in the data window. The data has now been decoded to NRZ.

The timing is such that the trailing edge of RD CLOCK occurs in the middle of a bit cell. This enables proper strobing of the NRZ data by the host system. (See figure 2-27).

MISCELLANEOUS FUNCTIONS

SECTOR AND INDEX

Refer to figure 2-28, part of RWA board).

The Index/Sector Circuit amplifies and shapes the pulses transmitted from the Optical Sector Transducer, and monitors the rotational speed of the disk. The signal from the Optical Sector Transducer is amplified by IC7 then sent through the Peak Detector, consisting of transistor Q12 through Q16. This converts the signal to TTL level to feed IC2A Delay, providing index alignment and adjustment. The signal is then shaped by IC3A and on to the circuit of IC3B, IC6B and IC6C which discriminates between Index and Sector pulses. Both Index and Sector pulses go to the CEM. IC2B is a speed detector fired

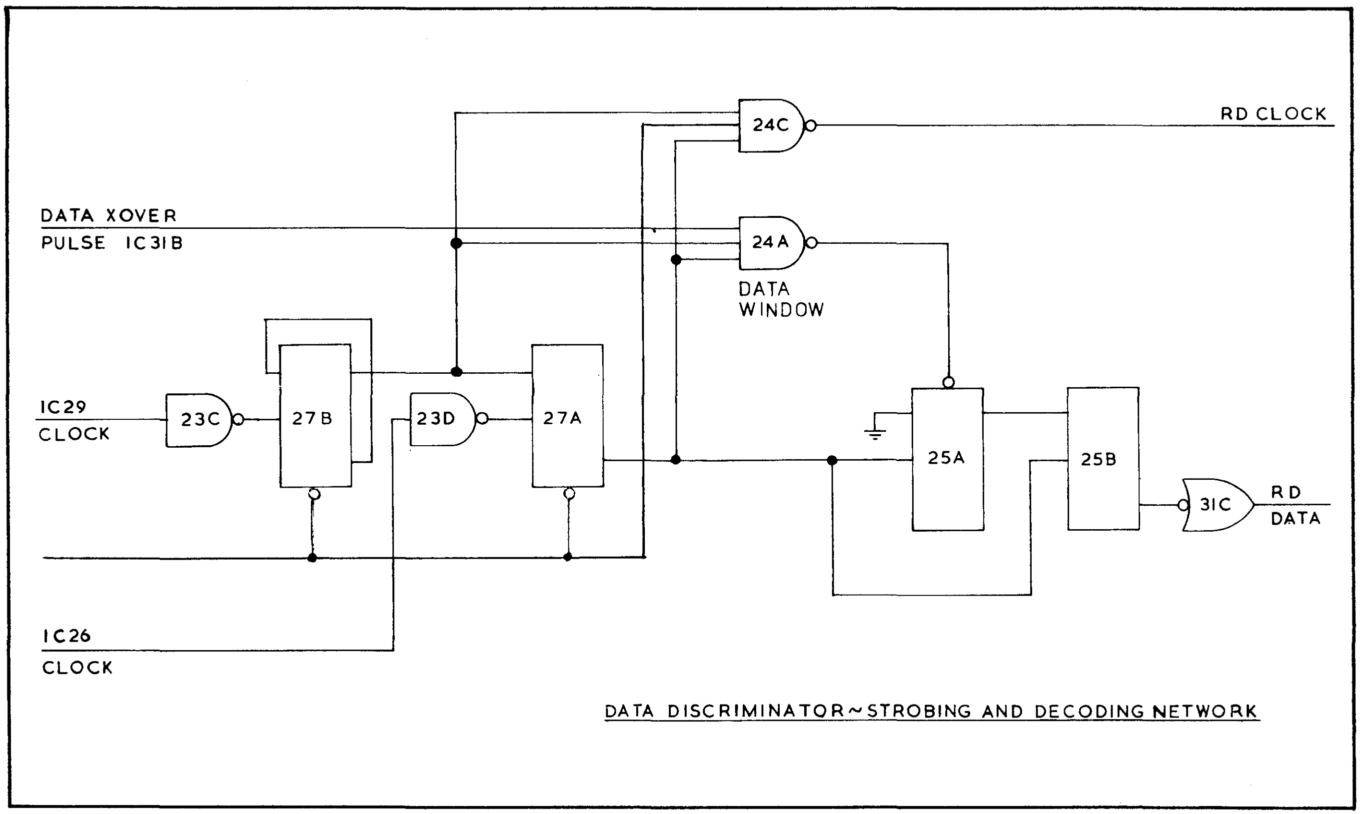

Figure 2-26. Data Discriminator Strobing And Decoding Network

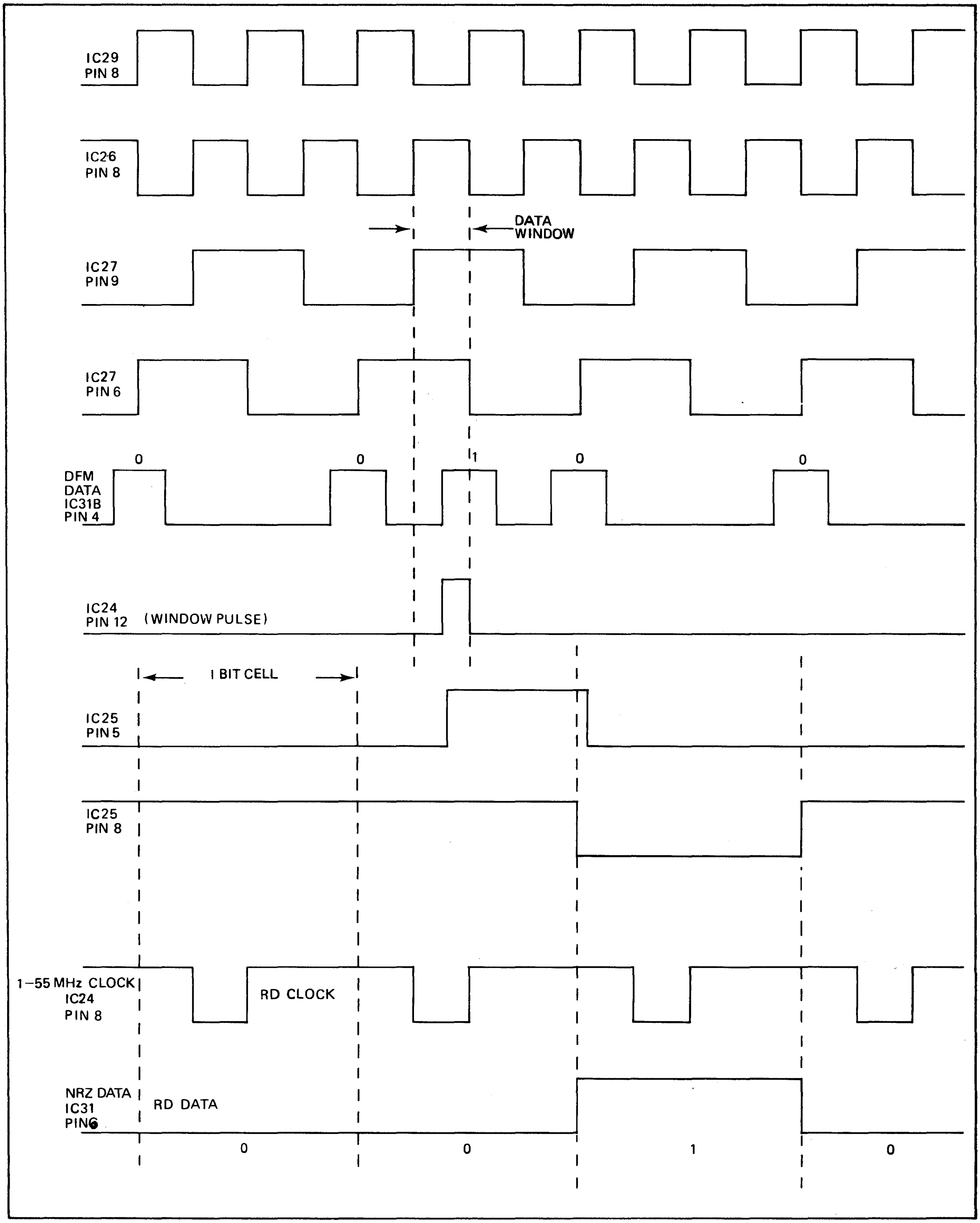

Figure 2-27. Data Discriminator. Window (Strobing) Timing And Decoding

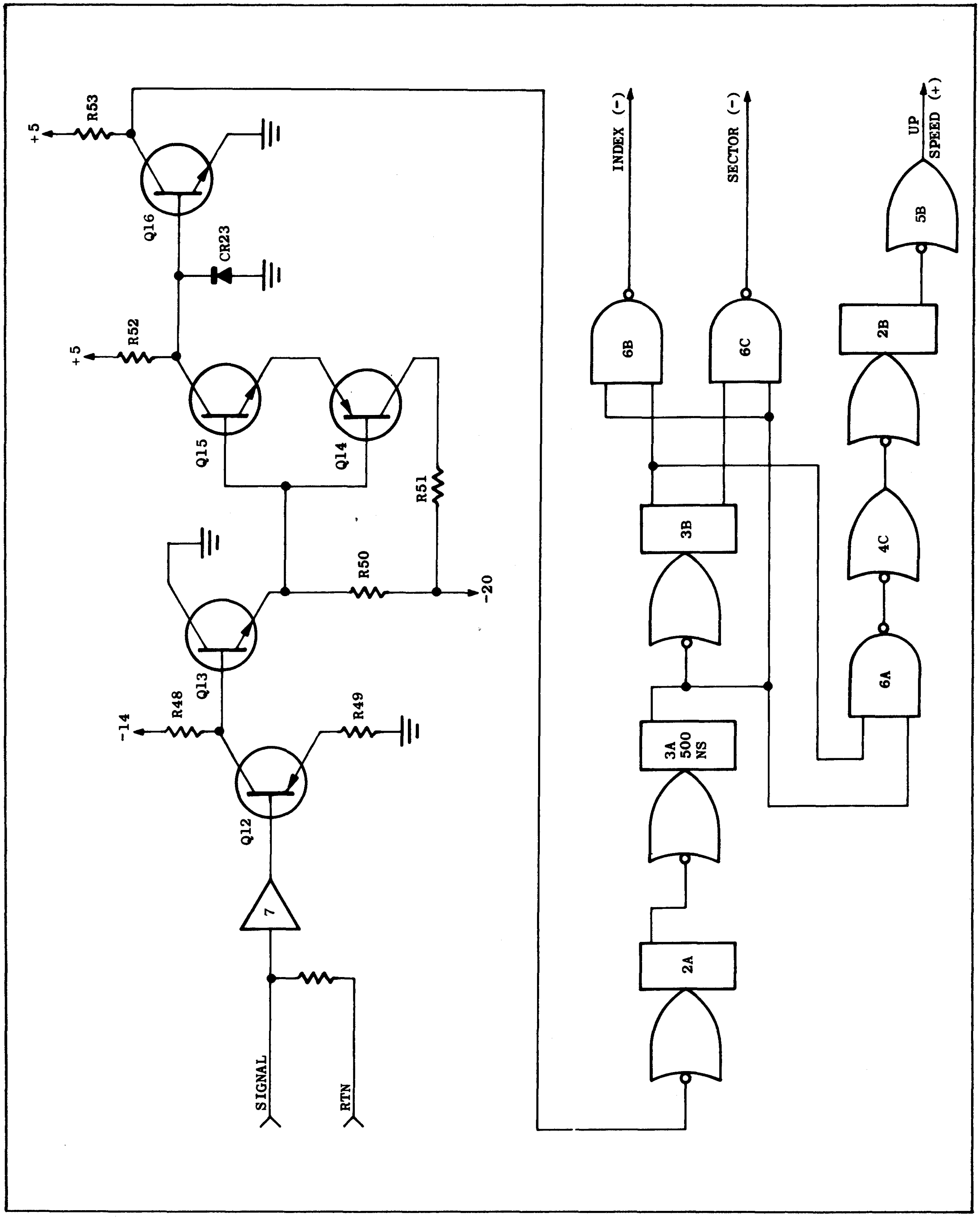

Figure 2-28. INDEX and SECTOR Circuits

by the index pulse through IC6A and IC4C. This is sent through IC5B to the SCM as UP SPEED providing Head Loading Initiate signals.

RECEIVER INTERLOCK

The receiver interlock circuitry was described in detail in the second part of this section. (See Positioning System, first seek and head retract logic).

TEMPERATURE COMPENSATION (9481-12 Only)

Refer to figure 2-29 Temperature Compensation board.

The D/A converter output voltage is buffered by a unity gain voltage follower U4. The output of this follower is applied to two OP amps, U1 and U2 which generate two voltages into the three thermistors RT1, RT2, RT3 and an adjustable reference point in two bridge circuits. Bridge circuit B1 (based on the relationship of the baseplate thermistor 1 to the reference pot) is differentiated and sends a voltage to the summing amplifier. Bridge circuit B2, (based on relationship of air thermistor 3 to baseplate thermistor 2) is also differentiated and sends a second voltage to the summing amplifier. The summing of these two voltages produces an output in the form of an offset voltage to the fine servo. This summing is a continuing function in the unit but is only triggered into use when detent enable signal is present and is not in use when in coarse servo mode.

The temperature compensation module provides its own voltage regulator which enables it to utilize existing voltages in the drive.

POWER SUPPLIES

Refer to figure 2-30.

Six dc supply voltages used in the drive are provided by a common power supply mounted in the cabinet base.

The +36V, −36V and +12V are unregulated and taken direct from the rectifiers and smoothing capacitors.

The +20V, −20V and +5V use integrated circuit regulators and power transistors. Operation of these circuits is similar and the following description is typical.

AC voltage from the output of the mains transformer T1 is rectified and smoothed. The unregulated D.C. voltage is applied through 2 power transistors operating in emitter follower mode with the base control voltage being provided from the output of a 723 voltage regulator chip (see integrated circuit descriptions at the beginning of this section).

The electronic components are mounted on the Power Supply board, and in the case of the +5V logic supply, this also includes an over-voltage crowbar, SCR-1. If the +5V becomes too high, SCR1 will fire, shorting the +5V supply bus to ground, which blows fuse F5. This provides protection to the logic chips in the event of regulator failure.

The battery charge is maintained by dropping the +20V through R12 and CR2.

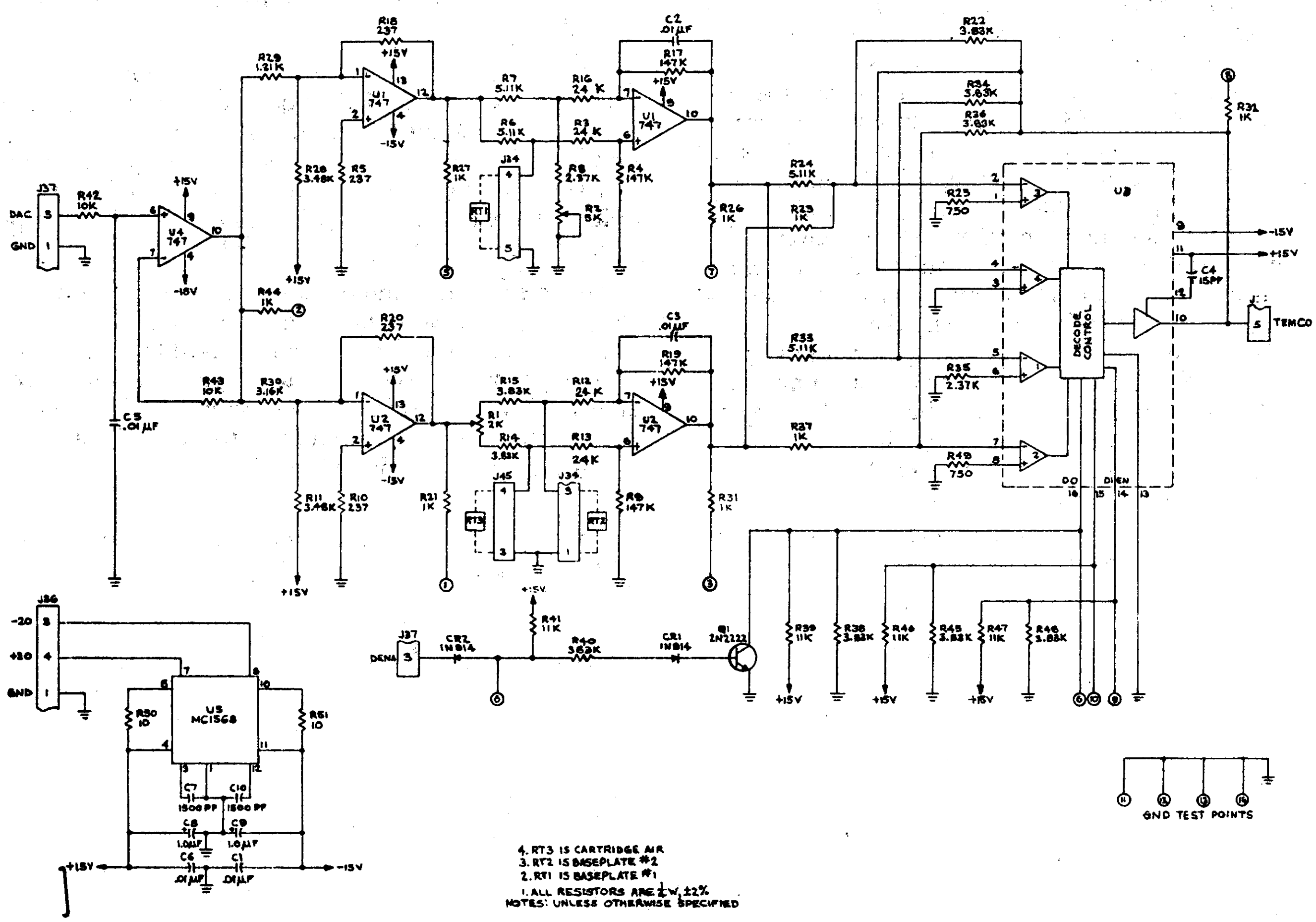

Figure 2-29. Temperature Compensation Board (9481-12 only)

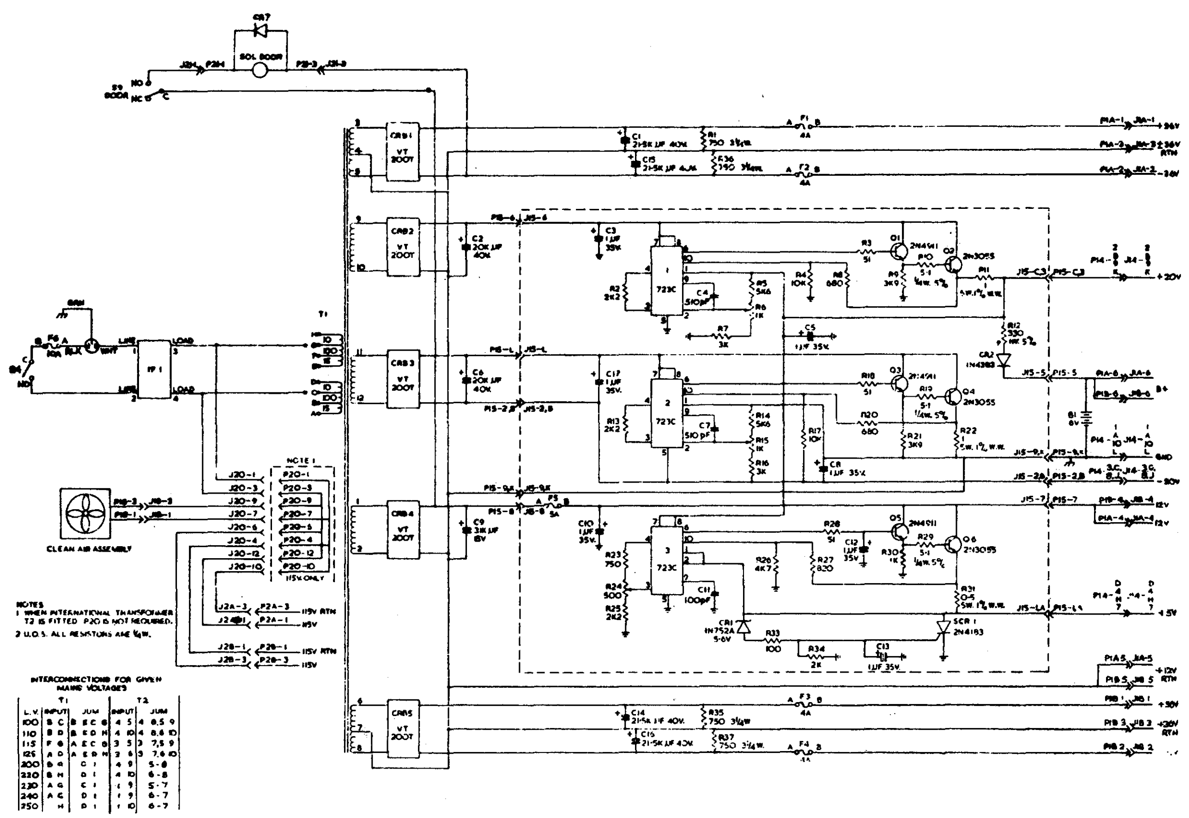

Figure 2-30. Power Supplies.

SECTION 3
BOARD SCHEMATICS

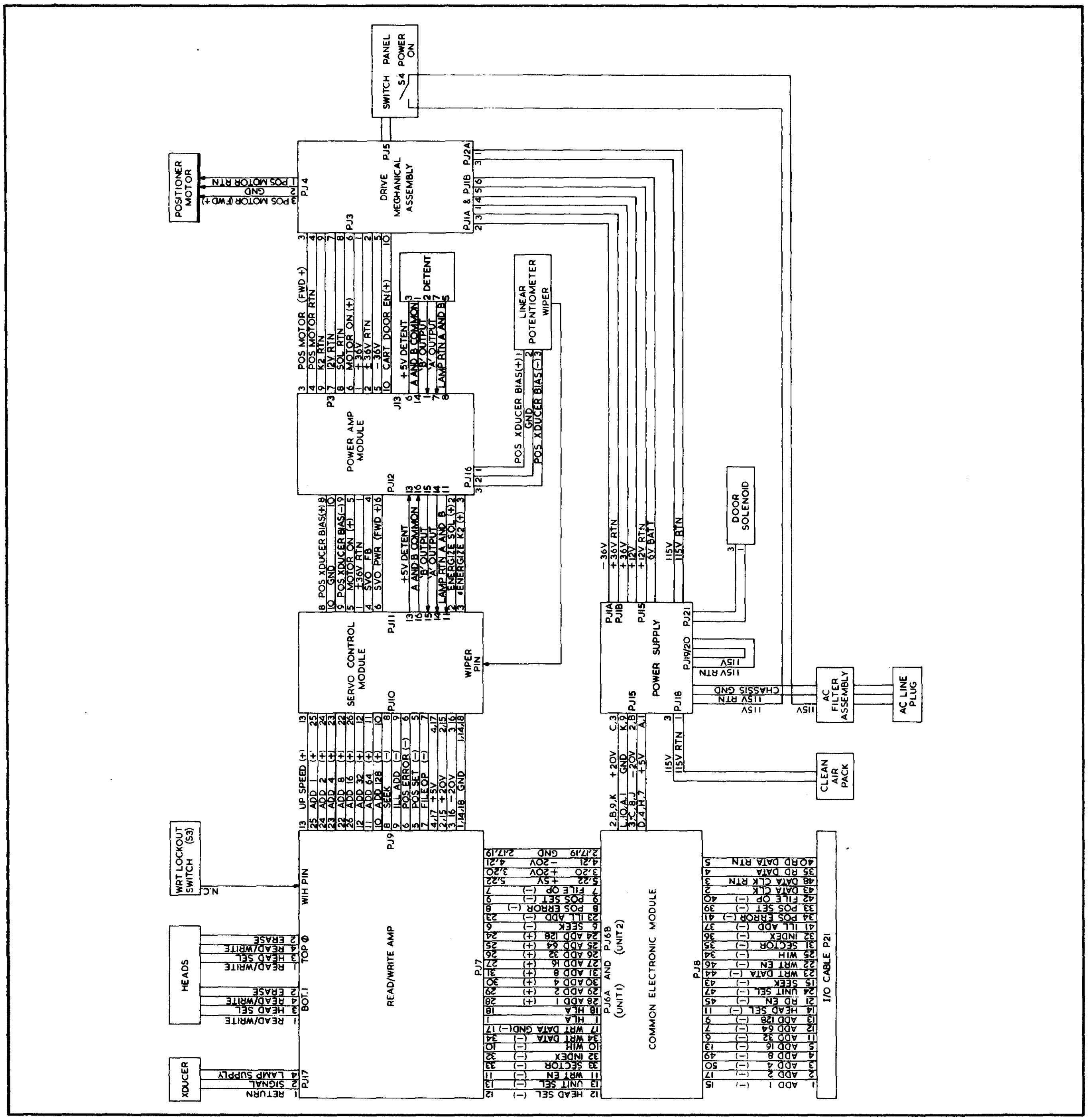

Figure 3-1. 9480-12 System Block Diagram

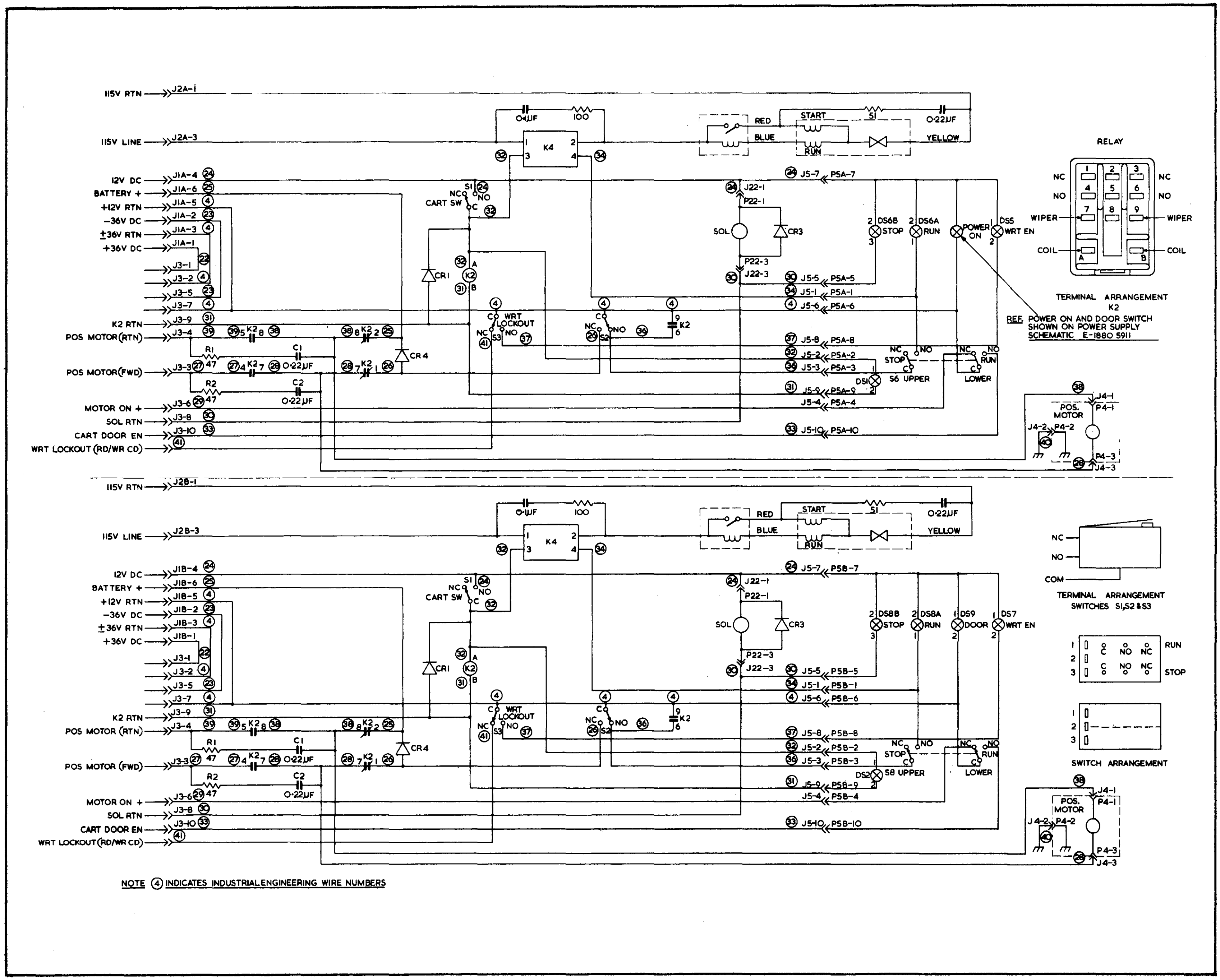

Figure 3-2. 9480-12 Main Drive Harness

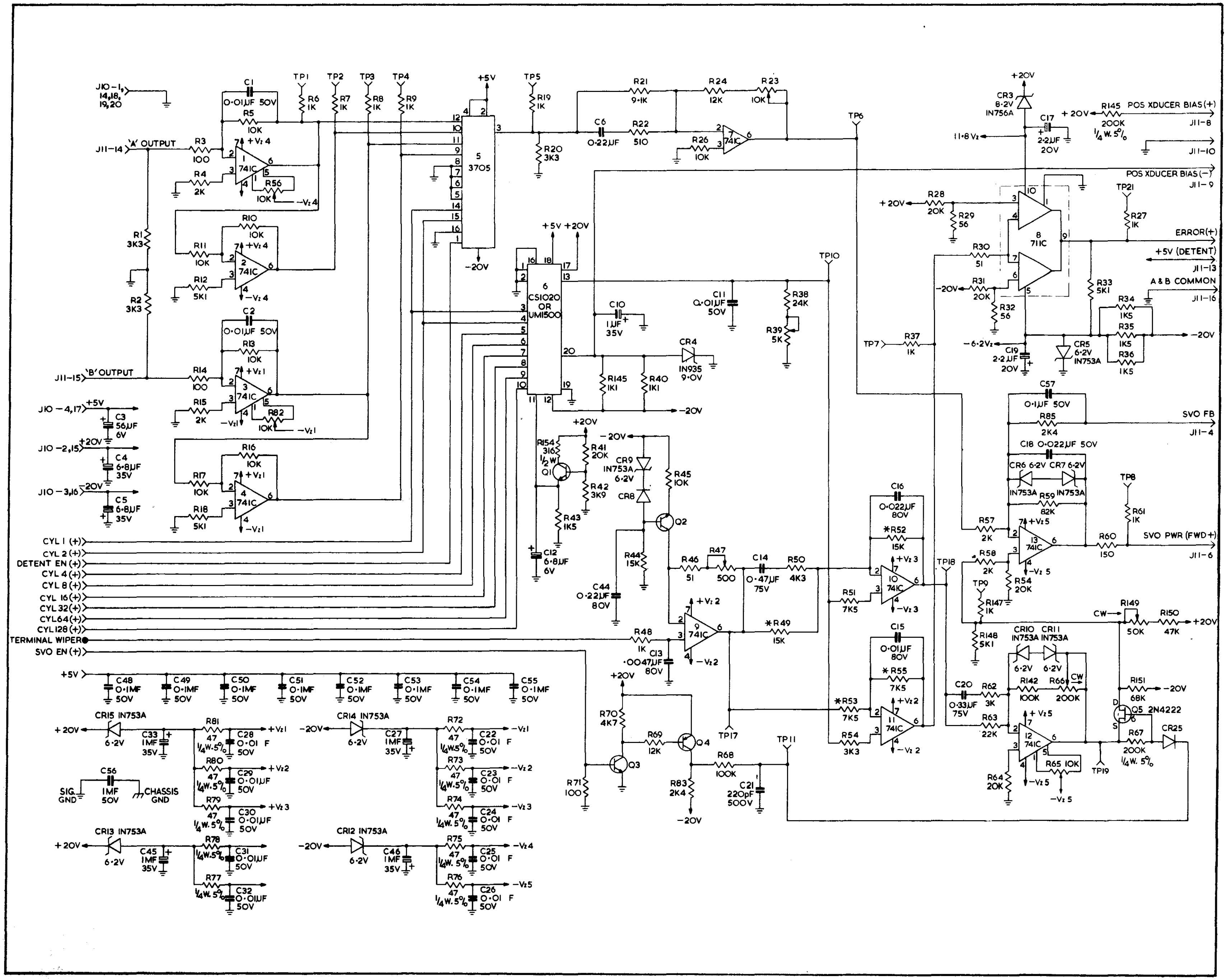

Figure 3-3. 9480-12 SCM Board, Sheet 1

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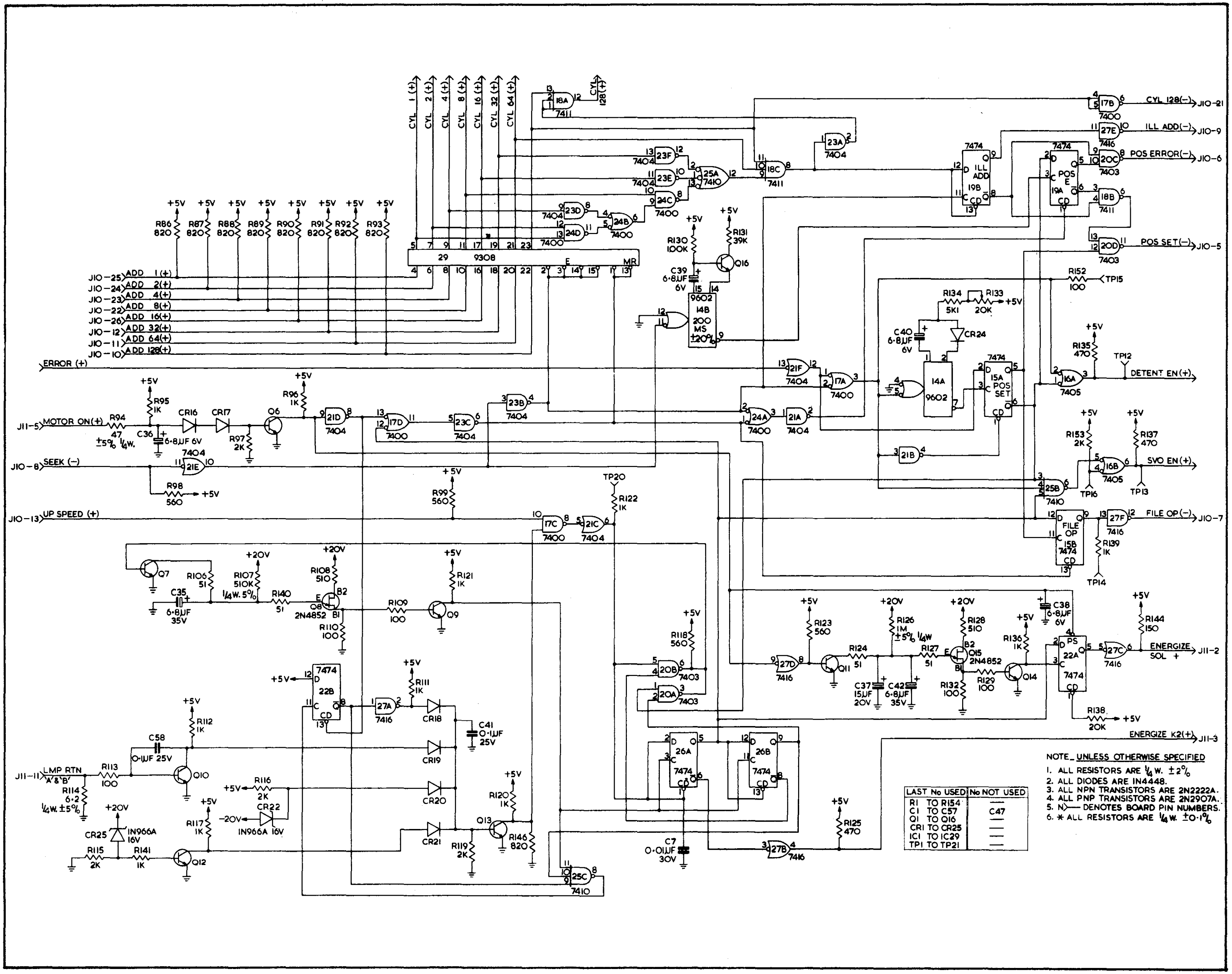


Figure 3-4. 9480-12 SCM Board, Sheet 2

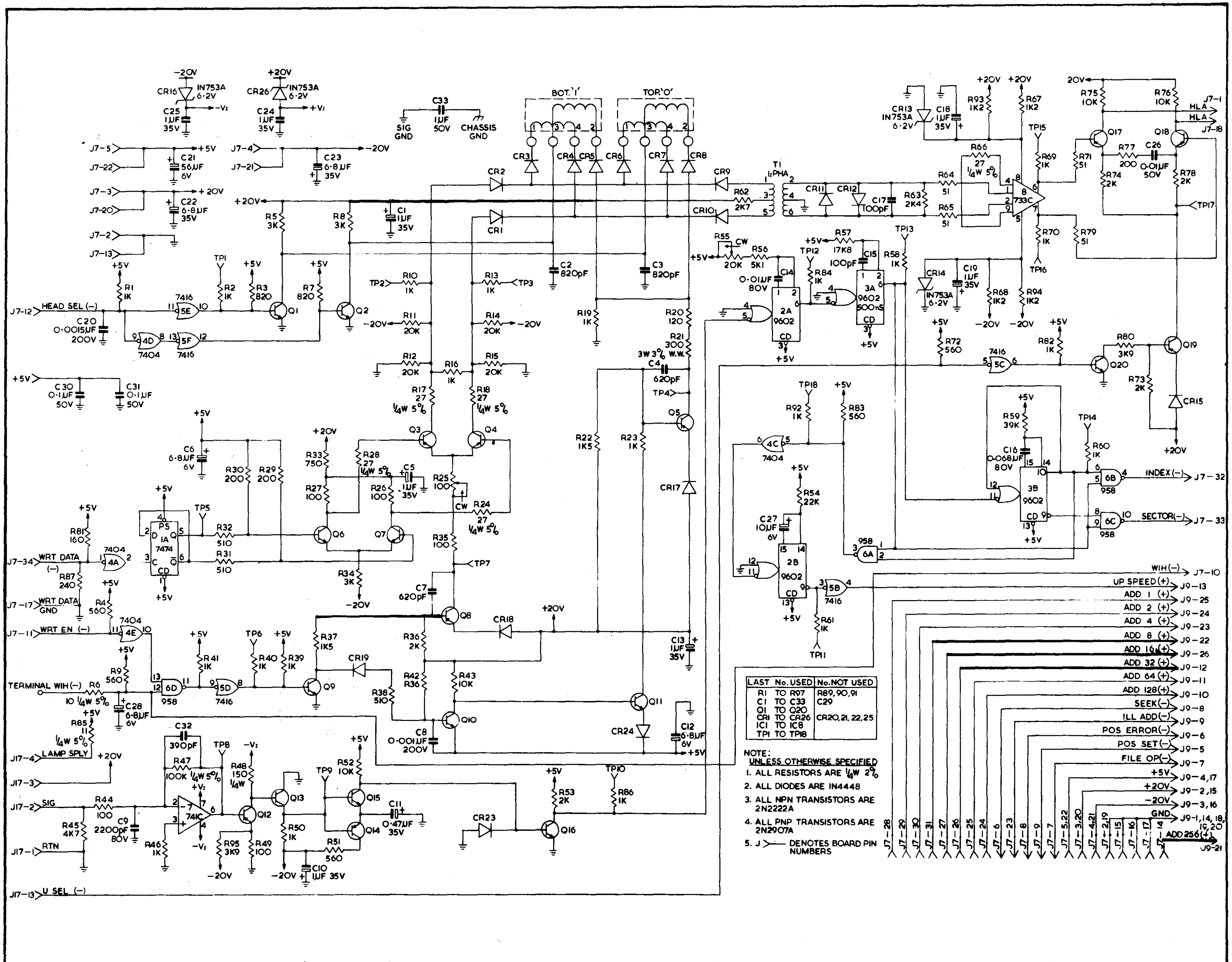


Figure 3-5. 9480-12 RWA Board

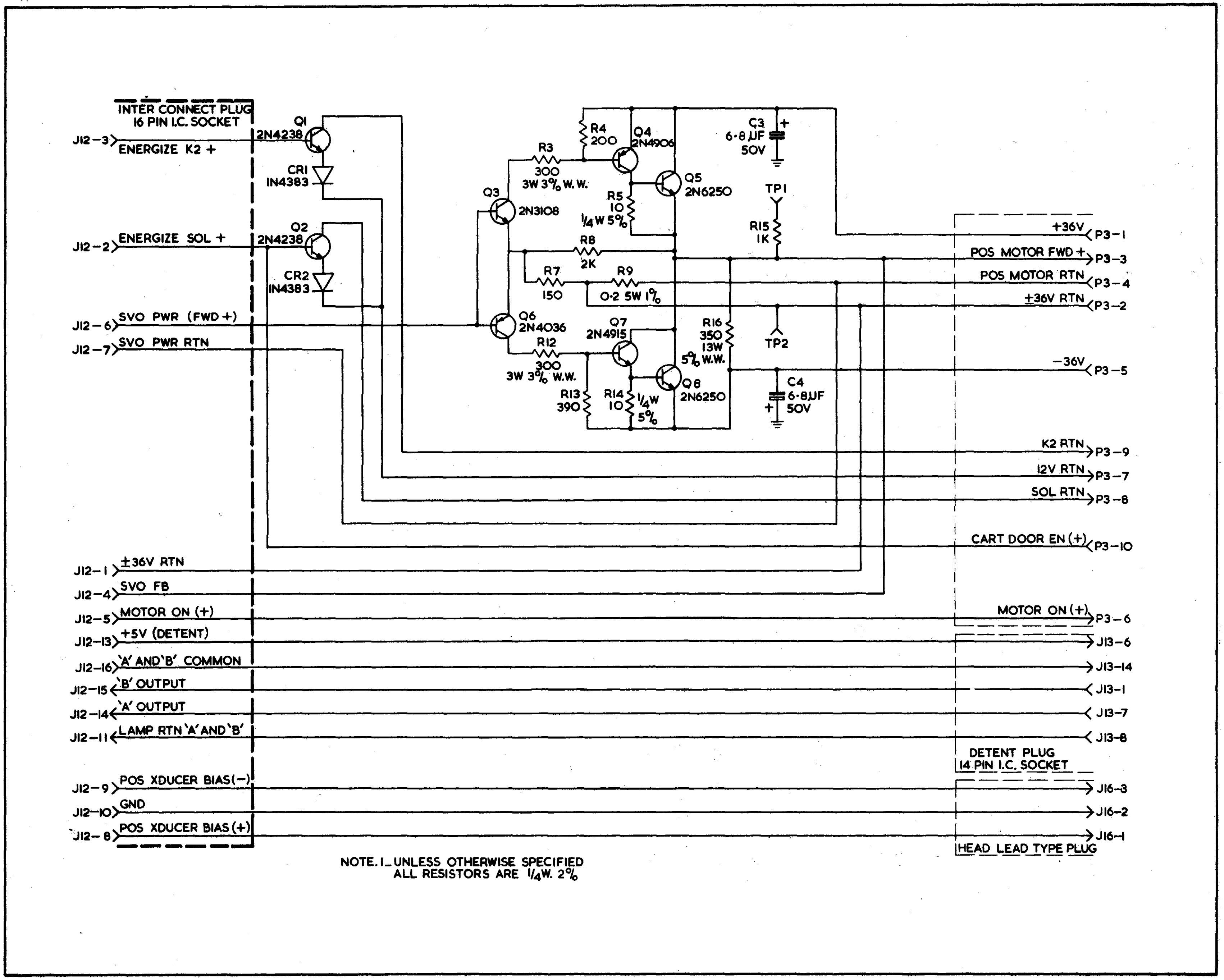


Figure 3-6. 9480-12 PAM Board

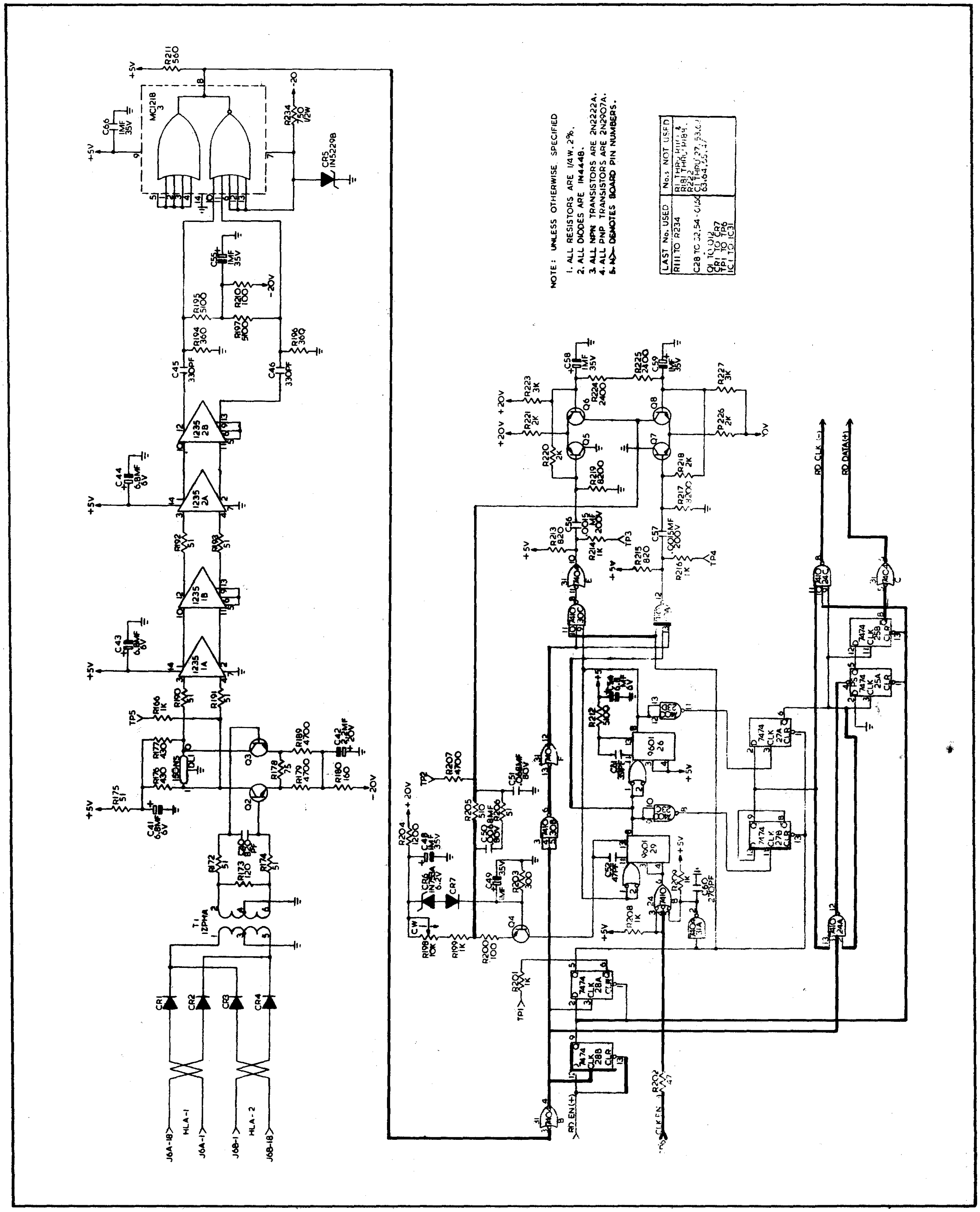


Figure 3-7. 9480-12 CEM Board, Sheet 1 (Data Discriminator)

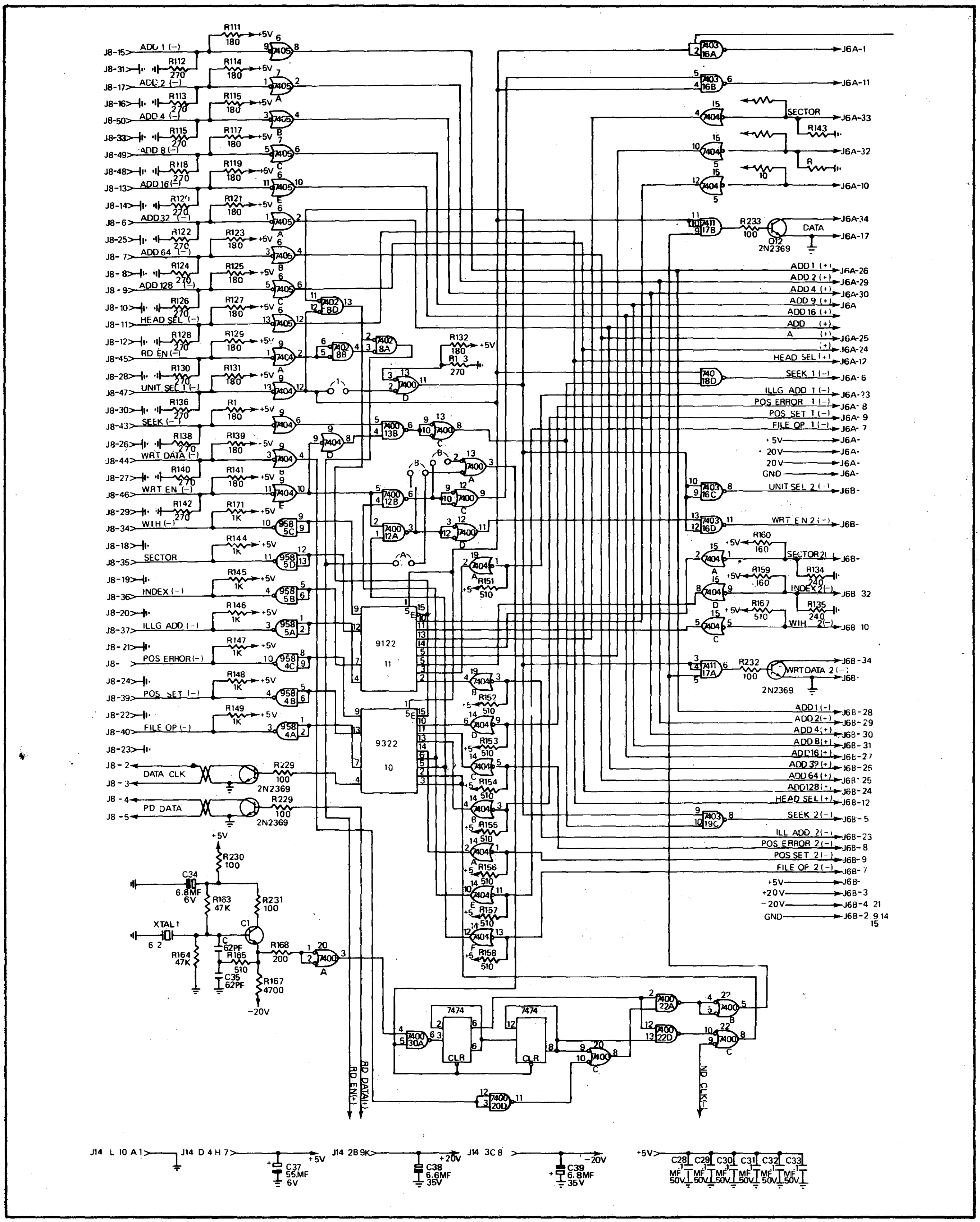
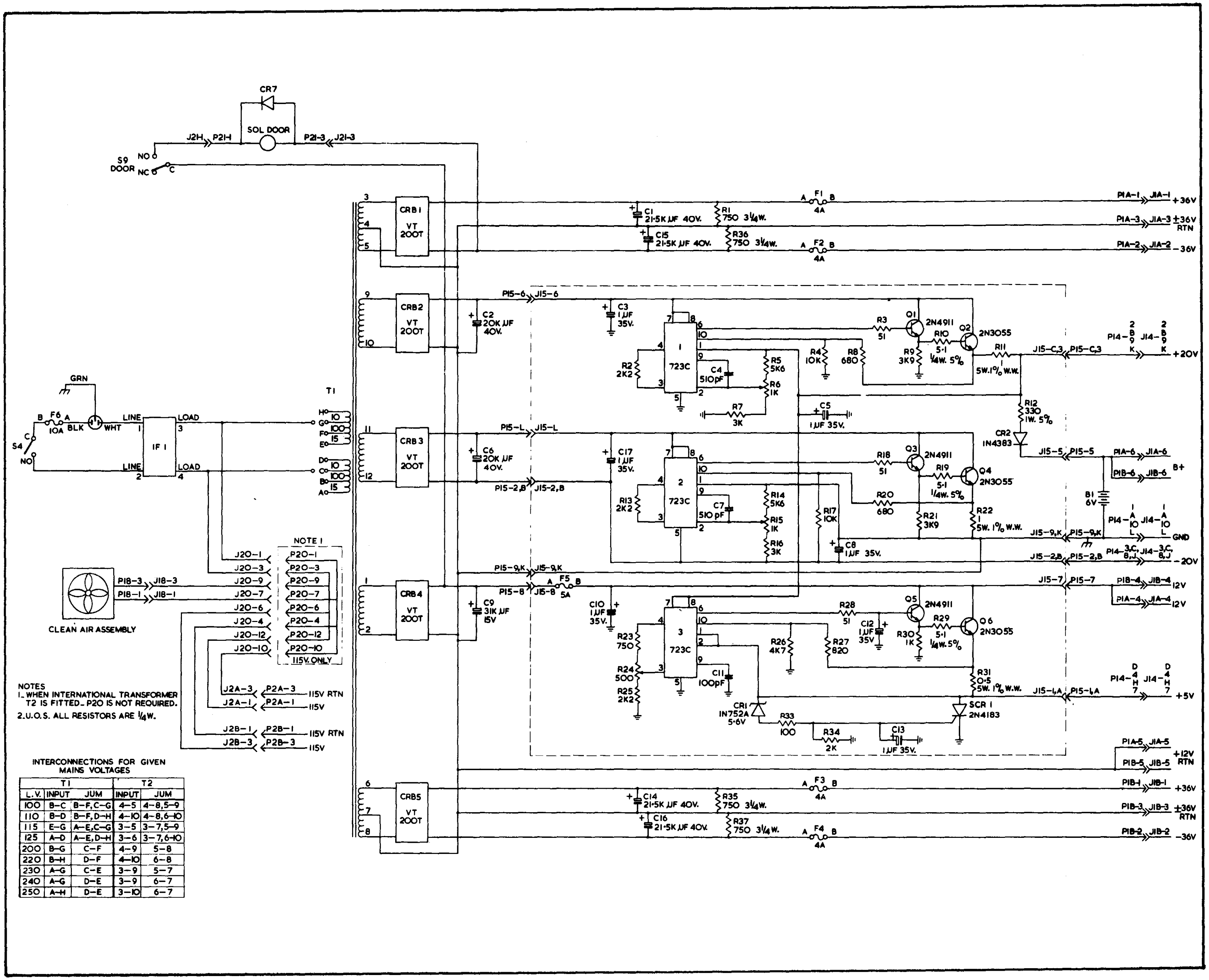


Figure 3-8. 9480-12 CEM Board, Sheet 2



NOTES
1. WHEN INTERNATIONAL TRANSFORMER T2 IS FITTED_ P20 IS NOT REQUIRED.
2. U.O.S. ALL RESISTORS ARE ¼W.

INTERCONNECTIONS FOR GIVEN MAINS VOLTAGES

T1			T2	
L.V.	INPUT	JUM	INPUT	JUM
100	B–C	B–F, C–G	4–5	4–8, 5–9
110	B–D	B–F, D–H	4–10	4–8, 6–10
115	E–G	A–E, C–G	3–5	3–7, 5–9
125	A–D	A–E, D–H	3–6	3–7, 6–10
200	B–G	C–F	4–9	5–8
220	B–H	D–F	4–10	6–8
230	A–G	C–E	3–9	5–7
240	A–G	D–E	3–9	6–7
250	A–H	D–E	3–10	6–7

Figure 3-9. 9480-12 Power Supplies

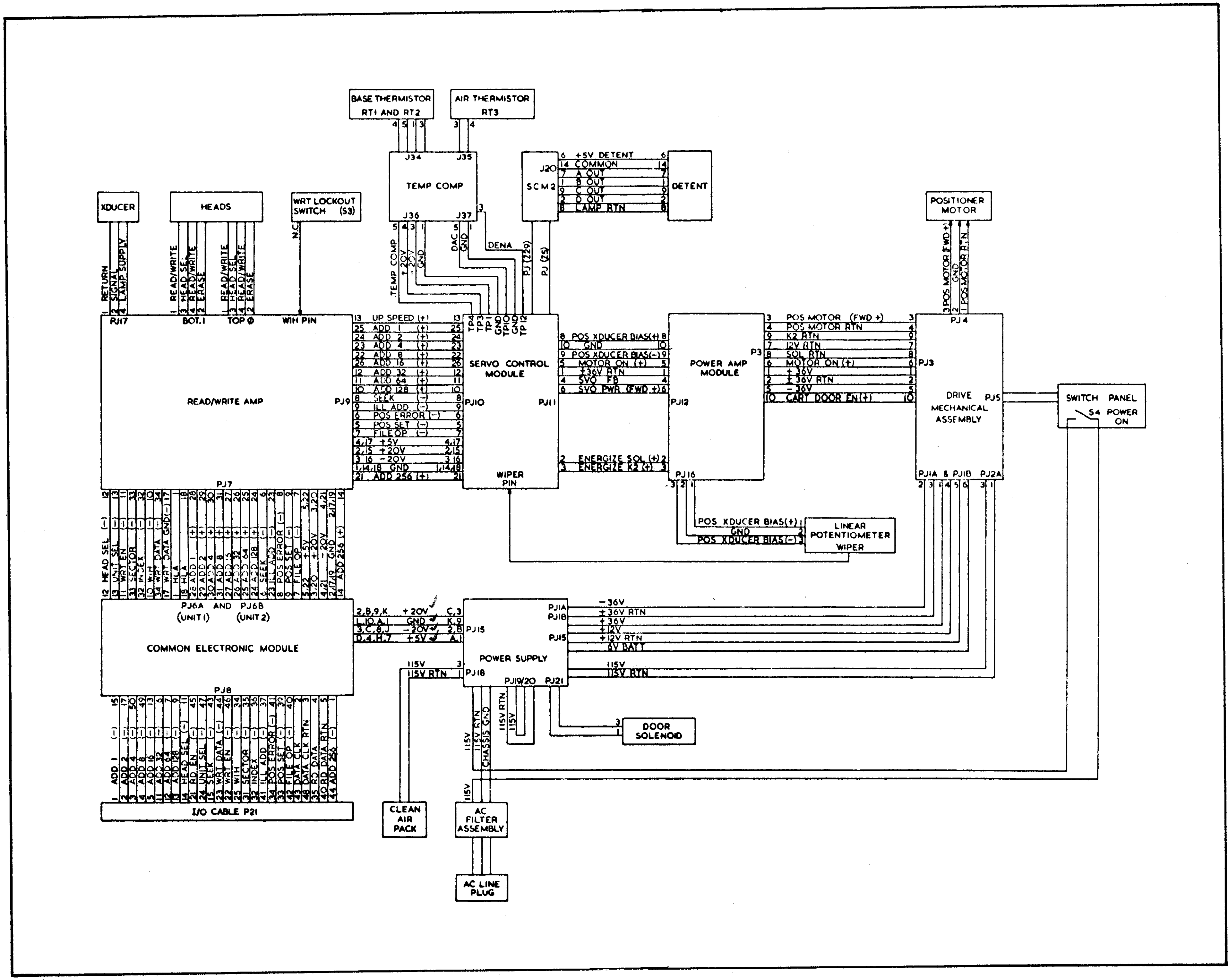


Figure 3-10. 9481-12 System Block Diagram

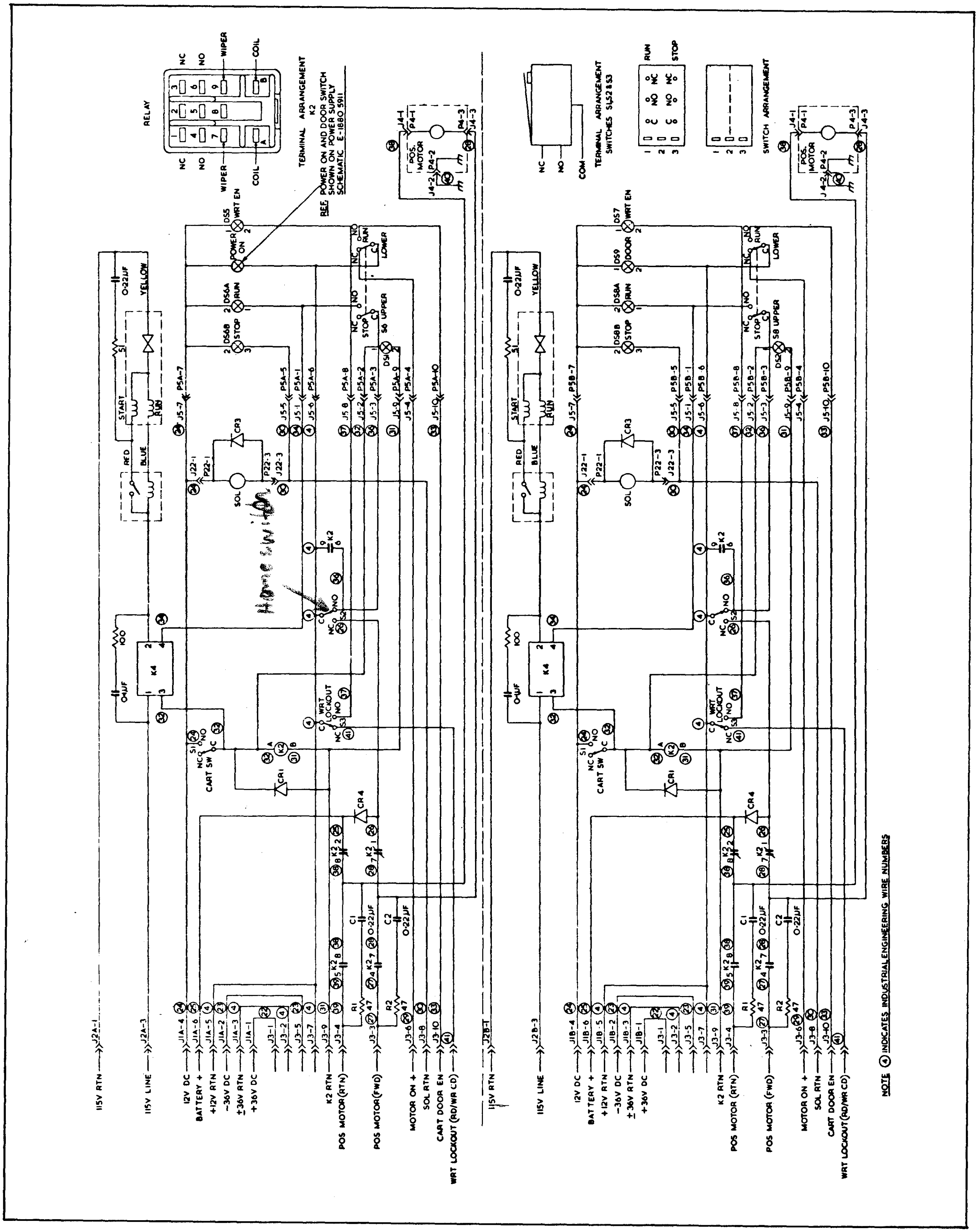


Figure 3-11. 9481-12 Main Drive Harness

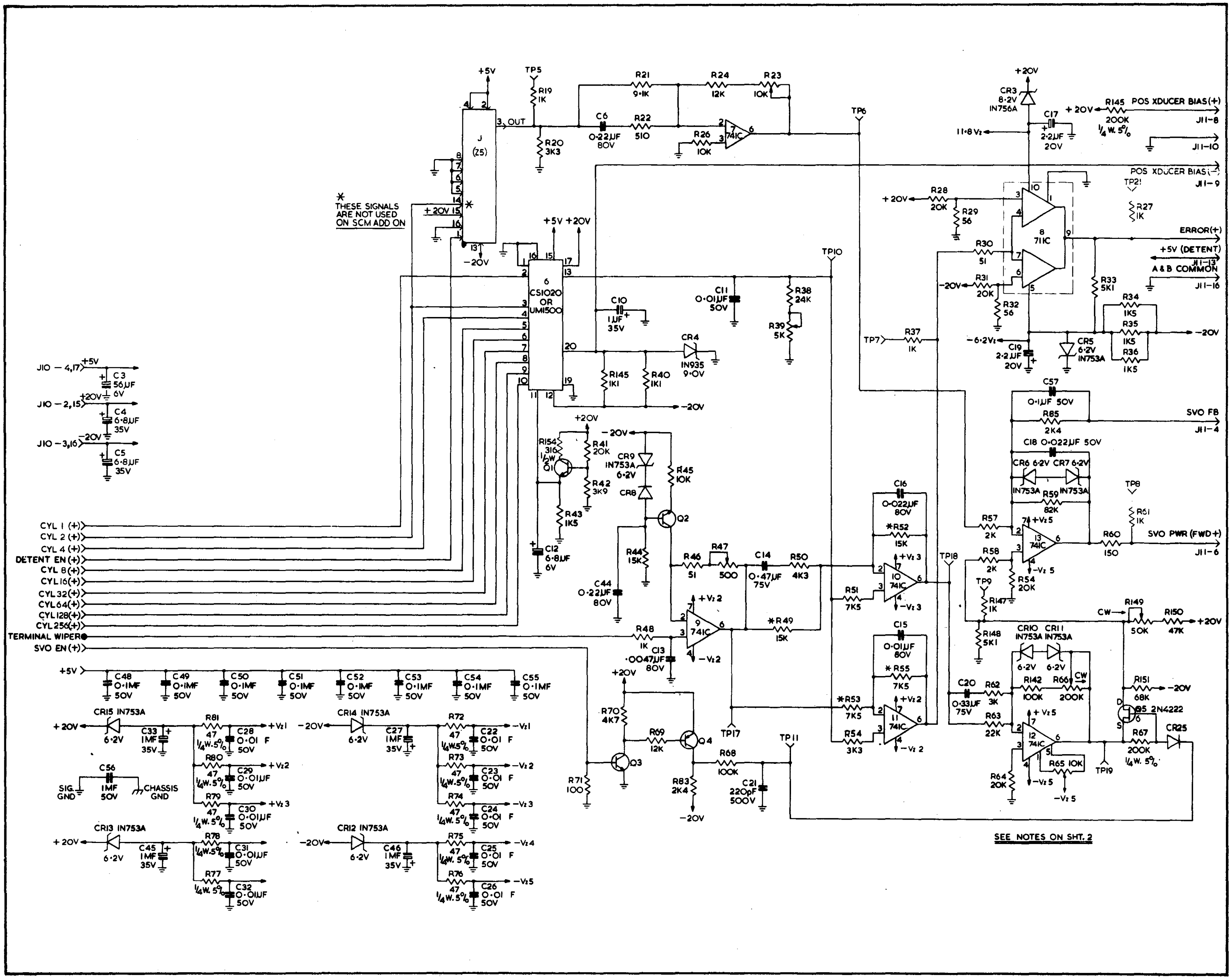


Figure 3-12. 9481-12 SCM-1 Board, Sheet 1

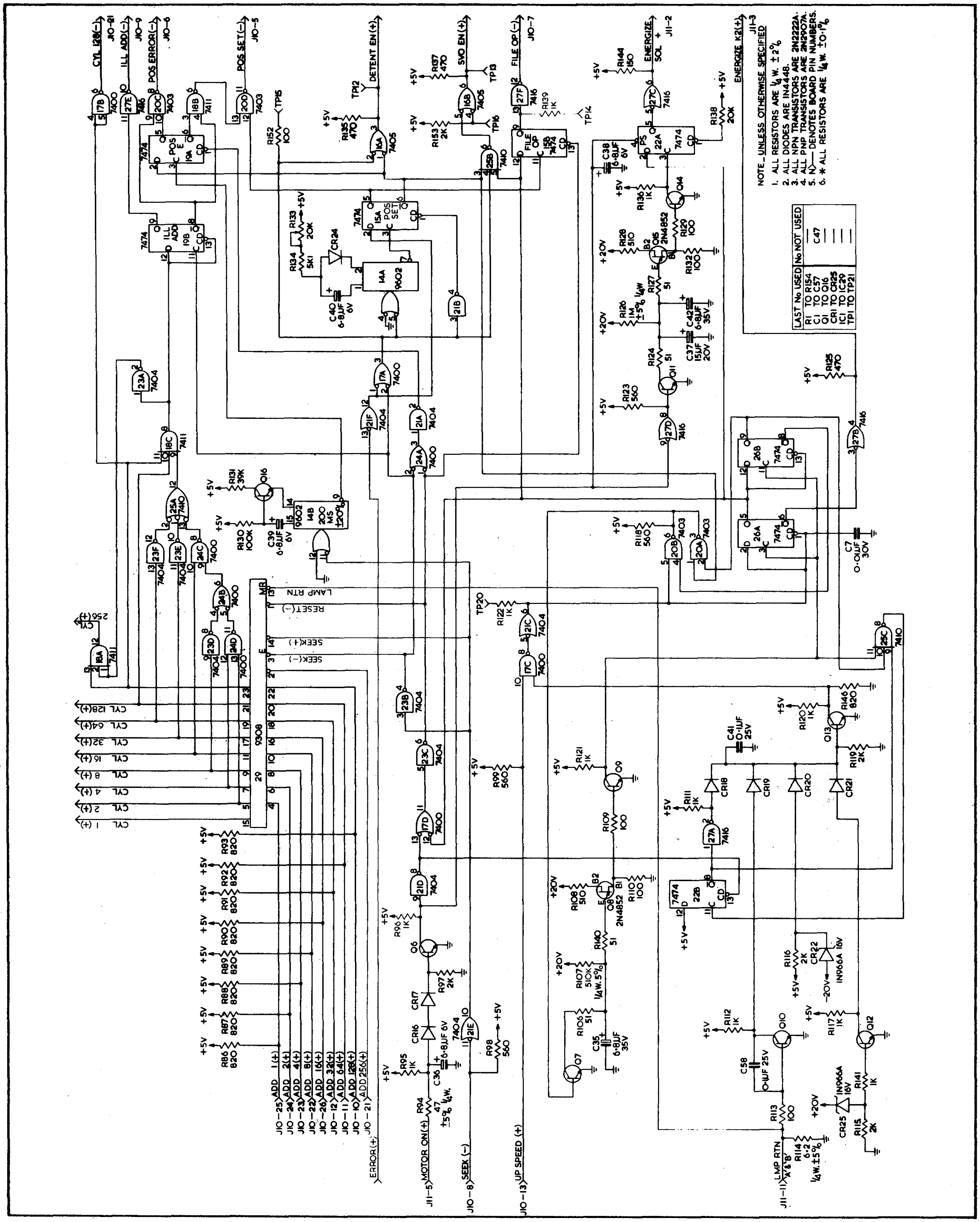


Figure 3-13. 9481-12 SCM-1 Board, Sheet 2

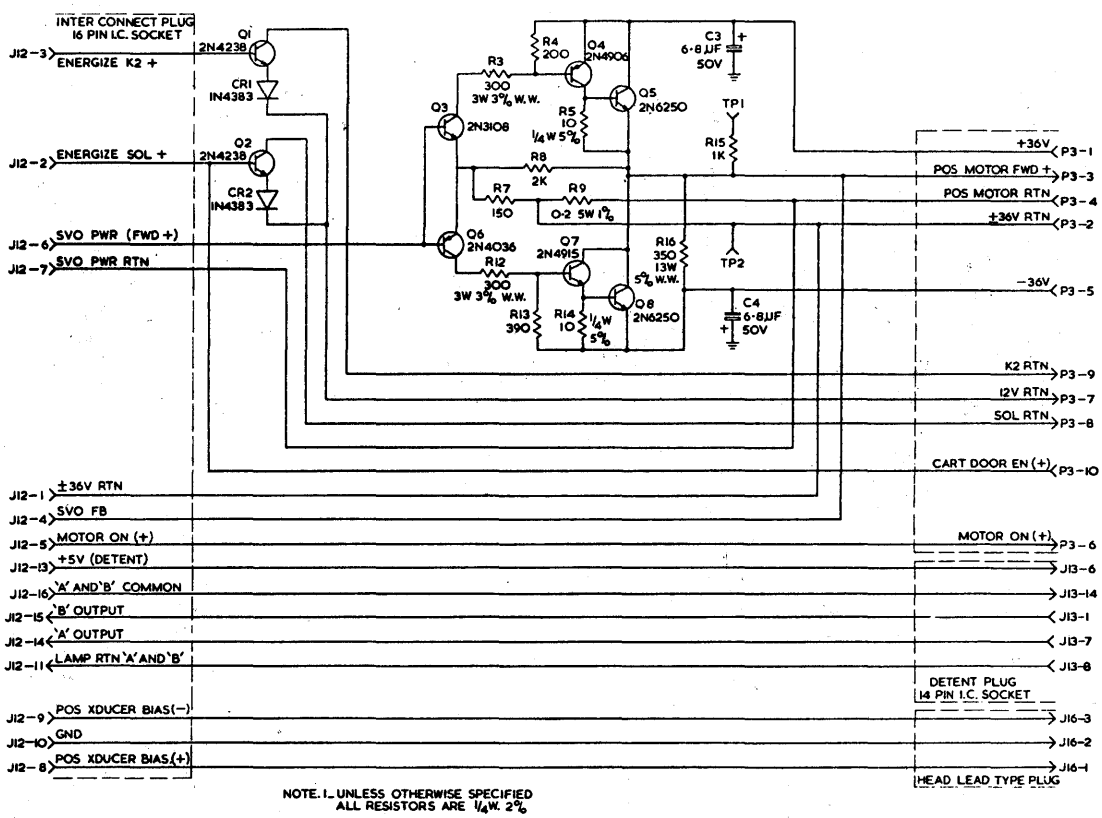


Figure 3-14. 9481-12 PAM Board

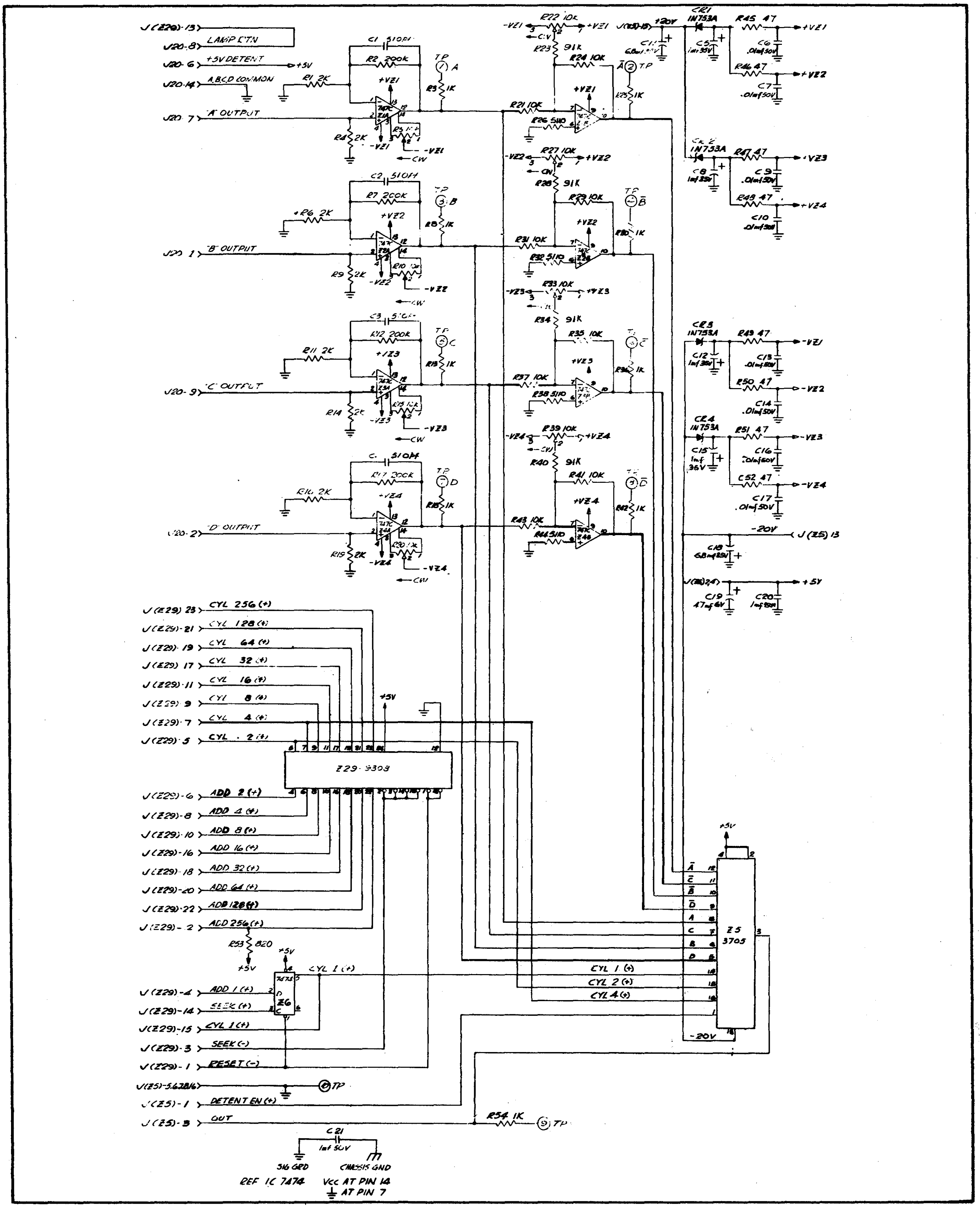


Figure 3-15. 9481-12 SCM-2 Board

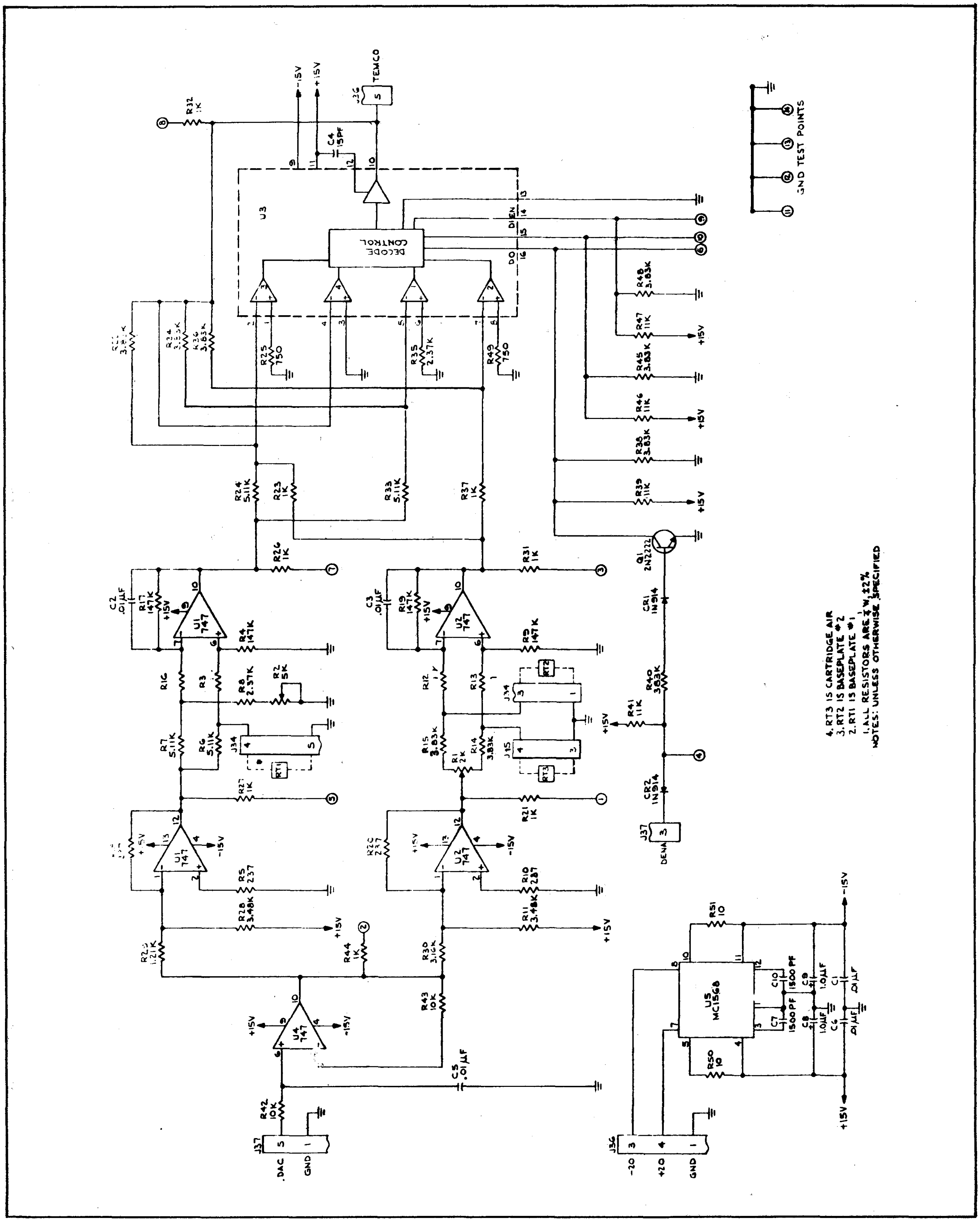


Figure 3-16. 9481-12 Temperature Compensation Board

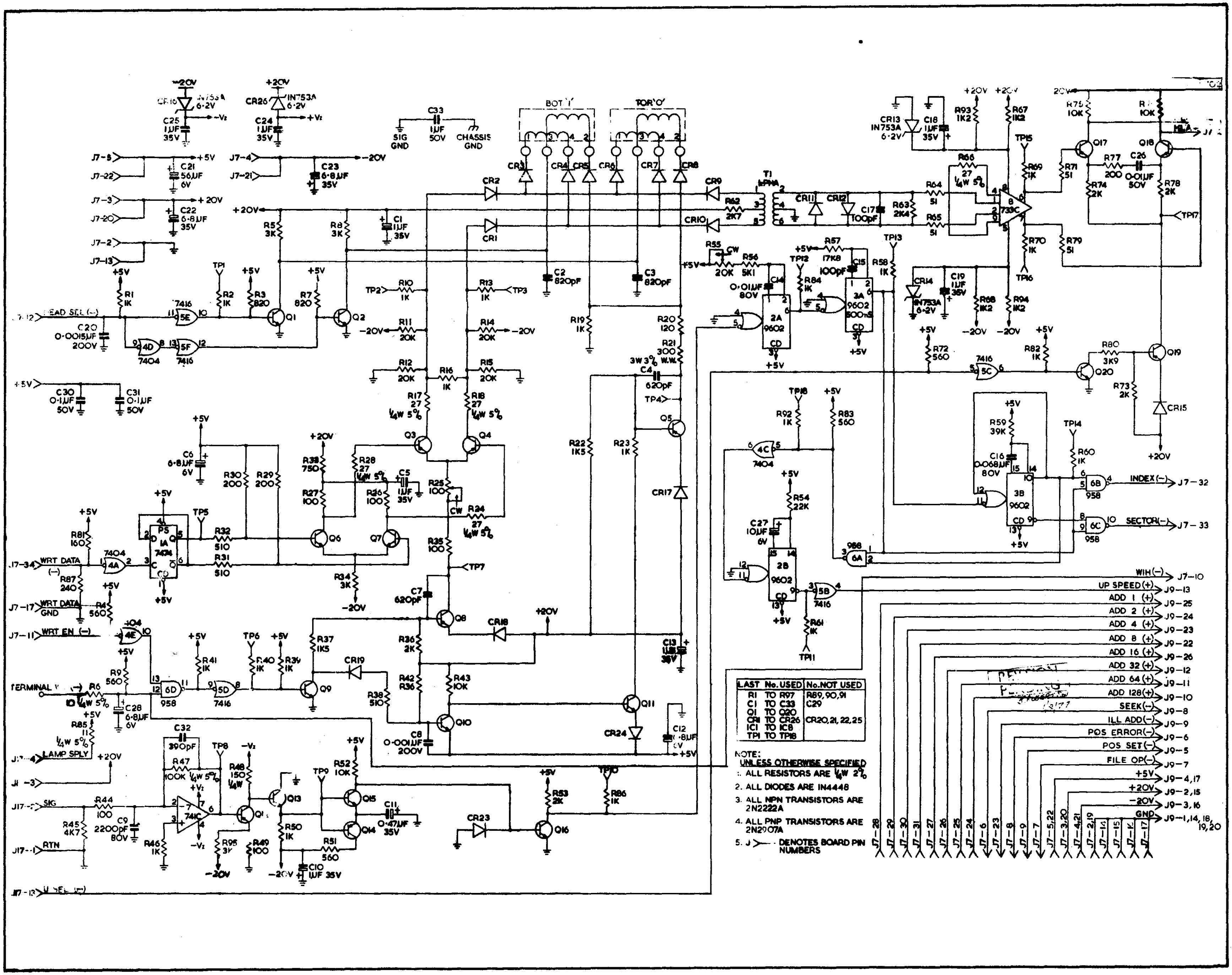


Figure 3-17. 9481-12 RWA Board

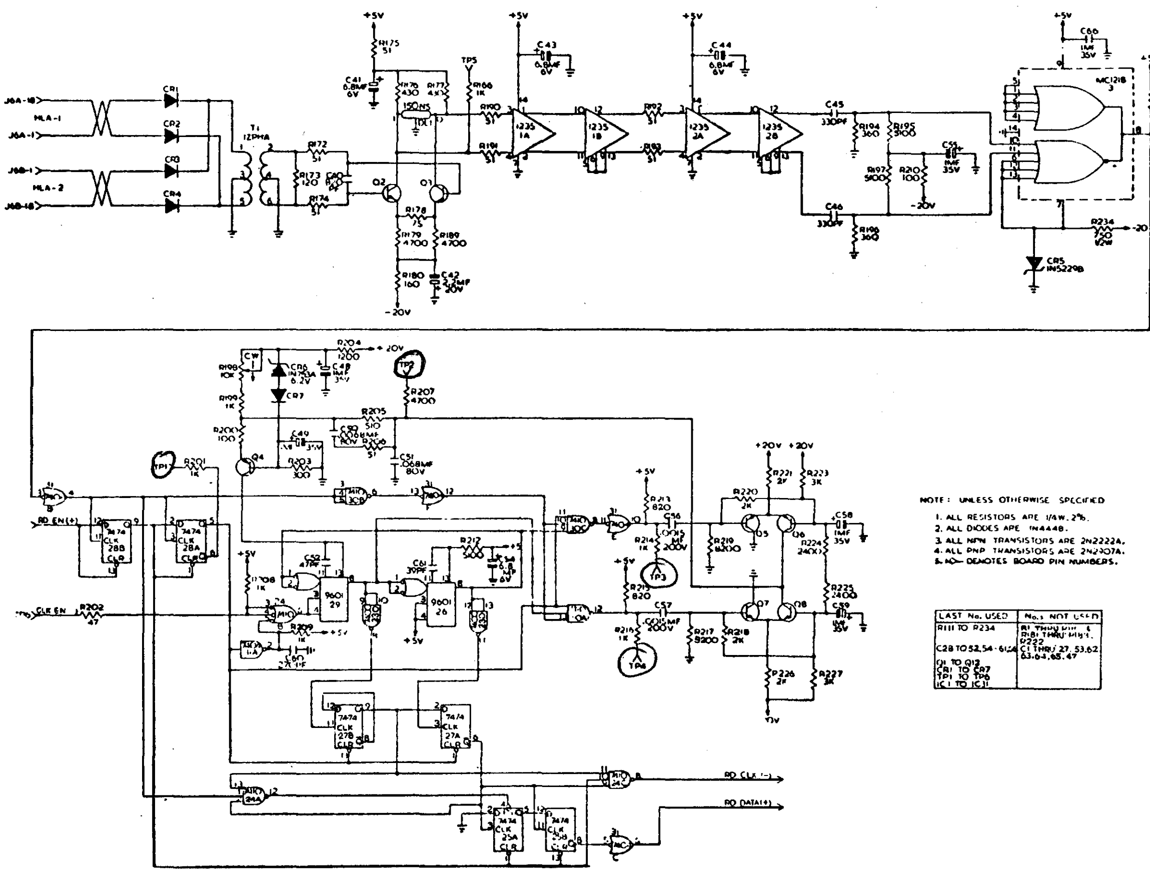


Figure 3-18. 9481-12 CEM Board, Sheet 1 (Data Discriminator)

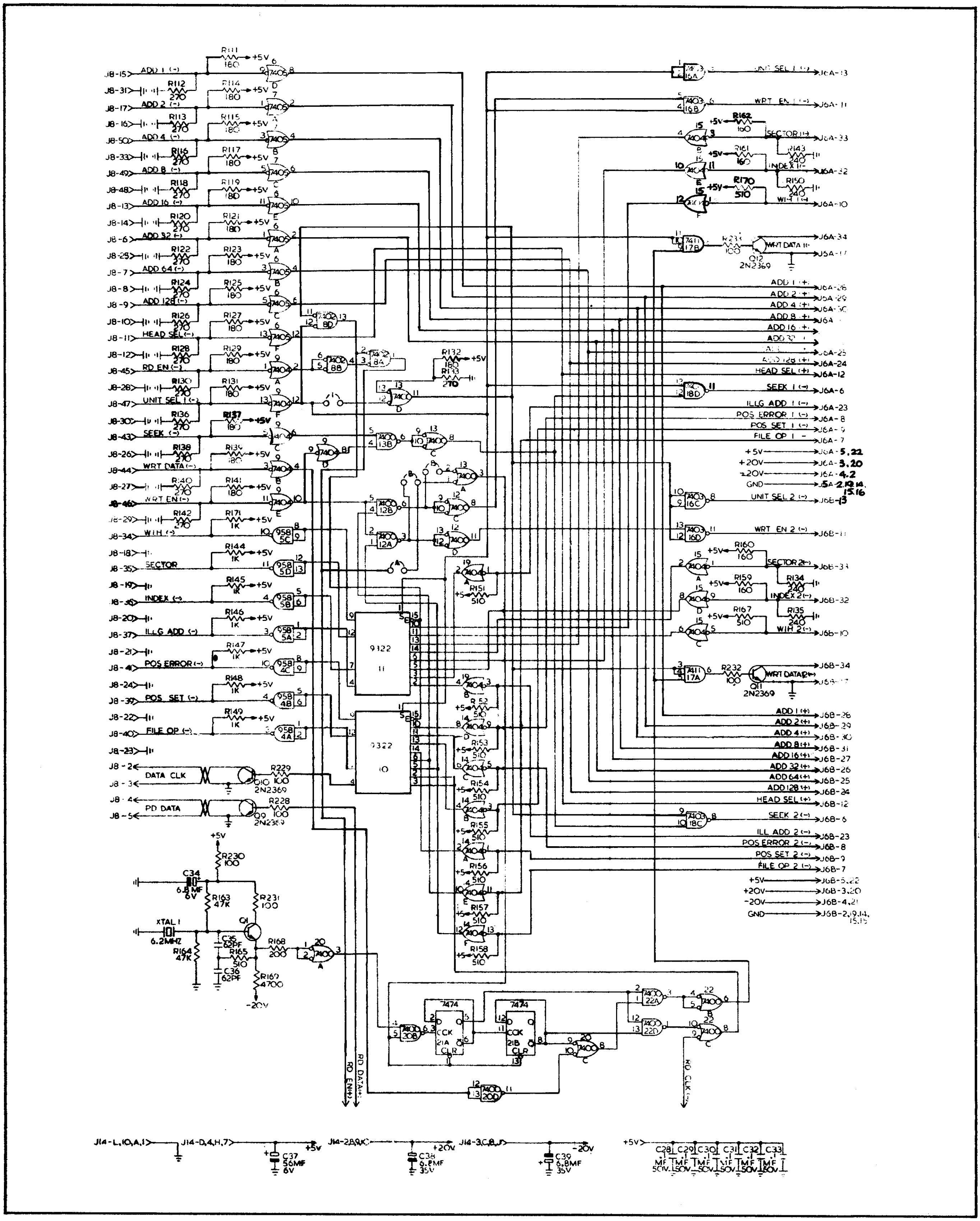
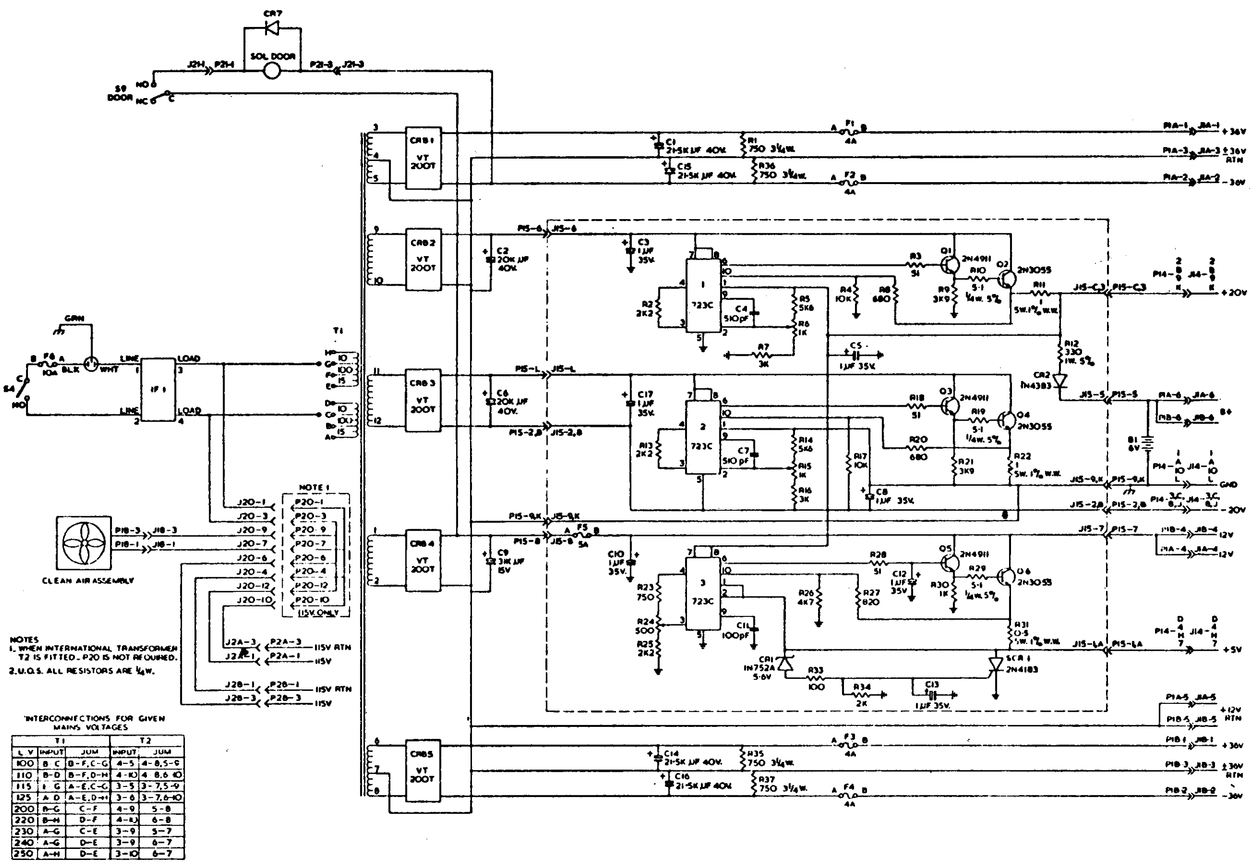


Figure 3-19. 9481-12 CEM Board, Sheet 2



NOTES
1. WHEN INTERNATIONAL TRANSFORMER T2 IS FITTED. P20 IS NOT REQUIRED.
2. U.O.S. ALL RESISTORS ARE ¼W.

INTERCONNECTIONS FOR GIVEN MAINS VOLTAGES

T1			T2	
L.V	INPUT	JUM	INPUT	JUM
100	B-C	B-F, C-G	4-5	4-8, 5-9
110	B-D	B-F, D-H	4-10	4-8, 6-10
115	I-G	A-E, C-G	3-5	3-7, 5-9
125	A-D	A-E, D-H	3-6	3-7, 6-10
200	B-G	C-F	4-9	5-8
220	B-H	D-F	4-10	6-8
230	A-G	C-E	3-9	5-7
240	A-G	D-E	3-9	6-7
250	A-H	D-E	3-10	6-7

Figure 3-20. 9481-12 Power Supplies

SECTION 4
TESTS AND ADJUSTMENTS

EQUIPMENT REQUIRED

The following equipment is required to perform the tests and adjustments outlined in this section.

Description	Part No.
Oscilloscope	
Exerciser or Run Box (as available)	
Digital volt meter (DVM)	
Cartridge test hub (from a discarded cartridge)	
Scratch cartridge	
Alignment cartridge	2158 7308
Upper head removal tool	1622 3489
Torque wrench preset to 8 in.lbs.	
IC pin extender	
Position Transducer Adjustment tool	1622 3356
Texwipes	1622 3778
Isopropyl alcohol	1624 9294
12" socket extension (electrically insulated)	1623 0740
3/32" Hex head Cap screwdriver	1622 2903
7/64" Ball driver	1622 3380
Trimpot Adjustment screwdriver	1623 1185
Servo coil positioning gauge	1622 3471
Jumper leads (hook-probes)	1622 1897

9480-12 TESTS AND ADJUSTMENTS

POWER SUPPLY VOLTAGES

Using the DVM, measure the power supply voltages as shown in table 4-1. Make adjustments as necessary.

Table 4-1. Power Supply Voltages

Voltage	Test Point	Adjustment	Tolerance
+5V	C37 CEM (+side)	R24 PS board	± 0.1V
−20V	C39 CEM (−side)	R15 PS board	± 0.4V
+20V	C38 CEM (+side)	R6 PS board	± 0.4V
+36V	C3 PAM (+side)	Fixed	± 5.0V
−36V	C4 PAM (−side)	Fixed	± 5.0V

INDEX AND SECTOR

INDEX PULSE

1. Install a scratch cartridge and power up the drive.
2. Set up oscilloscope as follows:

Channel 1	T.P.18, Read/Write board 2V/cm.
Time base	5 milliseconds/cm
Sync	Internal negative.
Mode	Channel 1 only.

3. Check that the interval between INDEX pulses is 40±0.5 milliseconds, as shown in figure 4-1.

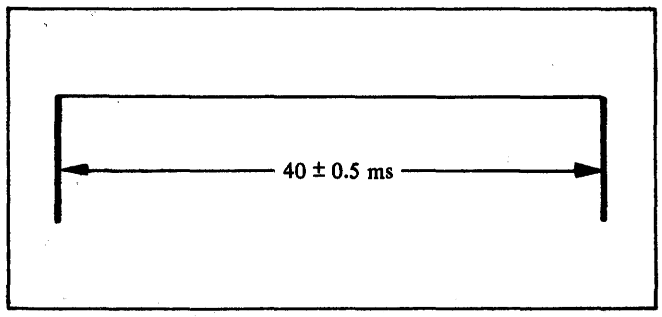


Figure 4-1. INDEX Pulse

SECTOR PULSE

1. Set up oscilloscope as follows:

Channel 1	T.P.8 Read/Write board 1V/cm
Time base	5 milliseconds/cm.
Sync.	External negative on INDEX (T.P.18 on Read/Write board)
Mode	Channel 1 only.

2. Observe the SECTOR pulses, as shown in figure 4-2, and count them. There should be 32 sector pulses between the INDEX pulses.
3. Each SECTOR and the INDEX pulse must have a minimum peak-to-peak amplitude of 2.2V and a maximum peak-to-peak amplitude of 4.0V.
4. If any SECTOR pulse is less than 2.2V, then check:
   a. Cartridge hub slots for blockages.
   b. Transducer photo-cell for partial masking with

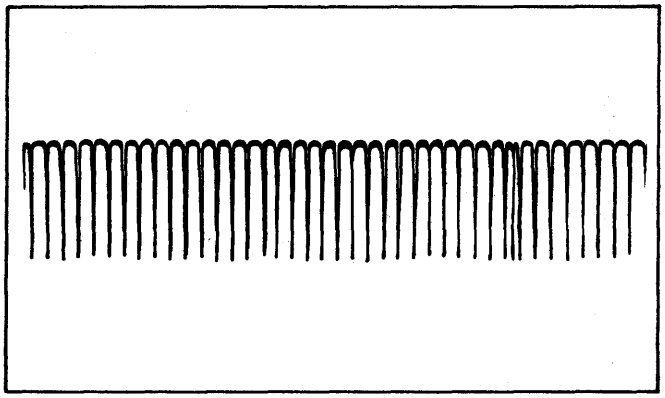


Figure 4-2. SECTOR Pulses

black paint. If so, carefully remove the paint until a satisfactory output is obtained.

c. If an improvement cannot be obtained as in a. through b. above, then the Sector Transducer must be replaced.

IF THE SECTOR TRANSDUCER OUTPUT IS INSUFFICIENT, THE DRIVE WILL GIVE SEEK ERRORS AND/OR UNCOMMANDED HEAD RETRACTS.

5. If any SECTOR pulse is greater than 4.0V, this may be corrected by carefully using black paint to mask off an uninterrupted line across the top of the transducer photo-cell.

IF THE SECTOR TRANSDUCER OUTPUT IS EXCESSIVE, THE HEADS MAY FAIL TO RETRACT AT THE CORRECT TIME DURING POWER-DOWN, OR THE HEADS MAY LOAD BACK ONTO THE DISK WHEN SECTOR PULSES SLOW TO 40mS APART.

WRITE CURRENT

1. Set up oscilloscope as follows:

Channel 1	One side of R35, Read/Write board 1V/cm
Channel 2	The other side of R35. INVERTED. 1V/cm.
Time base	10 milliseconds/cm.
Mode	Added.

2. Install a scratch cartridge and power up the drive.
3. Using exerciser, run box, or processor, write a continuous all '0's pattern.
4. Obtain the trace shown in figure 4-3. The peak-to-peak amplitude must be 3.9V±0.1V. Adjust R25 on the Read/Write board as necessary.

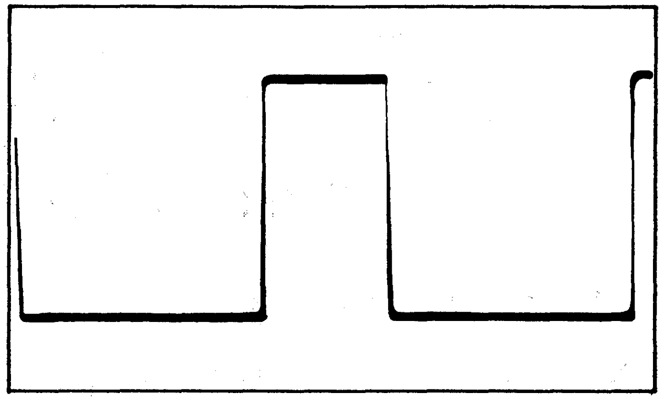


Figure 4-3. Write Current

CLEANING CARRIAGE GUIDE AND LINEAR POT (Refer to figure 4-4)

NOTE

THIS IS A PREREQUISITE TO PERFORMING THE DETENT, SERVO AND HEAD ALIGNMENT PROCEDURES

1. Power down the drive, remove any cartridge which may be present, and remove A.C. power.
2. Remove the Cartridge Door Opener Bail.

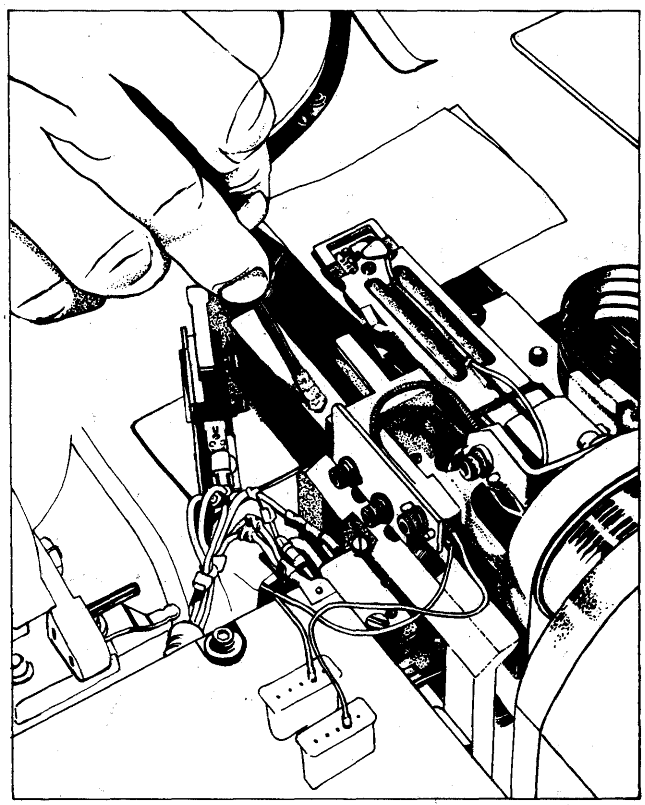


Figure 4-4. Cleaning Carriage Guide and Linear Pot

NOTE
This is necessary to prevent damage to the heads.

3. Place a folded Texwipe pad between the heads.
4. Disconnect the Servo Plug, P/J4.
5. Remove the Magnet Shield (if present), by unscrewing the two screws securing the flexible circuit bracket.
6. Using Texwipe, Cotton Buds and Isopropyl Alcohol, carefully clean the carriage rails and linear pot. Take great care not to damage the Wiper. Ensure complete free, unrestricted movement of the carriage over the total Guide length. Do not forget to clean the underneath surfaces.
7. Visually check that the Wiper is correctly positioned on the Linear Pot, that is, the center of the track, and is undamaged.

DETENT, SERVO ALIGNMENT AND SERVO RESPONSE

DETENT AMPLIFIERS

1. Ensure that P/J4 is disconnected, and that the Texwipe pad is still in place beneath the heads.
2. Set up oscilloscope as follows:

Channel 1	T.P.2 on SCM board. 500mV/cm.
Time base	5 milliseconds/cm.
Sync.	Internal positive.
Mode	Channel 1 only.

3. ENSURE THE CARTRIDGE DOOR OPENER BAIL IS REMOVED.
4. Apply A.C. power.
5. While manually moving the Carriage back and forth, check for a minimum signal amplitude of 1.5V over the entire range of the carriage. If variation is greater than 15%, re-align the mask to transducer assembly, as per Section 5.
6. Move channel 1 of the oscilloscope to T.P.4 on the SCM board, and repeat step 5.
7. The signals obtained from T.P.2 and T.P.4 must be of equal amplitude, +15%. If not, adjust by physically re-positioning the transducer assembly.
8. Turn off A.C. power and disconnect the SCM board plug, P/J11.
9. Turn on A.C. power.
10. Connect the DVM leads to T.P.1 on SCM board and the ground nearest T.P.1.
11. Adjust R56 on SCM board for 0±5mV.
12. Move the D.V.M. lead from T.P.1 to T.P.3 on the SCM board.
13. Adjust R82 on SCM board for 0V+5mV.

NOTE
The signal obtained from TP1 and TP3 must be of equal amplitude, ± 15%. If not, adjust by physically re-positioning the transducer assembly

14. Turn off A.C. power.
15. Replace the SCM board plug, P/J11.
16. Replace the Servo Plug, P/J4.

SERVO ALIGNMENT

NOTE
THESE ADJUSTMENTS MUST BE PERFORMED STRICTLY IN SEQUENTIAL ORDER. IF A MISTAKE IS MADE, GO BACK TO THE BEGINNING AND START AGAIN.

1. Install the Test Hub and override the Cartridge Interlock Switch (for example, with a cardboard strip).
2. Ensure that Texwipe pad is in place between the heads.
3. Turn on A.C. power.
4. Monitor T.P.8 and adjust R149 on SCM board for 0+100mV. (This is an initial setting only).
5. Power up the drive. When the heads are loaded jumper to ground the end of R152 opposite T.P.15 on the SCM board. (This is to force the drive into DETENT mode while performing the Positioner Coil Adjustment).
6. Insert the Servo Coil Positioning Gauge between the magnet and the rear of the carriage assembly as in figure 4-5.

NOTE
Gauge must be above rubber ring.

7. Position the carriage assembly such that the gauge is a snug fit. Resistance will be felt as the carriage is moved against the detent, but this is of no consequence provided the jumper has

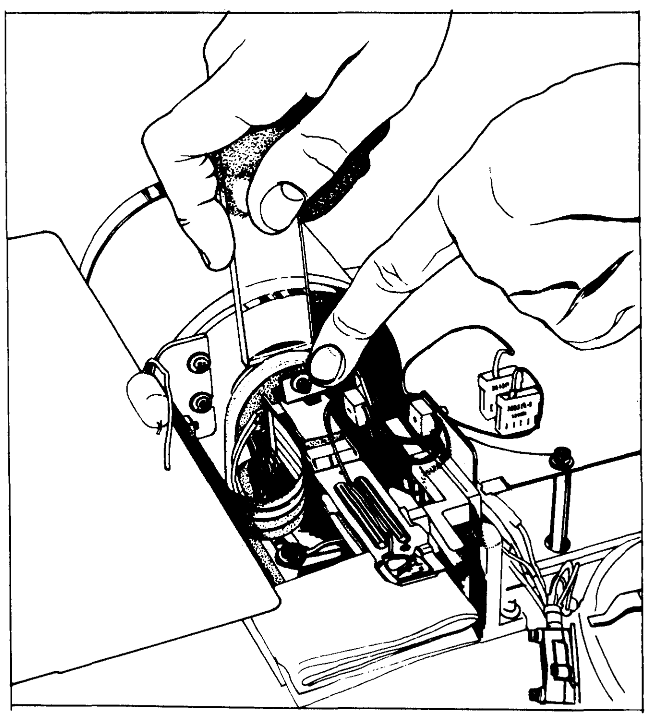


Figure 4-5. Positioner Coil Adjustment

been installed in step 5.
Remove the gauge and allow the carriage to detent.

8. Using the DVM, monitor the voltage between T.P.0 on the SCM board and the ground adjacent to R56 for −85mV+5mV. If correct go to step 13.

NOTE
The Wiper tension must be correct.

9. Loosen the Linear Pot securing screws until they are just snug.
10. Using the Position Transducer Adjustment Tool, re-position the Linear Pot until the reading at T.P.0 is −85mV±5mV.
11. Tighten the Linear Pot securing screws. DO NOT OVER-TIGHTEN THE SCREWS – THIS CAN BREAK THE LINEAR POT.
12. Check that the Linear Pot connecting leads have not risen and fouled the carriage path. If so, tighten them by slackening the cable clamp and pulling the slack to the plug end.
13. Monitor the voltage at T.P.7 on SCM board, using the D.V.M., and adjust R47 on SCM board for 0+0.5mV.
14. Power down the drive and turn off A.C.
15. Remove the jumper installed in step 5.
16. Replace the Magnet Shield if necessary.
17. Turn on A.C., and power up the drive. (Test Hub and Texwipe pad still in place).
18. Recheck the following, and fine adjust as necessary:
    a. T.P.0 on SCM board for −85mV+5mV. (Linear Pot position).
    b. T.P.7 on SCM board for 0+0.5mV. (R47).
19. Using exerciser, run box or processor, step the Positioner out one track at a time, and monitor the voltage at T.P.7 with the D.V.M.
    Track 00 must be 0+0.5mV.
    Tracks 01 through 202 must be 0+14mV.
    Adjust R39 and R47 on SCM board and repeat as necessary until an optimum setting has been obtained for all tracks.

SERVO RESPONSE

1. Power up the drive. (Test hub and Texwipe pad still in place).
2. Install the I.C. Pin Extender on I.C.15 on SCM board.
3. Set up oscilloscope as follows:

Channel 1	I.C.15, pin 5, on SCM board. 2V/cm.
Time base	2 milliseconds/cm.
Sync.	Internal negative.
Mode	Channel 1 only.

4. Set exerciser or processor to alternately seek tracks 00 and 01.
5. Obtain the signal shown in figure 4-6, and adjust R133 on the SCM board such that the pulse width is 13+2 milliseconds.

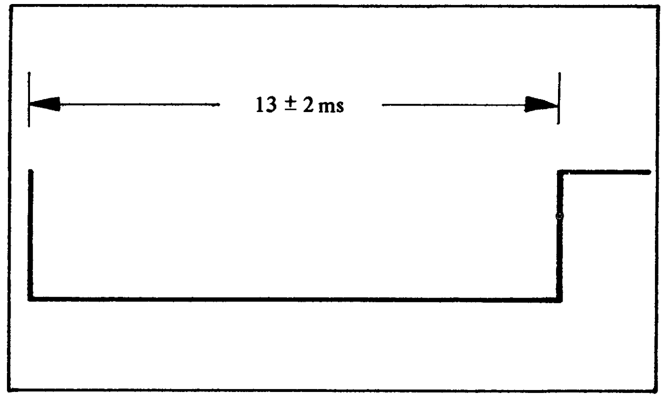


Figure 4-6. Short Servo Gate

6. Leave the oscilloscope connected as in step 3, but increase the time base to 10 milliseconds/cm.
7. Set the exerciser or processor to seek alternately between tracks 00 and 202.
8. Obtain the trace shown in figure 4-7. Move the positive-going edge to coincide with the centre graticule. Switch in the X10 magnifier.
9. Adjust R65 on the SCM board to give minimum jitter, that is, less than 10 milliseconds.
10. Switch out the X10 magnifier on the oscilloscope, and reset the horizontal position to normal.
11. Adjust R66 on the SCM board to give a pulse width of 80±5mS, as in figure 4-8.

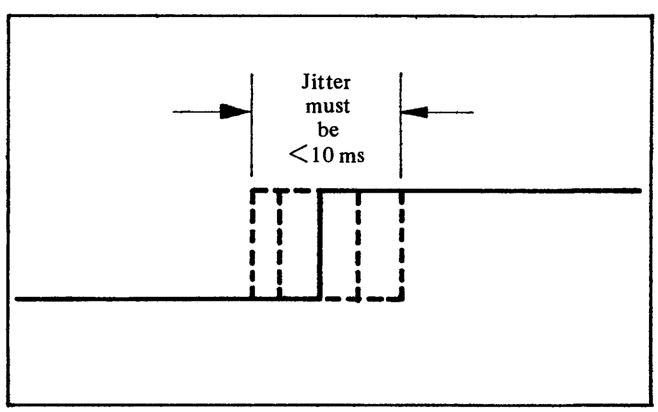


Figure 4-7. Long Servo Gate Jitter

12. Set up oscilloscope as follows:

Channel 1	T.P.5 on SCM board. 50 millivolts/cm.
Time base	2 milliseconds/cm.
Sync.	External negative, I.C.15 pin 5 on SCM board.
Mode	Channel 1 only.

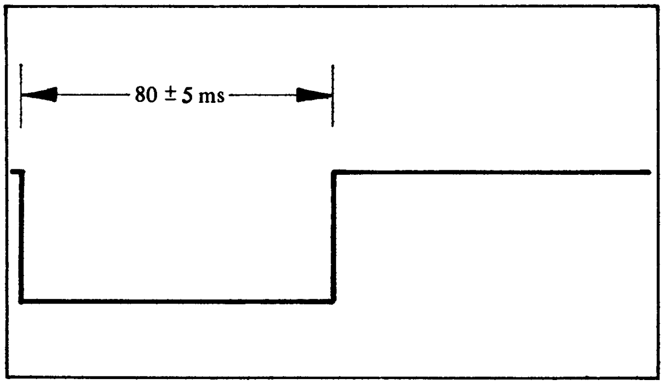


Figure 4-8. Long Servo Gate – Width

13. Set up exerciser or processor to seek alternately tracks 00 and 01.
14. Obtain the trace shown in figure 4-9. This signal is the output from 'the Detent Amplifier Circuits. As the positioner locates itself over the desired track, an overshoot occurs as the servo goes into DETENT. This overshoot is then compensated for by amplified feedback from the detent circuits, and the carriage therefore oscillates slightly for a period of time. It is important that this 'settle time' should be minimised, as excessive carriage oscillation can cause errors.

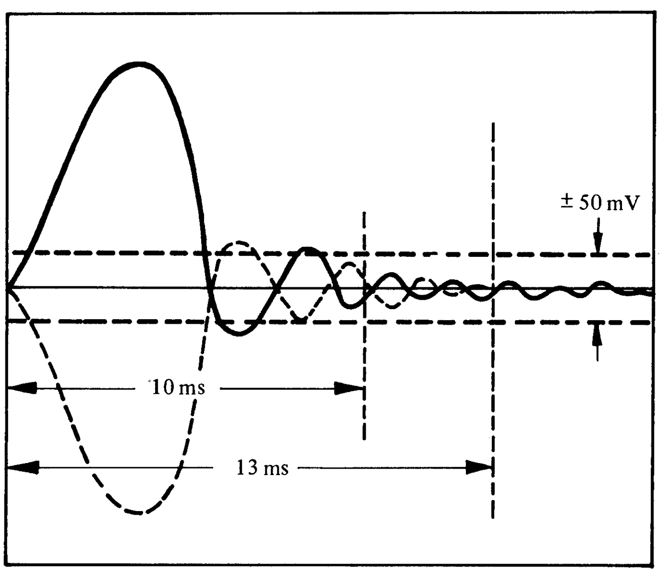


Figure 4-9. Servo Settle Time

15. Adjust R23 on the SCM board for the minimum overshoot within 10 milliseconds. After 13 milliseconds, no overshoot should exceed ±50mV.

NOTE

The first big overshoot (which can be positive or negative) should be ignored.

16. Set exerciser or processor to seek sequentially from track 00 through 202. Ensure that the settle time remains within ±50mV before 13 milliseconds. Re-adjust R23 if required.

17. With the exerciser or processor set to seek alternate between track 00 and track 202 move channel 1 of the oscilloscope to T.P.5 on the SCM board.
18. Ground channel 1 and accurately set the trace to the centre graticule line.

NOTE

Oscilloscope ground lead must be connected to ground on SCM board.

19. Switch the oscilloscope to 100mV/cm. Increase the time base to 10 milliseconds/cm.
20. The oscilloscope will now show both the forward and reverse long seeks. The object of this adjustment is to ensure that there is minimum offset voltage input to the PAM board, while the servo is in detent. Since the offset can be different for forward and reverse seeks, the adjustment is only correct when the trace obtained is as shown in figure 4-10. Fine adjust R149 on SCM board until the correct signal is obtained.

21. Power down the drive and remove the test hub.

22. Replace the cartridge door opener bail.

HEAD ALIGNMENT

1. Remove all case covers (skins) from the unit.

2. EXAMINE THE ALIGNMENT CARTRIDGE AND MAKE SURE THAT THE WRITE LOCKOUT PLUG IS PUSHED IN AND LOCKED.

3. Insert the Alignment Cartridge in the drive to be checked and a scratch cartridge in the other drive.

4. Power up both drives and position the heads at track 100. Leave to warm up for at least 30 minutes.

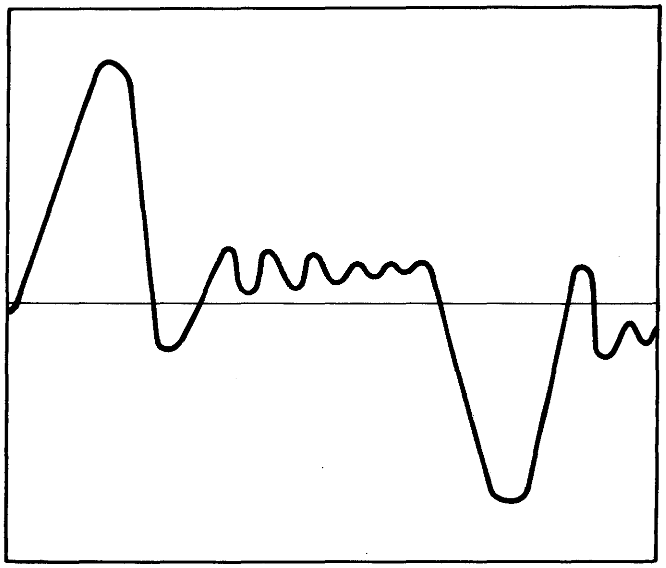


Figure 4-10a. Servo Offset Adjustment – Incorrect

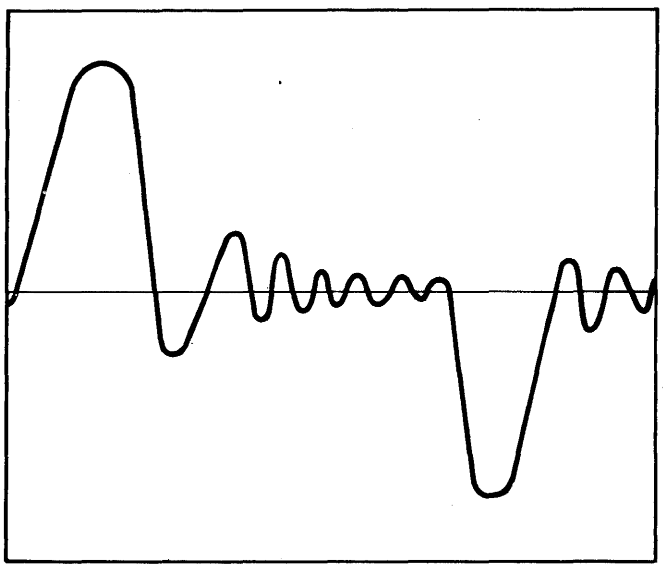


Figure 4-10b. Servo Offset Adjustment – Correct

5. Connect oscilloscope as follows:

Channel 1	T.P.15 on Read/Write board. 10mV/cm A.C.
Channel 2	T.P.16 on Read/Write board. 10mV/cm A.C. INVERTED
Time base	5 milliseconds/cm.
Sync.	External negative, T.P.18 on Read/Write board. (INDEX).
Mode	Added.

6. Condition the exerciser, run box, or processor to read continuously, "ignore errors".
7. Observe the Dibit pattern shown in figure 4-11. There should be two distinct signals, one overlapping the other, with a minimum of fringe area. The areas of overlap should be averaged out to compensate for spindle runout.
8. Perform steps 6 and 7 on both heads. If both heads are correctly aligned, ignore steps 9 through 17 and proceed straight to step 18.
9. If either head is out of alignment, then proceed as follows.
10. Slacken off the Head Locking Screw and turn the Head Adjustment Screw 6 turns counter-clockwise.

NOTE

Take great care to avoid shorting of components. Use well-insulated tools to adjust these screws.

11. Manually pull the head towards the Positioner Coil until it is snug.
12. While observing the oscilloscope trace, slowly turn the Head Adjustment Screw clockwise, until the Dibit pattern appears on the screen.
13. Continue adjusting the head until the conditions in step 7 are met. Refer to figure 4-11. The trace must look like figure 4-11b.
14. Tighten the Head Locking Screw to a torque of 8 in.lbs., using the Torque Wrench.

NOTE

OVERTIGHTENING THE SCREWS CAN DAMAGE THE HEAD SHAFT AND CAUSE DIFFICULTY IN ALIGNMENT.

15. Make a final check that the alignment has not drifted due to tightening the screw. Fine adjust if necessary.
16. Slacken the Head Adjustment Screw 1/2 turn counter-clockwise to release pressure on the shaft.
17. Repeat steps 10 through 16, if necessary, for the other head.
18. Position the heads over track 95.
19. Leave the oscilloscope settings as in step 5, but extend the time base to 5 microseconds/cm.
20. Set exerciser, run box or processor to read, "ignore errors".
21. Observe the trace illustrated in figure 4-12. The period from INDEX to data burst must be 30±5uS. Adjust R55 on Read/Write board as necessary. Check this adjustment while selecting each head, and adjust so that both heads are within the tolerance of ±5uS.
22. Repeat steps 20 and 21 with heads positioned at track 5.

NOTE

a. If there is insufficient adjustment at R55 the Sector Transducer must be re-positioned.

b. If both heads cannot be brought within the tolerance of ±5uS, head replacement should be tried. If this also fails, then the carriage assembly will have to be replaced.

23. Check the head load cam adjustment, as per Section 5.
24. Check the home position microswitch for correct adjustment.
25. If no other adjustments are to be made (such as the data discriminator), then replace the case panels (skin), and run a suitable "write/read" MTR on both drives. Use only known, good disks, and ensure no errors occur.
26. Swop the disks over between the drives, and run a "read only" option of the MTR.
27. If errors occur, the adjustments should be checked on both drives, as there may be a compatibility problem.
28. Remove the alignment cartridge.

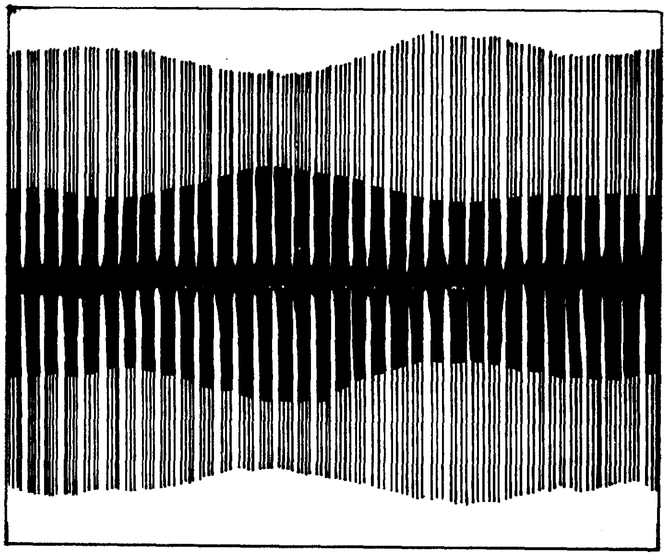


Figure 4-11a. Dibit Pattern-Head Alignment-Incorrect

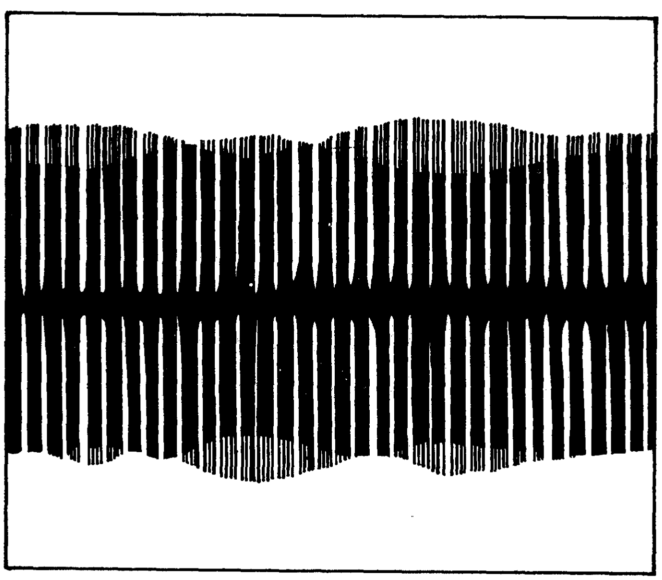


Figure 4-11b. Dibit Pattern-Head Alignment-Correct

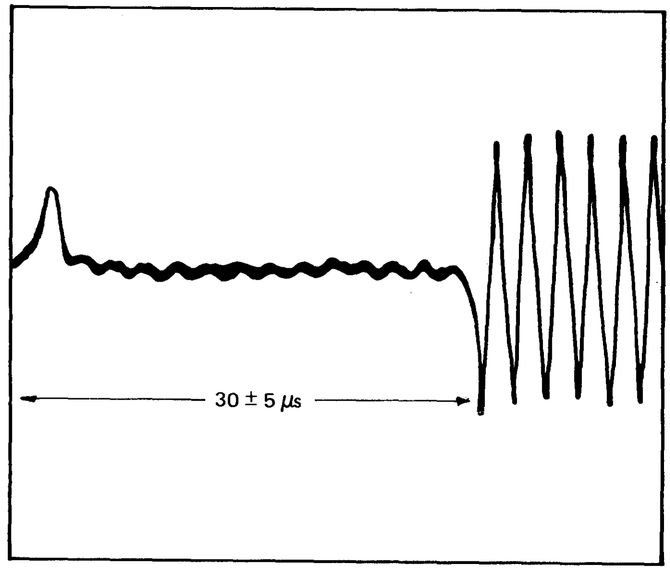


Figure 4-12. INDEX-To-Data Burst (Radial Alignment)

DATA DISCRIMINATOR

EXPLANATION

The Data Discriminator consists of a Voltage Controlled Oscillator (VCO), a Phase Comparator, and the Discriminator proper. The VCO and the Phase Comparator form a Phase-Locked-Loop, and it is this section which must be aligned.

Suitably amplified and shaped data pulses are fed to one part of the Phase Comparator, and the output from the VCO to the other. If there is a phase difference between the VCO and the data, the Phase Comparator detects this, and develops an Error Voltage which is used to increase or decrease the frequency of the VCO. (This is the signal which is monitored at T.P.2 on the CEM board). By this means, synchronization is maintained between the clock frequency (VCO) and the data frequency, thus compensating for local differences in disk rotation, etc.

When the signal READ ENABLE is false, both inputs to the Phase Comparator are disabled, and the Error Voltage will depend only on the bias applied to the transistors. At this point the Error Voltage represents the centre of the tracking range of the Phase Locked Loop.

When READ ENABLE is true, the Phase Comparator will compare the data and the clock (VCO). The set-up consists of adjusting the Error Voltage thus obtained, such that this too is at the centre of the tracking range of the Phase Locked Loop. When this is done, the VCO will be running at the same average frequency as the data coming from the disk, at the optimum point in the tracking range.

This ensures the best possible starting point for the

Phase Locked Loop to adjust itself to minor changes in data frequency, thus providing optimum clock-to-data strobing.

It is essential to make this adjustment as accurately as possible. If this is not done, a localised transient condition can push the Phase Locked Loop outside its accurate tracking range, thus inducing a strobing error, even though the drive appears to read most of the data error-free.

Such a reduction in margins can lead to intermittent and hard-to-find errors.

From this explanation, it can be seen that in order to correctly align the Phase Locked Loop, it is necessary to display the Error Voltage with READ ENABLE false, and to compare it with the Error Voltage when READ ENABLE is true. The D.C. levels of the two states can then be adjusted to be the same using R198 on the CEM board.

The Model 900 Exerciser is suitable for this set-up, since it reads 8 sectors at the beginning of a track, and then switches off. By displaying about 16 sectors, therefore, the two D.C. levels can be observed and compared.

If a processor MTR is used it is necessary to read at least 2 sectors of an initialised disk. When the processor receives a SECTOR pulse, READ ENABLE is switched off for about 70-80uSec. It is therefore necessary to locate a SECTOR pulse, observe this "switch-off" time and compare the D.C. level with the remainder of the sector being read.

A run-box is not suitable, as this reads a complete track of data without switching off READ ENABLE.

For these reasons, separate procedures are given for the Exerciser, or processor MTR.

EXERCISER METHOD

1. Insert scratch cartridges in both drives and power them up.
2. Connect oscilloscope as follows:

Channel 1	T.P.2 on CEM board. (Ground on CEM board). 10mV/cm. A.C.
Time base	2 milliseconds/cm.
Sync.	Internal negative.
Mode	Channel 1 only.

3. Write a pattern of all '0's on track 2 00 using the exerciser.
4. Turn R198 on the CEM board fully counterclockwise. (This is because there is a second position to which R198 can be adjusted, which gives the correct oscilloscope trace, but will in fact give errors).
5. Set the exerciser to perform a continuous read on the track just written in step 3, with the 'ignore error' switch 'on'.
6. Observe the traces shown in figure 4-13. The first portion of the trace is when the exerciser is reading, and is therefore the Error Voltage obtained from comparing the VCO with the data (with an ac component). During the second portion, the exerciser has switched off and this is the Error Voltage obtained with the Phase Locked Loop at the centre of its tracking range.
7. Adjust R198 until the D.C. level of the two signals is at the same point, that is, the top of the trace must be a straight line, as in figure 4-13C.

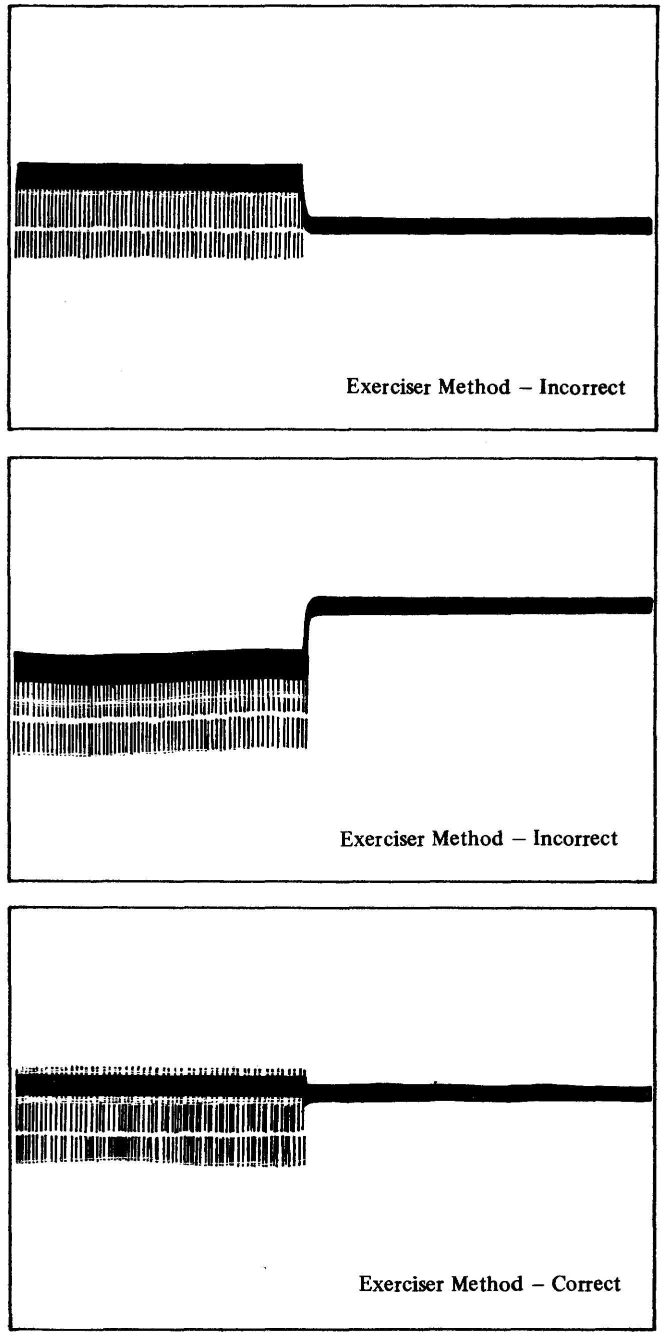


Figure 4-13. Phase Comparator Error Voltage

8. Use the exerciser and check that drive will run error-free. If not, go back to step 4 and re-check the adjustment.
9. Repeat steps 3 through 8 for the other drive in the cabinet. This will usually result in a slight difference in the oscilloscope trace, due to small variations in speed of the two spindles.
10. Fine adjust R198 such that the setting is an optimum for both drives in the cabinet.
11. Run MTR on both drives and ensure that no errors occur. USE KNOWN, GOOD, DISKS FOR TESTING.

PROCESSOR MTR METHOD

1. Insert a scratch cartridge and power up the drive.

NOTE
CARTRIDGE MUST BE INITIALISED.

2. Set up oscilloscope as follows:

Channel 1	T.P.13 on RWA board (SECTOR)
Channel 2	T.P.2 on CEM board (Phase comparator error voltage). Note: Use ground on CEM board. A.C.
Time base	0.2 milliseconds/cm.
Sync.	Internal positive, channel 1.
Mode	Alternate.

3. Using a suitable MTR option, write a pattern of all '0's on track 200.
4. Using a 'read-only' MTR option, perform a continuous read on the data just written, "ignore errors'.
5. Turn R198 fully counter-clockwise.
6. Adjust the oscilloscope triggering to obtain the signal shown in figure 4-14. The signal may not be precisely synchronized, but will be sufficient to observe the necessary comparison. Use the sector pulses to locate the period of 45-95uS when RD ENABLE is turned off. This represents the Error Voltage at the centre of the Phase Locked Loop.
The remainder of the signal is the Error Voltage obtained from the comparison of data and the VCO.
7. Slowly turn R198 clockwise, until the D.C. level of the two portions of the trace is the same; that is, the top of the trace must be a straight line, as in figure 4-14C.
8. Repeat this procedure for the other drive in the cabinet. The adjustment may be slightly different due to small variations in speed of the 2 spindles.
9. Fine adjust R198 such that the setting is an optimum for both drives in the cabinet.
10. Run a suitable write/read MTR, and check that both drives run error-free.

USE KNOWN GOOD DISKS AND CHECK COMPATIBILITY BY SWAPPING DISKS BETWEEN DRIVES.

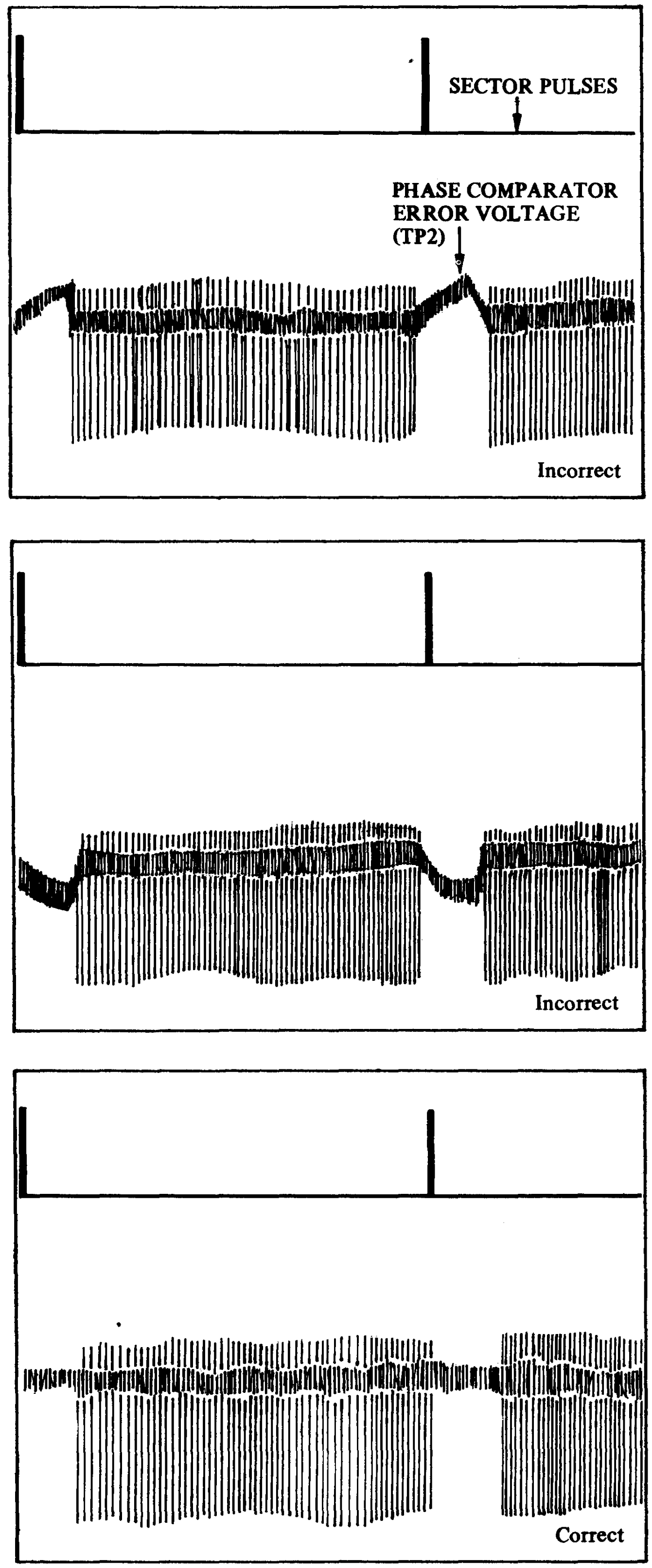


Figure 4-14. Data Discriminator Set-Up Using Processor

9481-12 TESTS AND ADJUSTMENTS

POWER SUPPLY VOLTAGES

Using the D.V.M., check the power supply voltages in accordance with table 4-2.

Table 4-2. Power Supply Voltages

VOLTAGE	TEST POINT	POT TO ADJUST	TOLERANCE
+5V	C37 C.E.M. (+side)	R24 P.S. board	±0.1V
−20V	C39 C.E.M. (−side)	R15 P.S. board	±0.4V
+20V	C38 C.E.M. (+side)	R6 P.S. board	±0.4V
+36V *	C3 P.A.M. (+side)	Fixed	±5.0V
−36V *	C4 P.A.M. (−side)	Fixed	±5.0V

(* use T.P.2. as ground)

Check the following voltages on the Temperature Compensation board, using the D.V.M.

a. +15±0.75V at large solder pad test point
b. −15±0.75V at large solder pad test point.

SECTOR AND INDEX

INDEX PULSE

1. Install a scratch cartridge and power-up the drive.
2. Set up oscilloscope as follows:

Channel 1	T.P.18, Read/Write board 2V/cm.
Time base	5 milliseconds/cm.
Sync	Channel 1, negative.
Mode	Channel 1 only

3. Check that the interval between INDEX pulses is 40±0.5 milliseconds, in accordance with figure 4-15.

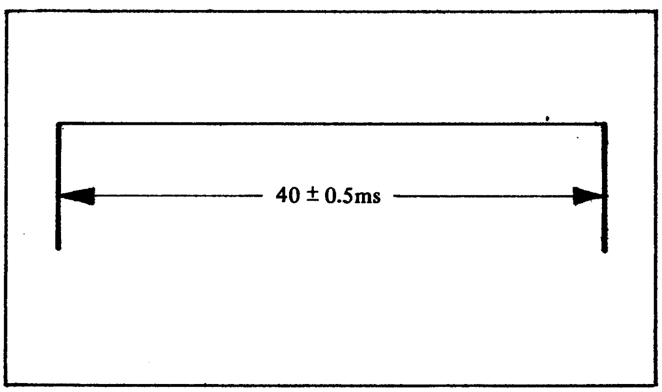


Figure 4-15. INDEX Pulse

SECTOR PULSE

1. Set up oscilloscope as follows:

Channel 1	T.P.8, Read/Write board 1V/cm.
Time base	5 milliseconds/cm.
Sync	External negative on INDEX (T.P.18 on Read/Write board)
Mode	Channel 1 only

2. Observe the SECTOR pulses as shown in figure 4-16, and count them. There should be 32, between the INDEX pulses.
3. Each SECTOR pulse and the INDEX pulse must have a minimum peak-to-peak amplitude of 2.2V and a maximum peak-to-peak amplitude of 4.0V.

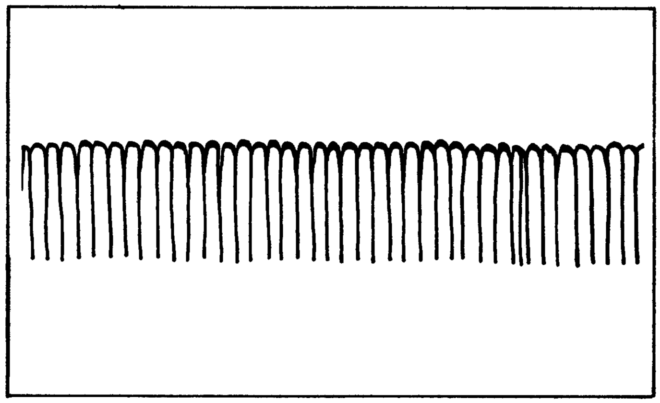


Figure 4-16. SECTOR Pulses

4. If any SECTOR pulse is less than 2.2V, then check:
   a. Cartridge hub slots for blockages.
   b. Transducer photo-cell for partial masking with black paint. If so, carefully remove the paint until a satisfactory output is obtained.
   c. If an improvement cannot be obtained as in a. through b. above, then the Sector Transducer must be replaced.

IF THE SECTOR TRANSDUCER OUTPUT IS INSUFFICIENT,THE DRIVE WILL GIVE SEEK ERRORS AND/OR UNCOMMANDED HEAD RETRACTS.

5. If any SECTOR pulse is greater than 4.0V, this may be corrected by carefully using black paint to mask off an uninterrupted line across the top of the transducer photo-cell.

IF THE SECTOR TRANSDUCER OUTPUT IS EXCESSIVE, THE HEADS MAY FAIL TO RETRACT AT THE CORRECT TIME DURING POWER-DOWN, OR THE HEADS MAY LOAD BACK ONTO THE DISK WHEN SECTOR PULSES SLOW TO 40mS APART.

WRITE CURRENT

1. Set up oscilloscope as follows:

Channel 1	One side of R35, Read/Write board 1V/cm.
Channel 2	The other side of R35. INVERTED. 1V/cm.
Time base	10 milliseconds/cm.
Mode	Added.

2. Install a scratch cartridge and power-up the drive.
3. Using exerciser, run box, or processor, write a continuous all '0's pattern.
4. Obtain the trace shown in figure 4-17. The peak-to-peak amplitude must be 3.9V±0.1V. Adjust R25 on the Read/Write board as necessary.

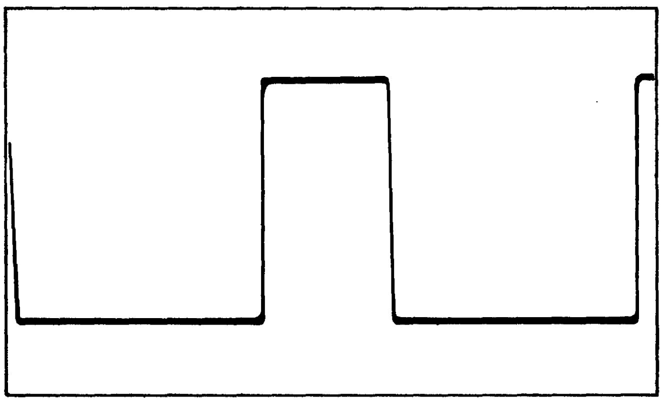


Figure 4-17. Write Current

CLEANING CARRIAGE GUIDE AND LINEAR POT (Refer to figure 4-18)

NOTE
THIS IS A PREREQUISITE TO PERFORMING THE DETENT, SERVO AND HEAD ALIGNMENT PROCEDURES

1. Power down the drive, remove any cartridge which may be present, and turn off ac power.
2. Remove the Cartridge Door Opener Bail. Note: This is necessary to prevent damage to the heads.
3. Place a folded Texwipe pad between the heads.
4. Remove the Servo Plug, P/J4.
5. Disconnect the Magnet Shield (if present), by unscrewing the two screws securing the flexible circuit bracket. Replace the bracket and the two screws.
6. Using Texwipes, Cotton Buds and Isopropyl Alcohol, carefully clean the carriage rails and linear pot. Take great care not to damage the Wiper. Ensure complete, free, unrestricted

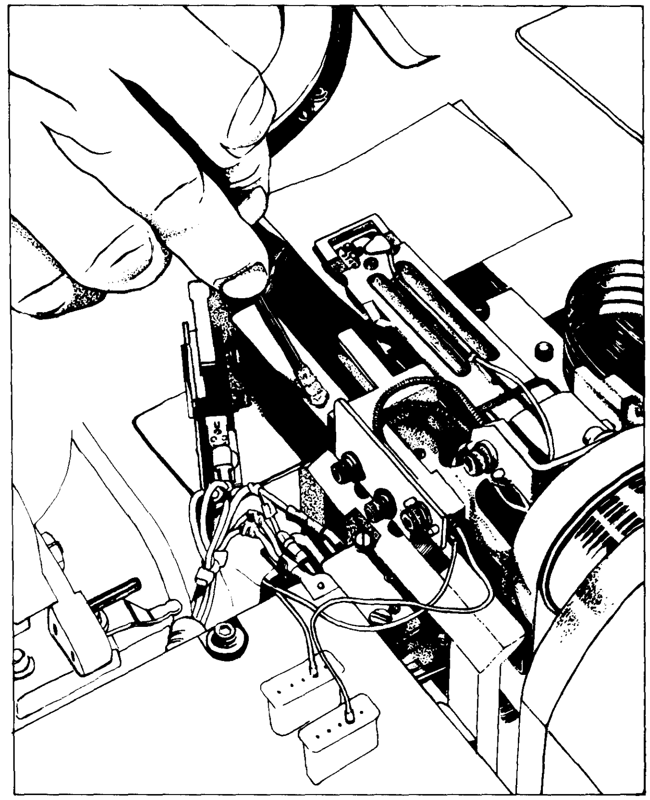


Figure 4-18. Cleaning Carriage Guide and Linear Pot

movement of the carriage over the total Guide length. Do not forget to clean the underneath surfaces.

7. Visually check that the Wiper is correctly positioned on the Linear Pot, that is, in the center of the track, and is undamaged.

DETENT, SERVO ALIGNMENT AND SERVO RESPONSE

DETENT AMPLIFIERS

1. Turn off ac power.
2. ENSURE THE CARTRIDGE DOOR OPENER BAIL IS REMOVED.
3. Check that the Servo Plug, P/J4 is disconnected, and that the Texwipe pad is still in place between the heads.
4. Disconnect P/J20 on the SCM-2 board. (This removes the input to the detent amplifiers).
5. Turn on ac power.
6. On the SCM-2 board, use the D.V.M. to monitor the test points shown in table 4-3. In sequential order, adjust the relevant pot for 0±5mV.
7. Turn off ac power, and re-connect P/J20.
8. Set up oscilloscope as follows:

Channel 1	T.P.1 on SCM-2 board 500mV/cm.
Time base	10 milliseconds/cm.
Sync	Internal positive.
Mode	Channel 1 only

Table 4-3. Detent Amplifier Balance

TEST POINT:	1	2	3	4	5	6	7	8
POT TO ADJUST:	R5	R22	R10	R27	R15	R33	R20	R39

NOTE

These are initial adjustments only. Final alignment is performed in the Temperature Compensation and Head Alignment.

9. Turn on ac power.
10. While manually moving the carriage back and forth, check for a minimum signal amplitude of 2.0V peak-to-peak, over the entire range of the carriage. If variation is greater than ±15%, re-align the mask to transducer assembly. (Technical Manual, Section V.
11. Check that the signal obtained in step 10 above, has an equal swing above and below 0 volts. Adjust R5 on the SCM-2 board if necessary.
12. Manually return the carriage to the home position and turn off ac power.
13. Re-connect the Servo Plug, P/J4.

SERVO ALIGNMENT

1. Install the Test Hub and override the Cartridge Interlock Microswitch (for example, with a cardboard strip).
2. Ensure that the Texwipe pad is in place between the heads.
3. Disable the Temperature Compensation Network by installing a jumper between T.P.4 and T.P.11 on the Temperature Compensation board. (This grounds DENA.)
4. Turn on ac power.
5. Using the D.V.M., monitor T.P.8 and adjust R149 on the SCM-1 board for 0±100mV. (This is an initial setting only, to ensure the heads will load).
6. Power-up the drive. When the heads are loaded, jumper to ground the end of R152 opposite T.P.15 on the SCM-1 board. (This is to force the drive into DETENT mode while performing the Positioner Coil adjustment).
7. Insert the Servo Coil Positioning Gauge between the magnetic and the rear of the carriage assem bly, as in figure 4-19.

NOTE

Gauge must be above rubber ring.

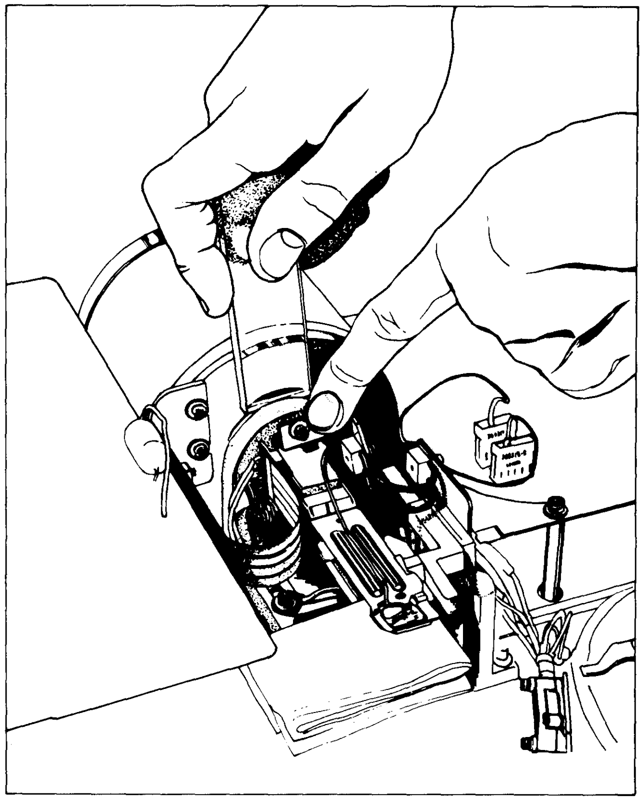


Figure 4-19. Positioner Coil Adjustment

8. Position the carriage assembly such that the gauge is a snug fit. Resistance will be felt as the carriage is moved against the detent, but this is of no consequence provided the jumper has been installed in step 6. Remove the gauge and allow the carriage to detent.
9. Using the D.V.M., monitor the voltage between TP0 (wiper terminal) on the SCM-1 board and ground.

NOTE

The Wiper tension must be correct.

10. Loosen the Linear Pot securing screws until they are just snug.
11. Using Position Transducer Adjustment Tool, re-position the Linear Pot until the reading at T.P.0 is −85±5mV.
12. Tighten the Linear Pot securing screws.

DO NOT OVER-TIGHTEN THE SCREWS – THIS CAN BREAK THE LINEAR POT.

13. Check that the Linear Pot connecting leads have not risen and fouled the carriage path. If so, tighten them by slackening the cable clamp and pulling the slack to the plug end.
14. Using the D.V.M., monitor the voltage at T.P.7 and adjust R47 on the SCM-1 board for 0±0.5mV.
15. Power down the drive and turn off ac power.
16. Remove the jumper installed in step 6.
17. Replace the Magnet Shield, if necessary.

NOTE

Ensure the Shield does not foul the carriage.

18. Turn on ac power and power up the drive. (Test Hub and Texwipe pad still in place).
19. Re-check the following and fine adjust as necessary.
   a. T.P.0 on SCM-1 board for −85±5mV at track 00. (Linear Pot position).
   b. T.P.7 on SCM-1 board for 0±0.5mV (R47).
20. Using exerciser, run box or processor, step the positioner out one track at a time, and monitor the voltage at T.P.7 with the D.V.M.
   - Track 00 must be 0±0.5mV.
   - Tracks 01 through 405 must be 0±14mV.

   Adjust R39 and R47 on SCM-1 board and repeat as necessary until an optimum setting has been obtained for all tracks.

SERVO RESPONSE

NOTE

Steps 2 through 4 are optional.

1. Turn off ac power.
2. Remove the SCM-2 board and drill a 1/4" diameter hole at the point shown in figure 4-20, exactly above R133 on SCM-1 board. Take great care not to damage any components, and ensure that the hole only passes through the ground plane etching.
3. Solder a test point onto I.C.15, pin 5 on SCM-1 board.
4. Re-install the SCM-2 board.

NOTE

The work carried out in steps 2 and 3 will greatly facilitate the adjustments in this section, and eliminate the need for the SCM-2 Extender Kit.

5. Power up the drive. (Test hub and Texwipe pad still in place).
6. Set up oscilloscope as follows:

Channel 1	Test point on I.C.15, pin 5, SCM-1 board. 2V/cm.
Time base	5 milliseconds/cm.
Sync	Internal negative.
Mode	Channel 1 only.

7. Set exerciser or processor to alternately seek tracks 00 and 01.
8. Obtain the signal shown in figure 4-21, and by inserting an insulated screwdriver through the hole drilled in the SCM-2 board, adjust R133 on the SCM-1 board for a pulse width of 35±2 milliseconds.
9. Leave the oscilloscope connected as in step 6, but increase the time base to 10 milliseconds/cm.

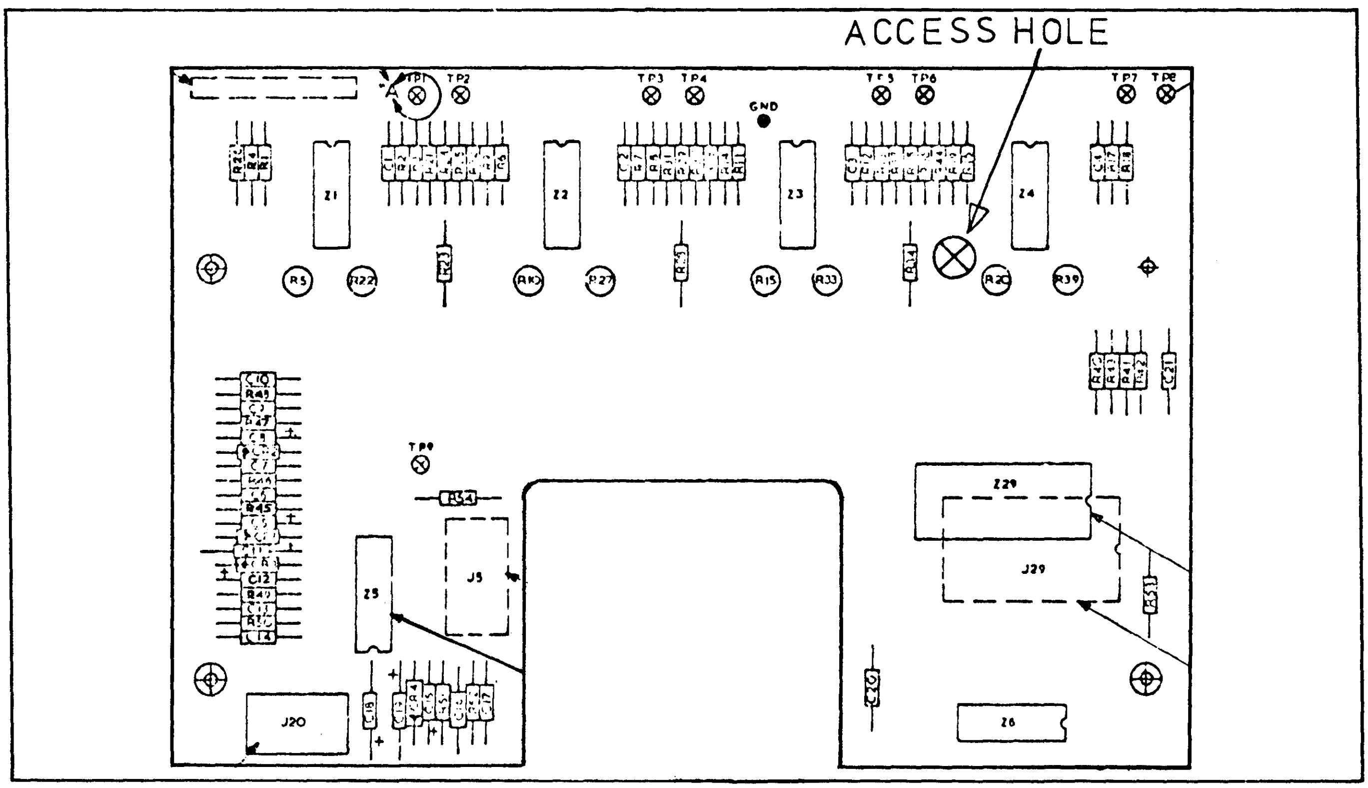


Figure 4-20. Location of Access Hole for R133 (SCM-2 board)

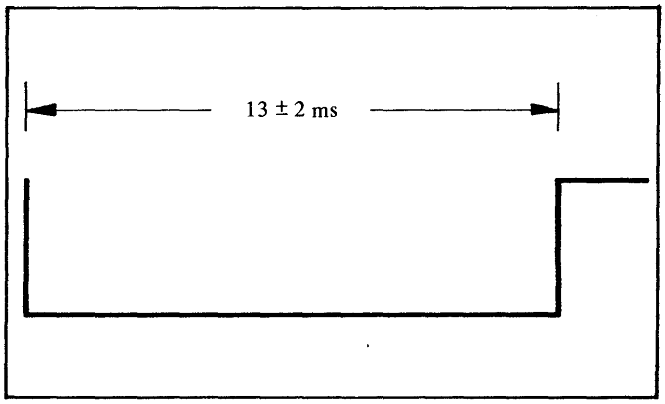


Figure 4-21. Short Servo Gate.

10. Set the exerciser or processor to seek alternately between tracks 00 and 405.
11. Obtain the trace shown in figure 4-22. Move the positive-going edge to coincide with the center graticule. Switch in the X10 magnifier.

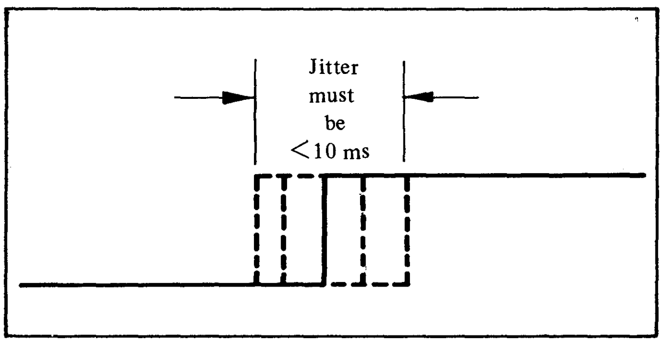


Figure 4-22. Long Servo Gate Jitter

12. Adjust R65 on the SCM-1 board to give minimum jitter, that is, less than 10 milliseconds.
13. Switch out the X10 magnifier on the oscilloscope, and reset the horizontal position to normal.
14. Adjust R66 on the SCM-1 board to give a pulse width of 100±5mS, as shown in figure 4-23.

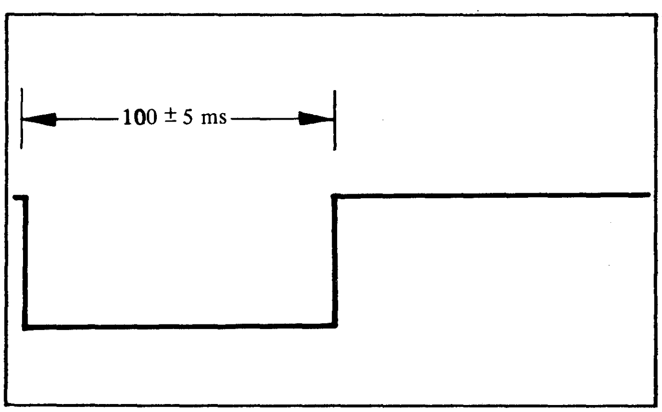


Figure 4-23. Long Servo Gate – Width

15. Set up oscilloscope as follows:

Channel 1	T.P.5 on SCM-1 board. 50 millivolts/cm.
Time base	5 milliseconds/cm.
Sync	External negative, I.C.15 pin 5 on SCM-1 board
Mode	Channel 1 only.

16. Set up exerciser or processor to seek alternately tracks 00 and 01.
17. Obtain the trace shown in figure 4-24. This signal is the output from the Detent Amplifier Circuits. As the positioner locates itself over the desired track, an overshoot occurs as the servo goes into DETENT. This overshoot is then compensated for by amplified feedback from the detent circuits, and the carriage therefore oscillates slightly for a period of time. It is important that this 'settle time' should be minimised, as excessive carriage oscillation can cause errors.
18. Adjust R23 on the SCM-1 board for the minimum overshoot within 10 milliseconds. After 35 milliseconds, no overshoot should exceed ±50mV.

NOTE

The first big overshoot (which can be positive or negative) should be ignored.

19. Set exerciser or processor to seek sequentially from track 00 through track 405. Ensure that the settle time remains within ±50mV before 35 milliseconds. Re-adjust R23 if required.

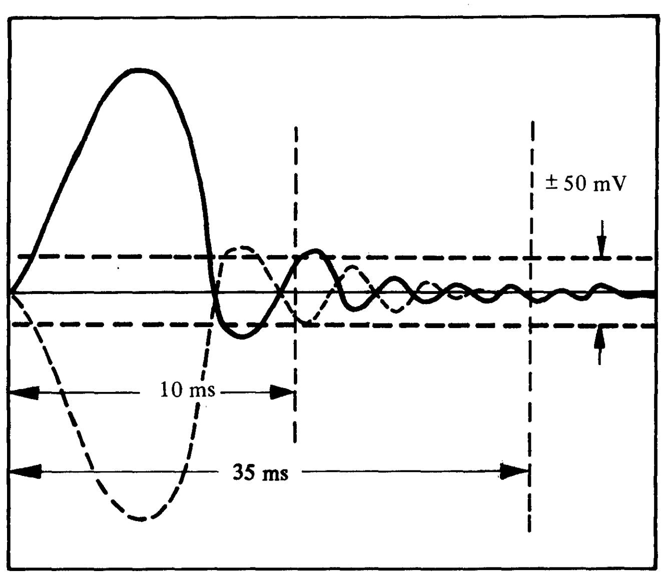


Figure 4-24. Servo Settle Time

20. With the exerciser or processor set to seek alternately between track 00 and track 01, move channel 1 of the oscilloscope to T.P.9 on the S.C.M. board.

21. Connect the oscilloscope ground lead to the ground test point on the SCM-2 board.
22. Use the oscilloscope switch to ground channel 1, and adjust the trace to the center graticule line. Extend the time base to 10 milliseconds/cm.
23. Set exerciser or processor to seek alternately tracks 00 and track 405.
24. Switch the oscilloscope to 100mV/cm.
25. The oscilloscope will now show both the forward and reverse long seeks. The object of this adjustment is to ensure that there is minimum offset voltage input to the PAM board. Since the offset can be different for forward and reverse seeks, the adjustment is only correct when the trace is obtained as shown in figure 4-25b.

Fine adjust R149 on SCM-1 board until the correct signal is obtained.

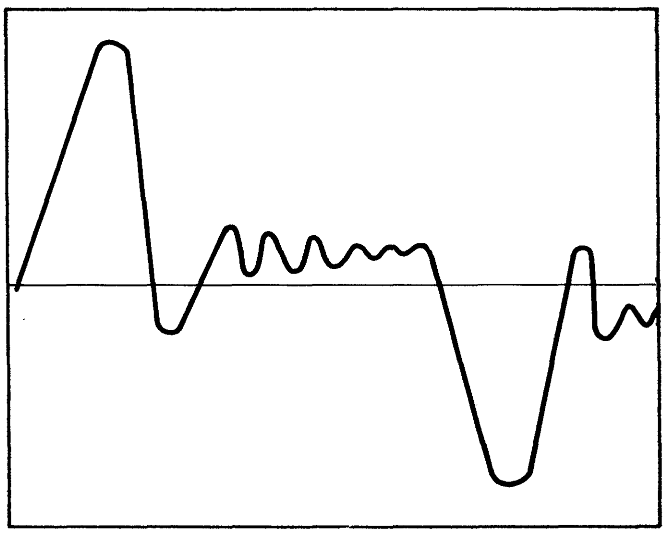


Figure 4-25a. Servo Offset Adjustment - Incorrect

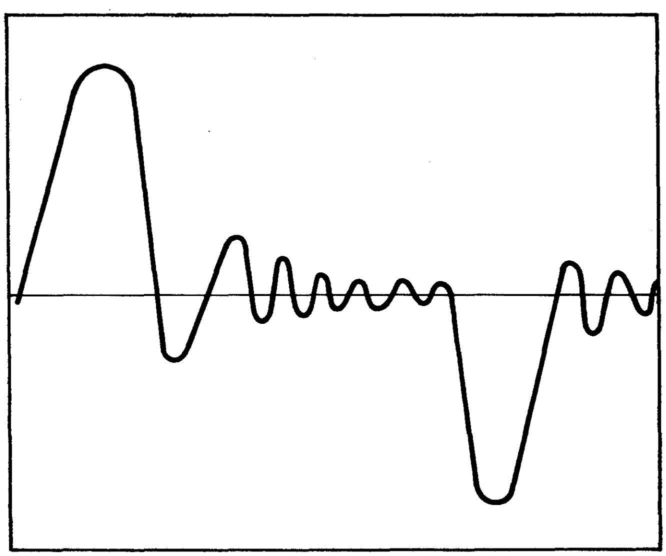


Figure 4-25b. Servo Offset Adjustment - Correct

26. Stop the exerciser or processor and position the heads at track 00.
27. Make a final check of the following, using the D.V.M.:
    a. T.P.0 (wiper terminal) for −85mV+5mV.
    b. T.P.7 for 0+0.5mV at track 00 (R47).
    c. T.P.7 for 0+14mV while accessing tracks 01 through 4-5 (R39).
28. Power down the drive and remove the test hub.
29. Remove the jumper from TP4/TP11 on temperature compensation board.
30. Remove the Texwipe pad from between the heads, and re-enable the cartridge interlock switch.
31. REPLACE THE CARTRIDGE DOOR OPENER BAIL.

TEMPERATURE COMPENSATION AND HEAD ALIGNMENT

EXPLANATION

Due to greater track density on the 9481-12, accuracy of head alignment is more critical than on the 9480-12. The head alignment can be accurately performed and should not drift provided the temperature stays constant. If the temperature changes, however, the mechanical components in the drive will expand or contract, causing the head alignment to have an unacceptable offset. It is for this reason that the Temperature Compensation Network was added (LIN 4392-004). This measures the temperature of the baseplate and air flow in the vicinity of the heads, and injects a compensating voltage to the servo to cancel out any offset induced by mechanical expansion or contraction.

The temperature at which the heads are aligned is not critical (provided it is not too extreme), but it is important that it should be stable. At this point offset from the Temperature Compensating Network to the servo should be zero; if later the temperature does change, however, a compensating offset voltage must be supplied.

With this in mind, the adjustments have been simplified to eliminate the need for a thermometer.

The procedure consists of first allowing the drive temperature to stabilise, and then disabling the Temperature Compensation Network and aligning the heads. The Temperature Compensation is then re-enabled, and any offset present zeroed out on the Temperature Compensation Board.

Fine adjustment can then be applied by adjusting the Detent Amplifiers.

METHOD

1. Remove all case panels (skins) from the unit.
2. Check that the jumper has been removed from

T.P.4/T.P.11 on the Temperature Compensation board.

3. CHECK THAT THE ALIGNMENT CARTRIDGE WRITE LOCKOUT PLUG IS PUSHED IN AND LOCKED.
4. Insert the Alignment Cartridge into the drive to be checked, and a scratch cartridge in the other drive.
5. Power up both drives, and leave the heads positioned at track 00.
6. Leave the drives to warm up for at least 30 minutes.
7. Monitor T.P.3 on the Temperature Compensation board with the D.V.M.

NOTE

At this point, the Temperature Compensation is still enabled and the voltage at T.P.3 is free to change relative to the change in temperature of the baseplate.

8. Observe the change of voltage at T.P.3. The change must not be greater than 0.5mV per minute. If it is, the drive must be left longer for the temperature to stabilise.
9. When the voltage at T.P.3 is stable, adjust R1 on the Temperature Compensation board for 0+0.5mV.
10. Jumper together T.P.4/T.P.11. on the Temperature Compensation board. (Thus disabling the Temperature Compensation Network).
11. Connect oscilloscope as follows:

Channel 1	T.P.15 on Read/Write board 10mV/cm.
Channel 2	T.P.16 cm Read/Write board 10mV/cm. ac INVERTED
Time base	5 milliseconds/cm.
Sync	External negative, T.P.18 on Read/Write board (INDEX)
Mode	Added.

12. Position the heads at track 164, and condition exerciser, run-box, or processor, to read continuously, "ignore errors".
13. Observe the Dibit patterns shown in figure 4-26. There should be two distinct signals one overlapping the other, with a minimum of fringe area. The areas of overlap should be averaged out to compensate for spindle runout.
14. Perform steps 12 and 13 for both heads. If both heads are correctly aligned, ignore steps 15 through 23 and proceed straight to step 24.
15. If either head is out of alignment, then proceed as follows.
16. Slacken off the Head Locking Screw and turn the Head Alignment Screw 6 turns counter-clockwise.

NOTE

Take great care to avoid shorting of components. Use well-insulated tools to adjust these screws.

17. Manually pull the head towards the Positioner Coil until it is snug.
18. While observing the scope trace, slowly turn the Head Adjustment Screw clockwise, until the Dibit pattern appears on the screen.
19. Continue adjusting the head until the conditions in step 13 are met.
20. Tighten the Head Locking Screw to a torque of 8 in. lbs., using the Torque Wrench.

OVERTIGHTENING THE SCREWS CAN DAMAGE THE HEAD SHAFT AND CAUSE DIFFICULTY IN ALIGNMENT.

21. Make a final check thaat the alignment has not drifted due to tightening the screw. Fine adjust if necessary.
22. Slacken the Head Adjustment Screw 1/2 turn counter-clockwise to release pressure on the shaft.
23. Repeat steps 15 through 22, if necessary, for the other head.

NOTE

When experience has been gained, it may save time to adjust the heads as above, such that the alignment is approximate only. Both heads, however, must be accurately aligned to each other. Fine alignment may then be performed by adjusting the Detent Amplifiers.

24. When the heads are correctly aligned, make a final check that the voltage at T.P.3 on the Temperature Compensation board is not changing by more than 0.5mV per minute. Re-zero R1 if necessary.
25. Remove the jumper from T.P.4/T.P.11 on the Temperature Compensation board. (The Temperature Compensation Network is now enabled).
26. Observe the Dibit pattern on the oscilloscope. If it has changed due to removing the jumper in step 25, then correct the alignment by adjusting R2 on the Temperature Compensation board.
27. With the oscilloscope still set up as before, use the exerciser, run box, or processor to position the heads on the tracks given in table 4-4 below. Perform a continuous read ("ignore errors") on each track in sequential order, and observe the Dibit pattern. Adjust the relevant pot on the SCM-2 board to give accurate alignment of the heads for each detent phase.

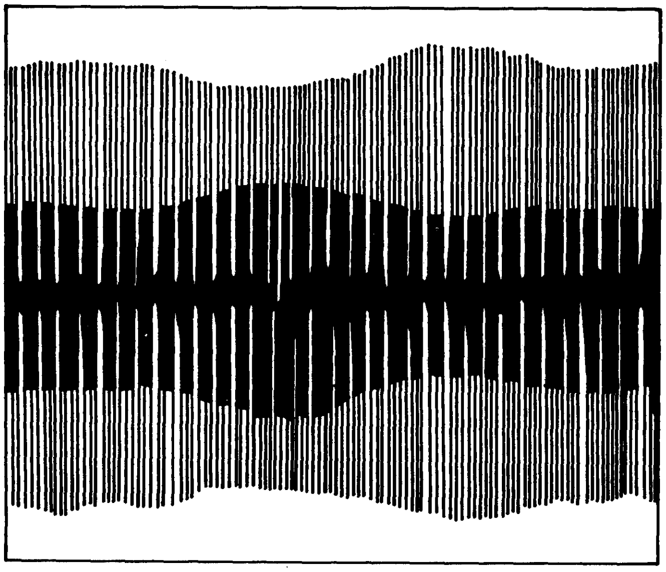


Figure 4-26a. Dibit Patterns - Head Alignment - Incorrect

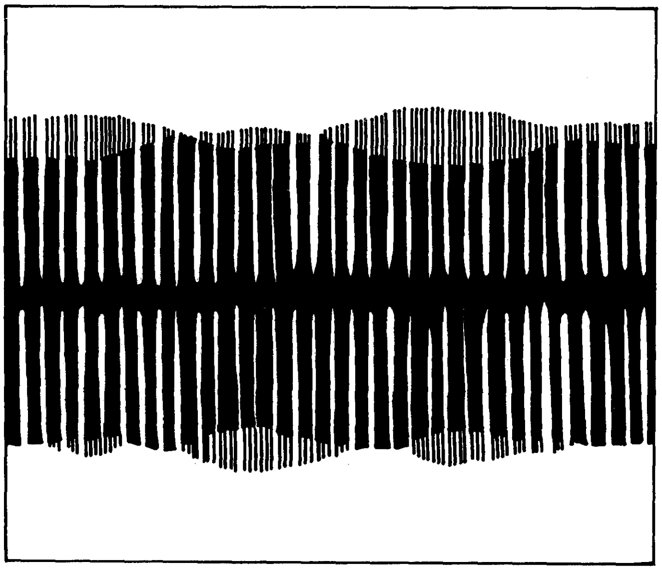


Figure 4-26b. Dibit Patterns - Head Alignment-Correct

Table 4-4. Detent Phase Alignment

TRACK	PHASE	ADDRESS BITS TO ENABLE	POT TO ADJUST
164	A	128, 32, 4	R5
200	$\overline{A}$	128, 64, 8	R22
230	B	128, 64, 32, 4, 2	R10
98	$\overline{B}$	64, 32, 2	R27
45	C	32, 8, 4, 1	R15
65	$\overline{C}$	64, 1	R33
23	D	16, 4, 2, 1	R20
131	$\overline{D}$	128, 2, 1	R39

The 'A' phase adjustment should be kept to a minimum, as it is used as a reference.

28. Re-check the following adjustments:
    a. Error voltage. T.P.7 on the SCM-1 board must be 0±0.5mV for track 00, and 0+14mV for tracks 01 through 405. Fine adjust R47 or R39 respectively on SCM-1 board if necessary.
    b. Linear Pot. T.P.0 on the SCM-1 board must be −85±5mV.
29. Leave the oscilloscope still set up as in step 11, but alter the time base to 5uS/cm.
30. Position the heads at track 190, and perform a continuous read, "ignore errors".
31. Adjust R55 on the Read/Write board such that the period from INDEX to data burst is 30±5uSecs as in figure 4-27.

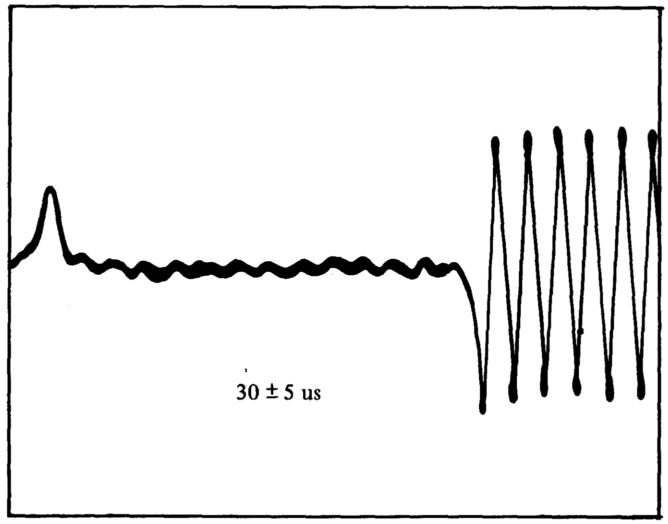


Figure 4-27. INDEX-to-Data Burst (Radial Alignment)

32. Repeat for both heads and ensure they both fall within the tolerance of ±5uSecs.
33. Re-position the heads at track 10, and perform a continuous read, "ignore errors".
34. Re-check INDEX-to-data-burst timing. Both heads must be within a tolerance of ±8uSecs, of the adjustment value at track 190.

NOTE

a. If R55 adjustment is insufficient, the Sector Transducer must be repositioned.
b. If heads cannot be brought within ±8uSecs., head replacement should be tried. If this also fails, then the carriage assembly must be replaced.

35. Power down the drive and remove the alignment cartridge.
36. Check the head load cam adjustment, as per Section V, page XX of the Technical Manual.
37. Check the home position microswitch for correct adjustment.
38. If no other adjustments are to be checked (such as the data discriminator), then replace the case panels (skins) and run a suitable

"write/read" MTR on both drives. Use only known, good, disks and ensure no errors occur.

39. Swap the disks over between the drives, and run a "read-only" option of the MTR.
40. If errors occur, the adjustments should be rechecked on both drives, as there may be a compatibility problem.

DATA DISCRIMINATOR

EXPLANATION

The Data Discriminator consists of a Voltage Controller Oscillator (VCO), a Phase Comparator, and the Discriminator proper. The VCO and the Phase Comparator form a Phase-Locked-Loop, and it is this section which must be aligned.

Suitably amplified and shaped data pulses are fed to one part of the Phase Comparator, and the output from the VCO to the other. If there is a phase difference between the VCO and the data, the Phase Comparator detects this, and develops an Error Voltage which is used to increase or decrease the frequency of the VCO. (This is the signal which is monitored at T.P.2 on the CEM board). By this means, synchronization is maintained between the clock frequency (VCO) and the data frequency, thus compensating for local differences in disk rotation, etc.

When the signal READ ENABLE is false, both inputs to the Phase Comparator are disabled, and the Error Voltage will depend only on the bias applied to the transistors. At this point, the Error Voltage represents the centre of the tracking range of the Phase Locked Loop.

When READ ENABLE is true, the Phase Comparator will compare the data and the clock (VCO). The set-up consists of adjusting the Error Voltagew thus obtained, such that this too is at the centre of the tracking range of the Phase Locked Loop. When this is done, the VCO will be running at the same average frequency as the data coming from the disk, at the optimum point in the tracking range.

This ensures the best possible starting point for the Phase Locked Loop to adjust itself to minor changes in data frequency, thus providing optimum clock-to-data strobing.

it is essential to make this adjustment as accurately as possible. If this is not done, a localised transient condition can push the Phase Locked Loop outside its accurate tracking range, thus inducing a strobing error, even though the drive appears to read most of the data error-free.

Such a reduction in margins can lead to intermittent and hard-to-find errors.

From this explanation, it can be seen that in order to correctly align the Phase Locked Loop, it is necessary to display the Error Voltage with READ ENABLE false, and to compare it with the Error Voltage when READ ENABLE is true. The dc levels of the two states can then be adjusted to be the same using R198 on the CEM board.

The Model 900 Exerciser is suitable for this set-up, since it reads 6 sectors at the beginning of a track, and then switches off. By displaying about 12 sectors, therefore, the two dc levels can be observed and compared.

If a processor MTR is used it is necessary to read at least 2 sectors of an initialised disk. When the processor receives a SECTOR pulse, READ ENABLE is switched off for about 45-95 uSec. It is therefore necessary to locate a SECTOR pulse, observe this "switch-off" time and compare the dc level with the remainder of the sector being read.

A run-box is not suitable, as this reads a complete track of data without switching off READ ENABLE.

For these reasons, separate procedures are given for the Exerciser, or processor MTR.

EXERCISER METHOD

1. Insert scratch cartridges in both drives and power them up.
2. Connect oscilloscope as follows:

Channel 1	T.P.2 on CEM board (Ground on CEM board) 10mV/cm ac
Time base	2 milliseconds/cm.
Sync	Internal negative
Mode	Channel 1 only.

3. Write a pattern of all '0's on one track using the exerciser.
4. Turn R198 on the CEM board fully counterclockwise. (This is because there is a second position to which R198 can be adjusted, which gives the correct oscilloscope trace, but will in fact give errors).
5. Set the exerciser to perform a continuous read on the track just written in step 3, with the "ignore error" switch 'on'.
6. Observe the traces shown in figure 4-28. The first portion of the trace is when the exerciser is reading, and is therefore the Error Voltage obtained from comparing the VCO with the data (with an ac component). During the second portion, the exerciser has switched off and this is the Error Voltage obtained with the Phase Locked Loop at the centre of its tracking range.
7. Adjust R198 until the dc level of the two signals is at the same point; that is, the top of the trace must be a straight line, as in figure 4-28C.
8. Use the exerciser and check that the drive will run error-free. If not, go back to step 4 and recheck the adjustment.

9. Repeat steps 3 through 8 for the other drive in the cabinet. This will usually result in a slight difference in the oscilloscope trace, due to small variations in speed of the two spindles.
10. Fine adjust R198 such that the setting is an optimum for both drives in the cabinet.
11. Run MTR on both drives and ensure that no errors occur.
USE KNOWN, GOOD, DISKS FOR TESTING, AND SWAP THE DISKS BETWEEN THE DRIVES TO CHECK COMPATIBILITY.

PROCESSOR MTR METHOD

1. Insert a scratch cartridge and power-up the drive.

NOTE
CARTRIDGE MUST BE INITIALISED.

2. Set up oscilloscope as follows:

Channel 1	T.P.13 on RWA board (SECTOR)
Channel 2	T.P.2 on CEM board (Phase comparator error voltage) Note: Use ground on CEM board. ac
Time base	0.2 milliseconds/cm.
Sync	Internal positive, channel 1
Mode	Alternate.

3. Using a suitable MTR option, write a pattern of all '0's on track 00.
4. Using a 'read-only' MTR option, perform a continuous read on the data just written, "ignore errors".
5. Turn R198 fully counter-clockwise.
6. Adjust the oscilloscope triggering to obtain the signal shown in figure 4-28. The signal may not be precisely synchronized, but will be sufficient to observe the necessary comparison. Use the sector pulses to locate the period of 45-95uS when RD ENABLE is turned off. This represents the Error Voltage at the centre of the Phase Locked Loop. The remainder of the signal is the Error Voltage obtained from the comparison of data and the VCO.
7. Slowly turn R198 clockwise, until the dc level of the two portions of the trace is the same; that is, the top of the trace must be a straight line, as in figure 4-28C.
8. Repeat this procedure for the other drive in the cabinet. The adjustment may be slightly different due to small variations in speed of the 2 spindles.
9. Fine adjust R198 such that the setting is an optimum for both drives in the cabinet.
10. Run a suitable write/head MTR, and check that both drives run error-free.
USE KNOWN GOOD DISKS AND CHECK COMPATIBILITY BY SWAPPING DISKS BETWEEN DRIVES.

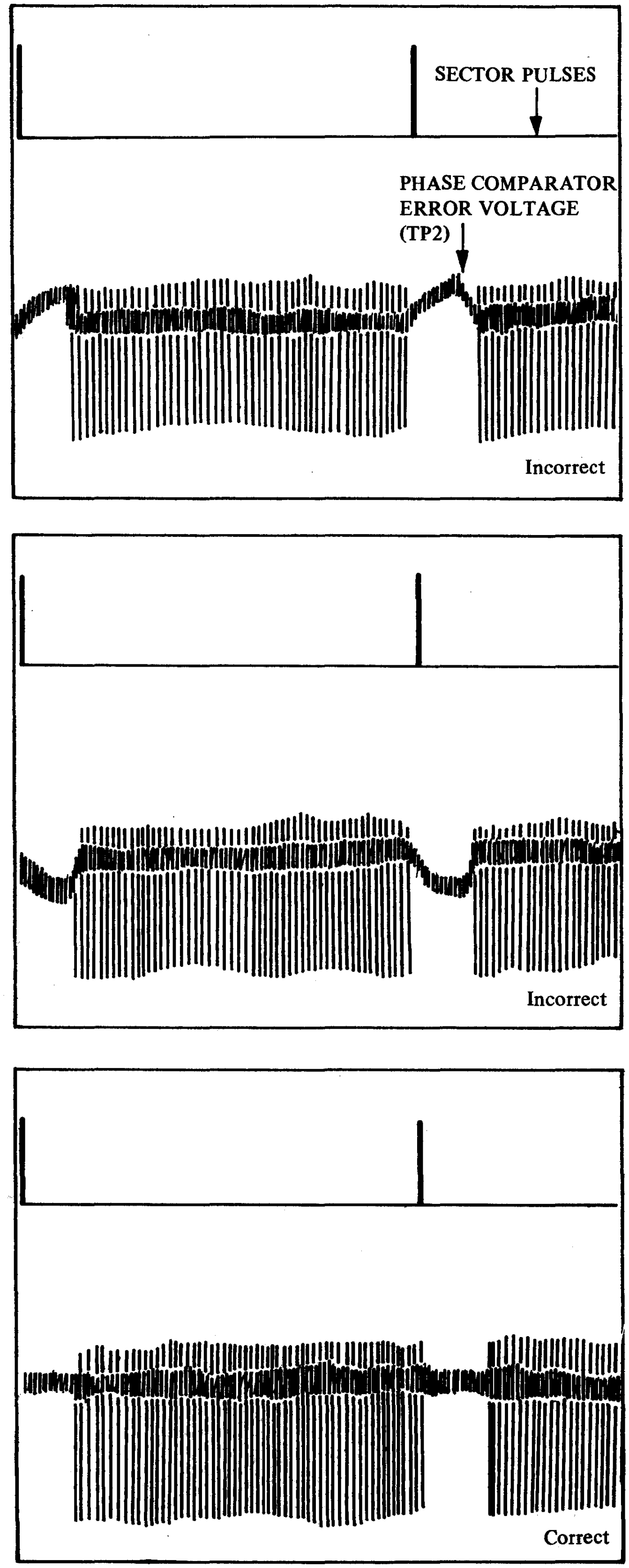


Figure 4-28. Data Discriminator Set-Up Using Processor

2. Switch on ac power, but do not power up the drive.

NOTE

At this point, there must be no read or write operation running on the drive. That is, the processor or exerciser should be halted. This allows the write clock to free-run.

3. Set up BDM 1250 as follows:

Probe	Test Point
A	IC21 Pin 6
FUNCTION : FREQUENCY	

4. The reading obtained will be the write clock frequency. Record this to 3 decimal places.
5. Disable the phase comparator by jumpering to ground IC30 Pin 10. This allows the read clock to free run.
6. Enable the read clock by jumpering TP6 to ground.
7. Move the BDM 1250 "A" probe to IC27 Pin 11. The reading obtained is the read clock frequency, without any feedback from the phase comparator.
8. Adjust R198 until the reading is the same as that obtained for the write clock, as recorded in step 4. This should be accurate to 3 decimal places.
9. Remove all jumpers.

A/B 9481-12 DCD TEST AND ADJUSTMENT PROCEDURE USING BDM 1250

EQUIPMENT REQUIRED

The following equipment is required to perform the tests and adjustments outlined in this section.

Description	Part Number
BDM 1250	
P6101 (Tektronix) Probe	
Exerciser or Run Box (as available)	
Cartridge Test Hub	
Scratch Cartridge	
Alignment Cartridge	2158 7308
Upper Head Removal Tool	1622 3489
Torque Wrench preset to 8 in.lbs.	
IC Pin Extenders	
Position Transducer Adjustment Tool	1622 3356
Texwipes	1622 3778
Isopropyl Alcohol	1624 9294
"Freon TF"	
12" Socket Extension	1623 0740
3/32" Hex Head Cap Screwdriver	1622 2903
7/64" Ball Driver	1622 3380
Trimpot Adjustment Screwdriver	1623 1185
Servo Coil Positioning Gauge	1622 3471
Jumper Leads	1622 1897

POWER SUPPLY VOLTAGES

1. Set BDM 1250 as follows:
   FUNCTION - DCV
   DISPLAY - NORM
   RANGE - AUTO
   Use DMM sockets/probes
2. Measure the power supply voltages as shown in table 4-6.

Table 4-6. Power Supply Voltages

Voltage	Test Point	Adjustment	Tolerance
+5V	C37 CEM (+side)	R24 PS board	± 0.1V
−20V	C39 CEM (−side)	R15 PS board	± 0.4V
+20V	C38 CEM (+side)	R6 PS board	± 0.4V
+36V	C3 PAM (+ side)	Fixed	± 5.0V
−36V	C4 PAM (−side)	Fixed	± 5.0V

3. Check the following voltages on the Temperature Compensation board:
   + 15 ± 0.75V at large solder pad test point.
   − 15 ± 0.75V at large solder pad test point.

INDEX AND SECTOR

1. Install a scratch cartridge and power up the drive.
2. Set up BDM 1250 as follows:

Probe	Test Point	Slope
A	RWA Board, TP14	Down
B	RWA Board, TP18	Up
C	RWA Board, TP18	Down
FUNCTION : TIME (B → C)		

3. Verify that the BDM 1250 reads 40 ± 0.5 milliseconds. (This is the period between 2 INDEX pulses).
4. Change FUNCTION switch to A COUNT (B→C).
5. Verify that the BDM reads 32. (Number of sectors).
6. Move the 'A' probe to TP8 on the RWA board.
7. Change to – Peak Mode.
   Verify that you have a minimum reading of 2.2V, and a maximum of 4.0V ± 0.5V. If the sector pulse voltage is less than 2.2V, check:
   a. Cartridge hub slots for blockages.
   b. Transducer photo-cell for partial masking with black paint. If so, carefully remove the paint until a satsifactory output is obtained.
   c. Position of transducer lamp. Carefully reposition the lamp to obtain sufficient output.
   d. If an improvement cannot be obtained as in a. through c. above, the sector transducer must be replaced.

   IF THE SECTOR TRANSDUCER OUTPUT IS INSUFFICIENT, THE DRIVE WILL GIVE ERRORS AND/OR UNCOMMANDED HEAD RETRACTS

   If the sector pulse voltage is more than 4.0V ± 0.5V, carefully use black paint to mask off an uninterrupted line across the top of the transducer cell to correct the condition.

   IF THE SECTOR TRANSDUCER OUTPUT IS EXCESSIVE, THE HEADS MAY FAIL TO RETRACT AT THE CORRECT TIME DURING POWER-DOWN, OR THE HEAD MAY LOAD BACK ONTO THE DISK WHEN THE SECTOR PULSES SLOW TO 40MS APART

WRITE CURRENT

1. Set up BDM 1250 as follows:

Probe	Test Point	Slope
A	RWA Board, R35	Up
FUNCTION : + V PEAK		

2. Install a scratch cartridge and power up the drive.
3. Using exerciser, run box, or processor, write a continuous all "0"s pattern.
4. Take the BDM readings on both sides of R35. The difference between the two readings should be 3.9V ± 0.1V.
5. Adjust R25 on RWA board if necessary.

CLEANING CARRIAGE GUIDE AND LINEAR POT

Refer to figure 4-4.

NOTE
This is a prerequisite to performing the detent, servo and head alignment procedures.

1. Power down the drive, remove any cartridge which may be present, and remove ac power.
2. Remove the Cartridge Door Opener Bail.

   NOTE
   This is necessary to prevent damage to the heads.
3. Place a folded Texwipe pad between the heads.
4. Disconnect the Servo Plug, P/J4.
5. Remove the Magnet Shield (if present), by unscrewing the two screws which secure the flexible circuit bracket.
6. Using Texwipe, Cotton Buds and Isopropyl Alcohol, carefully clean the carriage rails and linear pot. Take great care not to damage the Wiper. Ensure completely free and unrestricted movement of the carriage over the total Guide length. Do not forget to clean the underneath surfaces.
7. Visually check that the Wiper is correctly positioned on the Linear Pot, that is, on the center of the track, and is undamaged.

DETENT, SERVO ALIGNMENT AND SERVO RESPONSE

DETENT AMPLIFIERS

NOTE
If you are only checking adjustments, steps 2 through 7 may be omitted.

1. Ensure PJ/4 is disconnected and Texwipe pad is in place between heads.
2. Disconnect J20/P20 transducer plug from SCM-2. This removes the input to the detent amplifiers.
3. Switch on ac power.
4. Set up BDM 1250 to read dc volts. Connect ground lead to ground TP on SCM-2 board.
5. On the SCM-2 board, connect the positive voltage probe to the test points shown below. In sequential order, adjust the relevant pot for 0 ± 5mV.

Test Point	1	2	3	4	5	6	7	8
Pot to Adjust	R5	R22	R10	R27	R15	R33	R20	R39

Page 5-1 – 5-6 see PM PLAN

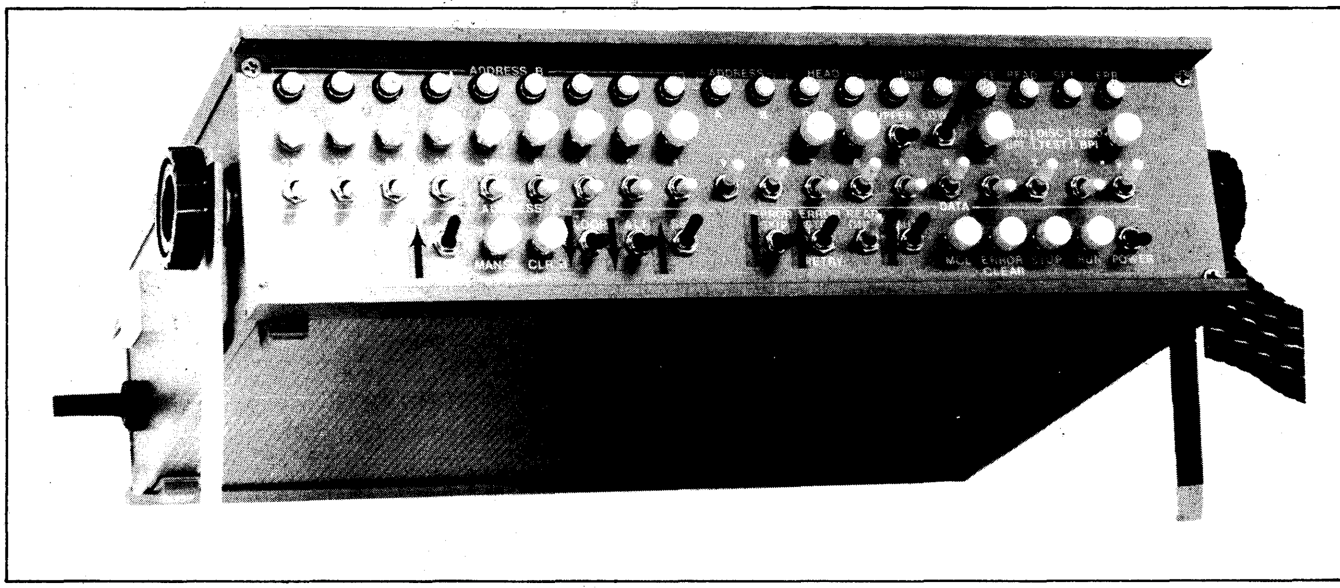


Figure 5-8. Model 900 Exerciser

of the internal conditions of the disk drive by the use of lighted indicators on the front panel.

SEEK MODES

1. Sequential – In this mode, the exerciser provides seek commands which position the Disk Drive in one-cylinder increments from cylinder 000 to cylinder 202 and in one step increments back to cylinder 000.
2. Alternate – In this mode, the exerciser provides seek commands which alternately position the disk drive between any A and B address.
3. SEQ/ALT – When Alternate and Sequential are used in conjunction with one another, the Exerciser provides seek commands which alternately position the disk drive from a designated A address to an advancing B address which is advancing in one-cylinder increments.

READ/WRITE, READ

For this mode, the Exerciser provides the capabilities of writing and reading or reading only, formatted in high density NRZ data.

CONTROLS AND INDICATORS

1. Power (toggle switch) – Switches the exerciser internal +5 VDC power on or off.
2. Upper/Lower (toggle switches) – These two switches can be used individually or together to select either the Upper, Lower or Both spindles.
3. Data (toggle switches) – These ten switches provide the desired data pattern.
4. Error Stop/Retry (toggle switch) – In Error Stop mode, the Exerciser data compare error register will stop on the first error encountered during sequential data comparison. In the Retry mode, the data compare register will keep retrying until data is compared.
5. Error Skip (toggle switch) – In this mode the Exerciser data compare is inhibited allowing it to ignore errors.
6. Read Only (toggle switch) – Provides write enable or read enable gating signals to the disk drive. When in the Write mode the Exerciser will send out write and read enable alternately. When in the Read Only mode the Exerciser will send out read enable only.
7. Auto (toggle switch) – Auto provides automatic sequencing of the operation selected after initiation. When not in Auto a manual step-by-step sequence is required by the operator to complete the operation selected.
8. Loop (toggle switch) – Allows Exerciser to repeat operation after final address is reached. When not in Loop the operation is completed upon reaching the final address.
9. TPI 100/200 (toggle switch) – To remain in the 100 TPI mode when used with a 9480 Unit. In this mode the B address register resets the circuit after cylinder 202.
10. Address A (toggle switches) – Binary coded switches from 1 to 256, used in conjunction with Alternate seek mode, provide the Exerciser with a designated A address from 000 to 202.
11. Address B (push buttons) – Binary coded switches from 1 to 256 are used to select any address from 000 to 202 for the B register.
12. Address A-B (lights) – Identifies whether A or B register is selected.
13. Address B (lights) – Provides binary readout of positioner location when B register is selected.
14. CLR B (push button) – Clears B register.

15. MANSK (push button) – Allows operator to do a seek opearation manually or when used in conjunction with address B pushbuttons allows operator to manually seek to any cylinder from 000 to 202.
16. Head 0/1 (lights) – When lit it indicates head selected.
17. Head 0/1 (pushbuttons) – Allows manual selection of either head.
18. Unit Upper/Lower (lights) – When lit indicates the unit selected, Upper or Lower. When both switches are in the up position the Upper and Lower units will be selected alternately.
19. Write (light) – When lit it indicates a write operation is being executed.
20. Read (light) – When lit it indicates a read operation is being executed.
21. Set (light) – When lit it indicates the positioner has settled on the selected cylinder.
22. ERR (light) – When lit it indicates either a data compare error or a positioner malfunction.
23. MCL (pushbutton) – Clears operation.
24. Error Clear (pushbutton) – Clears error condition.
25. Stop (pushbutton) – Stops operation.
26. Run (pushbutton) – Starts operation.
27. Disk Test 4400 BPI/2200 BPI (pushbuttons) – Used during a write or read operation to test the recovery of the VFO by decreasing its allowable lock up time to a selected value. NOT USED at the present time.

POWER REQUIREMENTS

All power to the Exerciser is provided by an internal +5 VDC power supply. An eight foot power cable is provided to plug into a 115/230 VAC, 50/60 Hertz power sources.

CARTRIDGE FLAWS

A cartridge flaw consists of an area of the disk where magnetic information cannot be stored. Examples of the causes of flaws are:

1. Oxide chipped or scratched.
2. "Pinholes" caused by small bubbles in the oxide.

Generally a flawed cartridge can be identified because it gives errors at the same address regardless of the drive on which it is run. However, some flaws may not be bad enough to fail on all drives. The following procedure allows a Field Engineer to examine the failed track with an oscilloscope in order to diagnose a flaw.

1. Select correct unit, head and seek to failing track (B 700 users use tests 22-25).
2. Trigger EXT –ve on Index (TP18 RW Card). Timebase 5ms/div.
3. CH1 on Data (TP15 RW Card) 50 mv/div AC.
4. CH2 on Sector and Index (TP13 RW Card) 2V/div.
5. Observe the complete revolution on TP15.

The amplitude observed depends on many things:

a. Bit packing density – due to increased bit packing towards the centre of the disk, the amplitude diminishes towards the centre. Also the data pattern affects bit packing density – zeros will appear bigger than ones. The preambles contain zeros – 32 preambles per revolution can generally be seen.
b. The head. Some heads may be unable to pick up high bit rates as well as low bit rates. The ratio of read back voltage of zeros to read back voltage of ones is the

read back voltage of ones

Attenuation Ratio. Attenuation Ratio should not be greater than 3 for any track. The flying height of the head also affects A.R.

c. The disk. The oxide coating may vary from disk to disk giving different amplitudes for different disks on the same head, track and data pattern.

The waveform seen over 1 complete revolution (40ms) is known as the envelope. An obvious flaw would appear as a dip in the envelope. See figure 5-9.

In other cases the flaw would be much smaller, in which case:

1. A intensified by B.
2. Delay out to failing sector (count sector pulse).
3. Display failing sector – check for flaws affecting only one or two bits.

The minimum acceptable readback voltage is 60 mv peak to peak at TP15.

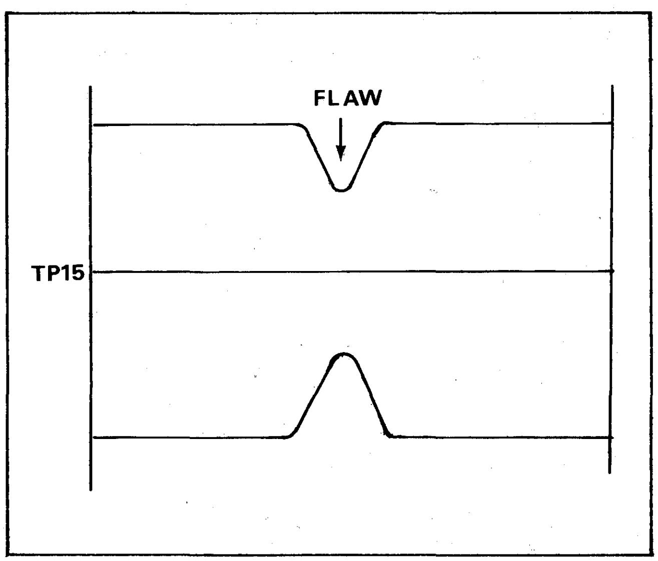


Figure 5-9. Disk Flaw

REPLACEMENTS AND ADJUSTMENTS

NOTE
The procedures given apply to both styles of drive, unless specific exceptions are stated.

CARRIAGE ASSEMBLY/POSITION TRANSDUCER/POSITION TRANSDUCER WIPER ASSEMBLY

Tools and Materials Required
1. 3/16" Allen wrench
2. 3/32" Allen wrench
3. 1/16" Allen wrench
4. 7/64" Allen wrench
5. Phillips screwdriver
6. Soldering iron
7. Head insertion/removal tool
8. Position transducer adjusting tool
9. Position transducer wiper adjusting tool
10. Detent shim

CARRIAGE ASSEMBLY/POSITION TRANSDUCER/POSITION TRANSDUCER WIPER ASSEMBLY REMOVAL

1. Initial set up.
   a. If STOP light is not lit then push STOP switch.
   b. Turn OFF main power by pushing switch S5.
   c. Remove necessary covers or pull Module out on rails to gain access.
   d. Disconnect Servo positioner plug P4/J4.
   e. Remove flexible circuit guide from servo positioner motor.

NOTE
Extreme care should be exercised as to not to crimp or kink flexible circuit strip.

2. Flexible circuit removal/replacement figure 5-10.
   a. If flexible circuit is to be replaced continue on, otherwise skip to Step 3.
   b. Remove flexible circuit from carriage assembly.

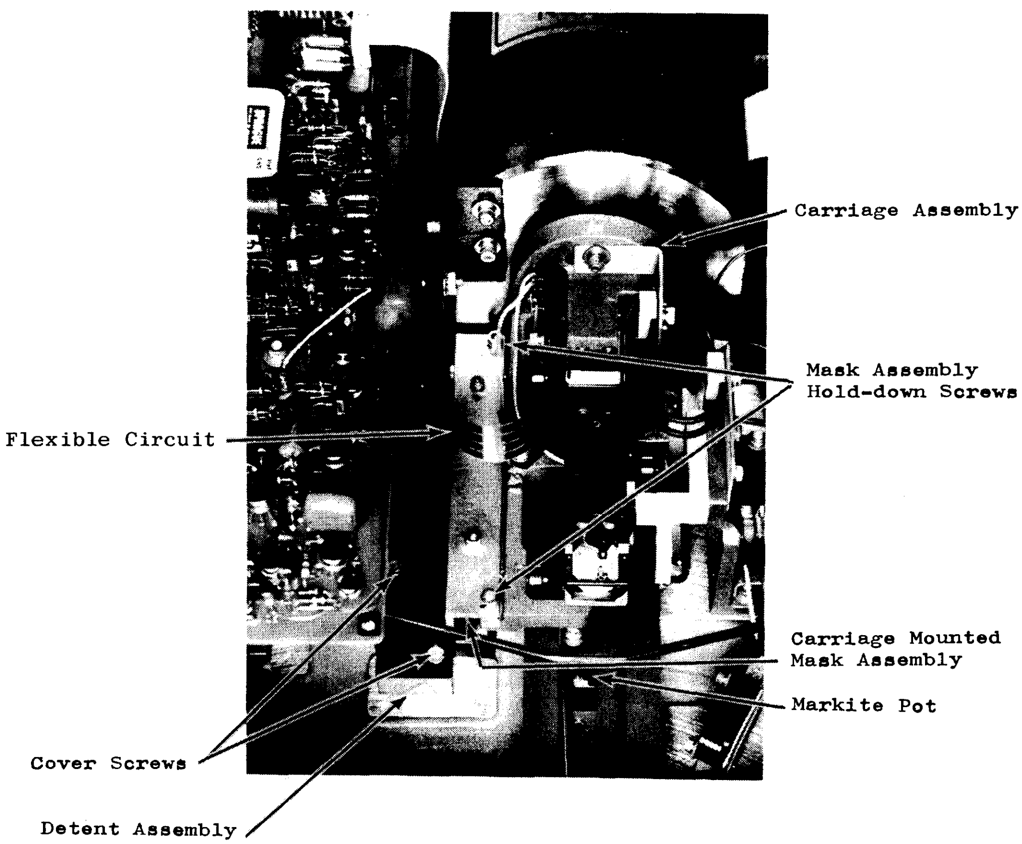


Figure 5-10. Detent Assembly

c. Unsolder three of the wires from the flexible circuit, the green wire is supplied with the new flexible circuit.
d. Solder wires to new flexible circuit, being sure that pins 3 and 4 have sleeving on them. Use Table 5-1 as a guide.

Table 5-1. Flexible Circuit Wiring

Pin 1	Wiper (White)
Pin 2	Ground (Green) furnished with assembly
Pin 3	Coil (White) sleeved
Pin 4	Coil (Copper) sleeved

e. Replace Flexible circuit on carriage assembly.
f. If Flexible circuit is the only thing to be replaced then go back to Step 1e and reverse the process to reassemble. Otherwise continue on.

3. Carriage Assembly Removal.
   a. Disconnect wire on SCM circuit board marked WPR.
   b. Loosen clamp that holds head leads in place, clamp does not have to be removed.
   c. Remove head leads from clamp.
   d. Loosen upper head position lock screw on carriage assembly.
   e. Insert head insertion/removal tool in place on upper head assembly. Figure 5-9.
   f. Hold carriage assembly in home position, depress button on tool and remove head assembly.
   g. Loosen lower head position lock screw.
   h. Slowly move carriage towards spindle to move lower head off of load ramp, continue moving carriage toward spindle until it stops.
   i. Grasp lower head arm assembly near carriage between thumb and index finger and remove head assembly.
   j. Loosen the two (2) hold down screws securing the mask assembly.

   WHILE HOLDING the mask assembly with one finger, remove the two hold down screws and then carefully remove the mask assembly.

   NOTE
   Mask assembly mounting fixture may be attracted by the magnet. DO NOT let go of assembly when removing mounting screws.

   k. Remove three (3) servo positioner motor screws.
   l. Carefully slide servo positioner motor straight back and set aside.
   m. Loosen wiper set screw in the carriage assembly and push wiper mounting block up into the carriage. Tighten set screw.
   n. Slide carriage assembly back off the rail, taking care not to damage the position transducer wiper arm and the flexible circuit assembly.

4. Position Transducer Strip (Markite) removal/replacement.
   a. If Markite is to be replaced continue on, otherwise skip to Step 5.
   b. Disconnect Plug P16 on the PAM circuit board.
   c. Remove two (2) cable tie downs.
   d. Remove two (2) mounting screws.
   e. Remove old Markite.
   f. Install new Markite with two (2) mounting screws.
   g. Position Markite towards servo positioner motor leaving the two mounting screws finger tight.
   h. Reconnect Plug P16 to PAM circuit board.
   i. Reconnect the two cable tie downs.
   j. If Markite is only thing to be replaced then go to Step 1a of Replacement Procedure.

5. Position Transducer Wiper Removal/Replacement.
   a. If Position Transducer Wiper is to be replaced continue on, otherwise skip to Step 6.
   b. Loosen hold down screw.
   c. Push wiper out of carriage.
   d. Remove wire from wiper and solder it to the new wiper.
   e. Insert new transducer wiper from bottom of carriage.
   f. Make sure that wiper is high enough not to contact transducer when carriage is replaced.
   g. Make certain wiper is facing armature then tighten set screw finger tight.
   h. If wiper is only thing to be replaced then go to Step 1 of a Replacement Procedure.

6. Carriage Assembly Bearings Removal/Replacement.
   a. Only five of the seven bearings can be replaced, see figure 5-11. If the two unreplaceable bearings seem to be bad then the carriage assembly must be replaced.
   b. Loosen bearing shaft set screw.
   c. Remove and replace bearing/s.
   d. Tighten bearing shaft set screw.
   e. For spring loaded bearing remove spring, replace bearings and spring.

CARRIAGE ASSEMBLY/POSITION TRANSDUCER/POSITION TRANSDUCER WIPER ARM REPLACEMENT

NOTE
Wipe carriage rail clean with isopropyl alcohol/water solution prior to replacement of carriage assembly.

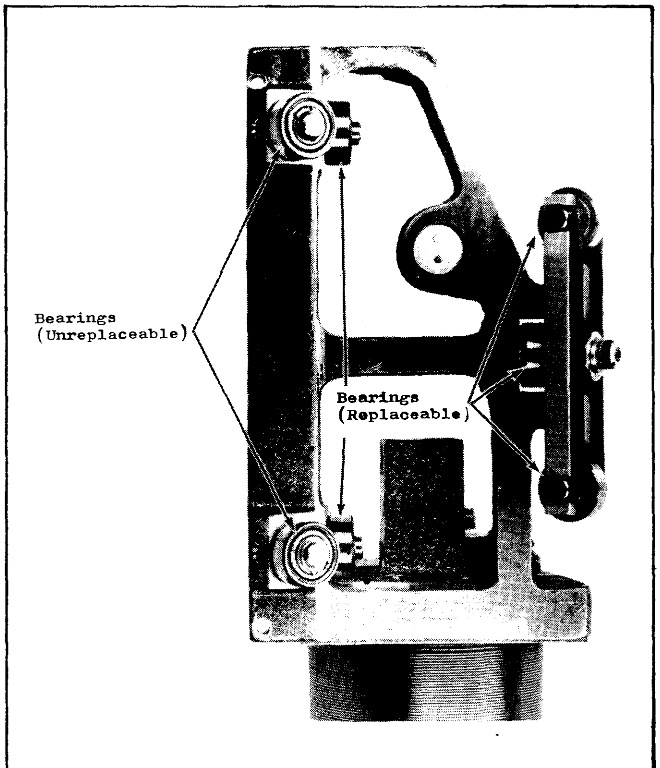


Figure 5-11. Carriage Assembly

1. Carriage assembly replacement.
   a. Remove detent cover and loosen two detent hold down screws.
   b. Depress micro switch and install carriage on the guide rail.
   c. Check two hold down bearings to assure that they contact side of guide rail flatly. Also ensure the position transducer wiper does not contact the position transducer.
   d. Move Carriage forward to spindle stop.
   e. Adjust position transducer wiper set screw just tight enough to support the weight of the wiper.
   f. Carefully replace servo positioner motor and replace mounting screws but leave them loose enough for motor to be moved.
   g. Attach flexible circuit to positioner motor.
   h. Insert the detent shim into the positioner motor around the carriage coil and very carefully move carriage back into the motor at the same time moving the motor if necessary to insure a minimum .005" gap between the coil OD and ID.

NOTE

With carriage in any position except the home position you should be able to run the shim between the coil and motor without any drag.

   i. Secure motor mounting screws and recheck gap.
   j. Perform Position Transducer Wiper Adjustment.

POSITION TRANSDUCER WIPER ADJUSTMENT

1. Installing alignment tool and alignment procedure.
   a. Install position transducer wiper adjustment tool in place with short locator pin in bottom head hole in carriage assembly (figure 5-12). Ensure the tool blade is engaged in slot in top of the wiper mounting block, secure tool by tightening head position lock screw.

Figure 5-12. Transducer Wiper Adjustment Tool

   b. In order to locate the wiper close to terminal #2 of the Markite, move carriage back until the upper rod on the tool is against the servo positioner motor face.
   c. Connect an ohmmeter between terminal # 2 of the Markite and the wiper wire.
   d. Turn large knurled knob clockwise (while holding small knob in place so wiper will not rotate) until wiper assembly is pushed down and just makes contact giving a continuity reading on ohmmeter.

e. Fully depress small knob on top of tool and hold while locking wiper in place with set screw. Small knob may be turned to position the wiper horizontally.
f. Release top knob and turn large knob counter-clockwise until tool blade clears the wiper mounting block and top surface of carriage casting.
g. Loosen lower head position lock screw, hold tool and push carriage to home position. This extracts the tool.
h. Disconnect ohmmeter.
i. Connect wiper wire to WPR pin on the SCM circuit board.
j. Proceed to Detent Assembly Replacement/Alignment procedures.
k. Perform an alignment check as per Alignment of Servo System.
l. Install heads as per Read/Write Head Assembly Replacement.
m. Align Read/Write heads as per Read/Write Head Assembly Adjustment.

DETENT ASSEMBLY

Due to the different types of assembly used for the two styles of drive, separate procedures are given for each.

CAUTION

ENSURE YOU ARE REFERRING TO THE CORRECT PROCEDURE BEFORE STARTING WORK

9480-12 DETENT ASSEMBLY (Refer to figure 5-13)

NOTE

The detent grid and photocell have been factory aligned and are not to be adjusted in the field. However, these items may be replaced by changing either the mask assembly or detent assembly, which are individually preadjusted at the factory.

TOOLS AND MATERIALS REQUIRED

The following tools and materials are required for the replacement/adjustment of the Detent Assembly.

1. 7/64" Allen wrench
2. Detent Shim Tool
3. Transducer Alignment Tool
4. Regular screwdriver.

DETENT ASSEMBLY REMOVAL

CAUTION

Extreme care should be exercised in handling the detent and mask assemblies to avoid BREAKAGE or SCRATCHING of the masks. HEAT should NOT be applied near the detent assembly. DO NOT TAMPER with any screws on the detent when installing or removing, other than the two hold down screws. If TAMPERED with, misalignment of detent will occur and necessitate replacement of whole assembly.

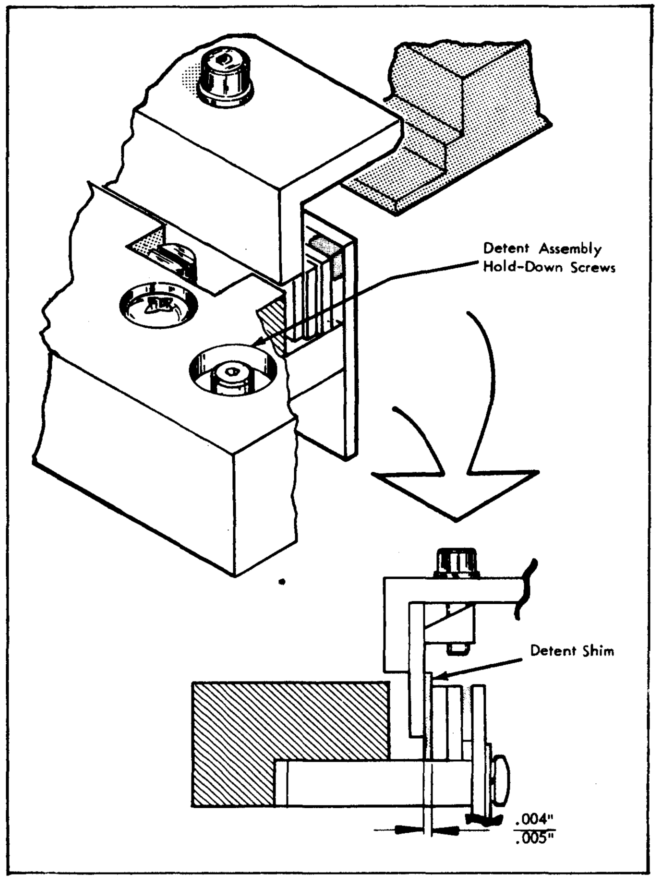


Figure 5-13. Positioning of Detent and Mask Assemblies (9480-12)

1. Removing Detent Assembly.
   a. Turn OFF main power switch S5.
   b. Remove necessary covers from cabinet.
   c. Disconnect detent connector P13.
   d. Loosen the two hold down screws securing the mask assembly. WHILE HOLDING the mask assembly with one finger, remove the two hold down screws and then carefully remove the mask assembly from the carriage. Figure 5-6.

   NOTE

   Mask assembly mounting fixture may be attracted by the magnet. DO NOT let go of assembly when removing mounting screws.

   e. Loosen the two hold down screws securing detent assembly.

f. Remove detent assembly from unit.

DETENT ASSEMBLY REPLACEMENT/ALIGNMENT

1. Replacing the Detent Assembly
   a. Carefully place assembly into position insert and start the two mounting screws (do NOT tighten) and leave cover off.
   b. Install mask assembly flush against the carriage shoulder and secure hold down screws using lock washers only.
   c. As you assemble, place detent shim between fixed mask on detent assembly and mask assembly on carriage (figure 5-13 so that 1" or less is protruding towards spindle.
2. Detent Assembly Alignment
   a. Disconnect servo positioner motor (P4).
   b. Place a clean pad of soft material between the Read/Write heads and manually load them by slowly moving carriage toward the spindle so that approximately 1/2" of coil is showing.
   c. Slide detent assembly away from carriage until shim is snug and make sure the two masks are parallel.
   d. While holding position firmly, secure the two detent assembly hold down screws.
   e. Remove shim. If there is no tension on shim then loosen the two hold down screws, replace shim, and go back to Step c above.
   f. Move carriage forward to full extent of travel and visually sight through the gap between masks. Light shining through will assure that there is no drag.
   g. Install detent cover with three screws. Carriage will have to be moved to both ends of travel to install screws.
   h. Plug in detent connector (P13).
   i. Return carriage to home position, remove protective pads from heads, and reconnect servo motor plug (P4).
   j. Proceed to Servo Alignment then to Head Alignment Sections.

NOTE

Whenever the detent assembly or Mask Assembly is removed the Servo and Head Alignments must be checked and recalibrated.

9481-12 DETENT ASSEMBLY (Refer to figure 5-14)

NOTE

The detent grid and photocell have been factory aligned and are not to be adjusted in the field. However, these items may be replaced by changing either the mask assembly or detent assembly, which are individually preadjusted at the factory.

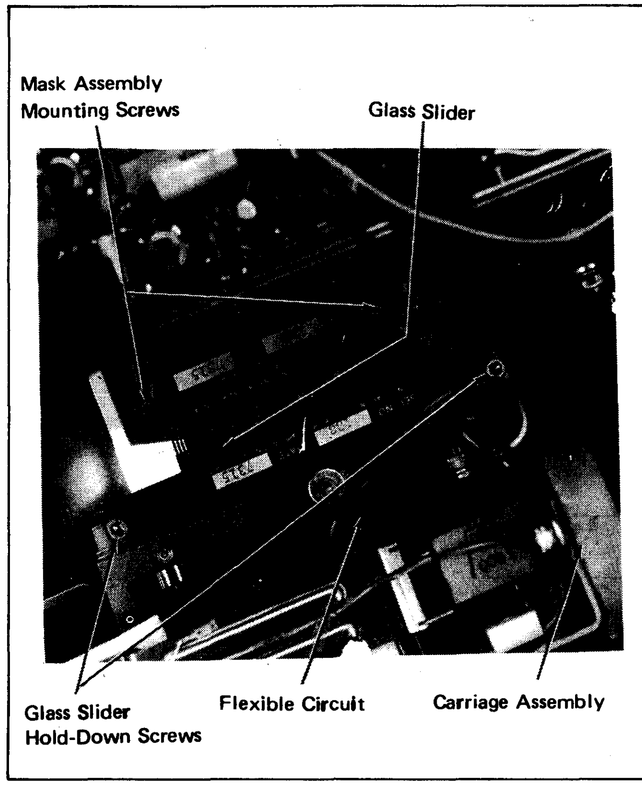


Figure 5-14. Detent Assembly (9481-12)

TOOLS AND MATERIALS REQUIRED

The following tools and materials are required for the replacement/adjustment of the Detent Assembly.

1. 7/64" Allen wrench
2. Detent Shim Tool
3. Transducer alignment tool
4. Regular Screwdriver

DETENT ASSEMBLY REMOVAL

CAUTION

Extreme care should be exercised in handling the detent and mask assemblies to avoid BREAKAGE or SCRATCHING of the masks. HEAT should NOT be applied near the detent assembly. DO NOT TAMPER with any screws on the detent when installing or removing, other than the two hold down screws. If TAMPERED with, misalignment of detent will occur and necessitate replacement of whole assembly.

1. Removing Detent Assembly
   a. Turn OFF main power switch S5.
   b. Remove necessary covers from cabinet.
   c. Disconnect detent connector P13.
   d. Loosen the two hold down screws securing the glass slider, WHILE HOLDING the glass slider with one finger, remove the two hold

down screws and then carefully remove the glass slider from the carriage.

NOTE

Glass slider mounting fixture may be attracted by the magnet. DO NOT let go of slider when removing mounting screws.

e. Loosen the two hold screws securing detent assembly.
f. Remove detent assembly from unit.

1. Replacement and Alignment of Detent Assembly (Figure 5-15)
   a. Install transducer alignment tool on carriage assembly, making sure that is is flush against the carriage assembly.
   b. Place detent assembly in a position that is flush against the alignment tool. Tighten detent hold down screws maintaining flush position.
   c. Remove transducer alignment tool.
   d. Place glass slider so that mounting fixture is flush against carriage. While holding glass slider in place installl hold down screws and tighten them.

NOTE

Glass slide mounting fixture may be attracted by the magnet. DO NOT let go of slider until it is bolted into place, as slider would be damaged.

   e. Loosen two screws on rear of transducer assembly. Place detent shim tool between glass slider and transducer mask.
   f. Move transducer mask up until gauge fits snugly. Tighten hold down screws. Verify gauge fits snugly.
   g. Plug in detent connector P13.
   h. Ensure carriage is in home position and servo motor is connected.
   i. Proceed to Servo Alignment then to Head Alignment Sections.

NOTE

Whenever the detent assembly or glass slider assembly is removed, the Servo and Head Alignment must be checked and recalibrated.

HEAD LOAD CAM ADJUSTMENT

NOTE

Head alignment must be correct before performing this adjustment

Tools required :
Flashlight
7/64" Allen wrench
Test Hub

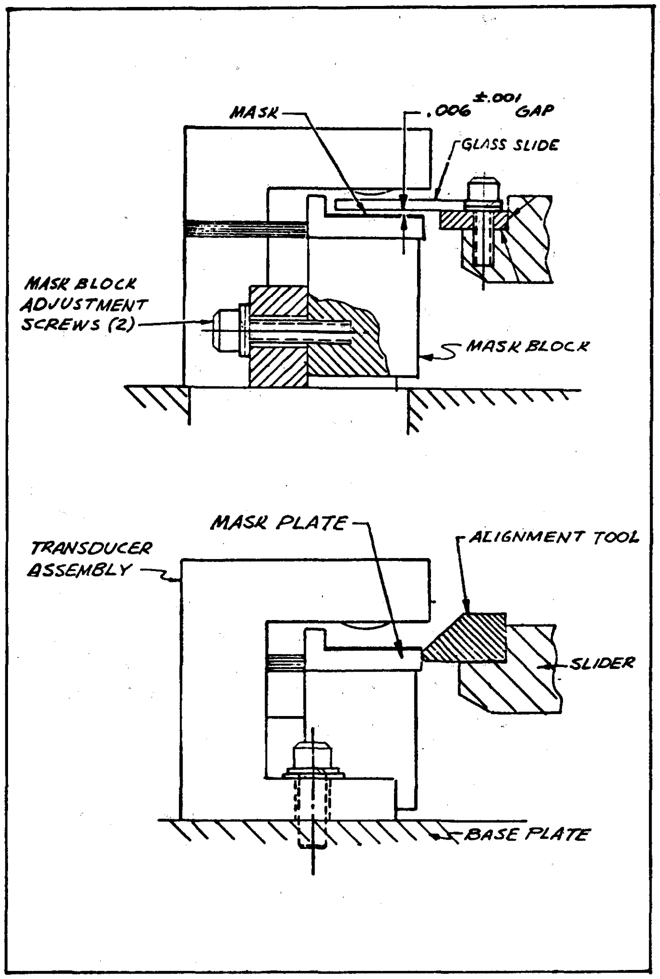


Figure 5-15. Positioning of Detent and Mask Assemblies (9481-12 Only)

1. Remove covers, or pull module out on rails to gain access to heads.
2. Install a Texwipe pad between the heads and over-ride the Cartridge Interlock Switch.
3. Install the Test Hub and power up the drive.
4. Loosen the 2 head load cam screws.
5. Push the ramp firmly downwards against the aluminium casting. Snug down the screws.
6. Adjust the ramp so there is a 0.020"-0.030" gap between the front of the cam and the "V" shaped ramp on the head arms. (See figure 5-16).
7. Power down the drive, remove the Test Hub and Texwipe pad.
8. Slowly insert a scratch cartridge and carefully adjust the ramp until the disk is centralised between the two prongs, when the cartridge is properly seated on spindle. (It will probably be necessary to use a flashlight to inspect this adjustment).
9. Tighten down the two head load ramp screws.
10. Power up the drive and power off again.

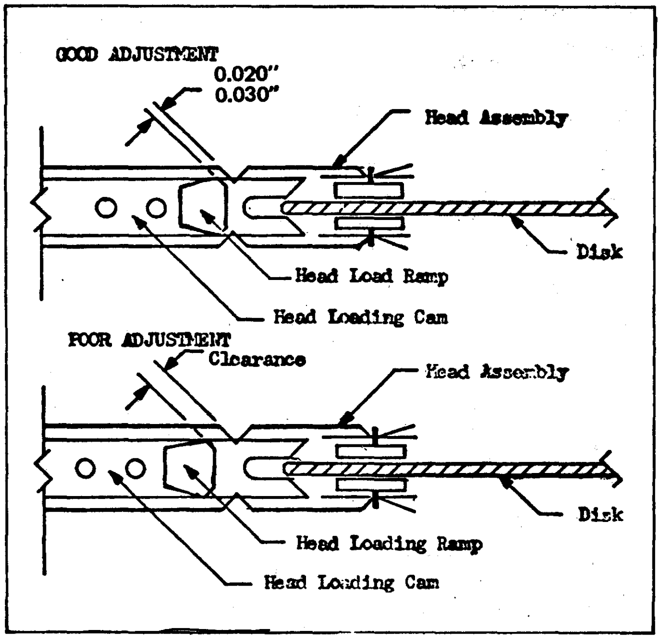


Figure 5-16. Head Load Cam Adjustment

11. If the carriage chatters and does not go to the home position, the home switch must be adjusted until the heads retract properly.

INDEX/SECTOR TRANSDUCER ASSEMBLY Figure 5-17

TOOLS AND MATERIALS REQUIRED

1. Oscilloscope
2. Exerciser or DPU
3. Alignment Cartridge (Dibit)
4. Trimpot adjusting screwdriver
5. 7/64" Allen wrench

INDEX/SECTOR TRANSDUCER REPLACEMENT/ALIGNMENT

1. Removal of Index/Sector Transducer assembly
   a. If STOP light is not lit, then push STOP switch
   b. Turn main power OFF by pushing switch S5.
   c. Remove necessary cabinet covers to expose baseplate assembly.
   d. Remove two (2) 6/32" hold down screws retaining transducer to baseplate.

   NOTE
   The following operation can be performed without removing the receiver assembly if the receiver is held in its full-up position (handle down).

   e. Disconnect cable at the Read/Write Amplifier P17/J17.
   f. Remove transducer and cable.

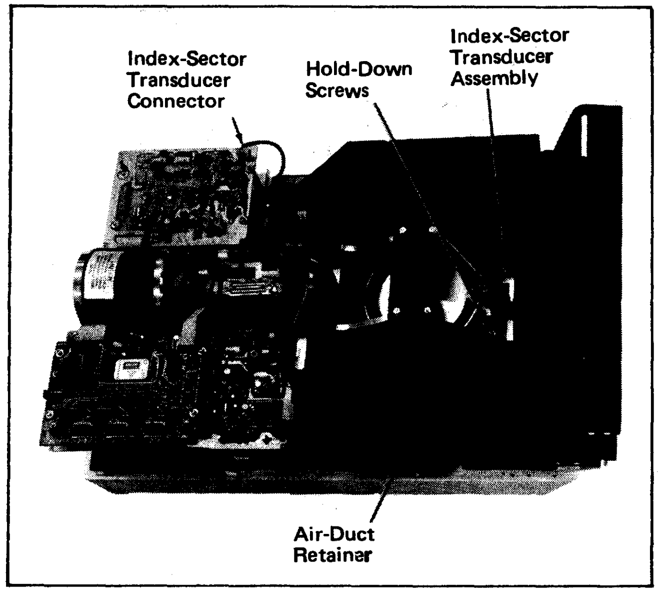


Figure 5-17. Index/Sector Transducer Assembly

2. Replacement of Index/Sector Transducer Assembly.
   a. Place new transducer assembly and wired cable into position.
   b. The transducer is to sit flush against the spindle assembly flange.
   c. Route the transducer cable around the spindle.
   d. Secure cable with existing tie down clamps.
3. Alignment of Index/Sector Transducer Assembly
   a. Pre-position the transducer before securing the hold down screws by rotating the assembly around the circumference of the spindle flange to an extreme clockwise position.
   b. While holding this position, secure the hold down screws.
   c. Install the Alignment cartridge.
   d. Proceed to Radial Alignment, step 3 of Head Alignment Procedures in Section IV.

CARTRIDGE RECEIVER ALIGNMENT

TOOLS AND MATERIALS REQUIRED

1. Cartridge Receiver Alignment Tool
2. 7/64" Allen wrench
3. 1/8" Allen wrench
4. 3/8" Open/Box wrench.

CARTRIDGE RECEIVER ALIGNMENT

1. Complete alignment procedure.
   a. If STOP light is not lit then push STOP switch.
   b. Turn OFF main power by pushing switch S5.

c. Remove necessary covers to gain access to drive module.
d. Using 3/8" wrench and 1/8" Allen wrench remove nut and shoulder screw from pivot bracket.
e. Reach through front of receiver assembly and unhook hold down spring.
f. Receiver assembly can now be lifted off of drive module.
g. Loosen pivot bracket mounting screws.
h. Install rceiver alignment tool, using shoulder screw previously removed, to pivot bracket.
i. Allow receiver alignment tool to rest on cartridge alignment posts with small portion of the post protruding through the alignment tools' holes. See Figure 5-18.
j. Tighten pivot bracket mounting screws being careful not to twist pivot bracket. If pivot bracket is allowed to twist then shoulder screws will bind against receiver assembly.
k. Remove receiver alignment tool.
l. Reinstall receiver assembly using two shoulder screws and lock nuts.
m. Work receiver assembly up and down a couple of times to ensure the shoulder screws are not binding.
n. Reconnect receiver assembly hold down spring.
o. Install and remove several disk cartridges to ensure assembly is working properly.
p. Replace covers that have been removed.

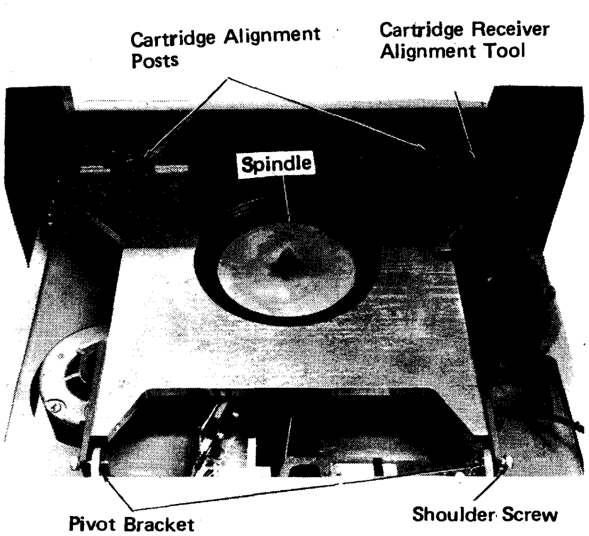


Figure 5-18. Receiver Alignment Tool

SPINDLE DRIVE MOTOR ASSEMBLY FIGURE 5-19

TOOLS AND MATERIALS REQUIRED

1. 3/16" Allen wrench
2. 1/8" Allen wrench
3. 1/16" Allen wrench
4. 12" Straight edge
5. Phillips screwdriver.

SPINDLE DRIVE MOTOR ASSEMBLY REMOVAL

1. Initial set up.
   a. Remove necessary covers to gain access to drive module.
   b. If STOP light is not lit then push STOP switch.
   c. Turn OFF main power by pushing switch S5.
   d. Disconnect main power plug.
2. Removing motor assembly.
   a. Remove wiring from motor start relay (K1-4) and terminal board (TB2-1) to free motor assembly.
   b. Loosen three socket screws on motor hold down plate.
   c. Remove drive belt tension spring from motor hold down plate.
   d. Remove drive belt.
   e. Secure motor by pushing motor hold down plate against baseplate and completely remove motor assembly from baseplate.
   f. Carefully remove motor assembly from baseplate.

SPINDLE DRIVE MOTOR ASSEMBLY REPLACEMENT

1. Replacing drive motor assembly.
   a. Position drive motor assembly in place and hold against baseplate.
   b. Install and snug the three socket screws on motor hold down plate.
   c. Replace drive belt.
   d. Replace tension spring on motor hold down plate.
   e. Secure the three motor hold plate socket head screws.
2. Adjusting drive motor pulley to align with spindle pulley.
   a. Place straight edge across the bottom of the spindle pulley in such a way that the edge will extend under drive motor pulley.
   b. Using a 1/16" Allen wrench loosen the two set screws in the drive motor pulley.
   c. Adjust height of drive motor pulley so the bottom of the pulley will touch the straight edge.
   d. Tighten two set screws in drive motor pulley and recheck alignment.

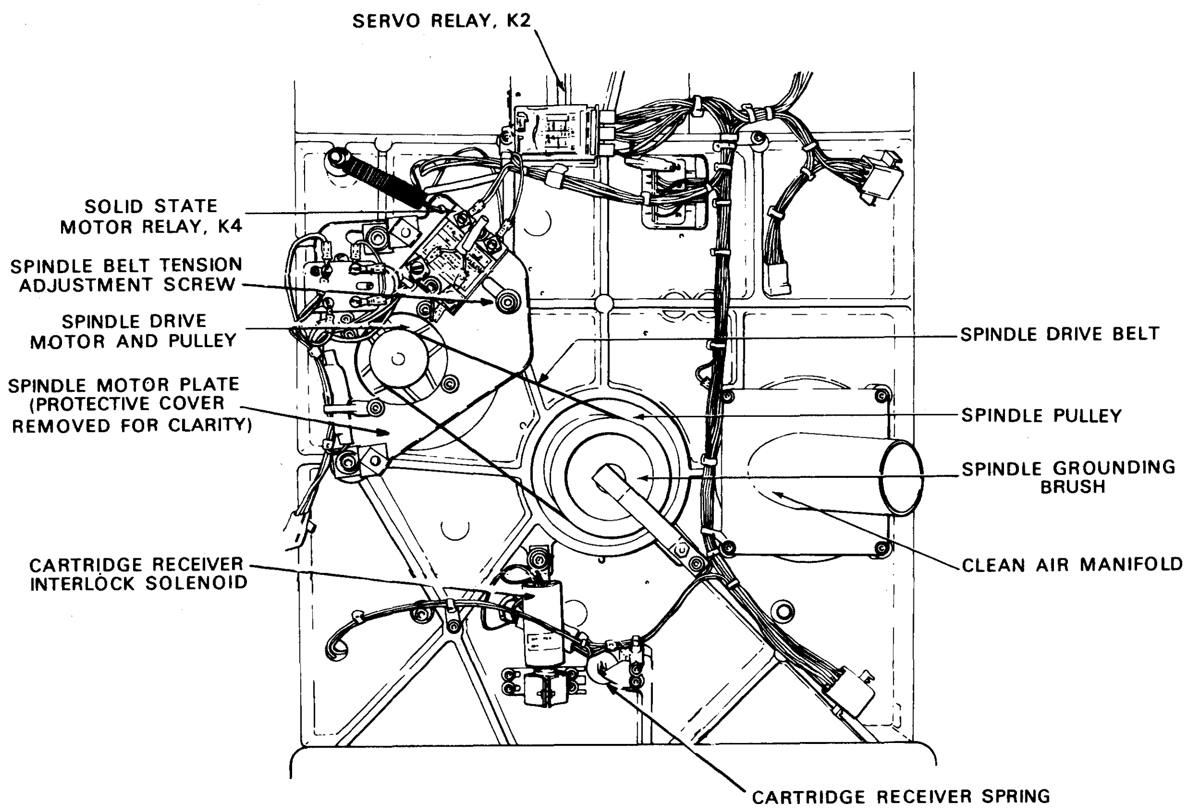


Figure 5-19. Spindle Drive Motor Assembly

3. Final assembly.
   a. Rewire motor wiring to K1-4 and TP2-1.
   b. Plug in main power plug.
   c. Turn ON main power switch S5.
   d. Push RUN switch.
   e. Visually check motor drive pulley to ensure it is tracking on pulley.
   f. Push STOP switch.
   g. Replace covers that have been removed.

DRIVE MOTOR PULLEY REMOVAL

1. Initial set up.
   a. If STOP light is not lit then push STOP switch.
   b. Turn OFF main power by pushing switch S5.
   c. Remove necessary covers to gain access to drive module.
   d. Remove main power plug.
2. Removing drive motor pulley.
   a. Remove spindle drive belt.
   b. Remove two (2) set screws from either side of the drive motor pulley.
   c. Remove pulley from motor shaft by exerting even pressure to avoid binding.

DRIVE MOTOR PULLEY REPLACEMENT

1. Replacing drive motor pulley.
   a. Push pulley on motor shaft being careful to exert even pressure to avoid binding.
   b. Insert the (2) set screws on either side of the drive motor pulley.
2. Aligning drive motor pulley with spindle pulley.
   a. Place straight edge across the bottom of the spindle pulley in such a way that the edge will extend under drive motor pulley.
   b. Adjust height of drive motor pulley so the bottom of the pulley will touch the straight edge.
   c. Tighten the two (2) set screws on the drive motor pulley and recheck alignment.
3. Final Assembly.
   a. Replace the spindle drive belt.
   b. Plug in main power plug.
   c. Turn ON main power switch S5.
   d. Push RUN switch.
   e. Visually check motor drive pulley to ensure it is tracking on pulley.
   f. Push STOP switch.
   g. Replace covers that have been removed.

SPINDLE ASSEMBLY

TOOLS AND MATERIALS REQUIRED

1. 3/16" Allen wrench
2. 1/8" Allen wrench
3. 7/64" Allen wrench
4. Spring hook

SPINDLE ASSEMBLY REMOVAL

1. Initial set up.
   a. If the STOP light is not lit then push the STOP switch.
   b. Turn OFF main power by pushing switch S5.
   c. Unplug the main power plug.
   d. Remove necessary covers to gain access to drive module.
2. Removing the spindle assembly.
   a. Loosen three socket screws on motor hold down plate.
   b. Remove spindle drive belt.
   c. Remove one end of receiver hold down spring.
   d. Remove two (2) shoulder screws from pivot bracket.
   e. Remove receiver assembly from unit.
   f. Lift magnet out of spindle chuck.
   g. Insert Allen wrench through hole in chuck and remove the three (3) socket screws holding spindle.
   h. Remove spindle.

SPINDLE REPLACEMENT

1. Replacing spindle assembly.
   a. Carefully place spindle assembly in unit. If assembly is cocked to one side, the resulting bind will damage base casting.
   b. Replace and secure the three socket screws using an Allen wrench through the hole in the spindle chuck.
   c. Install spindle chuck magnet with beveled edge down.
   d. Place receiver assembly in place and install the two (2) shoulder screws.
   e. Tighten shoulder screws and secure them with the jam nuts.
   f. Replace receiver hold down spring.
   g. Install a scratch cartridge to ensure everything works without binding.
2. Final Assembly
   a. Replace spindle drive belt.
   b. Tighten three socket screws on motor hold down plate.
   c. Plug main power cord in.
   d. Turn ON main power switch S5.
   e. Push RUN switch.
   f. Visually inspect to ensure unit is working properly.
   g. Proceed to Head Alignment Procedure Step 1a and check for proper Head Alignment.

SPINDLE ASSEMBLY GROUNDING BRUSH

To clean the spindle assembly grounding brush:

1. Lift brush away from bottom of spindle.
2. Place a piece of emery paper between spindle and grounding brush.
3. Release brush and move emery paper around to polish surface of grounding brush.
4. Remove emery paper.

SECTION 6
INSTALLATION

UNPACKING (Refer to figure 6-1)

1. Check Tip 'n' tell indicator for possible evidence of poor handling.
2. Remove banding.
3. Lift off top.
4. Remove internal packing.
5. Lift off cardboard sides.
6. Remove T & F document package.
8. Unscrew barrier (see figure 6-2).
9. Take plywood piece and place on step to form a ramp. (Plywood piece is packed loose in box). See figure 6-3. Use barrier to support the centre of the ramp.
10. Roll machine gently down ramp.

NOTE
Later units do not have cardboard sides and a tip 'n' tell indicator.

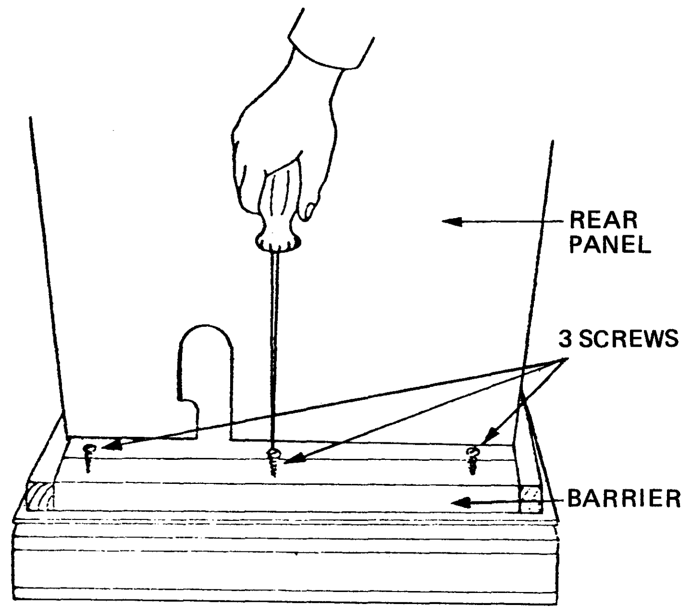


Figure 6-2. Removing Barrier

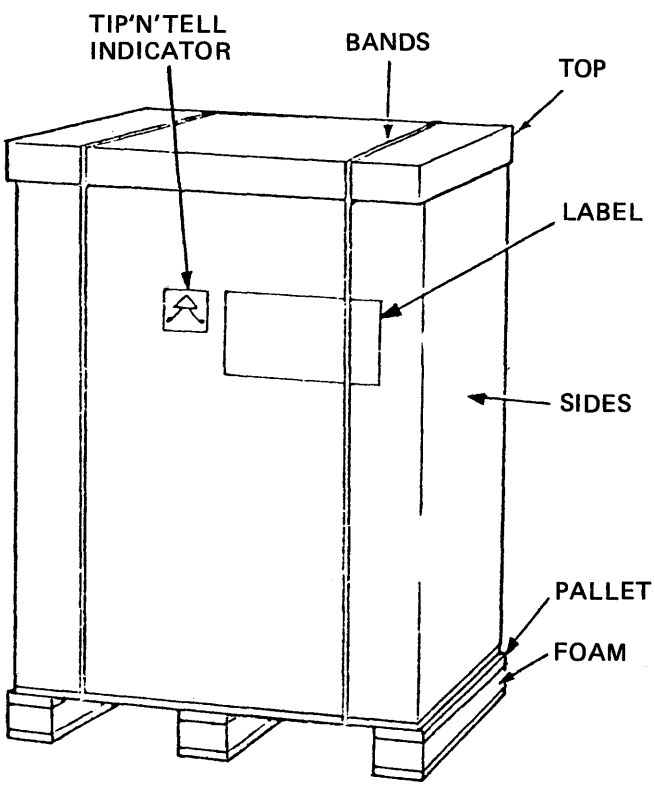


Figure 6-1. Shipping Carton

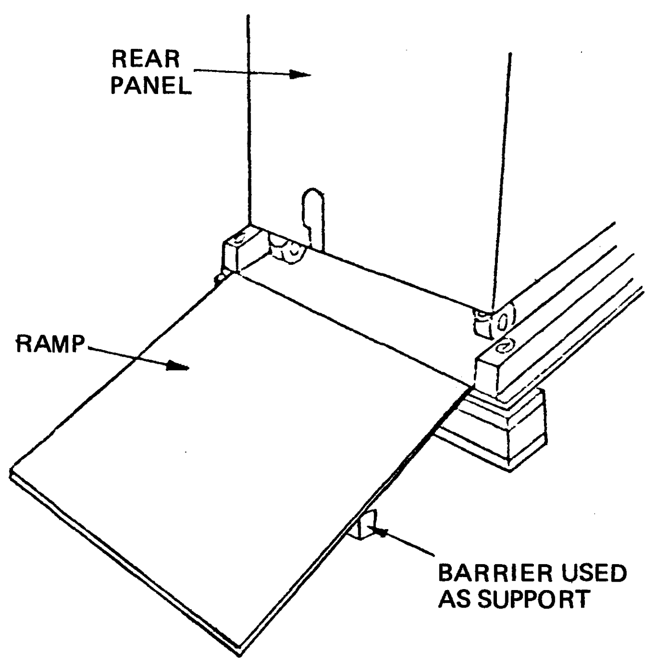


Figure 6-3. Ramp

CHECKOUT

1. Check cases for damage.
2. Remove cases.
3. Visually inspect the unit for the following:
   Loose/missing fasteners
   Damaged or broken parts
   Loose connection/connectors
   Spindle belt tension.
4. Check unit is manufactured for correct voltage and frequency. Refer to figure 6–4 for voltage settings and the I.D. plate for frequency. If incorrect, follow conversion instructions in this section.
5. Remove the cable tie from the positioner motor assembly.
6. Ensure the servo plug P/J 4 is disconnected.
7. Completely vacuum out the unit.
8. Clean the carriage guide, and linear pot as laid down in Section 4 page 3 or Page11.
9. Clean the heads as laid down in Section 5 page 4.
10. Install a texwipe pad between the heads, and move the carriage assembly so that the heads are just off the head load ramp.
11. Connect P/J4. If heads do not retract immediately, the unit must not be used until the battery has been replaced or charged up.
12. If the heads retracted correctly, then apply A.C.
13. Slowly insert a cartridge and check:
    a. Cartridge door opener bail operation.
    b. Disk is correctly positioned between prongs of head load ramp.
    c. Disk does not touch either head.
    If necessary, perform the head load cam adjustment, (section 5 page 15.
14. Power the drive up and ensure heads load correctly. (Listen carefully in case any head is touching the disk).
15. Check the INDEX pulse as per Section 4 page 1. If INDEX pulses are not 40mS apart, an incorrect diameter motor pulley may be the cause.
16. Power down the drive and check:
    a. Heads retract correctly onto head load ramp.
    b. Receiver handle does not unlock until disk comes to rest after about 30 seconds.
17. Repeat steps 5 through 16 for the other drive in the cabinet.
18. Check the head adjustment, Section 4 page 5 or page 15.
19. Check the data discriminator setting, Section 4 page 7 or page 18.
20. Run suitable MTR and check for errors.

    NOTE

    Use a known, good, disk.
21. If either drive gives errors, check the alignment as per the Test and Adjustment Procedure in Section 4.

	T1		T2		
Line Voltage	Input	Jumper	Input	Jumper	Output
100	B C	B–F C–G	4 5	4–8 5–9	1 2
110	B D	B–F D–H	4 10	4–8 6–10	1 2
115	A C	A–E C–G	USE 115V JUMPER		
125	A D	A–E D–H	USE 115V JUMPER		
200	B G	C F	4 9	5 8	1 2
220	B H	D F	4 10	6 8	1 2
230	A G	C E	3 9	5 7	1 2
240	A G	D E	3 9	6 7	1 2
250	A H	D E	3 10	6 7	1 2

Figure 6–4. Voltage Settings

22. FILL IN AND MAIL THE INSTALLATION REPORT.

CONVERSION PROCEDURES

CONVERSION INSTRUCTIONS 50/60 Hz

50 to 60 Hz and 60 to 50 Hz.

Standard Time: 30 minutes.

Frequency conversion is achieved by changing pulley sizes on the disk drive/motor.

1. Remove all AC from machine.
2. Remove case panels.
3. Slacken off 3 screws holding the motor plate on top drive.
4. Drop belt.
5. Remove 4 grub screws holding pulley to motor shaft. Two grub screws are inserted in each hole.
6. Remove pulley.
7. Install pulley. (pn 1880 5051) 60 Hz, pn 1880 5044 50 Hz).
8. Tighten down two grub screws onto flat of motor shaft.
9. Install belt.
10. Tension motor plate using spring (1446 4002) and post (1446 3292), see figure 6-7.

NOTE
The motor plate must remain isolated from the base plate.

13. Repeat for lower drive.
14. If voltages are to be changed proceed to voltage conversion. If not, proceed to check out procedure, Voltage Conversion Instructions.

U.S. DOMESTIC TO INTERNATIONAL

Standard Time: 1 Hour (including step 10).

All international machines must contain an International Transformer T2 in addition to T1 in the power supply. The purpose of the International transformer is to supply 115 VAC for the motors and blower.
1. Remove all AC.
2. Remove case panels. Remove modesty panel.
3. Bolt International transformer 1880 2835 to base using 4 screws 1447 0207 and washers 1447 0025 (or equivalents). Refer to figure 6-6.
4. Remove jumper plug P20.
5. Install harness 1880 7214 on International transformer as per figure and table.
6. Install any jumpers required on T2 input.
7. PLug the harness into J20.
8. Connect T1 connections as per table for the required input voltage. Install any jumpers required.
9. If input voltage is greater than 125V, replace Mains fuse with 10A MDA 250V pn 1102 7950.
10. Install protection covers on transformers. Replace modesty panel.
11. Perform checkout procedure.

VOLTAGE CONVERSION INSTRUCTIONS

INTERNATIONAL TO U.S. DOMESTIC (115 VAC).

Standard Time:
1. Remove all AC from machine.
2. Remove case panels.
3. Extract P20.
4. Insert jumper plug into J20 (1880 5481), see figure 6-5.
5. Change the tappings on T1 for 115V as follows:
   a. AC Line input A and C.
   b. Jumper A to E.
   c. Jumper C to G.
6. If conversion from 50 to 60 Hz is to be done, proceed to Frequency Conversion Instructions.
7. Otherwise, go to checkout procedure.

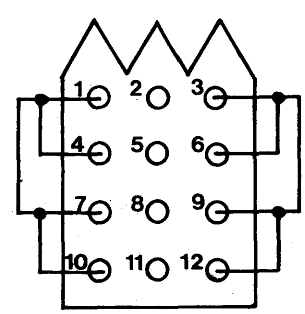


Figure 6-5. P20 Jumper 1880 5481

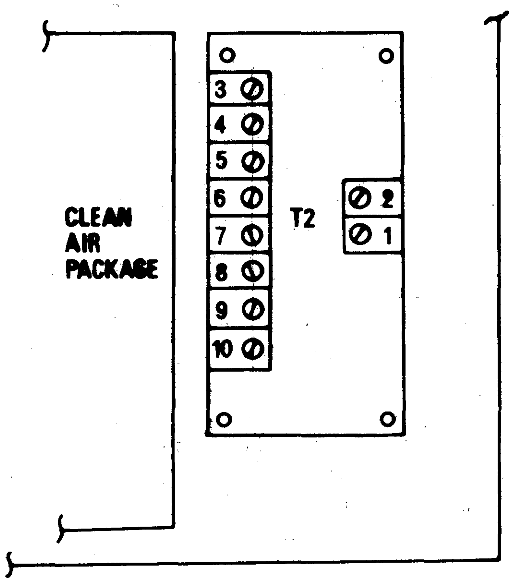


Figure 6-6. International Transformer Mounting

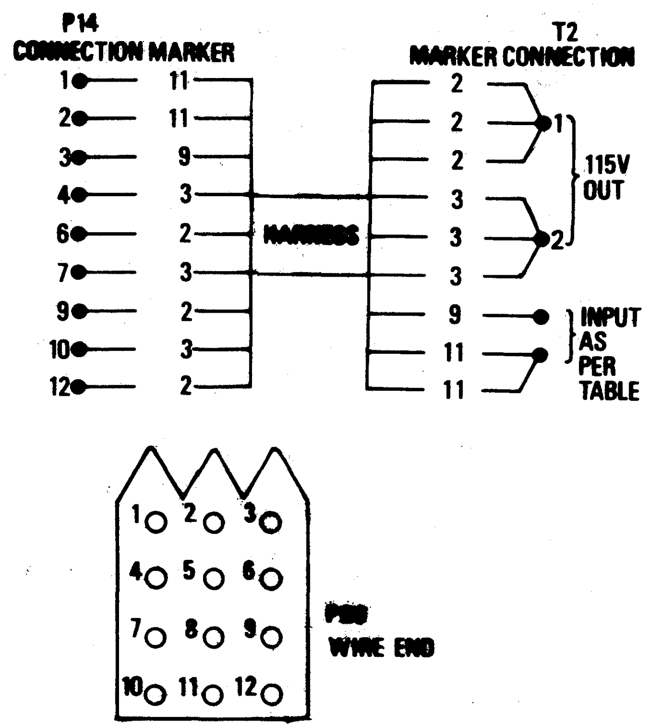


Figure 6-8. Transformer Link Harness

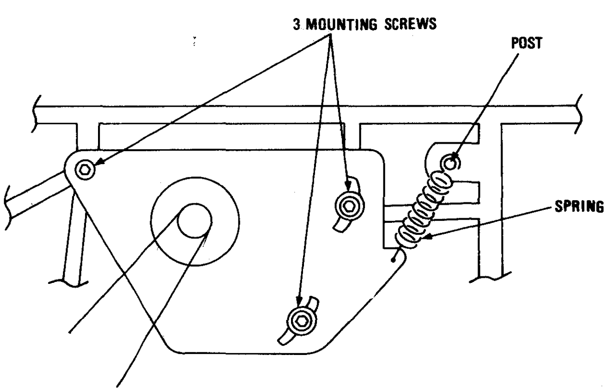


Figure 6-7. Motor Mounting Plate

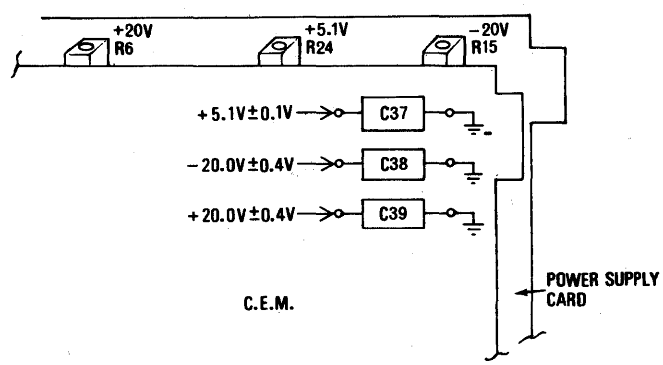


Figure 6-9. Voltage Adjustments

Burroughs

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