B9499-6 DISK DRIVE ELECTRONIC CONTROLLER (205, 206, 207)

TECHNICAL MANUAL VOLUME 3:

THEORY OF OPERATION

Burroughs

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INTRODUCTION

This Field Engineering manual describes the Basic Principles, Mode Flows, Address and Data Related Circuits, other Miscellaneous Circuits, and the Power Supply for the operation of the B 9499-6 Disk Drive Electronic Controller.

This Field Engineering Technical Manual is prepared in a revised format as follows:

1) Volume 1, Operation and Maintenance
2) Volume 2, Illustrated Parts
3) Volume 3, Theory of Operation

The division of the manual into volumes provides a more complete concentration of the subject matter with respect to machine maintenance and theory.

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SECTION 1
BASIC PRINCIPLES

GENERAL DESCRIPTION

The Disk Drive Electronic Controller (DDEC) enables the B9484-5 Disk Pack Drive (206) (DPD) and the B9494-4 Fixed Disk Drive (207) (FDD) to be operated by the B1800 or B1700 series computers. The DDEC receives commands from the Disk Pack Control (DPC) in the central system. Each command from the Disk Pack Control is translated into a series of commands to the disk drive. One command from the DPC may cause hundreds of messages to pass between the DDEC and the disk drive.

While the command from the DPC is being processed by the DDEC, data may be transferred from the DDEC to the DPC or vice-versa and from the DDEC to the drive or vice-versa. Generally, data is transferred from the system, through the DDEC to the drive during a WRITE operation; and from the drive, through the DDEC to the system on a READ operation. For some commands (OP codes), there is no data transfer.

When the OP is complete, the DDEC transfers a result descriptor to the central system which informs the system:

1) That the operation is complete.
2) If there has been an exception condition during the operation. An exception condition indicates to the system that the integrity of the last operation is questionable.
3) The type of exception (if any).
4) That there is additional failure information.

When the central system receives a result descriptor, it generally interrupts its normal processing and examines the result descriptor for exceptions. If there are no exceptions, it proceeds with processing. If the result descriptor contains an exception condition, it does the following:

1) Log the details of the operation and the result descriptor in the maintenance log.
2) Start a recovery procedure which usually includes retrying the operation again.

If the result descriptor indicates that there is additional failure information (TRY DIAGNOSTICS BIT), then a special operation is sent to the DDEC (READ EXTENDED RESULT DESCRIPTOR). This operation causes the additional failure information to be transferred to the system. This information should be used by the Field Engineer to assist in trouble shooting. It is found in the maintenance log.

CONFIGURATION

The DDEC is a 1 x 8 controller. This means it may connect to one Disk Pack Control and up to eight spindles of disk. The disk drives may be either 206 Disk Pack Drives or 207 Fixed Disk Drives or a mixture of 206 and 207. The maximum configuration is given in figure 1-1.

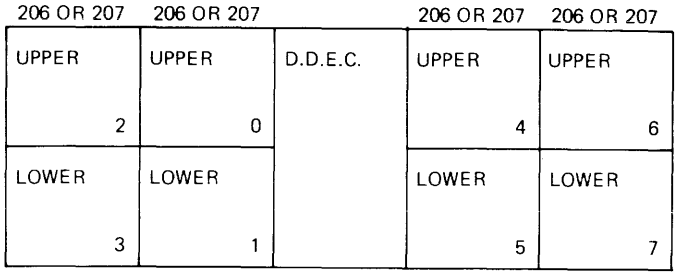


Figure 1-1. Maximum Configuration

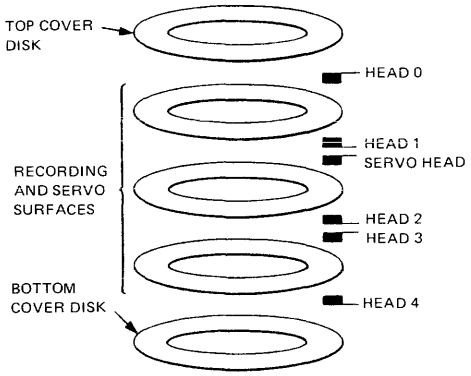


Figure 1-2. Pack Configuration (206)

It is not possible to intermix 206 and 207 in the same dual drive frame. The DDEC is preset at installation time by switches to indicate the type of drive on each port.

The I/O connection is made radially (i.e., from the controller to each drive). It is not possible to connect drives serially.

AC power, AC ground (frame ground) and logic ground are supplied to the drives by the DDEC.

DISK PACK DRIVE FORMAT

206

Platter Configuration

The 206 pack contains five platters. The top and bottom platters are used for protection only. The

three central platters are used for recording. The upper surface of the center platter is factory recorded with servo data. Therefore, there are five surfaces available to write and read data. Data is recorded by a read/write head. There is one read/write head for each data surface and a read only head on the servo surface. (See figure 1-2).

The read/write heads are moved to a correct concentric track by a servo driven carriage. Tracks are spaced 0.0027 inches apart. This corresponds to 370 tracks per inch.

The five tracks covered by the heads at any one time are known as a cylinder. The total number of cylinders is 815, numbered 000 to 814.

Recording surfaces	5
Tracks per surface	815
Tracks per cylinder	5
Tracks per inch	370
Track spacing	0.0027 inch
Tracks per pack	4075
Sectors per track	90
Sectors per cylinder	450 (incl. 5 spares on surface 4).
Bytes per sector	180
Bytes per track	16.2 KB
Bytes per cylinder	81 KB (incl. 5 spare sectors).
Bytes per pack	65,934 KB (incl. spare sectors).
Bit density maximum	6039 bits per inch.
Bit density minimum	3983 Bits per inch.
Transfer speed	9.86 M bits per second.

Table 1-1. 206 Format Characteristics

Track Configuration (206)

Each track contains 90 sectors. Sectors are interlaced as shown in figure 1-3.

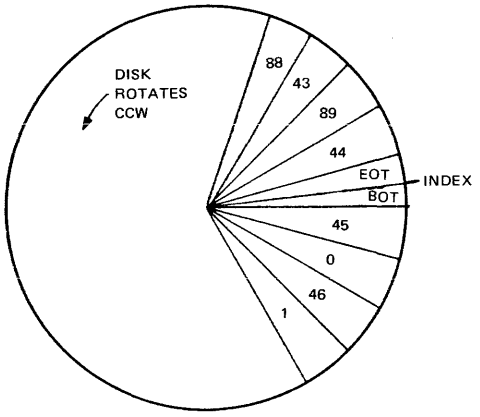


Figure 1-3. Interlaced Format (206)

Each cylinder contains five spare sectors reserved for relocation of sectors with media flaws. The spare sectors are situated on surface 4, sectors 85, 86, 87, 88, and 89. Relocation of bad sectors is usually performed by the INITIALIZE, VERIFY and RELOCATE (IVR) routines in the system software.

Cylinder 814 is reserved for maintenance use and is not available to the user through the MCP.

Figure 1-4 also shows the track configuration and the format for an individual sector.

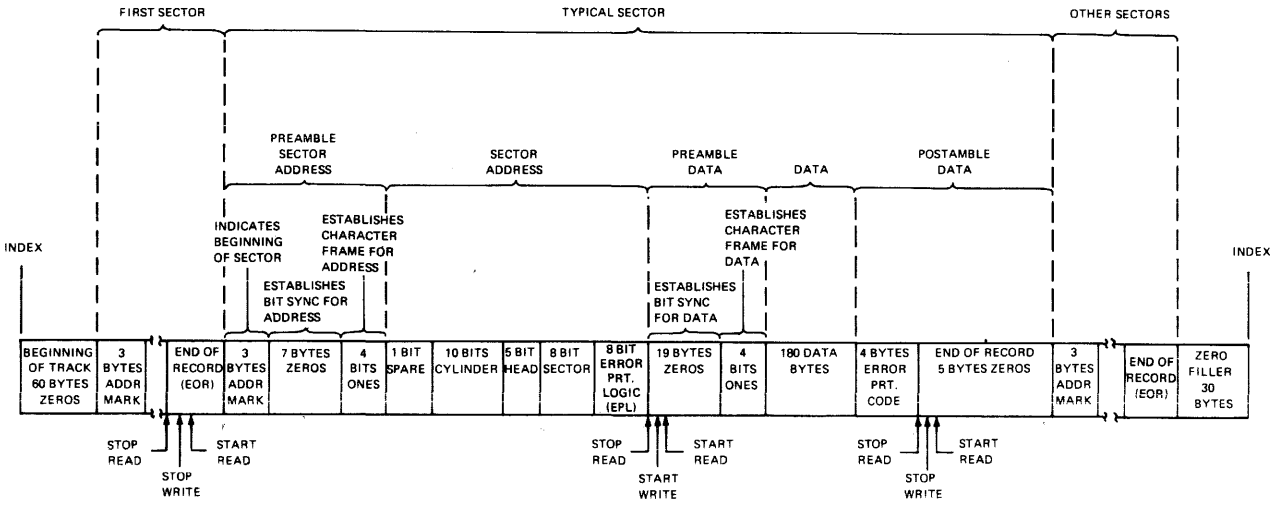


Figure 1-4. Track Format (206)

Error Protection Codes (206)

There are two error protection codes in each sector:

1) An 8-bit code for the address.
2) A 4-byte code for the data.

The address EPC protects against coincidence when an address is read incorrectly. Some examples of address error protection codes are given in table 1-2.

CYLINDER 0 HEAD 1		
Sector	**Hex. Pattern**	**EPC**
45	00012D	DC
46	00012E	BA
47	00012F	09
48	000130	20
49	000131	93
50	000132	F5
51	000133	46
52	000134	39
53	000135	8A
54	000136	EC
55	000137	5F
56	000138	12
57	000139	A1
58	00013A	C7
59	00013B	74
0	000100	8C
1	000101	3F
2	000102	59
3	000103	EA
4	000104	95
5	000105	26
6	000106	40
7	000107	F3
8	000108	BE
9	000109	00
10	00010A	6B
11	00010B	D8
12	00010C	A7
13	00010D	14
14	00010E	72

Table 1-2. Address EPC

The data EPC is a 4-byte code which is used by the system to correct an error if the retry procedure has failed to give a good READ. Some examples of data EPC are given in table 1-3. Data EPC is also known as firecode.

Data Pattern (Hex)	Firecode (Hex)
5555	A66AAD32
0000	00000000
1111	A1F772F0
AAAA	0CF55065
FFFF	AA9FFD57
FDFD	EAAA4AF3

Table 1-3. 206 Data Firecode

The DDEC contains hardware to perform the following functions (for 206 drives).

1) Generate the firecode to be written onto the disk.
2) Regenerate the firecode during a READ.
3) Detect a firecode error by comparing the regenerated firecode with the firecode READ from the disk.

Error correction is not performed for 206 drives. If the retry procedure fails, the system is able to correct the error with appropriate software. Bursts of up to five bits may be corrected.

207

The 207 contains four platters, fixed in the unit. All the platters are used for data storage. This gives eight surfaces, numbered 0 through 7. Servo information is included in the data tracks; therefore, there is no servo surface on the 207. (See figure 1-5).

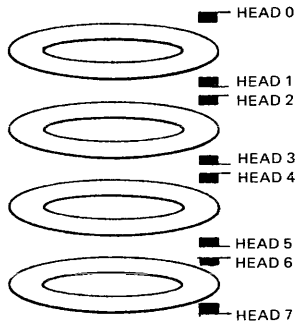


Figure 1-5. Platter Configuration (207)

Recording surfaces	8
Tracks per surface	1564
Tracks per cylinder	8
Tracks per inch	714
Track spacing	0.0014
Tracks per pack	12512
Sectors per track	90
Sectors per cylinder	720
Bytes per sector	180
Bytes per track	16.2 KB
Bytes per cylinder	129,600 (incl. 5 spare sectors on surface 7).
Bytes per unit	202,694,400 (incl. 5 spare sectors).
Bit density outer track	4320 Bits per inch.
Bit density inner track	6551 Bits per inch.
Transfer rate	10.71 M bits per second.

Table 1-4. 207 Characteristics

Cylinder Configuration

The 207 has one magnetic head for each surface. The heads are fixed to a carriage which is servo driven to a selected concentric track. The six tracks accessed by the heads at any one time are called a cylinder. The 207 tracks are spaced 0.0014 inch apart

(0.0357 mm). This corresponds to 714 tracks per inch. The total number of usable cylinders is 1564. These are numbered 0000 at the outside to 1563 on the inside. Table 1-4 gives 207 characteristics.

Each cylinder has five sectors allocated as spare sectors. These spare sectors are located on surface 7 sectors 85, 86, 87, 88 and 89. These sectors are used to relocate sectors containing media flaws. This is normally done during the INITIALIZE, VERIFY, and RELOCATE routine.

Cylinder 1563 is reserved for maintenance use and is not available to the user through the MCP.

Track Configuration

Each track contains 90 sectors, interlaced as shown in figure 1-6. The 207 has no Beginning-of-Track (BOT) or End-of-Track (EOT) gap. One sector is designated as the index sector by an extra pulse in the servo field.

Figure 1-7 shows the format of the individual sector. This is repeated 89 times around the track.

Error Protection Codes (207)

Each sector is protected by two codes:

1) An 8-bit code for the address.
2) A 7-byte code for the data.

The address EPC is identical to the EPC for the 206 drive. Examples are found in table 1-2.

Due to the increased area density (bits per square inch) and the typical size of media flaws, the fire-code for the 207 data field has been increased to 56 bits. This code is capable of correcting bursts of up to 11 bits.

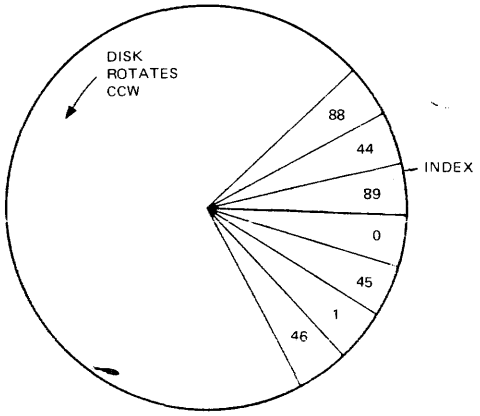
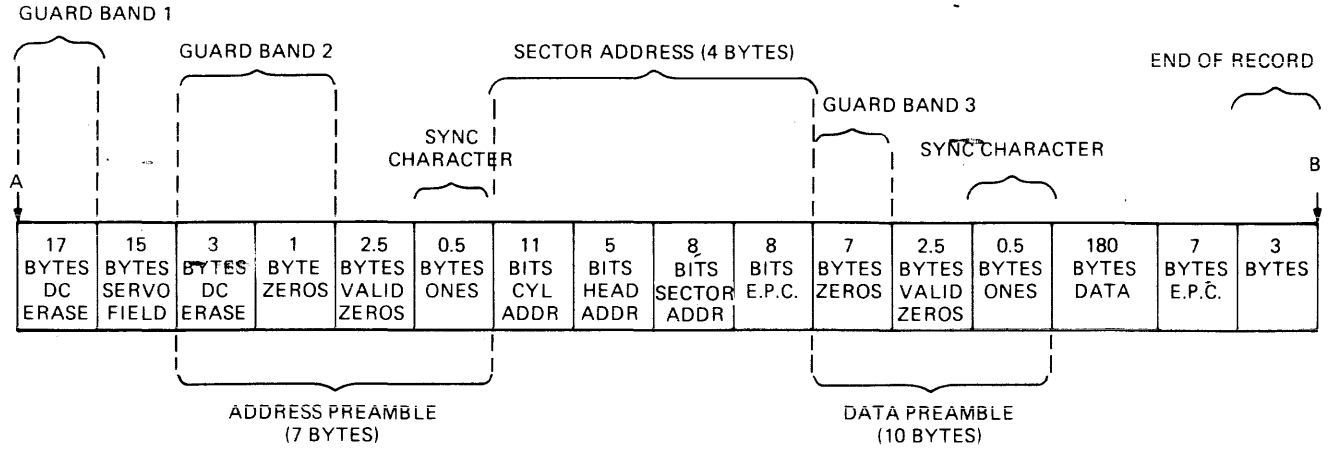


Figure 1-6. Interlaced Format (207)



NOTE: A TO B REPEATED 89 TIMES (90 SECTORS PER TRACK).

Figure 1-7. Track Format (207)

The DDEC contains hardware to perform the following functions (for 207 drives):

1) Generate the firecode to be written at the end of each data field.
2) Regenerate the firecode during a READ operation.
3) Detect an error by comparing the regenerated firecode with the code read off the disk.
4) Correct those errors which are correctable. Correction is performed when the retry procedure has failed. A variant in the read command initiates error correction.

Data Field	Firecode (54 Bits)
5555	A66AAD3235E8F5
0000	00000000000000
1111	A1F772F0ECDBD1
AAAA	OCF55065DEFF5D
FFFF	AA9FFD57EB17A8
FDFD	EAAA4AF3725360

Table 1-5. 207 Firecode Examples

The following notes apply to table 1-5.

1) Data is in hexadecimal.
2) Most-significant bit is left.
3) Data field is repeated 89 times.

INTERFACE DDEC TO DPC

General Description

The interface between the Disk Pack Control and the DDEC consists of a 25-wire coaxial cable. It may be split up into:

1) Sixteen (16) bi-directional data lines.
2) Eight (8) control and status lines.
3) One control line is not used.

The meaning and timing of the data lines is determined by the control and status lines. There are three types of information transfer on the 16-bit bus as described below.

Initiate Phase

The initiate phase consists of two consecutive data transfers from the DPC to the DDEC. The data transferred commands the DDEC to perform an operation. The bit significance of the two initiate words is detailed in table 1-6. The OP code and variant fields of initiate word 1 are further detailed in table 1-7.

Data Transfer Phase

The data transfer phase is used to transfer data from the DPC to the DDEC during a WRITE operation and, when specified, during INITIALIZE and RELOCATE operations. Data is transferred from the DDEC to the DPC during a READ operation, READ MAINTENANCE operation, VERIFY operation, and READ EXTENDED STATUS operation.

Data is transferred a word (16 bits) at a time.

Result Status Phase

The result status phase occurs at the end of each operation. It consists of a single word transfer informing the DPC if there were any errors or problems occurring during the operation. A detailed description of each bit is given later.

During a multiple sector READ or VERIFY operation, two words of firecode data and one word of result descriptor information are returned as data words 91, 92 and 93, respectively during the data transfer phase (not during the result status phase). At the end of the last sector, the result status phase is entered for the final result descriptor.

If a firecode error occurs at an intermediate sector, the result descriptor for that sector, all subsequent sectors, and the final result descriptor show the firecode error.

Information Lines	Initiate Word 1	Initiate Word 2
Least-significant bit		
INFO 00	OP1	B2*5
INFO 01	OP2	B2*6
INFO 02	OP3	B2*7
INFO 03	N0	B2*8
INFO 04	U1	B2*9
INFO 05	U2	B2*10
INFO 06	U3	B2*11
INFO 07	U4	B2*12
INFO 08	N1	B2*13
INFO 09	N2	B2*14
INFO 10	N3	B2*15
INFO 11	B2*0	B2*16
INFO 12	B2*1	B2*17
INFO 13	B2*2	B2*18
INFO 14	B2*3	B2*19
INFO 15	B2*4	B2*20
Most-significant bit		

OP1, OP2, OP3	OP code field
U1, U2, U3, U4	Unit address field
N0, N1, N2, N3	OP code variant bits
B2*0 — B2*20	Sector address field

Table 1-6. Initiate Words

OP Code Decode	OP Code Field			Variant Bits			
	OP1	OP2	OP3	N0	N1	N2	N3
Read 206	0	0	0	PLO	OF	E/L	I
Read 207	0	0	0	PLO	CR	E/L	–
Read Maintenance	0	0	1	–	–	0	–
Read Extended Status	0	0	1	–	–	1	–
Write 206	0	0	1	–	–	–	–
Write 207	0	1	0	–	–	F	–
Initialize	0	1	1	–	–	S	P
Relocate [1] (Data Specified)	1	0	0	–	N	N	N
Relocate [2] (Data = Address field)	1	0	1	–	N	N	N
Verify	1	1	0	–	N	N	N
Testop	1	1	1	–	–	C	W

NNN	=	(1-5)	Spare Sector Number
C	=	1	Clear Seek Status Condition
P	=	1	Full Pack
P	=	0	Track Only
W	=	0	Normal Test OP
W	=	1	Remote Power Down
PLO	=	1	Enable Early/Late Strobe
E/L	=	1	Late Strobe
E/L	=	0	Early Strobe
S	=	1	Data Specified
S	=	0	Data = Address Field
OF	=	1	Offset
I	=	1	Offset In
I	=	0	Offset Out
F	=	1	Diagnostic Write Firecode
CR	=	1	Error Correction Read

Table 1-7. OP and Variant Decode

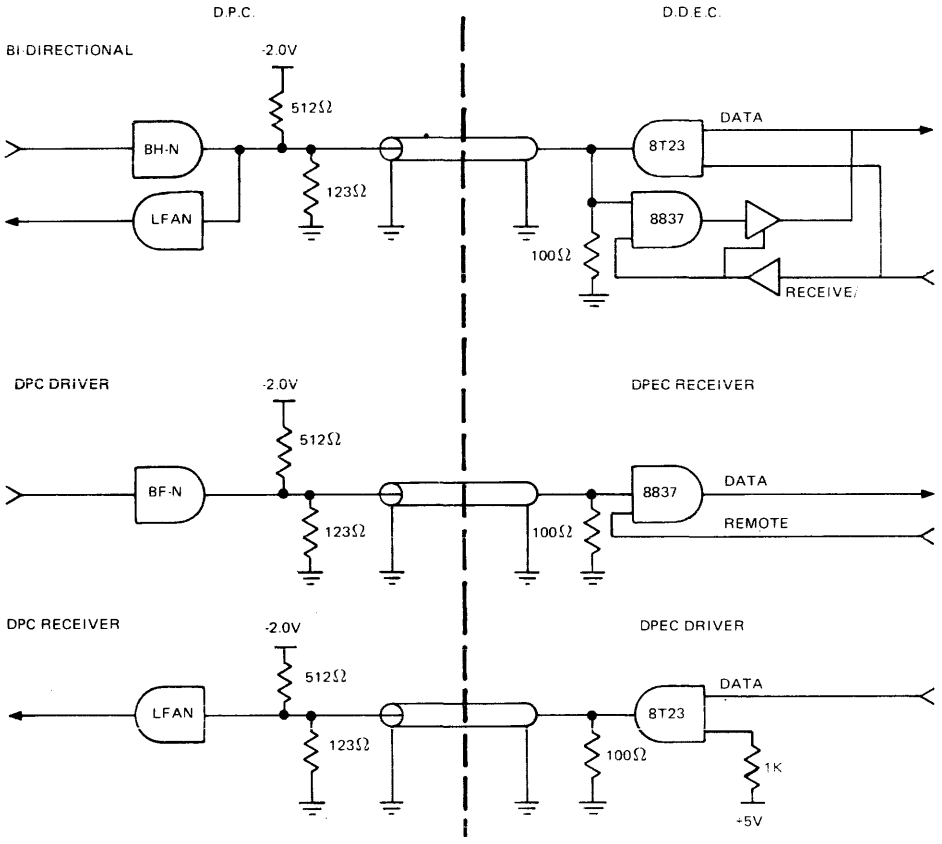


Figure 1-8. Interface Connections

Electrical Characteristics

Logical Levels

An interface line is logically false if it is in the range 0.0V to +0.4V at the receiving end of the line.

An interface line is logically true if it is in the range +2.4V to +5.0V at the receiving end of the line.

The switching time should not exceed 50 nanoseconds between the 90 percent and 10 percent points. The maximum cable length is 100 feet.

Figure 1-8 shows typical interface configurations. Figure 1-9 shows the pin designation, name, and direction of each signal.

Interface Lines and Timing

The eight control and status lines determine the timing and meaning of the data lines. The timing is determined by the CLOCK which goes from the DDEC to the DPC.

The following description should be followed using figures 1-9 and 1-10 as additional help in understanding.

SELECT line true indicates that the data lines contain the first initiate word.

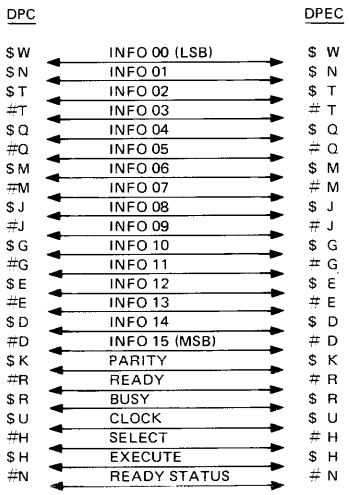


Figure 1-9. Line Details

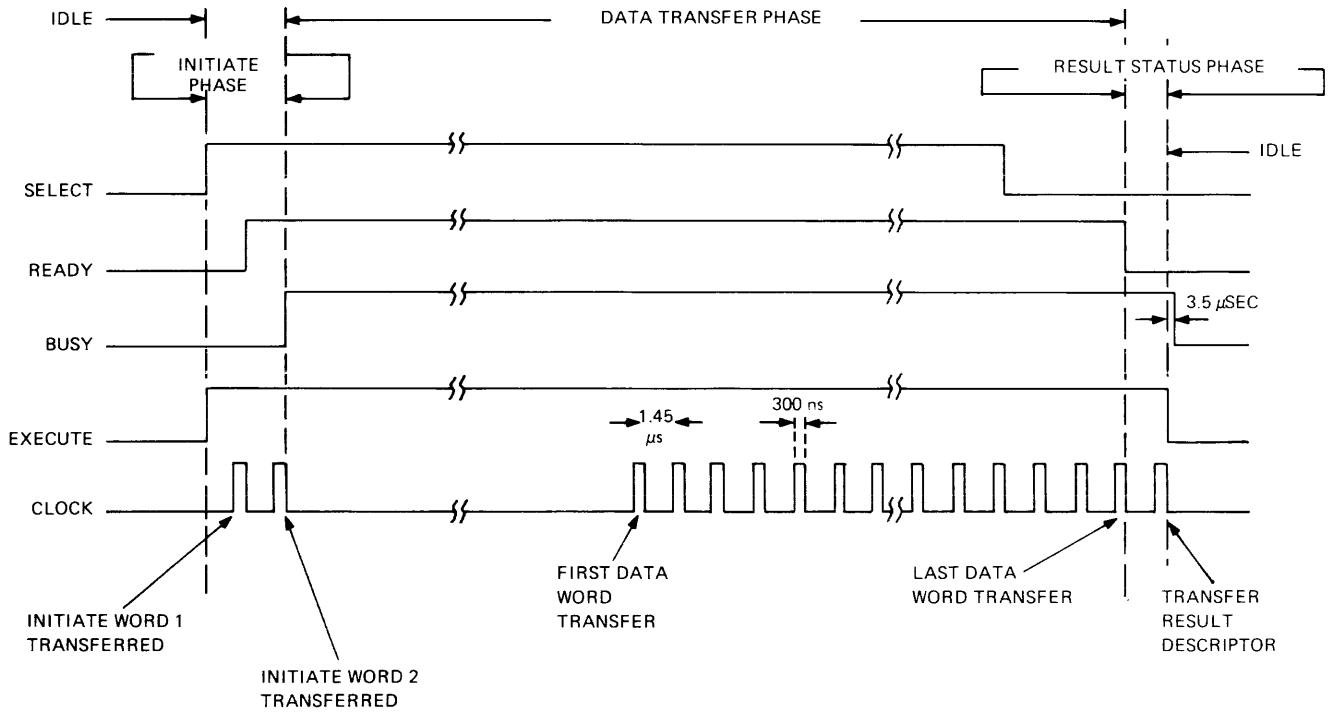


Figure 1-10. Typical Operation Terminated by DPC

READY*SELECT indicates that the data lines contain the second initiate word.

BUSY*READY*SELECT*EXECUTE indicates the data transfer phase. Data is transferred only when CLOCK pulses occur.

BUSY*READY*SELECT*EXECUTE/ indicates the data transfer phase but forces the DDEC into slip mode. Slip mode is forced when the DPC buffers are full during a READ or empty during a WRITE. Generally, the operation is suspended one revolution in order for the DPC to handle its buffers.

SELECT/*READY*BUSY indicates that the operation is terminated by the DPC. SELECT goes false before word 91 in order to terminate at the end of the sector. If SELECT goes false after word 92, the DDEC terminates at the end of the next sector.

SELECT/*READY/*BUSY indicates that the result descriptor information is on the data lines. This is the result status phase.

SELECT*BUSY*READY/ indicates that the DDEC has detected a serious error and is terminating the operation. When the DDEC DROPS READY, the DPC drops SELECT within one microsecond which indicates the result status phase as described above.

Parity is true when the MOD 2 sum of the information lines INFO NN is equal to zero (odd parity). Control and status lines are not checked.

READY STATUS true indicates that the DDEC is powered on, in remote, and ready to be selected. READY STATUS is false if the DDEC is in LOCAL.

CLOCK true informs the DPC that the data has been accepted during a WRITE or is stable on the lines during READ.

EXCHBUSY true informs the DPC that a drive on which it wants to act is busy with another controller. This only occurs with a dual port drive.

Result Descriptor Information

At the end of each operation, a result descriptor is sent to the DPC consisting of one word of information. Its purpose is to inform the DPC of any problems occurring during the operation. Table 1-8 gives the meanings of each bit.

Read Data Error

(FC ON MAINTENANCE PANEL)

indicates an error in the data field or firecode bytes. The DDEC does not terminate the operation if this occurs.

Write Lockout

(WL ON MAINTENANCE PANEL)

indicates that the drive is in a read only state (write enable switch not depressed), or the DDEC failed to send a write enable CM (controller message to drive) during a WRITE, INITIALIZE, or RELOCATE operation. This bit is also set at the end of an error correction read when correction has been attempted.

Information Lines	Result Descriptor
INFO 00	Read data error.
INFO 01	Write lockout or error correction used.
INFO 02	Seek status condition set.
INFO 03	Drive not ready.
INFO 04	Drive offline.
INFO 05	Drive unsafe.
INFO 06	Data sync error.
INFO 07	Sector address error.
INFO 08	Seek incomplete.
INFO 09	Drive not present.
INFO 10	Spare.
INFO 11	Spare.
INFO 12	Spare.
INFO 13	Spare.
INFO 14	Transmission parity error.
INFO 15	TRY DIAGNOSTICS.

Table 1-8. RD Bits

Seek Status

(SS ON THE MAINTENANCE PANEL)

indicates that the last operation on the selected drive is a SEEK, and a READ or WRITE operation has not taken place at the new cylinder. No other operation is permitted on the selected drive until a READ or WRITE has taken place. Seek status is the error if any other operation is attempted.

Drive Not Ready

(NR ON THE MAINTENANCE PANEL)

indicates that the drive positioner is not settled on a cylinder. The drive is not ready during a seek.

Drive Off-Line

(OL ON THE MAINTENANCE PANEL)

indicates that the drive is not up to speed and that the heads are not loaded.

Drive Unsafe

(US ON THE MAINTENANCE PANEL)

indicates the drive is unsafe. This could be due to:

1) DC power fault.
2) Temperature critical.
3) RPM low.
4) Carriage hits end stop.
5) In the 207 only, write current and no write gate. This condition could destroy servo-data on the disks.

Data Sync Error

(DS ON THE MAINTENANCE PANEL)

indicates a missing sync digit at the start of the data field (or failure to detect the sync digit).

Sector Address Error

(AE ON THE MAINTENANCE PANEL)

indicates the correct sector could not be found on the selected track or on the last head in the spare sectors allocated to that cylinder.

Seek Timeout

(ST ON THE MAINTENANCE PANEL)

indicates a seek incomplete condition in the drive.

Drive Not Present

(NP ON THE MAINTENANCE PANEL)

indicates that the drive selected is not present. The presence of a drive is detected by switches within the DDEC.

Transmission Parity

(TP ON THE MAINTENANCE PANEL)

indicates that the DDEC received a parity error on the information from the DPC. The interface line PARITY carries odd parity for the information lines (Refer to the interface lines and timing section).

Try Diagnostics

(TD ON THE MAINTENANCE PANEL)

indicates that the operation is not completed, and there is additional failure information. No further operations are permitted on that particular unit until a Read Extended Result Descriptor operation is performed. Other units continue to operate normally. If an operation is attempted on a unit with the TD bit set, the operation is terminated and a TD result descriptor is sent to the DPC.

The TD bit may be set from two sources:

1) A drive message containing a drive status fault or a controller message error.
2) The logic of the DDEC detecting various error conditions.

Extended Result Descriptor

At the end of an operation or when a TEST OP is performed, the DDEC transfers one word of result information. The 16 bits are described in the preceding pages. The TRY DIAGNOSTICS bit of the result descriptor locks up that unit until a READ EXTENDED STATUS OP is performed.

The Read Extended Status operation transfers four words of error information to the DPC. The central system logs this information for Field Engineering analysis. Since Extended Result Descriptors also convey information on intermittent errors, it is expected that the log analysis play an important role in analyzing these failures.

The DDEC only contains buffering for one ERD. If two or more units have TRY DIAGNOSTICS bits in their result descriptors, the ERD information only applies to the first unit. ERD information for the other units is lost. Examination of the unit number in word two of the ERD verifies to which unit the ERD belongs.

The READ ERD OP has no unit designation.

Table 1-9 gives the detailed content of the ERD. Bits 15-11 in Word 3 and bits 1 and 0 of Word 4 are generated in the DDEC. Word 1 and bits 15-10 in Word 2 give the DDEC decode (CYL,Head, and Sector) of the hexadecimal address supplied in the initiate words. Bits 09-00 give the OP, unit, and variants of the operation that failed.

Bits 10-00 of word 3 and bits 15-02 of word 4 are generated by the drive. Since drive information is stored in a shift register and originates from a DRIVE MESSAGE, the drive message bits (DMNN) and equivalent shift register bits (SRNN) are also given.

Each of the bits 10-00 in word 3 and 15-02 in word 4 can have two meanings. If bit 10 word 3 is 0, this indicates that bits 9 in word 3 through bit 2 of word 4 represent the drive status, represented in the left hand column. If bit 10 word 4 is 1, this indicates a CM error. In this case, bits 09 of word 3 through bit 02 of word 4 contain the CM in error. This information is returned by the drive. CM errors are represented in the right hand column of table 1-9.

Word 1

INFO	NN 15	Cyl	add 2*9	Address Decode
INFO	NN 14		add 2*8	
INFO	NN 13		add 2*7	
INFO	NN 12		add 2*6	
INFO	NN 11		add 2*5	
INFO	NN 10		add 2*4	
INFO	NN 09		add 2*3	
INFO	NN 08		add 2*2	
INFO	NN 07		add 2*1	
INFO	NN 06		add 2*0	
INFO	NN 05		add 2*10	
INFO	NN 04		Zero	
INFO	NN 03	Head	add 2*2	
INFO	NN 02	Head	add 2*1	
INFO	NN 01	Head	add 2*0	
INFO	NN 00	Sector	add 2*6	

Word 2

INFO	NN 15	Sector	add 2*5	Address Decode
INFO	NN 14		add 2*4	
INFO	NN 13		add 2*3	
INFO	NN 12		add 2*2	
INFO	NN 11		add 2*1	
INFO	NN 10	Sector	add 2*0	
INFO	NN 09	OP1		Command from DPC
INFO	NN 08	OP2		
INFO	NN 07	OP3		
INFO	NN 06	U4		
INFO	NN 05	U2		
INFO	NN 04	U1		
INFO	NN 03	N0		
INFO	NN 02	N1		
INFO	NN 01	N2		
INFO	NN 00	N3		

Word 3

INFO	NN 15	Fan Fail	
INFO	NN 14	Drive Clock OK/	
INFO	NN 13	Address Mark Missing	
INFO	NN 12	No Read Data Transitions	
INFO	NN 11	Index Mark Missing	
INFO	NN 10	CM Error = 0	CM Error = 1
INFO	NN 09	DM09 *SR01 - 206	CM01 - Mark
INFO	NN 08	DM10 *SR02 - 207	CM02 - Write/
INFO	NN 07	DM11 *SR03 - 0	CM03 - Read/
INFO	NN 06	DM12 *SR04 - 0	CM04 - Address Mark (206) Servo Search/ (207)
INFO	NN 05	DM13 *SR05 - Maintenance Mode	CM05 - Parity Even
INFO	NN 04	DM14 *SR06 - Write Data Missing	CM06 - Continue
INFO	NN 03	DM15 *SR07 - 0	CM07 - Address/Control
INFO	NN 02	DM16 *SR08 - Seek and not ready	CM08 - Head or Cyl/Offset on (206)
INFO	NN 01	DM17 *SR09 - Illegal head	CM09 - Add Info - Offset in (206)
INFO	NN 00	DM18 *SR10 - Illegal cylinder	CM10 - Add Info - Data Strobe Early

Word 4

INFO NN 15	DM19 *SR11	Spindle address error.	CM11 - Add Info - Data strobe late.
INFO NN 14	DM20 *SR12	Offset during write enable (206) - 0 (207) (206) - 0 (207)	CM12 - Add Info - Power up
INFO NN 13	DM21 *SR13	Offset during seek (206) - 0 (207)	CM13 - Add Info - Power down
INFO NN 12	DM22 *SR14	Seek incomplete	CM14 - Add info - restore
INFO NN 11	DM23 *SR15	Offtrack and Write	CM15 - Add info - Send status
INFO NN 10	DM24 *SR16	Carriage hits stop	CM16 - Add info - Find index
INFO NN 09	DM25 *SR17	0 (206) - Servo lost (207)	CM17 - Add info - 0
INFO NN 08	DM26 *SR18	Write current and no gate	CM18 - Add info - 0
INFO NN 07	DM27 *SR19	No MFM transitions (206, 207) or drive clock error (207)	
INFO NN 06	DM28 *SR20	Head select fault	CM20 - Add info - Set maint.
INFO NN 05	DM29 *SR21	DC power fault	CM21 - Write enable
INFO NN 04	DM30 *SR22	Temperature warning	CM22 - 0
INFO NN 03	DM31 *SR23	Temperature critical	CM23 - Parity even
INFO NN 02	DM32 *SR24	RPM less than 3420	CM24 - End
INFO NN 01	Bad DM response		
INFO NN 00	Address overflow		

Table 1-9. ERD Information

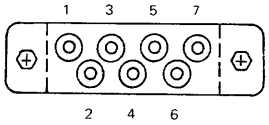
INTERFACE, DDEC TO DRIVE

Physical Characteristics

The DDEC and Drive communicate on a 4-signal, 6-wire interface. The four signals are:

CM (Controller Message)
DM (Drive Message)
CLOCK
DATA

The signals CLOCK and DATA are differential, requiring two lines each. Differential lines are used for noise rejection. The basic drive I/O cable is a 25-wire coaxial cable with an edge connector at the DDEC end. The 25 coaxial cables are split into four groups of six wires each to form the 1 x 4 cable. The edge connector wiring is given in table 1-10. The drive connector is given in figure 1-11.



PIN CONFIGURATION

PIN	SIGNAL NAME
1	CLOCK P
2	CLOCK N
3	DATAP
4	DATAN
5	CONTROLLER MESSAGE (CM)
6	DRIVE MESSAGE (DM)
7	SPARE

Figure 1-11. Drive Connector

Signal Description		PWB Edge Signal Lead	Connector Pin Ground Lead
CM	SPINDLE 1	$D	$C
DATA P	SPINDLE 1	$E	$F
DATA N	SPINDLE 1	$G	$F
CLOCK P	SPINDLE 1	$H	$I
CLOCK N	SPINDLE 1	$J	$I
DM	SPINDLE 1	$K	$L
DM	SPINDLE 2	$M	$L
CLOCK N	SPINDLE 2	$N	$P
CLOCK P	SPINDLE 2	$Q	$P
DATA N	SPINDLE 2	$R	$S
DATA P	SPINDLE 2	$T	$S
CM	SPINDLE 2	$U	$V
CM	SPINDLE 3	#D	#C
DATA P	SPINDLE 3	#E	#F
DATA N	SPINDLE 3	#G	#F
CLOCK P	SPINDLE 3	#H	#I
CLOCK N	SPINDLE 3	#J	#I
DM	SPINDLE 3	#K	#L
DM	SPINDLE 4	#M	#L
CLOCK N	SPINDLE 4	#N	#P
CLOCK P	SPINDLE 4	#Q	#P
DATA N	SPINDLE 4	#R	#S
DATA P	SPINDLE 4	#T	#S
CM	SPINDLE 4	#U	#V

Table 1-10. Edge Connector Wiring

Controller Message (CM)

The DDEC communicates with the drive through the CM line. Message information is passed serially on the line. The CM is either six bits or 24 bits long. Each CM bit is two clock periods (202 nano seconds) long. Figure 1-12 shows the CM format. Each CM is protected by parity. Bit 5 protects bits 1 through 5. Bit 23 protects bits 1 through 23. Table 1-11 explains each bit.

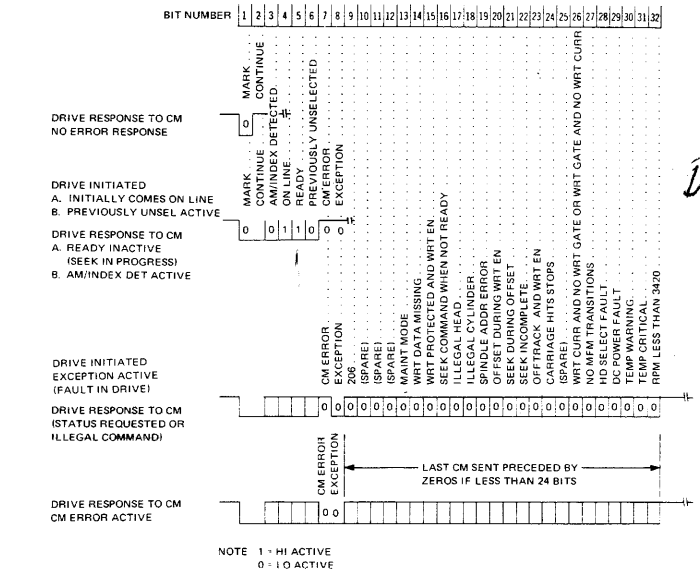


Figure 1-12. DM and CM Bits

CM

Before any communication may take place, the drive must be SELECTED. The DDEC selects a drive by making the CM line high. The drive is DE-SELECTED by the DDEC when the CM line goes low for five or more bit times. When the drive is unselected, it cannot send a drive message.

When a long CM is sent, bits 8 through 22 have different meanings depending on bits 7 and 8.

Figure 1-12 shows the format for drive and controller messages. Table 1-11 gives an explanation for each CM bit and the 207 differences.

Bit	206 Name	206 Function	207 Name	207 Function
1	MARK	Low indicates beginning of message.	MARK	Low indicates beginning of message.
2	WRITE	High starts a write operation when bit 6 is received correctly and WRITE ENABLE has been previously set. Low terminates write immediately.	WRITE	Same as 206.
3	READ	High starts read when bit 6 is received with no parity error. No parity error.	READ	Same as 206.
4	ADDRESS MARK	High with bit 3 indicates READ ADDRESS MARK. The search for address mark is reset by A.M. detection. High with bit 2 indicates WRITE ADDRESS MARK. Action starts when bit 6 is received with no errors.	SYNC SEARCH	High with bit 3 indicates SERVO SYNC SEARCH. Reset by servo sync detection. High with bit 2 indicates start write after guard band 2. This message is sent when the address is to be written on the pack. The search begins when bit 6 is received with no errors.
5	PARITY	Provides parity on bits 1-5 such that the number of low bits 1-5 is even. If a parity error occurs, operations indicated by the previous bits are not initiated, no further bits are processed and a DM with bit 6 high is initiated.	PARITY	Same as 206.
6	CONTINUE	Low indicates that this is a 24-bit CM. High indicates that this is a 6-bit DM. Bits 2 or 3 high with bit 6 low is an error condition. WRITE operations are prohibited and a DM with bit 6 high is initiated.	CONTINUE	Same as 206.
7	CONTROL	When high indicates that bits 8 through 24 are control bits. When low, definition of bits 8 through 24 is determined by bit 8.	CONTROL	Same as 206.
		DEFINITION OF BITS 8 THROUGH 24 WHEN BIT 7 is HIGH (CONTROL CM)		
8	OFFSET ON	When Low, indicates that the heads are to be offset. Bit 8 determines the direction of offset.	UNASSIGNED	
9	OFFSET IN	When Low, indicates that offset is towards the spindle. Action occurs at bit 24 time.	UNASSIGNED	
10	DATA STROBE EARLY	Low indicates that read data is detected with early strobe. Used to recover data errors.	DATA STROBE EARLY	Same as 206.
11	DATA STROBE LATE	Low indicates that read data is detected with late strobe. Used to recover data errors.	DATA STROBE EARLY	Same as 206.
12	POWER UP	Low indicates a power up, assuming that no interlock or fault conditions occur. Action occurs at bit 24.	POWER UP	Same as 206.
13	POWER DOWN	Low indicates that the drive should power down at bit 24 time.	POWER DOWN	Same as 206.
14	REZERO	Low causes a slow speed retraction to the outer guard band and then forward to cylinder zero.	RTZ	Low specified return return to cylinder zero, head zero. Resets illegal cylinder.
15	SEND STATUS	Low sets the drive exception bit and causes a long DM containing the 24-bit drive Status Register.	READ STATUS	Same as 206.
16	CHECK INDEX	When low, specifies that the drive returns a DM, when the next index mark is detected.	CHECK INDEX	Same as 206.

Table 1-11. Controller Message

CM

Bit	206 Name	206 Function	207 Name	207 Function
17	SPARE		SPARE	
18	SPARE		SPARE	
19	RESET MAINT. MODE	When low, maintenance mode is reset.	RESET MAINT. MODE	Same as 206.
20	SET MAINT. MODE	When low, sets maintenance mode flip-flop. Spindle address 64 is active. Remote power ups and downs are prohibited.	SET MAINT. MODE	Same as 206.
21	SPARE		SPARE	
23	PARITY	Parity is sent in a state such that the number of low bits 1-23 is even. If the drive receives a CM with incorrect parity, the operation is not performed and a DM is returned with bit 7 low.	PARITY	Same as 206.
24	END	Must be high. If this bit is low, this is an error condition. No operations are performed, and a DM with bit 7 low is returned.	END	Same as 206.
	DEFINITION OF BITS 8 THROUGH 24 WHEN BIT 7 LOW AND BIT 8 HIGH (CYL CM)			
8		High indicates cylinder to follow. This is a SEEK command.		Same as 206.
9	CYL 1	Cylinder bit 1	Cyl 1	Same as 206.
10	CYL 2	Cylinder Bit 2	Cyl 2	Same as 206.
11	CYL 4	Cylinder bit 4	Cyl 4	Same as 206.
12	CYL 8	Cylinder bit 8	Cyl 8	Same as 206.
13	CYL 16	Cylinder bit 16	Cyl 16	Same as 206.
14	CYL 32	Cylinder bit 32	Cyl 32	Same as 206.
15	CYL 64	Cylinder bit 64	Cyl 64	Same as 206.
16	CYL 128	Cylinder bit 128	Cyl 128	Same as 206.
17	CYL 256	Cylinder bit 256	Cyl 256	Same as 206.
18	CYL 512	Cylinder bit 512	Cyl 512	Same as 206.
19	SPARE		Cyl 1024	Cylinder bit 1024.
20	SPARE		SPARE	
21	SPARE		SPARE	
22	SPARE		SPARE	
23	PARITY	Even parity on bits 1-23.	PARITY	Same as 206.
24	END	Must be high.	END	Must be high
	DEFINITION OF BITS 8 THROUGH 24 WHEN BIT 7 IS LOW AND BIT 8 IS LOW			
8		When low, indicates a spindle and head address follows.		Same as 206.
9	HD 1	Head 1 bit	Hd 1	Head 1 bit
10	HD 2	Head 2 bit	Hd 2	Head 2 bit
11	HD 4	Head 4 bit	Hd 4	Head 4 bit
12	HD 8	Unused	Hd 8	Unused
13	HD 16	Unused	Hd 16	Unused
14	SPIND AD 1	Spindle address 1	SPIND AD 1	Spindle address 1
15	SPIND AD 2	Spindle address 2	SPIND AD 2	Spindle address 2
16	SPIND AD 4	Spindle address 4	SPIND AD 4	Spindle address 4
17	SPIND AD 8	Spindle address 8	SPIND AD 8	Spindle address 8
18	SPIND AD 16	Spindle address 16	SPIND AD 16	Spindle address 16
19	SPIND AD 32	Spindle address 32	SPIND AD 32	Spindle address 32
20	SPIND AD 64	Spindle address 64	SPIND AD 64	Spindle address 64

Table 1-11. Controller Message (cont)

Bit	206 Name	206 Function	207 Name	207 Function
21	WRITE ENABLE	Low sets write enable. Write enable is reset by this bit high, a cylinder CM, drive deselection, or any error condition.	WRITE ENABLE	Same as 206.
22	SPIND Only	Low indicates only a spindle CM, head switch not required.	SPIND Only	Low indicates only a spindle CM, head switch not required.
23	PARITY	Even parity on bits 1-23.	PARITY	Same as 206.
24	END	Must be high.	END	Must be high.

Table 1-11. Controller Message (cont)

Drive Message (DM)

The drive communicates with the DDEC via the drive message line. Bits are sent serially at half clock speed (202 nano-second bit time). A DM may only be sent if the drive is selected; however, status is stored in the drive and is sent when the drive is selected. There are three kinds of DM's: a 1-bit, an 8-bit, and a 32-bit.

The 1-bit DM consists of a mark bit only (see figure 1-11). The 1-bit DM is used to acknowledge receipt of a CM without error. In DDEC terms, it is known as a "ROGERDM". It is also used when the drive completes a seek operation.

The 8-bit DM is sent to the DDEC when three conditions occur:

1) When the drive is selected it returns the status of the drive (ON LINE, READY, etc.).
2) In response to a READ ADDRESS MARK (SYNC SEARCH-207) or CHECK INDEX when AM, servo field or index is detected.
3) When a seek operation starts (READY LOW).

The 32-bit DM is used to transfer the drive STATUS REGISTER or the contents of a CM which is in error. The 32-bit CM is initiated by the drive when an error is detected. It is also initiated in response to a SEND STATUS CM from the DDEC.

The drive STATUS REGISTER contains information about the type of drive and various error conditions that are detected in the drive. These conditions are listed in table 1-12.

When a CM is in error, bit 7 (CM ERROR) is made low, bit 8 is low (EXCEPTION), and the CM in error is echoed back to the DDEC.

The DDEC passes this information to the host for logging and subsequent Field Engineering analysis.

When a DM is being sent, the CM line is ignored.

Bit	206 Name	206 Function	207 Name	207 Function
1	MARK	Low indicates beginning of message	MARK	Same as 206.
2	CONTINUE	High indicates the last CM has been received without error. The drive is ready and there are no exceptions. Low indicates that the DM is continuing.	CONTINUE	Same as 206.
3	AM/INDEX	Address or index mark detected (low). Sent in response to a Read Address Mark or Check Index.	SERVO SYNC/INDEX DET.	Low indicates that the servo sync field has been detected in response to a servo sync search, or index is detected in response to Check Index.
4	ON LINE	High indicates that the drive is up to speed, and the heads are loaded.	ON LINE	Same as 206.
5	READY	High indicates that the drive is online, and the heads are on a cylinder (not seeking) when a seek is completed READY goes from LOW to HIGH generating a DM	READY	Same as 206.

Table 1-12. Drive Message

Bit	206 Name	206 Function	207 Name	207 Function
6	PREVIOUSLY UNSELECTED	Low when the drive goes from unselected to selected. This condition causes the generation of a DM (8 Bit). However, bit 6 is not used in the DDEC.	PREVIOUSLY UNSELECTED	Same as 206.
7	CM ERROR	Low indicates a CM error (parity error or control bit conflicts). This bit causes a 32-bit DM to be generated. Bits 9-32 contain the last CM sent to the drive (preceded by zeros if the CM is less than 24 bits). High indicates that bits 9 through 32 contain drive status bits (provided bit 8 is low).		Same as 206.
8	EXCEPTION	Low indicates a long DM and that an error condition exists. Bit 8 low causes generation of a 32-bit DM. Bit 8 is made low by an error condition or by the SEND STATUS CM from the DDEC.	EXCEPTION	Same as 206.
		DEFINITION OF STATUS BITS 9-32		
9	206	Low indicates a 206 drive.	NOT USED	
10	NOT USED		207	Low indicates a 207 spindle. High indicates not a 207 drive.
11	100/180	High indicates 180 bytes per sector. Low indicates 100 bytes per sector.	NOT USED	
12	SEQUENTIAL INTERLACE	Low for sequential format, high for interlace format.	NOT USED	
13	MAINT. MODE	Low indicates that the drive is in maintenance mode.	MAINTENANCE MODE	Same as 206.
14	WRITE DATA MISSING	Low if the data line has no transitions during a WRITE. Reported at the end of the WRITE.	WRITE DATA MISSING	Same as 206.
15	WRITE PROTECTED AND WRITE ENABLE	Low if the WRITE ENABLE switch is not in the WRITE ENABLE position, and a WRITE ENABLE command is sent. Also, low if a WRITE command is received (Bit 2 CM), and the drive has not previously received a WRITE ENABLE command.	WRITE PROTECTED AND WRITE ENABLE	Same as 206.
16	SEEK COMMAND WHEN NOT READY	Low if a cylinder CM is received, and the drive is not ready.	SEEK COMMAND	Same as 206.
17	ILLEGAL HEAD	Low if head address is greater than 4.	ILLEGAL HEAD	Low if the head address received is greater than 7.
18	ILLEGAL CYLINDER	Low if the cylinder address received is greater than 814. Reset by a rezero CM.	ILLEGAL CYLINDER	Low if the cylinder address received is greater than 1563. Reset by a rezero CM.
19	SPINDLE ADDRESS ERROR	Low if the spindle address received does not agree with the spindle address jumpers in the drive.	SPINDLE ADDRESS ERROR	Same as 206.
20	OFFSET DURING WRITE ENABLE	Low if an offset CM is received, and the unit is in write enable state.	NOT USED	

Table 1-12. Drive Message (cont)

Bit	206 Name	206 Function	207 Name	207 Function
21	OFFSET DURING SEEK	Low if an offset CM is received during a SEEK, or a SEEK CM is received while the drive is offset.	NOT USED	
22	SEEK INCOMPLETE	Low if a SEEK took more than 700 ms to complete.	SEEK INCOMPLETE	Same as 206.
23	OFF TRACK AND WRITE	Low if the heads are not within 500 micro-inches of track center, and write is on.	OFF TRACK AND WRITE	Low if the heads are not within 200 micro-inches of track center, and write is on.
24	END STOP	Low if the carriage hits either end stop. Causes an emergency retract. A power down is required to reset.	END STOP	Same as 206.
25	SPARE	Held high.	SERVO-ERROR	Servo tracking circuit in error.
26	WRITE CURRENT AND NO WRITE GATE OR WRITE GATE AND NO WRITE CURRENT	Low when write. Current is sensed and no WRITE command , or when no write current is sensed during WRITE.	WRITE CURRENT AND NO WRITE GATE OR WRITE GATE AND NO WRITE CURRENT	Same as 206.
27	NO MFM TRANSITIONS	Low if there are no MFM transitions during a WRITE.	NO MFM TRANSITIONS OR DRIVE CLOCK ERROR	Low if there are no MFM transitions during a WRITE, or if there is a drive clock error.
28	HEAD SELECT FAULT	Low if no heads are selected or more than one head is selected during READ or WRITE.	HEAD SELECT FAULT	Same as 206.
29	DC UNSAFE	Low if +5V, +12V, or 12V is low on the servo card in the drive.	DC UNSAFE	DC voltages out of limits.
30	TEMPERATURE WARNING	Low when the air exiting from the linear motor is 80° C.	TEMPERATURE WARNING	Low when the air from the linear motor is 80° C.
31	TEMPERATURE CRITICAL	Low when the air exiting from the linear motor is 88° C.	TEMPERATURE CRITICAL	Low when the air from the linear motor is 85° C.
32	RPM LOW	Low if the drive spindle drops below 3420 R.P.M.	R.P.M. LOW	Same as 206.

Table 1-12. Drive Message (cont)

Clock

The clock originates in the drive and is sent to the DDEC. The bit time is 101 nano seconds for the 206 (9.86 MHz). For the 207, the bit time is 92 ns (10.71 MHz).

Data

Data is bi-directional NRZ data, synchronized with the clock. Data transfers from the DDEC to the drive during WRITE and from the drive to the DDEC during READ.

Electrical Characteristics

Logical Levels

Figure 1-13 shows the interface arrangement. The logical levels for the CM and DM are listed below:

Logical High +2.5V to +4.0V.
Logical Low 0.0V to +0.2V.

The logical levels for the CLOCK and DATA signals are listed below:

Logical High +0.2V to +0.8V.
Logical Low 0.2V to 0.8V.

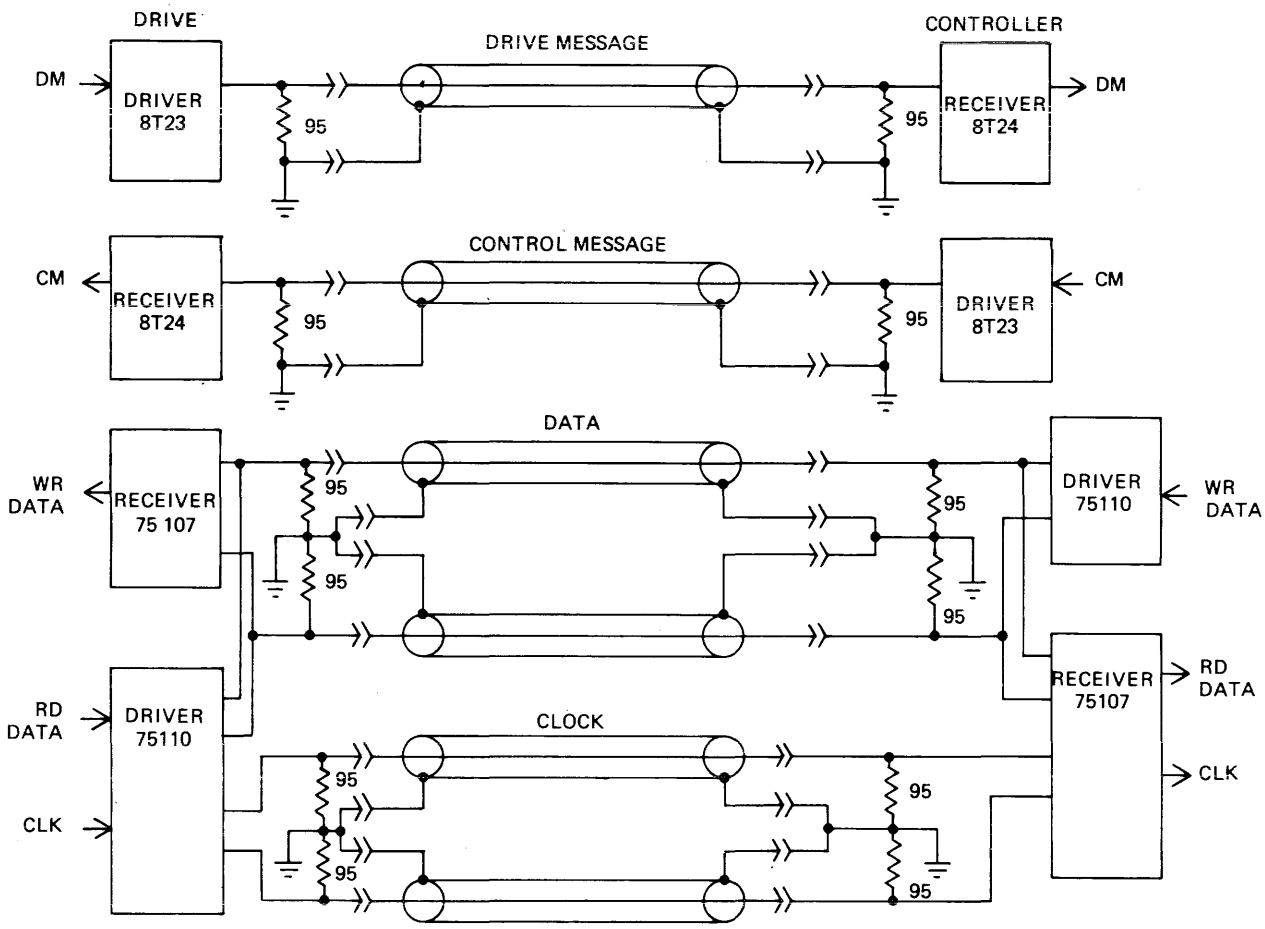


Figure 1-13. Drive Interface

FUNCTIONS

General Description

Each of the functions performed by the DDEC is described below. A basic flow chart is included. The 207 functions that are different to the 206 functions are described in later flow charts. (See figure 1-14).

The numbers at the top right of each block are the DDEC Modes. They are explained in the next section.

Power UP (206 and 207)

When the DDEC is powered on, a reset pulse occurs for 25 seconds. This time is necessary so that any drives powered on at the same time may complete their power up brake cycles. The reset pulse clears various flip-flops and counters within the DDEC.

At the completion of the reset pulse, the DDEC attempts to power up each drive. A power up command is sent to each drive that has AC power on. The DDEC starts with unit 0 and progresses to unit 7. When a power up command is sent, the DDEC waits eight seconds before going on to the next drive. This action prevents an overload of the circuit breakers caused by the start current of the drive motors.

When all the drives are complete, the DDEC goes into idle mode waiting for a command from the processor.

Initial OP Processing

See figure 1-15 for the following discussion.

Initial OP processing is the process of receiving a command from the disk pack controller. It is common to all operations. It is described here; however, in future flows it is shown as a single block.

As described previously, the command from the DPC consists of two initiate words of 16 bits each. The first contains the OP code, variants, and part of the address; the second contains address only information.

The three main functions performed are:

1) Receive initiate words.
2) Convert the binary sector address to cylinder, head and sector.
3) Test for error conditions.

The initial OP processing is described in a later section in detail.

Addresses are sent in binary from the DPC. Some examples illustrate the arrangement for the 206:

Binary	Decimal	Cylinder	Head	Sector
000000	000000	000	0	00
000001	000001	000	0	01
00000A	000010	000	0	10
00005C	000090	000	1	00
0001BE	000446	001	0	00

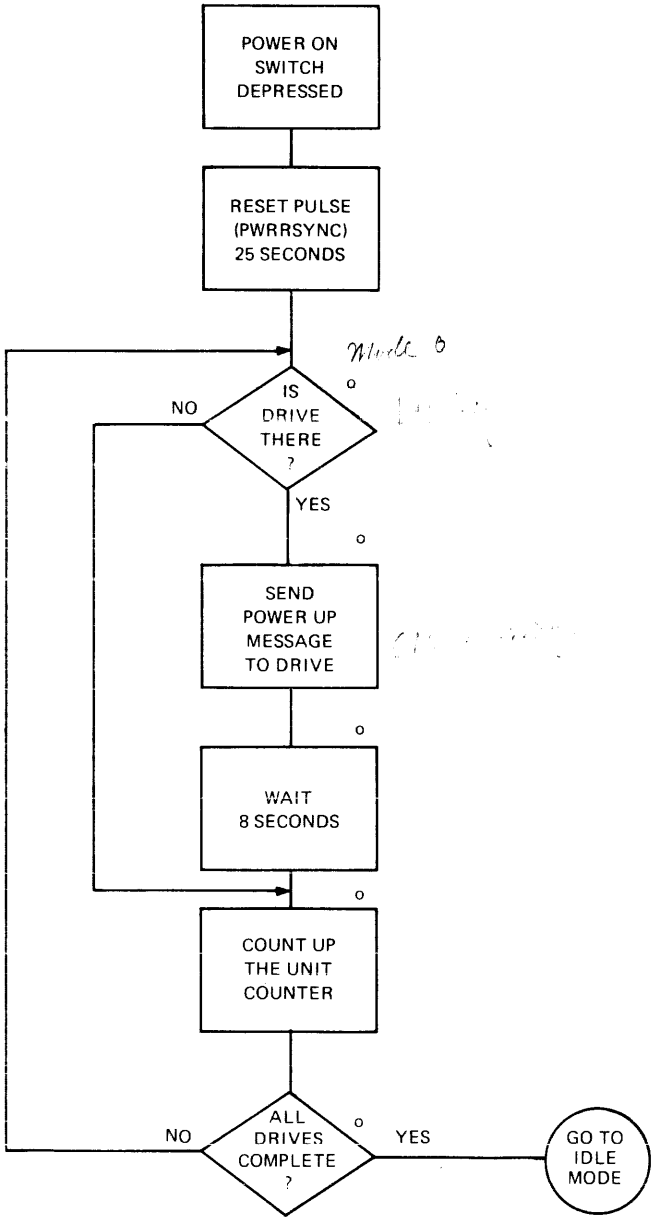


Figure 1-14. Spindle Spinup (206 and 207)

At the time of writing, a printout of binary and decimal addresses is available from the B1700 Test Routine. Use the options DECODE or PACK ADDRESS.

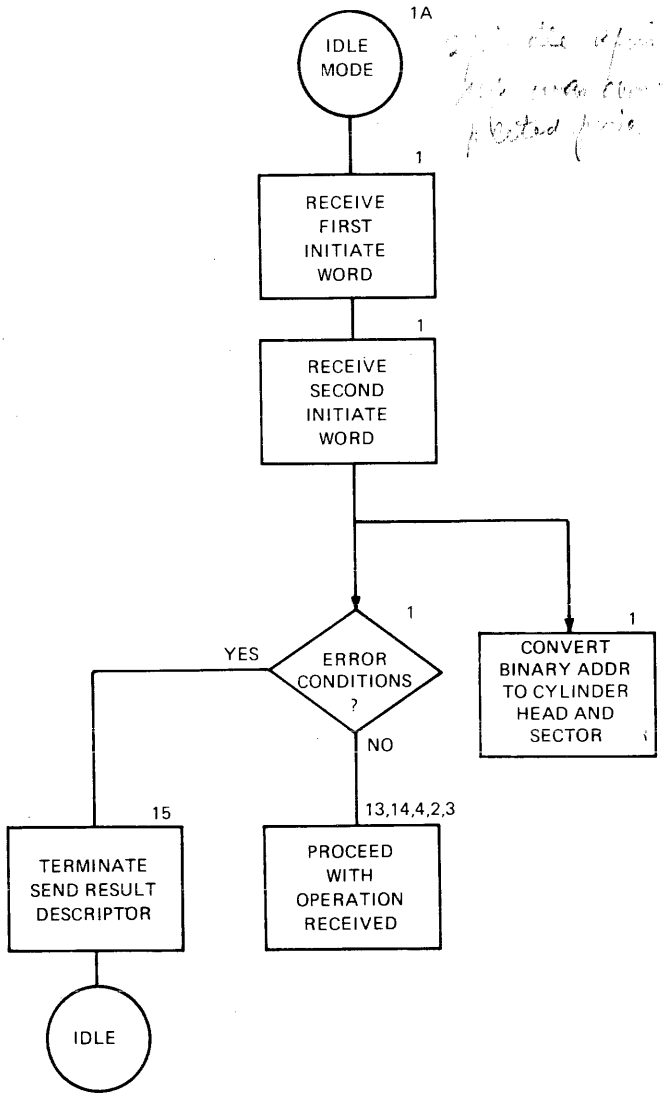


Figure 1-15. Initial OP Processing

INITIALIZE (206)

INITIALIZE is the operation used to format each track. This means writing the Beginning-of-Track (BOT), all the sectors (90), and the End-of-Track (EOT). In each sector, the address mark, address preamble, sync character, address, EPC data preamble, data sync character, data field, data firecode, and the End-of-Record are written.

Two options are available:

1) Single track or full pack INITIALIZE.
2) Write the data field with data supplied by the processor, or write the data field with address information supplied by the DDEC.

When the single track option is used, the address of the first sector in the track is sent in the initiate words. When the full pack option is used, the operation starts at the address sent and continues to the end of the pack. Generally, the beginning address of a full pack initialize is zero.

Data is always written in the data field. If the option specifies data from the processor, the DDEC accepts one data word and repeats this word 90 times. If data is specified from the DDEC, the two address words are repeated 45 times. (See figure 1-16).

Initialize (207)

INITIALIZE on the 207 consists of writing the address preamble, sector address, data preamble, data, EPC, and End-of-Record. This is repeated for every sector on the track. If the operation is not a single track INITIALIZE, this is repeated throughout all tracks until the end of the pack is reached.

Note that the servo field, guard band 1, and guard band 2 are not written during INITIALIZE. This information is recorded on the disks at the manufacturing plant and is never overwritten.

Another difference between the 206 and 207 is the absence of an end-of-track and beginning-of-track gap.

The options specified are identical to the 206. (See figure 1-17).

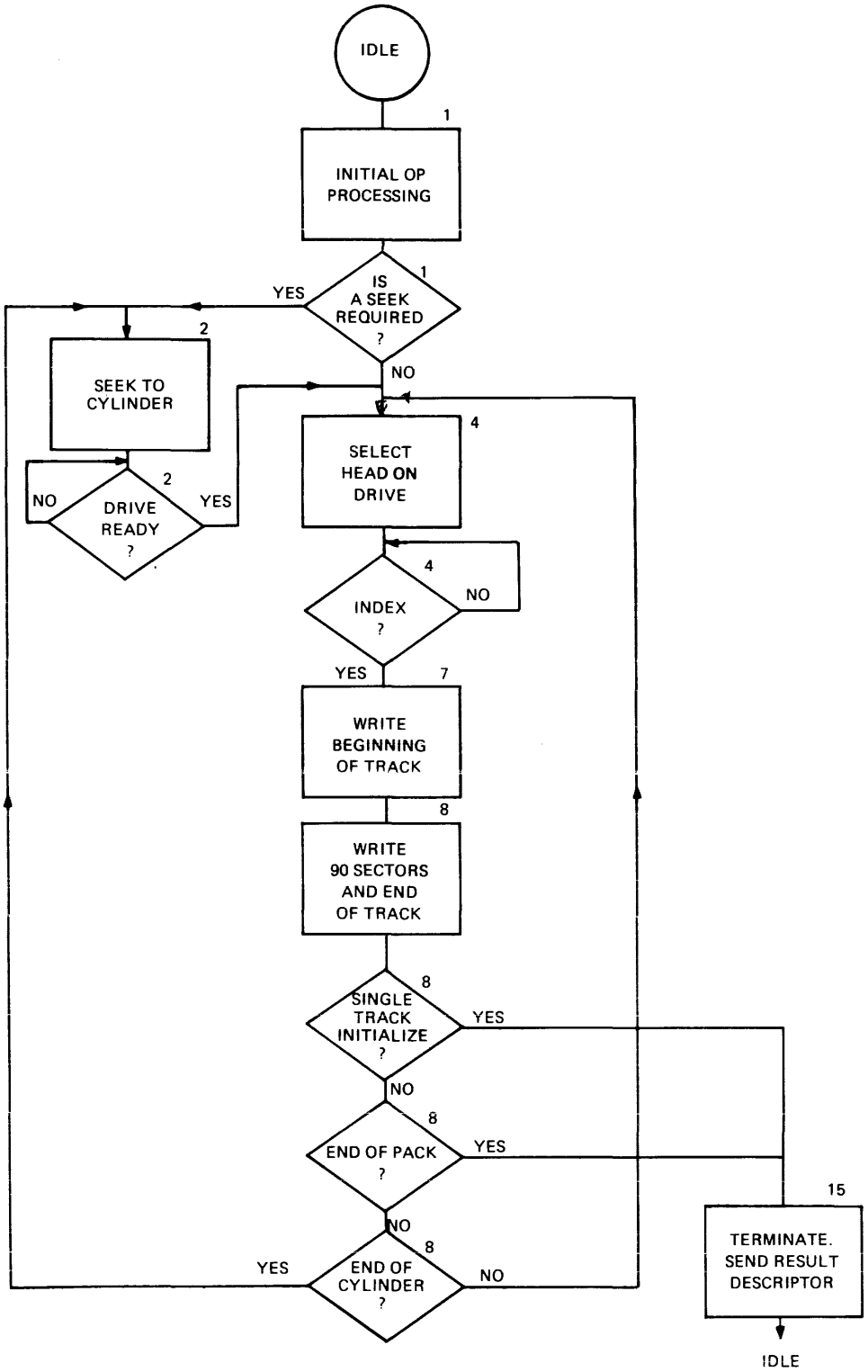


Figure 1-16. Initialize (206)

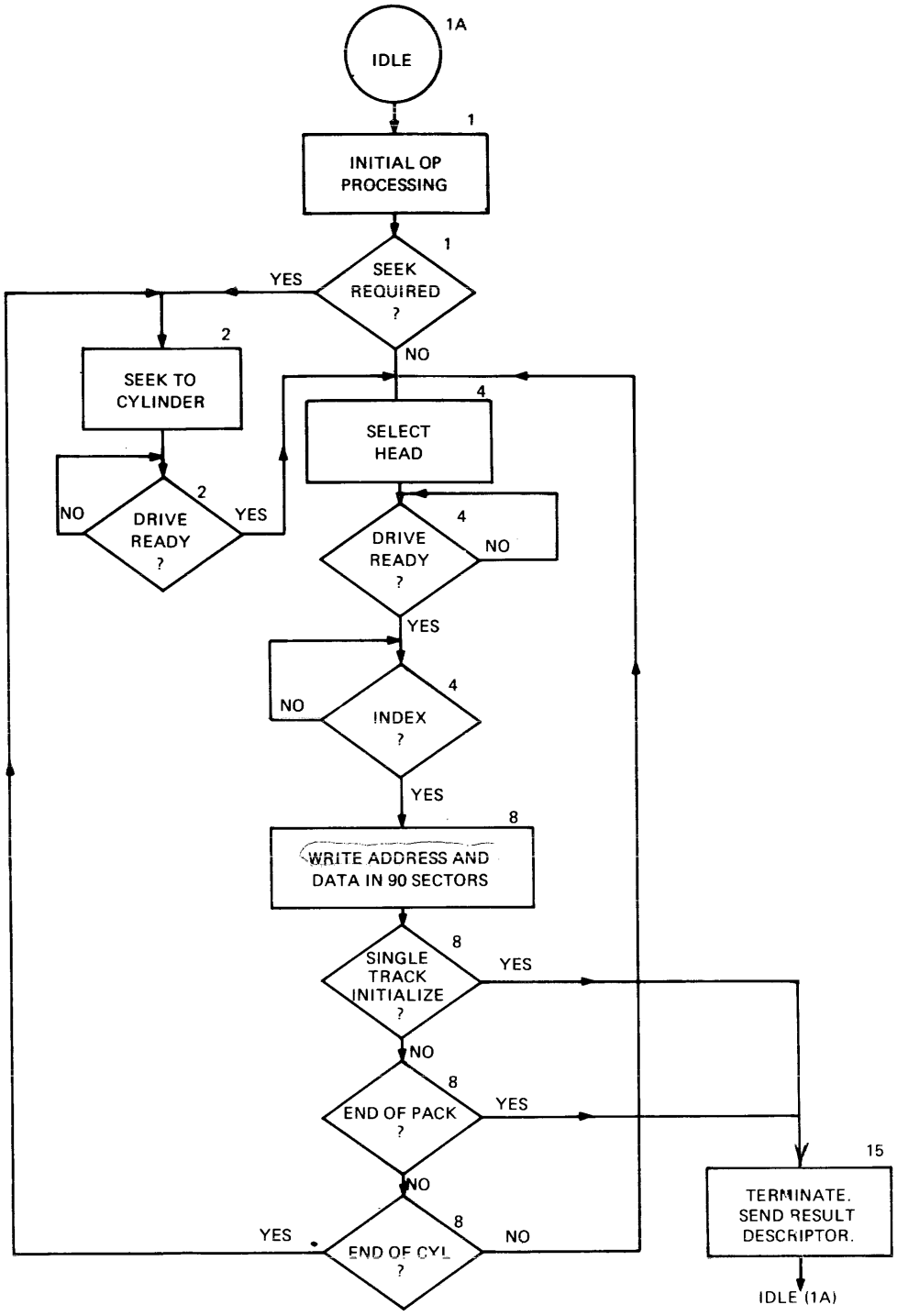


Figure 1-17. Initialize (207)

READ, WRITE, and VERIFY (206)

These three operations are very similar. They are all represented by one flow chart. The major difference is in the block marked DATA TRANSFER. During a WRITE, data and firecode are written onto the sector at this time. During a READ or VERIFY, data is transferred from the drive to the DDEC. The difference between READ and VERIFY is that VERIFY is a one sector operation if the N variants are on. In this case, it is a spare sector verify.

When the initial OP processing is complete, the DDEC determines whether a seek operation is necessary on the drive. This is determined by comparing the new cylinder address to the last cylinder address used. If they are the same (OLD = NEW), a

seek is not required. If they are not equal, a cylinder CM is sent to the drive, the seek status flag for that drive is set, and the operation is terminated.

When a seek is in progress, the controller is free to perform an operation on one of the other drives. This is known as an OVERLAPPING SEEK.

If the heads are on the correct cylinder, the required head is selected with a head CM. The address field of each sector being read from the disk is then compared to the starting address supplied in the initiate word. If the correct address has not been found in 128 sectors, the assumption is made that the sector may have been relocated into the spare sectors on head 4. Therefore, a head switch to head 4 is made, and the sectors on head 4 are searched. If the address is not found in another 128 sectors, the operation is terminated. A REZEROCM is sent to the drive, and an address error result descriptor is sent to the DPC.

If the sector address has been found, the data transfer is started. If the operation is a WRITE, data is supplied to the drive in serial form. A new data word is requested (DPC CLOCK) from the DPC every 16 bits. Data is converted from a parallel flow to a serial flow in the DDEC.

During the WRITE of a sector, the DDEC builds up the firecode. Immediately after the last data bit of the sector is written, the firecode is written.

During a READ or VERIFY data transfer, data from the drive is sent to the DDEC. Data is converted from serial flow to parallel. Sixteen bits are transferred with each DPC CLOCK pulse to the controller.

During READ or VERIFY, the DDEC builds up a new firecode from the data being read. Immediately after the last data bit is read, the firecode previously written is read. This is compared bit by bit with the firecode generated during the READ. If they do not agree, this indicates an error in the data (or firecode). A firecode error does not terminate the operation. At the end of each sector, a result descriptor is sent to the DPC. The firecode error bit is set if a firecode error occurs.

The operation is normally terminated by the processor dropping SELECT false during the sector. If SELECT remains high, the operation continues. The DDEC goes back into address search mode to search for the next sector. Address comparison is made on every sector. If the end-of-track is reached or the end of a relocated sector, a head switch is performed. If the end of cylinder is reached, a seek and a head switch is performed. If the end of the pack is reached before SELECT goes false, the operation is terminated.

When SELECT goes low, or at the end of a spare sector verify (which is a one sector operation) the DDEC terminates and sends a result descriptor. It then goes idle, waiting for the next command. (See figure 1-18).

READ, WRITE, and VERIFY (207)

READ, WRITE, and VERIFY is the same as the 206 operation except for the following items:

1) The spare sectors are located on head 7 on the 207; therefore when 128 addresses have been compared without an equal comparison, a head switch to head 7 is performed.
2) During a READ or VERIFY operation, a firecode error is detected in a different manner. In the 207, the data and firecode read from the disk are used in the generation of a new code. In addition, a pre-multiplication polynomial is added (explained in section 4). If the data and firecode have been written correctly and read back correctly, the firecode register contains all zeros. If the register is not zero, then FIRECODE ERROR is generated.
3) During a READ with error correction, the data is stored in a buffer memory. It is then read out of memory and sent to the DPC. Correction is performed on the information as required. (Error correction is explained in detail in section 4).

RELOCATE

The RELOCATE operation is used to relocate a sector containing a media flaw onto one of the spares on the most-significant surface. There are 5 spare sectors per cylinder; therefore, only 5 sectors may be RELOCATED per cylinder.

RELOCATE is a one sector operation. The processor designates the sector to be relocated. This is contained in the address of the initiate words. The processor also designates which spare sector to use. The N variants contain the value 1 through 5, corresponding to sectors 85, 86, 87, 88, and 89.

After the initial OP processing is complete, a test is made on the new cylinder address and the last cylinder address in order to determine if a seek is necessary. If OLD is not equal to NEW, a seek is required. A cylinder CM is sent to the drive. The DDEC waits for a READY drive message before continuing.

The correct head is selected in the drive by a head CM. The DDEC requests an index pulse from the drive and waits for the index drive message to return.

When the index is received, a READ operation is started on the drive and the first address is read. This occurs in order to check that we are actually on the correct cylinder and head. If the cylinder and head compare, continue. If the cylinder or head do not compare, try to get a comparison in the next sector. If 128 sectors pass without a comparison,

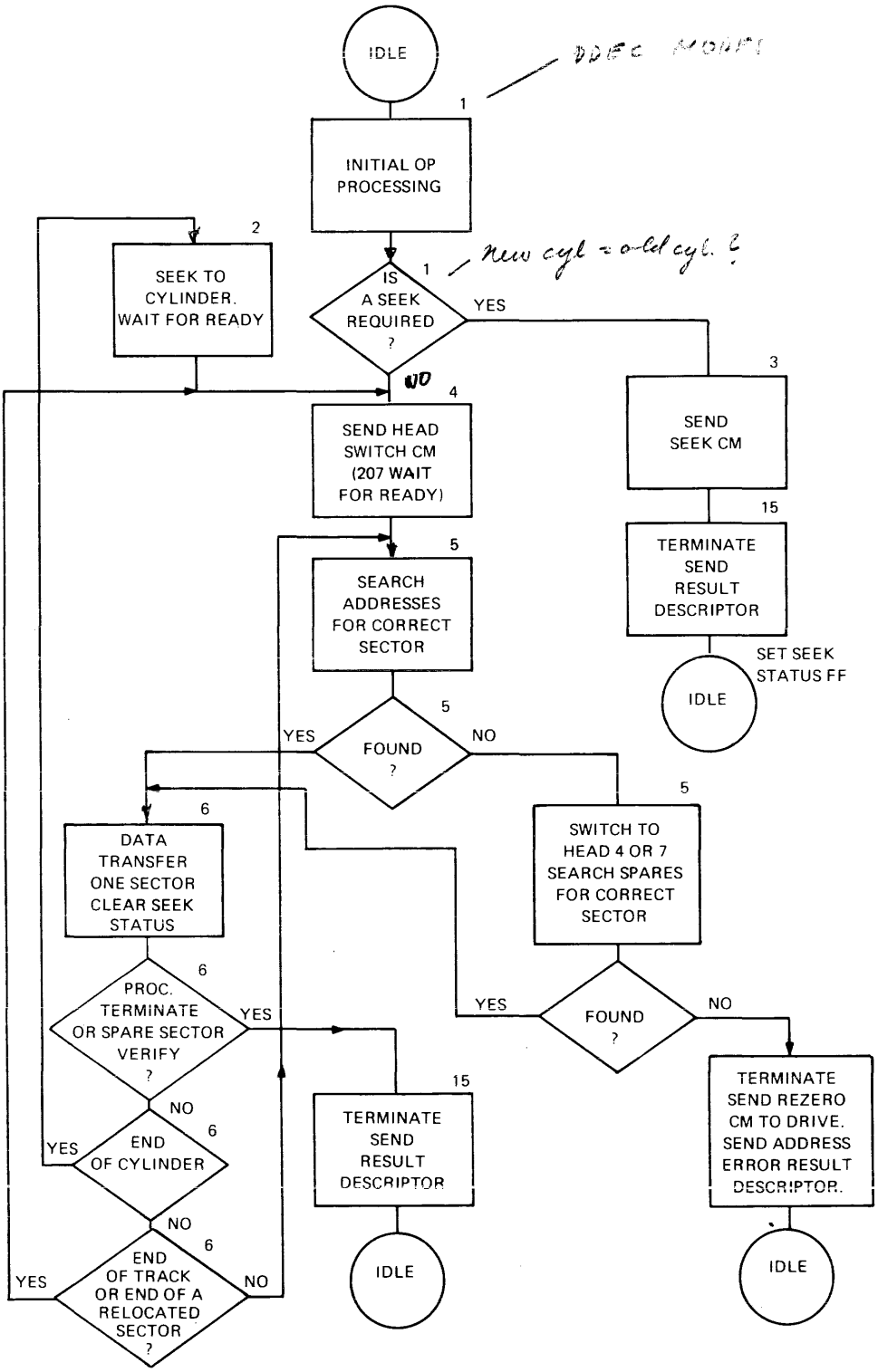


Figure 1-18. READ, WRITE, or VERIFY

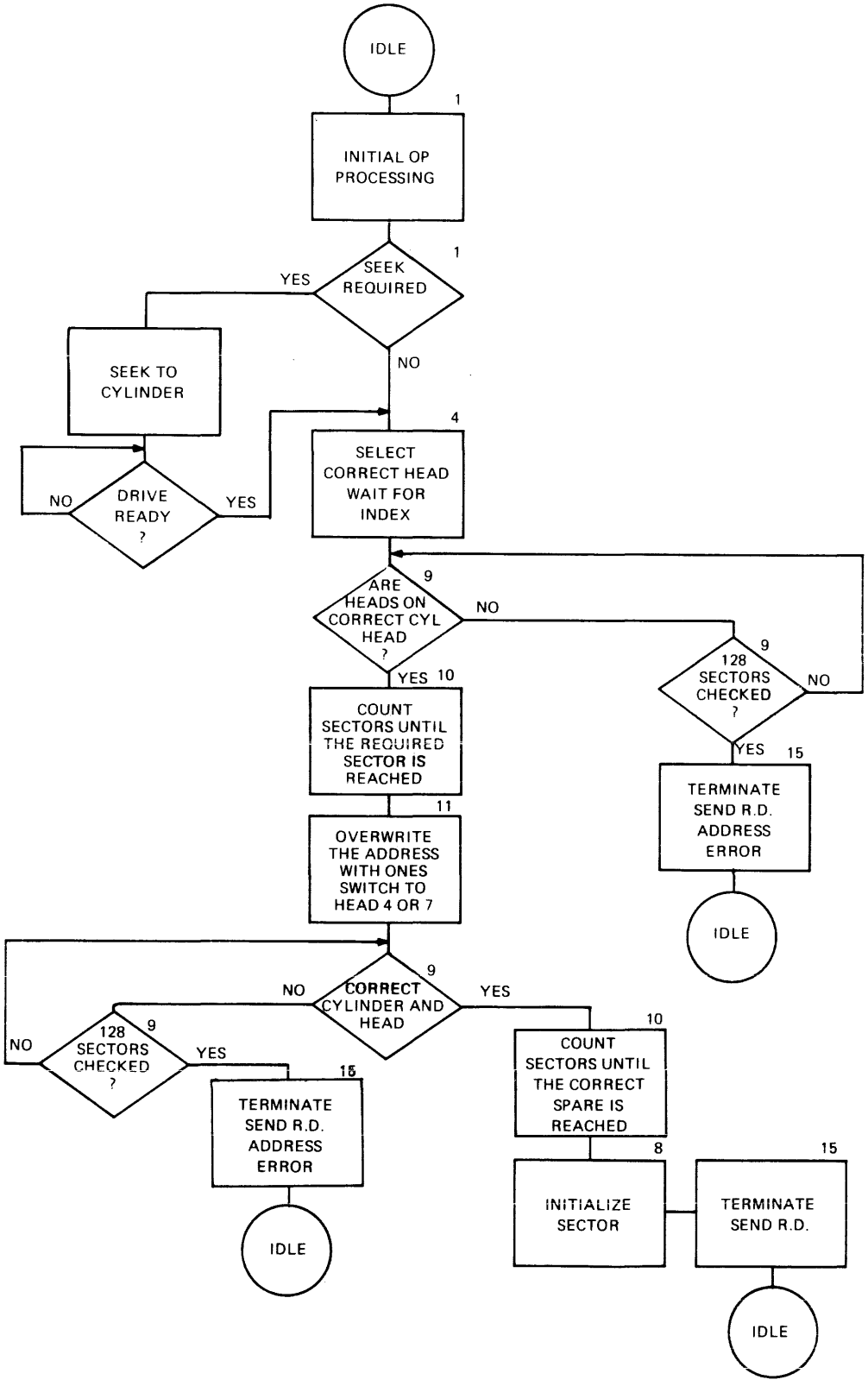


Figure 1-19. RELOCATE OP

exit to terminate and send an address error result descriptor.

CLOCK pulses from the drive are counted until the correct sector is reached. The address field of the sector is overwritten with ones. This action prevents an address comparison in this sector on subsequent writes, reads, and verifies. The most-significant head is then switched to in preparation for relocating the sector. Again, the correct cylinder and head are checked from disk. Again, if the correct cylinder and head are not found in 128 sectors, terminate and send a result descriptor.

CLOCK pulses from the drive are again counted until the disk has reached the spare sector designated in the N variants. The complete sector is then overwritten: address mark, address preamble, address sync bits, address (of the sector containing the media flaw) EPC data sync bits, data field, firecode, and End-of-Record.

The data written in the data field varies according to the OP code. Refer to table 1-7. With OP code 100, an extra word of information is received after the initiate words. This data is repeated 90 times in the data field. If the OP code is 101, the four bytes of address information are repeated 45 times.

At the completion of the sector, the operation terminates and sends a result descriptor to the DPC. (See figure 1-19).

Test OP

The purpose of the Test OP is to find out the status of the drive specified by the unit bits of the initiate words.

Test OP has two variants:

1) Clear seek status. This allows the processor to clear the seek status flip-flop for all units.
2) Power Down. This allows the processor to power down a spindle for a pack change (usually in response to the P.O. message).

During the initial OP processing, the drive unit is selected. In response to be being selected, the drive returns a status DM telling the DDEC whether it is online or offline and ready or not ready. This status is used for a result descriptor. See figure 1-20 for the basic flow diagram.

Read Extended Result Descriptor

The Read Extended Result Descriptor operation is sent in response to a regular result descriptor with the "TRY DIAGNOSTICS" bit set. Performing an ERD operation is the only way to reset the TRY DIAGNOSTICS bit in the DDEC.

When the TRY DIAGNOSTICS bit is set, any operation except a READ ERD and a Test OP is terminated immediately after the initial OP processing.

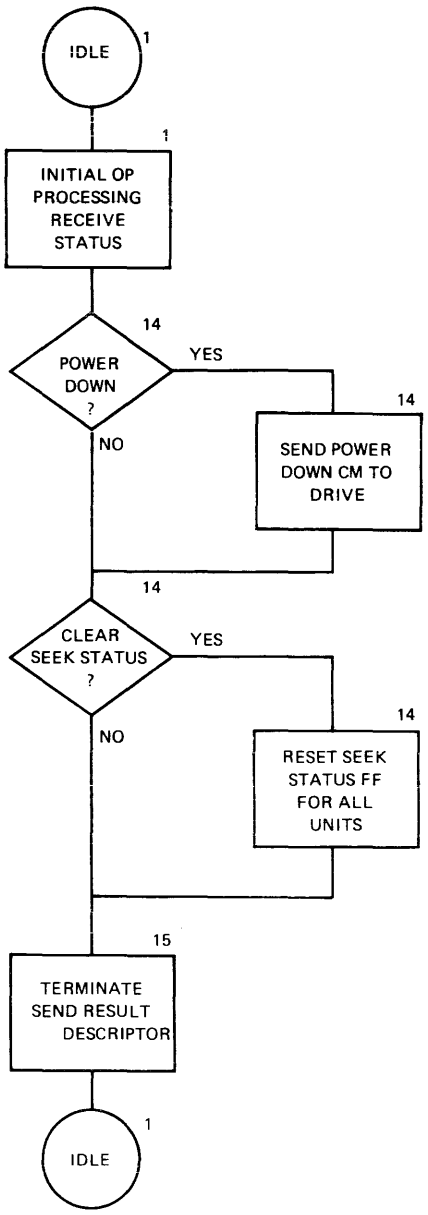


Figure 1-20. Test OP

Operations on other units continue unaffected.

The DDEC may only store one Extended Result Descriptor. If more than one drive sends extended status to the DDEC, the TRY DIAGNOSTICS bit and the ERD apply to the first drive. TD indicates that an ERD has been stored in the DDEC.

After the initial OP processing is complete, the four words of Extended Result Descriptor are placed, one at a time, on the INFO lines, and a DPC CLOCK pulse instructs the DPC to receive each word. After four words have been sent, the DDEC terminates, sending a regular result descriptor which always contains zeros. (See figure 1-21).

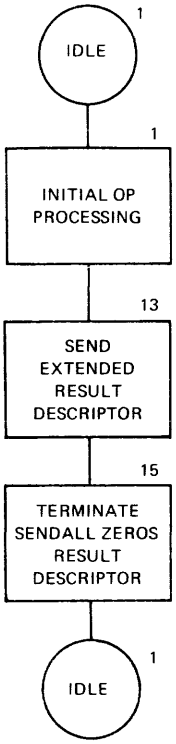


Figure 1-21. Read ERD

READ MAINTENANCE

The READ MAINTENANCE operation is primarily for the use of the Field Engineer. It enables the processor to read the entire contents of a sector, from the address mark or servo field to the End-of-Record. If this information is printed on a line printer, the Field Engineer may inspect the data for the correct address information, sync characters, preambles, and so forth.

The byte boundaries may not be in the correct place in relation to the bits because the sync character is not used.

The sector to be read is contained in the initiate words.

The READ MAINTENANCE operation consists of a SEEK (if required), a head selection, verification of the cylinder and head, a dead reckoning address search, a READ, and a terminate.

While the sector is being read, the DDEC does not compare the address and does not compare the firecode. (See figure 1-22).

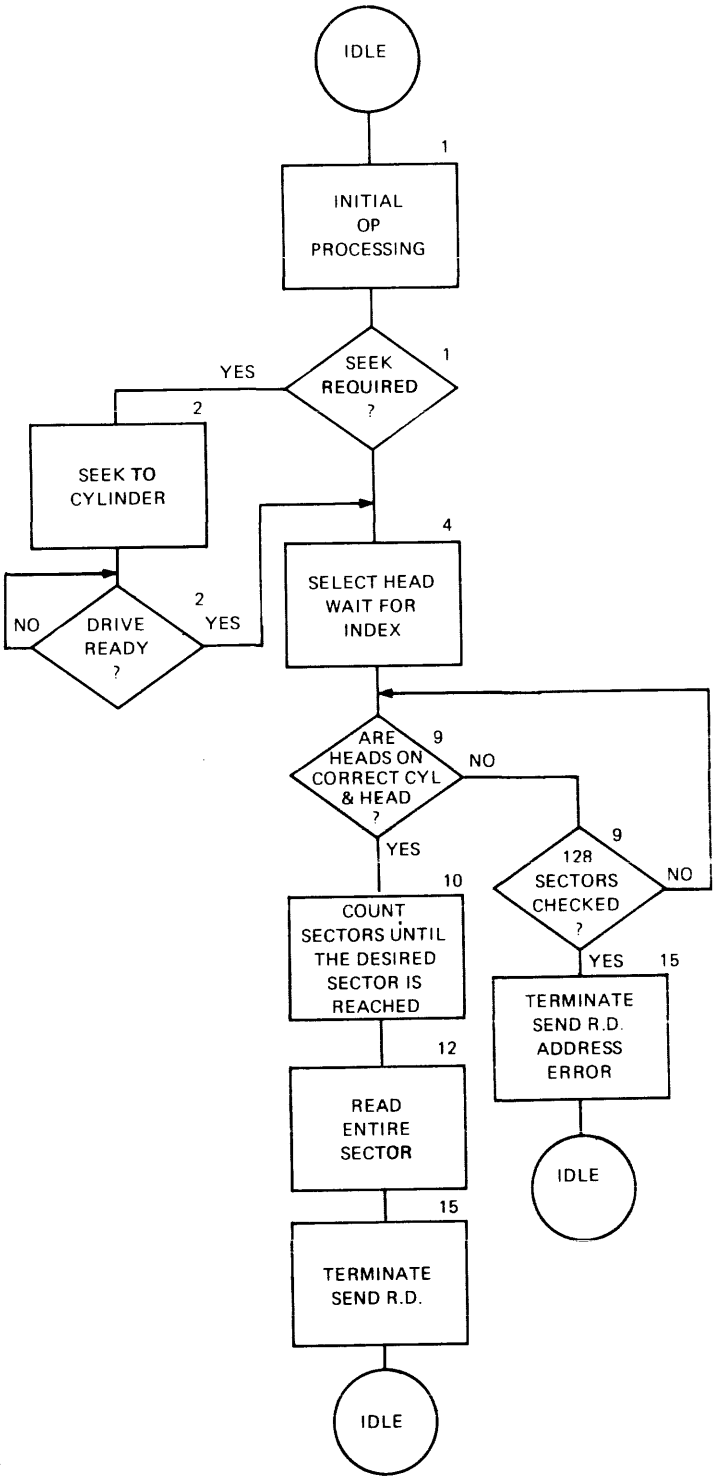


Figure 1-22. Read Maintenance

SECTION 2

MODE FLOWS

GENERAL DESCRIPTION

The operation of the DDEC is divided into 16 modes. Each mode has its own functions and flow. A mode may be used for several different OP codes.

Examples:

Mode 2 is used whenever an immediate SEEK is required. It is used in the INITIALIZE, RELOCATE, READ, WRITE, and VERIFY OP codes.

Mode 4 is used in order to switch heads. It is used by the INITIALIZE, RELOCATE, READ, WRITE, and VERIFY OP codes.

Mode 8 is used to initialize a sector in the INITIALIZE operation and the RELOCATE operation.

Table 2-1 lists all the modes and their primary functions. In the functional flow charts in the previous section, the modes are indicated by a numeral to the top right of each box.

Table 2-1. Mode Functions

Mode	Explanation
0	Power up spindles.
1	Take commands from processor; decide if an operation may be performed.
2	Second and subsequent seeks for READ, WRITE or VERIFY. All seeks for INITIALIZE, RELOCATE and READ MAINTENANCE.
3	First seek for READ, WRITE or VERIFY.
4	Find index, PLO and offset initiation, and most head switches.
5	Address search.
6	READ, WRITE or VERIFY data transfer.
7	Write beginning of track (BOT) gap for initialize (206 only).
8	Initialize a track with addresses and data. Initialize one sector on a RELOCATE.
9	Establish correct CYL-HD for RELOCATE and READ MAINTENANCE.
10	Count around a track for RELOCATE and READ MAINTENANCE (dead reckoning address search).
11	Overwrite bad sector (RELOCATE operation).
12	Transfer whole sector on a READ MAINTENANCE.
13	Send extended result descriptor to processor.
14	Power down drive and/or clear seek status.
15	Terminate all operations and send result descriptor. Go back to mode 1 idle condition.

In this section, the modes are discussed in detail. The hardware implementation is discussed in later sections. However, in order to understand the flows, it is necessary to have a basic knowledge of the following hardware blocks:

Sector location counter.
Disk location counter.

The flows consist of the control logic of the unit; all other actions in the DDEC are initiated or controlled by some action occurring in the flow. (See figure 2-1).

MODE 0 SPINDLE SPINUP

See figure 1-14 for a block diagram of this operation. Figure 2-2 shows the mode 0 flow.

Mode 0 is entered only after power up. PWRSYNC is a reset signal which resets various flip-flops in the DDEC. Of particular interest at this time is that the mode flip-flops are reset to mode 0, and the sector location counter is cleared to W0B0.

When the reset signal ends, the sector location counter starts to increment. At word 1 bit 11, the signal DRTHRCK (drive there check) is high. DRTHRCK samples the DM (drive message line). If the drive is connected and has AC power on, the DM line is high. In this case, DRTHERE is set.

At word 2 bit 3, two actions occur if DRTHERE is high:

1) SWTODR - this signal switches the 10Mhz clock from a local clock to the drive clock. Special circuitry prevents clock slicing (described later).
2) CMSEL - this causes the CM line to go high to the drive. When the drive senses a SELECT it returns a status DM; however, it is not used at this time.

At word 5 bit 14, three actions occur if DRTHERE is high:

1) RPUCM - this signal causes a "power" up controller message to be sent to the drive.
2) ST8TIMR - start eight second timer.
3) INSECLOC/ - this stops the sector location counter.

The flow is not controlled by the sector location

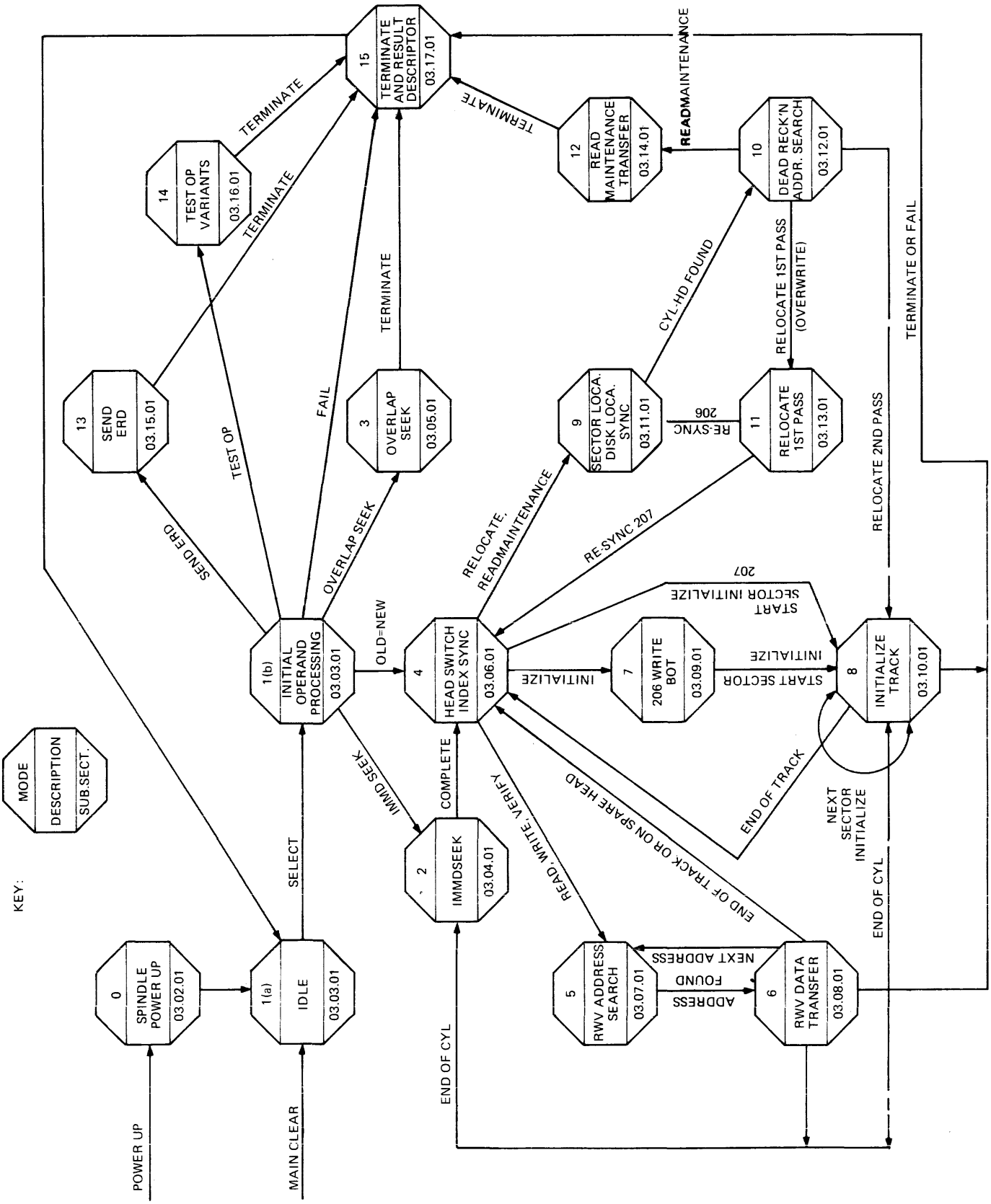


Figure 2-1. Overall Operation Flow

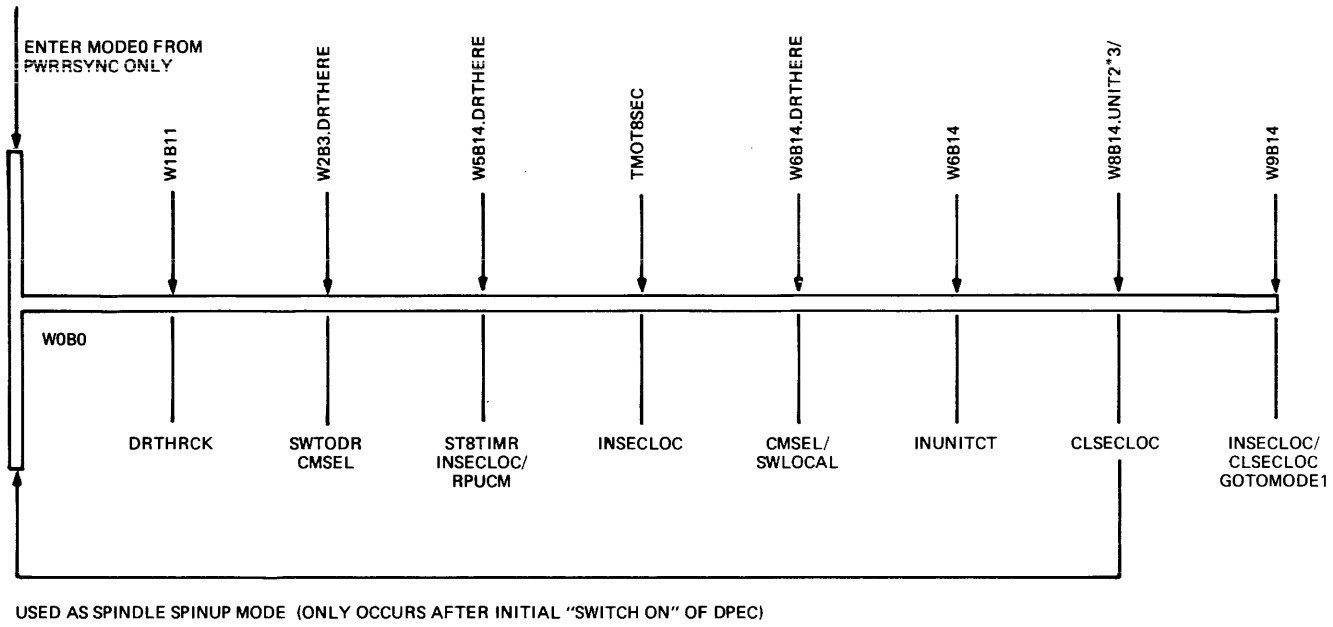


Figure 2-2. Mode 0, Spindle Spinup

counter now. The next action occurs eight seconds later when TMOT8SEC occurs. During the eight second waiting period, the drive motor is starting. When TMOT8 SEC occurs, INSECLOC is true so that the sector location counter resumes counting from its previous value.

At word 6 bit 14, with DRTHERE, two actions occur:

1) CMSEL/ - this caused the CM line to go low, deselecting the drive.
2) SWLOCAL - switch from drive clock to local clock.

If the drive is not there, the drive may not be selected, the eight second timer may not start, etc. There is no action until W6B14.

At W6B14, the unit counter is incremented in preparation for powering up the next unit.

At W8B14, if the unit counter has not reached 8, we receive the signal CLSECLOC. Clear sector location counter means that we are at the beginning of mode 0 again.

Mode 0 is looped eight times, one for each drive. If the drive is there, it is powered up, allowing a wait of 8 seconds; if the drive is not there, the operation continues to the next drive.

At word 8 bit 14, when the unit counter = 8, the sector location counter is not cleared. The word bit counter continues to W9B14.

At W9B14, three actions occur:

1) GO TO MODE 1.
2) INSECLOC/ - halt sector location counter.
3) CLSECLOC - clear sector location counter.

These three signals take the DDEC out of mode 0 and into mode 1, word 0, bit 0, with the word bit counter halted. This is considered as the idle mode of the DDEC.

MODE 1 INITIAL OP PROCESSING

See figures 1-15 and 2-3 for the following discussion.

The mode 1 idle condition is mode 1, W0B0. In this state, the DDEC is not performing any operations; it is waiting for a command from the DPC.

When the DPC places the first initiate word on the INFO lines, SELECT is made high by the DPC; SELECT causes INSECLOC, and the word bit counter starts counting.

At W0B11 three actions occur:

1) ADCKNWD2 - this pulse loads the address portion of the first initiate word (INFO 11 through 15) into the address multiplexor.
2) ADCLOCK - this pulse loads the address shift registers from the address multiplexors.

3) CKWORD1 - clock word one sets the OP registers, variant registers and unit counter to the values sent on the INFO lines. It also synchronizes the 5Mhz clock and resets the DRTHERE flip-flop.

The address decoding is described in a later section.

At W0B12 through to W0B14, CKDPC is high to the DPC At W0B15, the DDEC raises READY to the DPC This acknowledges receipt of the first word and requests the DPC to send the second word. CKDPC is derived from CKINTWRD/.

At W1B11, we clock in the second initiate word into the address registers with the signal ADCLOCK. The second initiate word contains only address information. At this time, a check is made on the DM line of the drive selected. DRTHRCK samples the DM for a high state, indicating that the drive has power on.

CKDPC is high from W1B12 through W1B14 (3 bits = 300 ns). At W1B15, BUSY is sent to the control. This acknowledges receipt of the second initiate word and informs the DPC that the DDEC is now busy.

If the OP code sent is READ ERD, the signal SENDERD is true. In this case, GOTOMODE13 and CLSECLOC are active at W2B1. This causes the flow to go to mode 13 W0B0 for the ERD transfer.

If the operation is not READ ERD, the word bit counter continues and, it remains in mode 1. At W2B3, if the drive is there (DRTHERE), we SELECT the drive (CMSEL) and switch to the drive clock (SW TO DR). Selecting the drive causes it to return a status DM.

At W2B4, an action occurs when the DDEC is not in REMOTE (REMOTE/). In other words, this is a maintenance action when offline. By jumpering ENCLDIAG true, the Field Engineer may clear the TRY DIAGNOSTICS bit prior to an operation. A TD bit prevents the operation from occurring. With TESTOP/ (not a Test OP), REMOTE/ and ENCLDIAG (enable clear diagnostics), the signal CLR DIAG is true, resetting the TD condition on the leading edge.

At W2B4, a test is made on two error conditions:

1) XMNTPERR - transmission parity error on the INFO lines.
2) TD - TRY DIAGNOSTICS.

If either of these is true, we go to mode 15 W0B0 and return a result descriptor.

At W3B1, the DDEC clears the seek status flip-flop for the unit selected if IMMDSEEK is true (immediate seek). IMMDSEEK is true on an INITIALIZE, RELOCATE, or READ MAINTENANCE operation. This action has no special significance; it is purely a "house-keeping" action.

By W4B5, the address decode logic has converted the binary sector address supplied by the DPC into cylinder, head, and sector. At W4B5, this address is loaded into the address counter with the signal LOADAC. There are two cases when this does not occur:

1) No address load (NOADDRLD) - this is a local term, true when the no address load switch is on. It retains the previous address in the address counter so that the operation may be resumed at the previous address when START is pushed.
2) Test OP.

At W4B7, the address in the address counter, the OP, variants, and units are loaded into the ERD register. This information forms part of the ERD if there is an exception condition during the operation. Note that this is the starting address of the operation. STROBADR (strobe address) also checks to see if the address supplied by the DPC is higher than the maximum allowed for this unit. If this occurs, the unit exits to mode 15 with DPEC EXCF (DPEC Exception flip-flop).

At W5B1, if the drive is not ready (DRREADY/) or not online (DRONLINE/), the flow exits to mode 15. By this time, the drive ready flip-flop and the drive online flip-flops have been set or reset according to the drive message returned in response to being selected at word 2 bit 3. STBLKRDY resets the drive ready flip-flop.

At W5B15, a head/spindle CM is sent to the drive (HD/SPDLCM). It has bit 32 set (spindle only). On the 207 drive, a head switch is not initiated by this CM. If the operation is a write, initialize, or relocate, the signal NEEDTOWR is high. In this case, the write enable bit in the the head/spindle CM is also sent. This prepares the drive for writing.

The next two actions at W10B14 and W10B15 are now redundant because the 207 drive does not do a

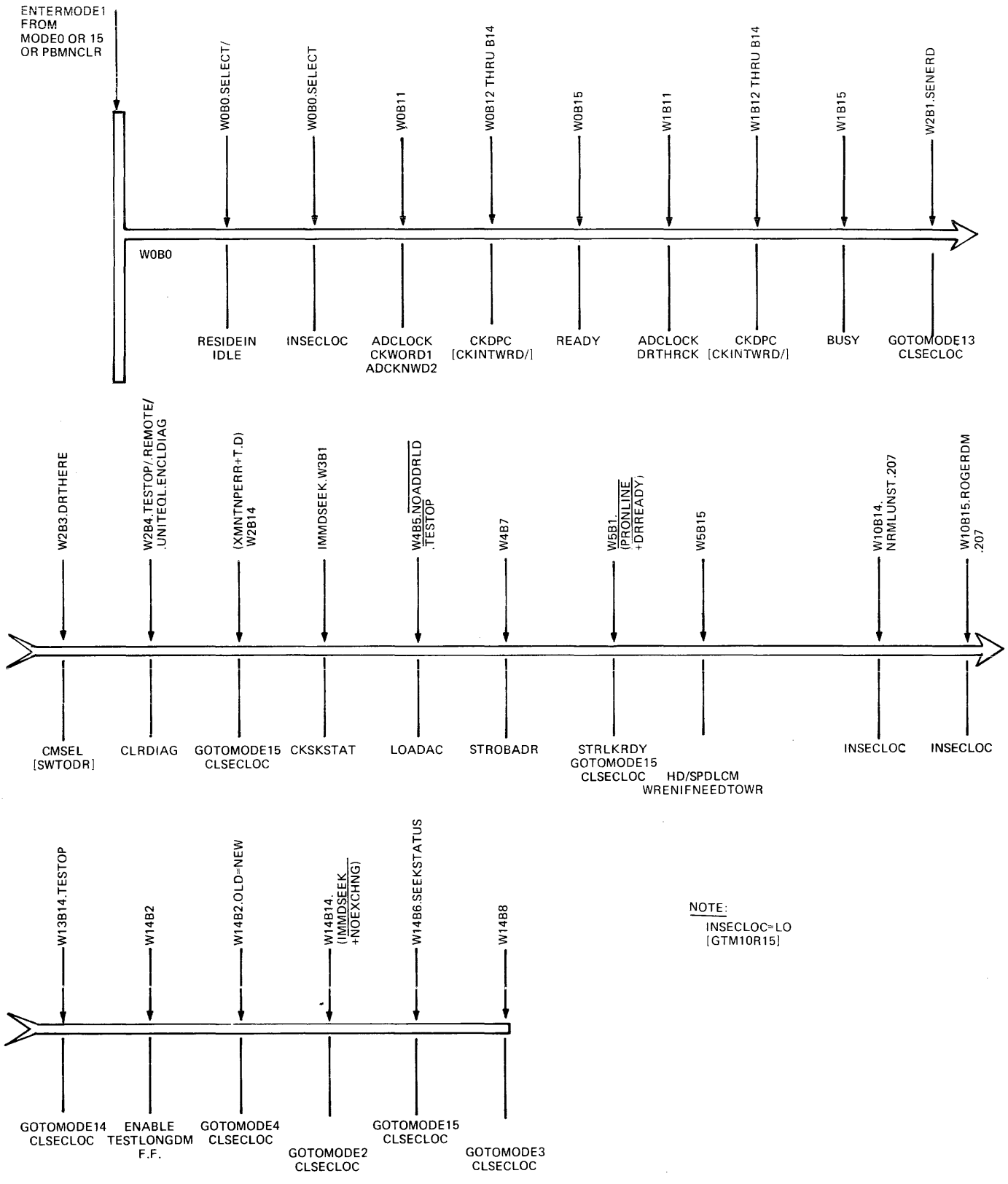


Figure 2-3. Mode 1, Initial OP Processing

head switch in response to a SPINDLE ONLY CM. NRMUNST does not go true at this point. At W13 on a test OP (for 206 and 207), the flow goes to mode 14 W0B0.

At W14 B2, the signal LONGDM is enabled to fail the DDEC. If an unexpected long drive message arrives at the DDEC, this signifies an error message from the drive. If LONGDM is high from a long drive message previous to this point in time, the flow goes to mode 15 to terminate. Similarly, if a long DM occurs at anytime from now till the end of the operation, the flow exits to mode 15 and terminates. In all cases, a result descriptor with the TD bit on is returned.

At W14B2, if there is no requirement to seek, the flow goes to W0B0. A seek is required if the next cylinder address is not equal to the last cylinder address used by this drive, (NEW ≠ OLD). If NEW = OLD, we go to mode 4 W0B0.

At W14 B14 with the signal IMMDSEEK, the flow goes to mode 2 W0B0 for a seek CM. IMMDSEEK is true when the operation is an INITIALIZE, RELOCATE, or READ MAINTENANCE. The flow also goes to mode 2 if there is an exchange.

At the time of writing, exchanges are not implemented. The exchange option is covered in a separate section if and when they are implemented.

If the flow reaches W14B6, the operation must be a READ, WRITE, or VERIFY, and a SEEK operation is required. If the SEEK status flip-flop for this drive is high at this time, the previous SEEK has not been serviced. (A READ, WRITE, or VERIFY operation has not been performed on track). This is an error condition. The flow goes to mode 15 where a result descriptor with the SEEK STATUS bit set is returned to the DPC

At W14B8, the flow goes to mode 3 W0B0 for an overlapping seek.

MODE 2 SEEK

Mode 2 is entered to perform the second and all subsequent seeks on READ, WRITE, or VERIFY, and for all seeks on INITIALIZE, RELOCATE, and READ MAINTENANCE. It may be entered from modes 1, 6, and 8.

The first action is at W0B15. At this time, the sector location counter is halted if the drive is not ready. The drive could be not ready if the heads are moving back on track from an offset position. When the drive goes ready, the flow continues (INCSECLOC). At W1B1, the cylinder CM is sent to the drive. This tells the drive to seek to the new cylinder.

At W9B13, a test is made to ensure that the drive went NOT READY. The drive always goes NOT READY during a seek. If NRMUNST is not true (normally unsettled), the flow goes to mode 15 to terminate.

One bit time later, at W9B14 the sector location counter is halted until the seek is completed. When DRREADY is true, the flow continues. (INSECLOC allows the sector location counter to increment).

At W29B8, a test is made on the SELECT signal from the DPC If the processor lowers the SELECT signal, this signifies that the operation is terminated. If SELECT is high, the flow goes to mode 4 W0B0. If SELECT is low, the flow continues to W30B6. The flow then goes to mode 15 W0B0, where it returns a result descriptor and terminates. (See figure 2-4).

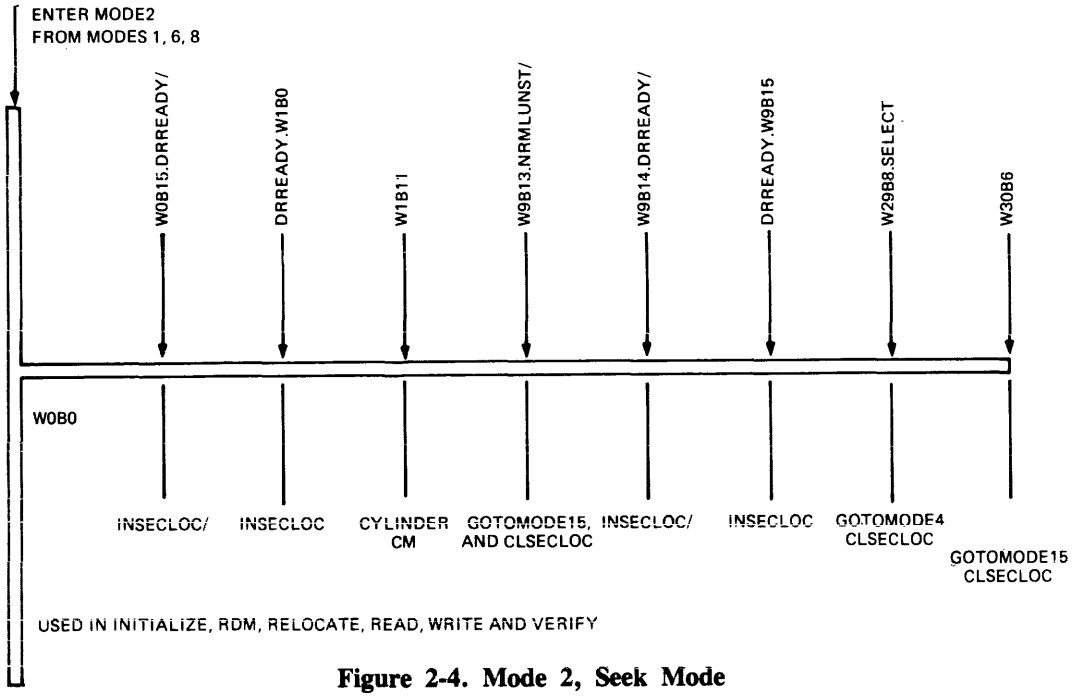


Figure 2-4. Mode 2, Seek Mode

MODE 3 OVERLAP SEEKS

Mode 3 is entered only from mode 1 on a READ, WRITE, or VERIFY operation when a SEEK is required. (See figure 2-5).

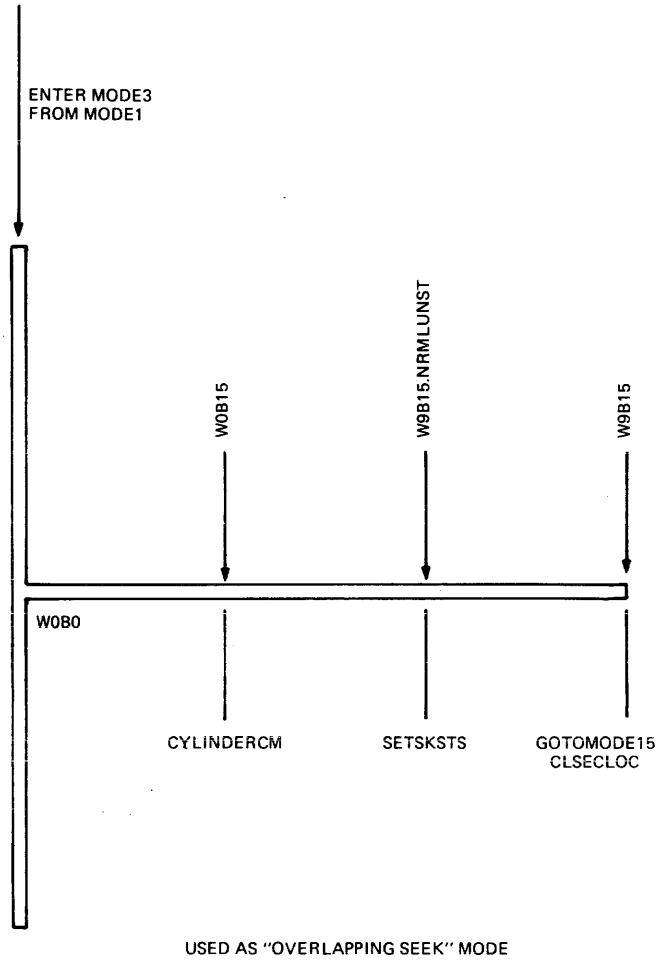


Figure 2-5. Mode 3, Overlap Seeks

At W0B15, the cylinder CM is sent to the drive. This causes the drive to seek to the new cylinder.

At W9B15, the signal SETSKSTS goes true and stays true until mode 15. Seek Status indicates that an overlapping seek operation has been performed on this drive. With seek status set, no other SEEK may be performed until a READ, WRITE, or VERIFY operation has taken place at this cylinder. (Refer to mode 1 W14B6).

At W9B15, the flow goes to mode 15 W0B0. A result descriptor is returned. After the result descriptor is sent, the signals CKSKSTS (CLOCK seek status) and SETSKSTS set the seek status flip-flop for the drive selected. While the seek is in progress, the DDEC is available to the DPC It could receive a command on another unit, thus using up the seek time profitably.

MODE 4 HEAD SWITCH AND INDEX SEARCH

See figure 2-6 for the following discussion.

Mode 4 is entered from modes 1, 2, 6, 8, and 11. It is used to perform the following functions:

1) Head switches.
2) Index search.
3) Initiate offset and PLO CMs.

At W0B11, the flow halts if the signal EXECUTE is low from the DPC and if the mode 4 flip-flop is reset (MDE4FLOP/). The DPC sends EXECUTE false if its buffers are full during a READ or empty during a WRITE. It instructs the DDEC to wait. When the DPC has handled its buffers, EXECUTE goes high and the flow continues. INSECLOC halts the flow when low and resumes the flow when high. MODE4FLOP indicates that a head switch is required. It is high every time mode 4 is entered; therefore, when first entering mode 4, the sector location counter is not stopped even if EXECUTE is low.

At W0B14, the flow splits up into two paths. The path taken depends on MODE4FLOP (Mode 4 flip-flop). Assuming that MODE4FLOP is on, the flow follows the path marked YES.

At W1B11 with MODE4FLOP, the head CM is sent to the drive.

The next three actions affect the flow if the unit selected is a 207. When a head switch is sent to a 207, a mini-seek occurs, while the carriage detents on the new track. Therefore, the signal NRMUNST (normally unsettled) is true.

At W6B11, the flow is halted until the 207 "mini-seek" is complete. ROGERDM signifies that the seek is complete.

At W9B14, MODE4FLOP is reset and the sector location counter is cleared. This takes the flow back to the beginning of mode 4. At this time, if EXECUTE from the D.P.C is low, the sector location counter is halted (INSECLOC/), and the flow waits until EXECUTE goes high. This is called slip. At W0B14, MODE4FLOP is now reset so that the flow follows the NO path.

The flow chart is split into two sections from here on. If the OP code is READ, WRITE, or VERIFY, the first path is taken. If the OP code is not READ, WRITE, or VERIFY (INITIALIZE, RELOCATE, or READ MAINTENANCE), the second path is taken. (See figure 2-6).

READ, WRITE, or VERIFY

At word 0 bit 15, a control CM is sent to the drive. If the offset or PLO variants were sent in the initiate word, the bits to implement these functions in the drive are included in the CM. If the drive is

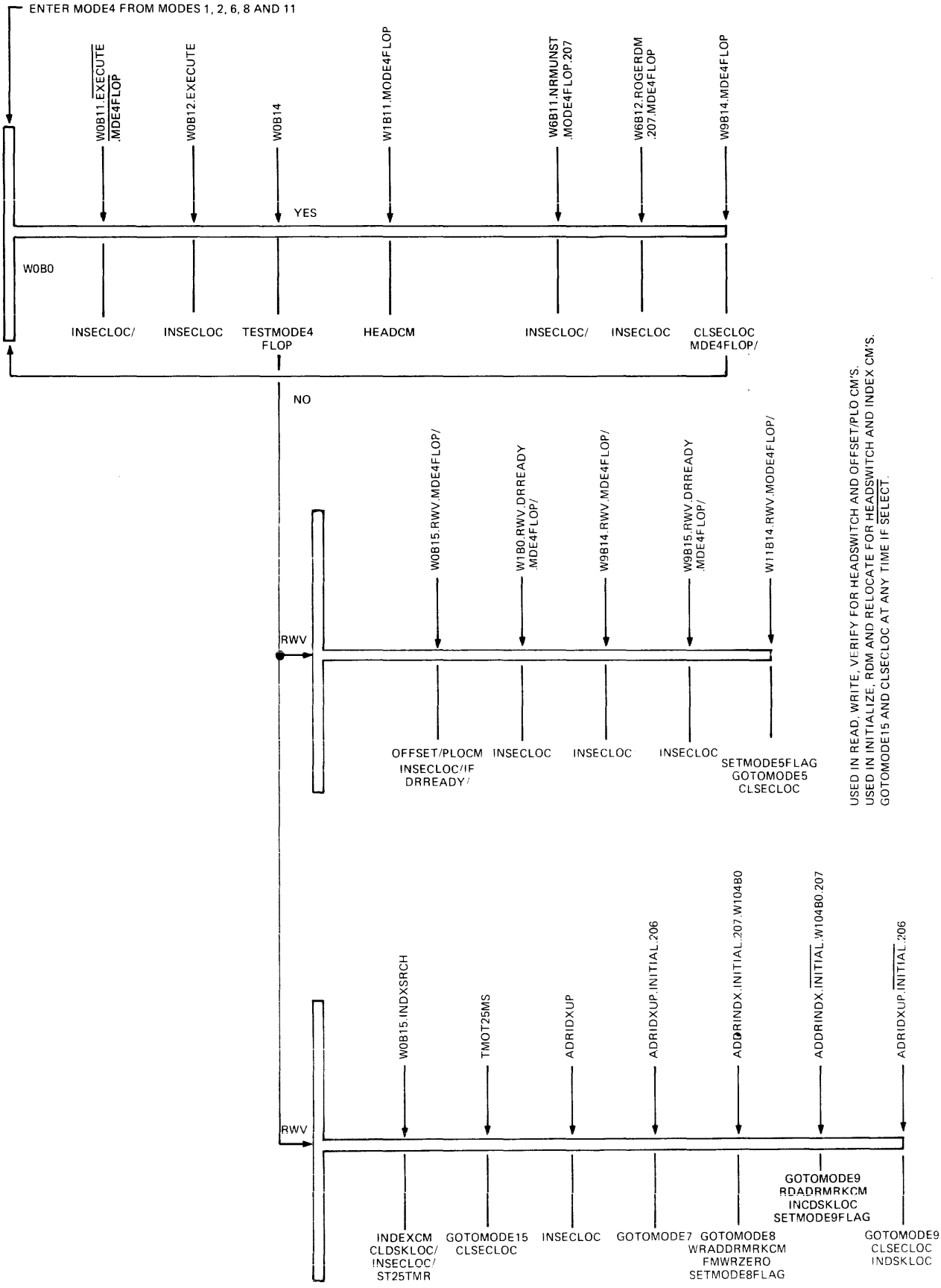


Figure 2-6. Mode 4, Headswitch/INDXSRCH

not ready at this time (which it should never be), the flow stops (INSECLOC/). If the drive is ready, the flow resumes on the next word bit (W1B0).

At W9B14, the drive should have received the CM initiated at W0B15. If an offset is initiated, the drive goes NOT READY while the heads move to their offset position. The flow is halted at W9B14.

When DRREADY is high, INSECLOC allows the flow to continue. DRREADY may be high immediately if the offset bit has not been set, in which case there is no delay.

At W11B14, the flow goes to mode 5 W0B0 for the address search. Mode 5 flag is set.

Read Maintenance, Initialize, or Relocate

Each of these operations requires the DDEC to be synchronized to the index mark on the drive. Index is a pulse occurring at a fixed time once per revolution of the disk. In order to receive the index pulse in the DDEC, the DDEC must request index. The drive sends back a DM when index occurs in the drive.

Index is required on INITIALIZE in order to place the sectors in the correct relative positions. During Relocate and Read Maintenance, it is required in order to do a dead reckoning address search (counting sectors and clocks).

At W0B15, the following actions occur:

1) An index CM is sent to the drive (INDEXCM) - this requests the drive for index.
2) CLDSKLOC (Clear disk location counter) - the disk location counter is cleared to zero.
3) INSECLOC/ - the sector location counter is halted.
4) ST25TMR - start 25ms TIMER.

The flow halts while the disk rotates to the index mark.

If the index drive message is not received in 25 milliseconds, the flow goes to mode 15 W0B0 to terminate. A TD result descriptor is sent to the DPC, and an ERD with INDEX MARK MISSING bit is stored. TMOT25Ms signifies that the 25ms timer timed out.

One revolution of the disk is 16 milliseconds (approximately), therefore, the signal ADRIDXUP (address or index up) should be true before TMOT25ms. When ADRIDXUP occurs, INSECLOC causes the flow to continue.

If the drive selected is a 206 (9484-2/5) and the OP is INITIALIZE, the flow goes to mode 7.

NOTE
The sector location counter is not cleared.

If the drive selected is a 207 (9494-2/4) and the OP is INITIALIZE, the flow goes to mode 8 at W10 bit 0. WRADRMRKCM causes the DDEC to send a write address mark CM to the drive. FMWRZERO (format write zeros) causes the data line to be held in the zero state for the address preamble. SET MODE 8 FLAG is set to prevent the address from counting up on the first time through mode 8.

If the drive selected is a 207, and the operation is READ MAINTENANCE or RELOCATE (INITIALIZE/), the flow goes to mode 9 for a dead reckoning address search. RDADRMKCM causes the drive to return a drive message with the address or index bit set when the next address mark is reached. The drive automatically starts reading immediately after the address mark. INCDSKLOC (increment disk location counter) increments the counter from 0 to 1. The effect of this action is to have the signal DSKLOCEQL (disk location equal) one sector location early. This is necessary for RELOCATE. (Since the address field must be over-written, we must know in advance). SET MODE 9 FLAG sets the MODE 9 FLAG. Mode 9 flag is used in mode 9 to check that a ROGERDM is returned in response to the read address mark.

If the drive selected is a 206, and the operation is not INITIALIZE, i.e., a RELOCATE or READ MAINTENANCE, the flow goes to mode 9 for a dead reckoning address search. INDSKLOC increments the disk location counter so that the disk location equal signal occurs one sector early. The word bit counter is cleared to zero.

MODE 5 ADDRESS SEARCH

(READ, WRITE, or VERIFY OPs)

Mode 5 is entered from mode 4 after a head switch, from mode 6 after a data transfer, or from mode 5 when the next sector is to be compared.

Mode 5 compares the address read from the disk with the address in the address counters. The comparison includes the error protection code. If the address and EPC compare, the flow goes to mode 6 for a data transfer. If an address is not found in 128 sectors, a head switch to the spares head is made, and that track is searched. (The sector may have been relocated). (See figure 2-7).

In case of a spare sector verify operation, the address read from the disk is compared to the address counter, except the sector address is replaced with the N-variants + 84.

At W0B1, the flow halts if EXECUTE is low from the DPC EXECUTE is made low when the DPC requires time to handle its buffers. If the unit selected is a 207, the flow only halts if MODE5FLAG is on.

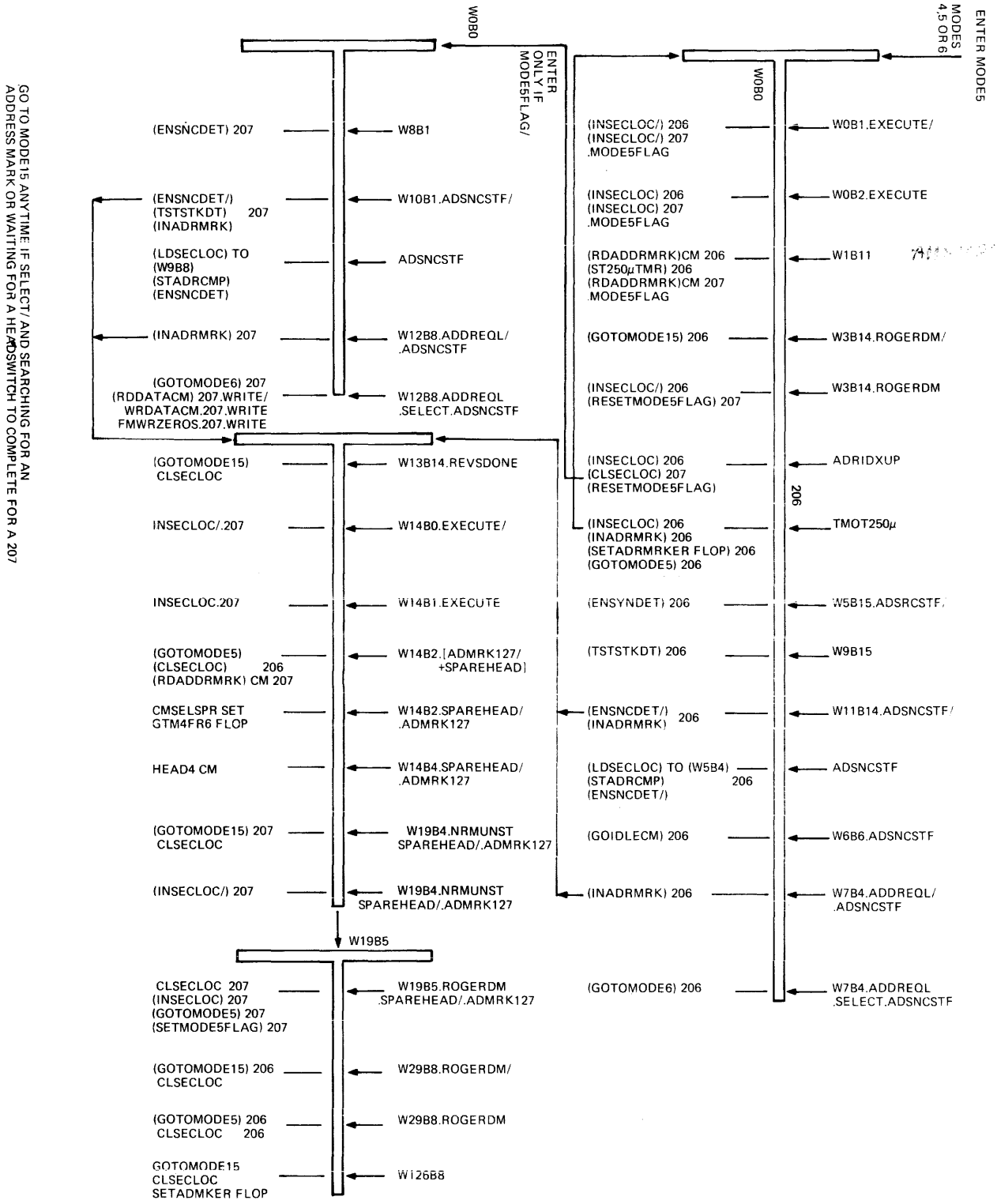


Figure 2-7. Mode 5, RWV Address Search

MODE5FLAG affects the flow if the unit is a 207, for the first address mark search only.

At W1B11, the DDEC sends a read address mark CM to the drive. A 250 microsecond timer is started. The DDEC expects an address mark DM within 250 microseconds.

At W3B14, the ROGERDM in response to the read address mark CM should be back. If it is not back (ROGERDM/), the flow goes to mode 15 to terminate. If the ROGERDM does come back, the sector location counter is halted if the unit is a 206. If the unit selected is a 207, the flow does not halt.

When the drive message containing the address mark returns from the drive (when the address mark is found), ADRIDXUP is high. The flow splits into two directions. If the unit selected is a 206, INSECLOC allows the flow to continue. If the unit is a 207, CLSECLOC takes the flow onto the lower line with W0B0. MODE5FLAG is reset. ADRIDXUP resets the stuck data flip-flop (not shown).

206 Operation

If the address mark failed to return within 250 microseconds, TM0T250U occurs. TM0T250U performs the following actions:

1) GOTOMODE5 - this signal takes the flow back to W0B0 of mode 5 for another address mark CM.
2) SETADRMKER - sets the address mark error flip-flop. This is loaded into the ERD if the operation subsequently fails.
3) INSECLOC - allows the sector location counter to start counting.
4) INADRMRK - increment address mark counter. The address mark counter causes the spare sectors to be searched after 128 sectors and a terminate if a further 128 sectors are read without the address being found.

At word 5 bit 15 with ADSNCSTF/ (address sync character start not yet found), the signal ENSNCDET enables the sync character detect logic. It also enables the stuck data flip-flop.

At word 9 bit 15, the signal TSTSTKDT allows the logic to monitor the stuck data flip-flop. If the sync character occurs on time, the transition from a zero to a one on the data line from the drive sets the stuck data flip-flop. If the output is low at TSTSTKDT time, a flip-flop is set to flag a stuck data condition. (Either the data line is stuck high or it is stuck low). This error condition is loaded into the ERD register if the operation subsequently fails.

If the sync character has not been detected by W11B14 (ADSNCFF), the sync character recognition logic is disabled (ENSNCDET/), and the address mark counter is incremented by one. The operation does not fail if this occurs because there is a 1:90 chance that this is not the correct sector. The sub-system may be able to recover by being able to correctly read the sector required.

If the sync character is detected, ADSNCSTF (address sync start found) goes high. At this point, the data is at the beginning of the address. The sector location counter is now loaded to W5B4. This action synchronizes the sector location counter with the format of the sector. (The first address bit is 10 bytes and 4 bits from the beginning of the address mark). The signal LDSECLOC performs the loading. ENSNCDET/ disables the sync character detection. STADRCMP (start address compare) starts the actual address comparison.

The data being read from the disk is compared, one bit at a time with the data in the address counters. If the address and E.P.C agree, ADDEQL is high. The address comparison lasts for 32 bits (2 words).

At word 6 bit 6, a GOIDLECM is sent to the drive. The drive receives the GOIDLECM and acts on the CM after the address has been read from the disk.

At W7B4, if the address is not found (ADDEQL/), the flow continues to W13B14.

If the addresses compared (ADDEQL), and SELECT is still high from the DPC, the flow goes to mode 6 W7B5 for a data transfer. If SELECT is low, it indicates a processor terminate. The flow goes to mode 15 (not shown).

207 Operation

The 207 Operation is very similar. The main difference is in the timing. The description starts from the point when the address mark is detected, and the sector location counter is cleared.

At W8B1, the sync character recognition logic is enabled. (ENSNCDET).

AT W10B1, if the sync character has not been detected, the flow does nothing until W13B14. ENSNCDET/ disables the sync character detect logic. TSTSTKDT tests the stuck data flip-flop, and the address mark counter is incremented.

When the sync character is found, the sector location counter is loaded to W9B8 in accordance with the format. The STADRCMP then starts the address compare, and ENSNCDET/ disables sync character detection.

AT W12B8, if the address and EPC do not compare (ADDEQL/), the address mark counter is incremented, and the flow continues to W13B14.

If the address and EPC do compare, the flow goes to mode 6 for the data transfer. If the OP code is not WRITE (READ or VERIFY), a READ data CM is sent to the drive. If the OP code is a WRITE, a WRITE data CM is sent to the drive. FMWRZEROS places zeros on the data line. The drive starts to write the data preamble (zeros).

206 and 207 Operation

At W13B14, the signal REVSDONE is checked. REVSDONE (revolutions done) is true when 128 sectors have been checked on the head addressed, and 128 sectors have been checked on the spare surface. If REVSDONE is true, this is an error condition, and the DDEC has failed to find the correct address. The flow goes to mode 15 W0B0.

At W14B0, the flow halts if the unit is a 207 and EXECUTE is low from the DPC. At W14B1, the flow continues if EXECUTE is high. At W14B2 and ADM127/ (address mark counter not equal to 127), or if the spare head is selected, the flow goes back to W0B0 for a 206, in order to compare the next address. If the unit selected is a 207, the flow continues with a Read Address mark CM to the drive.

At W14B2, if the address mark counter equals 127 and the head selected is not the head with the spare sectors, CMSELSPR is set (CM Select Spare). The Go To Mode 4 from Mode 6 flip-flop is also set. This flip-flop reminds the DDEC to switch the heads back to the addressed head after a spare sector read. At W14B4, a CM is sent to the drive selecting the spare head. In the 206, this is head 4. For a 207, this is head 7.

At W19B4 on a 207 unit, the DDEC expects the signal NRMUNST (normally unsettled) if a switch to the spare head is made. This is due to the mini-seek as the new head detents on the track. If NRMUNST is not true, this is an error condition. The flow goes to mode 15 W0B0. At W19B4, if NRMUNST is true after a head switch, the sector location counter is halted (INSECLOC/) until the ROGERDM is received indicating that the heads have settled.

At W19B5, with ROGERDM after a head switch to the spare head, and if the unit is a 207, flow goes back to mode 5 W0B0 and sets the mode 5 flag. This takes the flow to the top line of the flow, left hand side.

At W29B8, if the unit selected is a 206, the DDEC checks to see if ROGERDM has been returned in response to the head 4 CM. If ROGERDM is not true, the flow goes to mode 15 W0B0 to terminate and send a result descriptor. If ROGERDM is true, the flow goes back to mode 5 W0B0 in order to search the sectors on head 4.

W126B8 may only be reached if the unit is a 207, and ADRIDXUP has not been returned in response to the read address mark CM at W14B2 or W1B11. The DDEC sets the address mark error flip-flop, clears the sector location counter, and goes to mode 15.

If ADRIDXUP occurs before W126B8, the flow goes to the ADRIDXUP signal on the top of the flow (path not shown).

MODE 6 DATA TRANSFER

Mode 6 is entered in order to transfer one sector of data. Mode 6 may be entered more than once on a READ, WRITE, or VERIFY operation. (See figure 1-18). The flow is split up into the following sub-flows:

1) 206 READ or VERIFY (figure 2-8 upper left hand side).
2) 206 WRITE (figure 2-9 upper left hand side).
3) 206 End test routine (figure 2-8 upper right hand side).
4) 207 Read or verify (figure 2-8 lower left hand side).
5) 207 Write (figure 2-9 lower left hand side).
6) 207 End test routine (figure 2-8 lower right hand side).

The end test routine is used to make decisions about which mode to go to and to perform certain actions.

206 READ and VERIFY

All the terms in this flow are gated with WRITE/. Mode 6 is entered with the sector location counter at W7B5 and with the beginning of the data preamble passing under the head of the drive.

At W10B14, the DDEC sends a RDATACM to the drive. This allows the drive to synchronize its clock and read circuits on the preamble.

At W14B6, ENSNCDET enables the sync character detector. At this time, the DDEC does not know where the bytes of data begin and end. The sync character (four ones) gives the DDEC an accurate reference.

When the four ones of the sync character are detected, the signal STDTAXFR is true (start data transfer). At this time, the sector location counter is loaded to W17B0. This is in accord with the format of the disk. (The first byte of data is 17 words from the beginning of the address mark). Two other actions take place:

1) ENSYNCDET/ - the sync character detector is disabled.
2) FMRDATA - format read data permits data from the drive to enter the DDEC, be stacked into words and sent, one word at time, to the DDEC with a DPC clock, (format control circuits are discussed in a later section).

At W29B8, the address mark counter is cleared to zero. This insures that the next address search starts with the counter at zero. Also at W29B8, if the sync character has not been detected, DTSYNCSTF/ is true (Data sync start flip-flop). This is an error condition. The sync character detection logic is disabled (ENSYNCDET/). The flow goes to mode 15.

Word 106 bit 15 is the last bit of the data field. As the firecode information is about to start entering the DDEC from the drive, FMRDFIRE (format read firecode) conditions the DDEC to start checking the firecode read from the disk against the firecode generated internally, in the same way the data field is read.

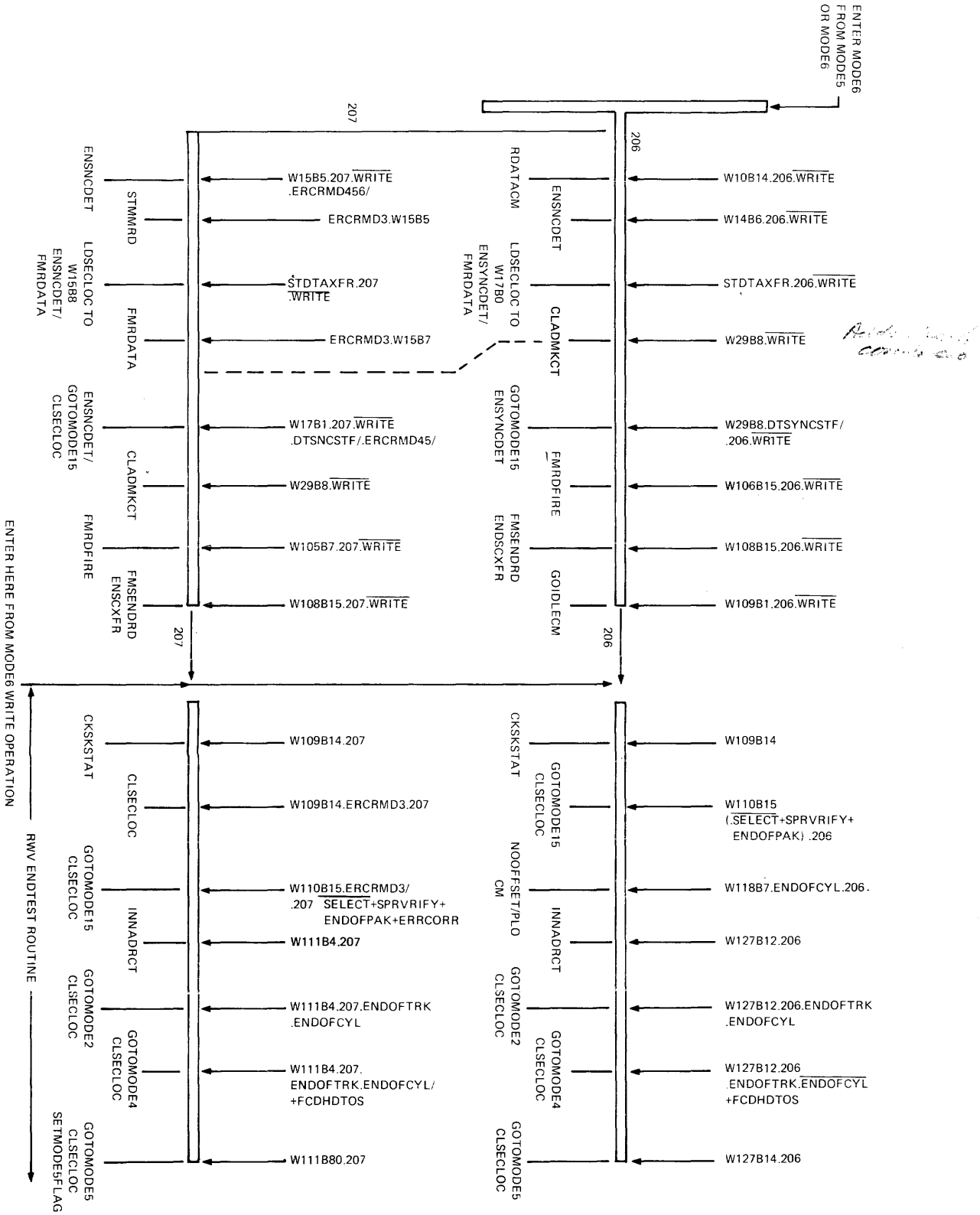


Figure 2-8. Mode 6, RWV DATAXFR

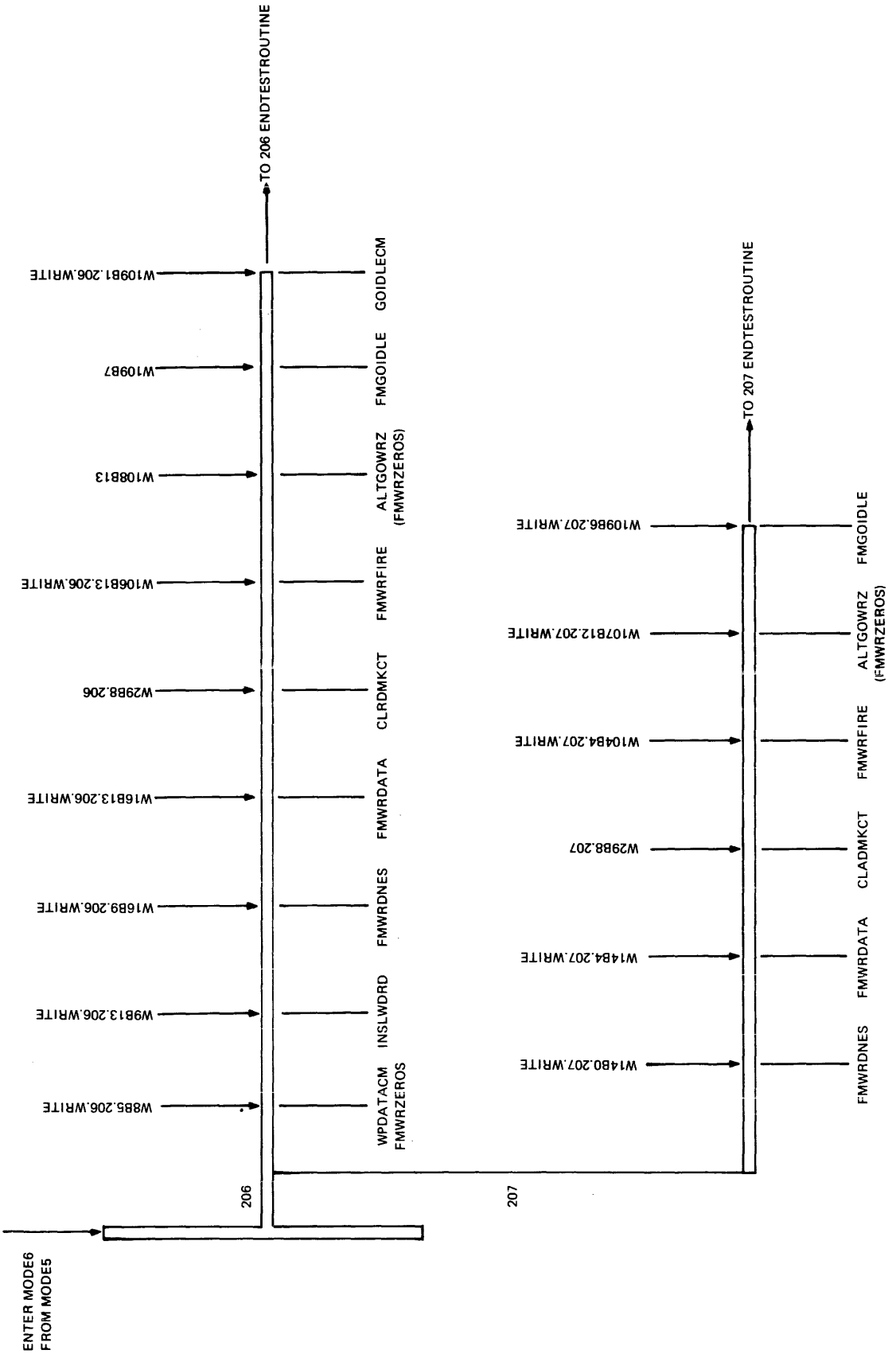


Figure 2-9. Mode 6, Write DATAXFR

At W108B15, FMSENDRD (format send result descriptor) sends the result descriptor to the DPC. ENDSCXFR is used when the unit is in local, doing single sector operations. It causes the maintenance logic to deselect the DDEC at the completion of the sector. The flow continues to the 206 end test routines.

206 Write Operation

Mode 6 is entered with the sector location counter at W7B5. At W8B5, the DDEC sends a write data CM to the drive (WRDATACM). FMWRZEROS ensures that the data line to the drive is low or in the zero state. This is necessary because the drive now rewrites the data preamble of zeros.

At word 9 bit 13, the sector location counter is incremented by one word (INSLWORD). This ensures that the data is written either in the same place or slightly earlier than on an INITIALIZE operation. Cable delays make this necessary.

At W16B9, FMWRONES (format write ones) places ones on the data line for writing the sync character. AT W16B13, FMWRDATA causes the data to go out to the drive serially. The format logic also sends DPC clocks to the DPC when a new word of data is required. While the data is being written on the disk the firecode logic generates the firecode to be written on disk at the end of the sector.

At W29B8, the address mark counter is cleared to zero, ready for the next address search.

At W106B13, FMWRFIRE (format write firecode) causes the firecode to be written on to the disk. At W108B13, ALTGOWRZ (alternate go write zeros) gives FMWRZEROS (format write zeros). This writes zeros in the End-of-Record.

The WRITE operation in the drive is terminated at W109B7. FMGOIDLE causes the format logic to go idle. The GOIDLECM is sent to the drive at W109B1 in order to go active at W109B7. The flow then goes to the 206 end test routine.

206 End of Test Routine

At W109B14, CKSKSTAT (clock seek status flip-flop) clears the seek status flag for this drive. This indicates that a previous SEEK has now serviced. AT W110B15, the operation is terminated under one of the three following conditions:

1) SELECT/ - this indicates that the DPC has terminated the operation.
2) SPRVRIFY - this is a spare sector verify which is a single sector operation.
3) ENDOFPAK - if the last sector of the pack is in the address counter.

If any of these conditions are met, the flow goes to mode 15 W0B0.

At W118B7, if this is the last sector of a cylinder (ENDOFCYL), a control CM is sent to the drive cancelling offset and PLO. At the end of a cylinder a SEEK is sent to the next cylinder. SEEK with offset is an illegal condition in the drive. This CM is sent regardless of whether the drive is in an offset condition.

At W127B12, the address counter is incremented. This is performed now in preparation for the address search for the next sector.

Also, at W127B12, the flow goes to mode 2 W0B0 for a seek if ENDOFCYL (end-of-cylinder). If ENDOFTRK (end-of-track) is high and ENDOFCYL/, or if this is a spare sector READ or WRITE (FCDHDTOS forced head to spares), the flow goes to mode 4 for a head change.

If the flow reaches W127B14, this means that the operation is continuing with the next sector on this track. The flow goes to mode 5 W0B0.

207 Read or Verify Without Error Correction

The flow proceeds along the lower line of figure 2-8. At W15B5, the sync character detector is enabled. When error correction is not being performed, ERCRMD45/ is high.

When the sync character in the data is detected, STDTAXFR goes true. The word bit counter is synchronized to the data by loading it to W15B8. FMRDATA (format read data) conditions the data circuitry to accept serial data from the drive, stack it into 16-bit data words, and transfer them to the DPC with CLKDPC. The sync character detector is disabled (ENSNCDET/), so that it does not detect another four ones.

An exit is made to mode 15 at W17B1 if the data sync character has not been detected (four 1's).

At W29B8, the address mark counter is cleared (CLADMKCT). This is no longer required since the sector has been found.

The reading continues until W105B7, when FMRDFIRE enables the firecode registers to be encoded by the firecode read from the disk. (The registers have already been encoded by the data). Firecode error flip-flop is set at the end of the firecode if the registers do not contain zero (not shown on the flow).

At W108B15, FMSENDRD causes a result descriptor for this sector to be transferred to the DPC.

A GOIDLECM is not required for the 207 drive to terminate a READ or a WRITE. This function is performed automatically by the drive.

At W17B1, a terminate to mode 15 is prevented by ERCRMD45/. At this point, an exit to mode 15 is made if the data sync character has not been detected. However, an exit is not made in the correction phase.

The address mark counter is cleared at W29B8.

At W105B7, FMRDFIRE allows the firecode data to be sent to the DPC.

FMSENDRD causes the result descriptor to be

sent. In the case of a successful error correction, bit 2 of the result descriptor is set. If the error is uncorrectable or if an error is made in correction, a result descriptor with firecode error is sent.

The remainder of the flow continues as described in 207 End Test Routine.

207 Write

The 207 WRITE operation starts in mode 5 W12B8, where the correct address has been found. WRDATACM and FMWRZEROS cause the 207 drive to start writing zeros at the appropriate point in the format.

NOTE

Unlike the 206, the 207 controls the format on disk. Although a WRDATACM is sent at this time, the drive may not actually start writing until it reaches the correct point. The data is stored in an expandable shift register and is written at a time determined by the 207.

The flow enters mode 6 at W12B0. At W14B0, FMWRONES causes the data line to go high. This is for writing the data sync pulse.

Four bits later, at a W14B4, FMWRDATA causes the data to go out on the data line.

At W29B8, the address mark counter is cleared. This is no longer required since the address has been found.

At W104B4, FMWRFIRE causes the firecode to go on the data line. Fifty-four bits later, at W107B12, ALTGOWRZ causes the 3-byte, End-of-Record to be written.

FMGOIDLE causes the data circuits to go back to the inactive state. The drive stops writing by itself. A GOIDLECM is not required on the 207.

207 READ or VERIFY With Error Correction

An error correction READ consists of two phases:

1) Reading the information off disk and storing it in buffer memory. During this phase, data is not transferred to the DPC.
2) Reading the data out of buffer memory and correcting it while it is being transferred to the DPC.

Phase 1 occurs during the normal read data time. Phase 2 occurs during the time that the interleaving sector is passing under the heads. It is accomplished by repeating mode 6.

Error correction logic is controlled by error correction modes. During READ phase, ERCRMD1 is high for 180 bytes and 32 bits of firecode. ERCRMD2 is high for the remaining 24 bits of firecode.

ERCRMD3 is high at the start of the correction phase. ERCRMD 4, 5, or 6 are high during correction. (This is explained in detail in in section 4).

See the flow in figure 2-8, lower line. During the READ phase the flow is identical to a READ without correction. However, during this time, data is written into the buffer memory and CKDPC is not permitted. (This prevents data from being accepted by the DPC).

At W108B15, ERCRMD3 goes high (not shown on flow) so that at W109B14, CLSECLOC takes the flow back to the start of mode 6.

At W15B5, ENSNCDET enables the sync character detector; however, since a Read CM has not been sent, the data line is low. Therefore, it is not possible to detect four ones and get the signal STDTAXFER. ENSNCDET goes low at W15B7 when ERCRMD4 or 5 goes high.

At word 15 bit 5, STMMRD (start memory read) starts the READ operation. One hundred and eighty bytes of data plus seven bytes of firecode are read out and corrected.

At W15B7, the first bit is about to be sent to the parallel/serial/parallel register for conversion from serial flow to parallel flow. FMRDDATA synchronizes and conditions the information circuitry to transfer the data to the DPC.

The flow then goes to the 207 End Test Routine.

207 End Test Routine

Clock Seek status occurs at W109B14. This resets the seek status flip-flop to show that an overlapping seek operation has been serviced.

At W110B15, the flow terminates under the following conditions:

1) The DDEC is deselected indicating an end of READ, WRITE, or VERIFY.
2) Spare sector verify - this is a one sector operation.
3) End of pack.
4) Error correction - this is a one sector operation.

If the flow does not terminate at W110B15, this indicates that the processor requires to READ, WRITE, or VERIFY another sector. At W111B4, INNADRCT increments the address counter to the next sector and causes a new EPC to be generated for that sector address.

At W111B4, the flow may go to one of 2 modes:

1) If the address of the sector just read or written is the sector of the cylinder (ENDOFTRK * ENDOFCYL), a seek is required to the next cylinder. The flow goes to mode 2 W0B0.

2) If the sector just read or written is the last sector of the track but not the last sector of the cylinder, a head switch is required. The flow goes to mode 4. Also, if the sector just read or written is a relocated sector (forced head to spares, FCHDTOS), a head switch back to the original head is required.

If the flow does not go to mode 15, 2, or 4, the flow reaches W111B8. This indicates that another sector on the same track must be read or written. The flow goes back to mode 5 in order to search for the next address.

MODE 7 WRITE BEGINNING-OF-TRACK

This flow is only used when the unit selected is a 206, and the operation is initialize. Mode 7 is entered from mode 4 when the index pulse has been found (see figure 1-16). The sector location counter is at W1B1.

At W1B6, a write data CM is sent to the drive, and the format control causes the data line to be in a zero state.

Fifty-four bytes later, at W29B8, a write address mark CM is sent. This writes the first address mark of the track.

At W30B6, the address mark is complete on the track. The flow goes to mode 8 W0B0, with the drive writing zeros. (See figure 2-10).

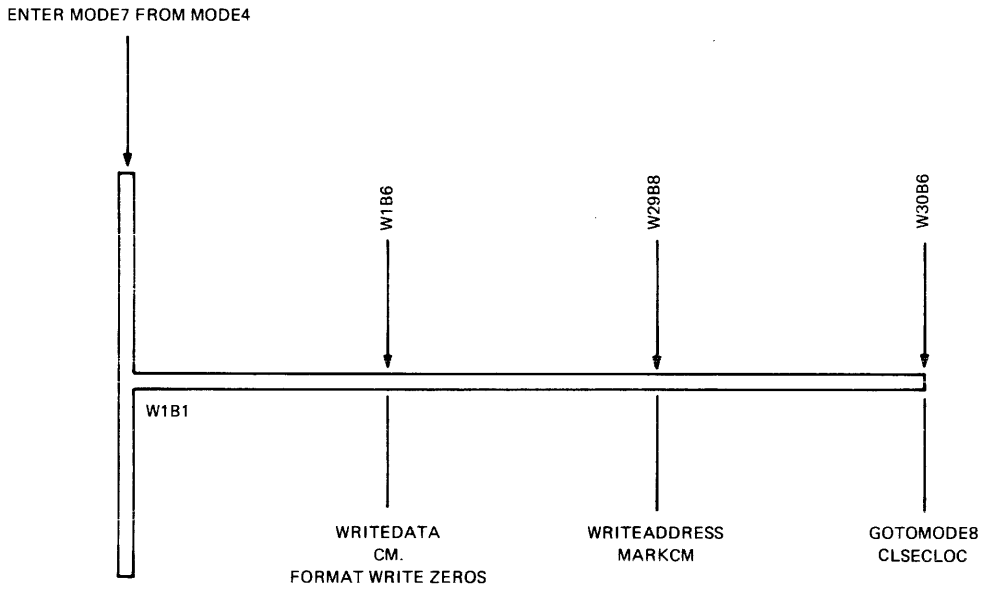


Figure 2-10. Mode 7, Write BOT OP

MODE 8 INITIALIZE SECTORS

Mode 8 is used in order to initialize the sectors into their format. Mode 8 is entered from mode 7 after writing the BOT and the first address mark (206), or from mode 4 when index is detected (207). Mode 8 is also entered from mode 10 when a sector is being relocated. (See figure 1-19). In all cases, the drive is performing a write when mode 8 is entered.

Mode 8 flow is divided into 206 and 207. Due to the different track format, the timing of the actions is slightly different. (See figure 2-11).

206 Operation

At W4B13, the format is changed to ones in order to write the sync character for the address field.

Four bits later, at W5B1, FMWRADDR causes the address to be placed, bit by bit, on the data line to the drive. The address includes the EPC which has been generated before the writing occurs. (EPC is described in a later section).

AT W7B1, the format is changed to FMWRZERO. This causes the data preamble of zeros to be written on the disk.

AT W16B9, FMWRONES places the sync character on the disk.

At W16B13, FMWRDATA places the data, bit by bit, on to the data line to the drive. During this time, the data used depends on the N2 variant of the OP. If N2=1, the DDEC requests one word of data from

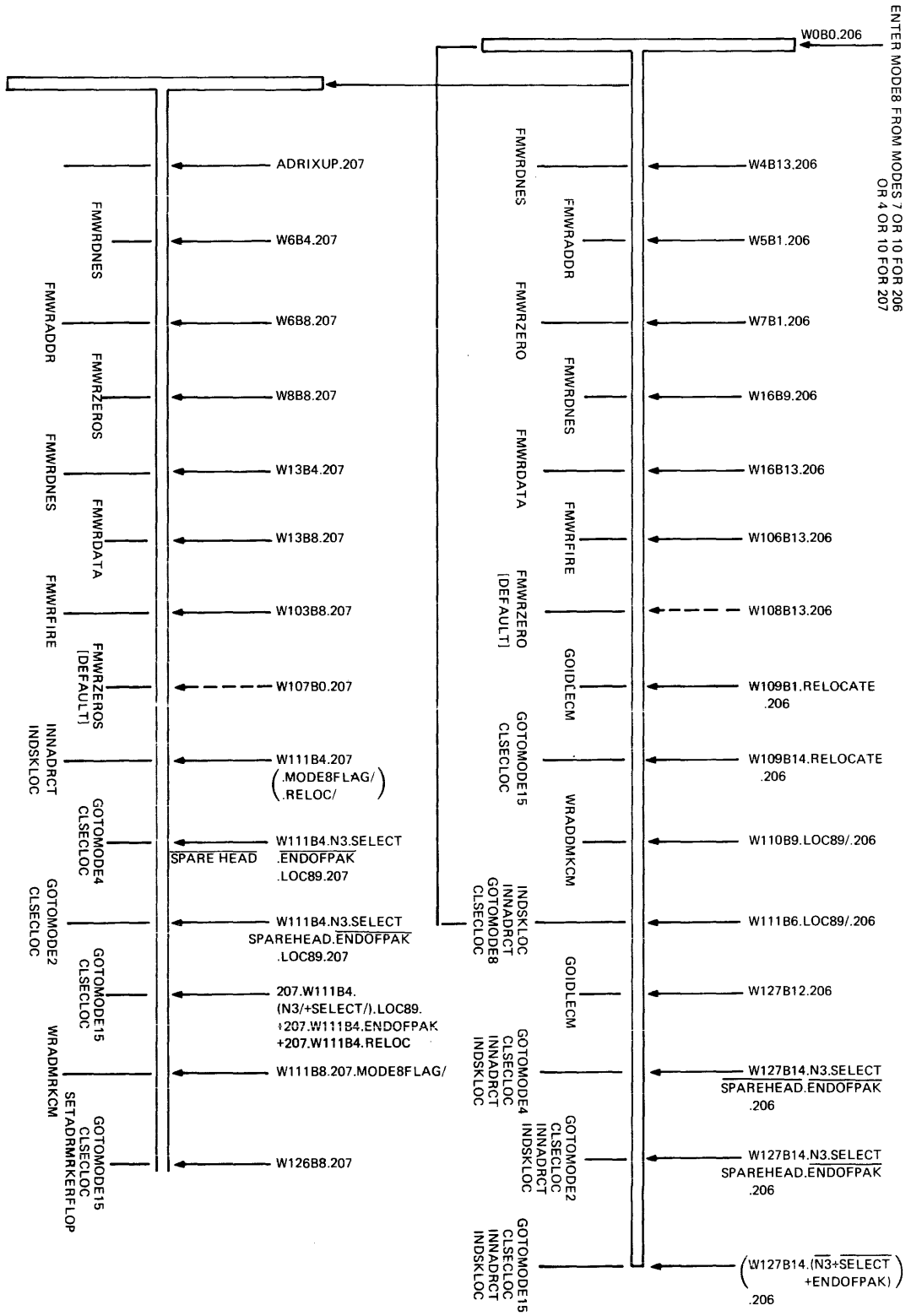


Figure 2-11. Mode 8, Track Format Mode

the DPC and uses this word 90 times. If N2=0, the two address words are repeated 45 times. As the data goes out to the drive bit by bit, the firecode is built up.

At W106B13, 180 bytes of information have been written. FMWRFIRE causes the firecode to be written to disk.

AT W108B13, FMWRZERO causes the End-of-Record zeros to be written. AT W109B1, on a RELOCATE OP, a GOIDLECM is sent to the drive. The GOIDLECM terminates the WRITE in the drive. During RELOCATE, only one sector at a time may be relocated; therefore, mode 8 lasts for only one sector.

At W109B14, on a RELOCATE OP, the flow goes to mode 15 W0B0 in order to terminate.

AT W110B9, if the disk location counter is not equal to 89 (LOC 89/), the DDEC sends another write address mark CM to the drive. Disk location counter not equal to 89 indicates that the disk has not reached the end of the track and more sectors must be initialized.

At W111B6 with LOC 89/, four actions are performed:

1) INDSKLOC - increment disk location counter places the new address at the output of the interleave logic for use in the next address header.
2) INNADRCT - increment address counter. This signal increments the address counter and causes the EPC to be generated for the next address.
3) GOTOMODE8 - go to mode 8.
4) CLSECLOC - cLear sector location counter. This is generated from the GOTOMODE8 signal. This takes the flow back to the start of mode 8 in order to initialize another sector.

If the disk location counter is equal to 89, indicating that 90 sectors have been initialized, the drive continues to write zeros from W108B13 through to W127B12. At this time, a GOIDLECM is sent to the drive. This action writes 38 bytes of zeros which includes:

1) Five bytes End-of-Record for the last sector.
2) Thirty bytes end-of-track.
3) Three extra bytes past the index pulse time. This ensures that there are no gaps left in the data.

At W127B14, the flow may go three ways:

1) If N3 is on (full pack variant), the DDEC is still selected, the head address is not head 4, and the end of pack has not been reached. The flow goes to mode 4 W0B0 for a head switch. The disk location counter is counted to 0, and the address counter is counted.
2) If N3 is on (full pack variant), the SELECT line is still high from the DPC, the head address is 4, and the end of pack has not been reached. The flow then goes to mode 2 for a seek to the next cylinder. This occurs when the end of a cylinder is reached. The disk location counter and the address counter are incremented.
3) If the operation is not a full pack initialize (N3/), the DPC has deselected the DDEC (SELECT/), or the end of the pack is reached, the flow goes to mode 15 W0B0 to terminate. The disk location counter and the address counter are incremented. This is redundant.

207 Operation

There are some fundamental differences between the 206 and the 207 which are reflected in the mode 8 flow.

1) The position of index. In the 206, index is in the EOT gap. The next sector is 45 which is the first sector to be initialized. In the 207, index is in the servo field for sector 89. The first sector to be initialized is 0. Therefore, sector 89 must be skipped at the start of INITIALIZE.
2) Address marks. In the 206, mode 8 writes the address marks. In the 207, the servo fields acts as address marks. The action of WRADDRMKCM on the 207 is to wait for the next servo field, return a DM with address or index mark detected, and to go into write mode at the end of guard band 2.
3) Write timing. In the 206, the flow of the controller determines the time at which the information is written on the track. In the 207, the time at which the WRITE takes place is determined by the 207. Therefore, write CMs and write data must be sent in advance of when they are required. The 207 buffers the information (up to 64 bits).

The flow is entered from mode 10 on a RELOCATE operation or mode 4 on an INITIALIZE operation.

If the flow has come from mode 4, index has been detected and sector 89 is about to pass under the heads. A WRADMRKCM has been sent to the drive. The drive does not go into write mode until after the servo field for sector 0 has been detected.

During the time that sector 89 is passing under the heads, the flow for mode 8 proceeds; however, the actions of the format logic are not significant since the drive is not writing. At W111B4, the address counter and disk location counter are not incremented because MODE8FLAG has been set at the end of mode 4.

AT W111B8, mode 8 flag prevents sending another WRADMRKCM to the drive.

When the servo field for sector 0 has been detect-

ed, ADRIDXUP goes true which takes the flow back to W0B0 by CLSECLOC. Mode 8 flag is reset.

The mode 8 flow starts again at W0B0 with the drive in WRITE mode.

If mode 8 is entered from mode 10, a WRADMKCM is sent at the end of the previous sector, and FMWRZEROS is holding the data line low. As soon as the address mark is detected, CLSECLOC takes the flow to W0B0. MODE 8 flag is low.

AT W6B4, ones are sent on the data line for the address sync character.

Four bits later, FMWRADDR places the address and EPC on the data line to the drive.

At W8B8, FMWRZEROS causes the date line to go low for the data preamble.

The data line goes high (FMWRONES) at W13B4. This is for the data preamble.

Four bits later, at W13B8, FMWRDATA causes the data to go out serially on the data line.

AT W103B8, the firecode (56 bits or seven bytes) is sent out, and at W107B0, FMWRZEROS causes the data line to go low. The drive uses this to write the End-of-Record gap. The drive automatically goes out of write mode at the end of the EOR gap, thereby protecting the guard band 1 and the servo field.

At W111B4, on an INITIALIZE operation only, the disk location counter is incremented so that the address from the interleave logic points to the next sector. INNADRCT increments the address counter and causes a new header to be generated (address and EPC).

If loc 89 is high at W111B4, the last sector of the track has been initialized (sector 89). If N3 is high (full pack initialize) and SELECT is high, the flow goes to mode 4 if a head switch is required or mode 2 if a SEEK is required. This is determined by the signal SPAREHEAD. SPAREHEAD being high indicates that head 7 is selected, and a SEEK is required.

The operation goes to mode 15 to terminate from W114B4 at the end of the track under the following conditions:

1) N3/ *LOC89 - the end of a single track initialize.
2) Select/* LOC89 - DDEC deselected by DPC.
3) End of pack.
4) RELOC - relocation is a single sector operation.

If the flow does not go to mode 4, 2, or 15, this indicates the end of a sector. There are more sectors to initialize on the same track.

At W111B8, WRADMRKCM requests an address mark for the next sector. When ADRIDXUP goes true, the flow returns to W0B0 and repeats.

If ADRIDXUP does not occur due to a failure, the flow continues to W126B8. At this time, the ADRMRKER FF is set and the flow goes to mode 15 W0B0 to terminate. A result descriptor with TD set is sent to the DPC.

MODE 9 DISK LOCATION SYNCHRONIZE

Mode 9 is used in the RELOCATE and READ MAINTENANCE operations. It is used to check that the cylinder and head address written in the addresses agree with the cylinder and head address requested in the initiate words of the operation. If the correct cylinder and head are not found in 128 sectors, the operation is terminated. See figures 1-19 and 1-22 in order to see how mode 9 is used in these operations.

Mode 9 is entered from mode 4 or mode 11, at W0B0.

206 Operation

At W1B11, a read address mark CM is sent to the drive and the 250 micro-second timer is started.

By W3B14, the ROGERDM should be back. If it is not back (ROGERDM/), the flow goes to mode 15 to terminate. If the ROGERDM is high, the sector counter is halted. The flow is now controlled by the address mark DM coming back from the drive.

When the address mark is received ADRIDXUP is true (Address Mark or Index Mark received). INSECLOC permits the sector location counter to continue.

If an address mark failed to return, the 250 microsecond timer times out (TM0T250U). If this occurs, the operation does not fail. Address mark error flip-flop is set in case the operation does subsequently fail. However, at this time the flow goes back to the beginning of mode 9 to read the next address mark. The DSKLOC counter and the address mark counters are incremented.

Assuming an address mark is received, the flow continues until W5B15. With address sync start not found (ADSNCSTF/), the sync character detection logic is enabled (ENSNDET). The drive is still reading.

At W9B15, the signal TSTSTKDT (Test Stuck Data) allows the logic to monitor the stuck data flip-flop. If the data line from the drive is either high or low, the stuck data flip-flop has failed to set. This error condition is loaded into the ERD register, if the operation subsequently fails.

When the sync character of the address field is found (ADSNCSTF), the sector location counter is loaded to W5B4, synchronizing it with the data on the disk. STADRCMP (start address compare) permits the address information being received from the disk to be compared with the address in the address counter.

At W6B6, with address sync start found (ADSNCSTF), a GOIDLECM is sent to the drive. The drive stops reading.

At W11B14, if the cylinder and head address are

not equal or the sync character has not been found and 128 addresses have not been tried (ADMRK 127/), the flow goes back to the beginning of mode 9 to try the next sector.

If the cylinder and head address are equal at W11B14, the sync detection logic is disabled (ENSNCDET/), and the flow goes to mode 10 for a dead reckoning address search.

If 128 sectors have been tested without an equal comparison (ADMRK 127), flow goes to Mode 15 W0B0 to terminate the operation.

207 Operation

Mode 9 is entered from mode 4 with a RDADRMRK in progress and the MODE9FLAG set.

A ROGERDM is required to the RDADRMKCM by W3B14; otherwise the flow goes to mode 15 to terminate. The purpose of the MODE9FLAG is to permit this action at this time.

When the address mark has been found, ADRIDXUP resets the mode 9 flag and clears the sector location counter to W0B0. The flow proceeds to the lower line of figure 2-12.

At W6B6, if 127 address marks have been counted, the address does not agree; therefore, the flow goes to mode 15 W0B0. On a RELOCATE, an address error is reported in the result descriptor.

At W8B1, the sync character detector is enabled. The address sync character is expected back by W10B1. If ADSNCSTF is not high by this time, the following actions occur:

1) ENSNCDET/ - sync character detector disabled.
2) TSTSTKDT - test the stuck data detector. If there have been no transitions, a TD is reported in the result descriptor.
3) INADRMRK - increment address mark counter. This enables the flow to detect when 127 addresses have been tested.
4) INDSKLOC - increment disk location counter. This is required for a dead reckoning address search in Mode 10.
5) RDADMRKCM - read address mark CM starts a read of the next address.

If the address sync character is found before W10B1, the previous five (5) actions do not occur. LDSECLOC to W9B8 synchronizes the sector location counter with the address information. STADRCMP starts the address compare looking for the cylinder and head addresses to be equal.

At W12B18, if the cylinder and head addresses are equal, the flow goes to mode 10 for a dead reckoning address search.

If CYLHDEQL/ is high at W12B18, the address does not compare. In this case, a RDADDRMRKCM is sent to try the next address. INADRMRK increments the address mark counter. INDSKLOC increments the disk location counter.

The flow is now controlled by ADRIDXUP. If the address mark returns before W126B8, the sector location counter is cleared and the flow starts again from W0B0 on the lower line of the flow.

If W126B8 is reached before ADRIDXUP occurs, ADRMRKER flip-flop is set and the flow goes to mode 15 W0B0 to terminate with a TD result descriptor.

MODE 10 DEAD RECKONING ADDRESS SEARCH

Mode 10 is used in the RELOCATE and READ MAINTENANCE operation in order to locate a sector by counting clocks and address marks. When mode 10 is entered, the disk location counter has been synchronized at index time and is holding the current disk location.

The interleave sector address is being compared to the sector address counter (on a READ MAINTENANCE or first pass of RELOCATE) or the N variants + 84 (on the second pass of RELOCATE). The result of this comparison is DSKLOCEQ (disk location equal) or DSKLOCEQ/ (disk location not equal).

206 Operation

The mode 10 flow goes two ways depending on DSKLOC EQL. If the comparison is not equal, the flow goes to the lower left hand side of figure 2-13.

The flow starts at W0B0.

At W29B8, and DSKLOCEQL/, the LOOPMODE 10 flip-flop is set. This prevents an exit from mode 10.

At W61B14, a test is made to see if the BOT/EOT gap is under the head. If LOC=0 (disk location = 0) is true, and the operation is a RELOCATE, the sector location counter is loaded 45 words backwards. This action ensures that the sector location counter is in synchronization at the beginning of the first sector. (The EOT gap is 90 bytes or 45 words long). The sector location counter is loaded to W17B0.

At word 108 bit 15, the data is at the end of a sector. The disk location counter is incremented so that a new comparison may be made.

At W111B7, the flow goes back to the start. Loop mode 10 flip-flop is reset.

The flow may loop for many sectors down to the DSKLOCEQL/ path; however, when the desired sector is reached, the signal DSKLOCEQL takes the flow along the upper path of figure 2-13.

The upper path of the mode 10 flow is divided into 206 and 207. On the left hand side is the 206 flow. On the right hand side is the 207 flow.

At W29B8, with DSKLOCEQ and not a RELOCATE OP, the operation must be READ MAINTENANCE. The correct sector has been found; therefore, a Read Address mark CM is sent to the drive.

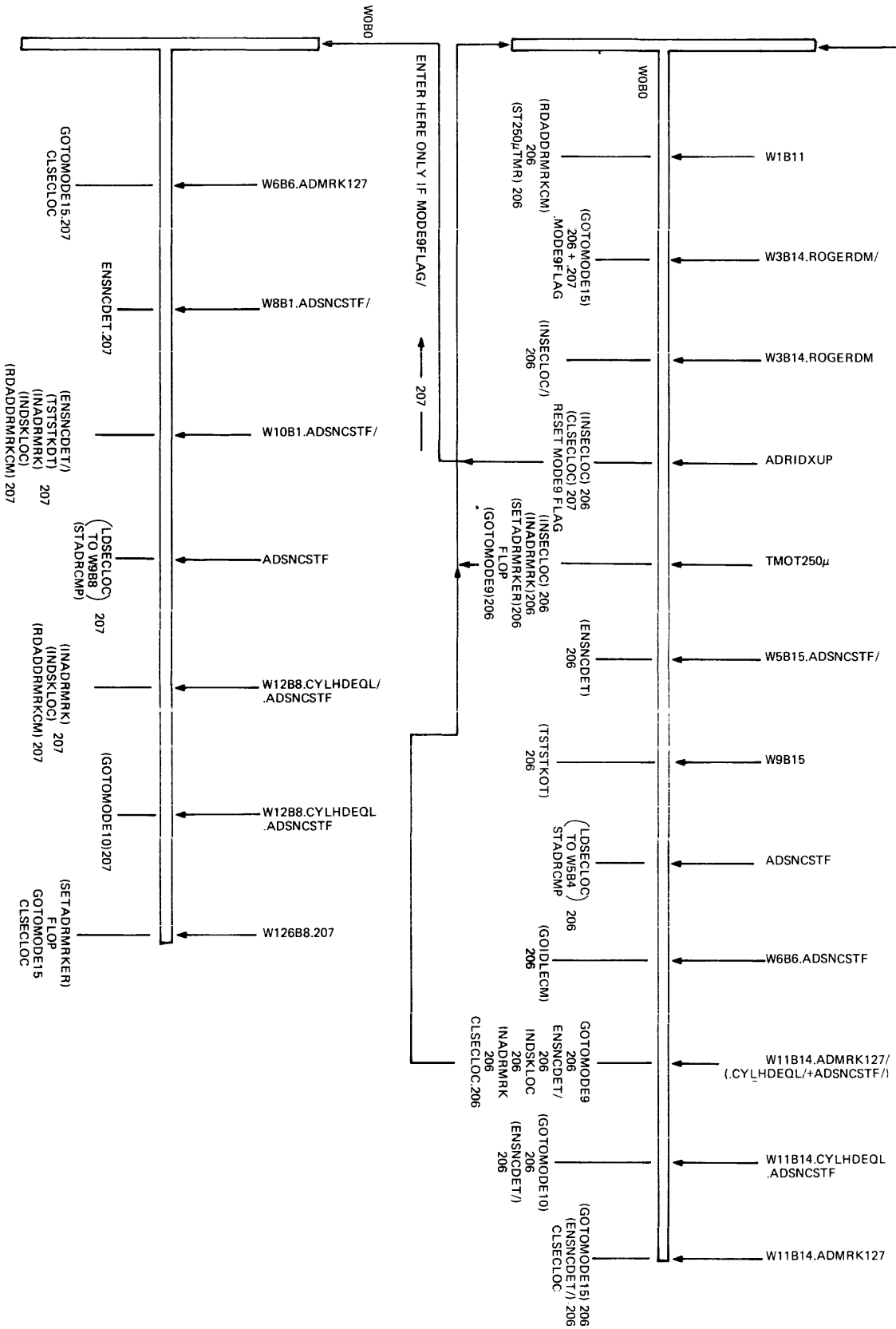


Figure 2-12. Mode 9, DSK LOC SYNC

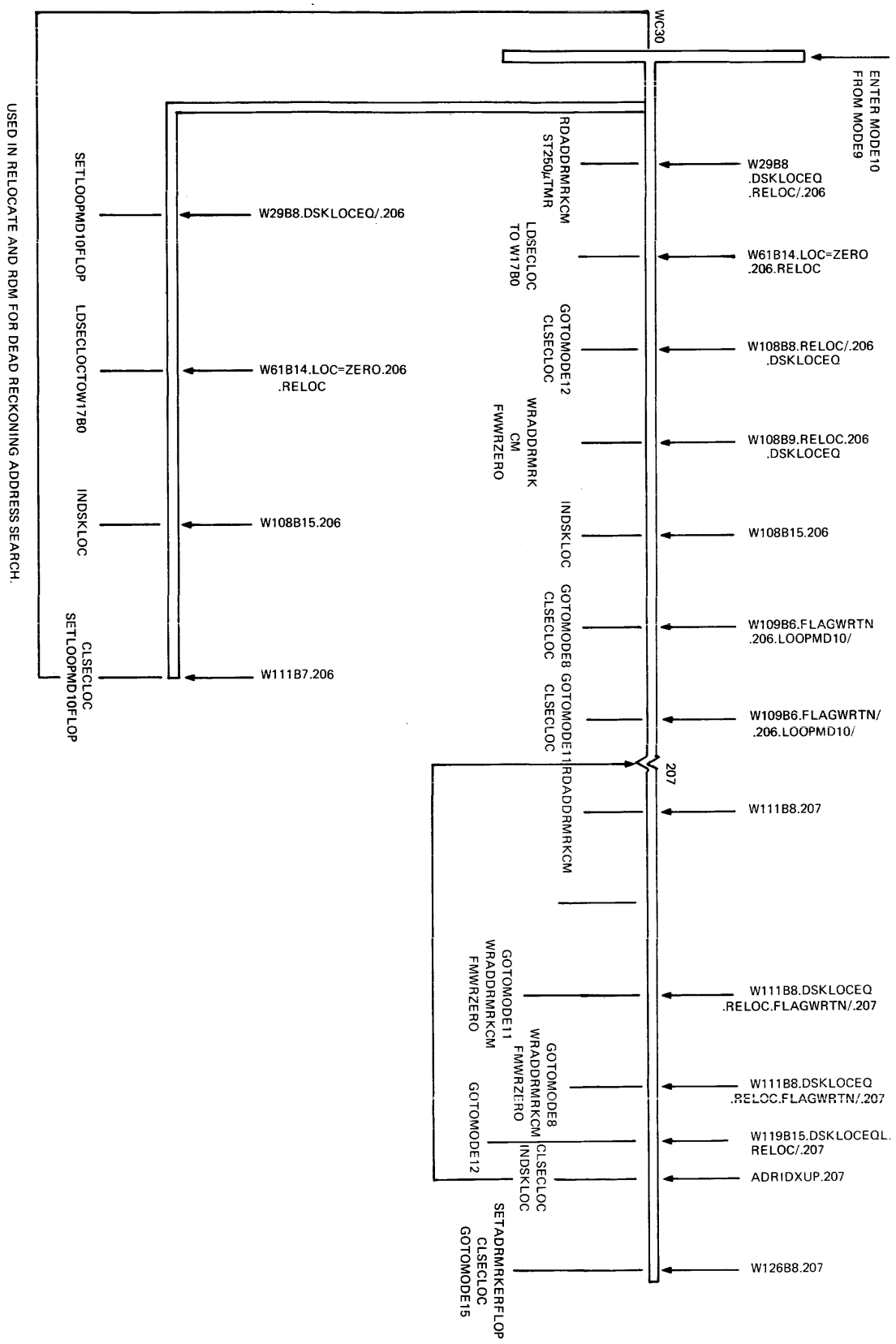


Figure 2-13. Mode 10, Dead Reckoning Address Search

However, the address mark is still approximately 80 words away.

At W61B14 and LOC=0 and a RELOCATION operation, the sector location counter is loaded to W17B0. This resynchronizes the sector location counter to sector 45 after the EOT/BOT.

At W108B8, on a READ MAINTENANCE (RELOC/), the flow goes to mode 12 for the READ operation.

At W108B9, on a RELOCATE operation, a write address mark CM is sent to the drive. This action writes an address mark. FMWRZEROS causes the drive to start writing zeros after the address mark.

At W108B15, the disk location counter is incremented. Although the address has been found, disk location sync is still required because this may have been the first pass of RELOCATE. Sync is retained so that the spare sector may be located the same way by a second pass through mode 10. (See figure 1-19).

At W109B6, the flow goes one of two ways depending on whether it is the first pass of RELOCATE or the second pass of RELOCATE. When the first pass of RELOCATE is complete, FLAGWRTN (flag written) is set to indicate that the address field of the sector containing the flaw has been overwritten. FLAGWRTN indicates the second pass.

If this is the first pass (FLAGWRTN/) the flow goes to mode 11 to overwrite the bad sector. The drive is in a write condition, writing zeros.

If this is the second pass (FLAGWRTN), the flow goes to mode 8 in order to initialize the spare sector just located. The drive is in a write condition writing zeros.

207 Operation (DSKLOCEQL)

The 207 flow is shown at the top right hand section of figure 2-13. The flow is entered from mode 9.

If the interleave sector address is equal to the address counter (sector inputs) on a READ MAINTENANCE or the first pass of RELOCATE, or equal to the N variant + 84 on the second pass of RELOCATE, DSKLOCEQL is high.

At W111B8, a RDADRMRKCM is sent so that the flow may be started on the next sector.

If DSKLOCEQL is high, at W111B8, and the operation is RELOCATE, the flow goes to mode 11 or mode 8. On the first pass of RELOCATE, the flow goes to mode 11 to overwrite the address of the defective sector. On the second pass of RELOCATE, FLAGWRTN is high; therefore, the flow goes to mode 8 in order to RE-INITIALIZE the sector with the new address.

At W119B15 and a READ MAINTENANCE operation, (RELOC/), DSKLOCEQ takes the flow to mode 12 for a READ operation.

If the flow does not go to modes 11, 8, or 12, it is controlled by ADRINDXUP. When the address mark is received, the flow goes back to W0B0. The disk location counter is incremented so that a new interleave address may be compared.

If the address mark is not returned by W126B8, the address mark error flip-flop is set and the flow goes to mode 15 W0B0. A result descriptor with TD is sent to the DPC.

MODE 11 OVERWRITING A BAD SECTOR

See figure 2-14 for the following discussion.

206 Operation

At W4B13, the address preamble is complete. FMWRONES places ones on the data line.

At W7B1, the address field has been overwritten with ones. FMWRZEROS now writes zeros. FLAGWRTN (flag written) is set so that the mode 10 flow goes to mode 8 after the next dead reckoning address search (in order to initialize the spare sector).

At W11B13, a GOIDLECM is sent to the drive so that it stops writing. FMGOIDLE places the format control in a idle state.

At W14B2, the signal CMSELSPR (CM select spare) causes head 4 to be selected in the DDEC internal logic. The old head address is still retained in the address counter.

At W64B14, and if the old head address is not four (SPAREHEAD/), a head 4CM is sent to the drive. The signal CM2-0M11 causes a new address header to be used in the mode 9 disk location sync.

At W104, the disk location counter is incremented because another sector has passed. The flow goes to mode 9 W0B0.

207 Operation

The 207 flow of mode 11 proceeds along the lower line of figure 2-14. Mode 11 is entered from mode 10. A WRADRMRKCM has been sent to the drive and the format logic is holding the data line low (FMWRZEROS).

ADRIDXUP is expected back from the drive before W126B8. If W126B8 is reached, address mark error flip-flop is set, and the flow goes to mode 15.

If ADRIDXUP occurs before W126B8, the sector location counter is cleared to W0B0.

At W6B4, FMWRONES places the data line high. This causes the address to be written with ones.

At W8B8, the address has been written with ones. FMWRZEROS changes the data line to low. FLAGWRTN is set to show that the address is overwritten. This causes the second pass of RELOCATE to go to mode 8 instead of mode 11.

At W11B13, CMGOIDLE causes the drive to stop writing so that the data field is not overwritten.

At W14B2, CMSELSPR causes the CM head address multiplexor to select head 7 if the head address

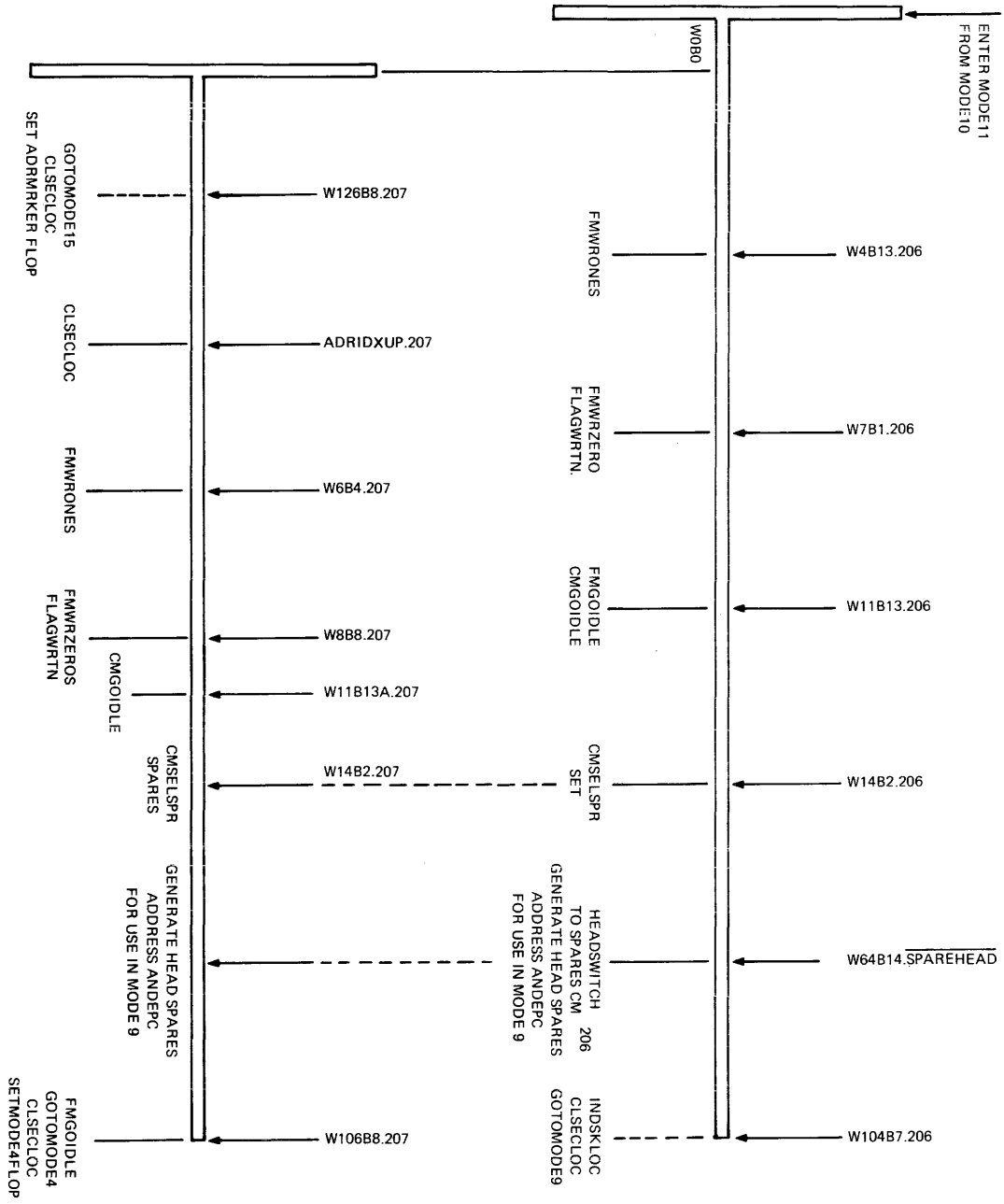


Figure 2-14. Mode 11, Overwriting Bad Sector

is not already equal to 7. The head address in the address counters is not affected, only the address going to the CM.

At W64B14, the signal CM2-0M11 causes a new header to be generated if the head address in the address counter is not 7. This header is be used in mode 9 to check that the drive is on head 7 of the correct cylinder. Again, the address counter is not affected; head 7 is selected through a multiplexor as input to the EPC generation circuit.

At W106B8, the flow goes to mode 4 in order to perform the head switch to the spare head. FMGOIDLE, CLSECLOC, and the set mode 4 flop are active.

MODE 12 READ MAINTENANCE SECTOR TRANSFER

Mode 12 is used in order to transfer the entire contents of the sector to the DPC. This includes preamble, sync character, address, EPC, data preamble, data sync character, data, firecode, and End-of-Record.

The data may be used for diagnostic purposes.

The sync detector is not used (because the problem could be in the sync detector); therefore, the byte/bit relationship may not appear correctly on a printout or display.

Mode 12 is entered from mode 10. The desired sector has been located by dead reckoning, and a read address mark has been started in the drive.

206 Operation

See the top line in figure 2-15.

At W2B1, the sector location counter is halted, while the drive searches for the next address mark (INSECLOC/).

When the address mark is received (ADRIDXUP), INSECLOC allows the sector location counter to continue. If the address mark failed to return, the 250 micro-second timer times out (TMOUT250U). This also allows the sector location counter to resume counting. (If the timer times out, the subsequent data has little or no meaning). TMOUT250U sets address mark error FF.

At W2B14, FMRDDATA causes the data being received from the drive to be stacked up from serial into parallel and sent to the DPC a word at a time.

At W6B12, the end of the address and EPC has been reached. GOIDLECM causes the drive to stop reading.

At W10B14, a RDDATACM is sent to the drive. This is necessary because the drive has to resync on the data preamble. (The address information and the data information are not in sync except after initialize).

At W118B7, the complete sector has been read. GOIDLECM terminates the read in the drive.

At W119B15, FMGOIDLE terminates the sending of data to the DPC. The flow goes to mode 15 W0B0. An address error is always reported in the result descriptor of a READ MAINTENANCE operation.

207 Operation

The 207 flow proceeds along the lower line of figure 2-15. The flow is entered from mode 10 after a dead reckoning address search. A read address mark is in progress.

If the sector location counter reaches W126B8, the flow goes to mode 15 to report an address mark error. Normally, ADRIDXUP occurs before this time, giving CLSECLOC which takes the flow to W0B0.

AT W2B14, FMRDDATA causes the incoming data to be converted from serial to parallel and sent to the DPC. At this time, the address is about to arrive from the drive.

At W12B8, the address has been read, RDDATACM causes the drive to resynchronize on the data preamble. FMRDDATA is still active; therefore, the data field is sent to the DPC, 16 bits with each CLKDPC.

The complete data field, including firecode and End-of-Record, has been transferred to the DPC. FMGOIDLE inactivates the format logic. The flow goes to mode 15 W0B0 to return a result descriptor containing address error.

MODE 13 SEND EXTENDED RESULT DESCRIPTOR

See figure 2-16 for the following discussion.

Mode 13 is entered from mode 1 on a Send ERD operation. This mode is the same for 206 or 207. The ERD has no unit identifier in the OP initiate word.

At W0B15, STERDOUT (start ERD OUT) causes the ERD logic to pass one word at a time on to the data bus. FMRDDATA causes these words to be sent to the DPC with a DPC clock pulse.

When the four ERD words have been sent, ERDXMTNG (ERD Transmitting) goes low. FM GOIDLE causes the format logic to stop sending data to the DPC.

At W11B14, the flow goes to mode 15 W0B0. On a send ERD operation, the result descriptor sent in mode 15 always contains zeros.

The ERD logic is described in detail in a later section.

MODE 14 TEST OP

See figure 2-17 for the following discussion.

Mode 14 is entered from mode 1. In mode 1, the DDEC received the status of the drive selected. Mode 14 is used to perform the two variants possible in a test OP.

At W0B14, if N3 is on, a Remote Power Down CM is sent to the drive.

Also, at W0B14, if N2 is on, CLALSKST (clear all seek status) clears the seek status flip-flops for all the units.

At W0B14, the flow goes to mode 15, in order to send the result descriptor containing the status of the drive.

MODE 15 TERMINATE AND REPORT

See figure 2-18 for the following discussion.

Mode 15 is used in order to terminate all operations, request the latest status from the drive, and send a result descriptor to the DPC. Mode 15 may be entered from any mode except mode 0.

The GOTOMODE15 signal causes the READY line to drop to the DPC. This informs the DPC that the result descriptor phase has started. GOTOMODE15 also resets INCSECLOC; therefore, the sector location counter is always in a halted state when mode 15 is entered.

All the conditions that cause the flow to GOTOMODE15 may be seen in the logical equations in the T & F (Test & Field) documents, section 5.

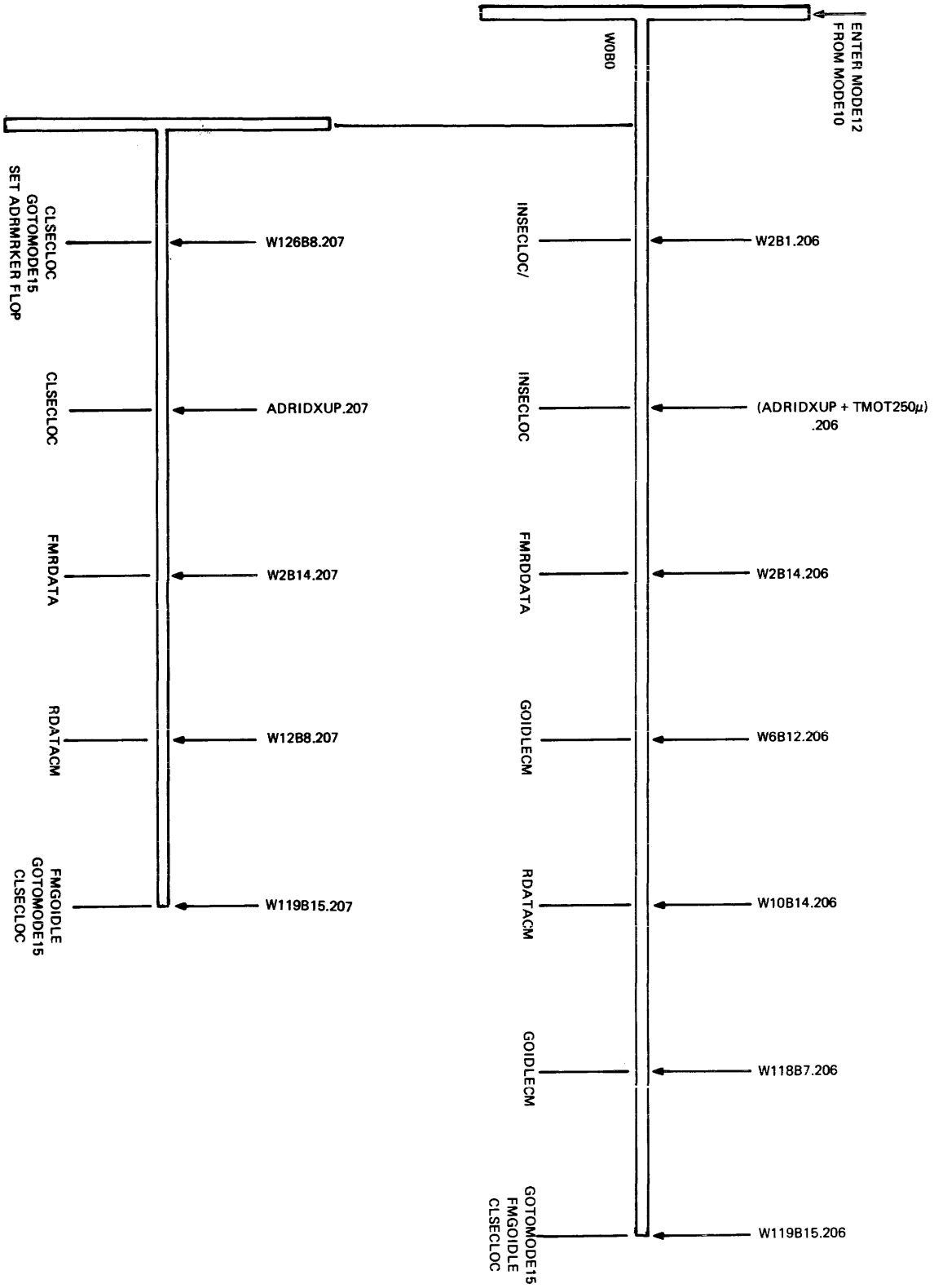
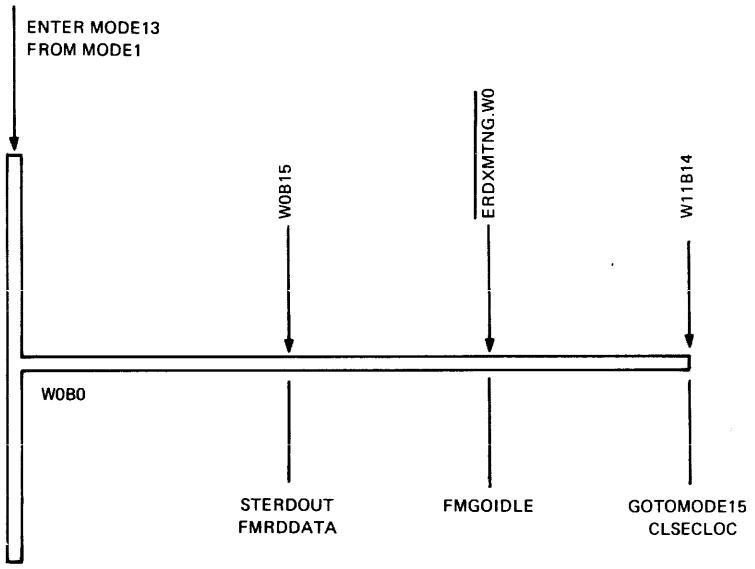
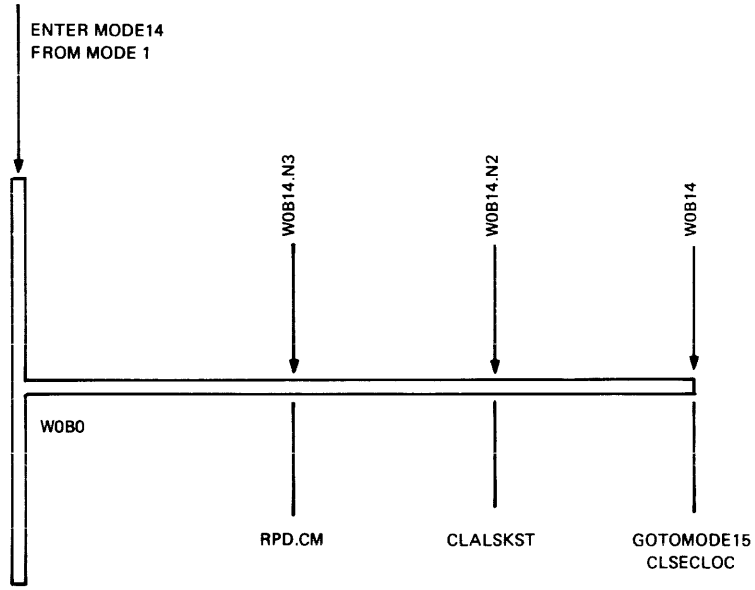


Figure 2-15. Mode 12, RDM Sector Transfer



USED TO SEND EXTENDED STATUS RESULT DESCRIPTOR TO PROCESSOR

Figure 2-16. Mode 13, SENDERD Mode



USED AS A TESTOP (OPTIONAL POWER DOWN AND CLALSKST)

Figure 2-17. Mode 14, Test OP

At W0B0, INSECLOC starts the sector location counter if either of the following conditions are true:

1) NO ROGERDM - this indicates that the drive failed to acknowledge a CM within 65ms.
2) DRONLINE/ - the drive is off line.
3) DMRCVD - DM received.

At this time, the flow waits until a DM has been received except if the drive is offline or if the drive is not responding to CMS. This allows any communications in progress to complete before proceeding. GOTOMODE15 may occur at any time with certain error conditions, even in the middle of a CM going out.

At W0B14, a status CM is sent to the drive provided that the operation is not a test OP or a send ERD. This is necessary so that the temperature warning bit in the drive may be tested. If temperature warning is on, the TRY DIAGNOSTICS bit must be set in the result descriptor. This occurs only if the previous long DM for this drive does *not* contain a temperature warning.

At W8B15, FMSENDRD causes the result descriptor to be sent to the DPC. If RDBIT15 is true (TRY DIAGNOSTICS) CKSKSTAT clears the seek status bit. This is done so that the system software does not miss the TD bit. (The system software ignores the TD bit if a seek status bit is found).

At W11B14, BUSY is dropped to the DPC indicating the end of the operation. Seek status flip-flop is set if SETSKSTS has been set in mode 3 (overlapping seek).

At W11B13, the flow goes to mode 1 W0B0 with the sector location counter halted. This is the idle condition.

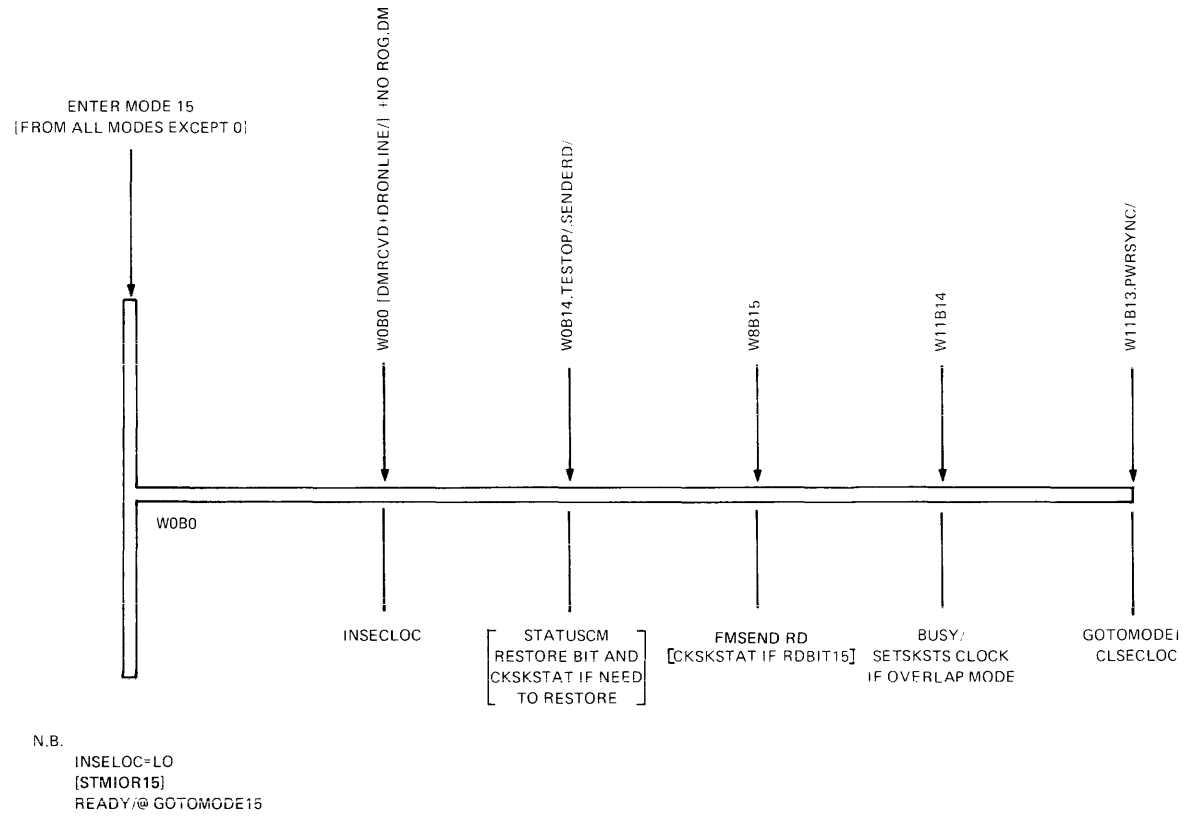


Figure 2-18. Mode 15, Terminate and Report

SECTION 3

ADDRESS RELATED CIRCUITS

DISK LOCATION COUNTER AND INTERLEAVE LOGIC

The disk location counter and interleave logic is used during INITIALIZE, RELOCATE, and READ MAINTENANCE. It is used to generate the sector information to be written during an INITIALIZE operation. It is also used in order to locate a sector by dead reckoning during READ MAINTENANCE and RELOCATE.

See the block diagram in figure 3-1.

The disk location counter is cleared to zero at index search time and is then counted up with each sector, 0 through 89, as the pack rotates. When the counter is at 89, this indicates the last sector of the track (which is 44 for 206, 89 for for 207). From 89, the counter starts at zero again. Refer to table 3-1. Column 1 is the sector position. Column 2 is the disk location counter.

The interleave logic generates a sector address from the disk location counter output in accordance with the interleaved format used. This is generated in the following manner.

The seven most-significant bits of the counter are taken to two places:

1) An adder where a fixed constant of 45 is added to it.
2) An 8-bit, two source, data selector. The other input to the data selector is the sum.

Therefore, the data selector has two inputs:

1) The seven most-significant bits of the disk location counter. (Refer to column 3, table 3-1).
2) The seven most-significant bits plus 45.

The selection of the inputs is accomplished by the least-significant bit of the disk location counter to give the interleave sector outputs shown in column 5. At every even disk location, 45 is added for 206. At every odd disk location 45 is added for 207.

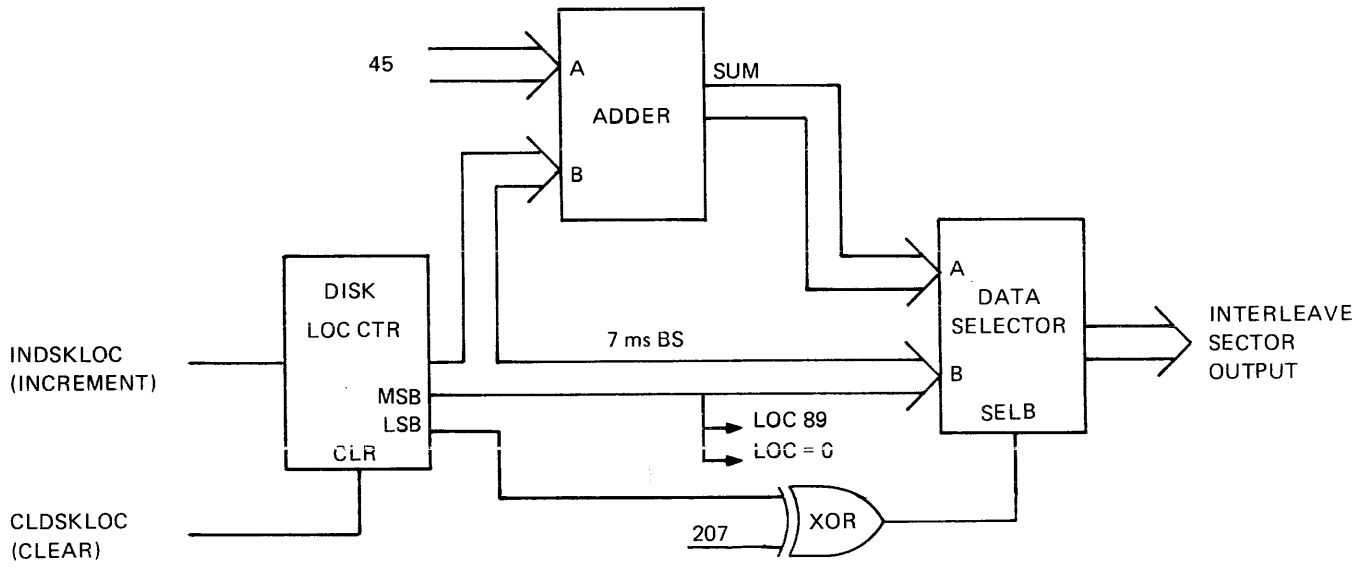


Figure 3-1. Disk Location Counter and Interleave Logic

SECTOR ADDRESS POSITION		DISK LOCATION COUNTER	DISK LOCATION COUNTER M.S. BITS	SELECTION M.S. BITS OR M.S. BITS +45		INTERLEAVE SECTOR OUTPUTS	
206	207			206	207	206	207
45	0	0	0	+45		45	0
0	45	1	0		+45	0	45
46	1	2	1	+45		46	1
1	46	3	1		+45	1	46
47	2	4	2	+45		47	2
2	47	5	2		+45	2	47
48	3	6	3	+45		48	3
3	48	7	3		+45	3	48
49	4	8	4	+45		49	4
4	49	9	4		+45	4	49
ETC	ETC	ETC	ETC	ETC	ETC	ETC	ETC
88	43	86	43	+45		88	43
43	88	87	43		+45	43	88
89	44	88	44	+45		89	43
44	89	89	44		+45	44	89

Table 3-1. Disk Location and Interleave Outputs

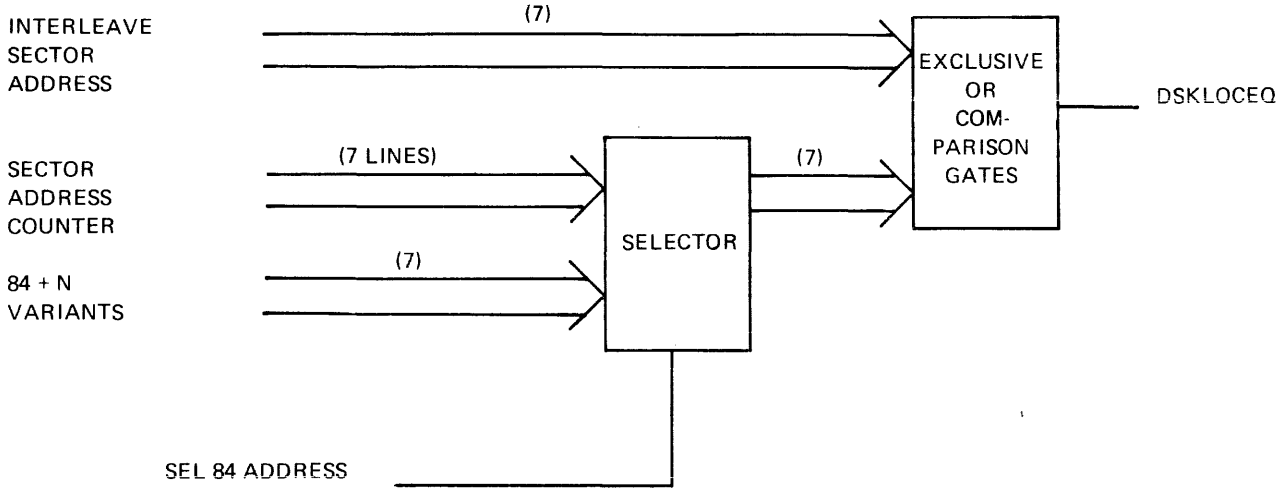


Figure 3-2. Disk Location Equal Logic

Disk Location Equal Logic

See schematic 09.02.05 for the following discussion.

During READ MAINTENANCE and the first pass of RELOCATE, a dead reckoning address search is performed. DSKLOCEQ (disk location equal) is made true when the address is found. (See figure 3-2).

The disk location counter is cleared at index time and is allowed to count up on each sector as the disk rotates. The interleave output is compared to the sector lines from the address counter. When the interleave output compares with the address counter, DSKLOCEQ is made high.

During the second pass of a RELOCATE operation or on a spare sector VERIFY operation, the N variants determine which spare sector is used.

N3	N2	N1	Sector
0	0	1	85
0	1	0	86
0	1	1	87
1	0	0	88
1	0	1	89

Table 3-2. N-Variant Address

The signal SEL84ADR (select 84 address) permits the N variants plus 84 to be compared with the interleave sector address. This is accomplished by two quad 2-1 line selectors. When the interleave sector address has counted up to the value of the N variants plus 84, DSKLOCEQ goes high. This indicates that the disk has reached the spare sector addressed.

ADDRESS DECODE

General Description

The purpose of the address decode circuit is to accept a binary address from the DPC and decode it into cylinders, heads, and sectors.

The decode is accomplished by a process of division. The following decimal example illustrates the principle:

Address received = 294342.
There are 445 sectors per cylinder (206).
Therefore, the number of cylinders = 294342÷445 = 661 with a remainder = 197.
There are 90 sectors per head.
Therefore number of heads = 197÷90 = 2 with a remainder = 17.
Therefore the decoded address = CYL 661, HD2, SEC17.

If the unit selected is a 207 unit, the number of sectors per cylinder is 715; therefore, division is performed by 715. The number of sectors per head is the same.

Division is accomplished in the logic by subtraction and shifting.

Throughout the rest of address decode, refer to schematic 01, pages 01 to 07; block diagram, figure 3-3; and timing diagram, figure 3-4.

Address Constants

Subtraction is accomplished by adding the complement of a constant plus 1. The constant varies according to whether cylinder or heads are being decoded. Also, when cylinders are being decoded, the constant varies according to whether the drive is a 206 or 207.

There are 12 bits of constant data fed to the adder, numbered 0 through 11. Table 3-3 shows the constant generator output under all possible conditions. Low totals are shown in parentheses.

Bit	Binary Weight CYL Decode	HD Decode	206 CYL Decode	207 CYL Decode	Head Decode
11	1024	128	H	H	H
10	512	64	H	L	L
9	256	32	L	H	H
8	128	16	L	L	L
7	64	8	H	L	L
6	32	4	L	H	H
5	16	2	L	H	H
4	8	1	L	L	L
3	4		L	H	L
2	2		H	L	L
1	1		H	H	L
0	0		L	L	L
Total	2047	255	1603 (444)	1333 (714)	166 (89)

Table 3-3. Address Constants

Cylinders are decoded while ADCYLHD is high. Heads are decoded while ADCYLHD is low during state 13, 14, and 15 of the address state counter.

Binary Address Loading

The binary address is received from the DPC in two words. In the first word, bits 2*0 through 2*4 (1,2,4,8,16) are received on INFO 11 through 15. They are placed on the data bus. In the second word, bits 2*5 through 2*19 are received on INFO 00 through 14 respectively. INFO 15 is labelled as 2*20; however, this bit is not used.

At W0B11, CKWORD1 is generated. This signal synchronizes the 5 MHz clock to the trailing edge of the 10 MHz clock and generates ADCLOCK and ADCKNWD2 (address clock not word 2).

ADCKNW2 clocks the address information received in the first initiate word into the 6-bit, D-type flip-flops. ADSTATE0 (address state 0) permits DATA11 to enter through the 2-to-1 multiplexor. The LSB is not used at this time.

ADCLOCK counts the address state counter so that ADSTATE0 goes low. The counter is now in state 1.

The DPC places the second initiate word on the INFO lines. AT W1B11, ADCLOCK is generated again. The address state counter is in state 1; therefore, ADLDREG/ is low. This permits the data bus to pass through the 12-bit multiplexor to the 12-bit register. ADCLOCK loads the address from the multiplexor into the 12-bit register. ADCLOCK also loads the 8-bit register in the following way:

Four bits from DATA 00 through 03 (data bus).
Four bits from the 6-bit, D-type flip-flops.

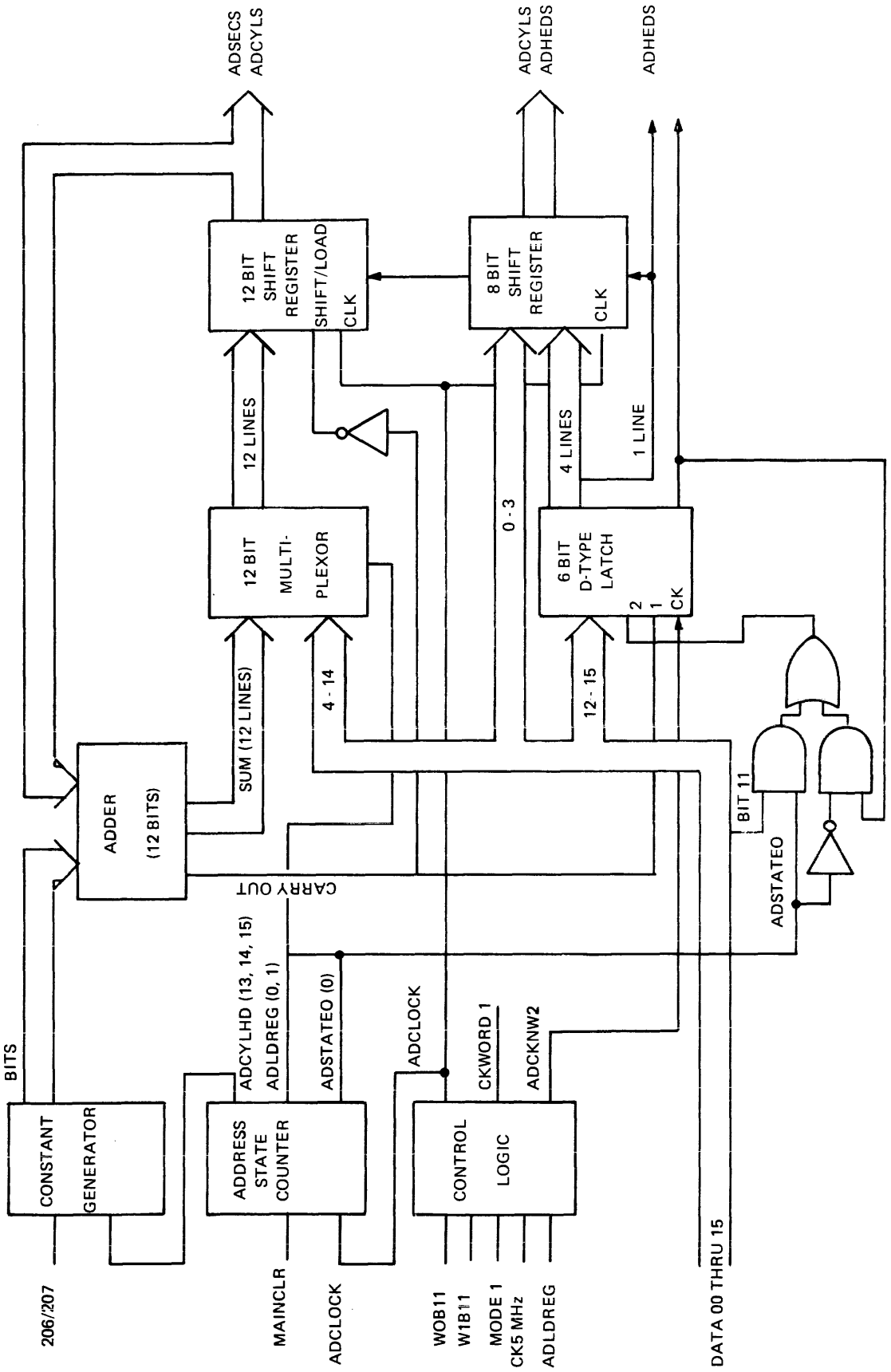


Figure 3-3. Address Decode Block Diagram

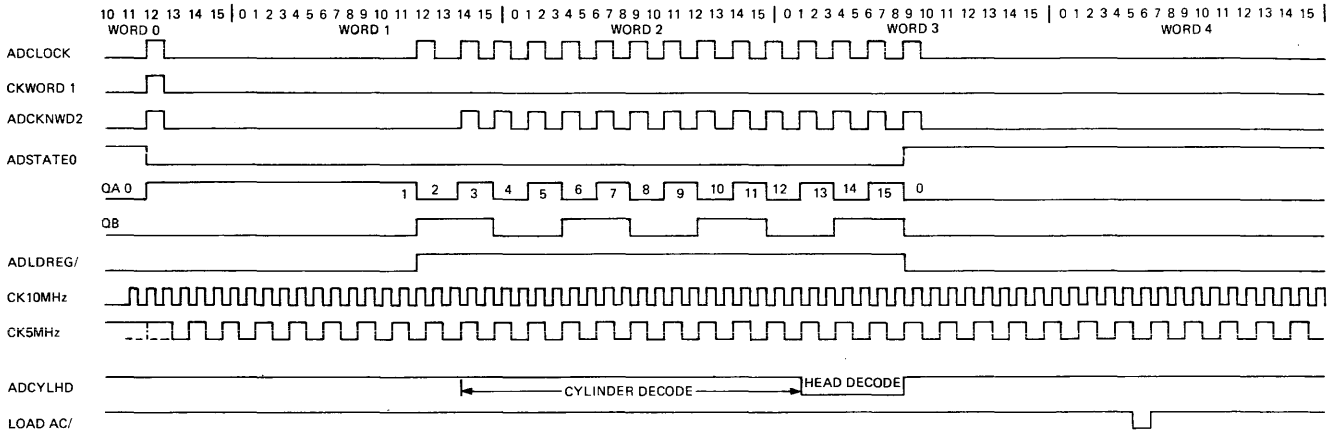


Figure 3-4. Address Decode Control Logic

The last bit of the address is at the shift input of the register. This completes the loading of the binary address. ADCLOCK counts the address state counter to 2 which causes ADLDREG/ to go high. This causes the sum output of the adder to go through the multiplexor to the 12-bit register.

Address Computation

When the 12-bit shift register and the 8-bit shift register have been loaded, ADLDREG/ goes high which permits the 5 MHz clock to give ADCLOCK pulses.

In state 2, the output of the 12-bit shift register is inputted to the adder with the cylinder constant. If there is no CARRYOUT, this indicates that the result of the subtraction is minus, and the sum is not valid. The decimal equivalent of this situation is: 094 ÷445,where the divisor is greater than the dividend. If a CARRYOUT does not occur, the sum is ignored, and the 8-bit and 12-bit shift registers are shifted up one position. A zero is shifted into bit 1 of the 6-bit, D-type latch. This zero indicates that division is not possible; therefore, the most-significant bit of the cylinder address is zero.

If a CARRYOUT occurs, this indicates that the divisor is less than the dividend. The sum is valid and is loaded into the 12-bit shift register. The sum is loaded back shifted one position. On the same clock, the 8-bit shift register is shifted one position, bringing the next bit of binary address into the 12-bit shift register. The CARRYOUT causes a one to be loaded into the 1 bit of the 6-bit, D-type latch. This indicates that division is possible; therefore, the most-significant bit of the cylinder address is one.

The shifted address is now being added to the constant. If CARRYOUT is true, the sum is shifted, and a one is shifted in on the next ADCLOCK. If there is no CARRYOUT, the previous address information is shifted, and a zero is fed in.

This process is performed 11 times to determine the cylinder address. In state 13, the constant is changed for the head decode. The address is complete at state 0. Table 3-4 shows the state of the register and adder in each state.

When address state 0 is reached from 15, ADLDREG/ goes low, preventing further ADCLOCKS.

At W4B5, LOAD AC loads the register output into the address counters.

Address Counter

At W4B5, the decoded address is loaded into the address counter. The address is used as the source of address information for seeks, head changes, header generation, etc. On multiple sector operations, it is counted up to provide the next address. The signal ENADRCNT (enable address count) causes the counter to address the next sector. (See figure 3-5).

When the sector counter reaches a count of 89 (or 84 with the spare head selected), ENDOFTRK is generated. ENDOFTRK causes the sector counter to be cleared (SECNTCLR/) and the head counter to be counted (HDCNTEN). The address counter is then addressing sector 00 of the next head.

In local, if LOOPSEC (loop sector) is on, the sector counter is disabled from counting. Also, ENDOFTRK decode is prohibited if the sector being looped is 89 (or 84 and the spares head). This prevents the head counter from counting.

If the head counter is at head 4 and the unit selected is a 206 (or at head 7 on a 207), and ENDOFTRK is decoded, the counter is addressing the last sector of a cylinder. PTENDCYL is decoded (part of end of cylinder). This signal enables the cylinder counter to count up to the next cylinder. It also clears the head counter. The address counter now contains sector 00, head 0 on the next cylinder.

BIT POSITION	CARRY	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	-1	-2	STATE
																								0
																								0
																								0
																		0	0	1	1	0		1
																								1
																								1
A INPUT		0	0	1	0	0	0	1	1	1	1	1	0	1	1	1	0	0	0	1	1	0	X	2
B INPUT		1	1	0	0	1	0	0	0	0	1	1	0											2
SUM	0	1	1	1	0	1	1	0	0	0	1	0	0											2
		0	1	0	0	0	1	1	1	1	1	0	1	1	1	0	0	0	1	1	0	X	0	3
		1	1	0	0	1	0	0	0	0	1	1	0											3
	1	0	0	0	1	0	0	0	0	0	0	1	1											3
		0	0	1	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	0	X	0	1	4
		1	1	0	0	1	0	0	0	0	1	1	0											4
	0	1	1	1	0	1	0	0	0	1	1	0	1											4
		0	1	0	0	0	0	0	0	1	1	1	1	0	0	0	1	1	0	X	0	1	0	5
		1	1	0	0	1	0	0	0	0	1	1	0											5
	1	0	0	0	0	1	0	0	1	0	1	0	1											5
		0	0	0	1	0	0	1	0	1	0	1	0	0	0	1	1	0	X	0	1	0	1	6
		1	1	0	0	1	0	0	0	0	1	1	0											6
	0	1	1	0	1	1	0	1	1	0	0	1	0											6
		0	0	1	0	0	1	0	1	0	1	0	0	0	1	1	0	X	0	1	0	1	0	7
		1	1	0	0	1	0	0	0	0	1	1	0											7
	0	1	1	1	0	1	1	0	1	1	0	1	0											7
		0	1	0	0	1	0	1	0	1	0	0	0	1	1	0	X	0	1	0	1	0	0	8
		1	1	0	0	1	0	0	0	0	1	1	0											8
	1	0	0	0	1	0	0	1	0	1	1	1	0											8
		0	0	1	0	0	1	0	1	1	1	0	1	1	0	X	0	1	0	1	0	0	1	9
		1	1	0	0	1	0	0	0	0	1	1	0											9
	0	1	1	1	0	1	1	1	0	0	0	1	1											9
		0	1	0	0	1	0	1	1	1	0	1	1	0	X	0	1	0	1	0	0	1	0	10
		1	1	0	0	1	0	0	0	0	1	1	0											10
	1	0	0	0	1	0	1	0	0	0	0	0	1											10
		0	0	1	0	1	0	0	0	0	0	1	0	X	0	1	0	1	0	0	1	0	1	11
		1	1	0	0	1	0	0	0	0	1	1	0											11
	0	1	1	1	1	0	0	0	0	1	0	0	0											11
		0	1	0	1	0	0	0	0	0	1	0	X	0	1	0	1	0	0	1	0	1	0	12
		1	1	0	0	1	0	0	0	0	1	1	0											12
	1	0	0	0	1	1	0	0	0	1	0	1	0											12
		0	0	1	1	0	0	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	1	13
		1	0	1	0	0	1	1	0	0	0	0	0											13
	0	1	1	0	1	0	1	1	1	0	1	0	0											13
		0	1	1	0	0	0	1	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	14
		1	0	1	0	0	1	1	0	0	0	0	0											14
	1	0	0	0	0	1	0	0	0	1	0	0	1											14
		0	0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	1	15
		1	0	1	0	0	1	1	0	0	0	0	0											15
	0	1	0	1	1	0	1	1	1	0	0	1	0											15
		0	0	1	0	0	0	1	0	0	1	0	1	0	0	1	0	1	0	1	0	1	0	0
		SECTOR								CYLINDER											HEAD			

Table 3-4. Address Decode

In local, if the loop head switch is up, LOOPHEAD prevents the head counter from counting and prevents PTENCYL. This prevents the cylinder counter from counting at the end of the track if the head being looped is 4 (206) or 7 (207).

ENDOFPAK is decoded by ENDOFTRK, PTENDCYL, and the maximum cylinder address. On a 206, this is cylinder 814. On a 207, it is cylinder 1563.

OLD = NEW

When an address is sent to the DDEC, the DDEC must make a decision on whether to send a seek to the drive. In order to make this decision, it must know the cylinder address of the previous seek command sent to that drive.

The DDEC contains a 12-bit memory for each drive. Whenever a seek is performed or at the end of an operation, the cylinder address from the address counter is written into the memory.

When a new address has been decoded, the new cylinder address is compared to the old cylinder address read from the memory. If they agree, OLD = NEW/ is low, indicating that a seek is not required. If they do not agree, OLD = NEW/ is high, indicating that a seek is required.

Initial Clearing

See schematic 02.04 and figure 3-6 for the following discussion.

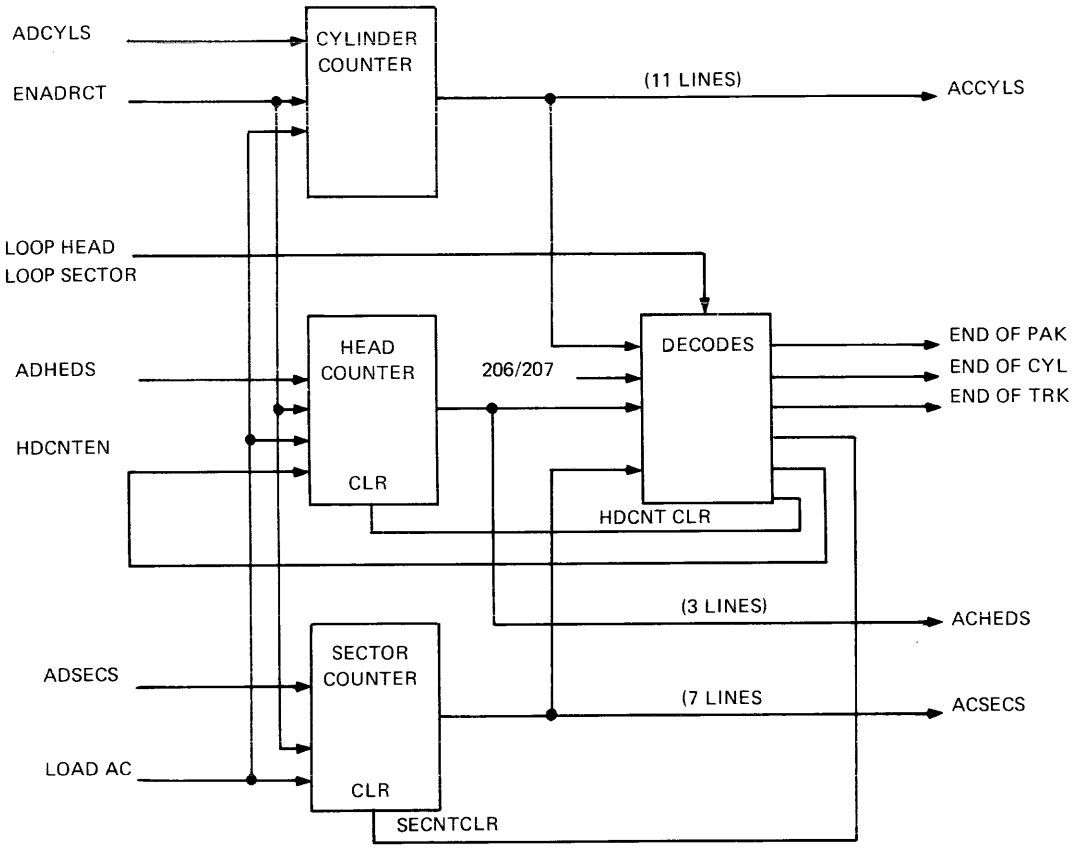


Figure 3-5. Address Counter

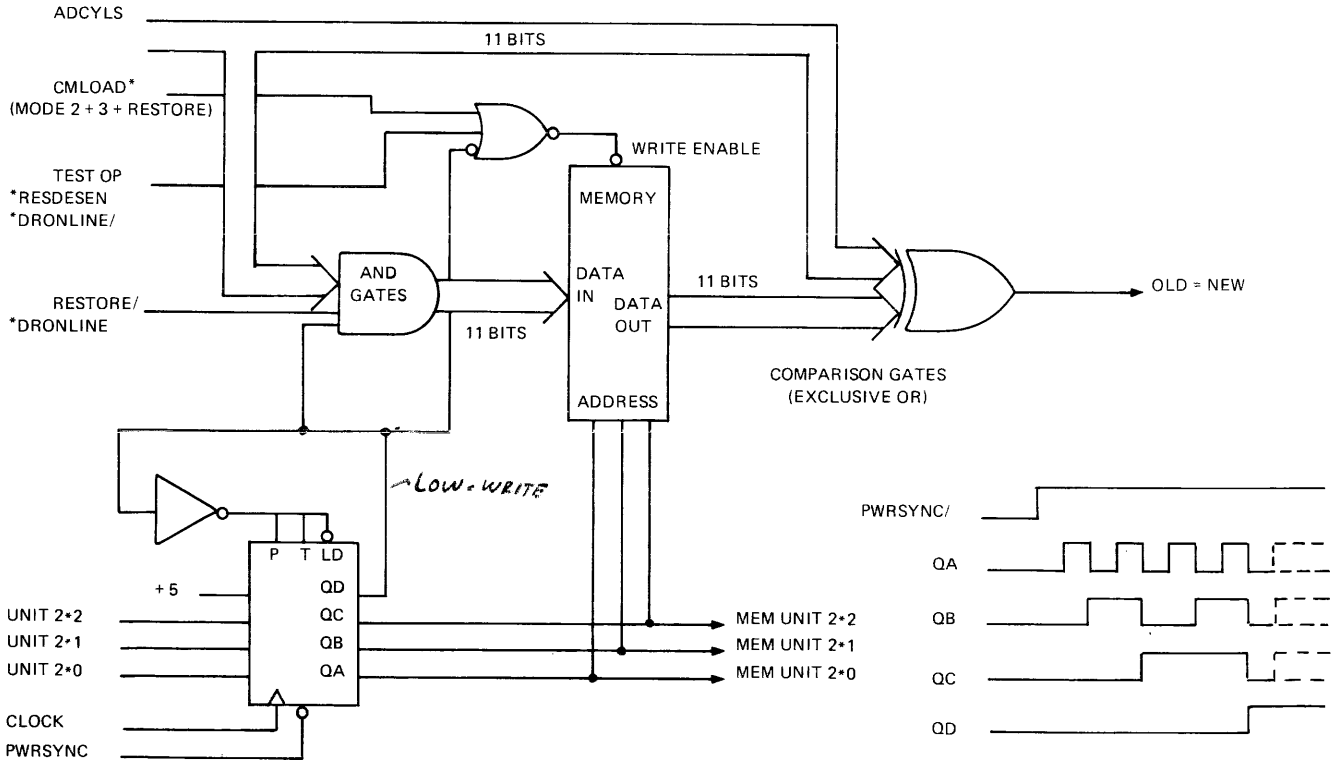


Figure 3-6. OLD = NEW

When the DDEC is powered up, PWRSYNC/ holds the outputs of the unit counter all low. QD being low enables the memory to write and holds the data input to the memory low. This clears the memory for unit 00. QD, through an inverter, enables the counter to count when PWRSYNC/ goes high.

When PWRSYNC/ goes high, the counter counts up until QD sets. In the process, each memory is addressed and is cleared out to zeros. With the load input low, the counter follows any change in the unit signals.

Memory Write

The memory is written with cylinder information during mode 2 or mode 3. If the signal CMLOAD is true in mode 2 or 3, a seek CM is being sent to the drive. At this time, write enable low at the memory writes the cylinder into the memory for the unit selected.

If a restore is required, the data input to the memory is zeros. When CMLOAD goes true, zeros are written into memory. (Restore causes a rezero CM to be sent to the drive. The drive rezeros onto cylinder 0000).

During a Test OP, if the drive is found to be offline, zeros are written into memory.

Comparison

When the memory is not writing, it is in a read mode, displaying the output of the memory addressed by the unit counter. This output is continuously compared with the address counter cylinder output. Comparison is achieved using exclusive OR gates. OLD = NEW is only used in mode 1 W14B2.

HEADER GENERATION AND EPC

General Description

The function of this section of logic is:

1) To generate a 32-bit header consisting of address and EPC information.
2) To shift the header out serially for writing on the disk during INITIALIZE and RELOCATE.
3) To shift the header out serially for address comparison during READ, WRITE, VERIFY, RELOCATE and READ MAINTENANCE.

Header Generation

See figures 3-7 and 3-8 for the following discussion.

The address information used in the header comes primarily from the address counter. However, head and sector information may come from different sources.

In mode 11, the head multiplexor selects the spares head. This is in preparation for a cylinder and head check on the spare tracks.

During INITIALIZE, because the sectors are in interleaved format, the sector information is derived from the interleave logic.

During a spare sector verify, the sector information is derived from the N. variants plus 84.

A new header is generated under four conditions:

1) When a new address has been decoded and is about to be loaded into the address counter.
2) Whenever the address counter is counted (ENADRCT/). This occurs during multiple sector READS, WRITES, and VERIFIES.
3) During RELOCATE on the first pass when a head CM is sent in mode 11 to select the head containing the spares. The new header is required for the cylinder and head check in mode 9 (CM2-0M11).
4) During RELOCATE on the second pass when the spare sector is about to be initialized (GTMD8FRIO).

When any of these conditions occur, EPCCLR/ goes low for one clock period. This pulse clears the EPC register and loads the new address into the shift register. S0 and S1 control both go high. The control logic counter is allowed to count 24 times. When the counter is at 23, S0 and S1 go low on the next clock, and the counter is reset.

CKIHBT goes low for 24 clock pulses. This allows the 24-bit shift register to shift 24 times. S1CTRL gates the serial output back to the input; therefore, after 24 clocks, the information in the shift register is identical to when it was loaded.

However, the address bits are presented, a bit at a time, to the EPC register.

With S0 and S1 high, the EPC register is in load mode. The output of A goes through an exclusive OR gate and is loaded into B. B goes into C, and so on. At each clock pulse, every flip-flop in the register is loaded either from an exclusive OR gate or from the previous stage. As each bit is presented from the shift register a pattern is built up in the EPC register. Table 3-5 shows an example of the EPC register bits during the EPC generation for cylinder 0, head 1, sector 0.

The header generation is complete after 24 clock pulses. The address is in the shift register and the EPC is in the EPC register.

Write Address

See figure 3-9 for the following discussion.

The signal WR32HDR causes CKIHBT to go low. This enables the shift register to shift. S0CTRL high and S1CTRL low also permits the EPC register to shift on each clock. S1CTRL/ allows the serial output of the EPC register to feed into the 24-bit shift register.

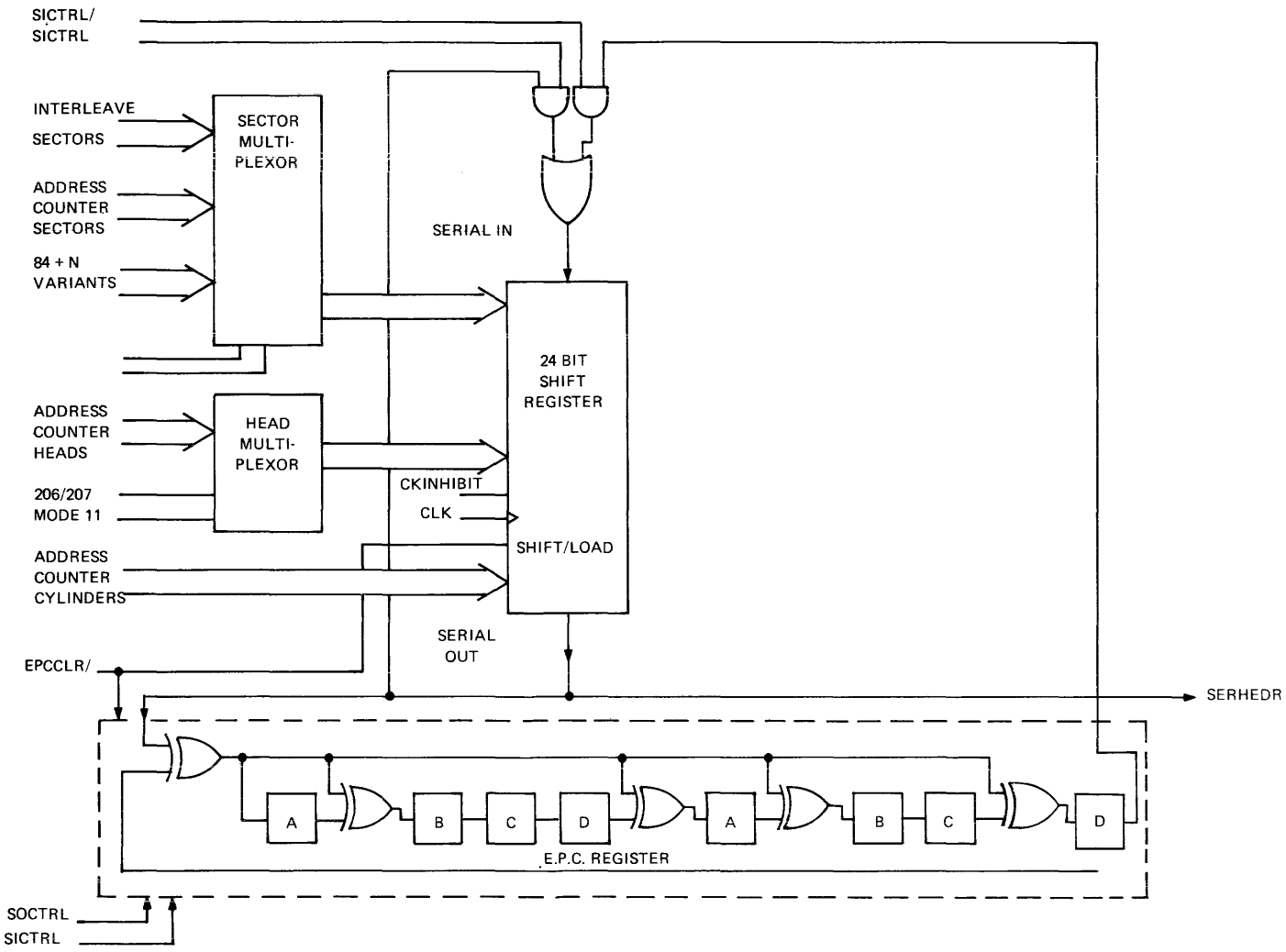


Figure 3-7. Header Generator

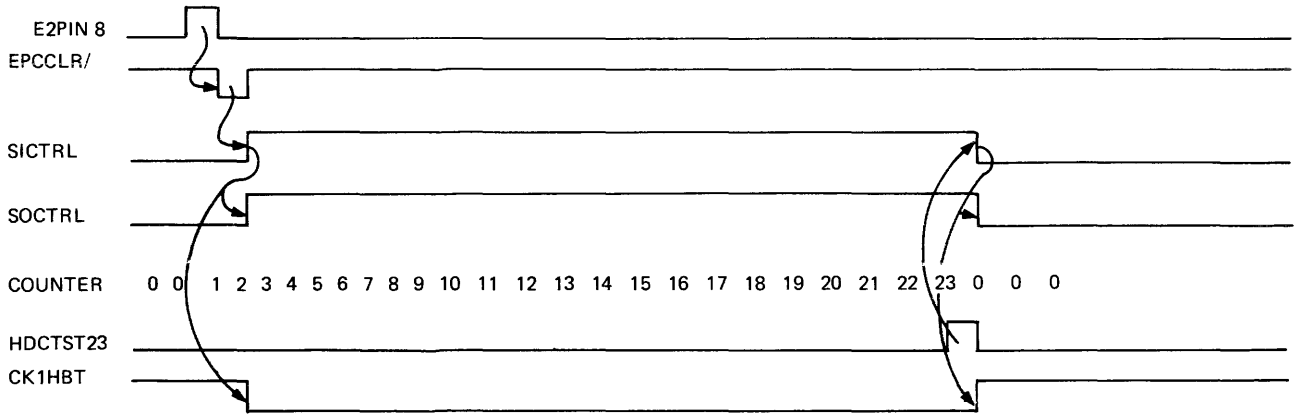


Figure 3-8. Header Generation Control Logic

SECTOR 0, CYLINDER 0, HEAD 1

SHIFT REG. OUTPUT	COUNTER	A	B	C	D	A	B	C	D
0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0
0	2	0	0	0	0	0	0	0	0
0	3	0	0	0	0	0	0	0	0
0	4	0	0	0	0	0	0	0	0
0	5	0	0	0	0	0	0	0	0
0	6	0	0	0	0	0	0	0	0
0	7	0	0	0	0	0	0	0	0
0	8	0	0	0	0	0	0	0	0
0	9	0	0	0	0	0	0	0	0
0	10	0	0	0	0	0	0	0	0
0	11	0	0	0	0	0	0	0	0
0	12	0	0	0	0	0	0	0	0
0	13	0	0	0	0	0	0	0	0
0	14	0	0	0	0	0	0	0	0
1	15	0	0	0	0	0	0	0	0
0	16	1	1	0	0	1	1	0	1
0	17	1	0	1	0	1	0	1	1
0	18	1	0	0	1	1	0	0	0
0	19	0	1	0	0	1	1	0	0
0	20	0	0	1	0	0	1	1	0
0	21	0	0	0	1	0	0	1	1
0	22	1	1	0	0	0	1	0	0
0	23	0	1	1	0	0	0	1	0
0	0	0	0	1	1	0	0	0	1

EPC = 8C

HEADER = 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 1 0 0 0 1 1 0 0

CYLINDER HEAD SECTOR E.P.C.

Table 3-5. EPC Generation

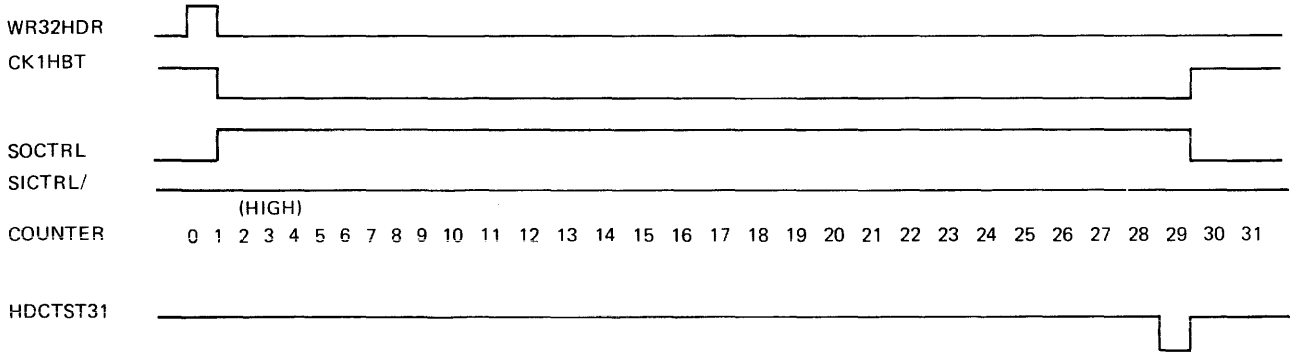


Figure 3-9. Header Control Write Header

CKIHBT is low for 32 clocks; therefore, the 24-bit address in the shift register and the EPC are fed out serially on SERHEDR (serial header). SERHEDR is fed to the drive via the main serial multiplexor for writing on the pack. The information in the shift register and EPC register is recycled through the EPC register and then is recycled back into the shift register as the header is shifted out. At the end of 32 clocks, the address and EPC is back in its original position.

Address Comparison

The header previously generated is shifted out bit by bit to be compared with the address information arriving from the drive. This occurs during an address search (mode 5) and during cylinder head verification (mode 9). The result of an equal comparison in mode 5 is ADDREQL. The result of an equal comparison in mode 9 is CYLHDEQL.

When the sync character in the address field is de-

tected, the signal STADRCMP occurs (start address compare). (See figures 3-10 and 3-11).

When STADRCMP occurs, CKIHBT goes low for 32 clocks. This allows the 24-bit shift register to be shifted out on to the SERHEDR line bit by bit. At the same time, S0CTRL high and S1CTRL low allows the EPC register to shift. S1CTRL/ being high, allows the output of the EPC register to be shifted into the 24-bit shift register. Therefore, after 32 clocks, the complete header consisting of the 24-bit address and 8-bit EPC has been shifted out on to SERHEDR (Serial header).

The signal ADCMPEN (address compare enable) is high during the compare. (See figure 3-11). The data coming from the drive is synchronized with the clock and compared through an exclusive OR gate with the serial header. If the inputs to the gate differ, HEDRERR goes high.

At the start of the address comparison, ADDEQL and CYLHDEQL flip-flops are preset. If HEDRERR goes high during ADCMPEN, the ADDEQL flip-flop is reset. If HEDRERR stays low throughout ADCMPEN, the ADDEQL flip-flop remains set indicating that an address comparison has been made.

If HEDRERR goes high during the first 16 bits of the comparison (CYLERREN), the CYLHDEQL flip-flop is reset. If HEDRERR stays low during CYLERREN, CYLHDEQL flip-flop remains set, indicating that the cylinder and head address compares.

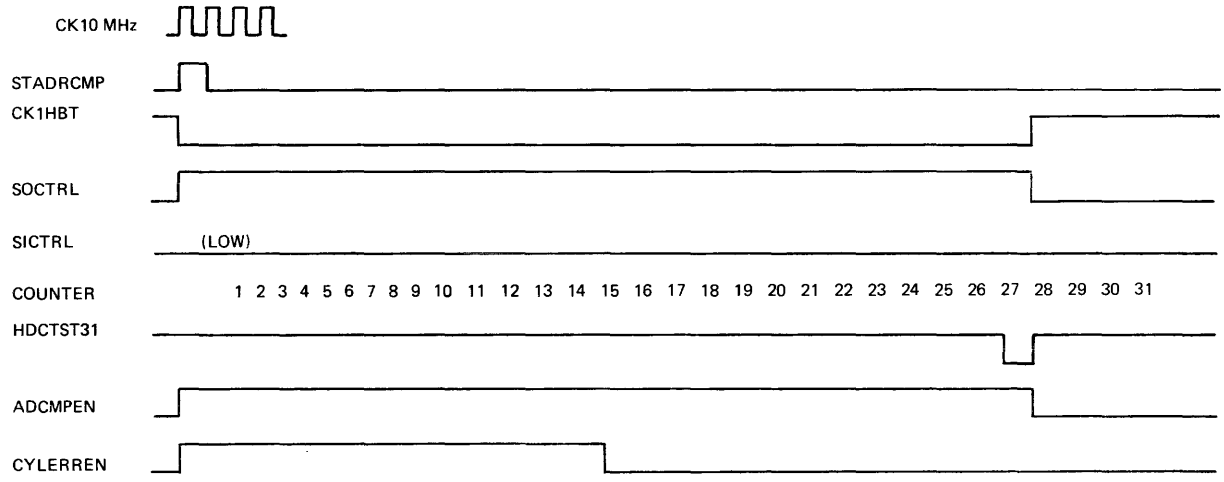


Figure 3-10. Header Control Address Compare

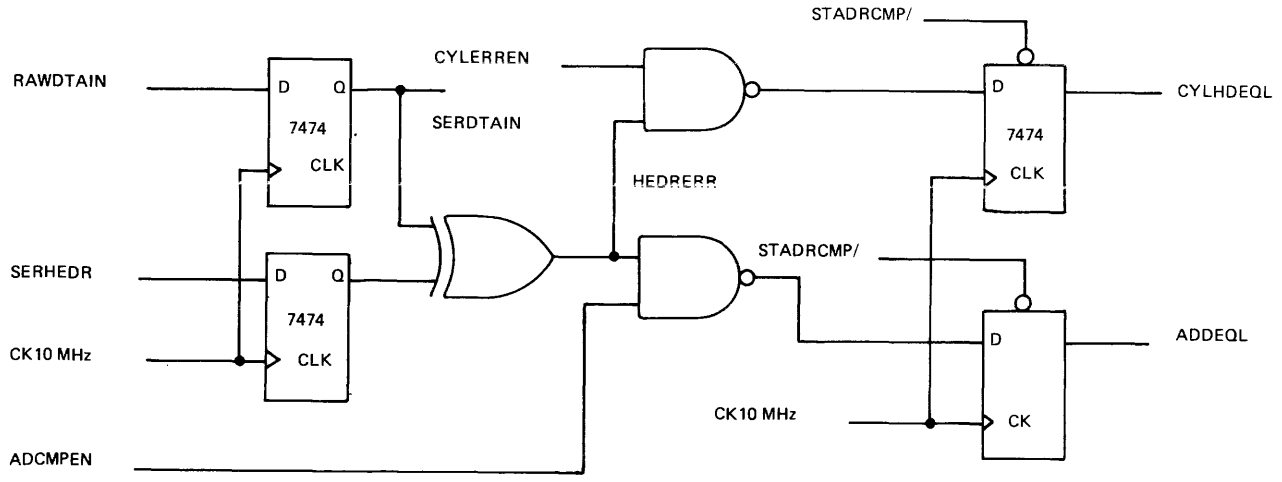


Figure 3-11. Simplified Schematic, Address Comparison

SECTION 4

DATA RELATED CIRCUITS

DATA FROM THE DRIVE

See figure 4-1 for the following discussion.

Data arrives from eight possible drives. Differential input receivers are gated with unit select signals in order to prevent high frequency oscillations from receivers with floating inputs. The receiver outputs DRNDTA go to an 8 to 1 multiplexor, where the unit inputs ensure that data from the selected unit becomes RAWDTAIN.

RAWDTAIN is synchronized with the clock in the DDEC to become SERDTAIN (Serial data in) SERDTAIN goes to the following places:

1) Stuck data detector - detects if the data line is continuously high or continuously low.
2) Sync character detector - when enabled, the sync character detector detects four ones at the start of address or data.
3) Firecode Comparison - during a READ, the firecode READ is compared to the firecode generated (206).
4) Address comparison - during an address search, the address read from the disk is compared to the address required.

SERDTAIN is delayed by one gate time to become SRDTDLYD (Serial data delayed). SRDTDLYD goes to the 206 and 207 firecode generation logic during a READ. SRDTDLYD also goes to the parallel serial parallel register for stack up into words.

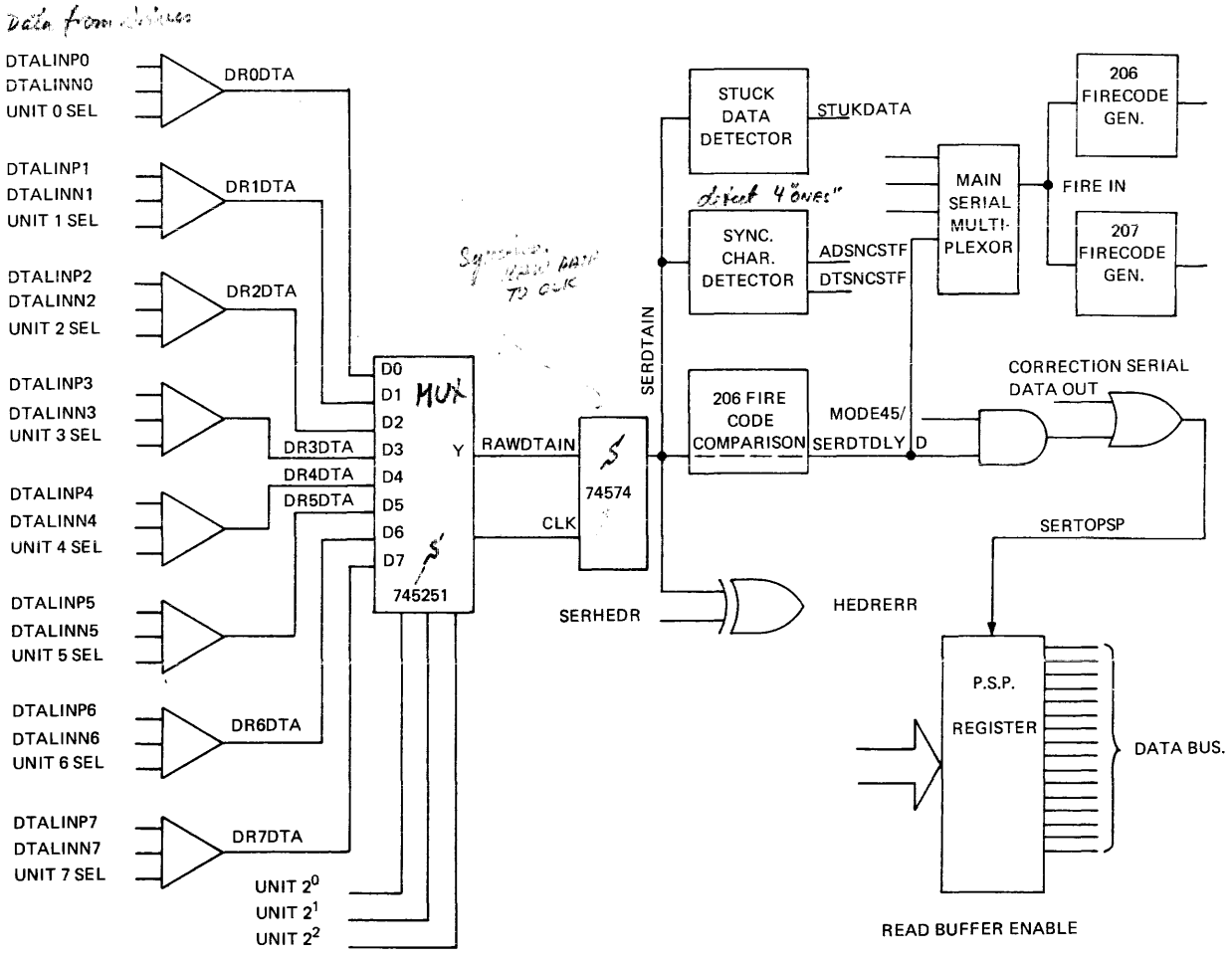
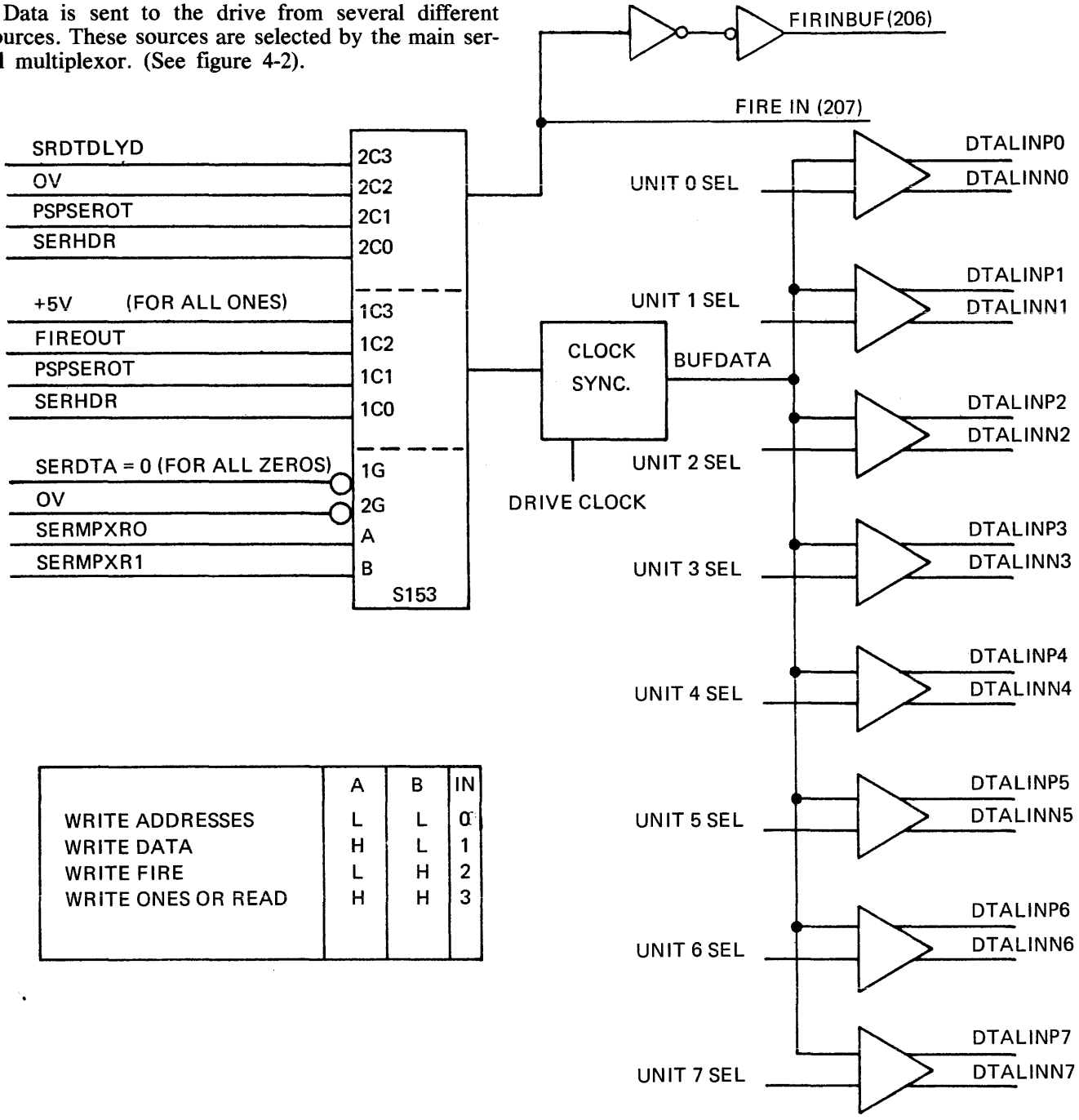


Figure 4-1. Data Input During READ

DATA TO THE DRIVE

Data is sent to the drive from several different sources. These sources are selected by the main serial multiplexor. (See figure 4-2).



	A	B	IN
WRITE ADDRESSES	L	L	0
WRITE DATA	H	L	1
WRITE FIRE	L	H	2
WRITE ONES OR READ	H	H	3

Figure 4-2. Main Serial Multiplexor

The Multiplexor supplies data to the firecode generation logic. This is shown as the 2 inputs to the multiplexor 1G. These do not concern this discussion. (Refer to the 1 gates).

The inputs are enabled when the 1G input goes low. When the 1G input is not low, the inputs are disabled and the output is low. This is used to write zeros. Whenever SERDTA = 0, a low is fed to BUFDATA (zeros). SERDTA = 0 is high whenever the flow gives FMWRZEROS. This occurs at several places in the flows. (For example during WRITE when the data preamble is to be written).

When SERDTA = 0 is low, the input selected depends on SERMPXR0 and SERMPXR1. The binary value of these two signals select the 0, 1, 2 or 3 input.

When the 1C0 input is selected, serial header information is fed through the IC to BUFDATA where it is sent to the unit selected. This occurs when the address is written during INITIALIZE or RELOCATE (second pass) or when processor data is not specified for the data field during INITIALIZE or RELOCATE.

The 1C1 input is selected during write data. The parallel/serial/parallel register serial output is fed to the selected drive. The PSP. register converts parallel words of information into bit serial.

The 1C2 input is used when the firecode is to be written onto the disk during WRITE or INITIALIZE or RELOCATE.

The 1C3 input is used when ones are to be written on to the disk. This occurs whenever sync characters are written, or during the first pass of RELOCATE, when the address field of the bad sector is overwritten with ones.

The multiplexor output is synchronized with the clock from the drive so that the data is correctly synchronized when it reaches the drive.

DATA BUS

Figure 4-3 shows a block diagram of the data bus. The data bus enables 16 bits of information to be transported to six places from eight origins using common lines. All the inputs to the bus are tri-state. The drivers are normally in a high impedance state. A control signal takes one of the drivers into low impedance state and allows the line to be driven high or low, depending on the input logic.

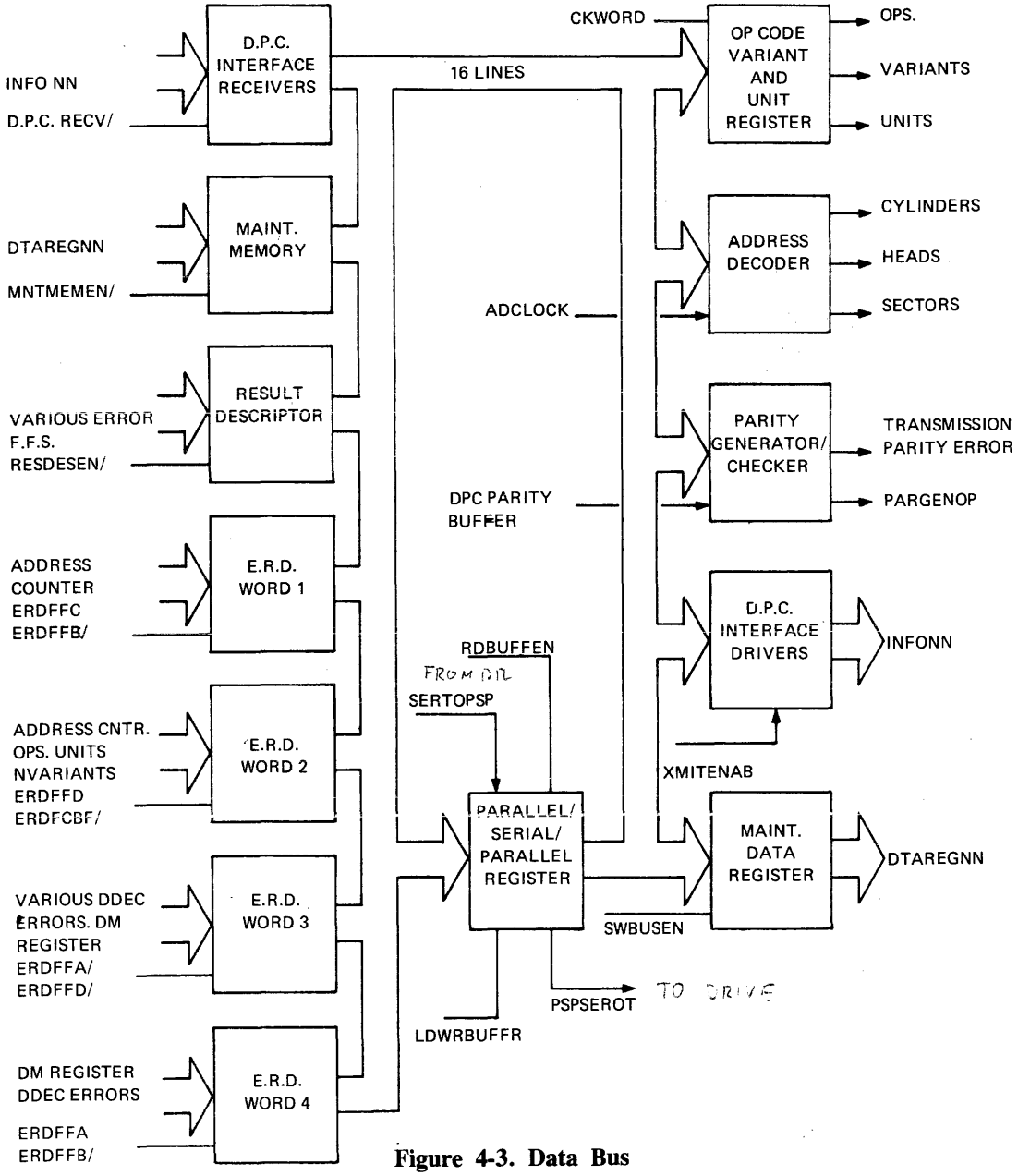


Figure 4-3. Data Bus

The outputs of the data bus are clocked into various registers when a control signal occurs. When XMITENAB is true, the data bus is placed onto the information lines to the DPC. Data is transferred to the DPC in this manner.

During the initial OP processing, data containing the OP, variants, addresses and units is placed on the data bus from the DPC interface receivers, (or, in local, from the maintenance memory). This data is clocked into the OP, variant, and unit register, and also into the address decoder.

During WRITE, data is received from the DPC Interface receivers. This data is loaded into the PSP. register by LDWRBUFFR (load write buffer). The data word is then shifted out to the drive serially.

During READ, serial data from the drive is fed into the serial input of the PSP. register and loaded into the read buffer at the completion of each word. RDBUFFEN (read buffer enable) places this information on to the data bus. The signal XMITENAB allows the information on the data bus to go to the DPC via the INFORMATION lines.

During the result status phase, RESDESEN places the result descriptor on the data bus. XMITENAB sends it to the DPC.

During send ERD, the four data words are placed, one at a time, on the data bus. XMITENAB sends them to the DPC. The maintenance data register permits result descriptors to be displayed while the operations are in progress.

The parity generator/checker is used to check parity when data is being received, and generates parity when data is being sent to the DPC. This circuit is used in conjunction with the signal DPCPARBF (DPC parity buffered). If a parity error is detected on the 16 information lines, the signal XMTNPERR (transmission parity error) occurs. If this occurs in mode 1, the flow goes to mode 15. If it occurs any other time, the result descriptor shows this bit at the end of the operation.

FORMAT CONTROL LOGIC

General Description

The format control logic controls the flow of data throughout the DDEC there are nine basic format functions that may be initiated during the flows:

FMRDDATA - read data.
FMRDFIRE - read firecode.
FMSNDRD - send result descriptor.
FMWRZEROS - write Zeros.
FMWRFIRE - write firecode.
FMWRDATA - write data.
FMWRONES - write ones.
FMWRADDRESS - write address.
FMGOIDLE - go idle.

Idle indicates that none of the other eight format functions are in effect.

The format control counter is a 16-bit counter counting at clock speed (one cycle through every word). This counter gives 16 timing pulses each word.

The combination of the format signals and the format control counter gives many signals that control the data.

Examples:

1) CKDPC (clock DPC) is derived from format counter 12 through 14 and FMWRITE DATA.
2) FIRE ENCEN (firecode encode enable) is derived from FMRDDATA or FMWRDATA.
3) LDRDBFFR/ (load read buffer) is given from FMRDDATA and FMCNTF (format counter full).

A block diagram of the format control logic is given is figure 4-4.

Block Diagram

Format Control Input

This block consists of gating to provide the nine basic FM signals. The inputs consist of word bit times, modes, and other conditions. The logic may be seen on the schematic pages. The equation for each FM signal is also listed in the T & F document. The result of this box is a pulse, usually 100 nanoseconds long on one of the FM signals, when the flow (control logic) requires a change in format.

Format Control Register

Since the FM signals consist of a pulse only, the signals must be stored in a register. The register is reloaded any time an FM signal occurs. Figure 4-5 shows the format signals seen during INITIALIZE of one sector.

Format Control Counter

The format control counter is a 16-bit counter cycling every word. It is resynchronized every time an FM signal occurs. On all FM signals, except FMWRONES, the counter is cleared. When FMWRONES is true, the counter is preloaded to 12. This has the effect of providing an immediate RAWCLKDPC. RAWCLKDPC goes high at a count of 12 and low on a count of 15. The early RAWCLKDPC is used to clock one word of information in from the DPC in advance of it being written on the disk.

Format Control Output Generator

This box consists mainly of gating. Many control signals are generated. It also contains two format state machines, one for READ and one for WRITE firecode.

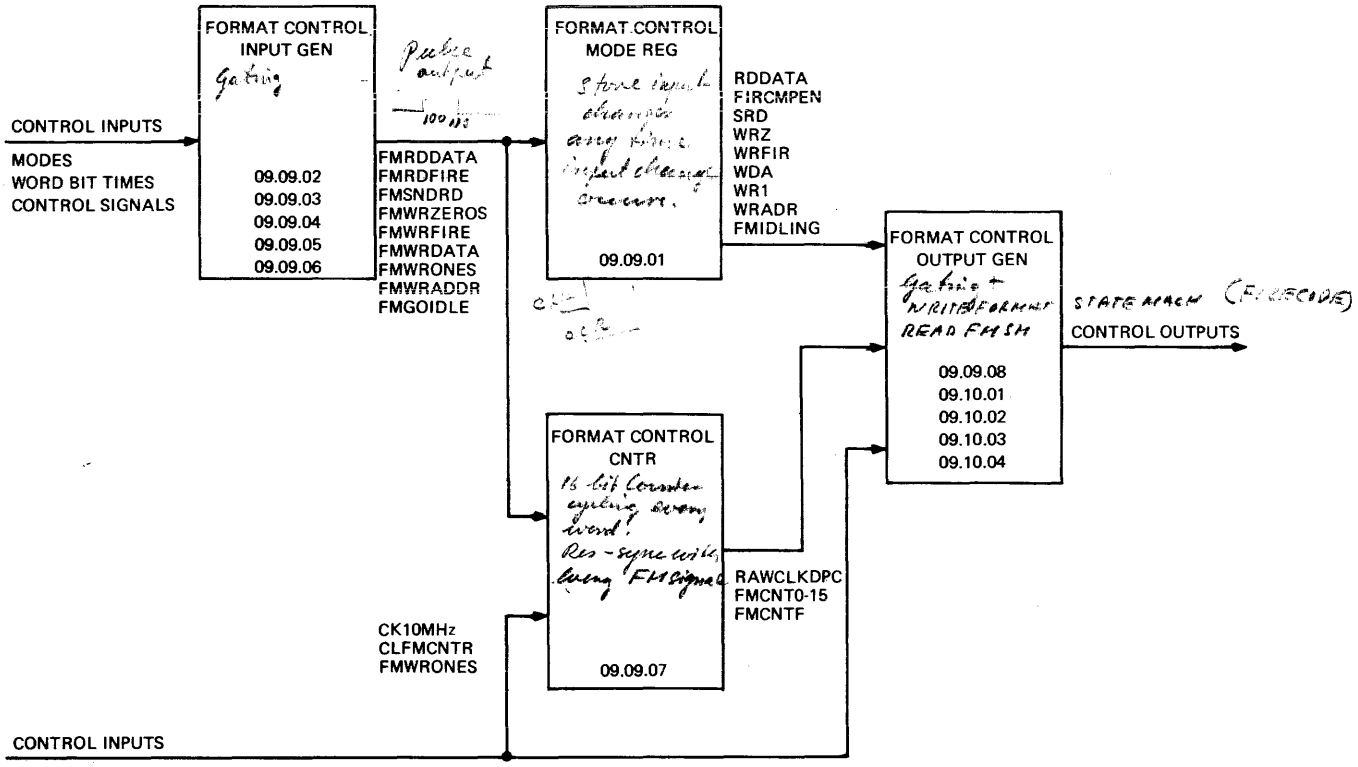


Figure 4-4. Format Control Logic

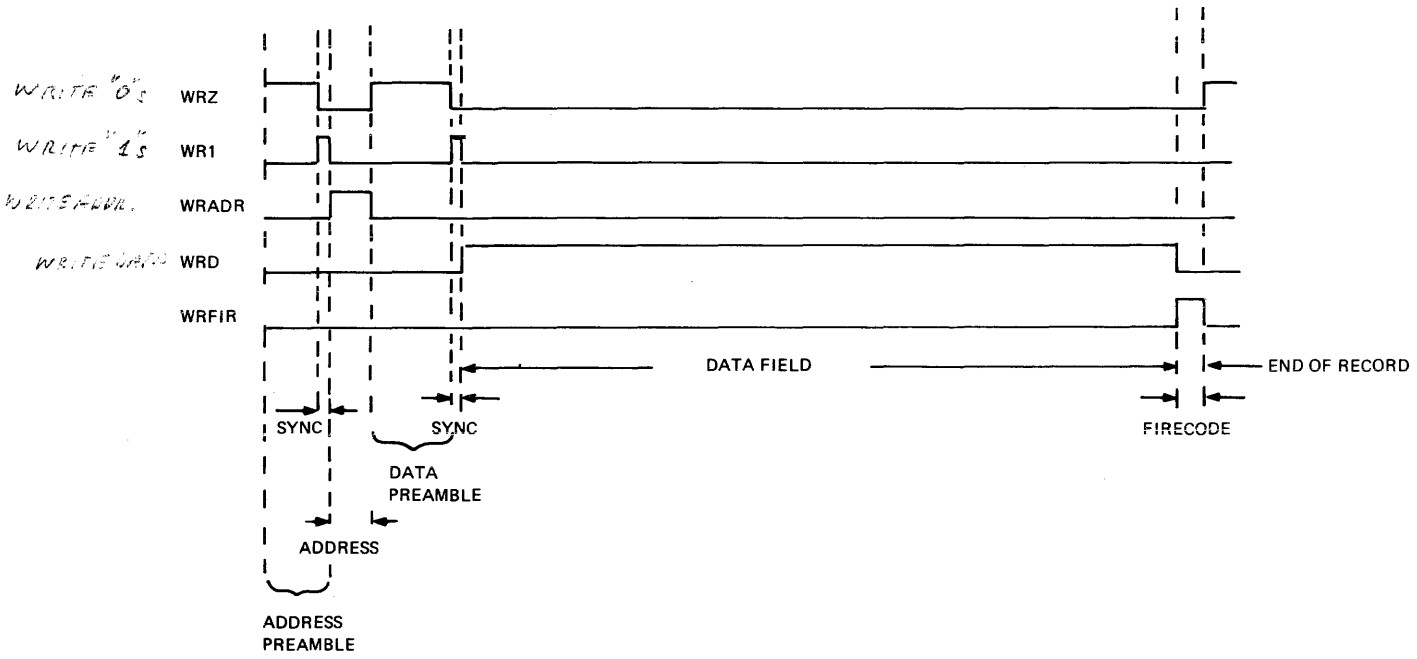


Figure 4-5. Format Signals During Initialize of One Sector

Format State Logic

Format State Logic (Read)

See schematic 09.10.01 for the following discussion.

The format state logic (READ) consists of two flip-flops which may be set or reset to any state. The outputs are decoded into FMST0, FMST1, FMST2, and FMST3.

FMST0 - prevents CKDPC. CKDPC pulses are allowed any time FMST0 is not true (i.e., in any other state).

FMST1 - gives XMENABLE. This enables the line drivers to the DPC RDBUFFEN is true if the OP is not send ERD. This signal enables the read buffer to receive data from the parallel/serial/parallel register.

FMST2 - gives RESDESEN if the operation is not send ERD. If the OP is send ERD, it gives the signal ERDENRD, which gives an all zeros result descriptor after an ERD OP.

FMST3 - gives XMENABLE and RDBUFFEN. The functions performed in state 3 are identical to those performed in state 1.

The format state flip-flops are set according to signals controlling the format. Table 4-1 lists the changes which may occur.

Table 4-1. Format State Counter (Read)

Input Signal	FM Counter	From State	To State
Main Clear, Go to M1 or 15	Any	Any	0
RD Data	15	0	1
SRD	15	0 or 3	2
FIRCMPEN	15	1	3
No input signal	15	2	0
SRD (207 only)	4	3	0

The format counter controls the time at which the flip-flops change state. The new state is set on the next clock pulse. State 2 is active for one word only; the next FMCNTF resets the state to 0. (Only one word time is required to send the result descriptor).

Format State Logic (Write Fire)

See schematic 09.10.02 for the following discussion.

The format state logic (WRITE fire) is active during WRITE firecode. It consists of two flip-flops which may be set or reset to any state. The outputs are decoded into WRFRS0, WRFRS1, WRFRS2, and WRFRS3.

WRFRS0 - permits one CLKDPC pulse during WRITE firecode (This is an interface requirement).

WRFRS1 - causes ALTGOWRZ/ at the end of writing the firecode on a 206. This causes the format to write zeros for the EOR gap. The 206 firecode is two words long.

WRFRS3 - causes ALTGOWRZ/ at the end of writing seven bytes of firecode on a 207. This causes zeros to be written for the EOR gap.

Table 4-2 shows how the states are changed. Timing diagrams (figures 4-9 and 4-10) illustrate the operation of the logic for a 206 and a 207.

Table 4-2. Format State Counter (Write Firecode)

Input Signal	FM Counter	From State	To State
Main CLR	Any	Any	0
WRFIR (Write Firecode)	15	0	1
206	15	1	0
207	15	1	3
No input signal	15	3	2
No input signal	7	2	0

Format Control Functions

FMRDDATA

(90 words)

See figure 4-6 for the following discussion.

FMRDDATA becomes RDDATA after the register. The following functions are performed:

1) FIRENCEN - enables the firecode logic to encode a new firecode from the data being read during READ (206).
2) LDRDBFFR - loads the read buffer from the parallel serial parallel register at the completion of a word (FMCNTF, format counter full).
3) FRRDMD - fire read mode except during error correction mode 4, 5 or 6 (207).
4) STMMWT - start memory write during a 207 READ with correction.
5) SERMPXR0 - serial multiplexor zero with SERMPXR1 permits serial data from the disk into the firecode logic.
6) FRENCD - fire encode permits the 207 firecode logic to encode a new firecode (207 only).
7) XMENABLE - transmit enable is true via the format state logic. This enables the line drivers to the DPC DATA BUS is sent to the DPC.
8) RDBUFFEN - enables the read buffer to output data from the parallel serial parallel register on to the data bus.

FMRDFIRE

(2 WORDS ON 206, 3-1/2 WORDS ON 207)

See figure 4-7 for the following discussion.

FMRDFIRE becomes FIRCMPEN (Fire compare enable) after the format control mode register. The following functions are performed:

1) FIRESHEN - enables the firecode developed during the READ operation to be shifted for a bit by bit comparison with the firecode being read (206).
2) FMST3 FIRCMPEN - takes the format state logic to state 3.
3) FRENCD 207 - fire encode. Permits continued except during portions of error correction.
4) FMRDFIRE - enables the firecode comparison flip-flops.

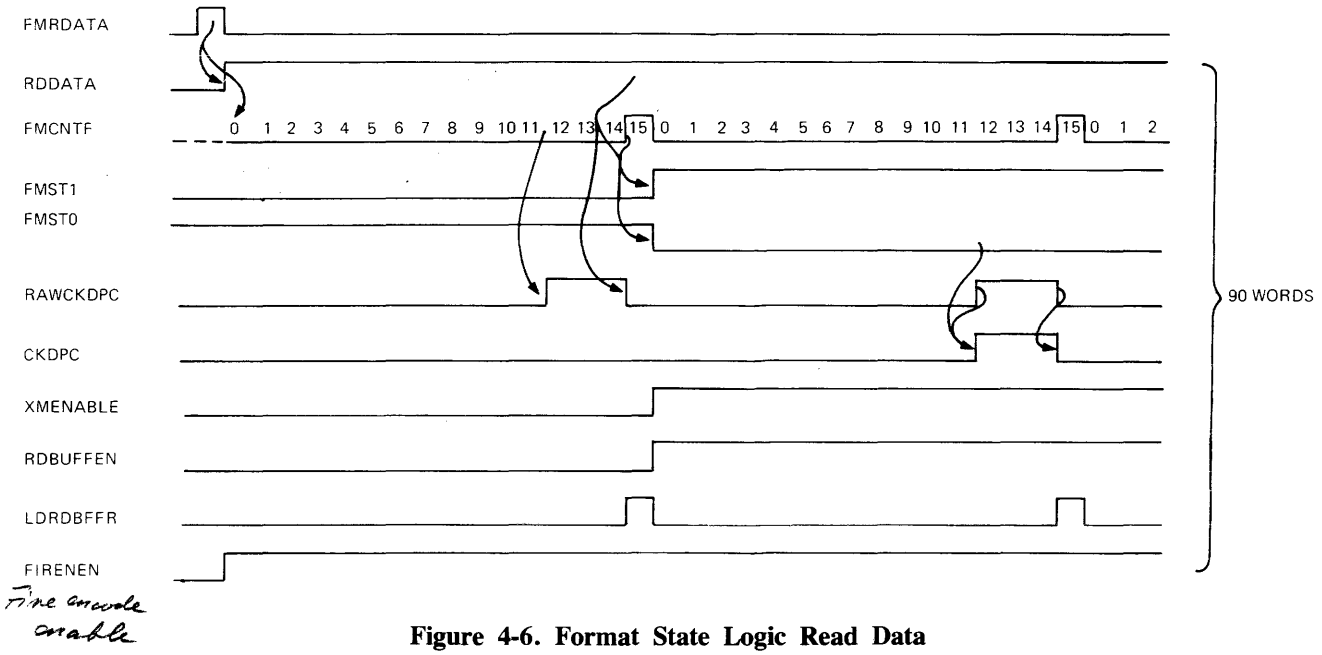


Figure 4-6. Format State Logic Read Data

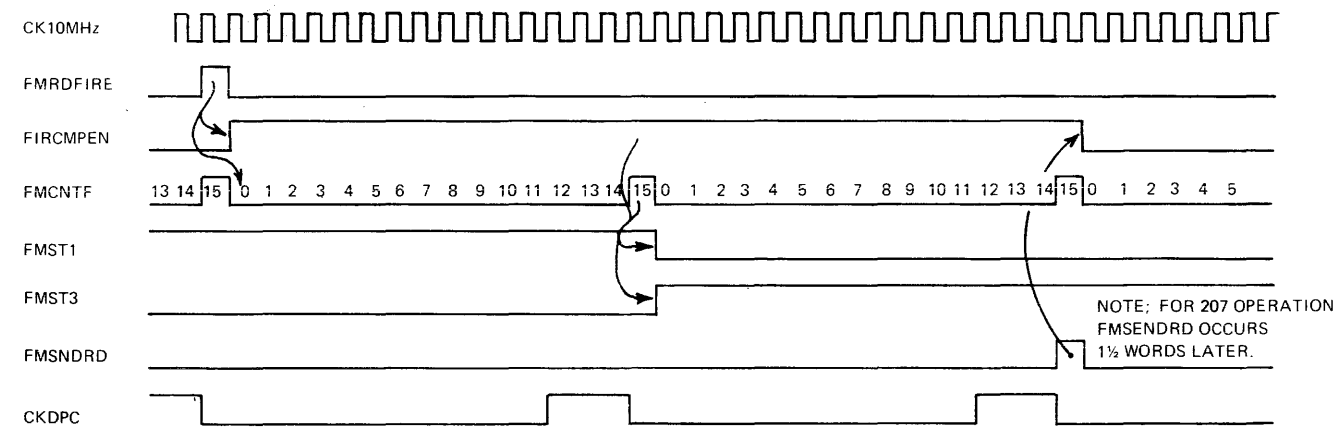


Figure 4-7. Format State Logic READ FIRE

FMSENDRD

See figure 4-8 for the following discussion.

This pulse is set in the format control register and becomes SRD whenever the flow requires a result descriptor to be sent (in mode 6 or mode 15).

SRD causes the read format state logic to go to state 2. This gives RESDESEN (result descriptor enable). RESDESEN places the result descriptor on the data bus, and gives XMITEN which turns on the information line drivers. CKDPC clocks the result descriptor information into the DPC.

SRD automatically generates FMGOIDLE 15 bits after it has gone true. This resets SRD. FMST2 automatically goes low at the completion of the next word.

FMWRZEROS

This signal occurs in various flows whenever zeros are to be written, e.g., when writing the data preamble, or BOT Gap. FMWRZEROS becomes WRZ after the format control mode register.

WRZ performs the following functions:

1) SERDTA = 0 - this causes the data output to the drive to be in the zero state.
2) FMGOIDLE - at the end of the EOR gap (mode 6) the format goes idle.
3) MNTMEMEN - the maintenance memory is enabled in local when WRZ is true during a WRITE OP, INITIALIZE with processor data or RELOCATE with processor data.
4) LDWRBFFR - loads write buffer on a WRITE operation, initialize with processor data or on RELOCATE pass two with processor data. This ensures that the first word of data is in the buffer ready for the write data format mode.

FMWRFIRE

FMWRFIRE occurs at the end of each sector during a write (mode 6), INITIALIZE (mode 8), or RELOCATE (mode 8). FMWRFIRE becomes WRFIR after the format control mode register. WRFIR is high for two words on 206 operation and 3-1/2 words on 207 operation. Refer to figures 4-9 and 4-10. During this time the firecode for the data is written on to the disk. At the end of the firecode, ALTGOWRZ changes the format to Writezeros for the EOR gap.

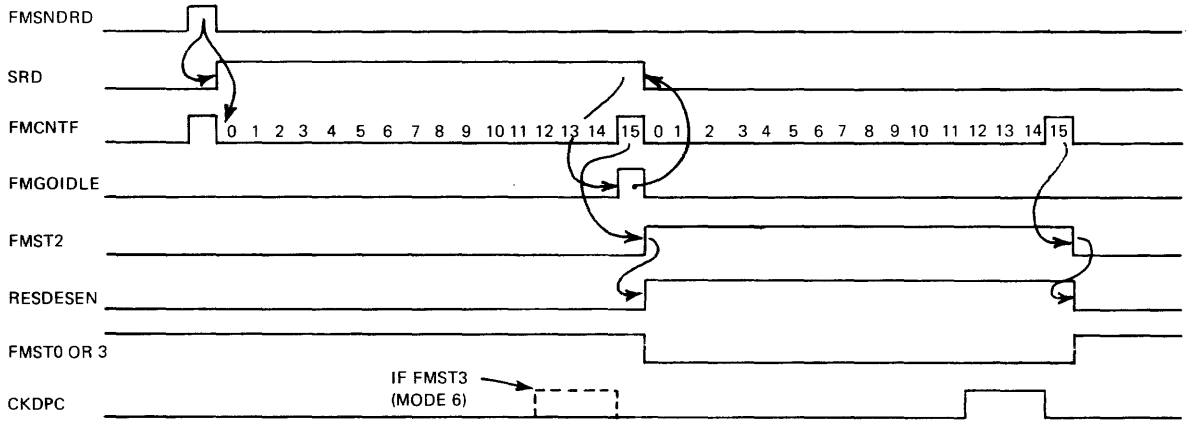


Figure 4-8. Format State Logic FMSNDRD

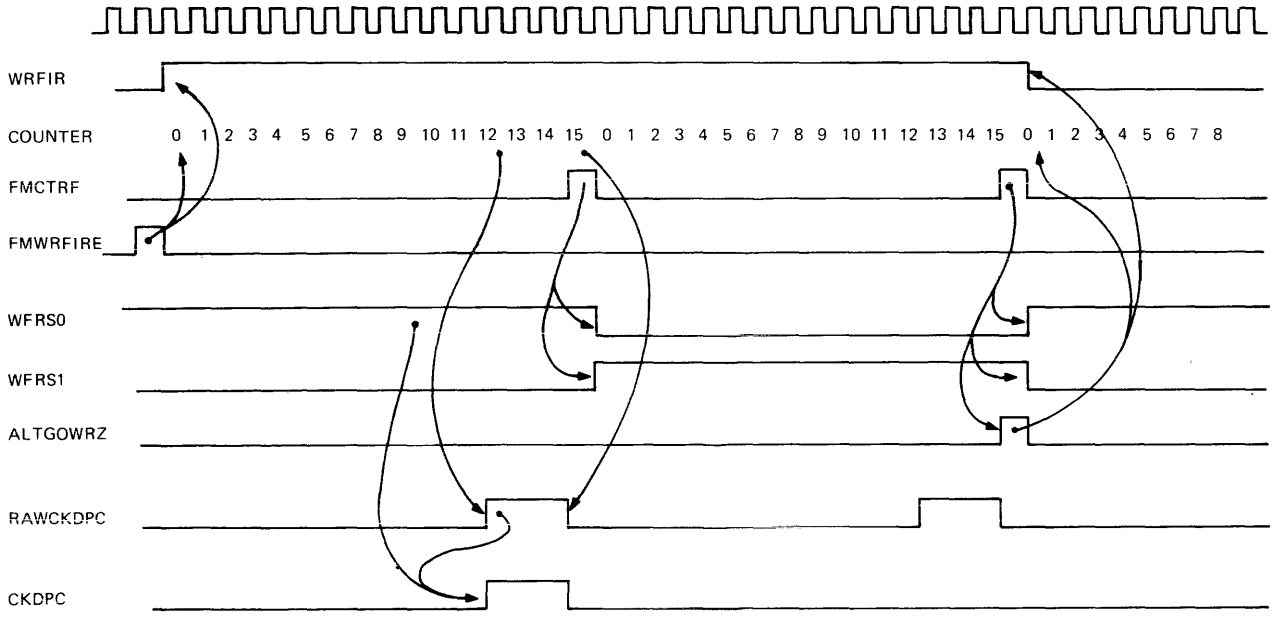


Figure 4-9. WRITE FIRE State Logic (206)

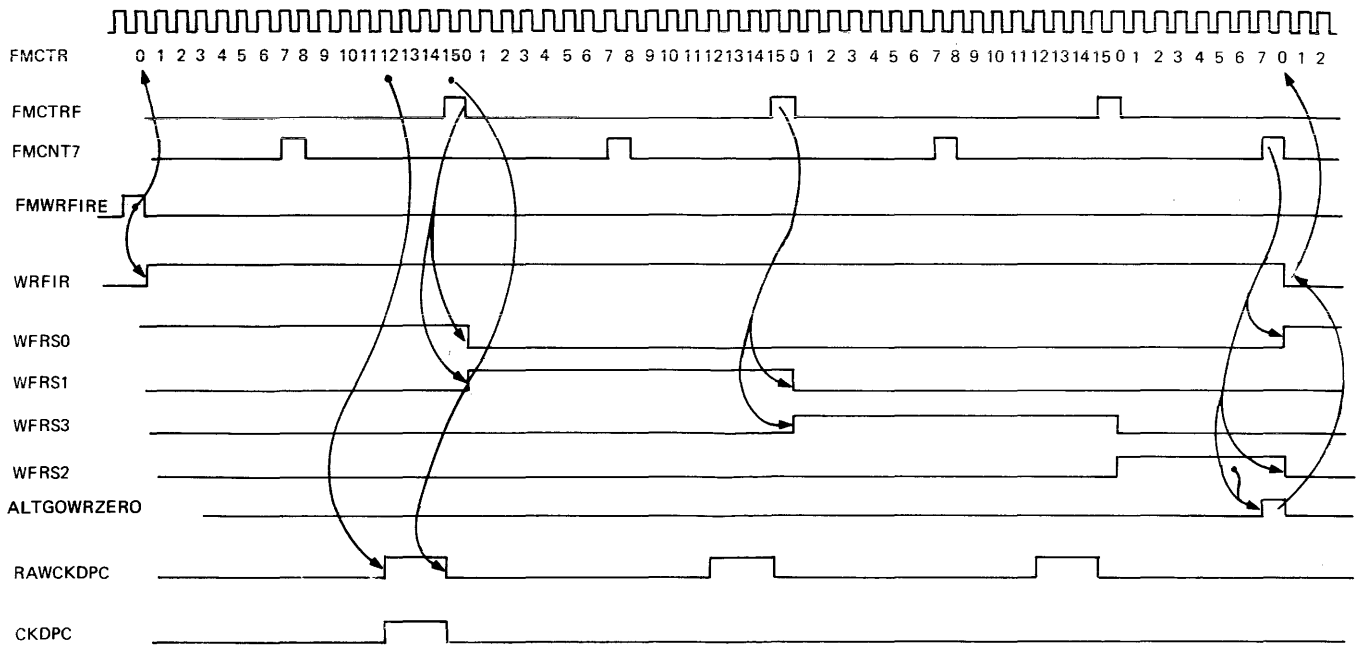


Figure 4-10. WRITE FIRE State Logic (207)

WRFIR performs the following functions:

1) FIRESHEN - enables the firecode generated to be shifted on to the data line for the drive.
2) WRFST1 - WRFST0 goes low. WRFST1 goes high.
3) CKDPC - one DPC clock is sent.

FMWRDATA

FMWRDATA occurs during the WRITE, INITIALIZE and RELOCATE flows. FMWRDATA becomes WRD after the register. WRD performs the following functions:

1) FIRENCEN - enables the firecode to be built-up.
2) LDWRBFFR - the write buffer is loaded at bit 11 of each word from the data bus.
3) LDPSPREG - the parallel to serial register is loaded at bit 15 (FMCNTF) of each word from the write buffer.
4) SERMPXR0, SERMPXR1/ - if the signal WTPROCDT is high, serial multiplexor 0 high and serial multiplexor 1 low causes the data line to the drive to contain the output of the parallel/serial/parallel register as the bits are shifted out. The firecode input (FIREIN) also receives the same data.
5) SERMPXR0/, SERMPXR1/ - if WTPROCDT is low, SERMPXR 0 and 1 are low. This causes the serial header to go out on the data line to the drive. This occurs on an INITIALIZE or RELOCATE when processor data is not specified in the variants.
6) WR32HEDR - is true when WTPROCDT is low. This causes the header to be cycled so that the header information may be supplied to the data multiplexor.
7) CKDPC - CLKDPC is required in order to request data from the DPC.
8) FRWTMD - firewrite mode (207).
9) MNTMEMEN - maintenance memory enable is true when the unit is in local, when the operation is a WRITE or INITIALIZE or RELOCATE with processor data. In this case the processor data is obtained from the maintenance memory.

FMWRONES

Format write ones occurs in mode 6 in order to write the data sync character. It also occurs in mode 8 for writing the address sync character and the data sync character. In mode 11, it occurs when the address field is to be overwritten with ones during a RELOCATE operation.

FMWRONES is latched into the format mode register and becomes WR1. WR1 performs the following functions:

1) LDSPSREG - the serial parallel serial register is loaded from the write buffer at bit 15 (FMCNTF). This only occurs on a WRITE or INITIALIZE or the second pass of RELOCATE. Bit 15 is the last bit of the sync character. FMWRDATA is high at the same time. The word loaded is shifted and the first bit written on the next clock.

2) SERMPXR0 - SERMPXR0 and SERMPXR1 allows a high level to go out on the data (BUFFDATA) line to the drive.
3) WR32HEDR - occurs on RELOCATE pass 2. It shifts the address out bit by bit for writing in the address field. WR32HEDR occurs at bit 15 (FMCNTF). WR32HEDR also occurs during INITIALIZE and RELOCATE pass when processor data is not specified. This allows SERHEDR (serial header) to be written in the data field.
4) CKDPC - occurs during mode 6 or mode 8 word 16. This instructs the DPC to place the second word on the information lines.

FMWRADDR (Write Address)

FMWRADDR occurs during the INITIALIZE flow or the RELOCATE flow (pass 2). FMWRADDR causes the address and EPC to be written on to the track. FMWRADDR becomes WRADR after being latched in the format control mode register. WRADR causes the following actions:

SERMPXR1/, SERMPXR0/ - this causes the serial header information to be selected for the data line to the drive.

SYNC CHARACTER DETECTOR

See schemtaic 09.15.01 for the following discussion.

The address and data fields are preceded by a sync character of four ones. This is required in order to synchronize the DDEC to the data so that the word boundaries are defined.

The detector is enabled when the flow causes the signal ENSNCDET (enable sync character detect) to be true. This signal removes the clear from the shift register at F0. SERDTIN (serial data in) is shifted into the shift register on each clock. When four ones are detected the output of the gate F1 goes low.

Address Sync

See figure 4-11 for the following discussion.

When the address mark is detected, ADSNCSTF is reset. When the four ones are detected at the end of the preamble, the signal STADRCMP (start address compare) goes true, and LDSECLOC/ (load sector location counter) goes low. On the next clock, ADSNCSTF (address sync start found) sets causing STADRCMP to go low and LDSECLOC/ to go high.

STADRCMP gives FMRDADDR (format read address) which resets the format bit counter and starts the address comparison. LDSECLOC synchronizes the sector location counter to the format.

Data Sync

See figure 4-12 for the following discussion.

When the address mark is detected, DTSNCSTF (data sync start found) is reset. When the four ones are detected, the signal STDTAXFR (start data transfer) goes high, and LDSECLOC/ goes low. This occurs because ADSNCSTF is now high. One clock pulse later, DTSNCSTF sets making STDTAXFR low and LDSECLOC/ high.

STDTAXFR gives FMRDDATA which synchronizes the sector location counter to the format.

PARALLEL/SERIAL/PARALLEL REGISTER

The purpose of the parallel/serial/parallel register is to convert 16-bit parallel words from the DPC into bit serial for the drive during WRITE and to convert bit serial data from the drive into 16-bit parallel words for the DPC during READ. (See figure 4-13).

The PSP. register consists of:

1) A write buffer to receive 16-bit words.
2) A shift register which may be loaded with 16 bits and shifted least-significant bit to most-significant bit during WRITE. It is also serially loaded during READ with data from the disk.
3) A read buffer which may be loaded whenever a word of information is complete in the shift register. The read buffer has a tri-state output. The output only drives the data bus when RDBUFFEN is true.

Write Buffer

See figure 4-14 for the following discussion.

The write buffer is loaded at bit 11 of each word with the signal LDWRBFFR. This occurs while the previous word is still being written. In the case of the first word, it is loaded at bit 11 during the write of zeros in the preamble.

Shift Register

The shift register is loaded parallel from the write buffer when LDPSPREG/ is low. When LDPSPREG/ is high, the shift register shifts least-significant bit to most-significant bit at clock speed. During a write, LDPSPREG/ goes low at bit 15. The write buffer is loaded on the next clock so that the most-significant bit of the next word follows the least-significant bit of the previous word without a break.

During READ, data is shifted in from the drive least-significant bit to most-significant bit. LDPSPREG/ is high.

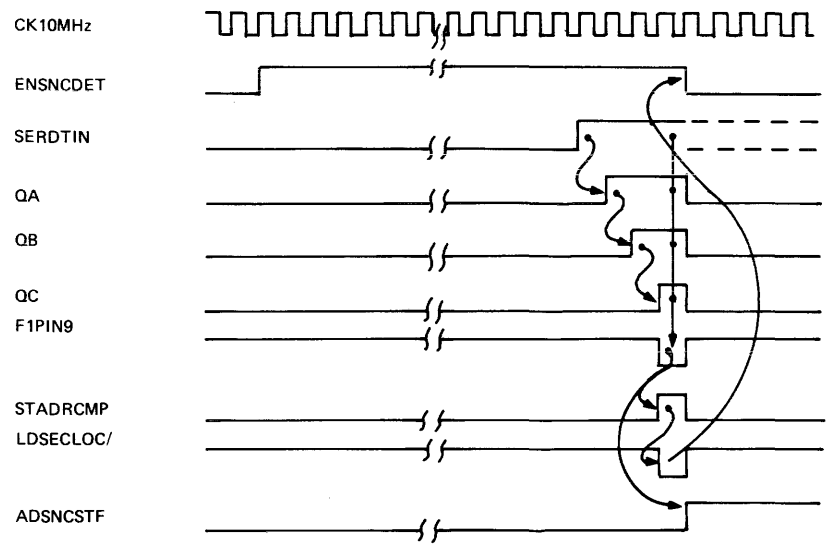


Figure 4-11. Sync Character Detect Address

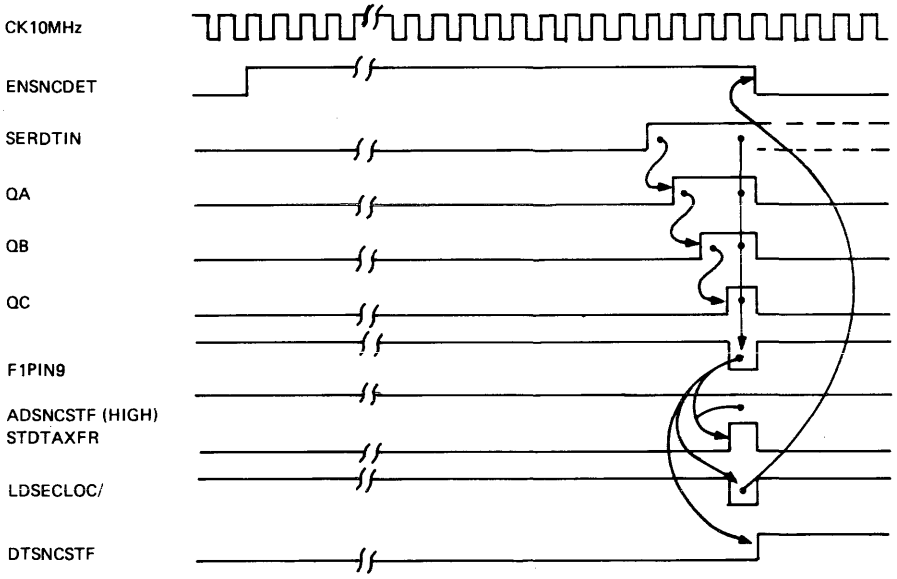


Figure 4-12. Sync Character Detect (Data)

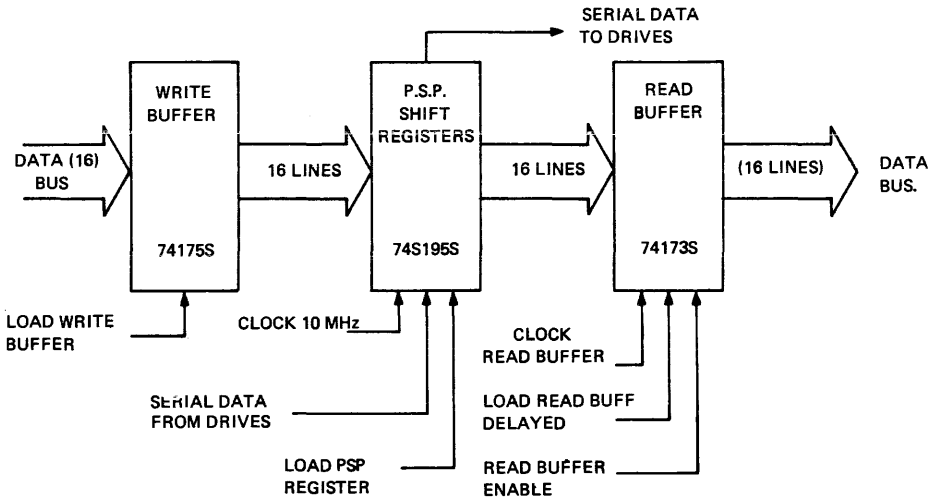


Figure 4-13. Parallel/Serial/Parallel Register

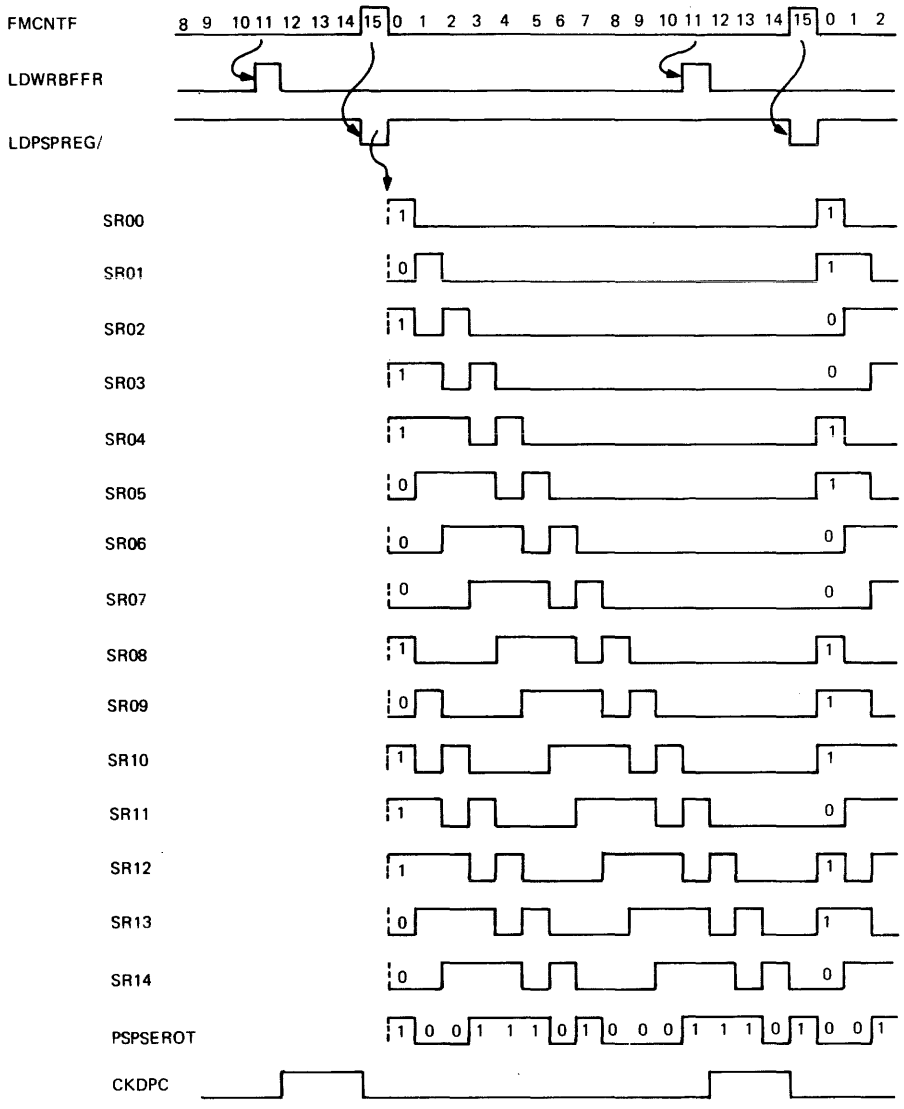


Figure 4-14. PSP Register (Write)

Read Buffer

During READ, the read buffer is loaded one clock after bit 15 of each word (see figure 4-15). At this time the word is complete. RDBUFFEN enables the read buffer output to go onto the data bus. XMITENABLE permits the information on the data bus to go on the INFO lines. CKDPC causes the DPC to accept the INFO data.

206 FIRECODE

Firecode Generation (206)

Firecode is generated in two conditions:

1) During WRITE data the firecode is built up for writing in the firecode field on the disk.
2) During READ, the firecode is built up from the data received from the drive. This is used for comparison with the firecode read off the disk.

The signal FIRENCEN (fire encode enable) permits the firecode to be built up in the firecode register. The data used as input to the firecode generation logic is derived from three sources and selected by the main serial multiplexor. (See figure 4-2).

1) During WRITE data, FIRINBUF is derived from PSPSEROUT.
2) During INITIALIZE or RELOCATE when processor data is not specified, FIRINBUF is derived from SERHEDR. (Addresses are written in the data field).
3) During READ Data, FIRINBUF is derived from SRDTDLYD (serial data delayed). This is READ data from the drive. (See the block diagram in figure 4-16).

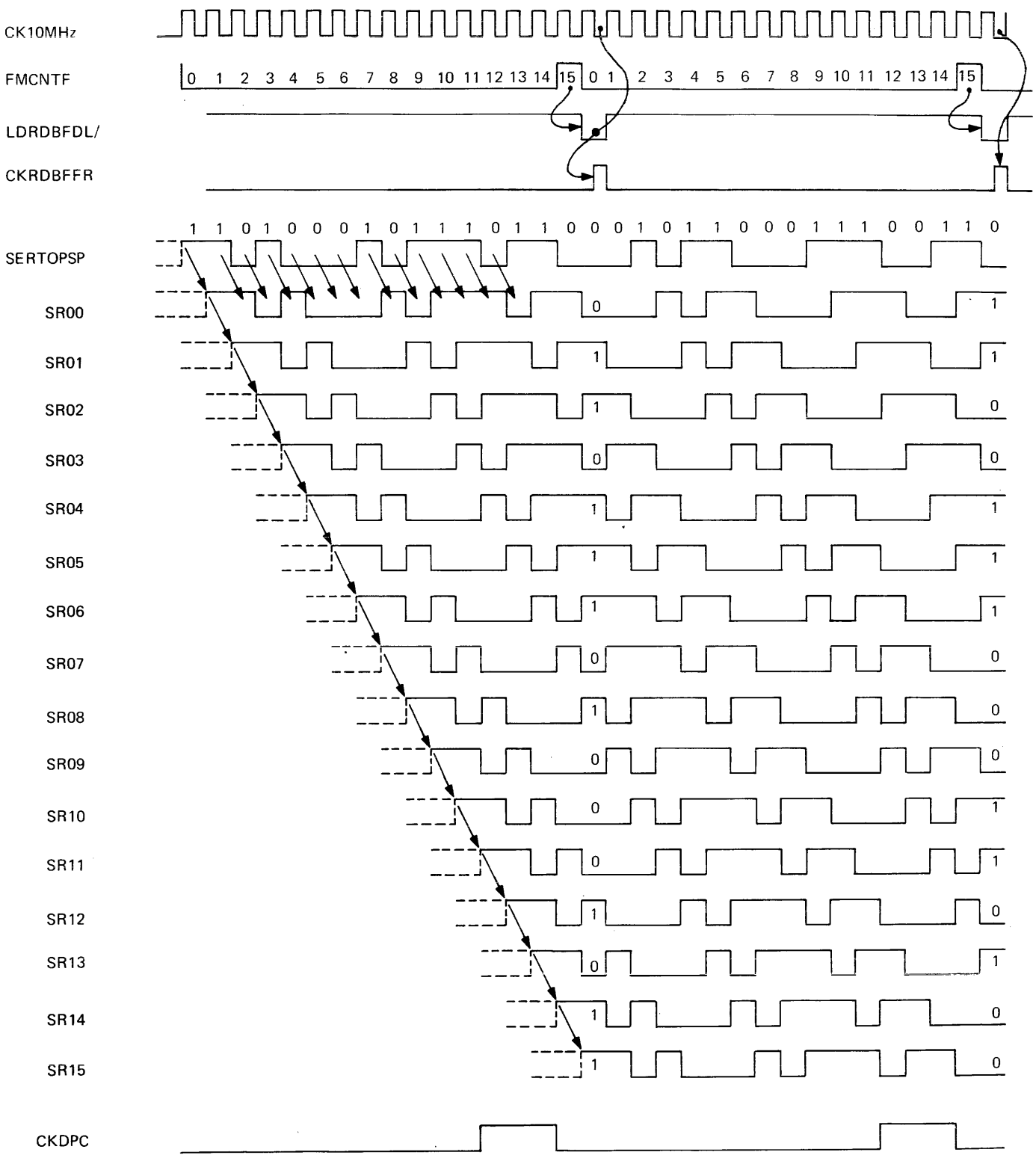


Figure 4-15. PSP Register (READ)

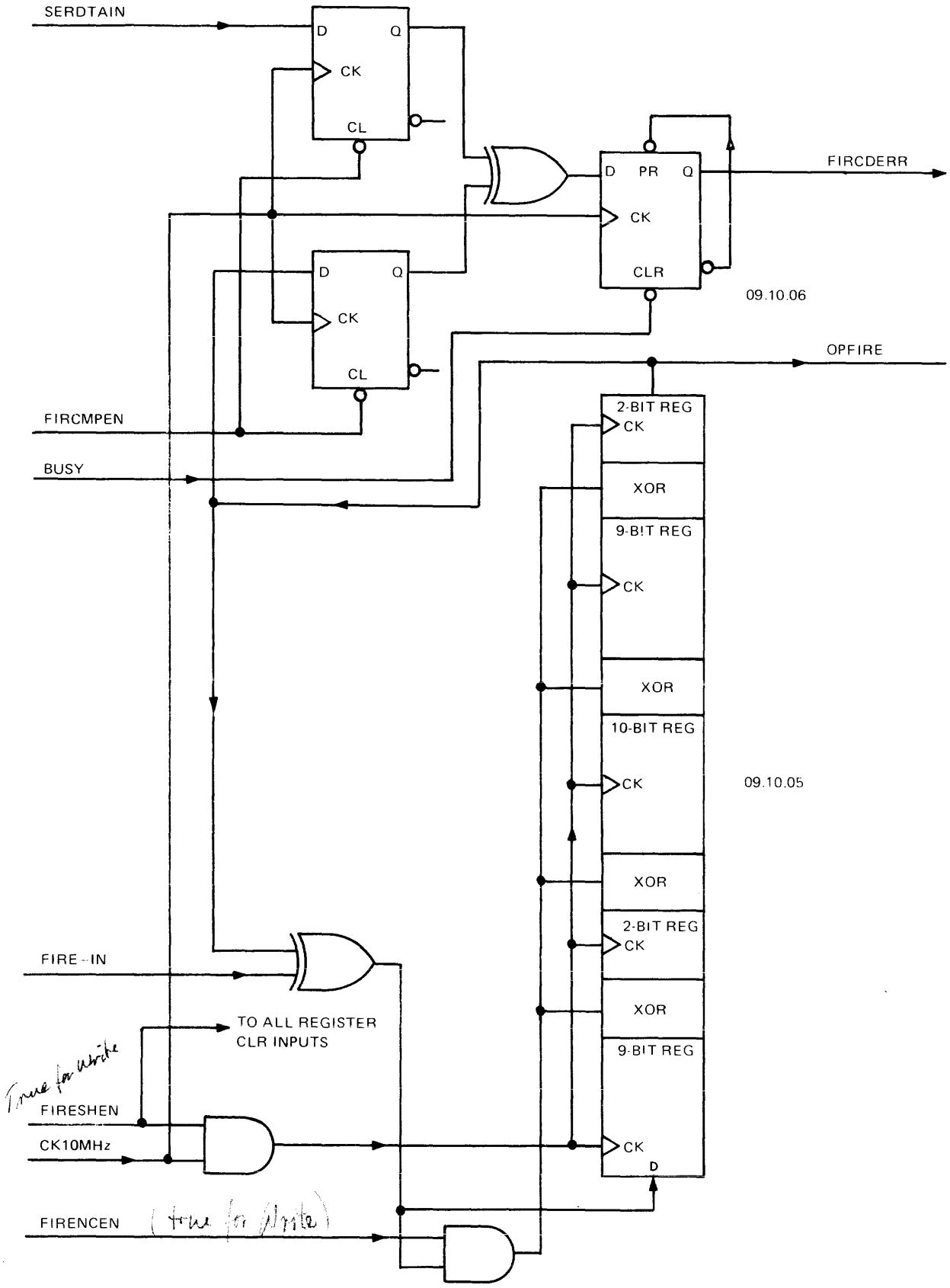


Figure 4-16. Firecode Block Diagram (206)

The firecode shift register consists of a 32-bit register. The output of each flip-flop is routed to either the next flip-flop or through an exclusive OR gate to the next flip-flop. The output of the last stage is routed through an input exclusive OR gate to the first stage, thus giving a circular path. All flip-flops start reset.

On the leading edge of each clock pulse, the shift register shifts one position. On the first high bit in ON FIRINBUF, bits 1, 10, 12, 22, and 31 set. If bit 32 is low, the next high bit in sets bit 1 and is exclusive ORed into bits 10, 12, 22, and 31. If bit 32 is high, a low FIRINBUF sets bit 1 and a high is exclusive ORed into bits 10, 12, 22, and 31.

This process continues for 1440 bits (180 bytes x 8 bits). During this time a complex pattern is built up in the 32-bit register.

Write Firecode (206)

During the generation of the firecode, FIRENCEN and FIRSHEN (fire shift enable) are true. At the end of the data field, FIRENCEN goes low but FIRSHEN stays high for 32 bits extra. During this time, the 32-bit shift register is shifted out on the OPFIR (output FIRE). During a WRITE OP, this output is gated through the main serial multiplexor and on to the selected drive.

Firecode Comparison (206)

At the end of each data field during READ or VERIFY, the firecode read from the disk is compared with the firecode generated during the READ. A non-comparison indicates an error in reading the data (or firecode) from the disk. It could also indicate that the data (or firecode) is written incorrectly.

At the end of the data field, the signal FIRESHEN is high for 32 bits. This allows the shift register containing the generated firecode to be shifted out a bit at a time on to OPFIRE. At the same time, the firecode read from the disk is fed in on SERDTAIN. Both inputs are synchronized to the same clock and are fed into an exclusive OR gate for comparison. FIRCMPEN enables the two synchronization flip-flops for the duration of the comparison.

As long as the two inputs are both high or both low, the output from the exclusive OR is low. If the inputs differ (one high and one low), the output goes high, setting the FIRECODE ERROR flip-flop.

The firecode error is reported in the result descriptor for this sector and all the subsequent sectors, and the final result descriptor.

207 FIRECODE

General Description

The 207 uses a 54-bit firecode which has the ability to correct bursts of up to 11 bits. The probability of correcting an 11 bit-error incorrectly is 1 in 2 x 10 to the –17th power. The DDEC performs the following firecode functions:

1) Firecode generation.
2) Error detection.
3) Error correction.

The 54 bits are split into two separate codes: a 32-bit code and a 24-bit code. The 32-bit code protects the 180 bytes of data. It is identical to the 206 code. The 24-bit code protects the 180 bytes of data and the 32-bit code. All 54 bits are generated during WRITE, and all 54 bits are used to detect errors.

During correction, the 32-bit code is used to perform the correction, and the 24-bit code checks the integrity of the correction.

A buffer stores each sector of information for reuse during a correction operation. The data in the buffer is only used if the DPC sends a READ with correction operation.

Firecode Generation During Write

The 207 WRITE operation has one variant. The N2 bit ON during WRITE is known as a diagnostic WRITE. A diagnostic WRITE intentionally writes the firecode incorrectly so that a diagnostic program may check out some of the hardware concerned with firecode. Diagnostic WRITE is covered later. The following paragraphs describe a normal WRITE operation.

Normal Write

See the block diagram in figure 4-17 for the following discussion.

During WRITE data, the data (FIREIN) goes to the drive and to the two firecode registers. As the data goes out bit by bit, both registers circulate the data through exclusive OR gates similar to the 206 firecode and EPC registers previously described. (See figures 4-18 and 4-19).

At the end of the data field, the 32-bit register holds the first 32 bits of firecode to be written. The multiplexors switch so that FIREOUT is derived from FIR31 (output from the 32-bit register). This causes the 32 bits of data to go to the main serial multiplexor for writing on the unit.

Also, at the end of the data field, the input multiplexor to the 24-bit register switches so that the 32 bits of firecode being written also get encoded into the 24-bit register.

When the 32 bits of firecode have been written, the 24-bit register holds the remainder of firecode. The multiplexors switch so that FIREOUT is derived from FIR55 (output from the 24-bit shift register).

Figure 4-20 gives detailed timing and table 4-3 shows the multiplexor controls.

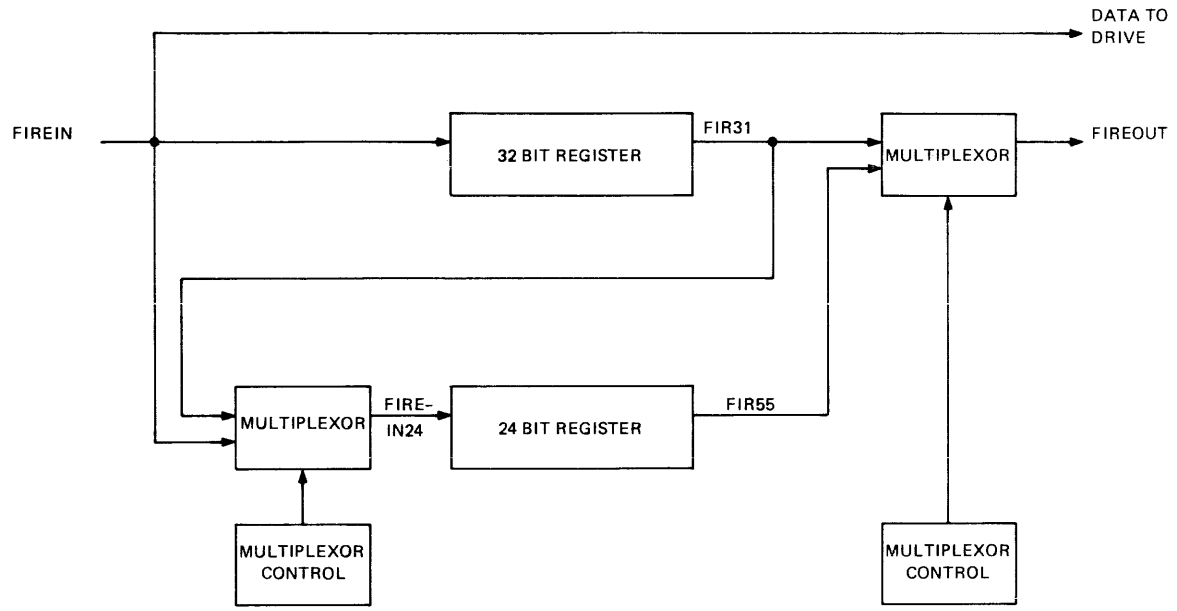


Figure 4-17. 207 Firecode Generation

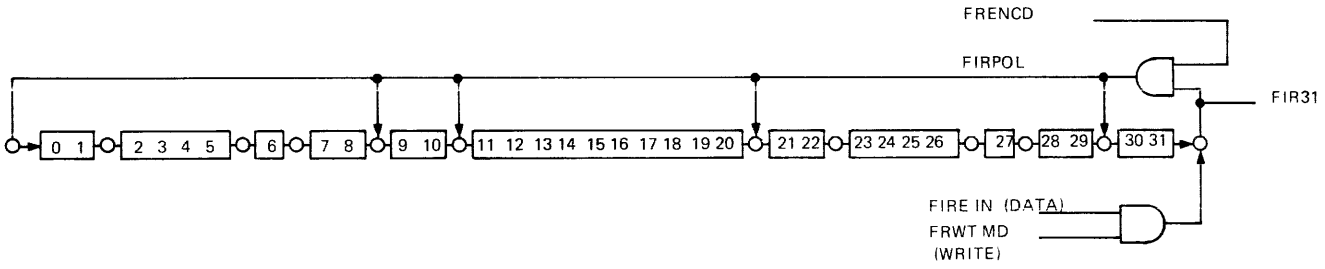


Figure 4-18. 32-Bit Firecode Register During Write

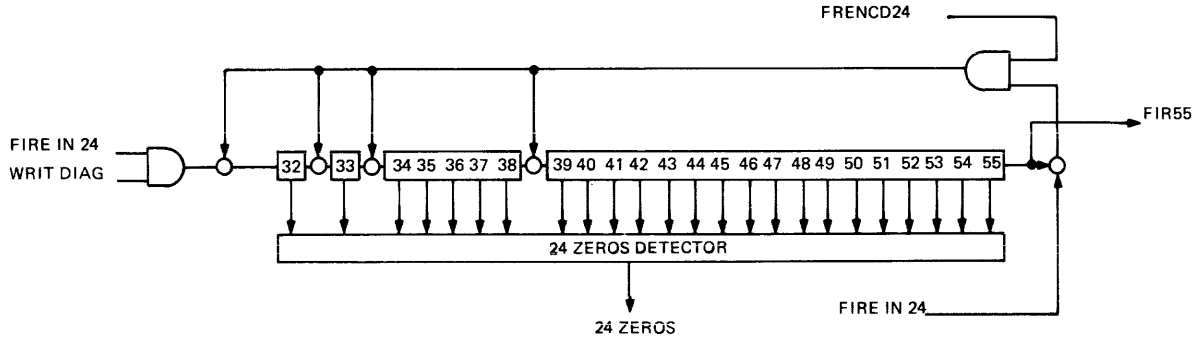


Figure 4-19. 24-Bit Shift Register

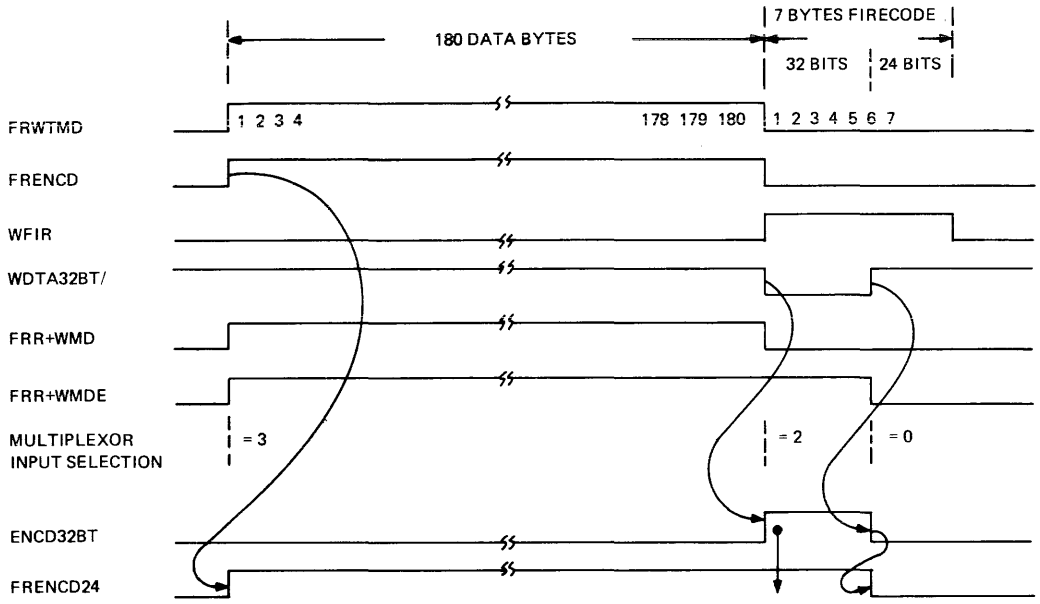


Figure 4-20. Firecode Generation Control Signals

Diagnostic Write

The N2 bit causes WRITDIAG/ to be low. This signal performs the following functions:

1) Causes FRENCD (fire encode) to be low.
2) ENCD32BT is low.
3) Forces the multiplexor to input zero.

FIREIN24 comes from FIR31; FIREOUT comes from FIR55).

In this condition, the two registers act as a straight shift register. At the end of the data field, the shift registers hold the last seven bytes of data information. This information is written in the firecode position.

Table 4-3. Multiplexor Control

Input Selection	A	B	FIREIN24	FIREOUT	Comments
0	A/	B/	FIR31	FIR55	24 Bits on write, 56 bits on diagnostic write.
1	A	B/	CRSRDTOT	OPFIR	Error correction.
2	A/	B	FIR31	FIR31	32 Bits on write
3	A	B	FIREIN	0V	180 Bytes on write, 187 bytes on read.

A = 206 + ERCRMD456+ (FRR+WMD) * WRITDIAG/
B = (FRR+WMDE) * WRITDIAG/

Error Detection

On the 206 error detection, the firecode is rebuilt in the firecode register from the read data and compared, bit by bit, with the firecode read from the disk. Due to the requirement for error correction, the method of error detection is changed on the 207.

On the 207, during READ, additional exclusive OR gates are enabled. These gates are enabled by the signal PRMPOL (pre-multiplication polynomial). (See figure 4-21). At the end of the sector, the 32-bit register and the 24-bit register must contain all zeros. If either register is not zero, this indicates a firecode error (207 FRER).

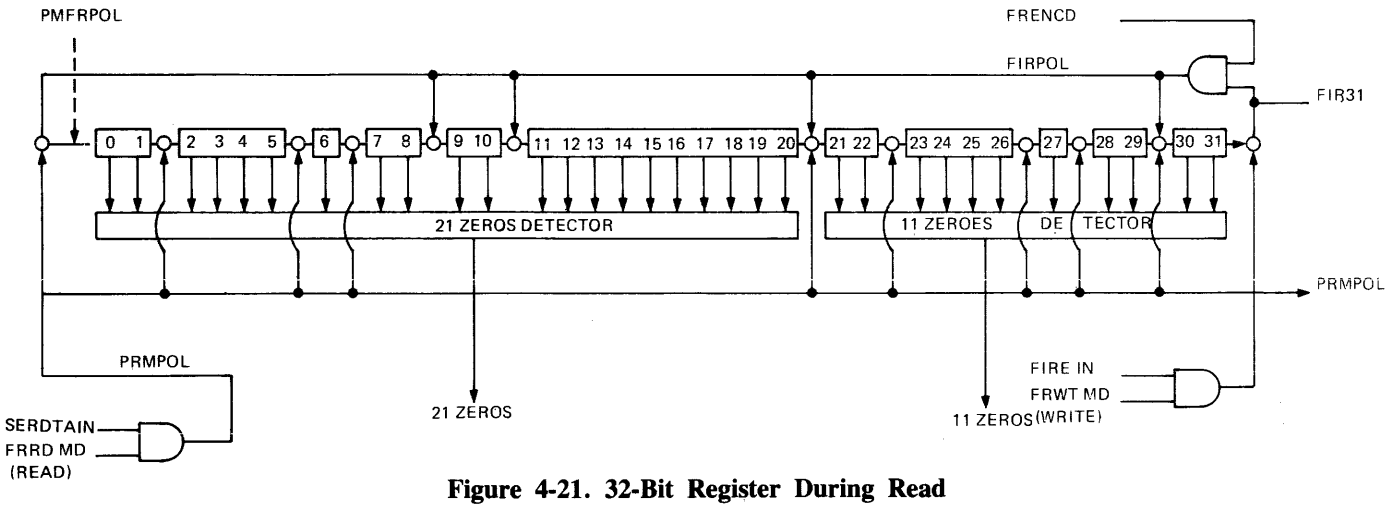


Figure 4-21. 32-Bit Register During Read

Figure 4-22 shows the timing of the control signals during READ. FIREIN is fed into both the 32-bit and the 24-bit shift register through the multiplexor. The 32-bit register encodes the data and the first 32 bits of firecode read from the disk. At the end of the 32 firecode bits, ERCRMO23/ goes low preventing further clock pulses to the 32-bit register. This action effectively traps the state of the register. This is necessary because the 24-bit register encodes for the entire 187 bytes.

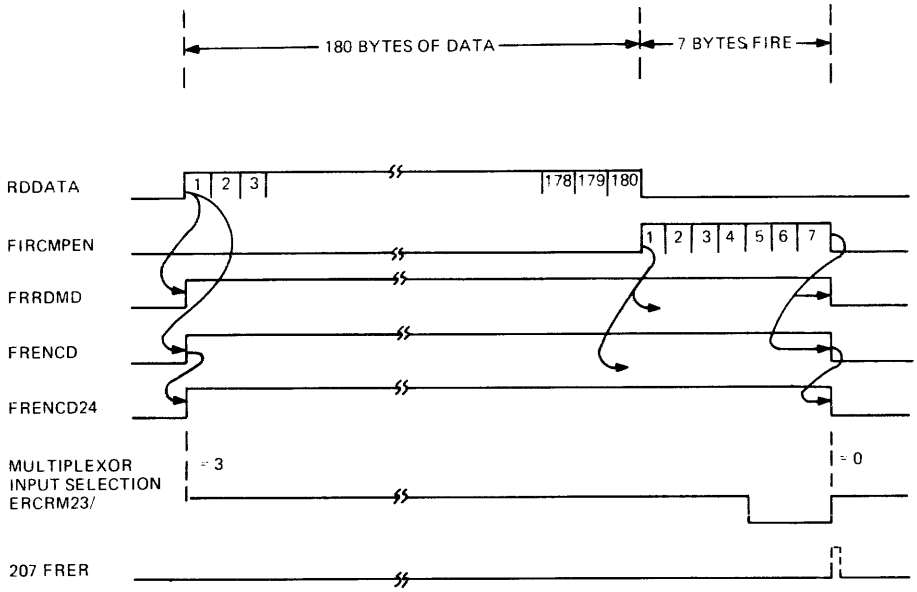


Figure 4-22. Error Detection Control Signals

At the end of 187 bytes for one clock period only, there should be all zeros in the registers. At W108B15, 207 FRER (207 FIRECODE ERROR) is gated to FIRCDERR flip-flop. If it is high at this bit time, FIRCDERR flip-flop sets.

During the READ operation, buffers store the data and firecode information for later use during a correction. The operation of the buffers is described later.

Error Correction

See figure 4-23 for the following discussion.

Error Correction occurs in two basic phases:

1) Reading the sector.
2) Correcting the data.

During the READ phase, CKDPCs are prevented from going to the DPC; this prevents data from reaching the DPC. The data and firecode are stored in the buffer memory. The 32-bit firecode is generated in the normal way. However, the 24-bit register is prevented from encoding so that it contains all zeros at the end of the READ phase.

The code in the 32 firecode register is divided into two sections:

1) The first 21 bits.
2) The remaining 11 bits.

The first 21 bits, known as the syndrome, determine the point at which the error starts in the data field. The remaining 11 bits contain the error pattern. (A one indicates that the bit in memory should be complemented; a zero indicates that the bit in memory is correct).

During the correction phase, data is sent to the DPC from the buffer memory. As each bit is read out of memory, the 32-bit firecode register receives further encoding. The first 21 bits are monitored for all zeros. When 21 zeros are detected, the correction is performed by exclusive ORing the 11 bits, one at a time with the data from the buffer memory. Where there is a one bit in the 11 bit shift register, the buffer memory bit is inverted.

If 21 zeros are not detected during the correction cycle, this indicates that the error is greater than eleven bits and is uncorrectable. A result descriptor containing firecode error is returned.

If a correction is performed successfully, in addition to returning a result descriptor without a firecode error, bit 2 of the result descriptor is set (WL). This distinguishes a successful error correction READ from a normal READ.

During the correction cycle, the 24-bit register encodes from the output of the corrected data. At the end of the 180 bytes + 56 bits, all the firecode registers must be zero. If they are not zero, FIRECODE ERROR FF is set.

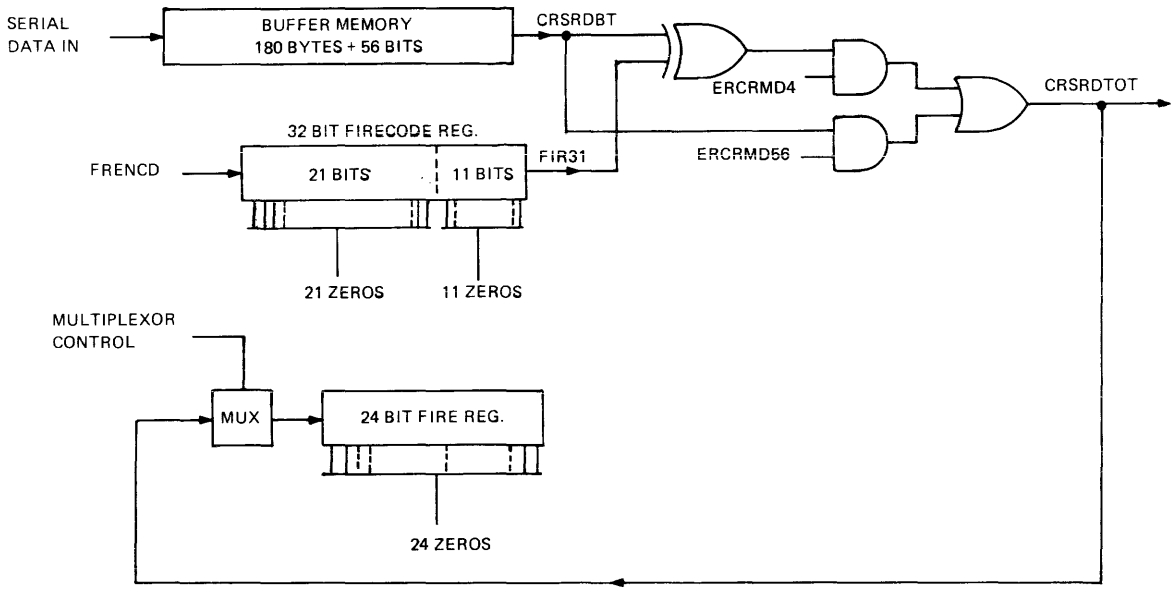


Figure 4-23. Block Diagram Error Correction

Error Correction Modes

The error correction operation is controlled by ERCR modes. (See figure 4-24). ERCR modes should not be confused with the main modes of the DDEC.

The error correction operation is a single sector operation. After a normal address search, the main flow enters mode 6 for the data transfer (READ). GTM6DLD (To go to mode 6 delayed) takes the ERCR mode from mode 0 to mode 1. ERCR mode 1 stays high until the end of 32 bits of firecode (W107B7). At this time, ERCR mode 1 goes low and ERCRMODE 2 goes high for 24 bits. At W108B15, ERCR Mode 3 goes high.

During the READ phase, CKDPC is prevented by the signal ERRCORCT* (ERCRMD1+ERCRMD2). The data and firecode are written into the buffer memory.

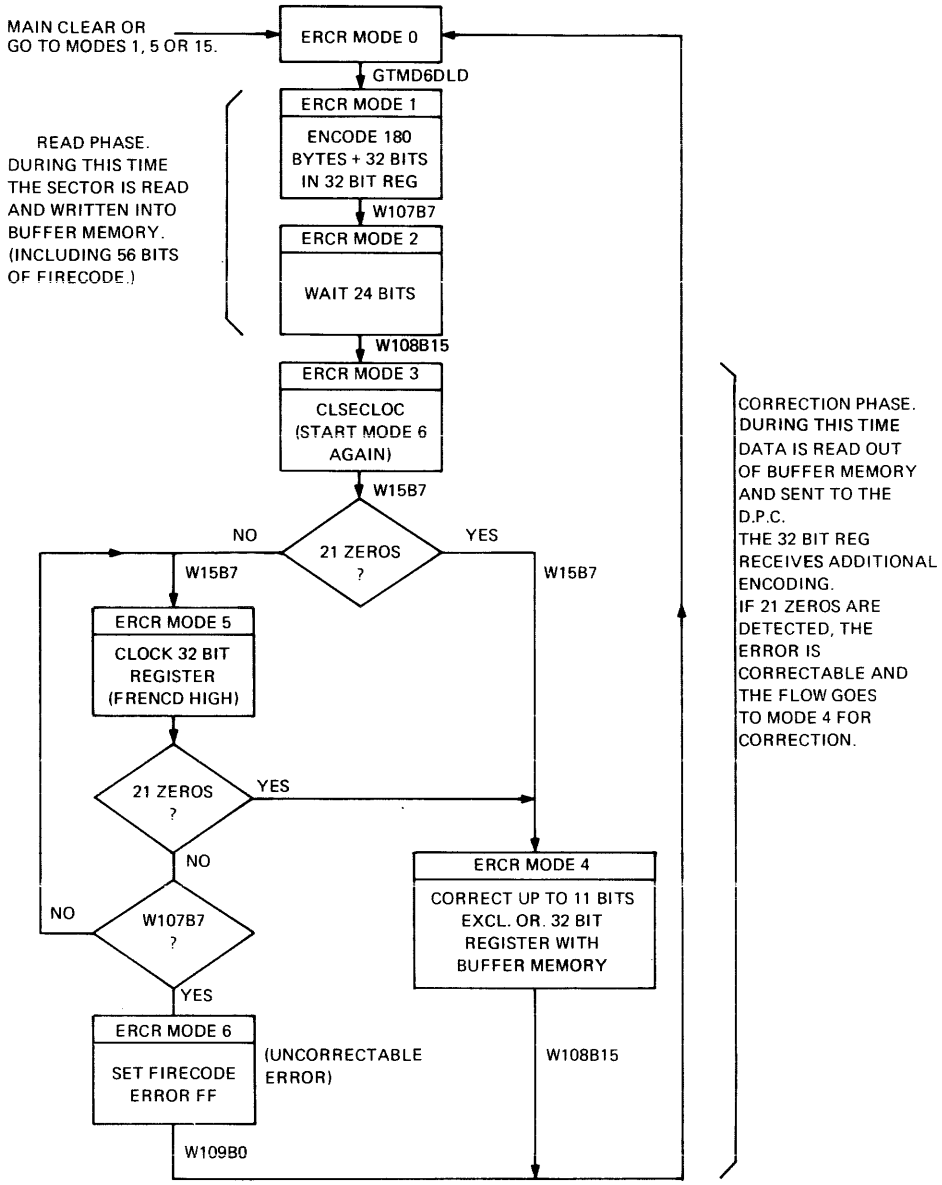


Figure 4-24. Error Correction Flow Chart

ERCRMD3 going high after the firecode causes CLSECLOC at W109B14 of the main mode 6 flow. This action causes the flow to go back to the beginning of mode 6.

At W15 B4, STMMRD starts the process of reading out of the memory buffer. (This is described later). At W15B7, FMRDDATA causes the format logic to start the normal read sequence. In this case, however, the data is received from the memory and correction circuit, not the drive.

Also at W15B7, the ERCR mode goes to 5 if 21 zeros are not detected, or mode 4 if 21 zeros are detected.

In ERCR mode 5, the code in the 32-bit register left over from the read phase is circulated with FRENCD. There is no new data fed into the register. At the same time, the data from the buffer memory is shifted out to the PSP. register. CKDPC transfers the data to the DPC as each byte is ready in the PSP. register.

If 21 zeros are detected, the flow goes to ERCR mode 4. ERCRMD4 is entered with the failure pattern in the last 11 bits and zeros in the 21 bits. FRENCD goes low preventing further encoding and allowing the 32-bit register to act as a shift register. The output of the 32-bit register (FIR31) is exclusive ORed with the data from memory.

Wherever the error pattern shows a 1, the bit from memory is inverted. ERCRMD4 stays true until the end of the firecode. The error correction flow then returns to 0.

During the correction phase, the 24-bit shift regis-

ter encodes from the correction serial data. Refer to table 4-3. Input selection 1 is selected. Firecode error flip-flop sets in the normal way if the complete firecode register is not equal to zero.

If 21 zeros have not been detected by W107B7, the error is uncorrectable. The flow goes to ERCR mode 6. Mode 6 gives the signal 207 FRER, which sets the firecode error flip-flop. At W108 B15, the flow goes to ERCR mode 0.

At the end of mode 6, the main flow goes to mode 15 to terminate and send a result descriptor.

Buffer Memory

See figures 4-25 and 4-26 for the following discussion.

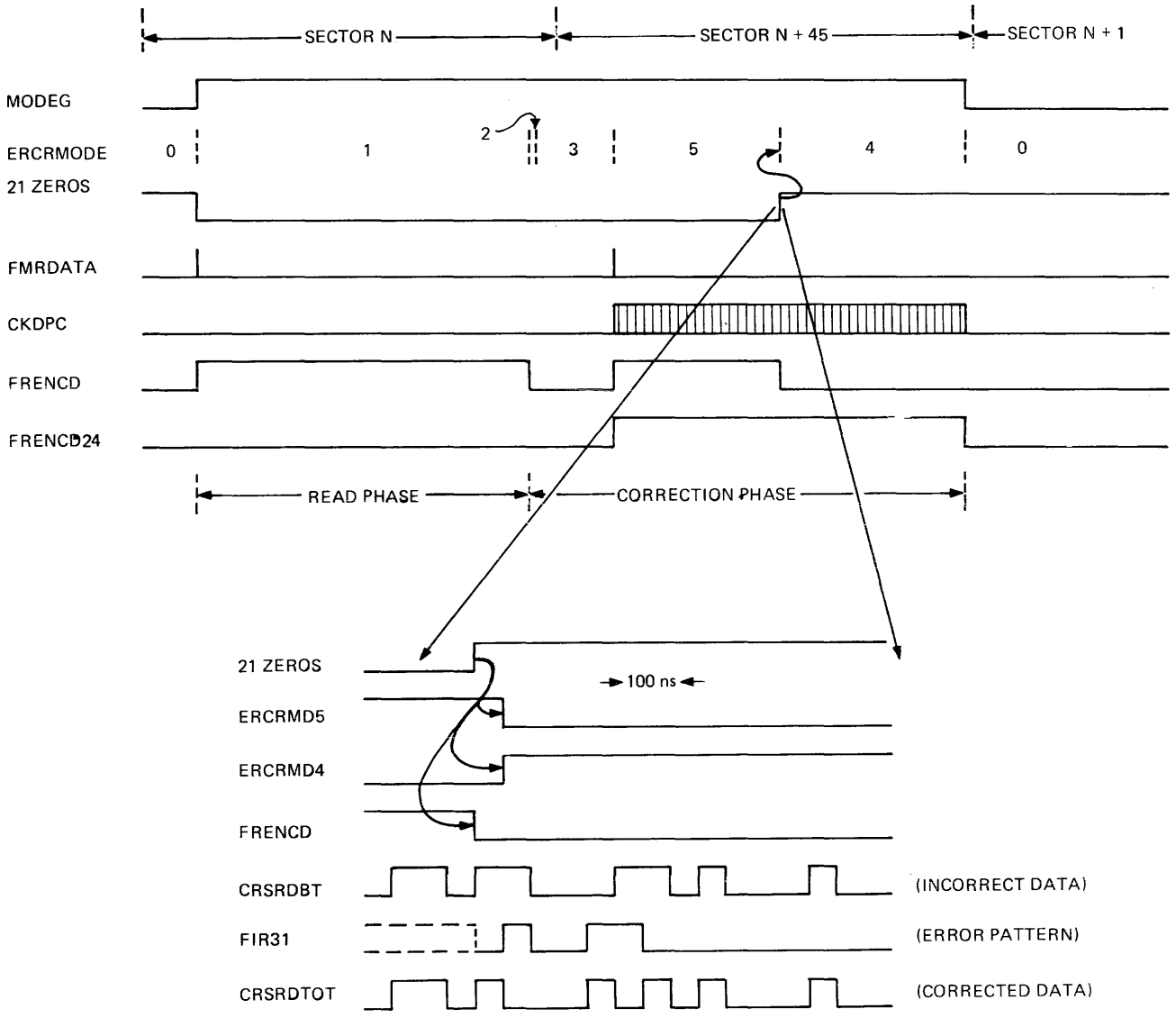


Figure 4-25. Error Correction Timing

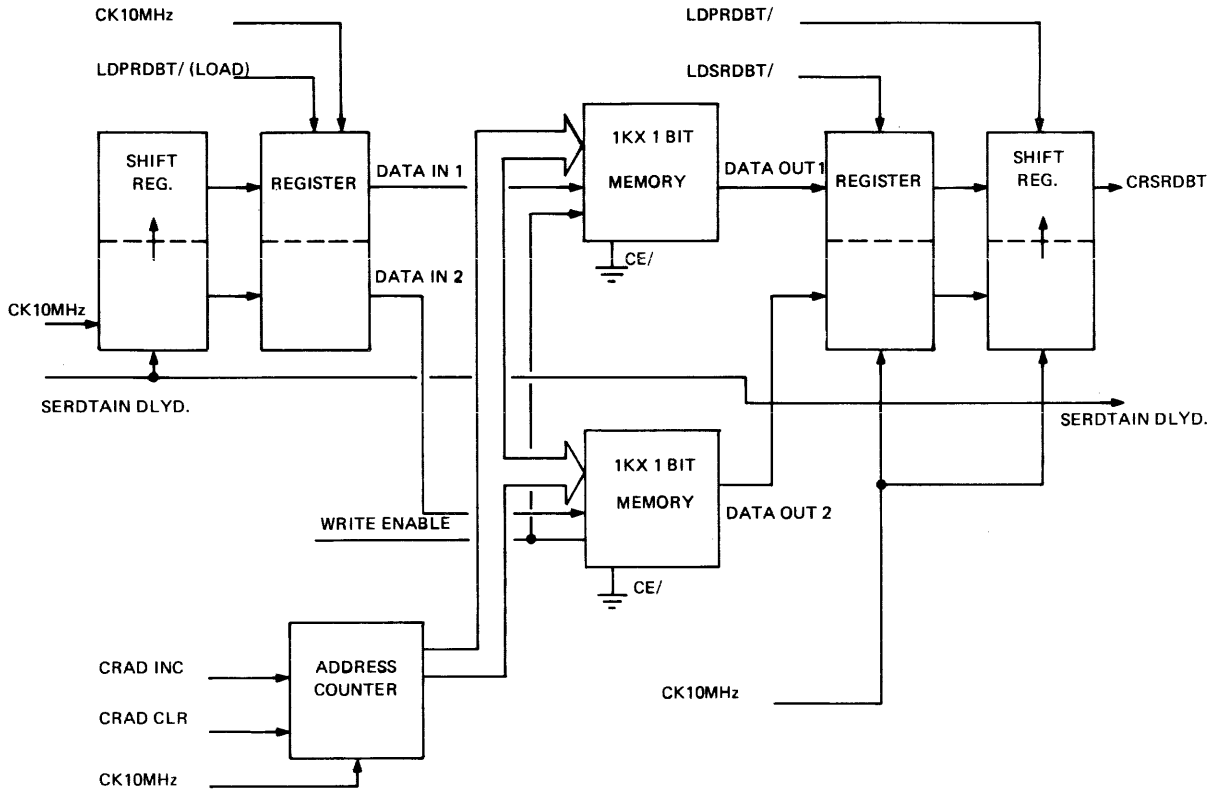


Figure 4-26. Buffer Memory

The buffer memory is used to store one sector of data and its associated 56-bit firecode. The information stored is used only if a read with error correction operation is performed.

Due to the amount of storage required, the cycle time of the memory IC and the availability of a standard, qualified memory IC, the buffer has been designed in an unusual manner. Two memory ICs are used, one storing the even bits of data and the other storing the odd bits of data. In this way, the cycle time of the memory IC may be twice the bit time.

During a WRITE to memory, serial data is shifted into a two-bit shift register, transferred to a register two bits at a time and written into memory. AN address counter is cleared at the beginning and end of the sector and is counted up every two bits which the data is reading from the disk.

During a READ from memory during the correction phase, data is read out two bits at a time, clocked into a register, and transferred to a shift register where it is shifted out serially bit by bit.

The MEMORY operation is controlled by a state machine giving MMSTATE 0 through MMSTATE 5. Refer the to timing diagram in figure 4-27 for the operation during WRITE and figure 4-28 for the operation during READ.

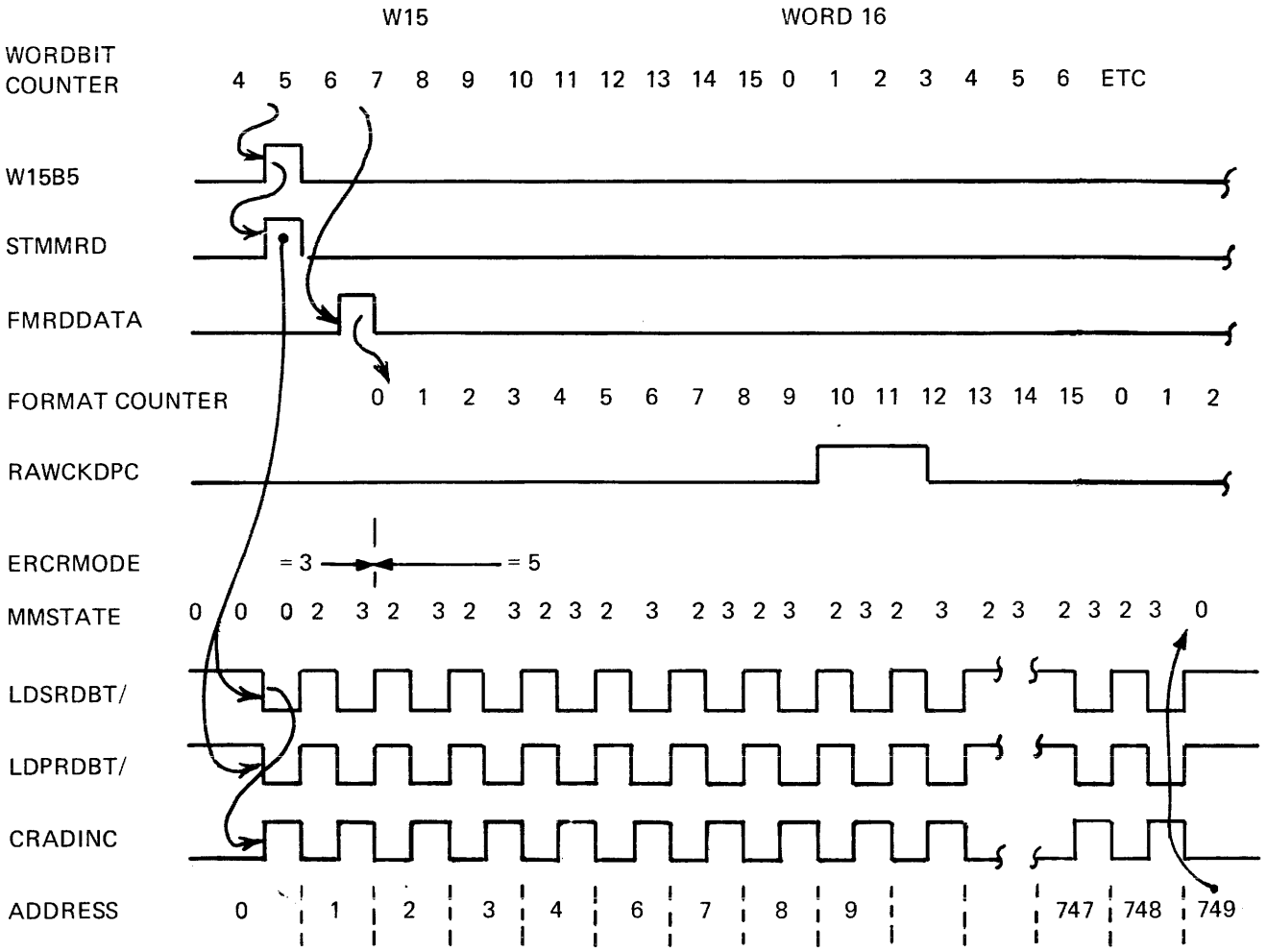


Figure 4-27. Buffer Memory WRITE

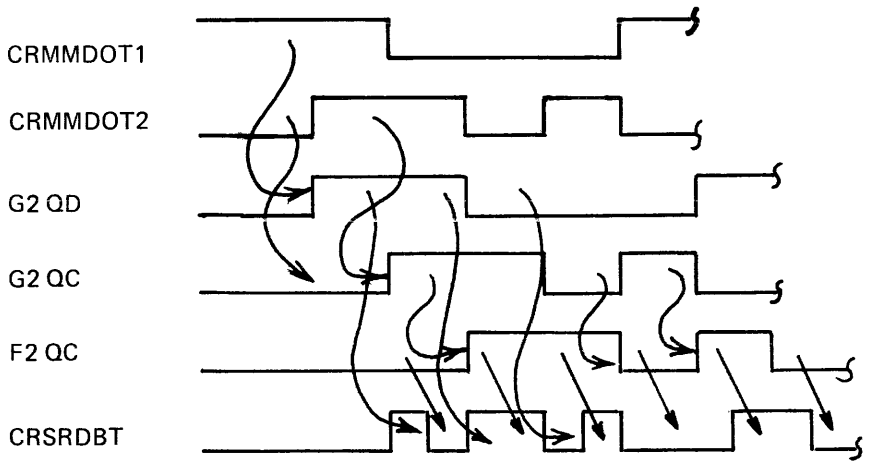


Figure 4-28. Buffer Memory READ

SECTION 5

MISCELLANEOUS CIRCUITS

RESET LOGIC

General Description

There are two sources of reset pulses in the DDEC:

1) When the unit is powered on, PWRRESET/ gives a 20 second reset pulse.
2) In local, when the MASTERCLEAR push button is pressed.

The various reset pulses are described below. (See schematic 09.16.05).

PWRRESET/ - this is a 20 second negative pulse. It resets the master clear signal in the maintenance logic and is used to generate all the other reset pulses except PBMNCLR/ (push button main clear).

PWRSYNC/ - this is PWRRESET/ synchronized with the 10 MHz clock. It resets the following logic:

OLD = NEW unit counter
DPEC EXCF
Mode flip-flops
Sets INSECLOC

MAINCLR - this is derived from PWRSYNC/ or PBMNCLR/. It presets the START/ flip-flop in the maintenance logic.

MAINCLR/, MAINCLR1/ - these two reset pulses reset:

Address decode control counter.
Maintenance memory address.
Sets the maintenance STOP latch.
Sets the LOAD/ latch.
Clears the error correction memory.
Format mode registers.
Format state logic.
Write fire state logic.
Unit register.
ERD control counter.
DMERD flip-flops.
CM select flip-flop.
CMSELSPRFF.
FCHDTOS FF.
MODE 4 FLOP.
LOOP MODE 10 FF.
READY FF.
BUSY FF.

MNCLRRAW - this is derived from PWRSYNC/ or MASTERCLEAR/. This pulse forces the DDEC to use the local clock.

PBMNCLR/ - this is MASTERCLR synchronized to the clock. It causes a GOTOMODE 1 signal so that the unit goes into the idle mode.

In addition to these reset pulses, many terms are reset by the signal IDLE which is mode 1, W0B0.

CLOCK LOGIC

General Description

See figure 5-1 for the following discussion.

The DDEC has two possible sources for the 10 MHz clock used internally:

1) A local oscillator in the DDEC.
2) The clock originating from the selected drive.

The local clock is used during the initiate phase of an operation. AT W2B3 of mode 1, the unit number has been received, and the clock from that unit is on CK10 DRV. The signal SW TO DR (switch to drive clock) occurs, which causes the CK10 MHz to be derived from CK10DRV. Special circuitry ensures that the clock switch does not split any clock pulses. (See figure 5-2 and schematic 09.11.04).

SW TO DR also occurs in mode 0 during the spinup sequence.

The clock switches back to local when the signal SWLOCAL goes true (see figure 5-3). Also, at the end of an operation, when BUSY and READY are low, the signal DRIVCKOK is forced low, which also causes the clock to switch back to local.

The drive clock dropout detector consists of a retriggerable one shot which is constantly retriggered by the drive clock. If the drive clock fails for 3-1/2 bit times, the one shot times out, resetting the drive clock OK flip-flop. This causes the local clock to be selected and a DPECEXCPT error signal.

Clock Stopper

The clock stopper is a maintenance aid designed to stop the clocks when a low to high transition is sensed on STOPCLOK. STOPCLOK must be jumpered to the signal or combination of signals required. It enables the Field Engineer to examine the state of the unit statically.

In order to use the stop clock, the DDEC should be in local with the ENABLE STOP switch on. When STOPCLOK goes high, it clocks a JK flip-flop giving DEADSTOP. DEADSTOP/ disables the clock drivers. At the same time, FCDESEL (forced deselect) deselects the drive. This action terminates a WRITE or a READ in the drive. Without this, the

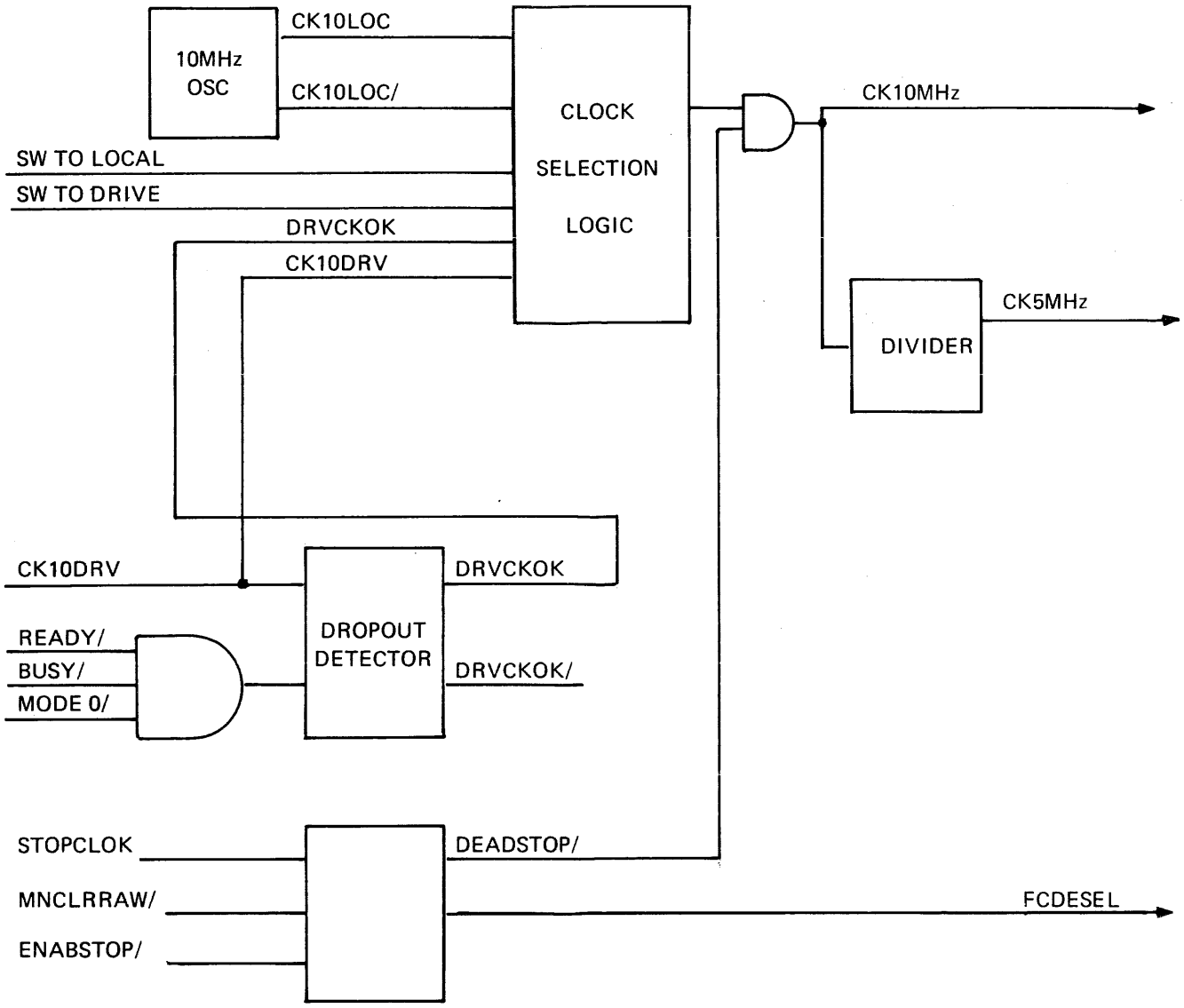


Figure 5-1. Clock Logic

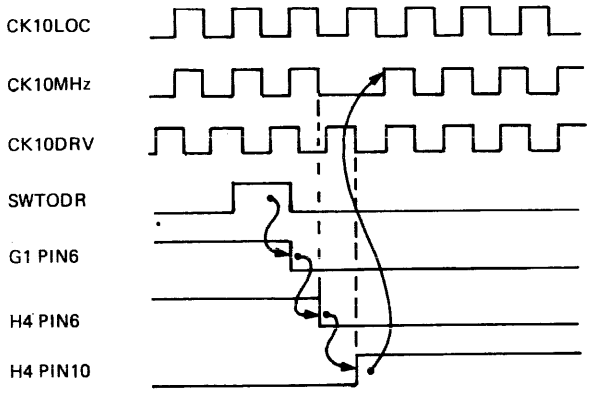


Figure 5-2. Switch to Drive Clock

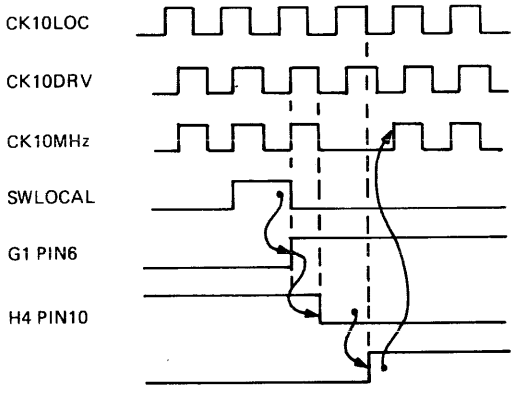


Figure 5-3. Switch to Local Clock

format of a complete track could be destroyed.

DEADSTOP is cleared by pressing the MSTRCLR pushbutton. When the DDEC is not in local, the DEADSTOP flip-flop is held reset by ENABSTOP/ being high.

CLOCKSTOP may be used in remote by jumpering ENABSTOP/ to ground; however, due to the possibility of noise setting the DEADSTOP flip-flop during operation, the jumper should be removed after use.

SECTOR LOCATION COUNTER

The sector location counter is used to control the timing of most of the functions within the DDEC. It consists of a bit counter and a word counter. The bit counter counts bits at the clock speed from 0 to 15, 0 to 15, etc. When a count of 15 is reached, the word counter is counted up. The word counter has a maximum count of 128 words.

Figure 5-4 shows a block diagram of the sector location counter. The bit counter and the word counter are decoded from binary into decimal. These decodes are then combined into gates to give a timing pulse at a certain word and bit time. For example:

W0B0 is high when the counter is at zero. W1B11 is high after 27 counts. W127B12 means word 127 bit 12.

There are several control signals for the sector location counter: CLSECLOC - clear sector location counter. This signal clears the word and bit counter to zero on the next positive edge of the clock pulse. W0B0 is high immediately after this signal. The sector location counter is cleared at the end of most modes.

INSECLOC - increment sector location counter. When this signal is high, the counters are counting. When this signal is low, counting is prevented. The counter retains its count.

LDSECLOC - load sector location counter. When this signal is high, a predetermined value is loaded into the counter. An example of this is when we wish to synchronize the counter with the data arriving from the drive during a READ.

INSLWDRD - increment sector location counter by one word.

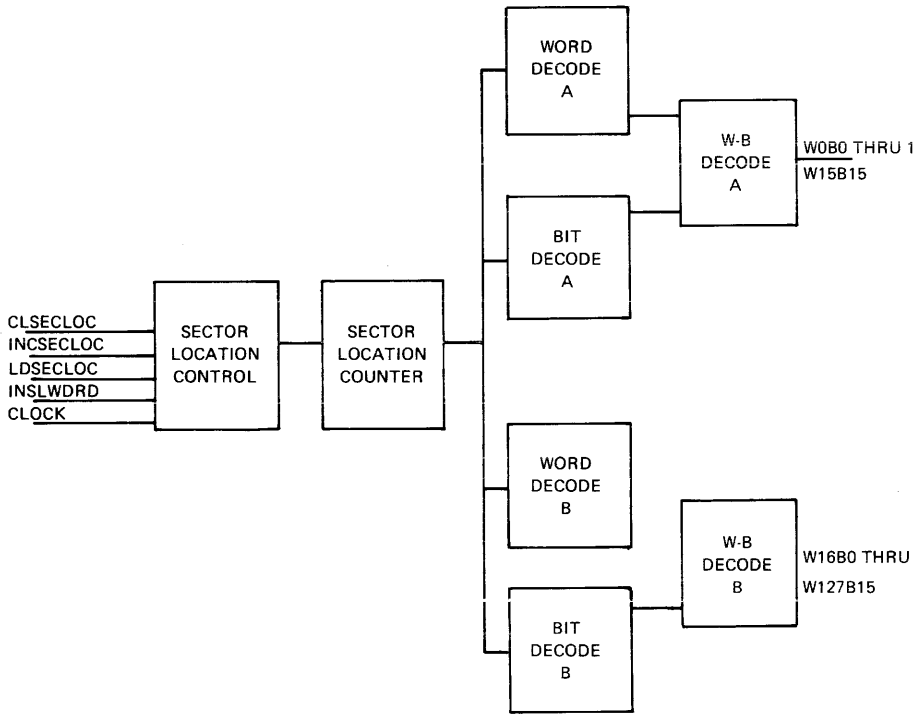


Figure 5-4. Sector Location Counter

The sector location counter takes up two PCBs. Word bits less than W16B0 are generated on card 18. Word bits greater than or equal to W16B0 are generated on card 19, schematics 18 and 19. No further explanation of the sector location counter is given in this manual.

CONTROLLER MESSAGE LOGIC

General Description

The CM logic sends bit serial controller messages to the drive. At various points in the mode flows,

the control logic causes a CM to be sent to the drive. In the flows, these actions are shown as HEADCM, CYLINDERCM, RPUCM, INDEXCM, etc. These are descriptive terms designed to inform the reader of the type of CM sent; there are no signals called HEADCM, CYLINDERCM, and so on. The CM is started by gating the mode, word time, bit time, and any conditions to provide the signal CMLOAD and CMSTART.

Block Diagram

See figure 5-5 for the following discussion.

The CM logic consists of five main blocks:

1) Control logic - this controls the loading of the shift register, the length of the CM, and the shifting of the shift register.
2) Data multiplexors - these control the source of data for the CM. The short CM data multiplexor has two sources: one for a short CM and all highs for a long CM. The long CM data selector has four sources which are selected according to whether the CM is a short CM, a control CM, a head CM or a cylinder CM. In the case of a short CM, the data selected is all lows.
3) Shift register - this is a 24-bit shift register that is loaded parallel with the CM data and shifted out serially to the deskew buffer and parity generator.
4) Parity generator - this generates the mode 2 sum of the CM bits and inserts parity at bit 23 (even).
5) Deskew buffer - in the deskew buffer, the CM is synchronized with the drive clock so that the bits are in the best positions for receiving in the drive.

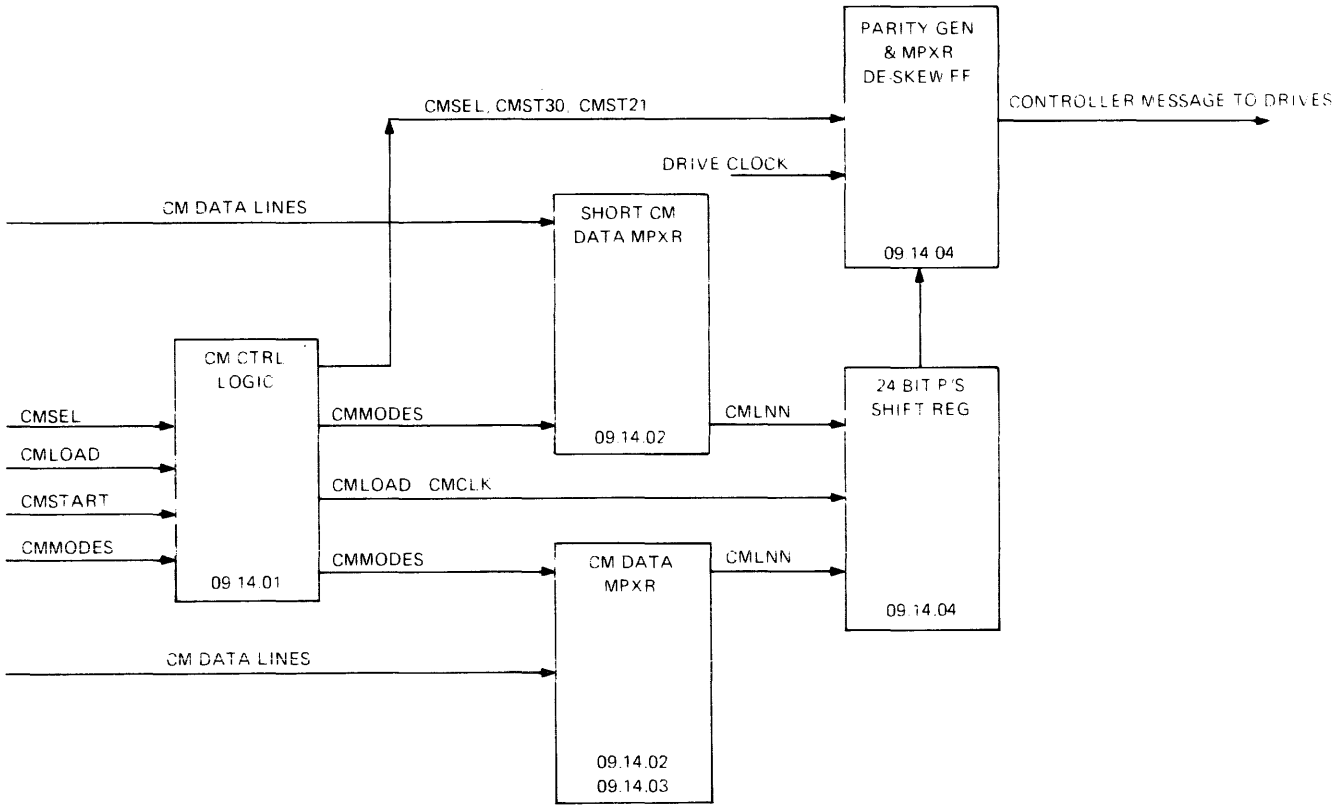


Figure 5-5. CM Logic

CM Sequence

CM Modes

The first action occurs before the CM is sent. The CMMODE signals select the source of data for the CMLNN lines. There are two CMMODE signals: (CMMODE 2* 1 and CMMODE 2* 0). Refer to table 5-1.

The CM modes are controlled mainly by the main modes. For example: modes 2 and 3 are used to send a seek to the drive only; therefore, mode 3 gives CMMODE 3. Control CMs only are required in mode 0; therefore, MODE 0 gives CMMODE 1. The equations for CMMODE 2* 1 and CMMODE 2* 0 are available in the T & F document package.

The CM mode signals control the short CM mul-

tiplexor and the long CM multiplexors.

Table 5-1. CM Modes

2*1	2 * 0	CMMODE	Meaning
0	0	0	Short CM
0	1	1	Control CM
1	0	2	Head CM
1	1	3	Cylinder CM

CM Load

At the appropriate word and bit time of a mode flow, the signal CMLOAD is generated. This pulse loads the output of the data multiplexors into the shift register. It also sets a flip-flop which controls the CM length (schematic 14.01).

On some occasions CMLOAD is prevented by the signal CMENABLE being low, specifically:

1) If the drive is not ready (but not in mode 0).
2) If GOTOMODE15 is active.
3) The check status CM in mode 15 is prevented if a long DM has been sensed or if an offset operation has been performed. This prevents the status from changing and prevents a NOT READY result descriptor if the drive is still not ready from an offset operation.

CMENABLE is true if MODE 0 is true, or if RESTORE is true.

CM Start

CMSTART occurs one clock time after CMLOAD. See the timing diagram in figure 5-6.

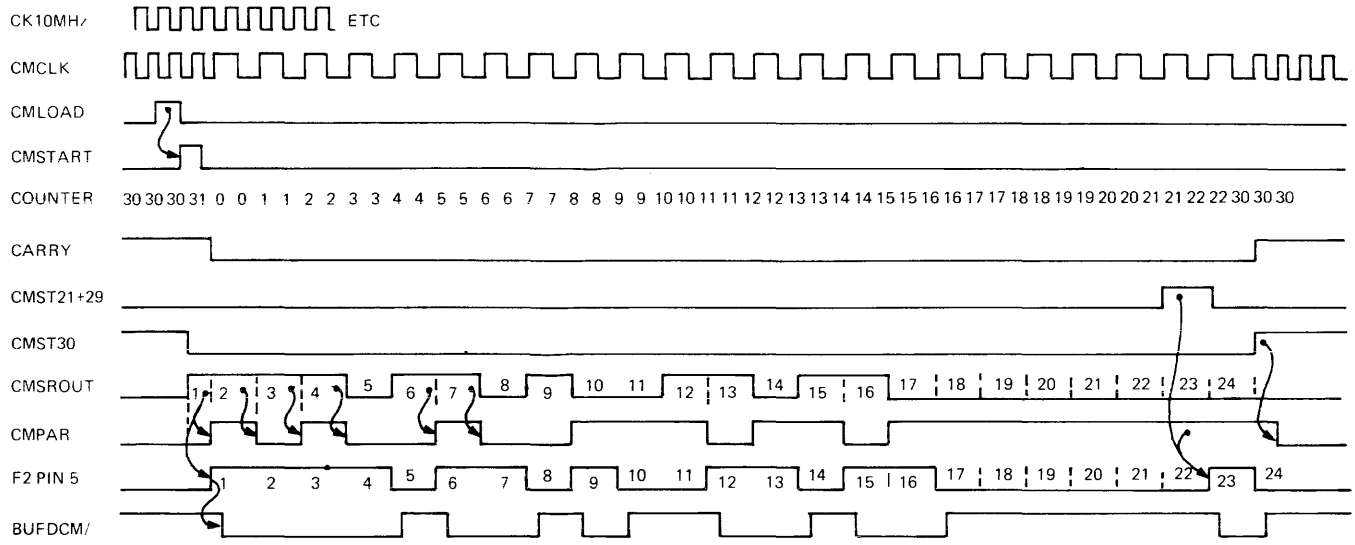


Figure 5-6. Long Controller Message

CMSTART counts the CM state counter from 30 to 31 and starts the counter counting. At a count of 0, the CMCLK is changed from 10MHz to 5MHz. The CMCLK shifts the contents of the shift register one position on the leading edge of each pulse, presenting a bit every two clock times to the deskew buffer and parity generation logic.

When a count of 22 is reached on a long CM or a count of four on a short CM, the counter is loaded to a count of 30. This action halts the counter and switches the CMCLK back to 10 MHz.

Parity

The parity bit 5 is inserted at the short CM multiplexor. CM line 05 is low whenever a long CM is being sent, or whenever an address mark CM is being sent. (An address mark CM always has either a READ bit or a WRITE bit in addition to the address mark bit). CM line 05 is also low during a go idle CM. Short CMs are given in table 5-2.

Table 5-2. Short CMs

Bit Position Name	1 Mark	2 Write	3 Read	4 Address Mark	5 Parity
Read data	H	H	L	H	H
Write Data	H	L	H	H	H
Read ADMK	H	H	L	L	L
Write ADMK	H	L	H	L	L
Go Idle	H	H	H	H	L

Parity bit 23 makes the total number of high bits one to 23 even. If bits one to 22 contain an odd number of high bits, CMPAR is high at CMS21. If

bits one to 22 contain an odd number of high bits, CMPAR is low at CMS21. See figure 5-6. CMPAR flip-flop is complemented every time a high is received from the shift register. At CMST21, if CMPAR is high, a high bit is 'ORed' into the CM.

Deskew Buffer

Deskew is performed through two flip-flops. The first is clocked by CMCLK; this causes bit 1 to be the full 2 clock periods wide. The second flip-flop is clocked by the drive clock. This causes the CM to have the correct relationship with the clock in the drive.

Select

Select is the process of making the CM line high to the drive. The signal causing the select is CMSEL. CMSEL flip-flop is set and reset in mode 0 during the spinup sequence. Also, it is set in mode 1 and remains set until the DDEC completes the operation and goes into IDLE mode.

CMSEL makes BUFDCM/ go high when no CM is in progress. (See schematic 14.04). When CMSEL is low, it prevents the DM status register from being cleared. This is a precaution against losing the status if the drive sends a long DM without being selected. (The drive should not send any DMs unless it is selected).

DRIVE MESSAGE LOGIC

General Description

The drive is permitted to send a serial drive message (DM) only when it is selected. In the DDEC, DMs may only be received if CMSEL (CM Select) is high. The DM logic monitors the DM line for messages. When a DM is received, it converts the data from bit serial into parallel data for use in the DDEC. There are four types of drive messages:

1) ROGERDM - this is a one bit DM sent by the drive acknowledging receipt of a CM without error.
2) Short DM - this is a 6-bit DM which contains the status of the drive and an address or index mark bit.
3) Long DM (status) - this 32-bit DM contains the contents of the drive 24-bit status register as well as the regular status of the drive (on line, ready, etc.).
4) Long DM (CM error) - this 32-bit DM contains the normal drive status bits and also the CM as received in the drive.

For more information on the content of drive messages, refer to section 1.

Block Diagram

See figure 5-7 for the following discussion.

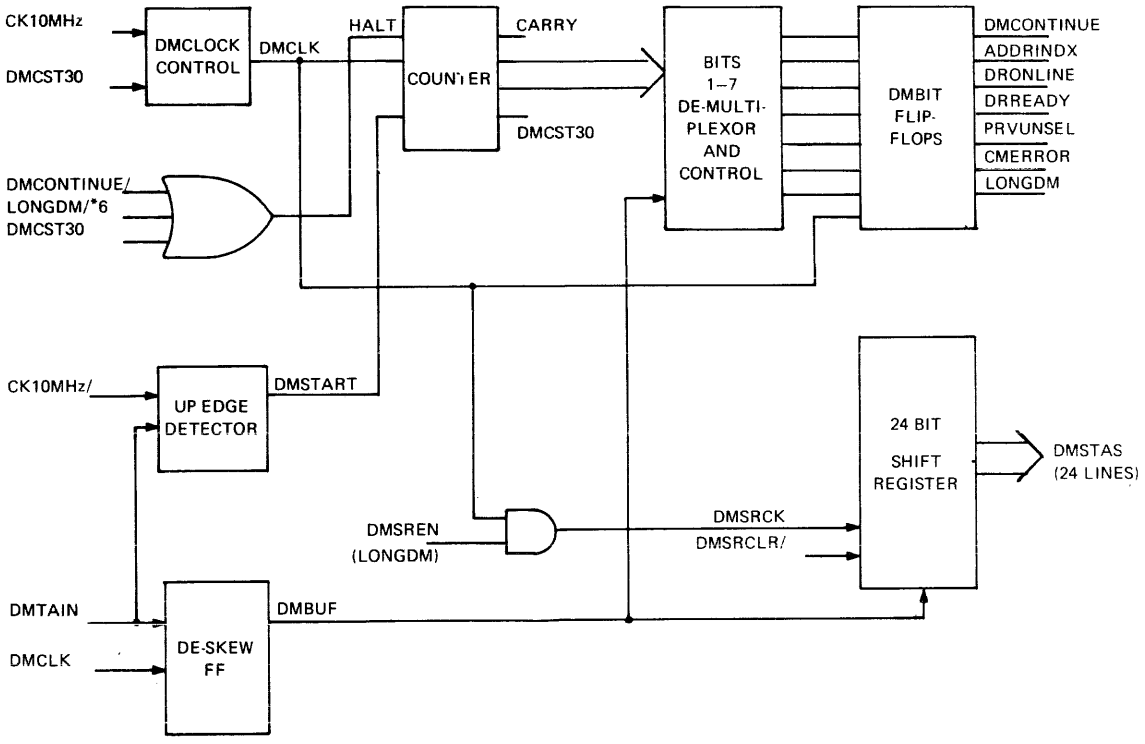


Figure 5-7. Block Diagram DMLOGIG

Up-Edge Detector

The DM logic is started by the mark bit of a DM. The up-edge detector detects a transition from low to high on DMDTAIN. It gives a single pulse (DM START) on each up-edge; however, only the first pulse is significant.

Counter

The DM state counter stays at a count of 30 when a DM is not being received. When DMSTART occurs the counter is permitted to start counting. The counter provides timing pulses at certain bit times. The signal DMCNTHLT (DM counter halt) preloads the counter to 30. When the counter is at 30 it cannot count unless DMSTART occurs.

DM Clock Control

The DM clock control determines the rate of DMCLK. When a DM is not in progress, DMCST 30 (DM counter state 30) is high, and the clock speed is 10 MHz. When a DM starts, the counter counts out of state 30, and the clock speed changes to 5 MHz. This is required because the bit rate of a DM is 4 MHz.

Deskew Buffer

The deskew buffer is a flip-flop clocked by DMCLK with DMDTAIN on the data input. The positive transition of DMCLK occurs in the center of the DM bit; therefore, any skew caused by cable lengths, and so forth, is removed. The output of the deskew buffer is DMBUF (DMBUFFERED).

Bits 1-7 De-Multiplexor

The de-multiplexor is controlled by the counter output bits 1, 2, and 4. It directs each bit to the relevant DM bit flip-flops. Example: Bit 2 goes to DMCONTINUE flip-flop, bit 3 goes to ADDRINDX flip-flop, etc. Bit 1 (mark) is dropped off because the counter is at 31 at this time.

DM Bit Flip-Flops

These flip-flops receive the latest status of the drive selected. They go mainly to the control logic where they influence the mode flows. If the drive is deselected, all the flip-flops are set. Since all the flip-flops are inverted, all the status bits are false. (low).

24-Bit Shift Register

If bit 8 is high, this indicates that the DM is long. The remaining 24 bits are shifted into the 24-bit shift register where they are kept for use in an ERD operation.

DM Sequence

Roger DM

See figure 5-8 for the following discussion.

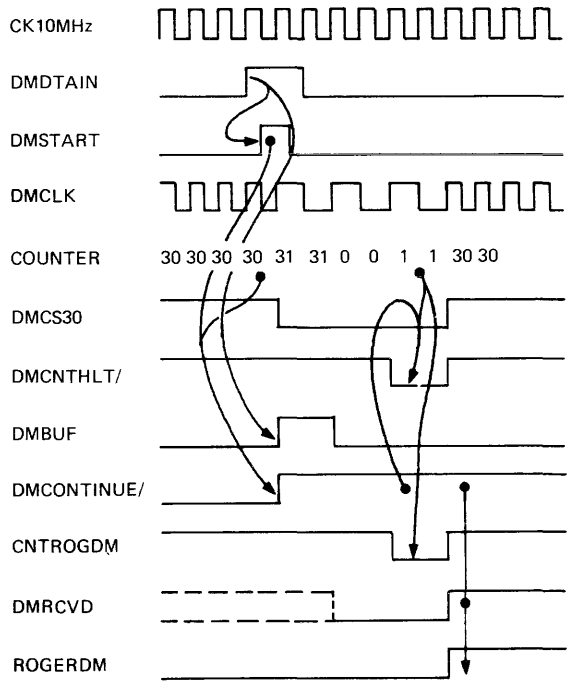


Figure 5-8. ROGER DM (1 Bit)

DMDTAIN gives DMSTART through the up-edge detector. DMSTART causes the counter to start counting. It also causes DMCONTINUE/ to go high by setting the DMCONTINUE/ flip-flop. DMBUF follows DMDTAIN by one clock.

At a count of 0, DMBUF is low. Through the de-multiplexor, this low is inverted to a high on the K/ input to the DMCONTINUE/ flip-flop.

With DMCONTINUE/ high at a count of 1, DMCNTHLT/ is low and CNTROGDM is low. DMCNTHT causes the counter to preload to 30 on the next DMCLK. CNTROGDM causes DMRCVD (DM received) to go high on the next clock. DMCONTINUE/ and DMRCVD give the signal ROGERDM.

This informs the control logic that a DM has been received, and that it is a ROGERDM.

Short DM

See figure 5-9 for the following discussion.

The leading edge of DMDTAIN causes DMSTART. DMSTART starts the DM state counter counting and sets the following DM bit flip-flops:

LONGDM/, PRVUNSEL/, DMCONTINUE/, and ADDRINDX.

When the counter is not in state 30, i.e., as soon as it counts to 31, DMCLK changes to 5 MHz. DMBUF follows DMDTAIN by one clock period (100 nanoseconds).

DMBUF goes to the de-multiplexor, where each bit is directed to the appropriate flip-flop.

If bit 8 is low, indicating a short DM, the long DM/ flip-flop remains set. At a count of 7, with LONGDM/ high, DMCNTHLT/ goes low. On the next DMCLK the counter is preset at 30. CNTSHTDM/ is also low at the same time. This signal sets DMRCVD.

Long DM

See figure 5-10 for the following discussion.

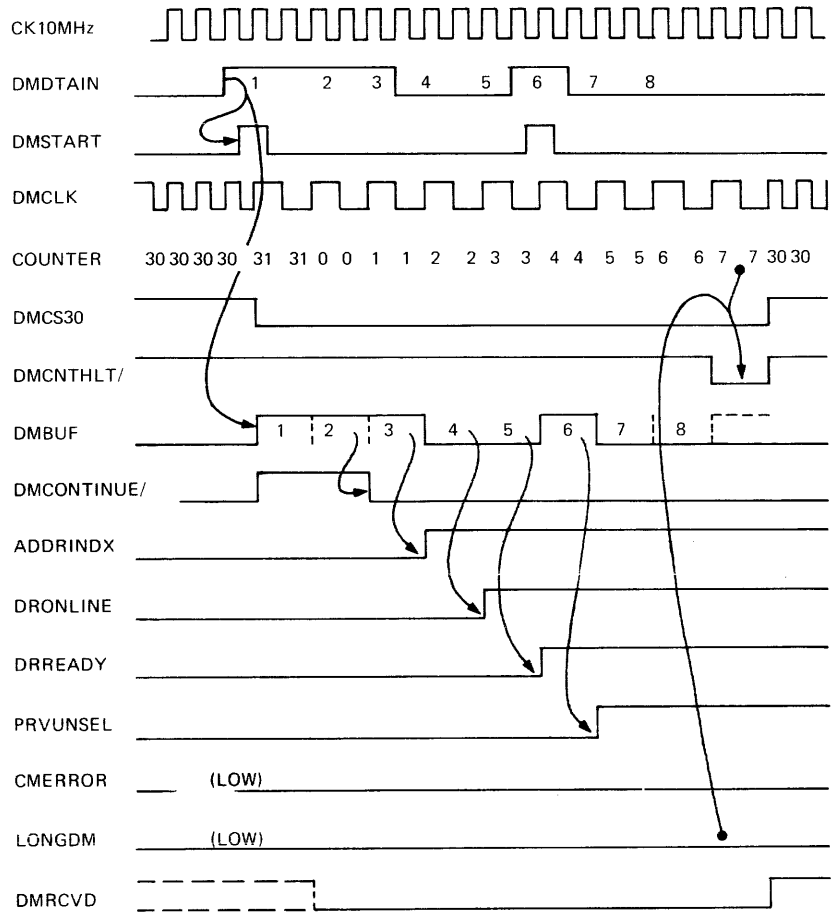


Figure 5-9. Short DM (6 Bit)

The first seven bits of a long DM are received in the same manner as a short DM. On a long Dm, bit 8 is high . At a count of 6, with CMBUF high, DMSRFFK/ is low (DM shift register K/ input). This signal resets long DM/ flip-flop and resets the DMSRENB/ flip-flop (giving LONG DM and DMSRENB).

DMSRENB (DM shift register enable) permits DMSRCK (DM shift register clocks) to occur. These clock pulses clock the remaining 24 bits of the CM into the DM shift register. When the counter reaches 30, it halts. DMSRENB/ flip-flop sets on the next clock causing DMSRENB to go low, thus preventing any further DMSRCKS. A count of 30 and DMSRENB sets DMRCVD.

Drive Ready

The DRREADY/ flip-flop is updated to show the status of the drive on every Short or Long DM/. However, at certain times the DRREADY/ flip-flop is preset to show DRREADY/.

1) In mode 1, W5B1 and the drive is not on line, the signal STBLKRDY sets a flip-flop which sets the DRREADY/ flip-flop. This prevents a result descriptor containing offline and ready during a test OP.
2) In mode 3, W9B15, a cylinder CM has been sent to the drive. FCDRRDY/ sets the DRREADY flip-flop so that a not ready bit ap-

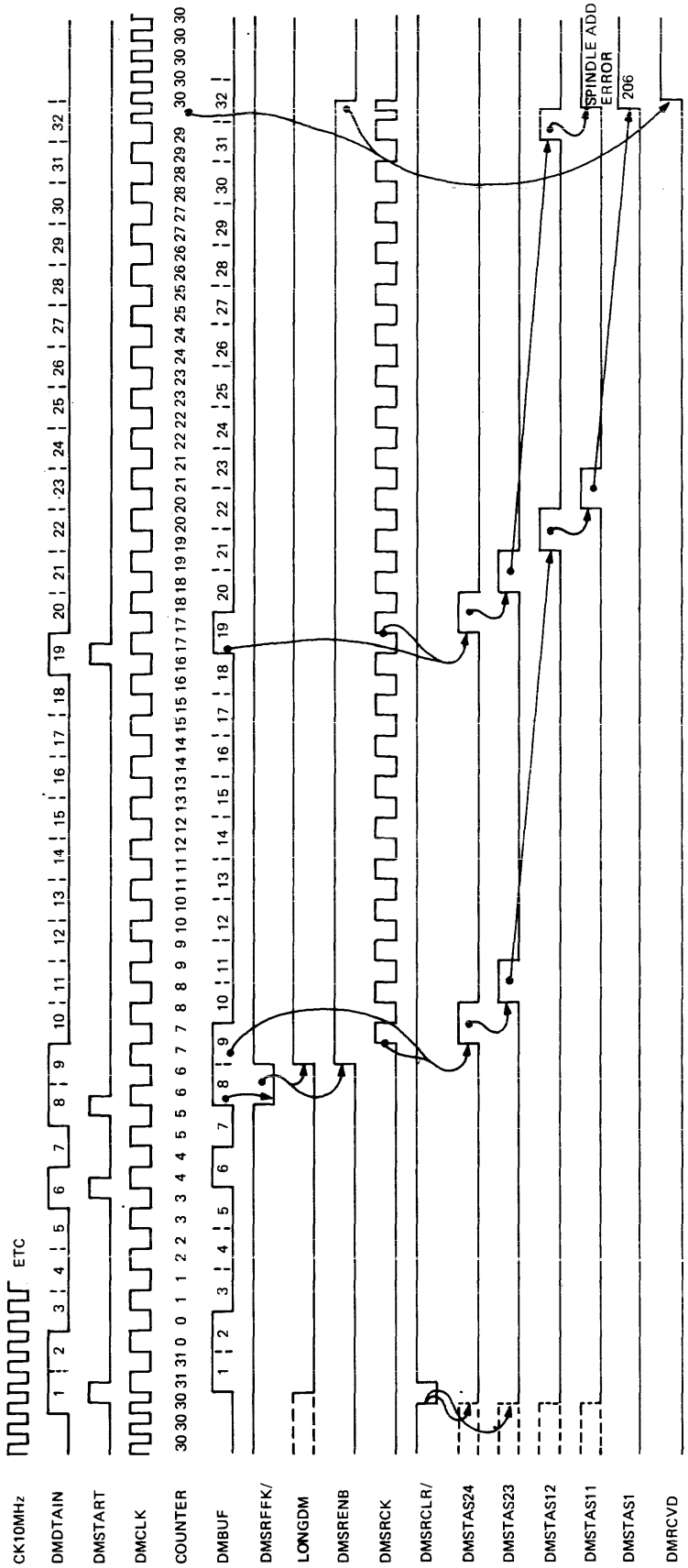


Figure 5-10. Long DM (32 Bits)

pears in the result descriptor. This is a duplicate action because the drive should have returned a short CM containing a not ready indication in response to the cylinder CM.

When a cylinder CM is sent to the drive, the drive immediately returns a short DM containing NOT READY. When the drive completes the seek, it sends back a ROGERDM. DRREADY/ flip-flop, therefore, is reset if bit 2 of DMBUF is low. This causes DRREADY to go high when a ROGERDM is received.

ERROR LOGIC

There are two error signals which cause the TD bit to be set in the result descriptor:

1) DPECEXF (DDEC) exception).
2) DMEXCPT (DM exception).

The equations for these two signals are given below.

DPEC Exception

```
DPECEXF = FANFAIL
+ TESTOP/* (ADOVFLAG+DRIVCKOK/*ENCKTEST)
+ REVSDONE*PBNOHALT/*(STUKDATA + ADMRKER)
```

FANFAIL - failure of the fan or fan switch.

ADOVFLAG - illegal cylinder decoded in the DDEC from the address supplied by the DPC.

DRIVCKOK - 3-1/2 bit time drop-out on CK10DRV.

ENCKTEST - whenever the drive clock is being used. It is set by SWTODR and reset by IDLE.

REVSDONE - failure to find address coincidence on the surface selected and in the spare sectors.

PBNOHALT/ - this signal is normally high. It may only be low during local operation with the NO HALT switch active.

STUKDATA - no transitions on SERDTAIN

ADMRKER - the 250 usec timeout on 206. On the 207, is set if an address mark is not returned within 124 words and 12 bits from the read address mark CM.

DM Exception

```
DMEXCPT = DMERDFF1* DMERDFF2
*(TEMP WARNING + BADDMRSP + MODE 15/*(LONGDM
+ INDXMRKR*ADMRKER*207)
```

DMERDFF1*DMERDFF2 - control the timing of the DM exception pulse. See figure 5-11. FF1 and FF2 occurs after the long DM has been stored but before the temperature warning bit is written into its memory.

TEMP WARNING - only gives DMEXCPT if the previous long DM does not have a temp warning bit on, i.e., a temperature warning bit only causes a DM exception the first time it comes on.

BADDMRSP - bad DM response. This comes from a number of sources:

1) The drive is expected to go NOT READY at certain times, i.e., after a seek and after a head switch on the 207. If it does not, BADDMRSP is true.
2) No ROGERDM received within 65 ms of a CM.
3) No ROGERDM received within 2 words and 3 bits of a READ address mark CM in mode 5 or mode 9.

LONG DM - the exception bit on in a long DM (bit 8).

INDXMRKR - an index pulse not returned within 25 MS of a check index CM.

ADMRKER*207 - address mark errors are not permitted on the 207. An address mark error indicates that the drive has made an error in the servo circuit.

Each of these errors is reported in the ERD as well as causing the TD bit to occur in the result descriptor.

Temperature Warning

Due to the time required for the drive to heat and cool, temperature warning could be on for a significant time. In order to prevent unnecessary send ERD operations, the TD bit is only set on the first time the DM contains temperature warning. To accomplish this, a 1-bit memory is provided for each unit to store the previous temperature warning bit.

See figure 5-11 for the following discussion.

When a long DM is being received, DMSRENB is true. When the DM is complete, DMSRENB goes low and FF2 is set. At this time, the temperature warning bit (DMSTAS22) is compared to the previous bit stored in the memory. If the new bit is on and the memory output is high (indicating that the previous temperature warning is low), DMEXCPT is true.

One clock later, FF1 resets and the new temperature warning bit is written into memory in readiness for the next comparison.

RESULT DESCRIPTOR LOGIC

General Description

At the end of each operation, a 16-bit result descriptor is returned to the DPC, informing the DPC of any errors or exceptions that occurred during the operation.

See figure 5-12. The result descriptor buffer consists of a 16-bit tristate buffer which is placed on the data bus by RESDESEN. The status input to the buffers comes from various flip-flops in other sections of the unit.

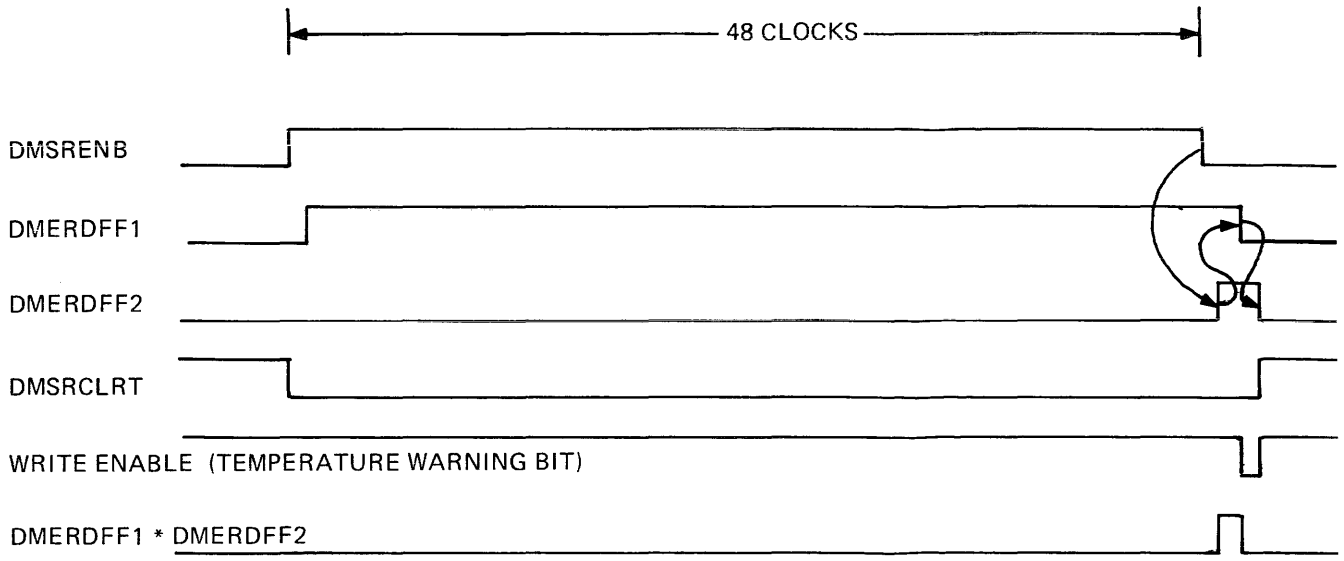


Figure 5-11. DMERD Flip-Flops

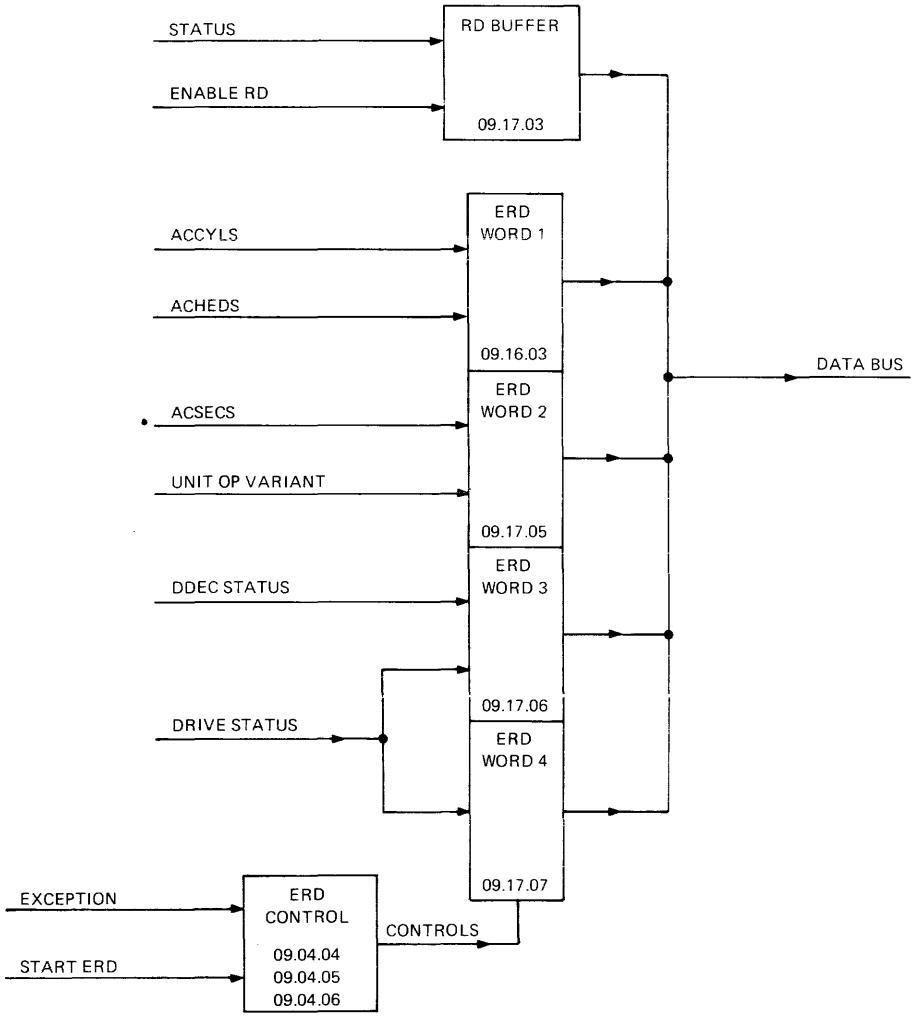


Figure 5-12. RD and ERD LOGIC

For more information on result descriptors, refer to:

Section 1 for the meaning of the bits.
Section 2 for mode 15 flow.
Section 4 for the format logic timing.

EXTENDED RESULT DESCRIPTOR LOGIC

General Description

The extended result descriptor provides additional information about the type of operation performed and the errors occurring during the operation. The ERD consists of four 16-bit words containing:

1) Address decode information.
2) OP code, unit and variants received from DPC.
3) DDEC detected errors.
4) Drive detected errors.

Refer to table 1-9 if details of the bits are required. The ERD may be looked at as two phases:

1) Loading the ERD information.
2) Sending the ERD to the DPC as the result of a SENDERD operation.

Loading the ERD Information

Words 1 and 2 are loaded in mode 1 on every operation except SENDERD. At W4B7, the signal STROBADR loads the decoded address, OP Codes, and variants into the word 1 and 2 buffers.

The DDEC detected errors are loaded into the appropriate bits by the signal ERDXFREN/ (ERD TRANSFER ENABLE).

The DM status register is loaded into words 3 and 4 only if the signal DMEXCPT is true. DMEXCEPT is true in the following instances:

1) Mode 15/* (long DM + index mark error).
2) Bad DM response.
3) On a new temperature warning bit.

ERD Control Logic

See figures 5-13 and 5-14 for the following discussion.

The ERD control logic contains a counter having eight states. For this description, the states are numbered 0 through 7. State 0 is the normal state of operation; the unit may perform all operations in this state. On each operation the ERD words 1 and 2 are loaded as previously described. If a DDEC exception or a DM exception occur, the other words of ERD are loaded and the counter goes to state 1.

In state 1, the signal ERDXFREN goes false. This prevents any further loading of information into the ERD register. This "locks" in the ERD data. Also in state 1, TRY DIAGNOSTICS is true. TRY DIAGNOSTICS causes every operation attempted to go from mode 1 to mode 15 and terminate (except TESTOP and READ ERD). The TD bit is returned in the result descriptor to the system. The system must recognize this bit and respond with a READ ERD operation.

When the READ ERD operation is received, the control logic goes to mode 13, and the signal STERDOUT (start ERD out) is generated. The counter is counted to state 2. In this state, word 1 is placed on the data bus. The format logic generates the CLOCK DPC to transfer it to the DPC and count to state 3.

In state 3, word 2 goes to the DPC. In state 4 and 5, words 3 and 4 are sent to the DPC.

With FFB reset, the clock to the counter is switched to 10 MHz, and the counter counts back to zero.

In state 7, the signal ERDCLR clears the ERD registers ready for the next ERD.

MAINTENANCE LOGIC

General Description

The purpose of the maintenance logic is to simulate a disk pack control, interfacing with the DDEC at the normal DPC rate.

The maintenance logic permits the Field Engineer to enter one or two complete INITIATE commands and to execute them singly, continuously, or alternately. Variations to the operation may be introduced, such as single sector, loop head, and so on, by switches.

Also, the Field Engineer has access to result descriptor information, extended result descriptor information, and firecode information through the LED display.

See the block diagram in figure 5-15. The principal components of the maintenance logic are listed below.

Sixteen-Word Read Write Memory

This is a 16-word memory with 16 bits per word. It is used to store information entered through the data input keyboard. It also stores firecode information and extended result descriptor information. The words are addressed from 0 through 15. Table 5-3 shows the use of each word.

Data Input Keyboard

This consists of 16 push-button switches situated on the right hand side of the maintenance panel. (See figure 5-16). These switches are used to enter the INITIATE words and data into memory prior to performing an operation. Data entered by pressing an input switch is latched into the switch bus register.

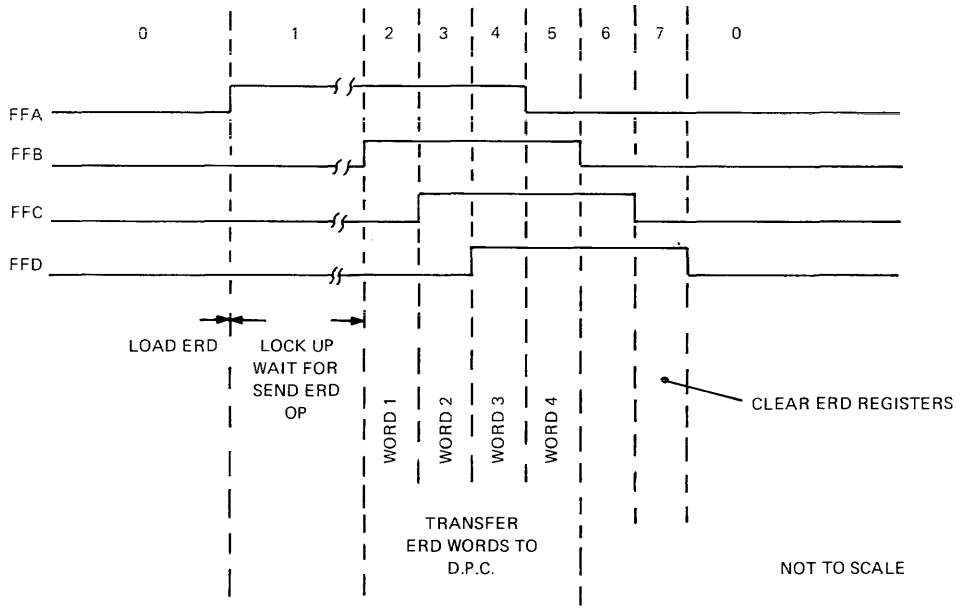


Figure 5-13. ERD Control Counter

The data input keyboard is only enabled when the unit is in LOCAL. The signal MNTSWEN/ is low only if the unit is in IDLE and LOCAL.

Switch Bus Register

The switch bus register consists of 16 set/reset latches. The entire register is cleared by pressing the CLEAR push button. The bits are set from two sources:

1) From the data input keyboard.
2) From the data bus.

The switch bus register is the input to the memory; therefore, ERD information and firecode information are inputted from the data bus via the switch bus register into memory. Additionally, at the end of each operation, the result descriptor is latched into the switch bus register for display, but is not written into memory.

Switch Bus Display Drivers and LEDs

The 16-bit display is driven by the register and drivers. The following information may be displayed:

1) Data input from the keyboard.
The contents of any memory word.
The result description from any operation.

Switch Bus Buffers

The switch bus buffers (16) interface the data bus to the switch bus register. They consist of tri-state buffers enabled (when required) by the signal SWBUSEN/.

Memory Address Display

The memory address display displays the memory address in binary. It also displays the binary DDEC "mode" when the ENSTP switch is in the down position.

Table 5-3. Maintenance Memory Word Usage

Word	Description
0	Initiate Word 1 - first OP.
1	Initiate word 2 - first OP.
2	Data word - first OP.
3	ERD word 1 or 16 bits firecode on an alternate OP.
4	ERD word 2 or 16 bits firecode on an alternate OP.
5	ERD word 3.
6	ERD word 4.
7	Not used.
8	Initiate word 1 - second OP.
9	Initiate word 2 - second OP.
10	Data word - second OP.
11	16 bits firecode on an alternate OP.
12	16 bits firecode on an alternate OP.
13	Not used.
14	Not used.
15	Not used.

Control Keys and Switches

General Description

The control keys and switches control the operation of the DDEC in local. When the DDEC is in remote, all the switches are disabled so that if any switch is pressed, the operation of the unit is not interfered with.

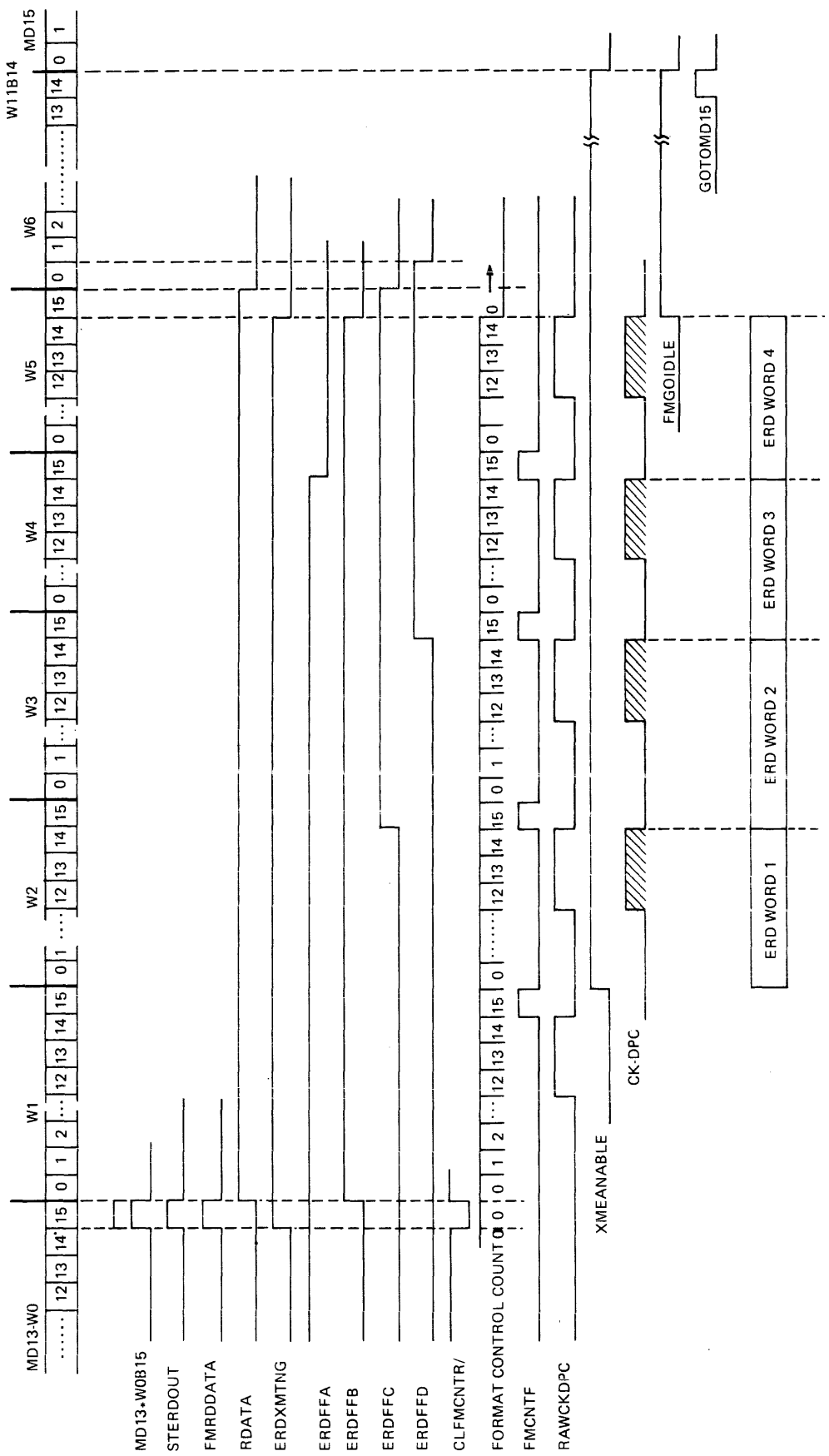


Figure 5-14. Read ERD Timing

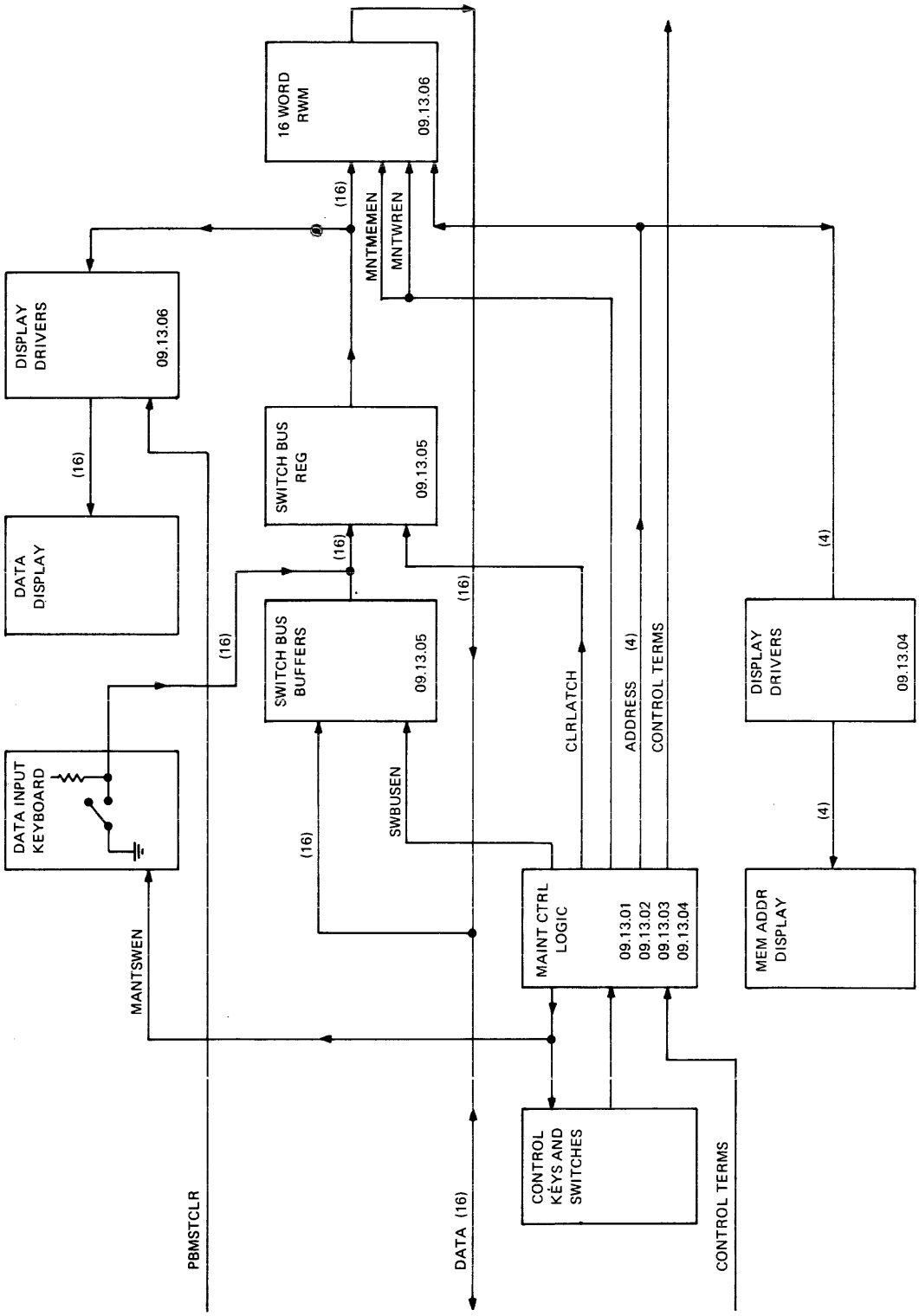


Figure 5-15. Maintenance Logic

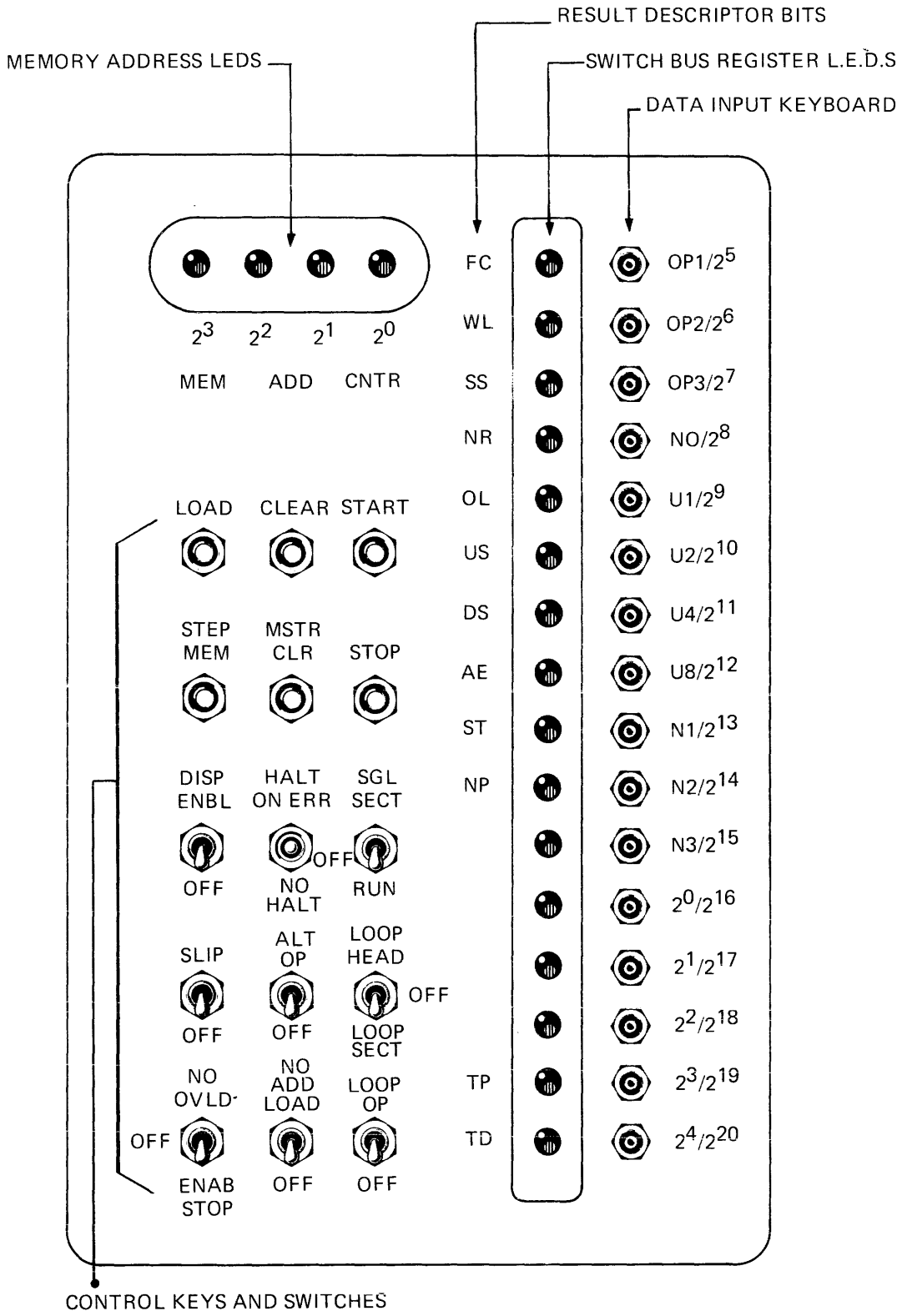


Figure 5-16. Maintenance Panel

There is one exception to this: In mode 0 W1, the switches are enabled. By pressing master clear pushbutton switch during the spin-up sequence, the operation may be forced to IDLE (mode 1 W0). This could save waiting eight seconds for each spindle to sequence up by by passing the spin-up sequence.

In order to reduce the effects of switch bounce, critical switches and push buttons are fed into RS latches.

Listed below are the control keys and switches for the DDEC in local.

Single Sector/Run

Perform one sector operation, and then terminate (single sector position). Perform multiple sector operation until the end of pack, and then terminate (RUN position).

Loop Head/Off/Loop Sector

This is a three position switch. Loophead causes a full track READ, WRITE, INITIALIZE, or VERIFY continuously on the same track. Loop sector causes a single sector continuous loop on READ, WRITE, or VERIFY.

Loop OP

This switch causes the operation to be restarted at the termination of the previous operation.

Halt on Error/Off/No Halt

Halt on error causes the OP to terminate if a firecode error is detected or if a data sync error is detected.

In the OFF position, the unit terminates on address errors and ignores firecode errors.

In the NO HALT position, the unit ignores address errors and firecode errors.

Alternate OPs

Alternate OPs allows two areas of maintenance memory to be used alternately as the source of initiate information. Typical use might be:

1) Alternate seeks for servo checking.
2) Write pack, read pack for data checking.

No Address Load

If halt on error is ON, the unit terminates on a firecode error displaying an address one sector beyond the sector containing the error. If START is depressed with NO ADDRESS LOAD on, the operation continues from the displayed address. This is accomplished by preventing the signal LOAD ADDRESS COUNTER (LOAD AC) at the end of address decode.

If NO ADDRESS LOAD is not on, the operation restarts from the address contained in memory.

Display Enable/Off

Display Enable has the following functions when OFF:

1) CLEAR resets the memory address to zero.
2) Step memory does not function.

Slip

This switch simulates the effect of the EXECUTE LINE going low during a processor operation. It suspends the transfer of data for the time that slip is on and resumes the operation when slip is OFF.

No Overlap/Off/Enab Stop

No Overlap disables the overlap seek function. With this switch on, a seek to a new cylinder does not result in a NOT READY result descriptor.

Enab stop enables the stop clock feature.

Master Clear

This pushbutton causes a MAINCLEAR to the rest of the DDEC forcing it to idle.

Clear

Clear clears the switch bus register.

Step Mem

When DISPLAY ENABLE is on, step mem advances the memory address. The contents of the memory is displayed on the vertical LEDs.

Load

Load writes the data in the switch bus register into the memory and steps the memory address to the next address.

Start

Start starts the operation.

Stop

Stop terminates the operation at the end of a sector.

Loading Sequence

When the unit is in LOCAL and in IDLE mode, the signal MNTSWEN/ is at ground level. This signal provides a low level for the signals SW00/ through SW15/. Pressing any data input switch causes a low level to set the switch bus register bits.

Pressing the load push button causes the following events to occur. (See figure 5-17).

1) MNTCK1A and MNTCK1B are generated by one-shots.
2) MNTCK1A and LOAD give MNTMEMEM/ and MNTWREN (maintenance write enable).

This causes the content of the switch bus register to be written into the memory addressed.

3) MNTCK1B and LOAD give CLRLATCH/ which clears the switch bus register.
4) MNTCK1B and LOAD Gives CKCLRADR/. This signal counts the memory address up by one in preparation for the next LOAD.

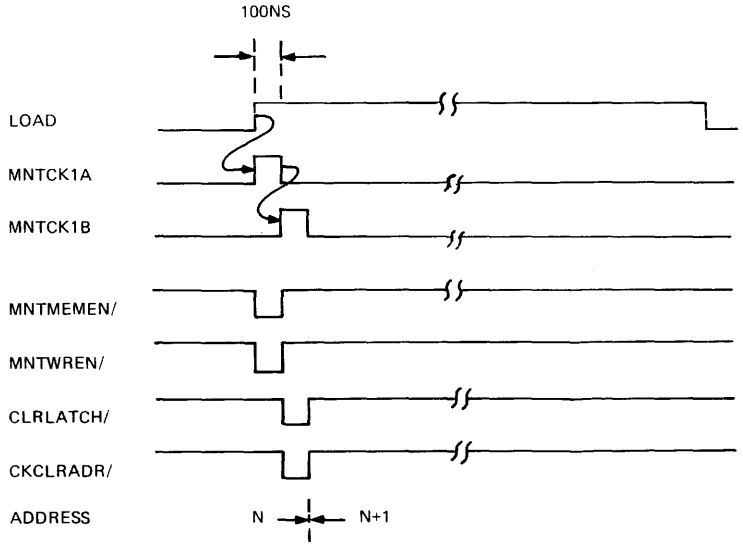


Figure 5-17. Load Maintenance Memory

Display Sequence

The contents of the maintenance memory may be displayed one word at a time. The DISPLAYENABLE switch must be ON. Depression of the STEPMEM pushbutton switch advances the memory address and displays the next word. (See figure 5-18).

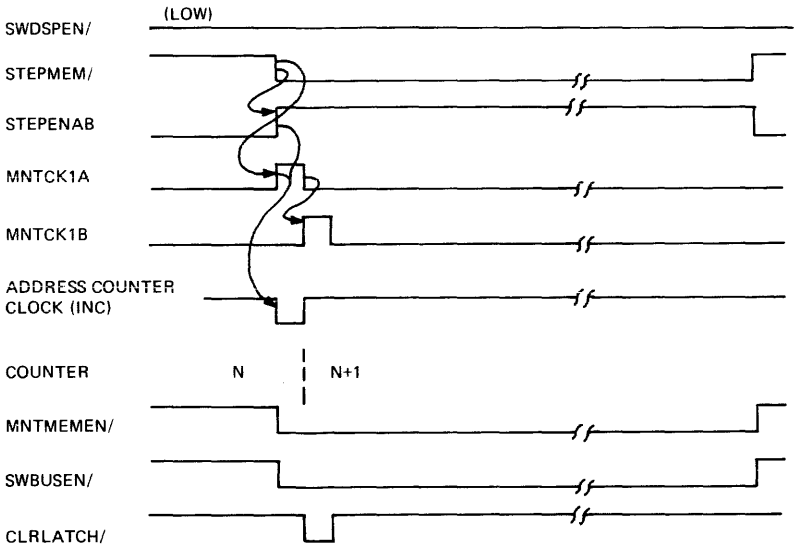


Figure 5-18. Display Sequence

When STEPMEM/ goes low, the one-shot clocks are triggered. STEPMEM/ and SWDSPEN/ (switch display enable) are ANDed to give STEPENAB. MNTCK1A and STEPENAB provide a clock to the memory address counter, incrementing it one word. STEPENAB also gives MNTMEMEN. This signal

enables the memory output, placing the contents of the memory on to the data bus. STEPENAB also gives SWBUSEN. SWBUSEN permits the data bus through the SWITCH BUS BUFFERS to latch into the SWITCH BUS REGISTER. The LEDs display the contents of the switch bus register.

MNTCK1B clears the switch bus register before the new data is latched in. (Refer to CLRLATCH/).

Start Sequence

After loading an initiate word into memory, the operation is started by pressing the start push button. Figure 5-19 shows the start sequence.

PBSTART gives STRTLTCH (start latch). STRTLTCH triggers the clock one-shots giving two 100 Nsec pulses, MNTCK1A and MNTCK1B. MNTCK1A clears the memory address to zero. The trailing edge of MNTCK1B sets MNTSEL (maintenance select). MNTSEL resets STRTLTCH.

MNTSEL is equivalent to the SELECT line being raised by the DPC. The signal SELECT goes true in the DDEC approximately 200 nanoseconds after MNSTEL. SELECT starts the mode 1 initiate flow in the DDEC. Also, MNTMEMEN (maintenance memory enable) goes high placing the first initiate word on the data bus. At W0B11, the first initiate word is clocked into the OP, UNIT, and Variant registers and address latches.

CKDPC occurs at W0 bits 12 through 14. CKDPC triggers the maintenance clock one-shots. MNTCK1A counts up the memory address so that the second initiate word is on the data bus.

At W1B11, ADCLOCK clocks the second initiate word into the address decode circuit. At W1B12, CKDPC fires the one-shots again. MNTCK1A counts the address to 2. Address 2 contains a data word for WRITE, INITIALIZE, or RELOCATE.

At W2B0, BUSY goes high. If the operation is a WRITE or INITIALIZE with processor data or a RELOCATE with processor data, MNTMEMEN is kept high. On any other operation, MNTMEMEN goes low.

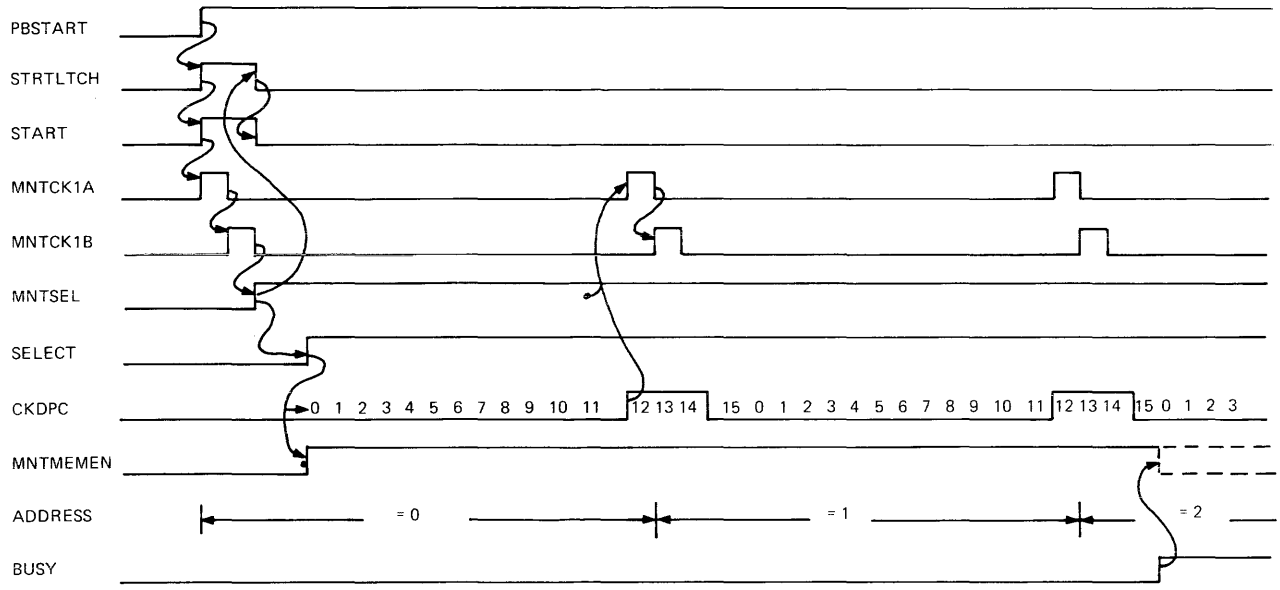


Figure 5-19. Start Sequence

The DDEC has received the command in a similar manner as from a DPC and continues to perform the operation received.

Stop Sequence

The DDEC operation is terminated by the signal MNTDESEL/ (Maintenance deselect). This signal is equivalent to SELECT from the DPC. It causes the DDEC flow to go to mode 15 from certain modes to terminate and send a result descriptor.

MNTDESEL/ is given by the following conditions:

1) STOP (stop pushbutton).
2) PBHALTER (halt on error), FIRCDERR (firecode error), and RESDESEN (end of the sector).
3) SGLSECTR* ENSCXFR* MODE 6 (end of a single sector operation).
4) If the flow is in mode 15 to terminate CKDPC*MNTRDEN*MODE 15.

MNTDESEL/ causes the MNTSEL FF to reset. MNTSEL/ goes to the DDEC to deselect it. It also enables the load and start latches and the restart flip-flop.

Loop OP

Loop OP/ is low when the switch is on. This enables the operation to restart. When the unit reverts to IDLE, IDLE clocks the restart flip-flop. If Loop OP is on, the START signal is generated. (See Start Sequence).

A restart is inhibited under three conditions:

1) STOP is high (stop pushbutton).
2) MAINCLR is high.
3) PBHALTER (halt on error) and a firecode error, data sync error address error.

Result Descriptor Display

See figure 5-20 for the following discussion.

At the end of each operation (in local or remote), the result descriptor is displayed in the LEDs.

In mode 15, when the signal FMSENDRD (format send result descriptor) occurs, the signal MNTRDEN occurs. At this time, the format logic places the result descriptor information on the data bus in the normal manner. The CKDPC which occurs to transfer the data gives the signal TRCKDPC to the the maintenance logic.

TRCKDPC fires the one-shot clocks, generating MNTCK1A and MNTCK1B. MNTCK1A and CKDPC gives a CLRLATCH/ signal which clears the switch bus register, ready to receive new information.

TRCKDPC also gives SWBUSEN which allows the result descriptor information through the switch bus buffers to latch into the switch bus register. The LEDs display the content of the switch bus register which now contains the result descriptor.

Alternate Operations

The ALT OP switch enables two separate operations to be performed alternately. The first OP is stored in location 0, and the second OP is stored in location 8.

Pressing the CLEAR switch ensures that the first operation starts from location 0.

At the start of the first operation, TRCKDPC causes a flip-flop to be set. When the signal START occurs, the memory address counter is loaded to a value of 8. Therefore, the initiate information is loaded from 8 and 9 instead of 0 and 1.

At the end of the second operation, the flip-flop is reset. When the signal START next occurs, the memory address is cleared to zero.

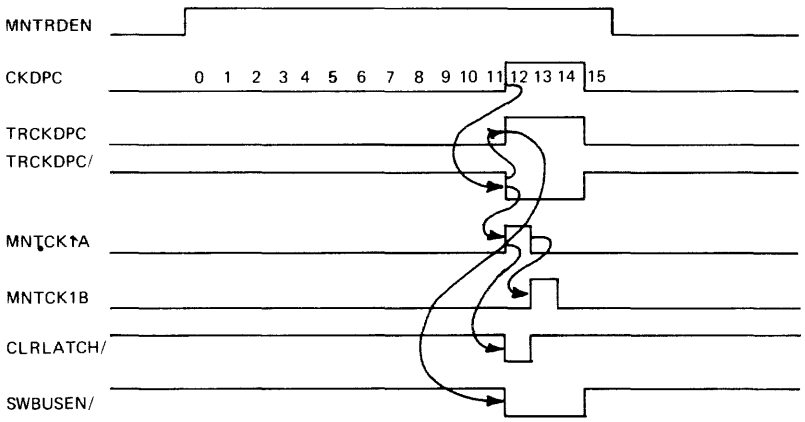


Figure 5-20. Result Descriptor Display

Firecode Storage

See figure 5-21 for the following discussion.

The ALT OP switch also enables firecode storage. (Refer to table 5-3). Firecode is stored for the first sector read only for each operation.

The operation starts in the normal way and continues until the signal FIREONBS/ (firecode on data bus) goes low. This causes MFIRCDEN which in turn gives SWBUSEN/. SWBUSEN/ allows the first word of firecode data to pass through the switch bus buffers to the switch bus registers.

When CKDPC occurs, MNTCK1A and 1B are developed. MNTCK1A gives CLRLATCH/ which clears the switch bus register. When CLRLATCH/ goes high, the data is latched into the switch bus register.

MNTCK1A also develops CKCLRADR/ which counts the memory address from 2 to 3. MNTCK1B develops MNTWREN/ which writes the firecode information into address 3.

Similarly, the next CKDPC causes the next word of firecode information to be written into address 4.

When FIREONBS/ goes high, it sets a flip-flop which inhibits firecode from other sectors read on the same operation from being written into memory.

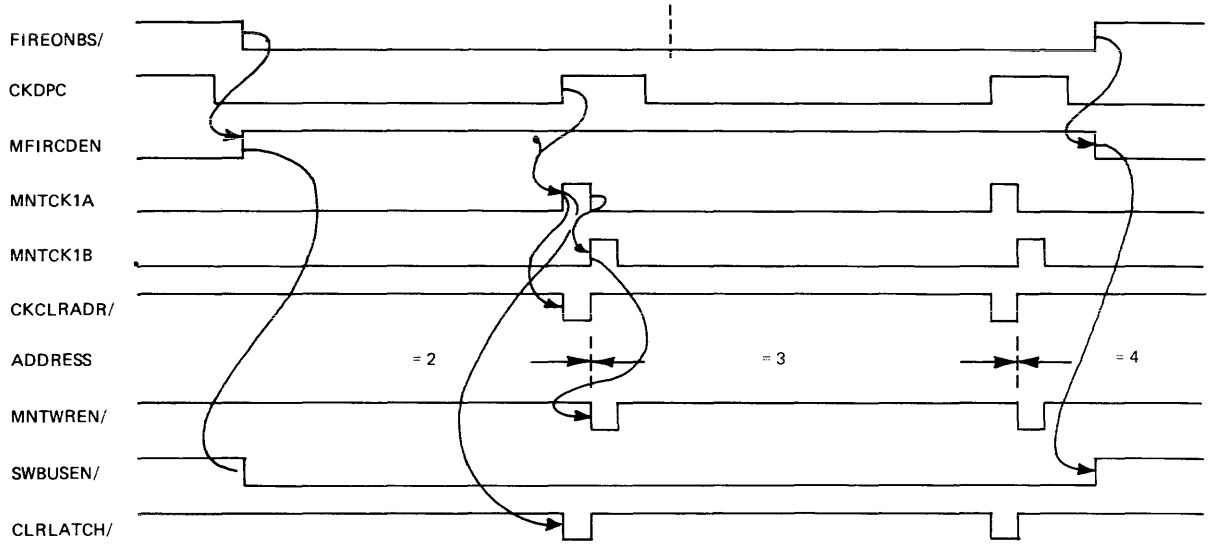


Figure 5-21. Firecode Storage

Send Extended Result Descriptor OP

See figure 5-22 for the following discussion.

When a send ERD operation is performed in local, the ERD is written into words 3, 4, 5, and 6 of the maintenance memory.

During the execution of the send ERD operation, the flow goes to mode 13, where the signal STERDOUT (start ERD out) occurs. This initiates the ERD operation, placing each ERD word onto the data bus and generating a CKDPC.

The maintenance logic receives the signal ERDXMTNG (ERD transmitting) during this time. ERDXMTNG gives SWBUSEN/ to permit the data bus to the switch bus register.

When word 1 is on the data bus, the signal MNERDW1/ is received. This signal loads the address counter to three, ready for writing the first word.

CKDPC generates MNTCK1A and 1B. 1A gives CLRLATCH/ which clears the switch bus register. The new information loads as soon as CLRLATCH/ goes high. CKCLRADR/ also occurs at this time; however, the address counter is inhibited from counting by the signal MNERDW1/.

MNTCK1B generates MNWREN/ which writes the first ERD data into address 3 of the memory.

On the next CKDPC, word 2 is on the data bus. CLRLATCH/ clears the latches and CKCLRADR/ counts up the address to 4. MNTCK1B generates MNWREN/ which writes word 2 into address 4.

Similarly, ERD words 3 and 4 are written into memory address 5 and 6.

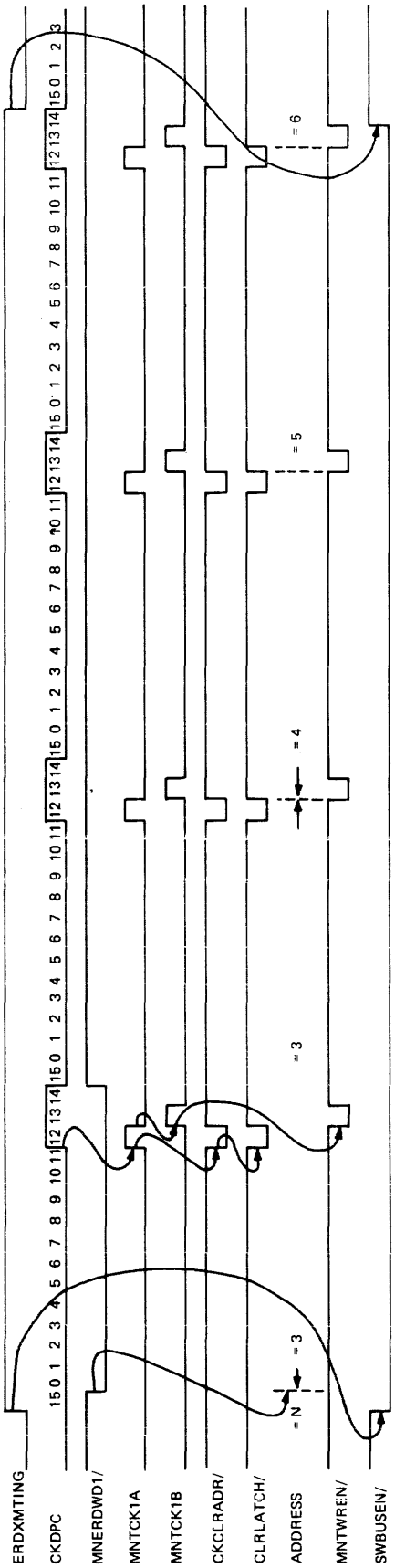


Figure 5-22. ERD Write to Maintenance Memory

SECTION 6

POWER SUPPLY

GENERAL DESCRIPTION

The power supply for the 206/207 DDEC is a compact, high efficiency unit. Full protection is provided against short circuits, overvoltage, and overheating. The supply operates normally at +10-15 percent input voltage and under the following transient conditions:

1) Input voltage five times peak value for a duration of 100 microseconds recurring not more often than once every six seconds.
2) Input voltage impulse surge of 2.5 times peak value for a duration of ten milliseconds recurring not more than once every six seconds. Input voltage impulse sag of –100 percent for a duration of ten milliseconds recurring not more than once every six seconds.
3) Input voltage surge of +20 percent RMS for a duration of ten milliseconds or longer, recovering to +15 percent in 50 milliseconds and then to +6 percent in 0.5 seconds. The maximum event rate is one during any six second interval.
4) Input voltage sag of –30 percent RMS for a duration of ten milliseconds or longer, recovering to –20 percent in 50 MS and then to –13.3 percent in .5 sec. The maximum event rate is one during any six second interval.

The Power Supply characteristics are given in Table 6-1.

BLOCK DIAGRAM

See figure 6-1 for the block diagram.

PRIMARY POWER SUPPLY

The primary input power is protected by CB3, a 4A circuit breaker. Primary power goes to a ferro resonant transformer which provides line regulation and protection from brownouts. Input taps are provided for 208V and 240V at 60 Hz, and 200, 220, 230, and 240V at 50 Hz. Secondary voltages of +16.5, +13.5, +7.8, and –8.3 are produced. All secondary voltages are fused in order to provide fire safety.

+12V REGULATOR

The +12V regulator consists of a 7812 monolithic IC featuring internal current limiting and short circuit protection. CR107 and CR108 protect the device from negative voltages which could occur in a failure of external circuits. The +12V is used for the front panel switches and lights and is present as soon as ac power is applied to the supply through CB3.

–5V REGULATOR

The –5V regulator is a series regulator consisting of Q102 and u106 (schematic 09.41.01). The –5V output is summed with a variable reference voltage in order to provide the correction voltage into the OP Amphere. If the –5V output goes more negative, u106 pin 12 and 14 go more negative so that Q102 is turned further off. This action restores the –5V to the correct value.

–5V OVERCURRENT DETECTOR

See schematic 09.41.01 u106 for the following discussion.

Table 6-1. Power Supply Characteristics

Nominal Output (V)	Max. Load (A)	Max. Transient (A)	Voltage Regulation	Ripple P-P (V)	Adjustment (V) Min.	
+5	30	18	±3%	0.02	+0.25	+0.50
–5	1	0.6	±3%	0.02	–0.25	Max. –0.50
+12	0.5	0.25	±10%	0.8		

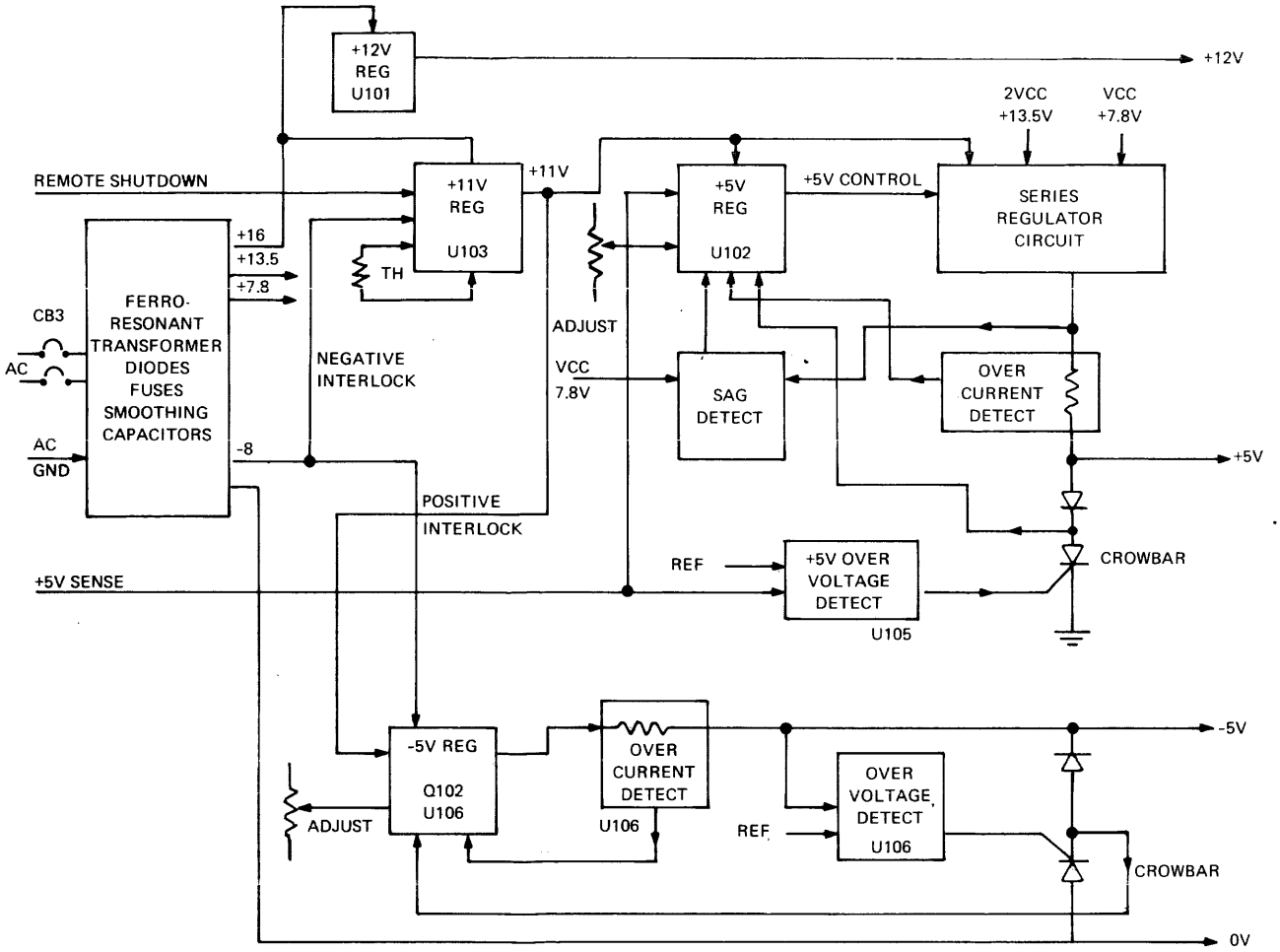


Figure 6-1. Power Supply Block Diagram

A small positive bias is applied to pin 2 by the divider R155 and R158. This bias keeps u106 with a low output. When the current on the 5V line exceeds 1 Amphere, the voltage across R156 is higher than the bias. This causes the output of pin 1 to rise. At approximately +1V, CR112 starts to conduct causing pin 13 to rise. This action causes pin 14 to go to –8V, cutting off the supply. If the short circuit condition is removed, the supply automatically restores to normal operation.

POSITIVE INTERLOCK

Positive power for u106 comes from the +11V regulator; therefore, if the +11 volt regulator is off, the –5V regulator switches off. This is the condition when the ON/OFF switch is in OFF.

–5V OVERVOLTAGE DETECTION

Over voltage is detected at –6.5V. –5V is summed with a +7V reference voltage to produce a positive voltage of 0.53 to 0.91V at u106 pin 9. If the –5V goes to –6.5V, pin 6 and 9 go below 0V. This causes pins 7 and 8 to go high, forward biasing CR111 and switching on Q112. This SCR pulls the voltage to within –1V of ground.

The positive voltage at the cathode of Q112 causes Q101 to switch on so that the regulator switches off. This allows the SCR to switch off, so that the circuit may resume normal operation. If the overvoltage condition persists, the cycle is repeated.

Removal of link W102 causes the SCR to keep conducting even if the overvoltage cause is no longer present.

+11V REGULATOR

The +11V regulator provides power for the +5V regulators. The +5V regulators are switched off by switching off the +11V regulator.

See schematic 09.41.02 for the following discussion.

The +11V output is fed back through divider R106 R107 to the inverting input of the 723 where it is compared to the +7V reference generated within the IC. (Vref. is connected to the non-inverting input). Any differences result in a correcting voltage from Vout. The regulator is current limited by monitoring

the voltage across R105. If the current limit (pin 2) is .7V more positive than the current sense (pin 3), the regulator shuts off.

There are three other conditions which may shut off the regulator:

1) If REMOTE SHUTDOWN goes high (i.e., if the ON/OFF switch is moved to OFF position), u107 conducts, grounding the frequency compensation pin 13.
2) If negative power is lost, u107 conducts, taking pin 13 to ground.
3) If the temperature of the heatsink reaches 65° C, RT101 goes low resistance shorting the base to emitter on the output transistor of the IC. This removes the bias so that no current may pass.

+5V REGULATOR

An adjustable reference voltage is compared to the +5 sense voltage returning from the backplane. An output control voltage is sent to the series regulator circuit.

The +5V regulator is shut off under two error conditions:

1) Over current is detected (over 30A).
2) OVer voltage is detected.
3) If an input voltage sag of –30 percent is detected for more than 10ms.

The regulator is shut off by grounding the F.C. pin for over current and sag. For overvoltage, the regulator is shut down by lowering the current sense input lower than the current limit.

SERIES REGULATOR CIRCUIT

The series regulator circuit actually consists of four similar circuits acting in parallel. Several features result in a high efficiency (low power dissipation) compact supply.

1) To ensure accurate current sharing, an OP Amphere is used to amplify the voltage across the current sharing resistors R139 through R142. This results in a very low value resistance, and consequently, very little power loss.
2) Due to accurate power sharing, fewer output stages are required.
3) The power for normal use comes from the +7.8V line. This means that only 2.5 volts are dropped per transistor, resulting in less power wasted in the form of heat.
4) The driver transistors Q103 through Q106 are high powered so that in the event of a power sag below 30 percent, Q107 through Q110 act as diodes, and the power is provided by Q103 through Q106 from 2VCC (+13.8). This may only occur for 10-20 ms periods due to the action of the sag detector.

Current Sharing

If the current through Q109 increases, there is an increased drop across R141. This results in a more positive voltage being applied to u104 pin 9. Pin 8 goes negative, reducing the current. C112 provides frequency stability.

Regulation

If the load draws more current, this is sensed by the +5V regulator as a drop in the sense voltage. The +5V regulator responds by increasing the +5V control voltage. U104 pin 8 goes higher, permitting the emitter voltage to rise and the current to increase until the voltage on u104 equals the control voltage.

If the load draws less current, the opposite action occurs.

+5V OVERCURRENT DETECT

U105 pin 6 is biased slightly more positive than pin 5 by the +7 volt reference voltage through R123. This keeps the output pin 7 high. If the current through R143 exceeds 30A, the voltage at pin 6 overcomes the bias so that pin 7 goes low, shutting off the +5V regulator.

+5V OVERVOLTAGE DETECT

If the +5V sense voltage goes higher than the +6.5V reference on pin 2 of IC U105, pin 1 goes high, switching on u107 transistors. This switches on the SCR Q111 which CROWBARS (shorts) the voltage to less that +1V. The +5V regulator is shutoff so that current is removed from the SCR, enabling it to switch off. This enables the circuit to restore to normal operation after a temporary overvoltage. Removal of line W101 causes the supply to latch up with Q111 on, if an overvoltage occurs.

SAG DETECT

See schematic 09.41.02. +Vcc is compared to the +5V regulated voltage. If +Vcc sags by 30 percent to +5.6V, u104 pin 5 goes more negative than pin 6. This causes a low out of pin 7. C108 discharges from + 10.8V towards or through CR109 and R111.

If the sag condition lasts for more than 10ms, the voltage on pin 3 U104 goes lower than pin 2. This causes SAG CONT to go low, shutting off the +5V regulator.

This is necessary because the driver transistors Q103-106 may overheat if held on for longer.