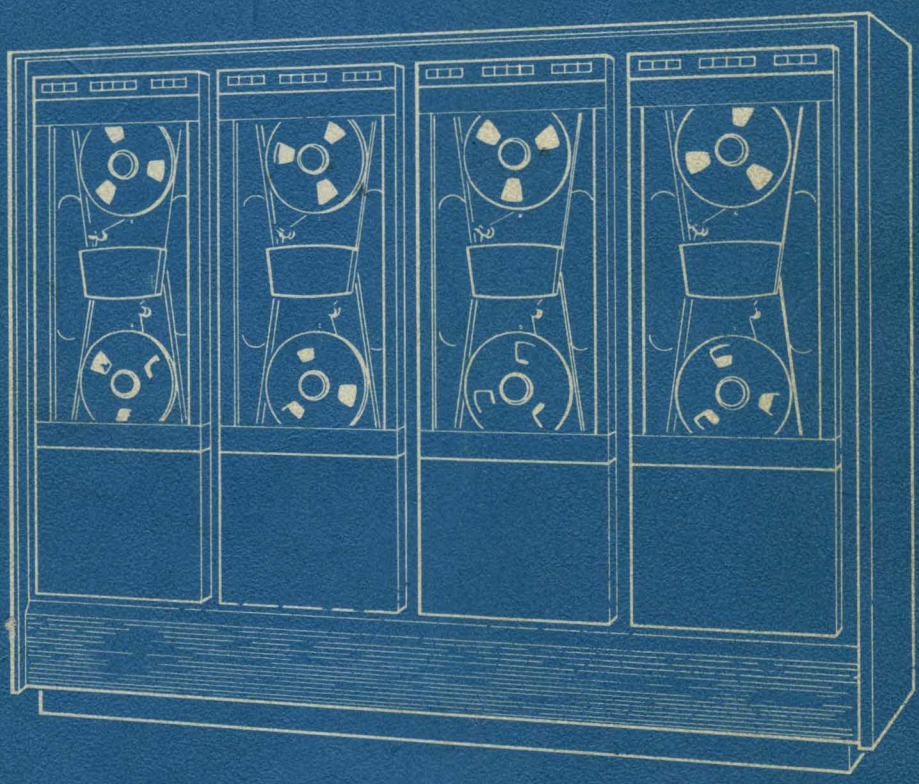
1607 MAGNETIC TAPE SYSTEM

Volume 1: DESCRIPTION AND OPERATION



INSTRUCTION BOOK

CONTROL DATA CORPORATION
MINNEAPOLIS, MINNESOTA

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Volume 1:
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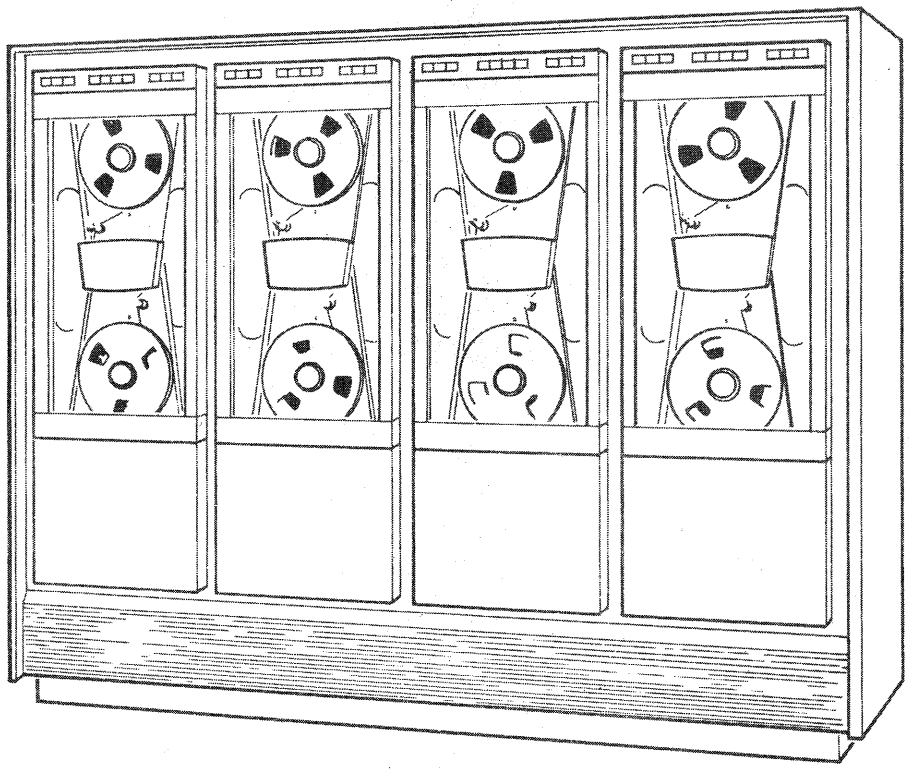

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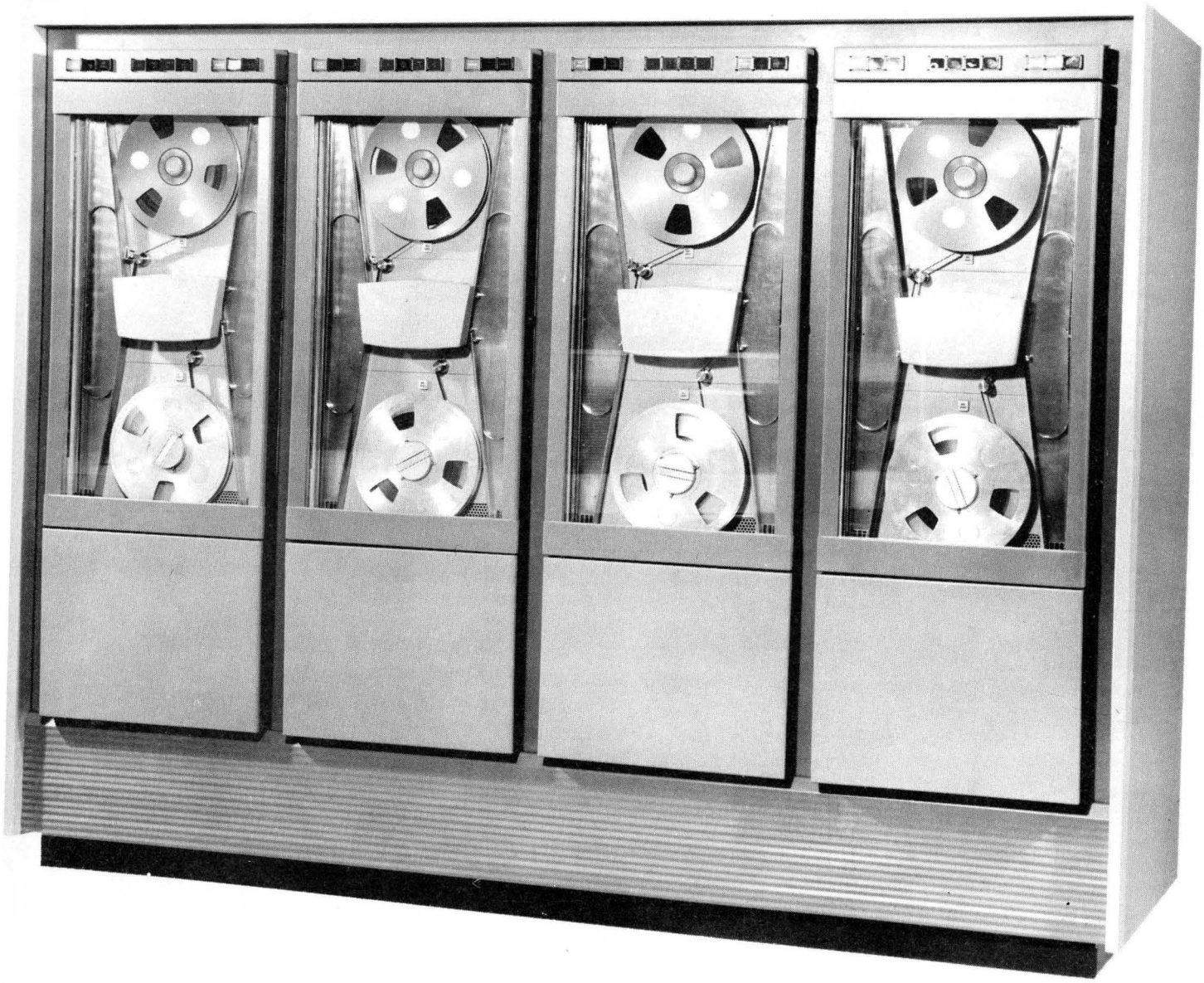


Figure 1-1. Magnetic Tape System.

CHAPTER 1. GENERAL DESCRIPTION

INTRODUCTION

The Control Data Corporation model 1607 Magnetic Tape System (MTS) (figure 1-1) is an optional input-output and auxiliary memory storage device for the Control Data Model 1604 Computer. A MTS is comprised of four Ampex FR307 digital tape handlers and a synchronizer control unit, all housed in a single cabinet. Each tape unit handles and processes plastic base tape on which data are stored as magnetized spots. The synchronizer buffers and controls the flow of data between the computer and the individual tape units. Transfer of data from the computer memory to the magnetic tapes, and vice versa, and exchange of control information is accomplished through coded programmed External Function (74) instructions.

Chapter 1, 2, and 3 describe the 1607 MTS as designed for use with the 1604 Computer only. Additional design features now provide for the use of the 1607 MTS with either the 1604 Computer or the 160 Computer. These features are described in Chapter 4, "The Satellite Computer System".

Information contained in this instruction book is subject to correction and change.

PHYSICAL DESCRIPTION

The MTS cabinet is 88 1/2 inches long, 67 3/4 inches in over-all height, and 27 1/2 inches wide. The approximate weight of the cabinet is 2500 pounds. Components within the cabinet are air cooled by blowers at the bottom of the cabinet which circulate air-conditioned room air. The equipment operates from a 208-vac, 3-phase, 400-cps supply at 5 amps and a 208-vac 3-phase 60-cps supply at 25 amps.

The cabinet is subdivided into four standard 19-inch relay rack sections, each of which holds the chassis associated with one tape unit (figure 1-2). The tape unit circuits use vacuum tubes and transistors in conjunction with printed circuit board wiring techniques. Each tape unit has self-contained d-c power supplies. The glass door at the front of each unit provides access to the tape handler for loading and unloading reels of tape.

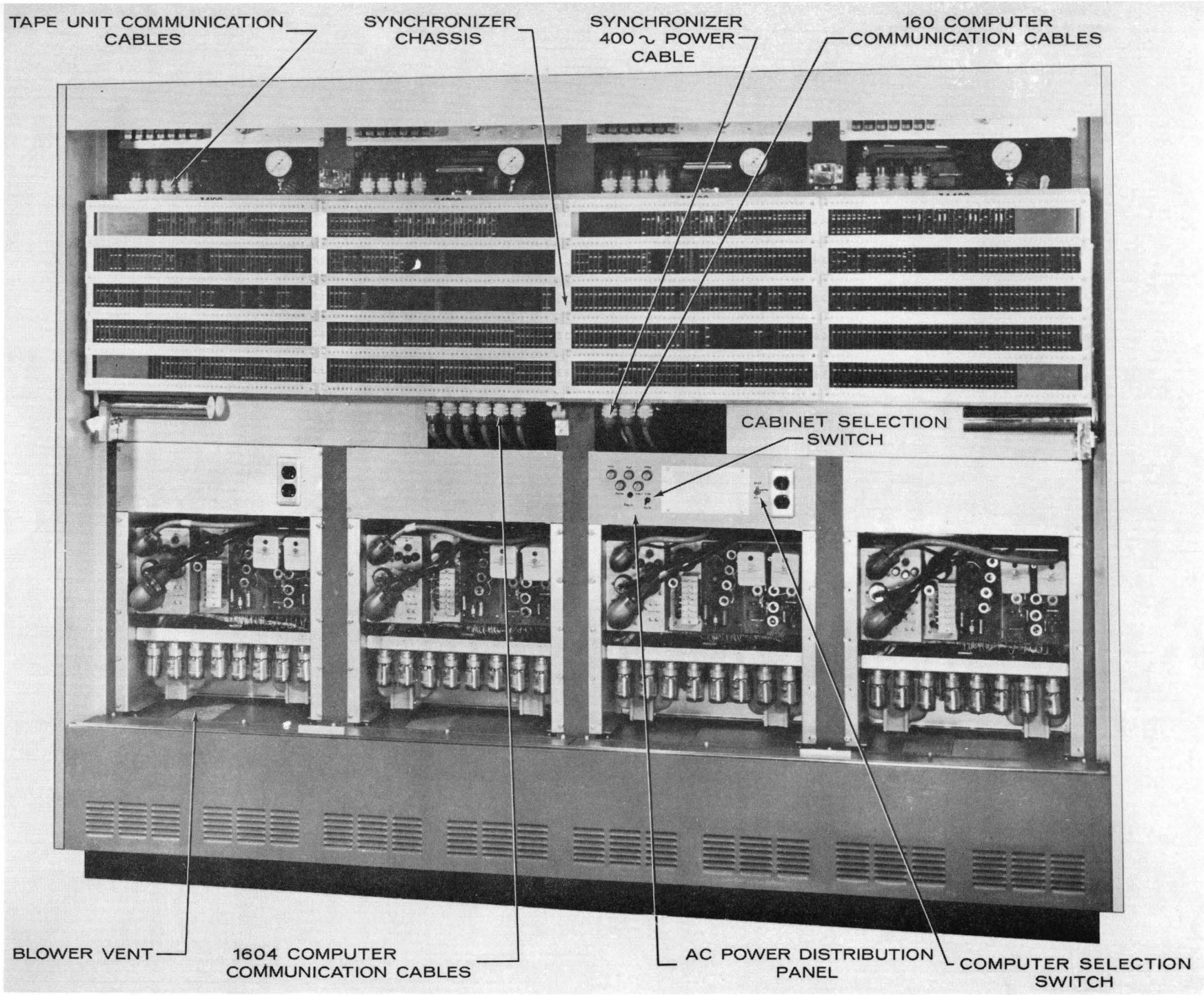


Figure 1-2. Rear View Magnetic Tape System.

The switches and indicators above the front door allow the operator to monitor and manually control tape unit conditions.

The synchronizer chassis is mounted at the rear of the cabinet (figure 1-2). Spring-loaded hinges in the lower corners of the chassis and release catches and handles at the top allow horizontal positioning of the chassis (with the sliding doors removed) for maintenance purposes. The circuits of the synchronizer are composed of printed circuit cards identical in construction to those used in the computer. The majority of the cards contain the standard building-block circuit properly interconnected to form the logical networks necessary to communicate with the tape units and computer.

Data is transferred between the MTS and the computer via six cables which connect to the bottom of the synchronizer chassis (figure 1-2). Jumper wires from these six cable connectors to another set of six cable connectors allow other equipment to communicate with the computer on the same communication paths. Data is transferred between each tape unit and the synchronizer via separate cable groups of four cables each which connect at the top of the synchronizer chassis.

Separate cables carry 400-cps and 60-cps, 208-vac primary power to the MTS a-c power distribution panel (figure 1-2). From this panel 400-cps power is cabled to the bottom of the synchronizer chassis and distributed from this point to the d-c power supply circuits located in the four corners of the chassis. The 60-cps power is routed to the blowers and to the convenience outlet panels in each cabinet section. Power cables carry 110-vac, 60-cps power from the outlets to each tape unit.

MAGNETIC TAPE CHARACTERISTICS

The MTS provides the computer with a high-speed non-volatile data storage system. Computer output data is recorded on the tape in a format compatible in all respects with the IBM 727 magnetic tape system. This facility enables communication with IBM 700 series computers as well as with a variety of IBM peripheral equipment.

A seven track non-return to zero (change-on-ones) recording scheme is used. Six tracks are assigned to the data (termed a character) and one track contains a parity check bit for the character. A character and its parity bit comprise a line of tape data.

Data is recorded in two formats: binary and binary-coded-decimal (coded). The parity bit is chosen to make the total number of "1" bits in a line odd in binary format, even in coded format. The format is chosen by the EF instruction, and the synchronizer generates the appropriate parity bit for each character. Figure 1-3 shows the bit assignments on the tape for the two formats. Table 1-1 gives the IBM character code used when generating tapes for reproduction by IBM peripheral equipment. The parity bit is recorded in tracks 6 and C for binary and coded format, respectively; the least-significant bit position is in tracks 0 and 1, respectively.

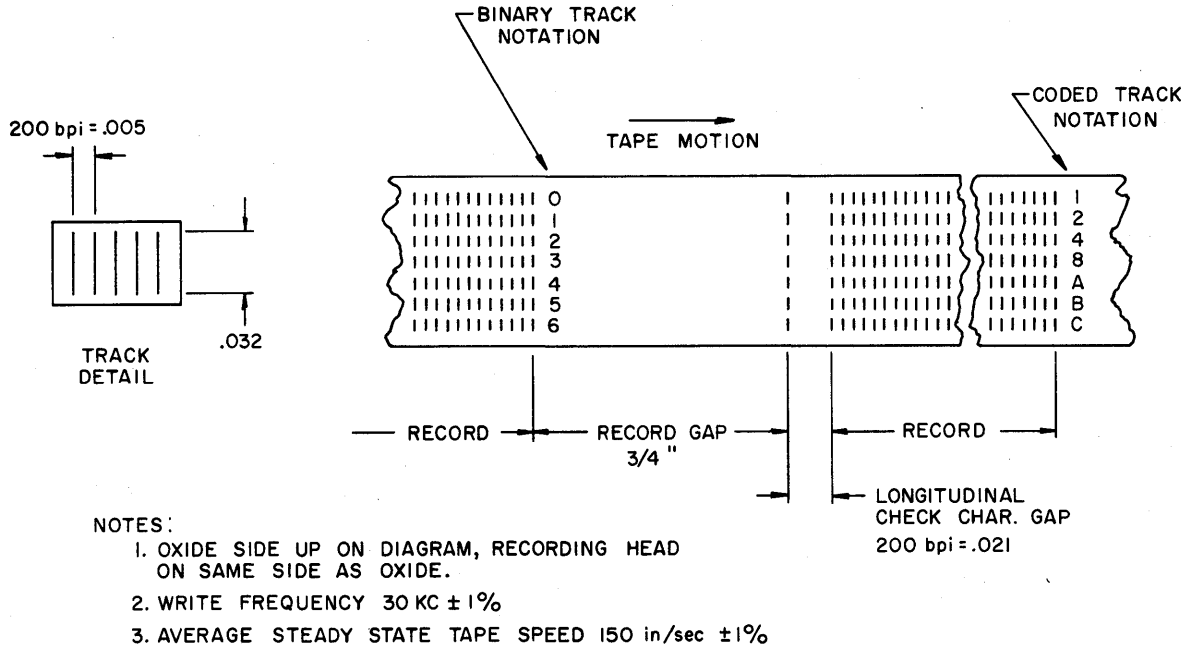


Figure 1-3. Magnetic Tape Specifications

Data is recorded on the tape at a density of 200 lines per inch and in records of varying length. A 3/4-inch unrecorded area or blank space separates adjacent records. A number of records may be grouped into a file of information on the tape by recording of a special character (octal 17 code) spaced 6 inches from the last record in the file.

Tape speed during reading and writing operations is 150 inches per second; the character transfer rate is 30 KC. Standard tape is 1/2 inch wide and up to 3600 feet long. Small reflective spots attached to the tape mark the beginning and end of the useable portion of tape. These markers are referred to as load-point and end-of-tape and are detected by photo-sensing means.

BASIC PRINCIPLES OF OPERATION

The MTS communicates through the synchronizer with the computer on a 12-bit function channel, a 48-bit input buffer channel, a 48-bit output buffer channel, and associated control signal lines (figure 1-4). The channels and control signals are activated by the External Function (EF 74) instruction.

Depending on the installation, a MTS can communicate with the computer on buffer channel pairs 1 and 2, 3 and 4, or 5 and 6 (even numbers denote computer output channels, odd numbers input channels). This instruction manual assumes a MTS connected to channels 3 and 4.

Each tape unit communicates with the synchronizer on a 7-bit read bus, a 7-bit write bus and associated control lines. The appropriate unit and its cable lines are activated in response to the EF instruction.

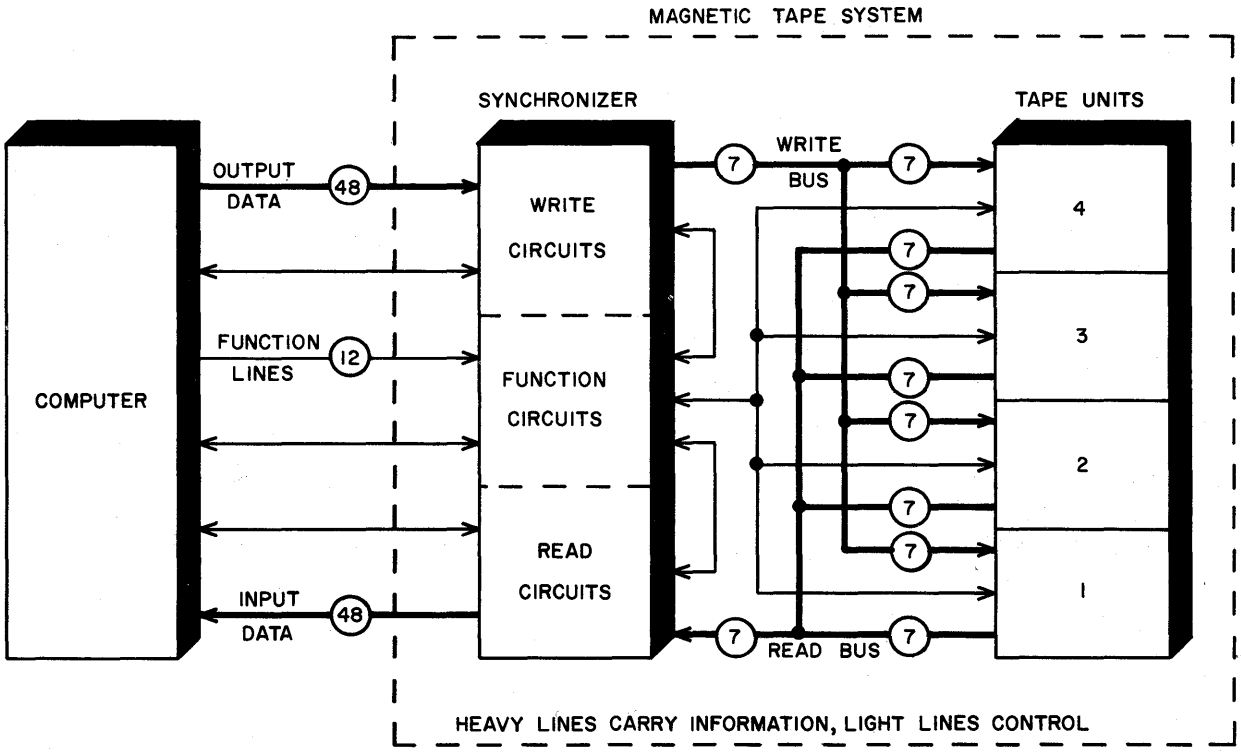


Figure 1-4. Magnetic Tape System, Information Flow.

The circuits of the synchronizer portion of the MTS are organized into function, write, and read circuits. The function circuits store control information regarding the tape units that is received from the computer or the units themselves. The write and read circuits provide independent write and read channels (to accommodate simultaneous read and write operations) and use information stored in the function circuits to direct writing and reading. The write and read circuits each have access to the four tape units; a tape unit must be assigned to operate with the read or write channel. This unit assignment and other functions are accomplished by the EF instruction.

EXTERNAL FUNCTION INSTRUCTION

The various subinstructions of the EF instruction are used to initiate and control all MTS operations. Briefly, their function are as follows:

(EF Select) 74.0X ----	requests specific tape operations and assigns a tape unit to a read or write channel (X).
(EF Sense) 74.7X ----	enables computer to determine status or condition of particular tape unit. For example, determines if unit is ready to be operated, if error was detected in previous operation, and so forth.
(EF Output Buffer) 74.4 ----	initiates and controls buffering of 48-bit words from computer to MTS for recording on tape.
(EF Input Buffer) 74.3 ----	initiates and controls buffering of MTS data to computer.

Select Operations

During select (74.0X----) instructions the lower-order 12 bits of the instruction are sent out on the function channel with a function ready signal to all equipment connected to channel X. The upper 3 bits of the code specify the equipment, the lower-order 9 bits the operation requested. The synchronizer function circuits interpret the EF code and store the information in control flip-flops. In general, input channel codes are stored in control FFs which communicate with the read circuits; output channel codes are stored in control FFs which communicate with the write circuits. Table 1-2 lists all MTS select codes.

As noted earlier the write and read circuits each have access to the four tape units and it is necessary to assign a unit (n=1, 2, 3, 4) to one channel or the other. In table 1-2 the first two instructions in the two select code groups assign a tape unit to a read or write

channel. All other selections and sense operations (see below) in the same group are accomplished on the previously selected unit. By means of manual controls on each tape unit, any of the four tape units can be operated as the unit designated by the program.

Write. A write select (20n1, 2) instruction assigns unit n to the output channel specified and prepares the synchronizer for an impending output buffer operation (a 2001, 2 select instruction is used if unit was selected previously). Execution of a subsequent 74.4 output buffer instruction establishes the output buffer initial address and causes the computer to issue an output buffer active signal (buffer terminal address is generally established prior to write select).

The computer signal starts the selected tape moving and after a short delay the write circuits accept the initial 48-bit word indicated by an output data ready signal. The word is transferred to a disassembly register and an output data resume signal is returned to the computer after which the word is recorded. Each word is disassembled into 6-bit characters, a parity bit generated for each, and the 7 bits transmitted over the write bus to the tape unit for recording on the tape. One character is recorded every 33 μsecs.

The sequence continues with exchange of ready and resume signals until the end of the buffer is reached as indicated by turn-off of the active signal. This causes a record check character to be recorded .02 inch from the last character of the record. The check character provides for a longitudinal parity check for IBM compatibility.

During the sequence each recorded line (exclusive of the check character) is sensed by a read head (spaced .390 inch from the write head), returned to the write reply circuits for a parity check and any error condition stored for subsequent sensing by the computer. An additional check determines if the number of lines read was an integral multiple of eight; if not a write reply length error is stored for later sensing by the computer.

After the last character is read the tape is stopped with the heads positioned in the interrecord space ready to write the next record. If the end-of-tape reflective spot marker is sensed during the operation, the fact is stored for later sensing by the computer.

Read. A read select (20n1, 2) instruction assigns unit n to the input channel specified and prepares the synchronizer for an impending input buffer operation. As in the write select case, establishment of the buffer initial address causes an input buffer active signal to be generated by the computer.

The computer signal starts the tape moving and, after a suitable delay to position the read head over the data, reading begins. The lower-order 6 bits of each line are assembled into 48-bit words in an assembly register and then transferred to an input register for transmission to the computer. An input data ready signal from the synchronizer initiates computer storage action for the assembled word. A computer input data resume signal acknowledges the word and clears the input register in preparation for the next word.

A parity check is performed on each line read (exclusive of the check character) and an error condition stored for later sensing by the computer.

A lack of tape information for a predetermined period indicates the end of the record and the tape is stopped with the read head positioned in the inter-record gap ready to read the next record.

The computer may call for more or less words than are available in a record. Under these conditions a read length error is detected and stored for later sensing by the computer. If the computer buffer is equal to or less than the tape record length the buffer active signal is terminated automatically; if the buffer length is greater than the tape record length the computer executes additional instructions to artifically terminate the buffer and turn off the active signal.

Reading of an end-of-file mark (17_8) is also stored for sensing by the computer.

Write End-Of-File Mark. An end-of-file mark is used to group a number of records into a file of information. An output channel select write end-of-file mark (2003) instruction causes the 17_8 code to be recorded on the tape 6 inches after the last record in the file. The mark is treated as a 1-character record and a longitudinal check character (also an octal 17) is also written. No computer buffer is established for this operation.

Backspace. An input or output channel select backspace (2006) instruction moves the tape backwards past one record to the preceding inter-record gap. None of the information passed over is available to the computer and therefore no computer buffer is established.

Rewind. An input or output channel select rewind (2005) instruction rewinds the tape from its current position to the load point.

Rewind Interlock. An input or output channel select rewind interlock (2007) instruction rewinds the tape from its current position to the load point and provides an interlock at that point so that the tape is not again available to the computer. Tape speed is 225 inches per second in this operation.

Interrupt. An input or output channel interrupt select (2004) instruction may be executed after any of the select instructions (except rewind interlock) to automatically interrupt the main computer program upon completion of the previously selected tape operation. For read or write select instructions, the interrupt select is executed after the read or write operation is selected and after the buffer initial address has been established.

Sense Operations

During sense (74.7X----) instructions the lower-order 12 bits of the instruction are sent out on the function channel with an appropriate sense ready signal to all equipment connected to channel X. As in select instructions the upper 3 bits specify the equipment, the lower-order 9 bits, however, request an indication of the status or condition of a tape unit (unit selected previously). If the condition being sensed is present, the synchronizer returns (immediately) a positive sense response to the computer; if the condition is not present a negative response is generated. The computer interprets the response internally. Table 1-2 lists the sense codes for determining MTS conditions. A brief description of the conditions follows.

Ready to Read. A tape unit must be ready to accept new input channel (or output channel; see below) select instructions. This sense instruction (2000,1) enables the computer to determine a unit's readiness. A unit is ready if:

1) Unit has power on and all protective interlocks are closed (front door closed, etc).
2) No current input channel select operation is in process.

3) Unit is not rewound with interlock.

Read Parity Error. This input channel sense instruction (2002,3) enables the computer to determine a parity error (vertical). A positive response indicates:

1) A previous read binary operation detected one or more lines with an even number of "1" bits.
2) A previous read coded operation detected one or more lines with an odd number of "1" bits.

Read Length Error. This input channel sense instruction (2004,5) enables the computer to determine if, in a previous read operation, the word length of the tape record was in agreement with the computer buffer length. A negative response indicates non-agreement and it is necessary for the computer to insure that its input buffer is terminated. Tape motion will be prevented if a previous input buffer was not completed and the input buffer active signal turned off.

End-of-File Mark. This input channel sense instruction (2006,7) enables the computer to determine if an end-of-file mark (octal 17) was read in a previous read operation.

Ready to Write. This output channel sense instruction (2000,1) enables the computer to determine a unit's readiness to perform an output channel select operation. Ready conditions are the same as described for the Ready to Read sense instruction.

Write Reply Parity Error. This output channel sense instruction (2002,3) enables the computer to determine if a parity error (vertical) was detected in the write reply sequence of a previous write operation. Error conditions are as described for the Read Parity Error sense instruction.

Write Reply Length Error. This output channel sense instruction (2004,5) enables the computer to determine, for a previous write operation, if the number of lines read in the write reply sequence was an integral multiple of eight.

End-of-Tape Marker. This output channel sense instruction (2006,7) enables the computer to determine when no more tape is available for writing. The end of the useable portion of the tape is indicated by a reflective marker on the tape. Enough useable tape is available between the marker and the physical end of the tape to store approximately 20,000 characters.

TABLES CHAPTER ONE

TABLE 1-1. IBM CHARACTER CODE

Character	Code (Octal)	Character	Code (Octal)
A	61	2	02
B	62	3	03
C	63	4	04
D	64	5	05
E	65	6	06
F	66	7	07
G	67	8	10
H	70	9	11
I	71	&	60
J	41	-	40
K	42	(blank)	20
L	43	/	21
M	44	. (period)	73
N	45	$	53
O	46	*	54
P	47	, (comma)	33
Q	50	%	34
R	51	#	13
S	22	@	14
T	23	¤	74
U	24	0 (numerical zero)	12
V	25	record mark	32
W	26	0 (minus zero)	52
X	27	0 (plus zero)	72
Y	30	group mark	77
Z	31	tape mark	17
0	00		
1	01		

TABLE 1-2. EXTERNAL FUNCTION CODES

Channel		Select Codes
Input Channel	20n1	Select read tape n, binary
	20n2	Select read tape n, coded
	2001	Read selected tape, binary
	2002	Read selected tape, coded
74.03----	2004	Interrupt when selected tape ready
	2005	Rewind selected tape
	2006	Backspace selected tape
	2007	Rewind selected tape with interlock
Output Channel	20n1	Select write tape n, binary
	20n2	Select write tape n, coded
	2001	Write selected tape, binary
	2002	Write selected tape, coded
	2003	Write end-of-file mark on selected tape
74.04----	2004	Interrupt when selected tape ready
	2005	Rewind selected tape
	2006	Backspace selected tape
	2007	Rewind selected tape with interlock
		Sense Codes
Input Channel	2000	exit on ready to read
	2001	exit on not ready to read
	2002	exit on read parity error
74.73----	2003	exit on no read parity error
	2004	exit on read length error
	2005	exit on no read length error
	2006	exit on end-of-file mark
	2007	exit on no end-of-file mark
Output Channel	2000	exit on ready to write
	2001	exit on not ready to write
	2002	exit on write reply parity error
74.74----	2003	exit on no write reply parity error
	2004	exit on write reply length error
	2005	exit on no write reply length error
	2006	exit on end-of-tape marker
	2007	exit on no end-of-tape marker

Notes: Code for alternate MTS: 3---
n=1, 2, 3, or 4 for tape units

SUMMARY OF EQUIPMENT CHARACTERISTICS

A summary of MTS equipment characteristics is listed in table 1-3.

TABLE 1-3. SUMMARY OF EQUIPMENT CHARACTERISTICS

Equipment	Four Ampex FR307 digital tape handlers and a synchronizer control unit all contained in a single cabinet
Tape speed	a) 150 inches per second during read, write, backspace, and rewind operations b) 225 inches per second during rewind interlock
Recording density	200 lines per inch
Character transfer rate	30,000 six-bit characters per second
Seven track recording	six bits contain data, seventh bit is parity bit
Data format	a) binary: provides odd parity b) binary-coded-decimal: provides even parity
Tape length	up to 3,600 feet
Tape width	1/2 inch
Tape thickness & material	1 mil Mylar base
Reel diameter	10 1/2 inches
Inter-record gap	3/4 inch
Character spacing	.005 inches (33 μsec)
Read or record time per 48-bit word	264 μsec
Record check character	recorded .02 inch after last character in record
End-of-file mark	Octal 17 code recorded 6 inches from last record in file. Check character written for file mark.
Tape markers	Small reflective spots are placed on tape to denote usable portion of tape.
Record length	Varies from 1 computer word to capacity of magnetic core storage.
Spacing of read & write heads	.390 inch
Recording method	non-return to zero (change-on-ones)

TABLE 1-3. (CONT'D.)

Recording current	75 ma
Read head signal	13 to 17 mv peak-to-peak
Spacing of erase head	7/8 inch (approx.) from write head
Erase head current	110 ma
Cabinet size	length, 7 feet 4 1/2 inches height, 5 feet 7 3/4 inches width, 2 feet 3 1/2 inches
Cabinet weight	2,500 pounds
Power requirements	208 vac, 3-phase, 400 cps, 3-wire, 5 amps 208 vac, 3-phase, 60 cps, 4-wire, 25 amps
Cooling requirements	21,000 BTU/hr. (minimum)

SUMMARY OF DATA AND CONTROL LINE CHARACTERISTICS

Summary descriptions and electrical characteristics of all signal lines between the MTS and the computer are presented in table 1-4. Table 1-5 provides cable and pin number designations for the various signals. Figure 1-5 shows the relation of the signals to the over-all MTS.

TABLE 1-4. DATA AND CONTROL LINE CHARACTERISTICS

Number of cables	6
Number of wires/cable	24 twisted pair (one wire each pair connected to pin b (ground) each end of cable).
Signal information on cables (static)	represented as binary "1" (-0.5v) or binary "0" (-16v).
Signal rise & fall times	2 μsec (minimum) to 4 μsec (maximum).
Signal current required	10 ma (maximum).
Line capacity	variable, 0 -.002 μf (maximum)
Cable ground return d-c resistance	1/2 ohm (maximum).
Signal stabilization time required	2 μsec (minimum) is required from the instant data signals appear on the lines until an accompanying ready signal is generated.
Data lines	48 output data lines carry computer information to the MTS; 48 input data lines carry MTS information to the computer.
Output data ready	accompanies each word of computer output information; turned off by output data resume signal from MTS.
Output data resume	indicates that MTS has accepted the computer word; turns off computer output data ready signal.
Input data ready	indicates information is present in the input register of MTS in a state which computer may sample; signal is dropped by reception of input data resume from computer.
Input data resume	indicates the computer has accepted a MTS input word. The signal turns off the MTS input data ready. The end of the input data ready turns off the input data resume at the computer.
Output buffer active	indicates the computer output buffer channel is active; remains on until the final word of the record is buffered to MTS and the last output data resume is returned to the computer.
Input buffer active	indicates that computer input buffer channel is active; remains on until computer buffer is terminated.
Function lines (12)	These lines are continuously monitored by MTS. Only the presence of the proper input or output function ready signal or input or output sense ready signal enables the sampling of the content of these lines by MTS as an external function code.

TABLE 1-4. (CONT'D.)

Output function ready	indicates an output channel external function select code is present on function lines for translation by MTS; selects output channel operations within MTS. Signal is automatically dropped after 8 μsecs.
Input function ready	indicates an input channel external function select code is present on function lines for translation by the MTS; selects input channel operations within MTS. Signal is automatically dropped after 8 μsecs.
Output sense ready	indicates an output channel external function sense code is present on the function lines to sense existence of an output channel condition within MTS. Signal is automatically dropped after 8 μsecs.
Input sense ready	indicates an input channel external function sense code is present on the function lines to sense existence of an input channel condition within MTS. Signal is automatically dropped after 8 μsecs.
Sense response	indicates to computer the presence of the condition specified by the upper 11 bits of the 12-bit sense code sent to MTS via the function lines. The line is sampled by computer at end of sense ready (input or output) signal.
Interrupt	indicates the MTS has reached the end of an operation for which interrupt has been selected. Interrupt is possible after all MTS select operations except rewind interlock. MTS signal causes computer to interrupt the main program and enter a special subroutine which determines cause of the interruption, takes appropriate action and then returns to main program. The signal remains on until computer senses for ready condition on interrupting tape unit.
External master clear	establishes initial conditions in MTS and is produced whenever Clear switch at computer console is placed in the up position.

TABLE 1-5. CONNECTOR PIN NUMBER ASSIGNMENTS

	Input Buffer Channel			Output Buffer Channel		
Pin No.	Cable 1	Cable 2	Cable 3	Cable 1	Cable 2	Cable 3
A	Bit 47	Bit 24	Bit 01	Bit 00	Bit 23	Bit 46
B	46	23	00	01	24	47
C	45	22	Input Data Ready	02	25	Output Data Ready
D	44	21	Input Data Resume	03	26	Output Data Resume
E	43	20	Input Buffer Active	04	27	Interrupt
F	42	19	External Master Clear	05	28	Input Function Ready
H	41	18	Not used	06	29	Input Sense Ready
J	40	17		07	30	Output Function Ready
K	39	16		08	31	Output Sense Ready
L	38	15		09	32	Sense Response
M	37	14		10	33	Output Buffer Active
N	36	13		11	34	Function Bit 00
P	35	12		12	35	01
R	34	11		13	36	02
S	33	10		14	37	03
T	32	09		15	38	04
U	31	08		16	39	05
V	30	07		17	40	06
W	29	06		18	41	07
X	28	05		19	42	08
Y	27	04		20	43	09
Z	26	03		21	44	10
a	25	02	Not used	22	45	Function Bit 11
b	ground	ground	ground	ground	ground	ground

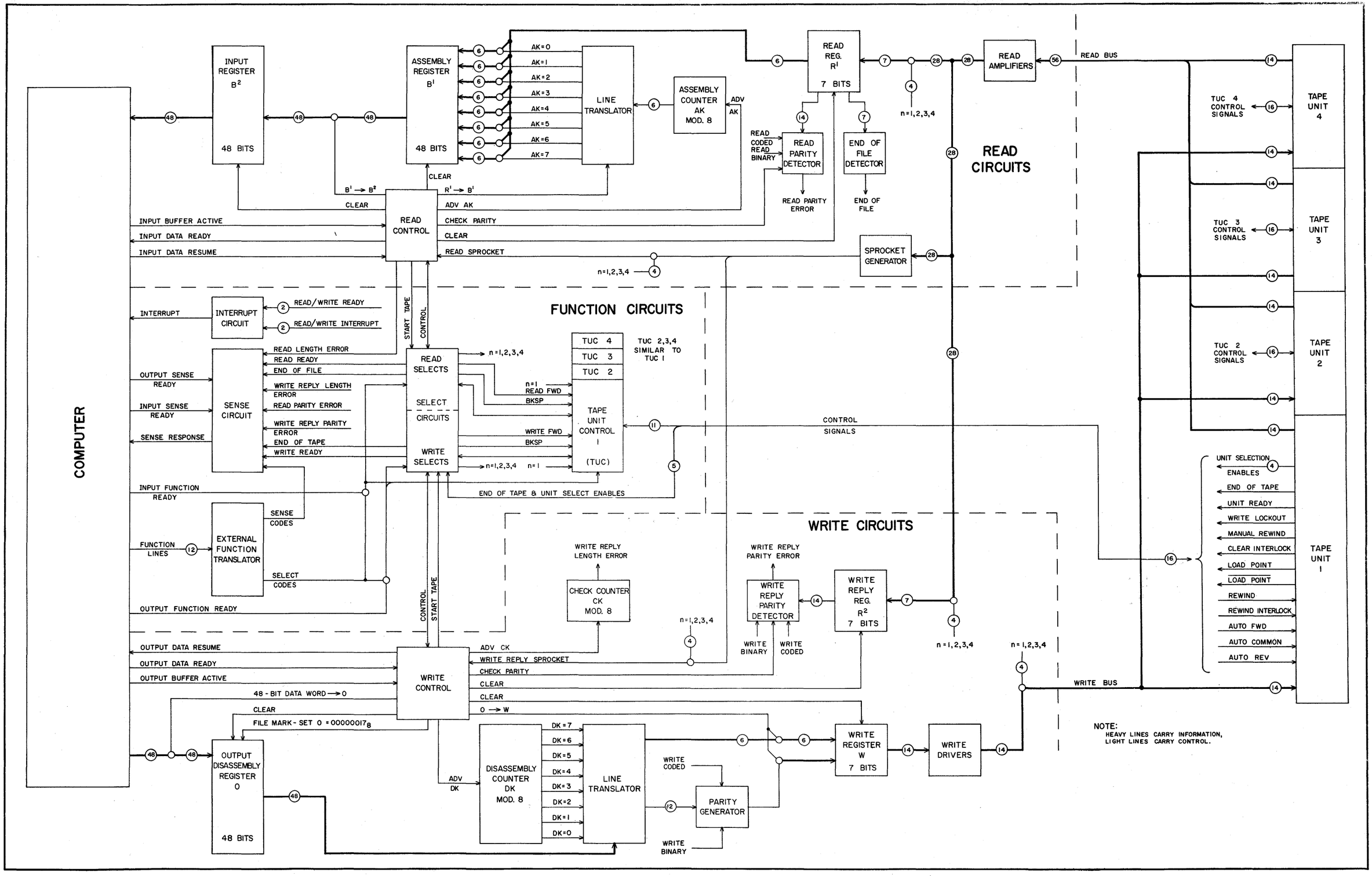


Figure 1-5. Over-all Magnetic Tape System.

CHAPTER 2. OPERATION

INTRODUCTION

This chapter contains information necessary to prepare the MTS for operation under computer program control or manual control. The discussions assume that all power and control cables have been connected as required. Because of differences in manual controls, the instructions to follow supersede those presented in the operation chapter of the Ampex instruction book.

Operating information under the general heading assumes that the equipment has been placed in initial operating status by maintenance personnel and that it is only necessary for the operator to load reels of tape on the units for processing by the computer and to unload them when processing is complete. More detailed information is provided under the supplementary heading.

GENERAL OPERATING INSTRUCTIONS

When the tape unit has been properly prepared for use, the following conditions will apply when a reel of tape is to be loaded (refer to figure 2-1): 1) the lower (takeup) reel is installed and a permanent machine leader of metal-backed tape is threaded from that reel to a point just beyond the tape leader clamp which is holding the tape (this assumes there is no file reel installed); and 2) a file tab of opaque mylar tape is spliced to the file reel which is to be installed. (Threading permanent machine leader is a maintenance procedure; refer to maintenance in Ampex instruction book). Under the stated conditions the tape is said to be at change tape position. The following load tape procedure assumes that load-point and end-of-tape reflective spot markers have been attached to the tape. A later paragraph details the procedure necessary to attach the markers.

TAPE LOAD PROCEDURE

To load tape (figure 2-1):

1) Open door to handler.
2) Check that file reel to be loaded has been file protected as necessary.
3) Mount reel on file reel hub and tighten hub knob. To insure proper reel alignment push reel firmly against reel hub stop before tightening knob. If file protection ring has been removed from reel, check that Write Lockout

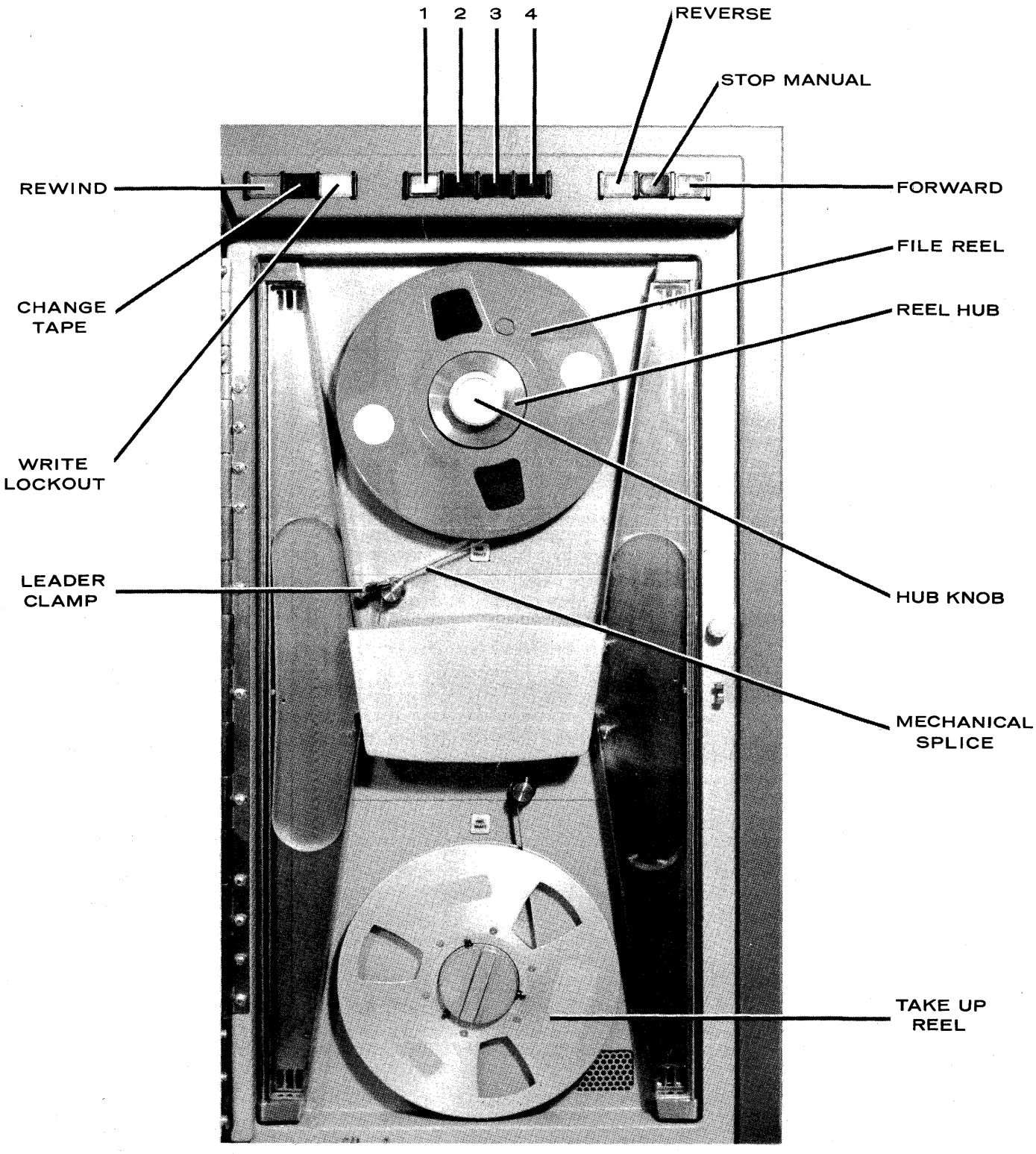


Figure 2-1. Tape at Change Tape Position.

lamp is on when reel is loaded. If lamp is not on call maintenance.

4) Press upper Reel Brake pushbutton (to release mechanical brake) and check that pulling tape from reel causes it to rotate clockwise. Pull sufficient tape from reel to reach end of permanent machine leader held by leader clamp.
5) Connect file tab to permanent machine leader.
6) Take up slack by turning file reel while depressing upper Reel Brake pushbutton.
7) Lift leader clamp and close door.
8) Depress one of the switches labelled 1, 2, 3, 4 to apply power to unit and assign unit a logical program selection number. After two minutes Stop Manual lamp should turn on; if it does not, call maintenance.
9) Depress Forward button; wait 10 seconds.
10) Depress Stop Manual.
11) Depress Rewind button. Unit is ready when Rewind lamp turns off. If Stop Manual lamp remains on, unit is not ready; call maintenance.

TAPE UNLOAD PROCEDURE

To unload magnetic tape:

1) Depress Stop Manual button to select manual mode.
2) Depress Reverse button to move tape backwards to change tape position.
3) Open front door of tape unit.
4) To secure tape, lower leader clamp.
5) Depress upper Reel Brake button (to release mechanical brake) and pull tape from file reel to provide slack.
6) Unfasten mechanical splice which connects file tab to permanent machine leader.
7) Loosen file reel hub knob and remove file reel.
8) Check if reel needs to be file protected and also if it is labelled adequately prior to storage.

SUPPLEMENTARY OPERATING INFORMATION

APPLICATION OF POWER

Primary 60 cps and 400 cps power is routed to a MTS cabinet through separate circuit breakers located in switch panels from which power is distributed to the entire computing system. With the respective circuit breakers in ON position, power is applied to the cabinet by operation of the Power On/Off switch on the computer console. The above action should start the four blowers in the bottom of the cabinet and energize the convenience outlets. Check that all blowers are operative as evidenced by air flow

from the screen grille located above each blower on the bottom rear deck of the cabinet behind the sliding doors. A lack of air flow will generally be accompanied by a blown 60 cps power fuse F30004 and/or F30005. Do not operate the equipment with one or more blowers inoperative.

A blown fuse in the 400 cps power lines is indicated by F30001, F30002, or F30003 (blown fuse indicated by a glowing fuse cap).

CABINET SELECTION SWITCH

Each external equipment connected to the computer is assigned a unique equipment selection code for reference by the External Function instruction; each equipment recognizes its code when called on to communicate with the computer. This code is contained in the fourth lower-order octal digit of the base execution address of the External Function instruction. The MTS is assigned two equipment selection codes to allow two cabinets to communicate with the computer on the same pair of buffer channels. The assigned MTS codes are 2 and 3. The cabinet selection switch, located at the back of the cabinet on the a-c power distribution panel, is labelled CAB 2 (down position) and CAB 3 (up position) and must be positioned to correspond with the code used by the program for that cabinet, or the cabinet referred to will not respond.

FILE PROTECTION RING

The back of the 1607 file reel has a slot near the hub which accepts a plastic ring called the file protection ring (figure 2-2). Writing on a tape is possible only when the reel contains a file protection ring, however, the tape may be read with or without the ring. Presence of a ring on a reel of tape is signalled to turn-off of the Write Lockout indicator immediately after the reel is loaded onto the tape unit. The ring should be removed from the file reel after writing is completed to avoid loss of valuable records through accidental rewriting.

ATTACHING REFLECTIVE SPOTS

Reflective spots are placed on the tape to enable sensing of the beginning and end of the useable portion of the magnetic tape. The markers also provide compatibility with IBM equipment. The reflective spots are small pieces of plastic 1 inch long and 3/16 inch wide, coated with an adhesive on one side and vaporized aluminum on the other. They are placed on the base or uncoated side of the tape and detected by photo-sensing circuits. The marker at the beginning of the tape is the load-point marker; the marker at the end of the tape is termed the end-of-tape marker.

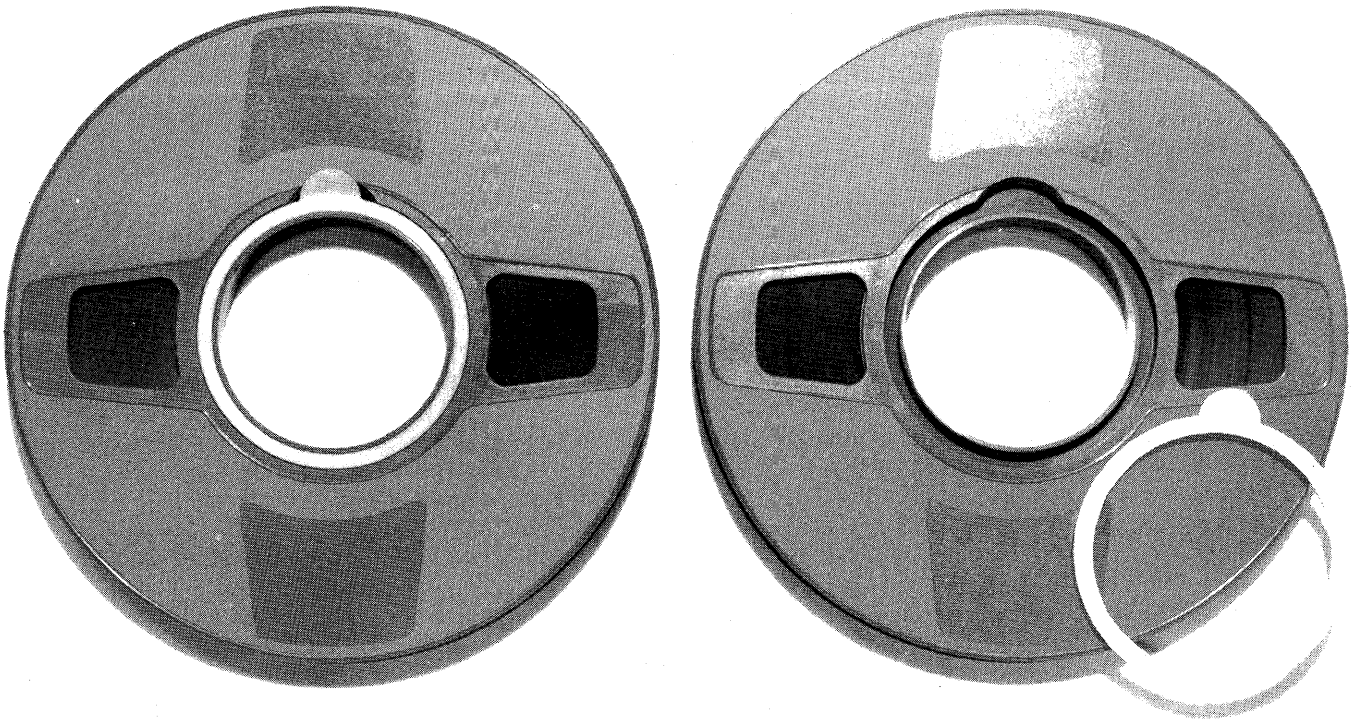


Figure 2-2. File Protection Ring.

The load-point marker must be placed at least 10 feet from the splice of the file tab and magnetic tape (figure 2-3). The marker is placed with its 1-inch dimension parallel to, and not more than 1/32 inch from, the edge of the tape nearest the operator when the file reel is mounted.

The end-of-tape marker should be placed not less than 18 feet from the physical end of the tape attached to the takeup reel hub. This space includes approximately 10 feet of tape trailer (which may be metal-backed tape) and enough tape to hold a record of 20,000 characters after the end-of-tape marker is sensed. The marker is placed with its 1-inch dimension parallel to, but not more than 1/32 inch from, the edge of the tape nearest the tape unit (when reel is mounted).

The markers should be properly aligned and firmly attached to the tape. It is recommended they be applied while the reel is removed from the tape unit. Use care to avoid dust accumulating on the tape.

MANUAL OPERATION

Manual operation of the tape unit is selected by the Stop Manual pushbutton. Tape motion is controlled then by operation of the Forward, Reverse, Rewind, and Stop Manual pushbuttons.

Forward tape motion is selected by depressing the Forward pushbutton. If the entire reel is to be run, tape is stopped automatically when the metal backing of the file reel trailer contacts the upper sensing post (assuming tape loaded as outlined in Tape Load Procedure paragraph); otherwise tape motion must be stopped by operating the Stop Manual pushbutton.

Reverse tape motion at normal speed (150 inches per second) is selected by depressing the Reverse pushbutton. Tape is stopped by operation of the Stop Manual switch or is stopped automatically in the change tape position when the metal backing on the permanent machine leader contacts both the lower and upper sensing posts. If the Rewind pushbutton is operated following operation of Reverse, tape will move backward to change tape position at high speed (225 inches per second).

NOTE: If tape motion is interrupted for any reason (for example, if the front door is accidentally opened and the drive system thus de-energized) it will be necessary to reselect the direction mode of tape motion.

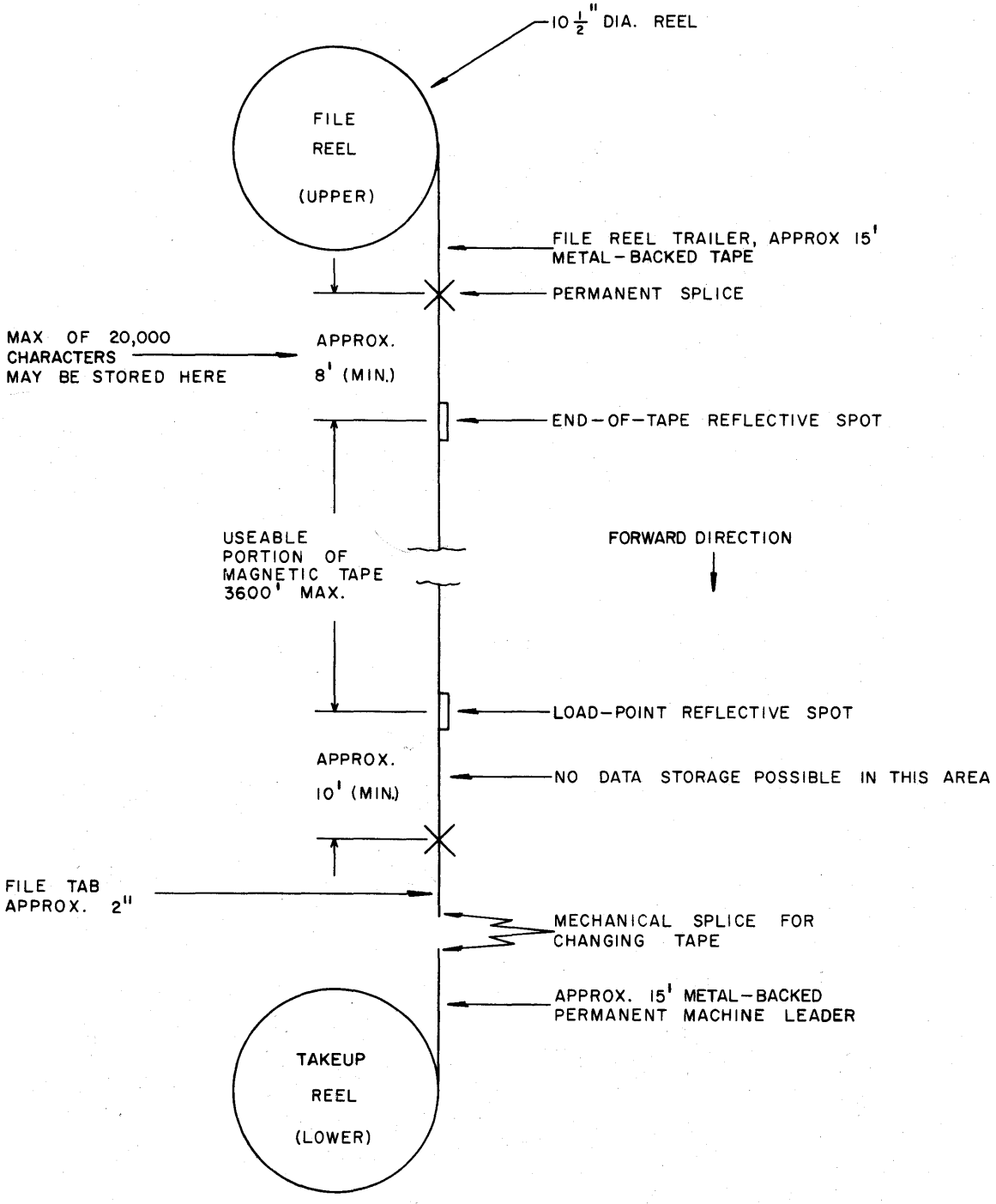


Figure 2-3. Physical Layout of Tape.

MANUAL CONTROLS AND INDICATORS

The controls for manual operation are mounted on a panel located above the front door of each tape unit (figure 2-1). The functions of the controls are shown in table 2-1.

TABLE 2-1. FUNCTION OF MANUAL CONTROLS AND INDICATORS

Control		
Rewind	S	Controls manual rewind to load point.
	I	Indicates rewind in progress.
Change Tape	S	Drops manual selection and places tape unit in automatic or program control mode.
	I	When lighted, indicates tape rewound under program control and interlocked at load point. Interlock prevents operation of tape unit and prevails until Stop Manual switch is operated.
Write Lockout	S	Drops power and removes program designation from unit.
	I	When lighted, indicates that tape unit is loaded with a reel which does not contain a file protection ring. Tape cannot be written as long as light is on, but may be read.
1, 2, 3 or 4	S	Designates program selection of unit and applies power to unit. Each new unit designation cancels an existing designation.
	I	Indicates unit selection and power on condition.
Reverse	S	Initiates reverse tape motion during manual operation.
	I	Indicates reverse tape motion.
Stop Manual	S	Drops unit from program control or drops Forward or Reverse selection and places unit in manual mode.
	I	Indicates manual mode.
Forward	S	Initiates forward tape motion during manual mode.
	I	Indicates forward tape motion.

S = switch

I = indicator

CHAPTER 3. PRINCIPLES OF OPERATION

INTRODUCTION

A 1607 Magnetic Tape System (MTS) is composed of four Ampex FR307 digital tape handlers and a synchronizer control unit (figure 3-1). The tape units handle and process plastic-base tape on which computer output data are stored as magnetized spots. The computer communicates with the tape units through coded External Function (EF) instructions which are interpreted by the synchronizer control unit. The synchronizer recognizes MTS operation requests by the computer and accepts computer output data for recording on the tape, reads tape data and transfers it to the computer input-output (I/O) section, or variously positions the tape without transfer of data to or from the computer.

This chapter discusses the principles of operation of the synchronizer. The principles of operation of the tape units are described in the Ampex instruction book. The material to follow assumes that the reader has a general knowledge of the tape unit principles of operation.

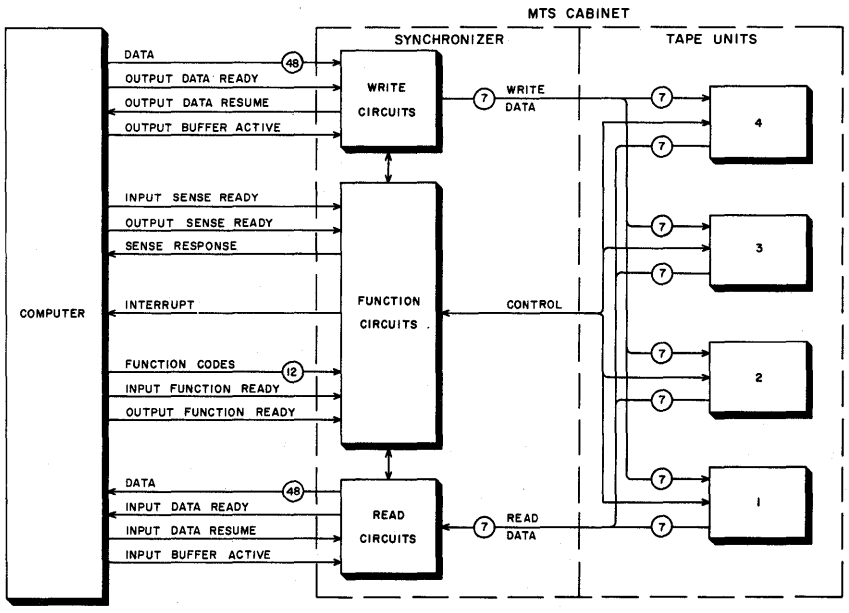


Figure 3-1. Simplified Block Diagram, Magnetic Tape System.

PRESENTATION OF MATERIAL

For purposes of discussion, the synchronizer circuits are organized (figure 3-1) into three main groups: function circuits, write circuits and read circuits. The functions of each of these main circuits in the over-all operation of the synchronizer and the operation of the individual circuits comprising each main group is discussed initially. With this circuit background, a tabular description of the sequence of events (as they occur with respect to time) for each tape operation is presented next. These descriptions are intended to summarize and tie together the individual circuit descriptions. Following the tape operation descriptions, the manual control circuits and the power and cooling system are discussed. Detailed descriptions of selected circuits appear at the end of the chapter.

Emphasis in the discussions to follow is placed on the logical operation of a circuit, because the majority of synchronizer circuits are composed of many electrically similar stages which may have varying logical properties. The circuits are contained on standard Control Data Corporation printed circuit cards. Most synchronizer card types and circuits are identical with those used in the computer; refer to the computer instruction manual for a detailed description of the basic building block circuit and its variations. Circuits and card types unique to the synchronizer are discussed at the end of the chapter.

SUMMARIES OF REFERENCE MATERIAL

The synchronizer circuit discussions assume reader familiarity with certain information basic to the synchronizer and computer logic circuits, such as equation files, logic diagrams and their symbols, the computer I/O section and other reference information. For those not familiar with this information, the paragraphs following summarize the more complete discussions found in the computer instruction manual.

Equation File

The equation file, using Boolean algebra terms, provides a detailed logical representation of the synchronizer. The subject term of each equation is the logical designation of a building block; the remainder of the equation describes all inputs to the building block. The outputs and physical location of the building block are listed below the equation.

A unique logical designation is assigned each building block used in the synchronizer. The designation consists of a base letter followed by three superscript digits, such as A^{102}. The base letter identifies the logical element of which the building block is a part. The assignment of base letters within the synchronizer is presented in table 3-1.

The superscript digits provide a unique identification of the building block within the logical element and may have additional significance. For example, for registers, the first two digits specify the stage of the register with which the FF is associated. The third digit identifies the FF output: an even digit indicates a "0" output, an odd digit a "1" output.

TABLE 3-1. EQUATION SYMBOL ASSIGNMENT

A. function and ready line drivers and translations	N. transmission control
B. assembly and input registers	O. output disassembly register
C. not used	P. load point inverters
D. tape unit control	Q. master clear
E. disassembly counter translations, read amplifier selectors	R. read register, write reply register, and parity check
F. read control	S. not used
G. write control	T. write driver and tape unit actuator inverters
H. not used	U. not used
I. inverter ranks	V. not used
J. not used	W. write register and write parity generator
K. control flip-flops	X. not used
L. output conversions and delay output elements	Y. delays, read amplifiers, write drivers, filter cards
M. input conversions and delay input elements	Z. not used

The circuits are represented in equation form by combining the logical designations according to basic rules of Boolean algebra. An example of an equation is:

$$B^{000} = B^{001} + R^{001}\ N^{025}$$

The symbol on the left of the equal sign denotes the basic circuits whose inputs are described on the right of the equal sign. The plus sign represents an OR function; the absence of a sign between symbols represents an AND function. From the above equation, B^{000} provides a "0" output if the output of B^{001} is a "1" or the outputs of both R^{001} and N^{025} are "1".

The equation file is volume 2 of this instruction book. Equations are listed alphabetically according to the base letter; within each alphabetical group, the listing is in numerical order.

Logic Diagrams

The synchronizer circuits are depicted on logic diagrams which replace electronic components with equivalent logical elements. The diagrams and the equation file complement each other; the logic diagrams provide the over-all logical picture of the synchronizer and the equation file provides detailed information concerning the interconnections between building blocks. Diagrams which show the complete logic of the synchronizer are contained in volume 2 of this instruction book and are intended as an aid to maintenance. Extracts from these diagrams are included as text illustrations in the circuit discussions to follow.

The maintenance logic diagram use the symbols shown in figure 3-2, to represent the logical properties of circuits. The text included diagrams use the same symbols and others as noted below. In general, the shape of each symbol designates a basic logical function.

The single inverter is represented by a rectangle and since it is the basic building block, all the other symbols are formed by combinations of this rectangle. The FF, which consists of two interconnected inverters, is represented by a square. The set side of the FF is at the top and the clear side is at the bottom.

The AND junction is represented by a small circle. The AND is one of the input terms of an inverter, and thus the circle is connected to the inverter rectangle by a line. The

OR junction is represented by the inputs of the inverter. Each input is identified by an arrow terminating at the inverter rectangle. For simplification, the OR function is represented on some text included diagrams by a + sign within a small square or rectangle. No signal inversion is intended by this representation.

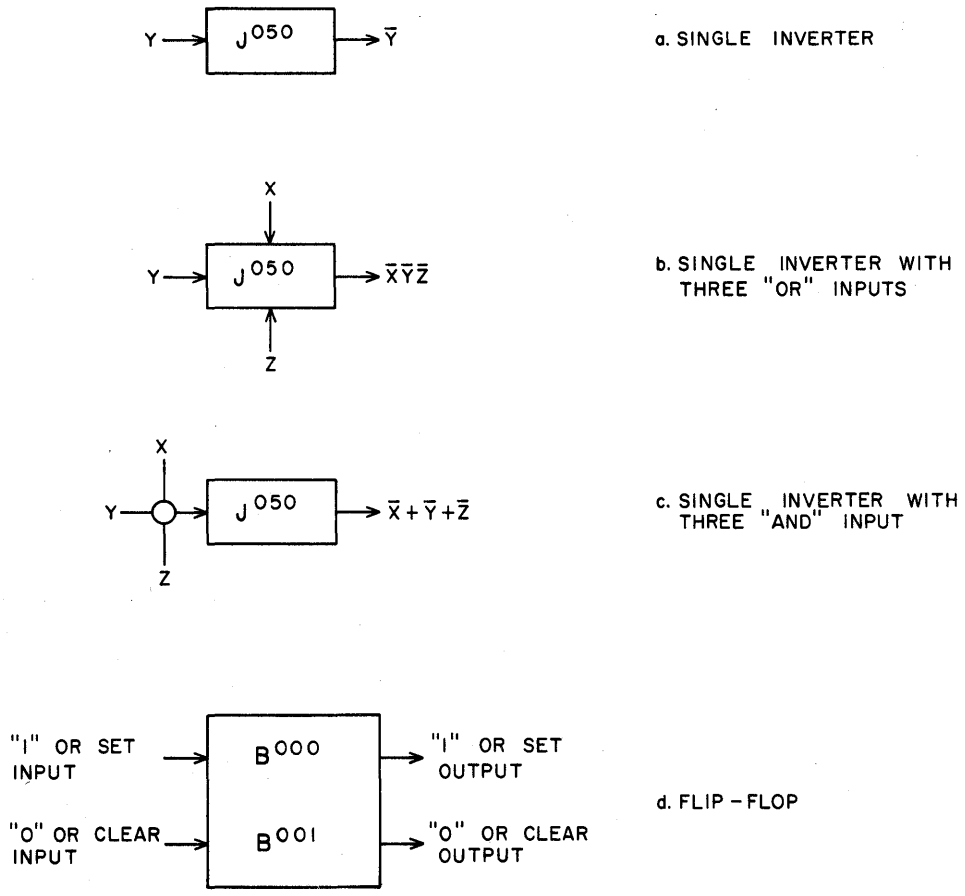


Figure 3-2. Logic Diagram Signals.

The delay function (not shown) is represented on the diagrams by a small rectangle. The time delay of the element is shown within the rectangle. The circuit involved in the delay is discussed at the end of the chapter.

I/O Conversion Cards

All electrical interconnections between the logical networks of the synchronizer, the tape units, and the computer are made via I/O conversion cards. As shown in figure 3-3, an output card (type 62) designated by an L^{---} symbol converts the low-level signal voltages of -0.5v ("0") and -3v ("1") used within the synchronizer and computer to high-level voltages -16v and -0.5v, respectively, for transmission by cables between the units. An input card (type 61) designated by an M^{---} symbol converts the high-level cable signal to the normal low-level signals used within the synchronizer and computer. When the input to an M^{---} symbol is ground or -0.5v, its output is -3v or a "1". Similarly, if its input is open, its output is at -0.5v and is considered a "0". These M^{---} properties are used extensively in the MTS for connecting the tape unit manual control relay and switch circuits to the synchronizer logical networks.

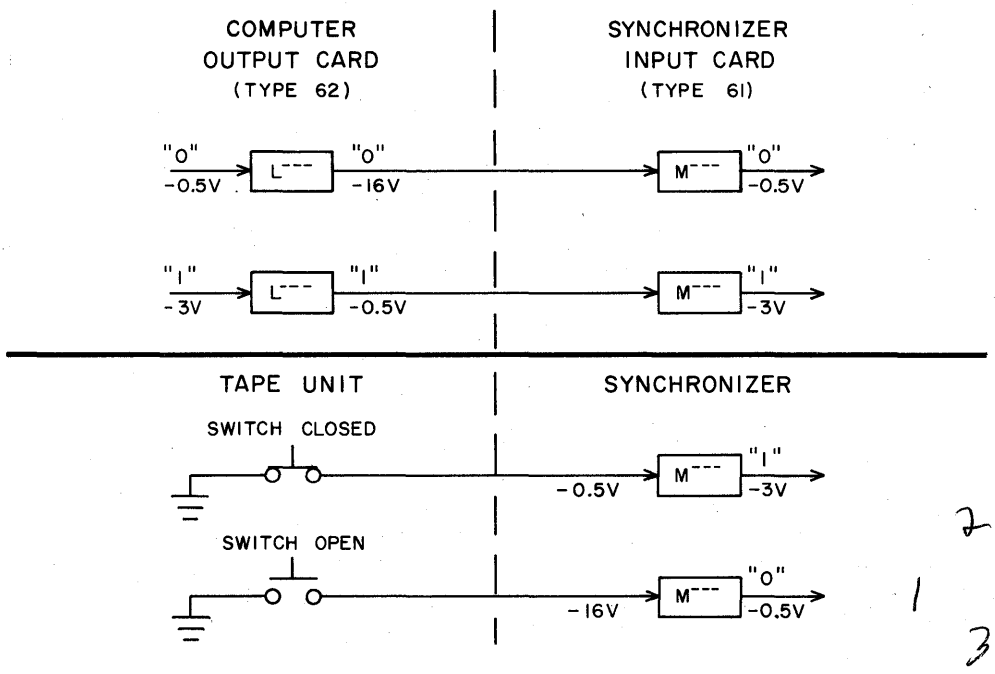


Figure 3-3. I/O Conversions.

Computer I/O Characteristics

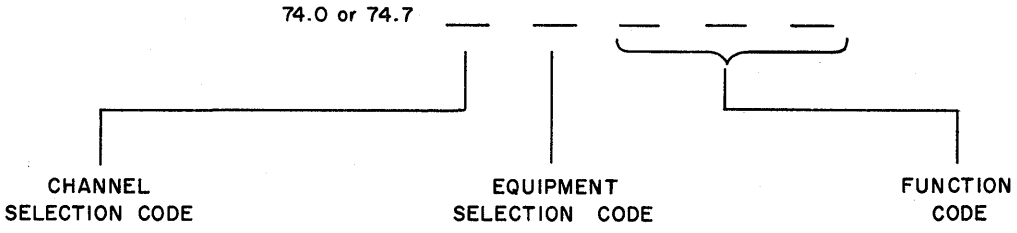
The computer I/O section (figure 3-4) comprises four sets of information channels and an I/O control system. Three sets of channels are used for buffer operations, the remaining set for high-speed transfer operations.

Each buffer channel consists of an external function channel and two information channels. The external function consists of 12 function lines and six control lines. The function lines of all channels are connected in parallel and are fed by the lower-order 12 bits of the X^2 register when an external function instruction is executed. The six control lines originate or terminate in the I/O control system. Each information channel consists of 48 information lines and 3 control lines. The information channels are designated 1, 2, . . . 7. Channels 1, 3, and 5 are used for input buffer operations; channels 2, 4, and 6 are used for output buffer operations; channel 7 is used for high-speed input and output transfer operations. Input information originates at output registers in the external device; output information originates from registers O^1, O^2, O^3, and O^4. All connections between the computer and external equipment are made by cable groups each consisting of six 24-wire cables. The cables connect to one external function channel, one input channel, and one output channel.

The external function instruction has eight subinstructions which exchange control information and data between the I/O section and external equipment. These subinstructions are: 74.0 (select external equipment), 74.1 through 74.6 (activate communication channels 1 through 6) and 74.7 (sense external condition).

The 74.0 subinstruction selects a particular external equipment and places it in a mode of operation. Subinstructions 74.1 through 74.6 initiate buffering of 48-bit data words between the computer and the previously selected external equipment. The 74.7 subinstruction permits the computer to sense certain conditions, such as error or ready conditions, in an external equipment.

During the execution of 74.0 and 74.7 instructions the five octal digits of the base execution address (m) in X^2 specify the conditions shown below.



Channel selection bits are translated by I/O control which generates one of the following ready signals for the appropriate function channel:

	Channel	Signal		Channel	Signal
74.0	Input	Input Function Ready	74.7	Input	Input Sense Ready
74.0	Output	Output Function Ready	74.7	Output	Output Sense Ready

The equipment selection and function bits are applied to function lines on all buffer channels. Each external equipment is assigned a unique code and each recognizes its code and the function or operation requested. The external equipment does not send a resume signal to indicate receipt of the information. Generally a 74.7 sense instruction is executed prior to a 74.0 select instruction to determine if the external equipment is ready to be operated or if an error condition exists. The external equipment sends a sense response signal to the computer if the sensed condition exists. Also, when interrupt is selected in the external equipment by a 74.0 select instruction the external equipment sends an interrupt signal to the computer when it has completed a selected operation.

The 74.1 through 74.6 instructions initiate buffer operations between the computer and external equipment. The index codes 1 through 6 specify the buffer channel; the base execution address designates the buffer operation starting address in the storage section. The address is automatically entered in the upper address portion of the special storage location (00001 through 00006) reserved for buffer operations. The terminal address plus one of the block of data is entered in the lower address portion of the appropriate special address previous to recording the initial address.

Each word transferred during a buffer operation requires the execution of three references to computer storage. The first reference reads the appropriate control word from the special storage address and extracts from the upper address position the current storage location for the word being buffered. The second reference is made to this storage location and transfers the data to (or from) the external equipment. The third reference replaces, in the upper address position, the next buffer address, which is the previous address plus one. The new address and the terminal address are compared and if they are equal, the buffer operation is terminated.

During the execution of input buffer operations (initiated by 74.1, 74.3 and 74.5 instructions), the signal input buffer active is sent out on the selected input channel to start the previously selected external equipment. The external equipment assembles data

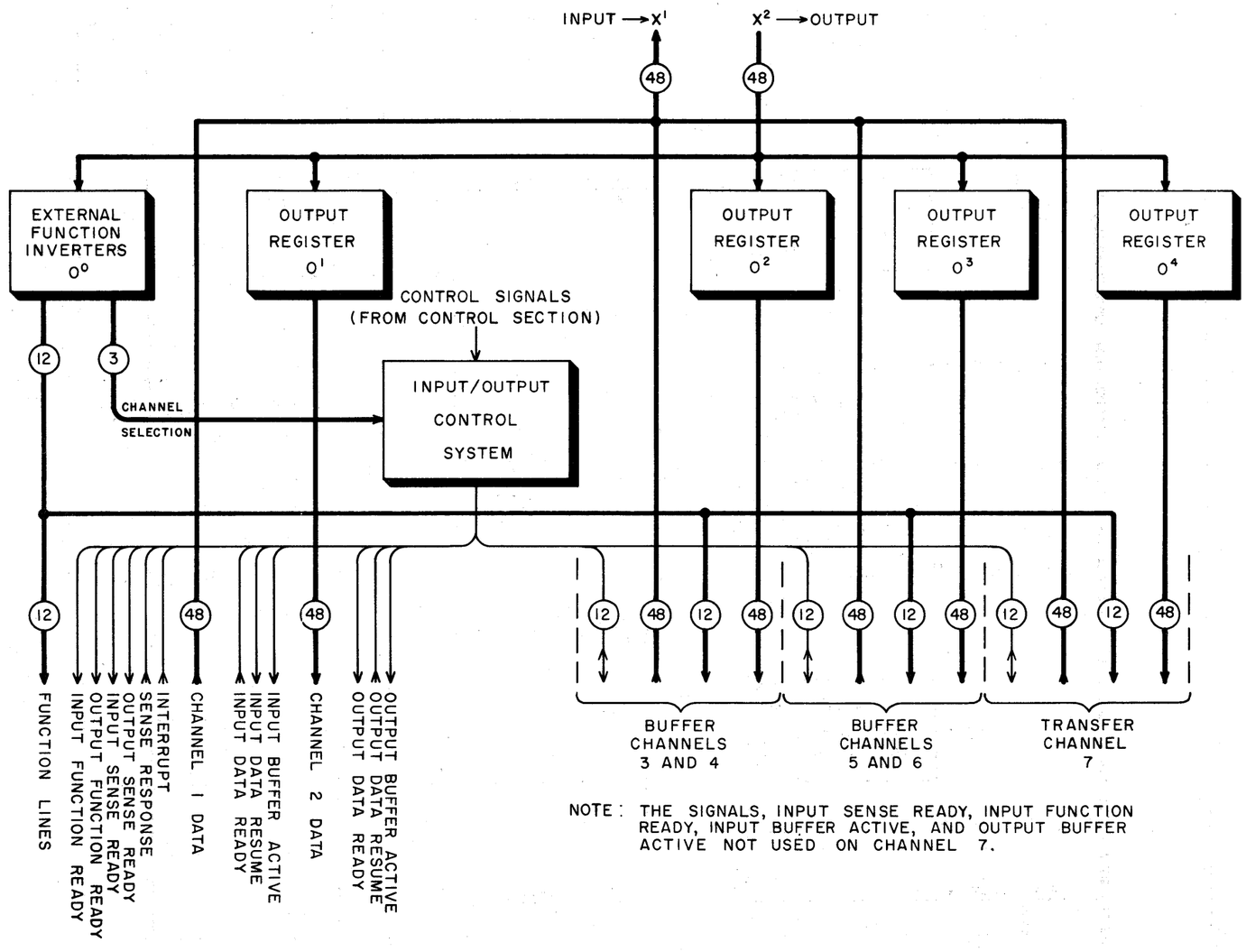


Figure 3-4. Simplified Diagram, Computer Input-Output Section.

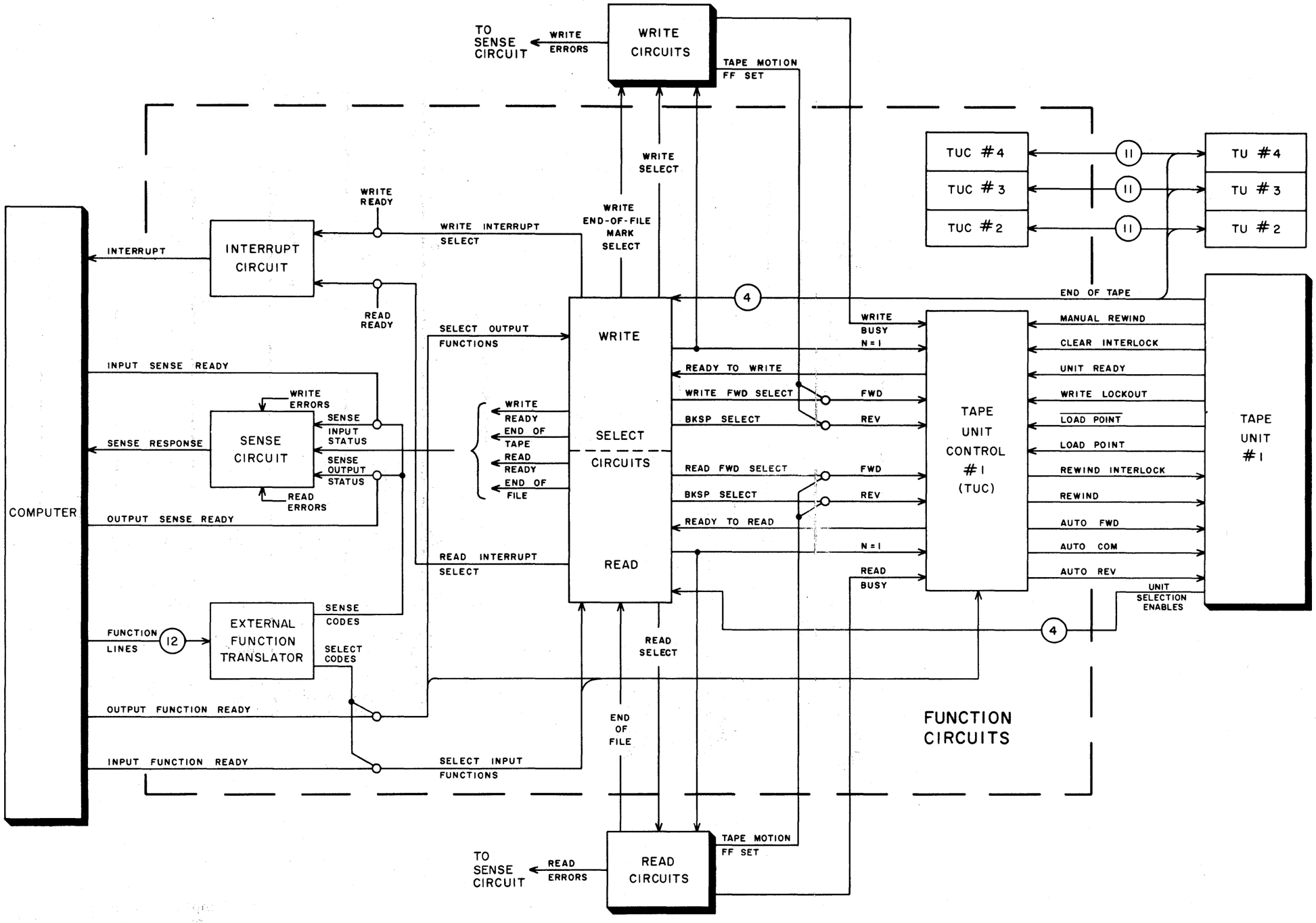


Figure 3-5. Function Circuits.

(generally in character form) into computer words and sends them to the computer via the input channel. The words are temporarily stored in the X^1 register of the computer. An input data ready signal, accompanying each word, initiates actions within the I/O control system which store the word in the computer storage section. When the computer has stored the word, it sends an input data resume signal to the external equipment. Upon completion of the input buffer operation, the input buffer active signal is terminated. As a result, the external equipment is stopped and its control circuits cleared in preparation for the next operation.

During the execution of output buffer operations (initiated by 74.2, 74.4 and 74.6 instructions), the signal output buffer active is sent out on the selected output channel to start the selected external equipment and, following this, words from computer storage are transferred to the external device via the appropriate output register (O^1, O^2, O^3) and corresponding output channel (2, 4, or 6). An output data ready signal, accompanying each word, initiates actions within the external device which disassemble the word into characters as required and store the data in the associated storage medium. The external device sends an output data resume signal to the computer upon acceptance of each word. Upon completion of the output buffer operation, the output buffer active signal is terminated. As a result, the external device is stopped and its control circuits cleared in preparation for the next operation.

All the channels of the I/O section are treated with equal priority by a scanner within the I/O control which examines each channel in turn. If a channel requires processing, as indicated by the presence of the ready signal (on input channels) or resume signal (on output channels), the scanner stops while the word is transferred and then scanning resumes. In the event that all channels should request action when scanned, the last channel would be processed in a maximum of 200 microseconds. This limits the rate of communication to a 5 kc word rate per channel if all channels are used simultaneously.

DESCRIPTION OF LOGIC CIRCUITS

Synchronizer circuits are organized into three main logical groups: 1) function circuits, 2) write circuits, and 3) read circuits (figure 3-1). Each main group is composed of a number of smaller circuits each of which has a specific function in a given tape operation. The discussions to follow present the over-all function of each main group and then describe the individual circuits and the role each plays in accomplishing group functions.

FUNCTION CIRCUITS

The individual function circuits which accomplish the events listed below, and the principle inter-circuit connections are shown in figure 3-5. Refer to this figure throughout the following discussion to locate each circuit and review its relation to other circuits.

1) Decode computer EF select (74.0) and sense (74.7) instructions requesting tape operations.
2) Provide storage for EF select codes (as necessary) and other control information, and inform the necessary circuits of a tape operation selection.
3) Control direction and motion of tape and communicate control information with the tape units.
4) Provide the computer with an indication of the status (such as: error present, or is unit ready?) of the individual tape units when so requested by a sense instruction.
5) Interrupt the computer upon completion of certain operations when so requested by the computer.

External Function Translator

The 15-bit base execution address of the 74.0 and 74.7 instruction details the EF select or sense code. The upper three bits of the code are translated within the computer to select the computer I/O channel which is to receive the code contained in the lower-order 12 bits. The lower-order 12 bits are then transmitted by cable to each equipment connected to the selected channel. The external function translator decodes the 12 bits transmitted by the computer and transfers the results to the select, sense, and tape unit control circuits.

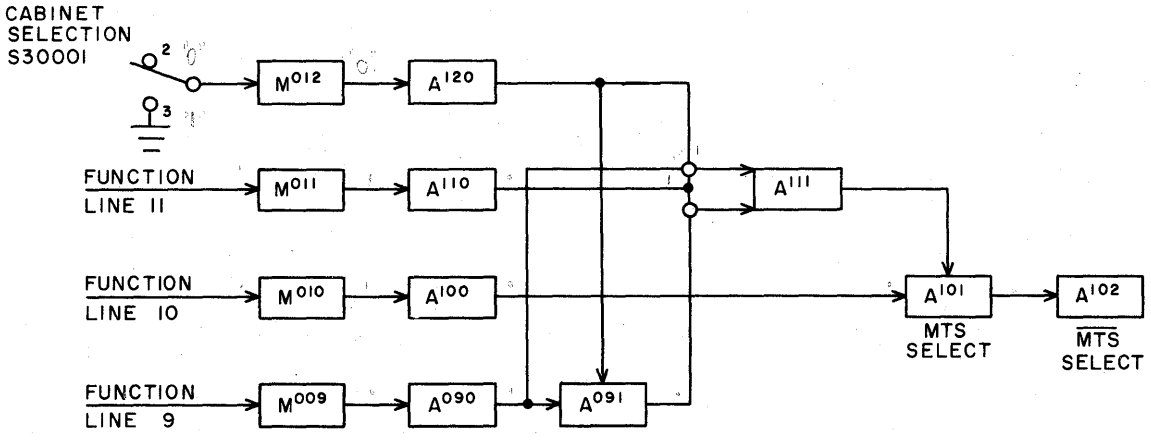


Figure 3-6. Translation of Equipment Selection Code.

Because each equipment connected to a computer channel receives the 12-bit EF code, each must recognize when it is being referenced. Each equipment is assigned a unique equipment selection code which is contained in the upper 3 bits of the 12-bit EF code. The lower-order 9 bits then detail the operation requested. The equipment select codes 2XXX and 3XXX are assigned to the MTS. The two codes allow two MTS cabinets to communicate with the computer on one pair of computer I/O channels or a total of six cabinets (24 tape units) on the three pairs of I/O channels. Figure 3-6 shows the translating circuit enabling the MTS to recognize the noted codes. A switch at the back of the cabinet labelled 2 (down position) and 3 (up position) permits a MTS to respond to one or the other code. With the switch in 2 position and a 2XXX code received (or 3 position and 3XXX code), inverter A^{101} will supply a "1" output and A^{102} a "0" output to allow the select, sense, and tape unit control circuits to respond to the translations of the operation codes presented on the remaining function lines. Table 3-2 lists all EF codes assigned to the MTS.

The select code translating circuit (Figure 3-7) recognizes a computer request for an input channel rewind or rewind interlock operation. The input function ready signal, which accompanies all input channel EF select codes, permits the circuit to respond to the appropriate rewind code. Inverter A^{205} responds to either code and allows a rewind interlock selection to use existing rewind circuits in accomplishing the interlock operation. A similar translating circuit is used to recognize output channel rewind and rewind interlock requests.

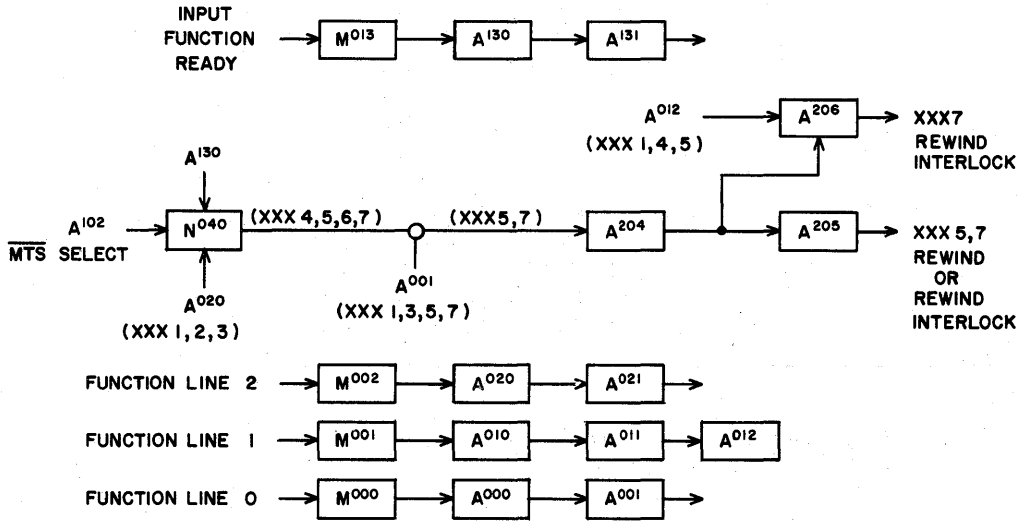


Figure 3-7. Typical Select Code Translating Circuit.

TABLE 3-2. EXTERNAL FUNCTION CODES

Channel		Select Codes
Input Channel	20n1	Select read tape n, binary
	20n2	Select read tape n, coded
	2001	Read selected tape, binary
	2002	Read selected tape, coded
74.03----	2004	Interrupt when selected tape ready
	2005	Rewind selected tape
	2006	Backspace selected tape
	2007	Rewind selected tape with interlock
Output Channel	20n1	Select write tape n, binary
	20n2	Select write tape n, coded
	2001	Write selected tape, binary
	2002	Write selected tape, coded
	2003	Write end-of-file mark on selected tape
74.04----	2004	Interrupt when selected tape ready
	2005	Rewind selected tape
	2006	Backspace selected tape
	2007	Rewind selected tape with interlock
		Sense Codes
Input Channel	2000	exit on ready to read
	2001	exit on not ready to read
	2002	exit on read parity error
74.73----	2003	exit on no read parity error
	2004	exit on read length error
	2005	exit on no read length error
	2006	exit on end-of-file mark
	2007	exit on no end-of-file mark
Output Channel	2000	exit on ready to write
	2001	exit on not ready to write
	2002	exit on write reply parity error
74.74----	2003	exit on no write reply parity error
	2004	exit on write reply length error
	2005	exit on no write reply length error
	2006	exit on end-of-tape marker
	2007	exit on no end-of-tape marker

Notes: Code for alternate MTS: 3---
n=1, 2, 3, or 4 for tape units

Select Circuits

The select circuits (read and write) store translated MTS select codes in control FFs. Outputs of the FFs signal the information stored to necessary circuits to initiate the selected operation.

The read circuits store all input channel select codes except rewind and rewind interlock; this is also true for the write circuits and output channel select codes (the rewind and rewind interlock codes are stored in the tape unit control circuits discussed later). The two select circuits are completely independent and each has access to the four tape units. Assignment of a tape unit to a particular channel is under program control; manual switches on each tape unit permit any unit to operate as number 1, 2, 3 or 4 (physical tape units numbered 1, 2, 3, 4 left to right when viewed from front).

Figure 3-8 shows a portion of the select circuits and how they operate to store a typical EF select code. Shown also are circuits informed of the selection and how a computer request for a select read tape unit 1 in binary (32011) is stored. The circuit must recognize from the 32011 code that: (1) a MTS read operation is requested (2) in binary data format (3) with forward tape motion required (4) on tape unit 1.

1) is recognized and the Read Select FF set if an input function ready signal is received when inverter A^{101} is a "1"
2) is recognized by "1" outputs from N^{060} and A^{010} to clear Format Control FF
3) is recognized because backward (XXX6 code) is not selected as indicated by a "1" from N^{060}. In this instance a signal from the read circuits keeps the Direction Control FF cleared to select forward
4) is recognized by set and clear input AND translators of the two unit select FF

The programmed unit 1 selection clears Unit Select 1 FF and sets Unit Select II FF. Assuming that unit 1 has been manually selected to operate as number 1 (as translated by relays K14 and K15 associated with the manual selection switches), the tape unit control no. 1 circuit (one such circuit for each tape unit) and the read circuits are alerted to the unit selection. Subsequent receipt by the read circuits of a computer input buffer active signal combined with the set state of the Read Select FF results in generation of an automatic forward signal from tape unit control no. 1 circuit to start tape moving in a forward direction on unit 1.

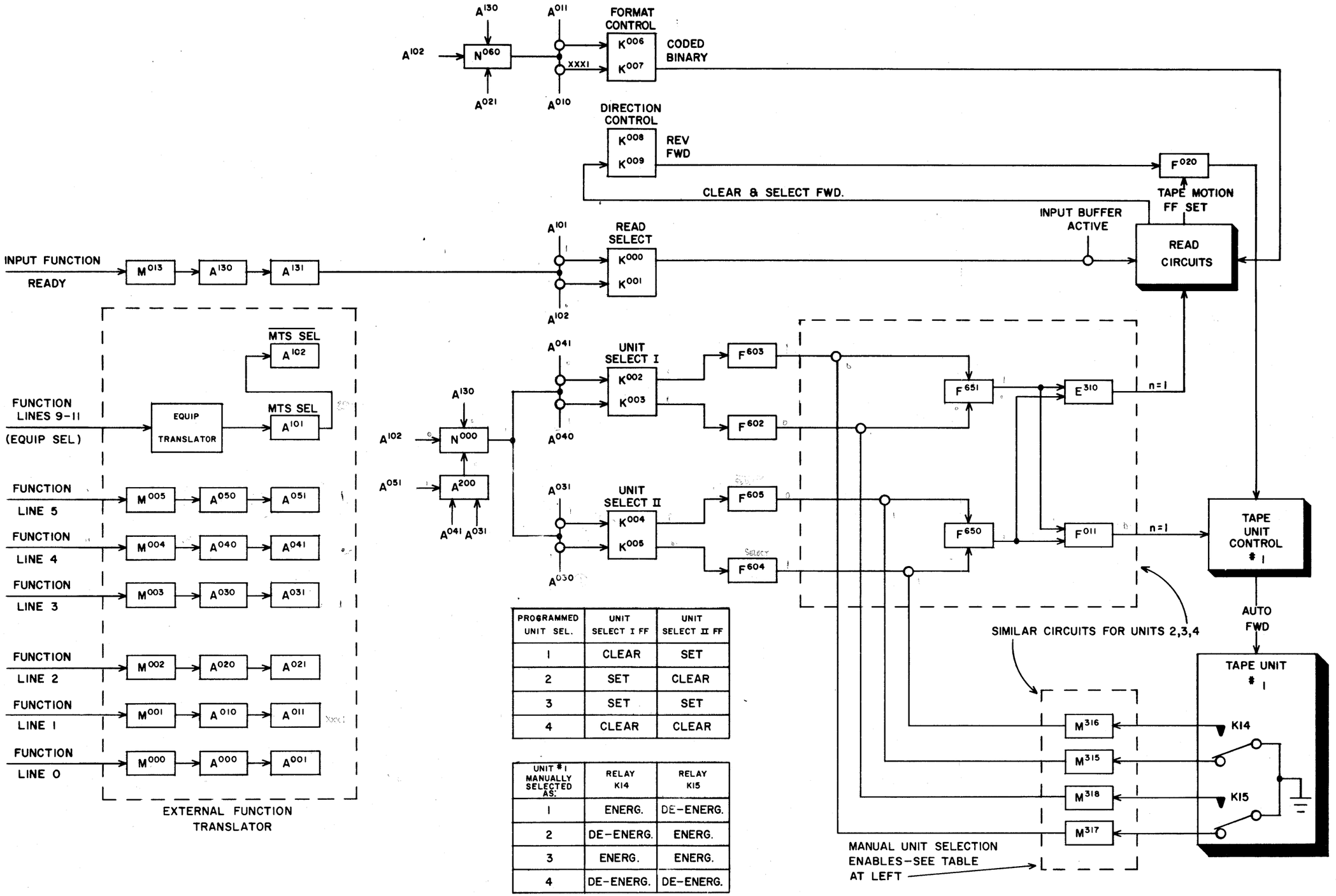
From the figure it can be seen that the relay network allows unit 1 to operate also as number 2, 3, or 4. This feature is particularly useful in that no program alteration is necessary in the event a given unit is not available for operation.

As shown in the table of EF codes, the above binary format illustration and the code for coded format reading are the only input channel select codes requiring a tape unit selection. The codes are so arranged that a tape unit selection is required to read the first record only. All subsequent input channel select and sense instructions for the unit are executed without a unit (n) selection. In figure 3-8, inverter A^{200} disables the input gating circuits of the two Unit Select FFs when n = 0 in the EF code to preserve a previous n = 1, 2, 3, or 4 selection. Direction and format changes can be made as required; intervening rewind operations are also possible without a unit selection (rewind is not illustrated in figure 3-8). The above statements concerning input channel instructions are true also for output channel (write) instruction, with the exception that once a unit is rewound with interlock it is not again available for an output channel operation until the interlock is released manually.

From figure 3-8 it can be seen that a computer-programmed external clear for the input channel to which the MTS is connected (in a typical installation, input channel 3, output channel 4)will result in clearing the Read Select FF to void an existing input channel selection. The same is true also for the Write Select FF (not shown) in the write select circuits. A computer reference to another equipment on the same input or output channel as the MTS will also clear the appropriate Read or Write Select FF to insure that only one equipment is communicating with the computer on any one channel.

Tape Unit Control

The tape unit control circuits control the direction and motion of the tape in accordance with commands from the select circuits (or from the tape unit) and communicate control information with the tape units. A separate identical tape unit control circuit is provided for each tape unit to accommodate certain simultaneous operations. The discussions to follow which refer to the tape unit control circuits for tape unit 1 apply equally to the other circuits.



PROGRAMMED UNIT SEL.	UNIT SELECT I FF	UNIT SELECT II FF
1	CLEAR	SET
2	SET	CLEAR
3	SET	SET
4	CLEAR	CLEAR

UNIT #1 MANUALLY SELECTED AS:	RELAY KI4	RELAY KI5
1	ENERG.	DE-ENERG.
2	DE-ENERG.	ENERG.
3	ENERG.	ENERG.
4	DE-ENERG.	DE-ENERG.

Figure 3-8. Storage of Select Read Tape Unit 1 in Binary, EF Code (32011)

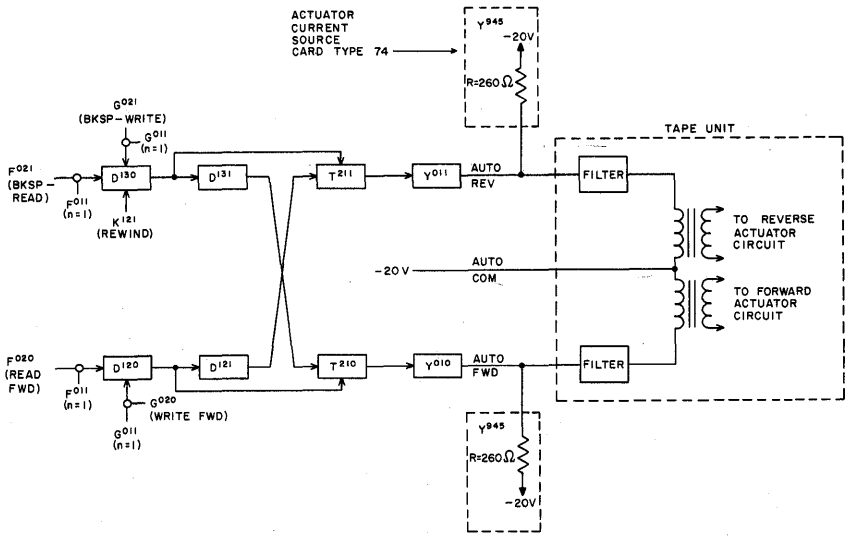


Figure 3-9. Tape Unit Motion and Direction Control Circuit.

Direction and Motion Control. Figure 3-9 shows the direction and motion circuit for controlling the forward and reverse actuators of tape unit 1. The tape unit requires that the auto forward and auto reverse commands be a stepped d-c level with the level held at -10v for an off command and raised to 0v (ground) for an on command. The rise time of the step function d-c signal should not exceed 10 μsecs. Provisions is required also to prevent simultaneous on conditions of the auto forward and reverse commands. The circuit satisfies these requirements.

Referring to the figure, a read forward or a write forward selection results in a "1" from T^{210} and grounding of the auto forward line through the circuit of Y^{010}. The auto forward signal line rises from -20v to 0v in less than the required 10 μsecs to result in energizing the tape unit forward actuator. Tape is brought to the full rate of 150 inches per second within 2.5ms of the actuator command. Coincident with this action the "1" from D^{121} insures that the auto reverse signal cannot be turned on. When the selected forward operation is completed, the input to D^{120} is removed to turn off the auto forward command and stop tape motion within 2.5ms. Circuit action for reverse tape motion is identical with forward tape motion.

Tape Unit/Synchronizer Control Signals. Figure 3-10 illustrates most control signals between tape unit 1 and the synchronizer.

A programmed or manual rewind selection for unit 1 sets the Rewind FF to rewind the tape at a rate of 150 inches per second. When load point is reached the Load Point FF is set to clear the Rewind FF and stop the tape. The not load point signal keeps the load point FF cleared during the time that the tape is not at load point.

A programmed rewind interlock selection (XXX7) sets the Rewind Interlock and Rewind FFs to rewind the tape to load point. The clear interlock command is generated by the tape unit to clear the Rewind Interlock FF as soon as the interlock condition is established. Tape rewinds at 225 inches per second in this operation and a Change Tape indicator is lighted at the unit to indicate an interlock condition. The unit is not again available for a programmed operation until the unit Stop Manual button is operated to release the interlock. The unit ready command is absent during the interlock condition to prevent a tape unit ready status being indicated to the computer.

The tape unit write lockout and unit ready commands indicate to the synchronizer and to the computer (through the sense circuits) that the tape units are ready to perform computer requests. Presence of the write lockout command indicates the tape unit is loaded with a file reel which does not contain a file protection ring. The unit is not ready to write under this condition and the sense and interrupt circuits are so informed by a "0" from G^{031}. A unit not ready condition is also produced when the write circuits are busy with a write, write end-of-file, or backspace operation.

The unit ready command indicates that: power is applied to the unit, protective interlocks are closed, it is not in rewind interlock mode (Change Tape indicator not lit) and it is in automatic mode. If the unit is not in a rewind mode and the read circuits are not busy with a read or backspace operation, then the unit is ready and a "1" is produced by F^{031} on the read ready line.

The write ready and read ready commands are used by the interrupt circuit to interrupt the computer at the end of those tape operations for which interrupt has been selected. The read or write ready signals are turned on at the completion of the operation for which interrupt was selected to enable production of an interrupt signal.

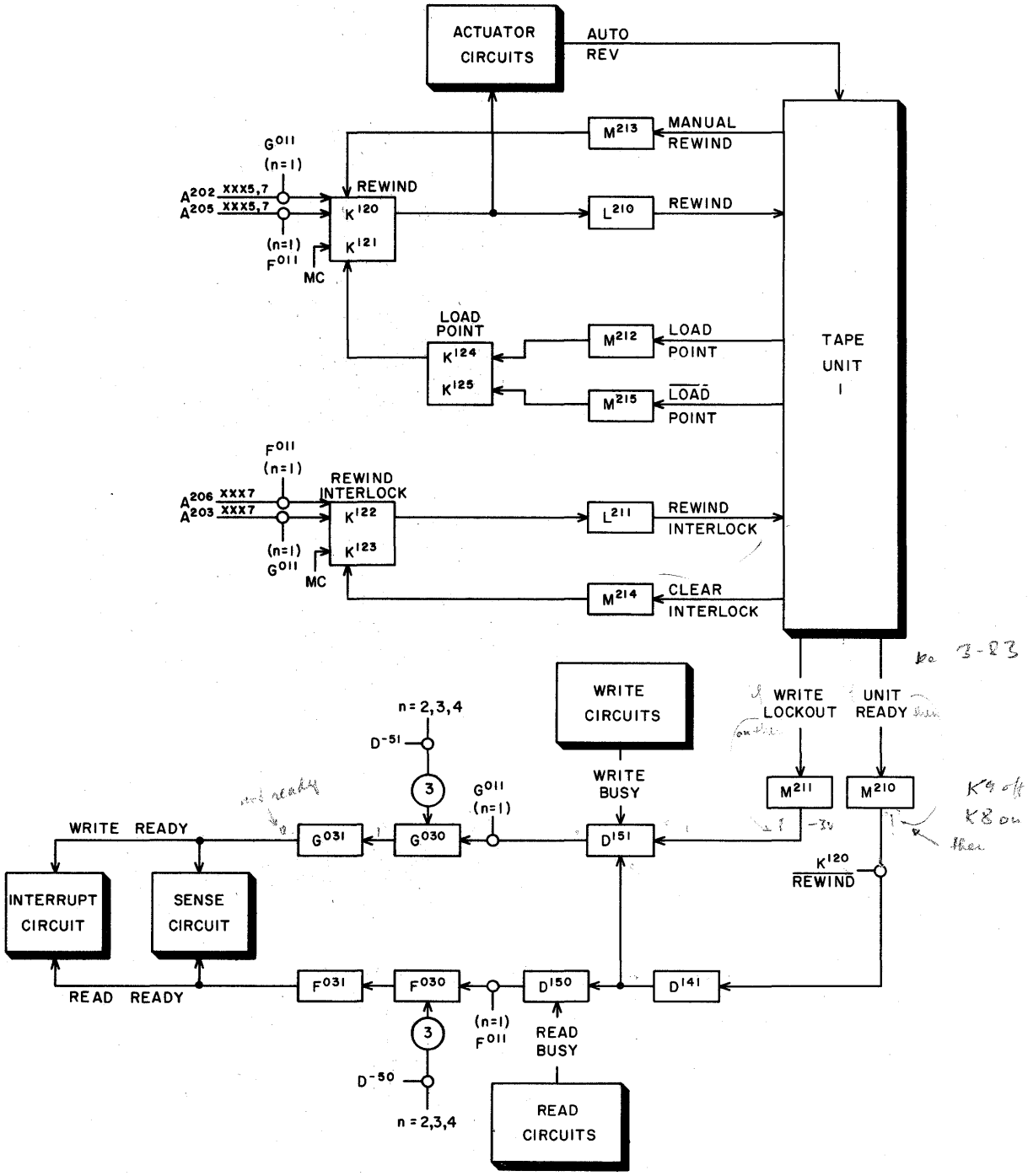


Figure 3-10. Tape unit control signals.

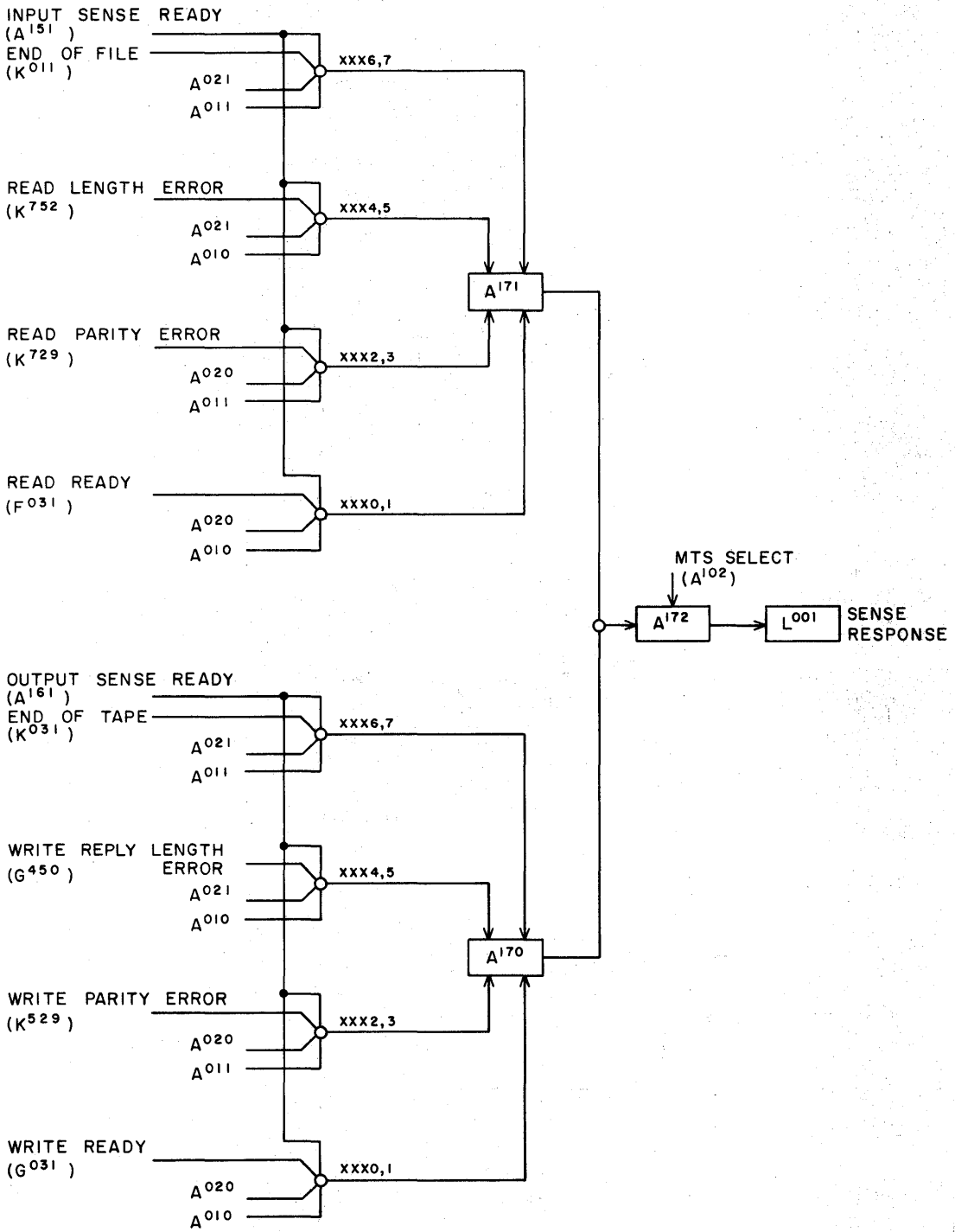


Figure 3-11. Sense circuit.

Because of the independent tape unit control circuits simultaneous rewind or rewind interlock operations are possible on the four tape units. The independent write and read circuits permit simultaneous read and write or backspace read and backspace write operations on two units.

Sense Circuit

The sense circuit, upon computer request, provides the computer with an indication of the status or condition of the tape units. The computer requests an indication of the status of a tape unit through a coded EF sense instruction. The sense circuit interprets the EF code received by the external function translator and transmits the desired information to the computer on the sense response line.

Figure 3-11 illustrates the sense circuit, the conditions which can be sensed and the EF codes for sensing the various conditions (see also table 3-2). Presence of an input or output channel tape unit condition when sensed completes the appropriate AND gate in the circuit and results in a "1" on the sense response line. The odd or even lower-order octal digit in the code enables the computer to interpret (internally) the synchronizer signal as either positive ("1") or negative ("0") regardless of the response.

Interrupt Circuit

The interrupt circuit, when so requested by the computer through the proper EF select code, will interrupt the computer program upon completion of any input or output channel select operation (see table 3-2) except rewind interlock. The EF select interrupt instruction is executed after a tape operation is selected. For those operations requiring a computer buffer it is executed after the buffer has been activated.

Figure 3-12 illustrates the interrupt circuit. An EF select code XXX4 selects interrupt to set the appropriate Read or Write Interrupt FF. At the end of the previously selected tape operation the appropriate A^{173} input AND gate is completed (see figure 3-10) allowing generation of a "1" interrupt signal to the computer.

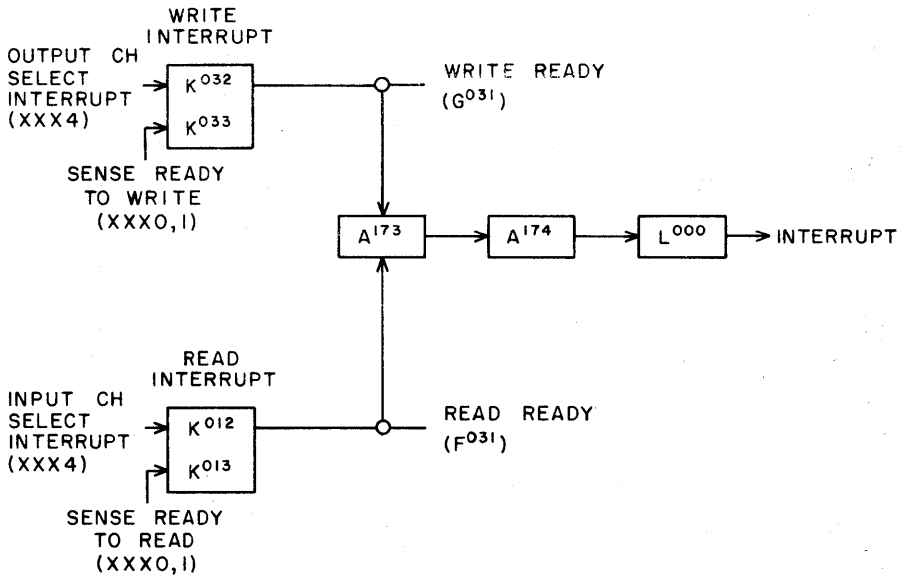


Figure 3-12. Interrupt Circuit.

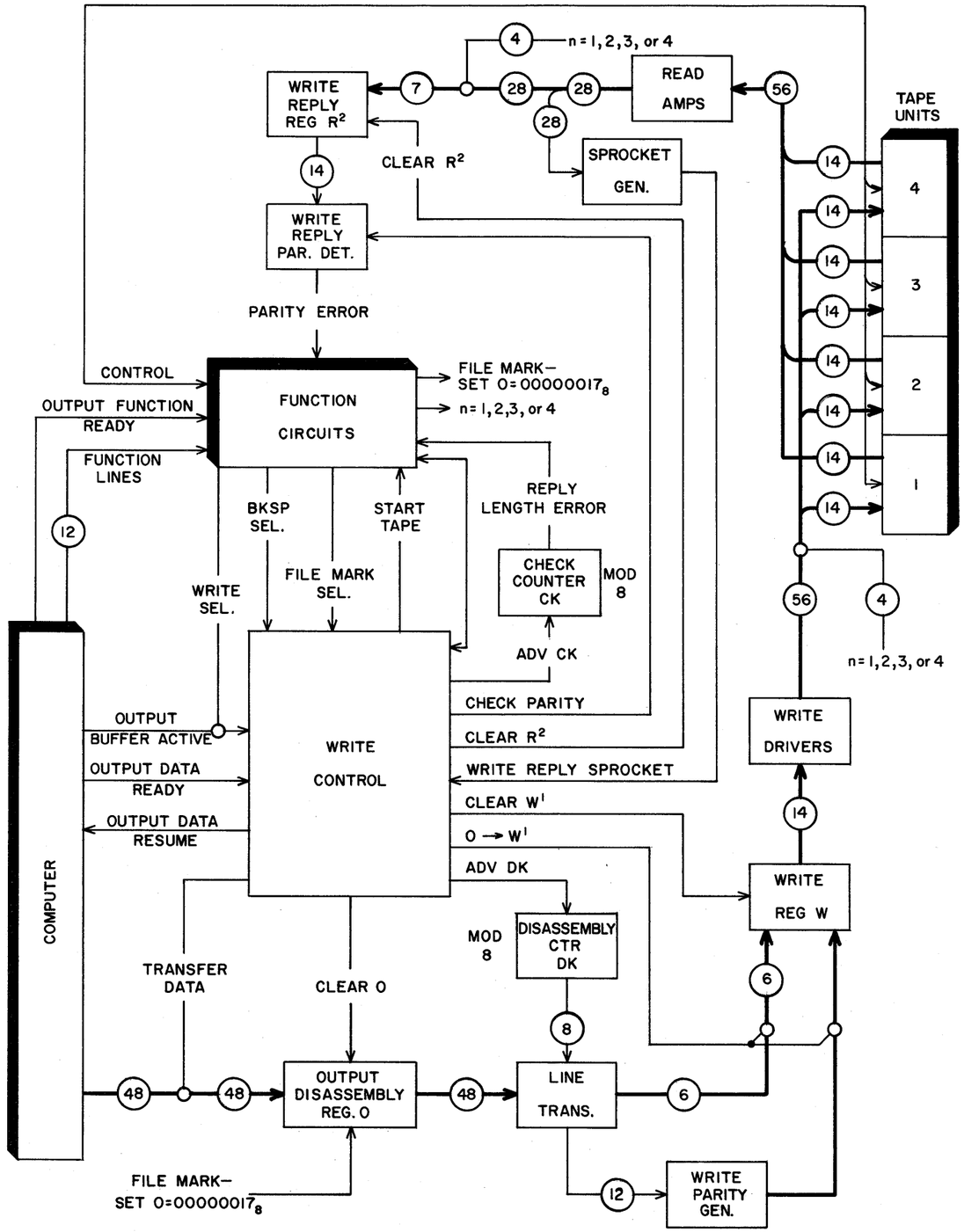


Figure 3-13. Simplified Block Diagram, Write Circuits.

In general, the static interrupt signal results in the computer program entering an interrupt subroutine which identifies the interrupting equipment and takes the steps necessary to satisfy the equipment. The subroutine recognizes the equipment which interrupted by sensing for a ready condition in those equipments for which interrupt was selected. Hence each time the computer selects external equipment interrupt it must enter the appropriate sense ready instruction for the equipment into the interrupt subroutine. A positive MTS response to a computer read or write ready sense request indicates the interrupting tape unit and clears the appropriate interrupt FF.

WRITE CIRCUITS

The primary function of the write circuits is to accept 48-bit computer output words and control the transfer of this data to the tape unit write heads for recording on the tape. This function, termed a write operation, is initiated by a computer EF select instruction requesting a write binary or write coded operation. Computer output data is presented to the synchronizer write circuits under buffer operation control as described earlier.

Secondary control functions of the write circuits which do not require a computer output buffer include:

1) Control of a backspace operation which moves the tape backward to the preceding record gap, as requested by an EF select instruction coded for an output channel backspace operation.
2) Recording a file mark on the tape which can signify end of a file of information consisting of one or more records, or can signify the end of information on the tape. The file mark is a 17 code recorded in coded format as a 1-character record. The mark is recorded in response to a computer EF select instruction requesting a write end-of-file mark operation.

Figure 3-13 shows in block form the individual write circuits which accomplish these functions and their relation to the function circuits and equipment in the system. Refer to this figure throughout the following discussions to locate each circuit and review its relation to other circuits.

Output Disassembly Register

The output disassembly register (O), holds each 48-bit computer word as it is being disassembled and recorded on the tape. The "1" bits in each computer output word are transmitted in parallel to the O register on an M → O command generated by write control. Before each transfer the register is cleared by a clear O command from write control. Inputs to the O register are made via M^{1--} series input conversion cards, (the last two superscript digits correspond to the associated register stage).

The 48-bit word is composed of eight 6-bit characters. The highest-order character in the register is recorded first, the second-highest order next, etc. The sequential extraction of characters for recording is accomplished by the line translator in conjunction with the disassembly counter, a modulus 8 counter.

For a write end-of-file mark selection the O register is set to 00000017_8 on a command from the function circuits, and characters are extracted and recorded as in a write operation.

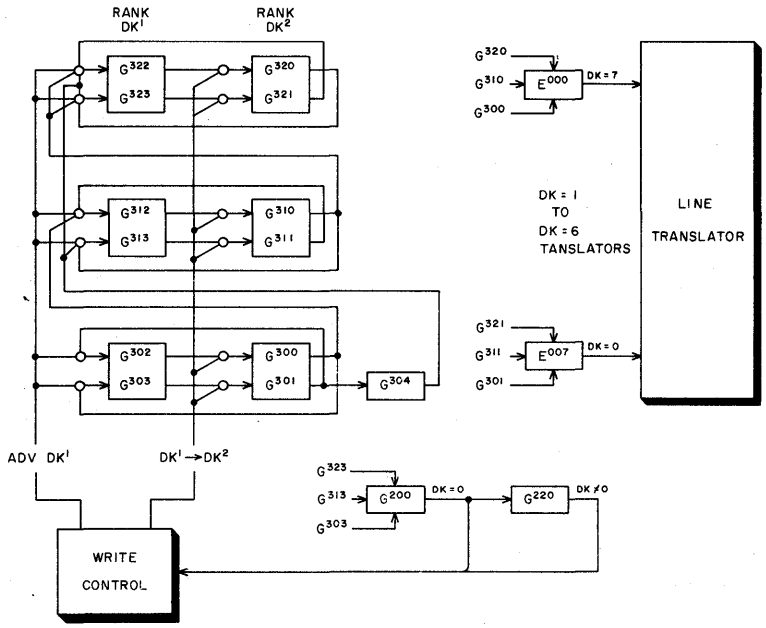


Figure 3-14. Disassembly Counter.

Disassembly Counter

The disassembly counter (DK) is a standard two-rank modulus 8 additive counter (figure 3-14). The counter controls the disassembly of 48-bit computer words into eight 6-bit characters. Counter operative signals and translation of the various counts are discussed here; operation of the counter is discussed in the computer instruction manual.

The counter is operated by repeated advance DK^1 and $DK^1 \rightarrow DK^2$ commands in that order. The advance DK^1 command stores the DK^2 count in DK^1; the $DK^1 \rightarrow DK^2$ command enters the DK^1 count in DK^2. DK is preset to 0 at the start of a write sequence through action of the write generator circuit in write control. This circuit produces counter commands until such time as DK = 0, as signalled by a "1" from translator G^{200}.

As shown in figure 3-14 translation of the 8 possible binary counts in DK is accomplished by single inverters. The DK = 0 (G^{200}) and DK $\neq$ 0 (G^{220}) commands are used by write control in determining completion of the 8 count DK cycle to enable generation of M $\rightarrow$ O and clear O commands.

Line Translator

The line translator sequentially extracts each 6-bit character from the O register and presents it to the write register input circuits for transfer to the magnetic tape. The highest-order character in the O register is extracted first, the next highest-order second, etc. Outputs of the line translator circuits are checked by the write parity generator circuit to determine parity for each character.

Character selection is accomplished by 12 single inverters of the I^{0--} series (figure 3-15), six of which have an odd third superscript digit and six an even. The odd inverters extract the four higher-order characters; the even inverters extract the four lower-order characters. The second superscript digit denotes the bit position in the character being translated. Each inverter gates the same bit position of four O register characters, gating is controlled by the count stored in the disassembly counter. A complete 8-count cycle of the counter extracts and presents to the write register all 8 characters. Circuit action in gating the even-order output of the O register stages is such that a "1" in a given stage is represented by a "1" from the associated I^{0--} inverter. Note that when odd inverters are being sampled all even inverter outputs are "1" and vice versa to enable transfer to the write register.

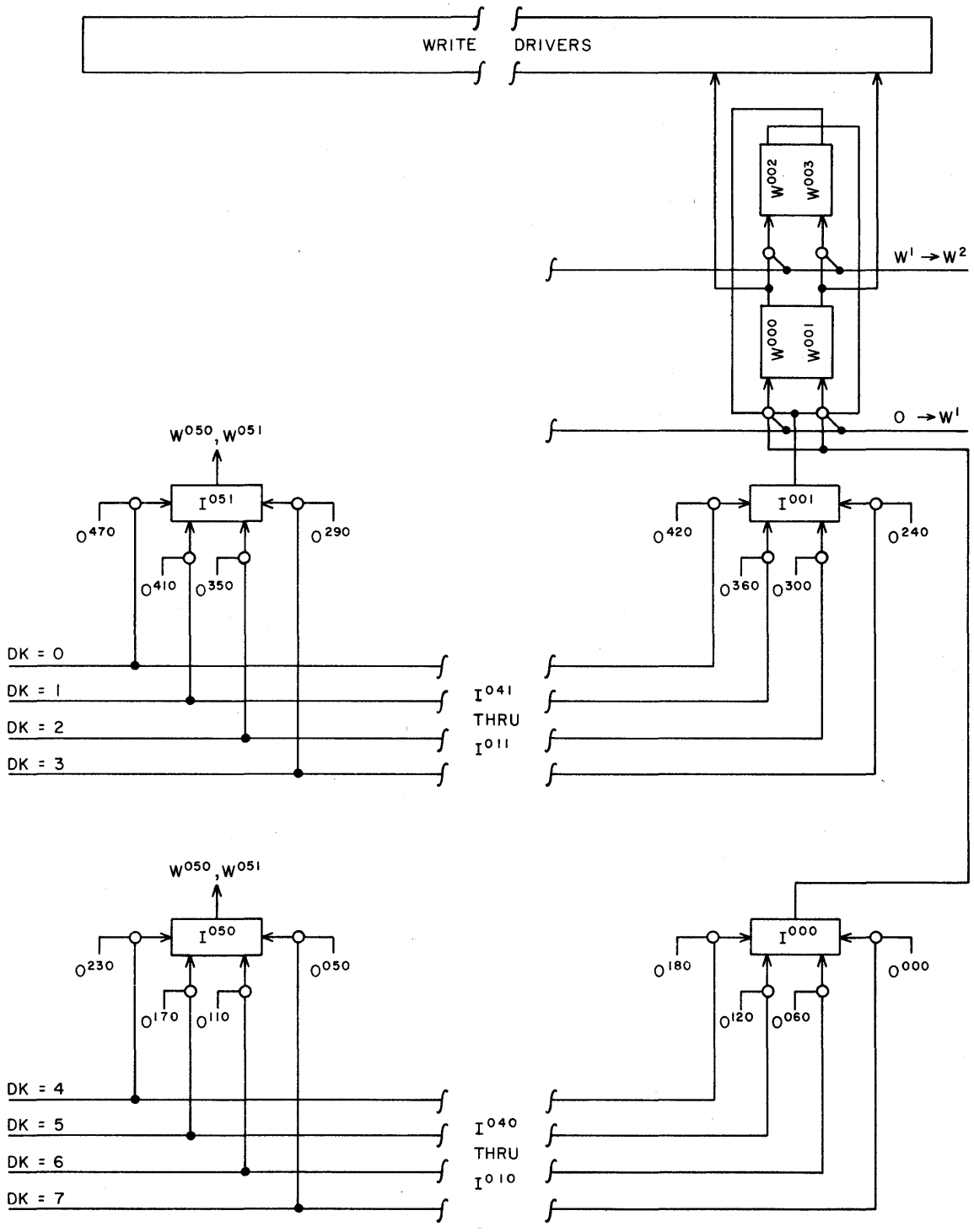


Figure 3-15. Typical Line Translator Circuit and Bit Transfer to Write Register.

Write Parity Generator

Each line recorded on the tape is composed of a 6-bit character and its parity bit for a total of 7 bits. Parity bits are used to check errors in the transfer of 6-bit characters to and from tape. The write parity generator makes the total number of "1" bits in a line odd if binary format is selected or even if coded format is selected by the EF select instruction. Each character presented to the write register by the line translator is translated by the parity generator to determine if the character contains an odd or even number of "1" bits. The result of the translation is stored as a parity bit in the highest-order stage of the write register.

As shown in figure 3-16, the circuit divides the 6 bits in each character into two 3-bit groups and checks each group for an odd or even number of "1" bits. The results of the two groups are compared and the final result checked against the binary or coded selection to determine necessity of a "1" parity bit. Of the 8 possible binary combinations in each 3-bit group, 4 contain an odd-number of "1" bits, for example, 001 = 1, 010 = 2, 100 = 4, and 111 = 7. The generator senses for these groups by gating appropriate combinations of enables from the line translator inverters. A "1" write parity signal is generated from W^{230} if an odd number of "1" bits is found in the two groups in a write coded operation, or if an even number of "1" bits is found in a write binary operation.

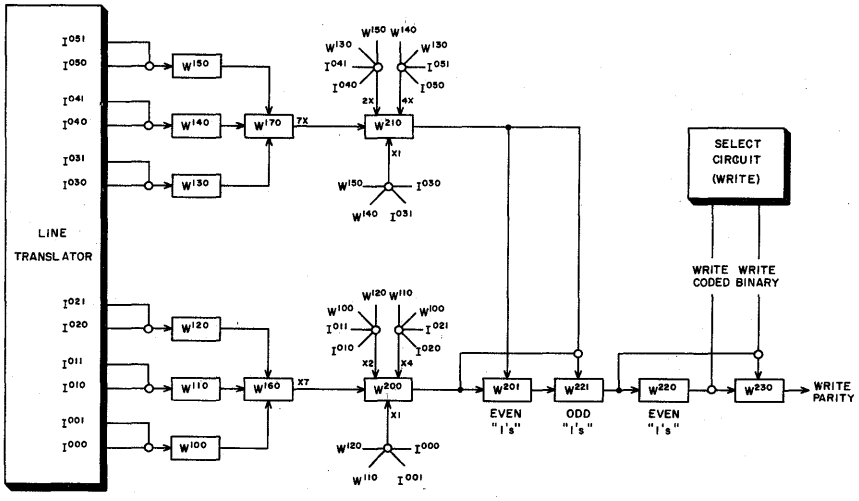


Figure 3-16. Write Parity Generator.

Write Register

The write register (W) is a 7-bit register which holds each line of data as it is being recorded on the magnetic tape. Each 6-bit character and its parity bit (one line) are transferred to W from the line translator and write parity generator circuits respectively. The 6-bit character is transferred to the lowest-order 6 stages of W, the parity bit is transferred to the highest-order stage of W. The transfer to W occurs in such a manner that each "1" bit in a line toggles an associated stage of W to its opposite state. This action produces the change-on-ones recording pattern necessary for compatibility with IBM tape units.

The W register consists of two ranks, W^1 and W^2. A typical stage of the register is shown in figure 3-15. As shown, each line is toggled into W^1 on an $O \rightarrow W^1$ command, a one μsec wide pulse generated by write control. The change in state of a W^1 FF is sensed by a corresponding write driver circuit which then acts to reverse the direction of current flow through its related write head to accomplish recording of the data. The

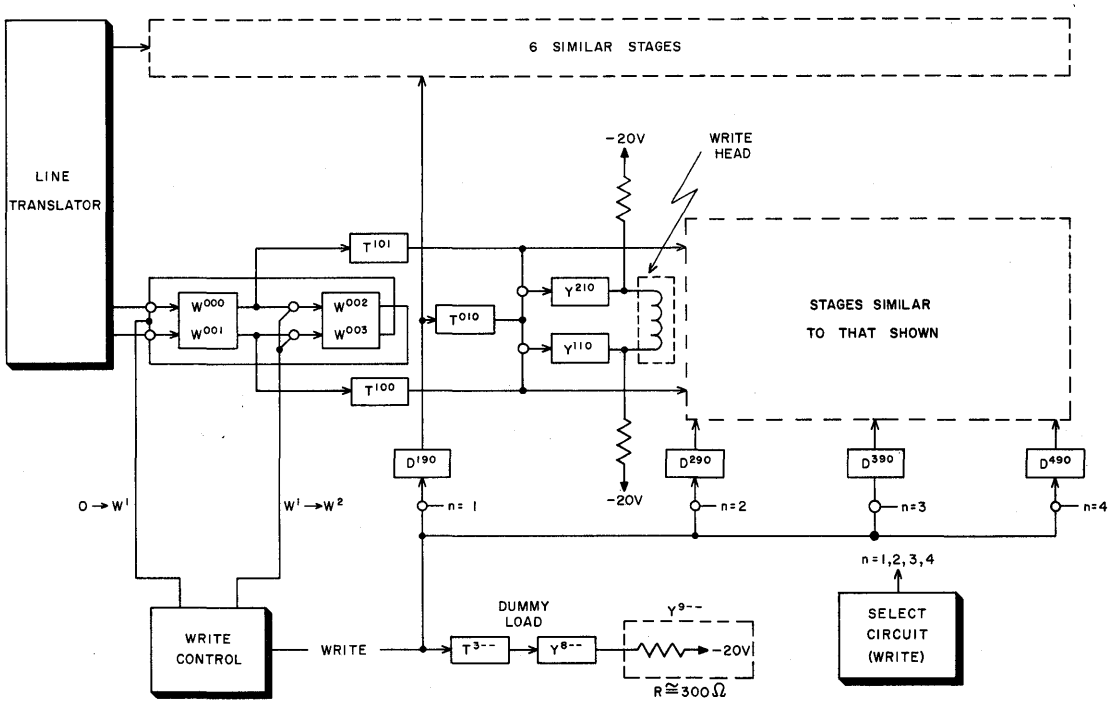


Figure 3-17. Typical Write Driver Circuit.

content of W^1 is transferred to W^2 by the $W^1 \rightarrow W^2$ command to prepare W^1 for receipt of the next line. The operation of each stage of W in producing the change-on-ones pattern is likened to the first stage of a standard counter which is toggled to its opposite state each time a "1" advance command is received.

Not shown in the figure is the clear W^1 command which clears W^1 prior to a write sequence and is generated 133 μsec after the last character in each record to write a check character for the record. The check character makes the total number of "1" bits even in each of the seven longitudinal data tracks on the tape and is recorded for IBM compatibility.

Write Drivers

The write drivers sense the change in state of rank W^1 Write Register FFs and act to reverse the direction of current flow in the tape unit recording heads for each change. The current reversal in the recording heads results in reversing the polarity of the head magnetizing flux to record the change in W^1 as a "1" on the tape.

Figure 3-17 shows the driver circuit of tape unit 1 that is associated with stage 0 of the W register. Prior to an EF write selection, W^1 is cleared and no head current flows; however, dummy load current flows so that the power supply load is approximately constant under non-writing conditions. Following the EF select instruction one of the 4 D^{---} terms is selected to correspond to the unit selection stored in the write select circuits. Receipt of the computer output buffer active signal by write control starts tape moving and turns off the dummy load current. Coincident with this the input AND gate is completed at the previously selected D^{---} term to turn on head current. Assuming unit 1 is selected, the Y^{210} output at this time is at ground potential and Y^{110} output appears as an open circuit so that current flows from the current source at the lower part of the diagram through the head and Y^{210} to ground. It can be seen that subsequent changes in the state of W^1 will cause a reversal in the head current and corresponding flux changes. Accordingly, a change in flux sensed during reading indicates a "1" read from the tape.

Write Reply Register

During write, write end-of-file mark, and backspace operations each recorded line on the tape is read into the write reply register (R^2) and checked for a parity error by the write parity detector circuit. Recorded tape data is sensed by the read heads and returned to R^2 via read amplifiers. Because of the mechanical spacing of the read and

write heads, during write and write end-of-file mark operations a line is read into R^2 approximately 2.6 ms after it is recorded. Each line remains in R^2 for a period sufficient to allow the parity circuits to register a possible parity error condition. The register is cleared initially and after each parity check on a clear R^2 command from write control. Write control is informed of each new line in R^2 by the sprocket generator circuit. Appropriate gating circuits at the input to R^2 are activated by the tape unit selection stored in the write select circuits to insure that R^2 receives data from the writing tape unit.

Write Reply Parity Detector

The write reply parity detector checks for a parity error condition on each line read into the R^2 register during binary or coded write operations, a write end-of-file mark (coded format), or a backspace operation (format dependent on previous write operation selection). The circuit stores an error condition in a FF and informs the sense circuit so that the computer can determine an error condition. Error conditions are signalled

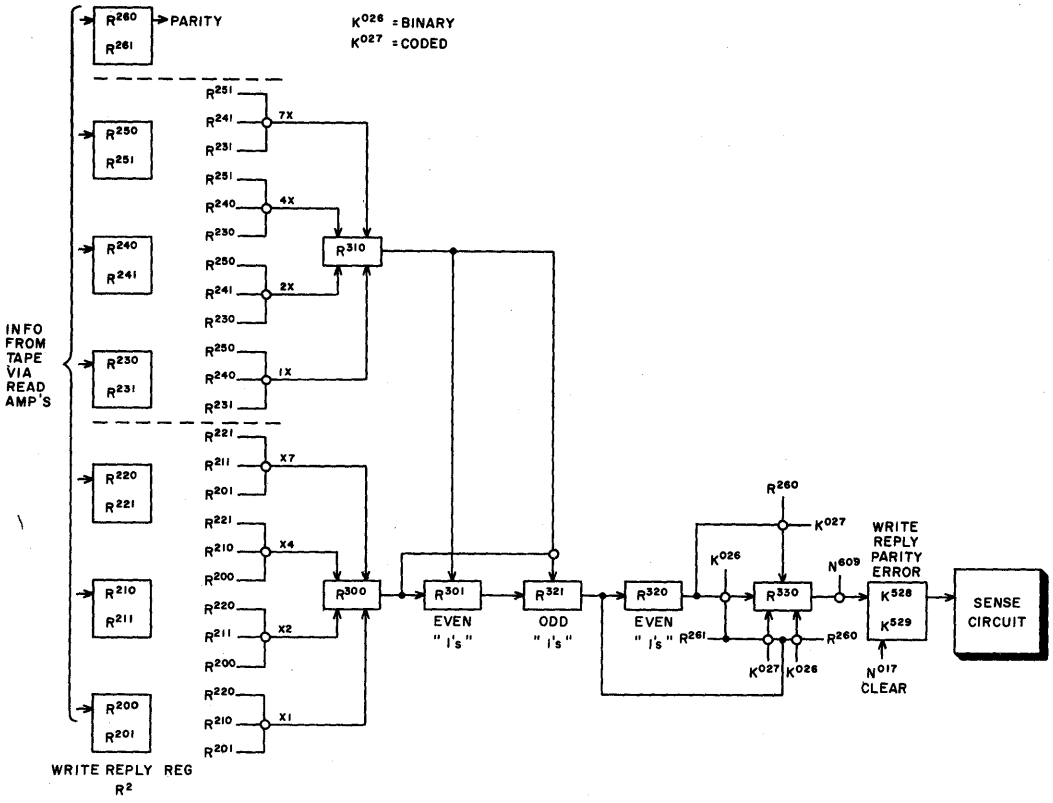


Figure 3-18. Write reply parity detector.

for any one of the following combinations sensed in R^2:

write operations during binary	if parity is a "1" and an odd number of "1" bits are found in the 6-bit character
	if parity is a "0" and an even number of "1" bits are found in the 6-bit character
write operations during coded	if parity is a "1" and an even number of "1" bits are found in the 6-bit character
	if parity is a "0" and an odd number of "1" bits are found in the 6-bit character

Figure 3-18 shows the circuit for detecting the error conditions described above. Circuit operation is similar to that of the write parity generator circuit. Detection of one of the above noted error conditions results in a "1" from R^{330} to enable the N^{609} pulse from write control to set the error FF. The error FF remains in a set state after the error is sensed and is not cleared until such time as a new write, write end-of-file mark, or backspace operation is selected.

Check Counter

The check counter (CK) counts each line read from the tape during a write, write end-of-file, or backspace operation. If the number of lines read in a record is not an integral multiple of 8 the counter signals a "write reply length error" to the sense circuits to enable the computer to sense the error condition. The error indicates that one or more lines in a record were dropped or added during the read back sequence. In general, the error could indicate: faulty recording circuits or tape, dust on the tape, or reading of extraneously recorded data. The error is always signalled for a backspace operation (because the check character is read) and for a write end-of-file mark operation (because only two lines are recorded); in these cases it has no meaning for the computer.

The counter is a standard 2-rank modulus 8 additive counter similar to the disassembly counter described earlier. A single inverter translates the counter content so that if CK ≠ 0 at the end of an operation an error is signalled. The counter is advanced one count for each line read from the tape as signalled to write control by the sprocket generator circuit. The counter is cleared at the start of each operation to insure that error conditions are not accumulative.

Write Control

The write control circuits direct operation of the individual write circuits to accomplish a write, write end-of-file mark, or backspace operation. For discussion purposes the circuits are divided as follows:

1) Tape Motion - initiates tape starts and stops
2) Write Generator - generates commands to sequence writing
3) Write Reply Sequence Control - generates commands to sequence read-back of written data for error checking

Each circuit is discussed with reference to a simplified block diagram. Omitted from the diagrams are many components included in the actual circuit to compensate for circuit loading, generation of the proper logic signal, etc. These circuit details are given in the maintenance diagrams in volume 2.

Tape Motion (figure 3-19)

Write Operation

The circuit is activated following an EF select write instruction by the computer output buffer active signal. If the selected tape unit is at load point a 200 ms delay is taken before the Tape Motion FF is set to start tape; if not at load point the FF is set and the tape started immediately. Receipt of the computer signal also informs the function circuits that the write circuits are busy. The 200 ms change direction delay allows stabilization time for the tape unit vacuum loops for the particular case when a rewind operation is completed immediately preceding the write selection.

The set state of the Tape Motion FF turns on write head current and informs the write select circuits to start tape moving. Tape is brought to full speed within 2.5 ms of the start signal. When at load point, the Write Load Point FF is set as Tape Motion FF is set. The state of the former FF selects the appropriate 40 ms or 4 ms write delay.

When at load point the 40 ms delay allows the reflective spot on the tape to move past the write head (and the read head) before writing begins. Approximately 6 inches of tape pass the write heads before writing begins to provide compatibility with IBM reading equipment. If not at load point, the 4 ms delay allows time for tape to come up to full speed before writing begins and fixes part of the inter-record gap (figure 3-22, part a). Elapse of the appropriate delay sets the Write Control FF to alert the write generator and write reply sequence circuits of tape motion. This allows writing to begin and the write reply circuits to respond to the recorded data.

At the end of operation, the write reply circuit generates an end-of-record signal to clear the Tape Motion FF which in turn clears the Write Load Point FF and initiates a tape stop. After a 200 ms delay the Write Control FF is cleared to end the operation. Clearing of the latter FF turns off write head current and informs the function circuits that the write circuits are no longer busy.

The 200 ms delay insures that the tape unit vacuum loops stabilize after the tape is stopped to accommodate a possible change in tape direction in an immediately following output channel instruction, (backspace, for example).

Write End-of-File Mark

Circuit operation for this selection is identical with a write operation except:

a) The Tape Motion FF is set as a result of the file mark active signal generated by the write select circuits upon storing a write end-of-file mark EF code.

b) A 40 ms load point delay is always taken prior to writing the file mark. This spaces the file mark 6 inches from the check character of the previous record.

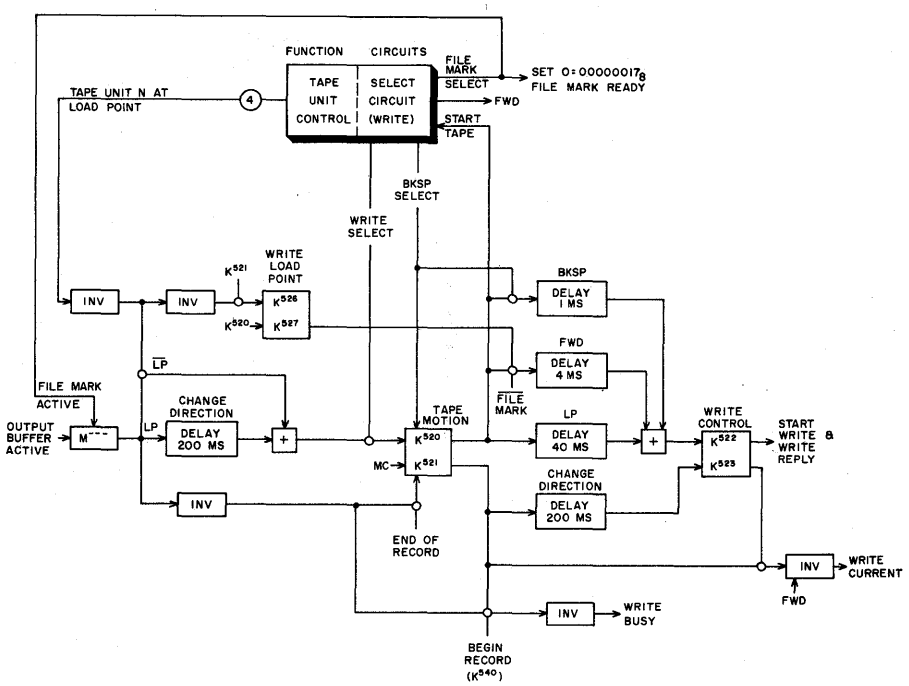


Figure 3-19. Write Control, Tape Motion Circuit.

Backspace Operation

Circuit operation for this selection is identical with a write operation except:

a) The Tape Motion FF is set immediately upon receipt by the write select circuits of a backspace EF code.

b) Write current is not turned on.

c) A 1 ms delay is incurred after the tape is started prior to turn-on of the write reply circuits. (Initially the read head is in closer approximation to the data to be read in a backspace operation than it is in a write operation, therefore the reply circuits must be enabled sooner to permit reading of the record check character.)

Write Generator (figure 3-20)

The write generator is a clocking circuit which generates the commands necessary to accept computer output information and record it on the tape.

Write Operation

Writing commands are sequenced by operation of FFs $K^{512/513}$, $K^{514/515}$, and $K^{516/517}$. The three FFs and interconnecting delays form a self-clearing 30 KC pulse-generating network for the $O \rightarrow W^1$, Adv DK^1, $W^1 \rightarrow W^2$, and $DK^1 \rightarrow DK^2$ commands, each of which is a 1 μsec pulse. As power is applied initially to the synchronizer circuits, the three FFs are set or cleared in a random manner. The nature of the 1 μsec delay elements is such that the three FFs cycle in a "set-set-set, clear-clear-clear" mode until DK = 0 to stop the cycle with the three FFs cleared. At this time DK and the W register are cleared. With the Write Control FF set indicating tape motion, the circuit is triggered by a computer output data ready signal.

The output data ready, after a short delay, sets the Data Ready FF. This allows transfer of a computer word to the O register via the $M \rightarrow O$ command and generates an output data resume to acknowledge acceptance of data. After a 1 μsec delay $K^{512/513}$ is set to initiate the 30 KC pulse-generating network.

The sum of the delays in one cycle of the write generator is 33 μsec, the period of a 30 KC generator. The 1 μsec delay in the set input to $K^{512/513}$, triggered by $K^{510/511}$, forms a part of the 33 μsec generator period when writing the first character of each word. Writing commands are generated in the following order for each cycle of the

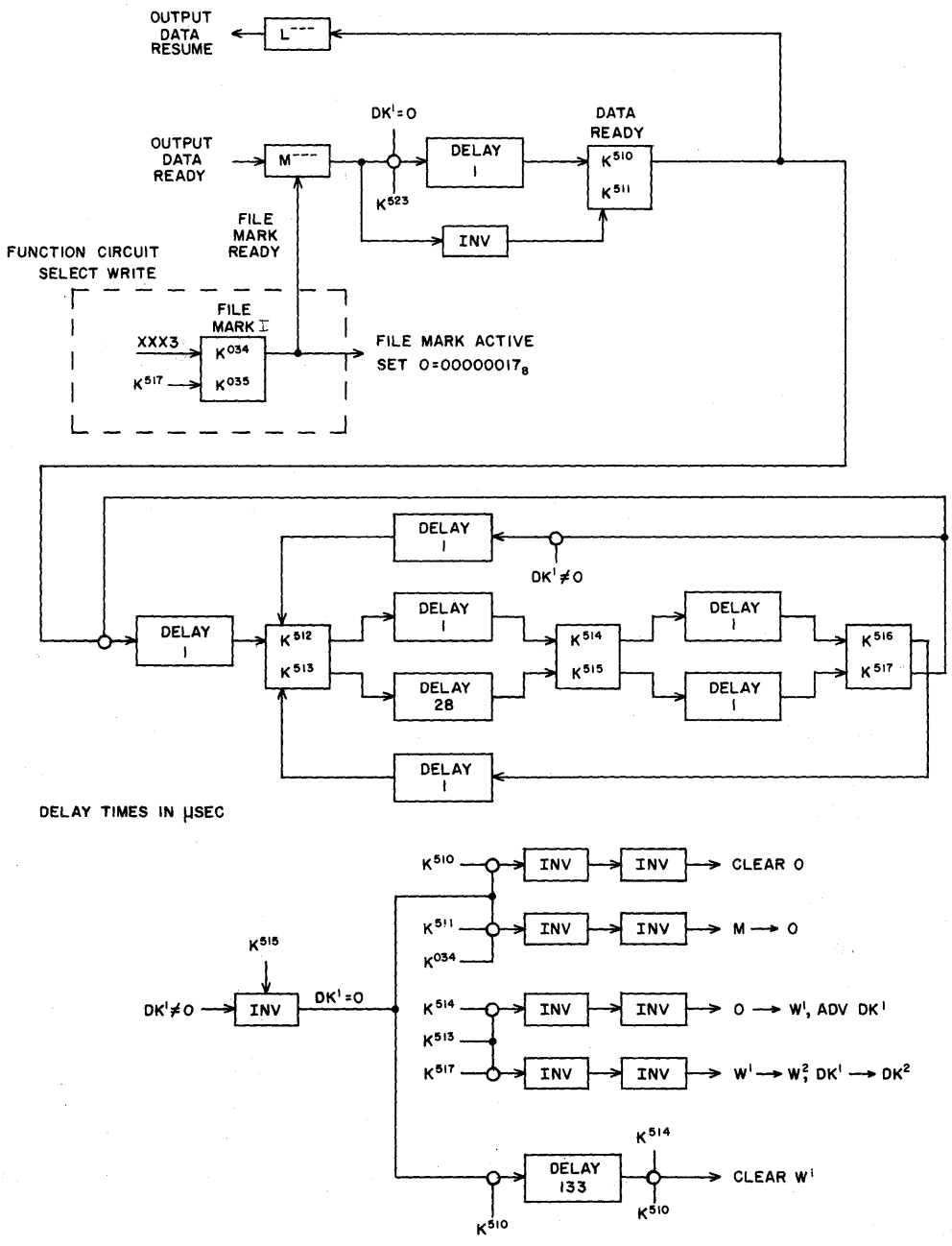


Figure 3-20. Write Generator.

generator: 1) O → W^1 and Adv DK^1; 2) W^1 → W^2 and DK^1 → DK^2

The above commands are produced 8 successive times to record the 8 characters in the 48-bit computer word stored in the O register. With DK cycled to O, the clear O command is generated and, after a short delay (which times the clear O command) the next computer word is accepted by the M → O and output data resume commands to repeat the cycle.

The absence of a computer word when DK = 0 indicates the end of the computer buffer and the 133 μsec delay is initiated after which the W^1 register is cleared to record the longitudinal record check character (figure 3-22, part b).

Write End-of-File Mark

Circuit operation for this selection is similiar to a write operation except that:

1) The 30 KC write generator circuit is initiated by the file mark ready signal generated as a result of storage in the write select circuits of an EF select write end-of-file mark code (XXX3).

2) Setting $K^{516/517}$ during the first character cycle of the write generator clears the File Mark FF to enable recording of the file mark check character when the one word recording cycle of the write generator is complete.

Backspace Operation

The circuit is not used during a backspace operation.

Write Reply Sequence Control (figure 3-21)

The write reply sequence control consists of a clocking circuit for generating the commands necessary to sequence read back of tape data for error checking, and a circuit for sensing the end of a record.

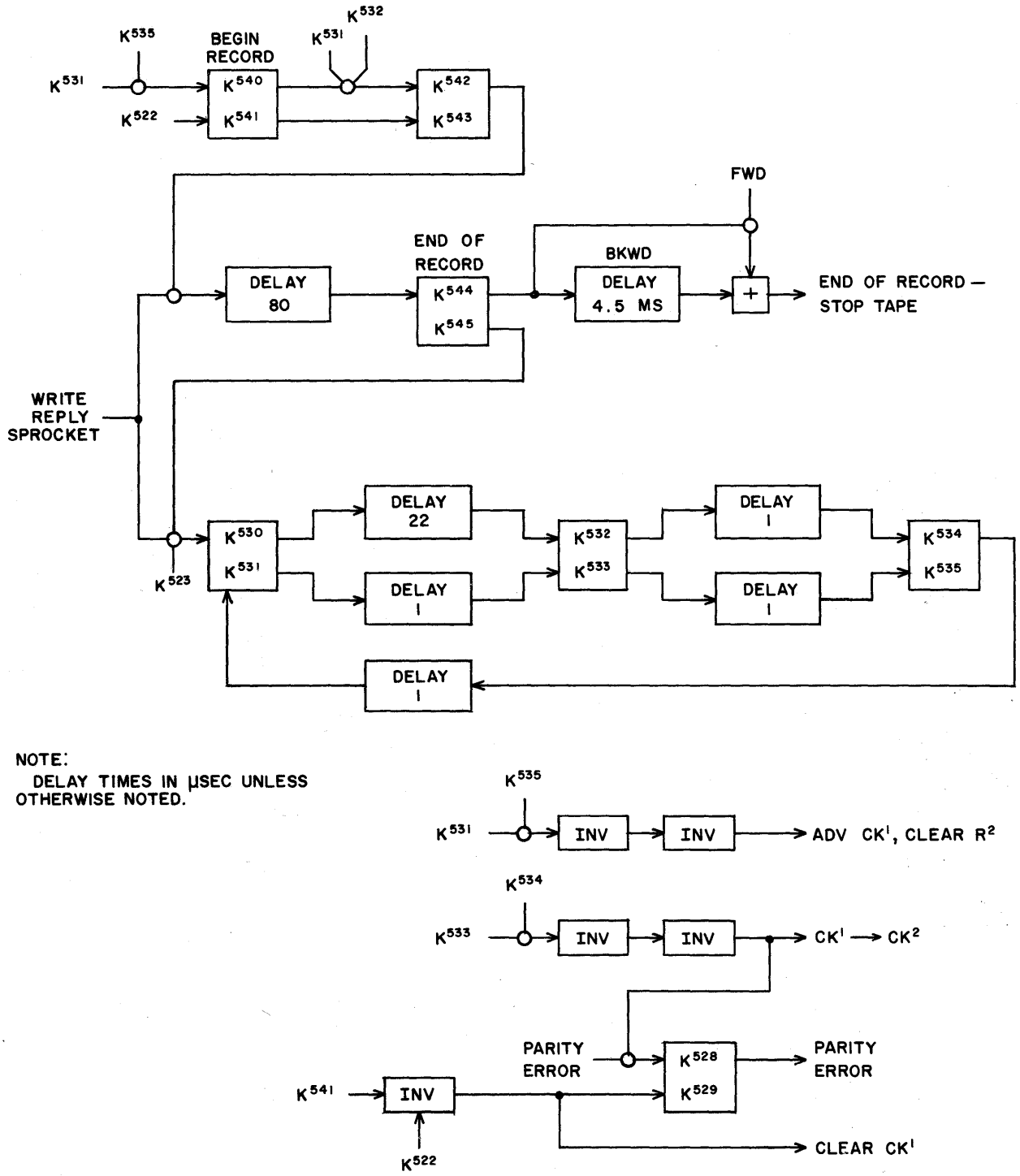


Figure 3-21. Write Reply Circuit.

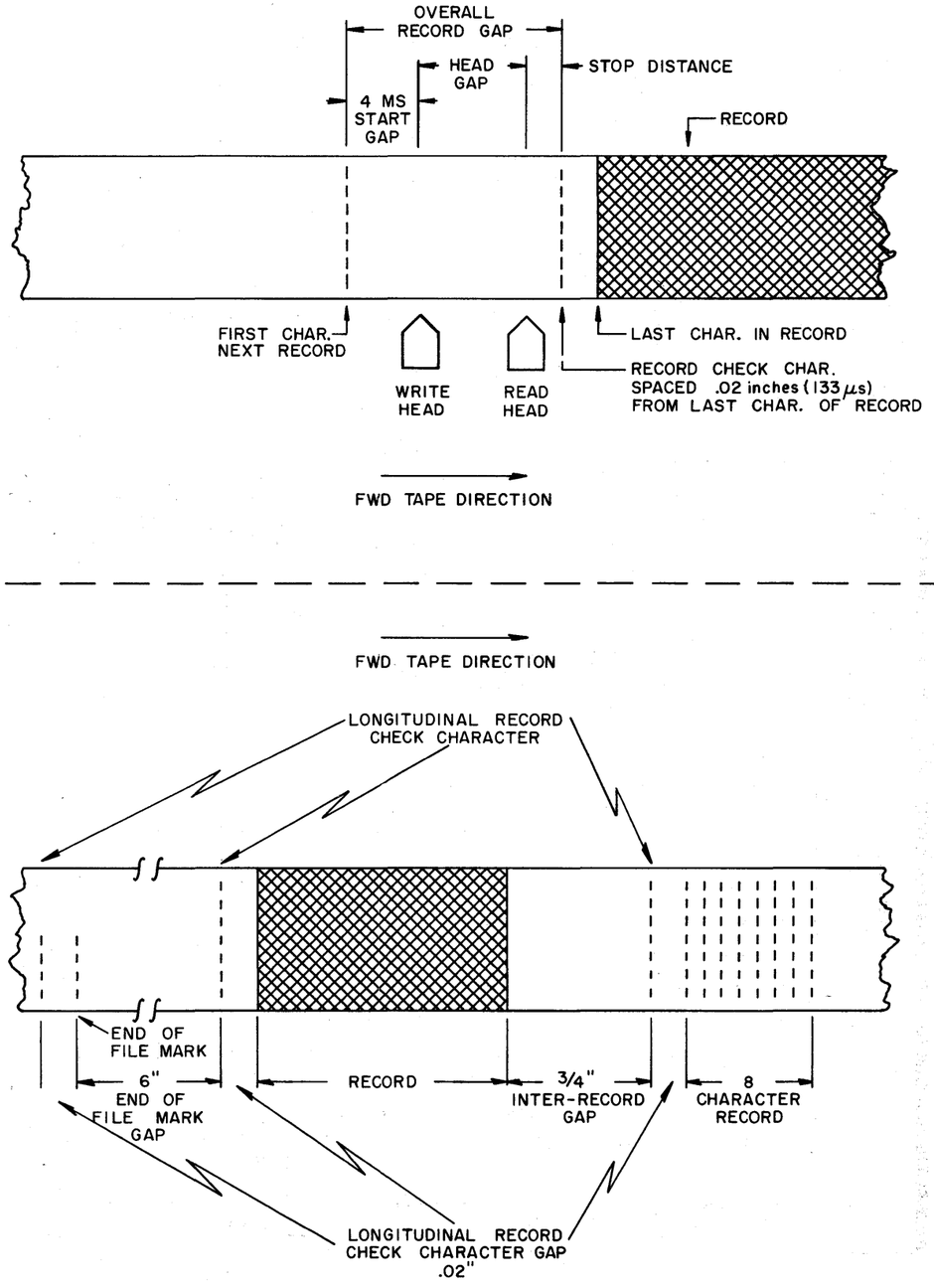


Figure 3-22. Arrangement of Data on Tape.

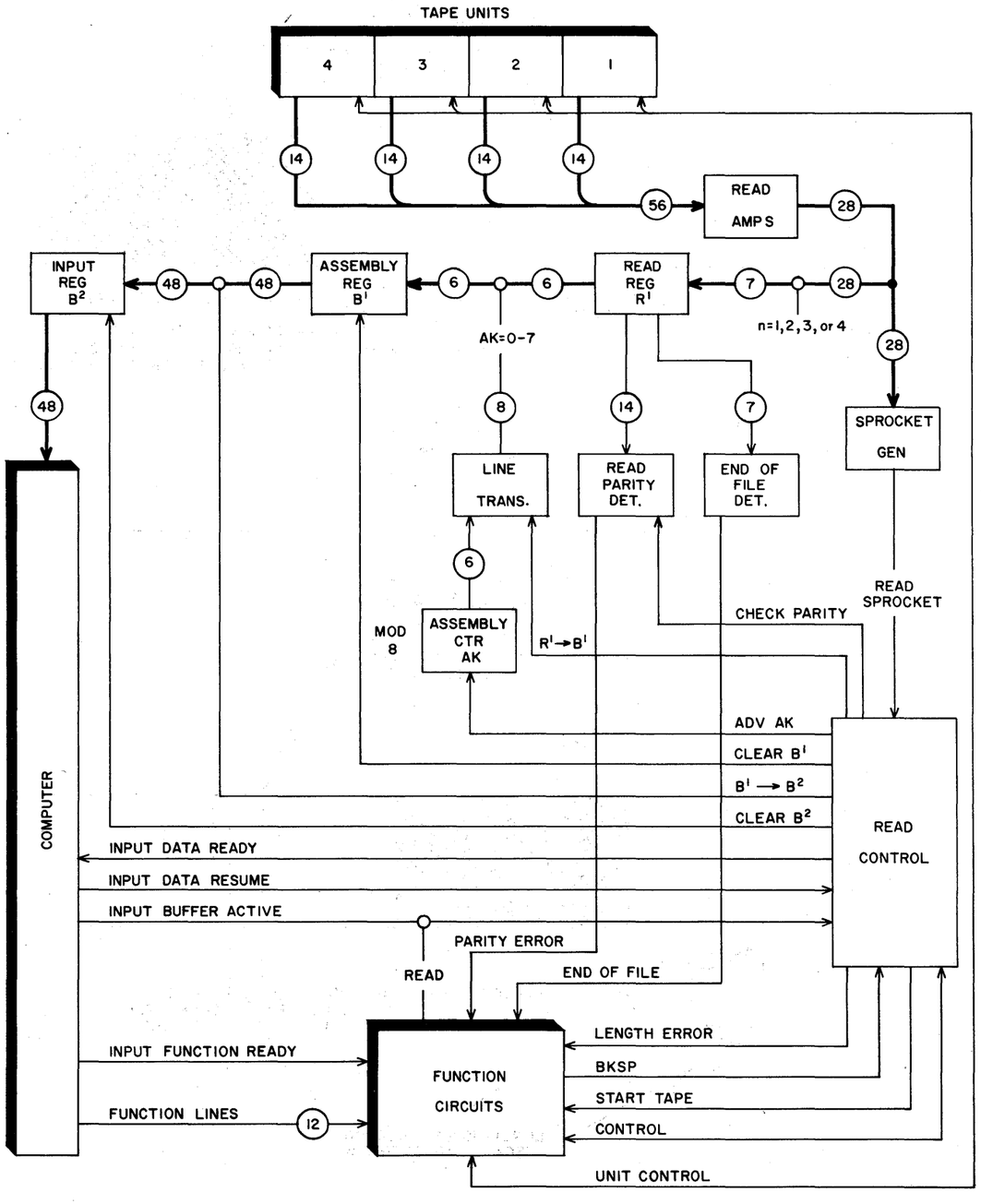


Figure 3-23. Simplified Block Diagram, Read Circuits.

Write Operation

The clocking circuit, enabled by the set state of the Write Control FF, is triggered by the write reply sprocket signal generated by the first "1" bit in each line read from the tape. The period of the circuit is 26 μsecs. The first 22 μsecs of the period compensate for tape skew and allow all bits in a line to read into R^2 and stabilize prior to performing a parity check. During the last four μsec of each period, one μsec pulses are generated in the following order:

1) $CK^1 \rightarrow CK^2$, and check parity
2) clear R^2, and Adv CK^1

The first tape character read sets the Begin Record FF; the second character read sets $K^{542/543}$ to allow each subsequent character read to trigger the 80 μsec delay. Absence of tape data for 80 μsec after at least two lines are read is sensed as an end-of-record condition and the End-of-Record FF is set to signal the condition. The latter action clears the Tape Motion FF to initiate stopping the tape. Because of mechanical stop time consumed by the tape unit, the tape travels a short distance after the above FF is cleared before a complete stop occurs. Figure 3-22, part a, shows how this distance plus the tape start time and head gap combine to fix the record gap.

Write End-of-File Mark

Circuit operation for this selection is identical with that in a write operation. The 80 μsec delay expires after $K^{542/543}$ is set (by the file mark check character) to signal the end-of-record.

Backspace Operation

Circuit operation for this selection is identical with a write operation except a 4.5 ms delay is incurred prior to clearing the Tape Motion FF. The delay in this case allows the read and write heads to be positioned in the record gap approximately the same as when completing an operation in the forward direction.

READ CIRCUITS

The primary function of the read circuits is to assemble tape data into 48-bit computer words and to control transfer of this data to the computer. This function, termed a read operation, is initiated by a computer EF select instruction requesting a read binary or read coded operation.

A secondary function of the read circuits not requiring a computer input buffer is to control an input channel backspace operation. As in an output channel (write) backspace operation, the input channel backspace operation moves the tape backwards to the preceding record gap as requested by an EF select instruction coded for an input channel backspace operation.

Figure 3-23 shows in block form the individual read circuits which accomplish the above functions and their relation to the function circuits and other system equipment. Refer to the figure throughout the following discussion to locate each circuit as well as to review the relation to other circuits.

Read Amplifiers

The read amplifiers amplify the tape data signals induced into the read heads as the tape moves past the heads. Outputs of the amplifiers are routed through gating circuits to read register R^1, write reply register R^2, and the sprocket generator circuit.

Figure 3-24 shows the read amplifier circuits for tape data track 0 and related circuits. A "1" is read from the tape each time a change is sensed in the polarity of the tape flux pattern. The voltage induced into the head winding and appearing at either end of the winding to represent a "1", is pre-amplified by the Y^{3--} circuit (type 71 card) and passed to a final amplifier (type 72 card) where it is converted to a single-ended signal. The final amplifier output is converted to standard logic circuit voltages by the I^{1--} series circuits which produce "1" outputs for each "1" read from the tape. The electronic operation of the type 71 and 72 cards is discussed at the end of the chapter.

Sprocket Generator

The sprocket generator circuits issue a timing signal to the read and write control circuits to inform them of each line of data read from the tape.

Figure 3-24 shows the circuit for tape unit 1; a similar circuit exists for each tape unit. Unit identification is provided by the middle superscript digit. The two single inverters provide an OR gate for the seven tracks so that the read and/or write control circuits respond to the first "1" bit read in a line. A tape "1" is represented by a "0" timing signal.

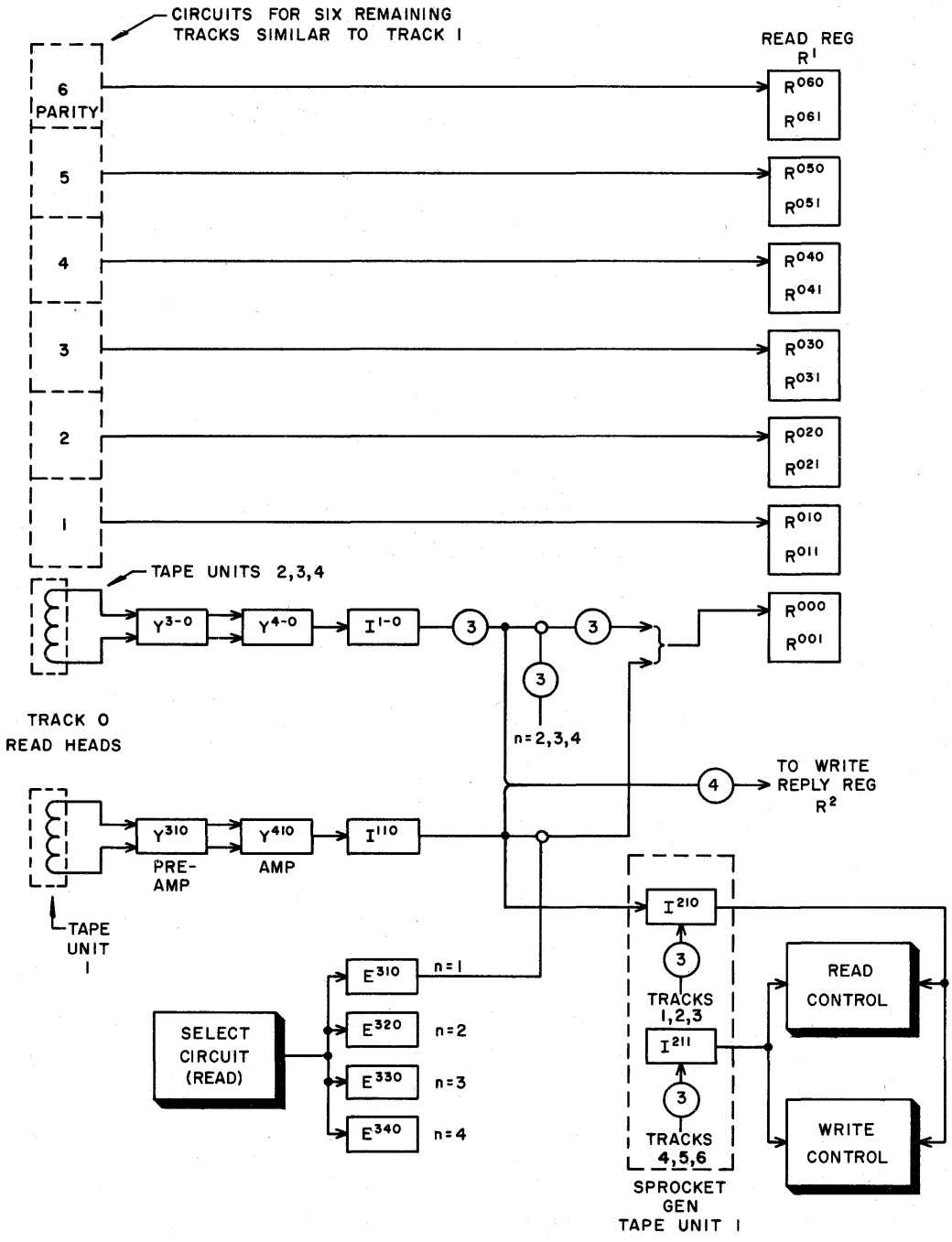


Figure 3-24. Read Amplifier Circuits.

Read Register

The seven-bit read register (R^1) receives each line of tape data during read forward or backspace operations. The lowest-order six stages of R^1 receive the information character, the highest-order stage receives the parity bit. Figure 3-24 shows how the R^1 register receives data from the read amplifiers.

During read forward operation only, the information characters of eight successive lines of tape data in R^1 are assembled into a 48-bit word in the assembly register for subsequent transfer to the computer. No tape data is transferred to the computer during backspace operations. Initially and after assembly of each line, R^1 is cleared by a clear R^1 command from read control.

Each line in R^1 is checked for a parity error and for an end-of-file mark (17 code) by appropriate detection circuits. Because of the many R^1 outputs required by these circuits and the assembly register each even-order output of the lowest-order six stages of R^1 is equipped with a single-inverter slave (not shown in figure 3-24) represented in the equation file by R^{002} through R^{052} symbols.

As shown in figure 3-24, data from the reading tape unit is gated into R^1 in accordance with the unit selection stored in the read select circuit. A similar circuit, activated by a different tape unit selection stored in the write select circuit, allows simultaneous gating of write reply information into write reply register R^2.

Assembly Counter and Translator

The assembly counter (AK) and translator circuits direct assembly of tape data in the 48-bit assembly register. The counter is a standard 2-rank modulus 8 additive counter similar to the disassembly counter. The translator circuit translates the binary counts in AK into octal equivalents and gates the tape data in R^1 into the assembly register.

Figure 3-25 shows AK and the translator. The counter, represented by F^{100} symbols in the equation file, is operated by repeated Adv AK^1 and $AK^1 \rightarrow AK^2$ commands in that order. The commands are generated by read control responding to sprocket generator signals. Initially AK is cleared so that when read control generates the $R^1 \rightarrow B^1$ command for the first record character, N^{327} gates the character in R^1 into the six highest-order stages of B^1. The cycle continues through AK = 7 with assembly of each character advancing AK to select the B^1 location for the next character. Following assembly of each eighth character, as signalled to read control by AK = 0 and AK $\neq$ 0 commands, the

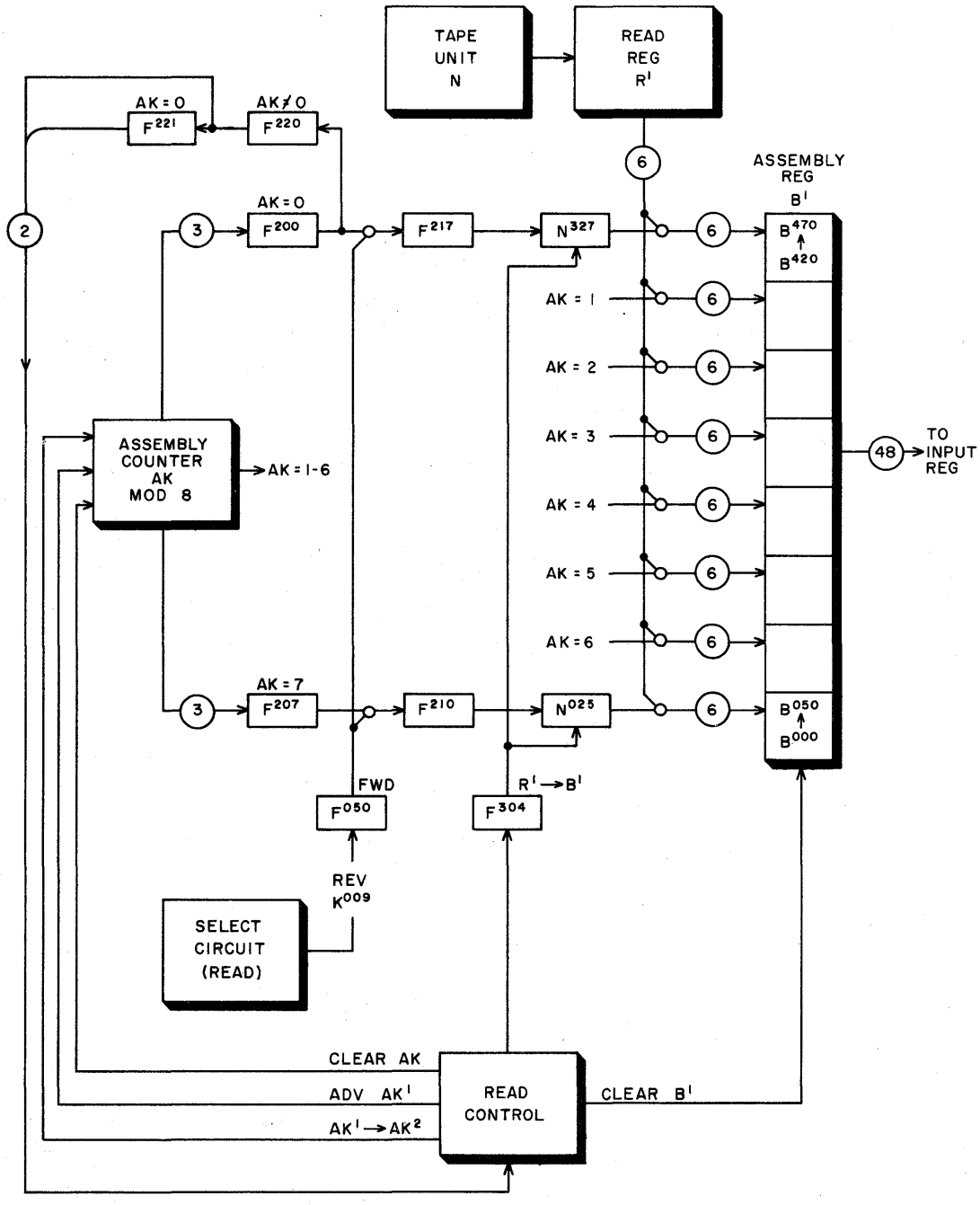


Figure 3-25. Assembly Counter and Translator.

48-bit B^1 word is transferred to a 48-bit input register (B^2) for transfer to the computer. The cycle repeats then.

Assembly Register

The assembly register (B^1) is a 48-bit register into which are assembled the information characters of eight successive lines of tape data. Character assembly (controlled by the assembly counter) is such that the first recorded character of each word is always assembled in the highest-order stages of B^1 (figure 3-25). Only the "1" bits of information characters are transferred into B^1, accordingly B^1 is cleared prior to assembly of each 48-bit word. An assembled word is transferred in parallel to the Input Register.

Input Register

The input register (B^2) is a 48-bit register which buffers transfer of assembled tape words in the B^1 register to the computer I/O section. The "1" bits in the B^1 register are transferred in parallel to the previously cleared B^2 register on a $B^1 \rightarrow B^2$ command from read control. Presence of each word in B^2 is signalled to the computer by an input data ready command from read control.

The B^2 register is necessary as a buffer because of the absence of a similar register within the computer (see paragraph on computer I/O characteristics) and because the computer may not be able to accept an assembled tape word before the first character of the next tape word is read. Tape characters are read at 30KC rate or approximately one every 33 μsecs, whereas the computer may require up to 200 μsec to process a channel if all I/O channels are busy.

Read Parity Detector

The read parity detector checks for a parity error condition on each line read into the R^1 register during binary or coded read or backspace operations. The circuit stores an error condition in a FF and informs the sense circuit so that the computer can determine an error condition. Except for symbol assignments (read circuit uses R^{1--} and K^{7--} symbols), this circuit is identical with the write reply parity detector.

End-of-File Detector

The end of a file of information (or the end of information on the tape) which may consist of one or more records, is denoted by a 17 code recorded on tape in coded format.

Figure 3-26 shows the end of file detector circuit. The circuit checks each line read into R^1 during read or backspace operations for the 17 code. Detection of the code sets the End-of-File FF in the read select circuits to notify the sense circuit of the condition. Because each non-17 coded line read results in clearing the FF, the condition generally is sensed for before a new read operation is initiated.

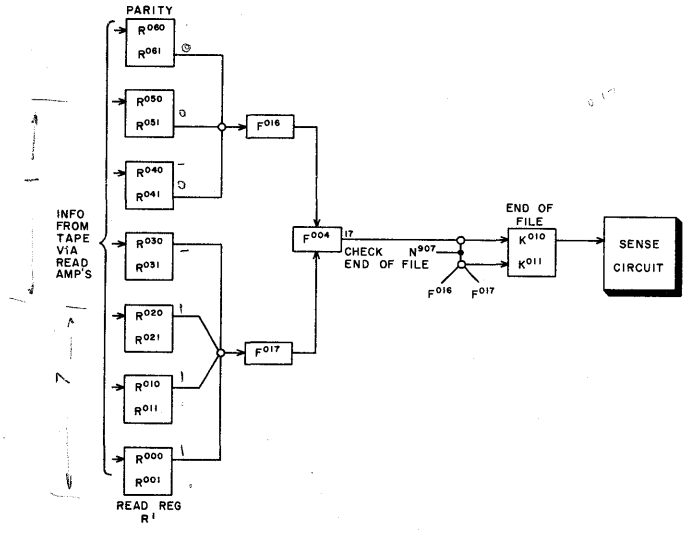


Figure 3-26. End-of-File Detector.

Read Control

The read control circuits direct operation of the individual read circuits to accomplish a read or backspace operation. For discussion purposes read control circuits are divided as follows:

1) Tape Motion Control - initiates tape starts and stops
2) Read Sequence Control - generates, for each line read from the tape, commands necessary to sequence a read or backspace operation

Each circuit is discussed with reference to a simplified block diagram. Circuit details not shown are found on the maintenance diagrams in volume 2.

Tape Motion (figure 3-27)

With few exceptions tape motion circuit operation is similar to the write control tape motion circuit. These exceptions are noted below:

Read Operation

Receipt of the computer input buffer active signal following an EF select read instruction sets the Tape Motion FF to start tape moving in a forward direction. The status of the signal is stored in the Input Buffer Active FF. The circuit prevents a tape start if the computer has not terminated a previous tape input buffer, but allows a tape stop at end-of-record regardless of the presence or absence of the computer signal. The tape start lockout condition results from reading a tape record whose word length is less than the computer input buffer length. In this case the input buffer active signal remains on and the FF set after the tape is stopped. The computer condition is detected as a read length error, and indication of which is available to the computer through sensing. The net effect of the circuit is to force the computer to sense for the error and terminate its input buffer as necessary before executing an EF select read instruction. The appropriate read delay, after a tape start and before the Read Control FF is set, prevents reading pulses from the tape sooner than necessary.

Backspace Operation

In this operation the Tape Motion FF is set to start tape moving in a backward direction upon receipt by the read select circuit of a backspace EF select code. The 1-ms delay

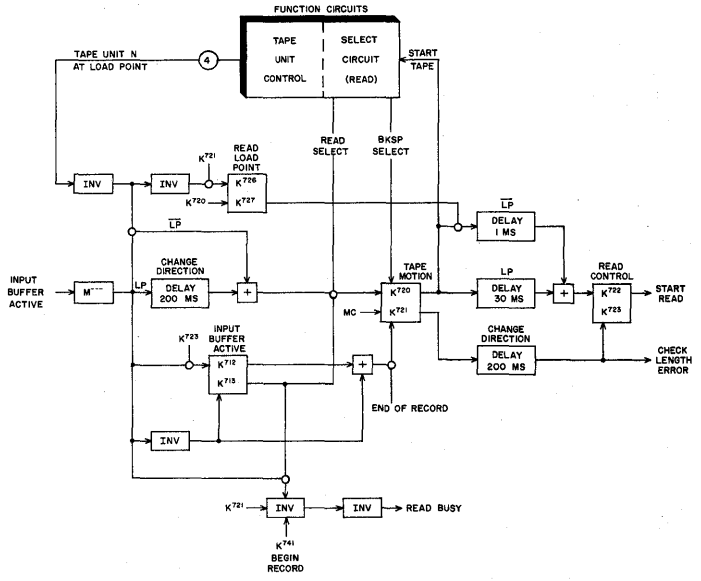


Figure 3-27. Read Control, Tape Motion Circuit.

after the tape start allows reading of the check character to locate the start of the record to be skipped.

Read Sequence Control (figure 3-28)

This control circuit consists of a clocking circuit for generating the commands necessary to direct a read or backspace operation, a circuit for sensing the end of the tape record, and a circuit for sensing read length errors. With few exceptions, this circuit is similar to the write control reply sequence control circuit.

Read Operation

The clocking circuit, enabled by the set state of the Read Control FF, is triggered by the read sprocket signal generated by the first "1" bit read in each line. The circuit period is 26 μsec; the first 23 μsecs of the period compensate for tape skew to allow all bits of a line to be read into the R^1 register before checking the data for a parity error or end-of-file condition and assembling the data into the B^1 register. During the last 3 μsec of each period, 1 μsec pulses are generated in the following order:

1) Check parity, check end-of-file, $AK^1 \rightarrow AK^2$, clear B^1 (latter generated prior to assembly of first character in each 48-bit word)
2) $R^1 \rightarrow B^1$
3) Clear R^1, Adv AK^1

A 48-bit word is assembled in the B^1 register after eight of the above command cycles. The word is transferred to the B^2 register upon detection of the first character in the next tape word. This action produces the $B^1 \rightarrow B^2$ command and sets the Input Data Ready FF to inform the computer of an assembled word. Computer acceptance of the word is signalled by the input data resume signal which clears the FF in turn clearing B^2 and causing the computer to drop the resume signal. The cycle repeats then. If the last tape word assembled is not a 48-bit word (when reading a file mark) an end-of-record signal initiates the $B^1 \rightarrow B^2$ transfer described above and "0's" are filled in for the missing characters. As shown on the diagram, static clear signals are produced initially to clear all registers and AK before word assembly begins.

The end of a tape record is sensed 80 μsecs after at least two lines (the minimum tape record length, one character and its check character) have been read. The first line read sets the Begin Record FF, and the second line read sets $K^{742/743}$ FF to enable

the End-of-Record FF to be set 80 μsec after the last line in the record is read. The set state of the latter FF triggers a 2 ms delay after which the Tape Motion FF is cleared to stop tape. Because of the delay and the mechanical stop time of the tape unit the tape is stopped with the read head in the approximate center of the record gap. The centering of the read head minimizes detection of extraneous tape signals in the record gap when reading is started in a new read or backspace operation.

At the end of the record a check is made to determine:

1) if the tape record contained an integral multiple of 48-bit words
2) if the tape record length in terms of 48-bit words is equal to the input buffer word length established by the computer

A negative finding on either check sets the Length Error FF to signal a read length error condition to the sensing circuit for interpretation by the computer.

The first condition above is sensed if AK $\neq$ 0 at end-of-record time. Assuming like reading and tape data formats, the condition may be due to: 1) reading a one-character record (file mark); 2) reading a tape generated on IBM equipment; 3) dropping an odd number of lines during reading.

In the second condition a long or short read length error is sensed if the tape record is longer or shorter by one or more words than the computer buffer. A long read length error is detected if the input buffer active signal is absent at end-of-record time; a short read length error is detected if the input active signal is present after the Tape Motion and Read Control FFs are cleared at the end of the record. In the latter case, the Input Buffer Active FF stores the fact that the computer signal stays on after the end of the record is reached. This action prevents re-starting the tape in a read forward mode until such time as the computer artificially terminates its input buffer (equalizes the buffer initial and terminal addresses to turn off the input buffer active signals).

Backspace Operation

A backspace operation is similar to a read operation except that data is not assembled in the B^1 register. Data assembly is prevented by removal of the forward enable in the $R^1 \rightarrow B^1$ circuit. Because the check character for the record to be skipped is read, parity error and length error indications are not valid.

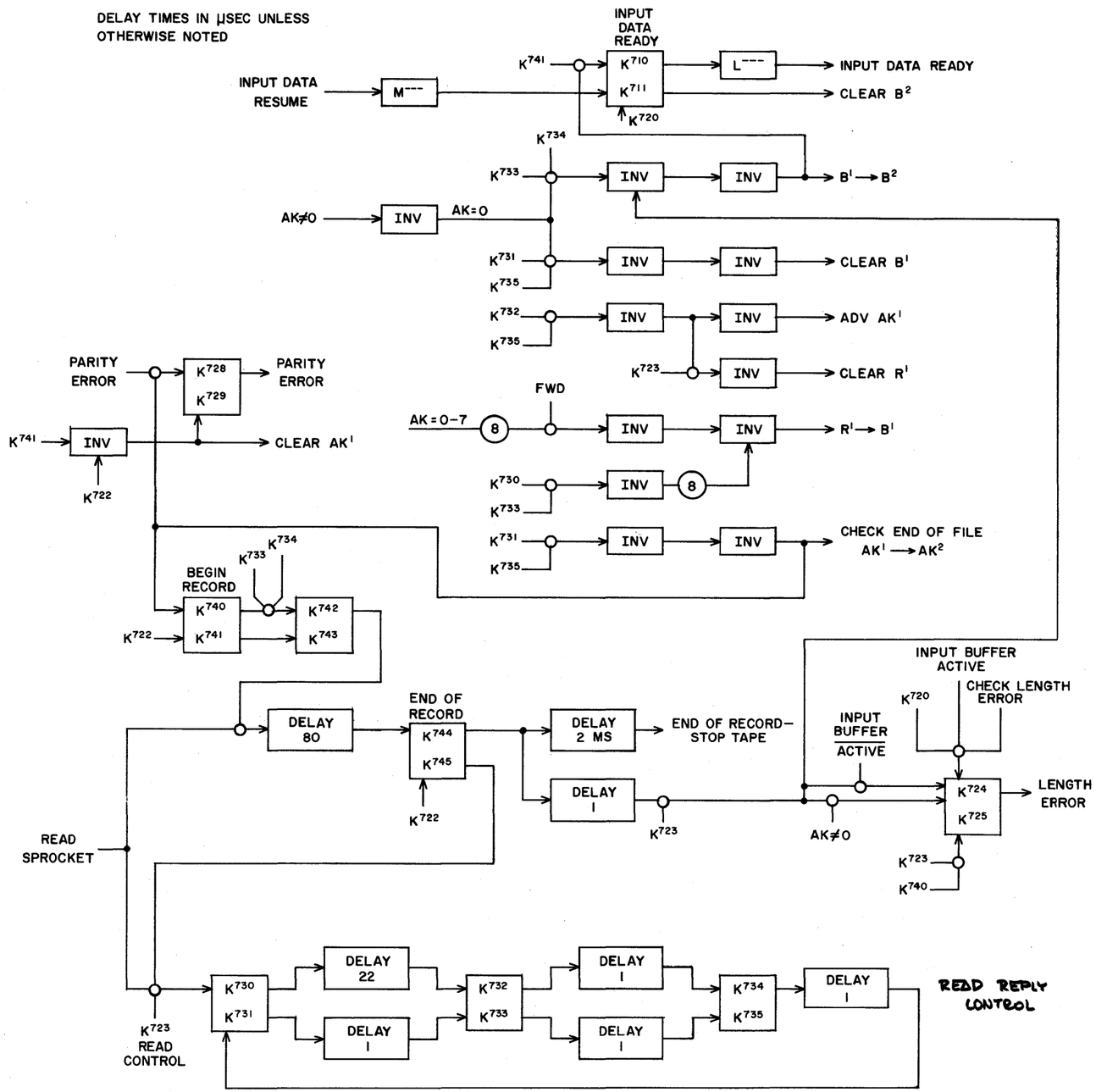


Figure 3-28. Read Control, Read Sequence Control.

DESCRIPTION OF TAPE OPERATIONS

The paragraphs to follow present summary descriptions of the various operations that the MTS performs under computer program control. The descriptions are intended to tie together the individual circuits discussed earlier.

The MTS operations can be grouped into select operations and sense operations. In general, select operations select one of the four tape units and place it in a mode of operation, for example, read or write. Sense operations enable the computer to determine the status of a given tape unit, for example, is tape unit n ready to be operated in a read or write mode? Select operations are requested by input or output channel EF select instructions (74.03XXXX or 74.04XXXX respectively), sense operations by input or output channel EF sense instructions (74.73XXXX or 74.74XXXX respectively). The codes used in the lower-order four octal digits of these instructions to select the MTS and a given operation are shown in table 3-2 located in the function circuits description presented earlier.

A brief description is presented here on the selection of a tape unit.

SELECTION OF A TAPE UNIT

Table 3-2 shows that a tape unit selection is required only in certain of the MTS EF select codes. These instructions are as follows.

Select read tape unit n, binary (20n1) Select read tape unit n, coded (20n2)	input channel
Select write tape unit n, binary (20n1) Select write tape unit n, coded (20n2)	output channel

The code arrangement is such that a given tape unit is selected initially to read or write and all subsequent select and sense operations on the corresponding input or output channel are carried out automatically on the previously selected unit.

As an example of this, one of the above instructions prepares a given tape unit to read in binary or coded format. Other subsequent input channel select and sense instructions not containing a tape unit selection allow the computer to continue reading the unit, to backspace or rewind the unit, or sense error conditions arising during read operations on the unit. A different input channel tape unit selection destroys a previous unit

selection so that all operations are always carried out on the current unit selection stored in the synchronizer. This is also true for write selections; but in this case, once a rewind interlock instruction is executed the unit is not again available for output channel select operations. The operation descriptions which follow assume the operation is occurring on a tape unit selected as noted above.

Manual selection switches labelled 1, 2, 3, 4 on the control panel of each tape unit allow any unit to be operated as the unit selected by the program. In the event a unit referenced in the program is not available for operation, the operator can manually assign this same reference number to another unit thus avoiding a change in the program.

SELECT OPERATIONS

WRITE

A write operation is initiated by an EF select write instruction followed by instructions which activate the computer output buffer. The write select information appears on the computer function lines and is accompanied by an output function ready signal which indicates an output channel operation. The information on the lines is decoded and stored in FFs in the function circuits; the stored information is then routed to the write circuits.

Following this action the computer generates an output buffer active signal to indicate that the output buffer is ready. The synchronizer responds to this signal by starting the tape. The computer informs the synchronizer of each output buffer word with an output data ready signal. When ready the synchronizer accepts each word and signals the computer with an output data resume. Each 48-bit word is disassembled into eight 6-bit characters which are recorded sequentially on the moving tape with an appropriate parity bit. When the computer output buffer is depleted, it turns off the output buffer active signal and writing stops.

During the writing sequence each line recorded is read from the tape and returned to the synchronizer and checked for errors. The write reply sequence lags the writing sequence and the tape is stopped after the last recorded line is read.

Figure 3-29 shows a simplified logic diagram for a write operation. The following steps describe the general sequence of events in a write operation with respect to the diagram.

Step	Event	Action
1	Function lines activated	Synchronizer decodes the information on the lines and recognizes an MTS select request.
2	Output function ready	Appears after the function lines have had time to stabilize and be decoded. The signal is used to gate storage of the translated select code into FFs located in the write select portion of the function circuits. Function lines drop with fall of this signal.
3	Output buffer active	Indicates the computer buffer is ready to start sending data. The signal remains on until the synchronizer has accepted the last word in the buffer.
4a	Start tape	If the selected tape unit is at load point when output buffer active is received, a 200 ms delay is taken before setting the Tape Motion FF. The set state of the FF combined with write forward and tape unit selections in the function circuits generates an auto forward signal which starts the tape moving on the selected unit. If the tape is not at load point when the computer signal is received, the FF is set and the tape started immediately. The 200 ms delay allows time for the tape unit vacuum loops to readjust to a change in direction in the event a rewind operation was completed on the unit immediately preceding the write select.
4b	Write current	As the Tape Motion FF is set to start tape, write head current is turned on and dummy load current turned off. Dummy load current is drawn during non-writing periods so that the power supply load is approximately constant at all times.
4c	Load point delay	As the tape is started a 40 ms delay is initiated. If the tape is at load point the delay allows the load point to be moved past the write head approximately 6 inches before writing begins. This distance is compatible with IBM equipment which may read the tape after the record is written.
4d	Write delay	If the tape is not at load point when started, a 4 ms delay is initiated to allow tape to arrive at full speed before writing begins. Tape moves approximately 1/2 inch during the delay to fix part of the interrecord gap.
5	Start write	Completion of the delay sets Write Control FF. This allows writing to begin and enables the write reply circuits to respond to recorded data. The FF remains set until the tape is stopped at the end of the record.

Step	Event	Action
6	Output data ready	This signal indicates to the synchronizer that the computer has placed a buffer word in the output register that is associated with the output channel to which the MTS is connected (typically, channel 4). Initially, the signal comes on shortly after output buffer active but is not recognized until Write Control FF is set. Subsequent output data ready signals are recognized upon completion of the recording sequence for each word.
7	Output data resume	When ready, the synchronizer transfers each computer word to a cleard 48-bit disassembly register (O) and indicates acceptance of the word to the computer with an output data resume signal. The synchronizer signal causes the computer to drop the output data ready and this in turn causes the synchronizer to drop its output data resume.
8	Write generator	Each output data resume signal triggers the write generator. The circuit produces writing pulses of one μsec duration at a 30 KC rate (33 μsec pulse interval). A 6-bit character and its parity bit are recorded during each 33 μsec period; 8 generator cycles complete recording of the 48-bit computer word.
9a	Line translator	The line translator, under direction of the disassembly counter, sequentially extracts each 6-bit character from the O register beginning with the highest-order character.
9b	Write parity generator	A parity bit is recorded on the tape with each character to facilitate error checking when the tape is read. The write parity generator produces a "1" parity bit which makes the total number of "1" bits in a line of tape data odd for binary format writing or even for coded format writing. The parity generator translates each character appearing on the outputs of the line translator to determine the necessity of an odd or even parity bit.
10a	Write register	Each character from the line translator and its parity bit is entered into a 7-bit write register (W) in a manner such that each "1" bit in a line toggles an associated stage (FF) of the register to its opposite state. The register is cleared at the start of each record.
10b	Write drivers	The write drivers sense the change-on-ones action of the W register FFs and, as necessary, reverse the direction of current flow through the write heads to record "1's" on the tape in the appropriate tracks.

Step	Event	Action
10c	Disassembly Counter	The disassembly counter (DK) is a modulus 8 additive counter. The stored count is advanced by one as each character is toggled into the W register. The new count allows the line translator to extract the next character from the O register.

The write generator continues to produce write pulses at 33 μsec intervals until DK is advanced through a complete 8-count cycle to return it to zero. Recording of the word in the O register is complete at this time; if the output data ready signal is again present, the O register is cleared and the next computer word accepted to repeat the cycle of steps 6-10 above. The end of the computer buffer is sensed if the output data ready is absent when DK completes its cycle. It remains then to write a record check character and to complete the write reply sequence and stop the tape. These events are described below.

The record check character is written 133 μsec (.02 inch) from the last character in the record. Clearing of the W register at this time records a "1" in those data tracks whose associated W register stage contained a "1" at the end of the record. The check character makes the total number of "1" bits even in each of the seven longitudinal data tracks and is recorded for compatibility with IBM magnetic tape format. The latter equipment uses the check character in performing horizontal read parity checks.

During the writing sequence each line recorded on the tape is sensed by the read heads and returned via reading amplifiers to a 7-bit write reply register (R^2). A line is read into R^2 every 33 μsecs; but because the read and write heads are mechanically spaced 0.39 inch apart, the over-all write reply sequence (reading) lags the writing sequence by approximately 2.6 ms. The steps listed below describe the action taken on each line read into R^2.

Step	Event	Action
11	Read amplifiers	As each bit in a line is read by the tape moving past the read head it is preamplified, passed to a final amplifier where it is converted to a single-ended signal, and then through a standard amplifier-inverter circuit where it is converted to standard logic signal voltages. A separate read amplifier circuit exists for each tape unit.
12a	Sprocket generator	The 7 bits in each line appearing on the outputs of the read amplifiers are combined in an OR circuit by the sprocket generator so that the first bit read in a line alerts the write reply sequence control of a line being read into the R^2 register. A separate sprocket generator circuit exists for the read amplifiers associated with each tape unit.
12b	Write reply register	The read amplifier outputs are gated into the 7-bit R^2 register in accordance with the tape unit selection stored in the write select portion of the function circuits.
13a	Write reply sequence control	The first bit read in each line triggers a clocking circuit which generates 1 μsec wide pulses for checking the line of data in R^2 . The period of the clocking circuit is 26 μsecs.
13b	Skew delay	The first μsecs of the 26 μsec period of the clocking circuit compensates for tape skew to allow all bits in a line to enter the R^2 register before the line is checked for a parity error condition. During writing, all bits of a line should be recorded perpendicular to the edge of the tape. However the tape does not always move in parallel across the write heads so that the data is recorded at a slight angle with the edge of the tape. The amount of deviation from the perpendicular is termed skew. A character skewed more than the delay will generally be recognized as a partial character and a parity error will be registered for it.
14	Write reply parity detector	Parity is checked for the line in the R^2 register following elapse of the skew delay. Any one of the conditions listed below is detected as a parity error and the error fact stored in a FF for later sensing by the computer. 1) write binary format a) parity is a "1" and the character (6 bits) contains an odd number of "1" bits b) parity is a "0" and the character contains an even number of "1" bits 2) write coded format a) parity is a "1" and the character contains an even number of "1" bits b) parity is a "0" and the character contains an odd number of "1" bits

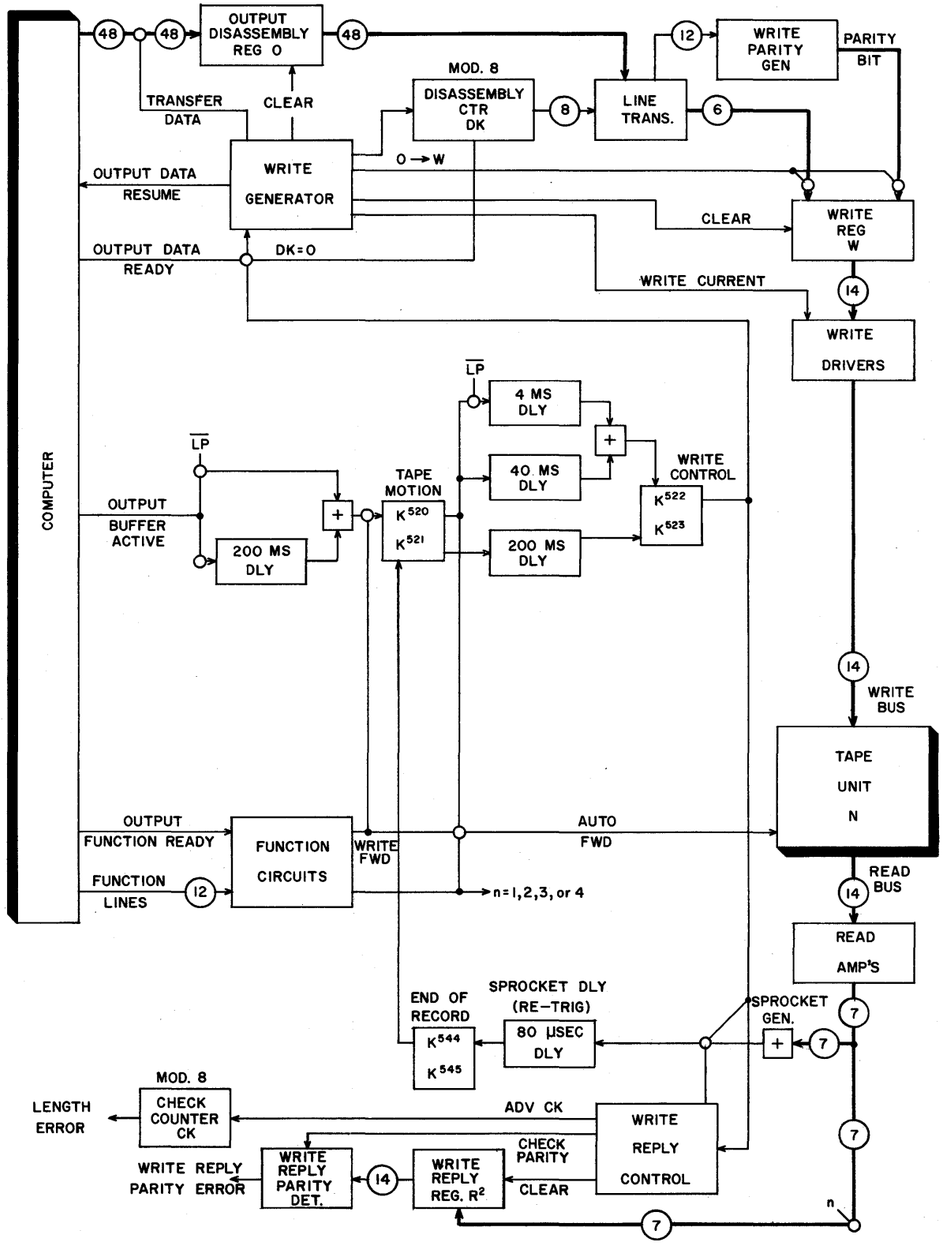


Figure 3-29. Write Logic Diagram.

Step	Event	Action
15	Check counter	The check counter (CK) is a standard modulus 8 additive counter. The stored count is advanced by one for each line read into R^2 . A CK $\neq$ 0 condition at the end of the record indicates that the number of lines read was not an integral multiple of 48-bit words. In general this indicates that one or more lines were dropped from or added to the record due to faulty recording (dust on the tape or noise extraneously recorded on the tape).

As explained earlier, a record consists of a number of characters spaced at 33 μsec intervals and a check character spaced 133 μsecs from the last character in the record. An end-of-record sensing circuit searches for the 133 μsec gap. The sensing circuit contains an 80 μsec retriggerable delay which is operative after at least two lines have been read; thereafter the delay is triggered by each line read (33 μsec intervals). Elapse of the delay indicates the end-of-record gap and an end-of-record FF is set at this time. The set state of the FF prevents reading the check character and causes clearing of the Tape Motion FF which in turn causes a tape stop. Because of the mechanical stop time of the tape unit the tape is stopped with the read head positioned approximately 1/8 inch past the record check character. This gap fixes the remaining portion of the record gap.

Clearing of the Tape Motion FF triggers a 200 ms delay after which the Write Control FF is cleared to turn off write head current and turn on dummy load current. The write operation is complete at this time and the function circuits are informed that the write circuits are no longer busy. The computer senses for the ready condition and then senses for the various error conditions described to determine if the record was in error.

The 200 ms delay after the Tape Motion FF is cleared allows stabilization time for the tape unit vacuum loops when an immediately following instruction calls for a change-in tape direction (rewind or backspace).

Read

A read operation is initiated by an EF select read instruction followed by instructions which activate the computer input buffer. As in a write operation, the read select information appears on the computer function lines; but in this case it is accompanied by an input function ready signal because the select instruction requests an input channel operation. The information on the lines is decoded and stored in FFs in the function circuits and then routed to the read circuits.

Following this action the computer generates an input buffer active signal to indicate the input buffer is ready to accept tape data. The synchronizer responds to this signal and starts tape moving. Reading begins after appropriate delays which allow proper positioning of the tape over the read head. Tape data is assembled into 48-bit words; the computer is informed of each word by an input data ready command. Computer acceptance (and storage) of each word is acknowledged by an input data resume. Reading continues with the exchange of input data ready/resume commands until the end of the tape record is reached at which time the tape is stopped and the computer input buffer deactivated.

Figure 3-30 shows a simplified logic diagram for a read operation. The following steps describe the general order of occurrence of events in a read operation with respect to this diagram.

Step	Event	Action
1	Function lines activated	Synchronizer decodes the information on the lines and recognizes an MTS select request.
2	Input function ready	Appears after the function lines have had time to stabilize and be decoded. The signal is used to gate storage of the translated select code into FFs located in the read select portion of the function circuits. Function lines drop with fall of this signal.
3	Input buffer active	Indicates the computer input buffer is ready to accept data. The signal remains on until the computer buffer is completed.
4a	Start tape	If the selected tape unit is at load point when input buffer active is received, a 200 ms delay is taken before setting the tape motion FF. The set state of the FF combined with read forward and tape unit selections in the function circuits generates an auto forward signal which starts the tape moving on the selected unit. If the tape is not at load point when the computer signal is received, the Tape Motion FF is set and the tape started immediately. The 200 ms delay allows time for the tape unit vacuum loops to readjust to a change in direction in the event a rewind operation was completed immediately preceding the write select.
4b	Load point delay	As the tape is started a 30 ms delay is initiated. If the tape is at load point, the delay allows the load point to be moved past the read head before reading begins.

Step	Event	Action
4c	Read delay	If the tape is not at load point when started, a 1 ms delay allows tape to arrive at full speed before reading begins. For either case, the delays are so timed as to prevent reading pulses from the tape sooner than necessary.
5	Start read	Completion of the delay sets the Read Control FF to allow reading to begin. At this time a static clear signal on the read register (R^{I}) is dropped and a clear signal for AK and the parity detector circuit generated. This signal remains on until the first line is read into R^{I}.
6	Read amplifiers	As each bit in a line is read by the tape moving past the read head it is pre-amplified, passed to a final amplifier where it is converted to a single-ended signal, and then through a standard amplifier inverter circuit where it is converted to standard logic signal voltages. A separate read amplifier circuit as described above exists for each tape unit.
7a	Sprocket generator	The 7 bits in each line appearing on the outputs of the read amplifiers are combined into an OR circuit by the sprocket generator so that the first bit read in a line alerts read sequence control of a line being read into R^{I}. A separate sprocket generator circuit exists for the read amplifiers associated with each tape unit.
7b	Read register	The read amplifier outputs are gated into the 7-bit R^{I} register in accordance with the tape unit selection stored in the read select portion of the function circuits.
8a	Read sequence control	The first bit read in each line triggers a clocking circuit which sequences assembly of tape data into 48-bit words and informs the computer of each assembled word. The period of the clocking circuit is 26 μsecs.
8b	Skew delay	The first 23 μsecs of the 26 μsec period of the clocking circuit compensates for tape skew to allow all bits of a line to enter the R^{I} register before the data is checked and assembled. The bits in a line are not always recorded perpendicular to the edge of the tape and the deviation from the perpendicular is termed skew. During reading, additional skew may be incurred and become additive to the write skew. The length of the skew delay is such as to cover these possibilities for maximum variations in tape speeds.

Step	Event	Action
9a	Parity detector	Parity is checked on the line in R^1 following elapse of the skew delay. Conditions for producing a parity error are identical with those described in the write operation but a separate read parity error FF is employed for error storage.
9b	End-of-file detector	Each line in R^1 is checked by the end-of-file detector for a 17_8 code recorded in coded format (even parity). Detection of the code sets an End-of-File FF in the read select portion of the function circuits. The condition can be sensed by the computer at the end of the record.
10	Assembly register	The "1" bits in the information character in R^1 are assembled in a 48-bit assembly register (B^1) on an $R^1 \rightarrow B^1$ command generated after the parity and end-of-file checks. Character assembly in B^1 is from higher to lower-order character position. The B^1 register is cleared prior to assembly of each 48-bit word.
11a	Clear R	The R^1 register is cleared after each tape character is stored in the B^1 register.
11b	Assembly counter	The position of characters assembled in the B^1 register is directed by a standard 2-rank modulus 8 additive counter, designated assembly counter, AK. The counter is advanced one count coincident with clearing of the R^1 register. Each count in AK is interpreted by a translating circuit which selects the B^1 storage location for the next character to be read.

Steps 6-11 above are repeated for eight successive lines of data at which time the B^1 register contains a 48-bit word. The assembled word is made available to the computer as soon as the first tape character for the next 48-bit word is detected. The transfer sequence to the computer is described below. (Transfer to the computer of the last tape word is discussed later.)

12a	Input register	An assembled 48-bit word in the B^1 register is transferred in parallel to a previously cleared input register, B^2. The B^2 register functions as a buffer storage register for the word while assembly of the next word takes place in the B^1 register. The buffer is necessary since the computer may not be able to accept an assembled word before the next tape character is read. In a typical installation the B^2 register is connected to computer input channel 3.

Step	Event	Action
12b	Input data ready	Each $B^1 \rightarrow B^2$ transfer sets an Input Data Ready FF; this action generates an input data ready signal. The signal informs the computer that a tape word is ready to be transferred to internal storage.
13	Input data resume	The computer acknowledges acceptance and storage of each tape word with an input data resume signal. The computer signal clears the Input Data Ready FF which in turn clears the B^2 register and causes the computer to drop its input data resume signal.

As in the write reply sequence of a write operation, the end of a tape record is detected by a circuit which searches for the 133 μsec gap between the last character in the record and the check character. The circuit contains an 80 μsec retriggerable delay which is operative after at least two lines have been read. Elapse of the delay signifies end-of-record and the condition is stored in an End-of-Record FF.

The set state of the End-of-Record FF:

1) insures that the last word* assembled in the B^1 register is transferred to the B^2 register and then to the computer;
2) Disables the read sequence control circuit so that the check character is not read for records greater than two lines;
3) checks for a discrepancy in word length between the computer buffer and tape record;
4) initiates a 2 ms delay after which the Tape Motion FF is cleared to stop the tape. The 2 ms delay plus the mechanical stop time of the tape unit positions the read gap in the approximate center of the record gap when the tape is stopped.

*Either a partial or complete 48-bit word; the last assembled word will generally be a partial word when reading tapes generated on IBM tape units or when an end-of-file mark is read.

As the Tape Motion FF is cleared, a 200 ms delay is taken after which the Read Control FF is cleared to terminate the read operation. The function circuits are then informed that the read circuits are no longer busy; the computer senses this fact with an appropriate sense ready to read instruction. Following a positive response to this instruction request, the computer generally will sense for an error and/or end-of-file condition and take appropriate steps as necessary before processing new tape data.

A read length error is detected at end-of-record time and stored in a FF for later sensing by the computer if the following conditions exist.

1) The tape record does not contain an integral multiple of 48-bit words. A tape record not containing an integral multiple of 48-bit words is detected if AK $\neq$ 0 when the End-of-Record FF is set. This condition will generally occur when reading tapes generated on IBM tape units.
2) The tape record in terms of 48-bit words is greater or less than the word length of the computer buffer. A long tape record is detected if the computer input buffer active signal is absent when the End-of-Record FF is set. A short tape record is detected if the input buffer active is present when the Read Control FF is cleared after the tape stop. Generally speaking, when reading tape the computer purposely establishes an input buffer known to be longer or shorter than the tape record and the error condition serves as a program reminder.

Simultaneous Read and Write

In any one MTS cabinet one tape unit can be reading while another is simultaneously writing. The computer selects the two operations by executing the read and write instructions; either read or write may be selected first because the operations are completely independent.

Write End-of-File Mark

An output channel write end-of-file mark selection (XXX3) causes a 17_8 code to be recorded in coded format (even parity) on the previously selected tape. The file mark signifies an end-of-file condition and is written for compatibility with IBM magnetic tape format. The instruction causes "1" bits to be recorded on the tape in tracks 0, 1, 2, and 3. Because the file mark is considered as a 1-character record, a check character identical with the file mark is recorded 133 μsecs from the mark. The file mark is written 6 inches from the check character of the previous record.

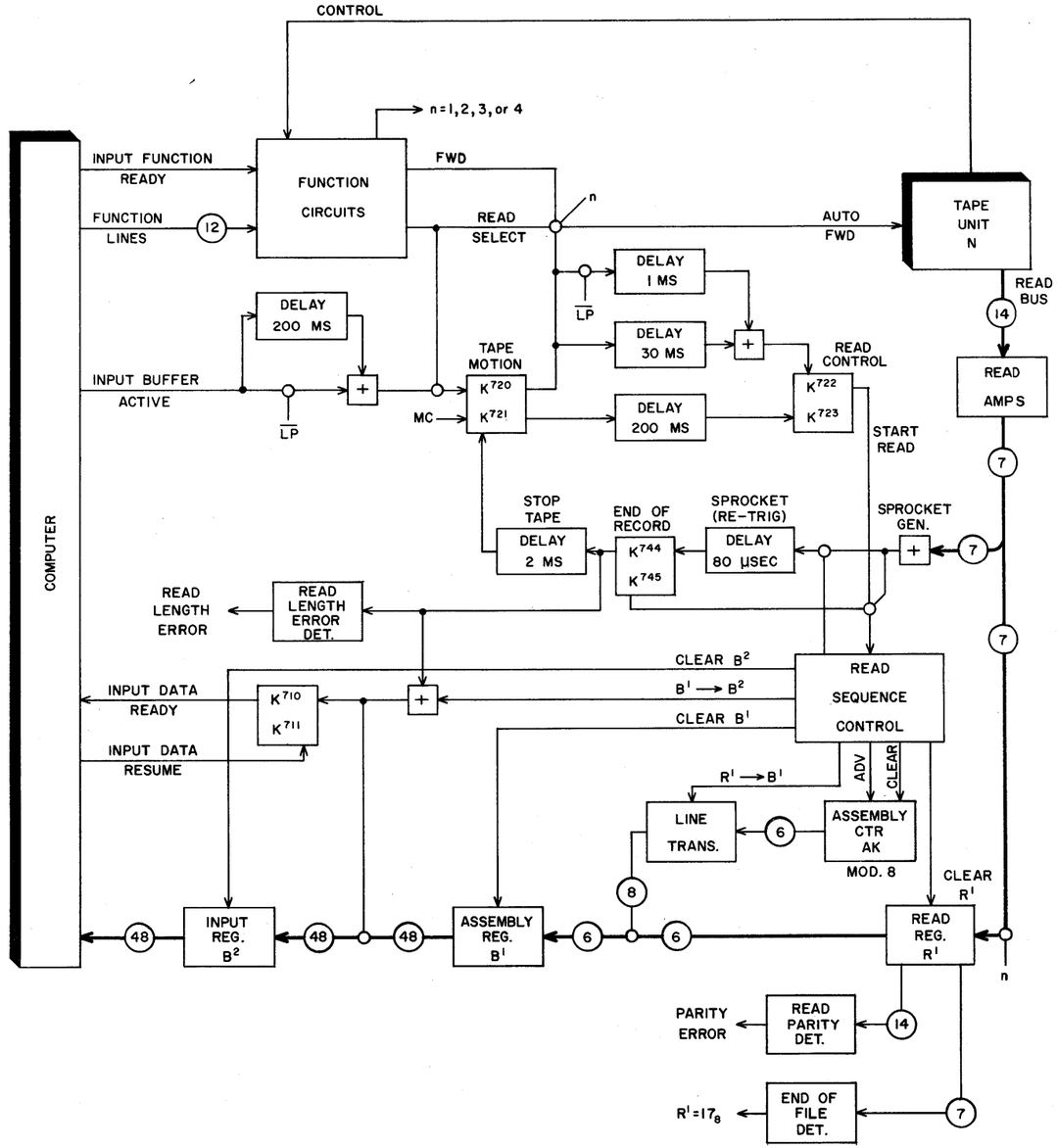


Figure 3-30. Read Logic Diagram.

The write circuits are used in normal fashion in writing the file mark, but because the computer buffer is not activated, synthetic output buffer active and output data ready signals are generated. An additional signal is generated to set the O register to 00000017_8. The signals are generated by the function circuits when the EF write end-of-file mark select code is received and stored in a FF.

A normal 8-character write sequence occurs then to record the file mark with the File Mark FF in the function circuits cleared during the first character write cycle. The standard 40 ms load point delay occurs before writing begins to space the mark 6 inches from the check character of the previous record. Tape is stopped as in a normal write operation as soon as the file mark and its check character are read in the write reply sequence.

Backspace

A backspace operation moves the tape backward past one record to the preceding record gap. A backspace operation can be thought of as a read operation in which data is read from the tape but is not made available to the computer; the computer therefore does not establish a buffer. As in a read operation or in the write reply sequence in a write operation, the end of the record being passed over is detected by an absence of tape data for 80 μsecs. The tape is stopped then in the appropriate position in the record gap.

An input or output channel backspace select instruction (XXX6) can be executed to backspace a previously read or written tape, respectively. Because of the independent read and write circuits two tapes can be backspacing simultaneously; either tape can be selected first.

In general, the respective backspace operations are similar to their read or write reply sequence counterparts, with the exception of data transfer to the computer; other differences are discussed below.

Backspace Write Tape

Tape is started as soon as the output channel backspace select code is translated by the function circuits. Write head current is not turned on nor are the write generator circuits activated. A 1 ms delay after the tape start permits reading of the check character for the record to be skipped to locate the start of the record. Parity and length errors

are sensed for and registered but, in general, are not considered valid because of the check character. A 4.5 ms delay before tape is stopped at the end of the record allows the read and write heads to be stopped in the record gap in approximately the same position as in a write operation. As in a write operation, the computer determines the end of a backspace operation with a sense ready to write instruction.

Backspace Read Tape

As in a backspace write tape operation, tape is started as soon as the input channel backspace select code is translated by the function circuits. The standard 1 ms read forward delay (non-load point) is taken after the tape start and the check character for the record to be passed over is read to locate the start of the record. Parity and length errors are sensed for and registered but in general are not considered valid because of the check character. At the end of the record a 2 ms delay is incurred before the tape is stopped. This delay period is identical with the read forward stop delay. The computer senses completion of the backspace operation with a sense ready to read instruction.

Interrupt

An interrupt selection (XXX4) permits automatic interruption of the computer program upon completion of the tape operations listed below.

1) read
2) write
3) write end of file
4) backspace
5) rewind

For 1 and 2 above (or simultaneous read/write), the interrupt select instruction is executed after a read or write tape instruction and after the computer establishes the initial address in its buffer. This sequence of instruction execution allows the read or write circuit to respond to the computer input or output buffer active signal and in turn generate a read busy or write busy signal before interrupt is selected. Turn off of the busy signal following a tape stop at the end of the operation (end-of-record) in conjunction with the set state of an appropriate Interrupt FF causes production of the interrupt signal. The interrupt signal remains on until the computer, in its search for the interrupting equipment, executes the appropriate sense ready to read (input channel) or write (output channel) instruction.

For operations 3, 4 and 5 above the interrupt instruction is executed immediately following the instruction selecting the operation as described above.

Rewind

A rewind select instruction is used to move a tape from its current position back to load point.

The rewind select code is stored in a Rewind FF corresponding to the previously selected tape unit (one FF for each tape unit). The FF set output starts tape moving backward and energizes a rewind relay in the tape unit. Contacts of the relay light the unit Rewind indicator. Tape moves at 150 inches per second to the load point reflective spot at which time the unit energizes a load point relay. Contacts of this relay produce a static load point signal which is stored in a Load Point FF in the synchronizer. The FF set output signal clears the Rewind FF to stop tape and drop the unit rewind relay and indicator. During rewind, a tape unit is in a not ready to read or write condition and the synchronizer indicates this to the computer with negative responses to sense ready to read or write requests. Upon completion of the operation the tape unit becomes ready to read or write and the synchronizer indicates this with a positive response to the noted sense instruction.

A rewind instruction will usually not be executed when the unit is positioned at load point or is rewinding; however, should this occur no harm will result.

Rewind Interlock

A rewind interlock selection is identical with a rewind operation; but in addition it interlocks the unit at load point so that under normal programming it is not again available for reading or writing until the interlock is manually released. This condition is indicated by the Change Tape light and the computer receives a negative response to repeated sense ready to read or write instructions. The interlock remains on until released through operation of the Stop Manual switch.

A rewind interlock select instruction can be executed regardless of whether the tape is at load point or not. Thus a rewound tape can be interlocked at any time.

The rewind interlock select code (XXX7) is stored in a rewind interlock FF corresponding to the previously selected tape unit (one FF for each tape unit). The set output of the FF energizes the tape unit interlock relay; the relay contacts light the Change Tape indicator, provide relay self-holding contacts, and open the unit ready signal line to the synchronizer. The latter action accounts for the unit not ready condition. Additional interlock relay contacts close to provide partial continuity in the tape unit fast reverse relay circuit.

Coincident with the above action, the appropriate rewind FF is set to start tape and energize the unit rewind relay. Contacts of the rewind relay light the Rewind indicator and energize the fast reverse relay. Contacts of the latter relay select the fast reverse winding of the capstan drive motor to move tape at a rate of 225 inches per second. As in a rewind operation, tape is stopped at load point and the Rewind FF and relay dropped. However, the interlock relay remains energized to retain the interlock until the Stop Manual switch is operated. This drops the relay and indicator to restore the unit ready signal to the synchronizer and enable a positive response to a subsequent sense ready to read or write instruction.

Under abnormal programming circumstances the computer may execute a read or write select instruction on a unit rewound with interlock without first sensing for a ready status. In this case, the selected read or write operation is carried out in a normal fashion with the Change Tape indicator lighted.

SENSE OPERATIONS

The sense operations allow the computer to determine the status of a previously selected tape unit. The synchronizer provides the computer with a positive response (table 3-3) if a condition is present when sensed; absence of a condition when sensed is indicated with a negative response. All sensed conditions are indicated to the computer over a common sense response signal line.

The EF sense codes appear on the computer function lines. After a brief period to allow the lines to stabilize and the codes to be decoded by the external function translator and sense circuits, the computer generates an input or output sense ready signal which turns on the synchronizer sense response signal. Fall of the computer signal turns off the synchronizer signal. The synchronizer response is stored in a FF in the computer so that the computer can act on the response as necessary.

Table 3-3. Sense Operations

EF Sense Instruction	Channel	Positive Response Indicates:
XXX0		
Ready to read	input	previously selected tape unit is ready for a read, backspace, rewind, or rewind interlock operation.
Ready to write	output	previously selected tape unit is ready for a write, write end-of-file, backspace, rewind, or rewind interlock operation.
XXX2		
Read parity error	input	for a previous read or write operation: coded format - 1 or more lines (vertical) contained an odd number of "1" bits
Write reply parity error	output	binary format - 1 or more lines contained an even number of "1" bits
XXX4		
Write reply length error	output	one or more lines of data was dropped from or added to previously written record
XXX6		
End-of-file	input	end-of-file mark was detected in a previous read operation
End-of-tape	output	end-of-tape reflective spot was detected in a previous write, or write end-of-file mark operation.

Generally errors are sensed for immediately following the reading or writing of each tape record; and the synchronizer retains the error fact until a new operation is begun.

MANUAL CONTROLS

The manual controls* are located on the panel above the glass front door of the tape unit. The principles of operation are discussed in this section. The use of these controls and indicators in normal operating procedures is presented in the operation chapter of this manual. The controls and indicators are described with reference to simplified diagrams; for detail circuit diagrams see volume 2.

UNIT SELECTION SWITCHES (1, 2, 3, 4)

These switches assign a program reference number to the unit. Because they also apply primary a-c power to the unit, manual unit assignment is always completed before any other manual or automatic operation on the unit can be accomplished.

The switches and related circuits are shown in figure 3-31. Each switch operates the appropriate combination of relays as indicated in the table to cancel an existing switch selection and establish the new selection. As shown, K13 is energized for all switch selections. Contacts of K13 energize K17 contacts which apply primary power to the unit. The -20v supply required for operation of these switch circuits is obtained from the synchronizer -20v power supply which is energized independent of the tape units.

Contacts of relays K14 and K15 supply enables representing the switch selection to the synchronizer function select circuits. The effect of these enables was discussed earlier in the description of the function circuits.

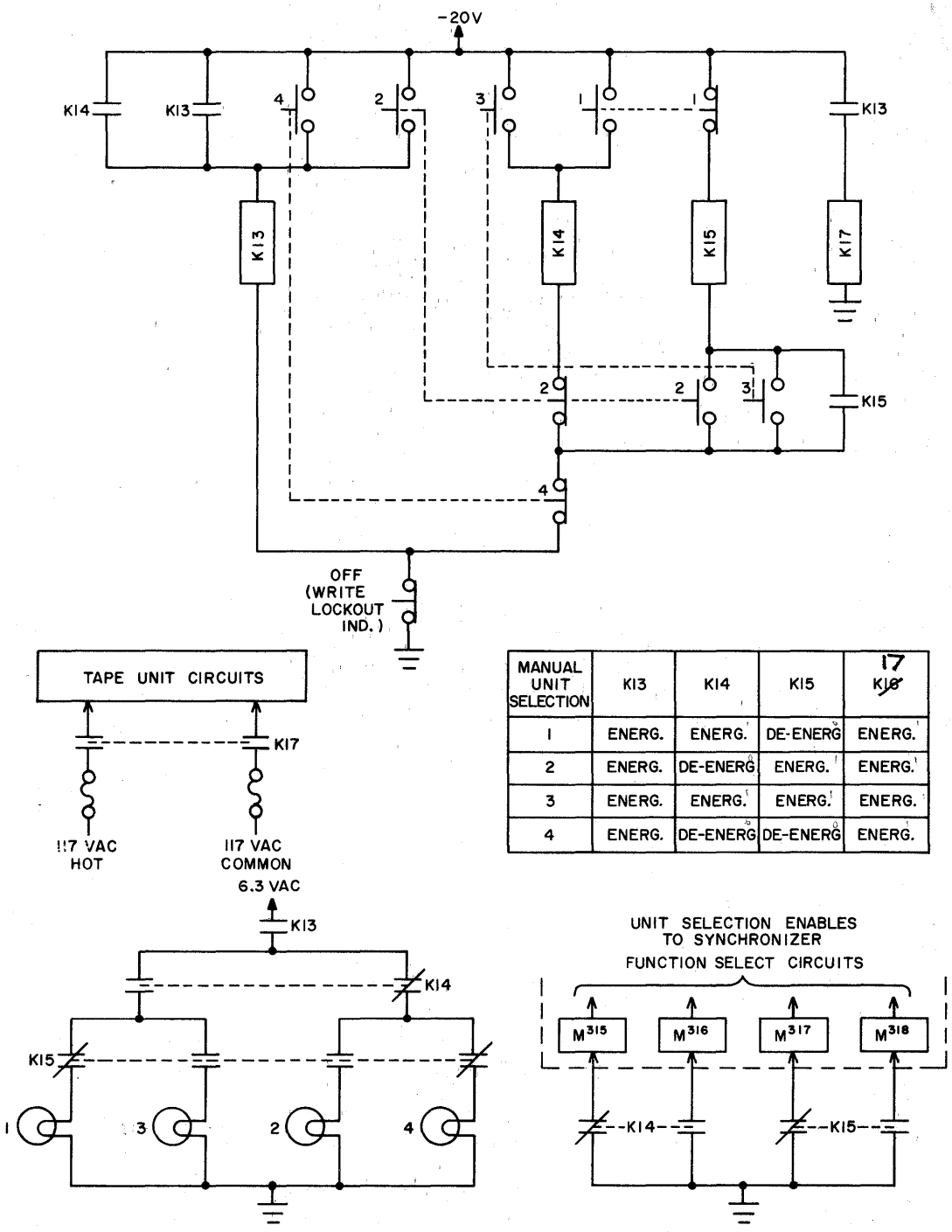
Depressing the Write Lockout button de-energizes all relays in the circuit to drop power from the tape unit.

REWIND

The Rewind switch allows a programmed rewind operation to be manually duplicated from the tape unit. The rewind circuit is shown in figure 3-32.

As the switch is operated a pair of its contacts ground the set input to the synchronizer Rewind FF to set the FF. Because the FF is set before the switch is released, rewind relay K10 is energized through another pair of switch contacts and a pair of normally closed contacts of forward II relay which apply -20v to the relay. As K10 is energized, a pair of its contacts light the plastic insert of the switch and allow -20v to energize

* Bypass Ampex instructions on manual controls



MANUAL UNIT SELECTION	K13	K14	K15	K17
1	ENERG.	ENERG.	DE-ENERG	ENERG.
2	ENERG.	DE-ENERG	ENERG.	ENERG.
3	ENERG.	ENERG.	ENERG.	ENERG.
4	ENERG.	DE-ENERG	DE-ENERG	ENERG.

Figure 3-31. Unit Selection Switches.

auto I and II relays K7 and K8 (through normally closed contacts of sense post relays K11 and K12) so that when the switch is released it is held energized through a pair of K7 contacts. When the reflective load point spot is reached, a load point relay is energized and its contacts set the synchronizer Load Point FF. The latter action clears the Rewind FF to drop K10 and stop the tape. Subsequently, when tape is started in a forward direction; the load point relay drops out and a pair of its contacts clear the synchronizer Load Point FF.

CHANGE TAPE

The indicator of this control is turned on by a programmed rewind interlock select instruction. This indicator signals that the tape is rewound and interlocked at load point. The switch of this control is used (primarily during maintenance procedures) to transfer the tape unit from manual to automatic or program control mode.

Indicator

As shown in the figure 3-32, the rewind interlock select code sets the synchronizer Rewind FF to energize rewind relay K10 and sets the Rewind Interlock FF to energize interlock relay K9 (relays K7 and K8 normally are energized when the rewind interlock operation is initiated). As K9 energizes, its contacts: light the Change Tape indicator; clear the Rewind Interlock FF; hold the relay energized after the Rewind Interlock FF is cleared; and allow fast reverse relay K17 to be energized. Contacts of the K17 relay select the fast reverse winding of the capstan motor to move tape at 225 inches per second to the load point. As in a rewind operation, the tape is stopped at load point and relay K10 and its indicator dropped, but the interlock relay and indicator remain energized to signal the condition.

Note that the unit ready signal line to the synchronizer is an open circuit when K9 is energized; this indicates to the synchronizer, and through the sense circuit to the computer, that the tape is in a not ready to read or write condition.

Switch

Assuming all tape unit protective interlocks are closed operation of the switch energizes relay K7 and K8 which hold in through self-holding contacts after the switch is released. Other K7 and K8 contacts: turn off the Stop Manual, Forward, or Reverse indicators; provide continuity in the signal paths for the actuator commands received from the synchronizer; disable access to the actuator circuits via the manual Forward and Reverse controls; and provide continuity in the rewind circuit.

The tape unit protective interlock circuit is a series circuit composed of switches and relay contacts. The function of these circuits is to prevent or stop tape motion when an abnormal operating condition is detected. With all protective interlocks closed, power interlock relay K4 is energized and its contacts apply d-c voltage to the various switch circuits.

WRITE LOCKOUT

The indicator of this control is on at all times when the unit is loaded with a file reel which does not contain a file protection ring. The lighted indicator signifies that the tape cannot be written on but may be read. The switch of the control is used to drop power from the unit; this function is shown in figure 3-31 and discussed in the unit selection switch paragraph.

A file protection ring is a circular plastic ring which fits into a groove in the back of the file reel (figure 2-2). When no ring is installed on the reel, contacts of a write lockout microswitch (figure 3-32) provide continuity in the ground circuit of the indicator to keep it turned on. The ground condition on the switch is reflected into the synchronizer function circuits as a not ready to write condition and the computer is so informed through a negative response to an EF sense ready to write instruction. The negative response prevents the computer from writing on the tape thereby destroying the record, but allows the computer to read the tape.

With the protection ring installed on the file reel, the microswitch is tripped to break continuity in the ground circuit of the indicator and synchronizer circuit to turn off the indicator and allow writing on the tape.

FORWARD

This switch is used during certain operational and maintenance procedures in which it is necessary to manually start the tape moving in a forward direction.

From figure 3-32 it can be seen that the forward actuator can be turned on through operation of the switch if: 1) relay K7 is de-energized indicating the unit is in a non-automatic mode; and 2) relay K6 is de-energized indicating the unit is not currently moving tape in a backward direction; 3) all protective interlocks are closed; and 4) the file reel is not void of tape. In condition 4, if the metal backing of the file reel trailer is contacting the upper sense post, relay K12 is energized to prevent forward motion since no tape is available to be transferred to the takeup reel.

Forward tape motion from a change tape position (unit is loaded with a fresh file reel of tape) is controlled by contacts of relay K11 which is energized by the metal backing of the permanent machine leader contacting the lower sense post.

STOP MANUAL

This switch is used to stop the tape after it has been manually started through operation of the Forward or Reverse switches. Additionally, the switch is used to transfer the unit from automatic to manual mode.

Operation of the switch will drop relays K5-K10 and K16 to de-energize the associated circuits (figure 3-32) and turn off the forward or reverse actuator commands to stop the tape.

REVERSE

The Reverse switch circuit functions in a manner similar to the Forward switch circuit with the exception that tape moves in a backward direction.

In the event the Stop Manual button is not operated to stop tape once it is started, an automatic stop is produced at the change tape position. Relays K11 and K12 are energized at this time by the metal-backed permanent machine leader contacting both the upper and lower sense posts. Reverse relay K6 is dropped and the reverse actuator command is turned off which stops the tape.

POWER AND COOLING SYSTEM

The MTS cabinet operates from 208-vac, 400-cps, 3-phase, 3-wire power and 208-vac, 60-cps, 3-phase, 4-wire power. The 400-cps power is rectified by -20v and +20v power supplies on the synchronizer chassis to supply d-c power for the synchronizer printed circuit cards. The 60-cps power is used to operate blowers in the cabinet and the individual tape units which convert the power to necessary d-c operating voltages.

The tape unit power supply system is described in the Ampex instruction book.

The distribution of a-c power within the MTS cabinet, and the synchronizer d-c power supplies are shown on a circuit diagram in volume 2.

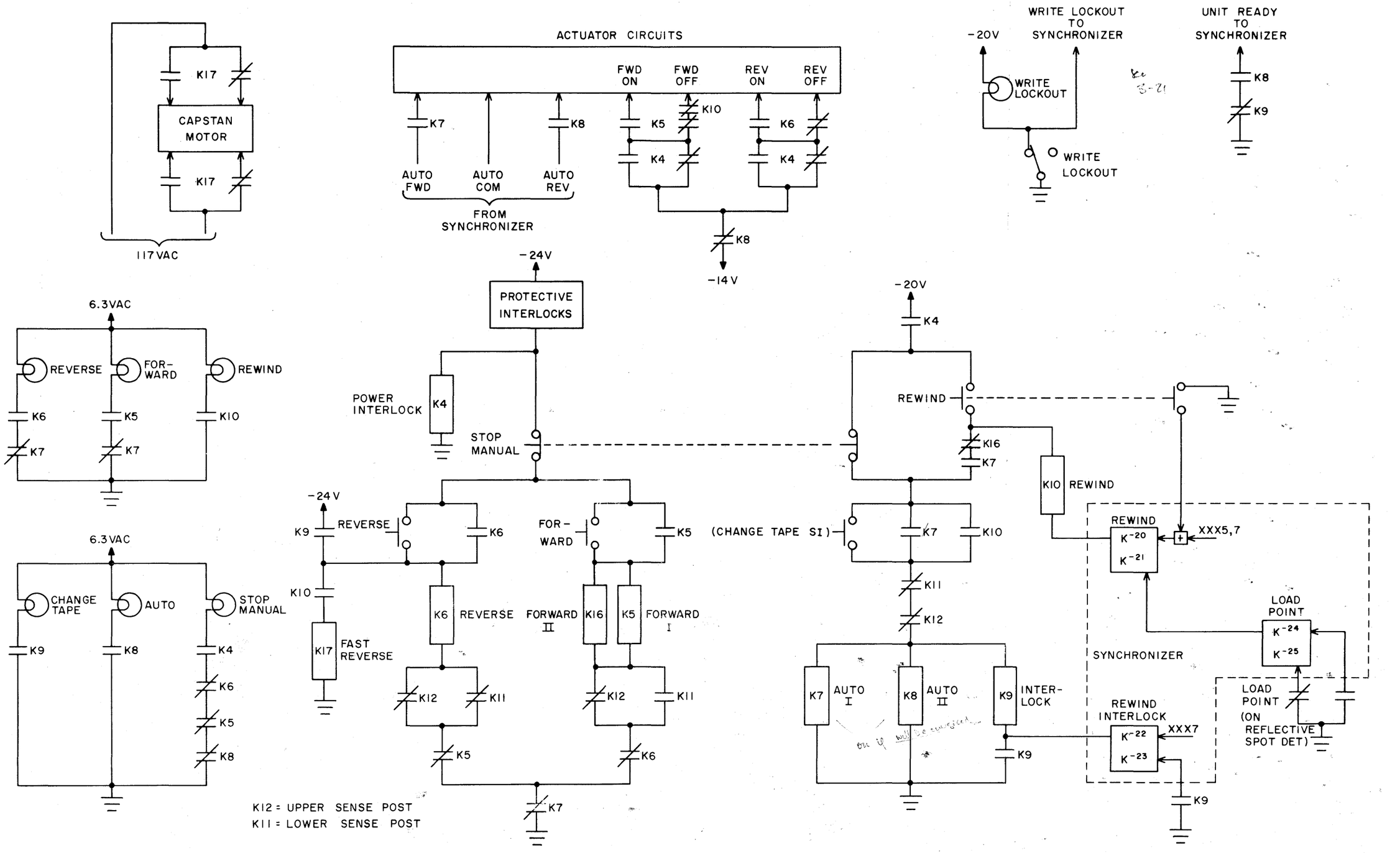


Figure 3-32. Manual Controls.

A-C POWER DISTRIBUTION

The 60-cps and 400-cps power is received on separate cables from the switch panels in the computer room. The cables terminate at the a-c power distribution panel at the back of the cabinet. Primary power is applied and removed by operation of the Power On/Off switch at the computer console.

Each phase of the 400-cps power is routed through a 2-amp fuse on the power distribution panel to the synchronizer logic chassis. From this point power is distributed to the d-c power supply transformers located in each corner of the chassis. The 400-cps power cable also contains a ground wire (common to all cabinets in the computer system) and one of the wires which connects the temperature interlock circuits of the computer and the MTS cabinet.

The 60-cps power is routed through the power distribution panel to convenience outlets on panels mounted in each 19-inch relay rack section of the cabinet. Two power cables from each tape unit connect to tne outlets which are wired from one phase to the neutral wire to provide 110 vac. Other outlets provide for connection of oscilliscopes, etc. for maintenance purposes. The 60-cps power cable also carries the return wire of the cabinet temperature interlock circuit.

Two phases of 60-cps power are routed from the power distribution panel through 5-amp fuses to the four blower motors in the bottom of the cabinet. Two blowers are connected from each fuse to the neutral wire.

D-C POWER SUPPLY

There are three -20v supplies and one +20v supply on the synchronizer chassis. Each voltage is produced from the 208-vac primary supply through a step-down, delta-star transformer and a 6-phase half-wave rectifier circuit. Choke-input filters are used on each supply. The 3 mh choke in each supply is housed in the transformer mounting case. The power supply filter capacitors (10 μf) are located on each tape 74 card on the chassis. The -20v and +20v levels are distributed throughout the chassis from the 74 cards. Each supply contains six silicon rectifiers mounted about the U-channel which forms the outer frame of the chassis.

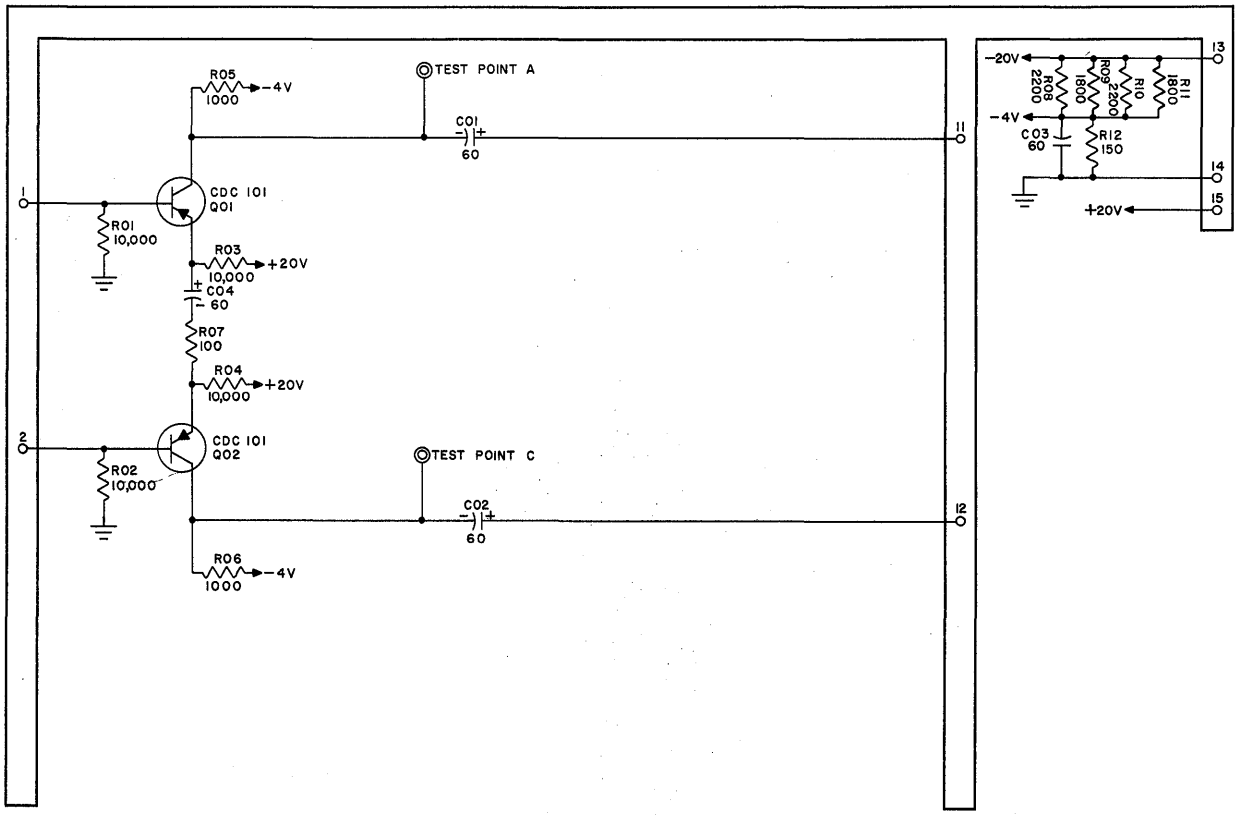


Figure 3-33. Schematic Diagram, Tape Preamplifier (Card Type 71)

COOLING SYSTEM

Four blowers at the bottom of the cabinet provide for circulating air-conditioned room air over cabinet components. The cool room air enters the cabinet at floor level, is forced through filters and grill work above the blower compartments, over cabinet components and out through louvres at the top of the cabinet. The air filters are anodized aluminum filters of a type that can be cleaned and re-used.

The exhaust temperature at the top of the cabinet is monitored by two 100^{o} thermostats which are wired in series with those in the computer (and any other external equipment) and an alarm system. Circuit action is such that if the exhaust temperature reaches 100^{o} F, a thermostat opens to operate a buzzer at the console. The buzzer provides an audible alarm for three minutes following which 400-cps power to the entire computing system is removed to stop system operation. A neon indicator on the power distribution panel is lighted when one (or both) of the thermostats is actuated. An actuated thermostat closes automatically when the cabinet temperature drops below 100^{o} F. Application of 400-cps system power is not automatic however, and must be re-applied by operation of the console Power On switch.

DETAILED CIRCUIT DESCRIPTIONS

The paragraphs following detail the operation of those synchronizer circuits considered as "special" circuits. In general, special circuits are considered as such because of their non-logical properties.

Tape Preamplifier

The tape preamplifier card (type 71) shown on figure 3-33, amplifies the data signal induced into the read head as the tape is moved past the heads. A "1"is read from the tape whenever a change in the polarity of the magnetic flux is sensed. The "1" signals from the tape appear alternately at either end of the head winding and are represented by a voltage level of 13-17 mv.

In figure 3-33, the ends of the read head windings connect to the base of transistors Q01 and Q02 which are connected in a differential amplifier circuit. The emitters are held at the difference potential by a difference network composed of R07 and C04. As a result noise voltage on the head cables is largely cancelled. Capacitors C01 and C02 couple the output signals of Q01 and Q02 to the tape amplifier cards.

TAPE AMPLIFIER

The tape amplifier card (type 72), shown in figure 3-34 amplifies the output signals of the preamplifier card. With the exception of certain resistor values, the 72 card is similar to the type 56 card used in the computer.

Transistors Q01, Q02, Q03, and Q04 are connected in a differential amplifier circuit similar to that of the type 71 card. The signals from the pre-amplifier are applied to Q01 and Q03. The emitters of Q01 and Q03 are held at the difference potential by a difference network composed of C01 and R04. As a result noise voltage on the wires connecting the preamplifier and tape amplifier cards is largely cancelled.

Capacitors C02 and C03 in the collector circuits of Q02 and Q04 provide d-c stabilization. Diodes CR01 and CR02, functioning as an OR input to transistor Q05, pass the negative going components of the signals from Q02 and Q04 and also serve as clippers.

Transistors Q05 and Q06 are connected in a slightly modified version of the standard amplifier-inverter building block circuit. The output signal from CR05 as a result of a "1" signal from the tape, is -0.5v.

DELAY CARD

The delay card (type 73) is used in conjunction with other card types to form delay circuits. Figure 3-35 is a schematic diagram of the card. Figure 3-36 shows how the delay card is used with card types 61 and 62 in a delay circuit which can be used as a retriggerable delay.

In figure 3-36, the delay network is triggered by the "0" to "1" change at the input to the inverter feeding the 62 card. The 62 card output follows this change and switches to -20v. This change is coupled through the integrating circuit of the delay card to the 61 card. The change at the input to the delay circuit is felt at the output of the 61 card after a period approximately equal to the RC time constant of the integrating network. By switching the input to the 62 card at a rate faster than the charge time of the capacitor in the integrating network, the delay becomes retriggerable.

Through external wiring the delay card capacitors are paralleled as necessary to provide coarse adjustment of the delay; the capacitors are connected externally to the variable resistor network which provides fine adjustment of the delay.

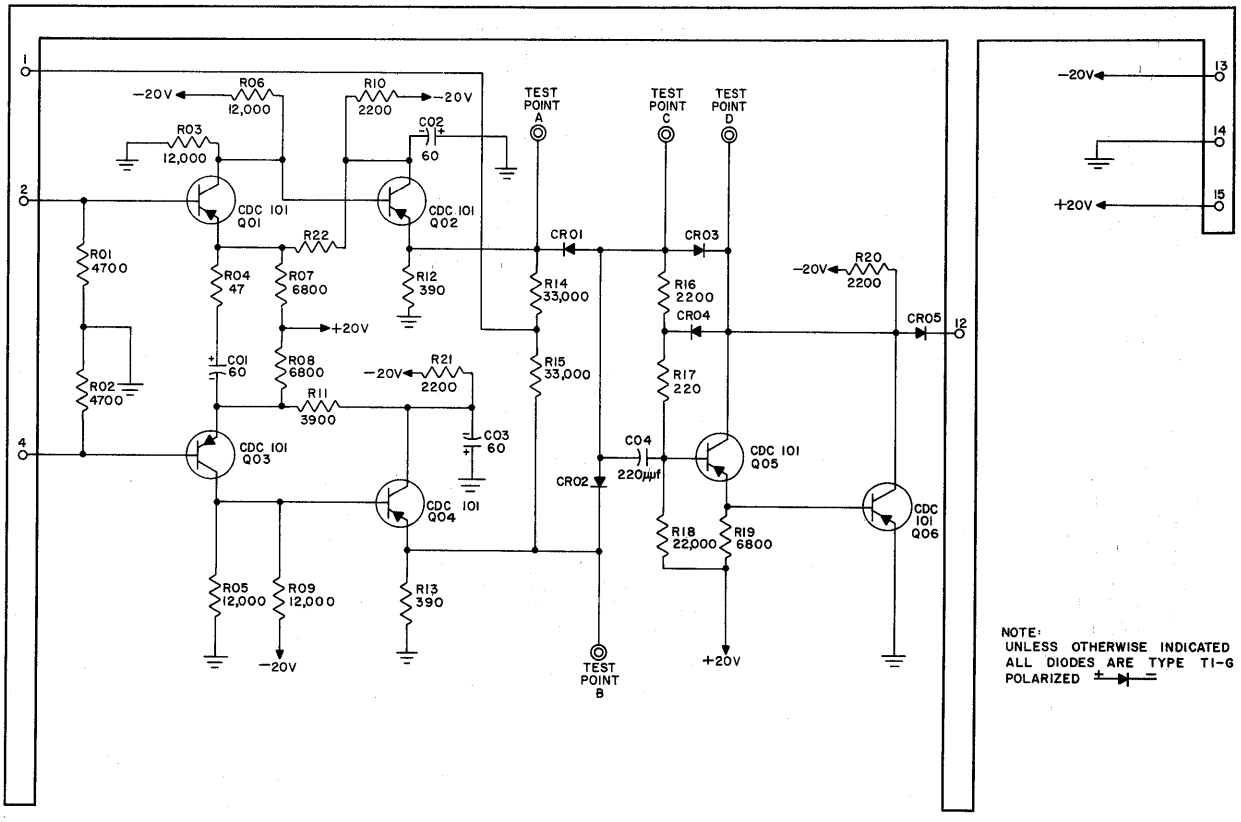


Figure 3-34. Schematic Diagram, Tape Amplifier (Card Type 72)

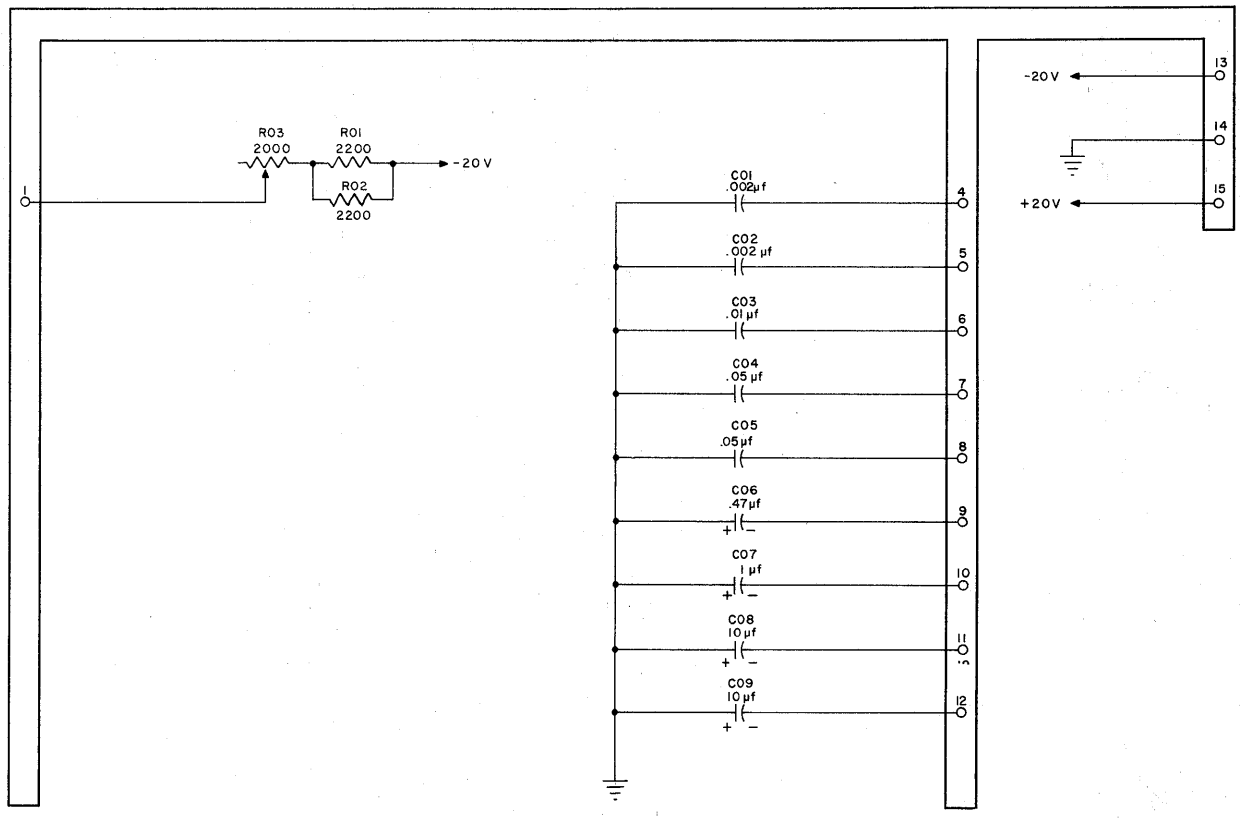


Figure 3-35. Schematic Diagram, Delay (Card Type 73)

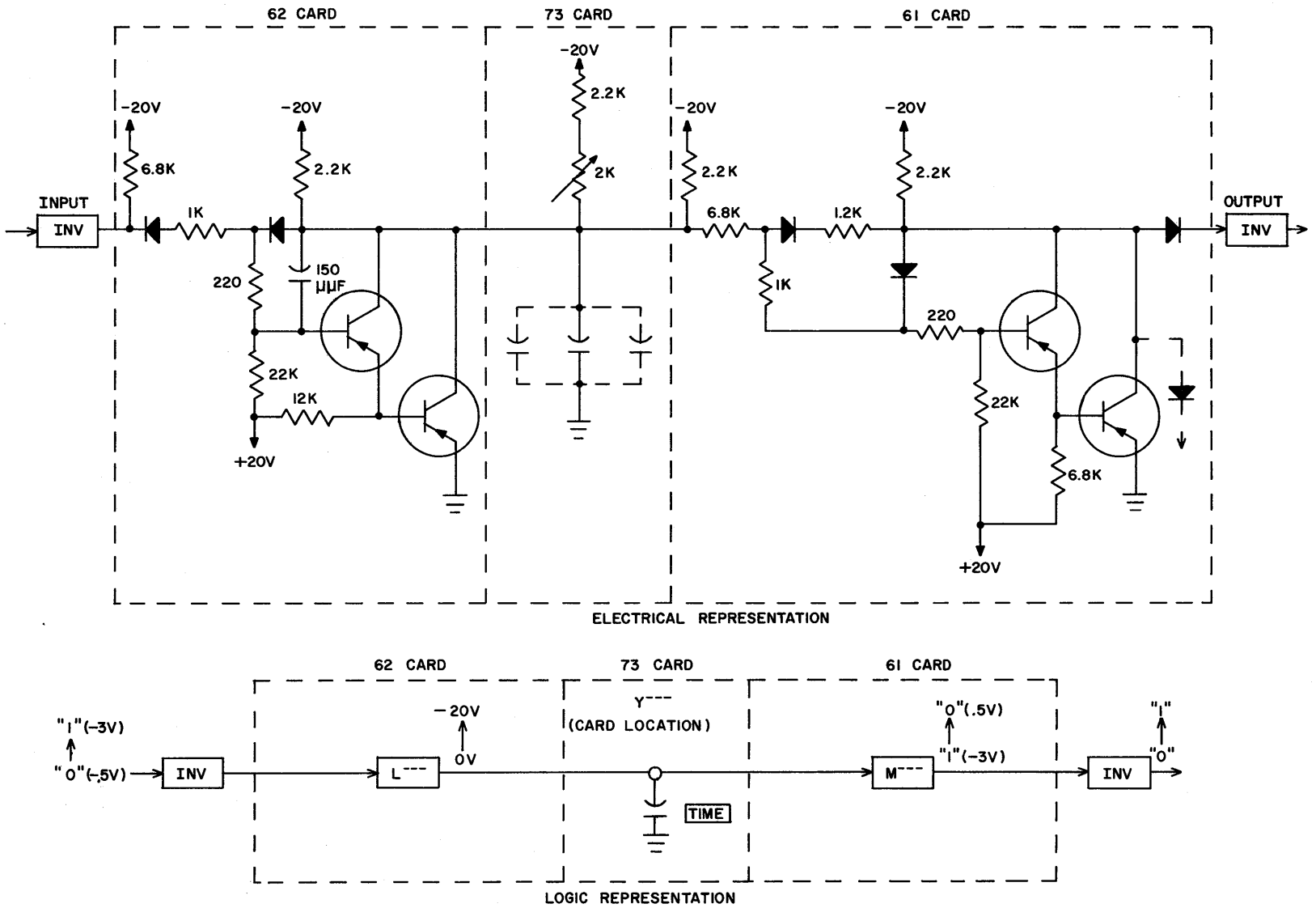


Figure 3-36. Delay Circuit.

TAPE CURRENT SOURCE

The tape current source card (type 74) shown in figure 3-37, consists of five banks of parallel resistors and two 10 μf capacitors. With the exception of resistor values the card is similar to the type 54 card used in the computer.

The effective resistance of each of four banks of resistors is 257 ohms; that of the remaining bank is 303 ohms. One end of each bank is connected to the -20v output of the power supply. The 257 ohm banks supply write current and current for the tape unit actuator commands. The 303 ohm bank supplies current to the dummy load circuits under nonwriting conditions.

The 10 μf capacitors provide filtering for the power supply.

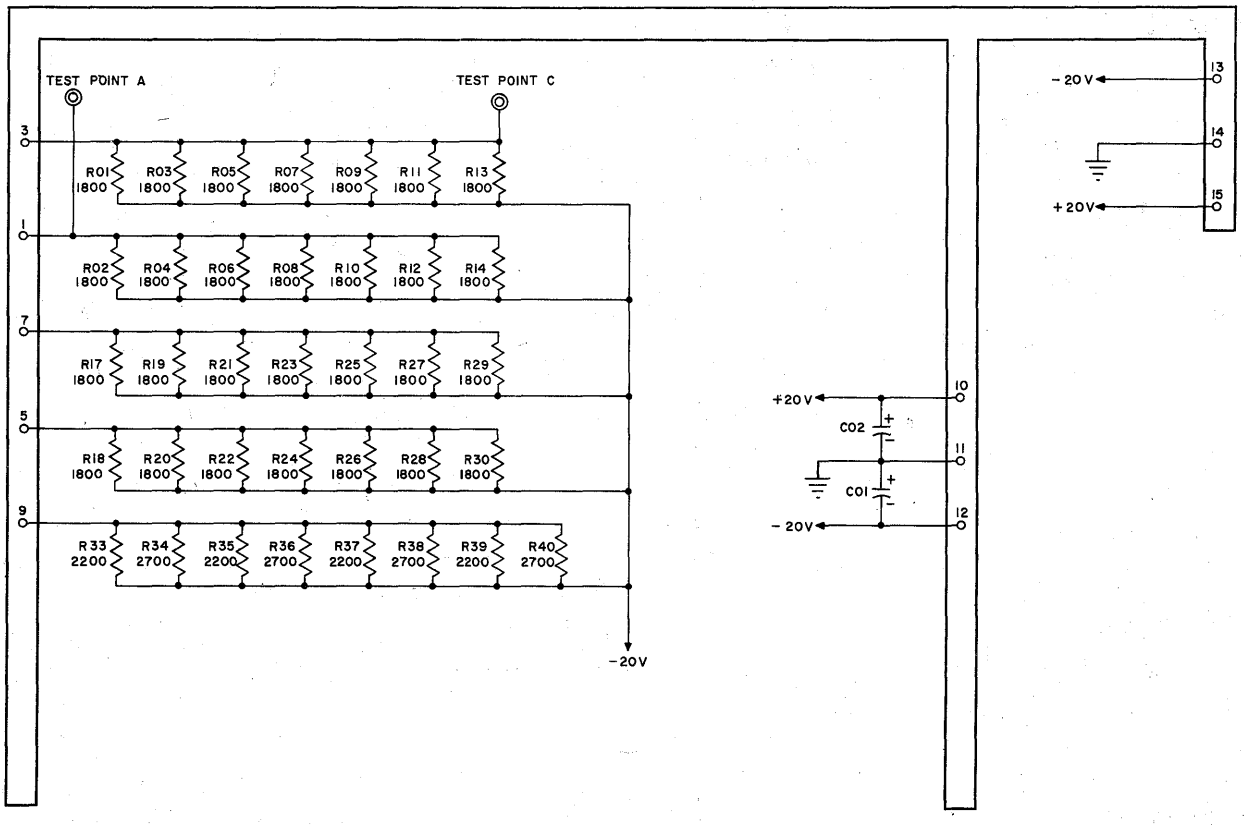


Figure 3-37. Schematic Diagram, Tape Current Source (Card Type 74).

CHAPTER 4. THE SATELLITE COMPUTER SYSTEM

The Control Data Satellite Computer System uses the 1607 Magnetic Tape System (MTS) to link the small-scale 160 computer with the large-scale 1604 computer. This arrangement allows both the 1604 computer and the 160 computer access to the 1607 MTS at the same time or independently. It also allows either computer to communicate directly with the other computer.

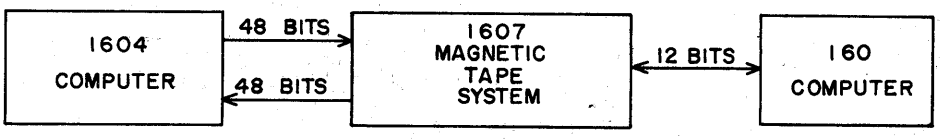


Figure 1. Basic Satellite Computer System

As a part of the Satellite Computer system, the 1607 MTS has three modes of operation: 1604 Mode, 160 Mode, and Program Control Mode. A three-position switch on the back of the MTS cabinet selects the mode.

1604 MODE

In this mode the 1604 and 160 computers are completely independent and the 1607 MTS is available only to the 1604 computer. (1604 programs written prior to the introduction of the Satellite Computer System require no change when this mode of operation is selected.)

160 MODE

In this mode the 1604 and 160 computers are completely independent and the 1607 MTS is available only to the 160 computer. Programs written for the 160 mode of operation require the same programming precautions necessary in 1604 programs (sense unit ready, sense parity errors, etc.)

PROGRAM CONTROL MODE

In this mode the 1607 MTS is available to both the 1604 and the 160 computers. In addition to having the same magnetic tape system available to both computers, the Program Control mode provides for a direct transfer of data between the two computers without using magnetic tape as a medium.

The Program Control mode of operation is selected for programs written for the Satellite Computer System. All discussions of MTS circuits or programs in this manual assume that the Program Control mode of operation has been selected unless stated otherwise.

BASIC PRINCIPLES OF OPERATION

The 1607 MTS consists of four digital tape handler units and a synchronizer control unit. The synchronizer control unit has independent read and write channels which permit simultaneous read and write operations. Any one of the four tape handlers may be operated through the synchronizer read channel while another of the four tape handlers may be simultaneously operated through the synchronizer write channel.

The synchronizer read and write channels may be assigned to either the 160 or 1604 computer; or the read channel may be assigned to one computer and the write channel to the other. The MTS also provides for the direct transmission of information between the 1604 and the 160 computers. This is accomplished with a direct line from the synchronizer write channel to the synchronizer read channel which completely bypasses the tape handlers. The available paths for information flow between the two computers are shown in figure 2.

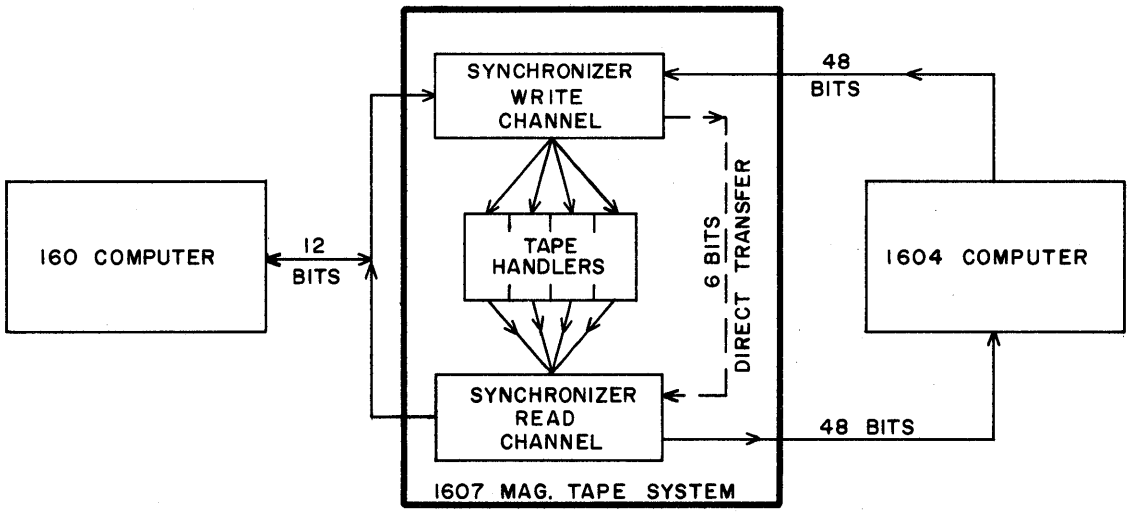


Figure 2. Information Flow in the Satellite Computer System

The 160 uses a single 12-bit channel for both read and write operations. The 1604 uses separate 48-bit channels for read and write operations because it is able to simultaneously read and write on tape. The 160 has separate input and output lines, but only one channel because it cannot read and write on tape simultaneously. The synchronizer read and write channels connect to each of the four tape handlers of the 1607. The dotted line in figure 2 denotes the 6-bit path from the write channel synchronizer to the read channel synchronizer. The tape handlers are bypassed completely to allow a direct transfer of data between the computers.

1607 MAGNETIC TAPE CHARACTERISTICS

These tapes are recorded in a format compatible with IBM magnetic tape equipment. Data is recorded in 6 bits plus a parity bit, commonly referred to as character-serial. A 1604 48-bit word is made up of 8 characters (6 bits each) with no parity. To record one 48-bit word, therefore, the word is disassembled as shown in figure 3, the upper 6 bits first, etc. A parity bit is added at this point.

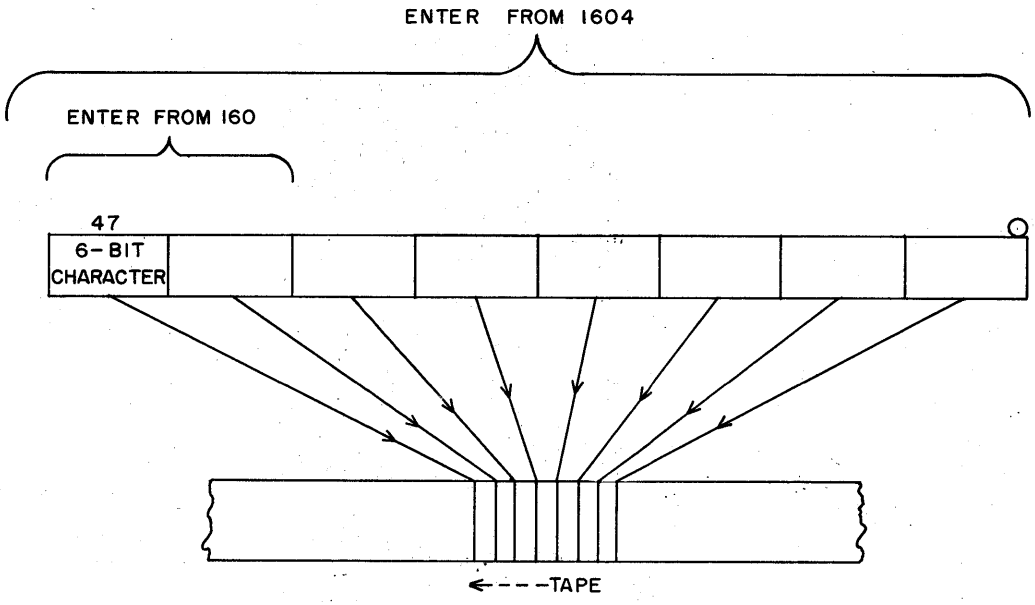


Figure 3. Word Disassembly

To read tape, the characters are read, checked for parity, and assembled into the 48-bit word, first character in the upper 6 bits. When reading or writing on the tape, one 48-bit word is transferred between the 1604 and 1607 for every eight characters on the

tape. The same system of channel controls in the 1607 is easily adapted to handle 12-bit words from the 160 computer. The 12 bits are entered in the upper two character positions of the 48-bit register (figure 3). The upper 6 bits are recorded first, then the lower, followed by another word transfer from the 160. For both 160 and 1604 writing and reading, the characters pass the head at 30, 000 per second. 1604 words transfer at 3750 per second and 160 words transfer at 15, 000 per second.

The 1607 MTS allows either the 160 or the 1604 computer access to the tape handlers. The following operations are available:

Read tape x to 1604 while writing tape y from 1604
Read tape x to 1604 while writing tape y from 160
Read tape x to 160 while writing tape y from 1604
Read tape x to 1604
Read tape x to 160
Write tape y from 1604
Write tape y from 160

The selection of tape handlers x and y is made from the 1604 only.

DIRECT TRANSFER OF DATA

Under Program Control mode, there can be direct transfer of data (D. T.) between the 160 and the 1604. The dotted line in figure 2 shows the direct 6-bit path from the write channel synchronizer to the read channel synchronizer. When using this path, the write control is assigned to one computer and the read control is assigned to the other. In 160 to 1604 transmission, the 12-bit 160 words are disassembled into characters in the write control synchronizer, transferred to the read control synchronizer, assembled into 48-bit words, and sent to the 1604.

For 1604-160 transmission, the 48-bit 1604 words are disassembled into characters in the write control, transferred to the read control, assembled into 12-bit words, and sent to the 160.

Transfer Rates

Since the direct path does not use magnetic tape, the rate of transfer depends only on the read and write controls and the transfer rate of the two computers. These rates are:

1604 word rate (8 characters)	5,000/sec. minimum
	50,000/sec. maximum
160 word rate (2 characters)	50,000/sec.

Therefore the transfer rate varies from 40,000 characters/sec. minimum to 100,000 characters/sec. maximum. There is a delay of approximately 20 usec to set the control circuits before transferring the data. In addition, there is an end of record delay of approximately 600 usec previous to transfer of the last word from the read synchronizer to the input computer. To sense the completion of a D. T., sense channel inactive and then sense read ready, or allow the input computer to flag the output computer when the D. T. is completed.

The 1604 word transfer rate is determined by the cycle time of the auxiliary scanner. This scanner sequentially samples each of the six buffer channels, the interrupt line, and the advance clock circuits. If none of these lines demand processing, the scanner completes one entire cycle in 3.2 usec.

When an auxiliary operation is necessary, the scanner stops at the line demanding action. The computer is forced to halt execution of the main program and to perform the indicated operation by entering the auxiliary sequence. When the request has been satisfied, the computer returns to the main program and the scanner resumes operation with the next count.

In the slowest case (action demands by all six buffer channels occurring with consecutive 66 usec instructions) communication is limited to a 5000 word/sec. rate. Ordinarily the word rate may be expected to be closer to 50,000/sec. The 160 character rate of 100,000/sec. is usually the limiting factor.

EXTERNAL FUNCTION CODES

1604 Only or 160 Only

With an independent operation the control and transfer of data to and from magnetic tape is accomplished exactly as in a non-satellite system. The following external functions apply:

Select	1604 Code	160 Code
Select read tape n, binary	320n1	50n1 *
Select read tape n, coded	320n2	50n2 *
Select write tape n, binary	420n1	60n1 *
Select write tape n, coded	420n2	60n2 *
Select previously selected read tape, binary	32001	5001 **
Select previously selected read tape, coded	32002	5002 **
Interrupt when selected read tape ready	32004	--
Rewind selected read tape	32005	5005
Backspace selected read tape	32006	5006
Rewind selected read tape, interlock	32007	5007
Select previously selected write tape, binary	42001	6001 **
Select previously selected write tape, coded	42002	6002 **
Write end-of-file mark	42003	6003
Interrupt when selected write tape ready	42004	--
Rewind selected write tape	42005	6005
Backspace selected write tape	42006	6006
Rewind selected write tape, interlock	42007	6007
Status request	---	6053

The External Sense instruction of the 1604 obtains specific status information. The 160 status request causes all status indicators to enter as a single 12-bit word, which is examined by the 160 program. The correspondence between the 1604 Sense Codes and the bit position of each indicator in the 160 input word is as follows:

---

* Available only when 1607 manually assigned to the 160.

** Useful for making read and write selects on Program Control mode.

Sense	1604 Sense Code	160 Status Response
Not ready to read	32000-1	X2XX
Read parity error	32002-3	XX4X
Read length error	32004-5	---
End-of-file mark	32006-7	XX1X
Not ready to write	42000-1	X1XX
Write reply parity error	42002-3	XX2X
Write reply length error	42004-5	---
End of tape marker	42006-7	XXX4

Program Control Programming

The following additional SELECT and SENSE codes are available for the Program Control mode of operation.

Select	1604 Code	160 Code
Select Read control for 160	32501	---
Release Read control to 1604	32502	5052
Select Write control for 160	42501	---
Release Write control to 1604	42502	6052
Select Direct 1604 to 160	42503	---
Select Direct 160 to 1604	32503	---
Release Direct selections	42500	---
Select Action request	42504	---
Select Interrupt	---	5053
Release Interrupt	32505	---
Release Action request	---	6050
Set communication flag 1	42540	5051
Clear communication flag 1	42560	6055
Set communication flag 2	---	6051
Clear communication flag 2	42520	6056

Sense	1604 Sense Code	160 Status Response
Read control available	32500-1	4XXX
Write control available	42500-1	2XXX
160 Action request	----	XXX2
Direct 160 to 1604	----	1XXX

Sense	1604 Sense Code	160 Status Response
Direct 1604 to 160	----	X4XX
160 interrupt	32504-5	---
Communication flag 1 set	42560-1	XXX1
Communication flag 2 set	42520-1	---

DIRECT TRANSFER

When the 1604 selects Direct Transfer (D. T.), a series of interlocks and delays are set in the 1607. Before the write chain is set the read chain must be set (figure 4). For this reason a sense on read or write ready is not valid until the D. T. has started. No information can pass through the write chain until the receiving computer has given the input command and is ready to receive information. For example, if the 160 gives an output instruction before the 1604 input buffer is activated, an AND circuit holds the write chain until the 1604 activates the buffer and sets the read chain. When both the write and read chains are set, information is transferred. There is no parity check on directly transferred data.

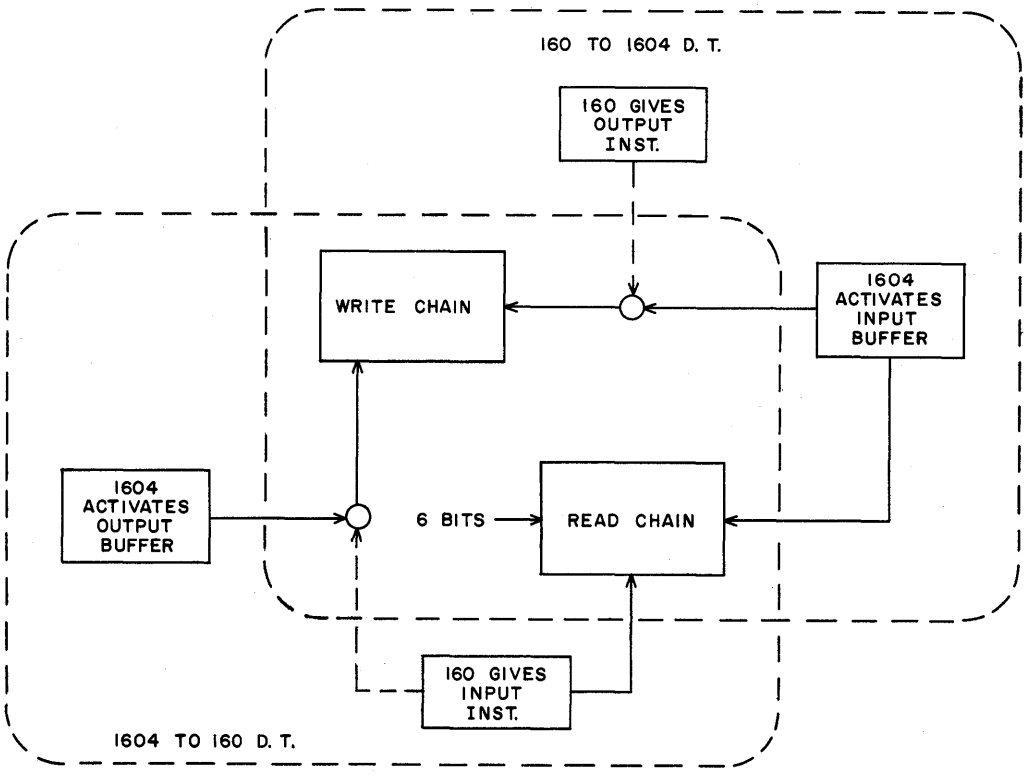


Figure 4. Direct Transfer Sequences

The AND circuits release the programmer from timing considerations in the direct transfer sequence of instructions. However, it is advisable for the two computers to give their input-output commands as close together as possible. If the 160 gives an input or output instruction before the 1604 activates the buffer, the 160 is held up on its instruction until the D. T. is completed. The 160 Action Request, Flag 1 and Flag 2 codes are useful in coordinating the instructions of the two computers.

Flag 1 can be set, cleared and sensed by either computer while Flag 2 can be cleared by either computer but can be set only by the 160 and sensed by the 1604. A 1604 external master clear will clear both Flags.

For direct transfer of information the 1604 and the 160 must be in close contact with one another. Efficient programming can keep to a minimum the amount of time wasted by one computer waiting for the other.

For example, in a 1604 to 160 D. T., the 1604 can prepare for the transfer, notify the 160, and continue with other operations while the 160 completes the D. T. The 160 must make appropriate selections followed by an input instruction as soon as the action request is received from the 1604. In this way the transfer is effected immediately, and the 160 is not held up on input-output operations.

CONTROLS

Program Control operation requires a set of controls for selecting and performing each operation. Each computer has a similar list of selections available to it.

Common Controls

Read Controls

Read selected read tape, binary
Read selected read tape, coded
Backspace selected read tape
Rewind selected read tape
Rewind and interlock selected read tape
Release read control to 1604

Write Controls

Write selected write tape, binary
Write selected write tape, coded
Backspace selected write tape
Rewind selected write tape
Rewind and interlock selected write tape
Release write control to 1604

The common controls listed above are essentially the same for each computer.

Each computer also has separate selections for controlling the 1607.

1604 Selections

Select interrupt on read channel ready
Select interrupt on write channel ready
Select direct transfer (D. T.) from 160 to 1604
Select direct transfer (D. T.) from 1604 to 160
Clear direct transfer selection
Select 160 action request
Clear 160 interrupt
Select tape unit N for writing, binary
Select tape unit N for writing, coded
Select tape unit N for reading, binary
Select tape unit N for reading, coded
Select read control for 160
Select write control for 160

160 Selections

Select interrupt 1604
Release 160 action request

The 1604 and 160 can select their interrupt conditions when either computer has control of the 1607. The 1604 can select a particular tape for reading or writing only when it has read or write control.

Both computers can select write or read control for the 1604, but only the 1604 can select write or read control for the 160. The Read I and Write I flip-flops (figure 5) are normally set by the 1604 and cleared by the 160. These flip-flops can be sensed by either computer.

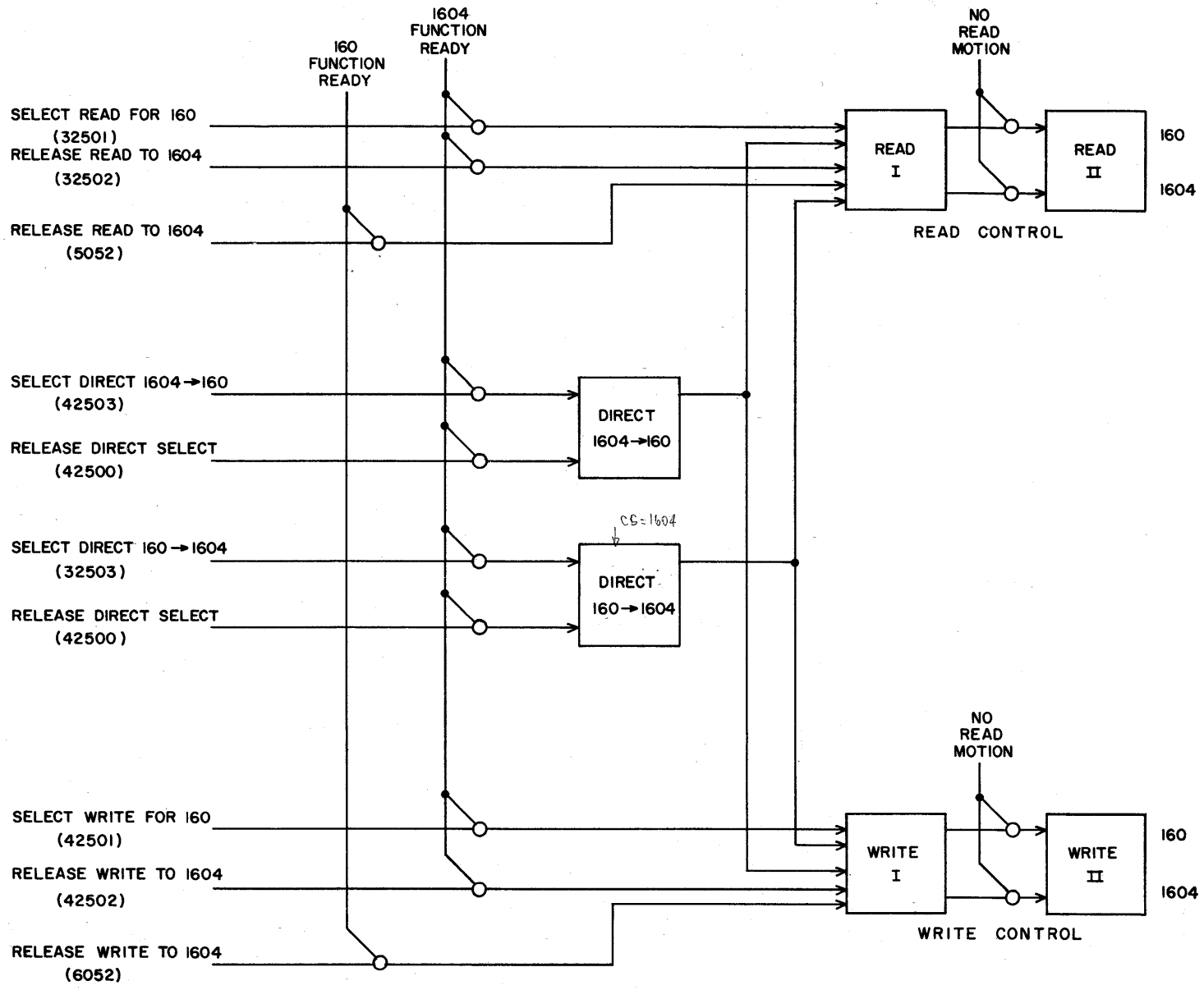


Figure 5. Computer Control Selection

When one computer selects channel control for the other computer certain interlocks take over. The Read I and Write I flip-flops will not receive a release selection from both computers simultaneously since one computer will consider that it already has the channel. The Read II and Write II flip-flops actually control the channels and are changed only when all previous motion is complete. The changing of the state of the control flip-flops clears the corresponding read or write select flip-flop. Therefore, before using control, the controlling computer should make the proper read or write selects.

Typical operation of an on-line Satellite System assigns the 1604 as the master control. When a 160 uses either direct transfer or tape operations, it must first interrupt the 1604. A typical sequence then follows:

... 160 interrupts 1604
... 1604 recognizes the interrupt and, in order to determine what the 160 wants, either senses the Flags or selects a Direct Transfer from 160 to 1604.
... In this example the 160 recognizes a Direct Transfer selection. The 160 selects write select, 1604 selects read select.
... The request is transferred from 160 to 1604.
... Any return communication is set up and transferred.
... The 1604 selects read or write control for the 160.

When the 160 completes the operation, it releases read or write control to the 1604. If the 1604 allows only a set time period for the 160 to use control, the 1604 is able to withdraw control. In this event the 1607 completes the current record (or motion).

Only the 1604 can select a particular tape unit for write or read operations. The 1604 must have write or read control when it selects a unit for writing or reading. In order for the 160 to write on tape n, the 1604 must first select write control, select unit n for writing, and then give write control back to the 160. A sequence similar to this is used in the program example which follows.

SATELLITE PROGRAMMING EXAMPLE

This program example illustrates the programming sequences used in the Satellite Computer System. Only the programming required for Satellite operations is shown; no attempt is made to make efficient use of time for both computers.

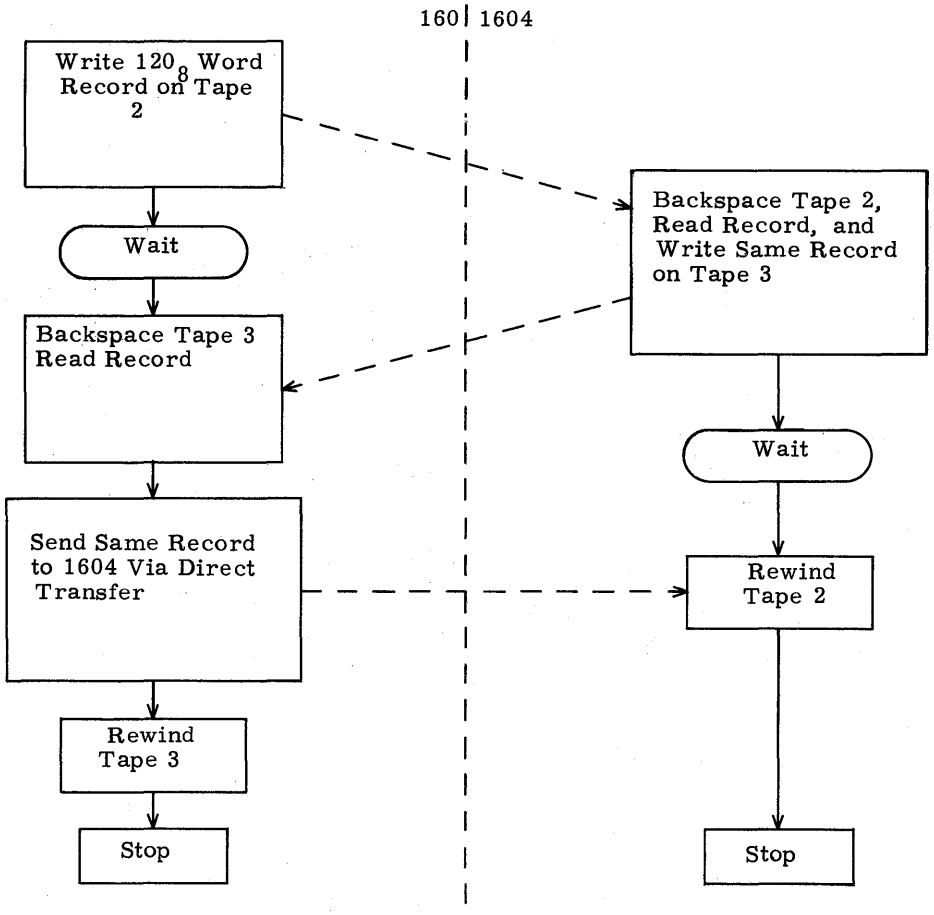


Figure 6. Simplified Flow Chart

This example assumes that the 1604 knows that it will be interrupted three times and jumps to the three interrupt routines in order.

The 1604 could also set up a 160 → 1604 D. T. communication each time it is interrupted. In this way the 160 can tell the 1604 why it is being interrupted and the 1604 can decide then what to do. Another approach would be for the 160 to send the actual 1604 instructions it wants executed to the 1604. The 1604 would receive the data and then transfer to the first word received.

SATELLITE PROGRAM EXAMPLE

PART I - 160 PROGRAM

```
START   EXF   WRTCNL    Select write control for 1604
        EXF   INTRPT    Interrupt the 1604 (first interrupt)
```

Note: Under Program Control mode only the 1604 can select particular tape units for reading or writing. For this reason, the 160 must interrupt the 1604 to select tape 2 for writing. The 1604 must have write control at the time it selects the unit for writing. After selection, the 1604 notifies the 160 by selecting 160 Action Request, which the 160 should be sensing (see below).

```
WAIT1   EXF   STATUS    Status request
        INA   00        Wait for
        LPN   02          action request
        ZJB   WAIT1         from 1604
        EXF   ACTION    When received, the action
        REM               request should be immediately
        REM                 released
        EXF   WRTSEL    Select write select
        OUT   BGNA      Write block (1000-1120)8 on
ENDA            1120      selected tape (2)
        EXF   STATUS    Status request
        INA               wait till
        LPF   READY         ready to
        NZB   03              write
        EXF   RDCNRL    Then give read
        EXF   WRTCNL      and write controls to
        EXF   INTRPT    the 1604 and notify via
        REM             another interrupt (the 2nd)
        JFI   01
              PAGE2
READY         0100
INTRPT        5053
STATUS        6053
ACTION        6050
BGNA          1000
WRTSEL        6002
```

Note: The 1604 during the second interrupt will read the record written by the 160 on tape 2, write the identical record on tape 3, and then select tape 3 for reading. When finished, the 1604 will select 160 Action Request, which the 160 should be sensing. The 160 could be doing other work while waiting, but in our example the 160 just waits.

```
        EXF     STATUS      Status
        INA                   request
        LPN     02          Wait for
        ZJB     PAGE2         action request
        EXF     RDSEL       Select read select
        EXF     BCKSPC      Backspace selected read tape
        REM                 (The 1604 had selected tape 3
        REM                 for reading previous to sending
        REM                 the last action request to the 160.)
        EXF     STATUS      Wait till
        INA     00            ready
        LPF     READ            to read
        NZB     03
        INP     BGNB        Read record into (2000-2120)8
ENDB            2120        From selected read
        REM                   tape (3).
        EXF     STATUS      Status request
        INA                   wait till
        LPF     READ            ready
        NZB     03                to read
        EXF     INTRPT      Interrupt 1604 when ready
        REM                   (3rd interrupt)
WAIT3   EXF     STATUS      Wait
        INA                   till
        LPN     01              contacted by
        ZJB     WAIT3       1604 via Flag 1
        JF1     01
                PAGE3
READY           0100
RDCNRL          5052
WRTCNL          6052
BCKSPC          5006
STATUS          6053
READ            0200
BGNB            2000
INTRPT          5053
RDSEL           5002
```

Note: When interrupted for the third time, the 1604 prepares for a direct transfer from 160 to 1604. When ready, the 1604 sets Flag 1 which must be sensed by the 160. The 160 can then go ahead with the D. T. (below).

```
        EXF     FLAG1       Clear Flag 1
        EXF     WRTSEL
        OUT     BGNB        Send information to
                2120          1604 from (2000-2120)8
        EXF     STATUS      Status request
        INA     00          Wait till ready to read. This
        LPF     READ        indicates that the D. T. has been
        NZB     03          completed and it is safe for the 1604
        REM                 to release the D. T. selection. 1
        EXF     FLAG2       set Flag 2
```

```
          EXF     STATUS          Wait
          INA                      for
          LPN     02                 action request
          NZB     03                   from 1604
          EXF     ACTION          Release action request
          EXF     REWIND          Rewind selected read tape (3)
          HLT     00
REWIND              5005
BGNB                2000
READ                0200
INTRPT              5053
STATUS              6053
FLAG1               6055          Clear Flag 1
FLAG2               6051          Set Flag 2
ACTION              6050
WRTSEL              6002
```

PART 2 - 1604 PROGRAM

Explanation: Each time the 1604 is interrupted, the 1604 automatically jumps to the lower instruction of address 00007. For this example, address 00007 jumps to a transfer routine which will (a) release interrupt selection (EXF 0 32505B) and (b) transfer to the next interrupt routine. The interrupt routines are shown below.

First Interrupt

Note: Before interrupting the 1604 the 160 had given write control to the 1604. Thus, the 1604 can select a particular tape for writing.

```
INTRPT1   EXF   0   42022B   Select tape unit 2 for writing (coded)
          EXF   7   42000B   Exit on ready to write
          EXF   0   42501B   Give write control back to 160
          EXF   0   42504B   Send action request to 160
          SLJ   0   00007B   Back to main program via cell 7
```

Second Interrupt

Note: The 160 had given read and write controls to the 1604 before the second interrupt.

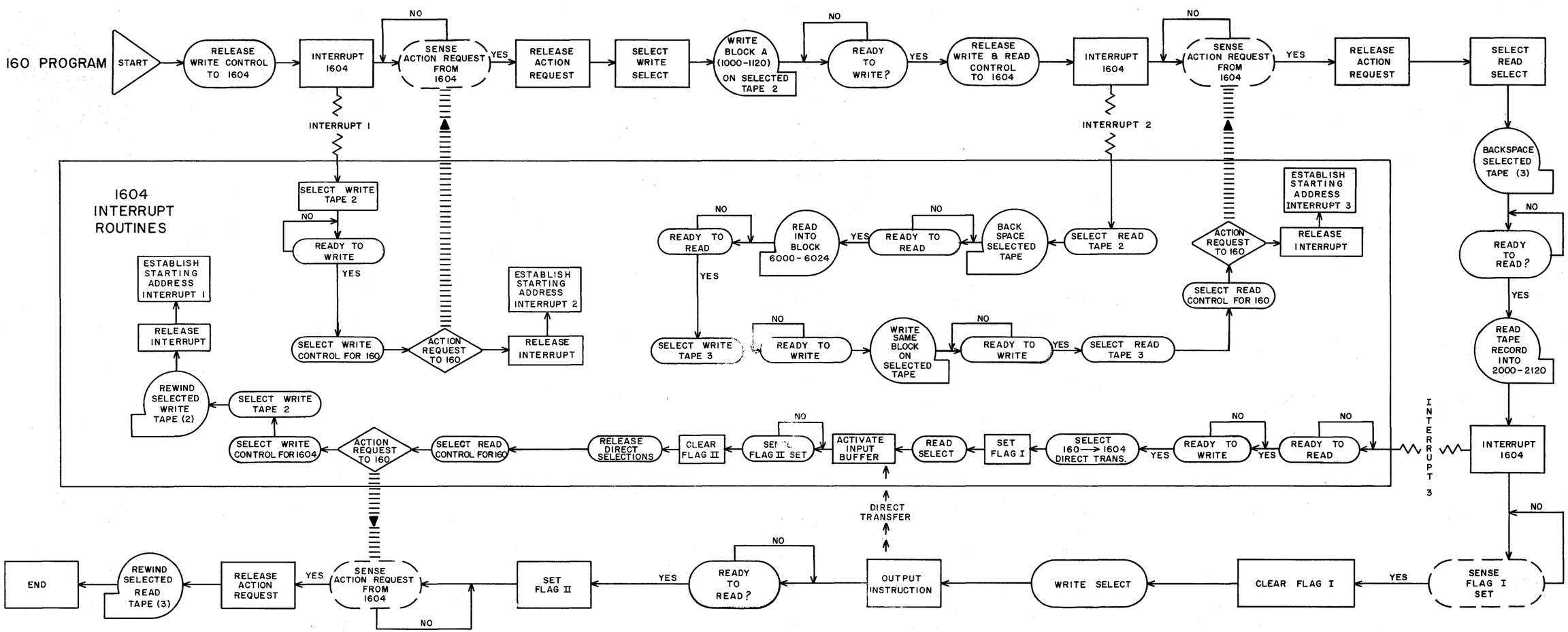
```
INTRPT2   EXF   0   32022B   Select tape 2 for reading, (coded)
-         EXF   7   32000B   Exit on ready to read
          EXF   0   32006B   Backspace selected read tape (2)
          ENA   0   06024B   Set up terminal
          STA   0   00003B     for input buffer
-         EXF   7   32000B   Exit on ready to read
          EXF   3   06000B   Read into (6000-6204)8
-         EXF   7   32000B   Exit on ready to read
          ENA   0   06024B   Set up terminal
          STA   0   00004B     for output buffer
          EXF   0   42032B   Select tape 3 for writing
```

```
-           EXF   7   42000B    Exit on ready to write
            EXF   4   06000B    Write on selected unit (3)
-           EXF   7   42000B    Exit on ready to write
            EXF   0   32032B    Select tape 3 for reading (coded)
            EXF   0   32501B    Select read control for 160
            EXF   0   42504B    Send action request to 160
            SLJ   0   00007B    Back to main program
```

Third Interrupt

Note: Here the 1604 prepares for direct transfer and notifies the 160 using Flag 1. Note that selecting 160 - 1604 direct transfer automatically gives the 160 write control and the 1604 read control.

```
INTRPT3     NOP                 Pass
            EXF   7   32000B    Exit on Ready to Read
            EXF   7   42000B    Exit on Ready to Write
            EXF   0   32503B    Select 160 → 1604 Direct Transfer
            ENA   0   07024B    Set up Terminal for
            STA   0   00003B      receiving data
            EXF   0   42540B    Set Flag 1
            EXF   0   32001B    Select Read Select
            EXF   3   07000B    Read (Activate Input Buffer)
            EXF   7   42520B    Exit on Flag 2 set
            EXF   0   42520B    Clear Flag 2
            EXF   0   42500B    Release Direct Transfer Selection
            EXF   0   32501B    Select Read Control for 160
            EXF   0   42504B    Send Action Request to 160
            EXF   0   42502B    Select Write Control for 1604
            EXF   0   42022B    Select Unit 2 for Writing (Coded)
            EXF   0   42005B    Rewind Selected Write Tape (2)
            SLJ   0   00007B    Back to Main Program
```



SATELLITE PROGRAM EXAMPLE

1607 EXTERNAL FUNCTION CODES (CH 3 & 4)

SELECT CODES	1604	160
Select read tape n, binary	320n1	50n1*
Select read tape n, coded	320n2	50n2*
Select write tape n, binary	420n1	60n1*
Select write tape n, coded	420n2	60n2*
Select previously selected read tape, binary	32001	5001**
Select previously selected read tape, coded	32002	5002**
Interrupt when selected read tape ready	32004	
Rewind selected read tape	32005	5005
Backspace selected read tape	32006	5006
Rewind selected read tape with interlock	32007	5007
Select previously selected write tape, binary	42001	6001**
Select previously selected write tape, coded	42002	6002**
Write end of file mark	42003	6003
Interrupt when selected write ready	42004	
Rewind selected write tape	42005	6005
Backspace selected write tape	42006	6006
Rewind selected write tape with interlock	42007	6007
Status Request		6053

* Available only when 1607 is operating in the 160 mode.

** Also used for making read and write selects when the 1607 is operating in the program control mode.

SENSE CODES	1604	160
Exit on ready to read	32000	
Exit on NOT ready to read	32001	X2XX
Exit on read parity error	32002	XX4X
Exit on NOT read parity error	32003	
Exit on read length error	32004	
Exit on NOT read length error	32005	
Exit on end of file mark	32006	XX1X
Exit on NOT end of file mark	32007	
Exit on ready to write	42000	
Exit on NOT ready to write	42001	X1XX
Exit on write reply parity error	42002	XX2X
Exit on NOT write reply parity error	42003	
Exit on write reply length error	42004	
Exit on NOT write reply length error	42005	
Exit on end of tape marker	42006	XXX4
Exit on NOT end of tape marker	42007	

The following additional SELECT and SENSE codes are available for the 1607 Program Control mode of operation.

Select read control for 160	32501	
Release read control to 1604	32502	5052
Select write control for 160	42501	
Release write control to 1604	42502	6052
Select direct 1604 to 160 (selects write control 1604, read control 160)	42503	
Select direct 160 to 1604 (selects write control 160, read control 1604)	32503	
Release direct selections (necessary before selecting read or write control)	42500	
Select 160 action request	42504	
Select 1604 interrupt		5053
Release 1604 interrupt	32505	
Release 160 action request		6050
Select Flag I set	42540	5051
Select Flag II set		6051
Release Flag I	42560	6055
Release Flag II	42520	6056

Note: Code for alternate 1607: 33XXX and 43XXX.

Exit on read control available to 1604	32500	
Exit on read control NOT available to 1604	32501	
Exit on read control available to 160		4XXX
Exit on write control available to 1604	42500	
Exit on write control NOT available to 1604	42501	
Exit on write control available to 160		2XXX
Exit on 160 action request		XXX2
Exit on direct 160 to 1604		1XXX
Exit on direct 1604 to 160		X4XX
Exit on 160 interrupt of 1604	32504	
Exit on NOT 160 interrupt of 1604	32505	
Exit on Flag I set	42560	XXX1
Exit on Flag I clear	42561	
Exit on Flag II set	42520	
Exit on Flag II clear	42521	

1607 MAG TAPE TEST

1. ~~MACHINE LOAD PAPER TAPE FROM P = 0000. NORMAL STOP P = 3777.~~ LOAD ROUTINE 11 OR ROUTINE 27 DEPENDIN ON TAPE.

2. MOUNT TAPES TO BE TESTED AT LOAD PT. WITH WRITE RINGS IN.

3. ~~CLEAR AND ENTER OCTAL DATE. FIRST THE DAY NUMBER, FOLLOWED BY THE MONTH AND YEAR. (1970 = 3662) AND RUN.~~

3. CLEAR AND ENTER OCTAL DATE. LOA
A = 00XX WHERE XX IS THE DAY NUMBER. NORMAL STOP Z = 7777. REPEAT FOR MONTH AND YEAR NUMBERS (IN THAT SEQUENCE, (NOTE: $1970_{10} = 3662_8$)).

4. ENTER ~~INTO~~ A = KLMN. WHERE K, L, M, N ARE THE LOGICAL UNIT NUMBERS OF THE TAPES TO BE TESTED. TURN ON PAPER TAPE PUNCH AND RUN.

5. TO LIST THE PAPER TAPE CONTAINI THE RESULTS SET P = 3000. PUT TAPE IN READER AND ACTIVATE THE 1612 LINE PRINTER AND RUN.

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