89858800

CONTROL DATA CORPORATION

CONTROL DATA®
FC602-A
DISTRIBUTED CLUSTER
LOCAL CONTROLLER

GENERAL DESCRIPTION
OPERATION AND PROGRAMMING
INSTALLATION AND CHECKOUT
THEORY OF OPERATION
DIAGRAMS
MAINTENANCE
MAINTENANCE AIDS
PARTS LIST
WIRE LIST

REFERENCE / CUSTOMER ENGINEERING MANUAL

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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

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MANUAL REV	FCO OR ECO	SERIES	S/N	LOGIC DIAGRAM			
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PREFACE

This manual supplies reference information for the CONTROL DATA CORPORATION® FC602-A Cluster Multiplexer Local Controller. This equipment, used with the AB107/AB108 Computer, controls up to eight key entry stations at a remote location. A knowledge of the computer, Modems, and key entry stations to be used is required before using this controller.

The following CONTROL DATA® publications may be useful as references:

Publication	Pub. No.
1784 Computer Reference Manual	89633400
AB107/AB108 Computer Customer Engineering Manual	89633300
I/O Specification Manual	89673100
SYSTEM 17 Installation Manual	88996000
OLYMPUS 1700 Diagnostic Package	39268100
FC701-A/B Reference/Customer Engineer Manual	89858300

NOTE: The names FC602-A Distributed Cluster Local Controller and FC602-A Cluster Multiplexer Local Controller are synonymous. The Cluster Multiplexer Local Controller name and its abbreviation, CMLC, are used exclusively throughout this publication.

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GENERAL DESCRIPTION

GENERAL DESCRIPTION

INTRODUCTION

The CONTROL DATA® FC602-A Cluster Multiplexer Local Controller (CMLC) is a special purpose communications multiplexer which allows up to eight key entry stations (CC108-A, or equivalent), to operate at a remote location in a CYBERDATA™ Key-To-Disk Data Entry System, or in similar applications.

The FC602-A local controller connects to the AB107 or AB108 computer via the A/Q channel. The local controller's logic circuitry is mounted on a single printed-wiring (PW) board, which fits into any A/Q position of the computer or the BT148 expansion enclosure.

A second controller at the remote end, the FC701-A or B Cluster Multiplexer Remote Controller (CMRC), operates in conjunction with the local controller to multiplex a remote cluster of terminals.

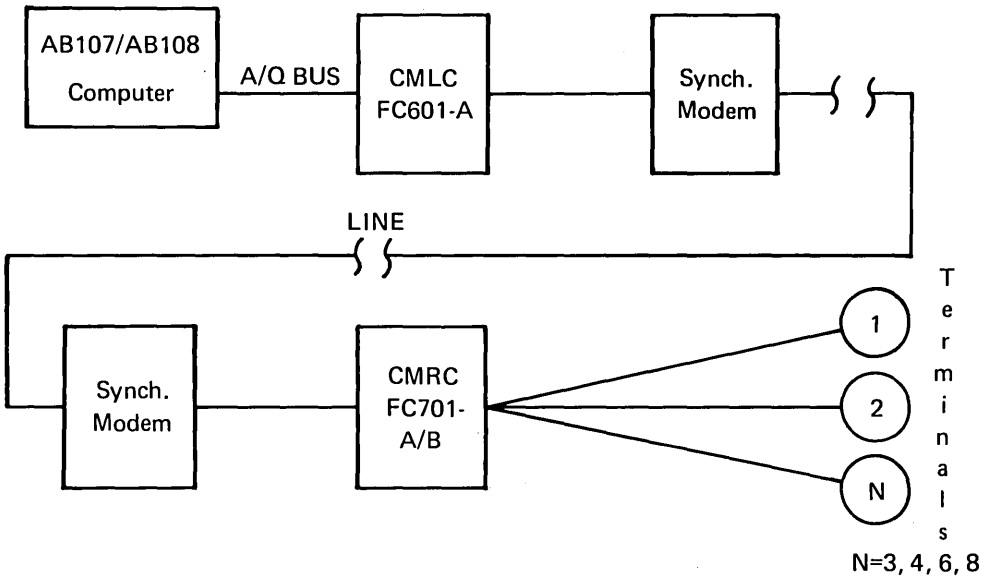


Figure 1-1. System Block Diagram

Data is transmitted and received over the line by two synchronous Modems (not part of the equipment) with EIA RS-232-C interface. Modems with 2400, 4800, or 9600 baud (bits per second) can be used.

The FC602-A is connected to a synchronous Modem in a duplex data transmission configuration.

The physical connection to the Modem consists of an internal cable (89641800) connected from P2 of the PW board to the computer's I/O connector panel and an external cable (89859300) connected between the computer's connector panel and the Modem. The standard and maximum length of the external cable is 25 feet.

Specifications

Data Format

The maximum number of terminals that can be multiplexed is jumper set to 3, 4, 6 or 8.

Time Division Multiplexing is used to assign each terminal a specific time slot to send or receive data.

The repetitive data block format consists of eight sync bits followed by eight data blocks, each block consisting of the characters multiplexed to and from the terminals. Each character consists of seven data bits plus one even parity bit. An all-zero character is used as an idle filler.

PARITY Generation/Checking

Each character received is checked for even parity. A parity error results in a status bit sent to the central processor. To each 7-bit character output by the computer an even parity bit is appended before transmission.

DATA BUFFERING

Data buffers for each terminal consist of two receive character buffers and two transmit character buffers.

DATA RATE

The data output rate (characters per terminal per second) is a function of the Modem baud rate, number of terminals selected, and the sync pattern length. The table below presents the maximum data rate, assuming the terminal baud rate is high enough to allow such a rate.

TABLE 1-1. DATA RATES

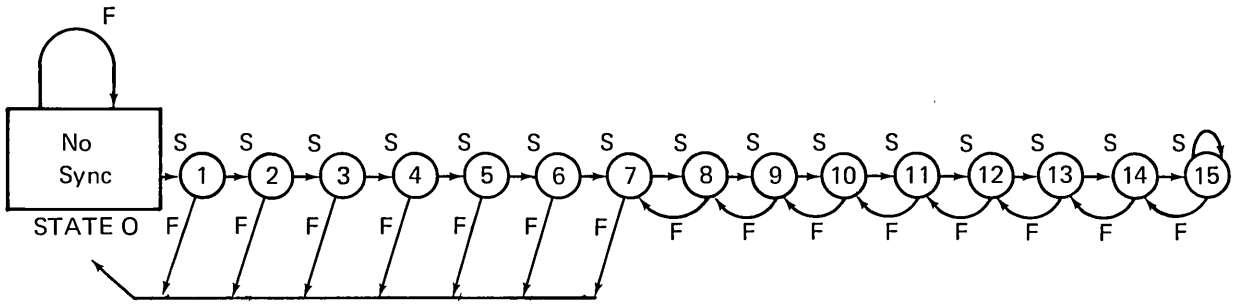
Modem Baud Rate \ Maximum Number of Terminals Multiplexed	3	4	6	8
2400	96	72.7	48.9	36.9
4800	192	145.4	97.9	73.8
9600	384	290.9	195.9	147.7

SYNCHRONIZATION

A synchronizing character is transmitted and received after every eight data blocks; the synchronization character is 10010110. The receiving circuits comprise a fly-wheel type of synchronizing logic which performs according to the state diagram.

In states 0 - 7 FC602-A is out of synchronization.

In states 8 -15 FC602-A is synchronized.



S = Sync character received correctly in the calculated time slot

F = Sync character received incorrectly in the calculated time slot

Figure 1-2. Synchronization State Diagram

REAL TIME CLOCK

A periodic clock interrupt is generated by dividing the transmitter signal element timing received from the Modem. The clock period is adjustable by jumper to the baud rate and the required interrupt period. The jumpers divide the baud rate by one of the following ratios: 12, 24, 48, 96. The combination of these division ratios and the Modem baud rates are presented below (clock interrupts are in milliseconds).

TABLE 1-2. CLOCK INTERRUPTS

Division Ratio \ Baud Rate	2400	4800	9600
12	5	2.5	1.25
24	10	5.0	2.50
48	20	10.0	5.00
96	40	20.0	10.00

INTERFACE TO MODEM

Interface circuits comply with RS-232-C. The physical connection comprises an internal cable from P2 of the CMLC PW board to the computer's connector panel and an external cable 89859300 from the computer's connector panel to the Modem. The length of the cable is 25 feet and is fitted with a 25-pin connector.

Electrical Requirements

Power required for the local controller is +5 volts ±5%, supplied by the computer. Current required is $2^{1}/2$ amperes with a maximum of 2.75 amps.

TABLE 1-3. ENVIRONMENTAL SPECS

Specification	Explanation
Temperature	
Shipping	-40°F to 158°F (-40°C to 70°C)
Storage	14°F to 122°F (10°C to 50°C)
Operating	40°F to 120°F (5°C to 50°C)
Humidity	
Shipping	0 to 100% RH non-condensing
Storage	10% to 90% RH non-condensing
Operating	10% to 90% RH non-condensing

SECTION 2

OPERATION AND PROGRAMMING

OPERATION AND PROGRAMMING

Operation

Operation of the system is under program control.

Programming

Q-Register Format

Instructions to the controller are determined by a 16-bit word contained in the computer Q register (Figure 2-1)

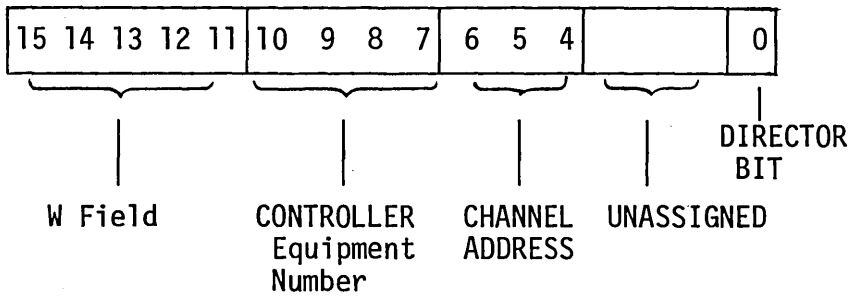


Figure 2-1. Computer Q-Register Word Format

The controller is connected to the computer when the following conditions are met:

a) Suitable equipment code on Q07 - Q10

b) The W = 0 line is active

c) The Read or Write lines are active.

The controller ignores all the unassigned Q register bits.

The controller communicates with the computer or terminal depending on the state of Director bit Q00.

TABLE 2-1. CONTROLLER FUNCTION VS STATE OF DIRECTOR BIT Q00

Q00 = 0	Q00 = 1
Associated with data transfer to and from the channels (terminals)	Associated with the Real Time Clock and Protect Status.

NOTE

In certain cases, two clusters containing four or less terminals at different locations can be connected via two local controllers, each assigned the same equipment number. In this "extended" equipment number mode, the state of Q06 in the Q register determines which one of the two clusters is being addressed.

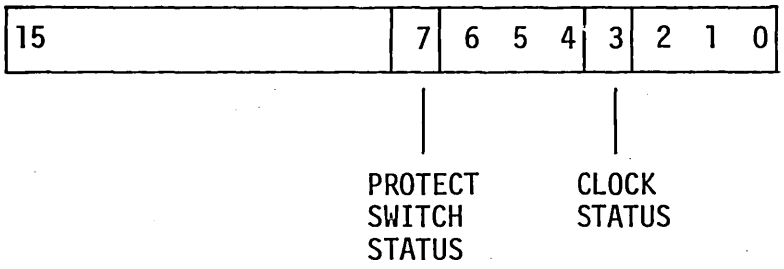
For example: if Q06 = 0, cluster 1, terminals 1-4 are addressed (as determined by channel address bits Q04 and Q05).

if Q06 = 1, cluster 2, terminals 5-8 are addressed (channel address bits Q04 and Q05).

This mode of addressing is fixed by jumpers set on the pc board. With such a mode of operation, fewer equipment numbers are required. The result is a savings in memory when software packages assign the terminal buffer and table areas in blocks of eight for each equipment number used.

A-Register Format

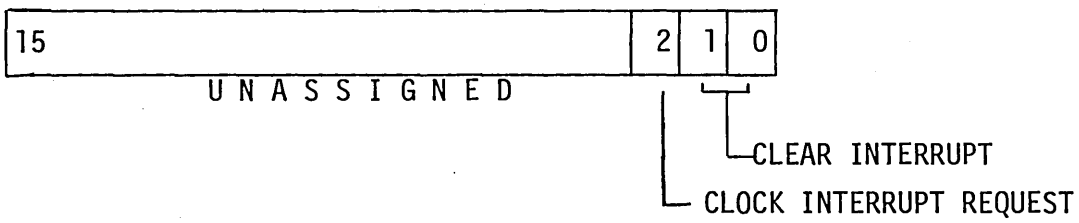
Q00 = 1: Status from the controller: when an input status instruction from the CMLC is performed, the A-register contents will adopt the following pattern:



A07 is set if the CMLC protect jumper is connected in the protect mode.

A03 is set if the CMLC internal clock has performed a time count from the last time it was reset.

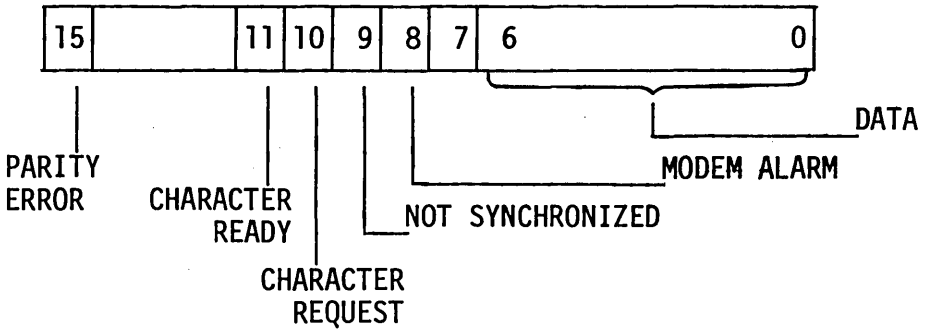
Q00 = 1: Function to the controller: when output function instructions to the CMLC are performed, the Q-register should be set to the following form:



1) When either A00 or A01 are set, the output instruction will clear the interrupt circuit, the interrupt request circuit, and the interrupt clock status bit.

2) When A02 is set, the real time clock interrupt circuits are activated. An interrupt will be generated and applied to the computer when the next clock pulse is received. The occurrence of the next clock pulse can fall within any time between zero and the full clock period. A set A02 bit overrides the operation of bits A00 and A01 with respect to the clock interrupt request circuits.

Q00 = 0: Input from the channel: when input data and status instructions directed to a specific channel are performed, the A register adopts the following format:



1) A00 - A06 contain a data word from a remote terminal.

2) A08 (Modem Alarm) when set indicates the Modem signal's "Data Set Ready" or "Received Line Signal Detector" is in the OFF state.

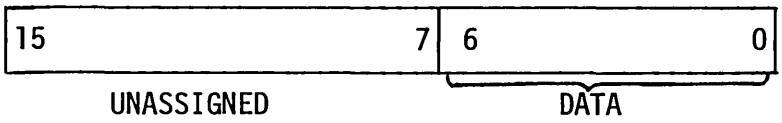
3) A09 (Not Synchronized) when set indicates the receiving circuitry is out of synchronization.

4) If A10 is set, the CMLC is ready to receive a character for transmission on the addressed channel.

5) When A11 is set, a valid received data character is present in bits A00 - A06.

6) When A15 is set, a parity error was detected when the character present in bits A00 - A06 was received.

QOO = 0: Output to channel: when an output data instruction directed to a specific channel is performed, the A register format is as follows:



NOTE

Since a character of all zeroes is used as an idle filler by the time division multiplexer, an all-zero character cannot be used as data. The all-zero character requires a time slot as all other characters do, however this character is not transferred to the terminal by the CMRC.

Reply/Reject

1) Output instructions creating a protect violation according to the I/O specifications for the AB107/AB108 computer cause a reject response.

2) Input instructions with QOO = 0 creating a protect violation according to the I/O Specification for the AB107/AB108 computer cause a reject response.

3) Output instructions with QOO = 0 directed to the channels, which do not have the character request flag set, cause a reject response. This reject directs the program to try and repeat the output instruction after a delay, allowing the transmitted data buffer to become available after the previously stored character is transmitted.

4) In all other correctly addressed I/O operations, a reply response is generated.

The Reply/Reject response is summarized in the table below.

TABLE 2-2. REPLY/REJECT CONDITIONS

	WRITE		READ	
	Q00 = 0	Q00 = 1	Q00 = 0	Q00 = 1
REJECT	Protect violation or status bit Q10 of addressed channel not set	Protect Violation	Protect Violation	Not Applicable
REPLY	No protect violation and status bit Q10 of addressed channel set (character request)	No Protect Violation	No Protect Violation	Always a Reply signal

System Operation With Slow Terminals

If the data rate of a remote terminal(s) is slower than the maximum data rate of the line (as indicated in Table 1-1 of data rates), the programmer must take the necessary precaution to insure the output from the computer to the CMLC is equal to, or less than, the data rate of the addressed device.

Two ways to overcome this mismatch in rates are:

1) by using the real time clock generated by the CMLC to control the output rate of the computer, or

2) by interleaving the data with all-zero characters, which will be ignored by the CMRC.

EXAMPLE:

Suppose a printer operates at 30 characters per second on a 2400-baud line, and the maximum number of terminals multiplexed is eight. The maximum data rate the system allows is 36.9 characters/terminal/second (Table 1-1). If an all-zero character is transmitted after every four actual data characters, the terminal will receive an average data rate of 29.5 characters/second.

(The double buffer feature in the CMRC will smooth out the bursts).

Lost Data — No programming aid is available to identify lost data. However, choosing the correct interrupt clock period will prevent such an event. The receiving circuits are equipped with a double buffer for each channel to minimize such occurrences.

Error Detection with Receive-Only Terminals

The possibilities of error detection of the data sent to receive-only terminals are discussed in the Cluster Multiplexer Remote Controller FC-701-A/B Manual 89858300.

SECTION 3

INSTALLATION AND CHECKOUT

INSTALLATION AND CHECKOUT

INSTALLATION

Unpacking

1. Carefully remove wrapping from the controller printed circuit board. Check for physical damage and record damage on the packing list. Check that part numbers agree with the packing list.

2. Remove wrapping from the cables and check for physical damage. Record damage on the packing list. Check that part numbers agree with the packing list.

3. Report all damage to both the shipping company and the CDC division that shipped the equipment.

Physical Limitations

Care must be taken to prevent damage to the controller card. The card must not be flexed, bent, dropped or exposed to extremes of temperature or humidity in excess of those described in Table 1-3.

Power Requirements

The controller card requires +5 vdc derived from the power supply of the computer.

Cabling and Connectors

An external interconnecting cable (part No. 89859300) connects the 66-pin connector of the controller with the Modem. The standard and maximum length of the cable is 25 feet.

The internal cable (part No. 89641800) used between the back of the computer and the connector pins on the back plane is 15.5 inches long.

A single wire (part number 89724700) connects the CMLC to the appropriate interrupt level from among the 15 external interrupt positions on the computer's backplane (see Table 3-1 for pin assignments).

Cooling Requirements

The controller card is cooled by the forced air system of the computer. No further cooling is required. Refer to the computer Customer Engineering Manual (89633300) for further information concerning cooling capabilities of the computer.

Environmental Considerations

The environmental considerations necessary for shipping, operation, or storage of the controller are listed in the Environmental Specifications Table 1-3.

Preparation and Installation

To install the controller, perform the following with the computer power switched "off":

1. Refer to Figure 3-1 for selection of the location for the board in A/Q bus (slots 1, 2, 6 or 7).

2. Inspect the enclosure, card slot, printed-wiring board slides and connector pins for physical damage.

3. Place the internal select jumpers in the positions on the card as as will be described. Location of the internal select positions are shown in Figure 3-2.

CAUTION

Do not install or remove cables or controller cards in computer or expansion enclosure with power on.

4. Install controller internal cable on backplane at P2 in the position assigned to the controller card and the output connector at the output location provided. The card location will be selected from slots 1, 2, 6 or 7.

5. Install the external cable at the location provided for it on the back of the computer enclosure and connect it to the Modem.

6. Carefully install the controller card in the assigned card slot. The card must slide in smoothly.

7. Install interrupt cable between P1B24 of the chosen A/Q slot and the correct interrupt position in the CPU (see Table 3-1).

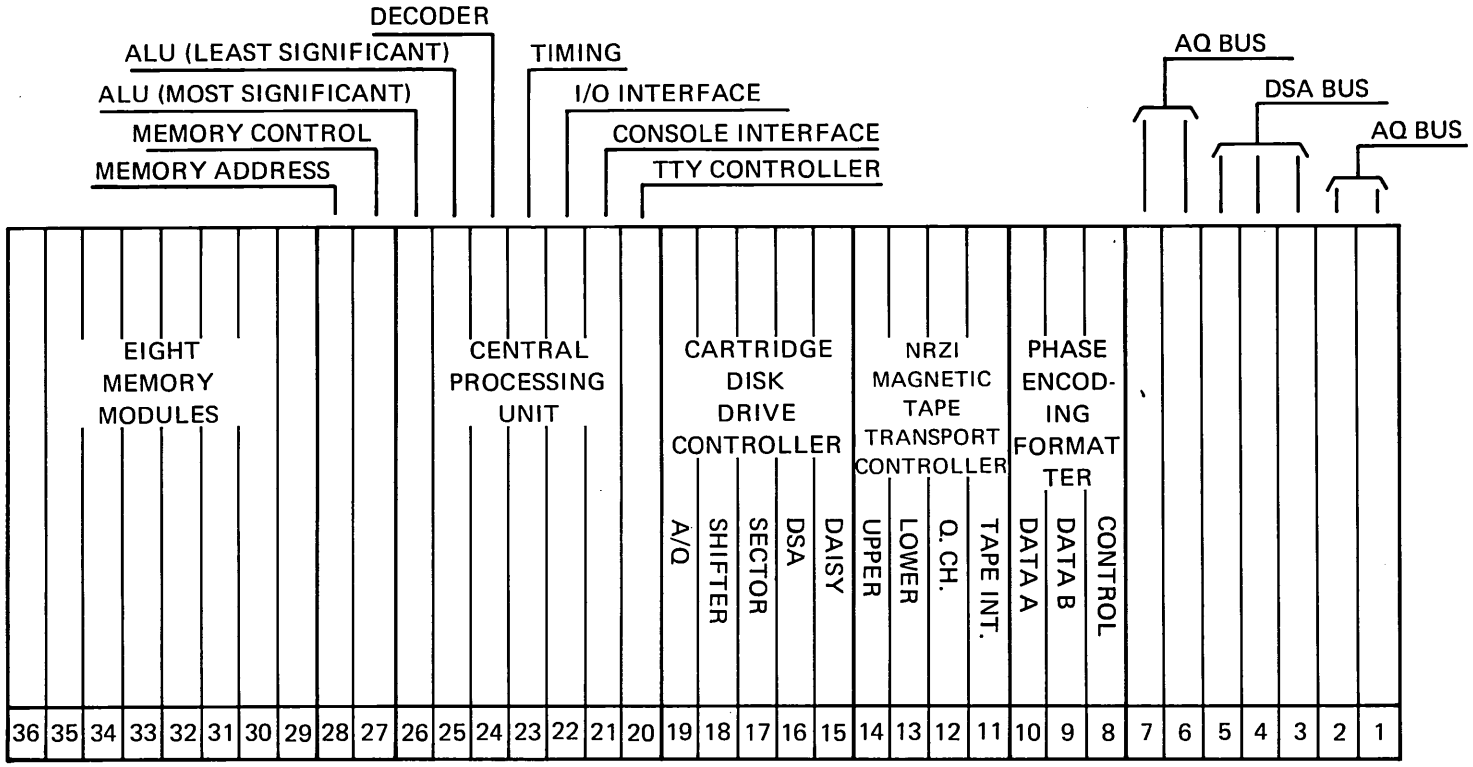


Figure 3-1. Location For Installation Of Cluster Multiplexer Local Controller (A/Q Bus)

TABLE 3-1. INTERRUPT PIN ASSIGNMENTS

Cluster Multiplexer Local Controller

Real Time Clock Interrupt	P1B24

Connections may be made to any of the following:

CPU	(Position)	
Line 1	25	P1B10
" 2	25	P1A7
" 3	25	P1B7
" 4	25	P1A5
" 5	25	P1A6
" 6	25	P1B6
" 7	25	P1B5
" 8	26	P1A10
" 9	26	P1B10
" 10	26	P1A7
" 11	26	P1B7
" 12	26	P1A5
" 13	26	P1A6
" 14	26	P1B6
" 15	26	P1B5

Jumper Selection of Programmed Parameters (refer to Figure 3-2)

Equipment Number

The Equipment Number of the CMLC is jumper-selected to any of the 16 combinations of bits Q7, Q8, Q9 and Q10.

The jumpers fixing the Equipment Number are placed on both sides of U81. A jumper should be inserted for each Q bit required to be a "1".

Extended Equipment Number

When two local controllers are used with the same Equipment Number (the maximum number of terminals multiplexed for this configuration can be three or four only), the value of Q6 determines which CMLC is addressed.

The jumpers associated with this feature are Q6, between U82 and U83, and two jumpers marked TOS1 and TOS2, between U14 and U15. When the feature is not used, no jumpers are inserted in TOS1 and TOS2 and jumper Q6 has no significance. When the Extended Equipment Number is required, jumpers are inserted for both TOS1 and TOS2. Selection of the CMLC is by Q6 = 0 if no jumper is inserted in jumper position Q6; Q6 = 1 when a jumper is inserted in Q6.

Protect

The CMLC is considered a protected device if no jumper is inserted and an unprotected device if a jumper is inserted. The protect jumper location is between U22 and U6.

Clock Interrupt Period

The clock interrupt period is reached by dividing the Modem baud rate by two dividers whose division ratio is jumper programmed. The combined division ratio is the product of the two dividers' ratios. The first divider divides either by 16, 8 or 4, the second divider by 3 or 6. (The jumper location replaces U53).

The top two jumpers determine the second dividing ratio - one jumper should be inserted either in the location marked 1:3 or in the one marked 1:6.

The bottom three jumpers determine the first dividing ratio - one jumper should be inserted in one of the three locations marked 1:4, 1:8, and 1:16 according to the desired division ratio.

Maximum Number of Terminals Multiplexed

This parameter can be set to either 3, 4, 6, or 8. The setting determines the number of character slots in the data block format transmitted and received. By setting this number to the lowest possible figure equal to or greater than the actual number of terminals in the cluster, the data transfer rate is optimized.

The 10 jumpers fixing this parameter are located between U41 and U43. The five jumpers on the left determine the receive circuit parameters, the five on the right determine the transmit circuit parameters.

Both settings must be the same and equal to the setting in the FC701-A/B with which the FC602-A is supposed to operate. Table 3-2 indicates the settings for each required parameter.

TABLE 3-2. TERMINAL MULTIPLEXING

Max. No. of Terminals Multiplexed \ Jumper Markings	5 Left Jumpers					5 Right Jumpers				
	A	C	D	B	unmarked	unmarked	B	D	C	A
3	X			X			X			X
4		X			X	X			X	
6		X		X			X		X	
8			X		X	X		X		

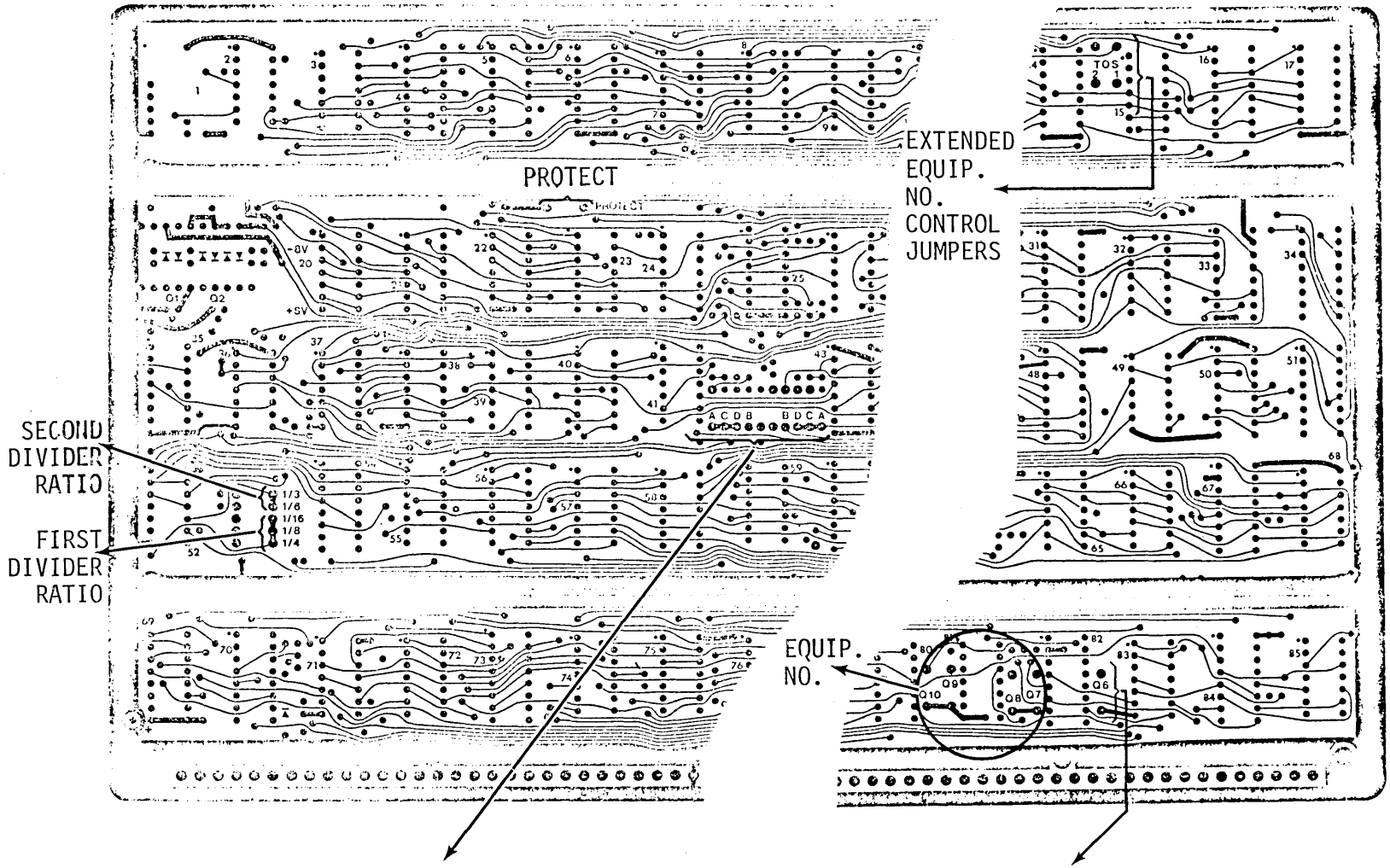


Figure 3-2. Jumper Selections

CHECKOUT

1. Refer to Section 2 of this manual and the CPU/Computer Reference Manual for operation of the controller.

2. Determine that the proper voltages are applied to the controller card by measuring +5 vdc between test points 1 (ground) and 63 on the PWA.

3. Perform diagnostic check with the Modem in loop-back test mode.

SECTION 4

THEORY OF OPERATION

Theory of Operation

Data Format

Characters and synchronization bits are interleaved according to the following format:

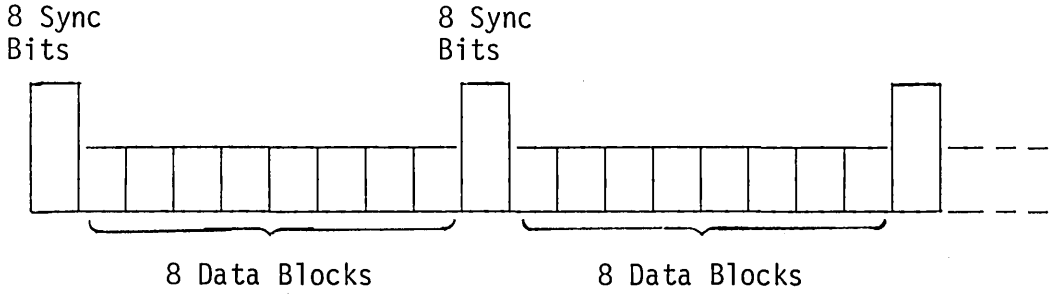


Figure 4-1. Data Format

The eight bits comprising a sync character are arranged in the following pattern:

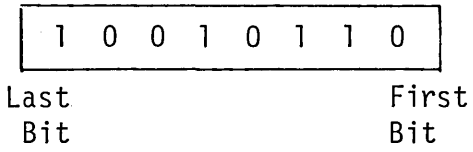


Figure 4-2. Sync Pattern

Each data block consists of a set of characters multiplexed to as many as eight terminals. The data character is made up of seven data bits and one even parity bit. The illustration below shows the format of the data blocks:

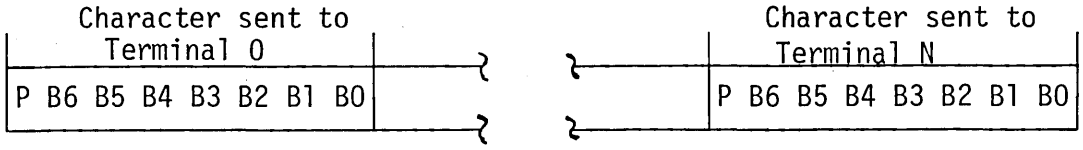
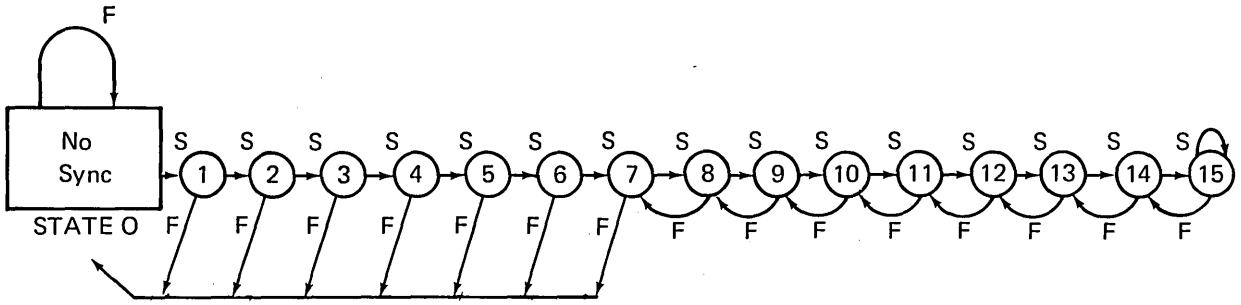


Figure 4-3. Data Block Pattern

B = bit
P = parity
N = 3, 4, 6, 8 (jumper selected)
(N is the maximum number of terminals which can be multiplexed.)

Synchronization

The following state diagram describes the method used to maintain synchronization.



S = Sync character received correctly in the calculated time slot

F = Sync character received incorrectly in the calculated time slot

Initially, the CMLC is out of synchronization with the sync logic in state "0". As bits are received, the sync logic checks the last eight bits for a match against the sync pattern (see Figure 4-2). If a match occurs, block counting starts and the sync logic shifts to state 1. In each of the states, from 1 through 15, the sync logic searches for the sync pattern, but at only the expected time of appearance, as specified by the character and block counting.

The sync logic shifts to the next higher state for every correct match.

In states 0-7, the CMLC is not considered in sync. If a mismatch occurs in any of these states, the sync logic will return to state 0.

In states 8-15, the CMLC is considered synchronized allowing the data received to enter the receive buffers. Failure to detect a sync pattern in the expected time slots during states 8-15 does not cause the sync logic to revert to state 0, but only to the next lower state.

Data Buffering

Two pairs of character data buffers and two status registers are associated with each of the eight possible terminals multiplexed by the CMLC. One pair of data buffers allows double buffering of the output data from the computer before the data is transmitted serially to the line.

The second pair of data buffers allows double character buffering of the serial data received from the line before the computer reads the data.

A 4-bit status register is associated with each pair of transmit buffers. The contents of the transmit status register specifies one of six possible states in which the terminal buffers may exist. The pair of data buffers, identified as "A" and "B", are loaded when the computer performs an output instruction and emptied by the CMLC Transmit Logic.

The 6 possible states of the terminal buffer are:

1) A and B empty; next data to be loaded in A
2) A loaded, B empty; next data to be loaded in B
3) B loaded, A empty; next data to be loaded in A
4) A and B loaded; initial data to be emptied from A and no loading allowed
5) B and A loaded; initial data to be emptied from B and no loading allowed
6) A and B empty; next data to be loaded in B

NOTE

States 1 and 6 are redundant to simplify the logic.

An identical set of status registers is associated with each set of receive buffers. The receive buffers are loaded by the CMLC logic from the serially-received data emptied by the computer's input instruction.

Data Transfer Operations

Six types of data transfer are handled to and from the Cluster Multiplexer Local Controller:

1) status of CMLC
2) function to CMLC
3) data from computer to CMLC destined for terminals (line)
4) data from CMLC to computer received from terminals (line)
5) data from CMLC to line
6) data from line to CMLC

The following description pertains to the CMLC block diagram for each of the six types of data transfer mentioned above. When the computer performs an input instruction from the CMLC (director bit Q00 = 1), the CMLC is directed to transfer its status to the computer.

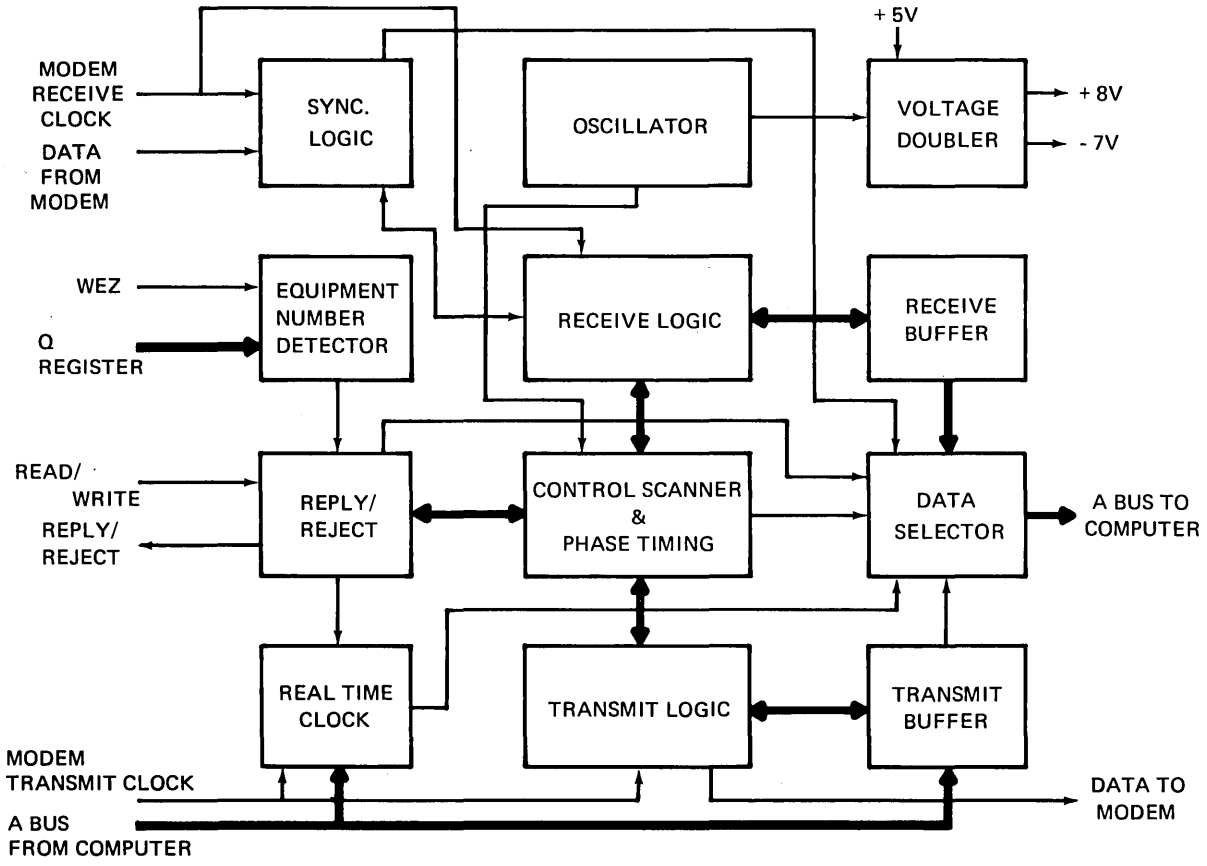


Figure 4-4. System Block Diagram

Status of CMLC

The Equipment Number Detector checks if the Q Register contains a valid address. Under the control of the Reply/Reject Logic, the state of the Real Time Clock and protect switch is transferred through the Data Selector to the computer's A bus.

Function to CMLC

When the computer performs an output instruction to the CMLC (Director bit Q00 = 1), the function command is transferred to the CMLC. The Equipment Number Detector checks if the Q Register contains a valid address. If a protect violation is detected by the Reply/Reject Logic, a "reject" is returned to the computer. If no protect violation occurs, the Reply/Reject Logic responds with a "reply" and applies the contents of the A Register bits A00 - A02 to the Real Time Clock.

Data from Computer to CMLC

The computer outputs an instruction (Director bit Q00 = 0) directing the CMLC to transfer a data character from the A Register to the remote terminal addressed by the contents of Q-Register bits Q04, Q05, and Q06. The Equipment Number Detector checks if the Q Register contains a valid address. If a protect violation occurs, the Reply/Reject Logic responds with a reject. If no protect violation occurs, the Reply/Reject Logic requests the Control Scanner and Phase Timing for access to the Transmit Buffer and Logic.

According to the timing generated by the Scanner, the Transmit Logic checks the state of the addressed terminal data buffers. If the buffers are full, a reject is generated, resulting in no data transfer.

If a buffer is available, data bits A00 - A06 are accepted and stored in the Transmit Buffer under the control of the Reply/Reject Logic. The contents of the Control Status Register (part of the Transmit Buffer) for the addressed channel is modified by the Transmit Logic to indicate that a new character is ready to be transmitted to the line. After the data transfer is completed, the CMLC responds with a reply.

Data from CMLC to Computer

The computer performs an input instruction from the CMLC (Director bit Q00 = 0) to READ the status and data of the channel addressed by Q04, Q05, and Q06 into the A Register. The Equipment Number Detector checks if the Q Register contains a valid address. If a protect violation occurs, the Reply/Reject Logic responds with a reject. If no protect violation occurs, the Reply/Reject Logic requests the Scanner for access to the Transmit/Receive Buffers and Logic.

According to the timing generated by the Scanner, the Receive Status Register (part of the Receive Logic) is checked. If a character from the remote terminal is waiting in the data buffers of the addressed channel, the character is sent by the Receive Logic to the Data Selector and then to the A bus with a status bit indicating the presence of the character and the parity's validity.

The contents of the Receive Status Register is modified by the Receive Logic to indicate that the received character has been read by the computer.

Three additional status bits are transferred to the A Register during this input operation:

1) One bit, read from the Transmit Status Register of the channels, indicates if a buffer is available for data transmission.

2) Another bit identifies the state of synchronization.

3) The remaining bit indicates Modem Readiness.

After the data and status bits have been sent to the A bus via the Data Selector, the Reply/Reject Logic generates a reply to the computer's READ signal.

Data from CMLC to Line

The Transmit Logic contains bit, character and block counters which control the sequence of the data format by dividing the transmit time element (clock) received from the Modem.

After the transmission of eight bits associated with a specific terminal is completed, the Transmit Logic requests access to the Transmit Buffer from the Control Scanner and Phase Timing (CSPT). Under the CSPT's control, the Transmit Status Register (part of the Transmit Buffer) of the next terminal for which a time slot will be transmitted is checked. If the register indicates a character is waiting to be transmitted, the character is transferred from the Transmit Buffer to the Transmit Shift Register (part of the Transmit Logic). The Transmit Logic modifies the contents of the Transmit Status Register to indicate the character has been transmitted.

If no character is waiting to be transmitted by the Transmit Status Register, an IDLE (all zero) character is loaded for transmission. When the block counter of the Transmit Logic shows that eight data blocks have been completed, the Transmit Logic sends the periodic sync. character to the line.

Data from Line to CMLC

The SYNC Logic synchronizes the bit, character and block counters of the Receive Logic according to the periodic sync character received.

After the bit counter (part of the Receive Logic) indicates that eight bits have been received, the Receive Logic requests access to the Receive Buffer from the CSPT.

Under the CSPT's control, the Receive Logic checks if the received character is an idle (all zero) character, for which no operation is performed.

If an actual character is received, the Receive Logic sends the character to the data buffer associated with the terminal whose character slot was last received. The Receive Logic modifies the contents of the Receive Status Register associated with the terminal to indicate a character is waiting to be read by the computer.

SECTION 5

LOGIC DIAGRAMS

KEY TO LOGIC SYMBOLS

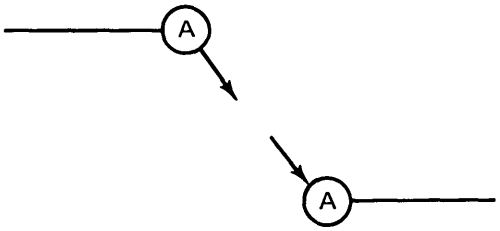
Publication 89723700 (Key to Logic Symbols) or equivalent, lists the symbols used in the logic diagrams in this manual and gives a short description of the functions they represent. The symbols conform generally to Control Data usage (Microcircuit Handbook, publication number 15006100), using the polarity logic convention.

The following paragraphs describe the signal flow conventions used.

SIGNAL FLOW

Input signals are drawn coming from the left or above; output signals are drawn going to the right or down.

The signal lines are sometimes interrupted to allow logical grouping of components. At each such interruption one of the following indicators is used:

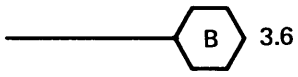


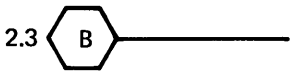
On-Sheet Continuation Reference Symbols

These symbols when used with the logic symbols in the following diagrams indicate that a connection exists between two points on a sheet. The arrows attached to each circle point from signal origin to signal destination. The letters, C, II, I, O and P are not used inside the circles, since they bear special significance on logic diagrams.

Off - Sheet Continuation Reference Symbols

(ON SHEET 2)

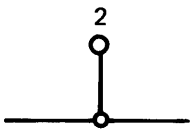




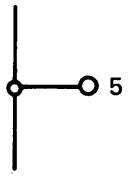
(ON SHEET 6)

These symbols when used with the logic symbols in the following diagrams indicate that a common signal point exists between two sheets in a series of related drawings. These symbols point from output to direction of input as shown in the illustration. The letters C, H, I, O and P are not used in the hexagons, since they bear special significance on logic diagrams. The number(s) next to each hexagon indicate the sheet(s) that the signal is continued from or on. For instance, the numbers 3.6 refer to sheets 3 and 6, while 2.3 refers to sheets 2 and 3. It should be noted that the referenced sheet number(s) is always placed opposite the line extending from the hexagon.

Test Points

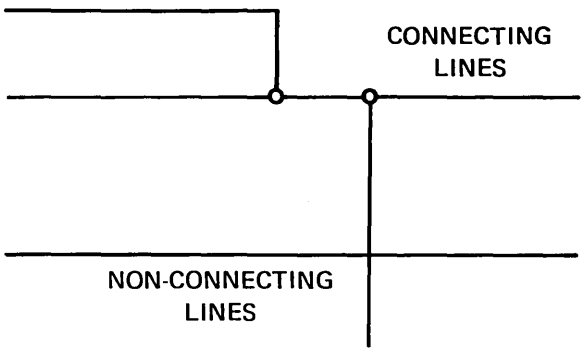


OR



The test point symbol on the logic diagram shows the connection of a test point on the printed wiring board (PWB). The number adjacent to the symbol refers to the test point position on the PWB at the edge opposite the connectors. Only test point one is labeled on the edge of the PWB.

Connecting and Non-Connecting Lines

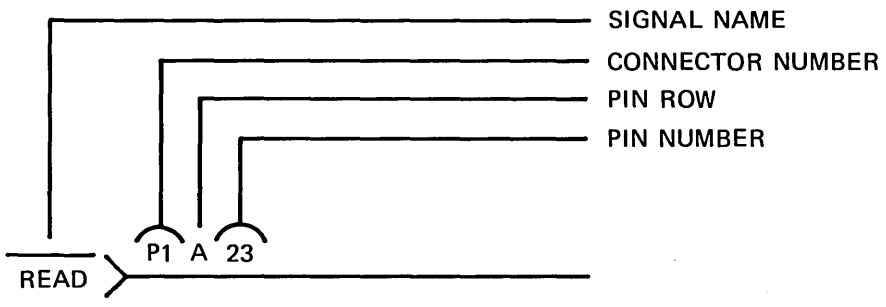


Lines connected to a common point or at a junction point are shown in the upper part of this illustration. No more than four lines are connected to a common point in the diagrams.

Lines crossing but not connected are shown in the lower part of this illustration.

Connectors

Connectors are represented on the logic diagram by the symbol for a female connector, for both input and output signals. The name of the signal is placed in the open end of the connector symbol (shown below), using the full name of the signal or the common abbreviation applicable to logic diagrams. The connector number, pin row and pin number are located above the line extending from the connector symbol.



OSCILLATOR (Drawing number 89926700, sheet 2)

The crystal-controlled oscillator generates a 7.04-Megahertz frequency which is fed through pins 1 and 2 of the inverter U55 to the counter U35. The counter divides the 7.04-MHz frequency by 16 and the resulting frequencies are used by various parts of the controller for timing and control functions. In addition, a 440-kilohertz frequency is supplied to output pin P2A22 so that the frequency can be used for self-testing the controller.

VOLTAGE DOUBLER (Drawing number 89926700, sheet 2)

The voltage doubler converts the V_{CC} supply of +5 volts into +8 volts and -7 volts, which are distributed to the line drivers that interface with the type RS-232-C Modem circuits.

Diodes D1, D2 and capacitors C12 and C16 form a positive voltage doubler with an output of +8 volts. The negative voltage doubler consists of one voltage doubler (C18, D3, D4 and C13) in series with a second one (C19, D5, D6 and C14) with a -7-volt output.

The collectors of transistors Q1 and Q2 are the drivers for the doubler. The waveform by the drivers is composed of four parts, each one corresponding to one of the four binary states at output pins 6 and 7 of the counter U35, which regulates the on and off states of Q1 and Q2. The four states are:

1) Q1 saturated, Q2 cutoff - voltage approximately 0.2V;
2) Q1 and Q2 cutoff;
3) Q2 saturated, Q1 cutoff - voltage approximately 4.8V;
4) Q1 and Q2 cutoff.

CONTROL SCANNER AND PHASE TIMING (Drawing number 89926700, sheet 2)

The Control Scanner and Phase Timing (CSPT) assures access requests to the buffers are acknowledged sequentially. Four types of requests can occur: 1) a WRITE operation by the computer seeking to load data to the buffers for transmission, 2) a READ operation by the computer seeking to read data and status information from the buffers, 3) a Transmit Logic request associated with the transfer of data from the Transmit Buffers to the line, and 4) a RECEIVE Logic request associated with the transfer of data from the line to the Receive Buffers. Each of these requests enters one of the following four gates: 1) U72-11, 12, 13 accepts Receive Logic requests, 2) U72-8, 9, 10 Transmit Logic requests, 3) U23-8, 9, 10, 11 computer READ and 4) U23-3, 4, 5, 6 computer WRITE.

The scanner section consists of a shift register U73 connected so as to switch through five states: 0000 (initial state), 1000, 0100, 0010, 0001. The initial state 0000 produces a high at the output of the four wired-or inverters U71-4, 8, 10, 12. On the next clock pulse U73 shifts to state 1000 after which the serial input to the scanner is 0.

Assume the shift register has reached the fifth state (0001), which enables the scanner to check the signal RCARQ. A "1" will produce a low output on pin 11 of gate U72. The output of NAND gate U40-6 switches to high. If U40's output switches to high during the first half of the clock pulse entering flip-flop U39-12, the flip-flop switches to low on pin 8 causing the operation of the scanner's shift register to switch into Parallel Load and freeze.

When output pin 9 of flip-flop U39 switches to high, the master reset of the Phase Timing shift register U11 releases. The shift register proceeds through the following five states, which result from its stage interconnections: 1) 0000, 2) 0001, 3) 1000, 4) 0101, and 5) 0010. The first three transitions in the state diagram are parallel load while the fourth is a shift operation. These timing phases are fed to other sections of the

controller. The cycle of an access request ends when the appropriate timing phases cause the acknowledged request to return to "0". At this point, U40's output switches to low. U37's output switches to high and therefore both inputs to U72-1, 2 are high. Consequently, U72's output switches to low, resetting the scanner.

When the scanner returns to state 0000, the wired-ors (U71) detect the change and through U37 reset U39. When the flip-flop resets, the Phase Timing shift register resets as well. The next clock pulse resumes scanner operation.

Output pin 10 of U22 switches high whenever a computer WRITE or READ request has been acknowledged. If the timing phase reaches 0010, the phase timer clock is inhibited (U64-12), freezing the timing phase and allowing other logic elements of the controller to send the computer a REPLY. To answer with a REJECT, an earlier time phase is used by different logic on sheet 3 whose output (reference AY) freezes the phase timer through U64-1.

EQUIPMENT NUMBER DETECTOR (Drawing number 89926700, sheet 3)

The four program jumpers on Q7, Q8, Q9 and Q10 form an input to the four exclusive-or gates U81. If the Q register bits Q07 - Q10 contain the correct equipment code for the CMLC according to the designated jumpers on the controller board, the output of gates U81 will be a "1".

U81's output is fed through the two AND gates of U64, whose output pin 8 switches high if all the conditions are met and signal $\overline{\text{WEZ}}$ is present on pin P1A20. The extended equipment number mode requires jumpers in positions TOS1 and TOS2. U15 compares the state of bit Q06 arriving on P1A15 through buffer gate U32 with the desired jumper-selected designation of Q6. When this mode is used, U77 ANDs the result of Q6's comparison with the check of Q7 - Q10 and $\overline{\text{WEZ}}$. The remaining gates of U32 act as a buffer for the channel address bits Q04, Q05, and Q06 which are sent to the Transmit and Receive Logic. In the extended equipment number operation mode, BQ6 (U32-6) is forced to "0".

DATA SELECTOR (Drawing number 89926700, sheet 3)

Controlled by signals from the Reply/Reject logic, gates U36, U52, U66, U63 and U83 open and close to allow data from various logical parts of the CMLC to be transferred to the computer A bus.

The presence of OPEND (reference AM, sheet 5), on a READ instruction from the computer and Q00 = 0, opens gates U66 and U83, which allow the seven data bits A00 - A06 to pass. In addition to transferring a data character, the Data Selector transfers the following status bits: A08 (Modem Alarm), A09 (Not Synchronized), A10 (controller ready to receive a character for transmission on the addressed channel), A11 (valid received data character is present in bits A00 - A06) and A15 (parity error detected when character in bits A00 - A06 was received).

The Data Selector also transfers status information on the protect switch and the Real Time Clock during a READ instruction when Q00 = 1. These bits are sent through U63-1, 2, 3 and U36-1, 2, 3, which are opened by the Reply/Reject logic via gate U78-6.

REAL TIME CLOCK (Drawing number 89926700, sheet 3)

The Real Time Clock (RTC) logic supplies the computer with a periodic time element that can either be sent to an interrupt line or can be sensed when the computer performs an input instruction with Q00 = 1. To generate the timing period, the CMLC uses the Transmit timing element from the Modem and divides it by the counters U69 and U70. Program jumpers are placed across the points labeled 1/16, 1/8 and 1/4 at the output of counter U70 and across 1/6 and 1/3 on U69's output to divide the Modem baud rates of 2400, 4800 or 9600 by 12, 24, 48 and 96.

The divided output of counter U69 enters the RTC flip-flop U62, which sets on a low-to-high transient from U69-7. If the Enable Interrupt FF (U62) is set, U63-6 will supply an interrupt to the computer on output pin P1B24. The computer checks the status of the RTC FF by reading the status bit A03 on output pin 3 of U63.

Both FFs, the RTC and the Enable Interrupt, are controlled by a computer output instruction using A register bits A00 - A02. (A02 sets the Enable Interrupt FF and overrides A00 and A01). A00 and A01 reset the RTC and Enable Interrupt FFs. The generation of bits A00 - A02 are enabled by signal EWFTC (from U78-8 of the Reply/Reject logic), which switches to high when the computer performs a legitimate WRITE instruction with Q00 = 1.

AND gates U65 serve as buffers to A register bits A00 - A02. A Master Clear from the computer resets FFs U62.

REPLY/REJECT LOGIC (associated with I/O and Q0 = 1) (Drawing number 89926700, sheet 3)

A computer WRITE operation, accompanied by the correct equipment number and Q00 = 1, switches U77-3 and U80-10 to high. U78-3 switches high, and if no protect violation occurs from U61-6, U78-8 switches high. The high of U78-8 is sent to the Real Time Clock logic as EWFTC (as explained earlier) and through the series of gates U37-1, 2, U23-1,12 and U36-4,5,6. U36-6 forwards a REPLY to the computer.

A protect violation occurs when the protect jumper is not inserted. P1A23 ($\overline{\text{Prog Protect}}$) is high and U61-6 low, inhibiting gate U78-9,10,8. The low output on pin 8 of U78 inhibits the RTC logic and prevents a REPLY from being generated. The protect violation is transmitted through U76-6 and ANDed at U61-12,13 to generate a low output on U61-11. This low is fed back through NAND gate U61 and inverter U44 resulting in the REJECT signal.

A READ operation by the computer results in a high on U80-4, which switches U78-6 to high (no protect violation is checked during a READ operation). The high on U78-6 opens the Data Selectors and is transmitted through gates U37-3,4, U23-12 and U36-6, generating a REPLY that ends the cycle.

MODEM INTERFACE CIRCUITS (Drawing number 8992670O, sheet 3; Data Line Driver explained elsewhere)

U74 converts the RS-232-C levels of the Modem to the TTL levels. A similar function is performed by transistor Q7 and its associated components.

Inputs DD and DB are clock inputs from the Modem that are filtered by FFs U76 and U59 and their associated capacitors. The filters prevent noise of up to approximately 2 microseconds in duration from passing to the logic on the CMLC.

CA and CD, tied to +8 volts through R20 and R21, are fixed control signals transmitted to the Modem. CB coming from the Modem is terminated by resistors to ground.

MISCELLANEOUS

The signal SYND (reference AQ, sheet 5), which indicates if the CMLC's receiving circuits are synchronized, is inverted by U71 and passed on to the Data Selectors.

During a READ instruction from the computer with QOO = 0, at time phase A and no data received, signal $\overline{\text{KCVSB}}$ becomes a high. U24-3 switches to low, U23-12 high, and U36-6 low, causing a REPLY to be sent to the computer from P1A22. Similarly, on a READ or WRITE with QOO = 0, if the time phase reaches C, signal $\overline{\text{CPCRP}}$ switches to high, thus transmitting a REPLY on P1A22.

The flip-flop U39 is used by the Transmit Logic to control the loading of the data buffers. U39 is set at Phase A if the Transmit Logic is able to receive another character from the computer. The output of U39 is fed to gate U36-12 of the Data Selectors, where the signal is read as status bit A10 when the computer performs a READ operation with QOO = 0.

TRANSMIT LOGIC (Drawing number 89926700, sheet 4)

The Transmit Bit Counter U60 counts the bits in each character from the filtered Modem clock FMKTX (reference AZ, sheet 3). On completing one character count (8 bits), U60-7 switches to high and triggers the Transmit Character Counter U43. The Character Counter holds the number of the time slot of the terminal to which data is being transmitted and advances after every 8-bit count by the Bit Counter. U60's output, TXARQ (reference BC), is delivered to the Control Scanner and Phase Timing logic on sheet 2 requesting the Scanner to allow access to the Transmit buffers. When access has been acknowledged, the Transmit Logic will perform a data transfer from the buffers to the transmit shift register, depending on the information contained in the Status Register associated with the terminal number as it appears in the character counter. The Bit Counter resets after the data transfer. The Character Counter advances through an entire data block count as determined by the number of terminals multiplexed. The maximum number of terminals is fixed by inserting program jumpers at A, B, C, and D in the feedback path between U43's output and parallel load input.

The Block Counter U10 serves a double purpose: 1) as a block counter when transmitting data and 2) as a sync bit counter when transmitting the 8 bits of the sync pattern. U10-6 switches from "1" to "0" after a count of 8 data blocks, driving U26-2 high, which triggers the clock input of Transmit Data Sync FF U9. U9-6 switches to high enabling U27-9,10,8, while disabling U27-1,2,3. This action changes the mode of U10 to counting 8 sync bits. During the sync mode, U9's output freezes the state of the Bit and Character Counter from advancing on inputs from the Modem's clock.

U41's logic is connected to generate the proper sequence of sync bits on output U41-6. Gates U24-4,5,6 and 9,10,8 — enabled or inhibited by FF U9 — determine whether the data transmitted to the line are the sync bits from U41 or the data bits from the shift register U13. From U24 the data passes through the Modem Data Line Driver, comprising transistors Q3, Q4, Q5, Q6 and associated components.

The Transmit Shift Register is composed of U13 and U30. U30's serial input is connected to ground (pins 2 and 3) so that if no new data is loaded into the parallel input after a character is shifted out, the register's next output transmitted to the line will be an all-zero character. U47 generates an even parity bit which is loaded as the most significant bit to U30-4.

The Data Buffers consist of two random access memory devices U48 and U82, each storing 16 four-bit words. Connected together, U48 and U82 store 16 eight-bit words. Under the double buffering scheme employed, the first eight words of memory belong to Buffer A and the second group of eight words to Buffer B. Four address bits from U46 determine which terminal buffer is being addressed. If, for example, the address is 0111, Buffer A associated with terminal 8 is addressed.

Data transmission from and to the buffers is controlled according to the state diagram in Figure 5-1. The 4-bit status word whose bits are labeled W, X, Y, Z, are stored in the random access memory U31 and describe the state of each buffer set as follows:

1) W = 0, computer allowed to load; W = 1, computer not allowed to load.

2) X = 0, computer should load into Buffer A; X = 1, load into Buffer B.

3) Y = 0, data in buffer; Y = 1, buffer empty.

4) Z = 0, take data from Buffer A and transmit to the line; Z = 1, take data from Buffer B.

When these definitions are applied to determine the status word of each buffer set, a six-state diagram is derived. The state designations and meanings are:

1) 0010 : Buffers A and B empty; computer should load to Buffer A

2) 0100 : A full, B empty; computer should load to B

3) 0111 : A and B empty; load to B

4) 0001 : A empty, B full; load to A

5) 1000 : A full, B full; remove first character from A, do not load

6) 1101 : A full, B full; remove first character from B, do not load.

If the computer attempts to load into a buffer when both buffers are full, a REJECT will be generated. The arrows in the state diagram indicate how data can be loaded and discharged from the buffers in each of the six states. For example, "A" means a load operation into Buffer A and "b" indicates a discharge operation from Buffer B to the line.

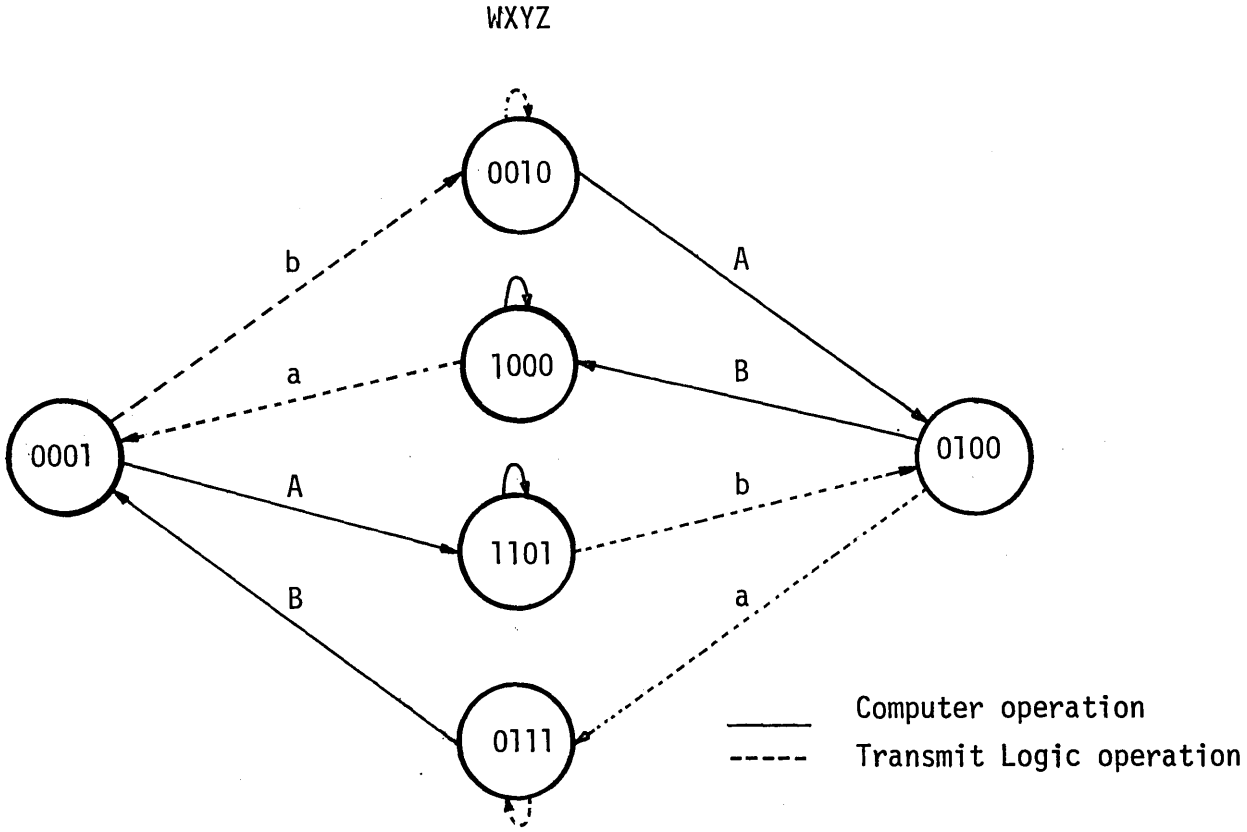


Figure 5-1. Double Buffer State Diagram - Transmit Logic

Two sets of functions are derived from the status bits to indicate the next status word: 1) when the computer performs a WRITE operation and 2) when the Transmit Logic sends data from the buffers to the line. The logic functions are represented in Table 5-1 with their explanation.

TABLE 5-1. GENERATION OF NEXT STATUS WORD

NEXT STATUS BIT	NEXT STATUS BIT WHEN TRANSMIT LOGIC OPERATION-BUFFER TO LINE	NEXT STATUS BIT WHEN COMPUTER WRITE TO CHANNEL	NOTES	
			TRANSMIT LOGIC	COMPUTER WRITE
W_N	0	$\overline{Y}_p$	At least one buffer must be empty hence next W = 0	Depends on the last state of the buffers
X_N	X_p	$\overline{X}_p$	No change	Next load is to the buffer not currently being loaded
Y_N	$\overline{W}_p$	0	If computer was allowed to load, a transmit operation now empties at least one buffer	Data must be in buffer after a computer WRITE operation
Z_N	$F_{(p)}$ $F=\overline{Y}_p \cdot \overline{Z}_p + \overline{W}_p \cdot X$	Z_p	F serves 2 purposes: 1) meets the logic conditions for the data transfer 2) insures that the logic will always converge to one of the six states in Figure 5-1 when power is turned on	No change
p = present N = next				

The change of the status word is inhibited when the computer performs a WRITE operation, which is responded to with a REJECT, because both buffers are full. The inhibit allows the functions for a computer WRITE operation to be implemented more easily.

Multiplexer U12 generates the next status word by the selection of the appropriate set of functions in Table 5-1 for a computer WRITE or a Transmit Logic operation. U12's output is loaded into U14, during phase A, prior to being loaded into the data inputs of the Status Register U31.

Due to the inversion properties of U31, the complement of W, X, Y and Z is present on output pins 11, 9, 7 and 5.

The address of the correct word in the buffer and status register is derived from the Q register bits Q04, Q05, and Q06 when the computer performs a WRITE operation, or the Character Counter when the controller performs a Transmit Logic operation. Signal CRQAP (reference K, sheet 2) indicates a computer operation has been performed and the Q register bits serve as the correct address.

Status Bit X (in the case of computer WRITE) and status bit Z (Transmit Logic operation) of the status word determine whether Buffer A or B is involved in the operation. These bits are used by the Address Multiplexer U46 and fed into the most significant bits of the Data Buffers U82 and U48.

SYNCHRONIZATION LOGIC (Drawing number 8992670O, sheet 5)

Sync Counter U4 contains the state of synchronization, as previously explained under the Theory of Operation in Section 4. When U4 equals 0, the Receive Logic is completely out of sync. Associated with the Sync Counter are two flip-flops, U38: one indicates the mode of operation - Sync or Data (a logic high on U38-5 indicates Data mode, a high on U38-6 indicates Sync mode), and a second FF which is set when the Sync Counter U4 equals 0 and is reset when U4 is advanced.

The Modem bits received from the line are checked for the correct sync pattern by U58 (checks the four 1's in the pattern) and U49 (checks the 0's). A correct pattern produces a low on U49-6. When FF U38-9 is high, indicating that U4 equals 0, the 1-microsecond (approx.) pulses generated by U5-10 for every receive clock timing element from the Modem is applied to U21-13. If the correct sync pattern is detected and FF U38-6 is low, the wired-OR connection U3-4,6 and U2-8 will respond with a positive pulse, advancing counter U4 through U21-8. Simultaneously, a reset is applied through U37 to the Sync Count Zero FF and a clock pulse is sent through U3-8 to the Sync-Data FF U38, switching the FF from Sync to Data mode. This activates the Bit, Character, and Block counters. After a count of eight data blocks, pin 6 of Block Counter U54 switches from high to low, triggering the End-of-Cycle One Shot U5. The One Shot fires a pulse of about 1.5 microseconds in duration following every completed cycle of data and sync bits. At the end of Data mode, the pulse from the One Shot is delivered to the Sync-Data FF, which now switches to Sync mode.

In Sync mode, the Block Counter U54, instead of counting data blocks, counts Modem bit pulses from the signal $\overline{\text{FMKCV}}$ (reference AV, sheet 3). At the end of eight bits, U54 triggers the One Shot. In order for the Sync Counter to advance to its next state and the Sync mode to switch back to the Data mode, three conditions must exist simultaneously:

1) a correct sync pattern (low on U49-6), 2) Sync-Data FF in Sync mode, and 3) an end-of-cycle pulse from the One Shot. A success produces a high on the wired-OR output U3-4,6 and U2-8, advancing the Sync Counter and switching the Sync-Data FF to the Data mode.

Each successful synchronization advances the Sync Counter until a count of 15 (all 1's). A further advance in the counter is blocked by the inhibit to U21-9. If an incorrect sync pattern has been received, U56-6 applies a countdown pulse to U4, causing the counter's state to decrease by one. If U4 is in state eight or higher, the mode will be switched back to Data through gate U20-4,5, and 6. If the sync state is lower than eight and an incorrect sync pattern occurs, a low appears on U3-10,12, which resets U4 to 0 and, through U37-10, sets U38-9 to indicate U4 is in the zero state.

RECEIVE LOGIC AND RECEIVE BUFFERS (Drawing number 8992670O, sheet 5)

Data received from the line enters the Receive Shift Registers U51 and U34. The Idle Character Detector U68 determines if an idle character has been received. U85 performs an even parity check and the resulting bit is stored in place of the eighth bit received in the data buffers (read by the computer on bit A15 with a "1" to represent an error). When Bit Counter U6 completes counting eight bits, pin 7 switches to high generating the request RCARQ (reference J, sheet 2) to the Control Scanner. Under the timing control of the Phase Timer, a data transfer occurs from the Shift Registers (seven bits plus a parity check bit result) to the Data Buffers U84 and U67. U84 and U67 are connected in the same way as the corresponding devices of the Transmit Logic (i.e. 16 words of eight bits each). The address associated with the character received from the line is determined by the Address Multiplexer U33, which accepts under control of CRQAP (reference K, sheet 2) either the Q register bits(for a computer operation) or the contents of the Character Counter U25.

The status of the buffers U84 and U67 is maintained by a state diagram similar to the one for the Transmit Logic (see Figure 5-1), which is derived from four control bits associated with each terminal buffer set. The four bits, labelled M, N, K, L, are stored in the Status Register U50. These bits mean:

M = 0 : a character can be loaded from the line;
M = 1 : both sides of the buffers are full

N = 0 : Receive Logic should load character into Buffer A;
N = 1: Receive Logic should load character into Buffer B

K = 0 : data in the buffers; K = 1: no data in the buffers

L = 0 : computer should Read from Buffer A:
L = 1: computer should Read from Buffer B

When these definitions are applied to determine the status word of each buffer set, a six-state diagram is derived. The state designations and meanings are:

1) 0010 : Buffers A and B empty; Receive Logic should load to Buffer A

2) 0100 : A full, B empty; computer should discharge from A; Receive Logic should load into Buffer B

3) 0111 : A and B empty; Receive Logic should load into Buffer B

4) 0001 : A empty, B full; computer should discharge from Buffer B; Receive Logic should load into Buffer A

5) 1000 : A full, B full; computer should first discharge the character in Buffer A; Receive Logic not allowed to load into the buffers

6) 1101 : A full, B full; computer should first discharge from Buffer B; Receive Logic not allowed to load into the buffers

Note: the four bits are labelled in the following order: M, N, K, L. Applying the six state designations above, a state diagram (see Figure 5-2) is generated similar to the state diagram for the Transmit Logic. The arrows in the state diagram indicate how data can be loaded and discharged from the buffers in each of the six states. For example, "A" means a load operation into Buffer A and "b" indicates a discharge operation from Buffer B to the computer.

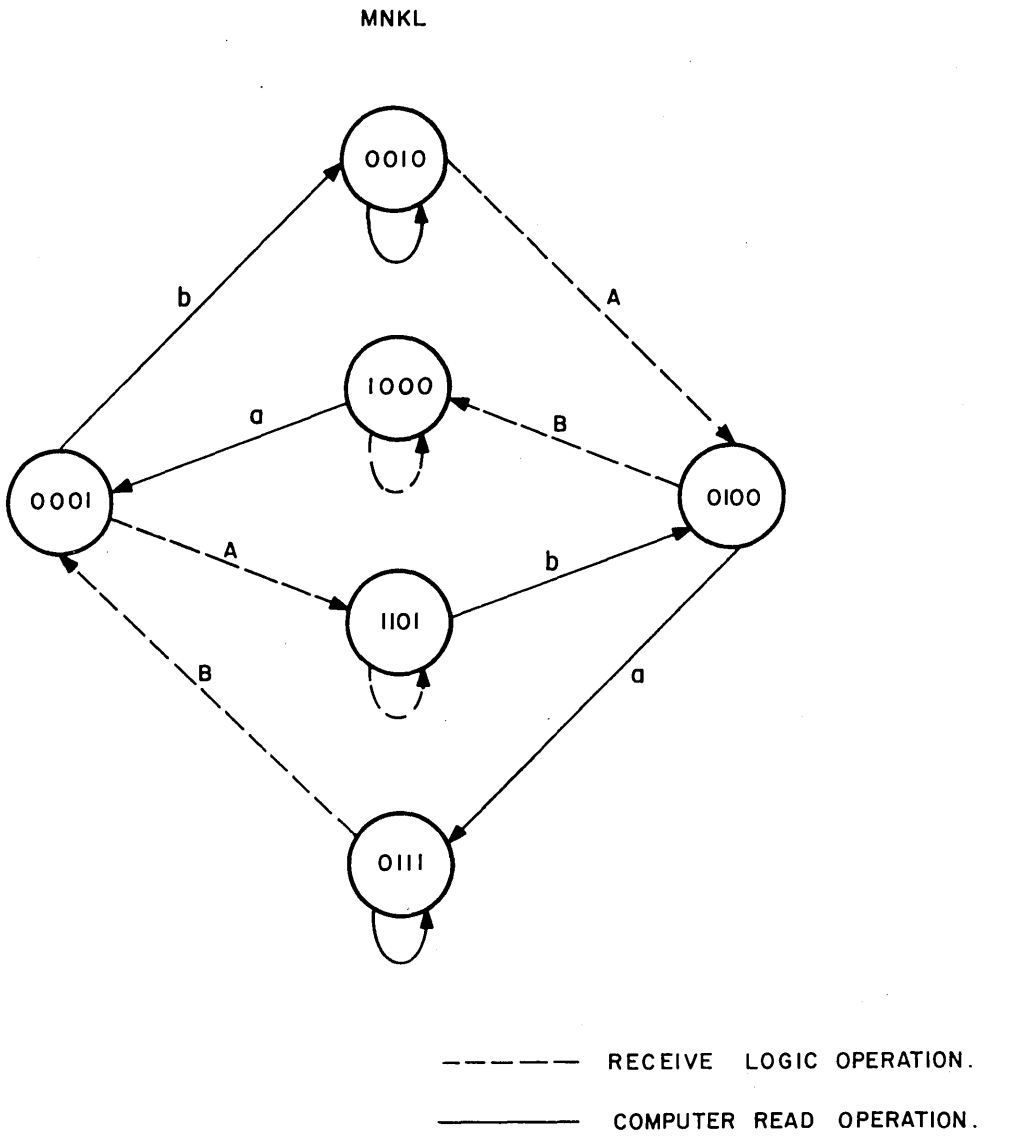


Figure 5-2. Double Buffer State Diagram - Receive Logic

Two sets of functions are derived from the status bits to indicate the next status word: 1) when the computer performs a READ operation and 2) when the Receive Logic receives data from the line and enters it into the buffers. The logic functions are represented in the following table:

TABLE 5-2. GENERATION OF NEXT STATUS WORD

NEXT STATUS BIT	NEXT STATUS BIT WHEN RECEIVE LOGIC OPERATION-LINE TO BUFFER	NEXT STATUS BIT WHEN COMPUTER READ
M_N	$\overline{K}_P$	0
N_N	$\overline{N}_P$	N_P
K_N	0	$\overline{M}_P$
L_N	L_P	$\overline{L}_P$

N = next

P = present

To simplify the functions in Table 5-2, when states 0010 and 0111 occur and a computer Read is performed, the status word will not be loaded into the status register, thus preventing the Next Status Word logic from generating a state which is not one of the six legitimate states derived in the state diagram of Figure 5-2. Similarly, when both buffers are full and a Receive Logic operation occurs, the functions in Table 5-2 will not be correct; but in this case as well, no loading occurs of the wrong outputs from the Next Status Word generating-logic into the Status Register. Hence, the previous correct status word is retained. With these exceptions just mentioned, Table 5-2 accurately depicts the correct transfer functions to one of the six legitimate states in the state diagram of Figure 5-2.

Logic consisting of U15, U8, and U22 is connected to status bits M, N, K, L. The output of U22-6 rises to a high level when the four status bits M, N, K, L fall within the six legitimate states, and is low otherwise. When U22-6 is low, the Receive Logic changes the next status word regardless of whether both buffers are full and/or an idle character has been received, thus assuring that the state diagram will always converge within three steps.

The next status word is generated according to Table 5-2 by directly connecting the output of the Status Register U50 to the Multiplexer U16 (or through Inverters U29-11,10 or U29-13,12). The next status word is temporarily stored by the Shift Register U17, operating in parallel mode, and then reloaded into the Status Register U50 under the control of the Scanner's timing.

Note that the outputs of status bits M, N, K, L are used in true phase opposite to the W, X, Y, Z status bits associated with the Transmit Logic.

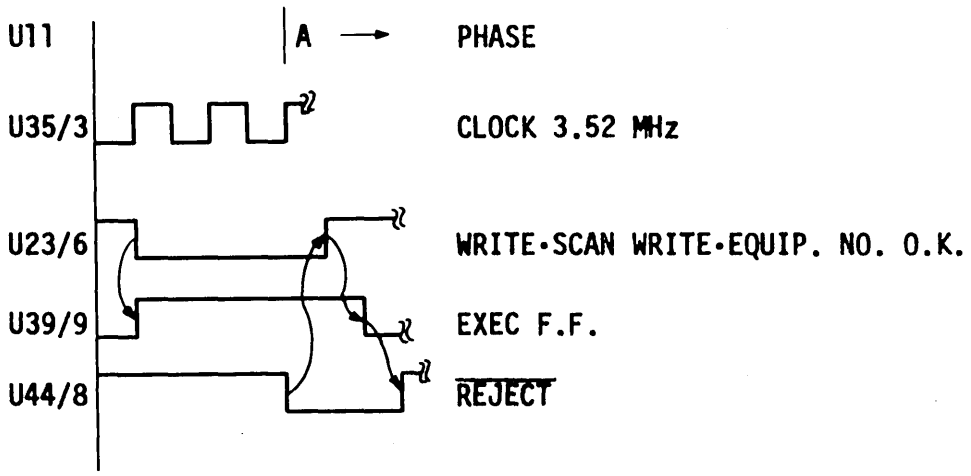
Timing Diagrams (A through I)

Following are a set of timing diagrams which show the significant waveforms during some of the data transfer operations.

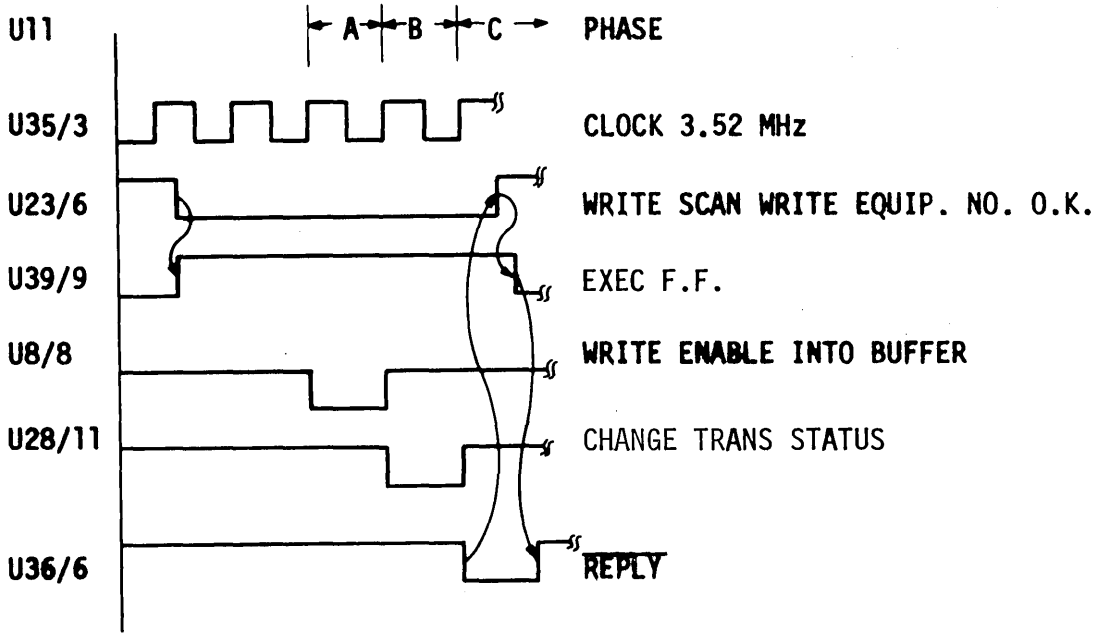
The timing shown is referenced to the phase timing shift register U11.

If scoping techniques are used to observe such waveforms, the fact that the various sources of data transfer (Computer WRITE, Computer READ, Receive Logic, Transmit Logic) interleave in an asynchronous way should be taken into account.

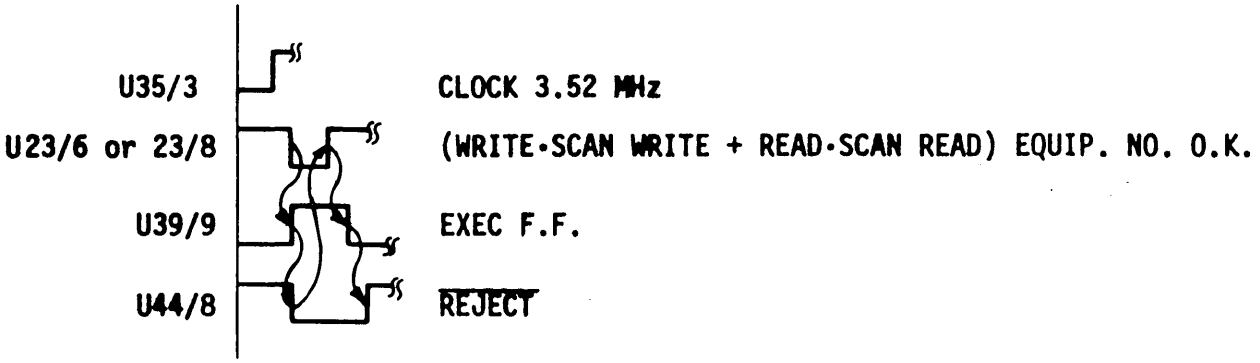
(A) COMPUTER PERFORMS WRITE TO CHANNEL: Q00=0, BUFFERS FULL, NO PROTECT VIOLATION.



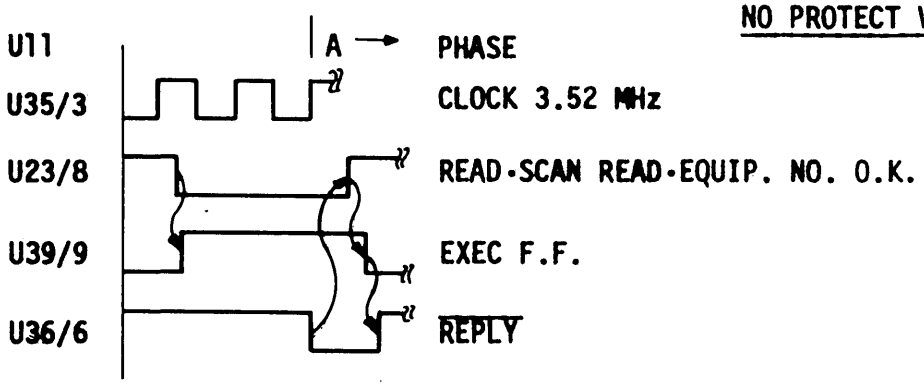
(B) COMPUTER PERFORMS WRITE TO CHANNEL: Q00=0, BUFFER AVAILABLE, NO PROTECT VIOLATION



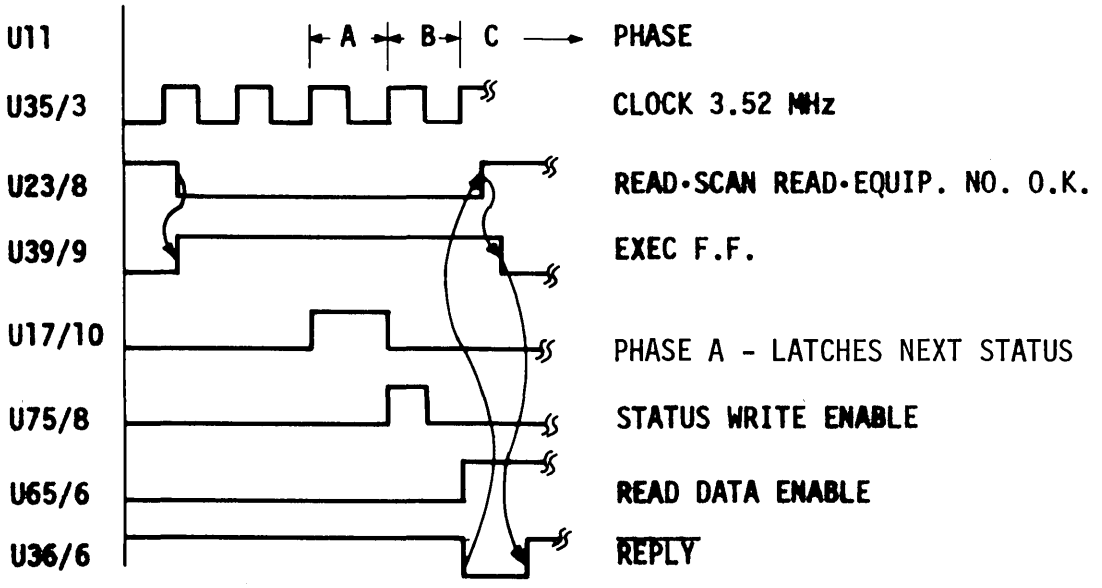
(C) COMPUTER PERFORMS WRITE OR READ TO CHANNEL:Q00=0, PROTECT VIOLATION



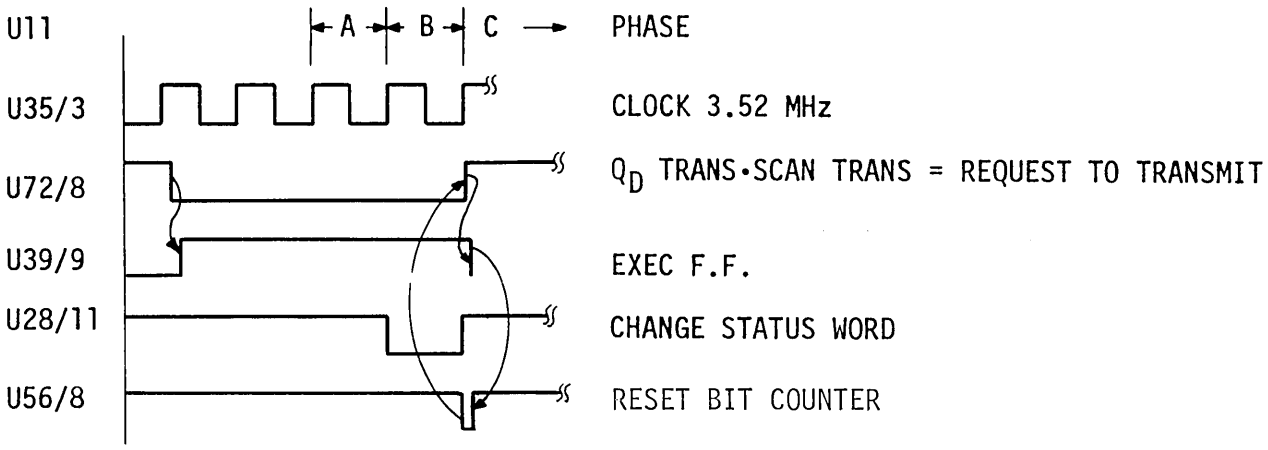
(D) COMPUTER PERFORMS READ FROM CHANNEL: Q00=0, BUFFER EMPTY, NO PROTECT VIOLATION



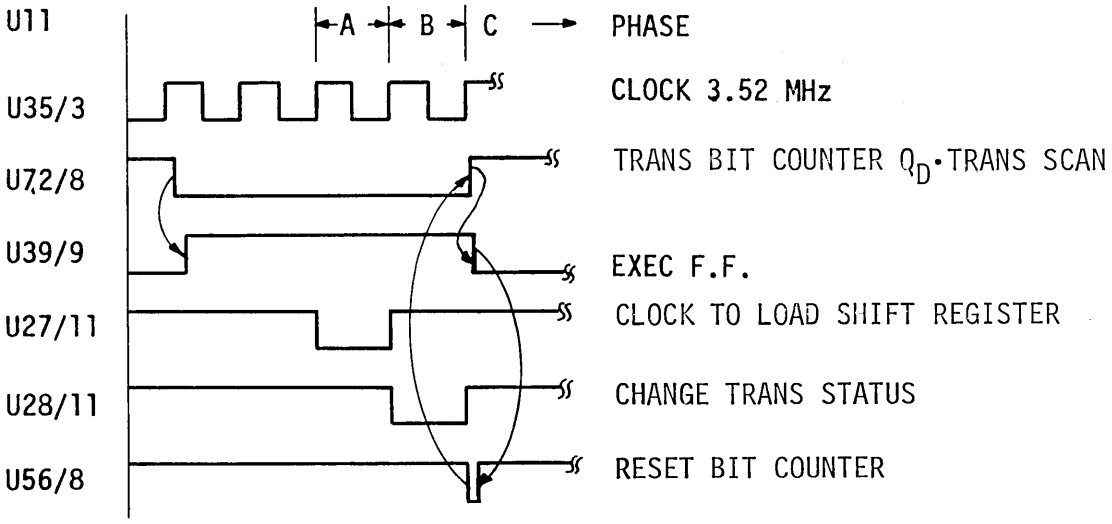
(E) COMPUTER PERFORMS READ FROM CHANNEL: Q00=0, BUFFER NOT EMPTY, NO PROTECT VIOLATION



(F) TRANSMIT LOGIC OPERATION - NO DATA IN BUFFER

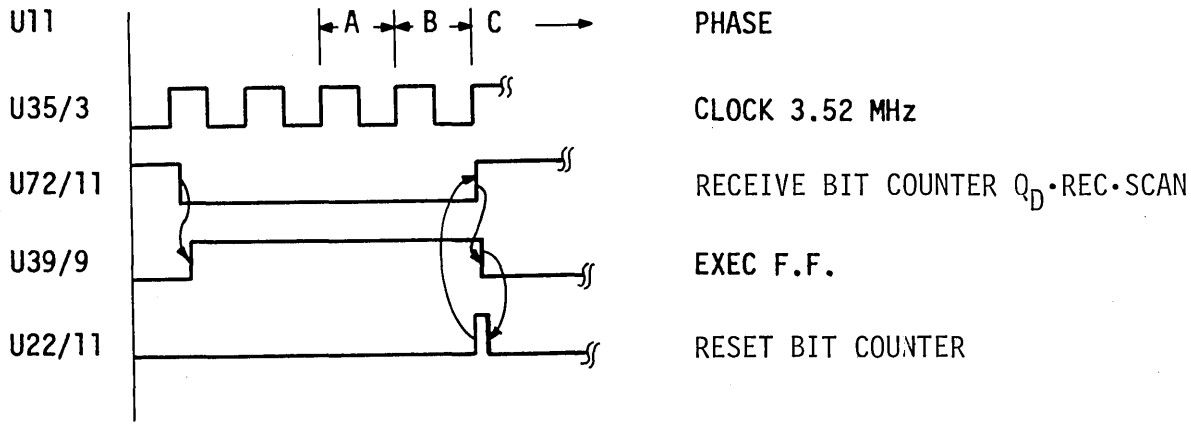


(G) TRANSMIT LOGIC OPERATION - DATA IN BUFFER



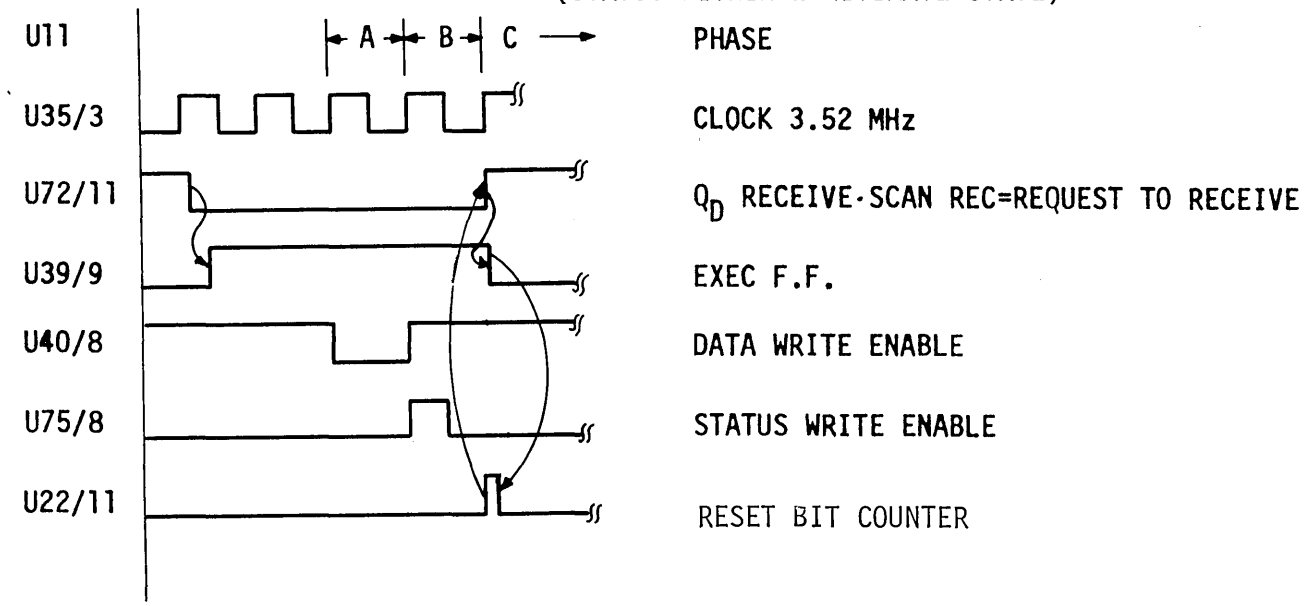
(H) RECEIVE LOGIC OPERATION - IDLE CHARACTER RECEIVED

(STATUS WITHIN LEGITIMATE STATE)



(I) RECEIVE LOGIC OPERATION - DATA CHARACTER RECEIVED

(STATUS WITHIN LEGITIMATE STATE)



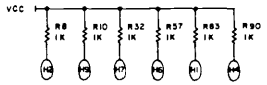
REVISION RECORD						
1 2 3 4 5			DESCRIPTION	DATE		
	01	CK 1205	RELEASED CLASS B	R S		

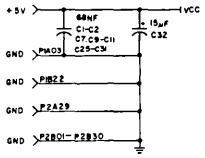
ØFF SHEET REFERENCE

ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION			
		2	3	4	5
A	SRQWC	5-A	6-C		
B	CPCRP	3-C	7-C		
C					
D	TPHA	1-B	6-C	4-B	2-B
E	TPHC	1-C		8-B	5-C
F	WCDEM	4-B		3-C	
G					
H	SRQTX	5-A		8-B	
I	EQEQO	5-B	6-D		
J	RCARQ	4-B			7-D
K	CRQAP	3-C	5-C	8-D	2-A
L	REC SIG DET		5-B	8-C	
M	PHTCK	2-C			5-B
N	ENACC	2-B	6-B		
O	RCDEM	4-B			5-C
P	CREAD	8-B	8-D		
Q	SRQRC	5-B	6-C		5-B
P					
S	PHAWC		5-C	8-C	
T	WTYSB		5-C	3-A	
U	A6		3-A	7-C	
V	A5		3-A	7-C	
W	A4		3-A	7-D	
X	A3		1-D	7-C	
Y	BA2		2-C	7-C	
Z	BA1		4-C	7-C	

ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION			
		2	3	4	5
AA	BA0		4-C	6-D	
AB					
AC	BQ5		4-B	8-D	5-A
AD	BQ4		4-B	8-D	5-A
AE	MCVA0		3-B		5-A
AF	MCVA1		3-B		5-A
AG	MCVA2		3-B		5-A
AH	MCVA3		3-B		5-A
AI	MCVA4		3-A		7-A
AJ	MCVA5		3-A		7-A
AK	MCVA6		3-A		7-A
AL	MCVPB		3-A		7-A
AM	OPEND		4-B		4-B
AN	TRDEA	4-B		3-C	
AO	RCVSD		7-B		3-B
AP	PHARC		7-B		5-B
AQ	SYND		8-B		3-B
AR	FMKCV		5-A		8-D
AS	TPHP	1-C		3-C	5-B
AT	WTXSB		6-B	6-A	
AU	MDCV		7-A		8-C
AV	FMKCV		6-A		6-D
AW	FMKTX		6-A	3-B	
AX	SRQCV	4-B			8-D
AY	FZFRJ	2-C	5-C		
AZ	FMKTX		6-A	8-B	

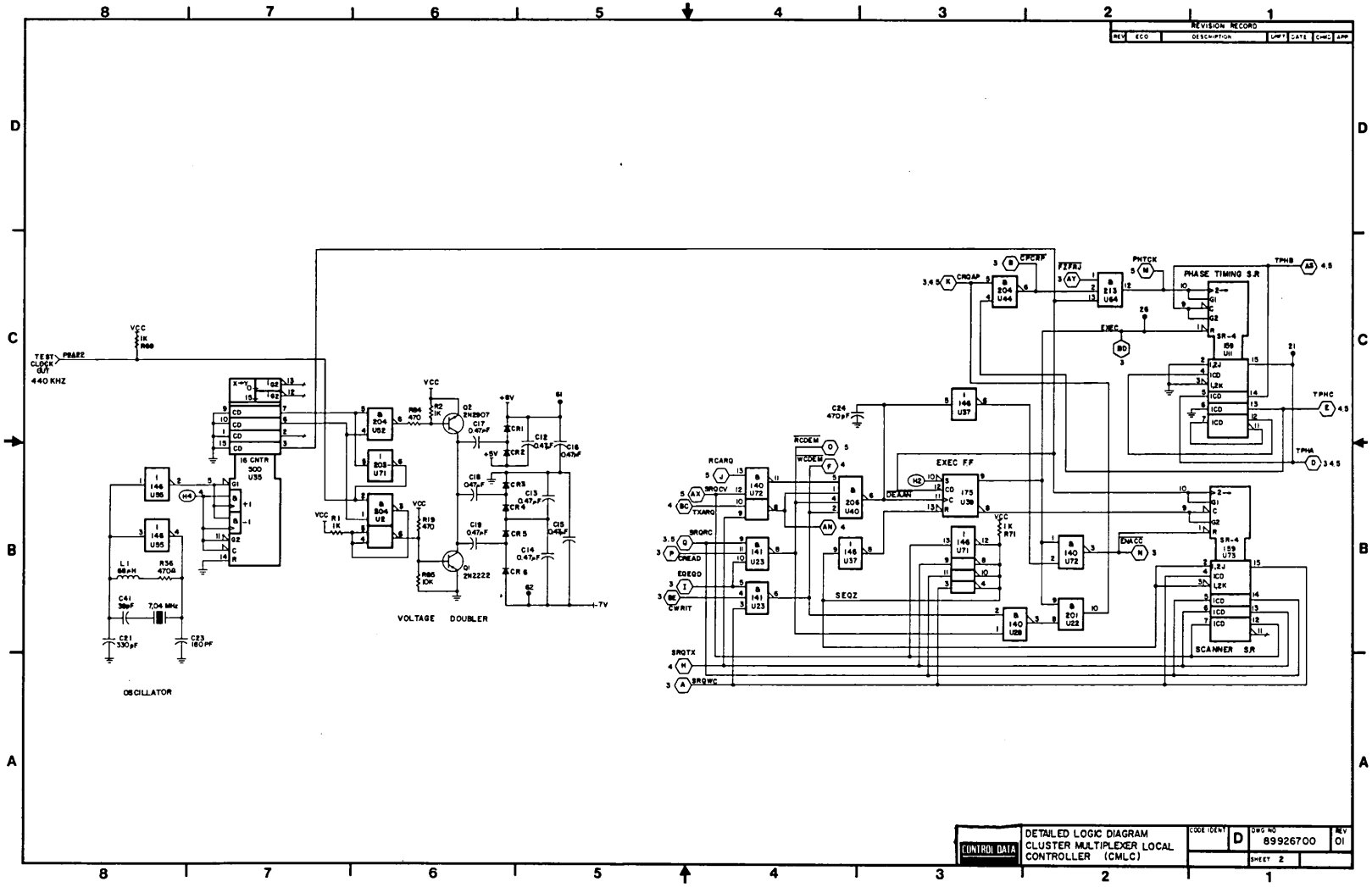
ØFF SHEET REFERENCE LETTER	SIGNALS	SHEET LOCATION			
		2	3	4	5
BA					
BB					
BC	TXAPQ	5-B		7-C	
BD	EXEC	3-C	6-C		
BE	CWRIT	5-B	6-D		
BF	BSQ6		4-B	8-D	5-A

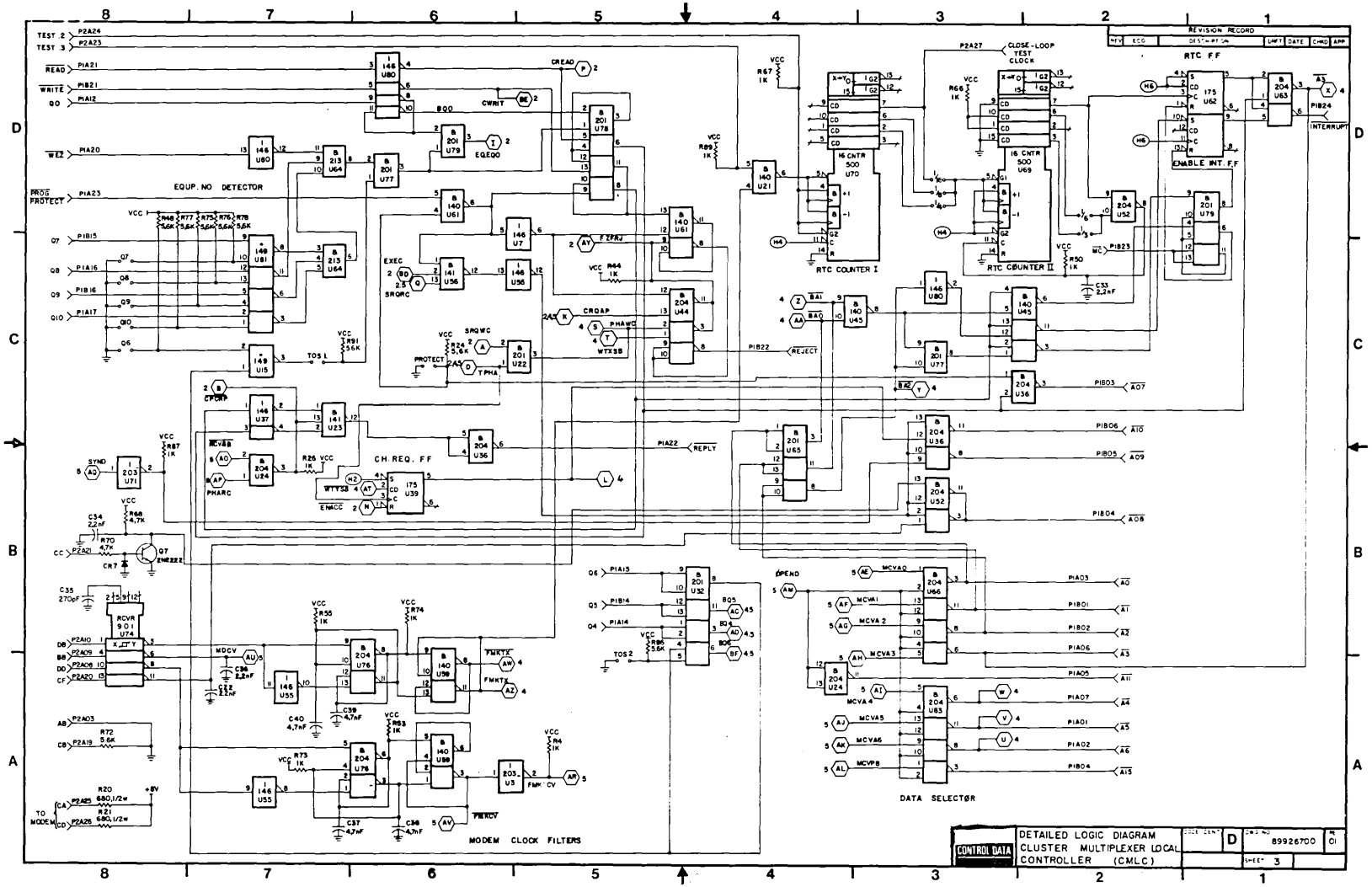


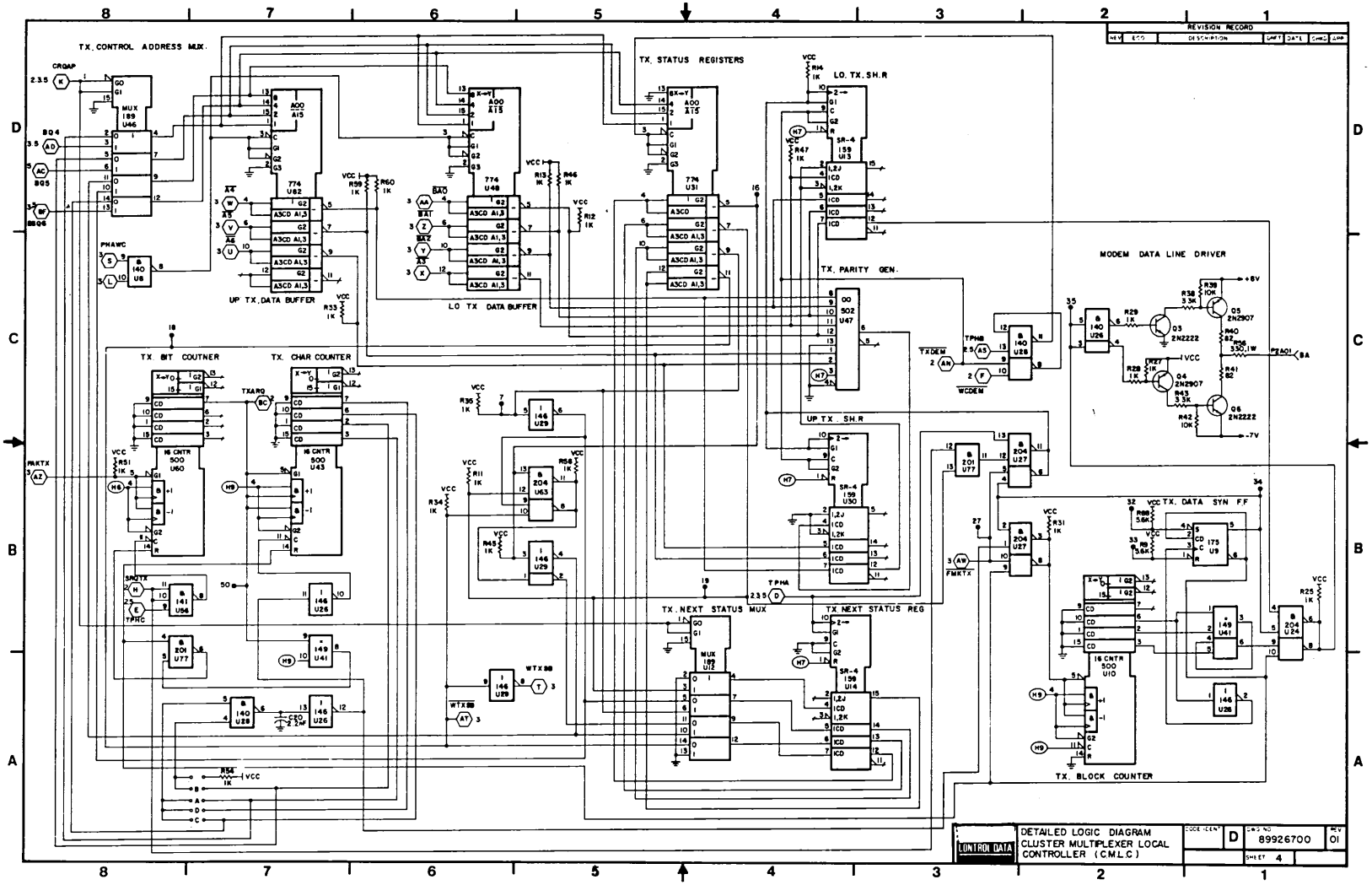


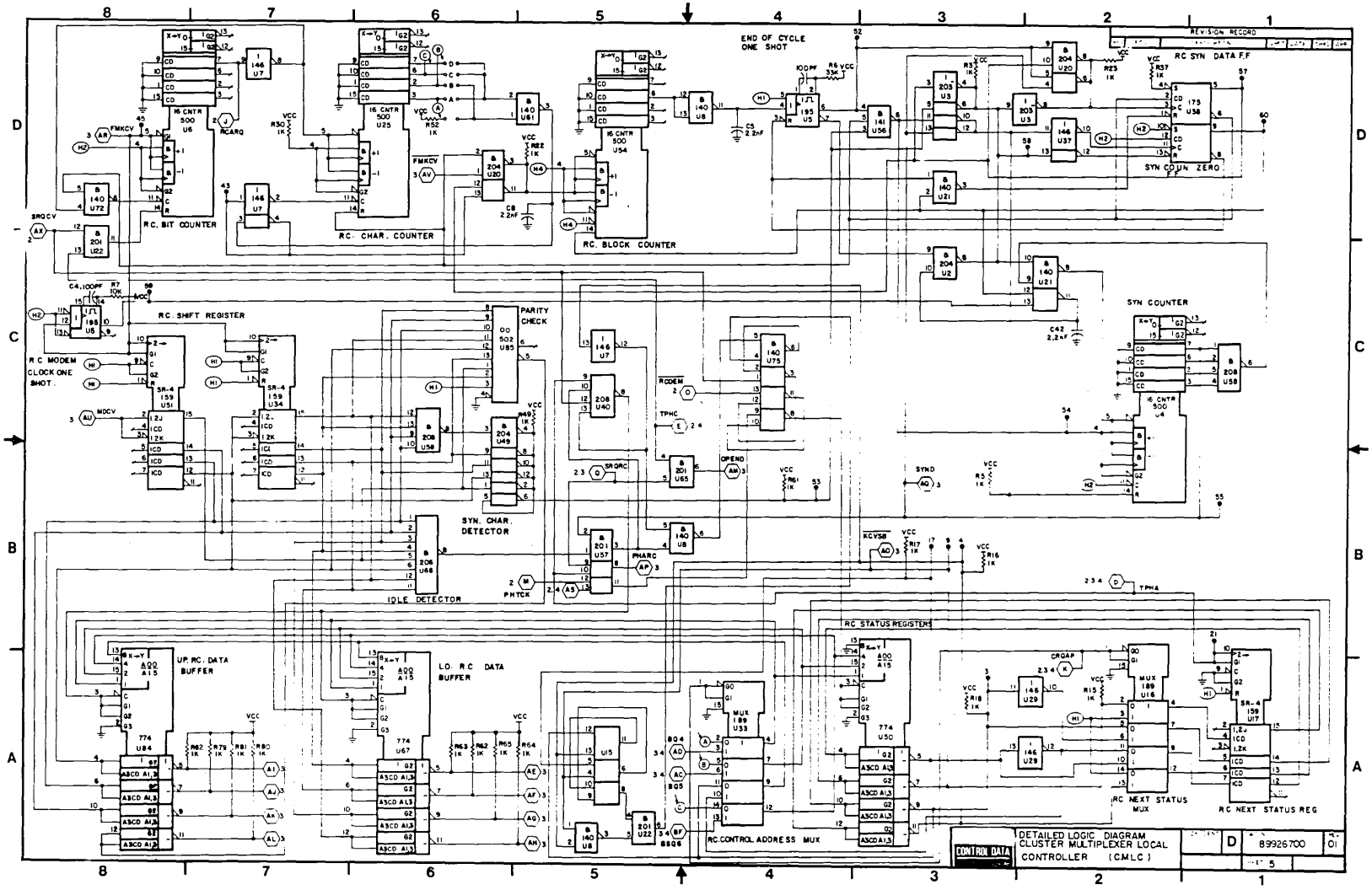
NOTES
1. ALL RESISTORS ARE 0.25 WATT 5% UNLESS OTHERWISE SPECIFIED.
2. CR1-CR7 ARE IN 4151

AY 89859700	CONTROL DATA	FC-60KA	DETAILED LOGIC DIAGRAM CLUSTER MULTIPLEXER LOCAL CONTROLLER (CMLC)	
AW 89859600 DETACHED LISTS	DO NOT SCALE DRAWING	DRAWN N P 03 3 79		
	MATERIAL	CHKD HAIM 8 15 79	CODE IDENT D	DRAWING 89926700
	FINISH	ENGR		
		MFG		
		APPR	SCALE	SHEET 1 OF 5


REVISION RECORD
REV ECO DESCRIPTION DWFT DATE CHKD APP
TEST CLOCK 0/1 440 KHZ
PBARZ
VCC 1K R66
16 CNTR 300 U35
OSCILLATOR
VOLTAGE DOUBLER
PHASE TIMING S.R
SCANNER S.R
EXEC FF
SEQZ
RCDEM
WCDEM
RCARQ
SRQCV
TXARQ
SRQRC
READ
EDEQD
CWRIT
SRQTX
SRQWC
CPCRF
CRQAP
FTPRJ
PHTCK
EXEC
TPHB
TPHC
TPHA
ENACC
DEXAM
CONTROL DATA
DETAILED LOGIC DIAGRAM CLUSTER MULTIPLEXER LOCAL CONTROLLER (CMLC)
CODE IDENT D
DWG NO 89926700
REV 01
SHEET 2


EQUP. NO DETECTOR
RTC FF
RTC COUNTER I
RTC COUNTER II
ENABLE INT. FF
CH. REQ. FF
MODEM CLOCK FILTERS
DATA SELECTOR
CONTROL DATA
DETAILED LOGIC DIAGRAM
CLUSTER MULTIPLEXER LOCAL
CONTROLLER (CMLC)
89926700
SHEET 3


TX. CONTROL ADDRESS MUX.
TX. STATUS REGISTERS
LO. TX. SH. R
MODEM DATA LINE DRIVER
TX. PARITY GEN.
UP TX. DATA BUFFER
LO TX DATA BUFFER
TX. BIT COUTNER
TX. CHAR COUNTER
UP TX. SH. R
TX. NEXT STATUS MUX
TX NEXT STATUS REG
TX. DATA SYN FF
TX. BLOCK COUNTER
REVISION RECORD
CONTROL DATA
DETAILED LOGIC DIAGRAM
CLUSTER MULTIPLEXER LOCAL
CONTROLLER (CMLC)
D
89926700
01
SHEET 4


REVISION RECORD
RC SYN DATA F.F
END OF CYCLE ONE SHOT
RC. BIT COUNTER
RC. CHAR. COUNTER
RC. BLOCK COUNTER
SYN COUN ZERO
SYN COUNTER
RC. SHIFT REGISTER
RC MODEM CLOCK ONE SHOT
PARITY CHECK
SYN. CHAR. DETECTOR
IDLE DETECTOR
UP. RC. DATA BUFFER
LO. RC DATA BUFFER
RC. STATUS REGISTERS
RC. CONTROL ADDRESS MUX
RC NEXT STATUS MUX
RC NEXT STATUS REG
DETAILED LOGIC DIAGRAM
CLUSTER MULTIPLEXER LOCAL
CONTROLLER (CMLC)
CONTROL DATA
D
89926700
01
5

SECTION 6

MAINTENANCE

MAINTENANCE

SCOPE

This section supplies maintenance references and procedures for the equipment listed in Section 1 of this manual.

TOOLS AND SPECIAL EQUIPMENT

The following is a list of maintenance tools recommended for maintenance of this equipment:

Part Number	Part Description	Quantity
89688700	Board Extender	1
89670300	Board Extractor	1
	Oscilloscope, Tektronix 453 or Equiv.	1
	Digital Voltmeter	1

The publications listed below are applicable to the equipment:

Publication	Pub. No.
1784 Computer Customer Engineering Manual	89633300
1784 Reference Manual	89633400
1700 Computer System Codes Manual	60163500
System Maintenance Monitor (SMM 17)	60182000
OLYMPUS 1700 Diagnostic Package	39268100

MAINTENANCE

Preventive maintenance of the controller is not required. After it is determined that the controller has failed, remove and replace the PW assembly with an identical trouble-free assembly. For removal and replacement of the assembly, refer to Section 3 of this manual. After replacement, a diagnostic check should be run.

CAUTION

Do not remove or replace cables
or PW Assembly with power on.

Before concluding that the FC602-A is defective, it is advised to perform loop-back tests gradually including the Modems, communication line, and FC701-A/B.

The FC602-A can be self-tested if the following connections are made on the 66-pin connector instead of the external cable.

Pin Number Connections	Signals Connected
43 - 47	Test Clock Out - Test Clock In
45 - 5	Test Inhibit - GND
53 - 15 - 19	Simulation Clock - DD,DB
1 - 17	BB-BA (Data In to Data Out)

Performing such connections loops back Data Out to Data In and supplies an internal clock substituting the Modem timing elements.

SECTION 7

MAINTENANCE AIDS

(NOT REQUIRED)

SECTION 8

PARTS LIST

PARTS DATA

The following parts list is applicable to the FC602-A Cluster Multiplexer Local Controller.

NOMENCLATURE	PART NUMBER
Controller PW Assembly	89859700
External Cable Assembly	89859300
Internal Cable Assembly	89641800
Interrupt Cable Assembly	89724700

SECTION 9

WIRE LIST

WIRE LIST

The included pin lists are applicable to the FC602-A Cluster Multiplexer Local Controller. Wire size in AWG, wire color, origin and destination, and signal names are included herein.

A pin list for the CMLC PWB is also included in this section in Table 9-3.

TABLE 9-1. EXTERNAL CABLE ASSEMBLY WIRING LIST

DWN.	S.D.	2.75
CHKD.	DD	2.75
ENG.	Hazeen	2.75
MFG.		
APPR.		

CONTROL DATA CORPORATION
CODE IDENT

TITLE: WIRING LIST for EXTERNAL CABLE ASSY. C.M.L.C.

PREFIX: W.L.

DOCUMENT No.: 89859300

REV.: 01

FIRST USED ON: FC601-A

SHEET 1 of 2

SHEET REVISION STATUS

1	2
01	01

REVISION RECORD

REV.	ECO	DESCRIPTION	DRFT.	DATE	APP.
01	CK 1131	RELEASED CLASS B	Logan	Feb 10, 75	DJ

NOTES:

P.L. 89859300
DETACHED LISTS

ET-5100

89858800

9-2

CONTROL DATA CORPORATION

EXTERNAL CABLE ASSY -
C.M.L.C.

CODE IDENT.

SHEET 2

WL

DOCUMENT No. 89859300

REV. 01

TABLE 9-1. EXTERNAL CABLE ASSEMBLY WIRING LIST

CONDUCTOR IDENT.	FIIND No	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	DESTINATION		ACCESS FIND No.	REMARKS
1	10	AWG20	BRN	SEE ASSY DWG	P1	2	F/N 1	J1	1	F/N 12	BA-T. DATA
2		AWG24	RED		P1	3		J1	17		BB-R. DATA
3		AWG24	ORN		P1	4		J1	49		CA-RTS
4		AWG24	BLU		P1	5	-	J1	37		CB-CTS
5		AWG24	VIO		P1	6		J1	39		CC-DSR
6		AWG20	BLK		P1	7		J1	5		AB-SG
7		AWG24	GRA		P1	8		J1	41		CF-RLSD
8		AWG20	BRN		P1	15		J1	19		DB-TSET
9		AWG20	BLK		P1	17		J1	15		DD-RSET
10		AWG24	WHT		P1	20		J1	51		CD-DTR

ZT:5103

DWN.		
CHKD.		
ENG.		
MFG.		
APPR.		

CONTROL DATA CORPORATION

CODE IDENT

TITLE: INTERNAL CABLE
CLUSTER MULTIPLEXER LOCAL CONTROLLER

PREFIX: W.L.

DOCUMENT No.:

REV.:

FIRST USED ON:

SHEET 1 OF 4

SHEET REVISION STATUS

REVISION RECORD

REV.	ECO	DESCRIPTION	DRFT.	DATE	APP.

NOTES: This is the wiring list of the internal cable used with the FC601-A.
The wiring list was generated by appending W.L. No. 89641800
with the appropriate signal names associated with the FC601-A.

DETACHED LISTS

ET-5100

CONTROL DATA CORPORATION

INTERNAL CABLE

CLUSTER MULTIPLEXER LOCAL CONTROLLER

CODE IDENT.

SHEET 2

WL

DOCUMENT No.

REV. 01

TABLE 9-2. INTERNAL CABLE WIRE LIST (CONT'D)

CONDUCTOR IDENT.	FIIND No	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	DESTINATION	ACCESS FIND No.	REMARKS
1	5	AWG28		14"	P2	A01	3,4	1	1,2	BA - TRANSMITTED DATA
2					P2	B01		2		GND
3					P2	A02		3		
4					P2	B02		4		GND
5					P2	A03		5		AB - SIGNAL GROUND
6					P2	B03		6		GND
7					P2	A04		7		
8					P2	B04		8		GND
9					P2	A05		9		
10					P2	B05		10		GND
11					P2	A06		11		
12					P2	B06		12		GND
13					P2	A07		13		
14					P2	B07		14		GND
15					P2	A08		15		DD - RECEIVED SIGNAL ELEMENT TIMING
16					P2	B08		16		GND
17					P2	A09		17		BB - RECEIVED DATA
18					P2	B09		18		GND
19					P2	A10		19		DB - TRANSMITTED SIGNAL ELEMENT TIMING
20					P2	B10		20		GND
21					P2	A11		21		
22					P2	B11		22		GND
23					P2	A12		23		
24					P2	B12		24		GND
25					P2	A13		25		
26	5	AWG28		14"	P2	B13	3,4	26	1,2	GND

ET-5103

CONTROL DATA CORPORATION

INTERNAL CABLE
CLUSTER MULTIPLEXER LOCAL CONTROLLER

CODE IDENT.

SHEET 3

WL

DOCUMENT No.

REV. 01

TABLE 9-2. INTERNAL CABLE WIRE LIST (CONT'D)

CONDUCTOR IDENT.	FIIND No.	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	DESTINATION	ACCESS FIND No.	REMARKS
27	5	AWG28		14"	P2	A14	3,4	27	1,2	
28					P2	B14		28		GND
29					P2	A15		29		
30					P2	B15		30		GND
31					P2	A16		31		
32					P2	B16		32		GND
33					P2	A17		33		
34					P2	B17		34		GND
35					P2	A18		35		
36					P2	B18		36		GND
37					P2	A19		37		CB - CLEAR TO SEND
38					P2	B19		38		GND
39					P2	A20		39		CF - RECEIVEDLINE SIGNAL DETECTOR
40					P2	B20		40		GND
41					P2	A21		41		CC - DATA SET READY
42					P2	B21		42		GND
43					P2	A22		43		TEST CLOCK OUT
44					P2	B22		44		GND
45					P2	A23		45		TEST 3
46					P2	B23		46		GND
47					P2	A24		47		TEST 2
48					P2	B24		48		GND
49					P2	A25		49		CA - REQUEST TO SEND
50					P2	B25		50		GND
51					P2	A26		51		CD - DATA TERMINAL READY
52	5	AWG28		14"	P2	B26	3,4	52	1,2	GND

(CONT.)

CONTROL DATA CORPORATION

INTERNAL CABLE

CLUSTER MULTIPLEXER LOCAL CONTROLLER

CODE IDENT.

SHEET 4

WL

DOCUMENT No.

REV. 01

CONDUCTOR IDENT.	FIIND No	GAUGE (REF.)	COLOR (REF.)	LENGHT (APPROX.)	ORIGIN		ACCESS FIND No.	DESTINATION	ACCESS FIND No.	REMARKS
53	5	AWG28		14"	P2	A27	3,4	53	1,2	CLOSE-LOOP TEST CLOCK
54					P2	B27		54		GND
55					P2	A28		55		
56					P2	B28		56		GND
57					P2	A29		57		GND
58					P2	B29		58		GND
59					P2	A30		59		
60	5	AWG28		14"	P2	B30	3,4	60	1,2	GND

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TABLE 9-2. INTERNAL CABLE WIRE LIST (CONT'D)

TABLE 9-3. PWB PIN LIST (CONT'D)

CONNECTOR/PIN	SIGNAL NAME
P2A1	BA
2	
3	AB
4	
5	
6	
7	
8	DD
9	BB
10	DB
11	
12	
13	
14	
15	
16	
17	
18	
19	CB
20	CF
21	CC
22	TEST CLOCK OUT
23	TEST 3
24	TEST 2
25	CA
26	CD
27	CLOSE-LOOP TEST CLOCK
28	
29	GND
30	
P2A31	VCC

CONNECTOR/PIN	SIGNAL NAME
P2B1	GND
2	
3	
4	
5	
6	
7	
8	
9	
10	
11	
12	
13	
14	
15	
16	
17	
18	
19	
20	
21	
22	
23	
24	
25	
26	
27	
28	
29	
30	
P2B31	GND

TABLE 9-3. PWB PIN LIST

CONNECTOR/PIN	SIGNAL NAME
P1A1	$\overline{A5}$
2	$\overline{A6}$
3	$\overline{A0}$
4	
5	$\overline{A11}$
6	$\overline{A3}$
7	$\overline{A4}$
8	
9	
10	
11	$\overline{A15}$
12	Q0
13	
14	Q4
15	Q6
16	Q8
17	Q10
18	
19	
20	$\overline{W=0}$
21	$\overline{READ}$
22	$\overline{REPLY}$
23	$\overline{PROTECT}$
24	
25	
26	
27	
28	
29	GND
30	
P1A31	

CONNECTOR/PIN	SIGNAL NAME
P1B1	$\overline{A1}$
2	$\overline{A2}$
3	$\overline{A7}$
4	$\overline{A8}$
5	$\overline{A09}$
6	$\overline{A10}$
7	
8	
9	
10	
11	GND
12	
13	
14	Q5
15	Q7
16	A9
17	
18	
19	
20	
21	$\overline{WRITE}$
22	$\overline{REJECT}$
23	$\overline{MC}$
24	$\overline{R.T.C.\ INT.}$
25	
26	
27	
28	
29	
30	
P1B31	

(CONT.)

COMMENT SHEET

MANUAL TITLE CDC® FC602-A Distributed Cluster Local Controller

Reference/Customer Engineering Manual

PUBLICATION NO. 89858800 REVISION A

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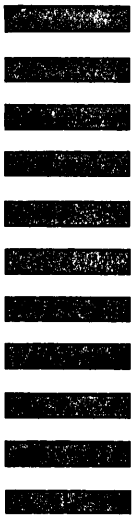

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