

CONTROL DATA[®] BUFFERED DATA CHANNEL

1706-A, DT129-A, FV430-A

**DIAGRAMS AND
CIRCUIT DESCRIPTION
MAINTENANCE
PARTS DATA**

**CONTROL DATA
CORPORATION**

CUSTOMER ENGINEERING MANUAL

MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

SHEET 1 OF 1

		EQUIPMENTS					
MANUAL REV	FCO OR ECO	DT129-A	1706-A	FV430-A			
G	FCO27468	A02	A06	--			
H	ECO29964	A02	A06	A01			
J	ECO28023	A08	A08				

CONTENTS

Part 1. <u>Diagrams and Circuit Description</u>					
Logic Diagram Symbols	1-ii	Incrementer, Storage Address Register, Storage Transmitter (ADR) Bits 00-07			1-21
Block Diagram	1-1	Incrementer, Storage Address Register, Storage Transmitter (ADR) Bits 08-14			1-23
A/Q Channel Timing	1-2	Storage Hold, Compare, Auxiliary Address Register			1-25
Direct Storage Access Timing	1-3	Timing Sequence			1-27
Scanner Detail Including Switch Receiver, Transmitter Control Signals	1-5	Card Placement Map			1-29
Status, Peripheral Read/Write Control	1-7				
Storage Address, W Translator, F Register Control Signals	1-9	<u>Part 2. Maintenance</u>			
Reply, Reject Control	1-11	Introduction			2-1
Data Transmitter, Data Receiver, X Register Bits 00-07	1-13	Physical Description			2-2
	1-15.1	Cabling Information			2-2
	1-15.3	<u>Part 3. Parts List</u>			
Data Transmitter, Data Receiver, X Register Bits 08-15	1-17.1	Introduction			3-1
	1-17.3	Parts List Breakdown			3-2
Q Receiver, Q Transmitter, W Translator, F Register	1-19	<u>Part 4. Card Placement</u>			
W Translator Z62, 63, 64 Cards L.S.	1-19.3	See Page 1-29			

FIGURES

1-1 Control Signal Transmission	1-6	1-6 Incrementer Network	1-20
1-2 Read/Write Timing	1-8	1-7 Compare Network	1-24
1-3 Data Flow in BDC	1-14	1-8 Z52 Module	1-24
1-4 BDC Address Flow	1-18	2-1 1706 Chassis	2-3
1-5 I/O Address Format	1-18	2-2 1706 Connector Panel	2-4

TABLES

1-1 Control Signals	1-6	2-1 Physical Characteristics	2-2
1-2 BDC Status Bits	1-8	2-2 A/Q Channel	2-6
1-3 1706 Addresses and Operations	1-18	2-3 Direct Storage Access Bus	2-7

FOREWORD

This manual contains logic diagrams and circuit descriptions, card placement, maintenance information, and a parts list for the CONTROL DATA* 1706-A/DT129-A Buffered Data Channel (BDC). Information for Standard Option FV430-A which provides the BDC with 65K addressing capabilities, is also contained in this manual.

The logic diagrams are arranged according to modules and wherever possible, a complete module appears on a logic diagram. The Logic Diagram Symbols, page 1-ii, precedes the logic diagrams. This page illustrates and describes each of the standard logic symbols used in the logic diagrams. The block diagram on page 1-1 indicates signal flow through the BDC. BDC operations are used in the description of the block diagram.

The maintenance section provides a physical description of the BDC, cabling information, and general maintenance information.

The parts list in this manual provides a listing of all parts of the BDC and its power supply.

*Registered trademark of Control Data Corporation

PART 1

DIAGRAMS AND CIRCUIT DESCRIPTION

LOGIC DIAGRAM SYMBOLS

Two signals, a logical "0" and a logical "1", are the possible input or output conditions of a circuit. By convention, "1" is considered "up" and "0" is considered "down" on a timing chart, for example. Detailed descriptions of logic symbols and their associated electronic representations are contained in the Printed Circuits Manual, Vols. 3 and 4.

STANDARD LOGIC SYMBOLS

The 1700 Computer logic is mainly composed of the CONTROL DATA 6000 Series printed circuit modules. Standard logic diagram symbols for this type of printed circuit modules are inverters, test points, flip-flops, and twisted pair line drivers.

INVERTERS

An inverter is a logic element which provides an output that is an inversion of its input. When an inverter receives more than one input, "0's" take precedence over "1's" and drive the output of the inverter to "1". Because all of the several inputs have to be "1" to drive the output of the inverter to a "0", the inverter may be considered an inverting AND (or NAND) gate when more than one input is present. Logic diagrams show the basic inverter as an arrow into either a circle or a square (see Figure 1). Both symbols represent the same electronic circuit and have the same logical interpretation. In a logic sequence of inverters, circle and square symbols are usually alternated as an aid in tracing signals, e.g., a "1" output from a square symbol implies a "1" output from subsequent squares in the logic chain if each symbol in the chain has only one input.

Acceptable conventions for showing multiple inputs and outputs are given in Figure 2. Note that the output of inverter A is "0" only if inputs X, Y, and Z are all "1". The multiple outputs are identical.

Figure 3 shows an example of an inverter network. Because multiple outputs are identical, Figure 4 shows only one arrow in cases where an inverter (A) serves as the single input to several succeeding inverters. In more complex inverter networks, multiple arrows are used (B to C and D because B is not the only input to C or D).



Figure 1. Inverter Symbols

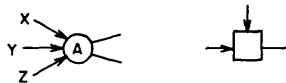


Figure 2. Multiple Inputs/Outputs

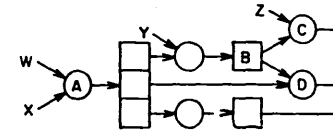


Figure 3. Inverter Networks

TEST POINTS

A test point performs no logic function. Logic diagrams show the test point as a triangle (see Figure 4). Test points are numbered from 1 to 6.

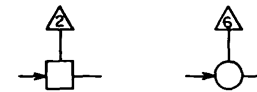


Figure 4. Test Point Symbols

FLIP-FLOPS (FF)

The flip-flop is composed of two inverters and functions as a storage device with two stable states designated as set and clear (see Figure 5). The flip-flop is set when the set output (B) is a "1" and clear when it is a "0". Note that the input (A) must be "0" to set the flip-flop, and (C) must be "0" to clear it.

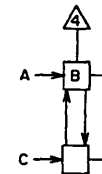


Figure 5. Flip-Flop Symbol

WIRE TAB DESIGNATIONS

Wire tab designations written next to a pin indicate where in the drawings the pin is connected. 3, 5, 7 - C37 - 6 indicates a connection with pin 6 of module C37, found on pages 3, 5, and 7. See Figure 5.1.

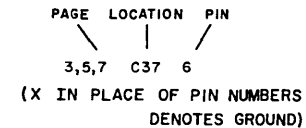


Figure 5.1. Wire Tab Designations

TWISTED PAIR DRIVERS

A Line Driver circuit transmits logic signals from one module to another. Modules are connected by twisted-pair lines. The standard square or circle represents the twisted-pair driver. However, the output of the square or circle connects to a pin of the module. The pin is then wired to a pin on another module (see Figure 6). The ground wire of the pair is wired to the connector ground bus of each module. The pins are represented by small circles and are numbered from 1 to 28. (Pins 29 and 30 are ground and +6 volts, respectively, and generally are not shown in logic diagrams.) The module location is shown above the card, and the module type is denoted in the upper right-hand corner.

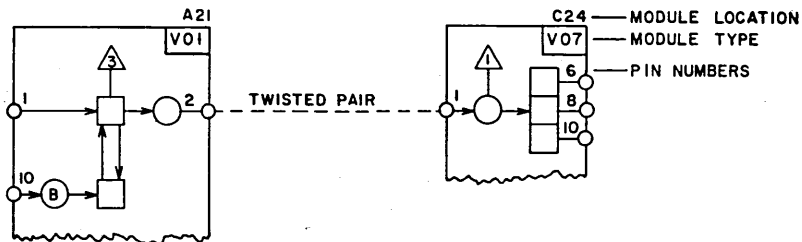


Figure 6. Twisted-Pair Line Driver

RECEIVER/TRANSMITTER CIRCUITS

The Receiver and Transmitter circuits detect and transmit signals from and to I/O interface respectively. The Receiver and Transmitter circuits are modifications of the standard 3000 Series circuits of the same name. These circuits are contained on a printed circuit module along with the standard inverter circuits.

Figures 7 and 8 shows that Receiver and Transmitter circuits are represented by the square symbol with an "R" or "T" respectively. The two inputs to the receiver are each connected to two pins on the module.

In Figure 7, a "1" input to R is inverted, causing a "1" output from pin 6 and a "0" output from pin 13. Thus, with a "1" input, the Receiver circuit produces both True and Not outputs.

The Transmitter circuit receives a "1" input signal from a standard inverter or FF and transmits a "1" output signal to the I/O interface. In Figure 7, a "1" input to pins 7 and 9 causes a "1" output from T and thus to the I/O line.

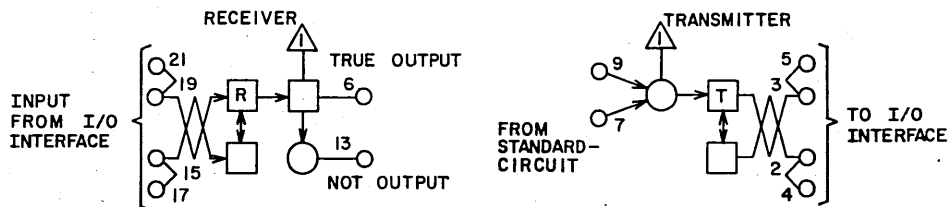
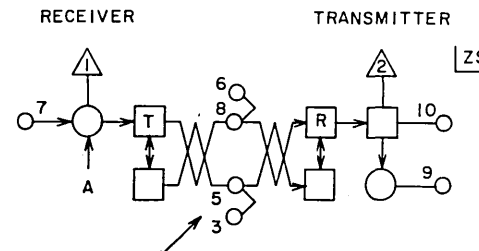


Figure 7. Receiver/Transmitter Circuit Examples



EACH STAGE OF THE ZS MODULE CONTAINS FOUR EXTERNAL PINS WITH INTERNAL CONNECTIONS.

Figure 8. ZS Transmitter/Receiver Module

SPECIAL CIRCUITS

In addition to the standard symbols, the diagrams also use symbols representing special nonstandard circuits. The symbols for these circuits along with a brief description are given below.

Special variations of the standard building block are indicated by the symbols shown on Figure 9. The symbol and schematic for the corresponding special circuit are shown on the applicable logic diagram and also on the module schematic in the Printed Circuits Manual.



Figure 9. Special Circuits

CAPACITIVE DELAY CIRCUITS

Capacitive Delay circuits delay input "1" signals a prescribed time before issuing an output "1" signal. The 1700 uses both fixed and variable delay circuits. Figure 10 shows examples of both types. The delay time of the circuit and capacitor value are listed beside the capacitor symbol. The variable potentiometer enables adjustment of the delay time of the circuit within certain limits.

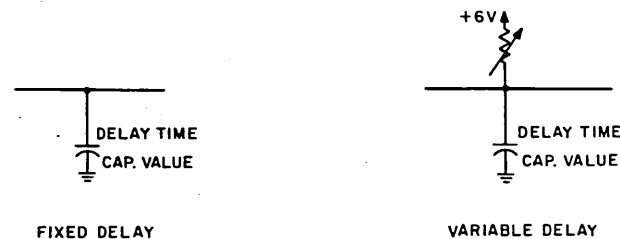


Figure 10. Capacitive Delay Circuits

**BUFFERED DATA CHANNEL
BLOCK DIAGRAM**

The 1706-A Buffered Data Channel (BDC) provides a 16-bit, bi-directional, buffered input/output path between the 1704 Computer and up to eight peripheral equipment devices (controllers).

The BDC contains no indicators or controls, so all operations must be initiated by the I/O instruction from the Q register of the computer. In response to an I/O instruction, the BDC connects the computer to one of the external controllers, and sets up the external controllers for a Read or Write operation. The BDC then controls the Read or Write operation, obtaining access to storage via the Direct Storage Access (DSA) when necessary to fetch or store information.

The Q receiver of the BDC receives the I/O instruction and transmits it to the W field translator and the F register. The W field translator translates bits 15-11 that control the BDC operation. The F register holds the I/O instruction during the entire buffered operation and gates it to the Q transmitter which in turn sends it to the peripheral controllers. Bits 10-00 select and address one of the peripheral controllers attached to the BDC.

The A transmitter and the A receiver of the BDC connect to the A register of the computer via the AQ channel. During a Direct Output operation, a 16-bit data word is transferred by the A receiver from the A register of the computer to the peripheral transmitter where it is presented to the selected peripheral device. During a buffered operation, the data word transmitted from the A register is the first word address minus one (FWA-1) of the block of data being transferred. During a BDC Function operation, the data word from the A register contains the function code. The A transmitter returns a 16-bit data word to the computer which contains:

- 1) Status information during a Status operation.
- 2) A 16-bit data word from the peripheral device through the peripheral receiver during a Direct Input operation.
- 3) The current address during a Terminate operation.

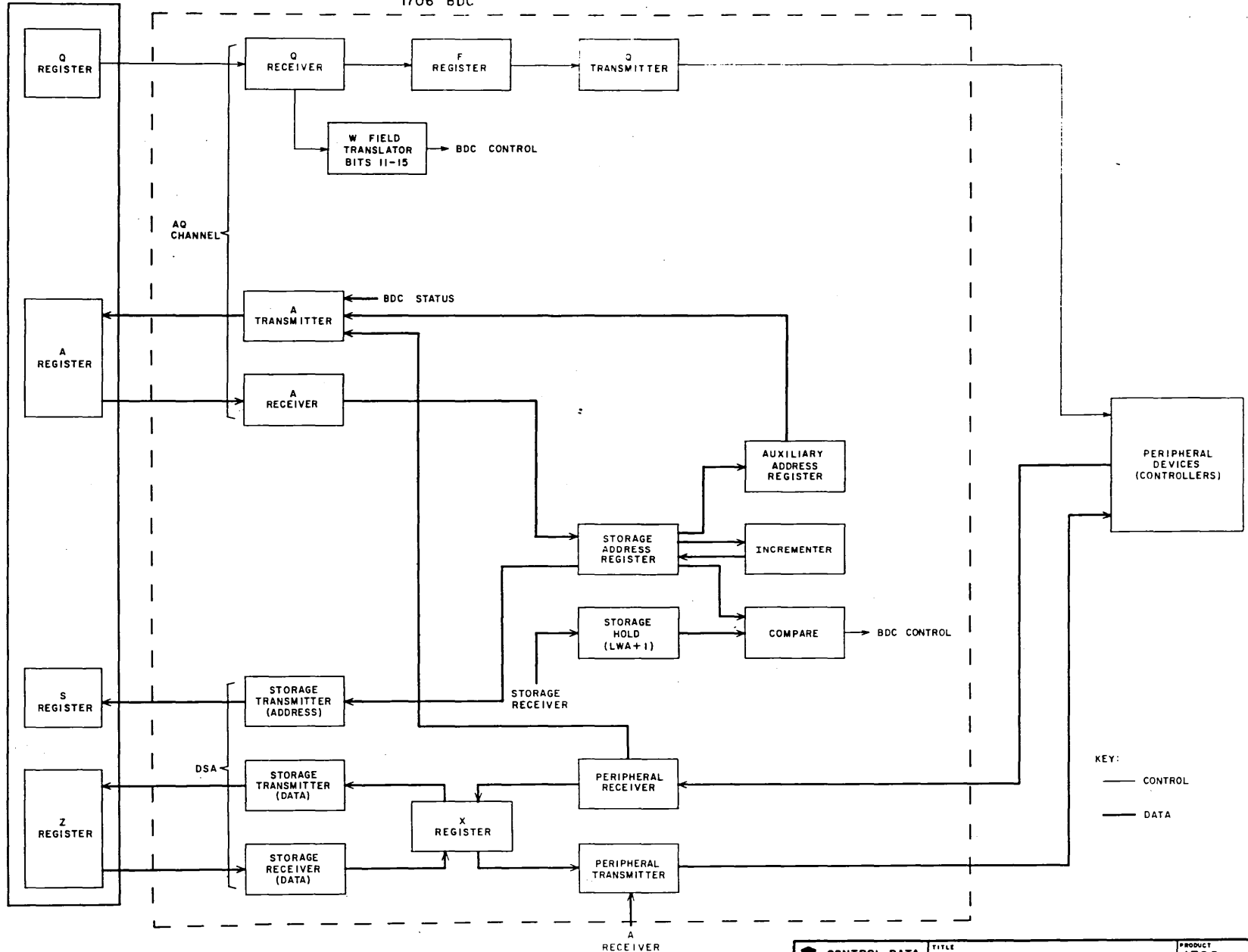
During a buffered operation, the Storage Address register receives the address of the control word (FWA-1) from the A receiver. The control word is the last word address plus one (LWA + 1) of the block of data being transferred and is held in the Storage Hold register. The current address is in the Storage Address register and temporarily held in the Auxiliary Address register where it is available to the computer upon request. After each transfer of a data word in the block, the current address is incremented by one in the Incrementer register. The Compare register compares this address to the LWA + 1 from the Storage Hold register. If the two addresses are equal, the buffered operation is complete and a signal is sent to BDC control that terminates the buffered operation. If the addresses are not equal, the current address is sent to storage by the Storage transmitter. A transfer to that location occurs during an Input operation or a transfer from that location occurs during an Output operation.

The Storage transmitter (address) sends the address of the location in storage from which the Storage receiver (data) receives data or to which the Storage transmitter (data) transmits data.

The peripheral transmitter and peripheral receiver transmit data to and from the peripheral controllers. The X register is a temporary holding register, holding a data word until storage or the peripheral controller is ready to accept it.

1704 COMPUTER WITH
1705 INTERRUPT/DATA CHANNEL
1704 COMPUTER

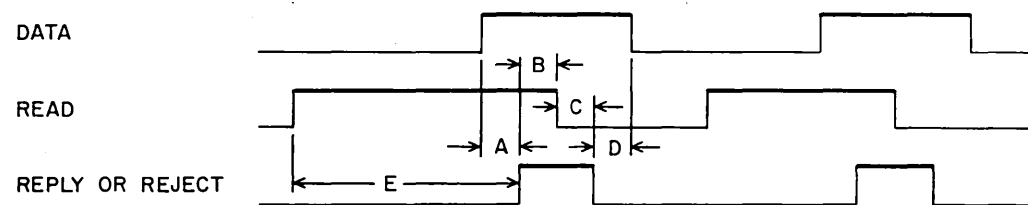
1706 BDC



KEY:
— CONTROL
— DATA

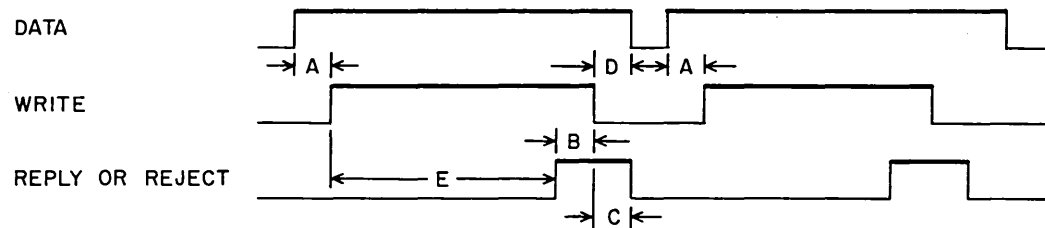
CONTROL DATA CORPORATION COMPUTER DIVISION	TITLE BUFFERED DATA CHANNEL (BDC) BLOCK DIAGRAM	PRODUCT 1706
		SIZE DRAWING NO C 60165700
		REV A
		SHEET 1-1

INPUT OPERATION



- | | |
|---|---|
| A = 0 μ SEC MIN (Q) PERIPHERAL DEVICE | D = 0 μ SEC MIN (Q) PERIPHERAL DEVICE |
| B = 0.0 μ SEC MIN (Q) COMPUTER | E = 4.0 μ SEC MAX (Q) PERIPHERAL DEVICE |
| C = 0.0 μ SEC MIN (Q) PERIPHERAL DEVICE | 0.2 μ SEC MIN (Q) PERIPHERAL DEVICE |

OUTPUT OPERATION

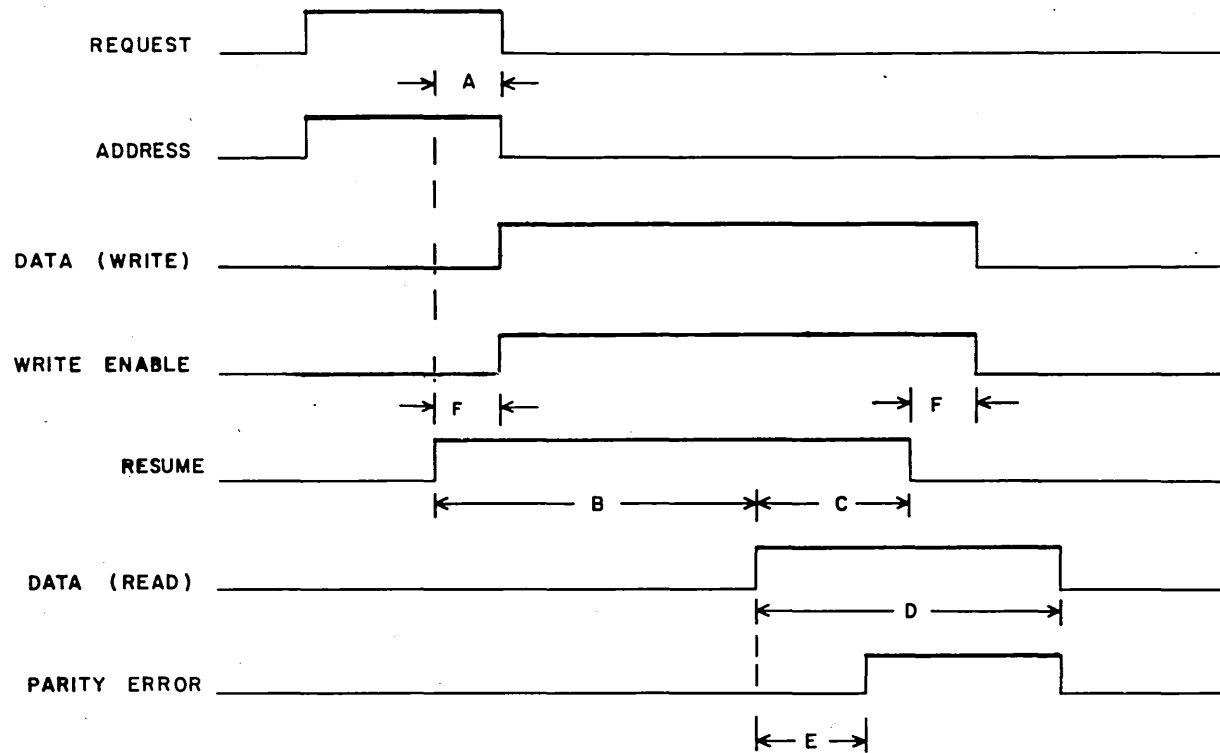


- | | |
|---|---|
| A = 0.1 μ SEC MIN (Q) COMPUTER | D = 0.1 μ SEC MIN (Q) COMPUTER |
| B = 0.0 μ SEC MIN (Q) COMPUTER | E = 4.0 μ SEC MAX (Q) PERIPHERAL DEVICE |
| C = 0.0 μ SEC MIN (Q) PERIPHERAL DEVICE | 0.2 μ SEC MIN (Q) PERIPHERAL DEVICE |

NOTE:

THE ADDRESS BITS WILL BE ON THE CHANNEL A MINIMUM OF 0.1 μ SEC BEFORE AND AFTER THE READ OR WRITE SIGNAL.

A-Q CHANNEL TIMING



TIMES MEASURED AT DEVICE

A = 0 NS MIN., 200 NS MAX.

B = 300 NS \pm 25 NS

C = 100 NS \pm 10 NS

D = 400 NS \pm 30 NS

E = 75 NS \pm 10 NS

F = 0 NS MIN., 100 NS MAX.

DIRECT STORAGE ACCESS TIMING

SCANNER DETAIL
INCLUDING SWITCH

Each device that connects to the Direct Storage Access contains in its logic a Scanner FF that is one stage of a distributed scanner. The various stages of the scanner are connected together via receiver-transmitter transmission lines. The last stage of the scanner transmits its output to the first stage, thus forming an oscillating scanner. If there is only one device on the DSA, the output from the Scanner FF is gated from the transmitter to the receiver of that device, thereby completing the circuit and still maintaining an oscillating scanner.

Any device connected to the DSA has a 5-position selector switch that indicates the position of the scanner stage. The five positions of the switch are: FIRST, MIDDLE, LAST, ONE UNIT, and OUT. The switch must be set to FIRST, MIDDLE, or LAST depending on whether the device contains the first, middle, or last stage of the Scanner circuit. There may be more than one middle stage in the Scanner circuit since any stage that is not the first or last stage is considered to be a middle stage. The switch must be set to ONE UNIT if there is only one device connected to the DSA. If there is a need to remove one of the devices from operation temporarily, the switch of that device must be set to OUT and the switches on the other devices must be changed to correspond to the new position that they acquired in the Scanner circuit.

The Z61 module contains the scanner stage and storage reference control logic for the BDC. When the Need FF and the Scanner FF are both set, the Halt Scanner FF will set. The clear side of the Halt Scanner FF is used to block clearing of the Scanner FF, thus halting the scanner. The Need FF and the Halt Scanner FF are

both cleared by a (Resume and Request Memory) signal (Z61, pins 5 and 10).

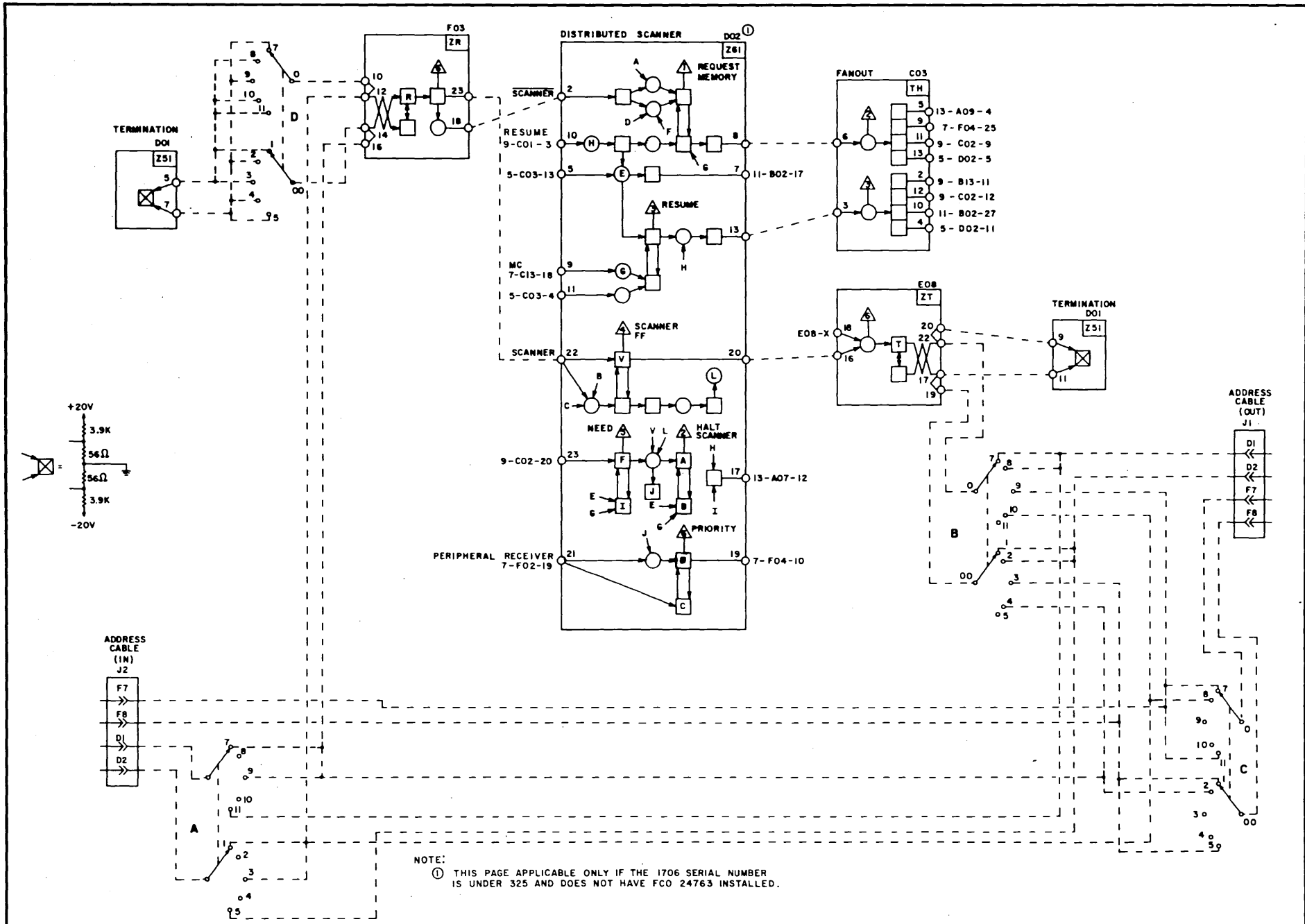
In a multiple word transfer the Need FF is cleared and reset after each word is transferred until current address equals the LWA + 1.

The Priority FF, when set, blocks clearing of the Scanner FF (output "C" of Priority FF). This prevents cycling of the scanner to allow multiple word transfers. Need and Halt continue to clear and reset after each word is transferred. The connected peripheral device will provide priority if it needs high speed transfer of data.

When the computer recognizes the memory request, it returns a Resume signal that enters the Z61 module at pin 10. The Resume signal is ANDed with the Request Memory signal at inverter E. A "0" output from inverter E sets the Resume FF and clears the Halt Scanner FF. This starts the scanner oscillating again.

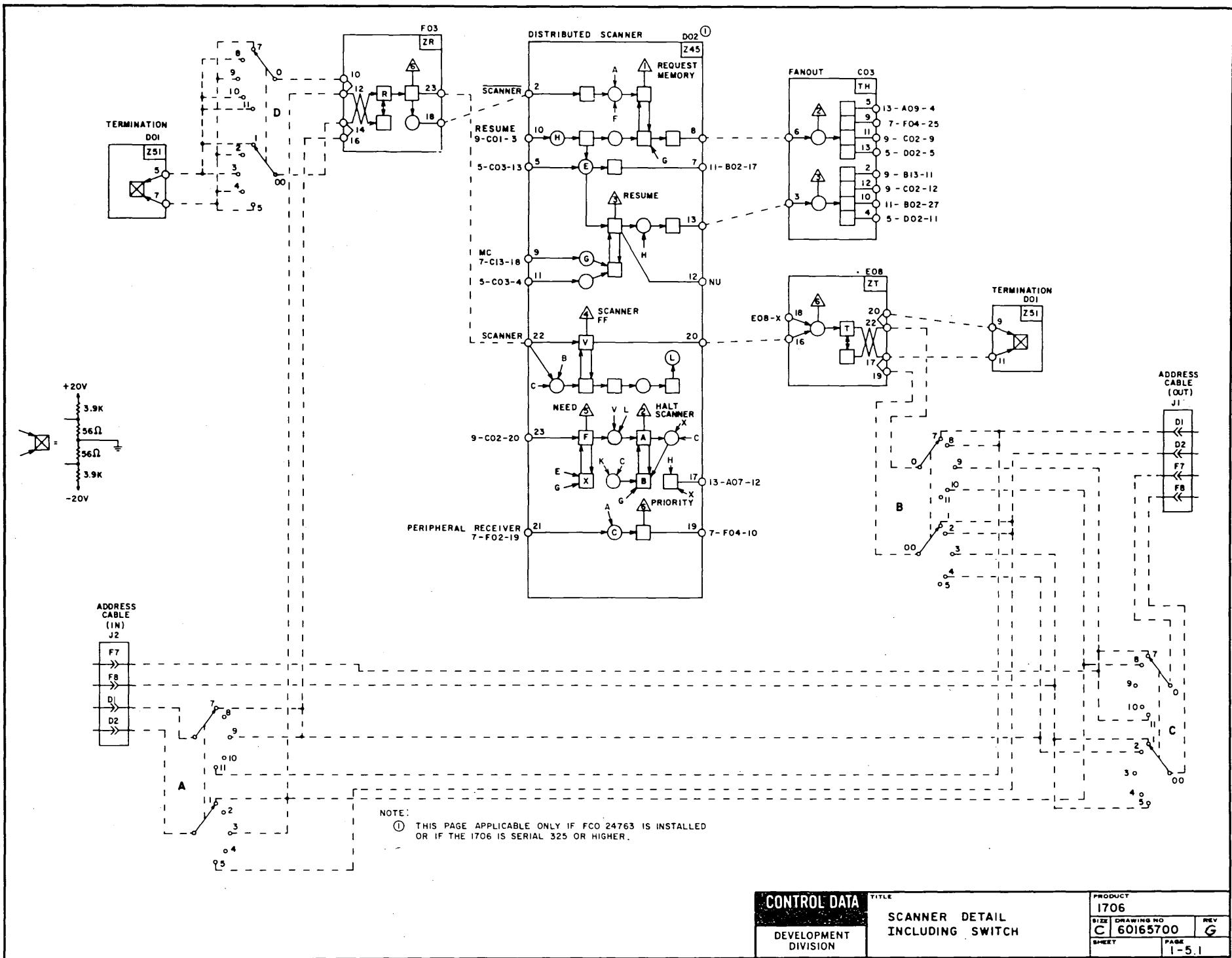
The ZR (page 1-5.0) and V36 (page 1-9) modules are receivers for the peripheral equipment and the computer memory. The ZT module transmits signals from the scanner to stage B of the switch. The schematic insert shows the 4 sections (A, B, C, and D) of the switch and the address cables that connect to it.

The Z51 module operates as a terminator for the transmission lines connecting the stages of the distributed scanner.



NOTE: ① THIS PAGE APPLICABLE ONLY IF THE 1706 SERIAL NUMBER IS UNDER 325 AND DOES NOT HAVE FCO 24763 INSTALLED.

CONTROL DATA	TITLE	PRODUCT
	DEVELOPMENT DIVISION	1706 SCANNER DETAIL INCLUDING SWITCH
	DATE	REV.
	C 60165700	6
	PAGE	1-5.0



NOTE:
 ① THIS PAGE APPLICABLE ONLY IF FCO 24763 IS INSTALLED OR IF THE 1706 IS SERIAL 325 OR HIGHER.

CONTROL DATA		TITLE		PRODUCT	
DEVELOPMENT DIVISION		SCANNER DETAIL INCLUDING SWITCH		1706	
SIZE	DRAWING NO	REV			
C	60165700	G			
SHEET	PAGE				
	1-5.1				

RECEIVER AND TRANSMITTER CONTROL SIGNALS

TABLE 1-1. CONTROL SIGNALS

SIGNAL	DEFINITION
Read	A "1" signal from the computer to the peripheral equipment initiating an input transfer of one data word.
Write	A "1" signal from the computer to the peripheral equipment initiating an output transfer of one data word.
Reply	A "1" signal from the peripheral equipment to the computer in response to a computer Read or Write signal. The Reply drops after the Read or Write signal drops.
Reject	A "1" signal from the peripheral equipment in response to a computer Read or Write signal indicating that the operation cannot be performed.
Master Clear	A "1" signal from the computer to clear the I/O channels and peripheral equipment.
Program Protect	A "1" signal from the computer to the peripheral equipment indicating that the data transfer is initiated by an instruction whose Program Protect bit is set.
Character Input	A "1" signal from the peripheral equipment to the computer during a Direct Input instruction transferring a lower 8-bit character into the lower 8 bits of the A register without disturbing the upper 8 bits.
Priority	A "1" signal from the BDC to the computer to obtain exclusive access to storage.
Buffer Active	A "1" output from the BDC to the peripheral equipment indicating that the BDC is in either a Buffered Input or Buffered Output operation.
Timing Pulse	A pulse from the computer to the BDC indicating that the computer is running.
W=0	A signal from the computer to the peripheral equipment enabling the operation of the peripheral equipment. (Peripheral equipment may be accessed through either the A/Q channel or the BDC. A W=0 signal is needed to enable peripheral equipment. The BDC uses the W field for selecting an operation and therefore cannot transmit a W=0 in a conventional method. The BDC gains access to the peripheral equipment by transmitting a signal that the peripheral equipment recognizes as a W=0 signal. This is accomplished by feeding Q15 to the Q transmitter at location F09.)

The block diagram in Figure 1-1 illustrates the transmission of control signals between the computer, the BDC, and the peripheral devices. It includes all the modules on page 1-7 except the storage receiver module at location F02. That portion of the storage receiver senses for a Program Protect fault. If a violation of the Program Protect system has occurred, storage returns a signal to the storage receiver which in turn transmits the signal to the control module at location B13 on page 1-9. Here the signal sets the Program Protect Fault FF.

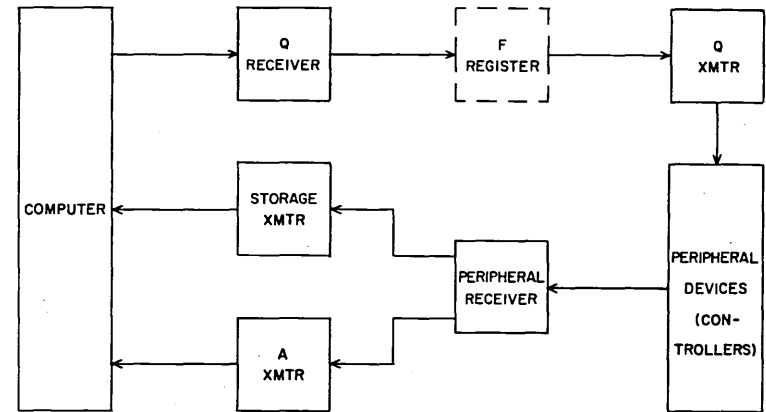
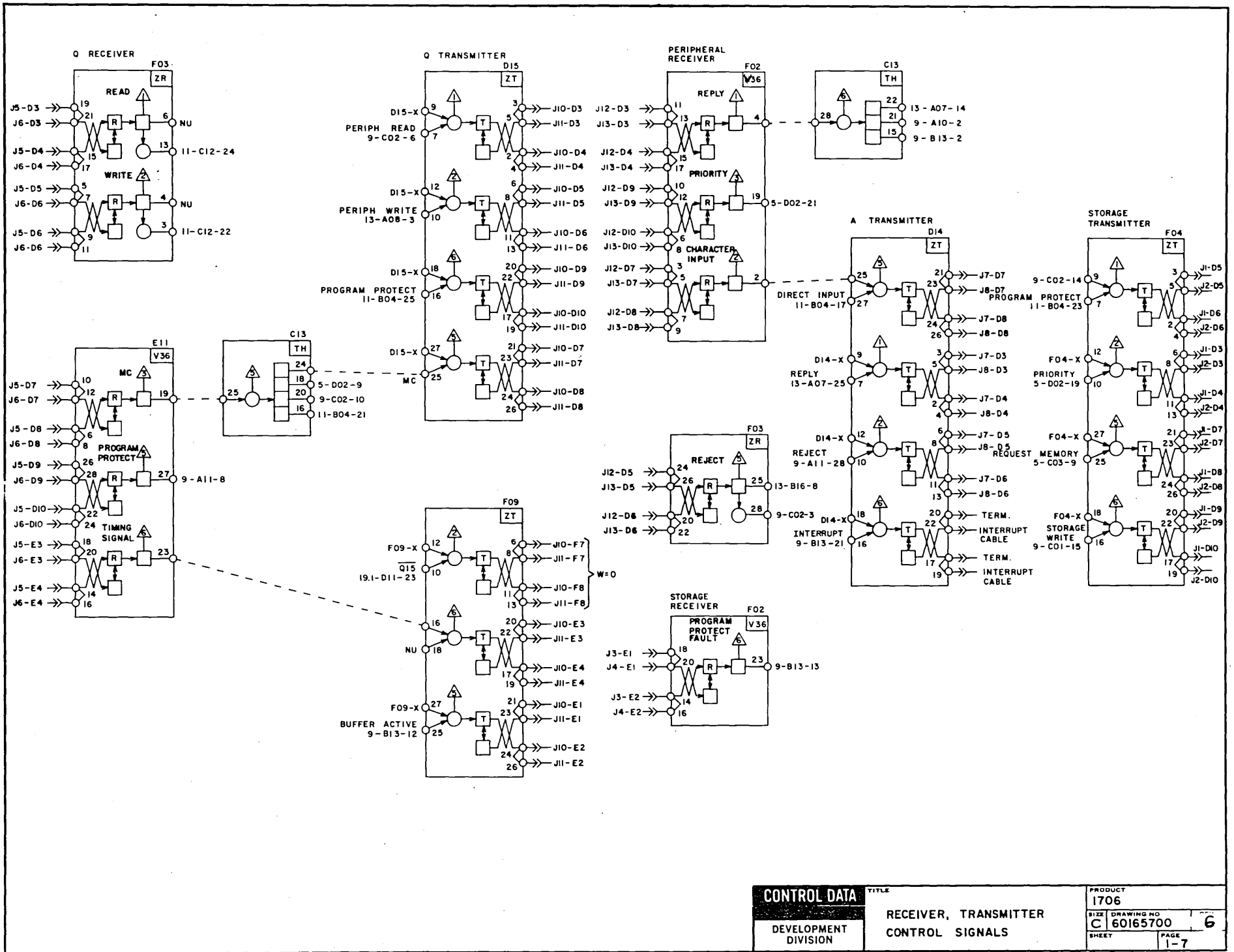


Figure 1-1. Control Signal Transmission



CONTROL DATA

TITLE

RECEIVER, TRANSMITTER
CONTROL SIGNALS

DEVELOPMENT
DIVISION

PRODUCT
1706

SIZE DRAWING NO
C 60165700

6

SHEET

PAGE
1-7

STATUS AND PERIPHERAL READ/WRITE CONTROL

The Z58 module contains the logic that controls BDC status. Table 1-2 defines the status bits that are represented in the logic by the corresponding FFs on the Z58 module.

The Buffer Active FF provides a signal to the BDC indicating that a buffered operation is in progress, but this signal is not a part of BDC status. The FF is cleared after the last Reply of the buffered operation,

Inputs to pins 15, 17, and 22 of the Z58 module determine the BDC Function operation. The only function operation available on the BDC is Interrupt on End of Operation. Bits A15 and A00 have the following definitions:

- A15 { =1 set condition for "1's" in A14-A00
- =0 clr condition for "1's" in A14-A00
- A00 enables interrupt on 1706 End of Operation

TABLE 1-2. BDC STATUS BITS

A-REGISTER BIT	FF NAME	DEFINITION
15-10		Not Used
9	Device Reply	Indicates that the peripheral device accepted the last data word transfer.
8	Device Reject	Indicates that the peripheral device rejected the last data word transfer.
7		Not Used
6	Program Protect Fault	Indicates that the reference to computer storage caused a Program Protect fault.
5		Not Used
4	End of Operation	Indicates that the buffered I/O transfer has been completed.
3		Not Used
2	Interrupt	Indicates the end of a buffered operation.
1	Busy	Indicates that BDC is busy. (This bit is set from the time the BDC accepts an output word from the computer initiating a block transfer until the block transfer is terminated, or during a direct operation.)
0	Ready	Indicates that the power is on.

READ/WRITE CONTROL

The Z96 module contains the control FFs for Read/Write operations.

The Peripheral Read FF is set during a Buffered Input operation. If a Reply signal is returned, the output of inverter C will gate the Read signal out to pin 6 (see Figure 1-2). A Reject will input a "0" on pin 3 and block the Read signal. The Reject signal does not clear the Read FF. The Read FF is cleared by Reply + Exit.

In a Direct Input the Read signal is fed to pin 4 and the resulting "0" signal forces pin 6 to a Read (constant "1"). Peripheral Read FF is not set during a Direct Input.

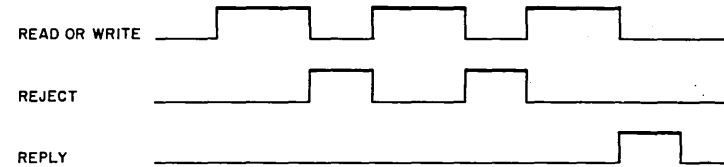


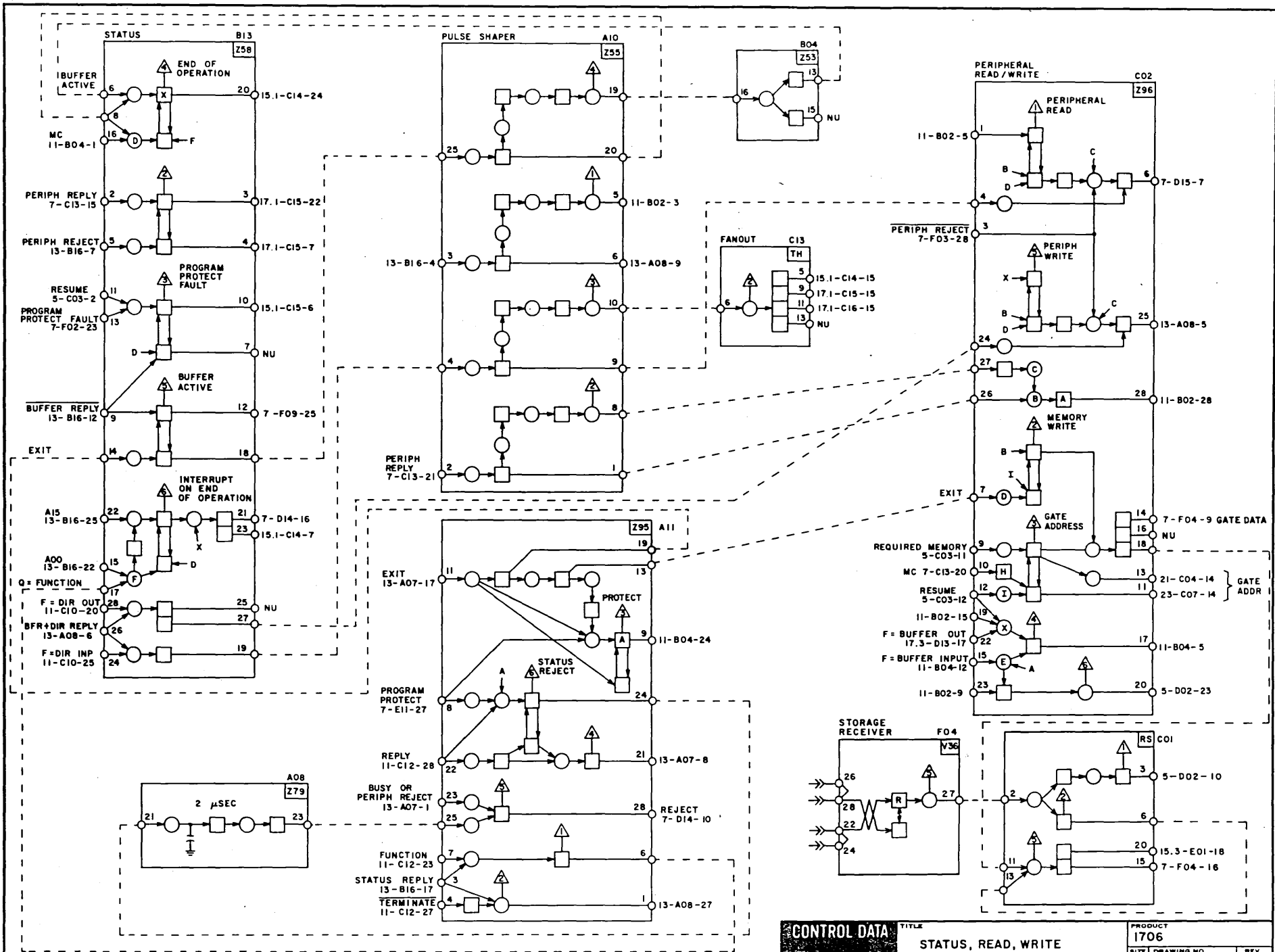
Figure 1-2. Read/Write Timing

The Peripheral Write FF is set during a Buffered Output operation and the oscillating output of pin 25 is identical to that of pin 6 with the Write pulse replacing the Read pulse (Figure 1-2).

If data can be accepted when the Write signal rises, data is transferred to the appropriate register, and within 4 usec a Reply signal is returned to BDC. The Reply signal drops when the Write signal drops.

During a Buffered Input operation the Memory Write FF is set. This output is ANDed with the set-side output of the Gate FF which enables data to be written into storage. The Gate FF being set also gates address information on the address cable.

The Z55 module is a time delay module that functions as a pulse shaper.



STORAGE ADDRESS, W TRANSLATOR, F REGISTER CONTROL SIGNALS

The storage address control module contains the logic for monitoring the address in buffered I/O operations.

During the first cycle of a buffered operation, the Buffered Reply signal sets the Fetch Control Word FF, indicating to the BDC that the current word being transferred is a control word and not a data word. These same conditions set the Change Storage Address FF which enables the contents of the A register to be transferred to the Storage Address register. The contents of the Storage Address register is then the FWA-1 of the block of data being transferred. The contents of the FWA-1 is the control word (LWA+1) and is stored in the Storage Hold register where it is compared to the current address during each cycle of the buffered operation.

During each succeeding cycle of the buffered operation, the Change Storage Address FF sets and enables the current address to be incremented by one. The Fetch Control Word FF sets only on the first cycle.

The Z56 module is part of the W translator, the other being the Z6X (C11) module on page 1-19.1. The Z56 module receives inputs from the Z6X (C11) module and transmits signals representing the translated BDC operation.

Bit 15 of the BDC address in the Z56 module is the continue bit.

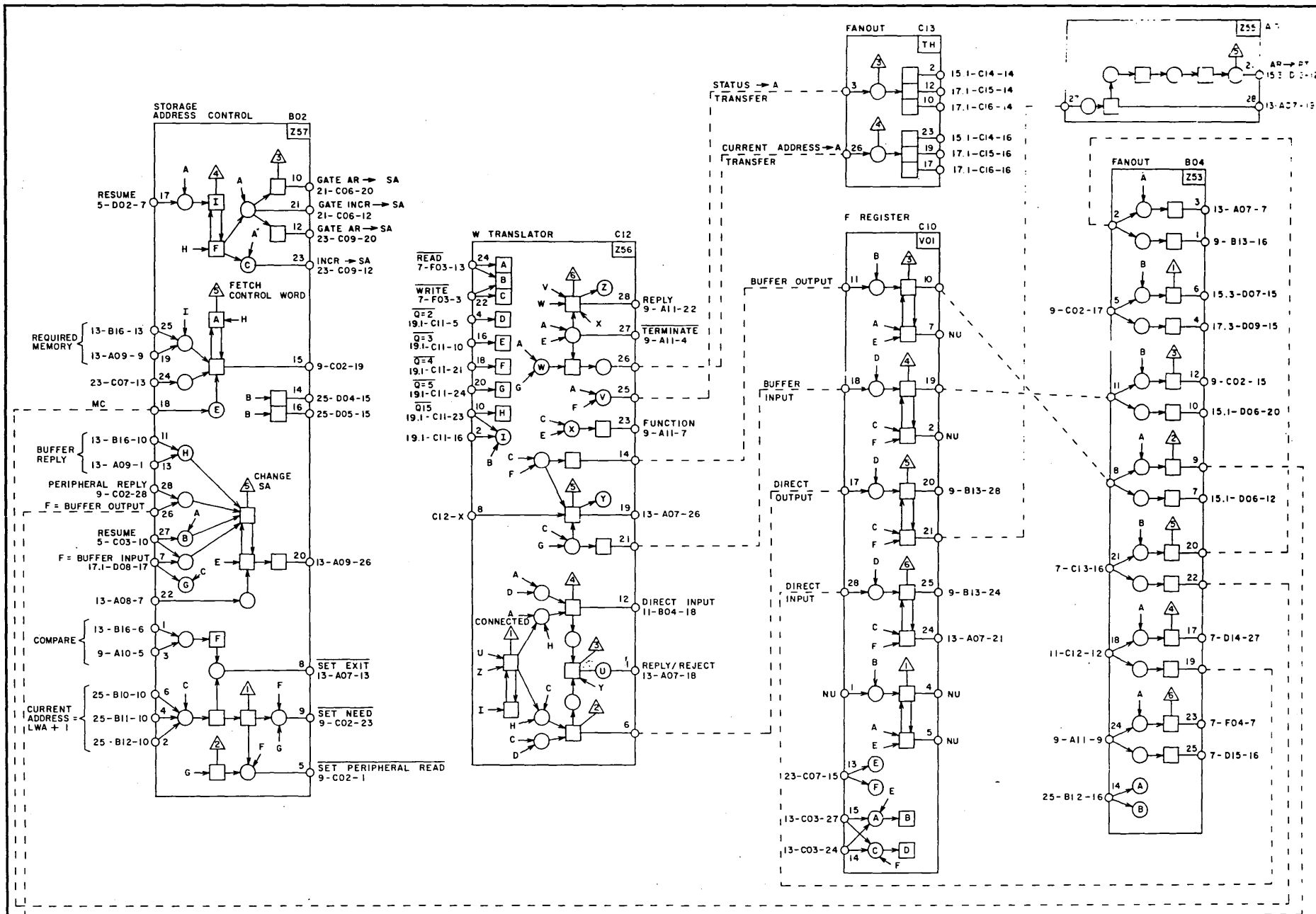
The BDC may be addressed using the continue bit. The continue bit operates as follows:

- 1) Address the device with the correct code and Q15 will set to "0".
- 2) All successive addresses with Q15 = 1 will be recognized by that device.
- 3) To access a different device, use the new address with Q15 = 0.

The BDC will interpret an access with Q15 = 1 as a Direct Input on a Read and a Direct Output on a Write.

The V01 module is a portion of the F register. This register holds the operation code that was translated in the W translator module.

The TH and Z53 modules are fan-out modules.



REPLY AND REJECT CONTROL

The Reply/Reject Z59 module contains the logic that senses the operating state of the BDC. It generates Reply, Reject, and Exit Control signals, and the status Busy signal.

To perform a buffered or direct operation, the appropriate address is transmitted via the A/Q channel to the BDC. The address is translated and its signal is ANDed with a BDC Not Busy signal. The resultant signal sets the B+D (buffered or direct) Reply FF that enables the operation. If the BDC is Busy, the clear output of the B+D Reply FF transmits a Reject signal out of pin 23 of the Z59 module.

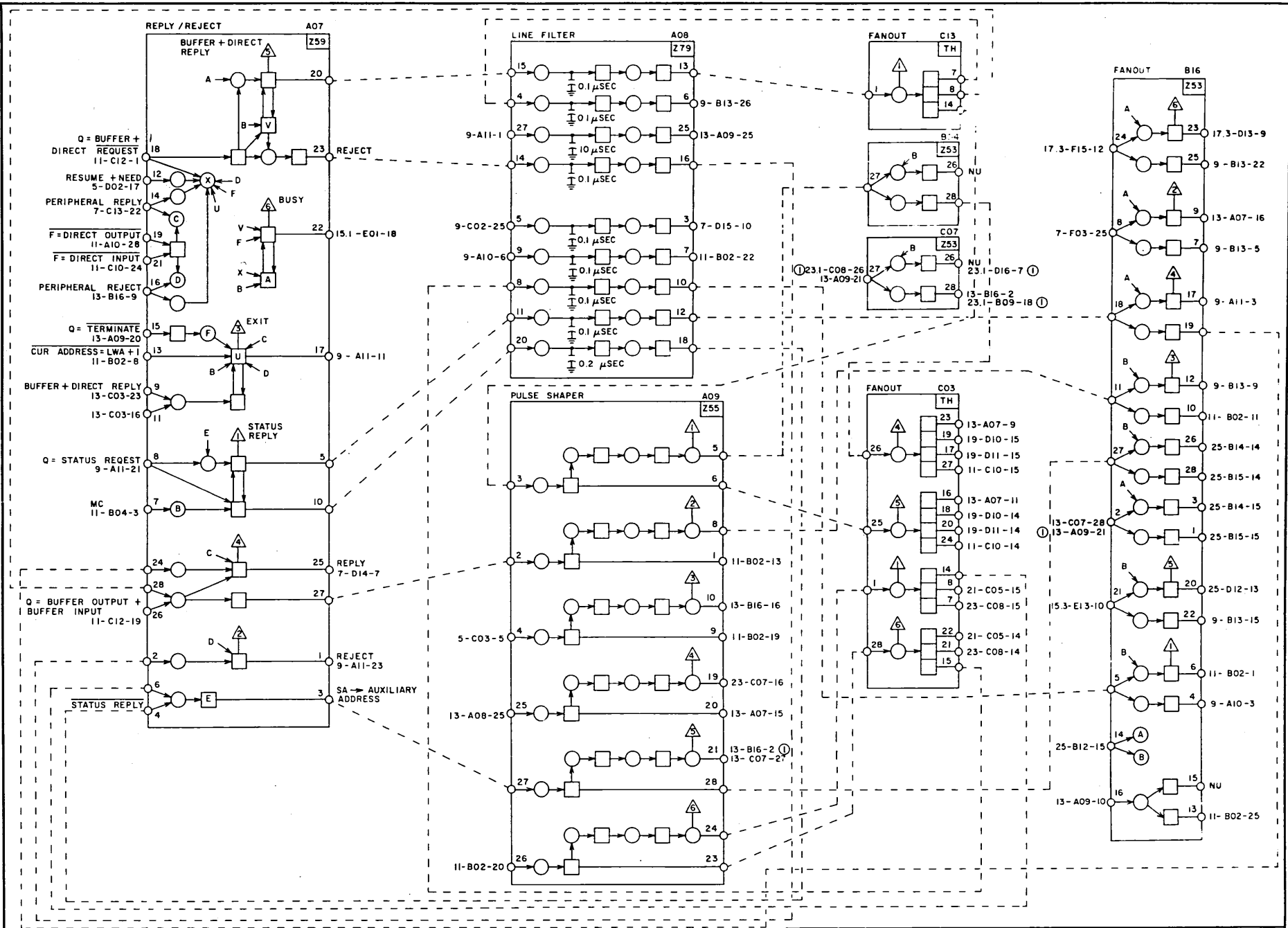
The computer requests BDC status by transmitting a W=03 (current address) or a W=04 (1706 Status). The W=03 or W=04 translation will gate the data to the A register of the computer (page 1-11, module C12). The BDC will respond to the status request within 4 microseconds with either a Reply or Reject. If a Reject occurs, there is a protect fault or the 1706 is not physically connected to the computer.

One of the bits associated with BDC status is the Busy signal controlled by the Busy FF. This FF sets at the beginning of a buffered, direct, or terminate operation and remains set until the operation is complete.

The Exit FF provides a signal to the BDC indicating completion of a buffered, direct, or terminate operation.

The Z79 module functions as a line filter, removing noise and transients from the various signals.

The Z53 and TH modules operate as fan-out modules. The Z55 module is a time delay module that functions as a pulse shaper.



NOTE:

① PERTAINS ONLY IF STANDARD OPTION FV430-A IS INSTALLED.

CONTROL DATA
CORPORATION
DEVELOPMENT
DIVISION

TITLE
REPLY, REJECT CONTROL

PRODUCT
1706
SIZE DRAW NO. N.
C 60165700
SHEET PAGE 1-13

DATA TRANSMITTER, DATA RECEIVER, X REGISTER BITS 00-07

The block diagram in Figure 1-3 illustrates the data flow (bits 00-07) in the 1706-A.

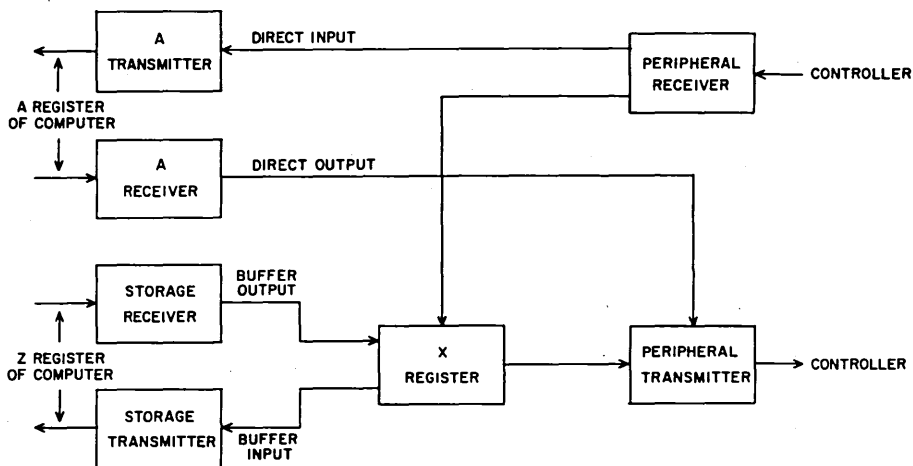


Figure 1-3. Data Flow in BDC

Data from the controllers enters the peripheral receiver (locations F10, F11, and F12). If the BDC is in a Direct Input operation, the data from the peripheral receiver enters a fan-in (locations C14 and C15), and is transferred to the A

transmitter (locations E13, E14, and E15). The data is then transmitted via the A/Q channel to the A register of the computer.

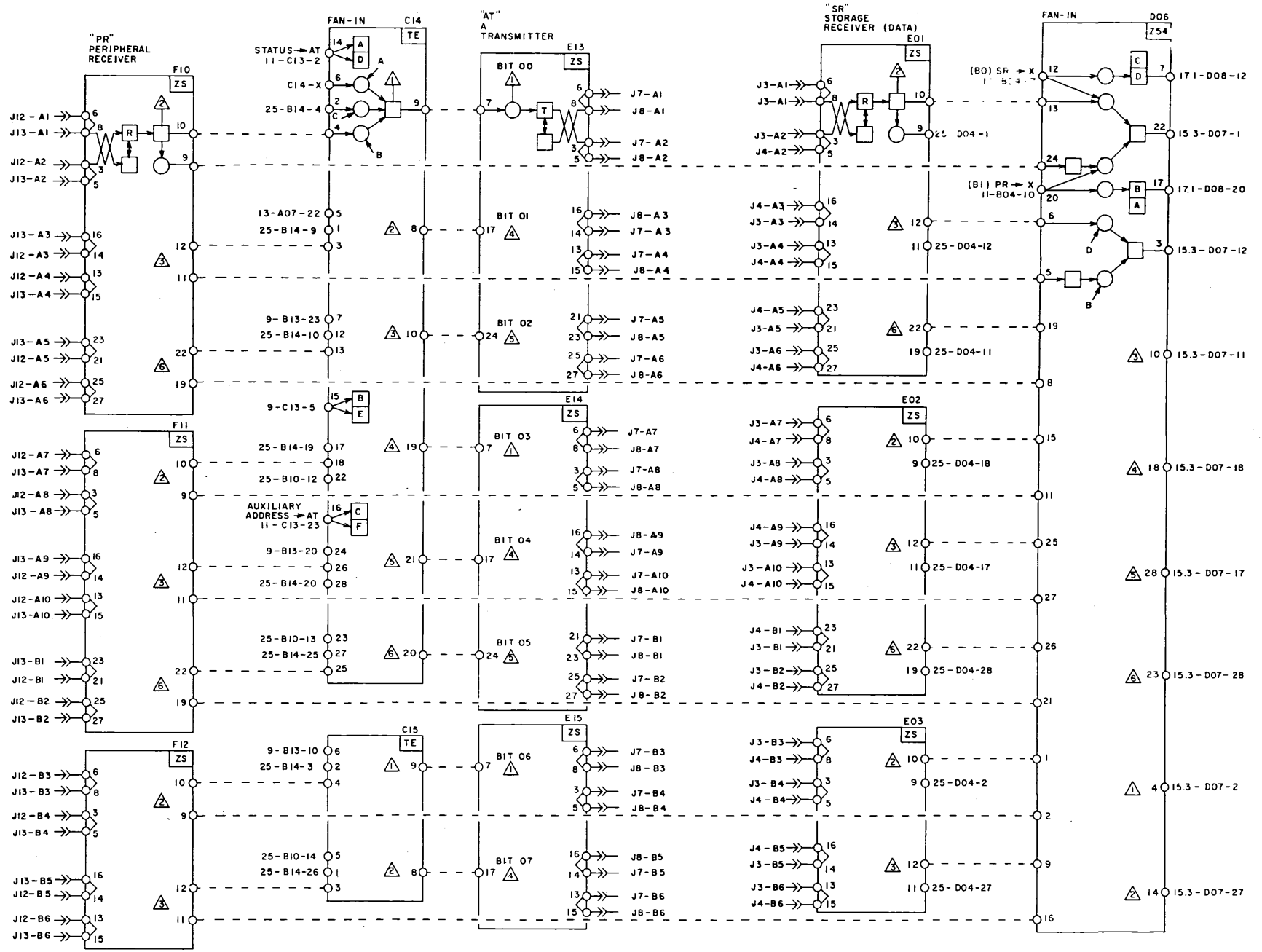
During a Buffered Input, the data from the peripheral receiver is gated into a fan-in (location D06). The output from this fan-in is transmitted to the X register (location D07) where it is held until the BDC has access to memory.

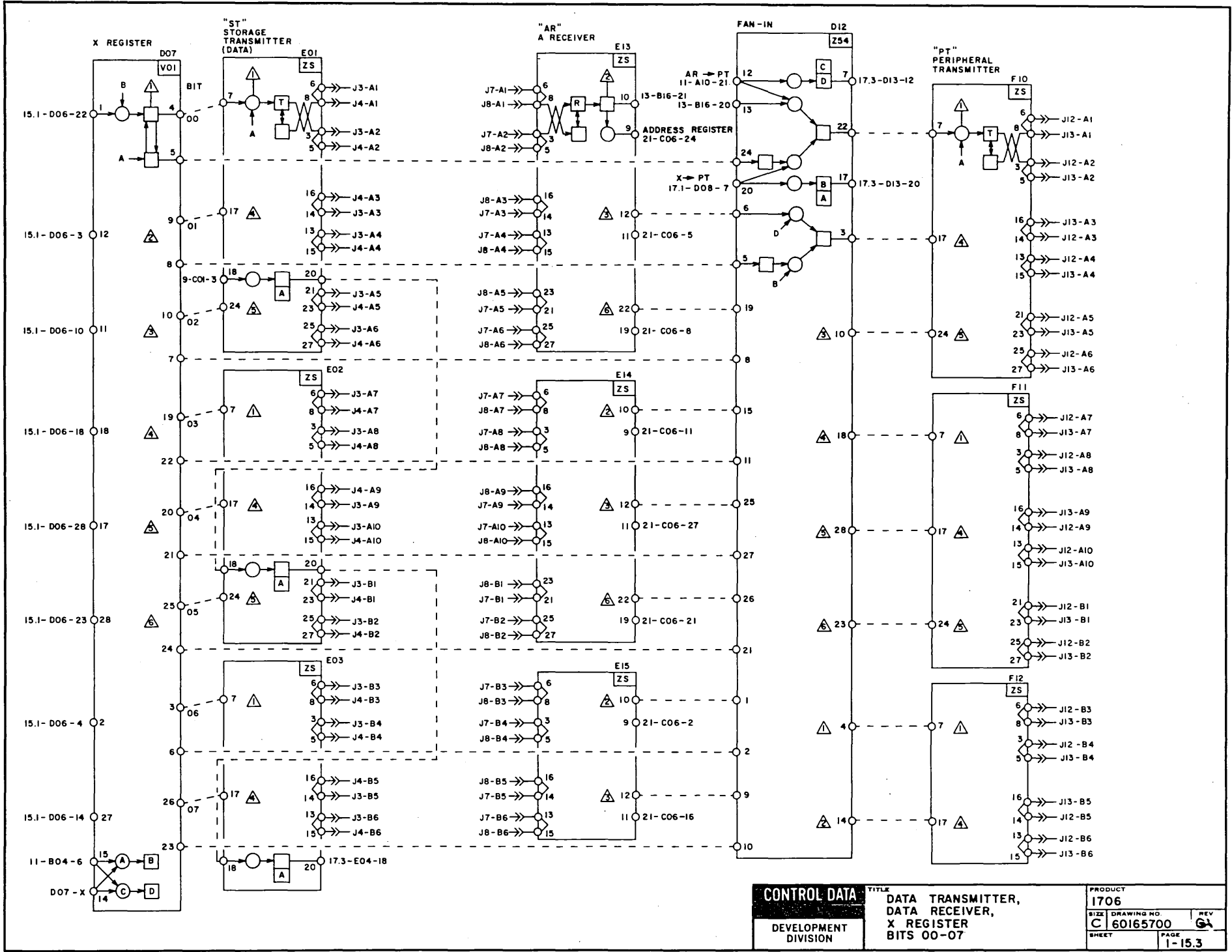
During a Buffered Input operation, data is gated from the X register to the storage transmitter (locations E01, E02, and E03) and then to storage.

During a Buffered Output operation, data is gated from the X register to a fan-in (location D12), to the peripheral transmitter (locations F10, F11, and F12), and then to the controllers.

The storage receiver (locations E01, E02, and E03) accepts data from storage and transmits it to a fan-in (location D06) and then to the X register during a Buffered Output operation.

The A receiver (locations E13, E14, and E15) receives data from the A register of the computer. It transmits the data to the peripheral transmitter via a fan-in (location D12) and then to the controllers.





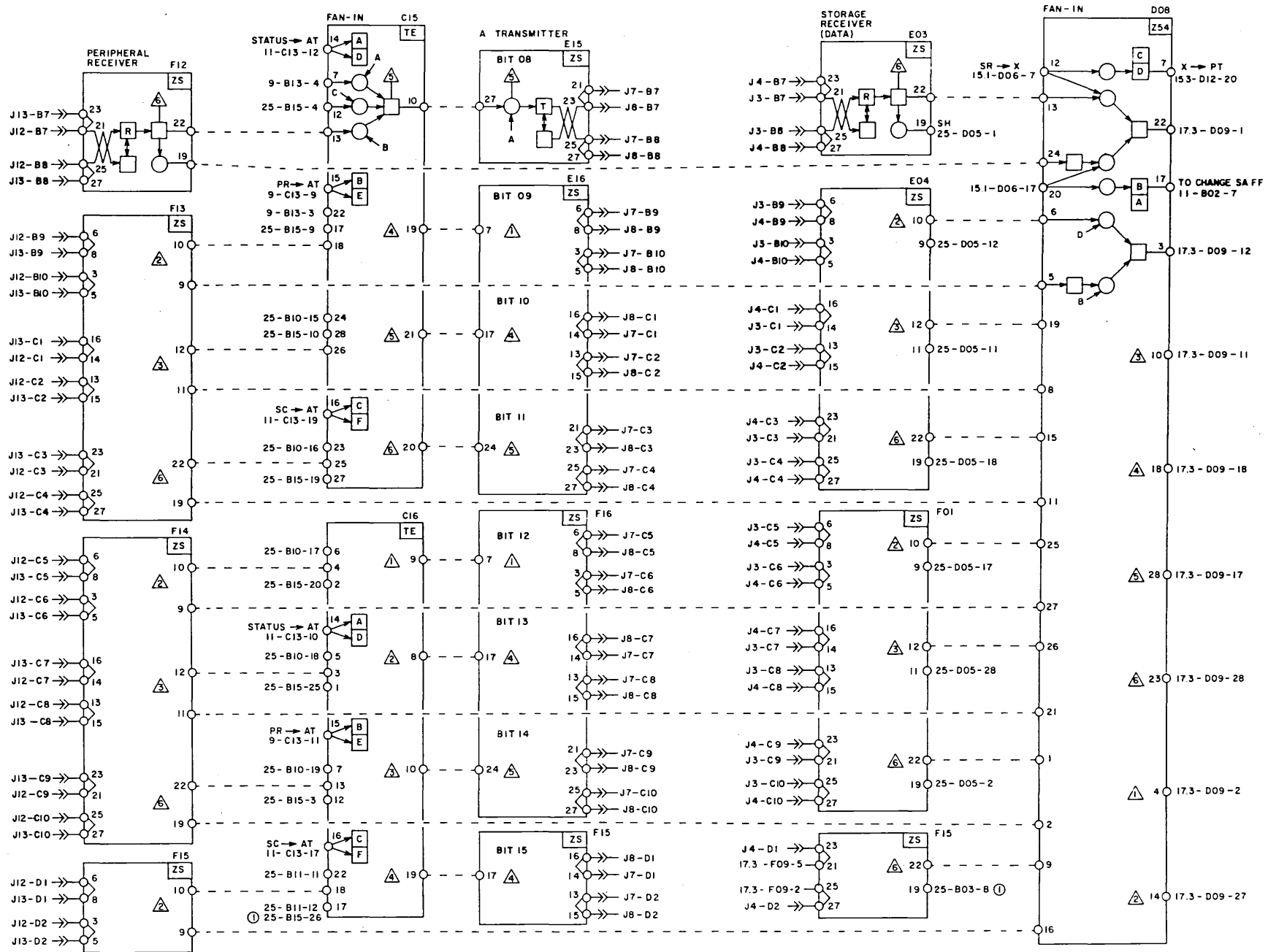
CONTROL DATA
DEVELOPMENT DIVISION

TITLE
DATA TRANSMITTER,
DATA RECEIVER,
X REGISTER
BITS 00-07

PRODUCT 1706		REV GA
SIZE C	DRAWING NO. 60165700	PAGE 1-15.3
SHEET	PAGE	

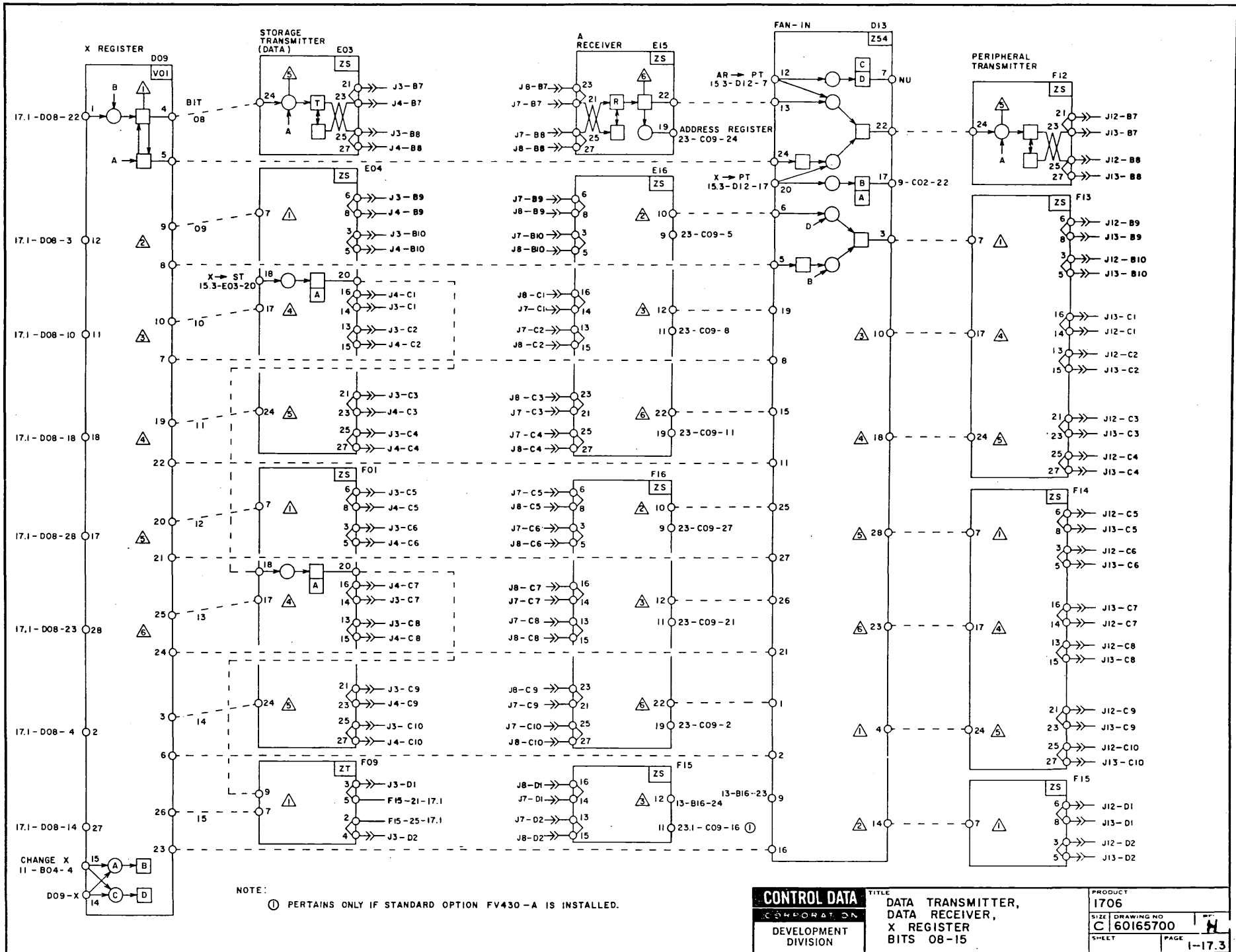
DATA TRANSMITTER, DATA RECEIVER, X REGISTER BITS 08-15

The logic diagrams on pages 1-17.1 and 1-17.3 show bits 08-15 of data flow in the BDC. The logic involved in bits 08-15 is identical to that in bits 00-07 shown on pages 1-15.1 and 1-15.3.



NOTE:
 ① PERTAINS ONLY IF STANDARD OPTION FV430-A IS INSTALLED.

CONTROL DATA CORPORATION	TITLE	PRODUCT
	DATA TRANSMITTER, DATA RECEIVER, X REGISTER BITS 08-15	1706
DEVELOPMENT DIVISION	SIZE	DRAWING NO
	C	60165700
	SHEET	PAGE
		1-17.1



NOTE:
 Ⓢ PERTAINS ONLY IF STANDARD OPTION FV430-A IS INSTALLED.

CONTROL DATA CORPORATION	TITLE	PRODUCT
	DATA TRANSMITTER, DATA RECEIVER, X REGISTER BITS 08-15	1706
DEVELOPMENT DIVISION	SIZE DRAWING NO.	C 60165700
	SHEET	1
	PAGE	1-17.3

Q RECEIVER, Q TRANSMITTER, W TRANSLATOR, F REGISTER

The logic diagram on page 1-19.1 shows the Q receiver, the F register, the W translator, and the Q transmitter. The block diagram in Figure 1-4 illustrates the flow through these modules. The Q receiver receives the contents of the Q register via the address cable and transmits it to the F register and the W translator. The F register temporarily stores the address (contents of the Q register). The W translator translates the W field (bits 11-15) of the address. The Q transmitter transmits the address to the controller.

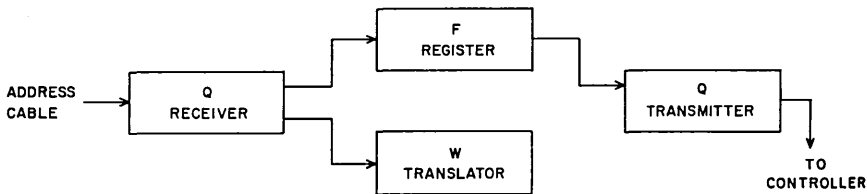


Figure 1-4. BDC Address Flow

The format of the address in the W field of the Q register which directs BDC operation is shown in Figure 1-5. The address consists of two digits (5 bits) with the left digit (bit 15) in binary and the right digit (bits 11-14) in hexadecimal.

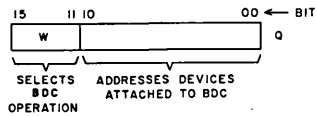


Figure 1-5. I/O Address Format

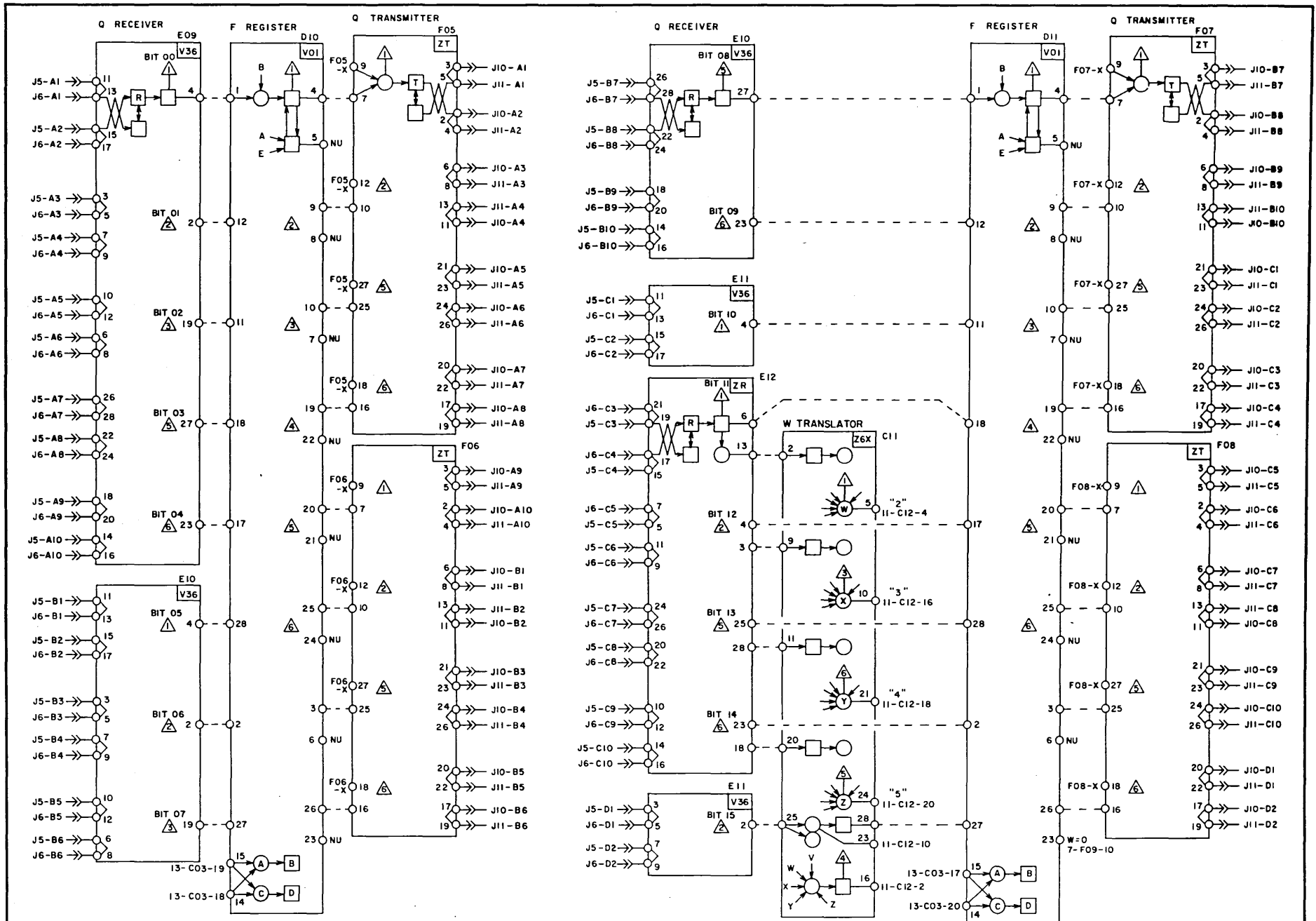
Table 1-3 lists the addresses and the corresponding operations for the BDC.

TABLE 1-3. 1706-A ADDRESSES AND OPERATIONS

W TRANSLATOR ADDRESS			COMPUTER OPERATION	
1706 No. 3	1706 No. 2	1706 No. 1	INPUT	OUTPUT
0C	07	02	Direct Input	Direct Output
0D	08	03	Terminate Buffer; 1706 Current Address	Function
0E	09	04	1706 Status	Buffered Output
0F	0A	05	1706 Current Address	Buffered Input

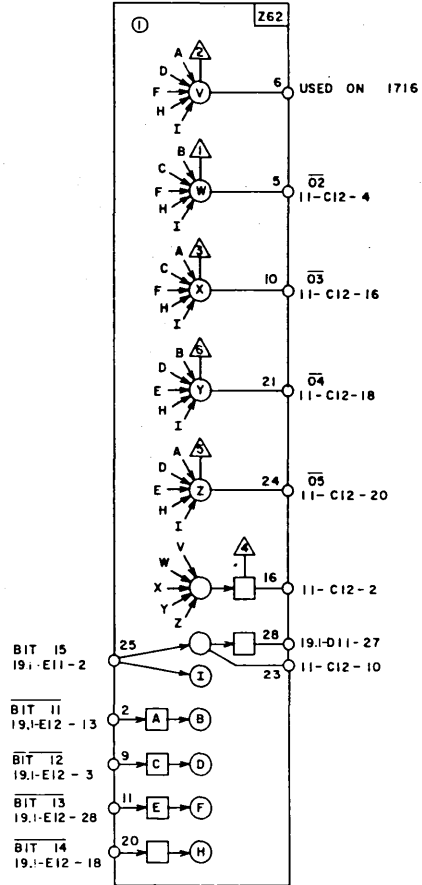
Bit 15 of the address which enters the V36 module at Location E11 is the continue bit. This is explained on page 1-10.

The W translator may be one of three types of modules. A Z62, Z63, or Z64 module is used depending on whether the 1706 is a number one, two, or three 1706. In the logic diagram the Z6X module is used to represent one of the three types of modules. (See page 19.3 for logic schematics.)

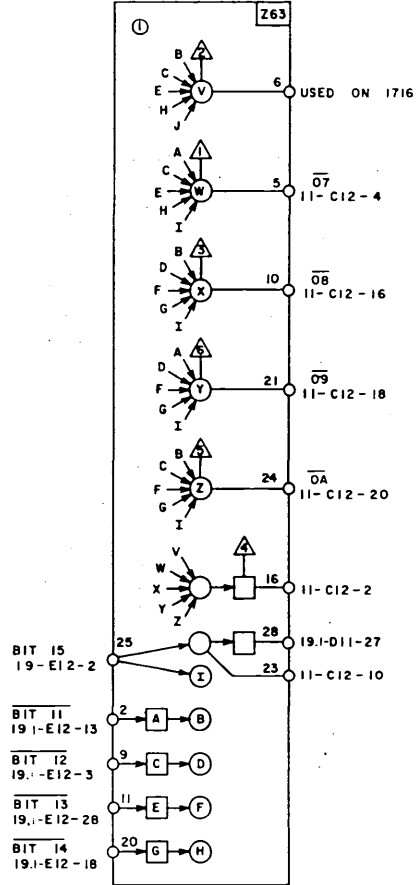


CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE RECEIVER, TRANSMITTER, W TRANSLATOR, F REGISTER BITS 00-15	PRODUCT 1706
		SIZE DRAWING NO. C 60165700
		REV. D
		SHEET PAGE 1-19.1

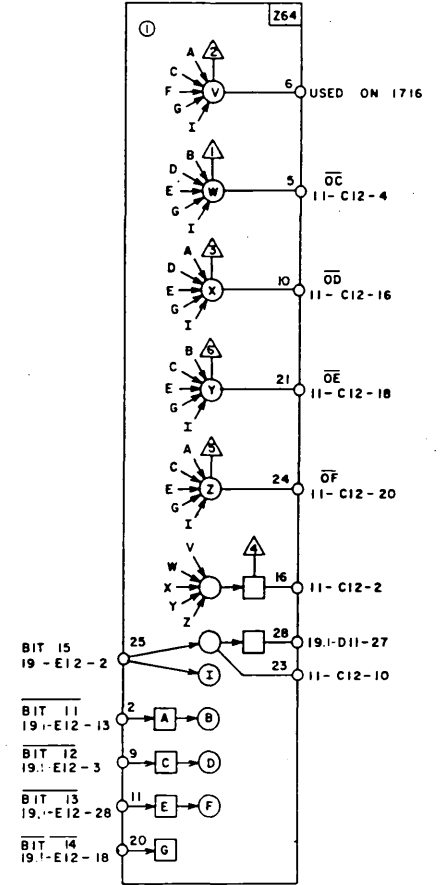
1706 NO 1



1706 NO 2



1706 NO 3



NOTE:
① W CODES ARE ON P. 1-18.

CONTROL DATA DEVELOPMENT DIVISION	TITLE W TRANSLATOR Z62, Z63, Z64	PRODUCT 1706
	SIZE C 60165700	REV.
SHEET		PAGE 1-19.3

INCREMENTER, STORAGE ADDRESS REGISTER, AND STORAGE TRANSMITTER ADDRESS BITS 00-07

The logic diagrams on pages 1-21 and 1-23 illustrate the logic associated with incrementing, storing, and transmitting of storage addresses. The block diagram in Figure 1-6 illustrates this sequence.

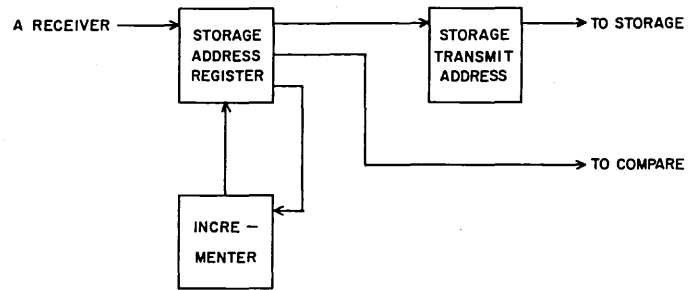


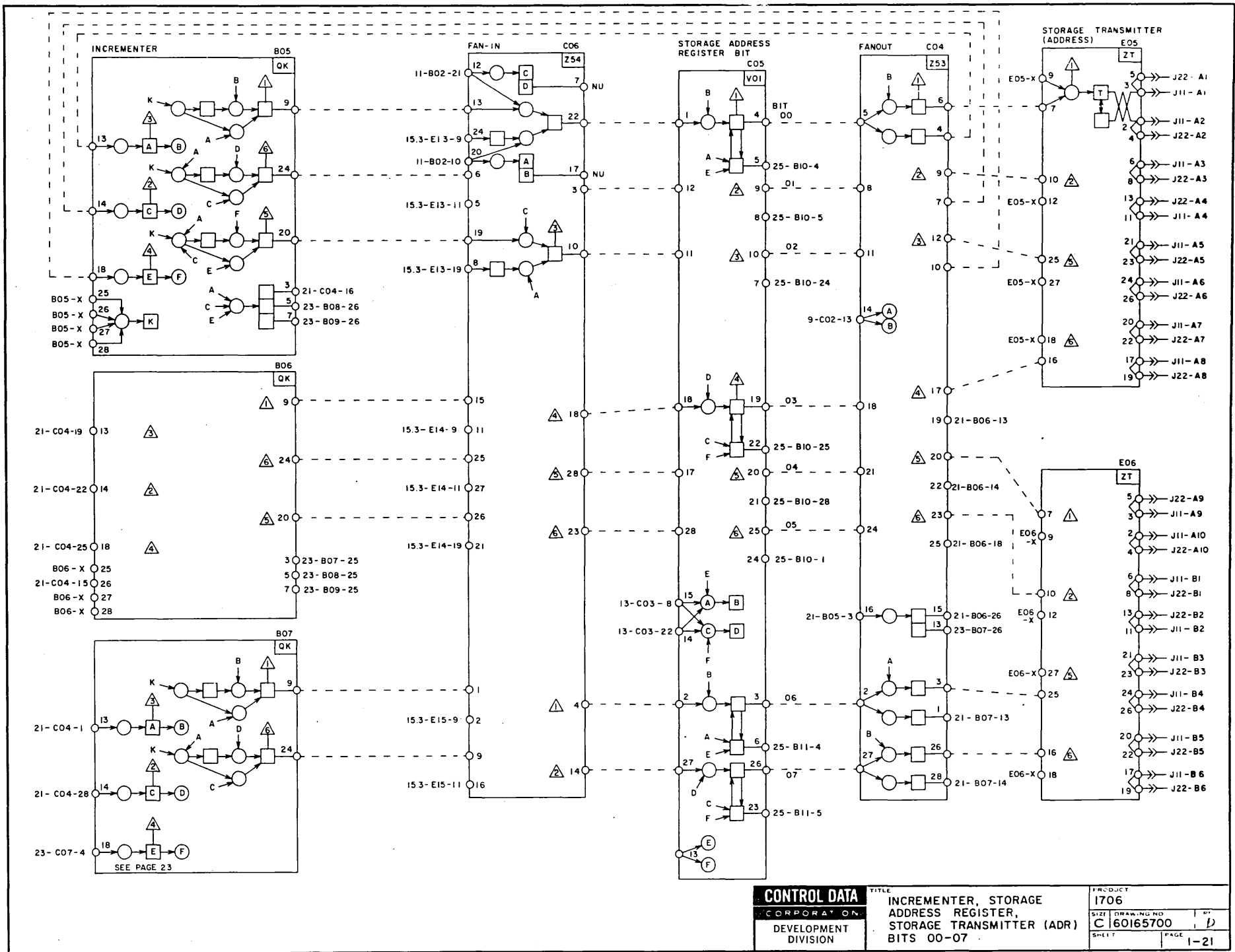
Figure 1-6. Incrementer Network

During the first cycle of a buffered operation, the fan-in receives the FWA-1 from the A receiver. (The contents of FWA-1 is the LWA+1.) The FWA-1 is sent to the Storage Address register where it is gated to the fan-out. The fan-out has two outputs. It transmits the address to the Storage Transmitter where it is sent to storage and it gates the address back to the incrementer to be incremented by one.

During all succeeding cycles of a buffered operation, the fan-in receives the address from the incrementer. The fan-in receives an input from the A receiver only on the first cycle.

The fan-in again gates output to the Storage Address register. The set-side outputs of the Storage Address Register FF's are applied to the fan-out and the clear-side outputs are applied to the compare module (page 1-25). The fan-out again transmits the address to the storage transmitter where it is sent to storage and gates the address back to the incrementer. This cycle continues until the current address equals the LWA+1. The compare module (page 1-25) checks for this equality.

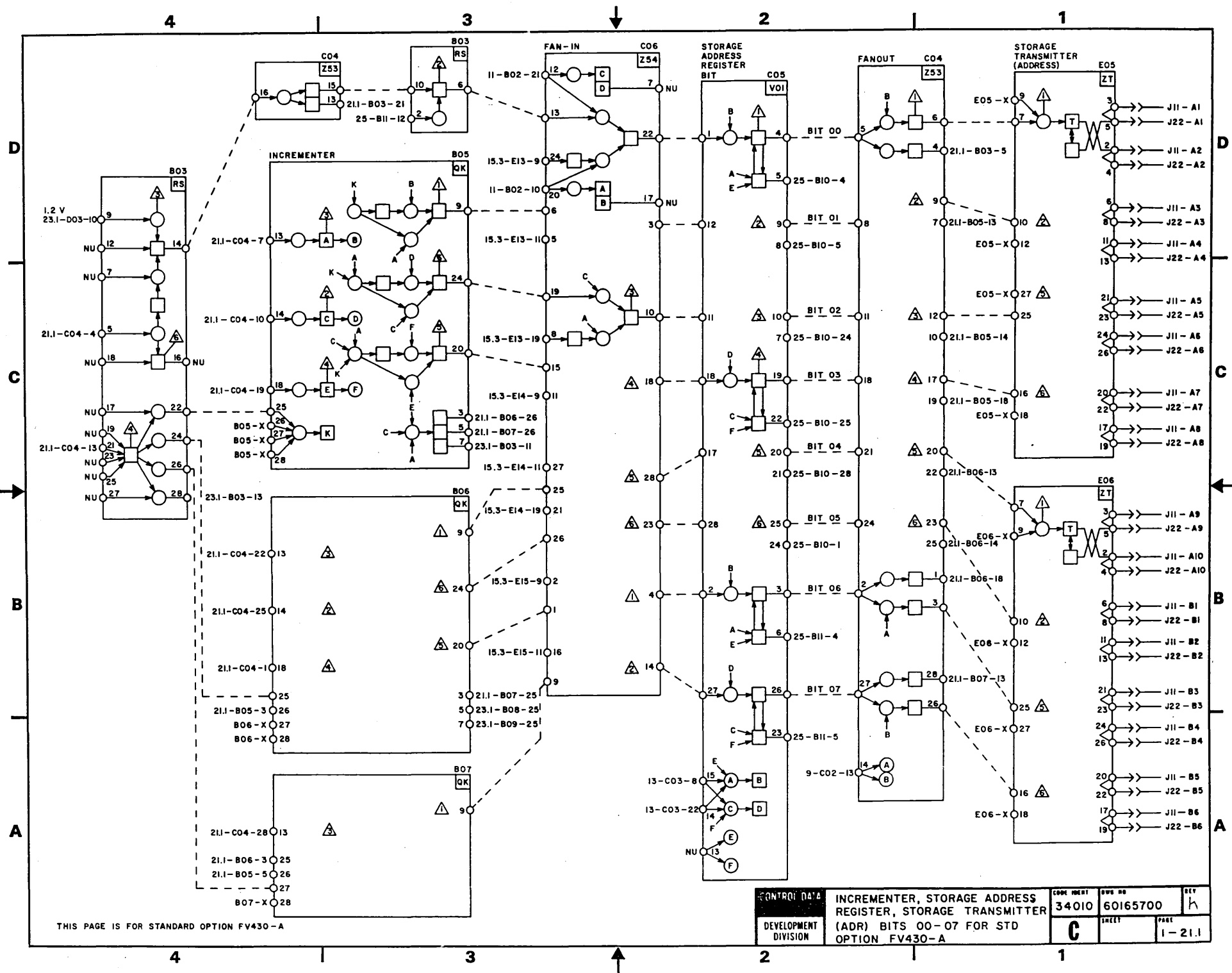
The incrementer is composed of five QK modules, each containing 3 bits of the address. The total of 15 address bits is sufficient to address any storage location. The input to pins 25 through 28 of each QK module enables a carry from one module to the next. A logical "1" from the K inverter in each QK module enables the logic of that module.



CONTROL DATA CORPORATION DEVELOPMENT DIVISION	TITLE INCREMENTER, STORAGE ADDRESS REGISTER, STORAGE TRANSMITTER (ADR) BITS 00-07	PRODUCT 1706
	SIZE C 160165700	DRAWING NO. 1
	SHEET 1	PAGE 1-21
	OF 1 OF 1	

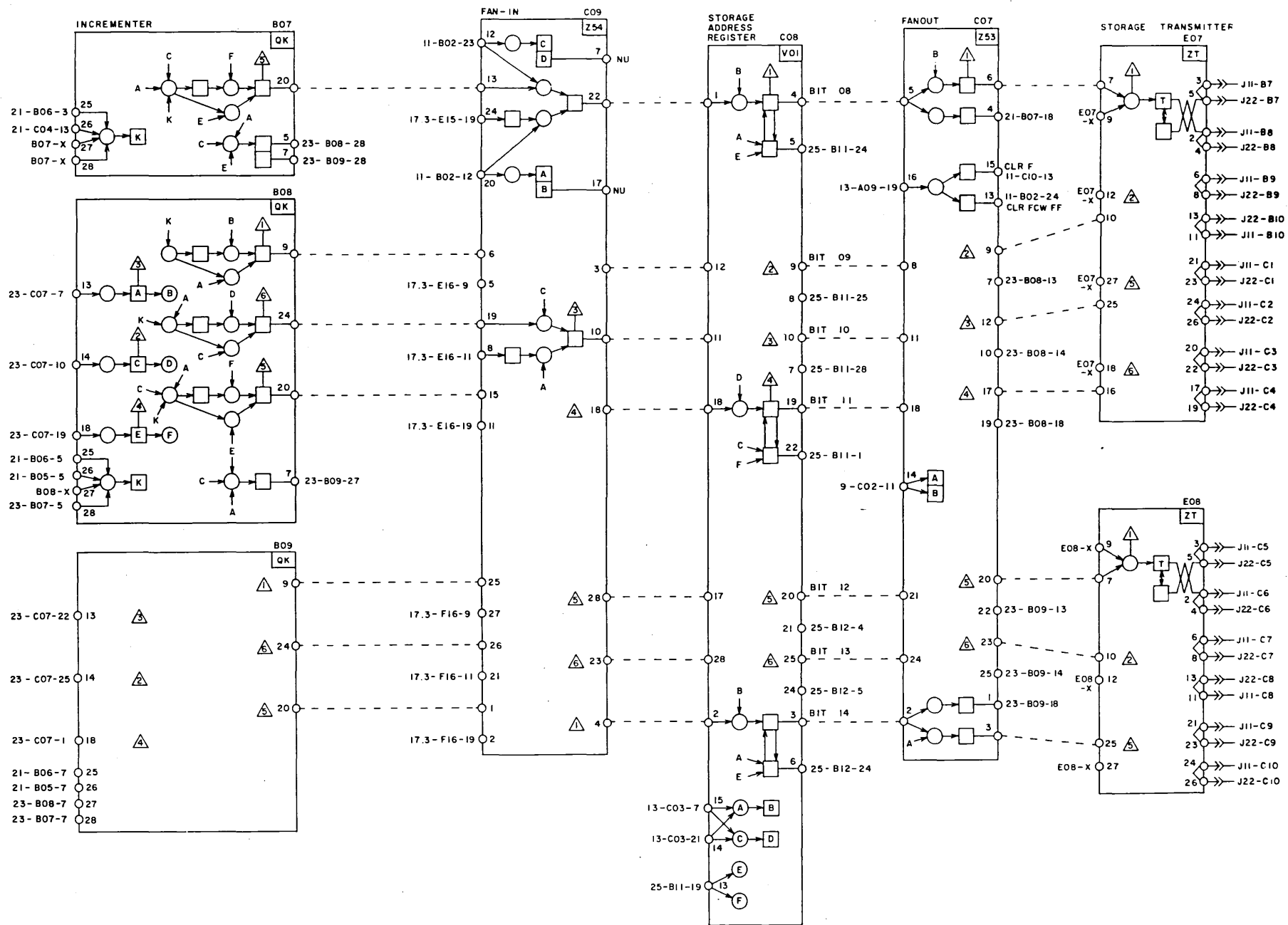
INCREMENTER, STORAGE ADDRESS REGISTER, AND STORAGE TRANSMITTER ADDRESS BITS 08-14

The logic diagram on page 1-23 shows bits 08-14 of the Storage Address register. The logic involved is identical to that in bits 00-07 shown on page 1-21.



THIS PAGE IS FOR STANDARD OPTION FV430-A

CONTROL NO. 4 DEVELOPMENT DIVISION	INCREMENTER, STORAGE ADDRESS REGISTER, STORAGE TRANSMITTER (ADR) BITS 00-07 FOR STD OPTION FV430-A	CODE IDENT	REV NO	REV
		34010	60165700	h
		SHEET	PAGE	
		C	1-21.1	



CONTROL DATA		TITLE		PRODUCT	
CORPORATION		INCREMENTER, STORAGE ADDRESS REGISTER, STORAGE TRANSMITTER (ADR) BITS 08-14		1706	
DEVELOPMENT DIVISION		DRAWING NO.		REL	
		C 60165700		P	
		SHEET		PAGE	
				1-23	

STORAGE HOLD, COMPARE, AUXILIARY ADDRESS REGISTER

The logic for the storage hold, compare, and auxiliary address register modules is shown on page 1-25. The block diagram in Figure 1-7 illustrates the flow through these modules during a buffered operation.

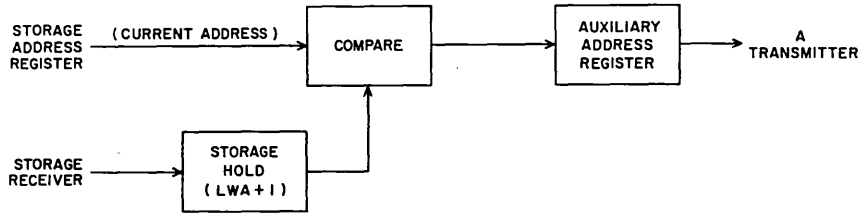


Figure 1-7. Compare Network

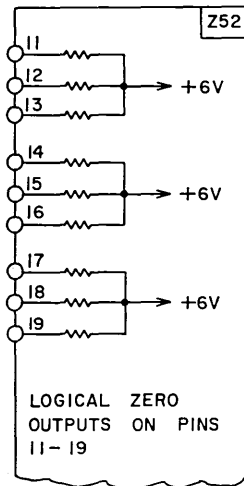
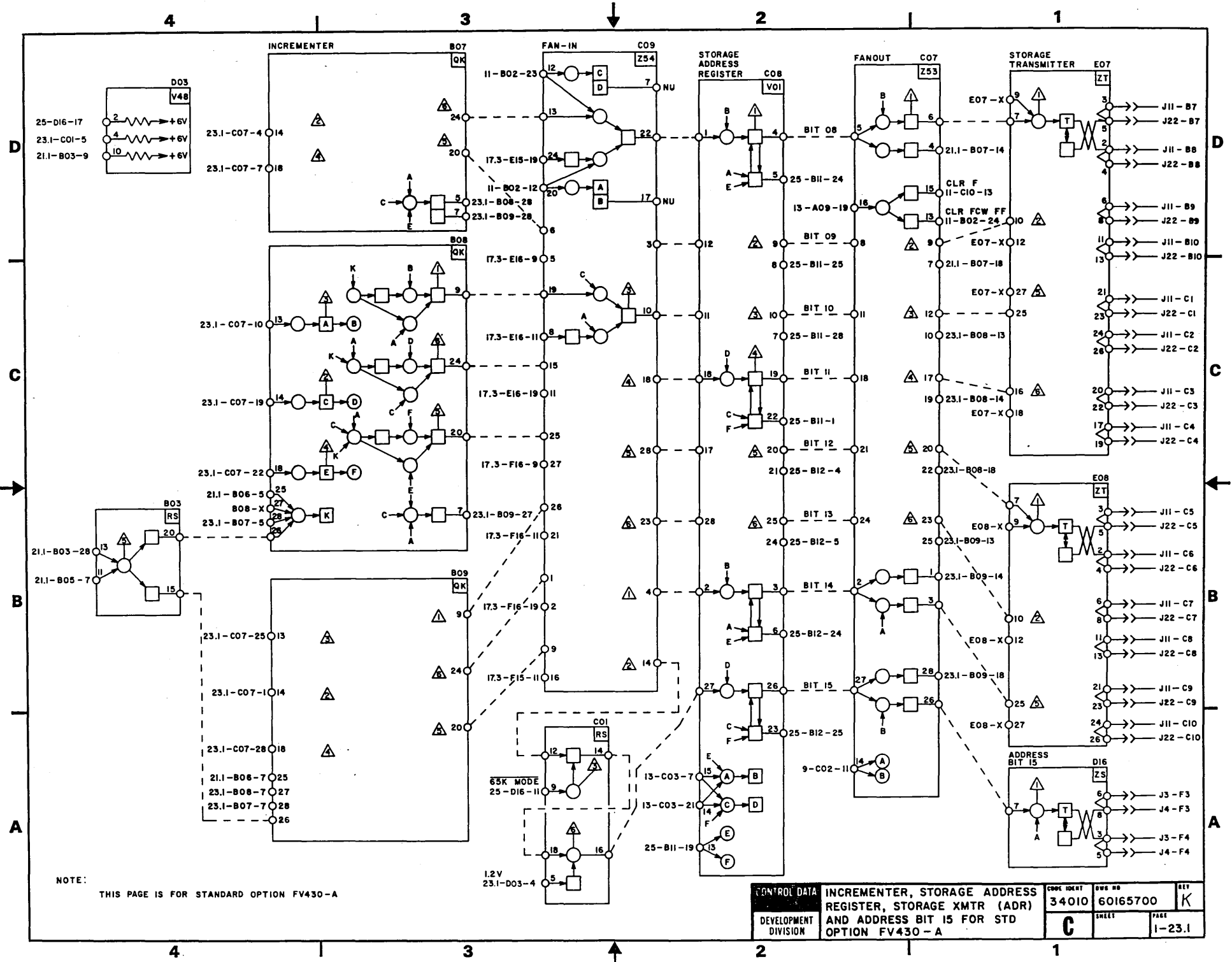


Figure 1-8. Z52 Module

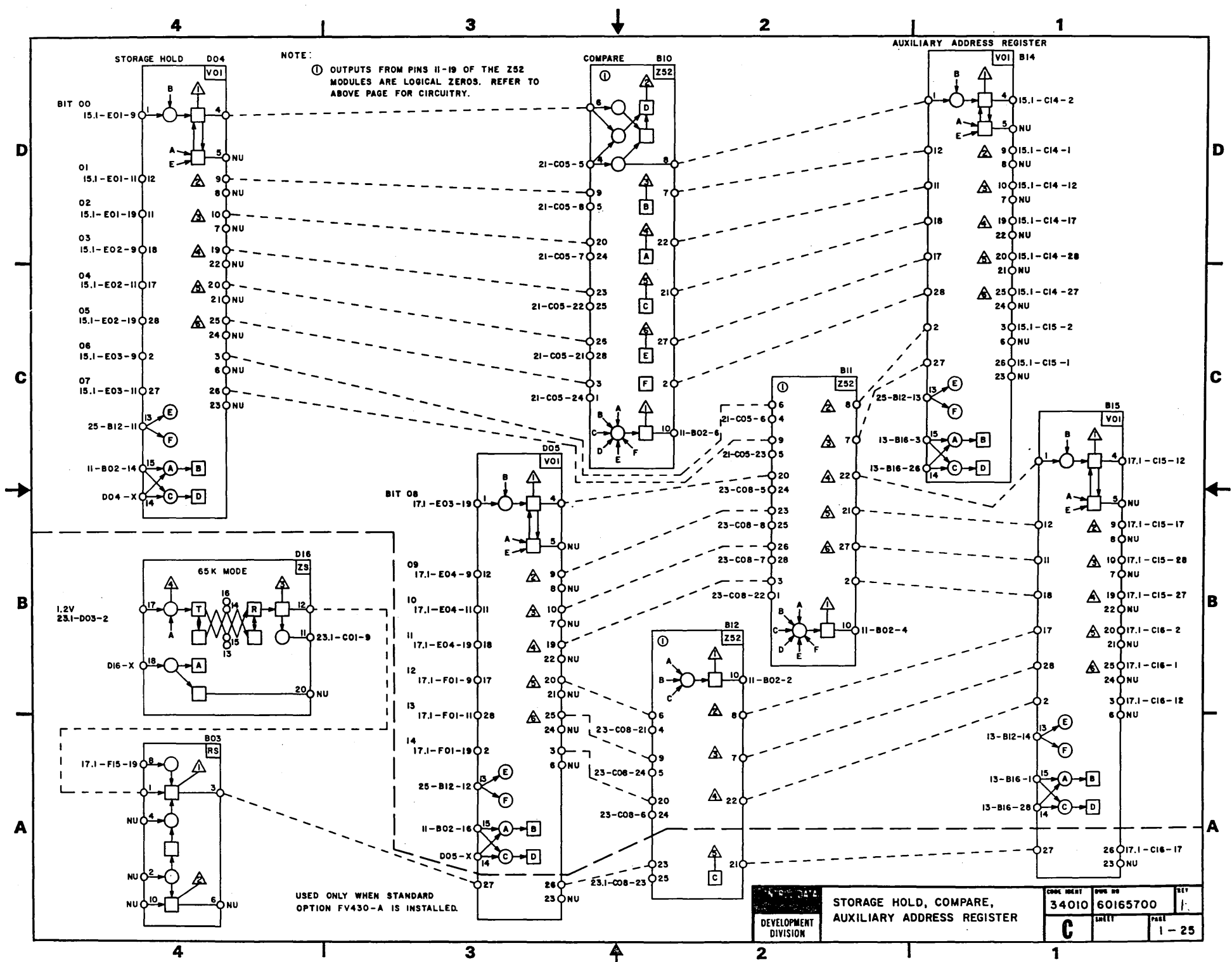
The complement of $LWA + 1$ enters the storage hold modules from the storage receiver and is then gated into the compare modules. The complement of the current address enters the compare modules from the Storage Address register (pages 1-21 and 1-23) and is then compared with the complement of $LWA + 1$. If the current address equals the $LWA + 1$, a logical "1" from pin 10 of the compare modules (locations B10, B11, and B12) is applied to the control circuitry (page 1-11) ending the buffered operation.

The Auxiliary Address register holds the current address and transmits it to the A transmitter during a Current Address operation. When the computer initiates a Current Address operation, the current address present in the Auxiliary Address register is transmitted to the computer. The incremented address that is generated during each step of the buffered operation is blocked from entering the Auxiliary Address register until the Current Address operation is completed.



NOTE:
THIS PAGE IS FOR STANDARD OPTION FV430-A

CONTROL DATA	INCREMENTER, STORAGE ADDRESS REGISTER, STORAGE XMTR (ADR) AND ADDRESS BIT 15 FOR STD OPTION FV430 - A	CODE IDENT	34010	DWG NO	60165700	REV	K
DEVELOPMENT DIVISION		C		PAGE	1-23.1		



NOTE:

① OUTPUTS FROM PINS 11-19 OF THE Z52 MODULES ARE LOGICAL ZEROS. REFER TO ABOVE PAGE FOR CIRCUITRY.

USED ONLY WHEN STANDARD OPTION FV430-A IS INSTALLED.

DEVELOPMENT DIVISION	STORAGE HOLD, COMPARE, AUXILIARY ADDRESS REGISTER		CODE IDENT	OWN NO	REV
			34010	60165700	1
			UNIT	PAGE	
			C	1-25	

INPUT

OUTPUT

INPUT				OUTPUT			
2	3	4	5	2	3	4	5
DIRECT INPUT	TERMINATE BUFFER CURRENT ADDRESS	STATUS	CURRENT ADDRESS	DIRECT OUTPUT	FUNCTION	BUFFERED OUTPUT	BUFFERED INPUT
(Q) → F	SET EXIT, BUSY	STATUS → A TRANS.	CURRENT ADDRESS → A TRANS.	(Q) → F	STROBE A REC. BIT 1: $A_{15} = 1$	BDC BUSY	BDC BUSY
PERIPH REC → A TRANS	CURRENT ADDRESS → A TRANS.	REPLY	REPLY	A REC. → PERIPH TRANS.	SET INT. FF IF $A_{15} = 1$	REJECT → COMPUTER	REJECT → COMPUTER
GATE PERIPH READ ON	REPLY			GATE PERIPH WRITE ON	SET INT. FF IF $A_{15} = 1$	+ BDC BUSY	- BDC BUSY
PERIPH REJECT → COMPUTER	CLEAR BUSY			PERIPH REJECT → COMPUTER	$A_{15} = 0$	REPLY → COMPUTER	REPLY → COMPUTER
EXIT				EXIT	CLEAR INT. FF IF $A_{15} = 1$	CHANGE F REG	CHANGE F REG.
+ PERIPH REPLY → COMPUTER				+ PERIPH REPLY → COMPUTER		SET FETCH CONTROL WORD FF (A REC) → STOR. ADDR. REG.	SET FETCH CONTROL WORD FF (A REC) → STOR. ADDR. REG.
EXIT				EXIT		SET NEED FF	SET NEED FF
						REQ. MEM.	REQ. MEM.
						STOR. ADDR. REG.) → STOR. TRANS.	(STOR. ADDR. REG.) → STOR. TRANS.
						RESUME STOR. REC → X (X REG.) → PERIPH TRANS CHANGE STOR. HOLD (LWA+1 → STOR. HOLD) INCREMENT STOR. ADDR. REG. COMPARE SET NEED EXIT	RESUME CHANGE STOR. HOLD (LWA+1 → STOR. HOLD) INCREMENT STOR. ADDR. REG. COMPARE SET PERIPH READ EXIT
						REQ. MEM. (STOR. ADDR. REG.) → STOR. TRANS.	GATE PERIPH READ ON REJECT GATE PERIPH READ OFF
						RESUME CHANGE X REG. (DATA WORD → X) SET PERIPH WRITE	REPLY CHANGE X REG. (DATA WORD → X) SET NEED
						GATE PERIPH WRITE ON REJECT GATE PERIPH WRITE OFF REPLY CLEAR PERIPH WRITE	SET WRITE CLEAR PERIPH READ
							REQ. MEM. STOR. ADDR. REG.) → STOR. TRANS. X → STOR. TRANS. WRITE RESUME

NOTES:

- (1) AFTER EVERY RESUME SIGNAL, THE NEED, HALT SCANNER, AND REQ MEM. FF'S ARE CLEARED.
- (2) THE BDC IS AN ASYNCHRONOUS DEVICE. THE BLOCKS IN THE CHART DENOTE SEQUENCE OF EVENTS. THERE MAY BE APPRECIABLE TIME DELAYS BETWEEN THE BLOCKS.

PART 2

MAINTENANCE

PART 2
MAINTENANCE

INTRODUCTION

This section of the manual includes a general physical description of the 1706 BDC. Detailed information regarding specific maintenance procedures will be distributed as the information is received from personnel in the field.

Supporting documents include:

1700 Site Preparation and Installation Manual	Pub. No. 60158400
1700 CE Maintenance and Parts List Manual	Pub. No. 60160400
1700 Customer Engineering Manual Diagrams and Circuit Description, Command Timing Sequences	Pub. No. 60152700
1700 Computer System Systems Manual	Pub. No. 60152900

PHYSICAL DESCRIPTION

The 1706 BDC is built on a chassis which mounts into the 1700 vertical cabinet or in some cases, the 1700 horizontal cabinet. Table 2-1 shows the physical characteristics of the BDC.

TABLE 2-1. PHYSICAL CHARACTERISTICS

PHYSICAL CONFIGURATION	
Height:	23 inches
Width:	18 inches
Depth:	10 inches
Weight:	90 pounds
POWER REQUIREMENTS	
+6 vdc at 27 amperes -6 vdc at 10 amperes	
OPERATIONAL ENVIRONMENT	
Temperature:	40°F to 120°F
Relative Humidity:	0% to 80%

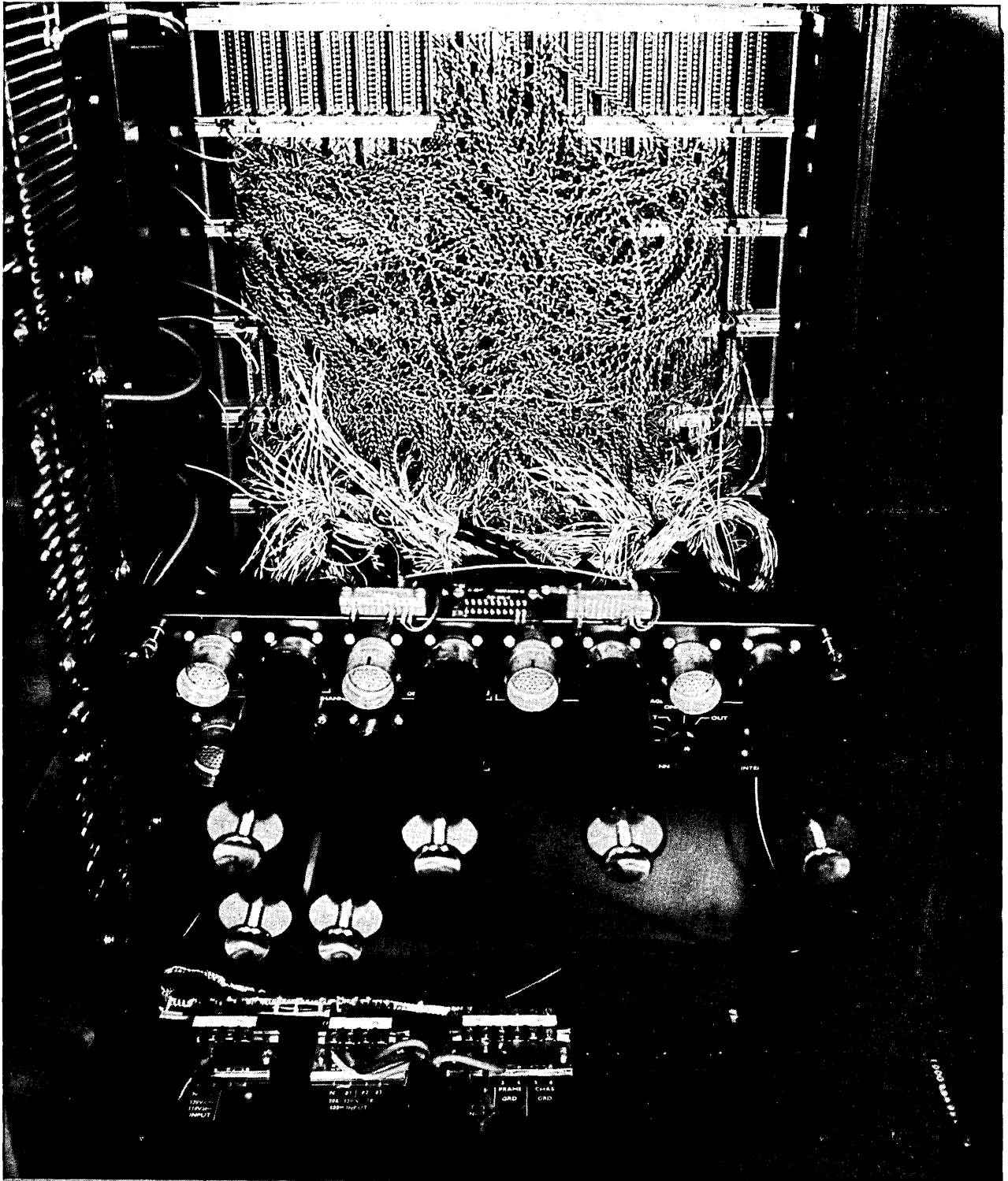
The logic chassis is cooled by forced air provided by the cabinet in which it is mounted. The logic modules are 6600-type, providing 100% silicon semiconductors.

A 40 vdc terminator power supply is required for the BDC. This power is provided by an external power supply which supplies power to all equipment in the 1700 system.

CABLING INFORMATION

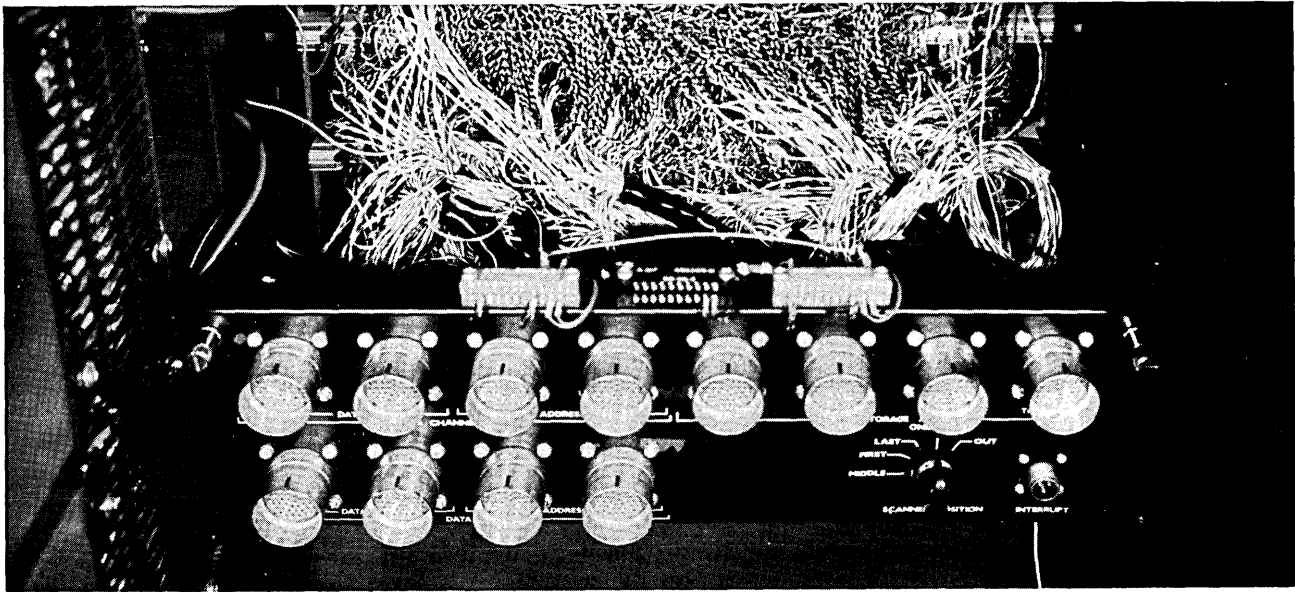
The BDC communicates with the computer via the A/Q channel and the Direct Storage Access (DSA) bus.

Both communication lines employ two 29 twisted-pair cables that terminate in 61-pin connectors. The communication lines use the transmission technique of a balanced,



1912

Figure 2-1. 1706 Chassis



1911

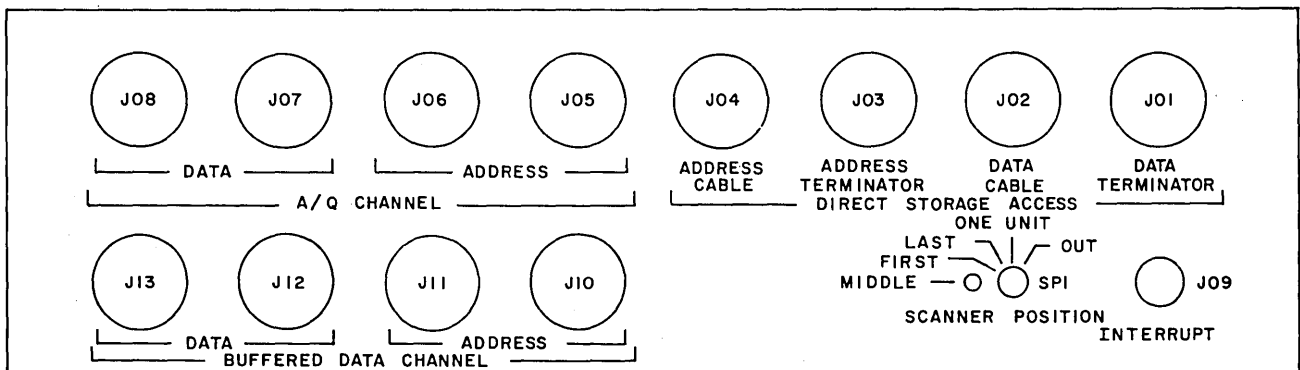


Figure 2-2. 1706 Connector Panel

terminated transmission line. Each pair of lines is terminated with its characteristic impedance by the use of an appropriate terminator plug. On the connector panel, the first receptacle of each corresponding pair is used to receive a signal cable, the second to terminate the cable or connect to a device via another signal cable.

CAUTION

Do not connect signal cables or terminators while terminator power is on. Pins F9 and F10 of each receptacle carry terminator voltage (+20 and -20 vdc). This 40 vdc can burn out terminator sections and printed circuits if it accidentally contacts a transmission line while the connector is being positioned. Turn off the toggle switch on the terminator power supply while cables are being connected or changed.

Table 2-2 lists the A/Q channel cables, signals, and pin assignment.

TABLE 2-2. A/Q CHANNEL

DATA CABLE SIGNAL (To/From A Register)		PIN	ADDRESS CABLE SIGNAL (From Q Register)	
Data Bit	00	A1-2	Address Bit	00
	01	A3-4		01
	02	A5-6		02
	03	A7-8		03
	04	A9-10		04
	05	B1-2		05
	06	B3-4		06
	07	B5-6		07
	08	B7-8		08
	09	B9-10		09
	10	C1-2		10
	11	C3-4		11
	12	C5-6		12
	13	C7-8		13
	14	C9-10		14
	15	D1-2		15
				} W
Reply		D3-4	Read	
Reject		D5-6	Write	
Character Input		D7-8	Master Clear	
Priority** (Unused)		D9-10	Program Protect	
↑		E1-2	Buffer Active**	
↓		E3-4	Timing Pulse	
		E5-6	Unused	
		E7-8	↑	
		E9-10	↓	
		F1-2	Unused	
		F3-4	W=0	
		F5-6		
		F7-8		
Termination Power		F9-10 *	Termination Power	

* Pins F9-10 of each connector are used to provide power to the terminator assembly and do not connect to lines in the A/Q cable.

** These signals exist in the cables from BAQ only and are for use with devices which use the BAQ channel exclusively.

Table 2-3 lists the DSA bus cables, signals, and pin assignments.

TABLE 2-3. DIRECT STORAGE ACCESS BUS

DATA CABLE SIGNAL (To/From Z Register)		PIN NO.	ADDRESS CABLE SIGNAL (To S Register)	
Data Bit	00	A1, 2	Address Bit	00
	01	3, 4		01
	02	5, 6		02
	03	7, 8		03
	04	A9, 10		04
	05	B1, 2		05
	06	3, 4		06
	07	5, 6		07
	08	7, 8		08
	09	B9, 10		09
	10	C1, 2		10
	11	3, 4		11
	12	5, 6		12
	13	7, 8		13
	14	C9, 10	Address Bit	14
Data Bit	15	D1, 2	Scanner Forward	
Storage Parity	16	3, 4	Priority	
Program Protect	17	5, 6	Program Protect	
Reply		7, 8	Request	
Storage Parity Error		D9, 10	Write Enable	
Program Protect Fault		E1, 2	Master Clear	
Interrupt Line 1	} *	3, 4	Interrupt Line 9	} *
Interrupt Line 2		5, 6	Interrupt Line 10	
Interrupt Line 3		7, 8	Interrupt Line 11	
Interrupt Line 4		E9, 10	Interrupt Line 12	
Interrupt Line 5		F1, 2	Interrupt Line 13	
Interrupt Line 6		3, 4	Interrupt Line 14	
Interrupt Line 7		5, 6	Interrupt Line 15	
Interrupt Line 8		7, 8	Scanner Return	
Terminator Power		F9, 10	Terminator Power	
*Termination for interrupt lines in 1700 computer main frame only.				

PART 3

PARTS LIST

INTRODUCTION

The parts list provides the identification and ordering data necessary for the replacement of electrical and hardware parts for the CONTROL DATA 1706-A.

Electrical Contents: All chassis items are included except jumper wires and bulk wire.

Hardware Contents: All chassis items are included except standard hardware such as screws, nuts, bolts, washers and raw material.

The chassis assembly and associated subassemblies are broken down into individual parts, listed in alphabetical rather than disassembly order.

The following publication contains information on peripheral cabinets and power supplies necessary to complete a total breakdown of the equipment:

Peripheral Controller Cabinets
Customer Engineering Instruction
Manual (includes power supplies) Pub. No. 60097300

ORDERING OF PARTS

When ordering Control Data parts, include the following information: CDC drawing number, description, quantity needed, equipment used on.

1706-A I/O Channel Assembly, CDC Dwg. No. 17846400
(Mounted in Vertical or Horizontal
Peripheral Cabinet) **PARTS LIST**

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
17801900	Bar, Mounting, Card	
18027900	Bar, Mounting, Connector	
17919700	Bar, Support, Chassis	
18088600	Bracket, Mounting, Chassis	
18028000	Bus, Bar, Horizontal	
17883209	Bushing, Flanged, Nylon, 0.312 OD	
18110700	Cable Assembly, 3 Pin	
18110600 through 18110611	Cable Assembly, 61 Pin	
17843500	Card Placement	
17841800	Chassis Assembly	
17900200	Clamp, Bus Bar	
17928300	Clamp, Bus Bar	
30000401	Connector, Plug, 61 Pin, Resistor-Terminator	
24562500	Connector, Receptacle, 30 Socket	
30092702	Connector, Receptacle, 20 Contact, Red	
30092706	Connector, Receptacle, 20 Contact, Blue	
30092710	Connector, Receptacle, 20 Contact, Black	
30092711	Connector, Receptacle, 20 Contact, Natural	
30000901	Connector, Receptacle, 61 Pin	
17896900	Connector, Receptacle, 3 Pin	
24554901	Enclosure Assembly, Resistor-Terminator	
00865004	Grommet, Rubber, for Connector 30000901	
17912700	Insulator Strip, Bus Bar	
00854100	Knob, Resistor-Terminator	
18031900	Member, Frame, Chassis RH Side	
18032000	Member, Frame, Chassis LH Side	
17711000	Plate, Identification, Serial	
18027800	Panel Assembly, Connector, 12 Position	

1706-A I/O Channel Assembly (Cont'd)

PARTS LIST

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
30001400	Panel, Mounting, Resistor-Terminator	
30001201	Resistor-Terminator Assembly	
17805300	Seal, Rubber, Connector	
30001900	Shield, Connector, Resistor-Terminator	
30113701	Shield, Resistor, Resistor-Terminator	
30000902	Socket for Connector 30000901	
17932700	Strip, Marker, Horizontal	
17932701	Strip, Marker, Horizontal	
18032200	Support, Connector Panel, LH	
18032100	Support, Connector Panel, RH	
24527400	Switch, Rotary, 8 Pole, 4 Section	
30095400	Termination Strip, Resistors Included, Resistor-Terminator	
00956610	Thumbscrew	
30001300	Washer, Plate, Resistor-Terminator	
18110800	Wire List, Switch	
17842700	Wire List, Logic	
18126600	Wire List, Power Jumper	
18126700	Wire List, Special I/O TW/PR	

1706-A Printed Circuit Module Assembly
 CDC Dwg. No. 17843500 PARTS LIST

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
17945201	Printed Circuit Module Assembly, Type V01	
17952101	Printed Circuit Module Assembly, Type V36	
18022001	Printed Circuit Module Assembly, Type Z51	
18024801	Printed Circuit Module Assembly, Type Z52	
18025001	Printed Circuit Module Assembly, Type Z53	
18035001	Printed Circuit Module Assembly, Type Z54	
18035201	Printed Circuit Module Assembly, Type Z55	
18042101	Printed Circuit Module Assembly, Type Z56	
18043201	Printed Circuit Module Assembly, Type Z57	
18042501	Printed Circuit Module Assembly, Type Z58	
18042701	Printed Circuit Module Assembly, Type Z59	
18043101	Printed Circuit Module Assembly, Type Z61	
*18047501	Printed Circuit Module Assembly, Type Z62	
*18047701	Printed Circuit Module Assembly, Type Z63	
*18047901	Printed Circuit Module Assembly, Type Z64	
18179301	Printed Circuit Module Assembly, Type Z79	
63061001	Printed Circuit Module Assembly, Type QK	
63063701	Printed Circuit Module Assembly, Type TE	
63064001	Printed Circuit Module Assembly, Type TH	
17876201	Printed Circuit Module Assembly, Type ZR	
17876101	Printed Circuit Module Assembly, Type ZS	
17876501	Printed Circuit Module Assembly, Type ZT	
17843501	Printed Circuit Module Assembly, Type RS	
	*Only one of these is used at any one time and is dependent on the code.	

Power Module Assembly, +6v,
25 amp, CDC Dwg. No. 18072600

PARTS LIST

DATE: _____

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
18100000	Base, Power Module	
18100100	Bracket, Rectifier	
17883206	Bushing, Flanged, Nylon	
30092519	Capacitor, Fixed, Electrolytic, 7000 uf, 10 wvdc	
24554602	Connector, Cable Clamp, Strain Relief, Nylon, Black, 0.560 O.D.	
24554603	Connector, Cable Clamp, Strain Relief, Nylon, Black, 0.870 O.D.	
17763801	Connector, Plug, Polarized, 6 Pin	
18099900	Cover, Power Module	
00839501	Grommet, Rubber, 1/8 Groove, 3/8 ID	
00838200	Nut, Sheet Spring, #6-32	
17711000	Plate, Identification	
24561603	Rectifier, Silicon, 40 Amp, Normal Polarity	
30092601	Retainer, Capacitor	
18112100	Transformer - Indicator, 6V, 25 Amp, 400 Cycle	
18155600	Wire List	

Power Module Assembly, -6v, 25 Amp,
 CDC Dwg. No. 18072900 PARTS LIST

DATE: _____

CDC - DRAWING NUMBER	DESCRIPTION	QUANTITY EACH MACHINE
18100000	Base, Power Module	
18100100	Bracket, Rectifier	
17883206	Bushing, Flanged, Nylon	
30092519	Capacitor, Fixed, Electrolytic, 7000 uf, 10 wvdc	
24554602	Connector, Cable Clamp, Strain Relief, Nylon, Black, 0.560 O.D.	
24554603	Connector, Cable Clamp, Strain Relief, Nylon, Black, 0.870 O.D.	
17763801	Connector, Plug, Polarized, 6 Pin	
18099900	Cover, Power Module	
00839501	Grommet, Rubber, 1/8 Groove, 3/8 I.D.	
00838200	Nut, Sheet Spring, #6-32	
17711000	Plate, Identification	
24561604	Rectifier, Silicon, 40 Amp, Reverse Polarity	
30092601	Retainer, Capacitor	
18112100	Transformer-Inductor, 6v, 25 amp, 400 Cycle	
1815 00	Wire List	

SH 2

53832000	E	CLA	A	16 BIT ADDRESSING OPTION	DSM	FV430A	11/05/71	
ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	CLASSIFICATION NUMBER

MF

08/06/74	1 / 1
PROCESSING DATE	PAGE NUMBER

CONTROL DATA
CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	CLASSIFICATION NUMBER	OP NUMBER	MAKE/BUY PART TYPE	PN NC	S OR N
	A	15000700	100	PC	EQUIPMENT IDENTIFICATION PLATE	IN					PPP1		N
12	D	17876100	100	PC	MODULE ASSY TYPE ZS	IN					AYM4		N
	C	17901502	600	PC	4-40SCR THD ROLL PHL H PAN	IN	032094	080172			PPP1		N
13	C	17949401	300	PC	RETAINER MODULE ASSY	IN	031058	041172			AYP4		N
17		17954500	100	PC	MODULE ASSEMBLY TYPE V48	IN	017026	073074			AYM4		N
14	C	24500707	800	PC	PIN TAPER	IN					PPP1		N
15	C	24528639	800	IN	INS SLEEVING, ELEC-BULK	IN					PPP1		N
1	C	24561201	200	PC	WIRE ELEC 3 IN WHITE/BLACK	IN					KTM3		N
2	C	24561202	500	PC	WIRE ELEC 5 IN WHITE/BLACK	IN					KTM3		N
3	C	24561203	3300	PC	WIRE ELEC 7 IN WHITE/BLACK	IN					KTM3		N
4	C	24561204	700	PC	WIRE ELEC 9 IN WHITE/BLACK	IN					KTM3		N
5	C	24561205	500	PC	WIRE ELEC 11 IN WHITE/BLACK	IN					KTM3		N
6	C	24561206	300	PC	WIRE ELEC 13 IN WHITE/BLACK	IN					KTM3		N
7	C	24561207	200	PC	WIRE ELEC 15 IN WHITE/BLACK	IN					KTM3		N
16	C	24561208	300	PC	WIRE ELEC 17 IN WHITE/BLACK	IN					KTM3		N
8	C	24561209	100	PC	WIRE ELEC 19 IN WHITE/BLACK	IN					KTM3		N
9	C	24561210	100	PC	WIRE ELEC 21 IN WHITE/BLACK	IN					KTM3		N
10	C	24561230	100	PC	WIRE ELEC 108 IN WHITE/BLACK	IN					KTM3		N
11	D	63066400	200	PC	MODULE ASSY. TYPE RS	IN	031058	041172			AYM4		N

NUMBER OF LINE ITEMS = 19
HIGHEST FIND NUMBER = 17

PROJECT ENGINEER

D. KRAMER

3-7

Rev. K

COMMENT SHEET

MANUAL TITLE 1706-A, DT129-A, FV430-A Buffered Data Channel

Customer Engineering Manual

PUBLICATION NO. 60165700 REVISION K

FROM NAME: _____

BUSINESS
ADDRESS: _____

COMMENTS: This form is not intended to be used as an order blank. Your evaluation of this manual will be welcomed by Control Data Corporation. Any errors, suggested additions or deletions, or general comments may be made below. Please include page number.

CUT ALONG LINE

STAPLE

STAPLE

FOLD

BUSINESS REPLY MAIL
NO POSTAGE STAMP NECESSARY IF-MAILED IN U.S.A.

FIRST CLASS
PERMIT NO. 333

LA JOLLA, CA.

POSTAGE WILL BE PAID BY
CONTROL DATA CORPORATION
SMALL COMPUTER SYSTEMS DIVISION
4455 EASTGATE MALL
LA JOLLA, CALIFORNIA 92037

ATTN: PUBLICATIONS DEPARTMENT

FOLD

CUT ALONG LINE

STAPLE

STAPLE



▶ ▶ CUT OUT FOR USE AS LOOSE-LEAF BINDER TITLE TAB

CONTROL DATA
CORPORATION

**CORPORATE HEADQUARTERS, 8100 34th AVE. SO., MINNEAPOLIS, MINN. 55440
SALES OFFICES AND SERVICE CENTERS IN MAJOR CITIES THROUGHOUT THE WORLD**

Litho in U.S.A.