74700700

CONTROL DATA CORPORATION

CDC® SYNCHRONOUS COMMUNICATIONS LINE ADAPTER

DU138-A

DU139-A

DU140-A

HARDWARE MAINTENANCE MANUAL

REVISION RECORD

REVISION	DESCRIPTION
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MANUAL TO EQUIPMENT LEVEL CORRELATION SHEET

This manual reflects the equipment configurations listed below.

EXPLANATION: Locate the equipment type and series number, as shown on the equipment FCO log, in the list below. Immediately to the right of the series number is an FCO number. If that number and all of the numbers underneath it match all of the numbers on the equipment FCO log, then this manual accurately reflects the equipment.

EQUIPMENT TYPE	SERIES	WITH FCOs	COMMENTS
DU 138-A	01		
DU 139-A	01		
DU 140-A	01		

LIST OF EFFECTIVE PAGES

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PREFACE

This manual contains operation, maintenance, installation, and checkout as well as relevant programming considerations for the CDC® Synchronous Communications Line Adapter (SCLA). The manual contains SCLA programming and operating considerations as well as data on installation, checkout, and maintenance, including parts list and cabling information.

The manual is intended for use by Customer Service Engineers and presumes minimal knowledge of the 2550 Series network processor unit (formerly called host communications processor) within which the SCLAs are employed. Preventive maintenance and fault isolation procedures to the SCLA card level are given. Card repair is also described although system malfunctions are corrected by SCLA card replacement and card repair on-site should be limited to emergency conditions only.

The related publications listed below are available through the CDC Literature Distribution Services, Minneapolis, Minnesota.

Publication	Publication Number
2550 Series Host Communications Processor, Site Preparation Manual	74641200
2550 Series Host Communications Processor, Hardware Installation Manual	74700800
2551-1, 2551-2, 2552-2 Network Processor Unit, Hardware Maintenance Manual	60472000
2551-1, 2551-2, 2552-2 Network Processor Unit, Hardware Reference Manual	50472800

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INTRODUCTION

This section describes the physical and functional characteristics of the synchronous communications line adapter (SCLA).

The SCLA is a synchronous data conversion and control device which provides for the connection of synchronous communications facilities to a network processor unit (NPU). The SCLA consists of three functional sections: input, output, and modem interface. The input section receives serial data from the communications line and converts it to parallel format for input to the communications processor. The input section also monitors the data transfer process and communications facility (via the modem interface section) and reports status to the communications processor.

The output section converts parallel data output from the communications processor to serial form for transmission to the communications line. The output section also accepts commands from the communications processor, which are used to control the data transfer process and communications facility. The modem interface section contains circuits that convert the electrical interface signals required by the communications facility (Data Set or modem) to levels compatible with the internal SCLA logic.

Three models of the SCLA are described in this manual: the DU138-A, DU139-A and DU140-A. They differ basically in the type of communications facility interface provided.

DU138-A SCLA - contains interface circuits compatible with EIA Standard RS232C or CCITT Recommendation V.24. It operates with voice-grade channel modems compatible with AT&T 201, 203, 208, and 209 Data Sets at speeds up to 20,000 bits per second (bps).

DU139-A SCLA - provides a current switching mode interface compatible with AT&T 301B and 303 Data Sets (wideband) at speeds up to 50,000 bps.

DU140-A SCLA - contains interface circuits compatible with CCITT Recommendation V.35 at speeds up to 56,000 bps. It can be used to interface with the AT&T Digital Data System for 56,000 bps service.

The descriptions and procedures in this manual apply to all three models of the SCLA except where the differences are specifically delineated.

PHYSICAL DESCRIPTION

An SCLA card consists of integrated circuits and components mounted on a printed wiring assembly (circuit card), as shown in figure 1-1. Two complete, identical SCLA circuits are contained on a card. The rear edge of the card contains two 102-contact tab connectors, extending the full length of the card. When the card is inserted in its card cage, these tab connectors engage the cage backpanel to provide signal paths between the SCLA and its interfacing element in the multiplexing subsystem, the loop multiplexer.

The card is reinforced and protected with a metal frame which is riveted to the card. The front surface (card handle) provides an accessible mounting surface for switches, indicators, and cable connectors. The card handle when installed forms a cover to assure that cooling air is contained within the card cage. Two plastic ejectors on the handle facilitate removal of the card.

Two pairs of hexadecimal switches permit address selection of each SCLA and four signal indicators show when signals are passing through the SCLA. Two 25-pin connectors on the card handle provide the connection for SCLA-to-terminal/modem signal cables. Two toggle switches permit enabling/disabling of each SCLA (SCLA1 and SCLA2) on a card.

All SCLA cards are installed in a CLA and loop multiplexer card cage assembly which also contains either one or two loop multiplexer circuit cards, as shown in figure 1-2. The card cage assembly provides 16 positions (card slots) for communications line adapters; an SCLA may reside in any position. A loop multiplexer can connect a maximum of 32 communications lines.

Figure 1-3 shows the location of the card cage in an NPU system cabinet.

SCLA CHARACTERISTICS

A summary of the physical specifications for the SCLA are given in table 1-1. Nonoperating environmental requirements for the SCLA are given in table 1-2, and operating environmental requirements are listed in table 1-3.

TABLE 1-1. PHYSICAL CHARACTERISTICS

Characteristics	Value
Dimensions	
Length	14.6 inches (371 mm)
Width	11 inches (279 mm)
Thickness	
With card handle	0.9 inches (23 mm)
Card only	0.063 inches (1.6 mm)
Weight	1.6 pounds (0.73 kg)
Power Requirements	
Consumption	13.6 watts
Logic voltages	+5.0 ±0.25 volts dc, 2.00 amp +12.0 ±0.50 volts dc, 0.15 amp -12.0 ±0.50 volts dc, 0.15 amp

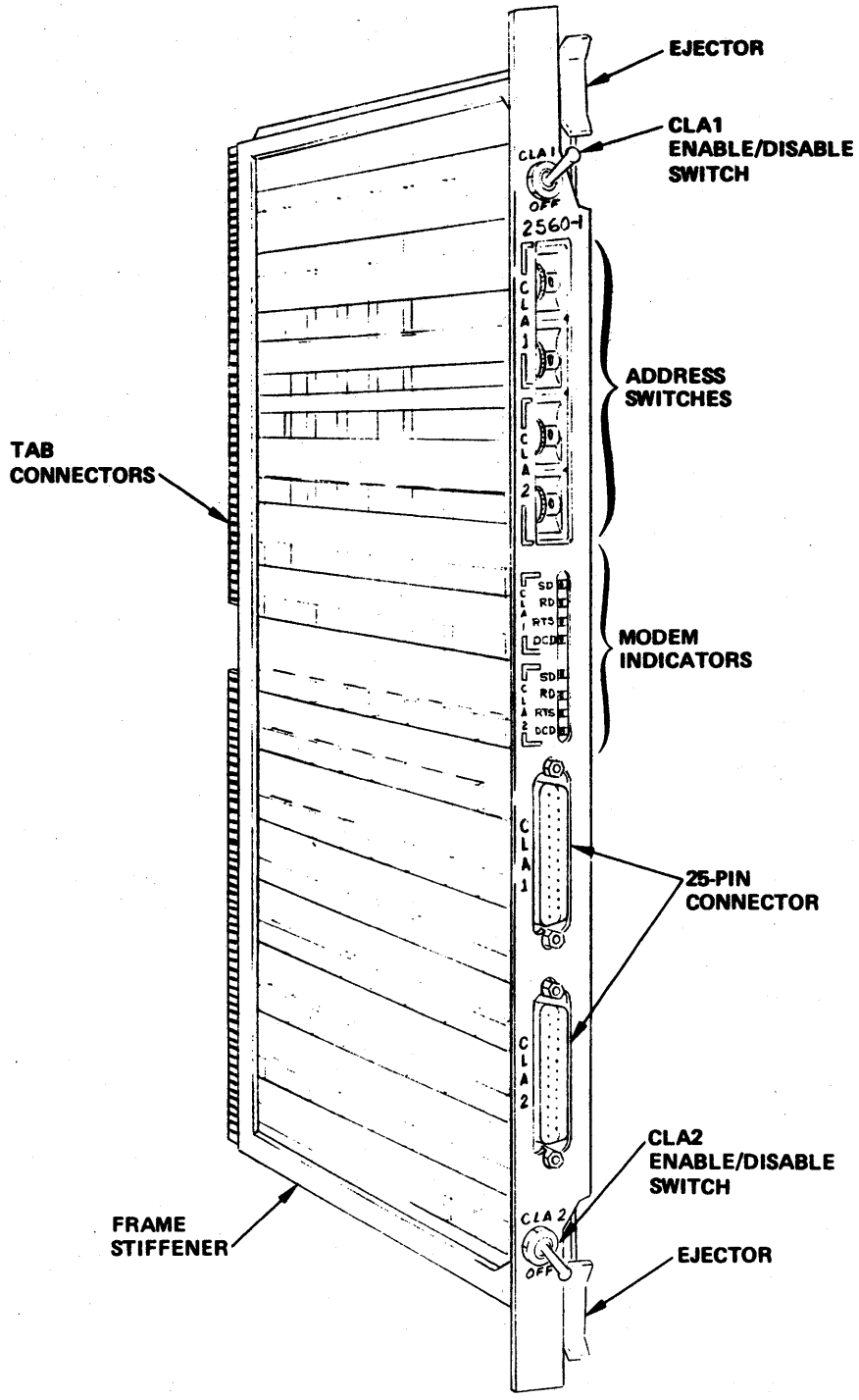


Figure 1-1. SCLA Circuit Card

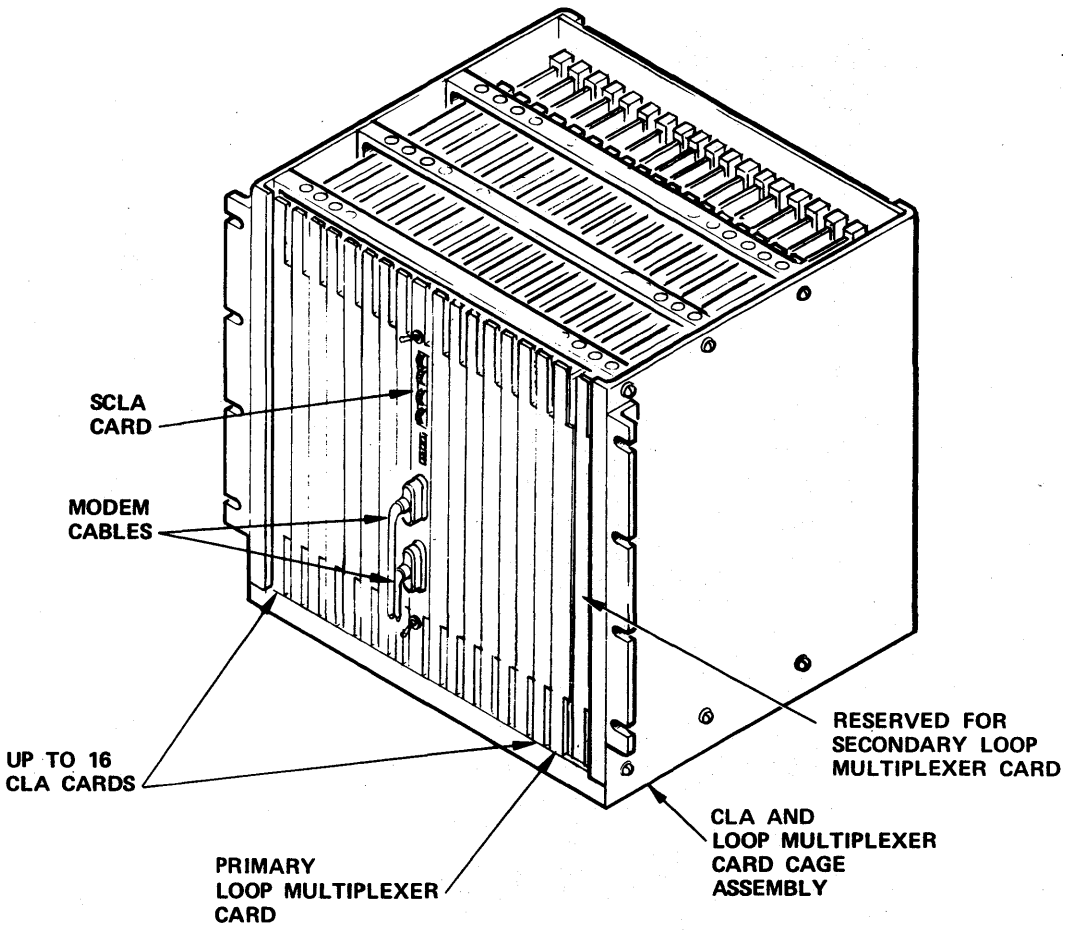


Figure 1-2. SCLA Card Placement

TABLE 1-2. NONOPERATING ENVIRONMENTAL REQUIREMENTS

Parameter	Requirement
Altitude	1000 feet (305m) below sea level to 15,000 feet (4575 m) above sea level
Temperature	-30°F to +150°F (-37°C to +66°C)
Thermal Shock	+80°F to -30°F (+27°C to -37°C) +80°F to +150°F (+27°C to +66°C) (rate of change not to exceed 20°F [12°C] per hour)
Humidity	5% to 95% (no condensation)
Shock	18 impacts of 5g ±10% for a duration of 11 ±1 ms, with maximum g occurring at 5.5 ms. Three impacts in each direction along three major axes
Vibration	Peak displacement ±0.005 inch at 5 to 60 Hz; acceleration of 2g at 60 to 500 Hz; as packed for shipment

TABLE 1-3. OPERATING ENVIRONMENTAL REQUIREMENTS

Parameter	Requirement
Altitude	1000 feet (305m) below sea level to 6000 feet (1830 m) above sea level
Temperature	Recommended: +72°F (+22°C) (ambient temperature for 2550 system)
Humidity	Continuous operation at 90% relative humidity and 104°F (40°C). No operational condensation requirements. Excursion rate: not to exceed 10% per hour
Particulate Contamination	Range 3
Caustic Chemical Environment	Not allowed

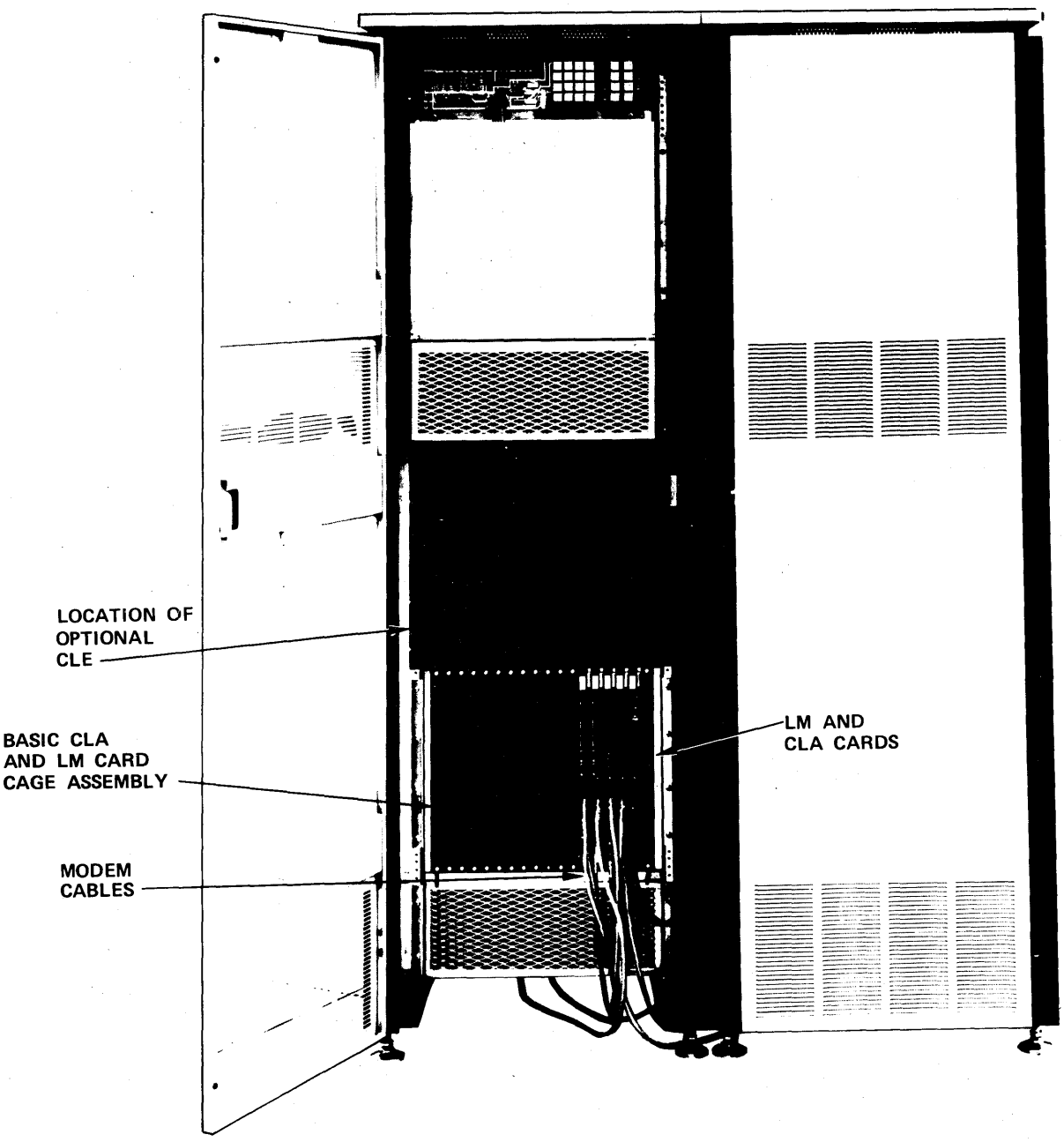


Figure 1-3. CLA and LM Card Cage Location in System Cabinet

SYSTEM APPLICATIONS

A sample system application is shown in figure 1-4, which is for illustrative purposes only; it does not necessarily represent an actual configuration.

The loop multiplexer, multiplex loop, multiplex loop interface adapter, and one or more CLAs make up the multiplexing subsystem. The multiplexing subsystem hardware elements function as follows:

- Communications line adapters (CLAs) provide data conversion and control between the loop multiplexer and communications lines that are connected to the customer-supplied terminals or modems.
- The loop multiplexer provides a multiplexed path between a group of CLAs and the multiplex loop.
- The multiplex loop interconnects several loop multiplexers and the processor.
- The multiplex loop interface adapter (MLIA) provides the hardware interface between the multiplex loop and the communications processor.

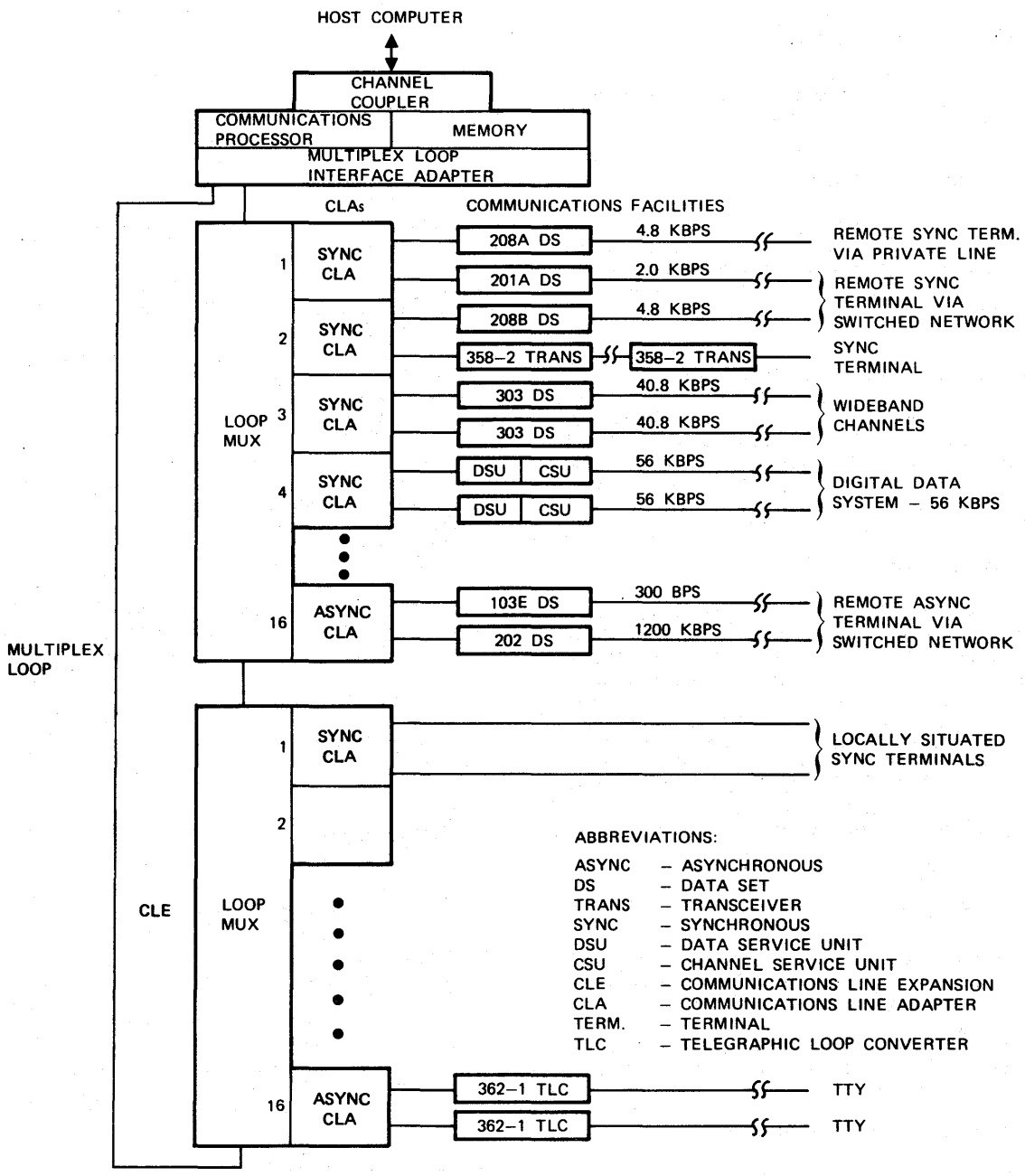


Figure 1-4. Typical CLA Application

Figure 1-4 also illustrates the use of a communications line expansion (CLE) unit. When more than 16 CLA cards are required or the number of communications lines exceeds 32, a CLE may be used. A second CLE is used for expansion beyond 32 cards or 64 lines, and a third CLE for expansion to 64 and 128 lines, respectively. Note that figure 1-4 also indicates use of an asynchronous CLA which is not treated in this manual.

Each CLE consists of a loop multiplexer and required power and cooling assemblies.

FEATURES

HALF- AND FULL-DUPLEX OPERATION

The SCLA can be operated in either the half- or full-duplex mode. A request-to-send function is under program control. For half-duplex operation, it can be turned on or off independent of other SCLA commands to switch the modem between transmit and receive modes. Also, the input section can be disabled while in transmit mode to avoid receiving back what is being sent. For full-duplex operation, request-to-send (program-controlled) is generally left on and the input section continuously enabled.

CODE LENGTHS

The SCLA can receive or transmit 5-, 6-, 7-, or 8-bit characters. A parity bit may also be added. The character length is selected by program command.

CHARACTER SYNCHRONIZATION

At the beginning of each incoming transmission, the SCLA acquires character synchronization by scanning the serial data stream for a bit pattern equal to the synchronization code (character). The synchronization character is specified by program command.

CHARACTER PARITY GENERATION/DETECTION

As a software option, the SCLA can be commanded to check input for and generate output with odd or even or without character parity. When a character is received with incorrect parity, parity error status is sent to the processor coincident with the character.

AUTOMATIC ANSWERING

The SCLA may be used with modems capable of automatic answering. Upon receipt of a call, the local modem sends a ring indicator signal to the SCLA, which in turn reports ring indicator status to the processor. If the software previously activated the data terminal ready (DTR) signal, the modem answers the call after one ring. If DTR is not on, the modem does not answer the call until the software issues a command to turn on DTR. Thus, the software may precondition DTR on and calls are answered when received, or DTR can be left off and the software decides, upon receipt of ring indicator status, whether to answer the call or not.

SIGNALING RATE TIMING SOURCE

Normally, the local modem provides the timing source (clock signals) for SCLA serial data transfer. For modems requiring an external clock source, or for local terminals connected directly to the SCLA without modems, three different clock rates are available at the card handle (modem) connector. These rates are 2.4, 4.8, and 9.6 kHz.

DATA TRANSFER OVERRUN AND UNDERRUN

The SCLA generates data transfer overrun status signal if it assembles a new character before a previously assembled character has been transferred to the processor. Because the SCLA is of the synchronous type, contiguous characters must be available during transmission in order to maintain character synchronization. If contiguous characters are not available (an underrun condition), the transmit data line is set to a marking condition and next character not available (NCNA) status signal informs the processor of this condition.

INTERNAL LOOPBACK TEST

On-line maintenance and checkout of the SCLA can be performed by use of an internal loopback test feature. When the SCLA receives a loop internal test (LIT) command from the processor, data from the output section is routed directly to the input section rather than to the modem. Also, modem control signal lines (e.g., request to send) are routed back to appropriate modem status lines (e.g., clear to send). The internal loopback test mode allows testing of all SCLA sections except the level conversion circuits in the modem interface section.

MODEM INTERFACE

Three different types of modem interfaces are provided by the three models of the SCLA. In addition to the normal data and clock signals, a number of modem control signals are accommodated. These control signals vary among the three SCLA models.

The DU138-A SCLA is designed for compatibility with EIA Standard RS232C or CCITT Recommendation V.24 signals and provides the following signal interfaces:

Request to send
Clear to send
Data set ready
Receive line signal detector
New sync
Quality monitor
Data terminal ready
Signal quality detector
Ring indicator
External transmit clock

The DU139-A SCLA provides a current switching mode capability compatible with AT&T 301B and 303 Data Sets. The interface signals with these Data Sets are:

Request to send
Local test
Clear to send
Data carrier detector
Data terminal ready
Ring indicator
Data set ready
External transmit clock

The DU140A SCLA is compatible with CCITT V.35 signals and interfaces the following signals:

Request to send
Ready for sending (Clear to send)
Data set ready
Data channel receive line signal detector
Local test (CCITT V.28)
External transmit clock (non-CCITT V.35)
Ring indicator (CCITT V.28)
Data terminal ready (CCITT V.28)

FUNCTIONAL DESCRIPTION

OPERATIONAL CONCEPT

The SCLA is a functional element of a demand-driven loop multiplexing subsystem. Figure 1-4 shows the interrelationship of the other functional elements of the subsystem.

The multiplex loop gathers input data and status from, and distributes output data and control to, many communications line adapters (CLAs). CLAs gain access to the multiplex loop through a loop multiplexer (LM). The loop multiplexer allows a group of CLAs to access the multiplex loop through a single attachment point. The LM is essentially a passive device.

Both ends of the multiplex loop terminate at the multiplex loop interface adapter (MLIA), a control unit attached to the processor's input/output and direct memory access channels. The MLIA controls the operation of the multiplex loop and

transfers data and supervision between the loop and the processor. For more detailed information on the operation of the multiplexing subsystem, refer to the NPU hardware reference manual.

The SCLA assembles data characters in its input section and disassembles them in its output section. On input, it converts serial data to parallel data, assembling the serial data at the signaling rate of the communications facility and transferring the data to the LM. On output, the SCLA functions as a parallel to serial converter, receiving the data characters from the LM and outputting them serially at the signaling rate of the communications facility. The data paths of the SCLA are shown in figure 1-5.

INPUT SECTION

The input section of the SCLA receives serial data and monitors control signals from the modem, then passes this information on to the processor via the LM. Figure 1-6 is a diagram of the input functions. The SCLA informs the LM that it requires data (output data demand), has data, or has status via the input available (IAV) signal. This signal is not activated unless the SCLA is commanded to receive or transmit data or report status. The SCLA is selected by the input select signal (SELI) from the LM. This enables the SCLA to load 11 bits of information (loop cell) on the input bus with each input-strobe signal. The first three bits are defined as cell format codes and determine whether the remaining eight bits of information are address, data, or supervision. The first byte of information is always the SCLA address, which must be identical to the settings of the address switches on the SCLA card handle.

If the SCLA has data ready for the LM, the data is reported as the next byte of information after the address. Once data transmission starts, character assembly continues, one in each character time, until the SCLA is commanded to stop assembling characters.

If the SCLA also has status information to report, the next two bytes of information will be status cells. During the last cell the input end (IEN) signal to the LM is activated, thereby directing the LM to terminate the selection.

If the SCLA has only status information ready, only two supervision cells are provided. During the second cell, the IEN signal to the LM is activated, thereby directing the LM to terminate the selection.

If the SCLA has no status or data to report but has output data demand, it sets the output data demand (ODD) flag in the address byte. The IEN line is then activated during the address byte, and the selection is terminated.

The SCLA is allowed to transfer data to the processor if the input on (ION) command becomes active. The SCLA monitors the receive data (RD) line for a bit pattern that is identical to the synchronization character for which it is programmed. When a match occurs, the SCLA becomes character-synchronized with the receive data line. In the center of the last bit of the following character, the received character is transferred to the receiver holding register. The input available (IAV) signal is then set to a logical 1, informing the LM that a character is available. This character is transferred to the LM when the SCLA input section is selected. Also at this time, parity error or data transfer overrun status is updated.

The SCLA uses three methods of error checking to detect the lack of integrity of incoming data and to guarantee that no data is lost or transferred in error without a report being made to the processor. The three error detection functions are:

- Input loop error (ILE)
- Data transfer overrun (DTO)
- Parity error (PE)

Input Loop Error

The LM informs the SCLA when an error occurs on the input loop while the SCLA is using the loop. The SCLA reports the condition to the LM by sending an input loop error (ILE) status signal.

Data Transfer Overrun

When assembling characters, the SCLA holds the previously assembled data character in the receiver holding register until the next data character is assembled. If the LM has not accessed the character in the receiver holding register by the time a new character is assembled, the SCLA erases the previous character, sets the new character into the register, issues an input available signal, and sets the data transfer overrun bit to one in the status buffer. The SCLA input does not store more than one data character.

NOTE

A data transfer overrun occurs and a DTO status is generated when the first character is not accessed 700 nanoseconds plus one-half of a bit time before the end of the next character.

Parity Error Status

By command from the processor, the SCLA can be instructed to check for either even or odd character parity or to ignore character parity. Upon detection of a character parity error, input available to the LM is set, and the parity error status bit is set to a 1 in the status buffer. The SCLA always transfers an included parity bit to the LM for characters containing five to eight bits. The parity bit is not transferred for codes containing nine bits.

OUTPUT SECTION

The SCLA output section receives parallel data from the LM and transfers the data in serial fashion to a modem at the signaling rate of the modem or at a rate determined by an internal timing source. Figure 1-7 is a functional diagram of the output process.

If the processor is ready to output data, it sends the output on command to the SCLA. When the SCLA is ready to accept a character for output, it sets the output data demand status signal. This causes input available to be set. Then the ODD bit in the SCLA address is presented to the LM when the input section is selected.

The output section of the SCLA is presented with an address and a select signal. If the address corresponds to the setting of its address switches, the SCLA recognizes commands and/or data received at the output bus.

Commands consist of the appropriate format bits and eight bits of information. When the SCLA receives a command, it is loaded into the command register. Commands are used to determine word length, parity selection, and the state of the modem control lines. These commands are described in detail in Section 2.

Data consists of the appropriate format bits and eight bits of information. When data is received during the output

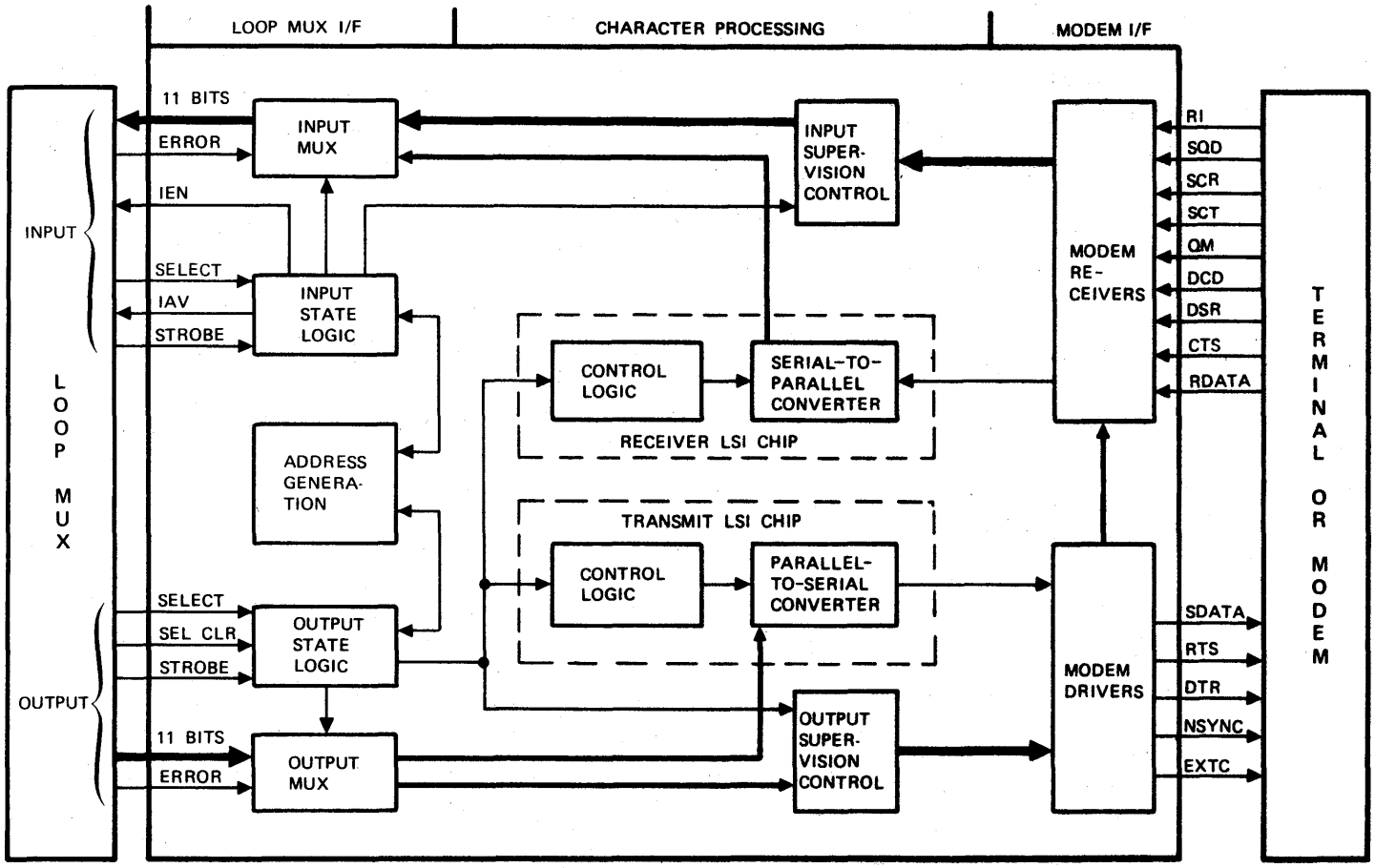


Figure 1-5. Synchronous Communications Line Adapter Block Diagram

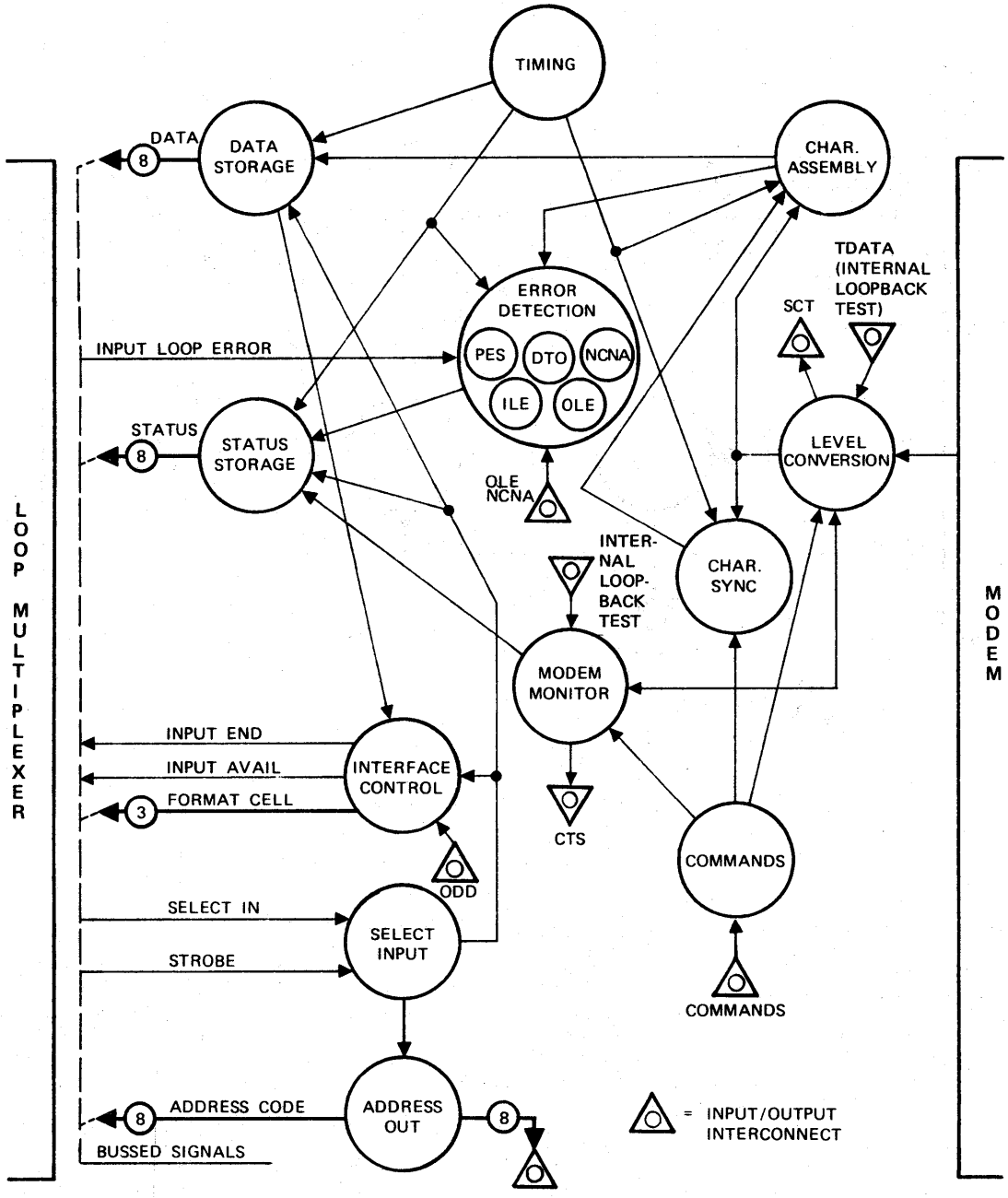


Figure 1-6. Input Function Flow Diagram

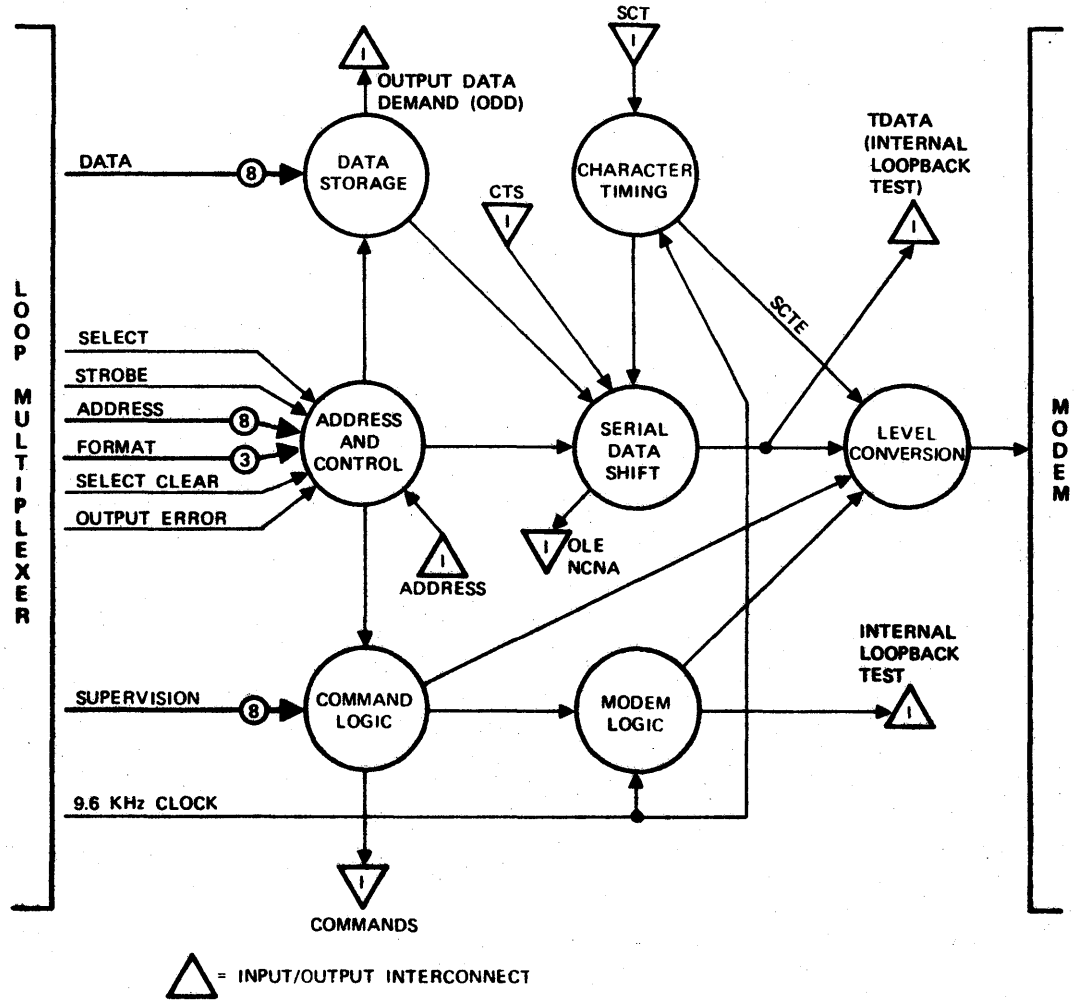


Figure 1-7. Output Function Flow Diagram

select cycle, the information bits are loaded into the transmitter holding register by the output strobe signal. The character is then loaded into the transmitter shift register if the clear to send signal is active from the modem. The data is then shifted out serially on the transmit data line. Upon initiating serial data transmission, an output data demand flag is sent to the processor via the input section of the SCLA. This signal notifies the processor that the transmitter holding register is ready for the next character.

The SCLA uses two methods of error checking to ensure that no data is lost or transferred in error without a report being made to the processor. These two techniques involve recognition of data transfer underrun and output loop error conditions.

Data Transfer Underrun

While transmitting a message, the SCLA must be supplied characters fast enough to keep the characters contiguous. If characters are not supplied in time to maintain contiguous timing, the SCLA sends a character time of marking (logical 1) condition, and posts next character not available (NCNA) status for the software.

Output Loop Error

The LM informs the SCLA when an error occurs on the output loop while the SCLA is using the loop. The SCLA reports this condition to the software by sending output loop error status. Information received from the line frame is processed normally.

MODEM INTERFACE SECTION

The modem interface section of the SCLA provides the level conversion logic to make the SCLA compatible with the signal levels of the modem. This section of the SCLA also monitors the modem status lines for a change of condition: either a logical 1-to-0 or 0-to-1 transition. When a change occurs, status is reported to the processor.

There are, however, two exceptions to this procedure. First, a change in the clear to send line does not activate a status report; and second, a ring indicator status change only triggers a status report on a logical 1-to-0 transition.

This section provides information on control set-up and operation of the SCLAs as well as program control. The format of address, data, status and command (supervision) characters flowing through or utilized by the SCLA is treated, and descriptions of the various status and command bits in the characters are included.

CONTROLS AND INDICATORS

The controls and indicators consist of four light-emitting diode (LED) indicators, two thumbwheel address switches and an enable/disable toggle switch for each SCLA. Each address switch has a total of 16 different positions (hexadecimal); thus each pair of switches can be set to a total of 256 (16 times 16) different settings. The numerals 0 thru 9 and the letters A thru F are used to display the 16 possible settings for each switch. The upper thumbwheel switch in each pair represents the most significant digit. Refer to appendix B for hexadecimal conversion data.

Functionally, the address switch settings are encoded as an 8-bit binary address. Each CLA in the user's system must be set to a unique address by means of the address switches. The communications processor receives data from or transmits data to an SCLA based on the setting of its address switches; this routing of data is independent of the location of an SCLA card in the CLA and loop multiplexer card cage.

The CLA1 and CLA2 enable/disable switches, when in the OFF position, disable the associated SCLA. This effectively cuts off all input from the SCLA to the processor. The switches should be at OFF while address switches are changed if the card is plugged in and the system is operating. The switches are set to the ON position only after the card has been inserted and the proper address selected. The names and functions of all SCLA switches and indicators are listed in table 2-1. The switches and indicators are shown in figure 2-1.

OPERATING PROCEDURES

Operation of the SCLA is automatic, and no operator action is required.

PROGRAMMING CONSIDERATIONS

The following programming reference information for the SCLA does not contain specific procedures for constructing an actual program. To prepare a program to control the SCLA requires detailed knowledge of the operation of the other multiplexing subsystem elements: the multiplex loop interface adapter, multiplex loop, and loop multiplexer. The information required may be found in the NPU hardware reference manual.

MULTIPLEXING SUBSYSTEM

The processor communicates with a CLA via the multiplex loop. The multiplex loop consists of two independent loops: the input loop and the output loop. The input loop carries output data demands, input data, and supervision (status) from the CLA to the processor. The output loop carries

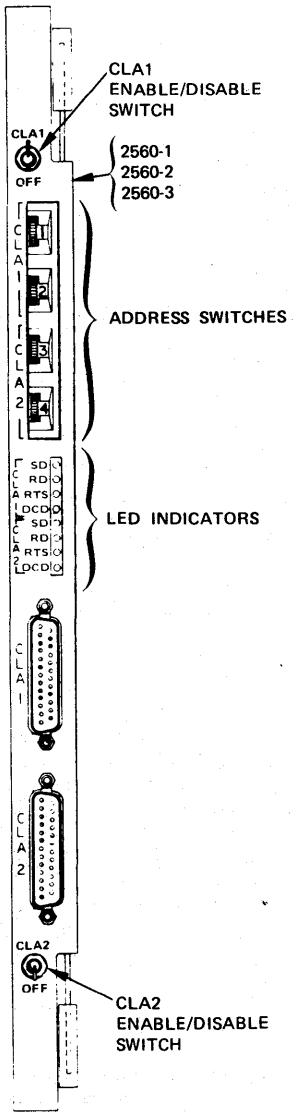


Figure 2-1. Controls and Indicators

output data and supervision (commands) from the processor to the CLA.

Information is transferred serially by bit on the loops. Loop cell structure is shown in figure 2-2. Every twelfth bit is a cell frame marker that defines a 12-bit loop cell. The cell frame marker is followed by a cell identification field (3 bits), which defines the contents of the remaining field (8 bits) of the cell. The loop multiplexer receives information from the output loop and presents the cells in parallel form to the CLA (an 11-bit interface is used; the cell frame marker bit is deleted). Similarly, the CLA transfers cells (11 bits) to the loop multiplexer which presents them serially (and adds the cell frame marker bit) to the input loop.

TABLE 2-1. SWITCHES AND INDICATORS

Name	Display/Status	Function
Address switches	Two hexadecimal digits	Designation of SCLA address; setting displayed in hexadecimal code (00 to FF). Top switch is most significant digit; bottom switch is least significant digit.
CLA (1 or 2)/OFF switches	OFF/on	Logical disconnection of each SCLA
Modem indicator SD	Blinking/off	Blinking, indicates SCLA sending data to modem
Modem indicator RD	Blinking/off	Blinking, indicates SCLA receiving data from modem
Modem indicator RTS	Lighted/off	Lighted, indicates request-to-send from SCLA is active
Modem indicator DCD	Lighted/off	Lighted, indicates data-carrier-detect from modem is active

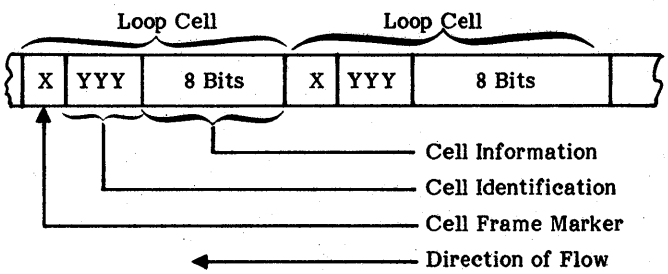


Figure 2-2. Loop Cell Framing Structure

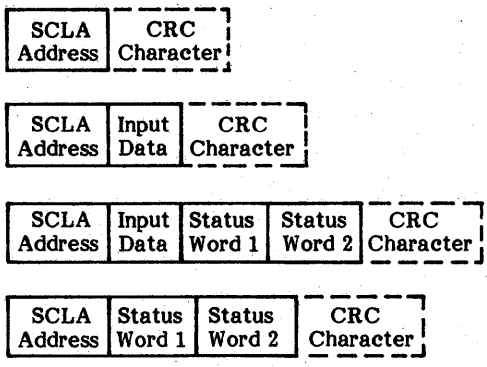


Figure 2-3. Input Loop Cell, Line Frame Format

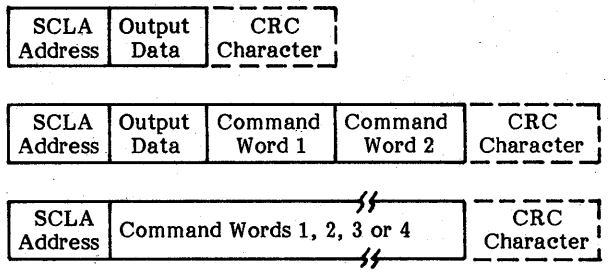


Figure 2-4. Output Loop Cell, Line Frame Format

A line frame is a group of contiguous loop cells related to a particular CLA. The first cell of a line frame contains the address of the CLA, and the last cell of the frame contains a cyclic redundancy check (CRC) character. On the input loop, the address cell also carries the output data demand (ODD) signal bit. Other cells within the frame may contain data and/or supervision (status or commands). All cells are passed unmodified between the multiplex loop and the CLA, except the check character which is removed from the output loop and added to the input loop by the loop multiplexer.

LINE FRAME FORMATS

The line frame format as compiled by the SCLA for transfer to the LM input loop and processor is shown in generalized form in figure 2-3. The SCLA address cell is always present and may contain an active output data demand bit. The data cell may appear next and contains input data. Two supervision cells may also follow and contain status word 1 and status word 2. If any status is to be reported, both status words always appear. The CRC character is added by the loop multiplexer and does not concern the SCLA.

The generalized line frame format presented to the SCLA by the multiplex output loop is depicted in figure 2-4. The SCLA address cell is always present. Either the data cell or command words may appear next. The data cell contains output data. One to four supervision cells may appear and contain command words 1, 2, 3 and 4. Allowable combinations of command words are: none; 1; 1 and 2; 1, 2 and 3; or 1, 2, 3 and 4. The CRC character is removed by the loop multiplexer before being transferred to the SCLA.

CELL AND WORD FORMATS

The formats of the various word types used within the SCLA are presented in table 2-2. Processor word and loop multiplexer (LM) bit position identifications are shown in the table. These are for reference only and are of no real concern to the SCLA. Within the LM and processor, each word consists of 12 bits. As noted earlier, however, bit position 0 of the LM is a cell frame marker used for loop timing. This bit is not employed within the SCLA as noted by the Xs in the table.

The rightmost eight bits (I1 thru I8) of the LM cell contain information while the leftmost three bits (F1 thru F3)

TABLE 2-2. CELL FRAME FORMATS

Word/Field Type	Bit Position												Flow
Processor Word LM Cell	11 0	10 1	9 2	8 3	7 4	6 5	5 6	4 7	3 8	2 9	1 10	0 11	
Information Field Identification Field	X X	F1	F2	F3	I1	I2	I3	I4	I5	I6	I7	I8	
Address ID Field	X	1	1	†	← Address →								LM ↔ SCLA
Data ID Field	X	1	0	0	← Data →								LM ↔ SCLA
Status ID Field	X	1	0	1	← Status →								SCLA → LM
Command ID Field	X	1	0	1	← Command →								LM → SCLA

†This bit is the output data demand during an address transfer to the LM (see text).

contain a code defining the type of information included in I1 thru I8. The codes utilized are shown in the table and designate the information as the SCLA address, data, an SCLA status report to the processor, or a command from the processor. Each of these are discussed in the following paragraphs.

Address Cell

Each SCLA is designated by a different 8-bit binary address as set by the hexadecimal address switches on the SCLA panel. Thus, when data, input supervision, or output data demand signals are presented to the loop multiplexer from the SCLA, the first operation of the SCLA is to present its particular address.

Data or output supervision presented to the SCLA from the LM is preceded by an address. The SCLA compares this address with the internally preset address. If the two agree, the SCLA accepts the data or supervision. The addressing code format is shown in table 2-2.

In table 2-3 bit position IF3 is the output data demand bit in the address code. When the address is presented to the LM from the SCLA, the bit is a logical 1 if an ODD is present and is a logical 0 if no ODD is present. This bit must be a logical 1 in an output loop address cell (OF3).

Address position A1 is the most significant bit and A8 is the least significant bit in the binary coded address.

Data Cell

The data cell transfers information into or out of the SCLA via the loop multiplexer. The data cell format is presented in table 2-4. Bit D1 is always the first bit received from or transmitted to the modem by the SCLA.

Supervision Cell

The supervision cell on output gives information to the SCLA in the form of commands. On input this cell gives information to the processor in the form of status words from the SCLA.

STATUS WORDS

Most status changes, error conditions, or a status request command cause status to be reported, and two characters are sent to the processor. The status word 1 and status word 2 formats are shown in tables 2-5 and 2-6, respectively. In both tables a logical 1 indicates that the associated modem signal or status condition is active (on), and a logical 0 indicates that the condition is not active (off).

COMMAND WORDS

The command cells are instruction commands from the processor in the form of command word 1, command word 2,

TABLE 2-3. ADDRESS CELL FORMAT

	Loop Cell Bit Position											
	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to SCLA interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
SCLA to LM interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
Bit content		1	1	0/1	A1	A2	A3	A4	A5	A6	A7	A8

Notes: OF - Output format
IO - Information output
IF - Information format
II - Information input

TABLE 2-4. DATA CELL FORMAT

	Loop Cell Bit Position											
	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to SCLA interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
SCLA to LM interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
8- or 9-bit† character		1	0	0	D8	D7	D6	D5	D4	D3	D2	D1
7-bit character		1	0	0	0	D7	D6	D5	D4	D3	D2	D1
6-bit character		1	0	0	0	0	D6	D5	D4	D3	D2	D1
5-bit character		1	0	0	0	0	0	D5	D4	D3	D2	D1

†For a 9-bit character the additional bit is a parity check bit. This is handled internally and does not appear at the SCLA/LM interface; consequently, only eight bits are shown in this table.

TABLE 2-5. STATUS WORD 1 FORMAT

		Loop Cell Bit Position										
	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
SCLA to LM interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
Bit content		1	0	1	CTS	DSR	DCD	RI	QM†	SQD†	ILE	OLE

CTS - Clear to send. This status bit indicates the state of the modem clear to send signal. Active condition indicates the modem is ready to accept data from the SCLA. It must be active to enable data output from the CLA. If this signal changes from a logical 1 to a logical 0 during character output, the current character is completed and the transmit data line is set to marking. A change of state of this signal does not cause status to be reported.

DSR - Data set ready. This status bit indicates the state of the modem data set ready signal. Active condition indicates that power is applied to the modem and that it is connected to the communications line. Any change of state of this signal causes status to be reported.

DCD - Data carrier detect. This status bit indicates the state of the modem receive line signal detector signal. Active condition indicates that a carrier signal is being received by the modem. Any change of state of this signal causes status to be reported. (For the DU139-A SCLA connected to an AT&T 303 Wideband Data Station, this status signal is called AGC Lock.)

RI - Ring indicator. This status bit is set and status reported each time the modem ring indicator signal goes from an on state to an off state. This indicates that the modem is receiving an incoming call from a remote station. The status bit is reset when the status words are sent to the processor.

QM - Quality monitor. This status bit indicates the state of the quality monitor modem signal. Off or 0 condition indicates that the adaptive equalizer in the modem receiver is reset or retraining itself automatically due to poor error performance. Any data received has a "high" probability of error. When on or 1, the automatic equalizer is in its normal trained mode and received data should have a "low" probability of error. Any change of state of this signal causes status to be reported.

SQD - Signal quality detector. This status bit indicates the state of the modem signal quality detector. It functions similarly to DCD but provides a fast responding indication of the presence (1) or absence (0) of a data carrier signal from the remote station. Any change of state of this signal causes status to be reported.

ILE - Input loop error. When set to a 1, the bit indicates that the LM has detected a loop error while the SCLA was using the input loop. This status is reset when the status words are sent to the processor.

OLE - Output loop error. When set to a 1, this bit indicates that the LM has detected a loop error while the SCLA was using the output loop. This status is reset when the status words are sent to the processor.

† DU138-A SCLA only; a logical 0 appears in these positions for DU139-A and DU140-A SCLAs.

TABLE 2-6. STATUS WORD 2 FORMAT

	Loop Cell Bit Position											
	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
SCLA to LM interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
Bit content		1	0	1	PES	DTO	0	NCNA	0	0	0	0

PES - Parity error status. This status is generated when the SCLA has been instructed to check for even or odd character parity and a character is received with incorrect character parity. The status always appears in the same line frame as the character. This status is reset when the status words are sent to the processor.

DTO - Data transfer overrun. This status is generated by the SCLA when it has a data character that is ready for transfer to the LM before the LM has accepted the previously assembled character. The previously assembled character is lost. This status is reset when the status words are sent to the processor.

NCNA - Next character not available. This status indicates that while the SCLA was in the process of transmitting, the next character was not received from the LM in time to maintain continuous character output. Thus character frame synchronization was lost. The output section must be enabled (output on active) for this status to occur. The status sets only once and does not repeat until the NCNA condition is alleviated (by receiving a character to output) and then can recur. The status is reset when the status words are transferred to the processor.

TABLE 2-7. COMMAND WORD 1 FORMAT

	Loop Cell Bit Position											
	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to SCLA interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit content		1	0	1	RTS	RSYN	0	NSYN, LT†	DTR	0	ION	OON

RTS - Request to send. A logical 1 activates the request to send line to the modem while a logical 0 in this position deactivates RTS.

RSYN - Resynchronize. When the input of the SCLA is activated, a logical 1 causes the SCLA to drop input synchronization and search for a new synchronization sequence. (This is a momentary, nonstored command. This bit position should normally be a logical 0.)

NSYN - New synchronization. A logical 1 in this location tells the SCLA to notify the modem via the new synchronization interface signal that another message is coming contiguous to the present message and the modem should drop and reestablish bit synchronization. This command should normally be on for one ms or more, depending on modem type (DU138-A only).

LT - Local test. A logical 1 in this position causes the SCLA to notify the modem to route transmit data back to the SCLA input (DU139-A and DU140-A only).

DTR - Data terminal ready. A logical 1 in this location causes the SCLA to notify the modem that the system is ready to communicate with the modem.

ION - Input on. When this bit is a logical 0, the input section of the SCLA drops out of synchronization and neither receives data characters nor transfers data to the LM. A logical 1 causes the normal acquisition of synchronization and transfer of data.

OON - Output on. A logical 1 causes the output section of the SCLA to report output data demand initially when the command is received if clear to send is active, and enables the output to report output data demand whenever the output buffer is empty. A logical 0 inhibits reporting of output data demand.

†Bit position B7 contains NSYN on DY138-A SCLA and LT on DY139-A and DY140-A SCLAs.

TABLE 2-8. COMMAND WORD 2 FORMAT

	Loop Cell Bit Position											
	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to SCLA interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit content		1	0	1	0	ISR	ISON	LIT	PSET	PI	CO1	CO2

ISR - Input status report. A logical 1 in this position causes the SCLA to report the status of the modem interface lines and any other SCLA status that may be active once each time the command is received. The ISR command is honored only when the SCLA has previously received a logical 1 in the ISON position. (If ISR=1 and ISON=1 appear in the same line frame, status is reported.)

ISON - Input status on. When a logical 1 is placed in this bit position, the SCLA monitors the modem interface and reports status. A logical 0 inhibits monitoring and reporting. Status is not reported automatically when this command bit is first received by the SCLA. The SCLA must receive either an ISR command or status change to report status.

LIT - Loop internal test. A logical 1 in this position causes the SCLA to go into internal loopback test mode. Data and modem control signals from the output section are routed (looped back) to the input section. The SCLA also switches to an internal clock (2.4 kHz) supplied by the LM. Refer to Programming Notes for additional information on this mode of operation. A logical 0 disables the internal loopback test mode.

PSET - Parity set. When this bit is a logical 1, concurrent with PI set to a logical 0, the SCLA generates and checks for even parity. A logical 0 concurrent with PI set to a logical 0 causes the SCLA to generate and check for odd parity.

PI - Parity inhibit. A logical 0 in this position causes the SCLA to check character parity on input and generate character parity on output. A logical 1 causes the SCLA to ignore parity.

CO1, CO2 - Code 1 and Code 2. These bits form a code so that each combination corresponds to a character information length of either 5, 6, 7, or 8 bits. The checking and generation of character parity adds one information bit to the character and therefore must be considered when selecting the unit code level. Table 2-9 shows these code bits in relation to the parity inhibit bit.

and command word 3. Formats for command word 1 and command word 2 are shown in tables 2-7 and 2-8. A logical 1 in the position indicated activates the associated signal, while a logical 0 deactivates the signal. The commands operate independently of each other.

In command word 2 the three least significant bit positions (B9, B10,B11) specify: 1) character length to be employed in interfacing with the external communications facilities, and 2) whether or not parity bits are included in the character(s). Parity bit management applies only to the modem interfaces. There is no parity bit exchange between the SCLA and the LM.

Bit position 9, denoted PI for parity inhibit, commands the SCLA to check for parity upon input and to add a parity bit to the transmitted serial data stream upon output. A PI bit of logical 0 initiates these functions whereas a bit content of logical 1 commands the SCLA to dispense with parity generation and checking. This is indicated in table 2-9, which also presents the code determining character length employed during data transfers with the modem.

The character length, in terms of information content may be either five, six, seven, or eight bits in length. However, if the PI bit is a logical 0, a parity bit is coupled with the information. In this case, the character length may be as long as nine bits. Bit positions 10 and 11 specify the character length without parity and are coded as shown in table 2-9.

Command word 3 contains the synchronization character, which is stored and used for obtaining synchronization. When the SCLA is attempting to acquire character frame synchronization, a 5- to 8-bit sequence (depending on code length) is compared against this stored command at each bit time. The format for this synchronization character command is shown in table 2-10. Bit D1 is the first bit received from the modem.

TABLE 2-9. CHARACTER LENGTH AND PARITY STATUS CODE

Parity	Code (B9-B11)			Character Length (Incl. Parity)
	PI	CO1	CO2	
Yes	0	0	0	6
	0	1	0	7
	0	0	1	8
	0	1	1	9
No	1	0	0	5
	1	1	0	6
	1	0	1	7
	1	1	1	8

While the SCLA is attempting to synchronize, no characters are transferred to the LM. After synchronization is achieved, the SCLA transfers all characters to the LM until the SCLA is directed to resynchronize upon command from the processor.

Each time a command is given to the SCLA, each bit in each command word must be set to the condition desired for the

TABLE 2-10. COMMAND WORD 3 FORMAT

	Loop Cell Bit Position											
	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to SCLA interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
8- or 9-bit†		1	0	1	D8	D7	D6	D5	D4	D3	D2	D1
7-bit character		1	0	1	0	D7	D6	D5	D4	D3	D2	D1
6-bit character		1	0	1	0	0	D6	D5	D4	D3	D2	D1
5-bit character		1	0	1	0	0	0	D5	D4	D3	D2	D1

†For a 9-bit character the additional bit is a parity check bit. This is handled internally and does not appear at the SCLA/LM interface; consequently, only eight bits are shown in this table.

associated function. Failure to do this results in the condition being cleared or set to a different condition. Each time a command is given to the SCLA, the SCLA reads each bit and takes the action dictated.

Whenever the SCLA receives command words, it assumes they are received in order. For example, to change command word 2, both words 1 and 2 must be sent to the SCLA in the same line frame. To change command word 3 all three command words must be sent.

To program command the SCLA to an idle (cleared) state, all bits in command words 1 and 2 must be zeros.

PROGRAMMING NOTES

The following notes provide additional information on the operation of the SCLA and are intended to assist the programmer. Typical input and output operations are presented.

SCLA INITIALIZATION

The SCLA must be cleared before any of the following actions:

1. Power-up of a system in which the SCLA is already installed
2. Installation of the SCLA in an operating system
3. Changing of enable/disable switch from disabled (OFF) to enabled (on)

To clear the SCLA the program must:

1. Send output supervision with command words 1 and 2 set to logical 0
2. Momentarily activate the input status on (ISON) command with the appropriate output supervision. This causes an erroneous status set during the power-up sequence to be reported and cleared

Any input line frames received from the SCLA before completion of the clear process should be ignored.

Once the SCLA is known to be in a cleared state, it can be initialized. Initialization generally consists of sending output supervision to activate ISON, selecting parity option and character length, and loading the synchronization character.

COMMUNICATIONS LINE CONNECTIONS

For switched (dial up) network connections, a ring indicator (RI) status signal indicates that the local modem is receiving an incoming call from a remote station. To cause the modem to answer the call, the program must send a command to turn data terminal ready (DTR) on. When the call has been answered, data set ready (DSR) is turned on and status reported.

For dedicated (private line) network connections, RI and DTR generally are not used. The program can determine the state of DSR by sending an input supervision report (ISR) command and observing the state of DSR status in the supervision data returned.

In either type of network connection, DSR on indicates that the modem is connected to the communications line and data transmission can take place. DSR off at any time indicates that the modem is not connected to the communications line and data transmission cannot take place. Loss of DSR can occur because of any one of the following conditions:

1. Local modem is in a power-off condition.
2. Local modem is in a nondata mode of operation (e.g., alternate voice or test modes).
3. SCLA to modem cable is disconnected.
4. Local modem has gone to an "on-hook" state and logically disconnected itself from the communications line.

INPUT OPERATION

To receive data (transmission block), ION must be activated. When the remote station begins transmission, a carrier signal is applied to the communications line. The local modem detects this carrier and DCD status is reported.

NOTE

In some situations, the carrier is present continuously and is not turned on and off with each transmission.

The transmission block is generally preceded by two or more (typically four) synchronization characters. When the SCLA receives a synchronization character (i.e., acquires character frame synchronization), it transfers all characters received to the processor. The first synchronization character, however, is not transferred.

The transmission block usually contains an end-of-block character (e.g., ETX) that is either the last character of the block or an indication that a predefined number of characters follow (e.g., check characters). When the program receives the last physical character of the block, it must send a command to deactivate ION if another block is not expected from the remote station prior to an output. Alternatively, the SCLA must send an RSYN command if another block could be received immediately.

OUTPUT OPERATION

To transmit data, the output on (OON) command must be activated. Also, request to send (RTS) must be turned on if not so conditioned previously. When the modem is ready to transmit data, it returns clear to send (CTS) signal, which causes the SCLA to generate the first output data demand (ODD). The overall output sequence is shown in figure 2-5. When the program receives an ODD, it should return a character to the SCLA. Each time the SCLA transfers a character from its buffer register to the shift (disassembly) register, it generates an ODD. This sequence is repeated until the last character (character n in figure 2-5) is transmitted. Most communications protocols also require a pad character (normally all marking) be sent (PAD1 in figure 2-5). A second pad character (PAD2) is used for timing purposes to ensure that PAD1 has cleared the SCLA. It is not completely sent if RTS is turned off.

INTERNAL LOOPBACK TEST OPERATION

To operate in the internal loopback test mode, the loop internal test (LIT) command must be sent to the SCLA. Data and modem control signals from the output section are routed (looped back) to the input section as described below:

1. Transmit data (TD) is connected to receive data (RD).
2. Serial clock transmit (SCT) and serial clock receive (SCR) are both connected to an internal 2.4 kHz clock.
3. Request to send is connected to clear to send.
4. DU138-A only: Data terminal ready is connected to data set ready, ring indicator, and signal quality detector.
5. DU139-A, DU140-A: terminal ready is connected to data set ready.
6. DU138-A only: New sync is connected to data carrier detect (receive line signal detector) and quality monitor.
7. DU139-A, DU140-A: Local test is connected to data carrier detect and ring indicator.

While in this mode, all signals received from the modem are blocked and ignored by the SCLA. However, on the output side, signals to the modem are not blocked and caution must be used while in internal loopback test mode to avoid undesirable operation of the modem. For instance, while testing the operation of data terminal ready, an on condition is received by the modem as well as being looped back as in item 4 above. If an incoming call was received in this situation, the modem would answer; this may confuse the calling station since no data transfer would occur. Therefore, DTR should only be turned on momentarily to test its operation and left off during other SCLA tests.

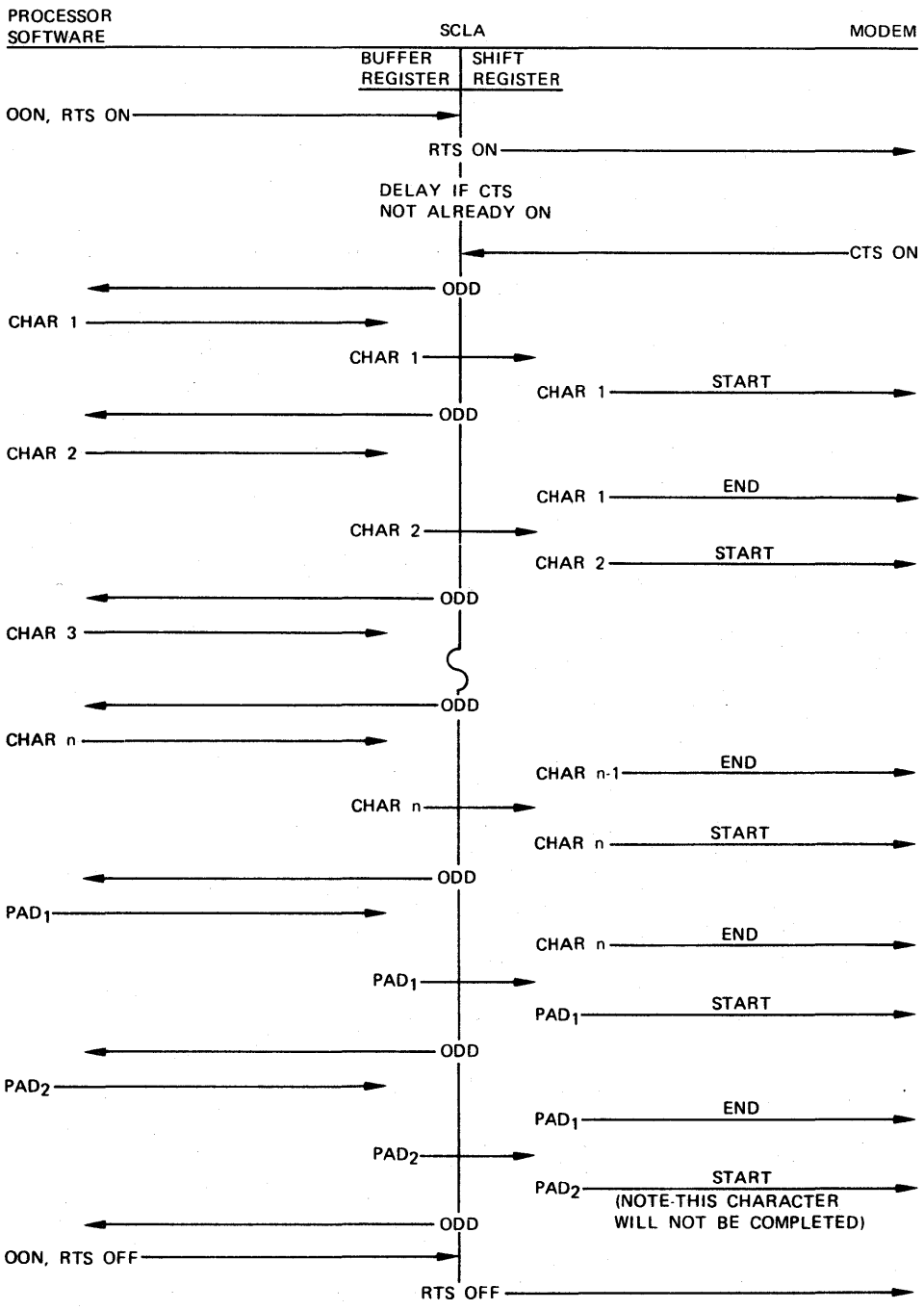


Figure 2-5. Typical Output Procedure

INTRODUCTION

This section covers uncrating of SCLA printed circuit cards and cables, as well as installation, checkout, crating, and shipping.

UNCRATING

CAUTION

Although the integrated circuits and discrete components mounted on the individual printed circuit card can withstand a considerable amount of shock, the units must be handled with care. In no case should units be stacked directly upon one another because the printed circuit foil, components, or integrated circuits may be loosened or broken by such action.

The SCLA may be shipped installed in a CLA and loop multiplexer card cage assembly or independently in a specially padded cardboard shipping container. Regardless of the method used for shipment, carefully unpack the units and check for damage. If any unit was damaged in shipping, refer to section 8:503:00 of the Field Procedures Guide for Customer Engineers for instructions relating to the disposition of damaged equipment.

IDENTIFICATION

CIRCUIT CARD TYPES

The SCLA circuit cards of each type are identical in size and similar in appearance. Although the product number appears on the card, the modem with which each CLA type is compatible must be determined from the cards assembly part number, as shown below:

Product Number	Assembly Part Number
DU138-A	74873381
DU139-A	74873612
DU140-A	74873630

CABLE TYPES

Two cables, one for each SCLA on a circuit card, are required to connect each SCLA to its compatible modem, or directly to a terminal. These cables are not supplied with the SCLA and must be ordered separately. Table 3-1 lists the available cable types and their applications. The cable type is identified by its assembly part number on a band around one end of the cable. Typical cables and the various types of connectors are illustrated in figure 3-1.

TABLE 3-1. SCLA CABLES

Equipment Number	Assembly Number	Application	Wire Type	Connector	
				CLA	Modem
XA131-A	74658500	DU138-A to AT&T 203A modem or equivalent		25-pin plug	25-contact receptacle
XA130-A	74658700	DU138-A to AT&T 201, 203A, 208B modems or equivalent	13 wires AWG 22	25-pin plug	25-contact receptacle
XA129-A	74658900	DU138-A to AT&T 208A, 209 modems or equivalent	13 wires AWG 22	25-pin plug	25-contact receptacle
XA132-A	74659100	DU138-A direct to terminal	9 wires AWG 22	25-contact receptacle†	25-contact receptacle
XA137-A	7466500	DU140-A to CCITT V.35 or equivalent modem	25 twisted pairs, 120-ohm, AWG 24	34-pin plug	25-pin plug
SA136-A	74666700	DU139-A to AT&T 301, 303 modems or equivalent	10 90-ohm coaxial cables	12-pin Bundy coaxial plug	25-pin plug

† Has threaded retaining spacers

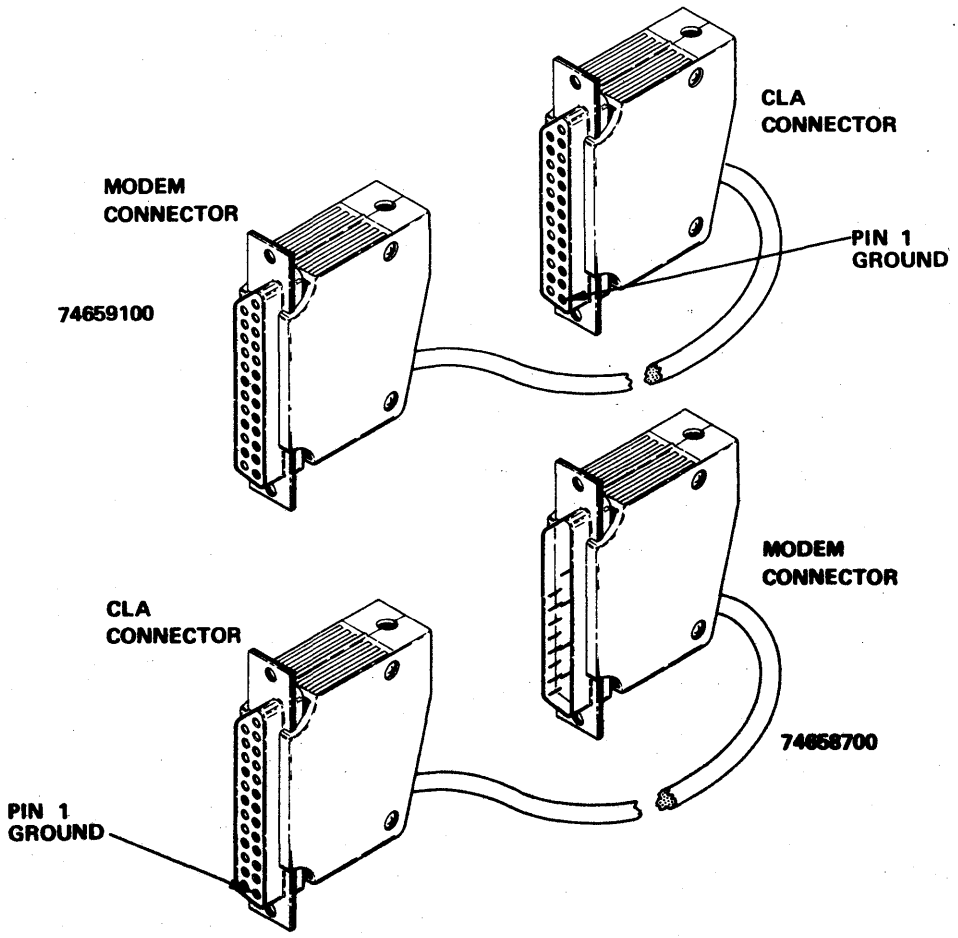


Figure 3-1. Typical SCLA Cable Connectors

INSTALLATION

CARD LOCATIONS

SCLA circuit cards are installed in a CLA and loop multiplexer card cage assembly. See figure 1-2. There may be one basic card cage and from one to three optional cages used in the multiplexing subsystem, all identical. If only one card cage is used, it is located in the lower section of the left-hand bay (in a double-bay cabinet configuration). See figure 3-2.

There are 18 card slots in each card cage, but the two rightmost slots are reserved for LM cards. SCLA cards can be installed in any or all of the remaining 16 slots.

The three optional card cages have the same capacity as the basic card cage and are known as communications line expansion (CLE) units.

The first optional expansion provides the second card cage assembly, which is mounted in the center of the cabinet above the first cage.

The second optional unit provides the third card cage assembly, which is mounted in the lower section of the second (right-hand, viewed from the front) bay. This option also includes a blower assembly and a power supply.

The third optional unit provides a fourth card cage assembly, which is mounted in the center section of the right-hand bay of the cabinet. This unit uses power and cooling from the second optional unit.

CARD LOCATION PRIORITIES

Because each CLE card cage assembly is identical in configuration and each CLA is the same as another in size, a CLA card can be physically installed in any card slot of any LM card cage.

Although random insertion of CLA cards into any of the available slots is permissible, best system performance is obtained when the cards having the highest character rates are inserted into the highest priority slots.

Character rate is the bit per second (bps) rate divided by the unit code. Thus:

$$\text{character rate} = \frac{\text{bps}}{\text{unit code}}$$

where the unit code equals the number of bits per character, including parity bits.

Each card cage is organized so that the leftmost card slot, as viewed from the front, has the highest priority, and each succeeding slot to the right has a lower operating priority

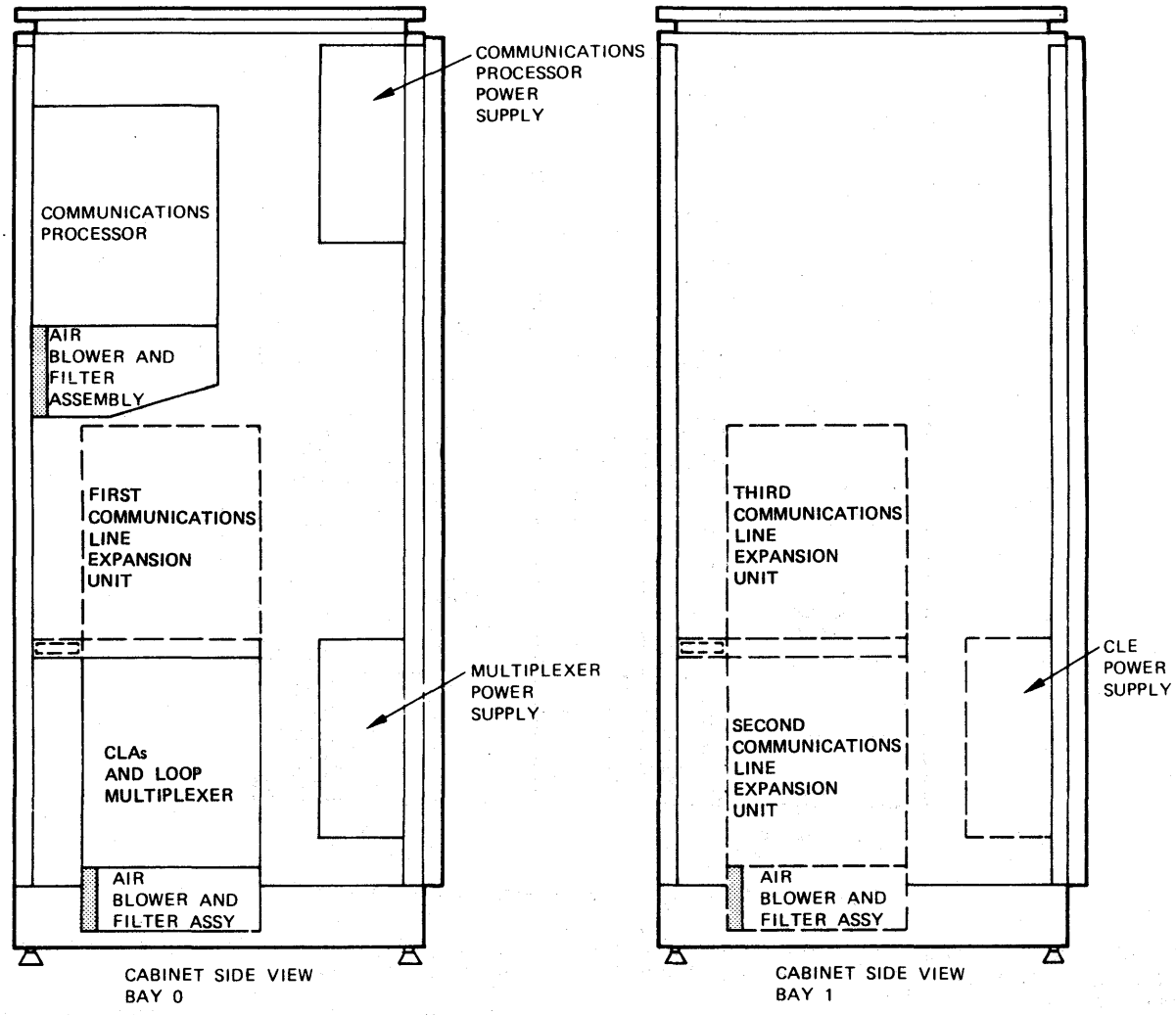


Figure 3-2. Component Location, Double-Bay Cabinet Configuration

than its neighbor on the left. Moreover, CLA1, as labeled on a card, has a higher priority than CLA2 on the same card.

If the system has more than one CLA card cage, the LM with highest priority has its upper cable connected to the MLIA. The LMs are connected serially so that the LM with top priority has its lower cable joined to the upper connector of the LM next in operating priority. These priorities of interconnection are illustrated in figure 3-3.

CARD INSTALLATION

CAUTION

Do not attempt to install an SCLA card in the communications processor card cage, located at the top of the basic cabinet. If attempted, the communications processor backpanel will be damaged.

SCLA cards are installed in the CLA and LM card cage assembly as follows:

1. Set both CLA1 and CLA2 enable/disable switches to the OFF position.
2. Position the card vertically so that the two connectors on the card handle are on the lower part and thumbwheel switches are on the upper part.
3. If the system is operating, set the thumbwheel address switches on the card handle to the proper hexadecimal address before installing the SCLA card. Refer to Controls and Indicators, section 2, for the method of setting an address.

CAUTION

Ensure that the 51-pin tab connectors on the rear edge of the card are properly aligned with their mating connectors on the card cage backpanel. Cross-slotting will destroy the backpanel.

4. Insert the rear edge of the card into the slotted guides, making certain that the card is perfectly vertical and not cross-slotted.
5. Slide the card into the card cage, applying firm pressure on the card handle to engage the connectors on the card with backpanel connectors. All card handles will be flush with one another when cards are correctly installed.

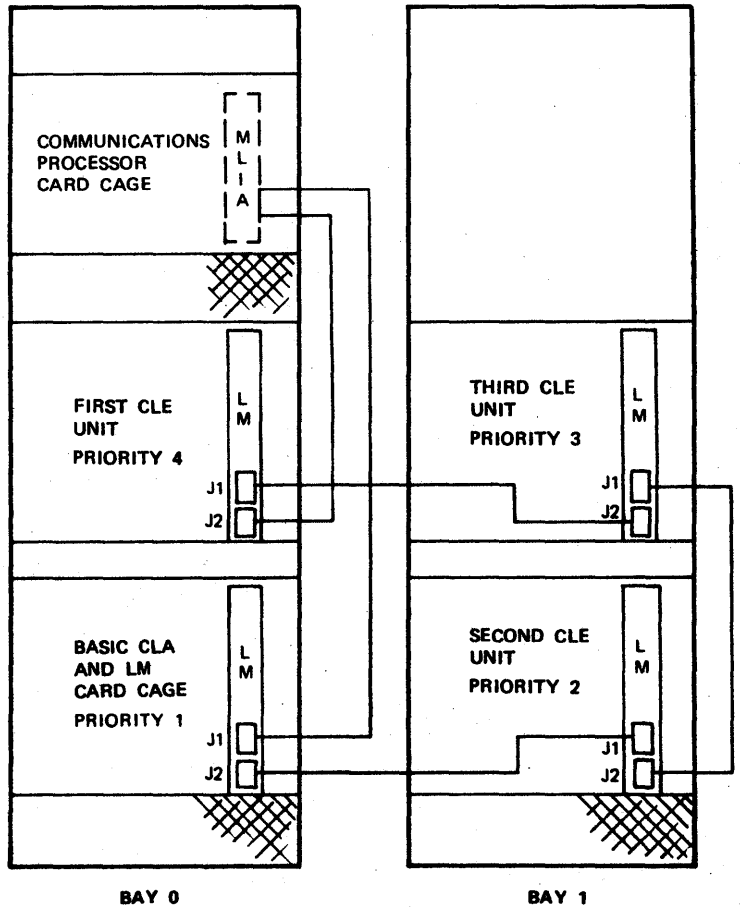


Figure 3-3. Loop Multiplexer Interconnection Priorities

6. Position blank slot covers in all card slots that will not be used to assure that blower air flow is contained in the card cage.

CABLE INSTALLATION

SCLA cables are installed as follows:

1. Select a cable that is compatible with the terminal or modem to be connected to the SCLA. See table 3-1 for the cable identification.

2. Attach cable to terminal or modem, then attach the other end of the cables to the SCLA card handle. All cables egress through the bottom of the cabinet. For SCLAs installed in the upper CLEs, route the cables through the cable tray provided to either side and then down along the side to the bottom of the cabinet.

3. Tighten down retaining screws on all cable connectors.

4. Lay out the surplus length of cable in a long, flat loop under the raised floor or in enclosures; this manner of storage minimizes kinking of cables.

5. Place protection padding, if available, over stored loops of cable before installing flooring.

INITIAL CHECKOUT

After all SCLA cards are installed and connected, diagnostic or system programs can be used to determine overall SCLA function.

If a fault is isolated to the SCLA, the following mechanical checks may be made:

1. Check that SCLA cable connectors are firmly attached.

2. Ensure card is firmly placed in the card slot.

3. Set both CLA1 and CLA2 enable/disable switches to the enabled position.

4. Monitor LED indicators under SCLA card handle to ensure electrical power is on the SCLA card.

5. If power is not on the SCLA card, check LED indicators on LM card handle to ensure power is passing through LM card to SCLA card.

CRATING AND SHIPPING

If SCLAs are to be shipped installed in a card cage assembly, the packaging must be designed to hold the SCLA cards securely in place during shipment, as well as to provide protection for the exterior of the card cage.

If the SCLA is to be shipped independently, it must be packaged in a well-padded cardboard container to protect the integrated circuits, discrete components, and printed circuit foil from damage during shipment.

Packaging should conform to the requirements of CDC Procedure 13-002, Packaging and Material Handling Documentation.

INTRODUCTION

This section describes the theory of operation for the SCLAs. Information is applicable to all three models except where differences are specified, as in the Modem Interface subsection of this section.

Each SCLA circuit card contains two separate SCLAs identified herein as SCLA1 and SCLA2. This description refers primarily to SCLA1. The SCLA2 portion is mentioned only in the description of certain circuits shared by both SCLAs.

SCLA1 contains three major functional sections: output, input, and modem interface. Refer to the logic diagrams in Section 5 as an aid to understanding the following information.

NOTE

In the descriptions and diagrams in this section, all mnemonics for signals that are active in the low or off condition are marked with an asterisk. Mnemonics shown without asterisks are active in the high or on state.

OUTPUT SECTION

The output section of the SCLA receives commands and data via the output loop multiplexer (LM) bus. The information in these command words is used to control both the output and input sections of the SCLA. Data received by the SCLA in parallel is shifted out serially to the modem.

BUS BUFFERS

All signals originating at the LM are interfaced to the SCLA in such a way that no more than one TTL load is created by the SCLA inputs. For the most part, this buffering is accomplished with inverters.

SELECT OUTPUT

Commands and data are only recognized by the SCLA after it has been selected. Each SCLA has an 8-bit address, which is set by two hexadecimal thumbwheel switches located on the card handle. The same address is used by both the output and input sections. When the LM has information for the SCLA, the LM places a unique address on the bus along with an output-select (OSL) signal. (A timing diagram of the LM to SCLA output interface is shown in figure 4-1). This address is compared with the setting of the address switches. Two 4-bit comparators are cascaded together with OSL applied to one of the "equals" inputs. If the address of the SCLA and the one presented to it are the same, OSL enables the output of the lower comparator, which is cascaded to the input of the upper comparator, forcing its output "high". This signal is applied to the J input select-output (SELO1) flip-flop.

On the rising edge of output strobe (OSTA*), SELO1 sets. The SCLA's output is now selected and is prepared to accept commands or data until it is deselected. When the LM has provided all information in a particular line frame to the SCLA, it causes output-select-clear to go to logical 1. This signal is applied to the $\overline{K}$ input of SELO1. On the rising edge of OSTA*, SELO1 resets, thus deselecting the output.

FORMAT DECODE

Output format code 2 and 3 (OF2 and OF3) are monitored by a 2-to-4 decoder, which looks for a data or supervision (command) format code. If OF2 and OF3 are inactive, a data format is assumed and output-data cell (ODATA) becomes true; this enables acceptance of a data character if the SCLA is selected. Likewise, if OF2 is inactive and OF3 is active, a supervision format is assumed and output-supervision cell becomes true, enabling the command counter.

COMMAND COUNTER

Since all commands given to the SCLA have the same format code, the SCLA must keep track of the sequence of commands so that it may route them to the proper section of the logic. The command counter accomplishes this task. It is implemented via a shift register. When any format other than supervision is seen by the format decode, the command counter is reset.

The $\overline{Q}$ (NOT Q) of the first stage represents command 1 (COM1). When a supervision code is detected, OSUP goes high and releases the reset, gating the COM1 signal out to the COM1 register. On the next rising edge of OST*, the counter is advanced to command 2 (COM2), then is advanced to COM3 on the following OST*. When the output format code (OF2, OF3) changes, the counter is again reset by OSUP*. Both the format decoder and the command counter are used by both SCLAs.

COMMAND REGISTERS

All stored commands (i.e., other than input-status-request [ISR] and resynchronize [RSYN]) are strobed into the command holding registers. There are three of these registers, one for each of the commands. Each register consists of a D-type register with a common clock and a clock-enable gate. After the SELO1 flip-flop is set, OST is enabled. OST is then gated with COM1 so that on the falling edge of the OST, the COM1 register is loaded with the information output bits at its D inputs. The Q outputs of this register are now associated with the function they control, i.e., request-to-send, new-sync, data-terminal-ready, input-on, output-on. This register does not change until COM1 is detected and SELO1 is true. The COM2 register is loaded in the same manner except that COM2 is gated with OST to produce its clock. The functions loaded into the COM2 register are input-status-on, loop-internal-test, parity-set, parity-inhibit, codes 1 and 2. COM3 is gated with OST to produce the clock for the SYNC register, which stores the character used by the input section for character synchronization. All signals stored in the command registers are active high.

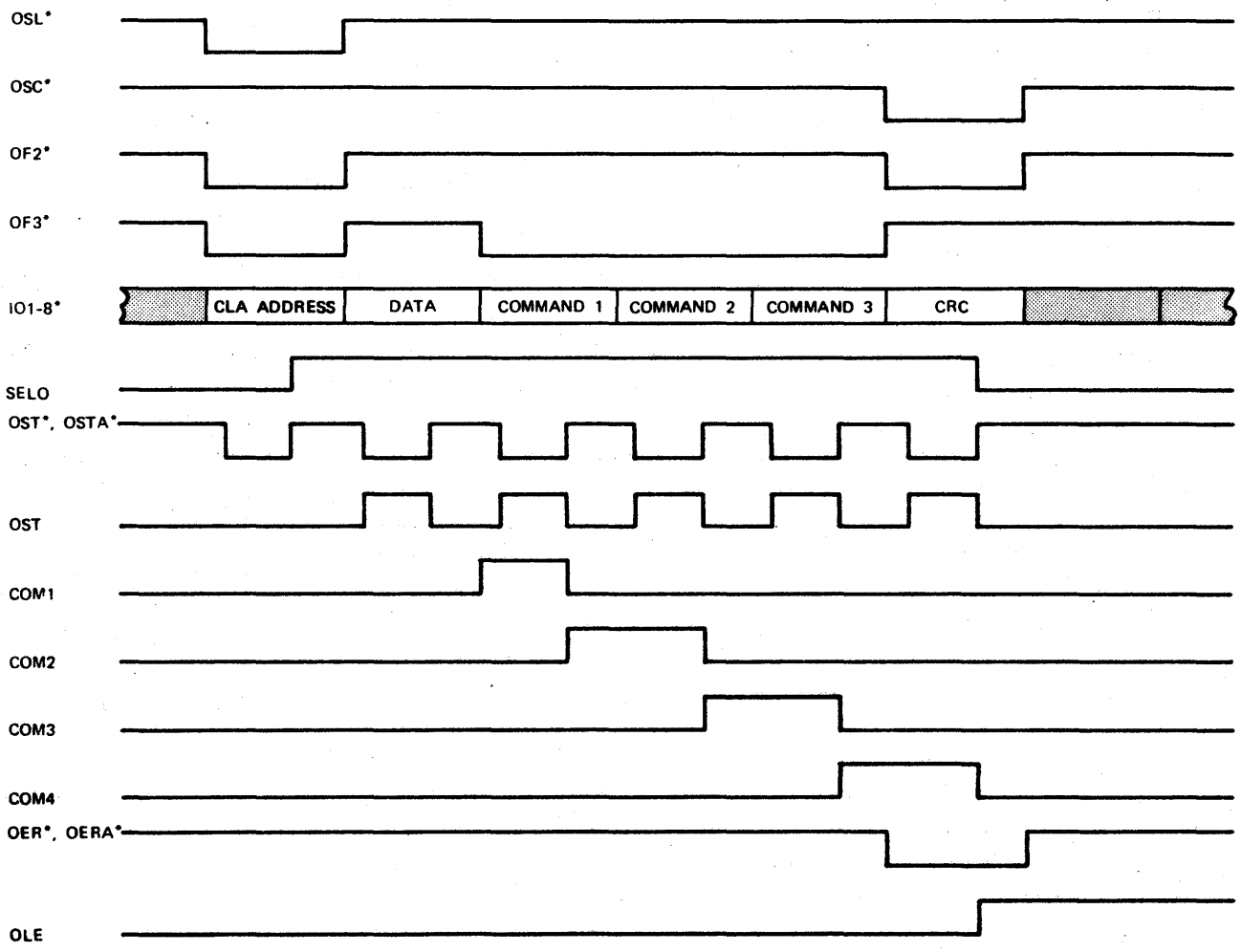


Figure 4-1. LM-to-SCLA Output Interface Timing Diagram

SYNCHRONOUS TRANSMITTER

The synchronous transmitter is a 40-pin LSI chip whose primary function is to make the parallel-to-serial conversion of the data and provide the proper character timing. It is completely programmable by the processor via the COM1 and COM2 commands, which were discussed in section 2. A functional block diagram of the transmitter is shown in figure 4-2. Also, a timing diagram for the transmitter function is shown in figure 4-3.

The synchronous transmitter has four main functional areas: transmitter holding (buffer) register (THR), multiplexer, transmit shift register (TSR), and timing and control. The THR accepts the parallel data on lines IO1 thru IO8 when it is strobed with THR load. THR empty (THRE) indicates the character strobed into the THR has been transferred to the TSR. The multiplexer allows either the character in the THR or a marking fill character to be transferred to the TSR. The TSR shifts out serially the data transferred to it with every rising transition of the serial-clock-transmit (SCTA) signal. Timing and control is responsible for the loading of the THR and the TSR, and is programmed via the parity-set (PSET), parity-inhibit (PI), CO1, CO2, and mode-select 1 (MS1) signals.

NOTE

MS1 is an input that involves isosynchronous mode of operation, and thus it is not used for the SCLA.

The character transferred into the TSR occurs at the center of the last bit of the character being transmitted. If, at this time, no character has been loaded into the THR, the fill character, all marking, is loaded into the TSR at the end of the bit being transmitted, and data-not-available ($\overline{DA}$) is set to a 1, indicating this condition. $\overline{DA}$ is reset with data-not-available-reset ($\overline{DAR}$). The fill character is repeatedly transmitted until the THR is loaded with another character. This new character is always contiguous with the last fill character.

The THRE flag indicates that the THR is empty and may be loaded with a character. Data on IO1 thru IO8 is loaded into THR when THRL is a low level, forcing THRE flag to a low level.

If the clear-to-send-status (CTSS) input is a 0 or if the TSR is in the process of transmitting a character, the character in the THR is not transferred to the TSR and THRE remains at a low level. Raising CTSS to a 1, or completion of

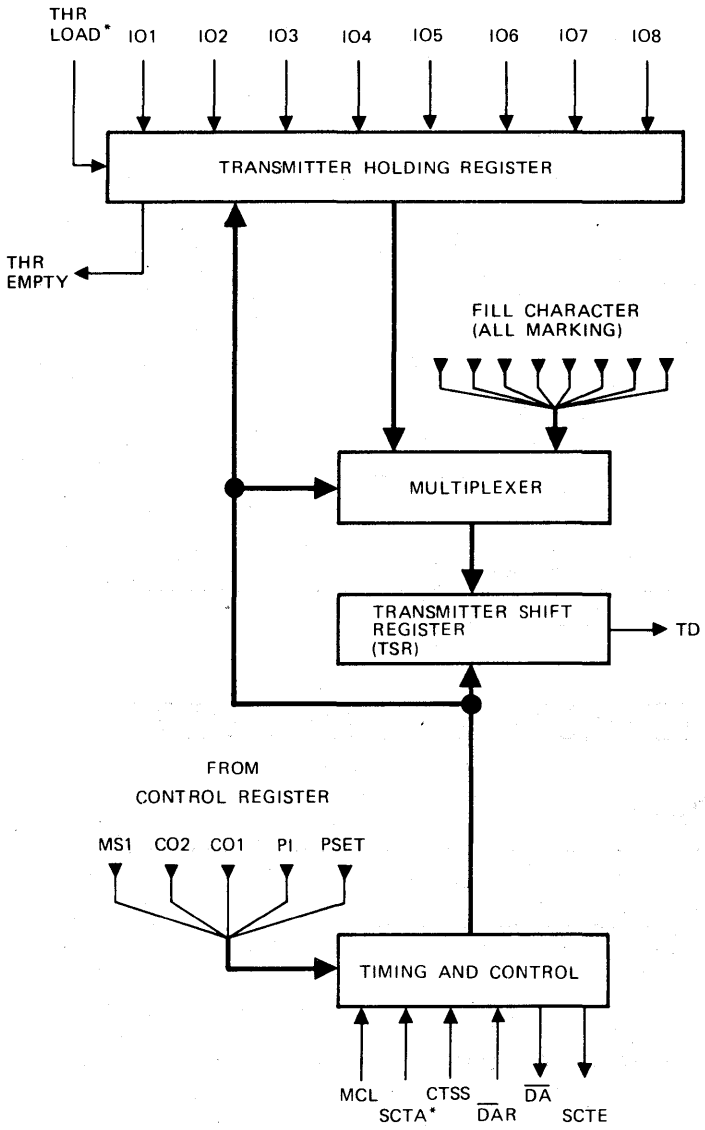


Figure 4-2. Synchronous Transmitter Block Diagram

transmission of a character from the TSR, causes the automatic transfer of the character in the THR to the TSR, forcing THRE to a 1. The selected parity is appended to the data during the transfer to the TSR and serial transmission is initiated. If CTSS goes to 0 during transmission, only that character is completed, after which transmit-data (TD) remains in a marking condition until CTSS is 1 again.

The synchronous transmitter enters an idle state when master clear (MCL) is 1. In this state all timing and control logic is reset, TD continues to mark and THRE goes to a 1.

Serial-clock-transmit-external (SCTE) signal has the same period as SCT but its rising edge is coincident with TD bit boundaries so that the falling edge of SCTE is in the bit center.

OUTPUT DATA DEMAND

When the SCLA is available to output data, it sets the output-data-demand (ODD) flip-flop which causes the input-available signal to be active. This signal informs the processor that it can send another character to the SCLA. The ODD flag bit is picked up when the input section is selected, and at that time the ODD flip-flop is reset.

THRE and OON are gated together to produce the clock for the ODD flip-flop (D-type). Since the D input is pulled up, the ODD flip-flop sets whenever THRE is 1 and OON makes a 0-to-1 transition, or whenever OON is active and THRE makes 0-to-1 transition. Resetting of the ODD signal flag is discussed in the input section.

OUTPUT DATA

After receipt of an ODD flag from the SCLA, a new character is sent by the processor to the SCLA output section. SELO1 is set to 1 when the correct address is detected. When a data format is detected by the format decoder, output-data (ODATA) goes to 1. The SCLA now assumes that the information on IO1 thru IO8 is a character to be outputted and loads it into THR when THRL* goes to 1. THRL* is derived by NANDing OST, ODATA, OON and output error (OERA*). THRL goes high again on the rising edge of OST*.

The loading of the character into the THR causes THRE to go to 0. When the character is transferred to the TSR, the THRE signal again goes to 1 and sets the ODD flip-flop.

If the THR has not been set with a new character prior to the falling transition of SCTA in the center of the last transmitted bit (the falling transition of SCTA) of the character in the TSR, the DA flag is set to 1. This signal in turn clocks the next-character-not-available (NCNA) flip-flop to a set condition if OON is active (OON enables the D input of NCNA). DA is reset with $\overline{DAR}$*, which is produced by NANDing OON, SODD*, and $\overline{DA}$ (delayed by two LPTTL inverters). When NCNA is set, IAV* becomes active, telling the LM that SCLA has status for the processor. NCNA status is picked up when the input is selected, at which time the NCNA flip-flop is reset. This is discussed in the input section.

Transmit-data (TD), the output from the TSR, is fed to the modem interface section for level conversion and transmission to the modem (or terminal). In addition to the functions that OON serves, its inversion is applied to the MCL of the synchronous transmitter, causing it to be reset to an idle state when OON is a logical 0.

OUTPUT LOOP ERROR

Whenever the LM detects an error condition on the loop while strobing output information to the SCLA, it also sets the OER* line (a bussed signal) to a true state coincident with IO1 thru IO8. OER is gated with SELO1 and applied as a low level to the D input of the output-loop-error (OLE) flip-flop, which is then clocked on the rising edge of OSTA*. This action stores the error condition. OLE causes IAV* to become active, telling the LM that the SCLA has status for the processor. OLE status is picked up when the input section of the SCLA is selected, at which time the OLE flip-flop is reset. This resetting is described in the input section.

INPUT SECTION

The input section of the SCLA is responsible for the transference of data and various statuses to the processor via the LM. Information is transferred in 11-bit parallel bytes (three format bits and eight information bits). It

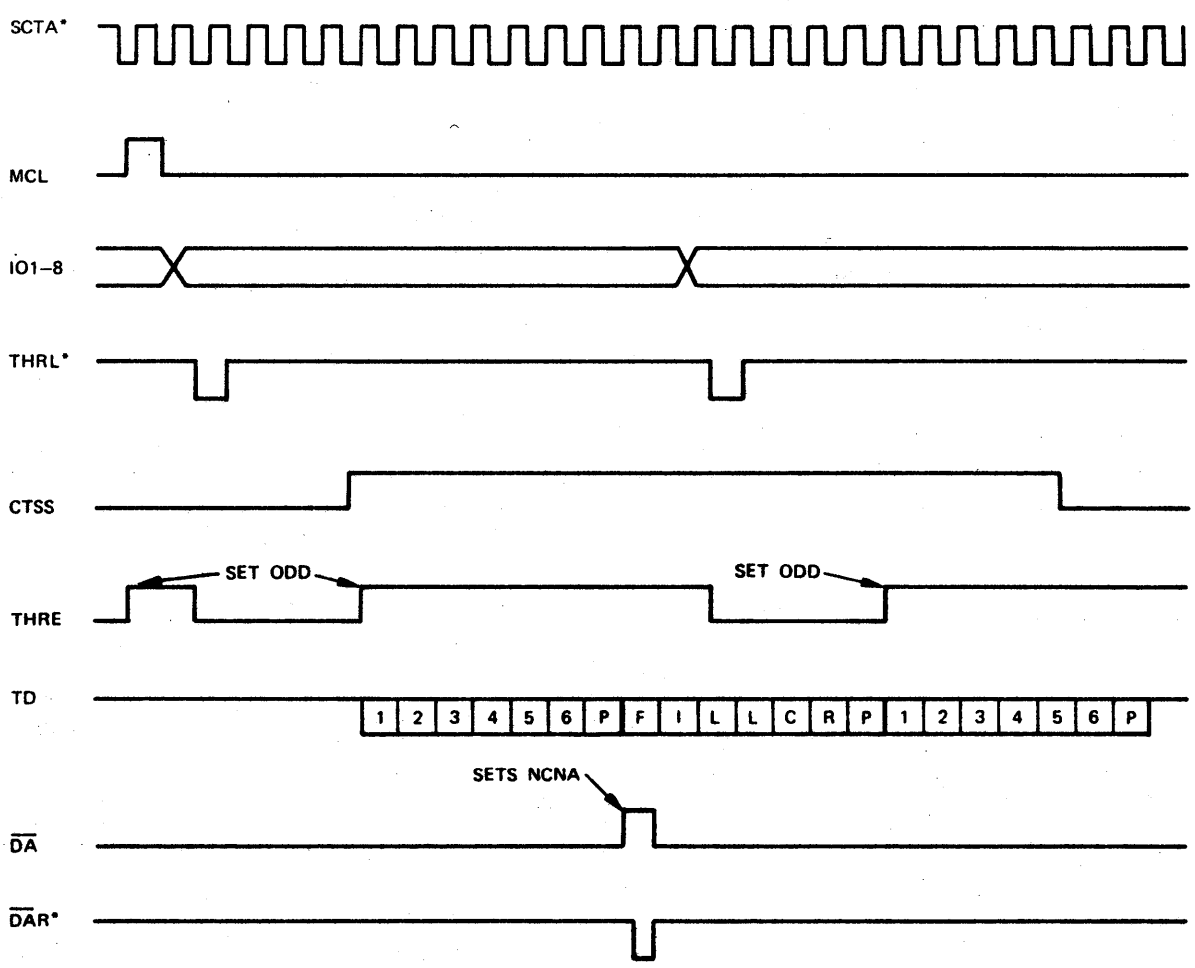


Figure 4-3. Synchronous Transmitter Timing Diagram

performs the serial-to-parallel conversion of data incoming from a modem or terminal device. The input section receives commands from the output section to program its characteristics.

SYNCHRONOUS RECEIVER

The synchronous receiver is another 40-pin LSI chip which is responsible for coordinating character assembly (serial-to-parallel conversion) and the setting of character-associated statuses of parity-error-status and data-transfer-overrun status. It is completely programmable via commands 1, 2, and 3 from the output section of the SCLA. A block diagram of the synchronous receiver as it is used in the SCLA is shown in figure 4-4. A timing diagram for the synchronous receiver is shown in figure 4-5.

Incoming synchronous data appears as a continuous bit stream of contiguous characters at receive-data. Character synchronization is accomplished by comparing this bit stream with the SYN character pattern which is present at S1 thru S8 inputs to the synchronous receiver.

The synchronous receiver has four main functional areas: receiver timing and control, receiver register, receiver comparator, and the receiver holding (buffer) register. The timing and control logic accepts parity and word-length command signals (parity-set command, CO1, CO2) which it uses to determine character timing.

NOTE

Mode-select 1 (MS1) signal is an input to the LSI chip that puts the synchronous receiver in an isosynchronous mode and therefore is not used for the SCLA.

When a character has been received, it is loaded from the receiver register to the holding register. The receiver comparator compares the incoming serial data bit-by-bit with the SYN character at S1 thru S8 inputs and notifies the timing and control when the two are the same. The receiver register is a shift register with input (receive-data) connected to the serial input data stream and clocked with serial-clock-receive (SCR). The holding register is parallel-loaded at the end of a character time with the information in the receiver register.

A high level on the synchronization-search (SS) input enables the synchronous receiver to look for SYN character. The holding register is transparent and its contents are identical to the receiver register. The data stream clocked into receive-data (RD) by the negative transition of SCR shifts

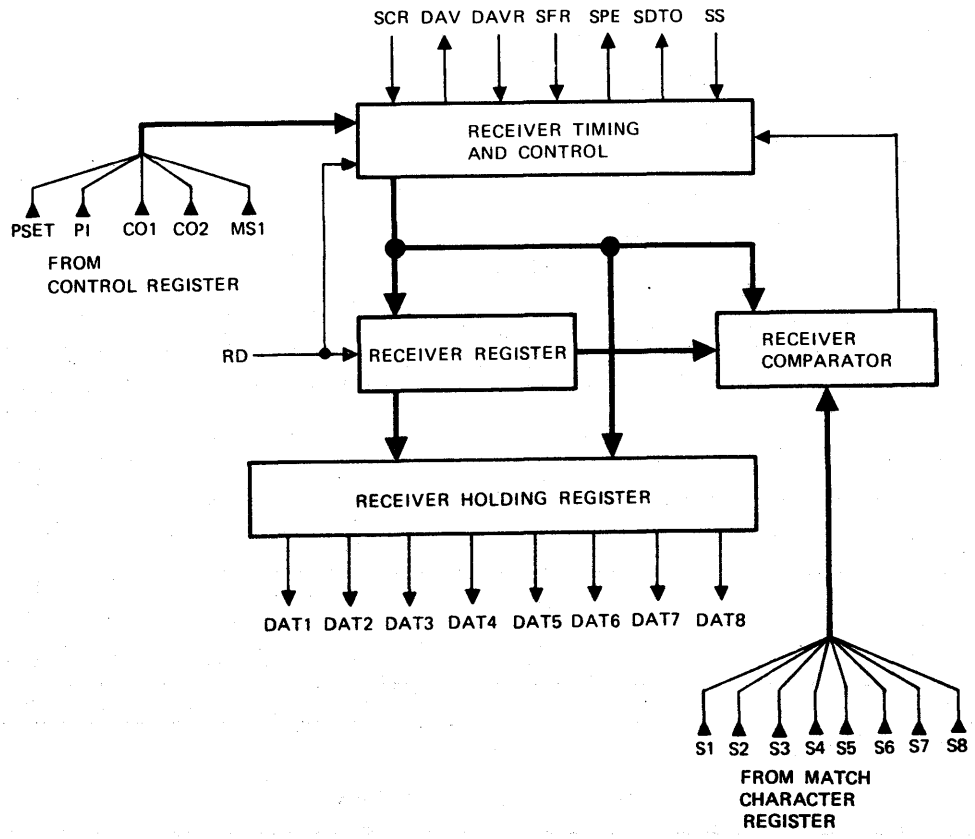


Figure 4-4. Synchronous Receiver Block Diagram

through the receiver register and is compared with the preprogrammed SYN character at inputs S1 thru S8.

A match returns the holding register to its nontransparent state and initializes timing and control logic but does not set data-available (DAV). The character immediately following the match is transferred to the holding register at the receipt of the center of the last bit, at which time DAV is raised to logical 1, notifying the LM of a character available.

DAV is normally reset to logical 0 by reset-data-available (RDAV*) when the LM picks up the character present on the outputs of the RHR (DAT1 thru DAT8). If this does not occur and another character time has elapsed, the contents of RHR are loaded with the new character overwriting the old one, causing set-data-transfer-overrun (SDTO) to set to 1 and indicating a data transfer overrun.

Parity, if programmed, is verified upon receipt of the center of the parity bit, the last bit of a synchronous character. If a parity error exists, set-parity-error (SPE) is set to logical 1.

Both SDTO and SPE are reset by status-flag-reset (SFR*). When SS goes to 0, character synchronization is lost and the receiver holding register is again transparent.

The synchronous receiver is forced to a defined idle state when master-clear (MCL) is pulsed to a 1. In this state all timing and control logic is reset (SDTO, SPE, and DAV go to 0) and the holding register outputs (DAT1 thru DAT8) are set to 1.

CHARACTER ASSEMBLY

Before the SCLA can receive serial data and transfer it to the LM, it must be programmed (via the output section) to the proper character length and parity or no parity. ION must also be set to 1, and the synchronization register must be loaded with a character.

ION* is ORed with RSYN* to reset the SS logic. When ION* goes to a high level, the SS synchronization search shift register is released. The first-stage input is pulled up to a 1 so that, when serial-clock-receive (SCR*) makes a high transition, this bit is transferred to the second stage, and so on to the third stage with each transition of SCR*. The third stage is applied to the SS input on the synchronous receiver, allowing it to look for the bit pattern that is in the SS register. This signal remains high until the SS register is reset with either ION* or RSYN*. ION is also indirectly applied, through ORing functions, to reset-data-available (RDAV*) and status-flag-reset (SFR*) inputs to the synchronous receiver, disabling DAV, SPE, and SDT, when it is logical 0. So, when ION goes to a logical 1, DAV, SPE, and SDTO of the synchronous receiver is allowed to search for a synchronization character. This is a requirement of the synchronous receiver.

Upon detection of a synchronization character, the synchronous receiver is character synchronized. DAV sets to logical 1 in the center of the last bit of the subsequent character and that character appears at DAT1 thru DAT8, ready to be given to the LM. The DAV signal is ORed with status-available (SAV) and output-data-demand (ODD) to produce IAV* (if select-input [SELI] is not active), telling the LM

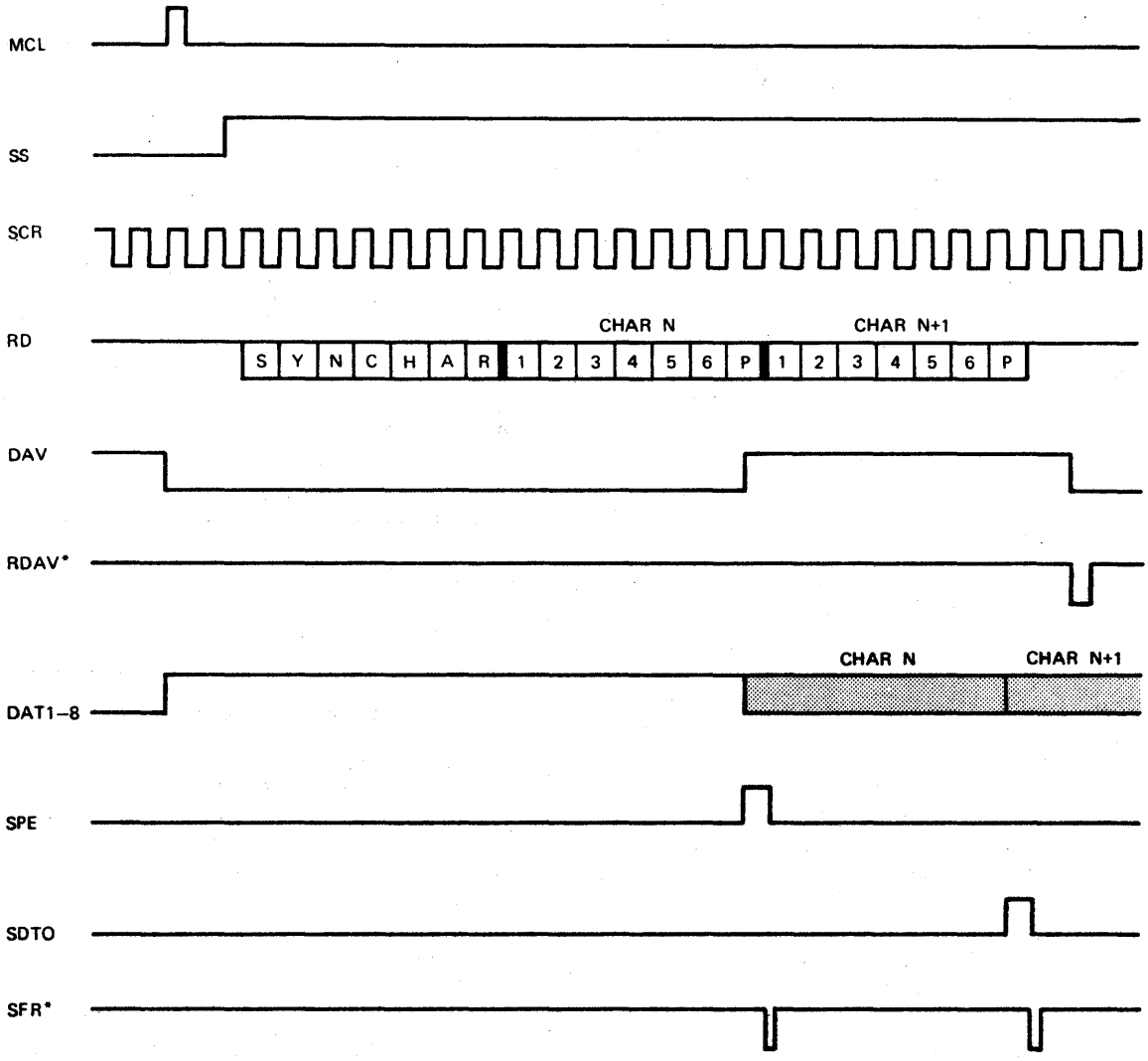


Figure 4-5. Synchronous Receiver Timing Diagram

that the SCLA has information for it. DAV is reset by the input control logic when the character is picked up by the LM.

If DAV is not reset by the center of the last bit of the next character after which it was posted, SDTO output from the synchronous receiver is set, indicating a character overrun error condition. This signal is inverted and direct-sets the DTO flip-flop. SDTO is delayed by three LPTTL gates to produce SFR*, which resets SDTO. DTO is ORed with modem-status (MODST), PE, NCNA, ILE, and OLE to produce IAV* if ISON command signal is active. DTO is also applied to one of the inputs of the status register. When the input of the SCLA is selected, the status register is clocked to produce the DTO status bit which is picked up as a bit in the second input supervision word. At this time DTO is reset.

If the synchronous receiver is programmed for parity and detects an error in the center of the parity bit, it sets the SPE to 1. This signal is inverted and direct-sets the PE flip-flop. SPE is delayed by three LPTTL gates to produce SFR*, which resets SPE. PE1 is ORed with DTO, MODST, NCNA, ILE, and OLE to produce IAV*, if the input-status-on (ISON) command is active. PE is also applied to one of the inputs of the status register. When the input of the SCLA is selected, the status register is clocked to produce PES, which is picked up as a bit by the second input supervision word. At this time PE is reset.

INPUT CONTROL LOGIC

The input control logic is activated when the input section is selected. This logic produces all signals that control the SCLA logic-to-LM input interface, and is used by both SCLA1 and SCLA2 on a time-sharing basis. It consists basically of a 2-bit states register (IC1 and IC2), a states decoder, a holding register, multiplexer, and other miscellaneous control logic. Diagrams of the input control and related signals are given in figures 4-6 to 4-9, for all the possible combinations of input frames.

If the LM selects the input section by dropping input-select (IS*) to a low level and providing input strobes (IST), on each falling transition of IST* the SCLA places information cells

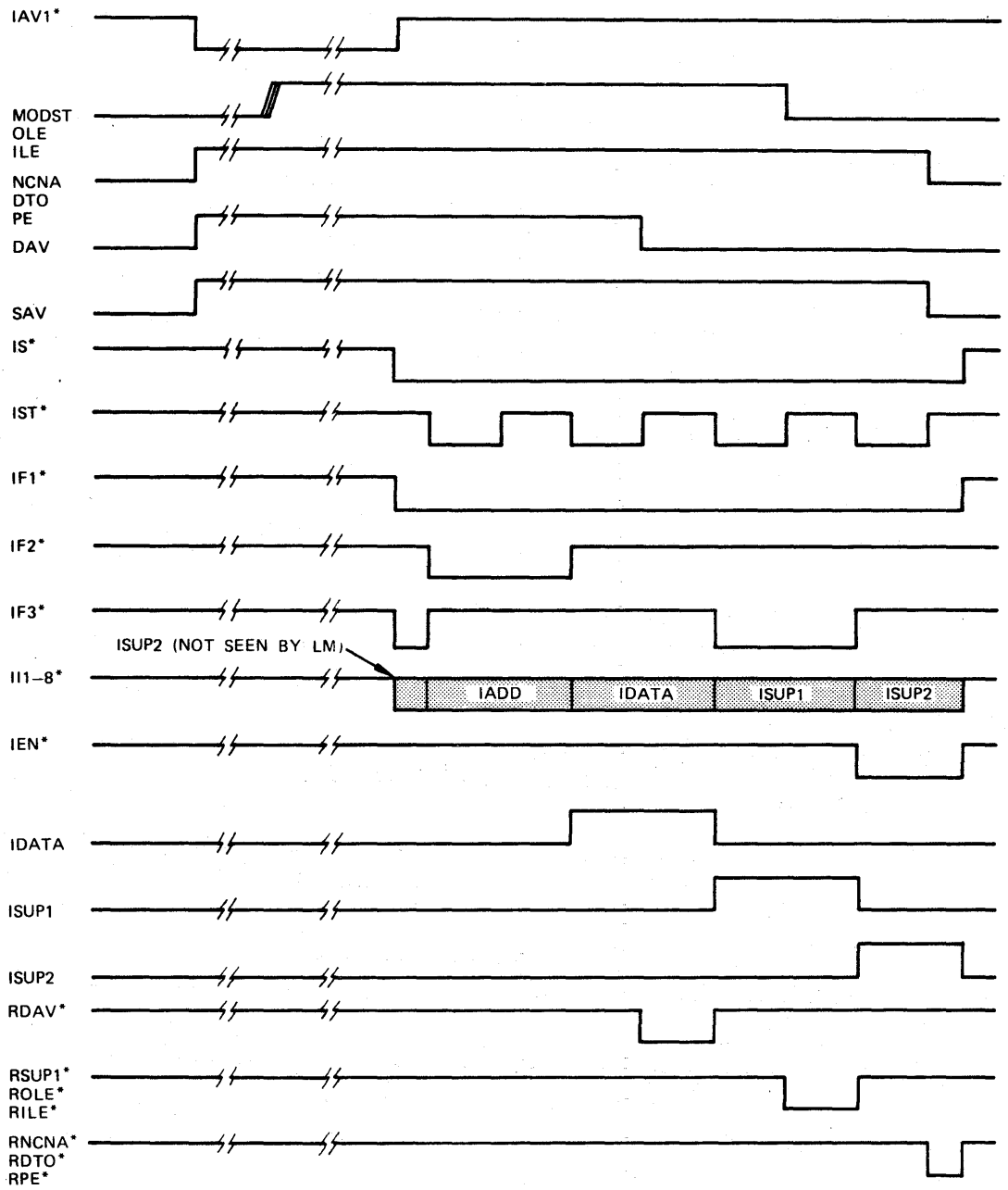


Figure 4-6. Input Control Timing Diagram - ODD, Data and Supervision

(address, data, or supervision) on the input bus. The LM picks up information on the rising edge of IST*. This transference continues until the input control logic activates the IEN signal on the input bus, indicating the last cell. The LM discontinues IST* and raises ISI*, at which time the input control again is in an idle state.

Assume for the following discussion that SAV1*, DAV1*, and ODD* are active. IS* going low forces SELI1* to a low level if IER* is high (inactive). SELI1* is ORed with SELI2* to produce SELI, which releases the input control states register (IC1 and IC2). (In the idle state, SELI is logical 0, holding IC1 and IC2 in a set condition.) DAV1*, DAV2*, ODD1*, ODD2*, SAV1* and SAV2* are applied to the inputs of a D-type holding register that is loaded on the rising transition of SELI. The outputs are connected to a 2-to-1 multiplexer, which is controlled by SELI2*. In this case, SELI2* is high since SELI1* is active (they are mutually exclusive); DAV1*, ODD1* and SAV1* become transformed on the outputs of the multiplexer to data-available-hold (DAVF*), output-data-demand-hold (ODDF*), and status-available-hold (SAVF*), respectively. These signals are used to determine the state changes as shown in figure 4-10.

The input states are decoded by a 2-to-4 decoder. The decoded states are defined as follows: State 0 is IADD

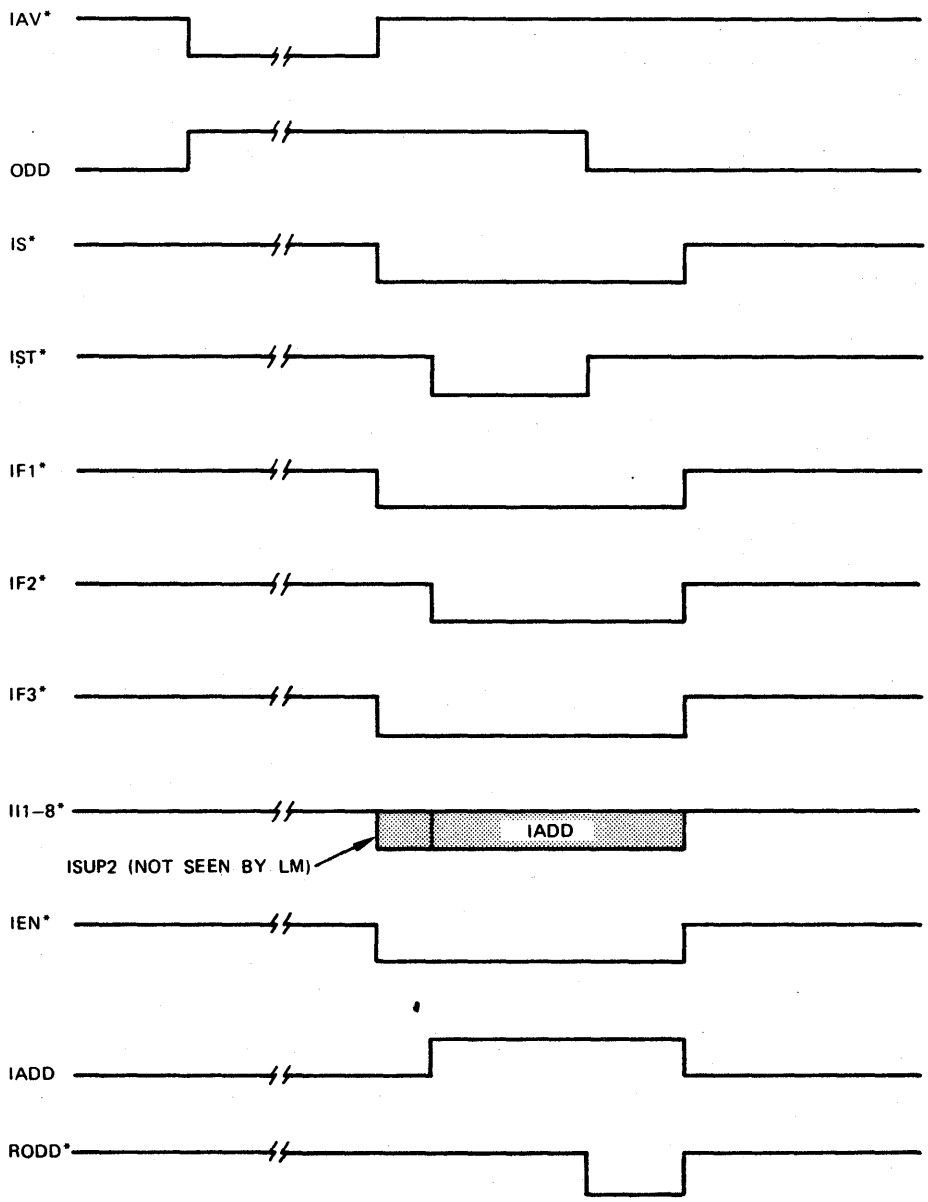


Figure 4-7. Input Control Timing Diagram - ODD Only

(SCLA address with or without ODD bit is placed on the input bus), State 1 is IDATA (data from the synchronous receiver is placed on the bus), State 2 is ISUP1 (the first supervision word is placed on the bus), State 3 is ISUP2 (second supervision word is placed on the bus). The decoder is enabled by a flip-flop that is clocked with the first leading edge of input-strobe (IST) low-to-high transition) after SELI is active.

IC1 and IC2 are $J\overline{K}$ flip-flops. The input control states always switch to input-address (IADD) state on the first IST after selection, since IC1 and IC2 are both set prior to IST, which makes their $\overline{K}$ inputs low. Since DAVF* is active, the J inputs to IC1 and IC2 are logical 1 and 0, respectively, causing the change to the IDATA state. State changes to ISUP1 and ISUP2 on subsequent ISTs are automatic provided ISTs are present and the SCLA is still selected. In the ISUP2 state the IEN signal is produced by the states decoder, telling the LM that the last information cell is on the input bus.

During the IADD state, only ODDF* was active at the time of selection, the inactive DAVF* and SAVF* are NANDed to produce IEN. If only DAVF* were active at the time of selection, the inactive SAVF* is NANDed with IDATA to produce IEN in the IDATA state.

INPUT MULTIPLEXER

The input multiplexer is common to SCLA1 and SCLA2. It provides the three-state interface with the LM input bus for

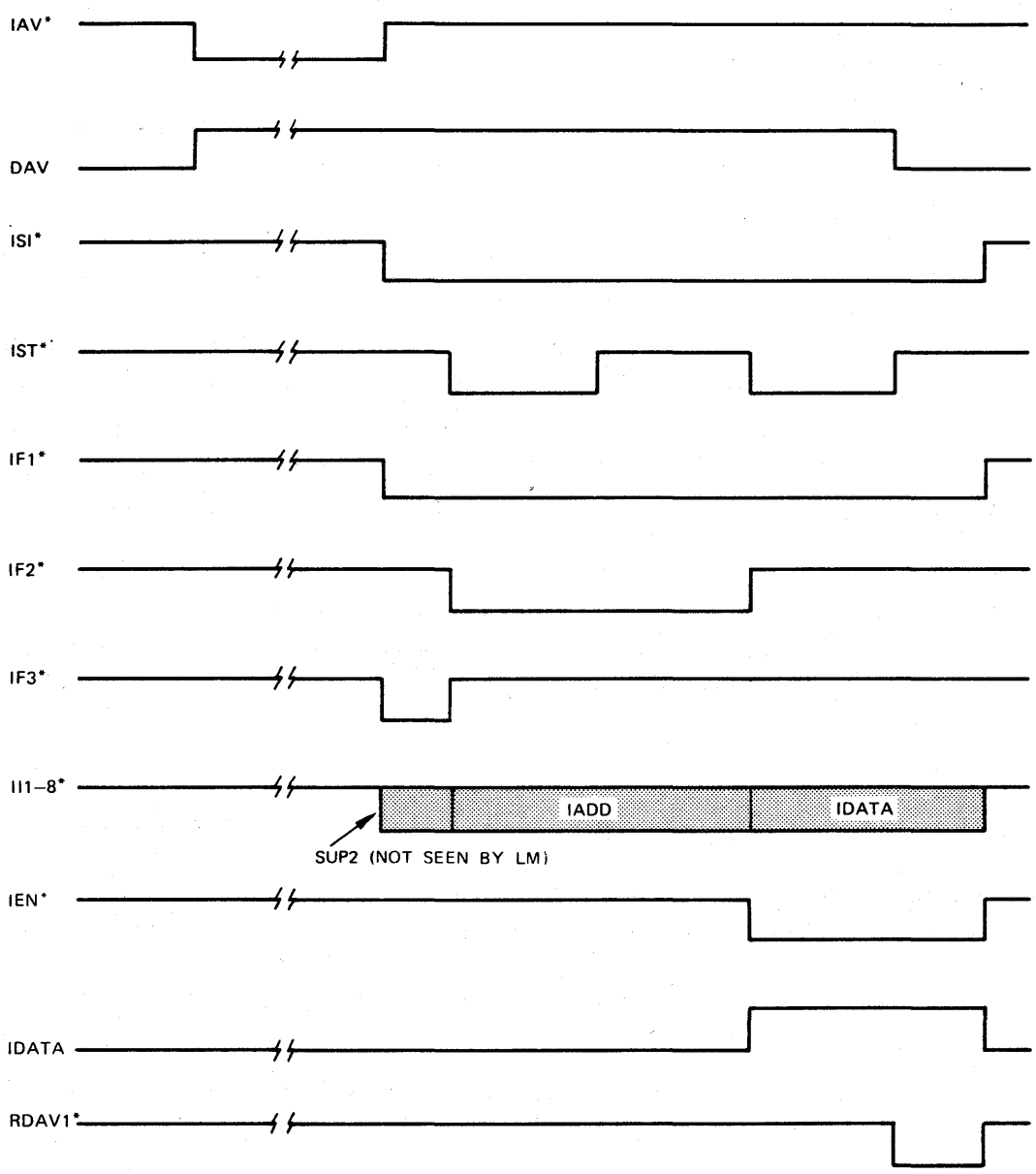


Figure 4-8. Input Control Timing Diagram - Data Only

input-format bit 2 (IF2*), input-format bit 3 (IF3*) and information-input bits (II1* thru II8*). IF1* is activated by an open-collector gate whenever SELI is a logical 1.

The input multiplexer is controlled by SELI*, SELI1*, IC1 and IC2 of the input control logic. Eight 8-to-1 multiplexer ICs are used for II1 thru II8. The respective address, data, and supervision bits from SCLA1 and SCLA2 are applied to the eight inputs of each multiplexer in such a way that the proper bit is selected for transfer to the LM, i.e., if IC1 is 1, IC2 is 0 and SELI1* is active, data bits DAT11 thru DAT81 appear at II1* thru II8*.

When SELI* is low, the three-state outputs to the II1 thru II8 bus are enabled. The 8-to-1 multiplexers for II1 and II2 have three-state outputs. The 8-to-1 multiplexers for II3 thru II8 have two-state outputs that are fed to a three-state buffer which connects the II3 thru II8 bus.

IF2 and IF3 are the outputs of two 4-to-1, three-state multiplexers controlled by SELI*, IC1 and IC2. They place the proper format code on the bus associated with each input control state. All inputs are "hardwired" except for the ODD flag bit which is connected to ODDF*.

INPUT LOOP ERROR

Whenever the MLIA detects an input loop error (ILE) in any loop batch, it notifies the LM via a restart loop end. If the SCLA1 used the last input loop batch, the LM activates the IER* line and selects the SCLA with one IST* and then de-

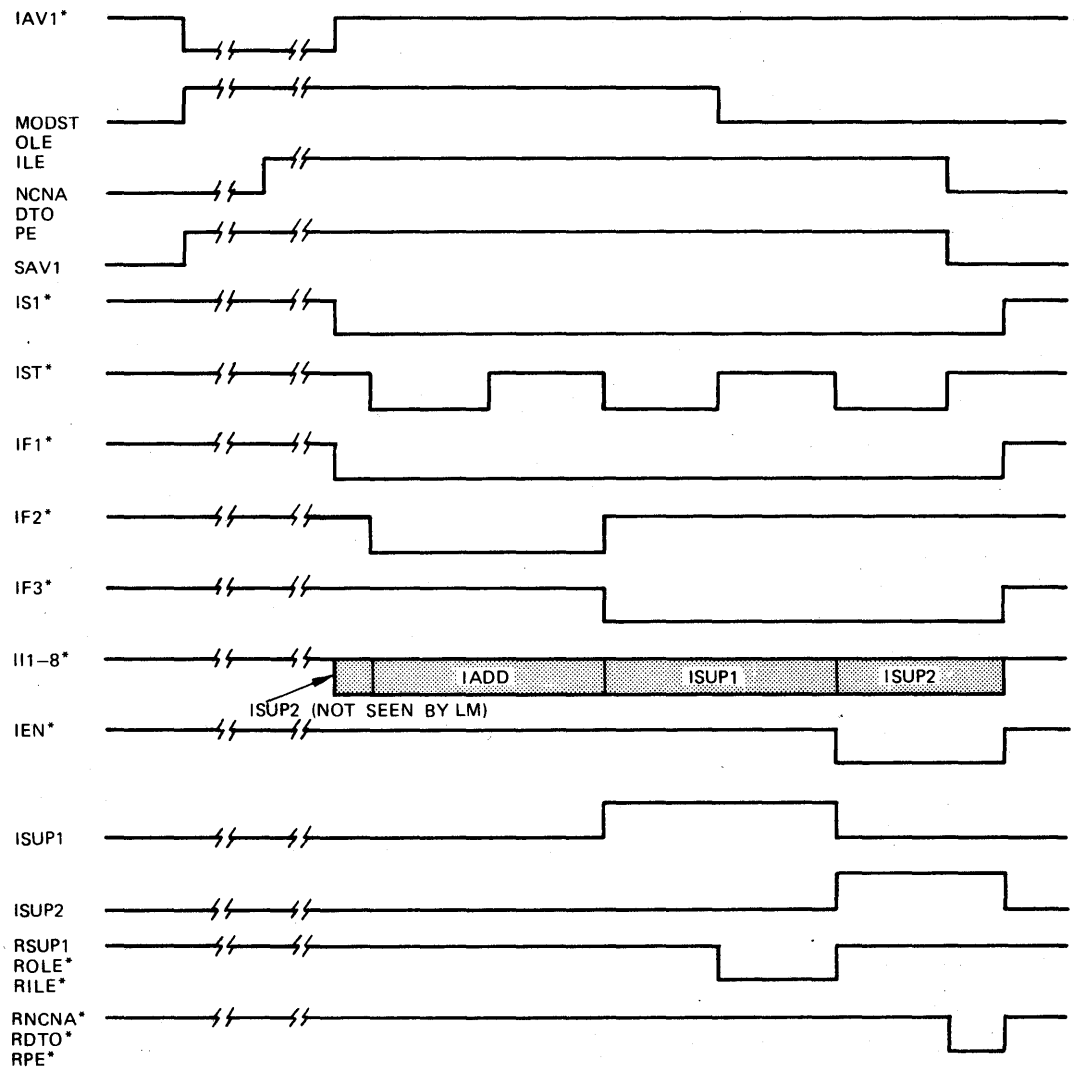


Figure 4-9. Input Control Timing Diagram - Supervision Only

selects it. When both IER* and IS* are active, a low level is applied to the D-input of the ILE flip-flop. On the trailing edge of ISTA*, the ILE is clocked to a true state. ILE1* is gated out, causing IAV1* to go low. ILES is picked up by the LM in ISUP1. Output loop error is reset by RSUP1, which results from the NANDing of ISUP1, SELI, and ISTA*.

ODD, DAV AND STATUSES RESET

All resetting of ODD, DAV and status flags occurs at the time each respective bit of information is accessed by the LM.

If the LM is accessing an ODD address, ODD is reset on the rising edge of ISTA* when ADD, ODDF and SELI are at logical 1.

Reset-data (RDATA*) is enabled by IDATA, SELI1 and ISTA*. RDATA* direct-resets a D-type flip-flop. The Q output (low) of the flip-flop indirectly causes RDAV to go low, resetting DAV, which in turn sets the D-type flip-flop back to its original state.

PE, DTO, OLE, and NCNA are loaded into the status register when IS* is activated. The outputs of this register are fed to the input multiplexer for access by the LM. If OLES is active, the OLEL flip-flop is reset on RSUP1. PE, DTO, or NCNA flip-flops are reset at RSUP2, if their corresponding PES, DTOS, or NCNAS signal is high.

Upon command, the SCLA can be programmed to post or ignore status. If ISON is active, SAV* is allowed to go low, causing IAV* activation when any of status condition becomes true. When ISON is logical 0, SAV* remains high.

RSYN is a nonstored, momentary command from the processor, telling the input section of the SCLA to drop and then re-establish character synchronization. It is applied to the synchronization search logic, which has the same effect as activating ION as described in the Character Assembly paragraph.

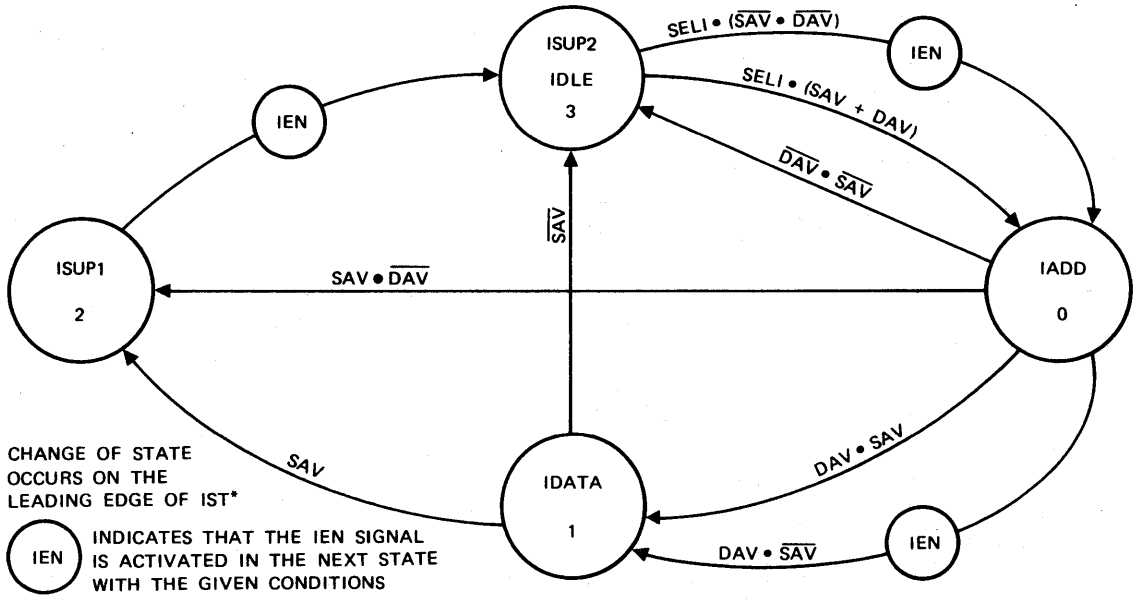


Figure 4-10. Input Control States Diagram

MODEM INTERFACE

The modem interface provides the level converting receivers and drivers to interface the input signals (±12 volts nominal) with the logic used on the SCLA.

DU138-A INTERFACES

The DU138-A SCLA interfaces with a modem conforming to EIA Standard RS232C or CCITT V.24. The RS232C signals are considered in the marking, off, or logical 1 condition when the voltage level is more negative than minus three volts with respect to signal ground. The signals are considered in the spacing, on, or logical 0 condition when the voltage is more positive than plus three volts with respect to signal ground. The SCLA driver outputs (RS-232) are, for the marking condition, less than -8.0 volts, and for the spacing condition, greater than +8.0 volts.

Signal Logic

The modem interface monitors the received signals of data-set-ready (DSR), data-carrier-detect (DCD), quality-monitor (QM) and signal-quality-detector (SQD) for a change in condition. It also monitors RI for a logical 1-to-0 transition. These changes are reported in supervision word 1. The modem interface contains the logic for the internal loopback test mode so that the following input and output signals are connected: SD to RD; RTS to CTS; DTR to DSR, RI, and SQD; and NSYN to QM and DCD. In the internal loopback test mode, serial-clock-transmit (SCT) and serial-clock-receive (SCR) are supplied by an internally generated 2.4-kHz clock.

All received modem signals are inverted by their associated receivers. The resulting signals are applied to the 2-to-1 multiplexers used for the internal loopback test mode. At this point, DSR*, DCD*, QM*, SQD* are presented to a change-detecting circuit. If there had been a change in any of the signals, their present condition would be stored in the modem status register. At the same time the modem status (MODST) flip-flop is set to logical 1, which causes IA* to activate when ISON is a 1; this indicates to the LM that the SCLA has a status change to report.

The change-detecting circuit consists of a D-type flip-flop of the modem status register, an inverter and an exclusive OR gate. If, for example, DCD* is low and data-carrier-detect-status (DCDS) is high, there is no change detected since both are logical 1. DCD* then makes a 1-to-0 transition. The exclusive ORing of these two signals produces a low level which is inverted, ORed, and applied to a NAND element, the output of which sets MODST flip-flop if it is not already set. The setting of MODST produces a clock pulse to the register, thus updating it to the change in DCD, along with the present status of the other modem signals connected to the inputs of the register.

This change-detecting circuit is now primed to respond in the same manner when DCD* makes a logical 0-to-1 transition. Changes in SQD, DSR, and QM are reported in an identical way. A timing diagram of the modem interface signals is shown in figure 4-11.

The ring-indicator-status bit (RIS) is also stored in the modem status register, but only a logical 1-to-0 transition of RI sets MODST and causes RIS to go to a logical 1. The next time that MODST is set, if not caused by RI, RIS changes to a logical 0. The RI detection circuit consists of an exclusive OR gate, a NAND gate, an inverter, one element of the register, and a resistor-capacitor network. When the RI* line changes to a low level, the capacitor discharges through the resistor until the voltage across the capacitor reaches ground potential. The input to the register is then armed with a high level. When RI* makes a low-to-high transition, the MODST flip-flop sets, since both inputs to the NAND gate are high. The high level at the input to RIS is clocked into the register. This level goes down 200 to 400 nanoseconds afterwards, when the capacitor charges to the turn-on potential of the exclusive OR gate.

The MODST flip-flop is reset at the time the first status word is picked up by the LM with RSUP1. When it is logical

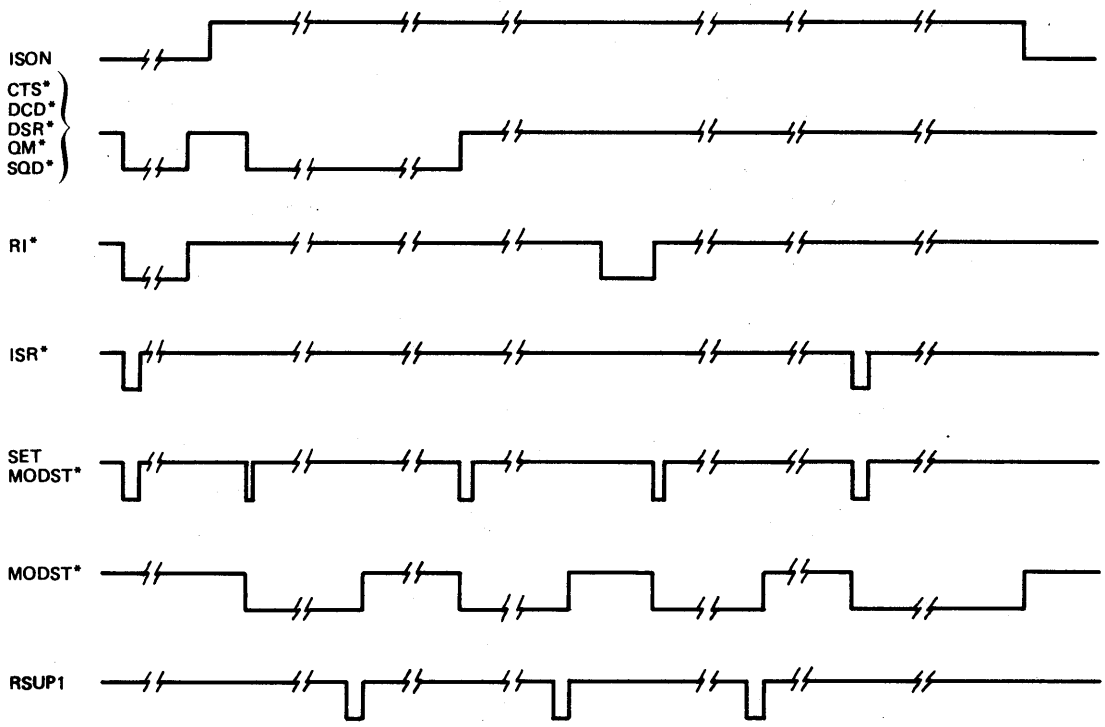


Figure 4-11. Modem Interface Timing Diagram

0 and is applied to the reset of the MODST flip-flop, ISON inhibits the setting of MODST.

Modem Clock Strapping

In normal operation, the DU138-A SCLA receives two clock signals from the modem: serial-clock-receive (SCR) and serial-clock-transmit (SCT). In order to allow two SCLAs to communicate without a modem, or an SCLA to communicate directly to a synchronous terminal without a modem, there is a strapping option that provides for transmission of external-transmit-clock (EXTC). This strapping is provided in the modem connector. Three different clock rates are available, depending on the strapping configurations used. The strapping configurations and their associated clock rates are given in table 4-1.

TABLE 4-1. STRAPPING CLOCK RATES

Strap	Rate
F1 to TCLK	9.6 kHz
F2 to TCLK	4.8 kHz
F4 to TCLK	2.4 kHz

DU139-A INTERFACES

The DU139-A SCLA interfaces a modem that is compatible with AT&T 301/303 Data Sets. Signals from these modems are considered in the marking, off, or logical 1 condition when the current into a 100-ohm load is less than 5 milliamperes. These signals are considered in the spacing, on, or logical 0 condition when the current into a 100-ohm load is greater than 23 milliamperes.

Two signals, ring-indicator (RI) and data-terminal-ready (DTR), conform to the EIA RS-232-C standard. These signals are considered in the marking, off, or logical 1 condition when the voltage level is more negative than minus three volts with respect to signal ground. The signal is considered in the spacing, on, or logical 0 condition when the voltage is more positive than plus three volts with respect to signal ground. The SCLA driver outputs (RS-232) are, for the marking condition, less than -8.0 volts, and for the spacing condition, greater than +8.0 volts.

The modem interface monitors the received signals of DSR and DCD (the AGC Lock on 303 Data Set) for a change of condition. It also monitors RI for a logical 1-to-0 transition. These changes are reported in input supervision word 1. The modem interface contains the logic for the internal loopback test mode so that the following output and input signals are connected: SD to RD, RTS to CTS, DTR to DSR, and LT to DCD and RI. In the internal loopback test mode, serial-clock-transmit and serial-clock-receive are supplied by an internally generated 2.4-kHz clock.

All received modem control signals (CTS, DSR, DCD, and RI) are inverted by their associated receivers. The resulting signals are applied to two 2-to-1 multiplexers used for the self-test mode. Two outputs of a multiplexer (DSR* and DCD*) are presented to a change-detecting circuit. If there had been a change in either of the signals, their present

condition would be stored in the modem status register. At the same time, MODST flip-flop is set to logical 1, which causes IA to activate if ISON is logical 1. This indicates to the LM that the SCLA has a status change to report.

The change-detecting circuit consists of D-type flip-flop of the modem status register, an inverter, and an exclusive OR gate. If, for example, DCD* is low and DCDS is high, there is no change detected since both are logical 1. DCD* then makes a 1-to-0 transition. The exclusive ORing of these two signals produces a low level which is inverted, ORed, and applied to a NAND element, the output of which sets MODST flip-flop if it is not already set.

The setting of MODST produces a clock pulse to the register, thus updating it to the change in DCD, along with the present status of the other modem signals connected to the inputs of the register. This change-detection circuit is now primed to respond in the same manner when DCD* makes a logical 0-to-1 transition. Changes in DSR are reported in an identical way. A timing diagram of the modem interface signals has been presented in figure 4-11.

The ring-indicator-status (RIS) bit is also stored in the modem status register, but only a logical 1-to-0 transition of RI sets the MODST flip-flop, and causes RIS to go to a logical 1. The next time that MODST is set, if not caused by RI, RIS changes to a logical 0. The RI detection circuit consists of two buffers, a NAND gate, an inverter, one element of the modem status register, and a resistor-capacitor delay network. When the RI* line changes to a low level, the capacitor discharges through the resistor until the voltage across the capacitor reaches ground potential. The input to the modem status register is then armed with a high level. When RIA* makes a low-to-high transition, the MODST flip-flop sets, since both inputs to the NAND gate are high. The high level at the modem status register is clocked into the register by MODST, causing RIS to go to a logical 1. The input to the modem status register goes down 200 to 400 nanoseconds afterwards, when the capacitor charges to the turn-on potential of the buffer. The next time that the modem status register is clocked by MODST, RIS goes to logical 0, if RI did not cause the setting of MODST.

The MODST flip-flop is reset at the time the first status word is picked up by the LM with RSUP1. When it is logical 0 and is applied to the reset of the MODST flip-flop, ISON inhibits the setting of MODST.

DU140-A INTERFACES

The DU140-A SCLA interfaces a modem in which two types of interface signals are used. The high data rate signals, including clocks and data, meet the CCITT V.35 balanced interface standard. The control signals have the electrical characteristics of the EIA RS232C standard.

The CCITT V.35 signals are considered in the marking or logical 1 condition when the terminal-to-terminal voltage is 0.55 ±20 percent so that A terminal is positive with respect to the B terminal. The signals are considered in the spacing or logical 0 condition when the terminal-to-terminal voltage is reversed. These signals are terminated by a 100-ohm resistive load.

The RS-232-C signals are considered in the marking, off, or logical 1 condition when the voltage level is more negative than -3 volts with respect to signal ground. The signals are considered spacing, on, or logical 0 condition when the voltage is more positive than +3 volts with respect to signal ground. The SCLA driver (RS-232-C) outputs are, for the marking condition, less than -8.0 volts, and for the spacing condition, greater than +8 volts.

The modem interface monitors the received signals of DSR and DCD for a change of condition. It also monitors RI for a logical 1-to-0 transition. These changes are reported in input supervision word 1. The modem interface contains the logic for the internal loopback test mode so that the following output and input signals are connected: SD to RD, RTS to CTS, DTR to DSR and LT to DCD and RI. In the internal loopback test mode, serial-clock-transmit and serial-clock-receive are supplied by an internally generated 2.4-kHz clock.

All received modem control signals (CTS, DSR, DCD and RI) are inverted by their associated receivers. The resulting signals are presented to a change-detecting circuit. If there had been a change in either of the signals, their present condition would be stored in the modem status register. At the same time, MODST flip-flop is set to logical 1 which causes IA to activate if ISON is logical 1. This indicates to the LM that the SCLA has a status change to report.

The change-detecting circuit consists of D-type flip-flop of the modem status register, an inverter, and an exclusive OR gate. If, for example, DCD* is low and DCDS is high, there is no change detected since both are logical 1. DCDA* then makes a 1-to-0 transition. The exclusive ORing of these two signals produces a low level which is inverted, ORed, and applied to a NAND element, the output of which sets MODST flip-flop if it is not already set.

The setting of MODST produces a clock pulse to the register, thus updating it to the change in DCD, along with the present status of the other modem signals connected to the inputs of the register. This change-detection circuit is now primed to respond in the same manner when DCD* makes a logical 0-to-1 transition. Changes in DSR are reported in an identical way. The timing of the modem interface signals has been shown in figure 4-11.

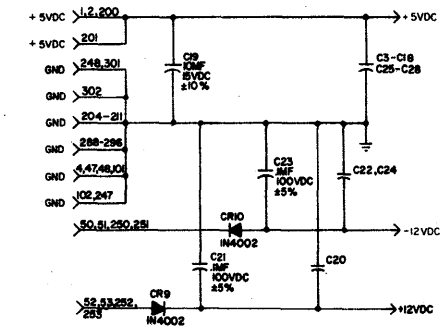
The ring-indicator-status (RIS) bit is also stored in the modem status register, but only a logical 1-to-0 transition of RI sets the MODST flip-flop, and causes RIS to go to a logical 1. The next time that MODST is set, if not caused by RI, RIS changes to a logical 0. The RI detection circuit consists of two buffers, a NAND gate, an inverter, one element of the modem status register, and a resistor-capacitor delay network. When the RI* line changes to a low level, the capacitor discharges through the resistor until the voltage across the capacitor reaches ground potential. The input to the modem status register is then armed with a high level. When RI* makes a low-to-high transition, the MODST flip-flop sets, since both inputs to the NAND gate are high. The high level at the modem status register is clocked into the register by MODST, causing RIS to go to a logical 1. The input to the modem status register goes down 200 to 400 nanoseconds afterwards, when the capacitor charges to the turn-on potential of the buffer. The next time that the modem status register is clocked by MODST, RIS goes to logical 0 if RI did not cause the setting of MODST.

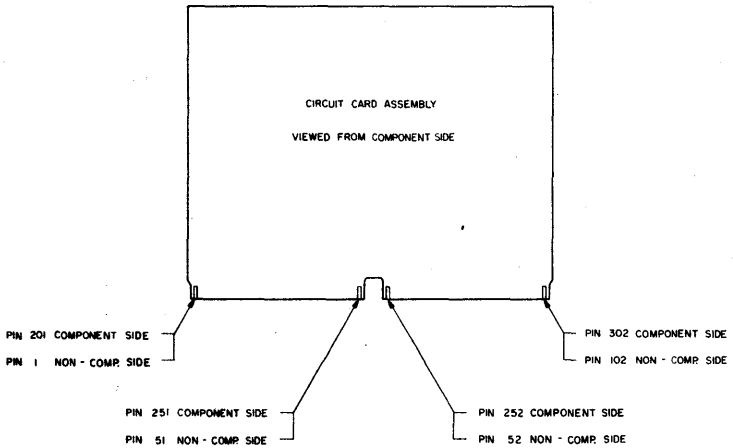
The MODST flip-flop is reset at the time the first status word is picked up by the LM with RSUP1. When it is logical 0 and is applied to the reset of the MODST flip-flop, ISON inhibits the setting of MODST.

DIAGRAMS

This section contains the diagrams for the communications line adapter logic circuitry. A key to the logic symbols used in these diagrams is provided on sheet two of the diagrams.

SHEET REVISION STATUS										REV	ECO	REVISION RECORD DESCRIPTION	DFT	DATE	CHK	APPD
10	9	8	7	6	5	4	3	2	1							
01	01	01	01	01	01	01	01	01	01	01	05394	ENG RELEASE	JTP	3-13-75		
01	01	01	01	02	01	01	01	01	02	02	05573	SEE E.C.O.	JTP	3-20-75	[illegible]	
03	03	03	03	03	03	03	03	03	03	03	05458	SEE E.C.O.	JTP	4-24-75		
04	04	04	04	04	04	04	04	04	04	04	06120	INITIAL RELEASE	PL	3-22-77	JN	M
A	A	A	A	A	A	A	A	A	A	A	08063	UP DATE FOR CBM	CT	11-29-77		M





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES 5% RI-R6
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: 01 MF 35 VDC +80-20%.(C3-C18,C24-C28,C20,C22)
   ALL DIODES: DIALCO 547-2003, 5V, 6MA (CR1-CR8)

2. COMPONENT ASSEMBLY NO. 74873381

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL-IN-LINE	14	7
16 PIN DUAL-IN-LINE	16	8

NON-STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all listing Divisions per CDC-STD 1.01.01. CA
AAL030

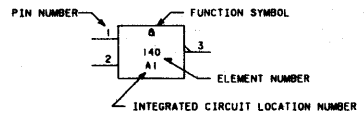
5BBY

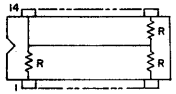
UNLESS OTHERWISE SPECIFIED DIMS ARE IN INCHES/MILLIMETERS TOLERANCES: 3 PLACE ± .010 / ±0.25; 2 PLACE ± .03 / ±0.8; ANGLES ±°	CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE: LOGIC DIAGRAM — SYNCHRONOUS CLAI — MODEM INTERFACE
DO NOT SCALE DRAWING	FIRST USED ON: DU13B-A		
MATERIAL	DR: [illegible] 3-17-75		D 34015 74873383
FINISH	ENG		SCALE NONE 45190-412 104 SHEET 1 OF 10
DETACHED LISTS	ENGR		
	MFG		
	APPD		

6650

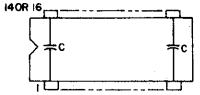
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
		SEE SHEET 1				

CIRCUIT ELEMENT SYMBOLOGY



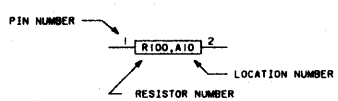


I.C. RESISTOR PACK
LOCATION U5,U20
10K

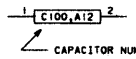


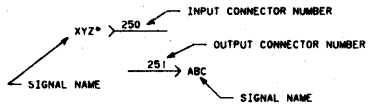
I.C. CAPACITOR PACK
LOCATION U27,U117(14PIN)
220PF U39,U43(16PIN)

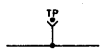
RESISTOR INTEGRATED SYMBOLOGY

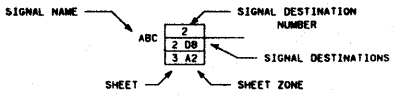


CAPACITOR INTEGRATED SYMBOLOGY









COMMON CONTROL BLOCK.
SIGNALS ENTERING THIS BLOCK
ARE COMMON TO MORE THAN ONE
SECTION OF THE CIRCUIT

IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
140	7400	TTL QUAD 2-INPUT NAND GATE
140L	74L00	TTL QUAD 2-INPUT NAND GATE
141	7410	TTL TRIPLE 3-INPUT NAND GATE
141L	74L10	TTL TRIPLE 3-INPUT NAND GATE
146	7404	TTL HEX INVERTER
146L	74L04	TTL HEX INVERTER
148	7402	TTL QUAD 2-INPUT NOR GATE
148L	74L02	TTL QUAD 2-INPUT NOR GATE
175	7474	TTL DUAL D-TYPE F/F
175L	74L74	TTL DUAL D-TYPE F/F
189	74187	MULTIPLEXER,TTL QUAD 2-INPUT GATE
201	7408	TTL QUAD 2-INPUT AND GATE
202	7403	TTL QUAD 2-INPUT NAND GATE
206L	74L30	TTL 8-INPUT NAND GATE
208	7420	TTL DUAL 4-INPUT NAND GATE
208L	74L20	TTL DUAL 4-INPUT NAND GATE
223L	74L51	TTL DUAL 2-WIDE 2-3 IN AND-OR-INVERTER
240	9024	TTL DUAL J-K F/F
505	74151	MULTIPLEXER,TTL 8-INPUT GATE
519	74174	LATCH,TTL 6-BIT D-TYPE
520	74175	LATCH,TTL 4-BIT D-TYPE
524L	74L85	COMPARATOR, TTL 4-BIT MAGNITUDE
538	9321	DECODER, TTL DUAL (1 OF 4)
542	8214	MULTIPLEXER TTL DUAL 4-BIT TRISTATE
551	7475	LATCH, TTL 4-BIT
900	MC1488	DRIVER, DTL TO RS-232C QUAD LINE
901	MC1489A	RECEIVER, RS-232C TO DTL QUAD LINE
—	74L86	TTL QUAD 2 INPUT EXCLUSIVE OR GATE
—	74251	MULTIPLEXER, TTL 8-INPUT TRISTATE
—	8096	DRIVER HEX INVERTER TRISTATE
—	9L24	TTL DUAL J-K F/F
—	93L00	REGISTER,TTL 4-BIT UNIVERSAL
—	4050	HEX BUFFER / NON INVERTING
—	P14728	P/SAR, MOS/LSI
—	PT14828	P/SAT, MOS/LSI

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
1⊓	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
OO	EVEN PARITY
OOO	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A 'D' INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⌐	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

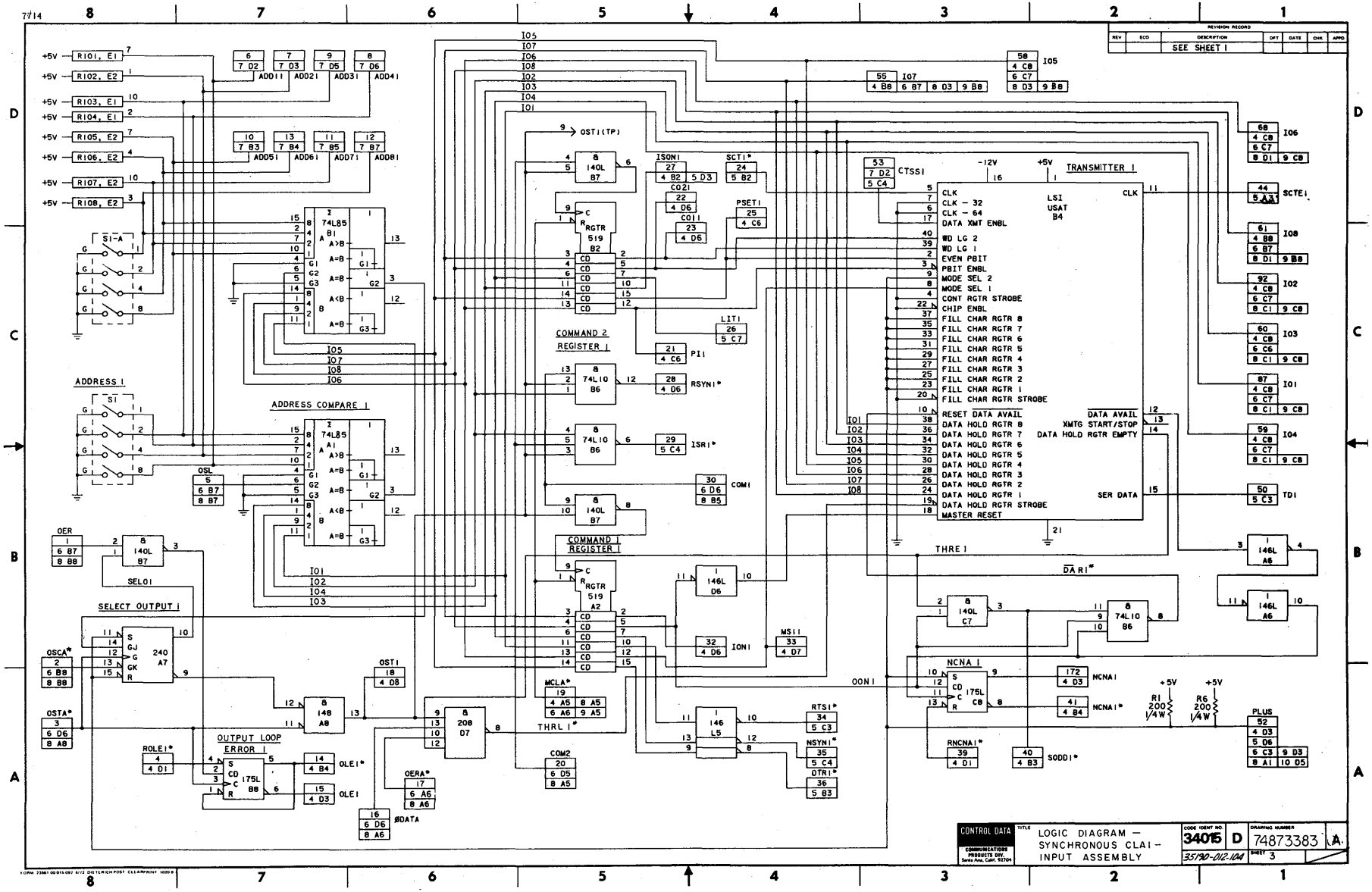
SIGNAL LINE INDICATORS

◇& OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
◺	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM '0' STATE TO '1' STATE
—/—	NON-STANDARD LOGIC LEVEL
—x—	ANALOG OR NON-LOGIC LEVEL
—↗—	VARIABLE PARAMETER CONTROL
—○—	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
—○	INHIBIT DESIGNATOR

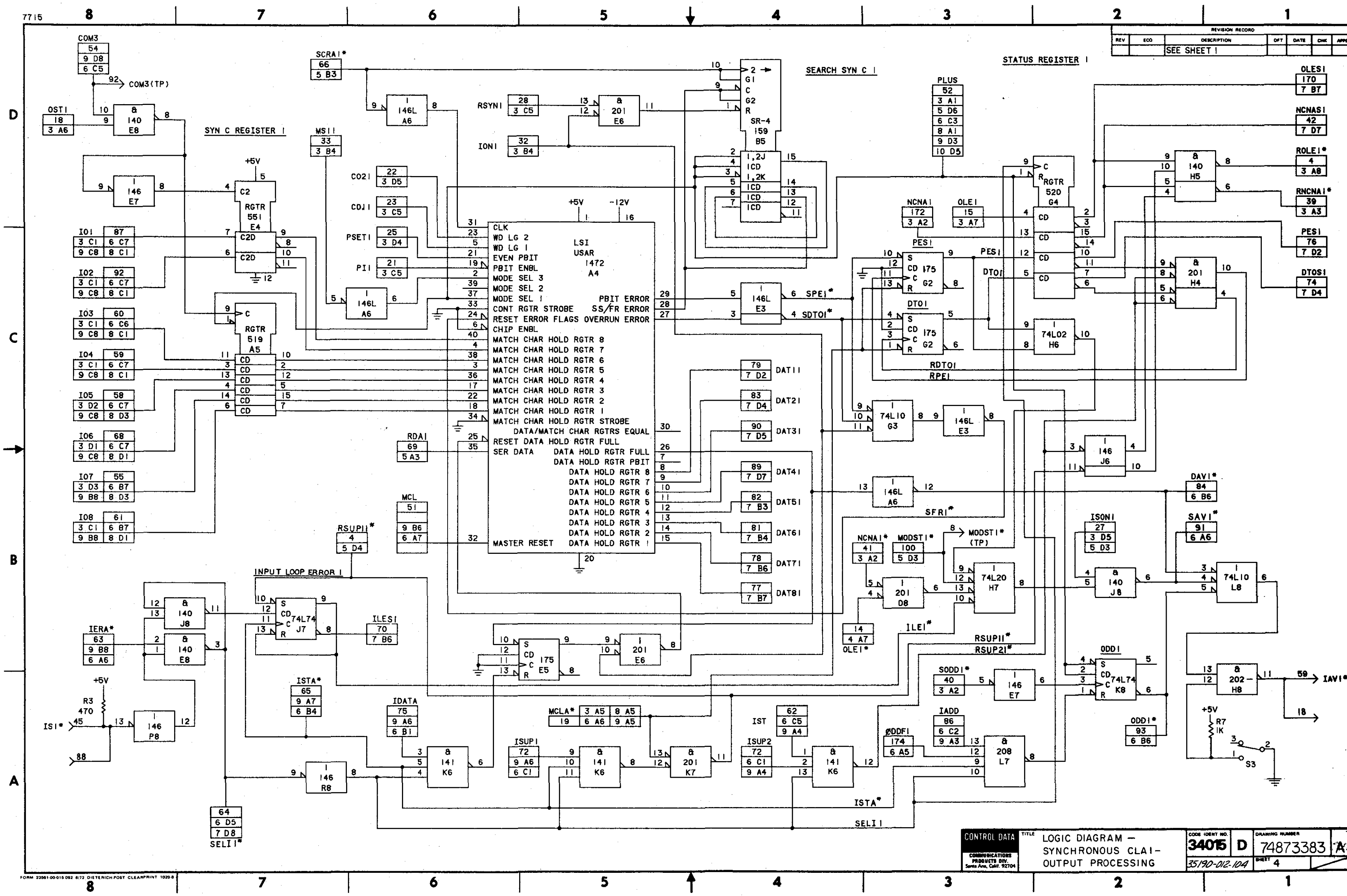
FUNCTION ABBREVIATIONS

ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. IOCNTR OR I6CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

CONTROL DATA	TITLE	CODE IDENT NO	DRAWING NUMBER
COMMUNICATIONS PRODUCTS DIV Santa Ana, Calif. 92704	LOGIC DIAGRAM— KEY TO SYMBOLS	34015 D	74873383 A
		35190-012-104	SHEET 2


REVISION RECORD
SEE SHEET 1
TRANSMITTER 1
LSI USAT B4
ADDRESS 1
ADDRESS COMPARE 1
COMMAND 2 REGISTER 1
COMMAND 1 REGISTER 1
SELECT OUTPUT 1
OUTPUT LOOP ERROR 1
NCNA 1
CONTROL DATA COMMUNICATION PRODUCTS DIV. Santa Ana, Calif. 92704
LOGIC DIAGRAM — SYNCHRONOUS CLAI-INPUT ASSEMBLY
34015
D
74873383
35730-012-104
SHEET 3

74700700 D



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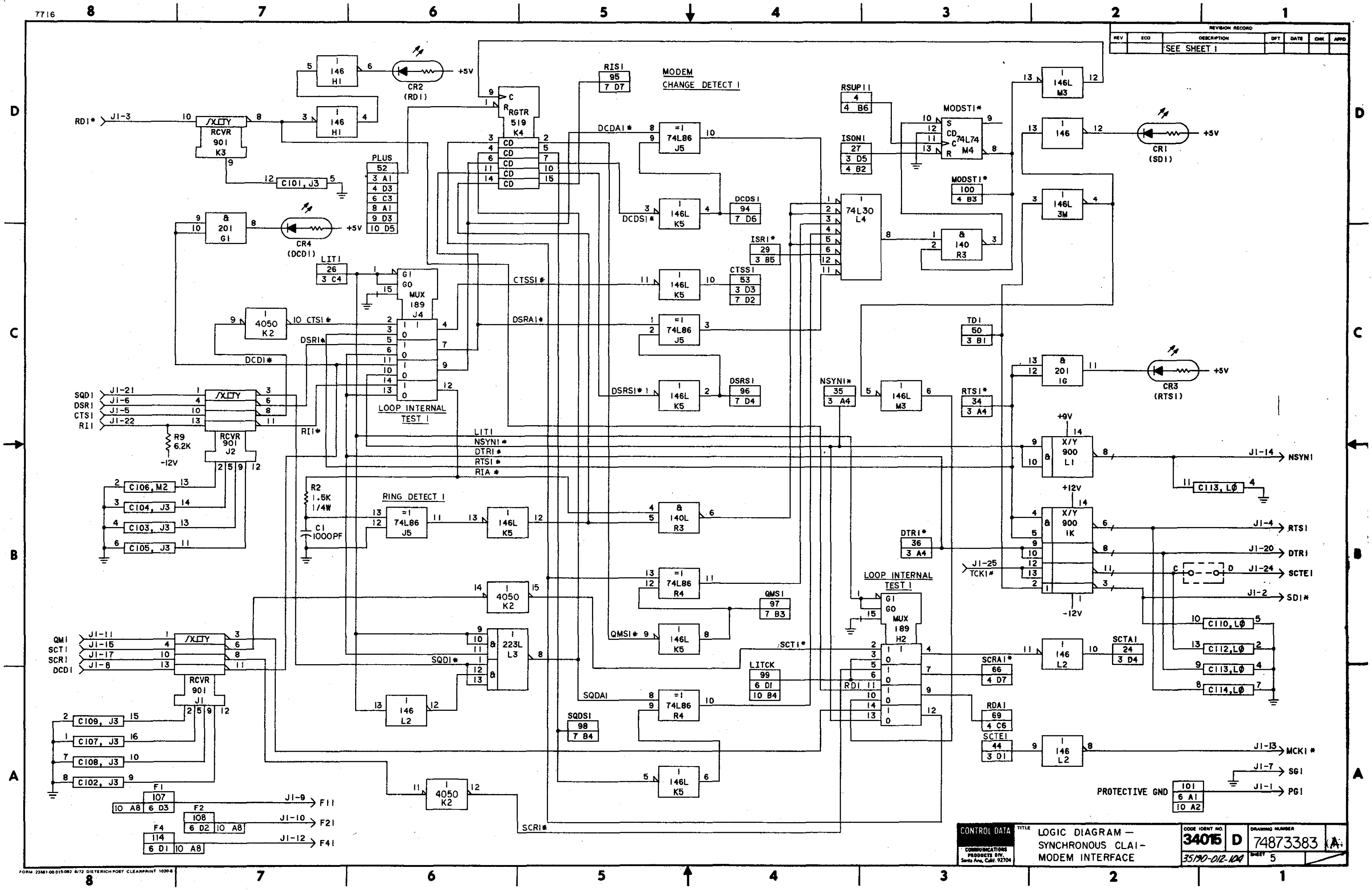
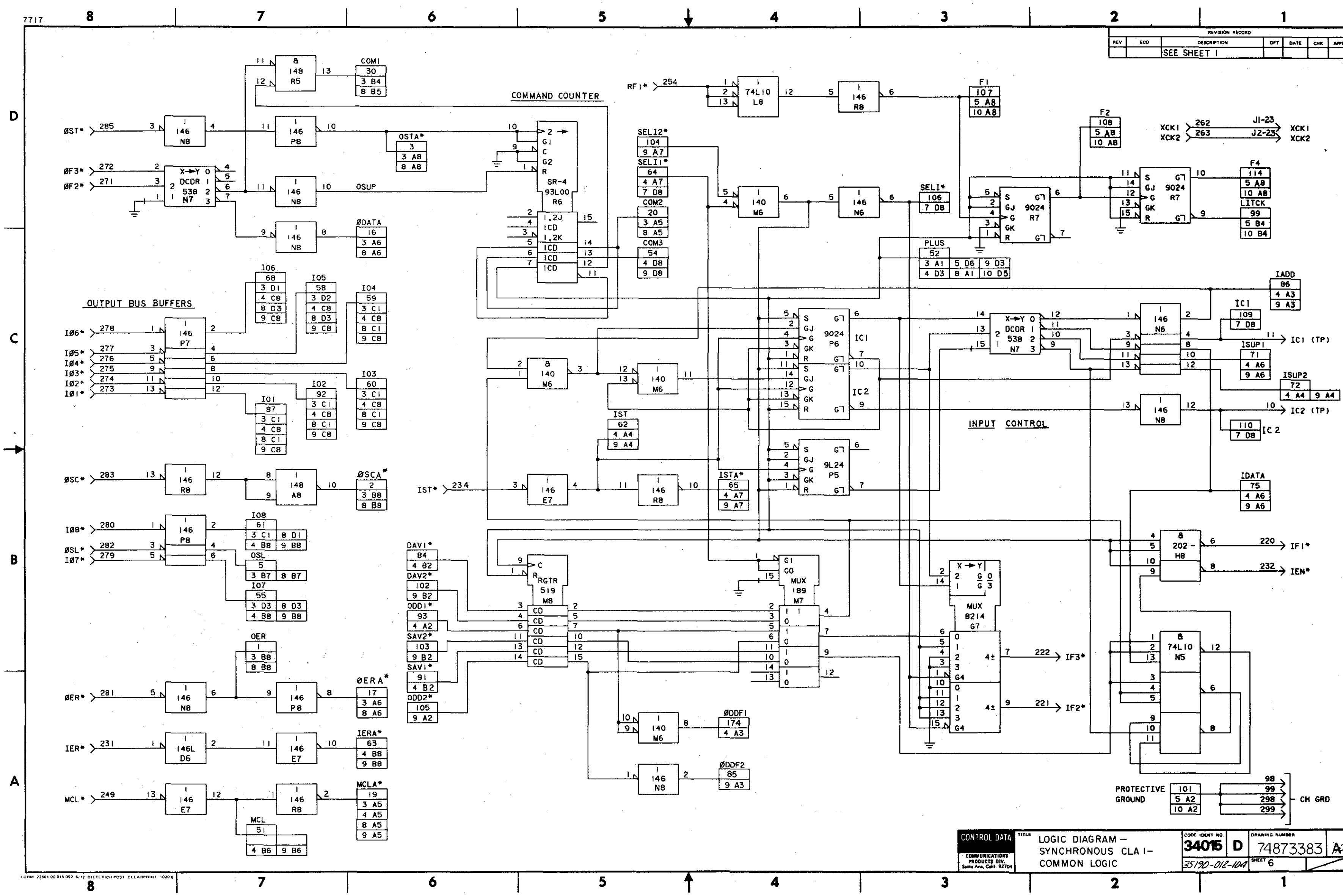
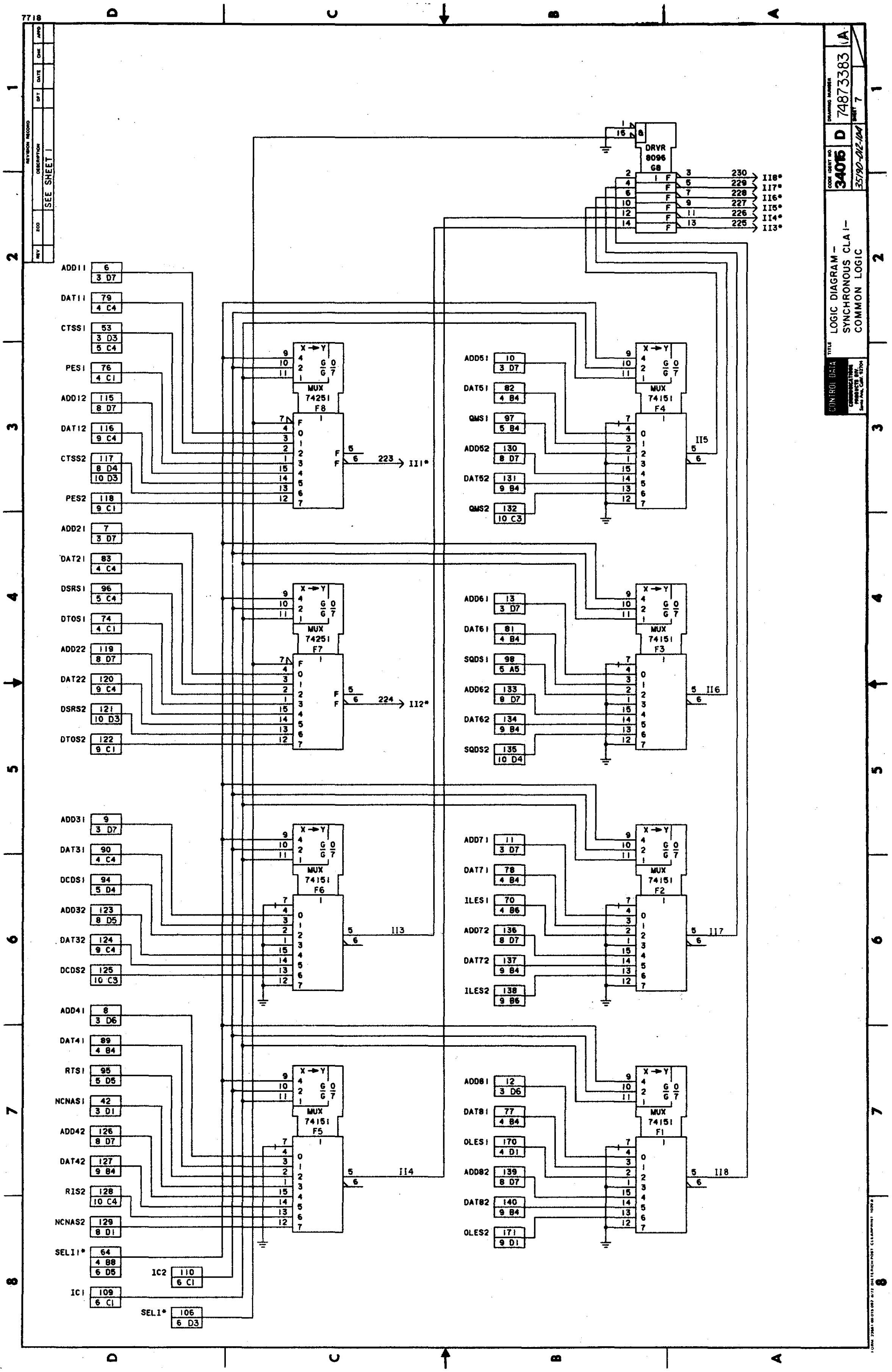

MODEM CHANGE DETECT 1
LOOP INTERNAL TEST 1
RING DETECT 1
PROTECTIVE GND
CONTROL DATA
COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704
LOGIC DIAGRAM — SYNCHRONOUS CLA1-MODEM INTERFACE
34015 D 74873383 A
35190-012-104
SHEET 5
SEE SHEET 1


COMMAND COUNTER
OUTPUT BUS BUFFERS
INPUT CONTROL
SEE SHEET 1
PROTECTIVE GROUND
CH GRD
CONTROL DATA
COMMUNICATIONS PRODUCTS DIV.
LOGIC DIAGRAM – SYNCHRONOUS CLA I– COMMON LOGIC
34015 D 74873383 A
SHEET 6


LOGIC DIAGRAM – SYNCHRONOUS CLA1– COMMON LOGIC
CONTROL DATA
34016
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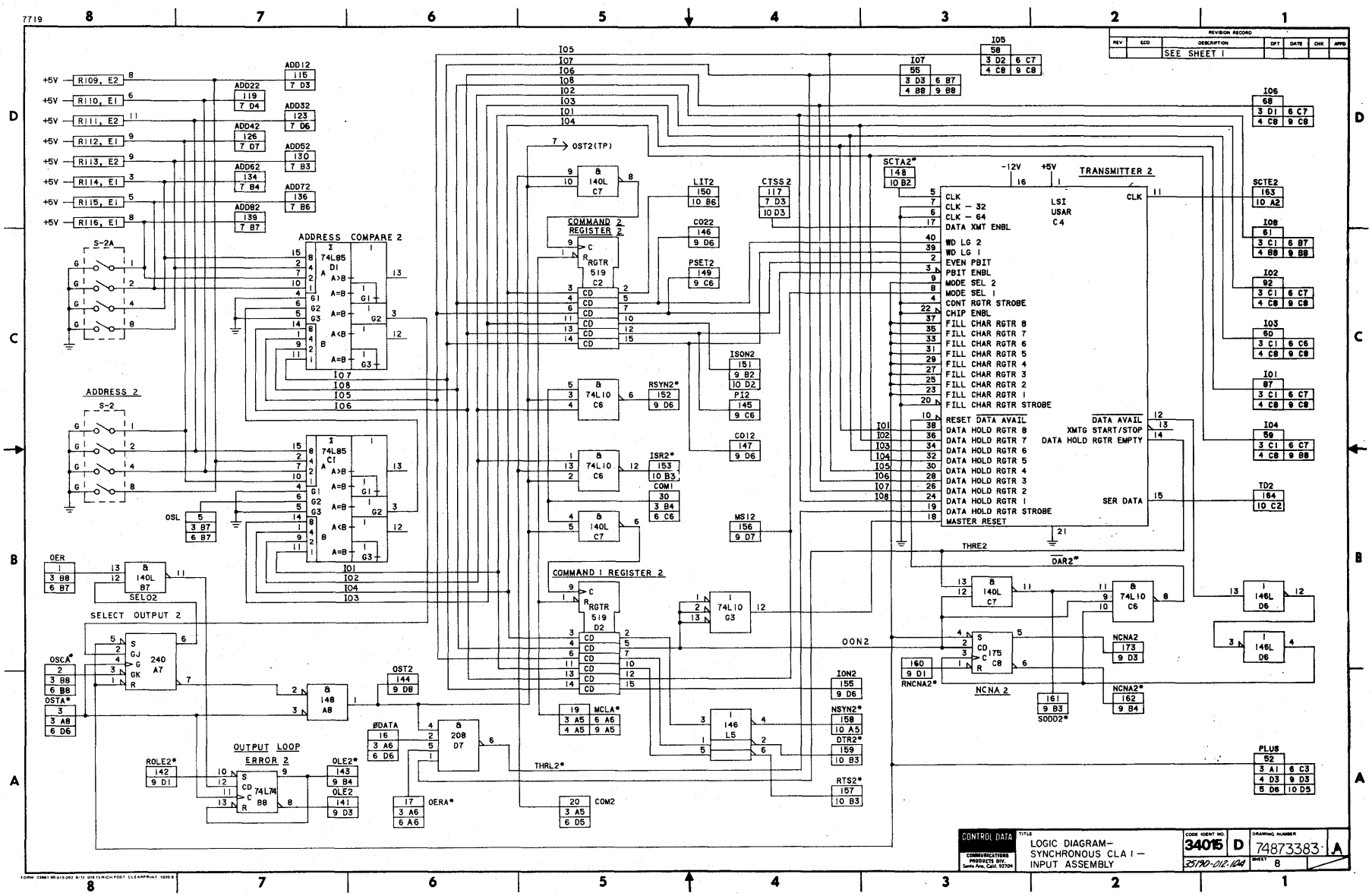
74873383
A
SEE SHEET 1
7718
DRVR 8096 G8
MUX 74251 F8
MUX 74251 F7
MUX 74151 F6
MUX 74151 F5
MUX 74151 F4
MUX 74151 F3
MUX 74151 F2
MUX 74151 F1
ADD11 DAT11 CTSS1 PES1 ADD12 DAT12 CTSS2 PES2
ADD21 DAT21 DSRS1 DTOS1 ADD22 DAT22 DSRS2 DTOS2
ADD31 DAT31 DCDS1 ADD32 DAT32 DCDS2
ADD41 DAT41 RTS1 NCNAS1 ADD42 DAT42 RTS2 NCNAS2
SEL11* IC2 IC1 SEL1*
ADD51 DAT51 QMS1 ADD52 DAT52 QMS2
ADD61 DAT61 SQDS1 ADD62 DAT62 SQDS2
ADD71 DAT71 ILES1 ADD72 DAT72 ILES2
ADD81 DAT81 OLES1 ADD82 DAT82 OLES2
223 I11*
224 I12*
I13 I14 I15 I16 I17 I18
230 I18*
229 I17*
228 I16*
227 I15*
226 I14*
225 I13*


TRANSMITTER 2
LSI USAR C4
ADDRESS COMPARE 2
ADDRESS 2
COMMAND 2 REGISTER 2
COMMAND 1 REGISTER 2
SELECT OUTPUT 2
OUTPUT LOOP ERROR 2
NCNA 2
CLK
CLK – 32
CLK – 64
DATA XMT ENBL
WD LG 2
WD LG 1
EVEN PBIT
PBIT ENBL
MODE SEL 2
MODE SEL 1
CONT RGTR STROBE
CHIP ENBL
FILL CHAR RGTR 8
FILL CHAR RGTR 7
FILL CHAR RGTR 6
FILL CHAR RGTR 5
FILL CHAR RGTR 4
FILL CHAR RGTR 3
FILL CHAR RGTR 2
FILL CHAR RGTR 1
FILL CHAR RGTR STROBE
RESET DATA AVAIL
DATA HOLD RGTR 8
DATA HOLD RGTR 7
DATA HOLD RGTR 6
DATA HOLD RGTR 5
DATA HOLD RGTR 4
DATA HOLD RGTR 3
DATA HOLD RGTR 2
DATA HOLD RGTR 1
DATA HOLD RGTR STROBE
MASTER RESET
DATA AVAIL
XMTG START/STOP
DATA HOLD RGTR EMPTY
SER DATA
THRE2
DAR2*
OON2
THRL2*
CONTROL DATA
COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704
LOGIC DIAGRAM– SYNCHRONOUS CLA I– INPUT ASSEMBLY
34015
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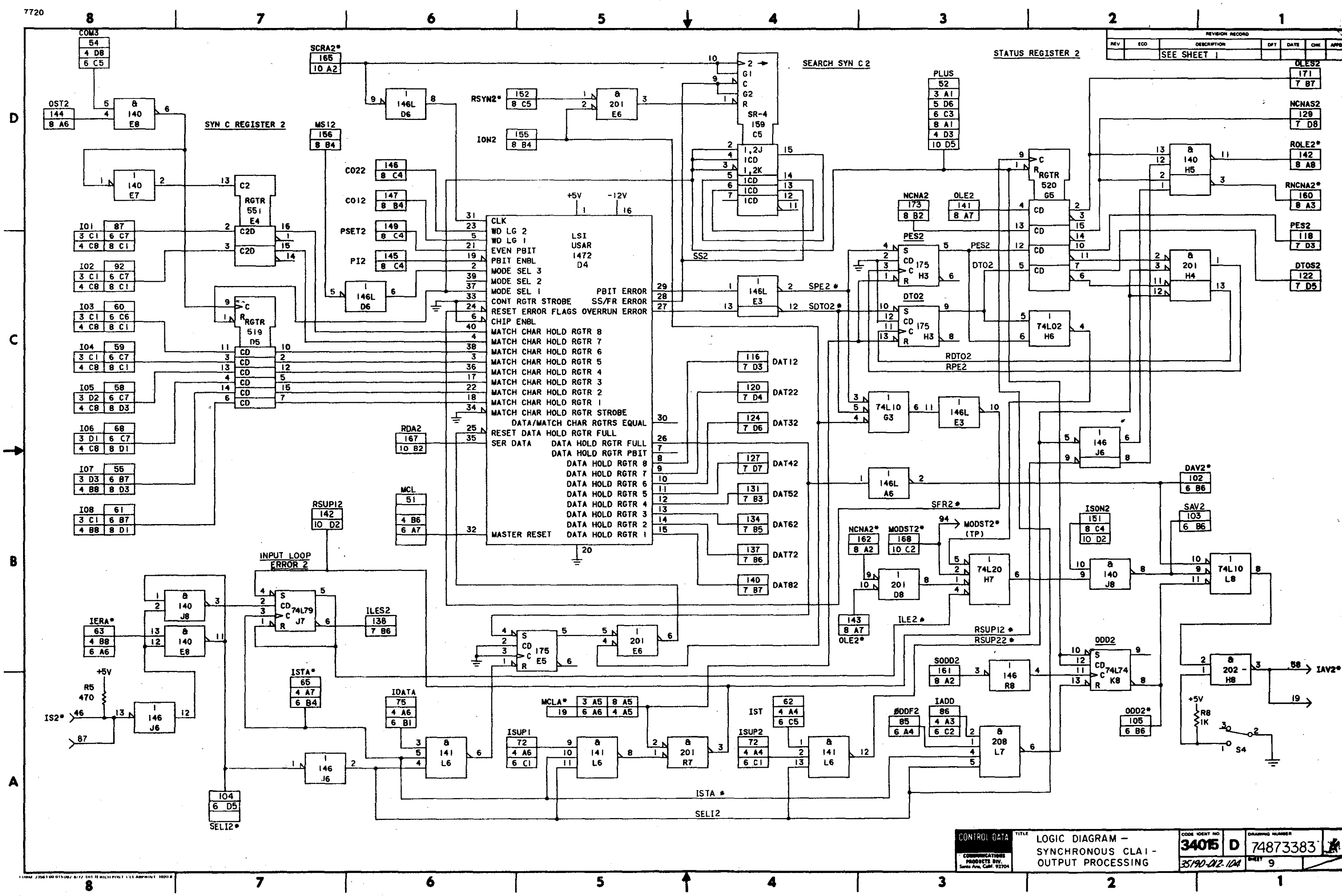
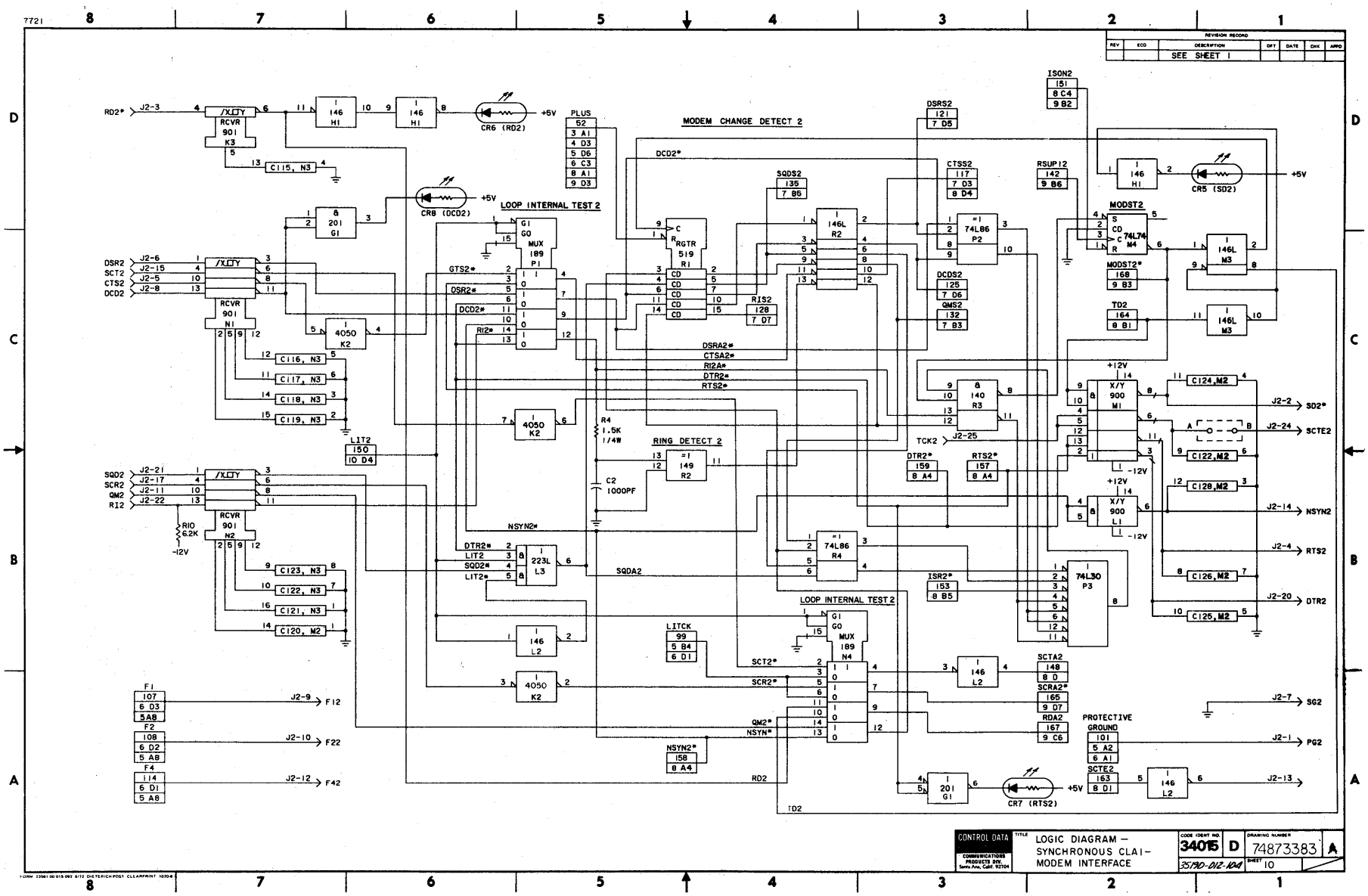
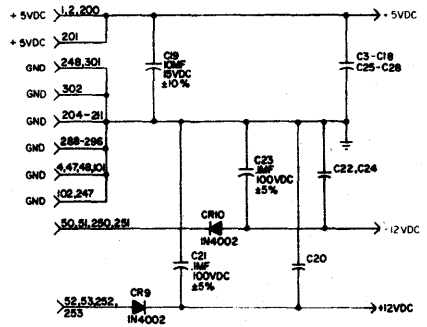
74873383
A
SHEET 8
35700-012-104

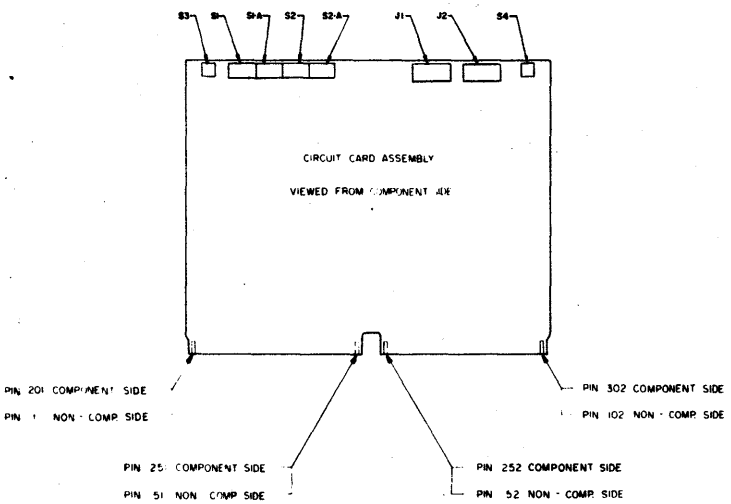


SYN C REGISTER 2
SEARCH SYN C 2
STATUS REGISTER 2
SEE SHEET 1
LSI USAR 1472 D4
CLK
WD LG 2
WD LG 1
EVEN PBIT
PBIT ENBL
MODE SEL 3
MODE SEL 2
MODE SEL 1
CONT RGTR STROBE
RESET ERROR FLAGS
CHIP ENBL
MATCH CHAR HOLD RGTR 8
MATCH CHAR HOLD RGTR 7
MATCH CHAR HOLD RGTR 6
MATCH CHAR HOLD RGTR 5
MATCH CHAR HOLD RGTR 4
MATCH CHAR HOLD RGTR 3
MATCH CHAR HOLD RGTR 2
MATCH CHAR HOLD RGTR 1
MATCH CHAR HOLD RGTR STROBE
DATA/MATCH CHAR RGTRS EQUAL
RESET DATA HOLD RGTR FULL
SER DATA
DATA HOLD RGTR FULL
DATA HOLD RGTR PBIT
DATA HOLD RGTR 8
DATA HOLD RGTR 7
DATA HOLD RGTR 6
DATA HOLD RGTR 5
DATA HOLD RGTR 4
DATA HOLD RGTR 3
DATA HOLD RGTR 2
DATA HOLD RGTR 1
MASTER RESET
PBIT ERROR
SS/FR ERROR
OVERRUN ERROR
INPUT LOOP ERROR 2
CONTROL DATA
LOGIC DIAGRAM –
SYNCHRONOUS CLA I -
OUTPUT PROCESSING
34015 D 74873383
35190-012-104
9


REVISION RECORD
SEE SHEET 1
MODEM CHANGE DETECT 2
LOOP INTERNAL TEST 2
RING DETECT 2
LOOP INTERNAL TEST 2
PROTECTIVE GROUND
CR6 (RD2)
CR8 (DCD2)
CR5 (SD2)
CR7 (RTS2)
RD2*
DCD2*
DSR2*
DCD2*
RI2*
DSRA2*
CTSA2*
RI2A*
DTR2*
RTS2*
TCK2
NSYN2*
SQDA2
SCT2*
SCR2*
QM2*
NSYN*
RD2
TD2
LITCK
SD2*
SCTE2
NSYN2
RTS2
DTR2
SG2
PG2
F12
F22
F42
CONTROL DATA
COMMUNICATIONS PRODUCTS DIV.
LOGIC DIAGRAM — SYNCHRONOUS CLAI- MODEM INTERFACE
34015
D
74873383
A
SHEET 10

SHEET REVISION STATUS										REVISION RECORD						
10	9	8	7	6	5	4	3	2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
02	02	02	02	02	02	02	02	02	02	02	06245	INITIAL RELEASE	TP	3-576	M	M
A	A	A	A	A	A	A	A	A	A	A	06157	INITIAL RELEASE	RL	3-22-77	M	M
A	A	A	A	A	A	A	A	A	A	A	[illegible]	CLAIM A [illegible]	TP	12 12 77	M	M





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES 5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: .01 MF 35 VDC +80-20% (C3-C18, C24-C28, C20, C22)
   ALL DIODES: DIALCO 547-2003, 5V, 6MA (CR1-CR8)

2. COMPONENT ASSEMBLY NO. 74-[illegible]

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL-IN-LINE	14	7
16 PIN DUAL-IN-LINE	16	8

   NON-STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA
AAL030

SBBY

DETACHED LISTS

DO NOT SCALE DRAWING

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV, Santa Ana, Calif. 92704

MFG	
USED ON	DU139-A
DR	
CHK	[illegible] 7-11-77
ENGR	[illegible]
MFG	
APPD	

TITLE: LOGIC DIAGRAM — SYNCHRONOUS CLAI — COAXIAL INTERFACE

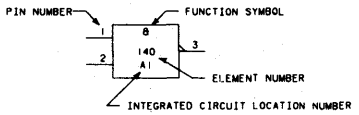
D | CODE IDENT NO 34015 | DRAWING NUMBER 74873013

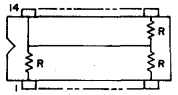
SCALE NONE | SHEET 1 OF 10

6650

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
		SEE SHEET 1				

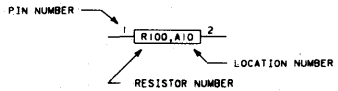
CIRCUIT ELEMENT SYMBOLOGY



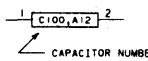


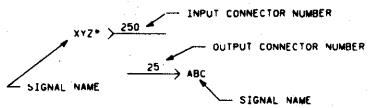
I.C. RESISTOR PACK
LOCATION U5,U20
10K

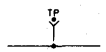
RESISTOR INTEGRATED SYMBOLOGY

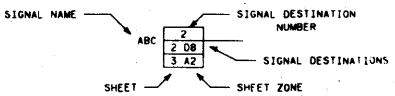


CAPACITOR INTEGRATED SYMBOLOGY

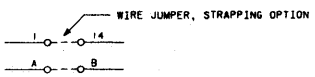








COMMON CONTROL BLOCK. SIGNALS ENTERING THIS BLOCK ARE COMMON TO MORE THAN ONE SECTION OF THE CIRCUIT



IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
140	7400	TTL QUAD 2-INPUT NAND GATE
140L	74L00	TTL QUAD 2-INPUT NAND GATE
141	7410	TTL TRIPLE 3-INPUT NAND GATE
141L	74L10	TTL TRIPLE 3-INPUT NAND GATE
146	7404	TTL HEX INVERTER
146L	74L04	TTL HEX INVERTER
148	7402	TTL QUAD 2-INPUT NOR GATE
148L	74L02	TTL QUAD 2-INPUT NOR GATE
175	7474	TTL DUAL D-TYPE F/F
175L	74L74	TTL DUAL D-TYPE F/F
189	74157	MULTIPLEXER, TTL QUAD 2-INPUT GATE
201	7408	TTL QUAD 2-INPUT AND GATE
202	7403	TTL QUAD 2-INPUT NAND GATE
180	75450	DRIVER, DUAL PERIPHERAL
208	7420	TTL DUAL 4-INPUT NAND GATE
—	7414	HEX SCHMITT TRIGGER INVERTER
223L	74L51	TTL DUAL 2-WIDE 2-3 IN AND-OR-INVERTER
240	9024	TTL DUAL J-K F/F
505	7451	MULTIPLEXER, TTL 8-INPUT GATE
519	74174	LATCH, TTL 6-BIT D-TYPE
520	74175	LATCH, TTL 4-BIT D-TYPE
524L	74L85	COMPARATOR, TTL 4-BIT MAGNITUDE
538	9321	DECODER, TTL DUAL (1 OF 4)
542	8214	MULTIPLEXER TTL DUAL 4-BIT TRISTATE
551	7475	LATCH, TTL 4-BIT
900	MC1488	DRIVER, DTL TO RS-232C QUAD LINE
901	MC1489A	RECEIVER, RS-232C TO DTL QUAD LINE
—	74L86	TTL QUAD 2 INPUT EXCLUSIVE OR GATE
—	74251	MULTIPLEXER, TTL 8-INPUT TRISTATE
—	8096	DRIVER HEX INVERTER TRISTATE
—	9L24	TTL DUAL J-K F/F
—	93L00	REGISTER, TTL 4-BIT UNIVERSAL
—	4050	HEX BUFFER / NON INVERTING
—	PR1472B	P/SAR, MOS/LSI
—	PT1482B	P/SAT, MOS/LSI

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
1⊓	ONE-SHOT MULTIVIBRATOR
⊢	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⌐	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

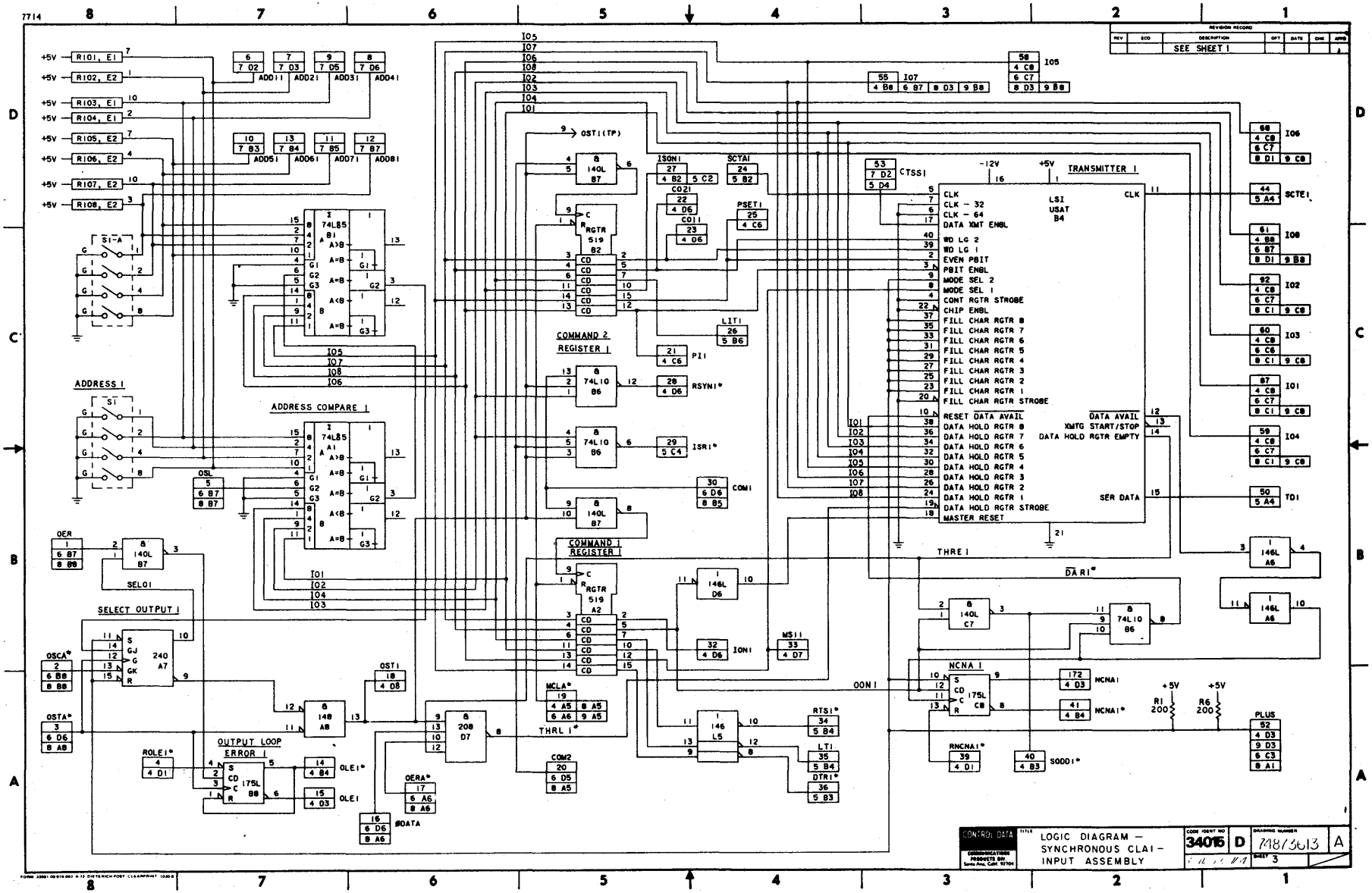
SIGNAL LINE INDICATORS

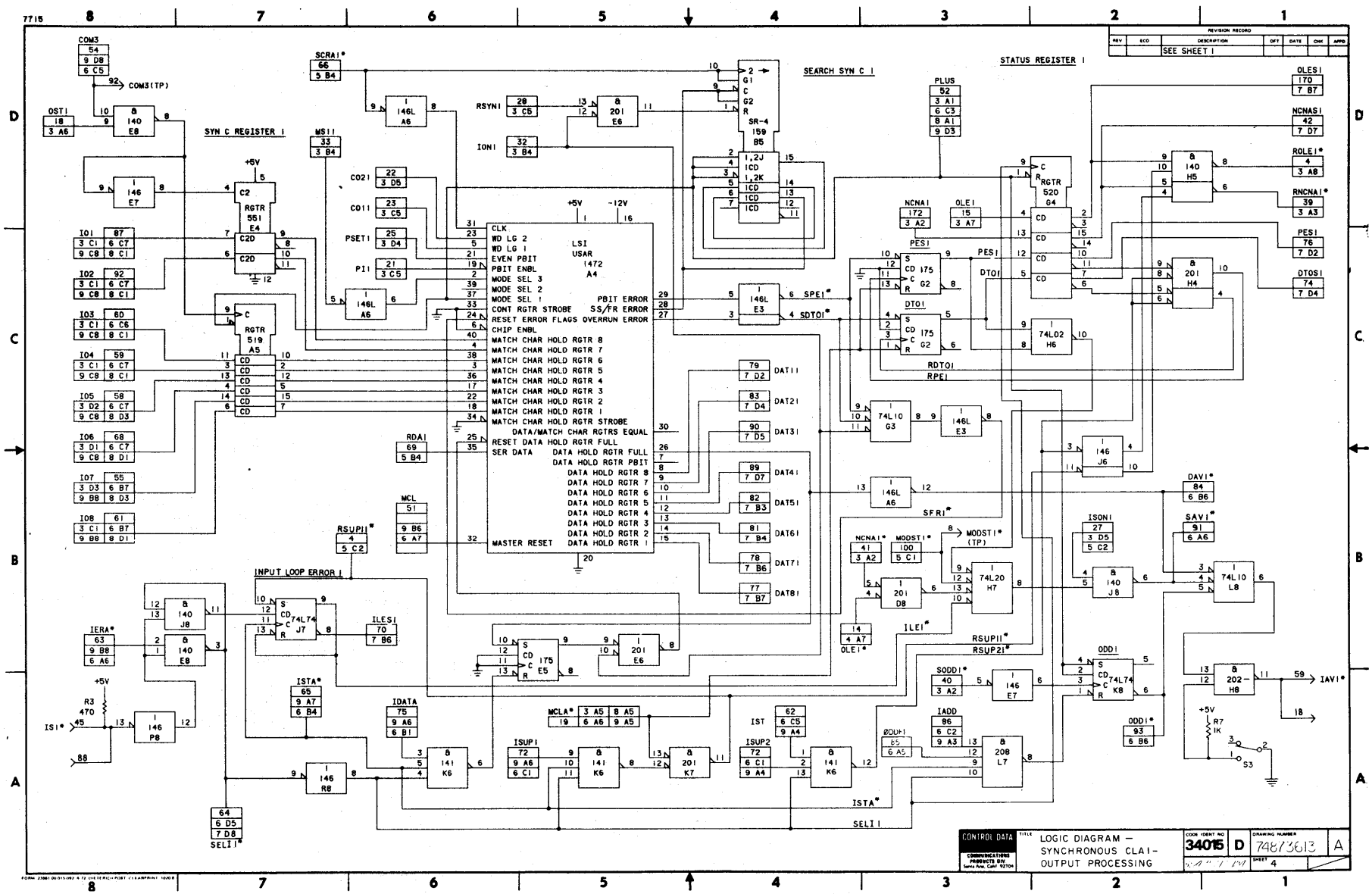
◇& OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
▷	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
⊣	NON-STANDARD LOGIC LEVEL
⊣	ANALOG OR NON-LOGIC LEVEL
⊣	VARIABLE PARAMETER CONTROL
⊣	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
⊣	INHIBIT DESIGNATOR

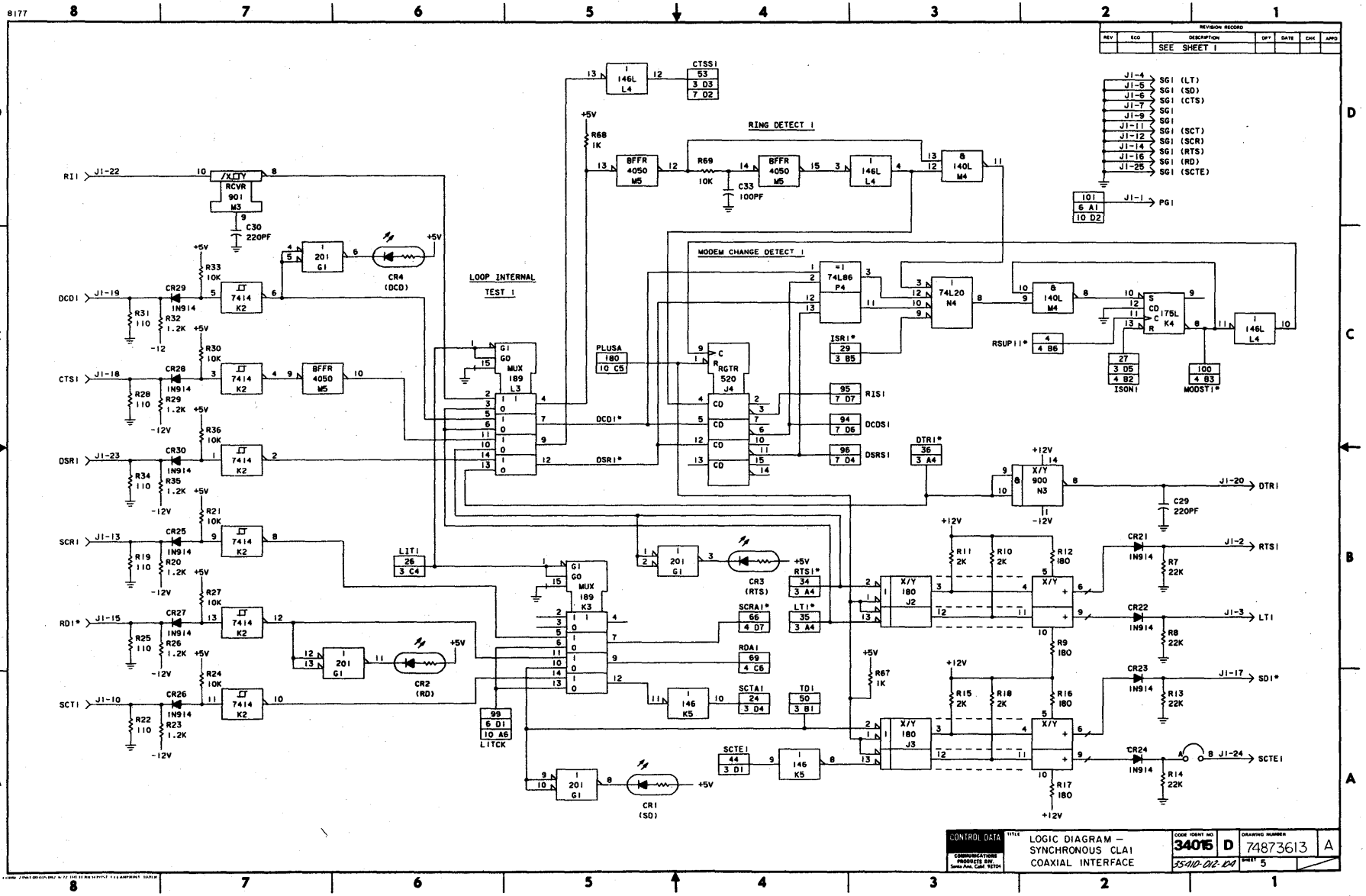
FUNCTION ABBREVIATIONS

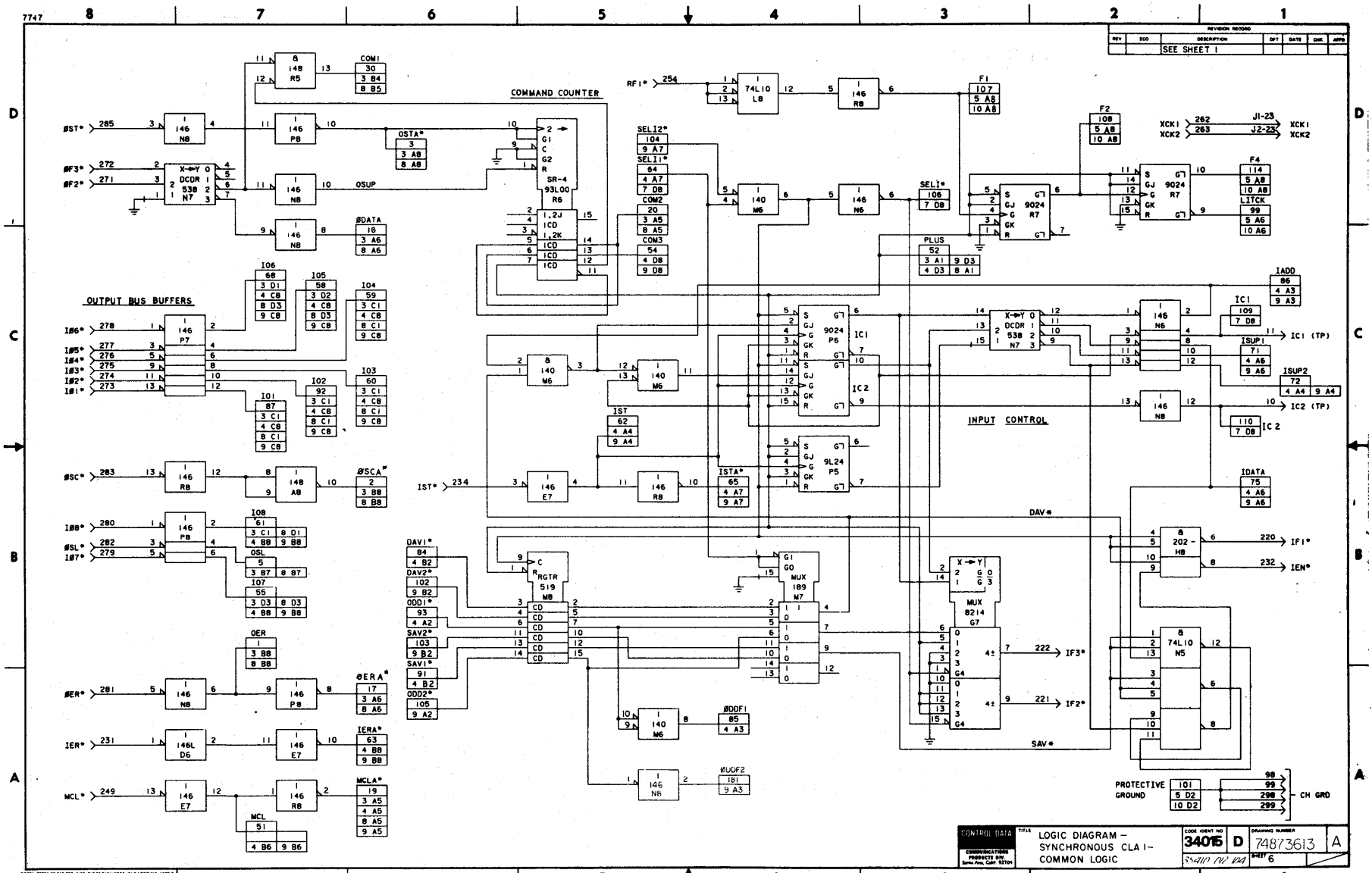
ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

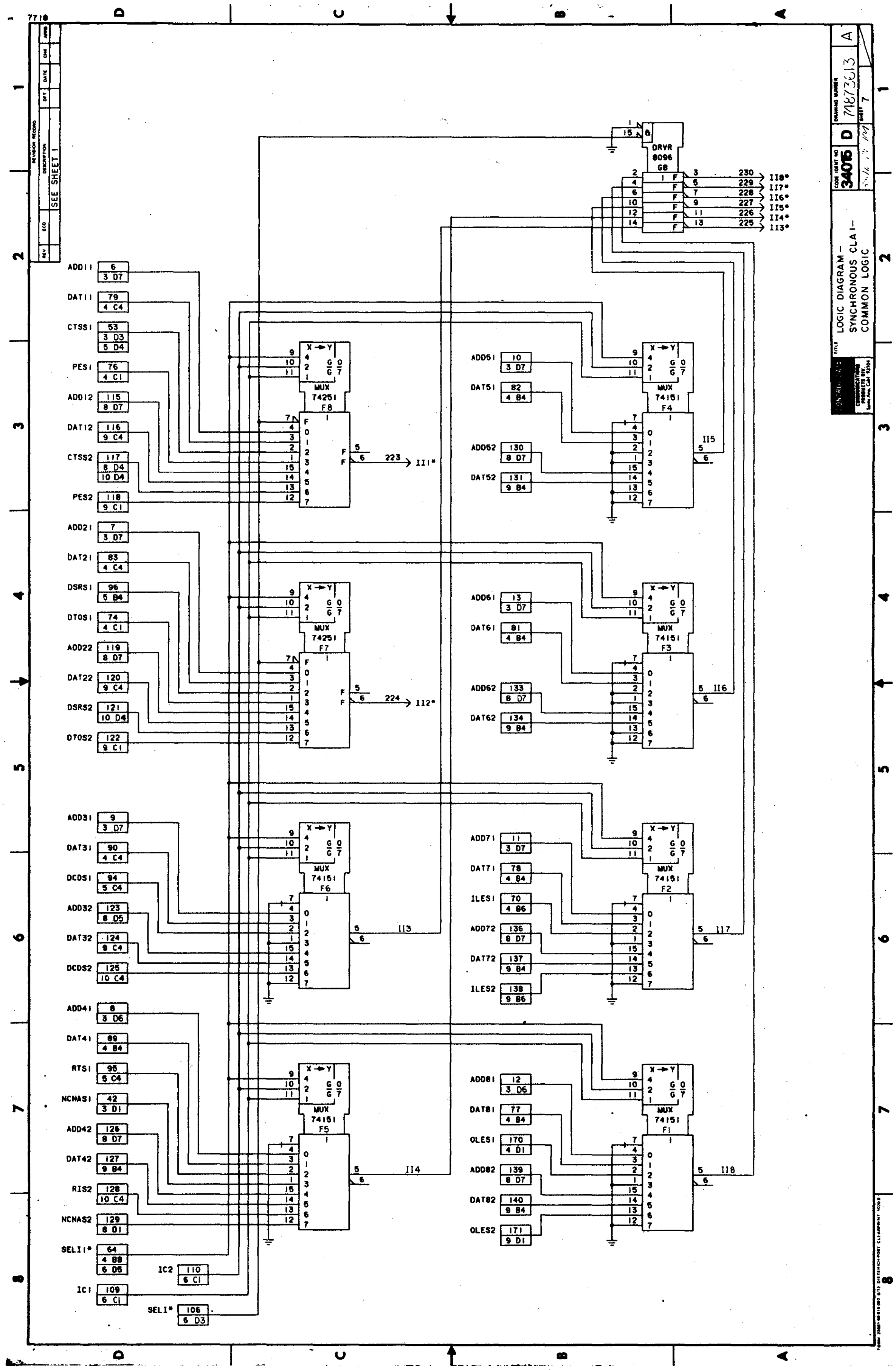
CONTROL DATA COMMUNICATIONS PRODUCTS DIV Santa Ana, Calif. 92704	TITLE: LOGIC DIAGRAM — KEY TO SYMBOLS	CODE IDENT NO 34015	D	DRAWING NUMBER 74873613	A
		8SAND PAT PEND		SHEET 2	

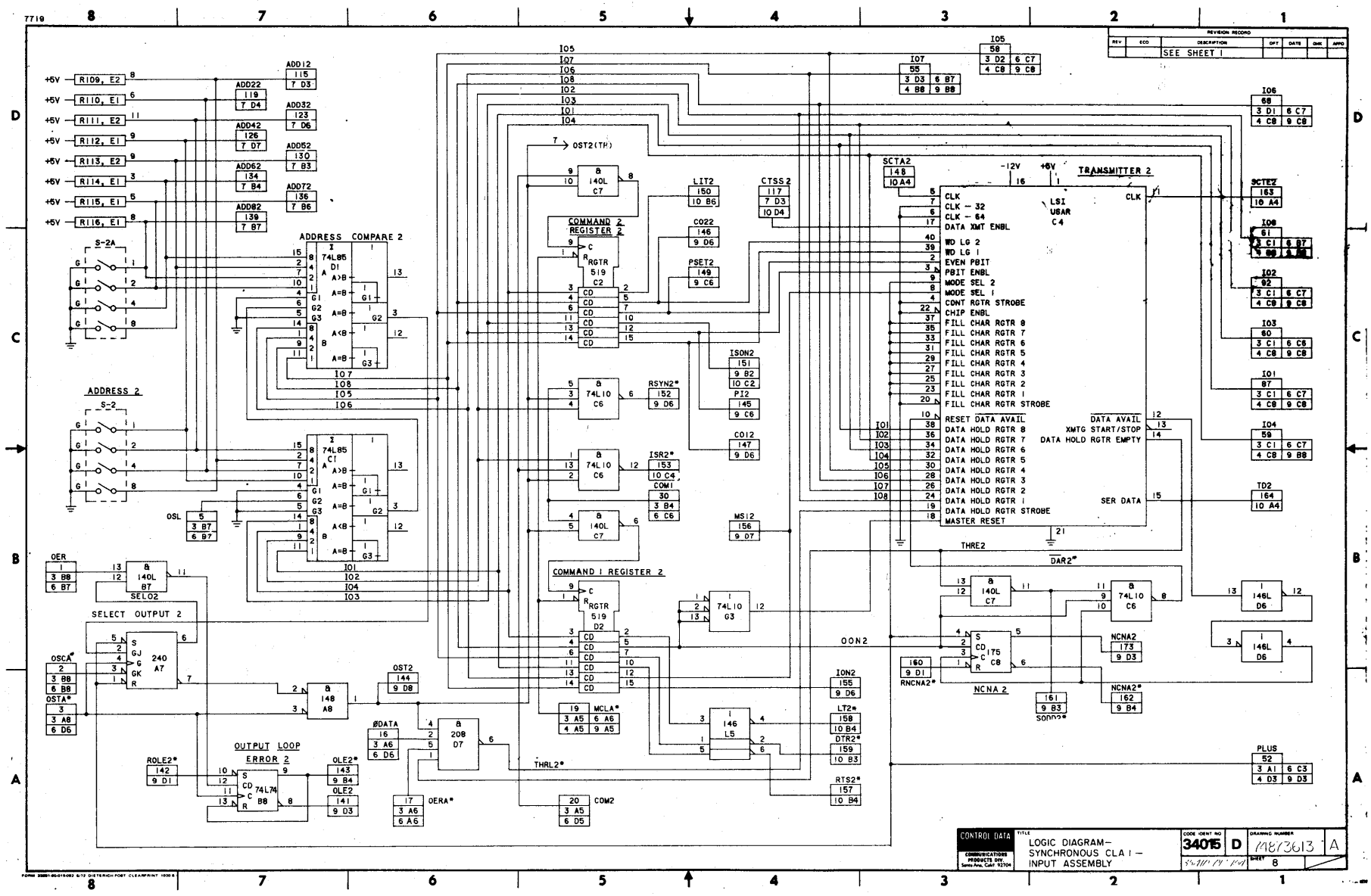

TRANSMITTER I
LSI USAT B4
CLK
CLK – 32
CLK – 64
DATA XMT ENBL
WD LG 2
WD LG 1
EVEN PBIT
PBIT ENBL
MODE SEL 2
MODE SEL 1
CONT RGTR STROBE
CHIP ENBL
FILL CHAR RGTR 8
FILL CHAR RGTR 7
FILL CHAR RGTR 6
FILL CHAR RGTR 5
FILL CHAR RGTR 4
FILL CHAR RGTR 3
FILL CHAR RGTR 2
FILL CHAR RGTR 1
FILL CHAR RGTR STROBE
RESET DATA AVAIL
DATA HOLD RGTR 8
DATA HOLD RGTR 7
DATA HOLD RGTR 6
DATA HOLD RGTR 5
DATA HOLD RGTR 4
DATA HOLD RGTR 3
DATA HOLD RGTR 2
DATA HOLD RGTR 1
DATA HOLD RGTR STROBE
MASTER RESET
DATA AVAIL
XMTG START/STOP
DATA HOLD RGTR EMPTY
SER DATA
ADDRESS I
ADDRESS COMPARE I
COMMAND 2 REGISTER I
COMMAND 1 REGISTER I
SELECT OUTPUT I
OUTPUT LOOP ERROR I
NCNA I
SEE SHEET 1
LOGIC DIAGRAM – SYNCHRONOUS CLAI – INPUT ASSEMBLY
CONTROL DATA
34015
D
A
3

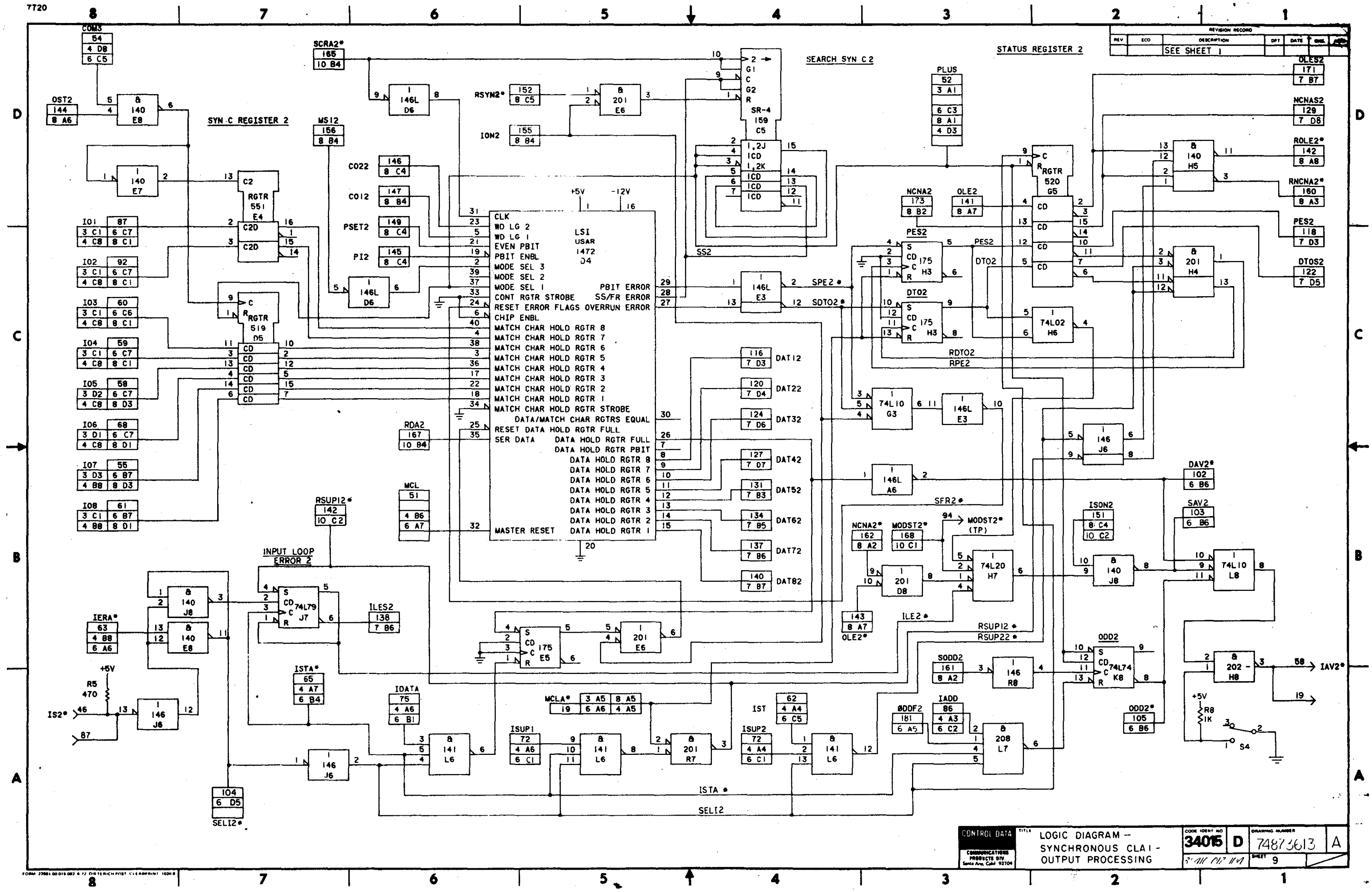

SYN C REGISTER 1
SEARCH SYN C 1
STATUS REGISTER 1
INPUT LOOP ERROR 1
SEE SHEET 1
LOGIC DIAGRAM — SYNCHRONOUS CLAI-OUTPUT PROCESSING
CONTROL DATA
34015
74873613
SHEET 4

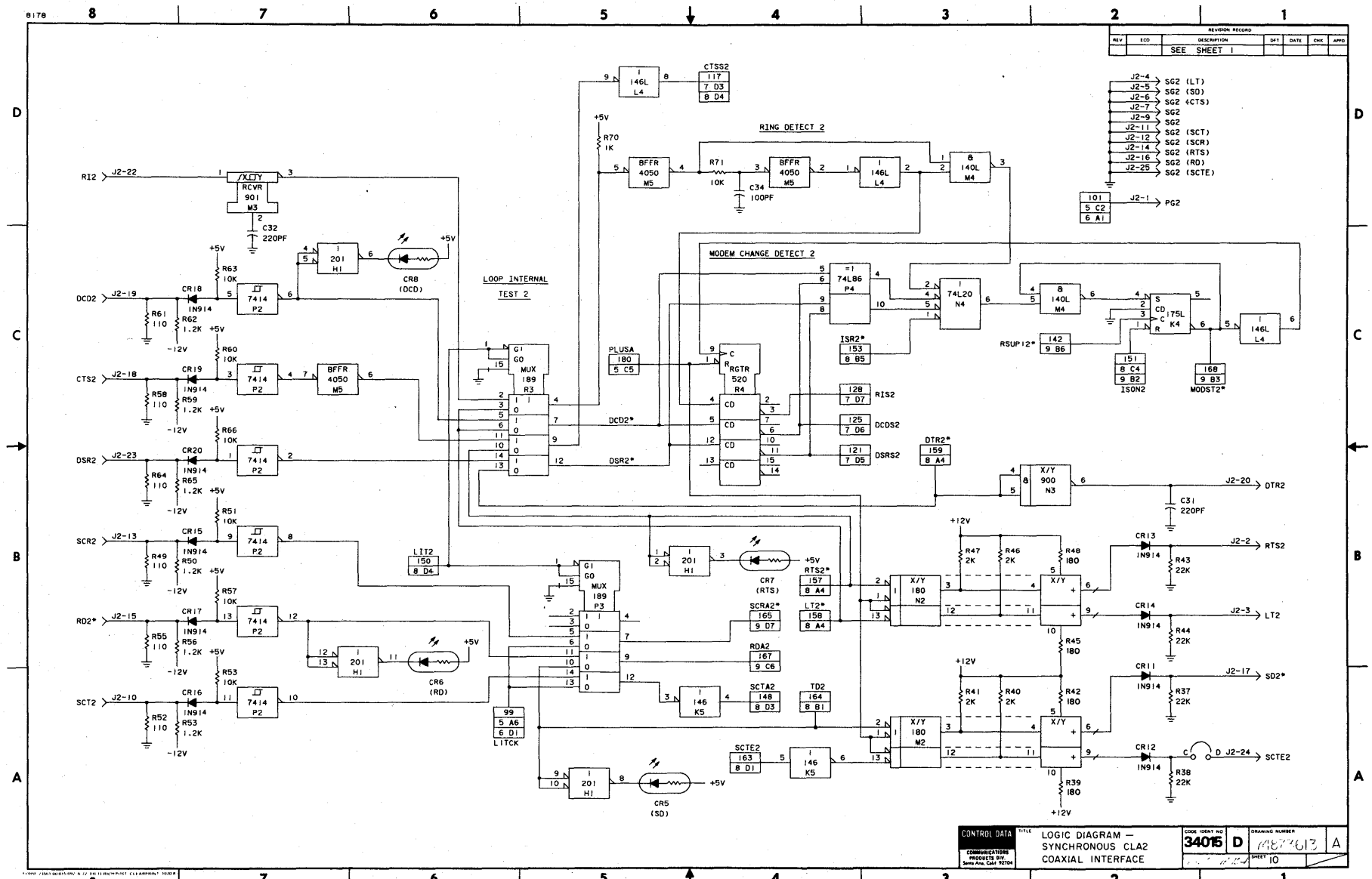

8177
REVISION RECORD
REV ECO DESCRIPTION DFT DATE CHK APPD
SEE SHEET 1
RING DETECT 1
MODEM CHANGE DETECT 1
LOOP INTERNAL TEST 1
RI1 J1-22
DCD1 J1-19
CTS1 J1-18
DSR1 J1-23
SCR1 J1-13
RD1* J1-15
SCT1 J1-10
J1-4 SGI (LT)
J1-5 SGI (SD)
J1-6 SGI (CTS)
J1-7 SGI
J1-9 SGI
J1-11 SGI (SCT)
J1-12 SGI (SCR)
J1-14 SGI (RTS)
J1-16 SGI (RD)
J1-25 SGI (SCTE)
J1-1 PG1
J1-20 DTR1
J1-2 RTS1
J1-3 LT1
J1-17 SD1*
J1-24 SCTE1
CR1 (SD)
CR2 (RD)
CR3 (RTS)
CR4 (DCD)
CONTROL DATA COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92701
TITLE LOGIC DIAGRAM — SYNCHRONOUS CLAI COAXIAL INTERFACE
CODE IDENT NO 34015
D
DRAWING NUMBER 74873613
A
SHEET 5
35410-012-104


COMMAND COUNTER
OUTPUT BUS BUFFERS
INPUT CONTROL
SEE SHEET 1
LOGIC DIAGRAM – SYNCHRONOUS CLA I– COMMON LOGIC
CONTROL DATA
34015
D
74873613
A
SHEET 6
PROTECTIVE GROUND
CH GRD

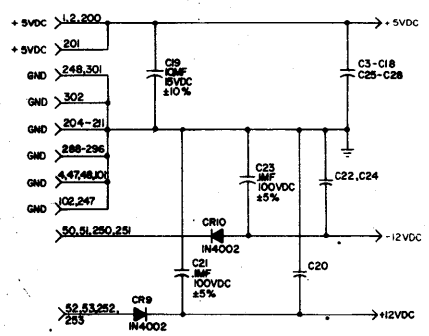

LOGIC DIAGRAM –
SYNCHRONOUS CLA I –
COMMON LOGIC
34015
D
74873613
SHEET 7
A
SEE SHEET 1
REVISION RECORD
REV
ECO
DESCRIPTION
DFT
DATE
CHK
APPD
DRVR
8096
G8
MUX
74251
F8
MUX
74251
F7
MUX
74151
F6
MUX
74151
F5
MUX
74151
F4
MUX
74151
F3
MUX
74151
F2
MUX
74151
F1
ADD11
DAT11
CTSS1
PES1
ADD12
DAT12
CTSS2
PES2
ADD21
DAT21
DSRS1
DTOS1
ADD22
DAT22
DSRS2
DTOS2
ADD31
DAT31
DCDS1
ADD32
DAT32
DCDS2
ADD41
DAT41
RTS1
NCNAS1
ADD42
DAT42
RIS2
NCNAS2
SELI1*
IC2
IC1
SELI*
ADD51
DAT51
ADD52
DAT52
ADD61
DAT61
ADD62
DAT62
ADD71
DAT71
ILES1
ADD72
DAT72
ILES2
ADD81
DAT81
OLES1
ADD82
DAT82
OLES2
I11*
I12*
I13
I14
I15
I16
I17
I18
I18*
I17*
I16*
I15*
I14*
I13*

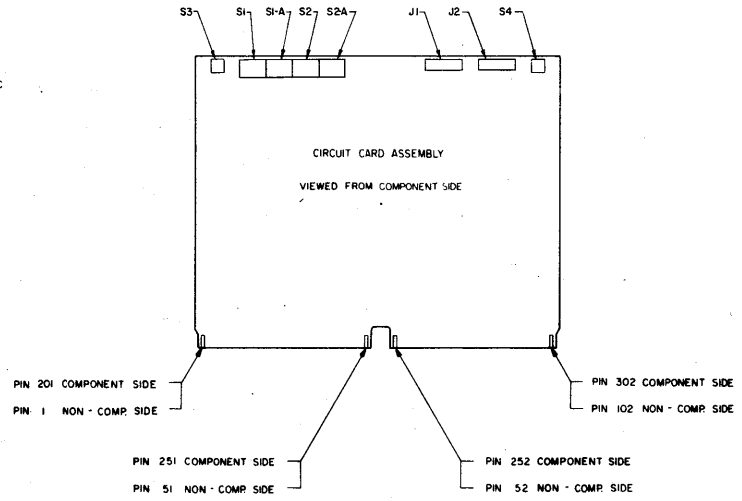

TRANSMITTER 2
ADDRESS COMPARE 2
ADDRESS 2
COMMAND 2 REGISTER 2
COMMAND 1 REGISTER 2
SELECT OUTPUT 2
OUTPUT LOOP ERROR 2
NCNA 2
CLK
CLK - 32
CLK - 64
DATA XMT ENBL
WD LG 2
WD LG 1
EVEN PBIT
PBIT ENBL
MODE SEL 2
MODE SEL 1
CONT RGTR STROBE
CHIP ENBL
FILL CHAR RGTR 8
FILL CHAR RGTR 7
FILL CHAR RGTR 6
FILL CHAR RGTR 5
FILL CHAR RGTR 4
FILL CHAR RGTR 3
FILL CHAR RGTR 2
FILL CHAR RGTR 1
FILL CHAR RGTR STROBE
RESET DATA AVAIL
DATA HOLD RGTR 8
DATA HOLD RGTR 7
DATA HOLD RGTR 6
DATA HOLD RGTR 5
DATA HOLD RGTR 4
DATA HOLD RGTR 3
DATA HOLD RGTR 2
DATA HOLD RGTR 1
DATA HOLD RGTR STROBE
MASTER RESET
DATA AVAIL
XMTG START/STOP
DATA HOLD RGTR EMPTY
SER DATA
SEE SHEET 1
CONTROL DATA
LOGIC DIAGRAM - SYNCHRONOUS CLA I - INPUT ASSEMBLY
34015
D
1873613
A
SHEET 8


LOGIC DIAGRAM — SYNCHRONOUS CLA I - OUTPUT PROCESSING
CONTROL DATA
COMMUNICATIONS PRODUCTS DIV.
34015
D
74873613
A
SHEET 9
SEE SHEET 1
SYN C REGISTER 2
SEARCH SYN C 2
STATUS REGISTER 2
INPUT LOOP ERROR 2
LSI USAR 1472 D4
CLK
WD LG 2
WD LG 1
EVEN PBIT
PBIT ENBL
MODE SEL 3
MODE SEL 2
MODE SEL 1
CONT RGTR STROBE
RESET ERROR FLAGS
CHIP ENBL
MATCH CHAR HOLD RGTR 8
MATCH CHAR HOLD RGTR 7
MATCH CHAR HOLD RGTR 6
MATCH CHAR HOLD RGTR 5
MATCH CHAR HOLD RGTR 4
MATCH CHAR HOLD RGTR 3
MATCH CHAR HOLD RGTR 2
MATCH CHAR HOLD RGTR 1
MATCH CHAR HOLD RGTR STROBE
DATA/MATCH CHAR RGTRS EQUAL
RESET DATA HOLD RGTR FULL
SER DATA
DATA HOLD RGTR FULL
DATA HOLD RGTR PBIT
DATA HOLD RGTR 8
DATA HOLD RGTR 7
DATA HOLD RGTR 6
DATA HOLD RGTR 5
DATA HOLD RGTR 4
DATA HOLD RGTR 3
DATA HOLD RGTR 2
DATA HOLD RGTR 1
MASTER RESET
PBIT ERROR
SS/FR ERROR
OVERRUN ERROR


REVISION RECORD
REV ECO DESCRIPTION DFT DATE CHK APPD
SEE SHEET 1
RING DETECT 2
MODEM CHANGE DETECT 2
LOOP INTERNAL TEST 2
J2-4 SG2 (LT)
J2-5 SG2 (SD)
J2-6 SG2 (CTS)
J2-7 SG2
J2-9 SG2
J2-11 SG2 (SCT)
J2-12 SG2 (SCR)
J2-14 SG2 (RTS)
J2-16 SG2 (RD)
J2-25 SG2 (SCTE)
J2-1 PG2
R12 J2-22
DCD2 J2-19
CTS2 J2-18
DSR2 J2-23
SCR2 J2-13
RD2* J2-15
SCT2 J2-10
CR8 (DCD)
CR7 (RTS)
CR6 (RD)
CR5 (SD)
PLUSA
ISR2*
RSUP12*
ISON2
MODST2*
RIS2
DCDS2
DSRS2
DTR2*
RTS2*
SCRA2*
LT2*
RDA2
SCTA2
TD2
SCTE2
LITCK
J2-20 DTR2
J2-2 RTS2
J2-3 LT2
J2-17 SD2*
J2-24 SCTE2
CONTROL DATA COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif 92704
LOGIC DIAGRAM — SYNCHRONOUS CLA2 COAXIAL INTERFACE
CODE IDENT NO 34015
D
DRAWING NUMBER 1887613 A
SHEET 10

SHEET REVISION STATUS										REVISION RECORD					
10	9	8	7	6	5	4	3	2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
01	01	01	01	01	01	01	01	01	01	01	06124	INITIAL RELEASE	JTP	12-16-75	JH	JH
02	02	02	02	02	02	02	02	02	02	02	06758	INITIAL RELEASE	PL	3-31-77	JH	JH
A	A	A	A	A	A	A	A	A	A	A	08063	CLASS A RELEASE CBM	TP	12-12-77	JH	JH





NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTOR VALUES 5%
   ALL RESISTOR VALUES IN OHMS
   ALL RESISTORS RATED 1/4 WATT
   ALL CAPACITOR VALUES: .01 MF 35 VDC +80-20%.(C3-C18,C24-C28,C20,C22)
   ALL DIODES: DIALCO 547-2003, 5V, 6MA (CR1-CR8)

2. COMPONENT ASSEMBLY NO. 74873630

3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS

	5VDC	GND
14 PIN DUAL - IN - LINE	14	7
16 PIN DUAL - IN - LINE	16	8

   NON - STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS

5BBY

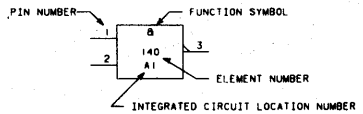
Changes to this document require approval of all Data Division per CDC-000 1.01.001. CA

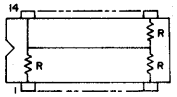
UNLESS OTHERWISE SPECIFIED DIMS ARE IN INCHES/ALL METRIC TOLERANCES: 2 PLACE ±.03, 3 PLACE ±.010, ANGLES ±1°	CONTROL DATA CORPORATION PERIPHERAL PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE	LOGIC DIAGRAM – SYNCHRONOUS CLAI – DIFFERENTIAL
DO NOT SCALE DRAWING	DRAWN DU140-A		
MATERIAL	CHK PRELIMINARY 4-20-76		
FINISH	ENGR 5-17-76	CODE IDENT NO. 34015	DRAWING NUMBER 74873631
DETACHED LISTS	MFG 12-16-75	SCALE NONE	35420-012-104
	APPD	SHEET 1 OF 10	

6650

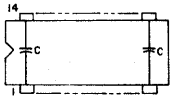
REVISION RECORD						
REV	ECO	DESCRIPTION	DRT	DATE	CHK	APPD
		SEE SHEET 1				

CIRCUIT ELEMENT SYMBOLOGY



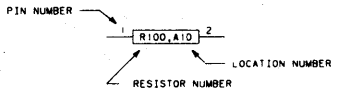


I.C. RESISTOR PACK
LOCATION U5,U20
10K

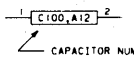


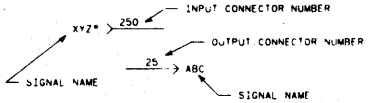
I.C. CAPACITOR PACK
LOCATION U24,U28
220PF

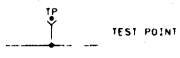
RESISTOR INTEGRATED SYMBOLOGY

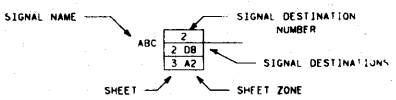


CAPACITOR INTEGRATED SYMBOLOGY

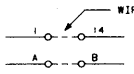








COMMON CONTROL BLOCK. SIGNALS ENTERING THIS BLOCK ARE COMMON TO MORE THAN ONE SECTION OF THE CIRCUIT



IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
140	7400	TTL QUAD 2-INPUT NAND GATE
140L	74L00	TTL QUAD 2-INPUT NAND GATE
141	7410	TTL TRIPLE 3-INPUT NAND GATE
141L	74L10	TTL TRIPLE 3-INPUT NAND GATE
146	7404	TTL HEX INVERTER
146L	74L04	TTL HEX INVERTER
148	7402	TTL QUAD 2-INPUT NOR GATE
148L	74L02	TTL QUAD 2-INPUT NOR GATE
175	7474	TTL DUAL D-TYPE F/F
175L	74L74	TTL DUAL D-TYPE F/F
189	74157	MULTIPLEXER, TTL QUAD 2-INPUT GATE
201	7408	TTL QUAD 2-INPUT AND GATE
202	7403	TTL QUAD 2-INPUT NAND GATE
187	96140	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
208	7420	TTL DUAL 4-INPUT NAND GATE
208L	74L20	TTL DUAL 4-INPUT NAND GATE
188	96150	TTL QUAD 2-2-2-4 INPUT NOR GATE
240	9024	TTL DUAL J-K F/F
505	74151	MULTIPLEXER, TTL 8-INPUT GATE
519	74174	LATCH, TTL 6-BIT D-TYPE
520	74175	LATCH, TTL 4-BIT D-TYPE
524L	74L85	COMPARATOR, TTL 4-BIT MAGNITUDE
538	9321	DECODER, TTL DUAL (1 OF 4)
542	8214	MULTIPLEXER TTL DUAL 4-BIT TRISTATE
551	7475	LATCH, TTL 4-BIT
900	MC1488	DRIVER, DTL TO RS-232C QUAD LINE
901	MC1489A	RECEIVER, RS-232C TO DTL QUAD LINE
—	74L86	TTL QUAD 2 INPUT EXCLUSIVE OR GATE
—	74251	MULTIPLEXER, TTL 8-INPUT TRISTATE
—	8096	DRIVER HEX INVERTER TRISTATE
—	9L24	TTL DUAL J-K F/F
—	93L00	REGISTER, TTL 4-BIT UNIVERSAL
—	4050	HEX BUFFER / NON INVERTING
—	P1472B	P/SAR, MOS/LSI
—	PT1482B	P/SAT, MOS/LSI

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
8	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⊓	SCHMITT TRIGGER
⊓⊔	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A 'D' INPUT ONLY
L	USED ONLY WITH INHIBIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH INHIBIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⊓	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

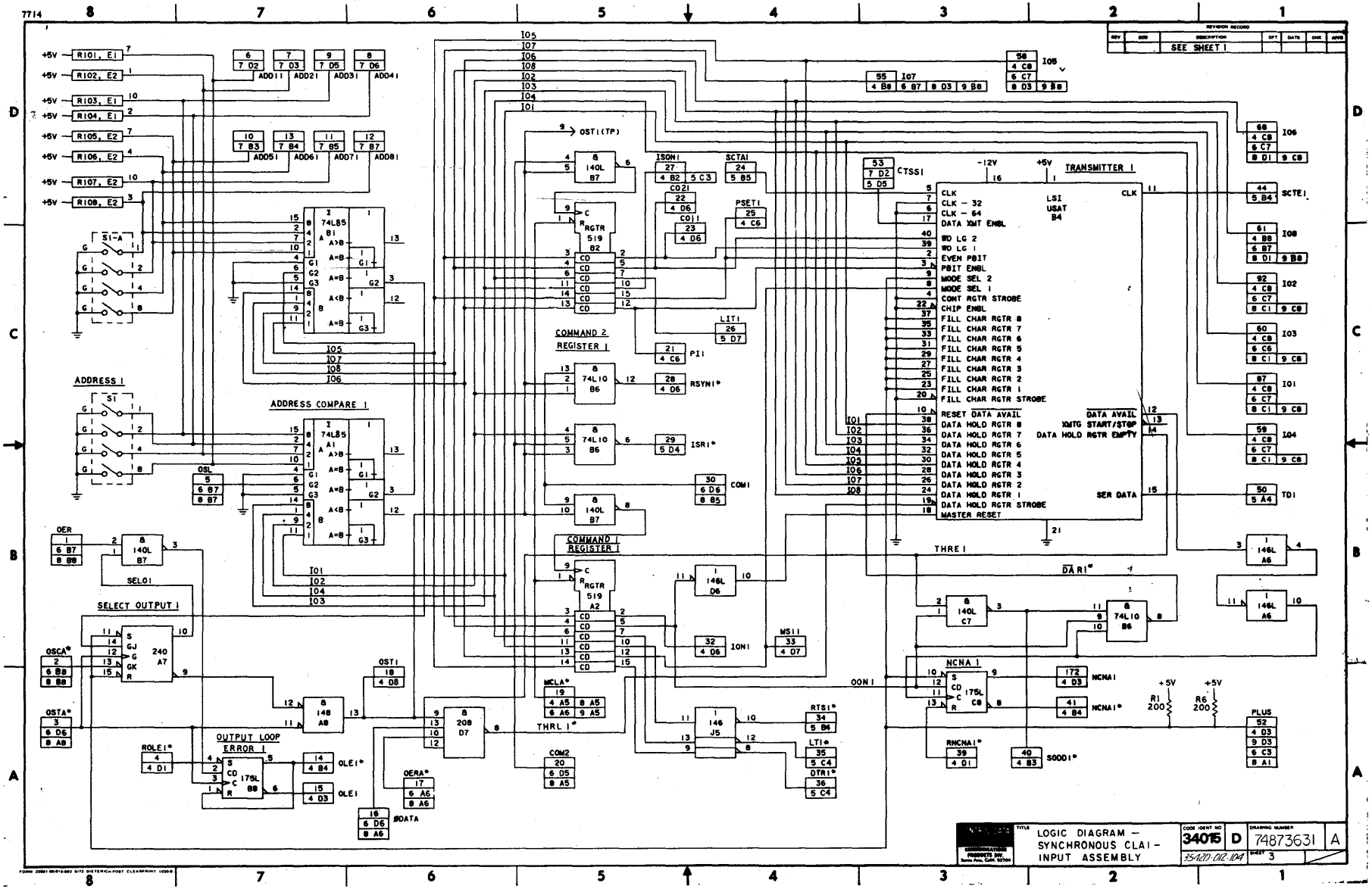
SIGNAL LINE INDICATORS

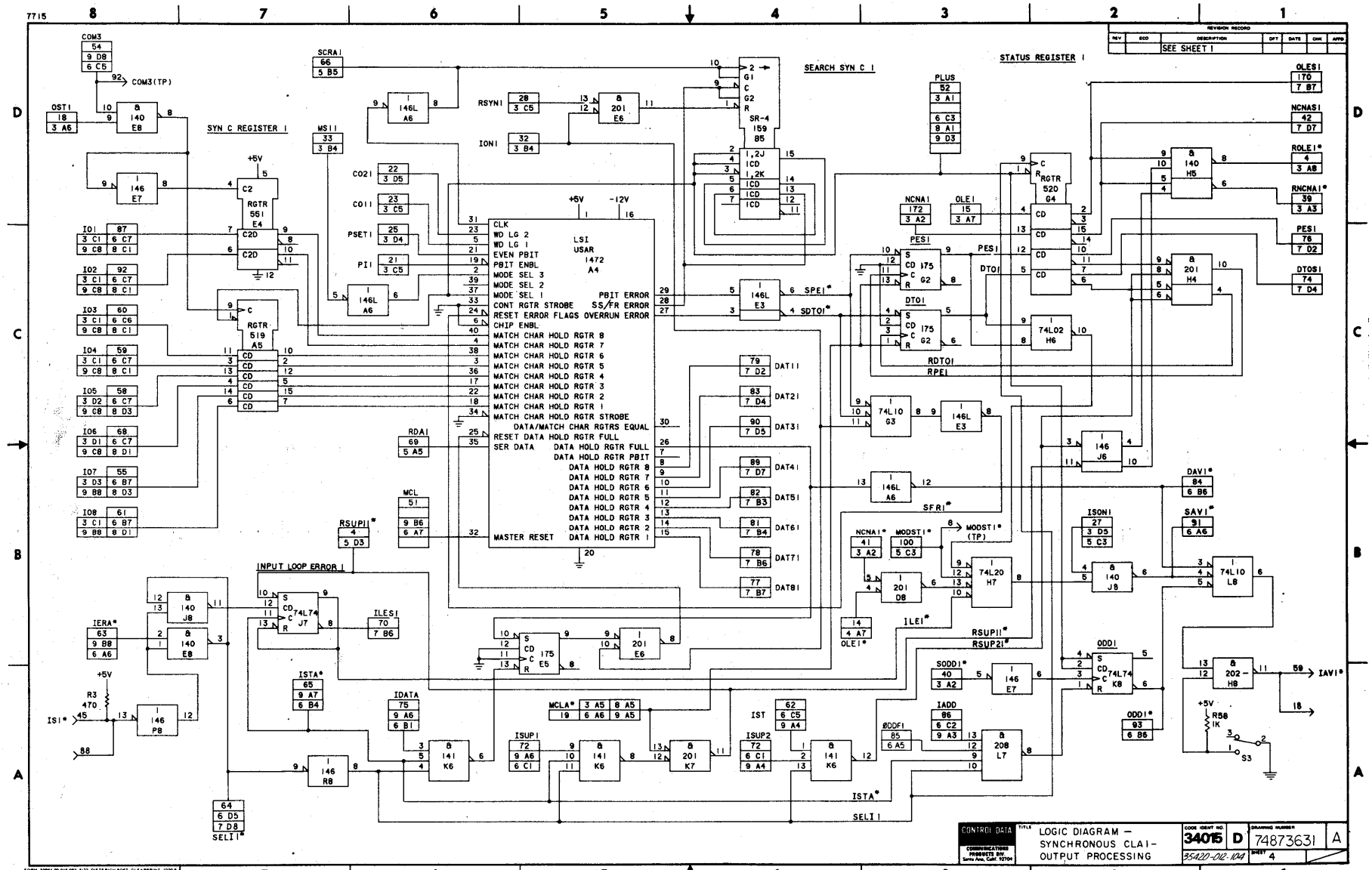
◇8 OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
◺	POLARITY CONVENTION, NEGATIVE POTENTIAL
▷	DYNAMIC INPUT, TRANSITION FROM '0' STATE TO '1' STATE
⊣⊢	NON-STANDARD LOGIC LEVEL
⊣⊢	ANALOG OR NON-LOGIC LEVEL
⊣⊢	VARIABLE PARAMETER CONTROL
⊣⊢	INHIBIT DESIGNATOR WITH POLARITY INDICATOR
⊣⊢	INHIBIT DESIGNATOR

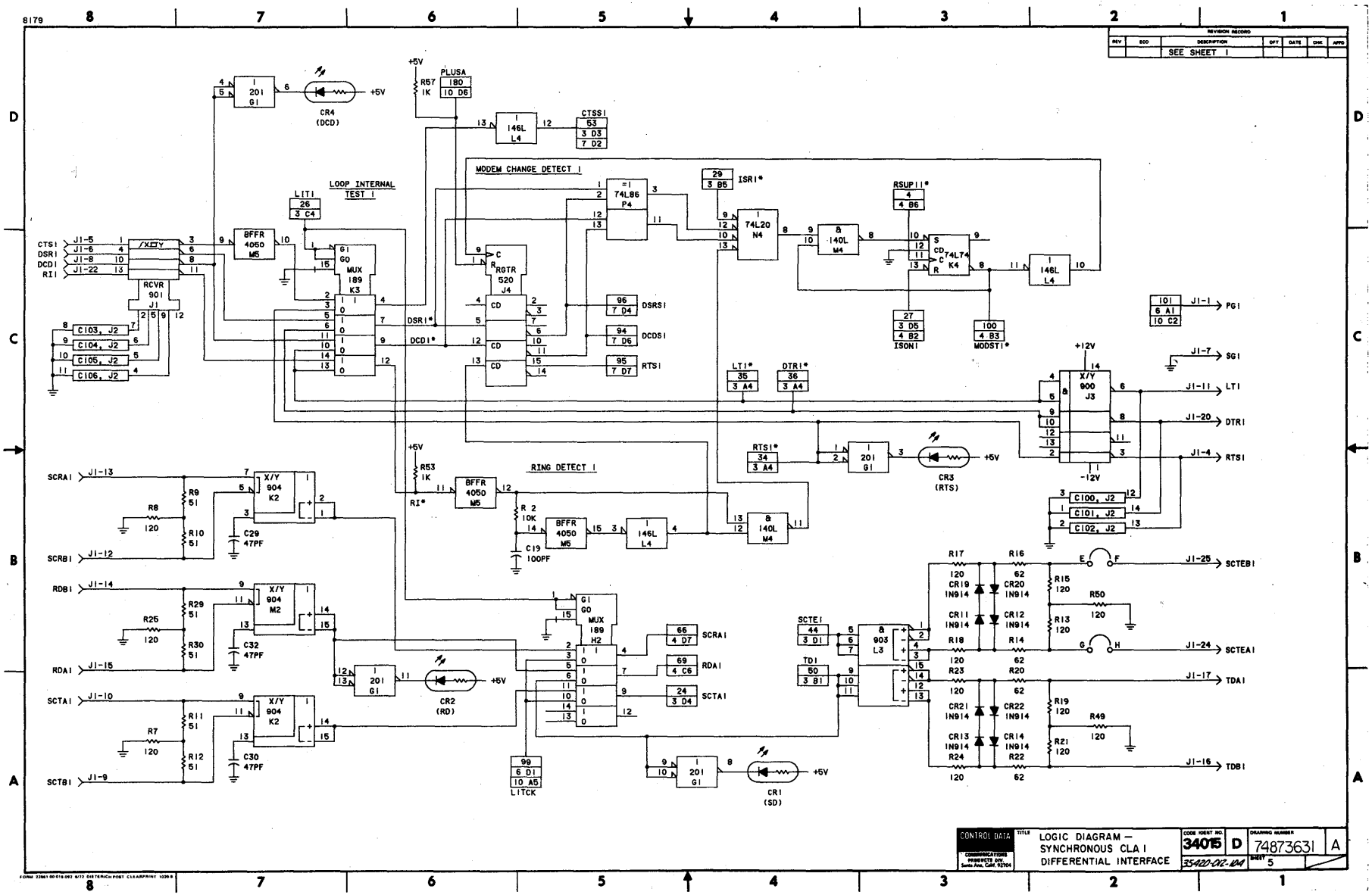
FUNCTION ABBREVIATIONS

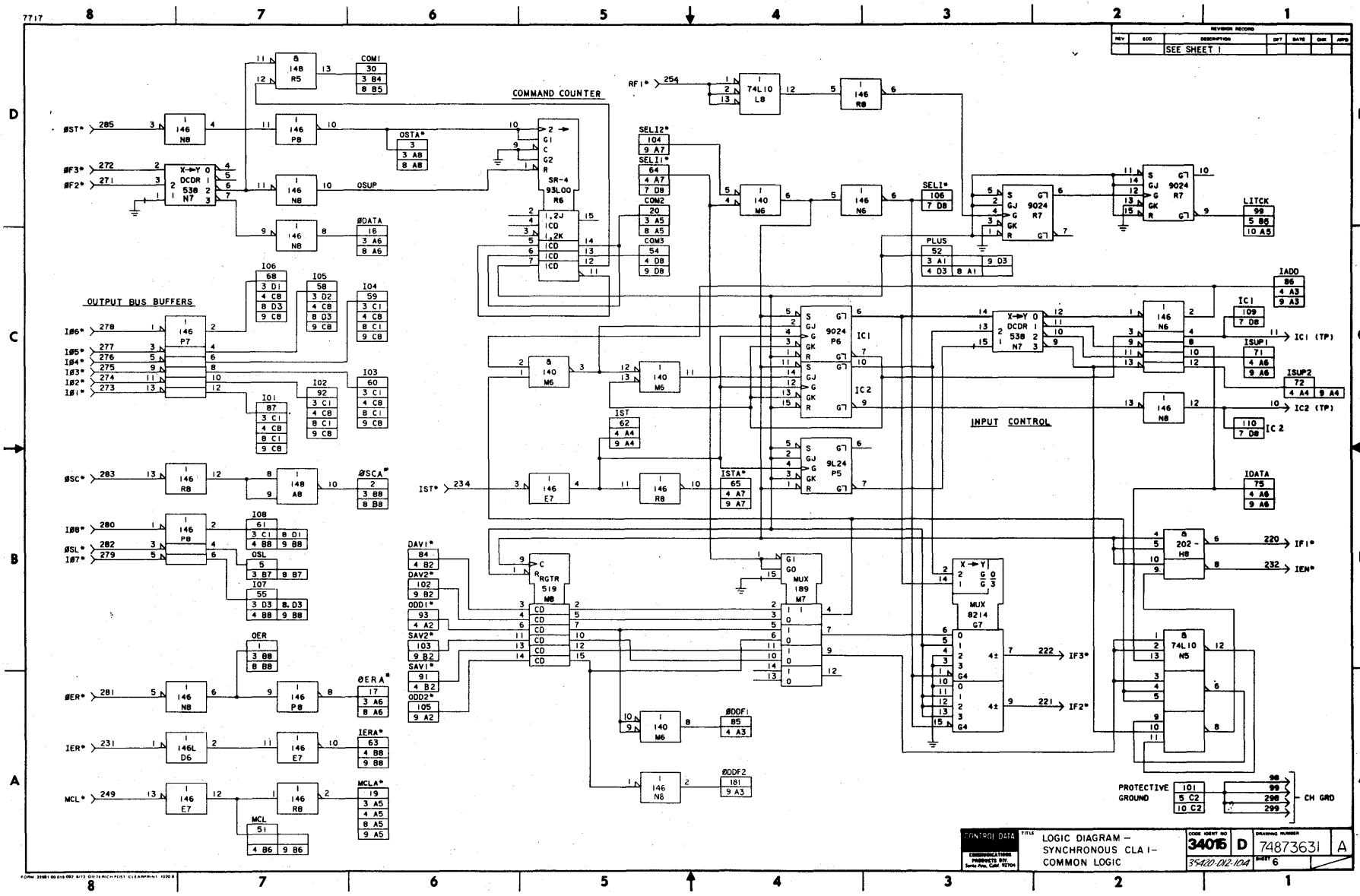
ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

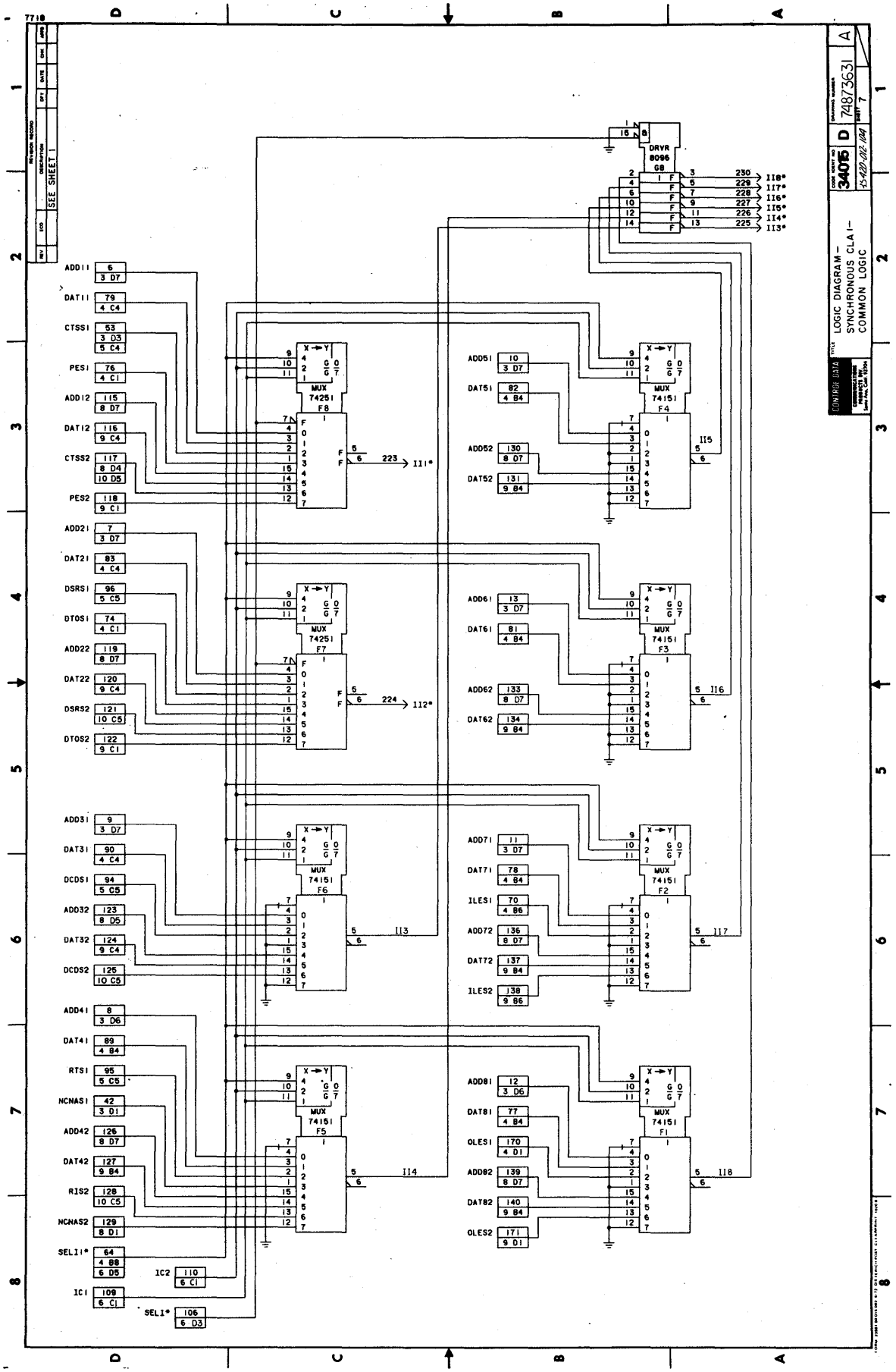
CONTROL DATA COMMUNICATIONS PRODUCTS DIV Santa Ana, Calif. 92704	LOGIC DIAGRAM — KEY TO SYMBOLS	DIVISION IDENT NO. 34015	D	DRAWING NUMBER 74873631	A
				SHEET 2	

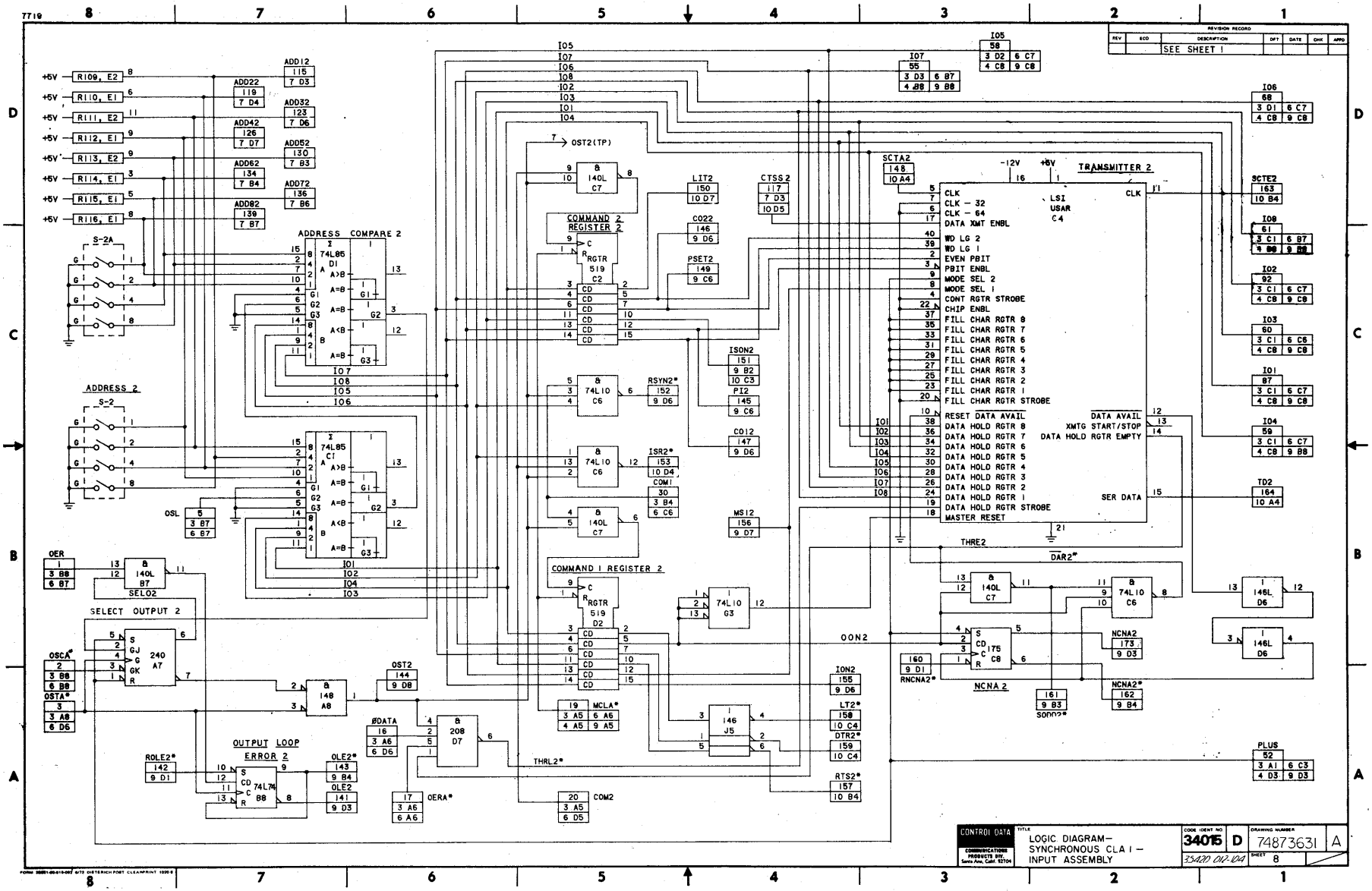

TRANSMITTER 1
LSI USAT B4
ADDRESS 1
ADDRESS COMPARE 1
COMMAND 2 REGISTER 1
COMMAND 1 REGISTER 1
SELECT OUTPUT 1
OUTPUT LOOP ERROR 1
NCNA 1
LOGIC DIAGRAM — SYNCHRONOUS CLAI-INPUT ASSEMBLY
34015
D
74873631
A
SHEET 3
SEE SHEET 1

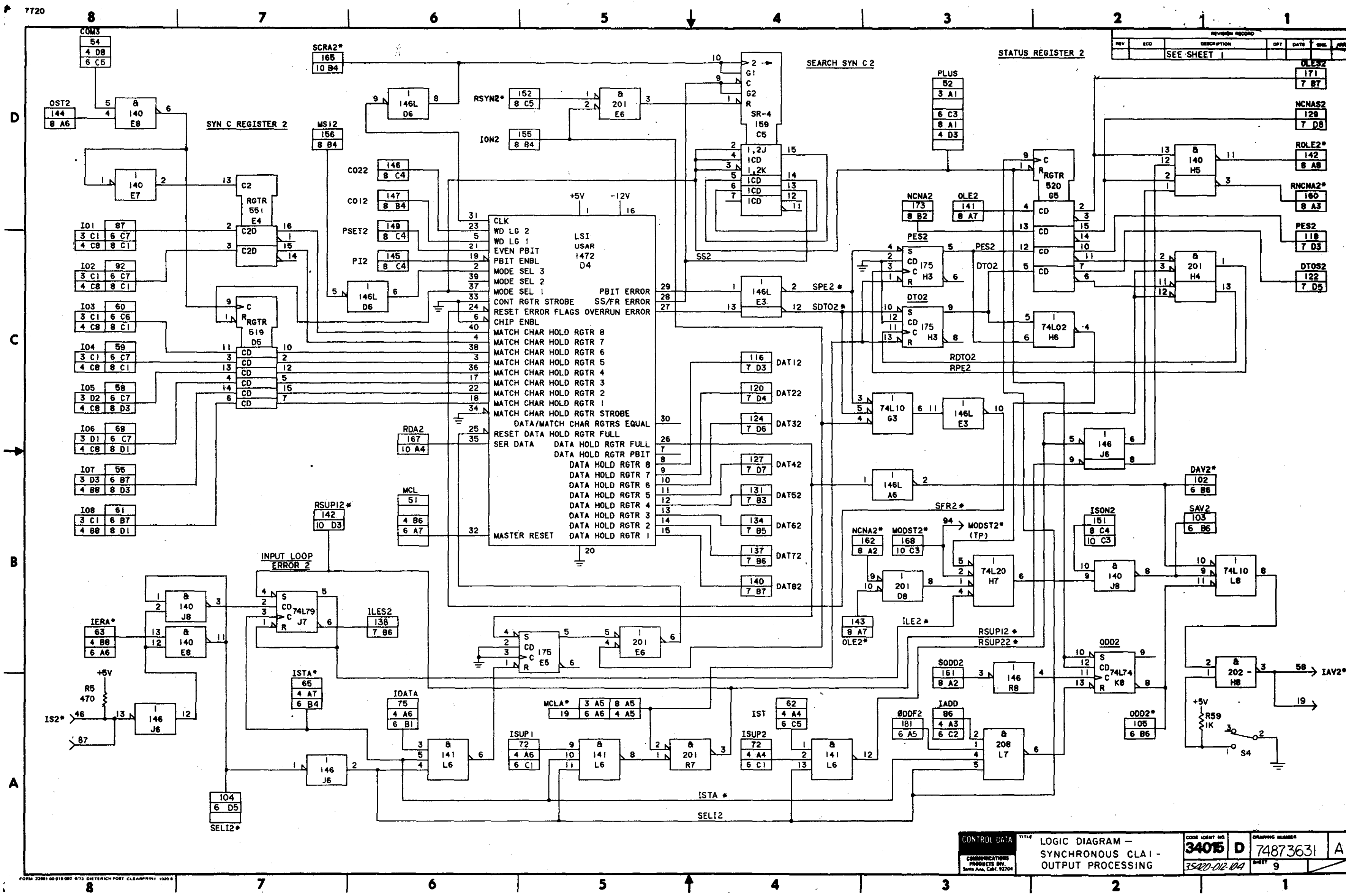

SYN C REGISTER 1
STATUS REGISTER 1
SEARCH SYN C 1
INPUT LOOP ERROR 1
SEE SHEET 1
LOGIC DIAGRAM — SYNCHRONOUS CLAI-OUTPUT PROCESSING
CONTROL DATA
34015
D
74873631
A
35420-012-104
SHEET 4

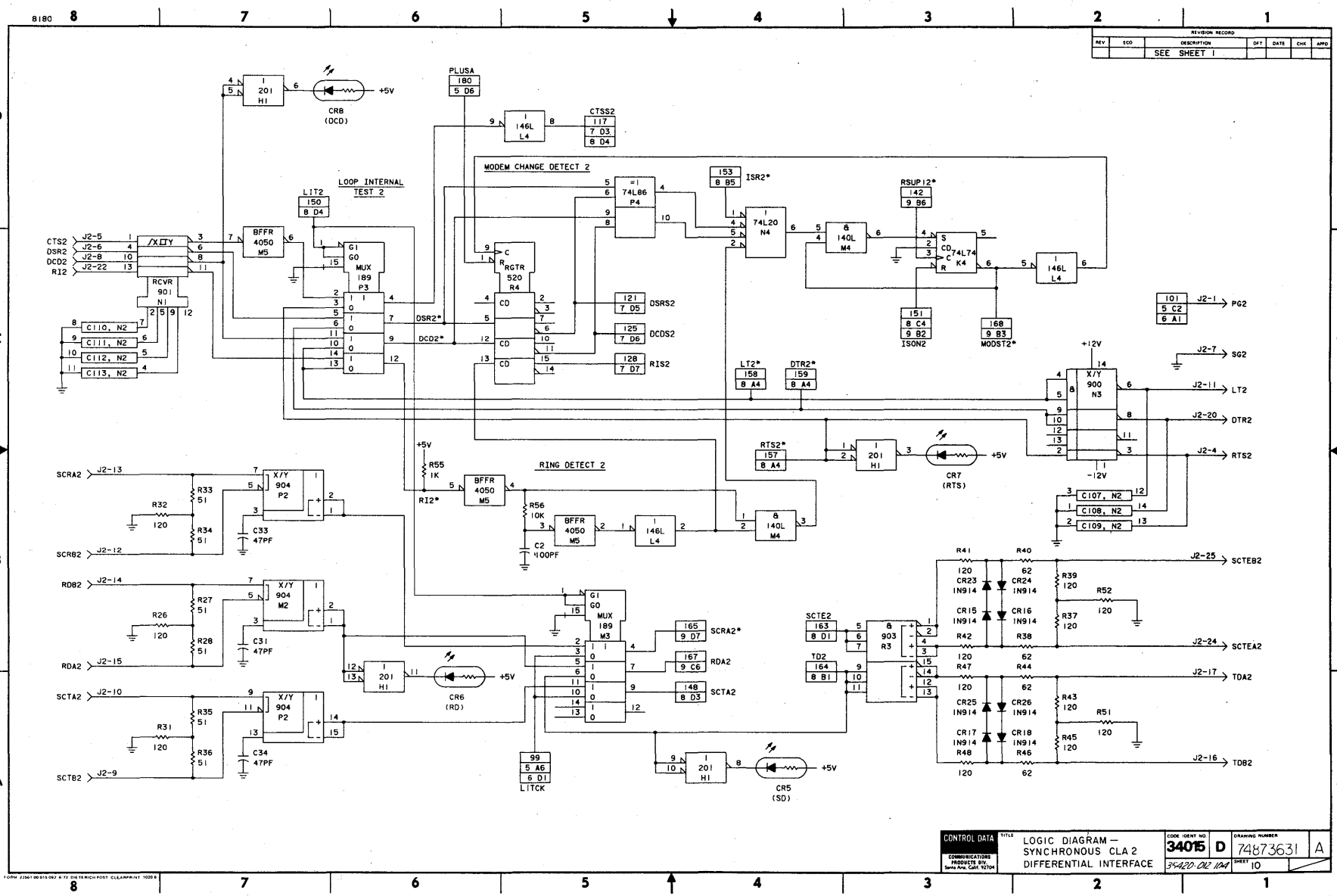

8179
REVISION RECORD
SEE SHEET 1
MODEM CHANGE DETECT 1
LOOP INTERNAL TEST 1
RING DETECT 1
CR4 (DCD)
CR3 (RTS)
CR2 (RD)
CR1 (SD)
LITCK
CTSI
DSRI
DCDI
RI
SCRAI
SCRBI
RDBI
RDAI
SCTAI
SCTBI
DSRI*
DCDI*
RI*
RTSI*
LTI*
DTRI*
ISRI*
RSUPII*
ISONI
MODSTI*
SCTEI
TDI
PG1
SG1
LTI
DTRI
RTSI
SCTEBI
SCTEAI
TDAI
TDBI
+5V
+12V
-12V
CONTROL DATA
COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704
LOGIC DIAGRAM — SYNCHRONOUS CLA I DIFFERENTIAL INTERFACE
CODE IDENT NO. 34015
D
DRAWING NUMBER 74873631
A
SHEET 5
35420-02-104


COMMAND COUNTER
OUTPUT BUS BUFFERS
INPUT CONTROL
SEE SHEET 1
LOGIC DIAGRAM – SYNCHRONOUS CLA I– COMMON LOGIC
CONTROL DATA
34015
D
74873631
A
6
34420-012-104
PROTECTIVE GROUND
CH GRD


DRVR 8096 G8
MUX 74251 F8
MUX 74251 F7
MUX 74151 F6
MUX 74151 F5
MUX 74151 F4
MUX 74151 F3
MUX 74151 F2
MUX 74151 F1
ADD11
DAT11
CTSS1
PES1
ADD12
DAT12
CTSS2
PES2
ADD21
DAT21
DSRS1
DTOS1
ADD22
DAT22
DSRS2
DTOS2
ADD31
DAT31
DCDS1
ADD32
DAT32
DCDS2
ADD41
DAT41
RTS1
NCNAS1
ADD42
DAT42
RIS2
NCNAS2
SELI1*
IC2
IC1
SELI*
ADD51
DAT51
ADD52
DAT52
ADD61
DAT61
ADD62
DAT62
ADD71
DAT71
ILES1
ADD72
DAT72
ILES2
ADD81
DAT81
OLES1
ADD82
DAT82
OLES2
II8*
II7*
II6*
II5*
II4*
II3*
II1*
II2*
II5
II6
II7
II4
II8
II3
LOGIC DIAGRAM - SYNCHRONOUS CLA I - COMMON LOGIC
CONTROL DATA
74873631


TRANSMITTER 2
ADDRESS COMPARE 2
ADDRESS 2
COMMAND 2 REGISTER 2
COMMAND 1 REGISTER 2
SELECT OUTPUT 2
OUTPUT LOOP ERROR 2
LSI USAR C4
SEE SHEET 1
LOGIC DIAGRAM— SYNCHRONOUS CLA I— INPUT ASSEMBLY
CONTROL DATA
34015
74873631


SYN C REGISTER 2
SEARCH SYN C 2
STATUS REGISTER 2
INPUT LOOP ERROR 2
SEE SHEET 1
LSI USAR 1472 D4
CLK
WD LG 2
WD LG 1
EVEN PBIT
PBIT ENBL
MODE SEL 3
MODE SEL 2
MODE SEL 1
CONT RGTR STROBE
RESET ERROR FLAGS
CHIP ENBL
MATCH CHAR HOLD RGTR 8
MATCH CHAR HOLD RGTR 7
MATCH CHAR HOLD RGTR 6
MATCH CHAR HOLD RGTR 5
MATCH CHAR HOLD RGTR 4
MATCH CHAR HOLD RGTR 3
MATCH CHAR HOLD RGTR 2
MATCH CHAR HOLD RGTR 1
MATCH CHAR HOLD RGTR STROBE
DATA/MATCH CHAR RGTRS EQUAL
RESET DATA HOLD RGTR FULL
SER DATA
DATA HOLD RGTR FULL
DATA HOLD RGTR PBIT
DATA HOLD RGTR 8
DATA HOLD RGTR 7
DATA HOLD RGTR 6
DATA HOLD RGTR 5
DATA HOLD RGTR 4
DATA HOLD RGTR 3
DATA HOLD RGTR 2
DATA HOLD RGTR 1
PBIT ERROR
SS/FR ERROR
OVERRUN ERROR
MASTER RESET
+5V
-12V
COM3
OST2
SCRA2*
MS12
RSYN2*
ION2
CO22
CO12
PSET2
PI2
RDA2
MCL
RSUPI2*
IERA*
IS2*
ISTA*
IOATA
MCLA*
ISUP1
ISUP2
IST
ØDDF2
IADD
SODD2
ODD2
ODD2*
PLUS
NCNA2
OLE2
PES2
DTO2
SPE2*
SDTO2*
SS2
RDTO2
RPE2
SFR2*
NCNA2*
MODST2*
MODST2* (TP)
ILE2*
RSUPI2*
RSUP22*
ILES2
ISON2
SAV2
DAV2*
OLES2
NCNAS2
ROLE2*
RNCNA2*
PES2
DTOS2
IAV2*
ISTA*
SELI2
SELI2*
DAT12
DAT22
DAT32
DAT42
DAT52
DAT62
DAT72
DAT82
S4
R59 1K
R5 470
CONTROL DATA
LOGIC DIAGRAM — SYNCHRONOUS CLA I - OUTPUT PROCESSING
34015
D
74873631
A
SHEET 9


8180
REVISION RECORD
SEE SHEET 1
LOOP INTERNAL TEST 2
MODEM CHANGE DETECT 2
RING DETECT 2
CR8 (DCD)
CR7 (RTS)
CR6 (RD)
CR5 (SD)
LITCK
CTS2
DSR2
DCD2
RI2
SCRA2
SCRB2
RDB2
RDA2
SCTA2
SCTB2
SCTE2
TD2
DSR2*
DCD2*
RI2*
RTS2*
DTR2*
LT2*
ISR2*
RSUP12*
ISON2
MODST2*
SCRA2*
RDA2
SCTA2
PG2
SG2
LT2
DTR2
RTS2
SCTEB2
SCTEA2
TDA2
TDB2
+5V
+12V
-12V
CONTROL DATA
COMMUNICATIONS PRODUCTS N.V.
LOGIC DIAGRAM — SYNCHRONOUS CLA 2 DIFFERENTIAL INTERFACE
34015
D
74873631
A
SHEET 10

This section covers troubleshooting, card replacement, card repair, maintenance checks, and preventive maintenance. In order for the SCLA to operate, the system must be operating. Refer to section 2 for system operation.

TROUBLESHOOTING

Troubleshooting is facilitated by the use of an Extender Board, CDC Part No. 74555600. The extender board is oriented so that its female connector is on the left when viewed from the front of the card cage assembly. The extender board is inserted into the card cage assembly in place of the suspected faulty SCLA card. The SCLA is then inserted into the guide rails of the extender board. All points on the SCLA card are thus made readily accessible for troubleshooting.

TEST EQUIPMENT

The following two items of test equipment are recommended for troubleshooting the SCLA circuit cards:

1. Oscilloscope, Tektronix Model 475, or equivalent
2. Volt-Ohm-Milliammeter, Simpson Model 261, or equivalent.

ON-LINE DIAGNOSTICS

On-line diagnostics are used to isolate trouble to the module level. This method is enhanced by the operator, or repair personnel, periodically checking the error counters built into the on-line diagnostic system. This method is preferred since it usually provides successful trouble isolation without creating system downtime.

OFF-LINE DIAGNOSTICS

Off-line diagnostics are used to isolate trouble to module and chip (IC) level. Solid or intermittent errors are found by using this method. In most cases, the solid error is located without difficulty, while the intermittent error may prove more difficult to detect and more exhaustive checks will be required to isolate the error. System downtime is a serious problem when off-line diagnostic methods are used and should be avoided if possible.

PIN CONNECTIONS AND SIGNALS

The following tables serve as troubleshooting aids by facilitating the monitoring of SCLA interface signals. The LM-to-SCLA interface signals with associated pin connections are listed in table 6-1. SCLA DU138-A modem interface signals using three different cables are listed in tables 6-2, 6-3, and 6-4. SCLA DU139-A signals and cable connections are listed in table 6-5, and table 6-6 lists SCLA DU140-A signals and cable connections.

CARD REPLACEMENT

To remove and reinstall SCLA cards in the card cage assembly, proceed as follows:

1. Set both CLA1 and CLA2 enable/disable toggle switches on the card handle to OFF positions.
2. Remove SCLA modem cables.
3. Trip plastic ejectors at top and bottom of SCLA card handle.
4. Grasp card by handle and pull card from card cage.
5. Inspect pins on cage backplane for bent, missing, or damaged pins.
6. Using caution described in Installation paragraph, section 3, insert proven card into cage slot and firmly engage card into connector on cage backplane.
7. Connect SCLA modem cables to connectors on card handle.
8. Set each address switch pair to the proper address setting.
9. Set both CLA1 and CLA2 enable/disable toggle switches on the card handle panel to on (enabled) positions.

NOTE

SCLA cards can be removed from and reinstalled in the card slots while the system is operating.

CARD REPAIR

The repair of the SCLA circuit card includes removing and installing integrated circuits, cutting copper foil conductors to facilitate wiring changes, and adding discrete wires and components.

NOTE

Repair of circuit card on-site is not authorized per maintenance contract. A faulty card should be replaced by a proven spare. However, for emergency card repair, the following information is provided.

Usually, failure analysis is effective only when the defective circuits are received in the condition the card was in when the failure occurred. Therefore, the following general precautions are given to minimize further damage to either the printed circuit board or any component (integrated circuit or discrete components) on the board:

1. Refrain from multiple bending of component leads. A lead may break off after being bent only a few times.

TABLE 6-1. LOOP MULTIPLEXER-TO-SCLA INTERFACE SIGNALS

SCLA Pin No.	Signal	Mnemonic	Function	Signal Destination
18/59†	Input Available SCLA1	IAV1	Notifies LM that SCLA1 has input	LM
19/58†	Input Available SCLA2	IAV2	SCLA2 has input	LM
231	Input Error	IER	Notifies SCLA of error on last input frame	SCLA
232	Input End	IEN	Notifies LM that present information is last	LM
220 thru 222	Input Format Bits 1 thru 3	IF1 thru IF3	Informs LM of address, data, or supervision on information bus	LM
45/88†	Input Select SCLA1	IS1	LM selects SCLA1 input	SCLA
46/87†	Input Select SCLA2	IS2	LM selects SCLA2 input	SCLA
234	Input Strobe	IST	LM notifies SCLA of access	SCLA
223 thru 230	Information Input Bits 1 thru 8	II1 thru II8	Information to LM (data, address, supervision)	LM
283	Output Select Clear	OSC	LM deselects SCLA output	SCLA
282	Output Select	OSL	LM presents SCLA address	SCLA
271 and 272	Output Format Cell Bits 2 and 3	OF2 and OF3	Informs SCLA of address, data, or supervision on information bus	SCLA
285	Output Strobe	OST	LM notifies SCLA of information present	SCLA
273 thru 280	Information Output Bits 1 thru 8	IO1 thru IO8	Information to SCLA (data, supervision, address)	SCLA
281	Output Error	OER	Notifies SCLA of errors in last frame	SCLA
249	Master Clear	MCL	Clears SCLA	SCLA
254	Reference Frequency	RF1	9.6 kHz Clock	SCLA

†Signals are available at two different pins, depending on location of card in card cage.

TABLE 6-2. SCLA DU138-A WITH CABLE XA130-A SIGNALS AND PIN CONNECTIONS

Description	Designation		SCLA Pin No.	Signal Description	Modem Pin No.
	RS-232-C	CCITT V.24			
Protective Ground	AA	101	1†		1†
Transmitted Data	BA	103	2		2
Received Data	BB	104	3		3
Request to Send	CA	105	4		4
Clear to Send	CB	106	5		5
Data Set Ready	CC	107	6		6
Signal Ground	AB	102	7	NA	7
Received Line Signal	CF	109	8		8
F Clock (9.6 kbps)			9		9
F/2 Clock (4.8 kbps)			10		10
F/4 Clock (2.4 kbps)			12		12
M Clock			13		13
Serial Clock Transmit	DB	114	15		15
Serial Clock Receive	DD	115	17		17
Data Terminal Ready	CD	108.2	20		20
Ring Indicator	CE	125	22		22
External Transmit Clock	DA	113	24		24
T Clock (TCLK)			25		25

†Cable shield terminated to connector shell and pin 1 at each end.

TABLE 6-3. SCLA DU138-A WITH CABLE XA129-A SIGNALS AND PIN CONNECTIONS

CLA Connector		Signal Flow	Modem Pin No.
Pin No.	Description		
1†	Protective Ground (AA)	↔	1†
2	Transmitted Data (BA)	→	2
3	Received Data (BB)	←	3
4	Request to Send (CA)	→	4
5	Clear to Send (CB)	←	5
6	Data Set Ready (CC)	←	6
7	Signal Ground (AB)	↔	7
8	Rcvd Line Sig Detector (CF)	←	8
11	Quality Monitor	←	11
14	New Sync	→	14
15	Serial Clock TX (DB)	←	15
17	Serial Clock RX (DD)	←	17
21	Signal Quality Detector (CG)	←	21

†Cable shield terminated to connector shell and pin 1 at each end.

TABLE 6-4. SCLA DU138-A WITH CABLE XA132-A SIGNALS AND PIN CONNECTIONS

CLA Connector		Signal Flow	Modem Pin No.
Pin No.	Description		
1†	Protective Ground (AA)	↔	1†
2	Transmitted Data (BA)	✕	2
3	Received Data (BB)	✕	3
4	Request to Send (CA)	→	8
5	Clear to Send (CB)	←	
6	Data Set Ready (CC)	←	20
7	Signal Ground (AB)	↔	7
8	Rcvd Line Sig Detector (CF)	←	4
9	F Clock (9.6 kbps)	→	5
10	F/2 Clock (4.8 kbps)	←	
12	F/4 Clock (2.4 kbps)	←	
15	Serial Clock TX (DB)	←	15
17	Serial Clock RX (DD)	→	17
20	Data Terminal Ready (CD)	→	6
24	External TX Clock (DA)	←	
25	T Clock	←	

†Cable shield is terminated to connector shell and pin 1 at each end.

2. To avoid damage to the substrate of an integrated circuit chip, do not twist its leads.

3. Heat application periods from a soldering iron must not exceed five seconds. Excessive heat can damage or shorten the life of components and loosens the copper foil from the printed circuit boards.

REMOVAL OF INTEGRATED CIRCUITS

Integrated circuits (ICs) are removed from a card as follows:

1. Heat the solder connections on the back side of the board with a miniature soldering iron. Use a slight rocking motion to help spread the heat. Solder will flow in about two seconds. Immediately withdraw melted solder from the connection with a "solder sucker." Repeat this procedure for all connections.

2. Using a sharp knife, loosen the wire leads on the IC chip from the holes. If some of the leads do not come free of the holes, it may be necessary to remove solder from the front side of the board also. Carefully lift chip from board.

3. Remove excess solder and clean the board with a soft bristle brush and a solvent, preferably trichloroethylene.

INSTALLATION OF INTEGRATED CIRCUITS

Integrated circuits may be installed as follows:

1. Correctly position a new integrated circuit on the board. Using a miniature soldering iron, solder the two end pins of the circuit to the board (typically pins 1 and 8). Make sure solder does not flow above the first bend of the circuit pin.

2. Solder the remaining pins to the board, using a crochet hook to press the pins down while being soldered.

2. Clean the board and inspect all solder joints.

CUTTING COPPER FOIL CONDUCTORS

Copper foil conductors can be cut as follows:

1. With a sharp knife, cut the copper foil in two places approximately 1/32-inch (1 mm) apart.

2. Peel off the copper strip between the two knife cuts. It is not necessary to remove the entire copper strip.

TABLE 6-5. SCLA DU139-A WITH CABLE XA136-A SIGNALS AND PIN CONNECTIONS

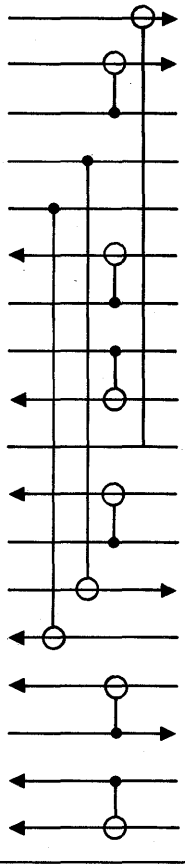
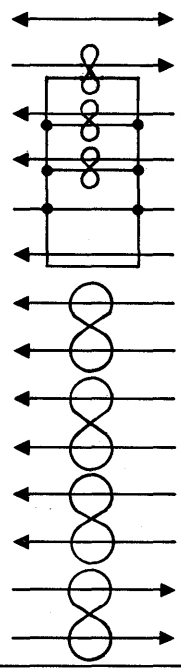
CLA Connector		Signal Flow	Modem Pin No.
Pin No.	Description		
2	Request to Send		D
3	Local Test		G
4	Signal Ground		G'
5	Signal Ground		E'
6	Signal Ground		C'
10	Transmit Clock		J
11	Signal Ground		J'
12	Signal Ground		L'
13	Receive Clock		L
14	Signal Ground		D'
15	Receive Data		K
16	Signal Ground		K'
17	Transmit Data		E
18	Clear to Send		C
19	Carrier Detect		M
20	Data Terminal Ready		M'
22	Ring Indicator		F'
23	Data Set Ready		F

TABLE 6-6. SCLA DU140-A WITH CABLE XA137-A SIGNALS AND PIN CONNECTIONS

CLA Connector		Signal Flow	Modem Pin No.
Pin No.	Description		
1	Protective Ground		A
4	Request to Send		C
5	Clear to Send		D
6	Data Set Ready		E
7	Signal Ground		B
8	Rcvd Line Sig Det		F
9	Serial Clock TX (B)		a
10	Serial Clock TX (A)		Y
12	Serial Clock RX (B)		X
13	Serial Clock RX (A)		V
14	Received Data (B)		T
15	Received Data (A)		P
16	Send Data (B)		R
17	Send Data (A)		S

Note: Signals designated (A) and (B) are balanced pairs, conforming to CCITT Std V.35; all other signals conform to RS-232-C.

ADDING DISCRETE WIRES

A tinned wire may be soldered to the pad on a printed circuit board or to an integrated circuit pin, but not to the very thin copper foil paths. It is not necessary to twist the wire around the pin of the integrated circuit before soldering.

A discrete wire may be soldered to a lifted integrated circuit pin also. This is done only when the integrated circuit lead is disconnected from the pad, bent parallel to the surface of the board and cut off, leaving a 1/8-inch (3 mm) stub. The wire is held against the stub of the pin and soldered. This type of joint must be insulated with a plastic sleeve or equivalent insulator.

REPLACEMENT OF CONNECTOR PINS

The removal and installation of damaged pins in the SCLA modem connectors is facilitated by the use of CDC Field Repair Kit, Part No. 74762000.

MAINTENANCE CHECKS

The LED indicators on the SCLA card handle are lighted when the LM is inputting and outputting to the SCLA. Observing these LEDs can readily indicate modem or system errors to the operator. When the RD indicator is blinking, it indicates that the SCLA is receiving data from the modem; when the SD indicator is blinking, it indicates that the SCLA is sending data to the modem; a lighted RTS indicator shows that request-to-send is active from the SCLA; and a lighted DCD indicator shows that data-carrier-detector signal from the modem is active.

Suspected input power failure to the card may be monitored for +5 vdc at the card.

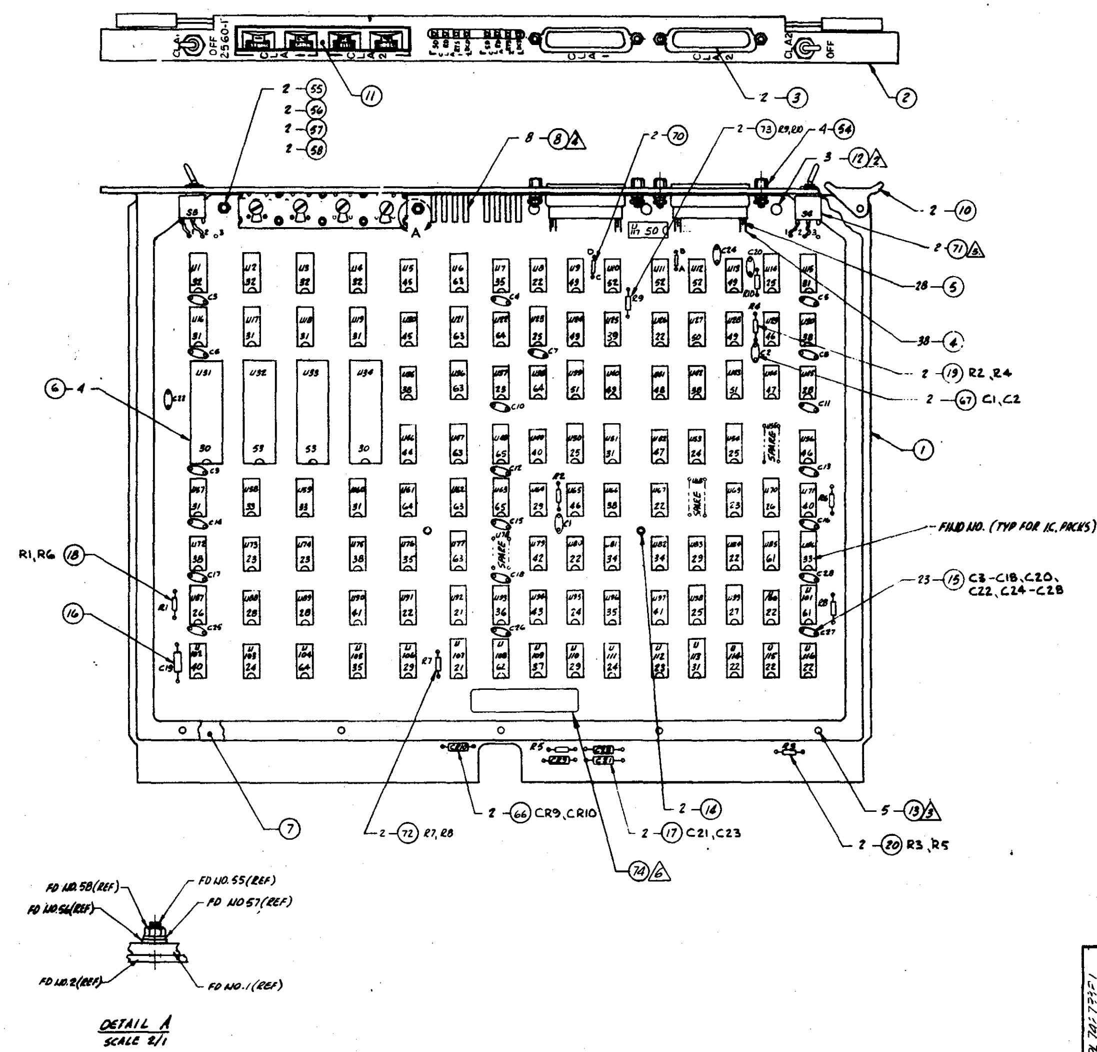
PREVENTIVE MAINTENANCE

Preventive maintenance of the SCLAs is minimal. Excessive handling of cards may induce faults and is thus discouraged. However, the following should be performed at regular intervals:

1. Use spare cards periodically to ensure integrity of the spares.
2. Inspect connectors and cables for fraying or other damage.
3. When a card is removed, inspect connectors at card cage backplane for bent, damaged, or burned pins.

This section contains the parts lists and assembly drawings for the three types of the synchronous communications line adapter and their associated cable assemblies. The lists are provided primarily for reference purposes. Field repair of SCLA cards by parts replacement is neither authorized by any maintenance contract nor is such on-site repair recommended. System repair is to be accomplished via card replacement with the spares provided. However, in the event of multiple card failures, exhausting spares, the parts information is furnished.

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
	00	05243	INITIAL RELEASE	JTP	12-3-74		
	01	05394	ENG RELEASE	JTP	2-11-75		
	02	05573	SEE ECO	JTP	3-20-75		
	03	05658	SEE ECO	JTP	4-24-75		
	04	05771	SEE ECO		6-9-75		
	05	05822	SEE ECO		7-18-75		
	G	06337	SEE ECO		6-11-76		
	H	06406	SEE ECO		6-16-76		
	J	06424	SEE ECO	ELG	7-1-76		
	K	06720	INITIAL RELEASE	PL	3-30-77		
	L	08063	UP DATE FOR CBM	CT	11-29-77		
	M	08106	REVISE PL ONLY	TP	1-5-78		
	N	08181	REVISED PL ONLY	TP	2-23-78		



NOTES:
1. WORKMANSHIP PER CDC-MFG SPEC 10120300.
2. INSERT RIVETS FROM COMPONENT SIDE.
3. INSERT RIVETS FROM NON-COMPONENT SIDE.
4. INDICATOR TO BE SEATED ON BOARD SURFACE DURING SOLDERING.
5. INSTALL FIND NO. 71 SWITCH USING ONE INTERNAL TOOTH LOCK WASHER AND ONE NUT ON OUTSIDE OF HANDLE. APPLY LOCK-TITE (RTN 05044, 95125313) SPARINGLY TO SWITCH THREADS OF CAP TO PREVENT TURNING.
6. TYPE PART NO. 74873381 AND TYPE CODE 5BBY PER CDC SPEC 10121505. LOCATE APPROX AS SHOWN.

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

5BBY

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES	CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704
DO NOT SCALE DRAWING	FIRST USED ON: DU138-A	TITLE: CIRCUIT CARD ASSEMBLY SYNC CLA-RS 232 MODEM
MATERIAL	DR: PARNARIAN 12-3-74	D 34015 DRAWING NUMBER 74873381
FINISH	CHK: 3-13-75	SCALE 1/1 & NOTED 35190-009-104 SHEET 1 OF 1

PL 74873381 DETACHED LISTS

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873381	N	CLA	D	SYNC CLA RS 232 MODEM	UM	2551	11/30/77	02/23/78	1/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
55	A	09006005	200	PC	SCR MACH FLAT PHL H NO. 2	IN			PPP1		N
12	C	09030409	300	PC	RIVET TUBULAR	IN			PPP1		N
13	C	09030419	500	PC	RIVET TUBULAR	IN			PPP1		N
58	A	10125102	200	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP1		N
57	A	10125200	200	PC	OV HD PHL MACH SCR 4-40	IN			PPP1		N
56		10125502	200	PC	WASHER	IN			PPP1		N
48	A	15111400	100	PC	INTEGRATED CIRCUIT 74L51	IN			PPP5		N
28	A	15112300	300	PC	INT CKT 74L00	IN			PPP5		N
38	B	15112700	600	PC	INT CKT 74L04	IN			PPP5		N
42	A	15116000	100	PC	INTEGRATED CIRCUIT 74L02	IN			PPP5		N
62	A	15124200	100	PC	16-PIN DUAL-IN-LINE	IN			PPP4		N
39	C	15134800	100	PC	IC HEX BUFFER 4050	IN			PPP5		N
53	A	15141700	200	PC	IC PT1482B	IN			PPP5		N
30	A	15141800	200	PC	IC PR1472B	IN			PPP5		N
21	A	15142800	200	PC	IC 74251	IN			PPP5		N
23	A	15142900	500	PC	MICROCIRCUIT TYPE 74L10 TTL 3	IN			PPP5		N
43	A	15143000	100	PC	MICROCIRCUIT TYPE 74L20 TTL DU	IN			PPP5		N
47	A	15143100	200	PC	MICROCIRCUIT TYPE 74L30 TTL 8	IN			PPP5		N
33	A	15143500	300	PC	MICROCIRCUIT TYPE 93L00	IN			PPP5		N
26	A	15143700	200	PC	MICROCIRCUIT TYPE 9L24 DL JK F	IN			PPP5		N
24		15156100	400	PC	IC 74L74 J	IN			PPP5		N
27		15163327	100	PC	IC 9321 TTL DUAL DECODER	IN	008181	022278			N
41	A	17182200	200	PC	I.C. SN7420	IN	008181	022278	PPP4		N
32	A	17184000	400	PC	I.C. 4 BIT	IN			PPP5		N
20	C	24500055	200	PC	RES FXD .25# 470 OHMS	IN	0		PPP5		N
72	C	24500063	200	PC	RES FXD .25# 1000 OHMS	IN			PPP5		N
19	C	24500067	200	PC	RES FXD .25# 1500 OHMS	IN			PPP5		N
73	C	24500082	200	PC	RES FXD .25# 6200 OHMS	IN			PPP4		N
18	C	24500139	200	PC	RES FXD COMP. .50# 100 OHM	IN			PPP4		N
66	C	24519100	200	PC	RECTIFIER SILICON 750 MA	IN			PPP4		N
17	C	24521125	200	PC	CAP, FXD METALIZED MYLAR .1 MF	IN	008106	123077	PPP4		N
70	C	24548306	600	IN	WIRE,ELECT,24 GA,PVC,UL,GRN	IN			PPP5		N
52	A	36186400	300	PC	IC CHIP,TYPE 1488	IN			PPP4		N
49	A	36186500	500	PC	IC CHIP,TYPE 1489	IN			PPP4		N
14	A	38607901	200	PC	TERMINAL HOLLOW SINGLE END,105	IN			PPP4		N
47	A	38836955	200	PC	CAP SILVERED MICA 1000PF	IN			PPP4		N

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873381	N	CLA	D	SYNC CLA RS 232 MODEM	UM	2551	11/30/77	02/23/78	2/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
22	B	39389700	1000	PC	INT CKT 7404	IN	008181	022278	PPP5		N
6	A	51856103	400	PC	KT IC PC WIRE WRA	IN			PPP4		N
59	A	52629925	1200	IN	WIRE 26AWG KYNAR GREEN	IN			PPP2		N
3	C	53397814	200	PC	CONN-RECTANGULAR,MALE PLUG	IN			PPP4		N
29	A	66299099	400	PC	MICROCIRCUIT TYPE 7400 (SPEC)	IN	008181	022278	PPP4		N
34	A	66299100	200	PC	MICROCIRCUIT TYPE 7410 (SPEC)	IN	008181	022278	PPP4		N
40	A	66299103	300	PC	INTEGRATED CIRCUIT 7402	IN	008181	022278	PPP4		N
16	A	72003616	100	PC	CAPACITOR 10 VF 15V TANT	IN			PPP4		N
74	C	73954300	100	PC	NAME PLATE IDENTIFICATION SMAL	IN			PYP4		N
2	C	74618502	100	PC	HANDLE SLKSCRND SYNCH CLA	IN			PYE4		N
7	C	74632700	100	PC	INSULTR CRD STIFFENER	IN			PPP4		N
1	D	74685701	100	PC	SYNCH CLA RS232 MODEM FAB.	IN			PYP4		N
50	A	74870522	200	PC	CAP ARRAY 220 PF	IN			PPP4		N
51	A	74870525	200	PC	CAP ARRAY 220 PF	IN			PPP4		N
8	A	74870580	800	PC	INDICATOR LED	IN			PPP4		N
15	A	74870616	2300	PC	CAPACITOR CERAMIC DISC 0.01 U	IN			PPP4		N
5	A	74870625	2800	PC	PIN RT ANGLE CONTACT 2ND ROW	IN			PPP4		N
4	A	74870626	3800	PC	PIN RT ANGLE CONTACT 3RD ROW	IN			PPP4		N
10		74870632	200	PC	RISK EJECTOR	IN			PPP4		N
11	A	74870638	100	PC	SWITCH THUMBWHEEL 4 STATION	IN			PPP4		N
71	A	74872299	200	PC	SWTCH LOCKNG TOGGLE 1 THRU 4 P	IN			PPP4		N
60	D	74873383	FF	PC	SYNC CLA RS 232 MODEM	IN			RFE4		N
45	A	75009943	200	PC	RES PKG 10 0K OHMS	IN			PPP5		N
46	A	77603738	300	PC	IC 74L86N TTL QUAD 2 INPUT OR	IN	008181	022378			N
63	A	88881100	600	PC	IC 74151A TTL DATA SEL MUX	IN	008181	022278	PPP4		N
36	A	88881700	100	PC	IC 8214 TTL DUAL 4/1 MUX	IN	008181	022278			N
31	A	88882800	900	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN	008181	022278			N
65	A	88882900	200	PC	IC 74175 TTL QUAD D F/F W/CLR	IN	008181	022278			N
61	A	88885400	200	PC	IC 9024 TTL DUAL FLIP/FLOP	IN	008181	022278	PPP4		N
25	A	88886400	500	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN	008181	022278	PPP4		N
44	A	88886700	100	PC	IC 7475 TTL 4-BIT BISTAB LATCH	IN	008181	022278	PPP4		N
35	A	88897000	400	PC	IC 7408 TTL QUAD 2-INPUT AND	IN	008181	022278			N
54	C	94268024	400	PC	CONNECTOR LOCKING DEVICE	IN			PPP4		N
37	A	96744154	100	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN	008181	022278			N
64	A	96744156	400	PC	IC 7474 TTL DUAL D EDGE F/F	IN	008181	022278	PPP4		N
					NUMBER OF LINE ITEMS = 71						

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
748/3381	N	CLA	D	SYNC CLA RS 232 MODEM	DM	2551	11/30/77	02/23/78	3/ 3

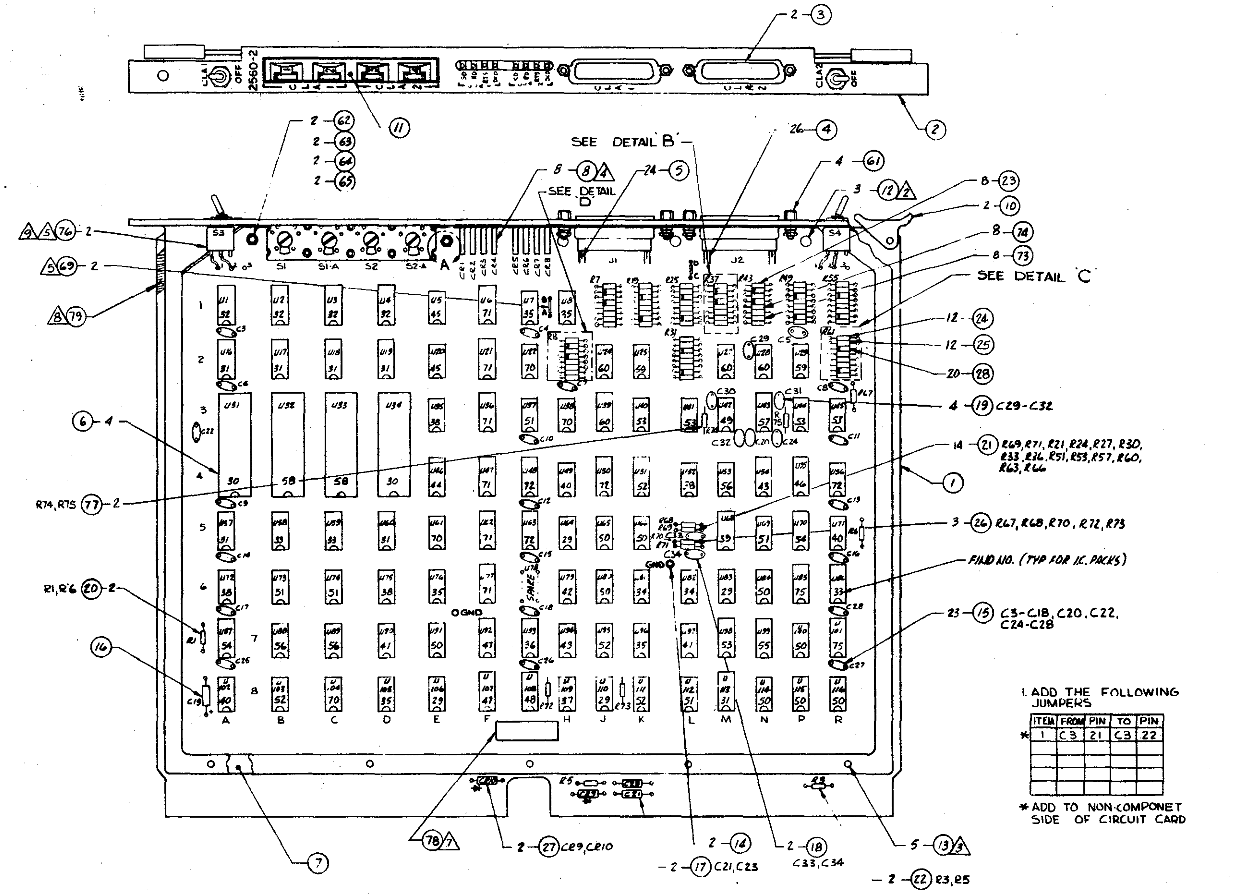
MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
					HIGHEST FINJ NUMBER = 74						
					ARDEN HILLS						

PROJECT ENGINEER

AA 2709 REV. 7-75

REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
00		PRELIMINARY RELEASE	JTP	2-1975		
01		ADD PRODUCT NO.	LA	8-18-75		
02		ADDED S3 & S4 & R72-R75	JTP	4-7-75		
03	06245	INITIAL RELEASE	JTP	3-5-75		
E	06337	SEE ECO	LA	6-1-76		
F	06393	REVISED FIND NO.3 PART NO.	TP	6-7-76		
G	06424	SEE ECO	ELG	9-1-76		
H	06757	INITIAL RELEASE	PL	3-30-77		
J	08063	CLASS A RELEASE CBM	TP	12-12-77	TP	
K	08210	REVISED PARTS LIST	TP	6-20-78	JK	JK

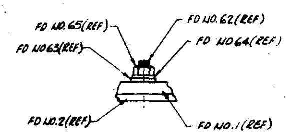


NOTES:
1. WORKMANSHIP PER CDC-MFG SPEC 10120300.
2. INSERT RIVETS FROM COMPONENT SIDE.
3. INSERT RIVETS FROM NON-COMPONENT SIDE.
4. INDICATOR TO BE SEATED ON BOARD SURFACE DURING SOLDERING.
5. WIRE AS SHOWN USING FIND NO. 69.
7. TYPE PART NO. 74873612 AND TYPE CODE 5BBY PER CDC SPEC 10121505. LOCATE APPROX AS SHOWN.
8. APPLY TAPE TO COMPONET SIDE OF CARD APPROX AS SHOWN.
9. INSTALL FIND NO. 76 SWITCH USING ONE INTERNAL TOOTH LOCK WASHER AND ONE NUT ON OUTSIDE OF HANDLE. APPLY LOCK-TITE (RTN 03044, 95125313) SPARINGLY TO SWITCH THREADS OF CAP TO PREVENT TURNING.

1. ADD THE FOLLOWING JUMPERS

ITEM	FROM	PIN	TO	PIN
* 1	C3	21	C3	22

* ADD TO NON-COMPONET SIDE OF CIRCUIT CARD



DETAIL A
SCALE 2/1

	1	2	3
22K	R7	R43	R37
1N914	CR	CR13	CR11
22K	R8	R44	R38
1N914	CR	CR14	CR12
180Ω	R9	R45	R39
2K	R10	R46	R40
2K	R11	R47	R41
180Ω	R12	R48	R42

DETAIL B
SCALE : NONE
3 PLACES

	1	2	3	4	5	6
110Ω	R19	R25	R31	R49	R55	R61
1.2K	R20	R26	R32	R50	R56	R62
1N914	CR25	CR27	CR29	CR15	CR17	CR19
10K	R21	R27	R33	R51	R57	R63
110Ω	R22	R28	R34	R52	R58	R64
1.2K	R23	R29	R35	R53	R59	R65
1N914	CR26	CR28	CR30	CR16	CR18	CR20
10KΩ	R24	R30	R36	R53	R60	R66

DETAIL C
SCALE : NONE
6 PLACES

	1
22K	R13
1N914	CR23
22K	R14
1N914	CR24
180Ω	R16
2K	R15
2K	R18
180Ω	R17

DETAIL D
SCALE : NONE
1 PLACE

5BBY

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.034. CA

AA6030

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES&MILLIMETERS TOLERANCES
3 PLACE ±.015 | 2 PLACE ±.03 | ANGLES ±2°
DO NOT SCALE DRAWING
MATERIAL
FINISH
DETACHED LISTS

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

FIRST USED ON: DU139-A
DR: T. PARUALIAN 3-4-76
CHK:
ENGR: 3-4-76
MFG:
APPD:

TITLE: CIRCUIT CARD ASSEMBLY SYNC CLA- COAXIAL

D | CODE IDENT NO 34015 | DRAWING NUMBER 74873612

SCALE 1/1 & NOTED | 35410-009-104 | SHEET 1 OF 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873612	K	CLA	D	SYNC CLA COAXIAL	DM	2551	12/19/77	06/20/78	1/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
62	A	09006005	200	PC	SCR MACH FLAT PHL H NO. 2	IN			PPP1		N
12	C	09030409	300	PC	RIVET TUBULAR	IN			PPP1		N
13	C	09030419	500	PC	RIVET TUBULAR	IN			PPP1		N
65	A	10125102	200	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP1		N
64	A	10125200	200	PC	OV HD PHL MACH SCR 4-40	IN			PPP1		N
63		10125502	200	PC	WASHER	IN			PPP1		N
37	A	15104200	100	PC	IC QUAD 2IN NAND GATE 7403	OUT	008210	062078	PPP4		N
31	A	15104400	700	PC	TTL HEX STOR REG D-TYPE 74174	OUT	008210	062078	PPP5		N
72	A	15104500	400	PC	ACCEPT TEST TYPE 74175	OUT	008210	062078	PPP5		N
70	A	15104800	400	PC	IC SPEC DUAL D TYPE FF 7474	OUT	008210	062078	PPP5		N
56	A	15112300	300	PC	INT CKT 74L00	IN			PPP5		N
38	B	15112700	400	PC	INT CKT 74L04	IN			PPP5		N
55	A	15115300	100	PC	INTEGRATED CIRCUIT 9321	OUT	008210	062078	PPP5		N
42	A	15116000	100	PC	INTEGRATED CIRCUIT 74L02	IN			PPP5		N
48	A	15124200	100	PC	16-PIN DUAL-IN-LINE	IN			PPP4		N
59	C	15124800	200	PC	IC SN7414	OUT	008210	062078	PPP4		N
36	A	15131300	100	PC	IC 8214 TTL 2 4I*1A MUX 542	OUT	008210	062078	PPP5		N
39	C	15134800	100	PC	IC HEX BUFFER 4050	IN			PPP5		N
58	A	15141700	200	PC	IC PT1482B	IN			PPP5		N
30	A	15141800	200	PC	IC PR1472B	IN			PPP5		N
47	A	15142800	200	PC	IC 74251	IN			PPP5		N
51	A	15142900	500	PC	MICROCIRCUIT TYPE 74L10 TTL 3	IN			PPP5		N
43	A	15143000	200	PC	MICROCIRCUIT TYPE 74L20 TTL DU	IN			PPP5		N
46	A	15143300	100	PC	MICROCIRCUIT TYPE 74L86 TTL QU	OUT	008210	062078	PPP5		N
33	A	15143500	300	PC	MICROCIRCUIT TYPE 93L00	IN			PPP5		N
54	A	15143700	200	PC	MICROCIRCUIT TYPE 9124 DL JK F	IN			PPP5		N
52		15156100	400	PC	IC 74L74 J	IN			PPP5		N
49	C	15163326	100	PC	IC 1489A RECEIVER RS232C DTL	IN	008210	062078	PPP5		N
55	C	15163327	100	PC	IC 9321 TTL DUAL DECODER	IN	008210	062078	PPP5		N
41	A	17162200	200	PC	I.C. SN7420	IN	008210	062078	PPP4		N
32	A	17184000	400	PC	I.C. 4 BIT	IN			PPP5		N
24	C	24500040	1200	PC	RES FXD .25W 110 OHMS	IN			PPP4		N
74	C	24500045	800	PC	RES FXD .25W 180 OHMS	IN			PPP5		N
22	C	24500055	200	PC	RES FXD .25W 470 OHMS	IN			PPP5		N
26	C	24500063	500	PC	RES FXD .25W 1000 OHMS	IN			PPP5		N
25	C	24500065	1200	PC	RES FXD .25W 1200 OHMS	IN			PPP5		N

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873612	K	CLA	D	SYNC CLA COAXIAL	DM	2551	12/19/77	06/20/78	2/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
73	C	24500070	800	PC	RES FXD .25W 2000 OHMS	IN			PPP5		N
77	C	24500082	200	PC	RES FXD .25W 6200 OHMS	IN			PPP5		N
21	C	24500087	1400	PC	RES FXD .25W 10000 OHMS	IN			PPP5		N
23	C	24500095	800	PC	RES FXD .25W 22000 OHMS	IN			PPP5		N
20	C	24500139	200	PC	RES FXD COMP. .50W 100 OHM	IN			PPP4		N
27	C	24519100	200	PC	RECTIFIER SILICON 750 MA	IN			PPP5		N
17	C	24521125	200	PC	CAP, FXD METALIZED MYLAR .1 MF	IN			PPP5		N
69	C	24548306	400	IN	WIRE,ELECT,24 GA,PVC,UL,GRN	IN			PPP5		N
28	A	25175800	2000	PC	DIODE(1N914)	IN			PPP4		N
57	A	36186400	100	PC	IC CHIP,TYPE 1488	IN			PPP5		N
49	A	36186500	100	PC	IC CHIP,TYPE 1489	OUT	008210	062078	PPP5		N
29	A	36186800	400	PC	INT CKT 7400 TTL QUAD 2 INPUT	OUT	008210	062078	PPP5		N
40	A	36187000	300	PC	INT CKT 7402 TTL QUAD 2 INPUT	OUT	008210	062078	PPP5		N
50	A	36187100	900	PC	INT CKT 7404 TTL HEX INVERTER	OUT	008210	062078	PPP5		N
41	A	36187300	200	PC	INT CKT 7420 TTL DUAL 4 INPUT	OUT	008210	062078	PPP4		N
44	A	36188000	100	PC	INTEGRATED CIRCUIT	OUT	008210	062078	PPP5		N
14	A	38807901	200	PC	TERMINAL HOLLOW SINGLE END.105	IN			PPP5		N
18	A	38836926	200	PC	CAPACITOR,SILVERED MICA 100 PF	IN			PPP4		N
19	A	38836935	400	PC	CAP, SILVERED MICA 240PF	IN			PPP4		N
50	B	39389700	900	PC	INT CKT 7404	IN	008210	062078	PPP5		N
34	A	50250700	200	PC	IC TTL TRPL 3 INPUT NAND 9003	OUT	008210	062078	PPP4		N
60	A	51768200	400	PC	I.C. TTL DUAL LINE TRANSMITTER	IN			PPP4		N
53	A	51784000	500	PC	I.C. 74157	OUT	008210	062078	PPP5		N
75	A	51786700	200	PC	INT CKT 9024	OUT	008210	062078	PPP5		N
35	A	51801200	500	PC	IC GATE QUAD 2-INPUT AND	OUT	008210	062078	PPP4		N
71	A	52342400	600	PC	I.C.DATA SELECT,MULTIPLX 74151	OUT	008210	062078	PPP5		N
3	C	53397814	200	PC	CONN-RECTANGULAR,MALE PLUG	IN			PPP5		N
29	A	66299099	400	PC	MICROCIRCUIT TYPE 7400 (SPEC)	IN	008210	062078	PPP5		N
34	A	66299100	200	PC	MICROCIRCUIT TYPE 7410 (SPEC)	IN	008210	062078	PPP4		N
40	A	66299103	300	PC	INTEGRATED CIRCUIT 7402	IN	008210	062078	PPP4		N
16	A	72003616	100	PC	CAPACITOR 10 VF 15V TANT	IN			PPP5		N
78	C	73954300	100	PC	NAME PLATE IDENTIFICATION SMAL	IN			PYP4		N
1	D	74567200	100	PC	SYNCH CLA COAXIAL	IN			PYP4		N
7	C	74632700	100	PC	INSULTR CRD STIFFENER	IN			PPP5		N
2	C	74759500	100	PC	HANDL SLKSCRND SYNC CLA COAXIA	IN			PYE4		N
8	A	74870580	800	PC	INDICATOR LED	IN			PPP5		N

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV.	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873612	K	CLA	D	SYNC CLA COAXIAL	DM	2551	12/19/77	06/20/78	3/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
15	A	74870616	2300	PC	CAPACITOR CERAMIC DISC 0 01 U	IN			PPP5		N
5	A	74870629	2400	PC	SOCKET RT ANGLE 2ND ROW	IN			PPP4		N
4	A	74870630	2600	PC	SOCKET RT ANGLE 3RD ROW	IN			PPP4		N
10		74870632	200	PC	RISK EJECTOR	IN			PPP5		N
11	A	74870638	100	PC	SWITCH THUMBWHEEL 4 STATION	IN			PPP5		N
76	A	74872299	200	PC	SWTCH LOCKNG TOGGLE 1 THRU 4 P	IN			PPP5		N
66	D	74873613	REF	PC	SYNC CLA COAXIAL LOGIC	IN			RFE4		N
45	A	75009943	200	PC	RES PKG 10 0K OHMS	IN			PPP5		N
46	A	7760373A	100	PC	IC 74L86N TTL QUAD 2 INPUT OR	IN	008210	06[illegible]78	PPP4		N
71	A	88881100	600	PC	IC 74151A TTL DATA SEL MUX	IN	008210	06[illegible]78	PPP5		N
36	A	88881700	100	PC	IC 8214 TTL DUAL 4/1 MUX	IN	008210	06[illegible]78	PPP5		N
31	A	88882800	700	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN	008210	06[illegible]78	PPP5		N
72	A	88882900	400	PC	IC 74175 TTL QUAD D F/F W/CLR	IN	008210	06[illegible]78	PPP5		N
75	A	88885400	200	PC	IC 9024 TTL DUAL FLIP/FLOP	IN	008210	06[illegible]78	PPP5		N
53	A	88886400	500	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN	008210	06[illegible]78	PPP5		N
44	A	88886700	100	PC	IC 7475 TTL 4-BIT BISTAB LATCH	IN	008210	06[illegible]78	PPP4		N
35	A	88889700	500	PC	CASSETTE DATA (095-0011036	IN	008210	06[illegible]78	PPP4		N
59	A	88896100	200	PC	IC 7414 TTL HEX SCHMITT TRIGER	IN	008210	06[illegible]78	PPP4		N
6	A	94202104	400	PC	SOCKET 3 PIN	IN			PPP4		N
61	C	94288024	400	PC	CONNECTOR LOCKING DEVICE	IN			PPP5		N
79		94897202	600	IN	RISK TAPE TEFLON 1 IN WIDE	IN			PPP4		N
37	A	96744154	100	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN	008210	06[illegible]78	PPP5		N
70	A	96744156	400	PC	IC 7474 TTL DUAL D EDGE F/F	IN	008210	06[illegible]78	PPP4		N

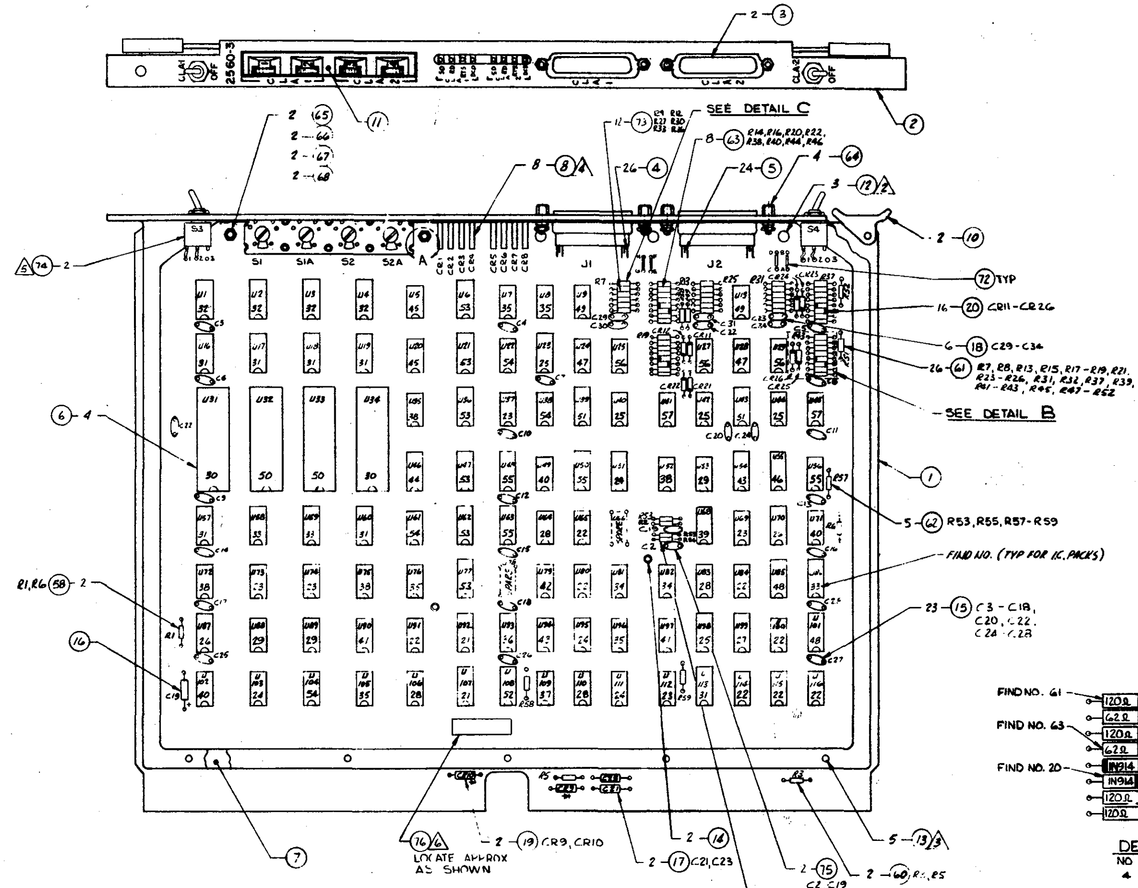
NUMBER OF LINE ITEMS = 95
HIGHEST FIND NUMBER = 79

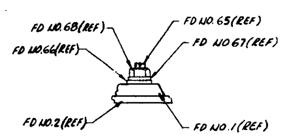
PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

SHEET REVISION STATUS	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
	00		PRELIMINARY RELEASE	JTP	2-19-75		
	01		REV CORP DWG NO.	JTP	2-26-75		
	02		REV. PARTS LIST	JTP	3-13-75		
	03		ADD PRODUCT NO.	LA	3-18-75		
	04		ADDED S3,S4,R58,R59,CR11-CR26	JTP	4-30-75		
	05		P L CHANGE ONLY	JTP	5-2-75		
	06		REV FIND NO.S 20,17,73, ADDED FIND NO. 75	JTP	8-18-75		
	07	06124	INITIAL RELEASE	TP	12-16-75	[illegible]	[illegible]
	J	06337	SEE ECO	LA	6-11-76	[illegible]	[illegible]
	K	06424	SEE ECO	ELG	9-1-76	[illegible]	[illegible]
	L	06758	INITIAL RELEASE	PL	3-30-77	RAR	RAR
	M	08063	CLASS A RELEASE CBM	TP	12-12-77	TP	TP
	N	08210	REVISE PARTS LIST	TP	6-20-78	VR	VR





DETAIL A
SCALE 2/1

FIND NO. 61

	1	2	3
120Ω	R7	R25	R31
120Ω	R8	R26	R32
51Ω	R9	R27	R33
51Ω	R10	R28	R34
51Ω	R11	R29	R35
51Ω	R12	R30	R36

FIND NO 73

DETAIL C
SCALE: NONE
3 PLACES

		1.	2.	3.	4.
FIND NO. 61	120Ω	R13	R19	R37	R43
FIND NO. 63	62Ω	R14	R20	R38	R44
	120Ω	R15	R21	R39	R45
	62Ω	R16	R22	R40	R46
FIND NO. 20	IN914	CR19	CR13	CR15	CR17
	IN914	CR20	CR14	CR16	CR18
	120Ω	R17	R23	R41	R47
	120Ω	R18	R24	R42	R48

DETAIL B
NO SCALE
4 PLACES

NOTES:
1. WORKMANSHIP PER CDC-MFG SPEC 10120300.
2. INSERT RIVETS FROM COMPONENT SIDE.
3. INSERT RIVETS FROM NON-COMPONENT SIDE.
4. INDICATOR TO BE SEATED ON BOARD SURFACE DURING SOLDERING.
5. INSTALL SWITCH (FIND NO. 74) USING ONE INTERNAL TOOTH LOCK WASHER AND ONE NUT ON OUTSIDE OF HANDLE. APPLY LOCK-TITE (RTN 03044, 95125313) SPARINGLY TO THREADS OF CAP TO PREVENT TURNING
6. TYPE PART NO. 74873630 AND TYPE CODE 5BBY PER CIC SPEC 10121505. LOCATE APPROX AS SHOWN.

5BBY

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.034.
CA
AA6030

UNLESS OTHERWISE SPECIFIED DIM ARE IN INCHES MILLIMETERS
TOLERANCE
2 PLACE ±.015 ±0.38mm | 2 PLACE ±.03 ±0.8mm | ANGLES ±2°
DO NOT SCALE DRAWING
MATERIAL
FINISH
DETACHED LISTS

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif 92704

FIRST USED ON: DU140-A
DR: [illegible]
CHK: [illegible] 12-17-75
ENGR: CRAWFORD 12-16-75
MFG:
APPD:

TITLE: CIRCUIT CARD ASSEMBLY SYNC CLA- DIFFERENTIAL

SIZE: D | CODE IDENT NO: 34015 | DRAWING NUMBER: 74873630

SCALE: 1/1 & NOTED | [illegible]-009-104 | SHEET 1 OF 1

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873630	N	CLA	D	SYNC CLA DIFFERENTL	DM	2551	12/14/77	06/21/78	1/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
45	A	09006005	200	PC	SCR MACH FLAT PHL H NO. 2	IN			PPP1		N
12	C	09030409	300	PC	RIVET TUBULAR	IN			PPP1		N
13	C	09030419	500	PC	RIVET TUBULAR	IN			PPP1		N
68	A	10125102	200	PC	HEXAGON MACHINE SCREW NUTS	IN			PPP1		N
67	A	10125200	200	PC	OV HD PHL MACH SCR 4-40	IN			PPP1		N
66		10125502	200	PC	WASHER	IN			PPP1		N
37	A	15104200	100	PC	IC QUAD 2IN NAND GATE 7403	OUT	008210	062078	PPP4		N
31	A	15104400	700	PC	TTL HEX STOR REG D-TYPE 74174	OUT	008210	062078	PPP5		N
55	A	15104500	400	PC	ACCEPT TEST TYPE 74175	OUT	008210	062078	PPP5		N
54	A	15104800	400	PC	IC SPEC DUAL D TYPE FF 7474	OUT	008210	062078	PPP5		N
29	A	15112300	300	PC	INT CKT 74L00	IN			PPP5		N
38	B	15112700	400	PC	INT CKT 74L04	IN			PPP5		N
27	A	15115300	100	PC	INTEGRATED CIRCUIT 9321	OUT	008210	062078	PPP5		N
42	A	15116000	100	PC	INTEGRATED CIRCUIT 74L02	IN			PPP5		N
52	A	15124200	100	PC	16-PIN DUAL-IN-LINE	IN			PPP4		N
36	A	15131300	100	PC	IC A214 TTL 2 4I*1A MUX 542	OUT	008210	062078	PPP5		N
39	C	15134800	100	PC	IC HEX BUFFER 4050	IN			PPP5		N
50	A	15141700	200	PC	IC PT14828	IN			PPP5		N
30	A	15141800	200	PC	IC PR1472B	IN			PPP5		N
21	A	15142800	200	PC	IC 74251	IN			PPP5		N
23	A	15142900	500	PC	MICROCIRCUIT TYPE 74L10 TTL 3	IN			PPP5		N
43	A	15143000	200	PC	MICROCIRCUIT TYPE 74L20 TTL DU	IN			PPP5		N
46	A	15143300	100	PC	MICROCIRCUIT TYPE 74L86 TTL QU	OUT	008210	062078	PPP5		N
33	A	15143500	300	PC	MICROCIRCUIT TYPE 93L00	IN			PPP5		N
26	A	15143700	200	PC	MICROCIRCUIT TYPE 9L24 DL JK F	IN			PPP5		N
24		15156100	400	PC	IC 74L74 J	IN			PPP5		N
49	C	15163326	200	PC	IC 1489A RECEIVER RS232C DTL	IN	008210	062078	PPP5		N
27	C	15163327	100	PC	IC 9321 TTL DUAL DECODER	IN	008210	062078	PPP5		N
41	A	17182200	200	PC	I.C. SN7420	IN	008210	062078	PPP4		N
32	A	17184000	400	PC	I.C. 4 BIT	IN			PPP5		N
73	C	24500032	1200	PC	RES FXD .25W 51 OHMS	IN			PPP5		N
63	C	24500034	800	PC	RES FXD .25W 62 OHMS	IN			PPP4		N
61	C	24500041	2600	PC	RES FXD .25W 120 OHMS	IN			PPP5		N
60	C	24500055	200	PC	RES FXD .25W 470 OHMS	IN			PPP5		N
62	C	24500063	500	PC	RES FXD .25W 1000 OHMS	IN			PPP5		N
59	C	24500087	200	PC	RES FXD .25W 10000 OHMS	IN			PPP5		N

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873630	N	CLA	D	SYNC CLA DIFFERENTL	DM	2551	12/14/77	06/21/78	2/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
58	C	24500139	200	PC	RES FXD COMP. .50W 100 OHM	IN			PPP4		N
19	C	24519100	200	PC	RECTIFIER SILICON 750 MA	IN			PPP5		N
17	C	24521125	200	PC	CAP, FXD METALIZED MYLAR .1 MF	IN			PPP5		N
72	C	24548306	600	IN	WIRE,ELECT,24 GA,PVC,UL,GRN	IN			PPP5		N
20	A	25175800	1600	PC	DIODE(1N914)	IN			PPP4		N
51	A	36186400	200	PC	IC CHIP,TYPE 1488	IN			PPP5		N
49	A	36186500	200	PC	IC CHIP,TYPE 1489	OUT	008210	062078	PPP5		N
28	A	36186800	400	PC	INT CKT 7400 TTL QUAD 2 INPUT	OUT	008210	062078	PPP5		N
40	A	36187000	300	PC	INT CKT 7402 TTL QUAD 2 INPUT	OUT	008210	062078	PPP5		N
22	A	36187100	800	PC	INT CKT 7404 TTL HEX INVERTER	OUT	008210	062078	PPP5		N
34		36187201	200	PC	IC-7410 TRIPLE 3 INPUT NAND	OUT	008210	062078	PPP4		N
41	A	36187300	200	PC	INT CKT 7420 TTL DUAL 4 INPUT	OUT	008210	062078	PPP4		N
44	A	36188000	100	PC	INTEGRATED CIRCUIT	OUT	008210	062078	PPP5		N
14	A	38807901	200	PC	TERMINAL HOLLOW SINGLE END,105	IN			PPP5		N
18	A	38836917	600	PC	CAP, SILVERED MICA 47PF	IN			PPP4		N
75	A	38836926	200	PC	CAPACITOR,SILVERED MICA 100 PF	IN			PPP4		N
22	A	39389700	800	PC	INT CKT 7404	IN	008210	062078	PPP5		N
25	A	51784000	500	PC	I.C. 74157	OUT	008210	062078	PPP5		N
35	A	51801200	500	PC	IC GATE QUAD 2-INPUT AND	OUT	008210	062078	PPP4		N
57	A	51802700	200	PC	IC DRIVER,DTL/TTL DUAL DIFF	IN			PPP4		N
56	A	51802800	300	PC	IC-9615 DUAL DIFF LINE RECEIVR	IN			PPP4		N
53	A	52342400	600	PC	I.C.DATA SELECT,MULTIPLX 74151	OUT	008210	062078	PPP5		N
3	C	53347814	200	PC	CONN-RECTANGULAR,MALE PLUG	IN			PPP5		N
28	A	66299099	400	PC	MICROCIRCUIT TYPE 7400 (SPEC)	IN	008210	062078	PPP5		N
34	A	66299100	200	PC	MICROCIRCUIT TYPE 7410 (SPEC)	IN	008210	062078	PPP4		N
40	A	66299103	300	PC	INTEGRATED CIRCUIT 7402	IN	008210	062078	PPP4		N
16	A	72003616	100	PC	CAPACITOR 10 VF 15V TANT	IN			PPP5		N
76	C	73954300	100	PC	NAME PLATE IDENTIFICATION SMAL	IN			PYP4		N
1	D	74568100	100	PC	CC FAB SYNC CLA DIFF	IN			PYP4		N
7	C	74632700	100	PC	INSULTN CRD STIFFENER	IN			PPP5		N
2	C	74749600	100	PC	HANDLE SILKSCREEN SYNC CLA DI	IN			PPP4		N
47	A	74870522	200	PC	CAP ARRAY 220 PF	IN			PPP4		N
8	A	74870580	800	PC	INDICATOR LED	IN			PPP5		N
15	A	74870615	2300	PC	CAPACITOR CERAMIC DISC 0.01 U	IN			PPP5		N
5	A	74870629	2400	PC	SOCKET RT ANGLE 2ND ROW	IN			PPP4		N
4	A	74870630	2600	PC	SOCKET RT ANGLE 3RD ROW	IN			PPP4		N

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74873630	N	CLA	D	SYNC CLA DIFFERENTL	DM	2551	12/14/77	06/21/78	3/ 3

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	RN NC	S OR N
10		74870632	200	PC	RISK EJECTOR	IN			PPP5		N
11	A	74870638	100	PC	SWITCH THUMBWHEEL 4 STATION	IN			PPP5		N
74	A	74872299	200	PC	SWTCH LOCKNG TOGGLE 1 THRU 4 P	IN			PPP5		N
69	D	74873631	DEF	PC	SYNC CLA DIFFERENTL LOGIC	IN			RFE4		N
45	A	75009943	200	PC	RES PKG 10 OK OHMS	IN			PPP5		N
46	A	77603738	100	PC	IC 74L86N TTL QUAD 2 INPUT OR	IN	008210	062078	PPP4		N
53	A	88881100	600	PC	IC 74151A TTL DATA SEL MUX	IN	008210	062078	PPP5		N
36	A	88881700	100	PC	IC 8214 TTL DUAL 4/1 MUX	IN	008210	062078	PPP5		N
31	A	88882800	700	PC	IC 74174 TTL HEX D F/F W/CLEAR	IN	008210	062078	PPP5		N
55	A	88882900	400	PC	IC 74175 TTL QUAD D F/F W/CLR	IN	008210	062078	PPP5		N
48	A	88885400	200	PC	IC 9024 TTL DUAL FLIP/FLOP	IN			PPP5		N
25	A	88886400	500	PC	IC 74157 TTL QUAD 2-INPUT MUX	IN	008210	062078	PPP5		N
44	A	88886700	100	PC	IC 7475 TTL 4-BIT BISTAB LATCH	IN	008210	062078	PPP4		N
35	A	88897000	500	PC	IC 7408 TTL QUAD 2-INPUT AND	IN	008210	062078	PPP5		N
6	A	94202104	400	PC	SOCKET 3 PIN	IN			PPP4		N
64	C	94288024	400	PC	CONNECTOR LOCKING DEVICE	IN			PPP5		N
37	A	96744154	100	PC	IC 7403 TTL QUAD 2-IN POS NAND	IN	008210	062078	PPP5		N
54	A	96744156	400	PC	IC 7474 TTL DUAL D EDGE F/F	IN	008210	062078	PPP4		N

NUMBER OF LINE ITEMS = 90
HIGHEST FIND NUMBER = 76

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

DWN	L. ANDERSON	5/3/76	CONTROL DATA	TITLE	CABLE ASSY - SYNC RS232 TO 203A	PREFIX	DOCUMENT NO.	REV
CHKD		5-11-76					74658500	E
ENG		5-17-76	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704					
MFG								
APPR			CODE IDENT 34015	FIRST USED ON XA131-A	31774-009-070		SHEET 1 OF 4	

SHEET REVISION STATUS

4	3	2	1
-	B	B	B
-	B	C	C
D	B	D	D
D	B	D	E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
B	06367	SEE ECO	LA	5.13.76	
C	06707	CLIP CONN. CONTACT CHG	PDM	1-11-77	
D	08139	FIND NO.4 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
E	08063	CLASS A RELEASE CBM	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA
AAL030

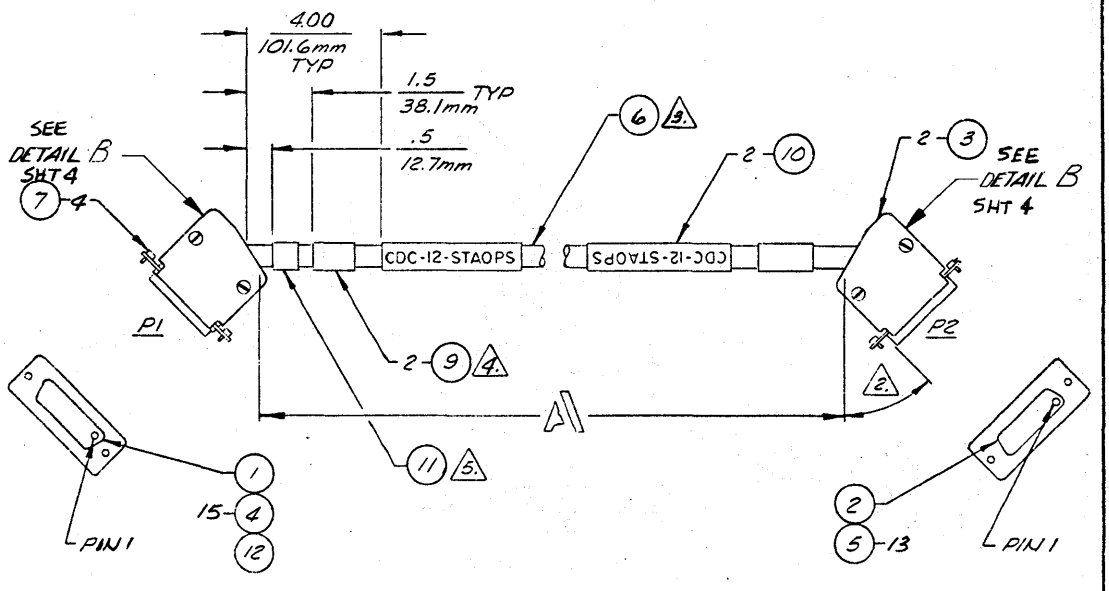
NOTES:

DN 74658500
WL 74658600 | PL 74658500
ASSOC. LISTS | DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

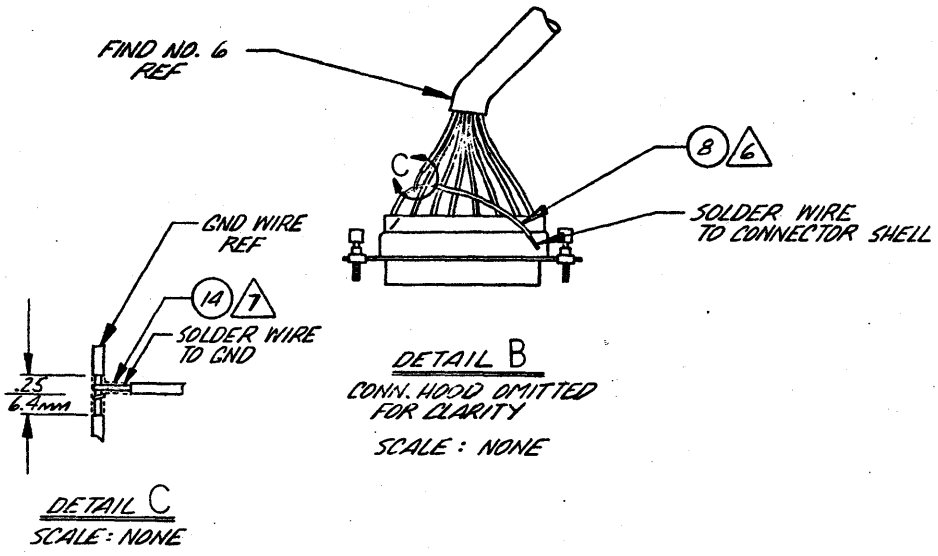
31774-009-070

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	DOCUMENT NO. 74658500	REV. D



FORM 19245-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CDC Nº	A LENGTH		RTN Nº
	FEET ±0.5 FT	METERS ±.15 METERS	
74658500	50.0	15.24	31774



DETAIL B
CONN. HOOD OMITTED FOR CLARITY
SCALE: NONE

DETAIL C
SCALE: NONE

DRWN	L. ANDERSON	5-13-76	CONTROL DATA	TITLE	CABLE ASSY - SYNC RS232 TO 203A	PREFIX	DOCUMENT NO.	REV
CHKD	D.P.	5-17-76				DN	74658500	D
ENG	R.A. Crawford	6-13-76	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704					
MFG								
APPR			CODE IDENT 34015	FIRST USED ON XA151-A	31774-009-070		SHEET 1 OF 2	

SHEET REVISION STATUS

2	1
B	B
B	C
D	D

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
B	06367	SEE ECO	LA	5-17-76	JM
C	06707	CLIP CONN. CONTACT CHG	DPM	1-11-77	RCW
D	08139	FIND NO.4 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	RCW

NOTES:

DETACHED LISTS

FORM 19246-01-015-082 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31774-009-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO. 74658500	REV. D

NOTES:

1. WORKMANSHIP PER CDC SPEC 10120300
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR PIN 1.
4. MARK FIND NO. 3 PER CDC SPEC 10121508 WITH PART NO. 74658500, CONNECTOR NO. P1 OR P2, AND SERIAL NUMBER.
5. P1 END OF CABLE TO BE COLOR IDENTIFIED YELLOW WITH FIND NO. 11.
6. STRIP BACK INSULATION AT BOTH ENDS OF WIRE .25(6.4mm).
7. SLEEVE ALL BARE WIRE USING ITEM FIND NO. 14.

FORM 19245-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74658500	E	CLA		CABLE ASSY SYNCRS232-203A	DM	2551	01/29/78	02/01/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
12	A	15003409	1200	IN	WIRE ELECT,20 GA,PVC UL 1061	IN			PPP2		N
14	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
8	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN	008063	020278	PPP5		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN					N
10		51904701	200	PC	CABLE LABLE	IN					N
1	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
4	A	62013606	1500	PC	SOCKET	IN					N
2	A	62013702	100	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
5	A	62013801	1300	PC	CONTACT PIN	IN			PPP4		N
9	B	73995400	200	PC	NMPLT KIT BLNK SMALL CABLES	IN			PPP4		N
13		74658600	REF	PC	WIRE LIST SYNC RS232 TO 203A	IN					N
6	A	74871633	60000	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
11	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	008500		PPP4		N
7	A	74873611	400	PC	RETAINER MALE SCREW	IN			PPP4		N

NUMBER OF LINE ITEMS = 14
HIGHEST FIND NUMBER = 14

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-78

DWN	LEVENTHAL	11-4-74	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD			COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	CABLE ASSY SYNCHRONOUS RS232 TO 201/208B MODEM		74658700/101	A
ENG		11-5-74					
MFG			CODE IDENT 34015	FIRST USED ON 31775-009-070 32466		SHEET 1 OF 4	
APPR							

SHEET REVISION STATUS

4	3	2	1
–	00	00	00
–	00	01	01
–	00	01	02
–	03	01	03
–	03	04	04
05	03	05	05
A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	–	INITIAL RELEASE	ML	11-5-74	
01	–	REV PI FD NO.	LA	1-3-75	
02	05360	CL "B" PREPRELEASED	DPM	1-10-75	
03	05514	SEE ECO, ADDED 01 TAB	DPM	2-25-75	
04	06707	CLIP CONN. CONTACT CHG	DPM	1-11-77	
05	08139	FIND NO. 5 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
A	08063	CLASS "A" RELEASE CBM	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

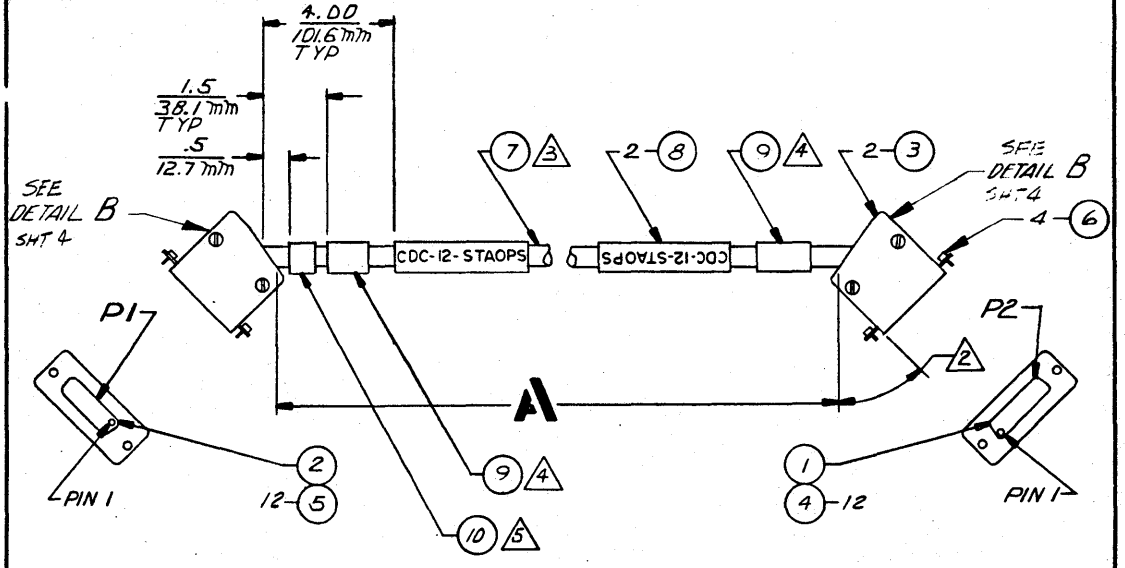
NOTES:

DN 74658700
PL 74658700
DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31775-009-070
32466

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	DOCUMENT NO. 74658700	REV. A



FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31775-009-070
32466

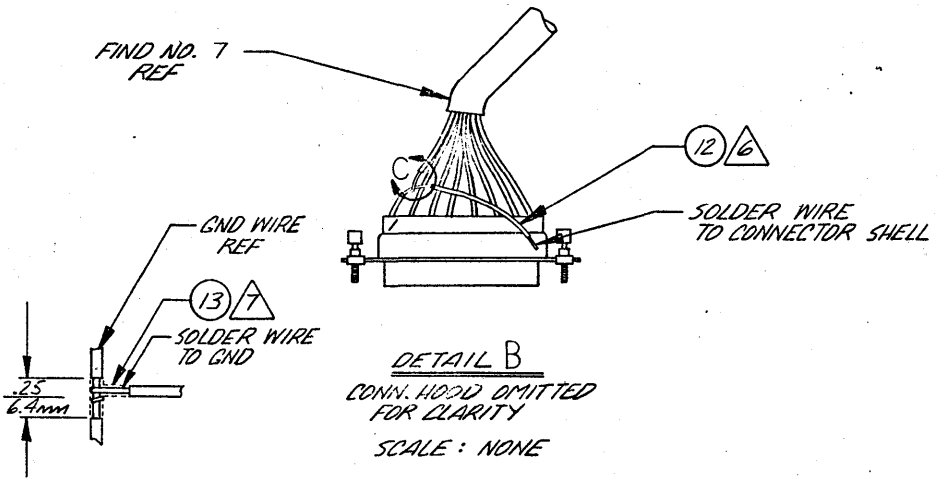
CONTROL DATA	MBM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	DOCUMENT NO. 74658700	REV. A

CDC NO.	LENGTH		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74658700	50.0	15.24	31775
74658701	100.0	30.48	32466

FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31775/32466 -009-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	DOCUMENT NO. 74658700	REV. A



DETAIL B
CONN. HOOD OMITTED FOR CLARITY
SCALE: NONE

DETAIL C
SCALE: NONE

FORM 19245-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	CENTRAL	11-4	CONTROL DATA CORPORATION PRODUCTS DIV. Santa Ana, Ca. 92704	TITLE CABLE ASSY SYNCHRONOUS RS232 TO 201/208B MODEM	PREFIX DN	DOCUMENT NO. 74658700	REV A
CHKD							
ENG	[illegible]	11-5-74					
MFG			CODE IDENT 34015	FIRST USED ON 31775-009-070 32466		SHEET 1 OF 2	
APPR							

SHEET REVISION STATUS

2	1
00	00
01	01
01	02
01	03
01	04
05	05
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	INITIAL RELEASE	ML	11-5-74	
01	-	REV NOTE 3	LA	1-3-75	
02	05360	CC "B" PRE RELEASED	DPM	1-10-75	
03	05514	SEE ECO	DPM	2-25-75	
04	06707	CL II CONN. CONTACT CHG	DPM	1-11-77	
05	08139	FIND NO. 5 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
A	08063	CL. "A" RELEASE CBM	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA

AA6030

NOTES:

DETACHED LISTS

31775-009-070
32466

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO. 74658700	REV. A

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300.
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR SHELL & PIN 1.
4. FIND NUMBER 9 TO BE MARKED PER 10121508 WITH PART NUMBER 74658700, CONNECTOR NUMBER P1 OR P2, AND SERIAL NUMBER.
5. P1 END TO BE COLOR IDENTIFIED YELLOW WITH FIND NUMBER 10.
6. STRIP BACK INSULATION AT BOTH ENDS OF WIRE .25(6.4mm).
7. SLEEVE ALL BARE WIRE USING FIND NO. 13.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74658700	A	CLA	A	CBL AY SYNC RS232 TO 201 2088	UM	2551	01/29/78	02/14/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP5		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN					N
8		51904701	200	PC	CABLE LABLE	IN					N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING ≤5 PIN	IN			PPP4		N
5	A	62013606	1200	PC	SOCKET	IN					N
1	A	62013702	100	PC	CONN PIN HOUSING ≤5 PIN	IN			PPP4		N
4	A	62013801	1200	PC	CONTACT PIN	IN			PPP4		N
9	B	73995500	200	PC	NMPLT KIT BLNK LARGE CABLES	IN			PPP4		N
11	A	74658800	REF	PC	WIRE LIST SYNC RS232 TO MODEM	IN			RFE4		N
7	A	74871633	60000	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
10	A	74871672	1400	IN	TAPE 3/4 WIDE VINYL CLOTH YEL	IN	008063	021578	PPP4		N
6	A	74873611	400	PC	RETAINER MALE SCREW	IN			PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74658701	A	CLA	A	CBL AY SYNC RS232 TO 201 2088	UM	2551	02/01/78	02/14/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP5		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN					N
8		51904701	200	PC	CABLE LABLE	IN					N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING ≤5 PIN	IN			PPP4		N
5	A	62013606	1200	PC	SOCKET	IN					N
1	A	62013702	100	PC	CONN PIN HOUSING ≤5 PIN	IN			PPP4		N
4	A	62013801	1200	PC	CONTACT PIN	IN			PPP4		N
9	B	73995500	200	PC	NMPLT KIT BLNK LARGE CABLES	IN			PPP4		N
11	A	74658800	REF	PC	WIRE LIST SYNC RS232 TO MODEM	IN			RFE4		N
7	A	74871633	120000	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
10	A	74871672	1400	IN	TAPE 3/4 WIDE VINYL CLOTH YEL	IN	008063	021578	PPP4		N
6	A	74873611	400	PC	RETAINER MALE SCREW	IN			PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

DWN	LEVENTHAL	11-4-74	CONTROL DATA	TITLE CABLE ASSY SYNCHRONOUS RS232 TO 208A MODEM	PREFIX /	DOCUMENT NO. 74658900	REV. A
CHKD							
ENG	[signature]	11-5-74	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON 31776-009-070		SHEET 1 OF 4	
APPR			CODE IDENT 34015				

SHEET REVISION STATUS

4	3	2	1
–	00	00	00
–	00	01	01
–	00	01	02
–	00	03	03
04	00	04	04
A	A	A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	–	INITIAL RELEASE	ML	11-9-74	
01	–	REV PI FD NOS	LA	1-8-75	
02	05360	CL "B" PRERELEASED	DBM	1-10-77	
03	06707	CL II CONN. CONTACT CHG	DBM	1-11-77	
04	08139	FIND NO. 5 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
A	08063	CLASS "A" RELEASE CBM	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

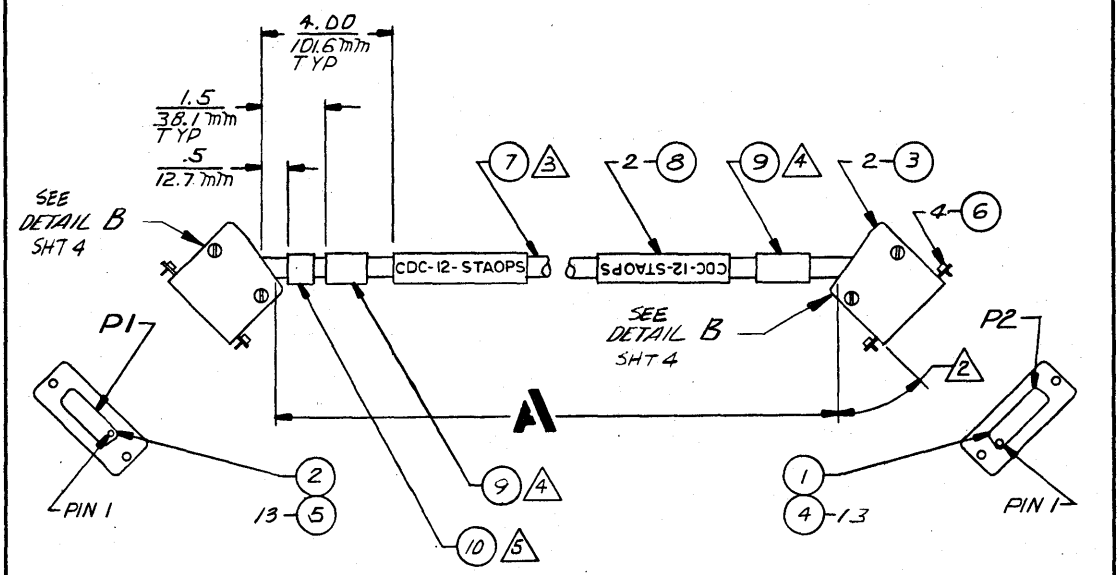
NOTES:

DN 74658900
PL 74658900
DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31776-009-070

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 4	DOCUMENT NO. 74658900	REV. A



FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31776-009-010

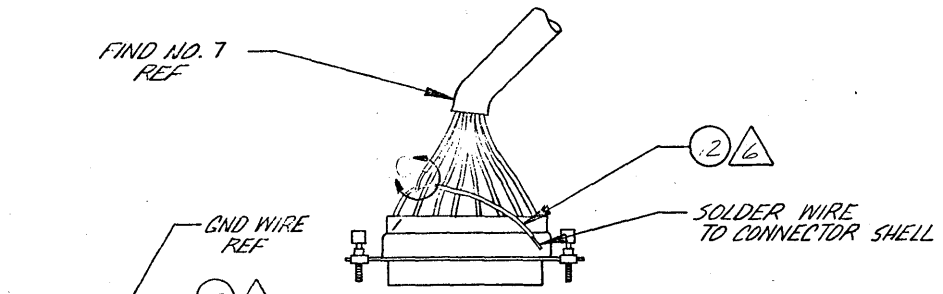
CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	DOCUMENT NO. 74658900	REV. A

CDC NO.	A LENGTH		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74658900	50.0	15.24	31776

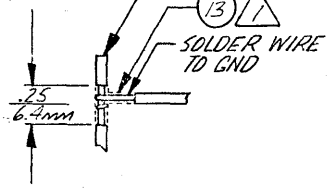
FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31776-009-010

	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	DOCUMENT NO. 74658900	REV. A



DETAIL E
CONN. HOOD OMITTED FOR CLARITY
SCALE: NONE



DETAIL C
SCALE: NONE

FORM 19245-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	LEVENTHAL	11-9-79	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY SYNCHRONOUS RS232 TO 208A MODEM	DN	74658900	A
ENG	D. Rael	1-15-79	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON		SHEET 1 OF 2	
APPR			CODE IDENT 34015	31776-009-070			

SHEET REVISION STATUS

2	1
00	00
01	01
01	02
01	03
04	04
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	INITIAL RELEASE	ML	11-9-79	
01	-	REV NOTE 3	LA	1-8-75	
02	05360	CL "B" PRERELEASED	PRM	1-10-75	
03	06707	CL II CONN. CONTACT CHG	PRM	1-11-77	
04	08139	FIND NO. 5 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
A	08063	CLASS "A" RELEASE CBM	TP	1-27-78	

NOTES:

DETACHED LISTS

FORM 19246-01-015-002 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31776-009-070

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO. 74658900	REV. A

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300.
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR SHELL & PIN 1.
4. FIND NUMBER 9 TO BE MARKED PER 10121508 WITH PART NUMBER 74658900, CONNECTOR NUMBER P1 OR P2, AND SERIAL NUMBER.
5. P1 END TO BE COLOR IDENTIFIED YELLOW WITH FIND NUMBER 10.
6. STRIP BACK INSULATION AT BOTH ENDS OF WIRE .25 (6.4mm).
7. SLEEVE ALL BARE WIRE USING FIND NO. 13.

FORM 19246-00-015-002 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74658900	A	CLA	A	CBL AY SYNC RS232 TO 208A MODL	DM	2551	01/29/78	01/29/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP5		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN					N
A		51904701	200	PC	CABLE LABLE	IN					N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
5	A	62013606	1300	PC	SOCKET	IN					N
1	A	62013702	100	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
4	A	62013801	1300	PC	CONTACT PIN	IN			PPP4		N
9	B	73995500	200	PC	NMPLT KIT BLNK LARGE CABLES	IN			PPP4		N
11	A	74659000	REF	PC	WIRE LIST SYNC RS232 TO 208A M	IN					N
7	A	74871633	A0000	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
10	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	008500		PPP4		N
6	A	74873611	400	PC	RETAINER MALE SCREW	IN			PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER ARDEN HILLS

AA 2709 REV. 7-75

DWN	LEVENTHAL	11-20-7	CONTROL DATA CORPORATION	TITLE CABLE ASSY SYNCHRONOUS RS232 TO TERMINAL 2.4K, 4.8K, 9.6K	PREFIX	DOCUMENT NO. 74659100 REV H
CHKD			COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704			
ENG		1-15-75				
MFG			CODE IDENT 34015	FIRST USED ON XA132-A	31777-009-D 7D	SHEET 1 OF 5
APPR						

SHEET REVISION STATUS

5	4	3	2	1
-	00	00	00	00
-	00	01	01	01
-	00	01	01	02
-	00	01	01	03
-	E	E	E	E
-	E	E	F	F
G	E	E	G	G
G	E	E	G	H

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00		PRELIM RELEASE	ML	11-20-7	
01	-	REV ALL FD NO. CALLOUTS ON SHTS 2 & 3	LA	1-3-75	
02	05360	CL B PREPRELEASED	DPM	1-10-75	
03	05240	SEE ECO	DPM	5-19-75	
E	06323	SEE ECO	LA	4-21-76	
F	06707	CL II CONN. CONTACT CHG	DPM	1-11-77	
G	08139	FIND NO. 3 WAS 62013601 ADDED: BLK WIRE (GND)	ELG		
H	08063	CLASS "A" RELEASE CBM	TP	1-27-79	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA

AA6030

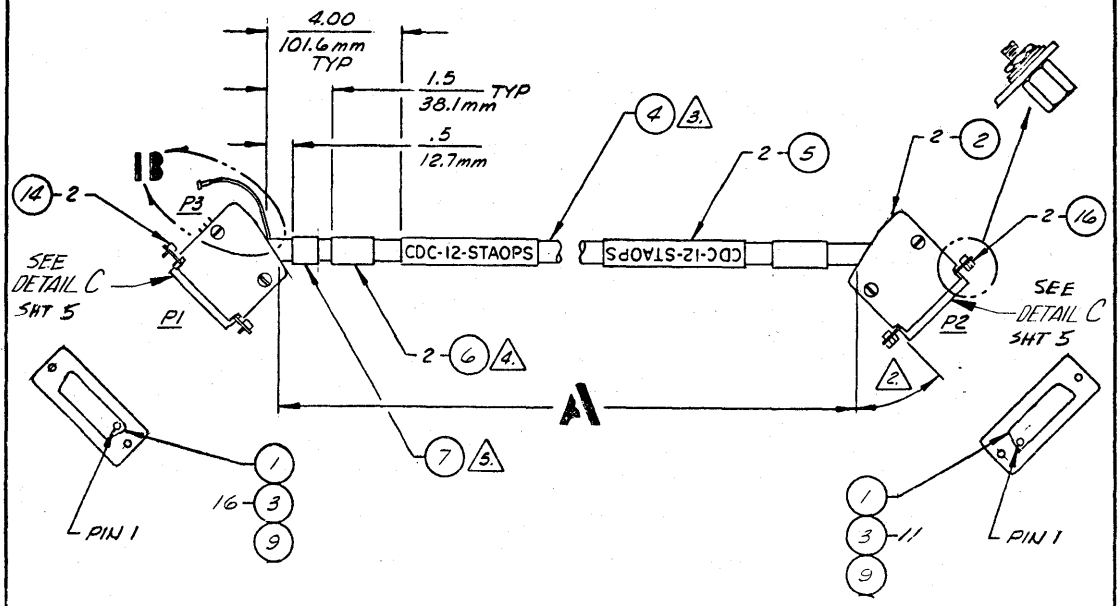
NOTES:

	DN 74659100
WL 74659200	PL 74659100
ASSOC. LISTS	DETACHED LISTS

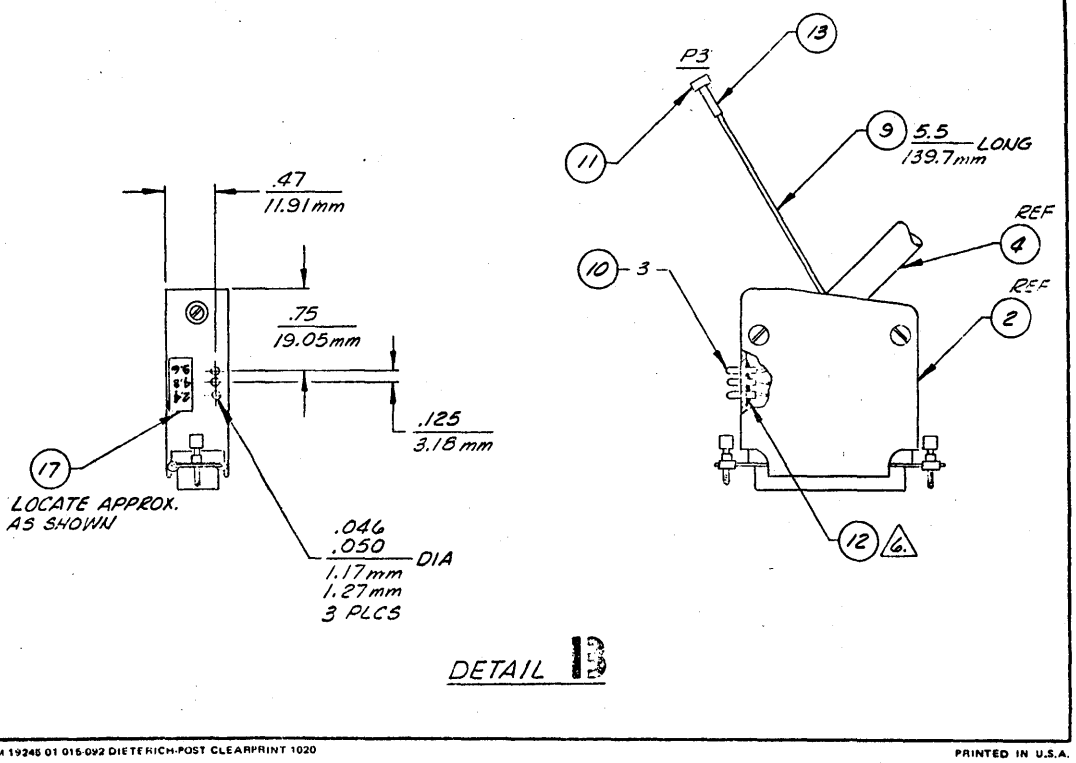
FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31777-009-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 5	DOCUMENT NO. 74659100	REV. G



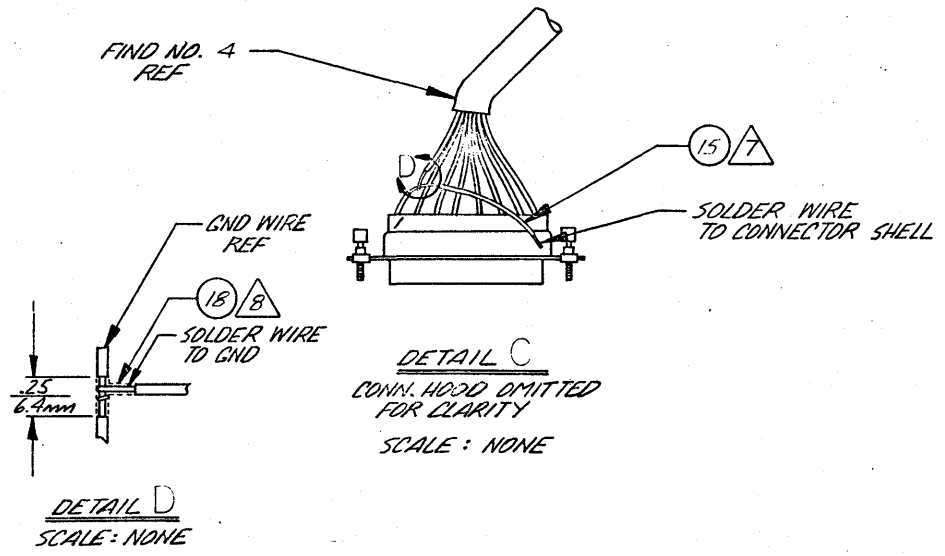
FORM 19245-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.



DETAIL B

CDC Nº.	A LENGTH		RTN Nº.
	FEET ±0.5 FT	METERS ±.15 METERS	
74659100	50.0	15.24	31777

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 5 OF 5		DOCUMENT NO. 74659100	REV. G



DETAIL C
CONN. HOOD OMITTED FOR CLARITY
SCALE : NONE

DETAIL D
SCALE: NONE

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

DWN	LEVENTHAL	11-20-9	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY SYNCHRONOUS RS232 TO TERMINAL 2.4K, 4.8K, 9.6K	DN	74659100	H
ENG	D Pal	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG							
APPR			CODE IDENT 34015	FIRST USED ON XA/32-A	31777-009-070		SHEET 1 OF 2

SHEET REVISION STATUS

2	1
00	00
01	01
01	02
01	03
E	E
F	F
G	G
G	H

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00		PRELIM RELEASE	ML	11-20-9	
01	-	REV NOTES 3, 4 & 6	LA	1-3-75	
02	05360	CL B PRERELEASED	DPM	1-10-75	
03	05240	SEE ECO	DPM	5-19-75	
E	06323	SEE ECO	LA	4-21-76	
F	06707	CL II CONN. CONTACT CHG	DPM	1-11-77	
G	08139	FIND NO. 3 WAS 62013601 ADDED: BLK WIRE (GND)	ELG	1-19-78	
H	08063	CLASS "A" RELEASE CBM	TP	1-27-78	

NOTES:

DETACHED LISTS

FORM 19246-01-015-002 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31777-009-070

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO. 74659100	REV. G

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300.
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR SHELL & PIN 1.
4. FIND NUMBER 6 TO BE MARKED PER 10121508 WITH PART NUMBER 79659100, CONNECTOR NUMBER P1 OR P2, AND SERIAL NUMBER.
5. P1 END TO BE COLOR IDENTIFIED YELLOW WITH FIND NUMBER 7.
6. SECURE FIND NUMBER 10 TO FIND NUMBER 2 WITH FIND NUMBER 12. USE SPARINGLY. DO NOT CONTAMINATE FIND NUMBERS 1 AND 3.
7. STRIP BACK INSULATION AT BOTH ENDS OF WIRE .25(6.4mm).
8. SLEEVE ALL BARE WIRE USING FIND NO. 18.

FORM 19246-00-015-002 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

MF

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74659100	H	CLA	A	CBL AY SYNCH RS232 TO TERMNL 2	DM	2551	01/29/78	01/29/78	1/ 1

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534704	6.00	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
18	C	24534706	1.00	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
15	C	24548301	3.00	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP5		N
9	C	24548310	24.00	IN	WIRE ELEC STRD INS. UL APPD	IN			PPP5		N
2	A	51892202	2.00	PC	HOOD CONNECTOR	IN					N
5		51904701	2.00	PC	CABLE LABLE	IN					N
1	C	62013502	2.00	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
3	A	62013606	27.00	PC	SOCKET	IN					N
6	B	73995400	2.00	PC	NMPLT KIT BLNK SMALL CABLES	IN			PPP4		N
8	A	74659200	REF	PC	WIRE LIST SYNCH RS232 TO TERM	IN			RFE4		N
4	A	74871632	600.00	IN	CABLE 9 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
7	A	74871672	14.00	IN	TAPE 3/4 WIDE VINYL CLOTH YEL	IN	008500		PPP4		N
12	A	74872047	REF	PC	RISK EPOXY RESIN	IN			PPP4		N
17	A	74872052	1.00	PC	LABEL FREQUENCY	IN			PPP4		N
14	A	74873611	2.00	PC	RETAINER MALE SCREW	IN			PPP4		N
16	C	94288024	2.00	PC	CONNECTOR LOCKING DEVICE	IN			PPP4		N
10		94871400	3.00	PC	PIN FORMED .058 DIA	IN					N
11		95828900	1.00	PC	RECEPTACLE RT ANGLE	IN					N

NUMBER OF LINE ITEMS = 18
HIGHEST FIND NUMBER = 18

PROJECT ENGINEER

ARDEN HILLS

AA 2709 REV. 7-75

DWN	L. ANDERSON	1-10-75	CONTROL DATA	TITLE CABLE ASSY- SYNC DIFFERENTIAL CLA TO MODEM	PREFIX	DOCUMENT NO. 74666500	REV E
CHKD							
ENG	[signature]	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG							
APPR			CODE IDENT 34015	FIRST USED ON XA137-A	31835-009-070		SHEET 1 OF 2

SHEET REVISION STATUS

2	1
00	00
01	01
C	C
D	D
D	E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05360	CL B PRERELEASED	LA	1-10-75	
01	05481	SEE ECO	LA	2-14-75	
C	06139	SEE ECO	LA	2-9-76	[illegible]
D	06305	SEE ECO	LA	4-2-76	[illegible]
E	08063	CLASS 'A' RELEASE	TP	1-27-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA
AA6030

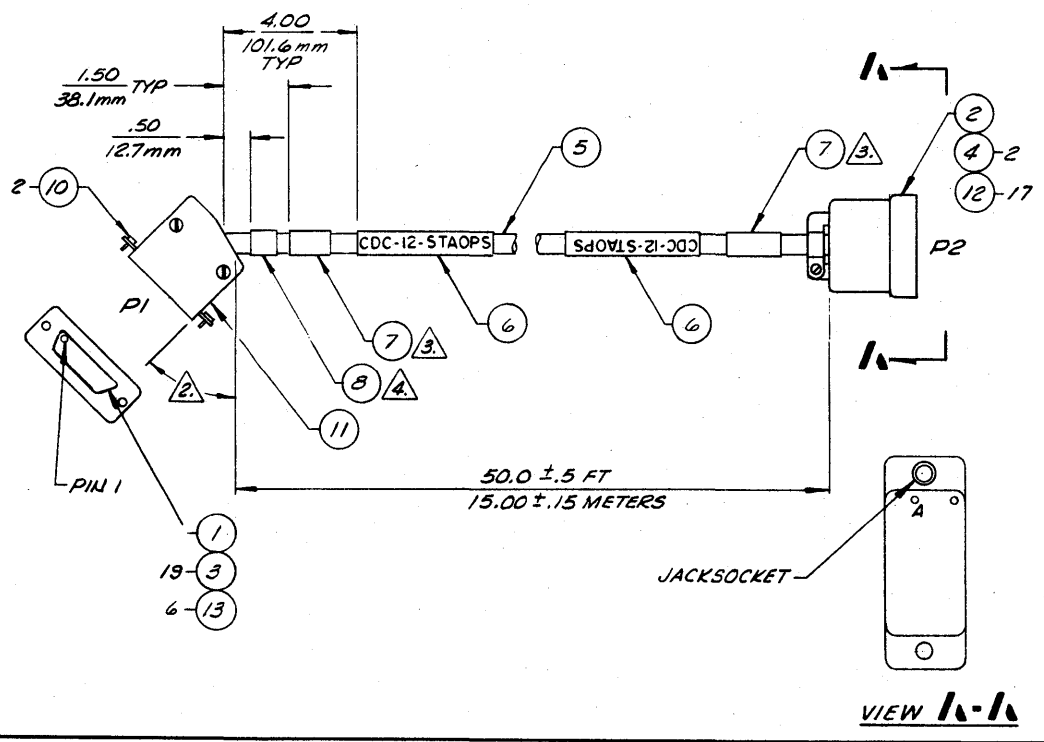
NOTES:

	DN 74666500
WL 74666600	PL 74666500
ASSOC. LISTS	DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31835-009-070

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DOCUMENT NO. 74666500	REV D



FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	L. ANDERSON	1-10-75	CONTROL DATA	TITLE CABLE ASSY- SYNC DIFFERENTIAL CLA TO MODEM	PREFIX DN	DOCUMENT NO. 74666500	REV E
CHKD							
ENG	[signature]	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG							
APPR			CODE IDENT 34015	FIRST USED ON XA137-A	31835-009-070		SHEET 1 OF 2

SHEET REVISION STATUS

2	1
00	00
01	01
C	C
D	D
C	E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05360	CL B PRERELEASED	LA	1-10-75	
01	05481	SEE ECO	LA	2.14.75	
C	06139	SEE ECO	LA	2.10.76	
D	06305	SEE ECO	LA	4.2.76	
E	08063	CLASS "A" REFERENCE	TP	1-27-78	

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

31835-009-070

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO. 74666500	REV. C

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°
3. FIND NO. 7 TO BE MARKED PER 10121508 WITH PART NUMBER 74666500. CONNECTOR NUMBER P1 OR P2, AND SERIAL NUMBER.
4. P1 END TO BE COLOR IDENTIFIED WITH RED USING FIND NO. 8

FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74666500	F	CLA	A	CRI AY SYNC DIFFRNTL CLA TO MD	DM	2551	02/04/78	02/04/78	1/ 1

PR

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PR HC	S OR N
14	A	15003409	800	IN	WIRE ELECT•20 GA•PVC UL 1061	IN			PPP2		N
10		18252504	200	PC	SCREW LOCK ASSY MALE	IN			PPP4		N
11	A	51892202	100	PC	HOOD CONNECTOR	IN			PPP4		N
6		51904701	200	PC	CABLE LABLE	IN			PPP4		N
1	C	53397814	100	PC	CONN•RECTANGULAR•MALE PLUG	IN			PPP5		N
4		65269700	200	PC	CONTACT REMOVABLE	IN			PPP4		N
7	B	73995500	200	PC	NMPLT KIT BLNK LARGE CABLES	IN			PPP4		N
3	A	74397800	1900	PC	CONTACT PIN	IN			PPP4		N
13		74397801	600	PC	CONTACT PIN	IN			PPP4		N
9	A	74666600	REF	PC	CRI AY SYNC DIFFRNTL CLA TO MD	IN			REF4		N
2	A	74871634	100	PC	CONNECTOR 34 CONTACT W HOOD	IN			PPP4		N
8	A	74871673	200	IN	TAPE 3/4 WIDE VINYL CLOTH RED	IN	008500		PPP4		N
5	A	74871722	40000	IN	CABLE 12 TW PR 24 AWG	IN	008500		PPP4		N
12		75770901	1700	PC	CONTACT REMOVABLE	IN			PPP4		N

NUMBER OF LINE ITEMS = 14
HIGHEST FIND NUMBER = 14

PROJECT ENGINEER

ARDEN HILL

AA 2709 REV. 7-79

DWN	L. ANDERSON	1-14-75	CONTROL DATA	TITLE	CABLE ASSY- SYNC COAX CLA TO MODEM	PREFIX	DOCUMENT NO. 74666700 REV E
CHKD							
ENG	S. K. M.	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG				FIRST USED ON	31836-009-070		SHEET 1 OF 3
APPR			CODE IDENT 34015	XA136-A			

SHEET REVISION STATUS

3	2	1
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00	01	01
C	C	C
C	C	D
C	C	E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05360	CL B PRERELEASED	LA	1-14-75	
01	05480	SEE ECO	LA	2-14-75	
C	06234	SEE ECO	LA	3-3-76	[illegible]
D	06440	SEE ECO	LA	7-21-76	[illegible]
E	08063	CLASS "A" RELEASE	TP	1-27-78	[illegible]

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
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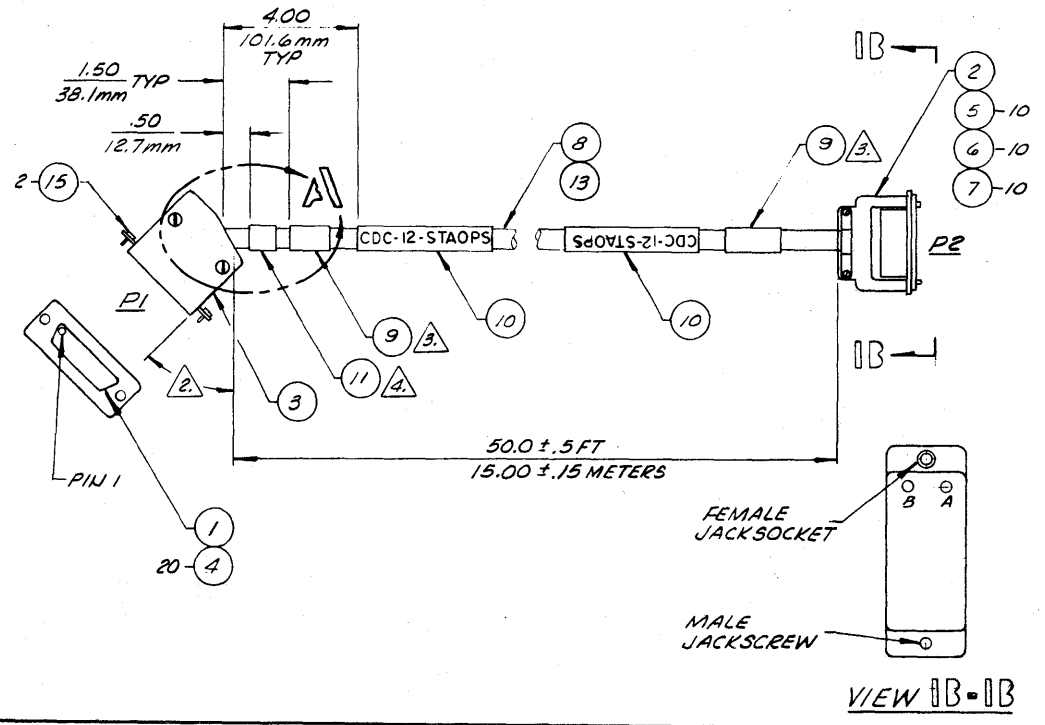
NOTES:

	DN 74666700
WL 74666800	PL 74666700
ASSOC. LIST	DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

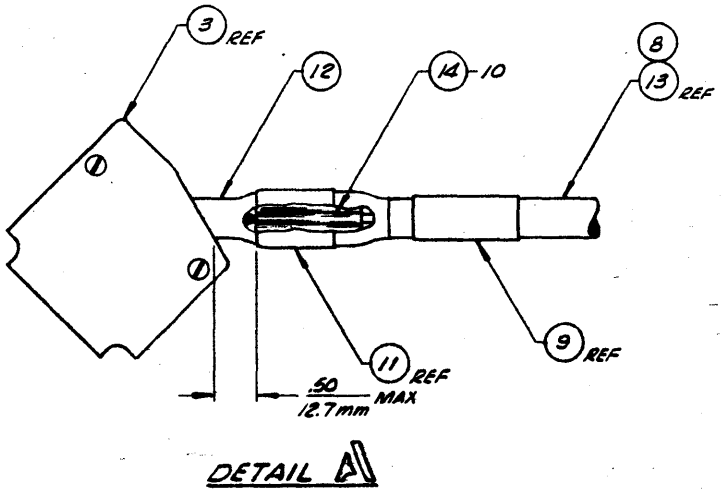
31836-009-070

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 3	DOCUMENT NO. 74666700	REV C



FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 3	DOCUMENT NO. 74666700	REV. C



DETAIL A

FORM 19248-00-015-092 DIETZGEN-POST CLEARPRINT 1020

PRINTED IN U.S.A.

DWN	L. ANDERSON	1-14-75	CONTROL DATA	TITLE CABLE ASSY- SYNC COAX CLA TO MODEM		PREFIX DN	DOCUMENT NO 74666700	REV E
CHKD								
ENG	L. Rod	1-5-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704					
MFG				FIRST USED ON XA136-A	31836-009-070		SHEET 1 OF 2	
APPR			CODE IDENT 34015					

SHEET REVISION STATUS

2	1
00	00
00	01
C	C
C	D
C	E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05360	CC 8 PRERELEASED	LA	1-14-75	
01	05480	SEE ECO	LA	2-14-75	
C	06234	SEE ECO	LA	3-3-76	
D	06440	SEE ECO	LA	7-21-76	
E	08063	CLASS 'A' RELEASE	TP	1-27-78	

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31836-009-070

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	DN	DOCUMENT NO 74666700	REV C

NOTES:

1. WORKMANSHIP PER CDC-SPEC 10120300
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°
3. FIND NUMBER 9 TO BE MARKED PER 10121508 WITH PART NUMBER 74666700, CONNECTOR NUMBER P1 OR P2, AND SERIAL NUMBER.
4. P1 END TO BE COLOR IDENTIFIED WHITE WITH FIND NUMBER 11

FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74666700-	F	CLA	A	CBL AY SYNC COAX CLA TO MODEM	DM	2551	01/29/78	07/30/78	1/ 1

PR

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN HC	S OR N
13	A	17510002	60000	IN	SLEEVE CABLE ZIPPER .625 DIA	IN	008500		PPP4		N
12	C	24534714	300	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
5		36172104	1000	PC	CONTACT	IN			PPP4		N
6		36172301	1000	PC	CONTACT	IN			PPP4		N
8	A	51003291	60000	IN	CABLE COAX RG180B U	IN	008500		PPP4		N
3	A	51892202	100	PC	HOOD CONNECTOR	IN			PPP4		N
10		51904701	200	PC	CABLE LABLE	IN			PPP4		N
1	C	53397814	100	PC	CONN-RECTANGULAR,MALE PLUG	IN			PPP5		N
9	B	73995500	200	PC	NMPLT KIT BLNK LARGE CABLES	IN			PPP4		N
4	A	74397800	2000	PC	CONTACT PIN	IN			PPP4		N
16	A	74666800	REF	PC	WIRE LIST SYNC COAX CLA TO MDM	IN			RFF4		N
14	A	74871108	1000	PC	SLEEVE SOLDER	IN			PPP4		N
11	A	74871676	200	IN	TAPE 3/4 WIDE VINYL CLOTH WHT	IN	008500		PPP4		N
2	A	74871816	100	PC	CONNECTOR BODY	IN			PPP4		N
15		94248020	200	PC	SCREW LOCK MALE	IN			PPP4		N
7		94333239	1000	PC	RING	IN			PPP4		N

NUMBER OF LINE ITEMS = 16
HIGHEST FIND NUMBER = 16

PROJECT ENGINEER ARDEN HILL

AA 2708 REV. 7-79

This section contains wire lists for the cable assemblies used with the synchronous data link control communications line adapter.

DWN	L. ANDERSON	5-13-76	CONTROL DATA	TITLE	CABLE ASSY- SYNC RS232 TO 203A	PREFIX	DOCUMENT NO.	REV
CHKD		5-17-76	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704			WL	74658600	D
ENG		5-13-76						
MFG			CODE IDENT 34015	FIRST USED ON XA131-A	31774-028-070		SHEET 1 OF 2	
APPR								

SHEET REVISION STATUS

2	1
B	B
C	C
C	D

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
B	06367	SEE ECO	L.A	5-13-76	
C	06707	CL II CONN. CONTACT CHG	PRM	1-11-77	
D	08063	CLASS "A" RELEASE CBM	TP	1-20-78	

INTER-DIVISIONAL DOCUMENT
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NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31774-028-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO 74658600	REV C

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	6	22	BLK		P1	1	4	P2	1	5	PROTECTIVE GND
2	↑	↑	BRN		↑	2	↑	↑	2	↑	TRANSMITTED DATA
3			RED			3			3		RECEIVED DATA
4			ORN			4			4		REQUEST TO SEND
5			YEL			5			5		CLEAR TO SEND
6			GRN			6			6		DATA SET READY
7			BLU			7			7		SIGNAL GND
8			VIO			8			8		DATA CARRIER DET
9			GRY			15			15		SERIAL CLOCK TX
10			WHT			17			17		SERIAL CLOCK RX
11			WHT/BLK			20			20		DATA TERM. READY
12	↓	↓	WHT/BRN			21		↓	21	↓	SIGNAL QUALITY DET
13	6	22	WHT/RED			22		P2	22	5	RING INDICATOR
14	12	20	WHT		↓	13	↓	P1	25	4	M/CLOCK - T/CLOCK
15	6	-	SHIELD		P1	1	4	P2	1	5	PROTECTIVE GND

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	LEVENTHAL		COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	TITLE CABLE ASSY SYNCHRONOUS RS232 TO 201/208B MODEM	PREFIX WL	DOCUMENT NO. 74658800	REV A
CHKD							
ENG	D Pal	1-15-74					
MFG			CODE IDENT 34015	FIRST USED ON 31775-028-070		SHEET 1 OF 2	
APPR							

SHEET REVISION STATUS

2	1
00	
01	01
01	02
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	INITIAL RELEASE	ML	11-5-74	
01	-	REV COLORS; DELETE COND 9; ADDED COND. 12: RENUMBERED COND 9-12	LA	1-3-75	
02	05360	CL "B" PRERELEASED	DPM	1-10-75	
A	08063	CLASS "A" RELEASE CBM	TP	1-20-78	

INTER-DIVISIONAL DOCUMENT
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NOTES:

DETACHED LISTS

FORM 19248-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31775-028-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74658800	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	7	22	SHIELD WIRE		CONN P1	1	5	CONN P2	1	4	PROTECTIVE GND
2	↓	↓	BLK		↓	2	↓	↓	2	↓	TRANSMITTED DATA
3			BRN			3			3		RCVD DATA
4			RED			4			4		REQ TO SEND
5			ORN			5			5		CLR TO SEND
6			YEL			6			6		DATA SET READY
7			GRN			7			7		SIGNAL GND
8			BLU			8			8		DATA CAR DET
9			VIO			15			15		SERIAL CLOCK TX
10			GRY			17			17		SERIAL CLOCK RX
11	↓	↓	WHT		↓	22	↓	↓	22	↓	RING INDICATOR
12	7	22	WHT/BLK		CONN P1	20	5	CONN P2	20	4	DATA TERM READY

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DWN	LEVENTHAL	11-4-74	CONTROL DATA	TITLE CABLE ASSY SYNCHRONOUS RS232 TO 208A MODEM	PREFIX WL	DOCUMENT NO. 74659000	REV A
CHKD							
ENG	D. Post	1-5-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG							
APPR			CODE IDENT 34015	FIRST USED ON 31776-029-070		SHEET 1 OF 2	

SHEET REVISION STATUS

2	1
00	00
01	01
01	02
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	—	INITIAL RELEASE	ML	11-4-74	
01	—	REV COLORS & COND 9	LA	1-3-75	
02	05360	CL "B" PRERELEASED	DPM	1-10-75	
A	08063	CLASS "A" RELEASE CBA	TP	1-20-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
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NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31776-028-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74659000	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	7	22	SHIELD WIRE		CONN P1	1	5	CONN P2	1	4	PROTECTIVE GND
2	↑	↑	BLK		↑	2	↑	↑	2	↑	TRANSMITTED DATA
3			BRN			3			3		RCVD DATA
4			RED			4			4		REQUEST TO SEND
5			ORN			5			5		CLEAR TO SEND
6			YEL			6			6		DATA SET READY
7			GRN			7			7		SIGNAL GND
8			BLU			8			8		DATA CARRIER DET
9			VIO			15			15		SERIAL CLOCK TX
10			GRY			17			17		SERIAL CLOCK RX
11			WHT			14			14		NEW SYNC
12	↓	↓	WHT/BLK		↑	21	↓	↑	21	↓	SIGNAL QUALITY DET
13	7	22	WHT/BRN		CONN P1	11	5	CONN P2	11	4	QUALITY MONITOR

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	LEVENTHAL	11-20-74	CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY SYNCHRONOUS RS 232 TO TERMINAL 2.4K, 4.8K, 9.6K	WL	74659200	F
ENG	[signature]	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG			CODE IDENT 34015	FIRST USED ON XA132-A	31777-028-070	SHEET 1 OF 2	
APPR							

SHEET REVISION STATUS

2	1
0000	00
01	01
01	02
D	D
E	E
E	F

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	PRELIM RELEASE	ML	11-20-74	
01	-	REV WIRE LIST	LA	1-3-75	
02	05360	CL B PRERELEASED	DPM	1-16-75	
D	06323	SEE ECO	LA	4-21-76	[signature]
E	06707	CL II CONN. CONTACT CHG	DPM	1-11-77	[signature]
F	08063	CLASS "A" RELEASE CBM	TP	1-27-78	[signature]

INTER-DIVISIONAL DOCUMENT
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NOTES: ⚠1. CONTACT SOCKET FOR TERMINATING TWO (2) 22 AWG WIRES.

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31777-028-070

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO 74659200	REV E

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	4	22	SHIELD WIRE		CONN P1	1	3	CONN P2	1	3	PROTECTIVE GND
2	4	↓	BLK		↓	2	3	P2	3	3	TRANS/RCVD DATA
3	4		BRN			3	3	P2	2	3	RCVD/TRANS DATA
4	9		WHT			4	3	P1	5	⚠1 3	REQ/CLEAR TO SEND
5	4		RED			5	⚠1 3	P2	8	3	CLR TO SND/DATA CAR DET
6	4		ORN			6	3		20	3	DATA SET/TERM READY
7	4		YEL			7	3		7	3	SIGNAL GND
8	4		GRN		P1	8	3	↓	4	⚠1 3	DATA CAR DET/REQ TO SEND
9	9		WHT		P2	4	⚠1 3	CONN P2	5	3	REQ/CLEAR TO SEND
10	9		WHT		P1	9	3	SOCKET	9.6	10	F/T CLOCK
11	9		WHT		↓	10	3	SOCKET	4.8	10	F/2 CLOCK/T CLOCK
12	9		WHT			12	3	SOCKET	2.4	10	F/4 CLOCK/T CLOCK
13	4		BLU			17	⚠1 3	CONN P2	17	⚠1 3	SERIAL CLOCK RX
14	9		WHT			17	⚠1 3	P1	24	⚠1 3	EXT SERIAL CLOCK TX
15	4		VIO			20	3	P2	6	3	DATA TERM SET READY
16	9		WHT		P1	25	3	P3	1	11	
17	9	↓	WHT		P2	15	3	↓	17	⚠1 3	SERIAL CLOCK TX/RX
18	12	22	WHT		CONN P1	24	⚠1 3	CONN P1	15	3	SERIAL CLOCK TX/RX

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DWN	L. ANDERSON	1-10-75	CONTROL DATA	TITLE	CABLE ASSY- SYNC DIFFERENTIAL CLA TO MODEM	PREFIX	DOCUMENT NO.	REV
CHKD						WL	74666600	E
ENG	D. Pal	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704					
MFG				FIRST USED ON	31835-028-070		SHEET 1 OF 2	
APPR			CODE IDENT 34015	XA137-A				

SHEET REVISION STATUS

3	2	1
00	00	00
B	B	B
-	C	C
	D	D
	D	E

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05360	CL B PRERELEASED	LA	1-10-75	
B	06139	SEE ECO	LA	2-10-76	
C	06305	SEE ECO	LA	4-2-76	
D	06419	SEE ECO	LA	6-29-76	
E	08063	CLASS "A" RELEASE	TP	1-20-78	

INTER-DIVISIONAL DOCUMENT
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NOTES:
1. CONTACT PIN FOR TERMINATING TWO (2) 22 AWG WIRES.
2. GREEN WIRES FROM P1, CONDUCTORS 1 THRU 7, ARE TO BE TERMINATED AT P2 PIN B.

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31835-028-070

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74666600	REV. D

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN		ACCESS FIND NO.	DESTINATION		ACCESS FIND NO.	REMARKS
1	5	24	CLEAR		CONN P1	5	3	CONN P2	D	12	CLEAR TO SEND
	5	↑	GRN		↑ ↑	2	13 1.	↑ P2	B	4	GND 2.
2	5		CLEAR			4	3	P2	C	12	REQUEST TO SEND
	14		GRN			2	13 1.	P1	3	1.	GND
3	5		CLEAR			8	3	P2	F	12	RCVD LINE SIGNAL DET
	14		GRN			3	13 1.	P1	7	1.	GND
4	5		CLEAR			6	3	P2	E	12	DATA SET READY
	14		GRN			7	13 1.	P1	18	1.	GND
5	5		CLEAR			20	3	P2	H	12	DATA TERM READY
	14		GRN			18	13 1.	P1	19	1.	GND
6	5		CLEAR			22	3	P2	J	12	RING INDICATOR
	14		GRN			19	13 1.	P1	21	1.	GND
7	5		CLEAR			11	3	P2	K	12	LOCAL TEST
	14		GRN			21	13 1.	P1	23	3	GND
8	5		CLEAR			10	3	P2	Y	12	SET CLOCK TRANS A
	↑		GRN			9	↑	↑	B	↑	SET CLOCK TRANS B
9			CLEAR			13			V		SER CLOCK RECEIVE A
			GRN			12			X		SER CLOCK RECEIVE B
10			CLEAR			15			R		RECEIVED DATA A
			GRN			14			T		RECEIVED DATA B
11			CLEAR			17			P		SEND DATA A
			GRN			16			S		SEND DATA B
12		↓	CLEAR			24			U	↓	EXT CLOCK TRANS A
	↓	24	GRN		↓ ↓	25	↓	↓ ↓	W	12	EXT CLOCK TRANS B
13	5	22	DRAIN WIRE		CONN P1	1	3	CONN P2	A	4	PROTECTIVE GND

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	L. ANDERSON	1-14-75	CONTROL DATA	TITLE	CABLE ASSY- SYNC COAX CLA TO MODEM	PREFIX	DOCUMENT NO.	REV
CHKD						WL	74666800	A
ENG	D. F. M.	1-15-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704					
MFG				FIRST USED ON			SHEET 1 OF 2	
APPR			CODE IDENT 34015	XA136-A	31836-028-070			

SHEET REVISION STATUS

2	1
00	00
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05360	CL B PRERELEASED	LA	1-14-75	
A	08063	CLASS "A" RELEASE	TP	1-20-78	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024. CA

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NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31836-028-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74666800	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	8	COAX			CONN P1	2	4	CONN P2	D	5	REQ TO SEND
2	↑	↑			↑	14	↑	↑		6,7	SHIELD GND
3						3			G	5	LOCAL TEST
4						4				6,7	SHIELD GND
5						17			E	5	TRANSMIT DATA
6						5				6,7	SHIELD GND
7						18			C	5	CLEAR TO SEND
8						6				6,7	SHIELD GND
9						10			J	5	TRANSMIT CLOCK
10						11				6,7	SHIELD GND
11						13			L	5	RECEIVE CLOCK
12						12				6,7	SHIELD GND
13						15			K	5	RECEIVE DATA
14						16				6,7	SHIELD GND
15						19			M	5	CARRIER DET
16						20				6,7	SHIELD GND
17						23			F	5	DATA SET READY
18						22				6,7	RING INDICATOR
19	↓	↓			↓	24	↓	↓	H	5	EXTERNAL TRANSMIT CLOCK
20	8	COAX			CONN P1	25	4	CONN P2		6,7	SHIELD GND

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

GLOSSARY

A

This appendix consists of an alphabetical listing of all acronyms and mnemonics used in this manual. For convenience, all mnemonics for signal names are presented in the true or conventional state, although some signal names exist only in the false or reverse level state.

ACLA	Asynchronous communications line adapter
ADD	Address (bit)
AGC	Automatic gain control
CLA	Communications line adapter
CLE	Communications line expansion (unit)
CO	Code bit
COMn	Command word (1, 2, or 3)
CRC	Cyclic redundancy check
CTS	Clear to send
CTSS	Clear to send status
DA	Data available
DAR	Data available reset
DAT	Data receive register (bit)
DAVF	Data available hold
DCD, DCDA	Data carrier detect
DCDS	Data carrier detect status
DSR, DSRA	Data set ready
DSRS	Data set ready status
DTO	Data transfer overrun
DTOS	Data transfer overrun status
DTR	Data terminal ready
ETX	End of block
EXTC	External transmit clock
Fn	Frequency (code 1, 2, 4)
FDX	Full duplex
HDX	Half duplex
IA	Input available
IADD	Input address state
IAV	Input available
IDATA	Input data state
IEN	Input end
IER	Input error
II	Information input (bit)
ILE	Input loop error
IO	Information output (bit)
I/O	Input/output
ION	Input on
IS	Input select
ISI	Input select idle
ISON	Input status on
ISR	Input status request
IST, ISTA	Input strobe
ISUPn	Input supervision word (1 or 2)
LED	Light emitting diode
LIT	Loop internal test
LITCK	Loop internal test clock
LM	Loop multiplexer
LSI	Large scale integration
LPTTL	Low power transistor-transistor logic
LT	Local test
MCK	Modem transmit clock
MCL, MCLA	Master clear
MLIA	Multiplex loop interface adapter
Modem	Modulator/demodulator
MODST	Modem status
MS	Mode select
NCNA	Next character not available
NCNAS	Next character not available status
NPU	Network processing unit
NSYN	New synchronization
ODATA	Output data
ODD	Output data demand
ODDF	Output data demand hold
OER, OERA	Output error
OF	Output format (bit)
OLE	Output loop error
OLES	Output loop error set
OON	Output on
OSC	Output select clear
OSL	Output select
OST, OSTA	Output strobe
OSUP	Output supervision
PAD	Dummy character
PE	Parity error
PES	Parity error status
PI	Parity inhibit
PSET	Parity set
QM, QMA	Quality monitor
QMS	Quality monitor status
RC	Receive comparator
RD	Receive data
RDAT, RDATA	Reset data
RDAV	Reset data available
RDTO	Reset data transfer overrun
RHR	Receiver holding register
RI, RIA	Ring indicator
RIS	Ring indicator status
RNCNA	Reset next character not available
RODD	Reset output data demand
ROLE	Reset output loop error
RPE	Reset parity error
RR	Receiver error
RSUP	Reset supervision
RSYN	Resynchronize
RTS	Request to send
SAV	Status available
SAVF	Status available hold
SCLA	Synchronous communications line adapter
SCR	Serial clock receive
SCT, SCTA	Serial clock transmit
SCTE	Serial clock transmit external
SD	Send data
SDT	Serial data transmit
SDTO	Set data transfer overrun
SELI	Select input
SELO	Select output
SFR	Status flag reset
SODD	Set output data demand
SPE	Set parity error
SQD, SQDA	Signal quality detector
SQDS	Signal quality detector status
SS	Synchronization search
SYN	Synchronization
TCK	Transmit clock
TD, TDA	Transmit data
THR	Transmitter holding register
THRE	Transmitter holding register empty
THRL	Transmitter holding register load
TSL	Transmitter shift register
TTC	Transmitter timing and control
TTL	Transistor-transistor logic

TO CONVERT DECIMAL TO HEXADECIMAL

1. Find decimal number in body of table (Example: 157).
2. Scan horizontally to the left to find the first hexadecimal digit (in this case, 9).
3. Scan vertically up (from 157 in table) to find second hexadecimal digit (in this case, D).
4. Thus decimal number 157 = hexadecimal number 9D.

TO CONVERT HEXADECIMAL TO DECIMAL

1. Find first hexadecimal digit in left-hand column (Example: D).
2. Find second hexadecimal digit in top row (Example: 9).
3. Simultaneously scan horizontally to right (from D) and scan vertically downward (from 9) to find point of intersection in body of table (in this case, 217).
4. Thus hexadecimal number D9 = decimal number 217.

TABLE B-1. HEXADECIMAL/DECIMAL CONVERSION

First Hexadecimal Digit	Second Hexadecimal Digit															
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
A	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
B	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
C	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
E	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
F	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

COMMENT SHEET

MANUAL TITLE Synchronous Communications Line Adapter, DU138-A, DU139-A, DU140-A Hardware Maintenance Manual

PUBLICATION NO. 74700700 REVISION D

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APPENDIXES

FIGURES

TABLES

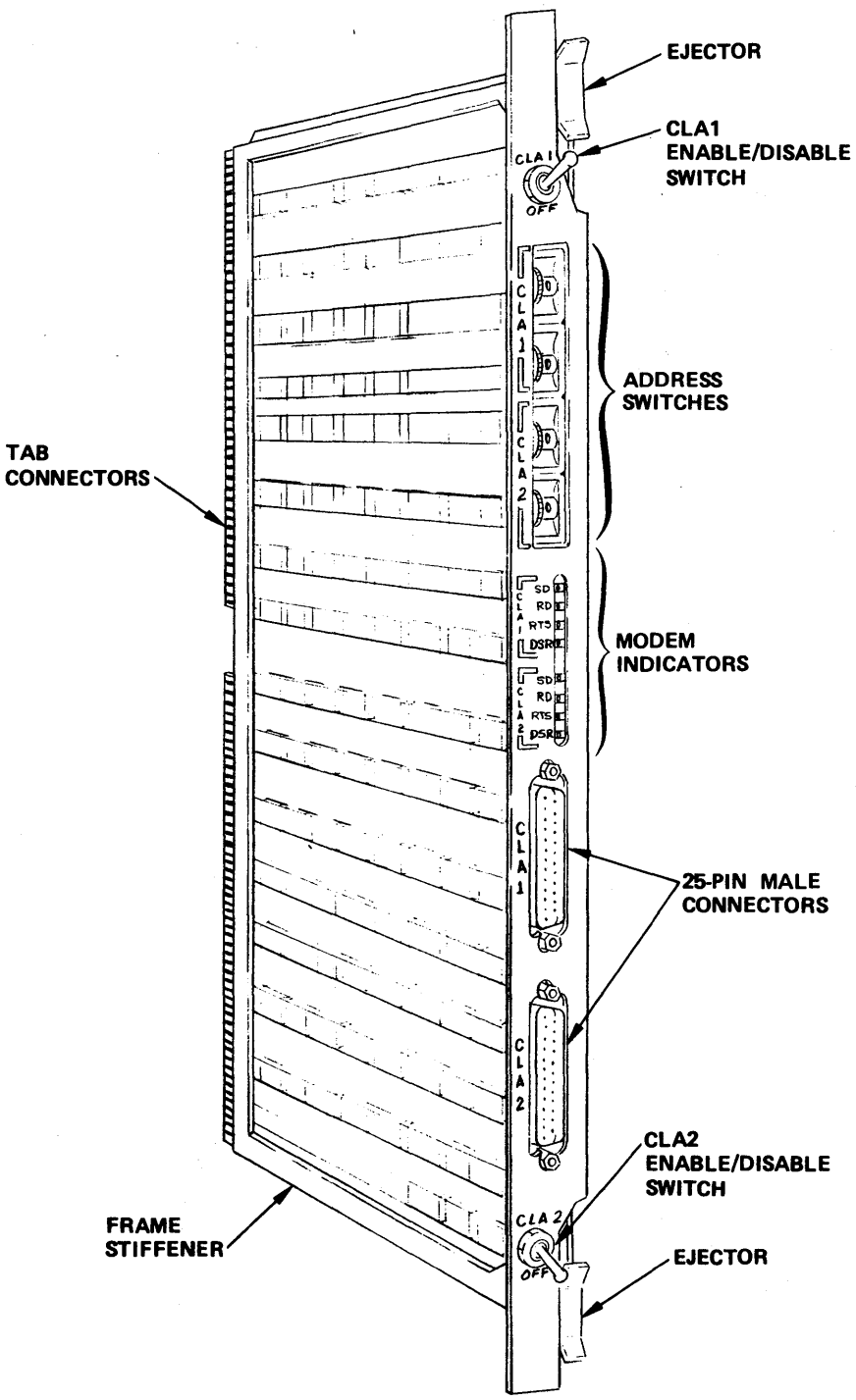


Figure 1-1. ACLA Circuit Card

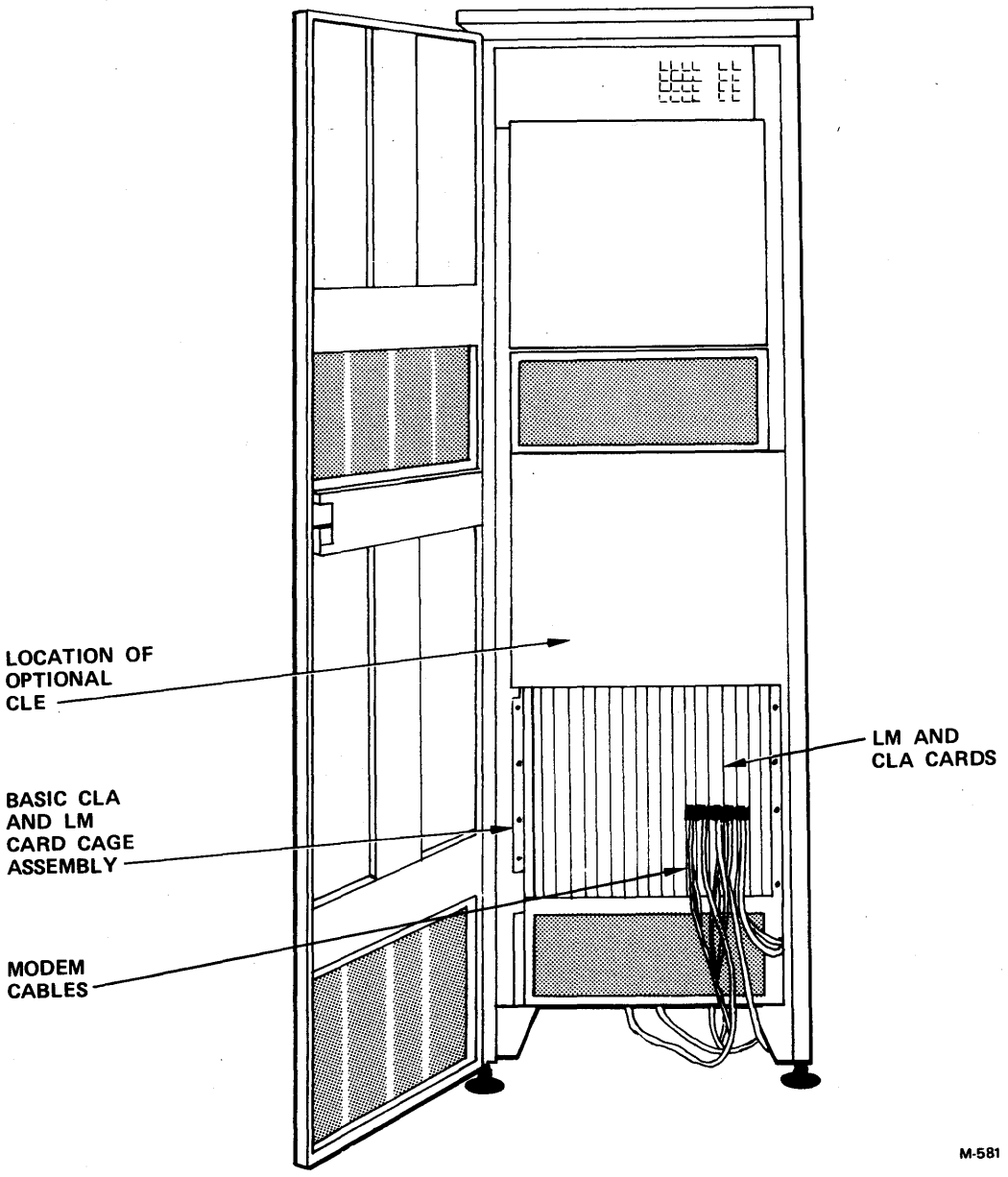


Figure 1-3. Location of CLA and LM Card Cage in NPU Cabinet

TABLE 1-1. PHYSICAL CHARACTERISTICS

Characteristics	Value
Dimensions	
Length	14 in. (356 mm)
Width	11 in. (279 mm)
Thickness	
with card handle	0.9 in. (23 mm)
card only	0.063 in. (1.6 mm)
Weight	1.6 lb (0.73 kg)
Power Requirement	
Consumption	13.6 watts
Logic voltages	+5.0 ±0.25 V 2.00 amp; +12.0 ±0.50 V 0.15 amp; -12.0 ±0.50 V 0.15 amp

TABLE 1-2. NONOPERATING ENVIRONMENTAL REQUIREMENTS

Parameter	Requirement
Altitude	1000 ft (305 m) below sea level to 15,000 ft (4575 m) above sea level
Temperature	-30°F to +150°F (-35°C to +66°C)
Thermal Shock	+80°F to -30°F (+27°C to -35°C) or +80°F to +150°F (+27°C to +66°C) (rate of change not to exceed 20°F (11.1°C) per hour)
Humidity	5% to 95% (no condensation)
Shock	18 impacts of 5g ±10% for a duration of 11 ±1 msec, with a maximum g occuring at 5.5 msec. 3 impacts in each direction along 3 major axes
Vibration	Peak displacement ±0.005 in. at 5 to 60 Hz, and acceleration of 2g at 60 to 500 Hz as packed for shipment

TABLE 1-3. OPERATING ENVIRONMENTAL REQUIREMENTS

Parameter	Requirement
Altitude	1000 ft (305 m) below sea level to 6000 ft (1830 m) above sea level
Temperature	Recommended: +72°F (+22°C) (ambient temperature for 255X Series system)
Humidity	Continuous operation at 90% relative humidity and 104°F(40°C). No operational condensation requirements. Excursion rate: not to exceed 10% per hour
Particulate Contamination	Range 3
Caustic Chemical Environment	Not allowed

SIGNALING RATE SELECTION

The ACLA can operate at any of the standard signaling rates: 75, 110, 134.5, 150, 300, 600, 1200, 2400, 4800, and 9600 baud. Other rates are also available. The signaling rate is selected by program command and can be different for transmit and receive.

RESTRAINT SIGNAL DETECTION

The ACLA provides the necessary interface for operating with an AT&T 811B Auxiliary Data Set used for TWX network connections. When the 811B detects a restraint condition from the TWX central office equipment, it activates a restraint-detection signal to the ACLA, causing the ACLA to suspend data transmission.

DATA TRANSFER OVERRUN

The ACLA generates data-transfer-overrun status bit if it assembles a new character before a previously assembled character has been transferred to the processor.

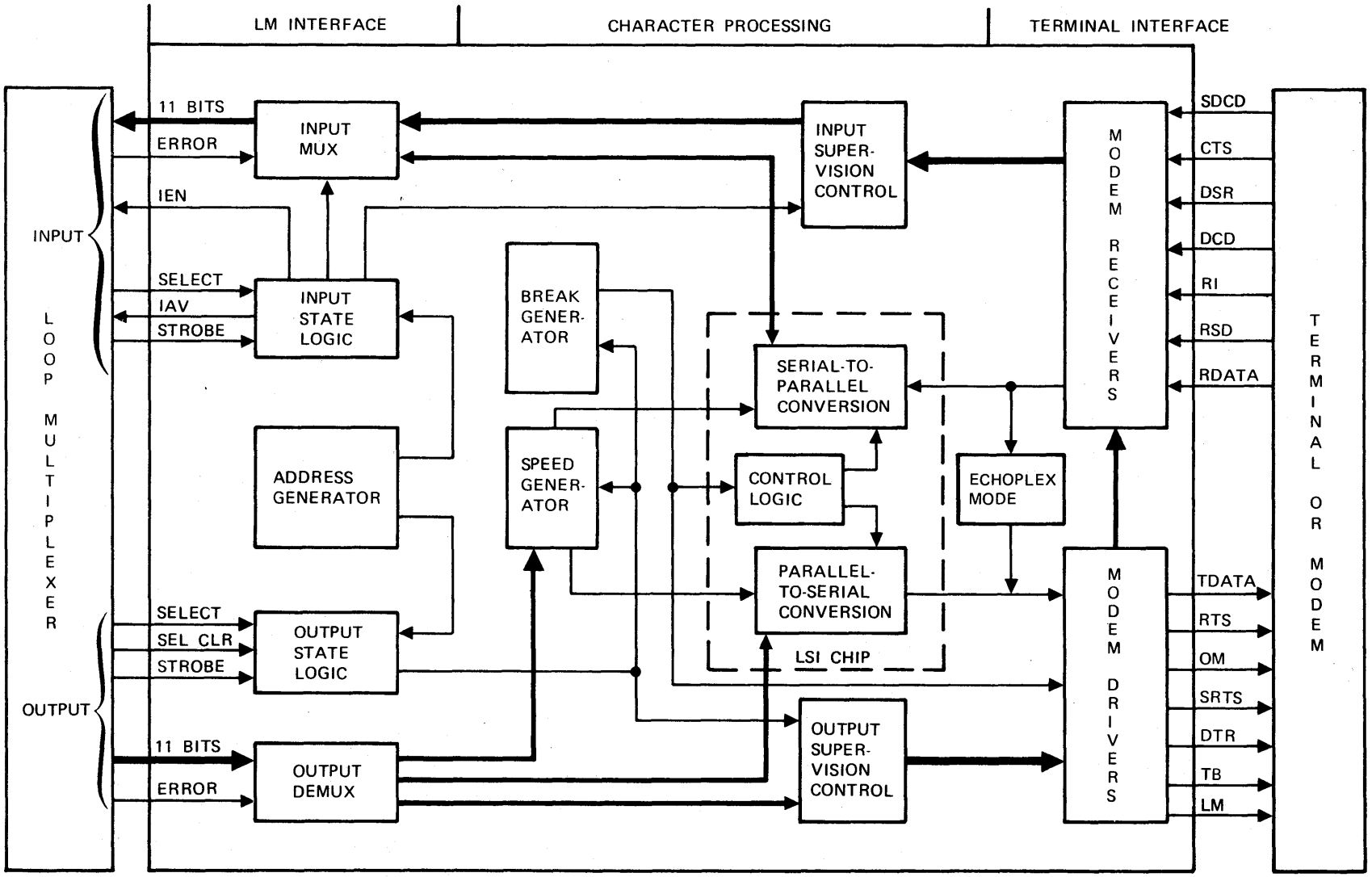


Figure 1-5. ACLA Block Diagram

the first data character to the ACLA. The ACLA is inhibited from generating ODDs if any one of the following conditions are met: clear-to-send (CTS) signal from the modem is inactive; restraint detector from the modem is active; or OON is inactive.

Data received by the ACLA is loaded into the transmitter holding register by the output strobe signal and then into the transmitter shift register in preparation for a serial transmission on the transmit data line. This transference of data from the holding register to the shift register causes an ODD to be generated, which is forwarded to the processor, informing the processor that the ACLA can accept another character. If another data character is not received by the ACLA before completion of the serial transmission of the character in process, the transmit data line remains in the marking condition.

ECHOPLEX MODE

Upon receipt of a command, the ACLA can route the data received from the modem back to the modem while accomplishing normal processing of the incoming data.

BREAK GENERATION

Following the receipt of a break command, the ACLA places the transmit-data line at a constant spacing condition. This condition continues until a command is received to turn break command to off.

LOOP ERROR DETECTION

The ACLA monitors two error lines from the loop multiplexer for the reporting of errors on the loop. One line indicates errors on the input loop while the other indicates errors on the output loop. The ACLA reports input error status if the input line toggles true during an input select or output error status if the output line toggles true during the output select.

CLA ADDRESSING

Each CLA may be one of 32 CLAs attached to the loop multiplexer backplane. In order to increase efficiency, many of the signals coming to the ACLA are bus organized. Because of this, each ACLA must be capable of generating an 8-bit address on input frames and recognizing the same 8-bit address on output frames. Figure 1-5 shows the data interchange between the ACLA and the loop multiplexer.

MASTER CLEAR

When the master-clear (MCL) signal originating at the LM attains a logic 1 condition, the ACLA is set to an idle state; all bits of command word 1, break and ISON bits of command word 2, and ECHO and LIT bits of command word 3 are set to a logic 0; in addition, the transmit and receive shift register, receive storage buffer, framing-error status, parity-error status, and data-transfer-overrun status are reset. The transmit-data line sets to a marking condition. Input-loop-error, output-loop-error status, and ODD are not reset. MCL must be active a minimum of 30 microseconds before the ACLA is guaranteed to be in the idle condition.

Modem Interface Section

The modem interface section of the ACLA provides the level conversion logic to make the ACLA compatible with the signal levels of the modem. This section of the ACLA also monitors the modem status lines for a change of condition: either a logic 1-to-0, or 0-to-1 transition. When a change occurs, status is reported to the processor. An exception of this procedure is that the ring-indicator signal only triggers a status report on a logic 1-to-0 transition.

Via command from the processor, the ACLA can route the transmit data back to the input data assembly logic to test the data handling logic. The ACLA also returns the modem control signals to the modem monitor lines to verify operation of the modem interface circuits. The ACLA displays the condition of four RS-232-C interface lines via lights located on the card handle.

Speed Generators

The receive and transmit sections of the ACLA require clock sources that have a frequency 16 times the desired baud rate. The ACLA provides a receive or a transmit speed generator that selects one of four clock frequencies, divides it by a predetermined number between 1 and 16, and applies the quotient to the respective receive or transmit section of the ACLA. The speed generators function identically but are controlled by the processor independently through use of command words 2 and 4.

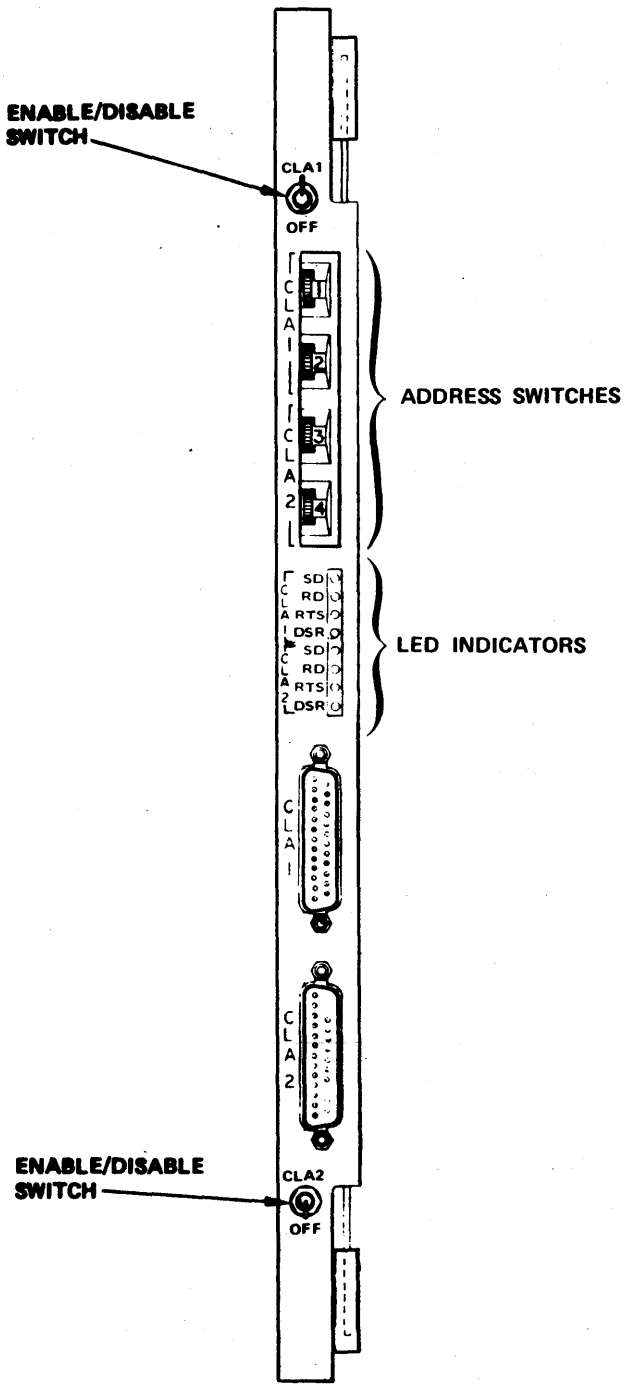


Figure 2-1. Controls and Indicators, ACLA Card Handle

MULTIPLEXING SUBSYSTEM OVERVIEW

The processor communicates with a CLA via the multiplex loop. The multiplex loop consists of two independent loops, the input loop and the output loop. The input loop carries output data demands, input data, and supervision (status) from the ACLA to the processor. The output loop carries output data and supervision (commands) from the processor to the ACLA.

Information is transferred serially bit by bit on the loops. Loop cell structure is shown in figure 2-2. Every twelfth bit is a cell frame marker that defines a 12-bit loop cell. The cell frame marker is followed by a cell identification field (three bits), which defines the contents of the remaining field (8 bits) of the cell. The loop multiplexer receives information from the output loop and presents the cells in parallel form to the CLA (an 11-bit interface is used; the cell frame marker bit is deleted). Similarly, the ACLA transfers cells (11 bits) to the loop multiplexer, which presents them serially (and adds the cell frame marker bit) to the input loop.

A line frame is a group of contiguous loop cells related to a particular ACLA. The first cell of a line frame contains the address of the CLA and the last cell contains a cyclic redundancy check (CRC) character. Other cells within the frame may contain data and/or supervision (status or commands). All cells are passed unmodified between the multiplex loop and the CLA, except the check character which is removed from the output loop and added to the input loop by the loop multiplexer.

LINE FRAME FORMATS

The ACLA uses the following general line frame format on the input loop:

ACLA Address	Input Data	Status Word 1	Status Word 2	CRC Character

The ACLA address cell is always present and may contain an active output data demand bit. The data cell may appear next and contains input data. Two supervision cells may also follow and contain status word 1 and status word 2. If any status is to be reported, both status words always appear. The CRC (cyclic redundancy check) character is added by the loop multiplexer and does not concern the ACLA.

The following general line frame format is required by the ACLA on the output loop:

ACLA Address	Output Data	Command Word 1	Command Word 2	CRC Character

TABLE 2-2. CELL FRAME FORMATS

Word/Field Type	Bit Position												Flow
Processor Word	11	10	9	8	7	6	5	4	3	2	1	0	
LM Cell	0	1	2	3	4	5	6	7	8	9	10	11	
Information Field	X				I1	I2	I3	I4	I5	I6	I7	I8	
Identification Field	X	F1	F2	F3									
Address ID Field	X	1	1	†	← Address →								LM ↔ ACLA
Data ID Field	X	1	0	0	← Data →								LM ↔ ACLA
Status ID Field	X	1	0	1	← Status →								ACLA → LM
Command ID Field	X	1	0	1	← Command →								LM → ACLA

†This bit is the output data demand (ODD) during an address transfer to the LM.

TABLE 2-3. ADDRESSING CODE FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
ACLA to LM Interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
Bit Content		1	1	0/1	A1	A2	A3	A4	A5	A6	A7	A8

TABLE 2-4. DATA CELL FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
ACLA to LM Interface		IF1	IF2	IF3	II1	II2	II3	II4	II5	II6	II7	II8
8- or 9-bit† character		1	0	0	D8	D7	D6	D5	D4	D3	D2	D1
7-bit character		1	0	0	0	D7	D6	D5	D4	D3	D2	D1
6-bit character		1	0	0	0	0	D6	D5	D4	D3	D2	D1
5-bit character		1	0	0	0	0	0	D5	D4	D3	D2	D1

†For a 9-bit character the additional bit is a parity check bit. This is handled internally and does not appear at the ACLA/LM interface; consequently, only 8 bits are shown in this table.

STATUS WORDS

Most status changes, error conditions, or a status request command cause status to be reported, and two characters are sent to the processor. The status word 1 and status word 2 formats are shown in tables 2-5 and 2-6, respectively. In both tables a logic 1 indicates that the associated modem signal or status condition is active (on), and a logic 0 indicates that the condition is not active (off).

COMMAND WORDS

The command words are instructions from the processor in the form of command words 1, 2, 3 and 4, which must be received in sequence. For example, words 1 and 2 must be received before word 3, and word 2 must always be preceded by command word 1. However, command word 1 can be received as a single word command. Formats for command word 1 and command word 2 are shown in tables 2-7 and 2-8. A logic 1, in the position indicated, activates the associated signal, while a logic 0 deactivates the signal. The commands operate independently of each other.

TABLE 2-7. COMMAND WORD 1 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit Content		1	0	1	RTS	SRTS	OM	LMA	DTR	TB	ION	OON

RTS - Request-to-send. A logic 1 here activates the request-to-send line to the modem while a logic 0 deactivates RTS.

SRTS - Secondary request-to-send. A logic 1 activates the secondary request-to-send line to the modem (referred to as secondary send-data on some modems). On modems equipped with a reverse channel transmitter, supervisory information can be sent to a remote station while the ACLA is receiving data from the station over a half-duplex, 2-wire circuit. Typical uses include circuit assurance, error control, and interrupt (break). A logic 0 deactivates SRTS.

OM - Originate mode/auxiliary. A logic 1 in this position causes the ACLA to notify the modem equipment that it is in the originate mode. A logic 0 indicates answer mode. This line is an auxiliary signal line and may be used for other functions as designated by system design.

LMA - Local mode/auxiliary. A logic 1 in this position causes the ACLA to notify the modem (when equipped) to loop back the analog signal on the modem. A logic 0 disables the loopback. This line is an auxiliary signal line and may be used for other functions as designated by system design.

DTR - Data-terminal-ready. A logic 1 in this location causes the ACLA to notify the modem that the system is ready to communicate with the modem. A logic 0 causes a not-ready signal to be reported.

TB - Terminal-busy. A logic 1 causes the ACLA to notify the modem to busy-out-the-line. A logic 0 disables this function.

ION - Input-on. When this bit is a logic 0, the input section of the ACLA cannot receive data characters nor transfer data to the LM. A logic 1 causes normal input operation.

OON - Output-on. A logic 1 causes the output section of the ACLA to report output-data-demand initially when command is received if clear-to-send is active, and enables the output to report output-data-demand whenever the output buffer is empty. A logic 0 inhibits reporting of output-data-demand.

TABLE 2-8. COMMAND WORD 2 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit Content		1	0	1	BREAK	ISR	ISON	DLM	RSR1	RSR2	TSR1	TSR2

BREAK - Break-mode. A logic 1 here causes the ACLA to place the transmit-data line in a spacing condition (0 state). A logic 0 inhibits the break operation and returns the line to marking condition (1 state).

ISR - Input-status-report. A logic 1 in this position causes the ACLA to report the status of the RS-232 interface lines and any other ACLA status that may be active once each time the command is received. The ISR command is honored only when the ACLA has previously received a logic 1 in the ISON position. This is a momentary nonstored command. (If ISR is a 1 and ISON is a 1 in the same line frame, status is reported.)

ISON - Input-status-on. When a logic 1 is in this bit position, the ACLA monitors the modem interface and reports input supervision. A logic 0 inhibits monitoring and reporting. Status is not reported automatically when this command bit is first received by the ACLA. The ACLA must receive either an ISR command or status change to report input supervision.

DLM - Data-line-monitor. A logic 1 here causes the ACLA to monitor the receive-data line that is in a break condition for one character time after reception of the command. This command is used to allow the processor to determine the length of a break condition on data input. This is a momentary, nonstored command.

RSR1, RSR2 - Receive-speed-range 1 and 2. This code causes the ACLA to select a reference frequency from the LM to provide a range of baud rates selectable by bits IO1 thru IO4 in command word 4. See table 2-9.

TSR1, TSR2 - Transmit-speed-range 1 and 2. This code causes the ACLA to select a frequency from the LM to provide a range of transmit baud rates selectable by bits IO5 thru IO8 in command word 4. Table 2-9 shows the code and related reference frequencies.

TABLE 2-10. COMMON BAUD RATES AND COMMAND CODES

Baud Rate	Speed - Command Word 4								Range - Command Word 2				
	Input				Output				Freq Desig	Input		Output	
	I1	I2	I3	I4	I5	I6	I7	I8		I5	I6	I7	I8
9600	1	1	1	1	1	1	1	1	C	0	1	0	1
7200 (Special)	1	1	1	1	1	1	1	1	D	1	1	1	1
4800	0	1	1	1	0	1	1	1	C	0	1	0	1
3600 (Special)	0	1	1	1	0	1	1	1	D	1	1	1	1
2400	0	0	1	1	0	0	1	1	C	0	1	0	1
1800 (Special)	0	0	1	1	0	0	1	1	D	1	1	1	1
1600	0	1	0	1	0	1	0	1	C	0	1	0	1
1200	0	0	0	1	0	0	0	1	C	0	1	0	1
1050	1	1	1	0	1	1	1	0	C	0	1	0	1
800	0	0	1	0	0	0	1	0	C	0	1	0	1
600	0	1	1	1	0	1	1	1	B	1	0	1	0
300	0	0	1	1	0	0	1	1	B	1	0	1	0
150	0	0	0	1	0	0	0	1	B	1	0	1	0
133.3	1	1	1	0	1	1	1	0	B	1	0	1	0
120	0	1	1	0	0	1	1	0	B	1	0	1	0
110	1	0	1	0	1	0	1	0	B	1	0	1	0
100	0	0	1	0	0	0	1	0	B	1	0	1	0
75	0	0	0	0	0	0	0	0	B	1	0	1	0
66.67	1	1	1	0	1	1	1	0	A	0	0	0	0
50.0	0	0	1	0	0	0	1	0	A	0	0	0	0

TABLE 2-11. COMMAND WORD 3 FORMAT

Loop Cell Bit Position	B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11
LM to ACLA Interface		OF1	OF2	OF3	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8
Bit Content		1	0	1	PSET	PI	CO1	CO2	SB		ECHO	LIT

PSET - Parity-set. When B4 is a logic 1, concurrent with PI set to a logic 0, the ACLA generates and checks for even parity. A logic 0 concurrent with PI set to a logic 0 causes the ACLA to generate and check for odd character parity.

PI - Parity-inhibit. When B5 is a logic 0, the ACLA checks character parity on input and generates character parity on output. A logic 1 causes the ACLA to ignore parity.

CO1, CO2 - Code 1 and Code 2 bits form a code so that each combination corresponds to a character length of either 5, 6, 7 or 8 bits. The checking and generation of character parity adds one information bit to the character and therefore must be considered when selecting the unit code. Table 2-12 shows these code bits in relation to parity-inhibit bit.

SB - Stop-bit. A logic 1 in B8 position causes the output logic to generate two stop bits (For 5 data bits, the stop bit is 1.5 units in length.) on output and a logic 0 generates one stop bit.

ECHO - Echoplex mode. A logic 1 in this position causes the ACLA to return all data received from the modem on the receive-data line back to the modem on the send-data line while maintaining normal data processing in the input logic. A logic 0 inhibits echoplex operation.

LIT - Loop-internal-test. A logic 1 in this position causes the ACLA to go into an echoplex mode. Data and modem control signals from the output section are routed (looped back) to the input section. Refer to Programming Notes for additional information on this mode of operation. A logic 0 disables the echoplex mode.

output to avoid receiving back the message transmitted.

OUTPUT OPERATION

To transmit data, output-on (OON) command must be activated. Also, request-to-send (RTS) must be turned on if not so conditioned previously. When the modem is ready to transmit data, it returns clear-to-send (CTS) signal, which causes the ACLA to generate the first output-data-demand (ODD) and to report CTS status.

When the program receives an ODD, it should return a character to the ACLA. Each time that the ACLA transfers a character from its buffer register to the shift (disassembly) register, it generates an ODD. This sequence is repeated until the last character of the message is transmitted. RTS can be deactivated one character time (or more, depending on the modem type) after the generation of the last ODD.

LOOPBACK TEST OPERATION

To operate in loopback test mode, the loop internal test (LIT) command must be sent to the ACLA. Data and modem control signals from the output section are routed (looped back) to the input section as follows:

1. Transmit-data (TD) is connected to receive-data (RD).
2. Request-to-send is connected to clear-to-send.
3. Data-terminal-ready is connected to data-set-ready.
4. Local-mode is connected to data-carrier-detector (receive-line-signal-detector).
5. Secondary request-to-send is connected to secondary-data-carrier detector (secondary-receive-line-signal-detector).
6. Terminal-busy connects to ring-indicator.

While in this mode, all signals received from the modem are blocked and ignored by the ACLA. However, on the output side, signals to the modem are not blocked and caution must be used while in loopback test mode to avoid undesirable operation of the modem. For instance, while testing the operation of data-terminal-ready, an on condition is being received by the modem as well as being looped back as in item 3 above. If an incoming call was received in this situation, the modem would answer; this may confuse the calling station since no data transfer would occur. Therefore, DTR should only be turned on momentarily to test its operation and left off during other ACLA tests.

BREAK/OPEN-LINE DETECTION

Break (one or more character times of a spacing) or open-line (continuous spacing) conditions on the receive-data line can be detected by use of framing-error-status (FES) and the data-line-monitor (DLM) command. When a character is received without a stop bit (spacing or logic 0 condition detected when receive-data line is sampled for first stop bit), FES is reported in conjunction with the character. Following detection of a framing error, the ACLA locks up and is not in a condition to assemble additional characters until it sees a space-to-mark transition on the receive-data line or a data-line-monitor command. The program must issue a DLM command each time it receives FES to cause the ACLA to monitor the receive-data line for another character time. The program detects a break condition by the receipt of one or more (the exact number is established by software) consecutive null (all zero) characters accompanied by FES. Once a break or open-line condition has been determined to exist, the program may periodically interrogate the state of the line by issuing a DLM command. If the line remains in a spacing condition, the DLM command causes a null character to be assembled and FES reported. If the line has returned to a marking condition, the DLM command has no effect.

The ACLA monitors for framing errors at all times. It transfers the character received and reports FES whenever the ISON command is active, independent of the state of the ION command. Thus, break detection is possible while the ACLA is transmitting to a remote station even though the input section may be disabled (ION off).

RESTRAINT DETECTOR

For operation on the TWX network, the local modem may occasionally signal the ACLA to suspend data transmission. This condition may occur when the ACLA can transmit data to the TWX central office faster than the central office can convert the data and transmit it on to the appropriate station. The ACLA simply inhibits generation of ODDs while the restraint-detection signal is active, the net effect on software being a momentary delay in receipt of ODDs.

TABLE 3-1. CABLES USED WITH DU137-A ACLA

Equipment Number	Part Number	Application	Connector to Modem/Terminal	Connector to ACLA
XA133-A YA228-A	74657700 74875756†	Compatible with AT&T 103/113 Data Sets	25-contact plug	25-contact receptacle
XA135-A YA230-A	74657900 74875846†	Connects directly to terminal without a modem. Compatible with any terminal with RS-232-C interface capable of operating AT&T 103/113 or 202 Data Sets.	25-contact receptacle with threaded retaining spacers	25-contact receptacle
XA134-A YA229-A	74658300 74875760†	Compatible with AT&T 103F, 202R Data Sets or CDC telegraphic level converter	25-contact plug	25-contact receptacle
XA229-A†† YA234-A††	74874002 74876194†	Compatible with AT&T 202 Data Sets with reverse channel option	25-contact plug	25-contact receptacle

†Used with B version cabinets
††Special application

TABLE 3-2. DU189-A/B, DU190-A/B, and DU191-A/B Cable Sets

Equipment Number	Part Number		
	ACLA Card†	Cable	
DU189-A	74872129	74657700	Compatible with AT&T 103/113 Data Sets
DU189-B ††	74872129	74875756	
DU190-A	74872129	74657900	Compatible with any RS-232-C interface capable of operating AT&T 103/113/203 Data Sets. Connects directly to a terminal without a modem.
DU190-B ††	74872129	74875846	
DU191-A	74872129	74658300	Compatible with AT&T 103F/202R Data Sets or CDC telegraphic level converter.
DU191-B ††	74872129	74875760	

†ACLA card, PN 74872129, is interchangeable with DU137-A ACLA, PN 74447001.
††Used with B version cabinet.

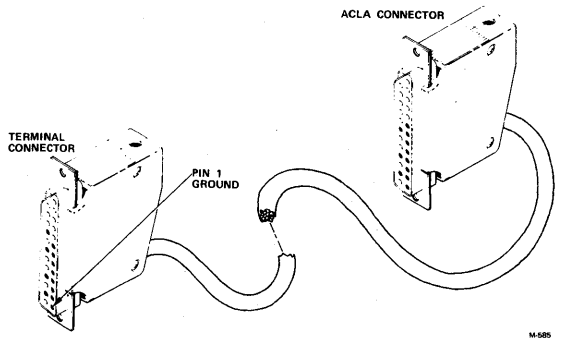


Figure 3-1. Typical ACLA Cable Connectors

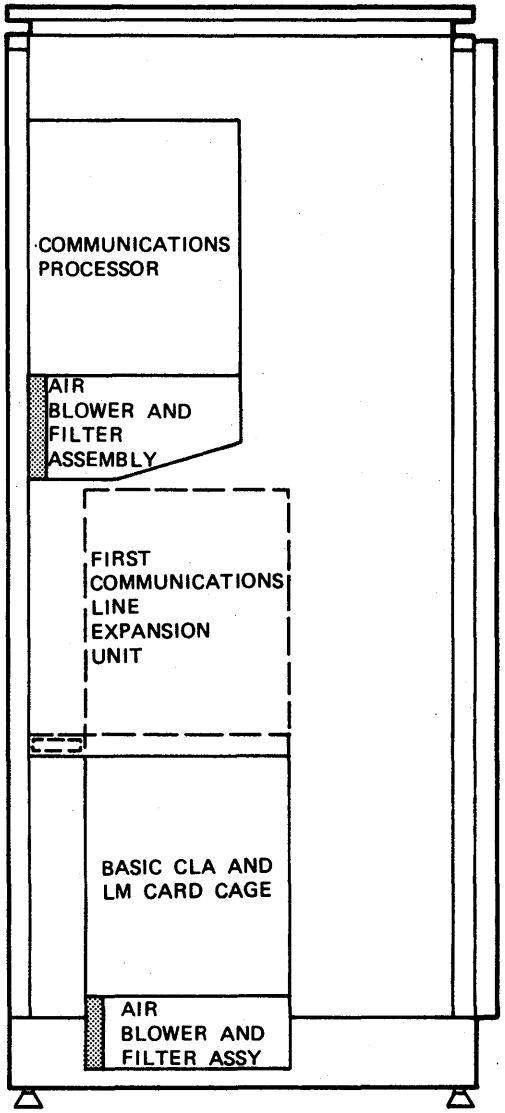


Figure 3-2. Component Location, Basic NPU Cabinet, Side View

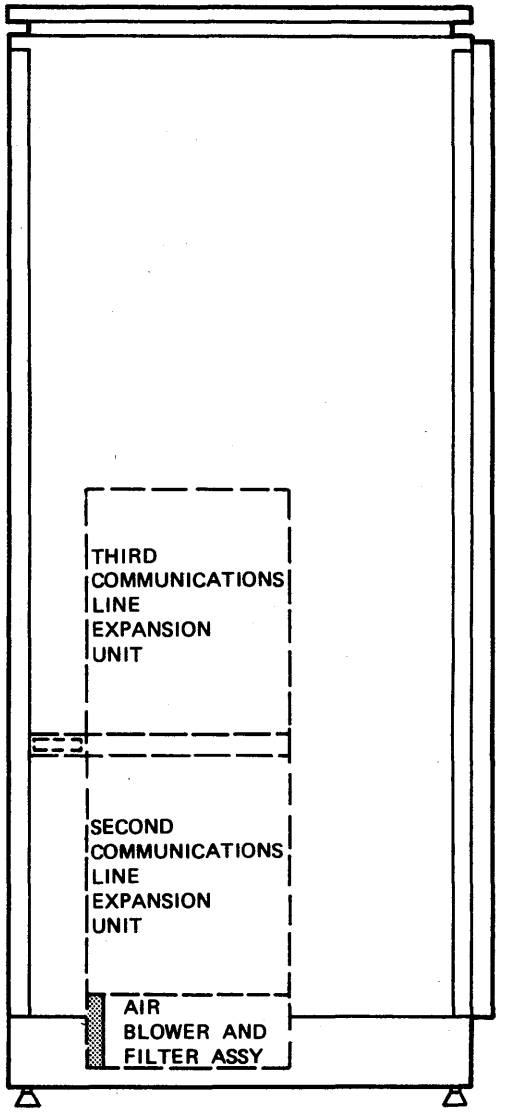


Figure 3-3. Component Location, Stand-Alone Cabinet, Side View

CAUTION

Do not attempt to install an ACLA card in the communications processor card cage, located at the top of the basic cabinet. If attempted, the communications processor backplane will be damaged.

1. Set CLA1 and CLA2 enable/disable switches to OFF.

2. Position card vertically so that connector on card handle is on lower part and thumbwheel switches are on upper part.

3. If system is operating, set thumbwheel address switches on card handle to the proper hexadecimal address before installing ACLA card. Refer to Controls and Indicators, section 2, for method of setting an address.

CAUTION

Ensure that 51-pin tab connectors on rear edge of card are properly aligned with their mating connectors on card cage backplane. Cross-slotting will destroy the backplane.

4. Insert rear edge of card into slotted guides, making certain that card is perfectly vertical and not cross-slotted.

5. Slide card into card cage, applying firm pressure on card handle to engage connectors on card with backplane connectors. All card handles will be flush with one another when cards are correctly installed.

6. Position blank slot covers in all card slots that are not used to assure that blower air flow is contained in card cage.

7. Set thumbwheel address switches on card handle. Refer to Controls and Indicators, section 2, for the method of setting an address.

8. Set enable switches to CLA1 and CLA2 (enable) positions.

CABLE INSTALLATION

ACLA cables are installed as follows:

1. Select a cable that is compatible with terminal or modem to be connected to ACLA. Refer to the cable indentification.

2. Attach cable to terminal or modem, then attach the other end of cables to the ACLA card handle. All cables exit through bottom of cabinet. In the B version cabinets, cables are routed through cable grounding assembly located at bottom of cabinet. See figure 3-5. For ACLAs installed in upper expansion position of cabinets, route cables through cable tray provided on either side and then down along the side to bottom of cabinet.

3. Tighten down retaining screws on all cable connectors. Apply pressure to grounding clamp (B version) and tighten screws.

4. Lay out surplus length of cable in a long, flat loop under the raised floor or in enclosures; this manner of storage minimizes kinking of cables.

5. Place protection padding, if available, over stored loops of cable before installing flooring.

INITIAL CHECKOUT

After all ACLA cards are installed and connected, diagnostic or system programs can be used to determine overall ACLA function.

If a fault is isolated to the ACLA, the following mechanical checks may be made:

1. Check that enable switch of ACLA in question is in the on (up) position.

2. Check that ACLA cable connectors are firmly attached.

3. Ensure card is firmly placed in card slot.

4. Monitor LED indicators under ACLA card handle to ensure electrical power is on ACLA card.

5. If LED indicators are not lit on the ACLA card, check LED indicators on LM card handle to ensure power is available to card cage.

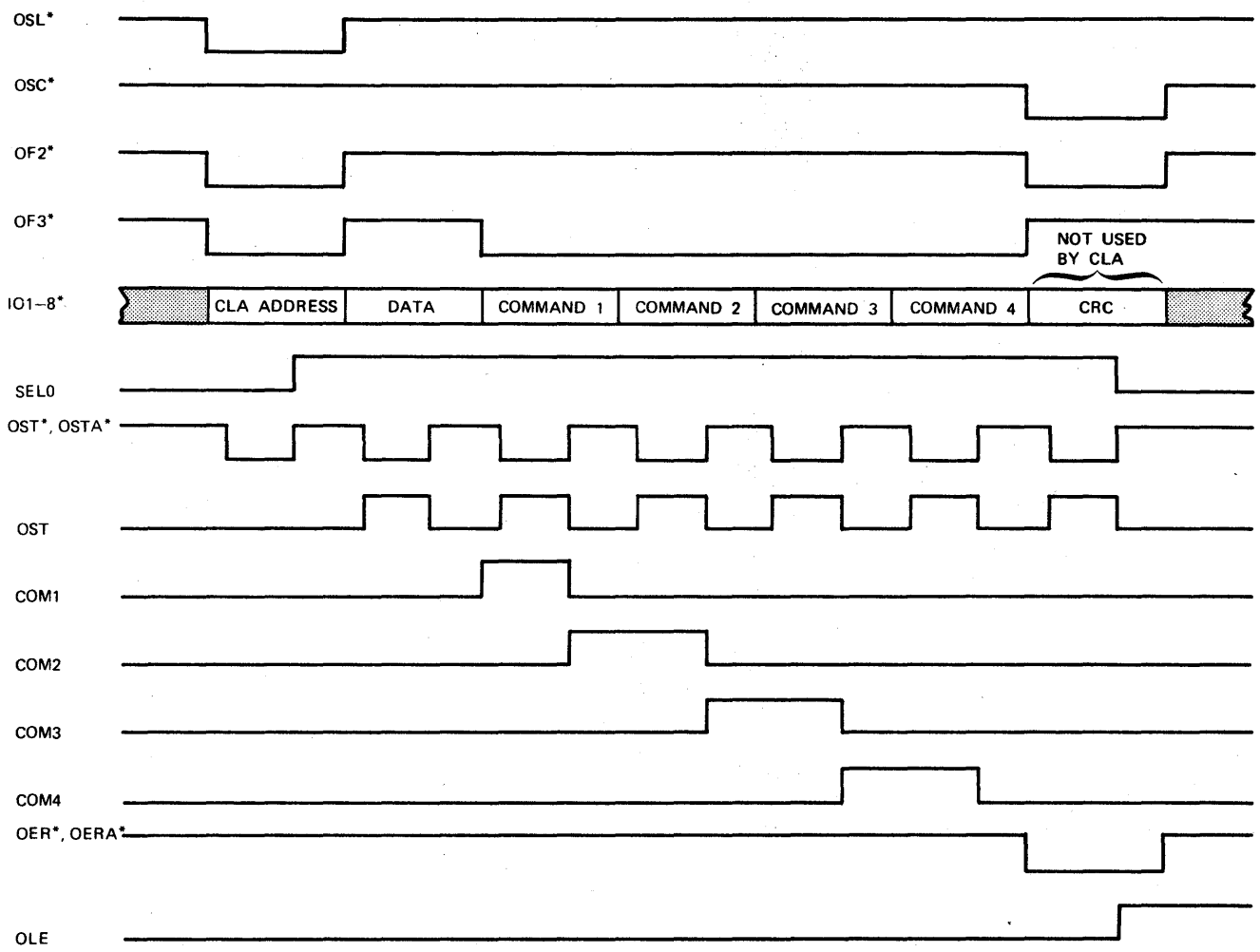


Figure 4-1. Loop Multiplexer-to-ACLA Interface and Command Timing Diagram

COMMAND REGISTERS

All commands are strobed into their associated registers with either COM1, COM2, COM3, or COM4, and OST. The command 1 register stores all of the modem control signals plus output-on (OON) and input-on (ION). It is implemented with two 4-bit parallel-load shift registers. COM1 enables parallel-entry, and on the falling edge of OST the registers are loaded with the information output IO1 thru IO8 bits present at their inputs. Break, input-status-on (ISON), receiver shift register, and transmitter shift register (RSR1, RSR2, TSR1, and TSR2) of the second command are stored in the same type of register in a like manner with COM2 and on the falling edge of OST. Also, the echo and loop-internal-test (LIT) commands of command 3 and all the speed generator divider bits of command 4 are stored in the same manner on the falling edge of OST and COM3 and COM4, respectively. The PSET, PI, CO1, CO2 and SB (stop bit) commands of command 3 are strobed into the control register of the UART with the rising edge of OST if COM3 is active. The data-line-monitor (DLM) and input-status-report (ISR) commands of command 2 are non-stored commands having an active duration equal to the pulse width of OST (300 nanoseconds with a 20-mHz loop).

UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

The universal asynchronous receiver/transmitter (UART), a large-scale integration (LSI) package, is the main functional element in the ACLA. The transmitter section converts parallel data into a serial word which contains the data along with start, parity, and stop bits. The receiver section converts a serial word with start, parity, and stop bits into parallel data and verifies proper code transmission by checking the receipt of a valid stop bit and proper parity if selected for parity.

The UART is programmable as to word length (5, 6, 7 or 8 bits), parity (even, odd, or parity inhibited) and the number of stop bits (normally 1 or 2 bits, but 1-1/2 bits with a 5-unit code). The transmitter and receiver share the control register and thus are configured in the same manner.

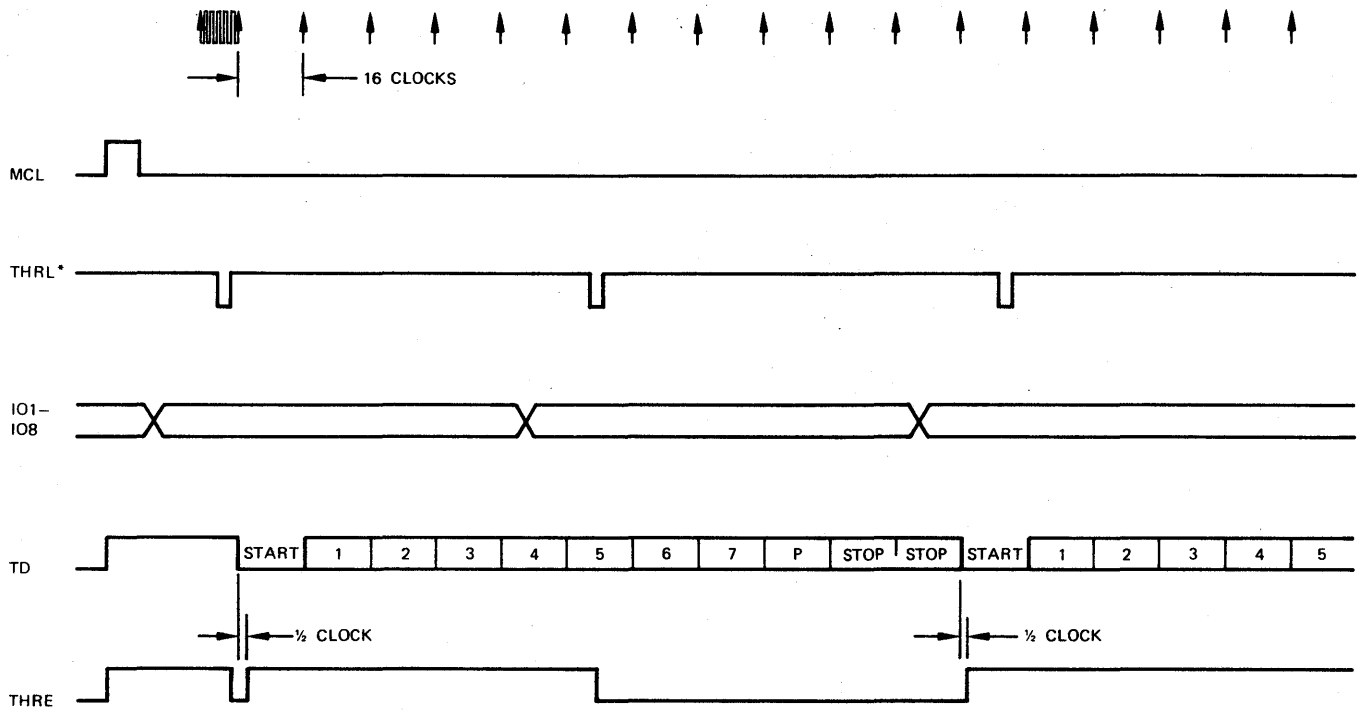


Figure 4-3. UART Transmitter Timing Diagram

If the UART is programmed to detect parity errors (even or odd) and a character is received with a parity error, the parity-error-status line is set to a logic 1 at the nominal center of the last stop bit. This signal is held until the next character is transferred to the RHR.

If the first stop bit is not a marking condition, the framing-error-status line (FES) is set to a logic 1 and held until the next character is transferred to the RHR. If the cause of FES is the receipt of a break character (null character without stop bits), the receiver is in a locked-up state so that the IBF does not set to a logic 1 until at least one character time has elapsed after a valid stop bit has been detected.

The timing for all receiver functions is obtained from the external receive clock (RCK) whose frequency is 16 times the desired baud rate. When the master clear line is strobed to a logic 1, the UART is set to an idle state. This resets TSR, RSR, RHR, FES, DTOS, PES and IBF, and sets TD and THRE.

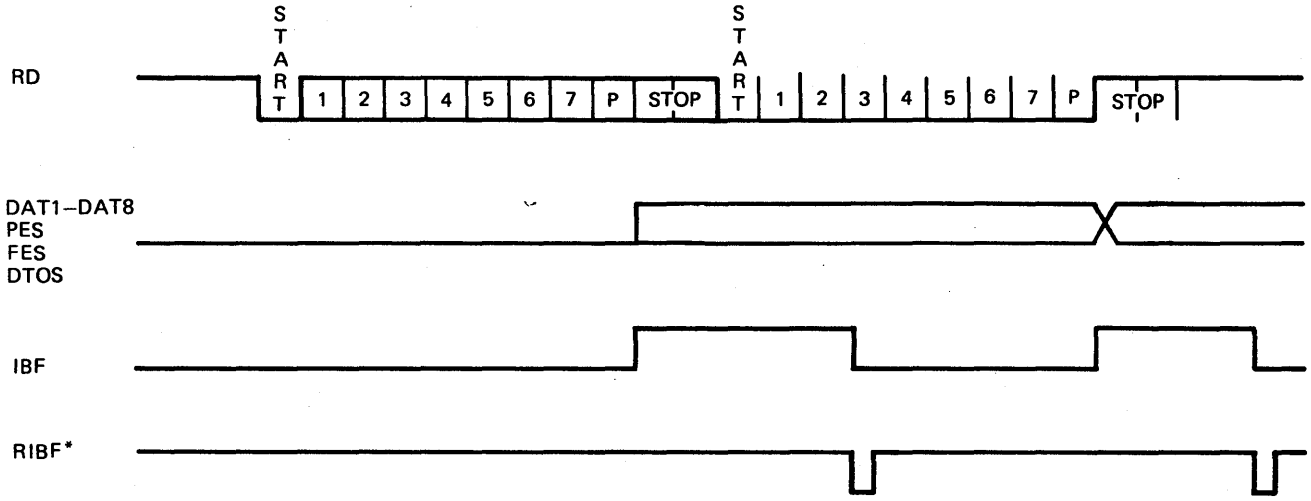
OUTPUT DATA DEMAND

When the ACLA is able to accept a character from the LM, it sets the output-data-demand (ODD) flip-flop, which in turn causes IAV to activate. The ACLA address with the ODD flag bit set is picked up by the LM when the ACLA's input section is selected. The ODD flip-flop is reset during this selection. The processor, responding to the ODD, provides a data character to the output section of the ACLA via the LM.

The setting of the ODD flip-flop is controlled by four signals: ODD, THRE, restraint-detector* (RSD*), and clear-to-send status (CTSS). These signals are ANDed together to produce the clock for the ODD flip-flop. Since the D input is pulled up, the ODD flip-flop is set whenever three of the signals are logic 1 and the fourth makes a logic 0-to-1 transition. The resetting of the ODD flip-flop is discussed in the input section. Normally THRE triggers the ODD flip-flop.

OUTPUT DATA

After receipt of an ODD from the ACLA, the processor sends a character via the LM to the output section of the ACLA. SELO sets to 1 when the ACLA's address is detected by the ACLA. After the address is presented, the next word may be a data character, in which case the data format code is detected by the format decoder, making ODATA a logic 1. The data character present on bits IO1 thru IO8 is loaded into the transmitter holding register of the UART with



DETAIL:

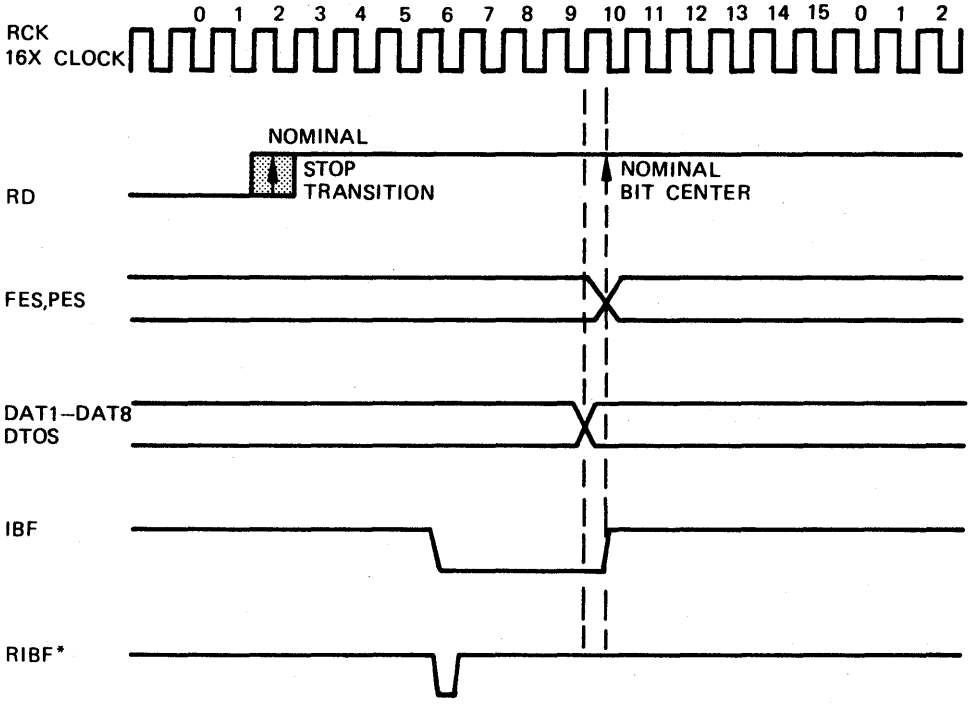


Figure 4-5. UART Receiver Timing Diagram

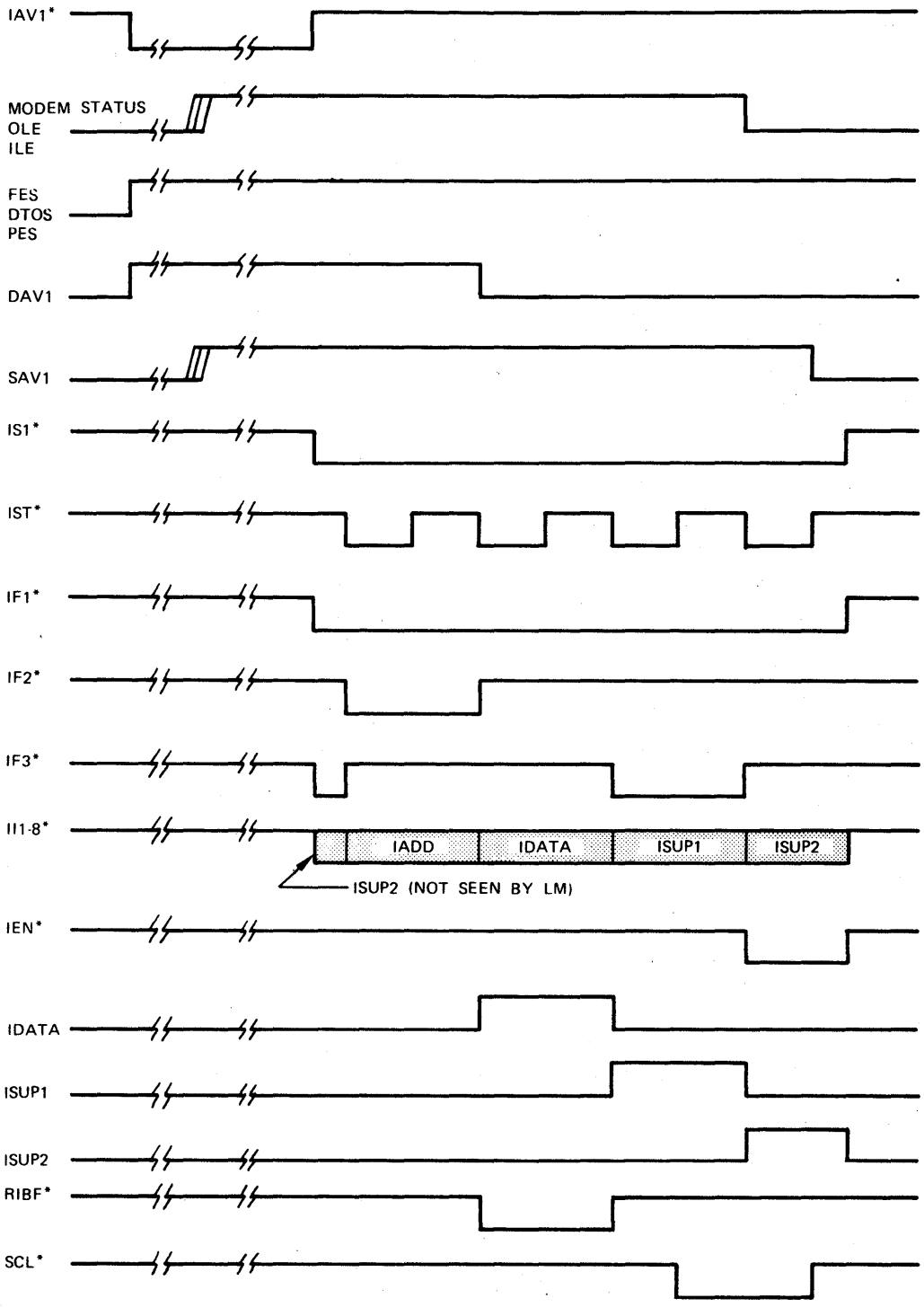


Figure 4-7. Input Control (ODD, DATA, SUPV) Timing Diagram

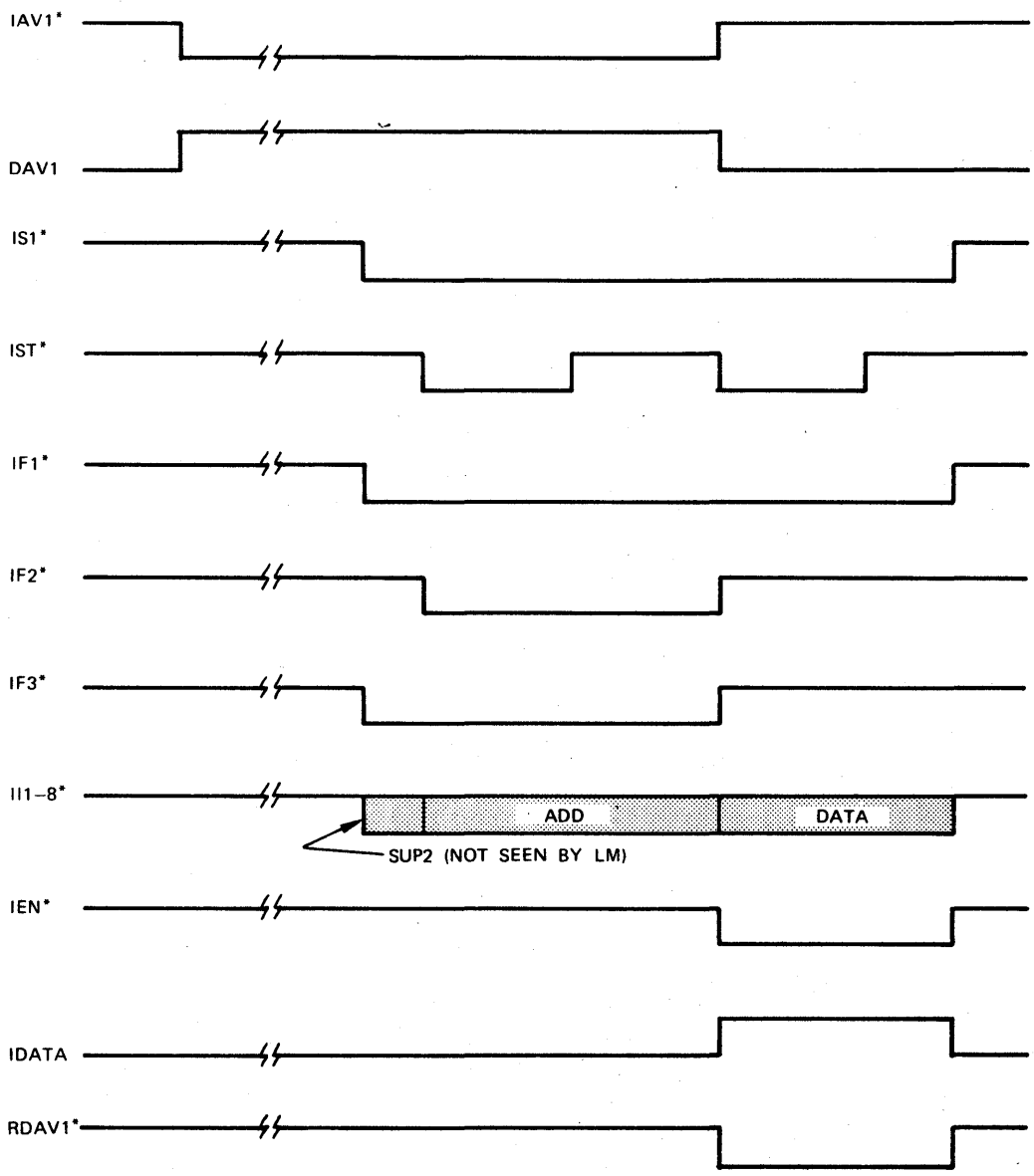


Figure 4-9. Input Control (DATA only) Timing Diagram

INPUT CONTROL STATES

The input control states are defined as follows:

State 0 is IADD, i.e., ACLA address with or without ODD bit is placed on the input bus;

state 1 is IDATA, i.e., data serially received from the communications line is placed in parallel on the input bus;

state 2 is ISUP1, i.e., the first status word is placed on the input bus;

and state 3 is ISUP2, i.e., the second status word is placed on the input bus.

INPUT MULTIPLEXER

The input multiplexer is used by both ACLA1 and ACLA2. It provides a 3-state interface with the LM input bus for the signals of IF2*, IF3* (input format) and II1* thru II8*. IF1* is activated by an open collector gate whenever SELI is a logic 1.

The input multiplexer is controlled by the signals SELI2*, SELI*, IC1 and IC2 of the input control logic. Eight 8-to-1 multiplexer integrated circuits make up the input multiplexer, the outputs of which are connected to the LM input bus lines of II1 thru II8. Address, data, and supervision bits from ACLA1 and ACLA2 are applied to the respective inputs of each multiplexer in such a way that the proper word is selected for transfer to the LM.

The signals SELI2*, IC1, and IC2 dictate which of the possible words are selected. SELI* enables the 3-state outputs of the multiplexers, i.e., if IC1 is logic 1, IC2 is logic 0 and SELI2 is logic 0, then receive data bits DAT1 thru DAT8 of ACLA1 appear at II1 thru II8, respectively.

Input format bits 2 and 3 (IF2, IF3) are produced by the outputs of two 4-to-1, 3-state multiplexers. These multiplexers are controlled by the signals of SELI*, IC1 and IC2. SELI* enables the 3-state outputs, while IC1 and IC2 place the proper format code on the bus. All of the multiplexed inputs are "hard-wired" except the ODD flag bit which is connected to ODD*.

INPUT LOOP ERROR

Whenever the multiplex loop interface adapter detects an input loop error during a loop batch, it notifies the LM via a restart loop end. If the ACLA used the last input loop batch, the LM activates the IER line and the IS line and provides one IST. When both IER and IS are logic 1, a low level is applied to the D input of the input loop error status (ILES) flip-flop. On the trailing edge of IST, the ILES flip-flop is clocked, thus storing the error condition. The ILES* signal sets the status R/W (if input-status-on is logic 1), which in turn activates the input available. ILES is picked up by the LM in ISUP1. The ILES flip-flop is reset when the status clear signal makes a logic 0-to-1 transition. The SCL signal is produced by a flip-flop which is set by the trailing edge of IST while in the input control state of ISUP1 and reset on the next trailing edge of IST.

CHARACTER ASSEMBLY

Before the ACLA can receive data from the communications line and transfer it to the LM, it must be programmed via the ACLA output section. It must be programmed to the proper character length and even or odd parity and programmed to enable the input section (ION is a logic 1).

After level conversion by the modem interface section, the receive-data signal is fed to the receive section of the UART. The UART monitors this signal for a start bit which begins the processing of the character as shown in the discussion of the UART. In the center of the first stop bit, the UART transfers the character to its receive holding register so that the character is present on DAT1 thru DAT8 and raises its input-buffer-full flag (IBF). ION is NANDed with IBF to activate input available. IBF is reset with reset-input-buffer-full (RIBF*), which is produced by the NANDing of IBF, SELI, IC1, and IC2.

The resetting occurs during the time that the LM picks up the data word. The preceding is the normal resetting procedure for IBF, but it is also reset when ION goes from the 0-to-1 condition by the NANDing of ION*, IO7, COM1, and OST.

When assembling characters, if IBF is not reset by the time that another character is transferred to the receive holding register, the data-transfer-overrun status (DTOS) flag sets to a logic 1. This signal is applied to the input multiplexer and accessed by the LM in the first status word. DTOS is reset on the first end of the next received character after the resetting of IBF. End of character is in the center of the first stop bit of the received character.

If the received data is in a spacing condition during the first stop bit of a received character, the framing error status (FES) flag of the UART sets to a logic 1 at the bit center of that stop bit. FES and IBF applied to an A-O-I gate set the status R/W, if ISON is logic 1. ISON also allows DAV to activate, which in turn allows data and status to be reported to the LM. This occurs regardless of the state of ION. This function facilitates the detection of a breaking condition: FES, reported to the LM in the same line frame as a data character of spacing, is interpreted by the

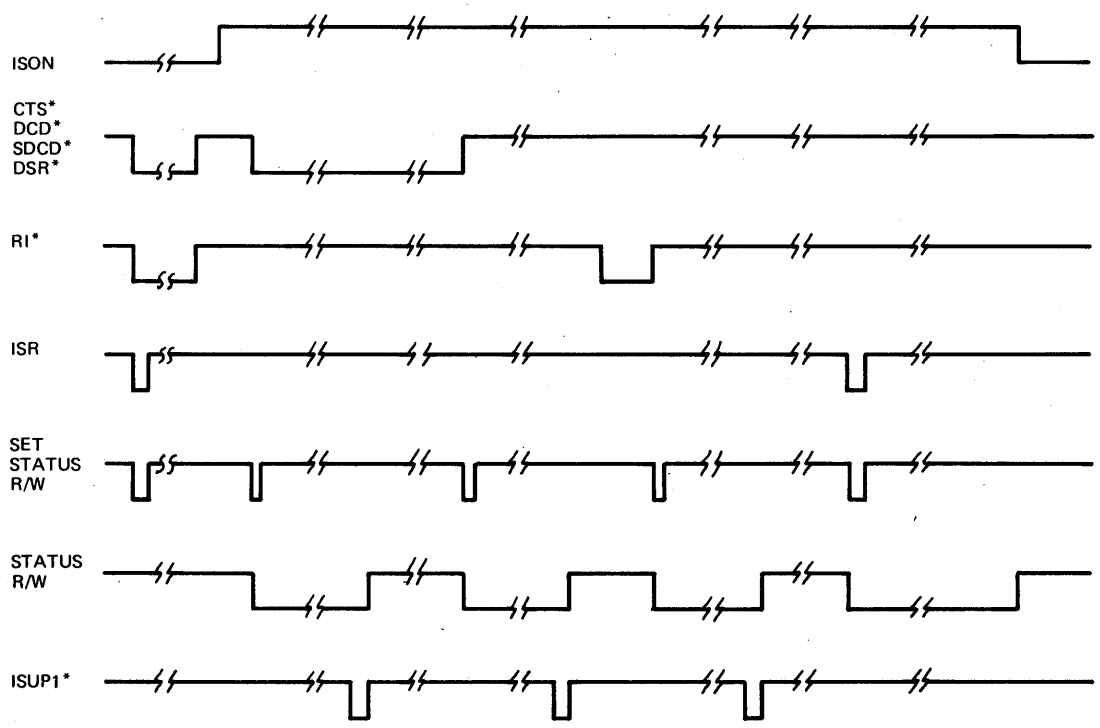


Figure 4-11. Modem Interface Timing Diagram

RING INDICATOR STATUS

Ring indicator status (RIS) is stored in a flip-flop. A logic 1-to-0 transition of ring indicator causes the status R/W to set. The setting of the status R/W causes the RIS flip-flop to be clocked to a logic 1. The next time the status R/W is set, if not caused by the toggling of the ring indicator (RI), the RIS flip-flop is clocked to a logic 0. The RI detection logic consists of an exclusive OR gate, a NAND gate, an inverter, the RIS flip-flop and a delay network. When the RI line goes to a logic 1, a low level is applied to the resistor-capacitor network, causing the capacitor to discharge through the resistor until the level across the capacitor reaches ground potential. The inputs to the RIS flip-flop are armed with a high level. When RI makes a logic 1-to-0 transition, the output of the NAND gate goes low, thereby setting the status R/W. The high level on the inputs to the RIS flip-flop is clocked into the RIS flip-flop by the setting of the status R/W. This level goes low 200 to 400 nanoseconds afterwards, then the capacitor charges to the turn-on voltage of the exclusive OR gate.

STATUS READ/WRITE

The status R/W is reset when the ACLA puts the second status word on the LM input bus. Since ISON is applied to the direct reset of the status R/W, this status is inhibited from setting when ISON is logic 0.

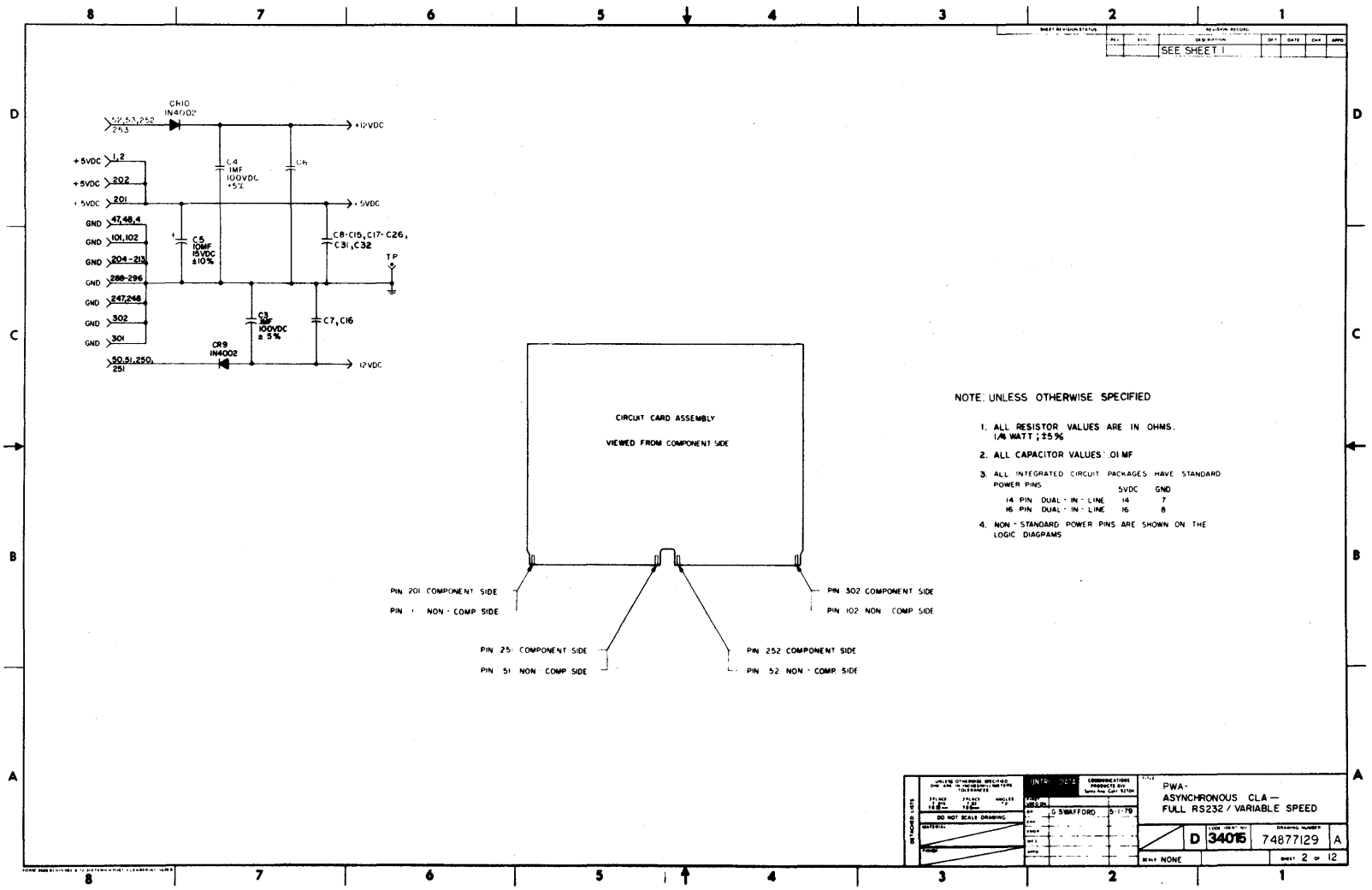
The status R/W can be set with any of the following eight signals: data-associated-status, input-loop-error, output-loop-error, or one of the five ouputs of the change detection circuit.

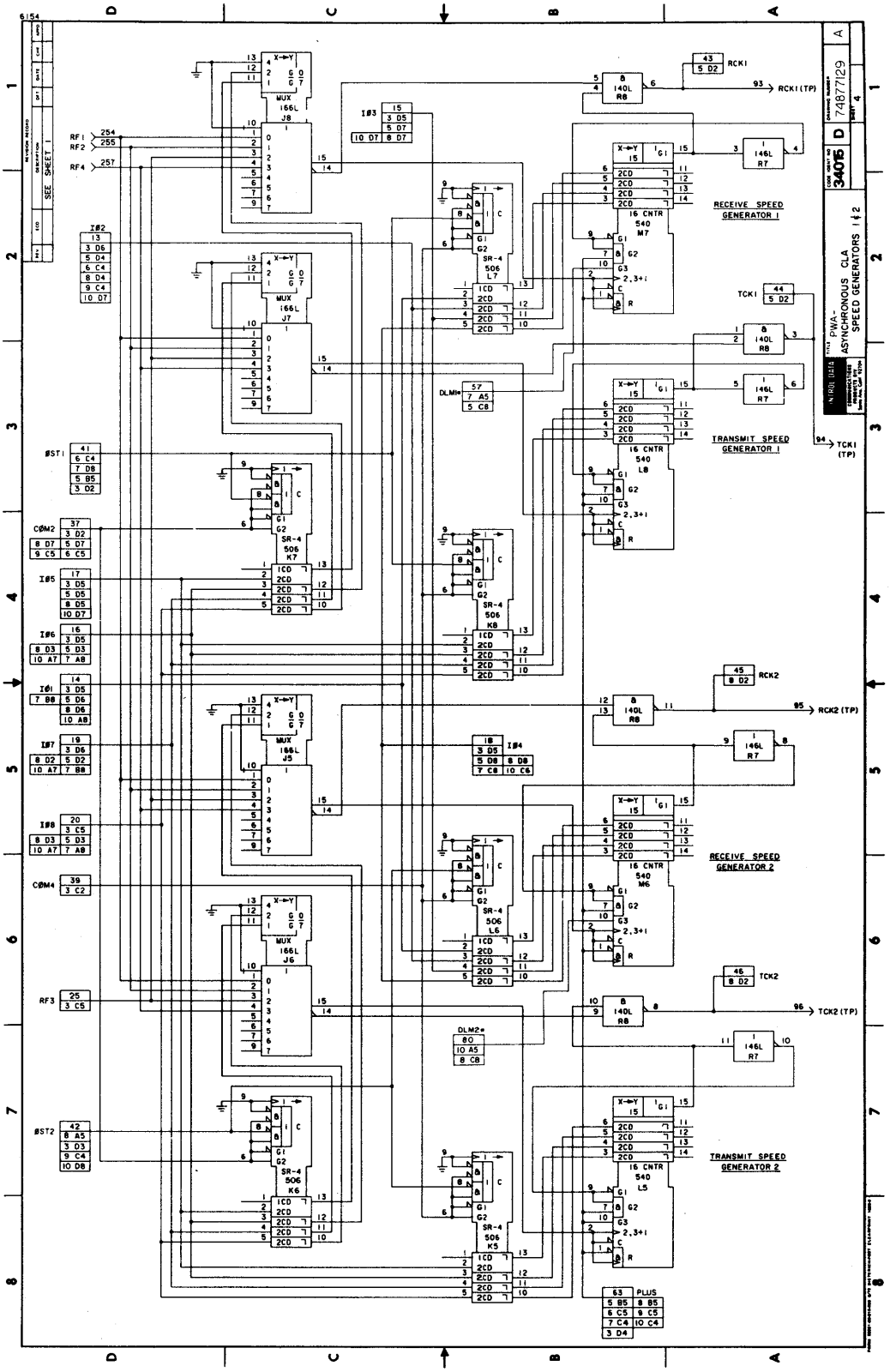
DATA ASSOCIATED STATUS

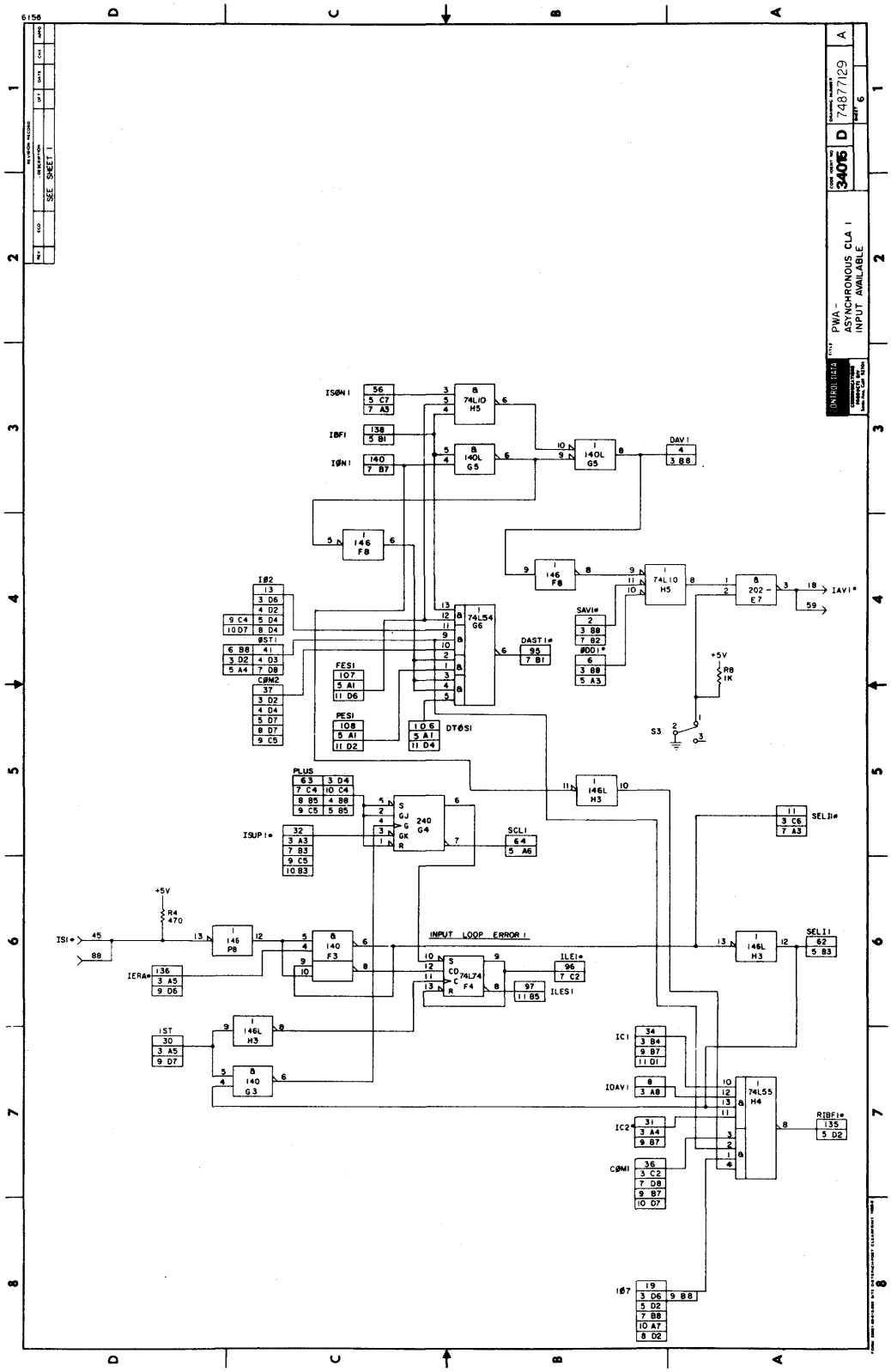
Data-associated-status* (DAST*) is produced by an A-O-I gate and may be activated by an input-data-error (parity or framing error or data-transfer-overrun) signal. FES, PES, and DTOS are applied to the A-O-I gate. If any one is logic 1, and IBF is logic 1, data-associated-status also goes to a logic 1. The remaining element of the A-O-I gate decodes the input-supervision-report command which causes data-associated-status to go to logic 1 if OST1, COM2 and IO2 are logic 1. The input-supervision-report command is a single-pulse signal.

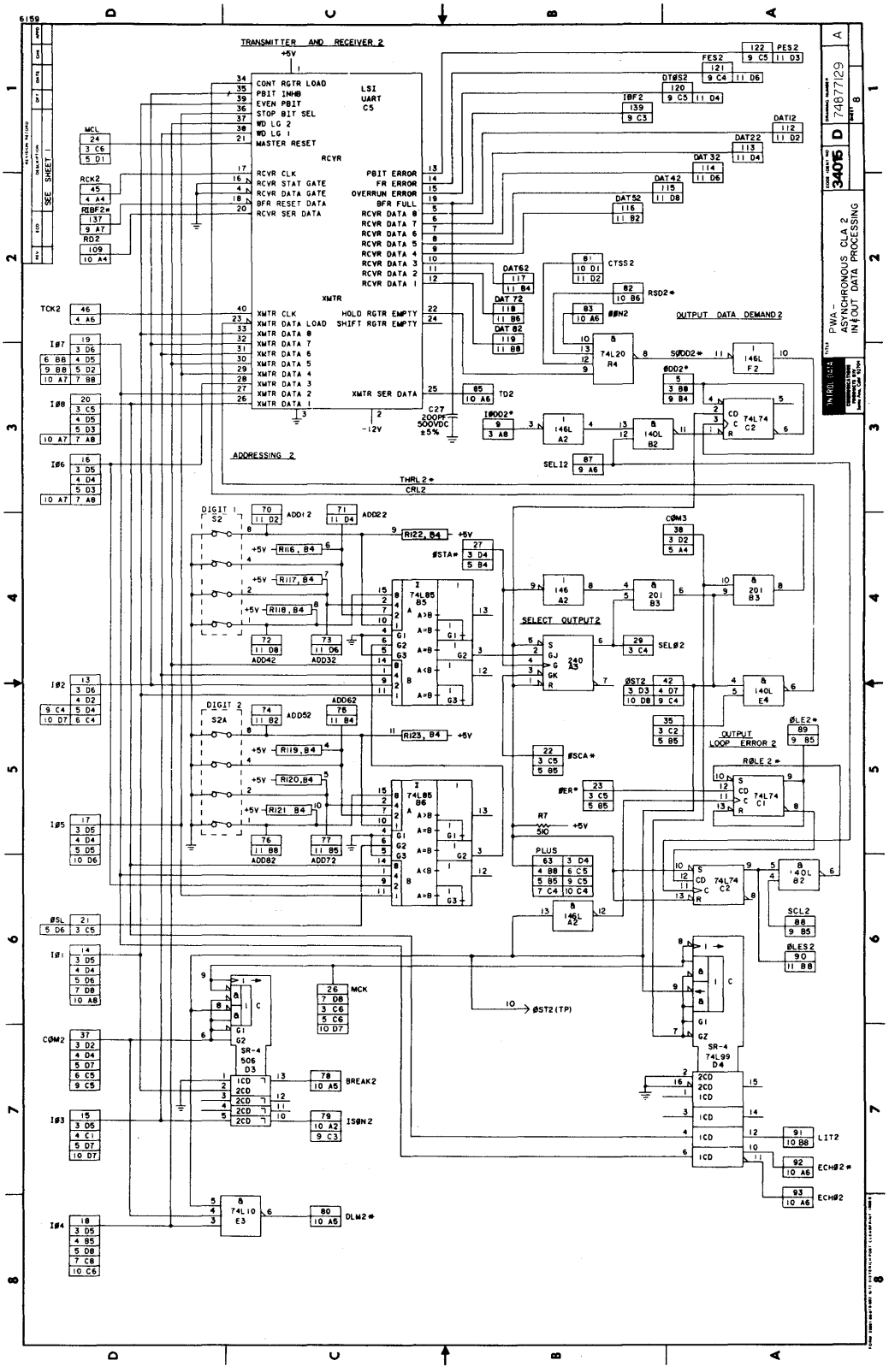
INDICATORS

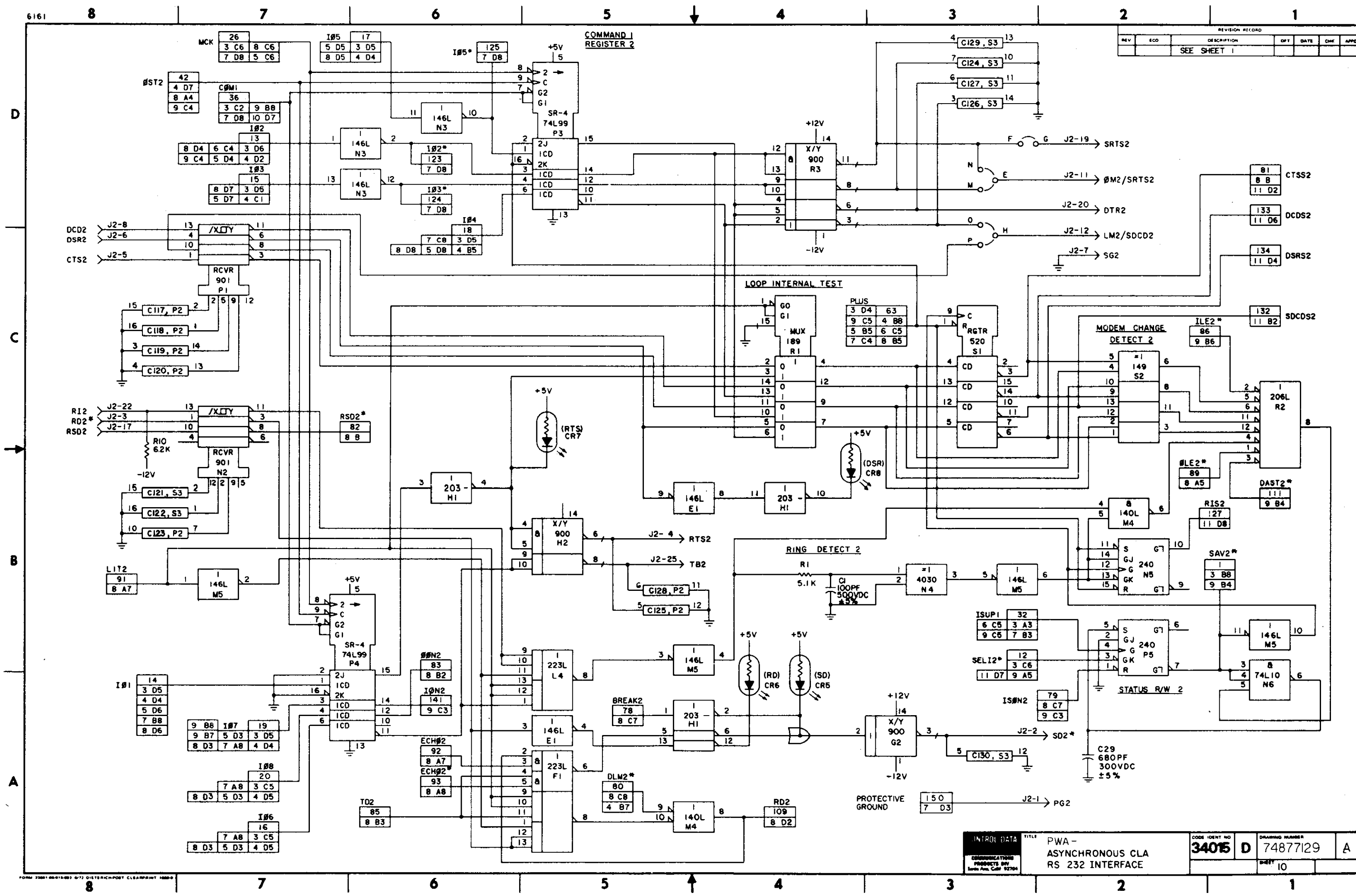
Light-emitting diodes are used to monitor the modem interface for the activity of the send-data, receive-data, request-to-send and data-set-ready. The indicators are activated with a logic 0, on, or spacing condition on their associated signals.


SEE SHEET 1
CR10 IN4002
+12VDC
+5VDC
GND
C4 1MF 100VDC ±5%
C5 10MF 15VDC ±10%
C8-C15, C17-C26, C31, C32
TP
C3 1MF 100VDC ± 5%
C7, C16
CR9 IN4002
CIRCUIT CARD ASSEMBLY
VIEWED FROM COMPONENT SIDE
PIN 201 COMPONENT SIDE
PIN 1 NON-COMP SIDE
PIN 302 COMPONENT SIDE
PIN 102 NON-COMP SIDE
PIN 251 COMPONENT SIDE
PIN 51 NON-COMP SIDE
PIN 252 COMPONENT SIDE
PIN 52 NON-COMP SIDE
NOTE: UNLESS OTHERWISE SPECIFIED
1. ALL RESISTOR VALUES ARE IN OHMS. 1/4 WATT ; ±5%
2. ALL CAPACITOR VALUES .01 MF
3. ALL INTEGRATED CIRCUIT PACKAGES HAVE STANDARD POWER PINS
14 PIN DUAL-IN-LINE 5VDC 14 GND 7
16 PIN DUAL-IN-LINE 5VDC 16 GND 8
4. NON-STANDARD POWER PINS ARE SHOWN ON THE LOGIC DIAGRAMS
PWA- ASYNCHRONOUS CLA — FULL RS232 / VARIABLE SPEED
D 34015
74877129 A
SCALE NONE
SHEET 2 OF 12


ASYNCHRONOUS CLA
SPEED GENERATORS 1 & 2
RECEIVE SPEED GENERATOR 1
TRANSMIT SPEED GENERATOR 1
RECEIVE SPEED GENERATOR 2
TRANSMIT SPEED GENERATOR 2
RCK1 (TP)
TCK1 (TP)
RCK2 (TP)
TCK2 (TP)
SEE SHEET 1

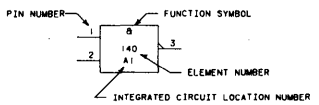

PWA - ASYNCHRONOUS CLA I INPUT AVAILABLE
3405
D
74887129
SHEET 6
SEE SHEET 1
ISØN1
IBF1
IØN1
74L10 H5
140L G5
DAV1
146 F8
74L10 H5
202 - E7
IAV1*
SAV1*
ØDO1*
74L54 G6
DAST1*
I Ø2
ØST1
CØM2
FES1
PES1
DTØS1
+5V
R8 1K
S3
PLUS
ISUP1*
240 G4
SCL1
146L H3
SEL3*
SEL1
INPUT LOOP ERROR1
+5V
R4 470
ISI*
IERA*
146 P8
140 F3
74L74 F4
ILE1*
ILES1
IST
140 G3
IC1
IOAV1
IC2
CØM1
74L55 H4
RIBF1*
IØ7


TRANSMITTER AND RECEIVER 2
LSI UART C5
RCVR
XMTR
ADDRESSING 2
OUTPUT DATA DEMAND 2
SELECT OUTPUT2
OUTPUT LOOP ERROR 2
PLUS
SR-4 506 D3
SR-4 74L99 D4
PWA - ASYNCHRONOUS CLA 2 IN&OUT DATA PROCESSING
74877129
34015

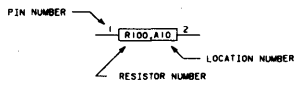

COMMAND I REGISTER 2
LOOP INTERNAL TEST
MODEM CHANGE DETECT 2
RING DETECT 2
STATUS R/W 2
PROTECTIVE GROUND
SEE SHEET 1
CONTROL DATA
PWA-
ASYNCHRONOUS CLA
RS 232 INTERFACE
34015
D
74877129
A
10

6650

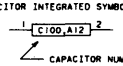
CIRCUIT ELEMENT SYMBOLOGY

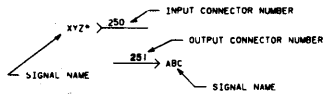


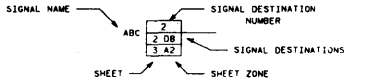
RESISTOR INTEGRATED SYMBOLOGY

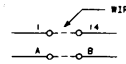


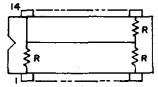
CAPACITOR INTEGRATED SYMBOLOGY



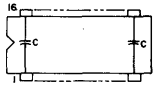








I.C. RESISTOR PACK
LOCATION U47,U48
10K



I.C. CAPACITOR PACK
LOCATION U25,U28,U41,U46
220PF

IDENTIFIER LIST

CDC ELEMENT IDENTIFIER	VENDOR TYPE NUMBER	FUNCTION
140	7400	TTL QUAD 2-INPUT NAND GATE
140L	74L00	TTL QUAD 2-INPUT NAND GATE
203	7405	TTL HEX INVERTER (OPEN COLLETOR)
141L	74L10	TTL TRIPLE 3-INPUT NAND GATE
146	7404	TTL HEX INVERTER
146L	74L04	TTL HEX INVERTER
—	74L54	TTL 4-WIDE 2 INPUT AND-OR-INVERTER
148L	74L02	TTL QUAD 2-INPUT NOR GATE
175	7474	TTL DUAL D-TYPE F/F
175L	74L74	TTL DUAL D-TYPE F/F
189	7487	MULTIPLEXER,TTL QUAD 2-INPUT GATE
201	7408	TTL QUAD 2-INPUT AND GATE
202	7403	TTL QUAD 2-INPUT NAND GATE
206L	74L30	TTL 8-INPUT NAND GATE
—	7486	TTL QUAD 2-INPUT EXCLUSIVE OR GATE
208L	74L20	TTL DUAL 4-INPUT NAND GATE
223L	74L51	TTL DUAL 2-WIDE 2-3 IN AND-OR-INVERTER
240	9024	TTL DUAL J-K F/F
166L	93LI2	MULTIPLEXER,TTL 8-INPUT GATE
519	74174	LATCH,TTL 6-BIT D-TYPE
520	74175	LATCH,TTL 4-BIT D-TYPE
524L	74L85	COMPARATOR, TTL 4-BIT MAGNITUDE
538	9321	DECODER, TTL DUAL (1 OF 4)
542	8214	MULTIPLEXER TTL DUAL 4-BIT TRISTATE
540	7463	COUNTER,TTL 4-BIT BINARY
900	MC1488	DRIVER,DTL TO RS-232C QUAD LINE
901	MC1489A	RECEIVER, RS-232C TO DTL QUAD LINE
506	7495A	REGISTER, TTL 4-BIT RIGHT/LEFT SHIFT
—	7425I	MULTIPLEXER, TTL 8-INPUT TRISTATE
—	74L99	REGISTER,TTL 4-BIT RIGHT/LEFT SHIFT
—	9L24	TTL DUAL J-K F/F
—	9300	REGISTER,TTL 4-BIT UNIVERSAL
—	4030	QUAD 2-INPUT EXCLUSIVE-OR GATE
—	74L55	TTL 2-WIDE 4-INPUT AND-OR-INVERTER

QUALIFYING FUNCTION SYMBOLS

SYMBOL	DESCRIPTION
&	AND ALL INPUTS ACTIVE
1	ONE OR MORE (OR) ANY INPUT ACTIVE
≥2	TWO OR MORE INPUTS ACTIVE
=1	ONLY ONE INPUT ACTIVE (EXCLUSIVE OR)
=	ALL INPUTS EQUAL
=2	ONLY TWO INPUTS ACTIVE, NO MORE, NO LESS
G	GENERATOR OR OSCILLATOR (WAVEFORM MAY BE ADDED)
⎍	SCHMITT TRIGGER
⎍⎍	ONE-SHOT MULTIVIBRATOR
⊢⊣	TIME DELAY
00	EVEN PARITY
000	ODD PARITY
X→Y	X INPUTS, DECODED OR ENCODED TO, Y OUTPUTS
X/Y	X INPUT LEVEL CONVERTED TO Y OUTPUT LEVEL
Σ	ARITHMETIC SUMMING CIRCUIT
F	COMPLEX FUNCTION

INPUT / OUTPUT DESIGNATORS

R	RESET
S	SET
G	GATING TYPE INPUT THAT OFFSETS OTHER INPUTS OR OUTPUTS
J	J INPUT OF J-K FLIP FLOP
K	K INPUT OF J-K FLIP FLOP
T	TOGGLE OR COMPLEMENT INPUT
D	DATA INPUT OF TYPE FLIP FLOP
C	GATING (CLOCK) INPUT FOR A "D" INPUT ONLY
L	USED ONLY WITH IN=1BIT INPUT; ALL LOW STATE OUTPUTS ARE INHIBITED
H	USED ONLY WITH IN=1BIT INPUT; ALL HIGH STATE OUTPUTS ARE INHIBITED
⊓	DELAY INDICATOR, FOR OUTPUT HAVING INPUT CONTROLLED DELAY
E	EXTENDER FOR EXPANDING THE NUMBER OF INPUTS
⊐	INDICATES GROUPED INPUTS THAT MAINTAIN FIXED RELATIONSHIP
⊏	INDICATES GROUPED OUTPUTS
→	SHIFT RIGHT (OR DOWN)
←	SHIFT LEFT (OR UP)
+1	INCREASE CONTENTS BY ONE (COUNT UP)
-1	DECREASE CONTENTS BY ONE (COUNT DOWN)
1, 2, 4, 8	INDICATES RELATIVE WEIGHTING OF INPUTS OR OUTPUTS IN CODES
A, B, C, ETC	INDIVIDUAL SIGNALS OR GROUPS OF SIGNALS WHEN TWO OR MORE

SIGNAL LINE INDICATORS.

◇8 OR ◇1	DOT-AND OR DOT-OR (WIRED AND, OR)
◺	POLARITY CONVENTION, NEGATIVE POTENTIAL
◸	DYNAMIC INPUT, TRANSITION FROM "0" STATE TO "1" STATE
—/—	NON-STANDARD LOGIC LEVEL
—⌇—	ANALOG OR NON-LOGIC LEVEL
—↗—	VARIABLE PARAMETER CONTROL
—∿—	IN=1BIT DESIGNATOR WITH POLARITY INDICATOR
—+—	IN=1BIT DESIGNATOR

FUNCTION ABBREVIATIONS

ALU	ARITHMETIC AND LOGIC UNIT
MCNTR	COUNTER, CHARACTER M IS MAX, NO. COUNTS (E.G. 10CNTR OR 16CNTR)
DCDR	DECODER AND/OR ENCODER
DRVR	DRIVER
MEM	MEMORY
MUX	MULTIPLEXER
RCVR	RECEIVER
RGTR	REGISTER
SRN-M	SHIFT REGISTER
DEMUX	DEMULTIPLEXER

REVISION RECORD

REV	ECO	DESCRIPTION	DRT	DATE	CHK	APPD
		SEE SHEET 1				

CONTROL DATA CORPORATION MINNEAPOLIS, MINN. Santa Ana, Calif. 92705	PWA - ASYNCHRONOUS CLA - FULL RS232/VARIABLE	34015	D	74877129 A
			SHEET 12	

TABLE 6-1. LOOP MULTIPLEXER-TO-ACLA INTERFACE SIGNALS

ACLA Pin No.	Signal Name	Mnemonic	Function	Signal To:
18/59†	Input Available ACLA1	IAV1	Notifies LM that ACLA1 has input	LM
19/58†	Input Available ACLA2	IAV2	Notifies LM that ACLA2 has input	LM
231	Input Error	IER	Notifies ACLA of error on last input frame	ACLA
232	Input End	IEN	Notifies LM that present information is last	LM
220 thru 222	Input Format Bits 1 thru 3	IF1 thru IF3	Informs LM of address, data, or supervision on information input bus	LM
45/88†	Input Select ACLA1	IS1	LM selects ACLA1 input	ACLA
46/87†	Input Select ACLA2	IS2	LM selects ACLA2 input	ACLA
234	Input Strobe	IST	LM notifies ACLA of access	ACLA
223 thru 230	Information Input Bits 1 thru 8	II1 thru II8	Information to LM (data, address, supervision)	LM
283	Output Select Clear	OSC	LM deselects ACLA output	ACLA
282	Output Select	OSL	LM presents ACLA address	ACLA
271 and 272	Output Format Cell Bits 2 and 3	OF2 and OF3	Informs ACLA of address, data, or supervision on information bus	ACLA
285	Output Strobe	OST	LM notifies ACLA of information present	ACLA
273 thru 280	Information Output Bits 1 thru 8	IO1 thru IO8	Information to ACLA (data, supervision, address)	ACLA
281	Output Error	OER	Notifies ACLA of errors in last frame	ACLA
249	Master Clear	MCL	Clears ACLA	ACLA
254	Ref Frequency 1	RF1	9.6 kHz Clock	ACLA
255	Ref Frequency 2	RF2	19.2 kHz Clock	ACLA
256	Ref Frequency 3	RF3	153.6 kHz Clock	ACLA
257	Ref Frequency 4	RF4	Special	ACLA

†Signals are available at two different pins depending on location of card in card cage.

6. Insert proven card into cage slot and firmly engage card into connector on cage backplane.

7. Connect ACLA modem cables to connectors on card handle.

8. Set each address switch to proper setting.

9. Set CLA1 and CLA2 toggle switches to enabled (on) position.

LED INDICATORS

The LED indicators on the ACLA card handle are lighted when the LM is inputting from and outputting to the ACLA. Observing these LEDs can readily indicate modem or system errors to the operator. A blinking RD indicator indicates that the ACLA is receiving data from the modem; when the SD indicator is blinking, it indicates that the ACLA is sending data to the modem; a lighted RTS indicator shows that request-to-send is active from the ACLA; and a lighted DSR indicator shows that data-set-ready from the modem is active.

Suspected power failure to the card may be monitored for +5 vdc at the card.

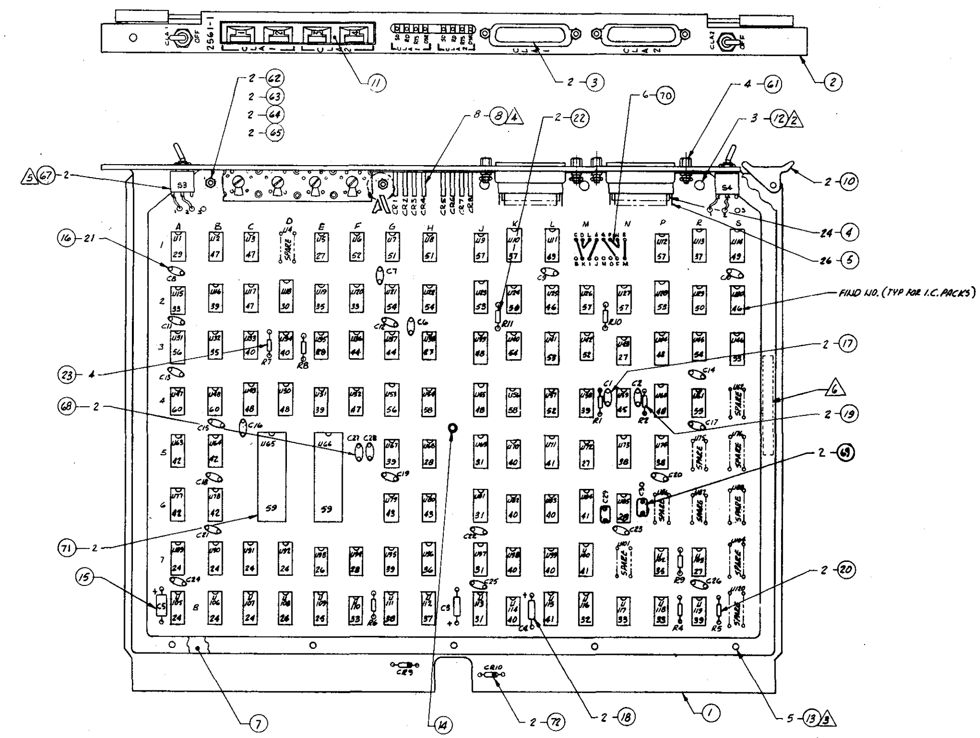
PREVENTIVE MAINTENANCE

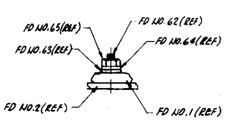
Preventive maintenance of the ACLAs is minimal. Excessive handling of cards may induce faults and is thus discouraged. However, the following should be performed at regular intervals:

1. Use spare cards periodically to ensure integrity of the spares.

2. Inspect connectors and cables for fraying or other damage.

3. When a card is removed, inspect connectors at card cage backplane for bent, damaged, or burned pins.





DETAIL A
SCALE 2/1

SHEET REVISION STATUS 3	2	1	REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
–	–	02	02		REVISED & REDRAWN		10-8-74		
–	–	03	03	05097	CL B PRERELEASE	ML	11-12-4		
–	–	04	04	05245	SEE ECO	DAW	12-31-74		
–	–	05	05	05496	SEE ECO	JTP	3-11-75		
–	–	06	06	05584	SEE ECO	LA	3-17-75		
–	–	07	07	05657	SEE ECO	JTP	4-14-75		
–	–	J	J	06337	SEE ECO	LA	5-11-76		
–	–	K	K	06406	SEE ECO	LA	6-16-76		
–	L	L	L	06471	SEE ECO	ELG	11-18-76		
–	L	M	M	06424	SEE ECO	G.D.	9-7-76		
–	N	N	N	08063	UP DATE FOR CBM	CT	11-29-77		
–	N	P	P	08192	REPLACE FIND 71	RD	2-16-78		
–	N	R	R	08181	REVISED PL ONLY	TP	2-23-78		
S	S	S	S	08208	ADDITIONAL REWORK ADDED	G.S.	4-19-78		
T	S	T	T	08246	REVISED PARTS LIST	RN	9-13-8	JK	VK
T	S	U	U	08736	INACTIVE : SUPERCEDED BY 74877129		9-26-79	JK	JK

NOTES:
1. WORKMANSHIP PER CDC-MFG SPEC 10120300
2. (△) INSERT RIVETS FROM COMPONENT SIDE
3. (△) INSERT RIVETS FROM NON-COMPONENT SIDE
4. (△) INDICATOR TO BE SEATED ON BOARD SURFACE DURING SOLDERING
5. (△) INSTALL FIND NO.67 SWITCH USING ONE INTERNAL TOOTH LOCK WASHER AND ONE NUT ON OUTSIDE OF HANDLE. APPLY LOCK-TITE (RTN 03044, 95125513) SPARINGLY TO SWITCH THREADS OF CAP TO PREVENT TURNING.
6. (△) STAMP PART NO. 74447001 AND TYPE NO. 5BBY PER CDC SPEC 10121505. LOCATE APPROX. AS SHOWN ON NON-COMPONENT SIDE.
7. WHEN ASSEMBLING CKT CARD USING 74872678 (RTN 34652) REV.04 CKT CARD FAB. SEE SHEET 2 & 3 FOR REWORK INSTRUCTIONS.

INACTIVE

5BBY

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.034.

PL 74447001 | DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS TOLERANCES
3 PLACE ±.015 ±0.38mm | 2 PLACE ±.03 ±0.8mm | ANGLES ±2°
DO NOT SCALE DRAWING
MATERIAL
FINISH

CONTROL DATA | COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

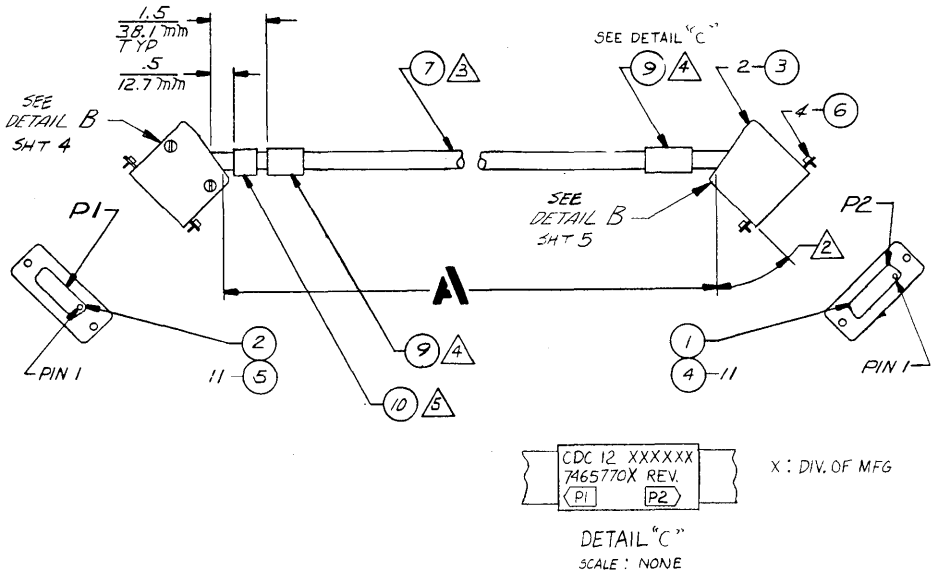
FIRST USED ON: DU137-A
DR: [signature] 10-8-74
CHK
ENGR
MFG
APPD

TITLE: CIRCUIT CARD ASSEMBLY ASYNCHRONOUS CLA-FULL RS232/VARIABLE SPEED

D | CODE IDENT NO 34015 | DRAWING NUMBER 74447001
SCALE 1/1 & NOTED | 32700-009-104 | SHEET 1 OF 3

FORM 5985-02-015-092 4/72 DIETERICH-POST CLEARPRINT 1020-8

CONTROL DATA CORPORATION	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 6	DOCUMENT NO. 74657700/03	REV. D



DETAIL "C"
SCALE : NONE

CONTROL DATA	MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 6	DOCUMENT NO. 74657700/03	REV. D

CDC NO.	LENGTH		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74657700	50.0	15.24	31770
74657701	100.0	30.48	38097
74657702	150.0	45.72	38098
74657703	200.0	60.96	38099

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
7465773J	C	CLA	A	CBL AY ASYNCH RS232 TO 103A 11	DM	2551	01/29/78	09/11/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP3		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP3		N
9	B	39296400	200	PC	LABEL, CABLE MARKING	IN	JJ8622	J82279	PPP4		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN			PPP4		N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
5	A	62013606	1100	PC	SOCKET	IN			PPP3		N
1	A	62J137J2	100	PC	CONN PIN HOUSING 25 PIN	IN			PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN			PPP3		N
7	A	74871633	6JJJJ	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	J08500		PPP4		N
10	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	J08500		PPP4		N
6	A	74873611	200	PC	RETAINER MALE SCREW	IN	JJ8622	J82279	PPP4		N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER: SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74657731	J	CLA	A	CBL AY ASYNC CLA TO 103A 100FT	DM	2551	07/23/78	09/11/79	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
13	C	24534706	100	IN	SLEEVING ELEC SHRINKABLE BULK	IN	008290	072678	PPP3		N
12	C	24548301	300	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN	008290	072678	PPP3		N
9	B	39296400	200	PC	LABEL, CABLE MARKING	IN	008622	082279	PPP4		N
3	A	51892202	200	PC	HOOD CONNECTOR	IN	008290	072678	PPP4		N
2	C	62013502	100	PC	CONN,SOCKET,HOUSING 25 PIN	IN	008290	072678	PPP4		N
5	A	62013606	1100	PC	SOCKET	IN	008290	072678	PPP3		N
1	A	62J137J2	100	PC	CONN PIN HOUSING 25 PIN	IN	008290	072678	PPP4		N
4	A	62013801	1100	PC	CONTACT PIN	IN	008290	072678	PPP3		N
7	A	74871633	12JJJJ	IN	CABLE 13 CONDUCTOR W OA SHIEL	IN	008290	072678	PPP4		N
10	A	74871674	1400	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	JJ8290	J72678	PPP4		N
6	A	74873611	200	PC	RETAINER MALE SCREW	IN	JJ8622	J82279	PPP4		N

NUMBER OF LINE ITEMS = 11
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER: SANTA ANA

AA 2709 REV. 7-75

Printed in U.S.A.

31771-009-070

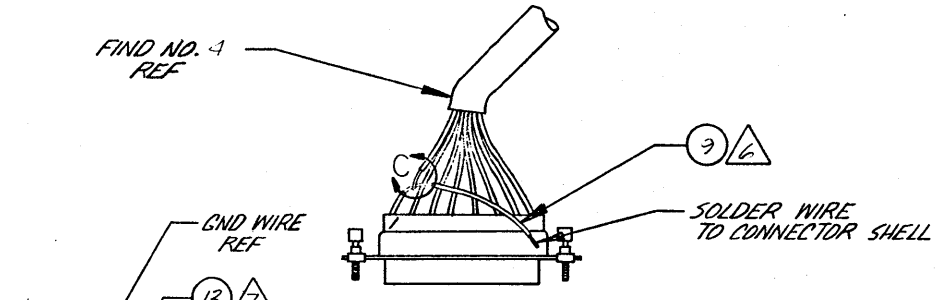
MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	DOCUMENT NO 74657900	REV D

CDC NO.	A LENGTH		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74657900	50.0	15.24	31771

FORM 19245-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31771-009-070

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	DOCUMENT NO. 74657900	REV. F



DETAIL B
CONN. HOOD OMITTED FOR CLARITY
SCALE : NONE

DETAIL C
SCALE: NONE

FORM 19245-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION

ASSEMBLY PARTS LIST

SPARE CODE
S = SPARE PARTS
N = NON SPARE PARTS

ASSEMBLY NUMBER	REV	CLASS	DW SZ	ASSEMBLY DESCRIPTION	DESIGN SOURCE	FIRST USAGE	RELEASE DATE	PROCESSING DATE	PAGE NUMBER
74657900	G	CLA	A	CBL AY ASYNC RS232 TO TERMINAL	DM	2551	01/29/78	01/29/78	1/ 1

MF

FIND NUMBER	DW SZ	PART NUMBER	QUANTITY	UNIT MEAS.	PART DESCRIPTION	IN/OUT STATUS	CHANGE ORD. NUMBER	DATE EFFECTIVE	MAKE/BUY PART TYPE	PN NC	S OR N
10	A	15003409	2.000	IN	WIRE ELECT,20 GA,PVC UL 1061	IN			PPP2		N
13	C	24534706	.100	IN	SLEEVING ELEC SHRINKABLE BULK	IN			PPP1		N
9	C	24548301	.100	IN	WIRE,ELECT,24 GA,PVC,UL,BLK	IN			PPP5		N
2	A	51892202	1.000	PC	HOOD CONNECTOR	IN					N
5		51904701	1.000	PC	CABLE LABLE	IN					N
1	C	62013502	1.000	PC	CONN,SOCKET,HOUSING 25 PIN	IN			PPP4		N
3	A	62013606	1.000	PC	SOCKET	IN					N
6	B	73995400	1.000	PC	NMPLT KIT BLNK SMALL CABLES	IN			PPP4		N
8	A	74658000	REF	PC	WIRE LIST ASYNC RS232 TO TERM	IN			RFE4		N
4	A	74871632	40.000	IN	CABLE 9 CONDUCTOR W OA SHIEL	IN	008500		PPP4		N
7	A	74871674	2.000	IN	TAPE 3/4 WIDE VINYL CLOTH BLU	IN	008500		PPP4		N
11	A	74873611	1.000	PC	RETAINER MALE SCREW	IN			PPP4		N
12	C	94288024	1.000	PC	CONNECTOR LOCKING DEVICE	IN			PPP4		N

NUMBER OF LINE ITEMS = 13
HIGHEST FIND NUMBER = 13

PROJECT ENGINEER ARDEN MILLS

AA 2708 REV. 7-75

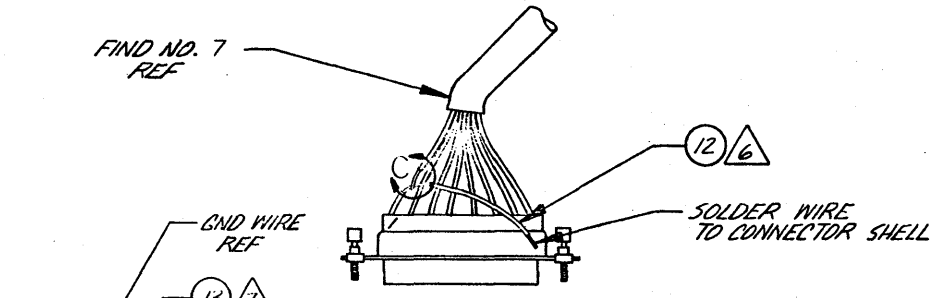
31773-009-070

MDM COMMUNICATIONS DIVISION Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	DOCUMENT NO. 74658300	REV. A

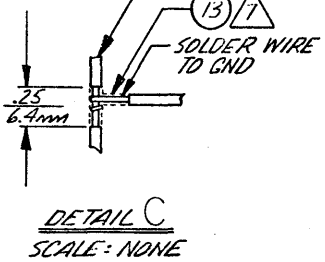
CDC NO.	LENGTH A		RTN NO.
	FEET ±0.5 FT	METERS ±.15 METERS	
74658300	50.0	15.24	31773

31773-009-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	DOCUMENT NO. 74658300	REV. A

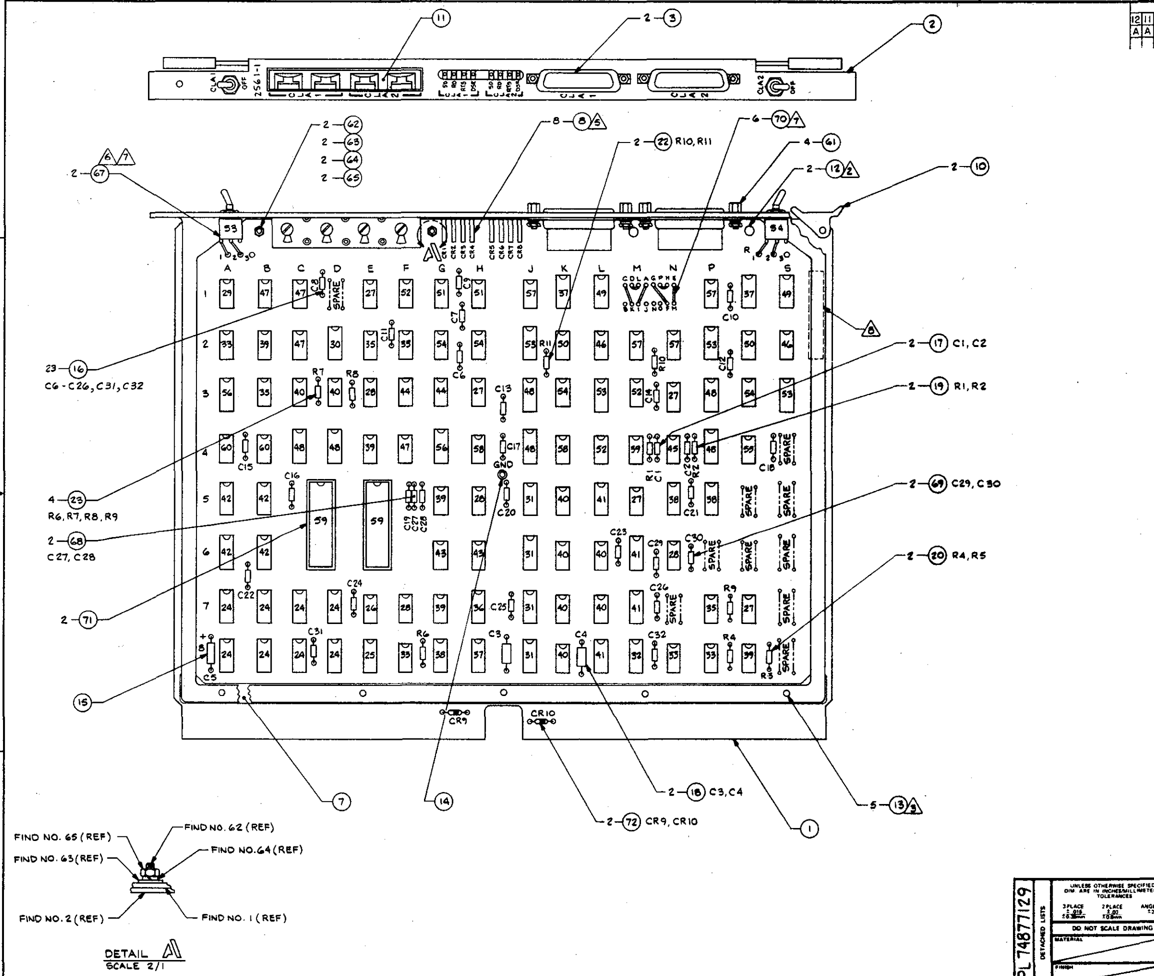


DETAIL B
CONN. HOOD OMITTED FOR CLARITY
SCALE : NONE



DETAIL C
SCALE: NONE

SHEET REVISION STATUS												REV	ECO	DESCRIPTION	OFF	DATE	CHK	APPD
12	11	10	9	8	7	6	5	4	3	2	1							
A	A	A	A	A	A	A	A	A	A	A	A	A	08786	CL. A REL	G.S	9/27/79		K



NOTES:

1. WORKMANSHIP PER CDC MFG SPEC 10120300.
2. △ INSERT RIVETS FROM COMPONENT SIDE.
3. △ INSERT RIVETS FROM NON-COMPONENT SIDE.
4. NUMBERS INSIDE IC OUTLINES ARE FIND NOS FROM P/L.
5. △ INDICATORS TO BE SEATED ON BOARD SURFACE DURING SOLDERING.
6. △ INSTALL SWITCH (FIND NO 67) USING ONE INTERNAL TOOTH LOCK WASHER AND ONE NUT ON OUTSIDE OF HANDLE. APPLY ONE DROP OF LOCKTITE CDC 95125313 TO THREADS OF CAP.
7. △ WIRE AS SHOWN USING FIND NO 70.
8. △ MARK PER CDC SPEC 10121508 PART NO 74877129 REVISION, DATE CODE, AND CARD TYPE CODE 9BBY LOCATE APPROX. AS SHOWN.
9. *REWORK INSTRUCTION FOR FAB. 74876907 ADD JUMPER FROM I.C. G4-2 TO G4-5 WITH FN 70.*

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

9BBY

PL 74877129

DETACHED LISTS

UNLESS OTHERWISE SPECIFIED DIM. ARE IN INCHES/MILLIMETERS
TOLERANCES
3 PLACE ±.015 ±0.38mm; 2 PLACE ±.03 ±0.8mm; ANGLES ±2°

DO NOT SCALE DRAWING

MATERIAL

FINISH

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704

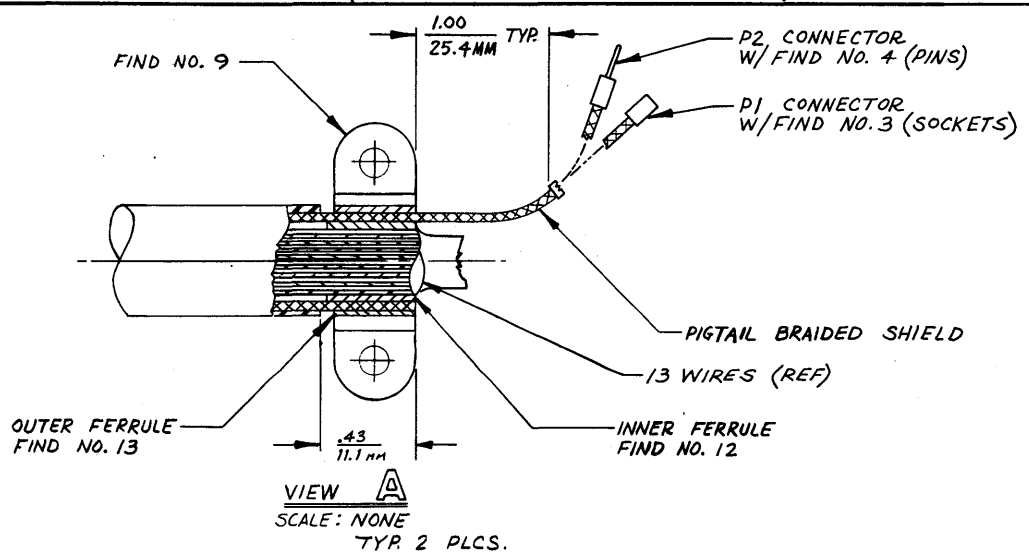
FIRST USED ON	DU137A	
DR	G. SWAFFORD	1-23-79
CHK	(signature)	6/7/79
ENGR	(signature)	6-7-79
MFG	(signature)	8-28-79
APPD	R.C. Gregory	9-26-79
	J. (signature)	9-79

TITLE: PWA - ASYNCHRONOUS CLA - FULL RS 232 / VARIABLE SPEED

SIZE: D — CODE IDENT NO: 34015 — DRAWING NUMBER: 74877129

SCALE 1/1 & NOTED — SHEET 1 OF 12

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	——	SEE SHEET 1	——	——		

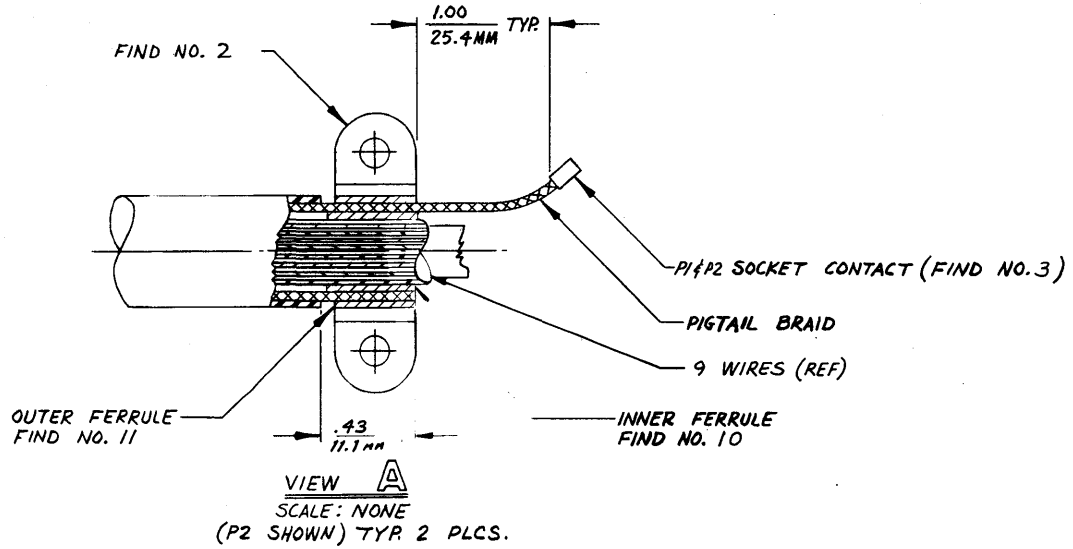


VIEW A
SCALE: NONE
TYP. 2 PLCS.

CONTROL DATA	TITLE	CODE IDENT NO.		DRAWING NUMBER	
COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CABLE ASSY- ASYNCHRONOUS RS 232 TO 103A/113	34015	C	74875756	A
		36947-009-070		SHEET 2 OF 2	

FORM 23580-00-015-092 6/72 DIETERICH-POST CLEARPRINT 1020-8

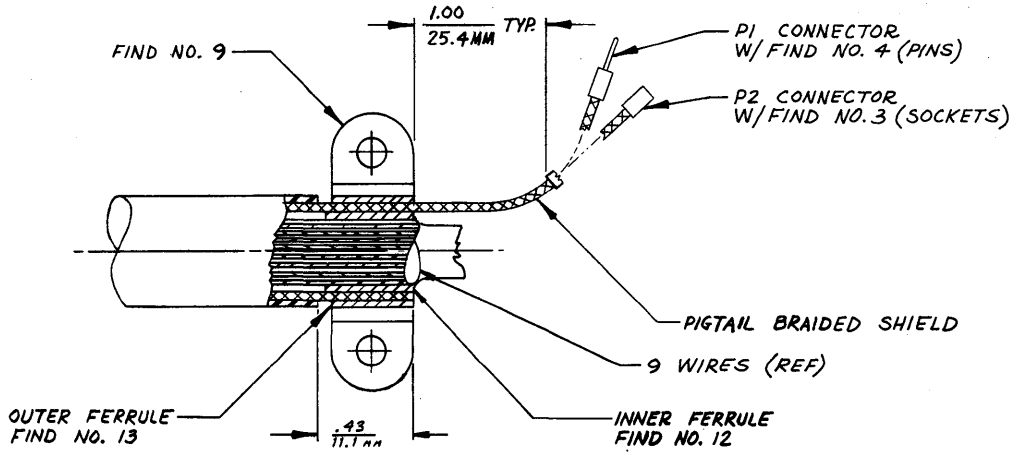
REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	———	SEE SHEET 1	—	———		



VIEW A
SCALE: NONE
(P2 SHOWN) TYP. 2 PLCS.

CONTROL DATA — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE: CABLE ASSY- ASYNCHRONOUS RS 232 TO TERMINAL	CODE IDENT NO. 34015	C	DRAWING NUMBER 74875846 A
		36949-009-070		SHEET 2 OF 2

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	—	SEE SHEET 1	—	—		

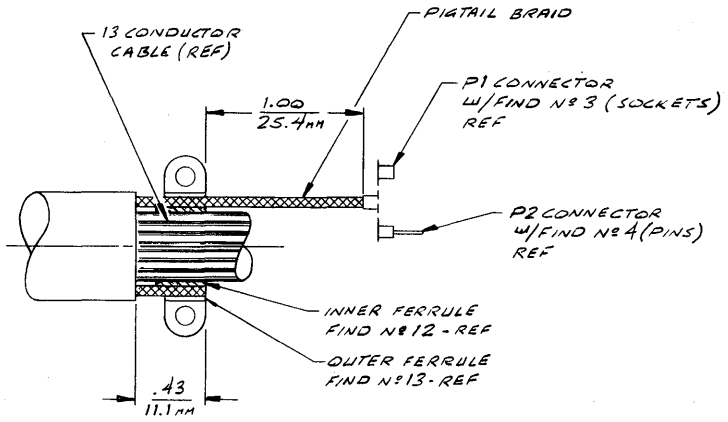


VIEW A
SCALE: NONE
TYP. 2 PLCS.

CONTROL DATA COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE CABLE ASSY- ASYNCHRONOUS RS 232 TO 103F MODEM	CODE IDENT NO. 34015	C	DRAWING NUMBER 74875760 A
		38007-009-070		SHEET 2 OF 2

FORM 23860-00-019-002 8/72 DIETERICH-POST CLEARPRINT 1020-B

REVISION RECORD						
REV	ECO	DESCRIPTION	DFT	DATE	CHK	APPD
—	———	SEE SHEET 1	AV	8.78		



DETAIL A
TWICE SIZE

CONTROL DATA COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	TITLE: CABLE ASSEMBLY ASYNCHRONOUS CLA TO 202S MODEM	CODE IDENT NO. 34015	C	DRAWING NUMBER 74876194 A
				SHEET 2 of 2

FORM 73560 00 015 092 6/72 DIETERICH POST CLEARPRINT 1020 B

35689-009-070

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 3 OF 4	SE	DOCUMENT NO. 74874002	REV. A

CDC Nº.	A LENGTH		RTN Nº.
	FEET ±0.5 FT	METERS ±.15 METERS	
74874002	50.0	15.24	35689

35689-009-070

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 4 OF 4	SE	DOCUMENT NO. 74874002	REV. A

NOTES:

1. WORKMANSHIP PER CDC SPEC 10120300
2. ANGLE OF CABLE EXITING CONNECTOR HOUSING TO BE 45°.
3. SHIELD IS TERMINATED TO THE CONNECTOR PIN 1.
4. MARK FIND NO. 9 PER CDC SPEC 10121508 WITH PART NO. 74874002, CONNECTOR NO. P1 OR P2, AND SERIAL NUMBER.

DWN	CRAWFORD	2-21-75	CONTROL DATA	TITLE CONNECTOR ASSY— ASYNC CLA LOOP EXTERNAL TEST CONNECTOR	PREFIX	DOCUMENT NO.	REV
CHKD					PL	74715600	00
ENG	LHC	2-21-75	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	FIRST USED ON			
MFG				32161-009-122		SHEET 1 OF 2	
APPR			CODE IDENT 34015				

SHEET REVISION STATUS

2	1
00	00

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	05515	CL B RELEASE		2-24-75	LHC

NOTES:

DETACHED LISTS

32161-009-122

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	PL	DOCUMENT NO 74715600	REV. 00

FIND NO	PART IDENTIFICATION	QUANTITY REQUIRED	UNIT OF MEAS		NOMENCLATURE OR DESCRIPTION	SPECIFICATIONS, NOTES, OR MATERIAL
1		1	FT		WIRE, 22GA	01435-002
2	7397700	1	PC		CONTACT, SOCKET	14198-002
3	73919803	1	EC		HOOD, CONNECTOR	26046-002
4	73954300	1	PC		LABEL	15486-002
5		1	PC		LABEL, SELF-ADHESIVE	01223-002
6	74394500	1	PC		CONNECTOR BLOCK-SOCKET	14196-002

DWN	LEVENTHAL	10/31/74	CONTROL DATA	TITLE CABLE ASSY - ASYNCHRONOUS RS232 TO 103A/113	PREFIX WL	DOCUMENT NO. 74657800	REV A
CHKD							
ENG	[signature]	11-5-74	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704	FIRST USED ON 31770-028-070		SHEET 1 OF 2	
MFG							
APPR			CODE IDENT 34015				

SHEET REVISION STATUS

2	1
00	00
01	01
01	02
A	A

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA
AAL030

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	PRELIM RELEASE	ML	10-31-74	
01	-	DELETED COND 9 & 10; RENUMBERED COND.; REV CABLE FO NOS	LA	1-3-75	
02	05360	CL B PRERELEASED	DDM	1-10-75	
A	08063	CLASS "A" RELEASE	TP	1-27-78	

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

31770-028-070

CONTROL DATA	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74657800	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	7	22	SHIELD WIRE		CONN P1	1	5	CONN P2	1	4	PROTECTIVE GND (AA)
2	↑	↑	BLK		↑	2	↑	↑	2	↑	TRANSMITTED DATA (BA)
3			BRN			3			3		RECEIVED DATA (BB)
4			RED			4			4		REQUEST TO SEND (CA)
5			ORN			5			5		CLEAR TO SEND (CB)
6			YEL			6			6		DATA SET READY (CC)
7			GRN			7			7		SIGNAL GND (AB)
8			BLU			8			8		RCVD LINE SIG DET (CF)
9			VIO			20			20		DATA TERM READY (CD)
10	↓	↓	GRY		↓	22	↓	↓	22	↓	RING INDICATOR (CE)
11	7	22	WHT		CONN P1	25	5	CONN P2	25	4	TERM BUSY (-)

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020

PRINTED IN U.S.A.

DWN	LEVENTHAL		CONTROL DATA	TITLE	PREFIX	DOCUMENT NO.	REV
CHKD				CABLE ASSY ASYNCHRONOUS RS232 TO 103F MODEM	WL	74658400	A
ENG	[illegible]	[illegible]	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG			CODE IDENT 34015	FIRST USED ON 31773-028-070		SHEET 1 OF 2	
APPR							

SHEET REVISION STATUS

2	1
00	00
01	01
02	02
02	03
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
00	-	PRELIM RELEASE	ML		
01	-	REV. IDENT NO. PER ECO REMARKS	DPM	12-12-74	
02	-	REV COLORS & CABLE PD NO; DELETE COND 10 & 12	LA	1-8-75	
03	05360	CL B PRERELEASE	DPM	1-10-75	
A	08063	CLASS A RELEASE CBM	TP	1-20-75	

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
CA

AA6030

NOTES:

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

31773-028-070

CONTROL DATA CORPORATION	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704	CODE IDENT 34015	SHEET 2 OF 2	WL	DOCUMENT NO. 74658400	REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	7	22	SHIELD WIRE		CONN P1	1	5	CONN P2	1	4	PROTECTIVE GND (AA)
2	"	"	BLK		"	2	"	"	2	"	TRANSMITTED DATA (BA)
3			BRN			3			3		RCVD DATA (BB)
4			RED			4			4		REQUEST TO SEND (CA)
5			ORN			5			5		CLEAR TO SEND (CB)
6			YEL			6			6		DATA SET READY (CC)
7			GRN			7			7		SIGNAL GND (AB)
8			BLU			8			8		RCVD LINE SIGNAL DET (CF)
9	"	"	VIO		"	11	"	"	11	"	ORIGINATE MODE
10	7	22	GRY		CONN P1	20	5	CONN P2	20	4	DATA TERM. READY (CD)

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	ECKHOLDT	3/16/78	CONTROL DATA	TITLE CABLE ASSY – ASYNCHRONOUS RS 232 TO 103A/113	PREFIX WL	DOCUMENT NO. 74875756	REV A
CHKD	ECH	3/16/78	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
ENG	[illegible]	[illegible]					
MFG	R. Frederick	[illegible]	CODE IDENT 34015	FIRST USED ON YA228-A		SHEET 1 OF 2	
APPR	J. Ramos	10-78					

SHEET REVISION STATUS

2	1
01	01
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	008457	CLASS B RELEASE	AV	6-78	VK
A	8648	REMOVED CL "C" PARTS	TD	4-79	VK

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.
TD
AA6030

NOTES: ⚠1 CUT OFF REMAINING WIRES FROM CABLE (FIND NO. 8) THAT ARE NOT USED.

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

CONTROL DATA CORPORATION — COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704 — CODE IDENT 34015 — SHEET 2 OF 2 — WL — DOCUMENT NO. 74875756 — REV A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	8	24	SHIELD WIRE		CONN P1	1	3	CONN P2	1	4	PROTECTIVE GND (AA)
2	↑	↑	BLK		↑	2	↑	↑	2	↑	TRANSMITTED DATA (BA)
3	↑	↑	BRN		↑	3	↑	↑	3	↑	RECEIVED DATA (BB)
4	↑	↑	RED		↑	4	↑	↑	4	↑	REQUEST TO SEND (CA)
5	↑	↑	ORN		↑	5	↑	↑	5	↑	CLEAR TO SEND (CB)
6	↑	↑	YEL		↑	6	↑	↑	6	↑	DATA SET READY (CC)
7	↑	↑	GRN		↑	7	↑	↑	7	↑	SIGNAL GND (AB)
8	↑	↑	BLU		↑	8	↑	↑	8	↑	RCVD LINE SIG DET (CF)
9	↑	↑	VIO		↑	20	↑	↑	20	↑	DATA TERM READY (CD)
10	↑	↑	GRY		↑	22	↑	↑	22	↑	RING INDICATOR (CE)
11	8	24	WHT		CONN P1	25	3	CONN P2	25	4	TERM BUSY (-)
12	8	24	W/BLK		——	—	—	——	—	—	⚠
13	8	24	W/BRN		——	—	—	——	—	—	⚠
14	8	24	W/RED		——	—	—	——	—	—	⚠

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

DWN	ECKHOLDT	3/15/78	CONTROL DATA	TITLE CABLE ASSY- ASYNCHRONOUS RS-232 TO 103F MODEM	PREFIX WL	DOCUMENT NO. 74875760	REV A
CHKD	[illegible]	3/15/78					
ENG	[illegible]	4/78	COMMUNICATIONS PRODUCTS DIV. Santa Ana, Ca. 92704				
MFG	R. Friedrich	10-4-78					
APPR	J. Kamp	10-78	CODE IDENT 34015	FIRST USED ON YA 229-A		SHEET 1 OF 2	

SHEET REVISION STATUS

2	1
01	01
A	A

REVISION RECORD

REV	ECO	DESCRIPTION	DRFT	DATE	APP
01	008457	CLASS B RELEASE	AV	8-78	JK
A	8648	REMOVED CL "C" PARTS	TD	9 APR 79	JK

NOTES:

INTER-DIVISIONAL DOCUMENT
Changes to this document require approval of all Using Divisions per CDC-STD 1.01.024.

AA6030

DETACHED LISTS

FORM 19246-01-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

COMMUNICATIONS PRODUCTS DIV. Santa Ana, Calif. 92704 | CODE IDENT 34015 | SHEET 2 OF 2 | WL | DOCUMENT NO. 74875760 | REV. A

CONDUCTOR IDENT.	FIND NO.	GAUGE (REF)	COLOR (REF)	LENGTH (APPROX)	ORIGIN	PIN	ACCESS FIND NO.	DESTINATION	PIN	ACCESS FIND NO.	REMARKS
1	8	24	SHIELD WIRE		CONN P1	1	3	CONN P2	1	4	PROTECTIVE GND (AA)
2	↑	↑	BLK		↑	2	↑	↑	2	↑	TRANSMITTED DATA (BA)
3	↑	↑	BRN		↑	3	↑	↑	3	↑	RECEIVED DATA (BB)
4	↑	↑	RED		↑	4	↑	↑	4	↑	REQUEST TO SEND (CA)
5	↑	↑	ORN		↑	5	↑	↑	5	↑	CLEAR TO SEND (CB)
6	↑	↑	YEL		↑	6	↑	↑	6	↑	DATA SET READY (CC)
7	↑	↑	GRN		↑	7	↑	↑	7	↑	SIGNAL GND (AB)
8	↑	↑	BLU		↑	8	↑	↑	8	↑	RCVD LINE SIGNAL DET (CF)
9	↓	↓	VIO		↓	11	↓	↓	11	↓	ORIGINATE MODE
10	8	24	GRY		CONN P1	20	3	CONN P2	20	4	DATA TERM. READY (CD)

FORM 23562-00-015-092 DIETERICH-POST CLEARPRINT 1020 PRINTED IN U.S.A.

OON	Output on
OSC	Output select clear
OSL	Output select
OST	Output strobe
OSUP	Output supervision
PES	Parity error status
PI	Parity inhibit
PSET	Parity set
RCK	Receive clock
RD	Receive data
RF	Reference frequency
RHR	Receive holding register
RI	Ring indicator
RIBF	Reset input buffer full
RIS	Ring indicator status
RLSD	Receive line signal detector
RODD	Reset output data demand
RSD	Restraint detector
RSR	Receive shift register
RTS	Request to send
R/W	Read/write
SAV	Status available
SB	Stop bit
SCL	Status clear
SCLA	Synchronous communications line adapter
SD	Send data
SDCD	Secondary data carrier detector
SDCDS	Secondary data carrier detector status
SELI	Select input
SELO	Select output
SODD	Set output data demand
SRLSD	Secondary receive line signal detector
SRTS	Secondary request to send
TB	Terminal busy
TCK	Transmit clock
TD	Transmit data
THR	Transmitter holding register
THRE	Transmitter holding register empty
THRL	Transmitter holding register load
TSR	Transmitter shift register
TTL	Transistor-transistor logic
UART	Universal asynchronous receiver-transmitter

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